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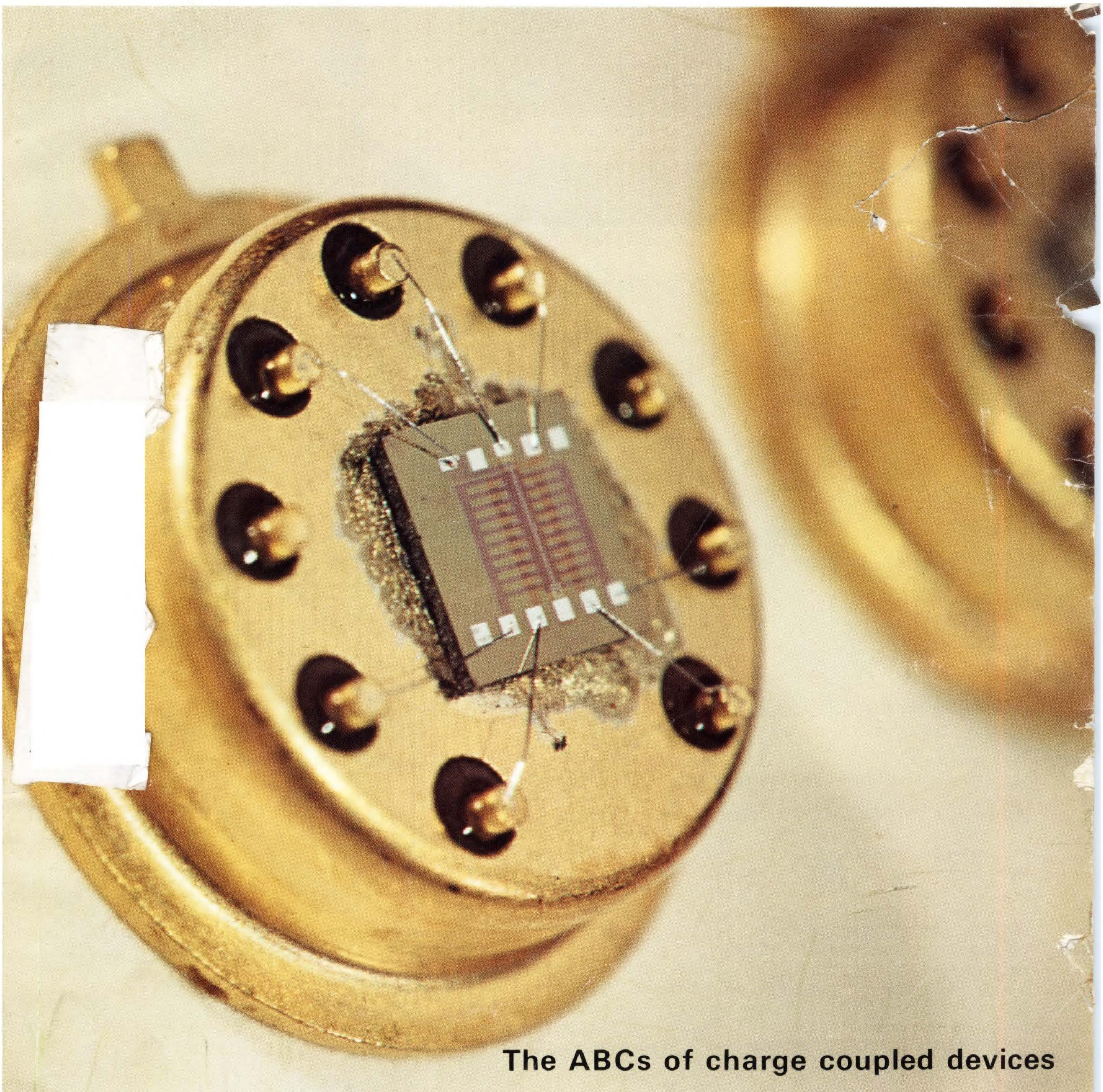

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JANUARY 20, 1973

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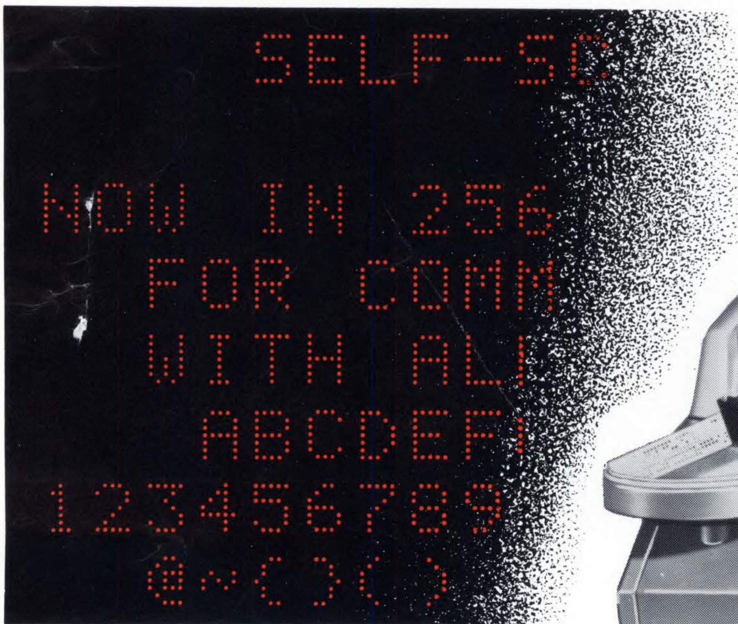

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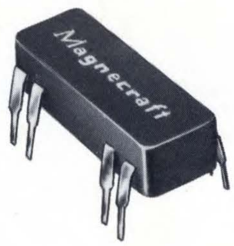

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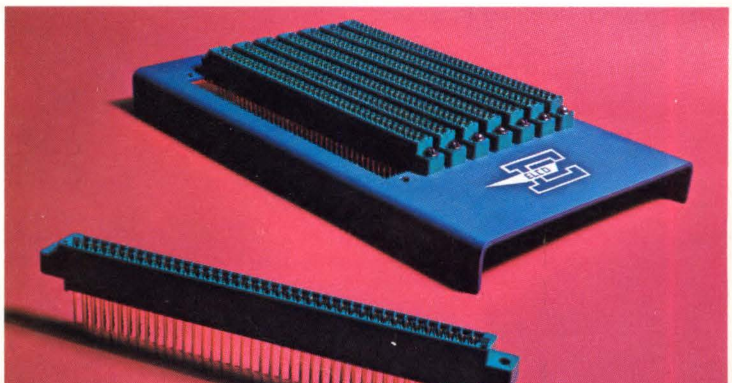

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EDN with EEE
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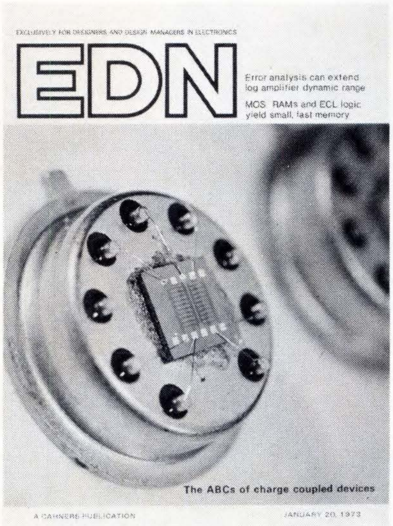

COVER

Overlapping gates propagate charge along channel from input to output p-n junction. Illustrated device is used to research basic CCD phenomena. Applications for CCDs lie in areas of high density memory, delay lines, and imaging devices. Cover photo supplied by North American Rockwell Corp. See pg. 34.

DESIGN NEWS

DESIGN FEATURES

PROGRESS IN PRODUCTS

DESIGN PRODUCTS

DESIGN DEPARTMENTS

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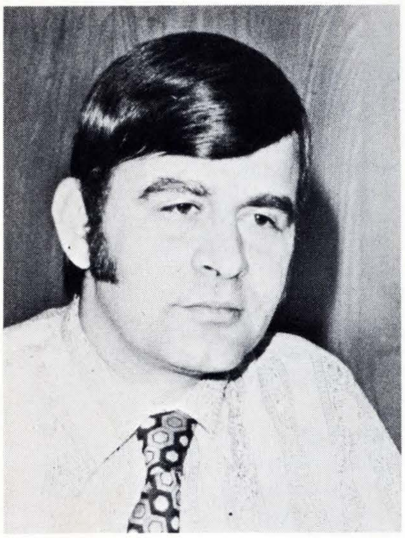

Should we wake the sleeping giant?

A couple of months ago I was invited for a ride in an experimental safety vehicle. The first thing I noticed was that as the transmission was engaged, all of the doors automatically locked. This gave me an uneasy feeling. It has never happened to me, but I can easily envision circumstances under which I would prefer to bail out of a moving vehicle (like rolling toward a cliff with defective brakes or to escape a fire). Unlike the pilot of an aircraft, apparently we of the motoring public will no longer have ultimate control over our vehicles, and that bothers me.

The larger symbolism of being locked into that car didn't strike me, however, until recently. Will the electronics industry become locked inescapably into the automotive industry?

The electronic calculator came at a time when we all needed a shot in the arm, and I'm glad it did. But have you checked delivery times on LED or gas discharge displays lately? Do you realize that more than half of the MOS-IC production of this country is tied up in calculators?

It was estimated that if all of the proposed "safety" controls for 1975 models were implemented electronically, it would cost buyers about $700 per car. Each of us will be paying that much more for our cars. What will that mean to the electronics industry? $100 per car? 200? If '75 is a 10 megacar year, that's $1 to $2 billion to our industry. Substantial to say the least, but is it desirable?

Surely there are problems more worthy of our design efforts than locking our families in cars, buzzing alarms at our wives when they put groceries on the seat without belting them in and blowing our children through the rear window with an idiot airbag!

Within the guidelines they were given, Detroit's engineers have done a fine job. How long has it been since you delivered a 4000 pound mobile system of similar complexity for $4000? Yet we insist on trying to install 25 custom ICs, 38 LEDs and a radar in each car.

Let's stop this silly courting of the auto industry before they take us up on it. They have some problems that we could probably be of considerable assistance with, like cleaner exhaust emissions and anti-skid sensors. Let's put the responsibility for safety squarely on the driver. Let's forget the frills that are unwanted and will only be circumvented anyway. And let's not tie up our production facilities to the point that it will take 2 years to get an op amp or a TTL gate.

The automotive market could be a shot in the arm for our industry, but shots are commonly given somewhere else, too.

Bill Furlow

Bill Furlow
Associate Editor

STAFF

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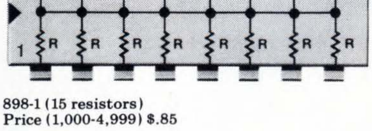

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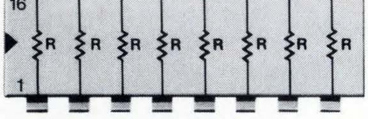

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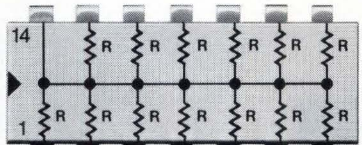
62*	110	330	1.0K	2.2K	6.0K	15.0K
68	150	470	1.5K	3.3K	6.8K	22.0K
100	220	680	2.0K†	4.7K	10.0K	

*Standard in 898-3 only.
†Standard in 898-1 only.



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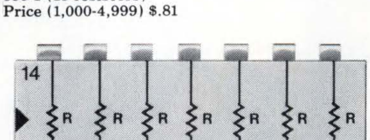

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STANDARD RESISTANCE VALUES
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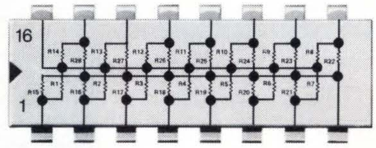
22	62	180	510	1.5K	4.3K	11K
24	68	200	560	1.6K	4.7K	12K
27	75	220	620	1.8K	5.1K	13K
30	82	240	680	2.0K	5.6K	15K
33	91	270	750	2.2K	6.0K	16K
36	100	300	820	2.4K	6.2K	18K
39	110	330	910	2.7K	6.8K	20K
43	120	360	1.0K	3.0K	7.5K	22K
47	130	390	1.1K	3.3K	8.2K	
51	150	430	1.2K	3.6K	9.1K	
56	160	470	1.3K	3.9K	10K	



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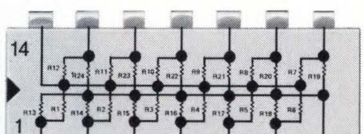

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Pulse squaring TTL terminator.
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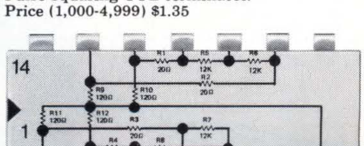

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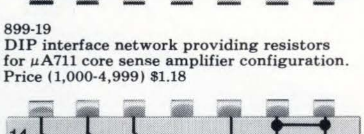

899-40
DIP network provides six line terminators and the threshold setting divider for the Intel 3208A sense amplifier.
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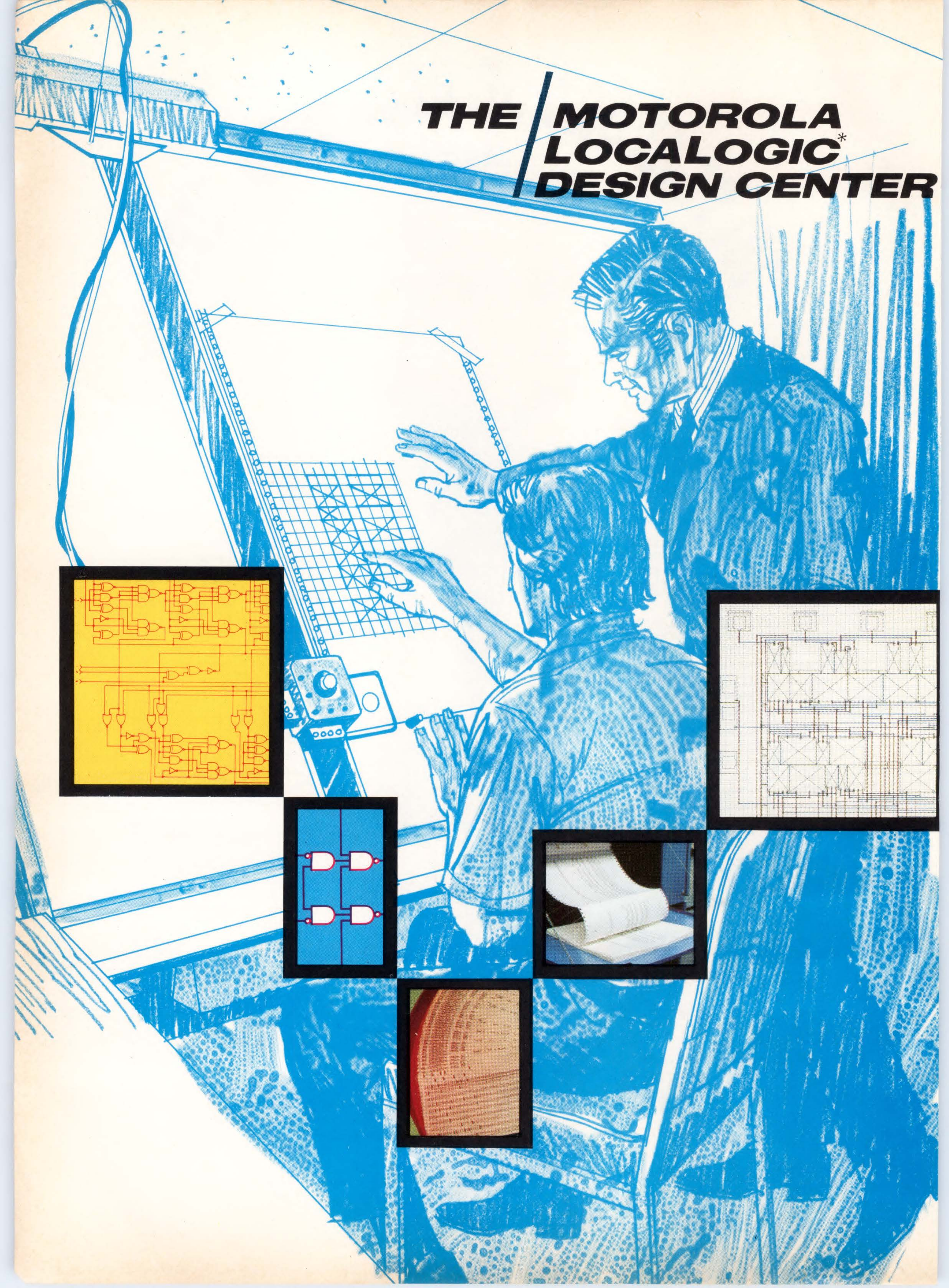
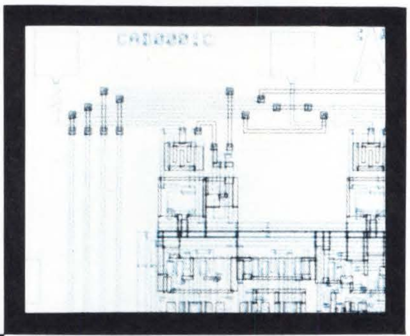
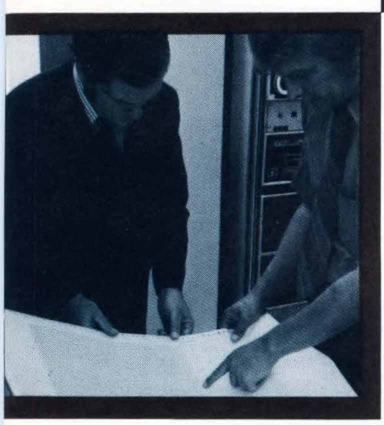
CHECK NO. 8

THE MOTOROLA LOCALOGIC* DESIGN CENTER



A New Concept in LSI Circuit Design





With the opening of the first LocaLogic Design Center in the Boston area, Motorola has brought complete LSI design capability into the field under the direct control of customer engineers. The Design Center utilizes the Polycell system . . . industry's most practical approach for designing custom LSI. The techniques are designed for use by customer (systems) designers. In this system, Polycells (proven, completely characterized logic cells, each comprised of several interconnected components) are handled as units on the computer as standard building blocks.

At the Center you are assigned an office as a base of operation during the course of your program. If you are new to the Polycell system, the Motorola design staff conducts a training program and once a design is started, the staff can help with any step in the sequence. Experience proves that, after brief familiarization, a logician or circuit designer with no prior background in semiconductor design or processing can very effectively use the system.

The LocaLogic Design Center is a completely self-contained operation covering the design stages between original logic definition and mask artwork generation.

Custom LSI approaches are the answer to increased system performance and lower costs. Now these custom designs can be accomplished by designers working close to their own facilities; quickly, easily, economically, with utmost design security. For complete details write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

The Boston facility is the forerunner of design centers to be located throughout the United States and Free World. Investigate this new tool and make LocaLogic a part of your design team.

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MOTOROLA LOCALOGIC

—the new concept in LSI design

CHECK NO. 9

Totally implantable heart depends heavily on electronics for timing and control

Heart disease is the number one cause of death in the U.S. and around the world. Of the more than 1,000,000 cardiovascular deaths that occur yearly, over 500,000 are directly related to the heart.

While prevention of heart disease is the ultimate medical goal, the immediate goal of researchers is the development of an artificial heart. Such a totally implantable artificial heart has been designed by Dr. Lowell T. Harmison, Chief of the National Heart and Lung Institute. Hardware has been developed by the Institute and tested extensively in animals. A version of this design may be ready for implantation in human patients as early as 1975.

The totally implantable heart consists of a left and right heart, an energy converter, a heart control computer, an energy storage pack and an energy recovery unit. The artificial heart (similar to the natural heart) is a four chambered pump having two atria with two large valves forming the inflow to the ventricles, tricuspid and pulmonary valves.

The heart is designed to satisfy the physiologic demands of the body for proper blood circulation. At any given time, the artificial heart will pump all of the blood returned to it. It must pump any given venous return without demanding more than is available at normal venous pressure into the pulmonary artery and aorta.

All timing and control for the implantable heart originate in the heart control computer. Stanford Research Institute and Statham Instruments have simultaneously developed two approaches to the design of this computer: one analog; the other digital. Both computers control the motor speed of the heart according to an algorithm proposed by Dr. Harmison which determines whether the heart is full or partially full or whether the left atrium is filled or partially filled. The computer then makes a decision to speed up, slow down or

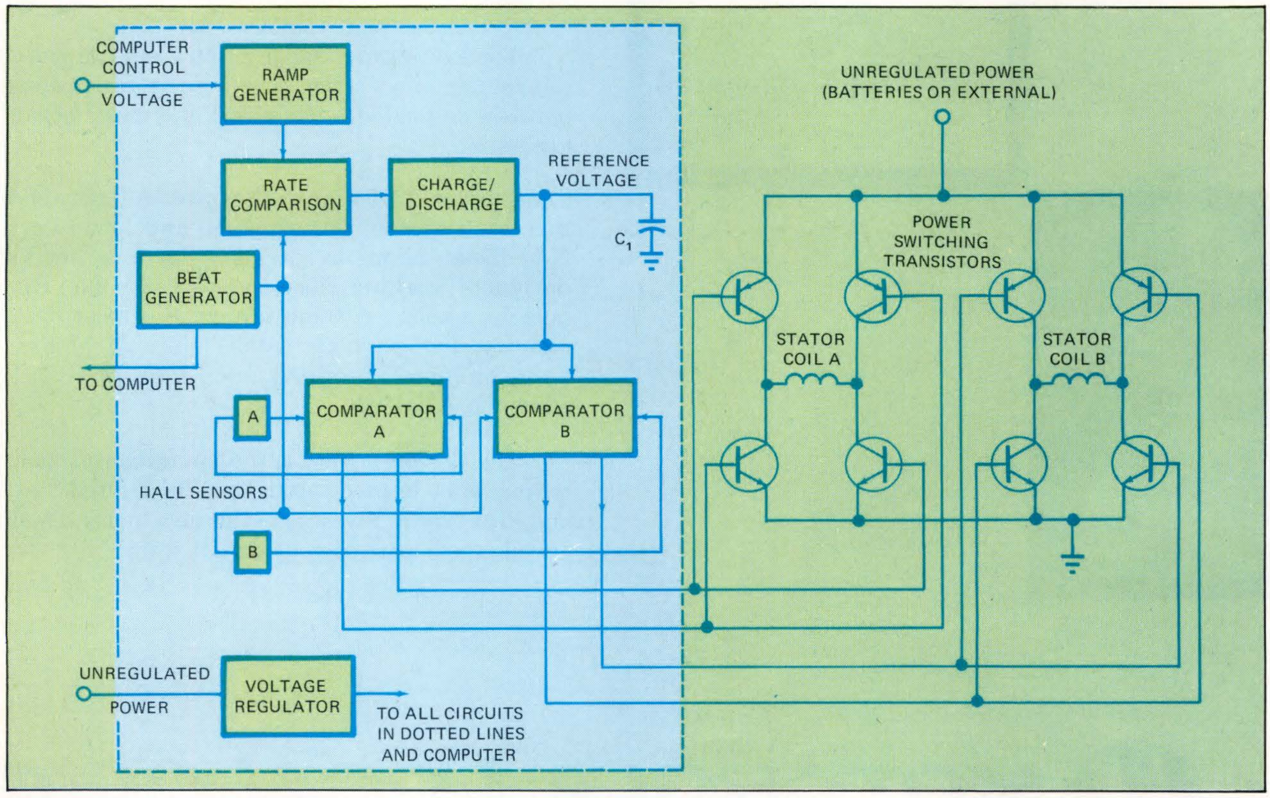


Fig. 1—Brushless motor control circuit of implantable heart is controlled by the heart control computer.

maintain the present heart rate. The artificial heart gets this information from a solid-state strain gauge activated in the last 5 percent of the atrium chamber displacement.

The computer continuously monitors beat rate and stroke volume, performing an analysis every five heart beats as follows:

If either the left or right ventricle has taken five full strokes, the computer will increase the heart rate by five beats per minute and automatically sample the next five.

If the left ventricle has taken three or four full strokes and the right ventricle no more than four full strokes, the computer will signal to hold the heart rate constant for the next five or ten seconds.

If the left ventricle has taken one or less strokes and the right ventricle no more than three full strokes, the computer signals the heart to decrease its heart rate by five beats per minute and hold for five or ten seconds.

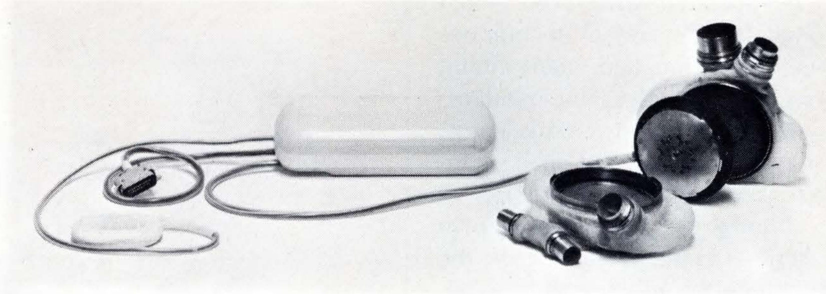
If the left ventricle has taken three or less full strokes and the right ventricle four or five full strokes, the computer increases the rate by five beats per minute.

The analog approach to designing the control computer, when fully refined, may require less power than the digital approach. However, the analog design requires a large number of capacitors to perform the required sample-and-hold functions. These capacitors not only take up space, they also have a tendency to fail. Also, with present integrated circuit technology, they cannot be incorporated on a chip.

With the digital approach, on the other hand, the entire computer can be fabricated on one or two chips. Nearly all timing can be performed by a timing capacitor operating a common clock.

The only real disadvantage to the digital system is that any small, single failure would cause a more catastrophic effect than with the analog computer. In either type of computer though, redundancy will be used to increase reliability.

Stanford Research Institute, designer of the analog computer, uses low-power operational amplifiers (HA2705) made by Harris Semiconductor, Inc., to reduce power dissipation to a minimum. They hope to try the Fairchild μA776. Statham Instruments, designer of the digital computer, uses CMOS devices from RCA's 4000 Series. The CMOS technology produces low power dissipation and substantial size reduction.—*JM*



The first totally implantable artificial heart system includes a heart control computer, energy conversion system and blood pump motor. The computer is housed in an implantable battery pack (center). No wires pierce the patient's skin. Batteries are recharged from a wall plug or battery pack outside the patient's body by means of an implantable pick-up coil (left).

Technique uses LSI to speed addition and multiplication in computers

An experimental technique for addition and multiplication in computer systems provides a good example of how Large Scale Integration can be used to advantage. Developed by IBM, the new technique results in faster operation at an attractive cost/performance level thanks to the present economics and availability of LSI.

Traditionally, the "carry save" adders used in today's computers are designed to add a maximum of three rows of numbers at a time instead of adding long columns. The new technique reduces the number of addition cycles by breaking the horizontal rows of numbers into vertical partitions of numbers several columns wide, and adding columns from different partitions simultaneously. The partial sums and carries of these columns are entered in the registers of a conventional "carry look ahead" adder for the final cycle, which completes the addition. With this technique, the optimum number of columns/partition (m) is determined by the formula $m \geq \log_2 (k - 1)$, where k is the number of rows to be added at one time.

In the case of a design for adding an arbitrarily large set of numbers with a fixed delay constraint, the new technique will need fewer LSI chips than the conventional technique which uses 3-input "carry save" adder-tree structures followed by a "carry look ahead" adder. Alternatively, for a design with a fixed number of LSI chips as a constraint, the new technique will add the numbers faster than conventional ones.

Although the technique requires more circuitry than conventional adders, the columnar adding approach becomes practical because of LSI technology, which packs greater amounts of logic circuitry in less space at lower cost. When conventional adder techniques were first formulated, many circuit components had to be hand assembled on larger circuit cards. This created cost and space constraints on computer designers.

Although the illustrations shown describe implementation of the technique for addition, it is equally applicable for multiplication which, in a computer's binary numbering system, is nothing more than addition of rows of the same number, appropriately shifted.

According to its developers, an arithmetic unit designed with the new technique would be particularly useful in computer systems used for both scientific and business applications. Scientific users frequently have to process large amounts of numerical data to get small amounts of output. The less time it takes them to process this data, the more computer time that is available to them and their business counterparts.

The columnar adding technique was developed by engineers Ronald Waxman and Shanker Singh at IBM's development laboratory in Poughkeepsie, NY. It is described in detail in their paper, "Multiple Operand Addition and Multiplication," which was presented last month at the Fall Joint Computer Conference in Anaheim, CA. — *FE* ▭

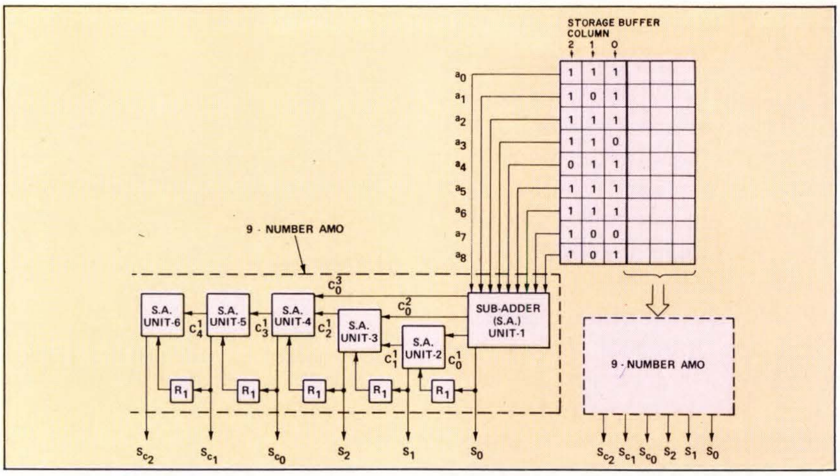


Fig. 1—A 3-bit wide column partition adds each column, in turn, yielding results at outputs S_{C_2} through S_0 after three cycles through the 9-number adder for multiple operands. During the first cycle, column 2 is added and the temporary results are stored in the registers labeled R_1. During the second cycle, column 1 is added with the contents of registers R_1 suitably shifted, and the result is placed back in registers R_1. During the final cycle, column 0 is added with the contents of register R_1, again suitably shifted, and the results are gated out on outputs S_{C_2} through S_0.

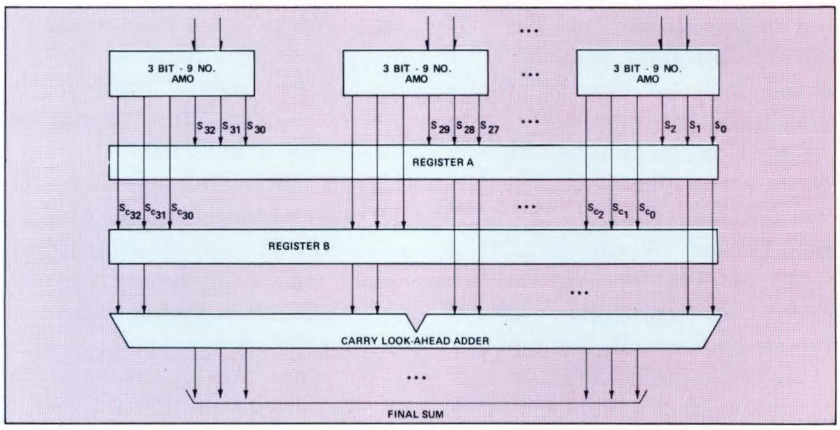


Fig. 2—The outputs from Fig. 1 are fed into register A and register B which in turn have their contents fed into a carry look-ahead adder, thus yielding the final result in one more cycle. A total of 4 cycles is used to add 9 numbers, which are divided into 3-bit wide column partitions.

Measurement breakthrough leads to new value for speed of light

The extension of direct frequency measurements for the frequency of visible light, a breakthrough announced earlier this year, has led to a 100 fold more accurate value of the speed of light. That value is 299, 792,456.2 meters/sec with an accuracy of ±1.1 meters/sec (or 186,282.3960 miles/sec ±3.6 ft/sec). The new value is 100 times more accurate than Froome's value measured in 1957 in England and is 20 times more accurate than that which Bay, Luther and White made just this year at the National Bureau of Standards (NBS) in Gaithersburg, Maryland.

The speed of light is one of the important fundamental constants of nature. Terrestrial and lunar distance-measuring experiments depend directly on its value. It is also involved directly in several fundamental relationships such as the famous $E=mc^2$ equation.

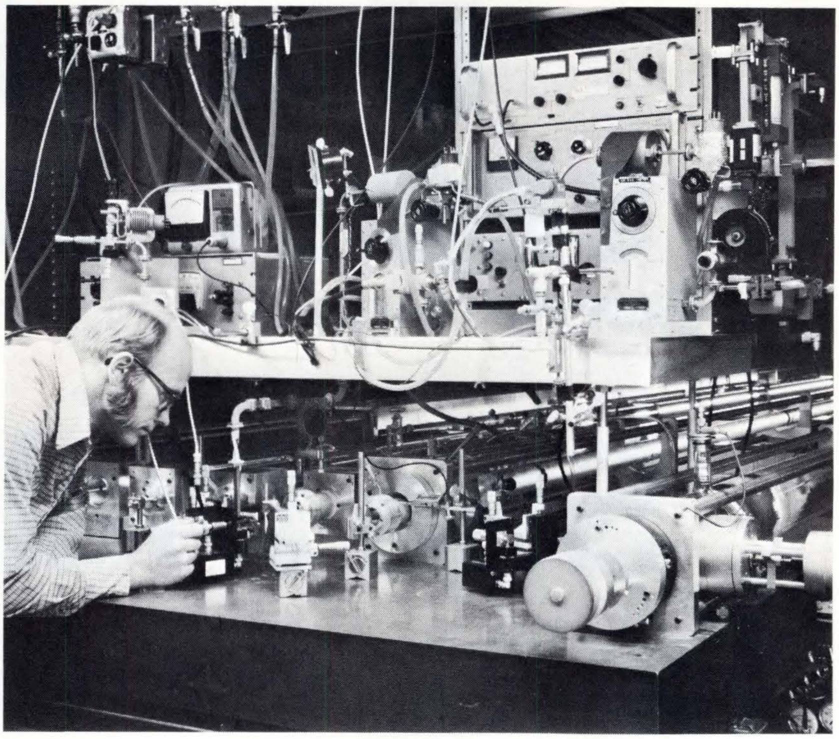
To obtain the new value of c, it was necessary to measure both the frequency and the wavelength of a very stable laser. The speed of light is the product of these two. The laser, an infrared 3.39-micrometer helium-neon device, is stabilized; that is, it has its frequency fixed by methane absorption as follows: A laser provides very pure light by ordinary standards, but the light tends to shift in frequency or wavelength. Only by accident will two lasers emit exactly the same frequency under nonstabilized conditions. The NBS research achieved a method of stabilizing the laser by passing the beam through a gas and locking its frequency to a certain narrow absorption line in the gas. Any other similar laser using the same kind of absorption gas will then operate at the same frequency. This reproducibility is essential to the effort of improving measurement standards in general and was crucial to this experiment in particular.

The technique to measure this high frequency employs a frequency multiplier chain which connected the atomic frequency standard at about 9 billion cps to an infrared laser nearly 100 times higher in frequency. Five different lasers and five other microwave oscillators (klystrons) were used in this chain.

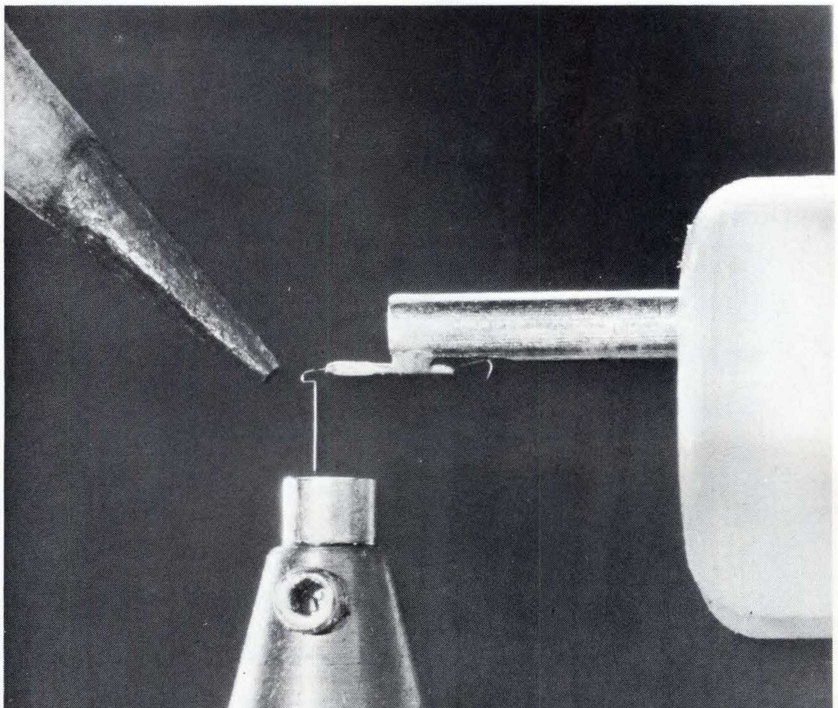
The world's highest speed detector, a catwhisker diode similar to that used in early crystal radio receivers, was used to multiply the laser frequencies. These diodes, developed at MIT and NBS, serve to compare successively an integral multiple of one laser frequency with the next higher laser frequency in the chain. In this succession of measurements, the atomic frequency standard was linked to the frequency of the helium-neon laser.

The wavelength measurement—one of the most accurate ever made—compared the wavelength of the methane stabilized laser with that of the length standard—radiation of the krypton atom. The accuracy of this measurement is limited only by uncertainties in the length standard itself.

This points to the desirability of improving the length standard, either by replacing it with a stabilized laser or defining the value of c. The first will permit still more accurate determinations of c. The second alternative, defining c, would enable an experimentalist to use a frequency standard to accurately establish the length of the meter. This combined frequen-



Contact adjustment of one of the catwhisker diodes concentrates the carbon dioxide laser beam on the diode. From right to left are the five lasers used—a hydrogen-cyanide laser, a water vapor laser, two carbon-dioxide lasers and a helium-neon laser.



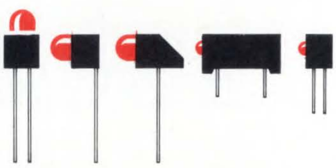
The tip of the pencil points to the catwhisker diode used in the frequency measurement experiments.

Dialight sees a need:

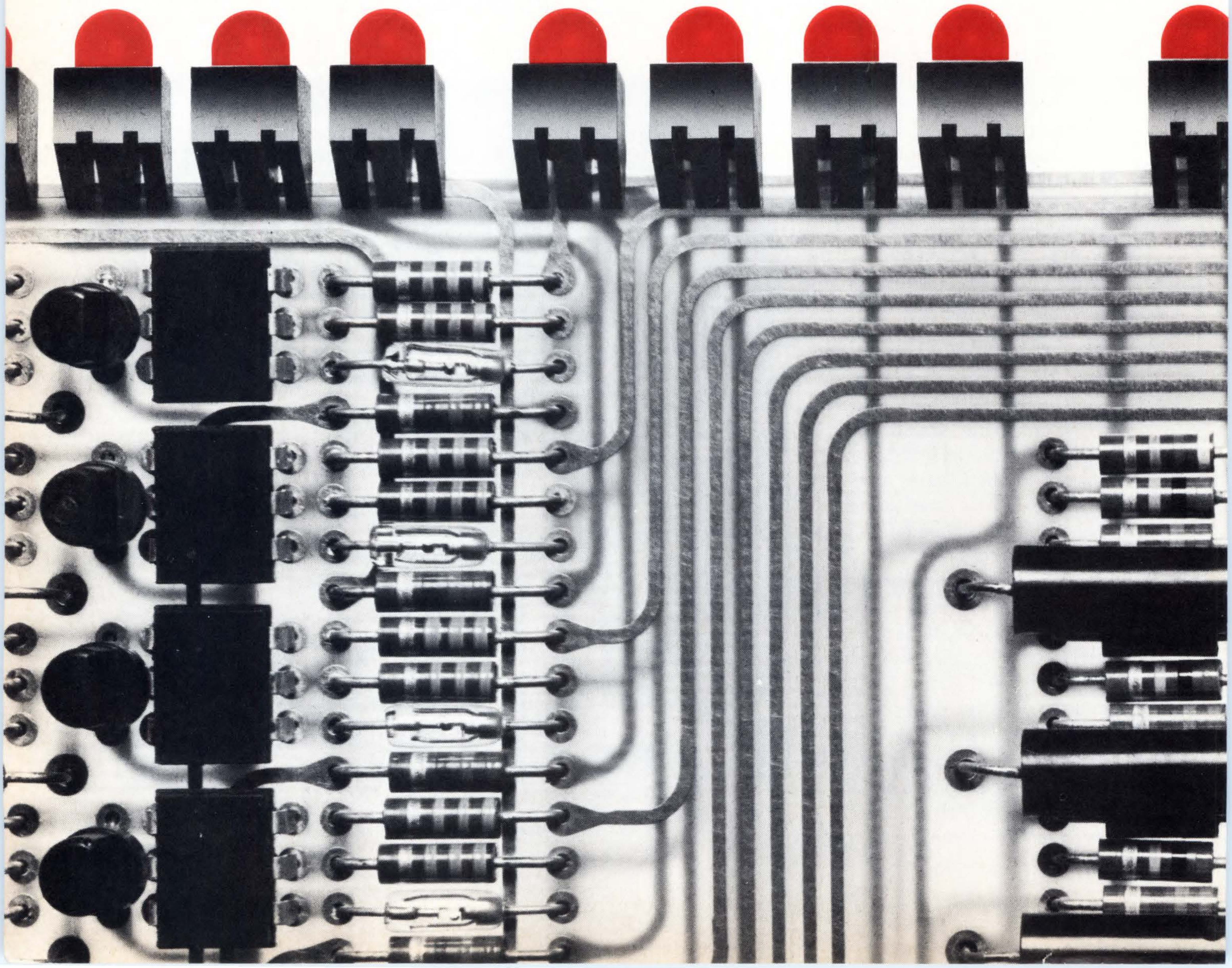
(**Need:** Find a very small fault in a very large system.)

See Dialight.

All printed-circuit boards need a fault indicator; that's why Dialight has developed such a broad family. These tiny LED devices signal where and when a fault occurs in a complex electronic circuit — and this can reduce downtime to a minimum. With some Dialight fault indicators, you can get as many as 10 units in just 1" of space. These devices, which come in a variety of sizes, are designed to operate from 1.6 to 14 volts and are available with both axial and right angle leads. They



can be driven directly from DTL or TTL logic and can also serve as logic-state indicators, binary data displays, or just as indicators, as in this p-c board furnished by Struthers-Dunn, Inc.* But Dialight's fault finders are only a small part of their fast growing family of light-emitting diodes. Additional opto-electronic devices are extensively used in cartridges, lighted push-button switches, opto-isolators, and readouts, all supplied by Dialight. A wide variety of discrete LEDs further adds to the broad family.



cy-length standard would suffice for both kinds of measurement. Thus, it would be possible to eliminate the need for a separate length standard.

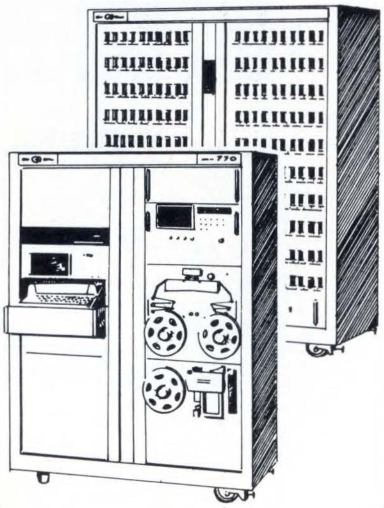
What the new value means!

The constant c appears in many physical equations describing the behavior of the universe. Long-distance measurements with lasers, and radar measurements of interplanetary distances require precise knowledge of time of flight of the light or radar pulse; the distance is calculated by multiplying this time by the value of c. The new value of the speed of light will enable engineers and space scientists to more accurately track satellite and space vehicles.

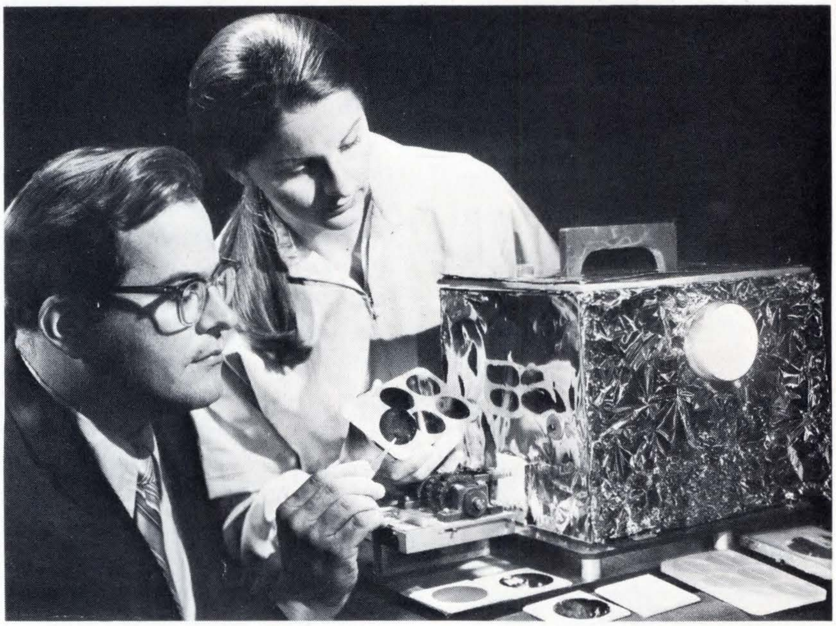
Spin-off benefits open up possibilities for a whole new frequency range for telecommunications, a 1000-fold increase over all the frequency bands presently utilized. Also, manufacturers can achieve finer accuracy in instrument manufacture.

A new standard?

The great accuracy in this measurement demonstrates the possibility of a single standard for both length and time. The importance of linking these standards was described by Dr. Lewis Branscomb, former director of NBS, who said, "Ever since Albert Einstein showed that time can be considered the fourth dimension of the space in which we live, scientists have looked forward to the possibility of using one gage—one yardstick so to speak—not only for the three dimensions of space but for the fourth dimension of time as well. To interchange clocks and rulers, scientists must know the speed with which light travels, which is equal to its wavelength times its frequency. With this demonstration that both the space (wavelength) and time (frequency) dimensions of a single light source can be measured with prodigious accuracy, this goal is now within our grasp." —*RF* □



Ultraviolet light removes excess photoresist—speeds SC fabrication



New process uses intense ultraviolet light to clean excess photoresist from semiconductor wafers. Here, Dr. Donald A. Bolon, developer of the technique, prepares to run sample wafers through a test chamber.

A long-standing problem in the semiconductor processing industry has been the cleaning of excess photoresist from semiconductor wafers. The photoresist, a polymer film sensitive to light, is used in etching microscopic circuit patterns onto the wafer. After etching takes place, the leftover plastic film must be completely removed.

A new process, developed by General Electric Co., holds promise of speeding and simplifying semiconductor fabrication.

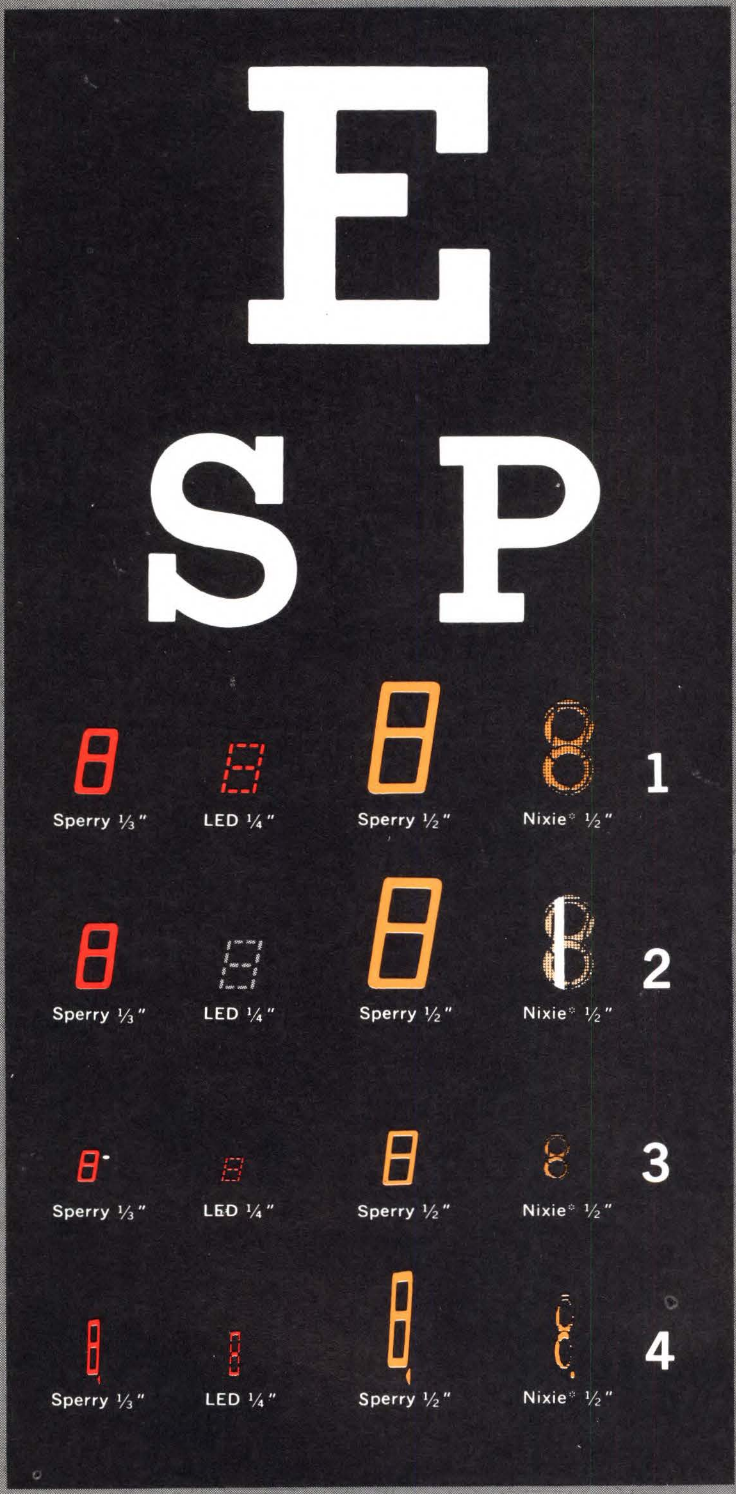
In the new GE process, the photoresist is exposed to intense ultraviolet light in the presence of air, causing the material to break down and vaporize. A typical film of photoresist plastic (depending upon its composition and thickness) can be completely removed from a semiconductor wafer in 25 to 40 minutes.

The process is reportedly the first that lends itself to the continuous removal of excess photoresist material. All other known techniques require the processing of wafers in batches and are thus inherently slower.

In addition, according to the developers, "ultraviolet depolymerization" is the first dry process that operates at atmospheric pressure and at modest temperatures (about 250°C). The most widely used methods for removing photoresists currently involve soaking the polymer film—either in a solvent that causes it to swell, after which it is shaken or abraided off, or in an acid solvent, which destroys the polymer. In many cases, however, a semiconductor processor desires to remove the photoresist without subjecting the substrate to solvents or acids. This is especially important where soft metal overlays are present that would be damaged by abrasion or by corrosive solvents.

In tests at the GE Research and Development Center in Schenectady, NY, Dr. Donald A. Bolon, developer of the process, has found that ultraviolet depolymerization of photoresists proceeds at rate of about 1000 Å per minute. The process can be made to operate some ten times faster simply by injecting about 2% ozone gas into the processing chamber. —*FE* □

The Sperry eye test for display equipment buyers



The above is a printed interpretation of the appearance of the more popular displays. You are encouraged to make the same comparison with actual devices.

The old saying "what you see is what you get" certainly applies to the purchase of equipment incorporating displays — panel meters, DVM's, multimeters, counters, instruments, calculators and other equipment. If you can't clearly and easily read the information being displayed then you're not getting full product value. And, you're obviously not getting equipment supplied with advanced Sperry planar displays†.

How do you tell if they're Sperry displays? Simply take the Sperry eye test.

1. **Do the displays appear as uniformly bright, continuous characters with no irritating gaps or filaments and screens to reduce readability?**
   ☐ YES ☐ NO
2. **Do the displays remain bright and clearly legible with no glare or appreciable fading even under direct sunlight conditions?**
   ☐ YES ☐ NO
3. **Can you quickly, easily and accurately read the displays from 20 to 40 feet away?**
   ☐ YES ☐ NO
4. **When the unit is positioned within a 130° viewing angle, can you still clearly read the displayed characters?**
   ☐ YES ☐ NO

If you answered YES to all four questions, you already have your eyes on equipment featuring preferred Sperry displays.

If you answered NO to any of the questions, you owe it to yourself to take a comparison look at products equipped with superior Sperry displays.

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To help you make the right equipment selection, Sperry offers the handy "Buyer's Guide for Equipment featuring Electronic Displays". It's your's for the asking. Order your copy today by checking the reader service card or phone or write: Sperry Information Displays Divison, P.O. Box 3579, Scottsdale, Arizona 85257, telephone (602) 947-8371.

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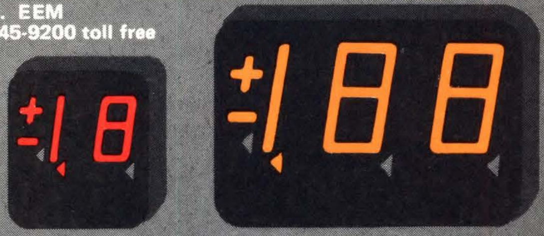

Sperry ⅓" Sperry ½"

units are available for use with red filters

It's a whole new ball game in displays!

†Patents Pending
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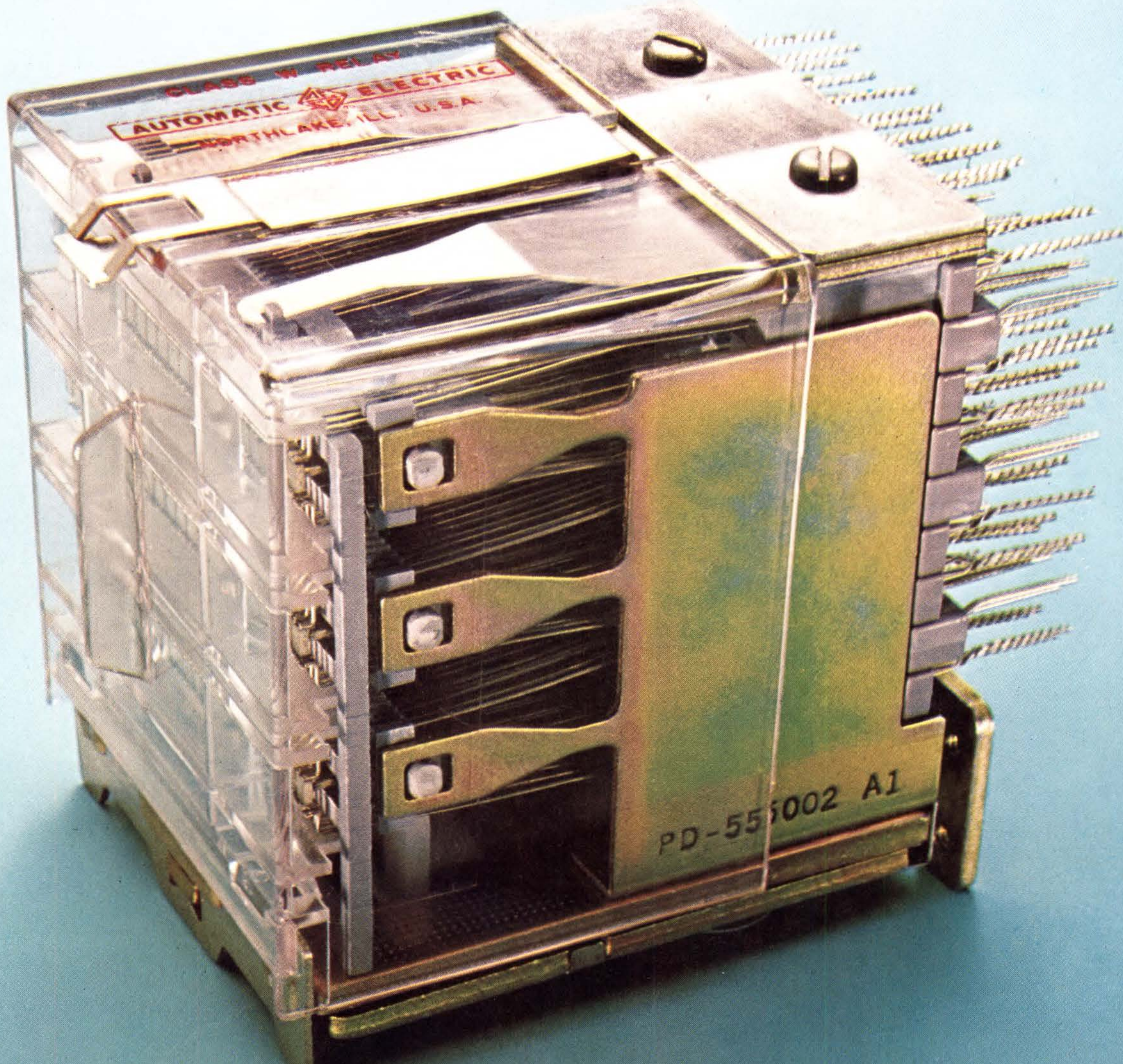
SPERRY RAND

CHECK NO. 39

Reliability is staggered steps and a hunk of DAP.



Expect over a billion operations.

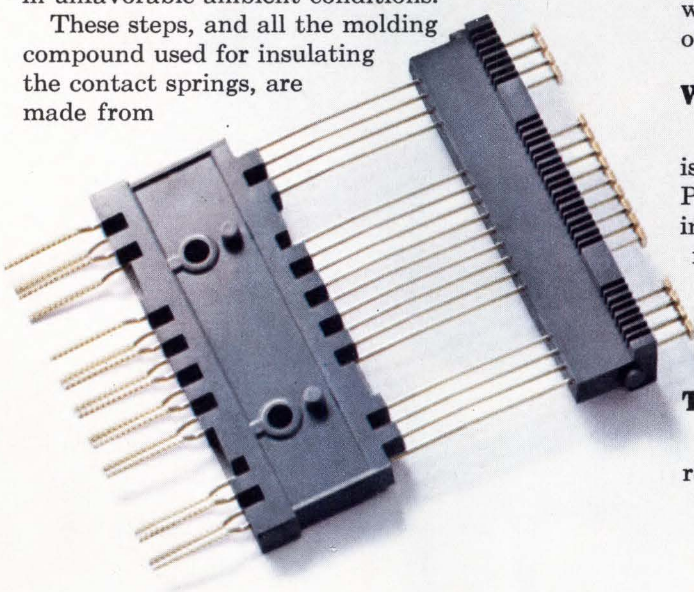
Our Class W wire-spring relay is different. In fact, there's nothing like it in the entire industry. Where else can you find a relay with lots of contacts and a mechanical life of more than a billion operations! That's about two and a half times the life of the best conventional relay around.

Another nice thing about our Class W is that it takes up a lot less space and costs less than using a bunch of other relays. That's because we build our Class W relay with one, two or three levels of contact assemblies, with 17 form C combinations per level. By the way, they're available with gold contacts for low-level switching.

Making it tough on creepage.

All those staggered steps you see on the side were put in to raise the breakdown voltage between terminals. These molded steps add extra creepage distance between the terminals. This really counts for high voltage testing, or when using our Class W in unfavorable ambient conditions.

These steps, and all the molding compound used for insulating the contact springs, are made from

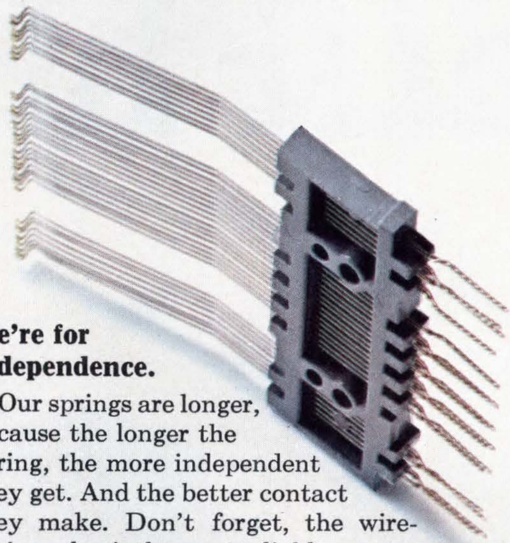


diallyl phthalate. (They call it DAP for short.) It has great insulating properties and it wears like iron. Even if the humidity is high, you have excellent protection.

Redundancy—two springs are better than one.

Each of our long wire-spring contacts has an independent twin with the same function. One tiny particle of dust could prevent contact on other relays. Not with our Class W. You can be sure one of the twins will function. That's back-up reliability.

The twin contacts are twisted together at the terminal end. Then we give them a spanking (you might call it swedging) to provide solderless wrap.



We're for independence.

Our springs are longer, because the longer the spring, the more independent they get. And the better contact they make. Don't forget, the wire-spring relay is the most reliable way to get a permissive make or break contact. You can rely on it.

The middle contact springs have to be stationary. To make sure they stay that way forever, we actually mold them between two thick pieces of DAP on both ends. Just try to move one.

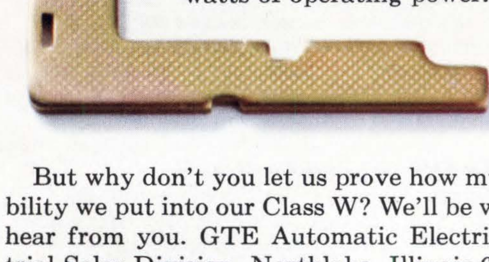
When we say flat, it's flat.

Each frame, banged out by a gigantic machine is extra thick and extra flat. Then they're planished. Planishing is another step we go through in forming the frame to add strength and stability by relieving surface strain.

We've made our spring-loaded pile-up clamp extra thick, too. Once it's tightened down, the whole pile-up is nice and tight, and stays tight.

There's more.

We could tell you a lot more about our Class W relays. Like how the tough high-temp molded



cover protects against dust and has molded ribs to keep the spring contacts in place. Or how this relay with 51 circuit transfers is so sensitive it requires only four to six watts of operating power.

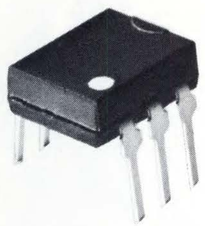
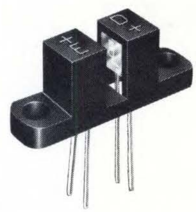
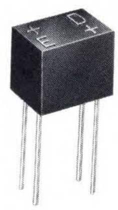
But why don't you let us prove how much reliability we put into our Class W? We'll be waiting to hear from you. GTE Automatic Electric, Industrial Sales Division, Northlake, Illinois 60164.

GTE AUTOMATIC ELECTRIC

CHECK NO. 26

GENERAL ELECTRIC

OPTOELECTRONIC COUPLER LINEUP

			
H10 SERIES COUPLERS	**H11 SERIES COUPLERS**	**H13 SERIES INTERRUPTER MODULES**	**H15 SERIES COUPLERS**
• 3 hermetically packaged models offer choice of SSL-Phototransistor, SSL-Photodarlington and SSL-light sensitive SCR	• 6 models offer interchangeability with popular industry types • H11A1 and H11B1 offer 50% and 500% min current transfer ratios respectively • 2,500V isolation	• 4 models offer "no contact" switching for use with shaft encoders, counters, position sensing, keyboards and limit switch application	• 4000V isolation • 4 low cost models for pulse transformer replacement, SCR and TRIAC triggering • Solid State reliability at low cost

OUR NO. 1 GOAL:
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GENERAL ELECTRIC
YOUR BEST BUY

BEST BUY
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QUALITY...SERVICE...VALUE

AVAILABLE NOW FROM YOUR AUTHORIZED GENERAL ELECTRIC DISTRIBUTOR

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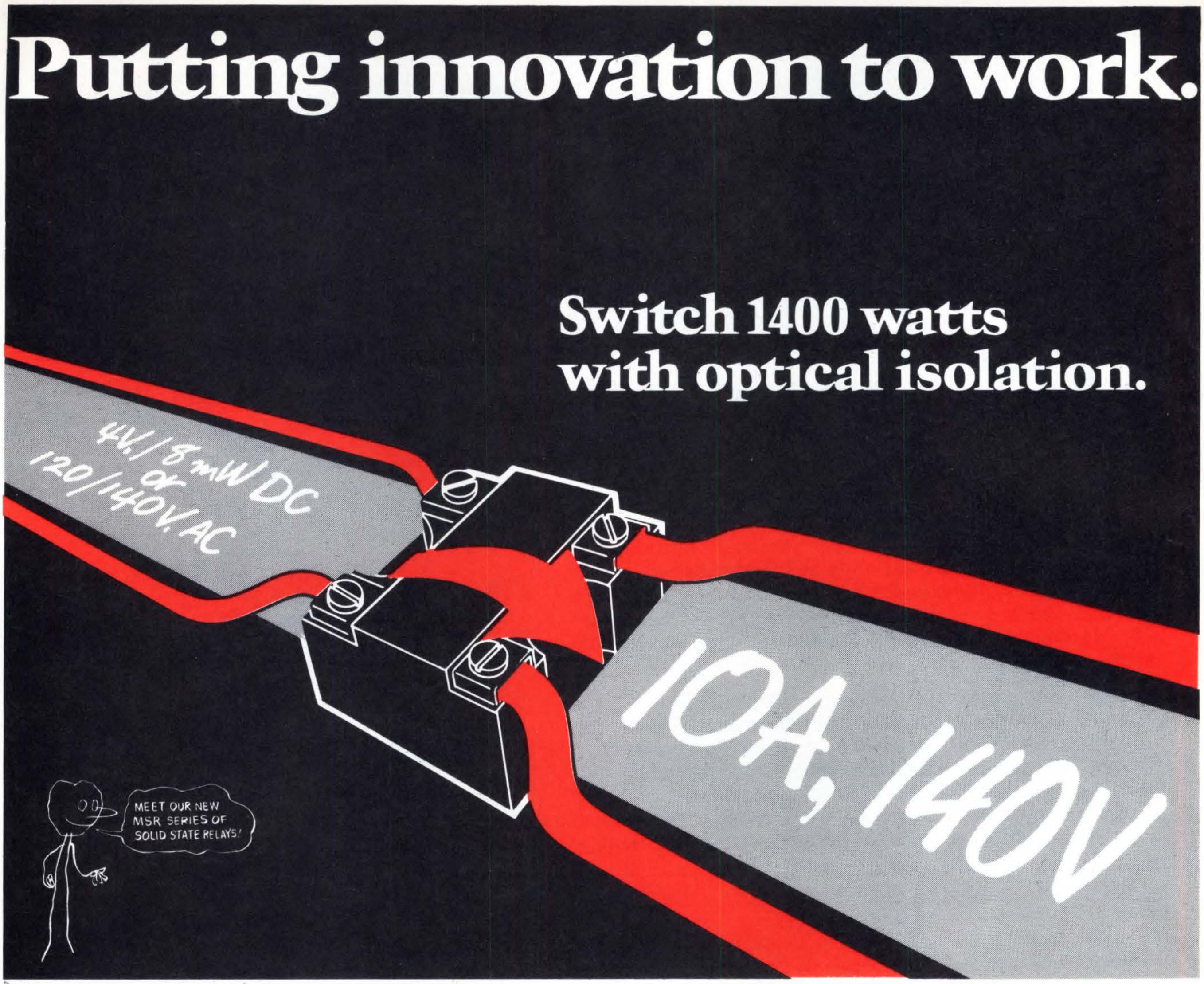
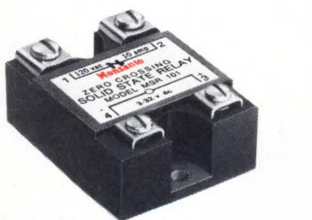


These solid state switches offer normally-open or normally-closed contacts that are compatible with TTL, DTL, or MOS inputs (8mW at 4 volts). That's for DC. For AC applications, they'll handle 120 or 240 VAC input. The output of either variety switches 140 volts AC at 10 amps.

There are many more features: **zero voltage turn-on; zero current turn-off;** they eliminate electrical noise from arcing contacts, transients from contact bounce, high voltage transients with inductive loads, and derating because of inductive or lamp loads.



MSR100
DC input, N.O. contacts

MSR101
DC input, N.C. contacts

MSR102
AC input, N.O. contacts

MSR103
AC input, N.C. contacts

They also have high noise immunity; they're protected from false actuation; they don't need electromagnetic shielding, coil-suppression diodes, transistor buffers or magnets.

And they're small (2¼" x 1¾" x 1⅞"), 4 ounces, with rugged screw terminals and a wide operating range. Ask for our new data sheet on the MSR Series of solid state relays from **Monsanto Commercial Products Co.,** Electronic Special Products, 10131 Bubb Road, Cupertino, California 95014. Phone (408) 257-2140.

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Monsanto

CHECK NO. 30

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The FET set! Everything you need in FET op amps

The Burr-Brown family of TO-99 FET op amps offers you a one-stop source for the exact FET units you need, regardless of your requirements. The three units highlighted below are representative of the performance and price advantages available from Burr-Brown's new 14 unit series. They are pin compatible with 741 types and are 100% tested to all min/max specifications.

Hybrid/thin-film techniques and a monolithic FET input stage provide excellent drift characteristics for source impedances to 1 MΩ. Active laser trimming of proprietary Burr-Brown high-stability, thin-film resistors contributes to outstanding performance at reasonable prices. Both output short circuit and input-to-supply-voltage protection are provided. Units are also available with MIL temperature ratings and MIL-883 screening.

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Initial Offset, 25°C, Max.	$250\mu V$	$\pm 500\mu V$	$\pm 15 mV$
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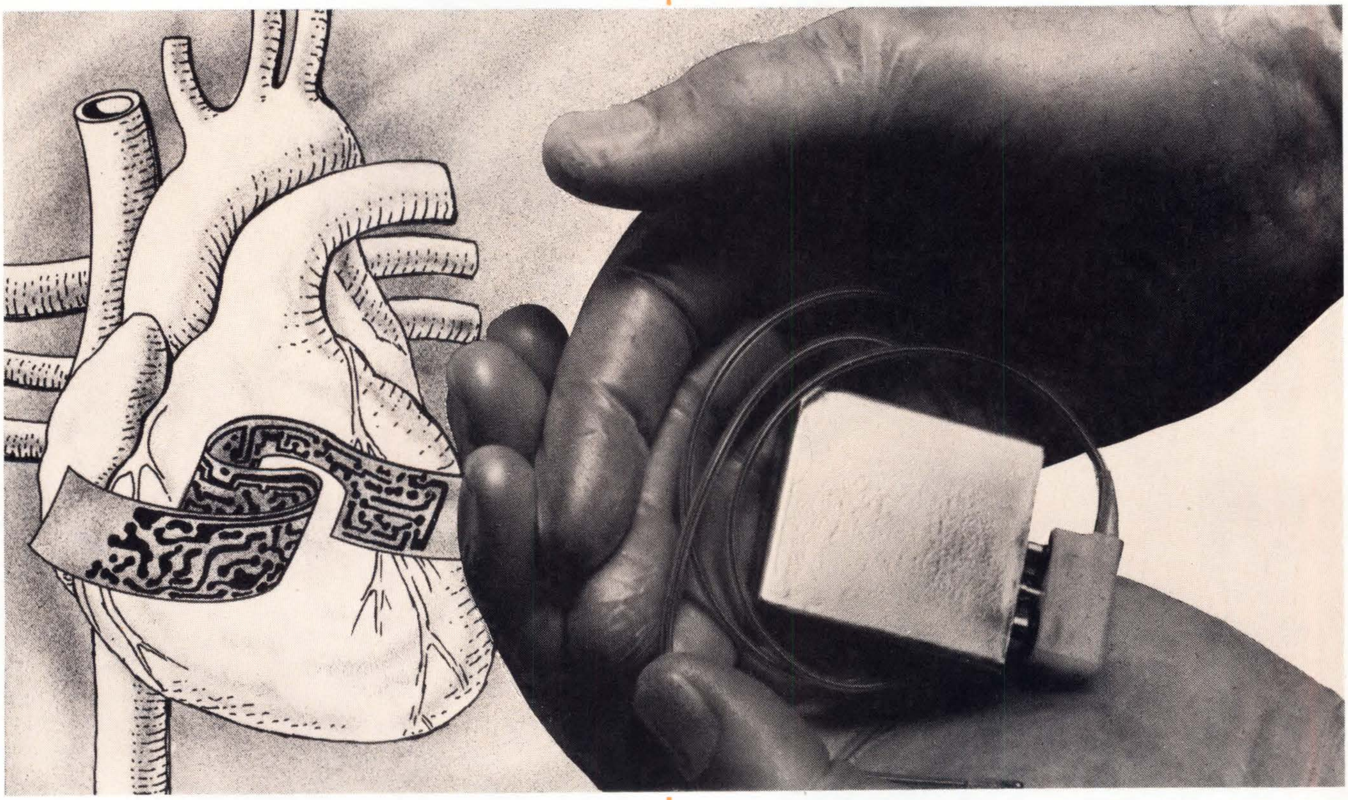
More and more heart patients are walking around with one of our flexible circuits in their chests. The circuit is inside a heart pacer — made by Medical Devices, Inc. of Seattle. This compact pacer, weighing just 110 grams, is literally a bundle of energy. It only paces when the heart needs help and, upon demand, will pace continuously up to 4 years without replacement.

We're mighty proud Medical Devices, Inc. chose Buckbee-Mears to meet their very exacting circuit requirements. They used our flexible circuitry because it was lighter weight than a printed board, more reliable, and made the unit easier to assemble.

Our flexible circuit enabled Medical Devices, Inc. to manufacture the entire 83 component assembly in a long, narrow, flat shape and fold it to fit into the hermetic sealed container. Our scientists had to create a special adhesive system to bond the annealed copper circuit to the dielectric.
But solving unique problems is a specialty with our Flexible Circuits Group. Whatever you need in flexible circuitry, call us. We'll get to the heart of the problem fast.

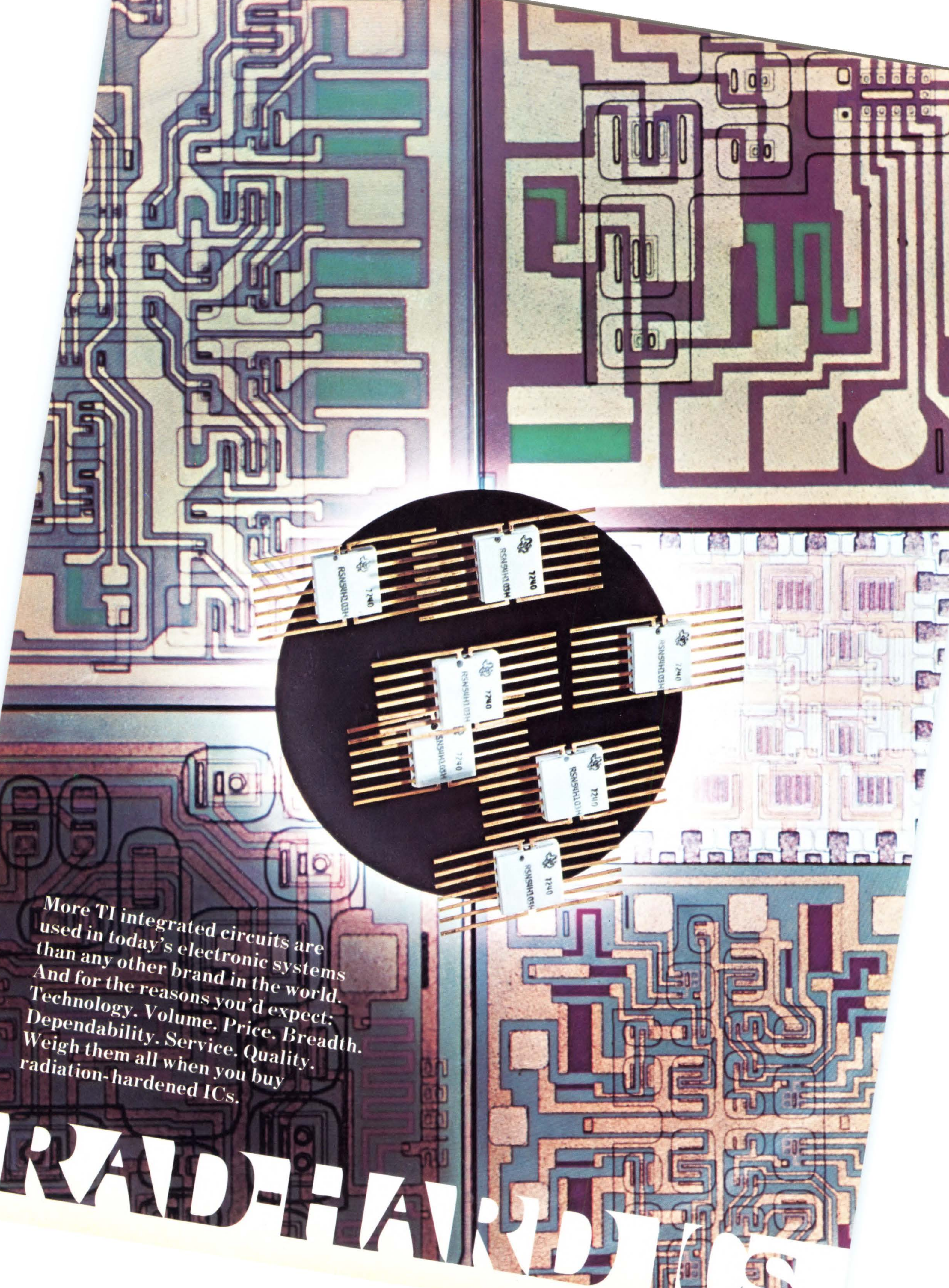
Buckbee-Mears Company, 245 E. 6th Street, St. Paul, Mn 55101, Telephone (612) 228-6371, Telex 297080



BMC lightweight flexible circuit helps this heart pacer work continuously for up to four years.

BUCKBEE-MEARS COMPANY
bmc
ST. PAUL, MINNESOTA 55101

CHECK NO. 27


More TI integrated circuits are used in today's electronic systems than any other brand in the world. And for the reasons you'd expect: Technology. Volume. Price. Breadth. Dependability. Service. Quality. Weigh them all when you buy radiation-hardened ICs.
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If your system calls for radiation-tolerant ICs, TI can provide full-service support.

49 standard digital and linear functions. Custom capability backed by more than a decade of "rad-hard" R&D and production experience. Computer-aided design. Comprehensive documentation.

Full service.

From materials technology to product design, manufacturing experience and capability, support data and program management—Texas Instruments can supply everything you need to meet the most challenging system and program requirements.

TI has been solving radiation effects problems for more than 10 years...and is a major supplier of radiation-hardened devices for strategic defense systems.

Technological strength—now and in the future

TI is thoroughly experienced in all technologies basic to radiation-tolerant integrated circuits, including dielectrically isolated substrates, thin-film resistors, minimum-size transistor geometries, narrow base widths, various packaging options and photocurrent compensation, where required.

Computer-aided design is now a matter of routine for both the design *and* layout of TI radiation-tolerant integrated circuits.

And TI will continue to extend its technological capability by combining radiation-hardening expertise with in-depth knowledge of MSI, beam leads and low-power Schottky TTL. (In addition, TI has depth experience in "rad-hard" discrete devices—both power and small-signal—and offers a broad line.)

Complete custom capability

In addition to its standard rad-hard line, TI has complete facilities, personnel and know-how—including all necessary R&D back-up—for the design of radiation-tolerant devices to your specifications and program requirements. A top-secret facility and storage security clearance, as well as provisions for comprehensive documentation, further strengthen TI's ability to provide full-service support.

Industry's broadest standard line

TI today offers industry's broadest line of standard rad-hard ICs—49 digital and linear functions, with more to come.

Digital ICs

	1mW/30ns TTL	10mW/10ns TTL	20mW/7ns TTL	DTL
Quad 2 NAND	RSN54L00	RSN5400	RSN54H00	-
Hex inverter	-	RSN5404	RSN54H04	-
Triple 3 NAND	RSN54L10	RSN5410	RSN54H10	RSN15962
Dual 4 NAND	RSN54L20	RSN5420	RSN54H20	RSN15930
Single 11 NAND	-	RSN5431	RSN54H31	-
Dual 4 buffer	-	RSN5440	RSN54H40	RSN15932
Dual 4 power gate	-	-	-	RSN15944
Dual 2-wide AOI	-	RSN5456	RSN54H56	-
Single 4-wide AOI	RSN54L57	RSN5457	RSN54H57	-
Single 2-wide AOI	-	RSN5458	RSN54H58	-
Dual 3-2 AOI	-	-	RSN54H66	-
RS flip-flop	RSN54L71	-	-	-
JK flip-flop	RSN54L72	-	-	RSN15945
Dual D flip-flop	RSN54L74	RSN5474	RSN54H74	-
Dual J-K flip-flop	-	-	RSN54H103	-
One shot	RSN54L122	-	-	-
Dual 3 NAND	RSN54L130	-	-	-
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3-to-8 decoder	-	-	RSN54H149	-

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TEXAS INSTRUMENTS
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84073

Designers Guide to: Charge coupled devices

It's not too early to start looking at CCDs. Although still in the development phase, they may soon offer simple, low-cost solutions for imaging and high-density storage problems.

Barry T. French, North American Rockwell Corp.

In many repects, the operation of a charge coupled device (CCD) is similar to that of the more familiar MOSFET. Both rely on the phenomenon of inversion. Inversion amounts to a change in semiconductor type in the narrow region adjoining the surface. As shown in **Fig. 1**, a small positive bias will push holes away from the surface, leaving behind a region that is depleted of majority carriers. Increasing the bias will bend the energy bands even further, to the point where the conduction band approaches the

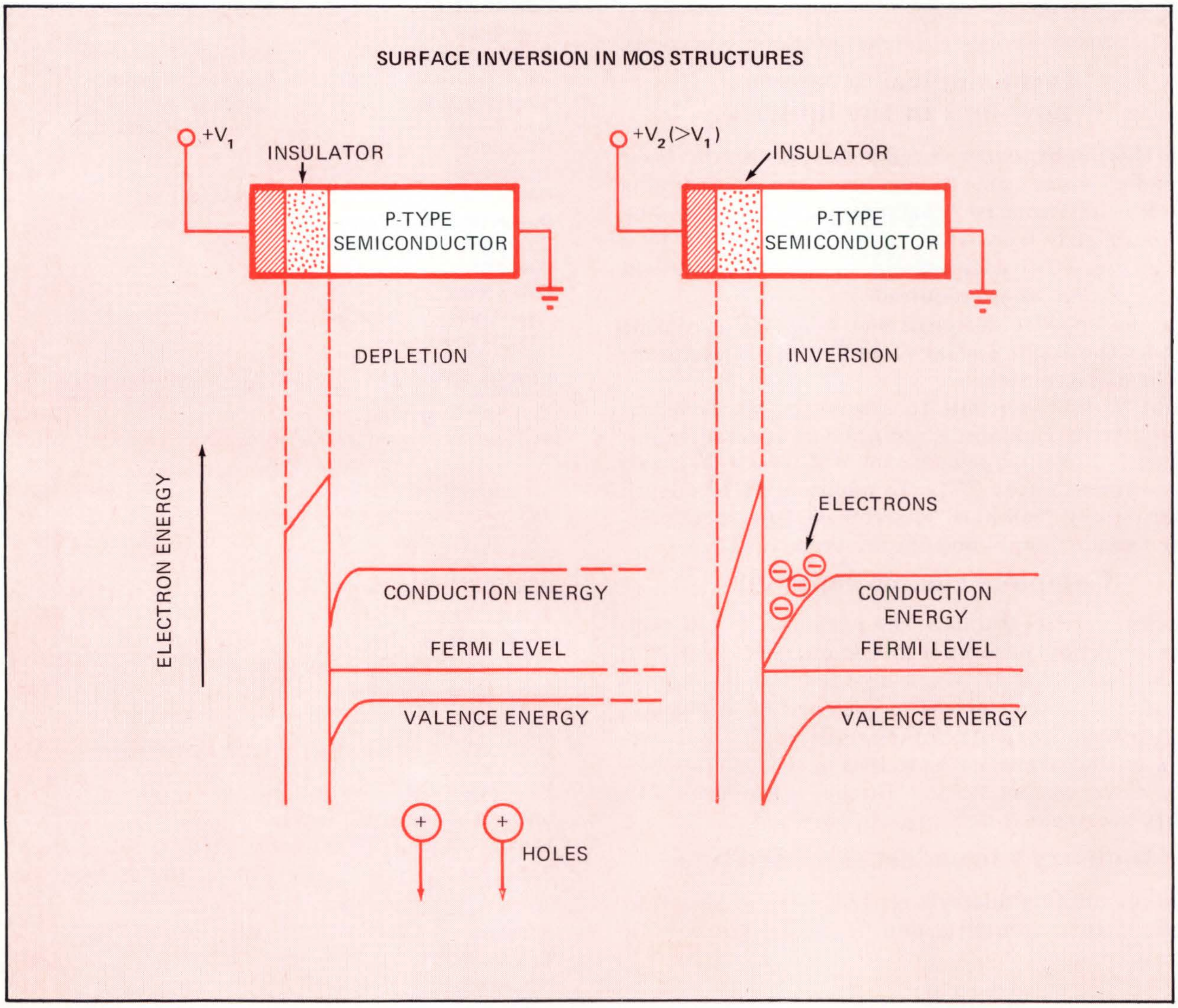


Fig. 1—Both MOSFETs and CCDs rely on the phenomenon of inversion for their operation.

Fermi level. When this happens, the concentration of electrons near the surface increases sharply and the material in this region takes on the characteristics of an n-type semiconductor.

CCDs operate by moving these minority carriers along the surface of a semiconductor in response to local changes in surface potential. In **Fig. 2**, a voltage applied at electrode A produces a surface potential sufficient to invert the semiconductor surface. When a larger voltage is applied at B, a deeper potential "well" is produced in that area, and mobile minority carriers move from A to B.

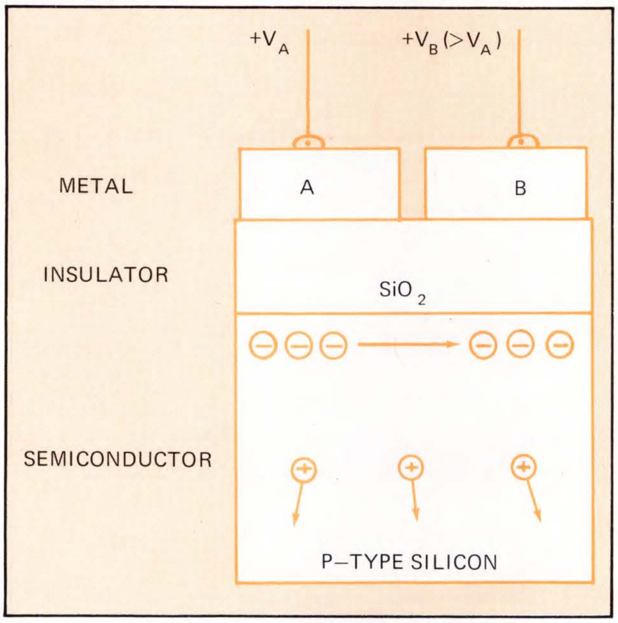


Fig. 2—Basic CCD mechanism uses familiar MIS (Metal-Insulator-Semiconductor) structure. Application of a sufficient potential at A will alter the characteristics of the semiconductor surface so that it behaves like n-type silicon (inverts). Application of a greater potential at B will transfer mobile charge from A to B.

If we build a long chain of these electrodes and apply potentials so as to continuously create deeper potential wells to the right of full wells, then charge will be caused to "flow" from left to right along the chain.

A simple system for scheduling such a chain of potential wells is shown in **Fig. 3**. Three synchronized ac voltages are applied to successive electrodes such that $\phi 3 > \phi 2 > \phi 1$. The graph below the semiconductor surface shows the depth of the resulting potential wells. Charge will move into the regions corresponding to the deepest wells. With this technique, the potential profile is changed at 120 degree intervals, advancing the charge to the next station. Three levels are required to prevent carriers from flowing in a reverse direction.

At North American Rockwell we prefer a four-electrode design, using two metallic layers separated by an insulator. This approach allows the use of two-phase drive voltages and also provides for some gate overlap, resulting in more efficient charge transfer. The potential-well diagram is considerably more complicated, as can be seen in **Fig. 4**.

Shift registers require refreshing

Quantities of charge can be inserted into a CCD chain by building a p-n junction into the semiconductor at the beginning of the line of cells. Another p-n junction will be required to extract the information at the output end. The resulting device can be operated as an analog delay line or digital shift register. A simple 10-bit, 4-electrode shift register is shown in **Fig. 5**. Such devices have been used extensively for the study of charge transport phenomena.

It should be noted that not all of the charge supplied by the input device will be delivered to the output diode. A certain fraction is waylaid in traps at the semiconductor surface and may be re-emitted later as noise. Also, it takes time to transport all of

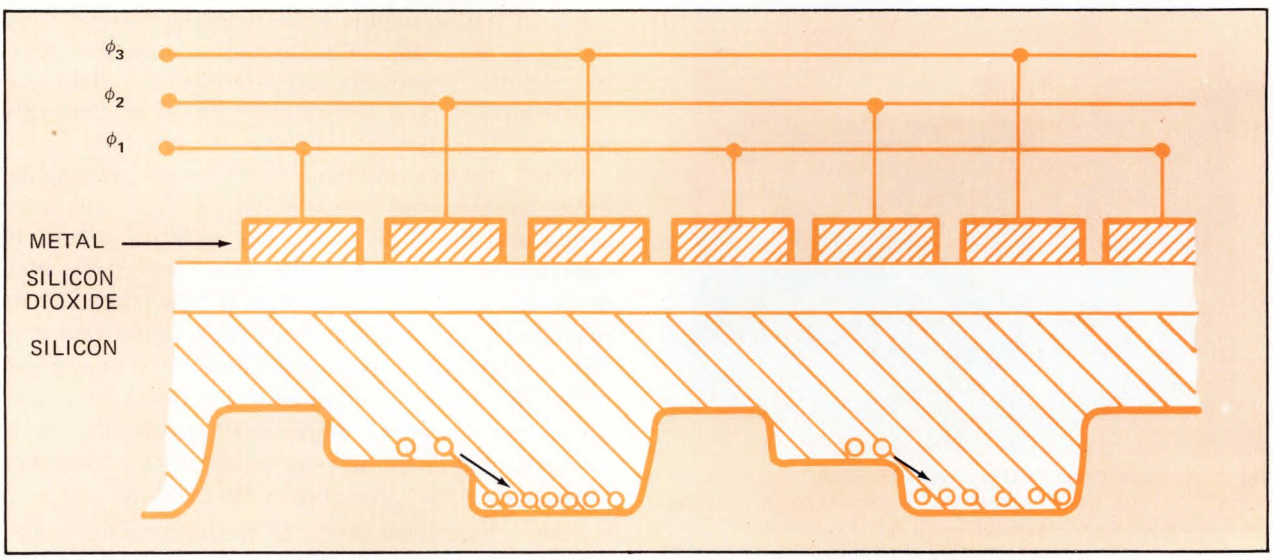


Fig. 3—Three-phase ac drive transports charge in CCDs. The graph shows depth of potential "wells" as seen by charge on the semiconductor surface.

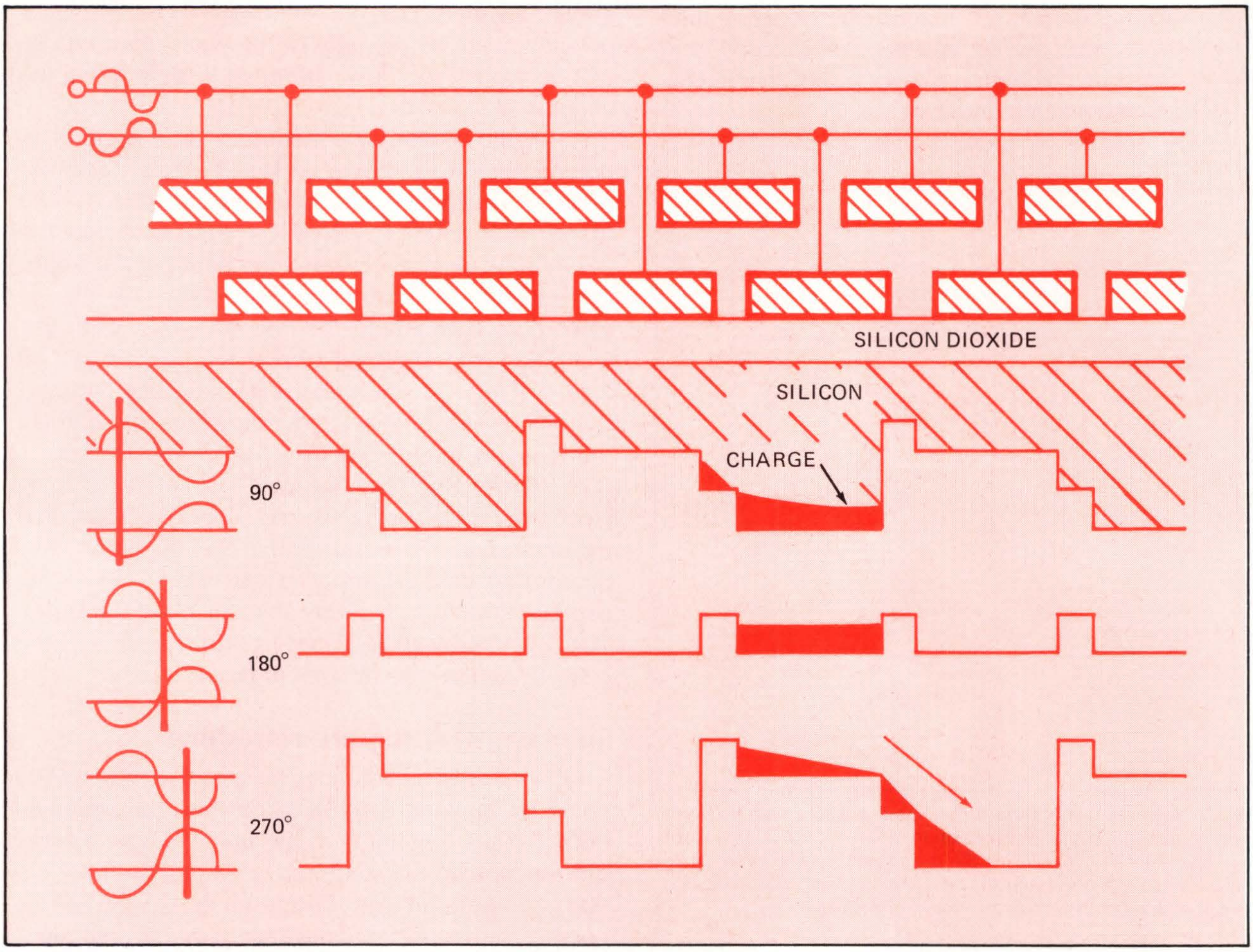


Fig. 4—A practical two-phase device. The potential-well diagrams represent surface potentials at three successive intervals. Note that voltages applied to the upper electrodes result in smaller surface potentials because they are farther away from the SC surface.

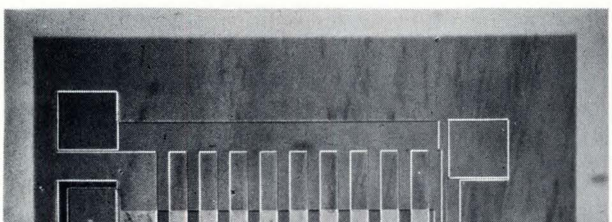


Fig. 5—A simple 10-bit CCD is used for the study of charge-transport phenomena. Center "Dogbone" is the conducting channel. P-diffusions at either end are for insertion and extraction of minority carriers. Upper (A) and lower (B) electrodes are sequenced to propagate charge along channel. Additional pads are provided for output gating.

the carriers, so transfer efficiency requirements impose limitations on operating frequency for any given device configuration.

Transfer efficiency may be improved by injecting a uniform small portion of charge in each well of the input so that no well is ever completely empty. This charge in the channel fills slow traps along the channel and thus improves charge transfer. A certain low signal level is then associated with binary zero detection. (This is termed "fat-zero" operation.)

When transfer efficiency falls below acceptable limits, the data may be extracted, restored, and reinserted into the CCD chain. **Fig. 6** shows a refresh operation for a simple digital data train. At the end of the first CCD chain, an output p-n junction detects degraded "bits" and supplies signals to the gate of a FET amplifier operated in the saturation mode. A set of "clean" ONES is supplied to the next chain, and the output of the FET amplifier modulates the input circuit of that chain. In practice the refresh circuit is fabricated on the same chip as the memory.

Power dissipation in the CCD shift register is approximately linear with clock frequency, and is highest when large quantities of charge are being trans-

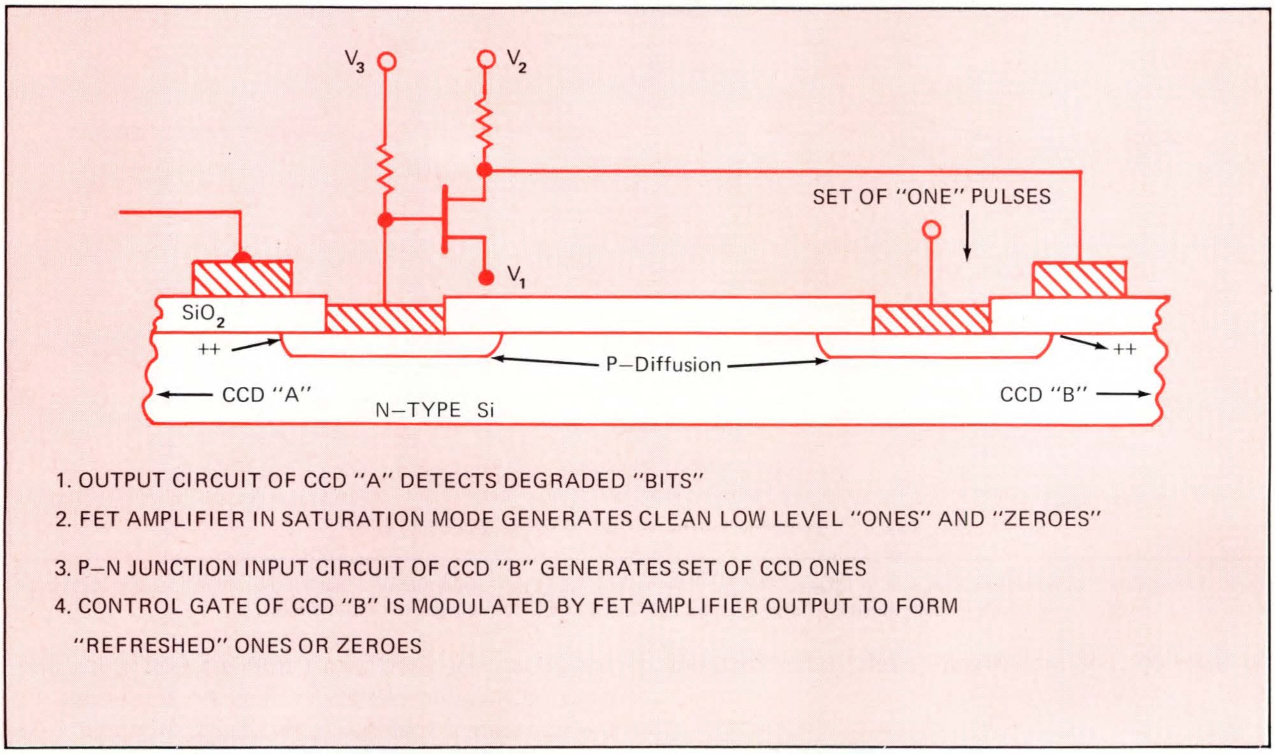


Fig. 6—Digital refresh circuit restores degraded signals to original levels.

ferred. Typical values for practical devices with small dimensions are in the 1 to 5 μW/bit range.

Ion implantation boosts transfer efficiency

High transfer efficiency (>99.99% per transfer) is necessary for high-frequency applications requiring long chains. One approach for improving high-speed transfer efficiency is to construct a potential slope inside each well so that charge is propagated by the built-in field rather than thermal diffusion. This reduces charge transit time across the well to a few picoseconds. Resistive gate layers and very closely-spaced small gates on thick insulator layers assist in providing built-in fields.

Transfer efficiency is also improved by reducing the number of traps (interface states) in the CCD channel. One promising method buries the transfer channel below the surface of the semiconductor where the material is more uniform. Minority carriers will follow a buried channel if the region is doped preferentially with ions of opposite charge (n-type silicon may be doped with boron). Satisfactory doping profiles can be attained with ion-implantation techniques.

Excellent transfer efficiencies up to frequencies of many megahertz have been achieved using ion-implantated channels. One limitation of this technique, however, is that only small quantities of charge can

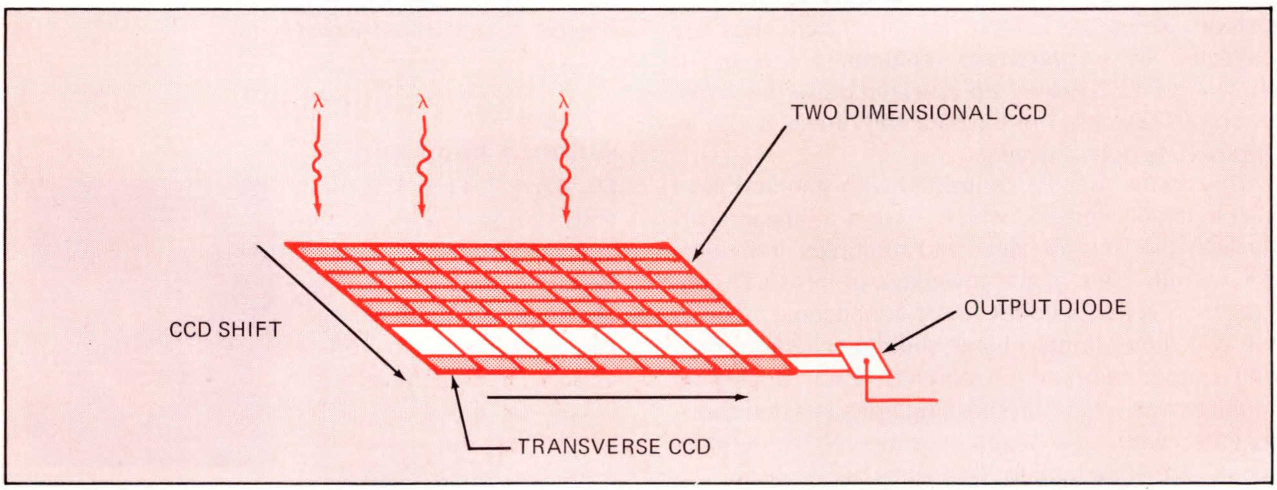


Fig. 7—In imaging applications, radiation (λ) impinges on 2-D CCD array, penetrates transparent superstructure and generates carriers in underlying semiconductor. Data is then shifted out, collected by transverse CCD and delivered to output circuit.

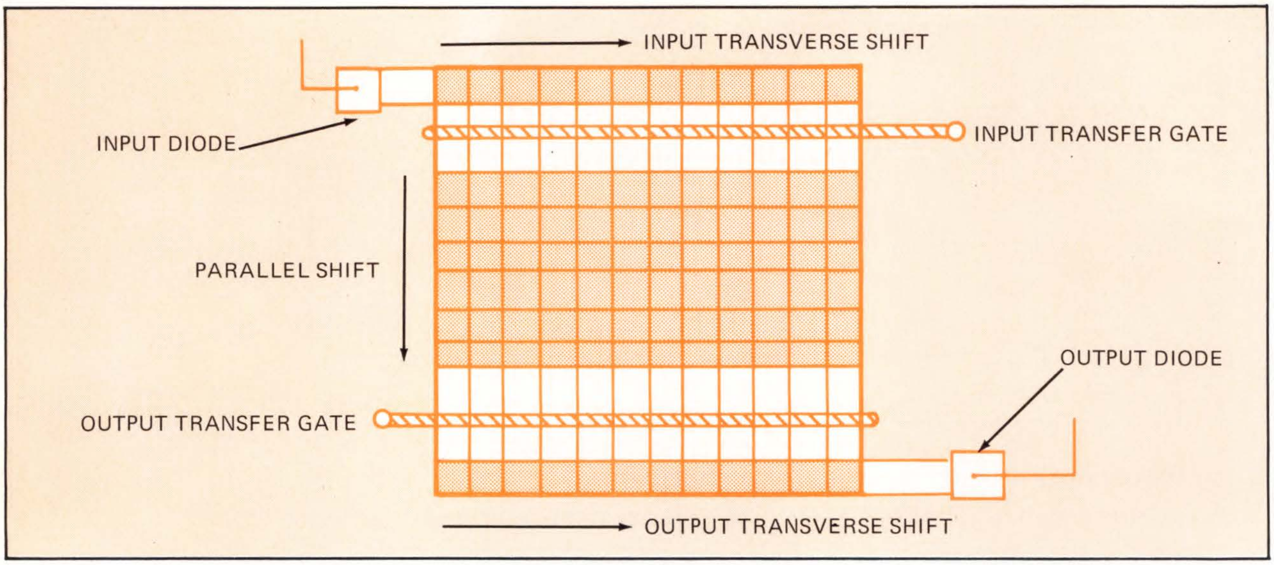


Fig. 8—Delay-line configuration is similar to imager. The input transverse CCD shifts information (charge) into device where it is transferred to 2-D array. Slower, parallel shift delivers charge to output transverse CCD for delivery to output circuit.

be handled. For high signal levels, other methods must be employed.

2-D arrays extend CCD applications

A number of two-dimensional arrays have been constructed, both as imaging devices and for applications requiring variable delay lines. Parallel-to-serial conversion is inherent in the two-dimensional imaging array. Radiation simultaneously impinges on the plane of the device, but readout occurs serially as the resulting charge is transferred in x-y sequences to the output terminal.

Here's how an imaging CCD works: During the read-in cycle, light is directed onto the array, through transparent conducting electrodes, past the insulator (also transparent) and into the semiconductor. There the photons interact with silicon, generating charge as a fuction of intensity. A shutter then closes so that light levels are not altered during the read process.

Readout is accomplished in straight forward x-y fashion. Rows are shifted laterally where they are collected in a transverse (columnar) register as shown in **Fig.** 7. After each row-shift pulse, the transverse CCD sweeps out the data and directs it into an appropriate output device.

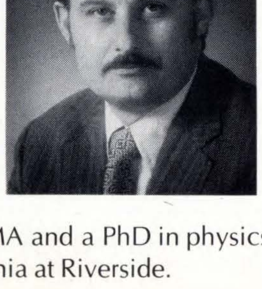
This design may be contrasted with standard IR or visible-region sensors which sweep a linear array through the field of view and multiplex individual cell outputs. One major advantage of this CCD configuration is the need for fewer connections. Due to the two-dimensional charge-shifting schedule, only one output terminal is required. Each dimension requires two sets of propagating voltages, and these, together with specialized biasing voltage requirements, bring the total to 8-10 wires per device.

If an additional transverse CCD is added at the input end of the rows and fed by a p-n junction, the device may be used as a variable-speed delay line. Opaque metallic electrodes may be substituted for the transparent material in this case, simplifying device manufacture. Slow clock speeds and long rows may be used, providing moderate-to-long delay times for large quantities of data (**Fig. 8**).

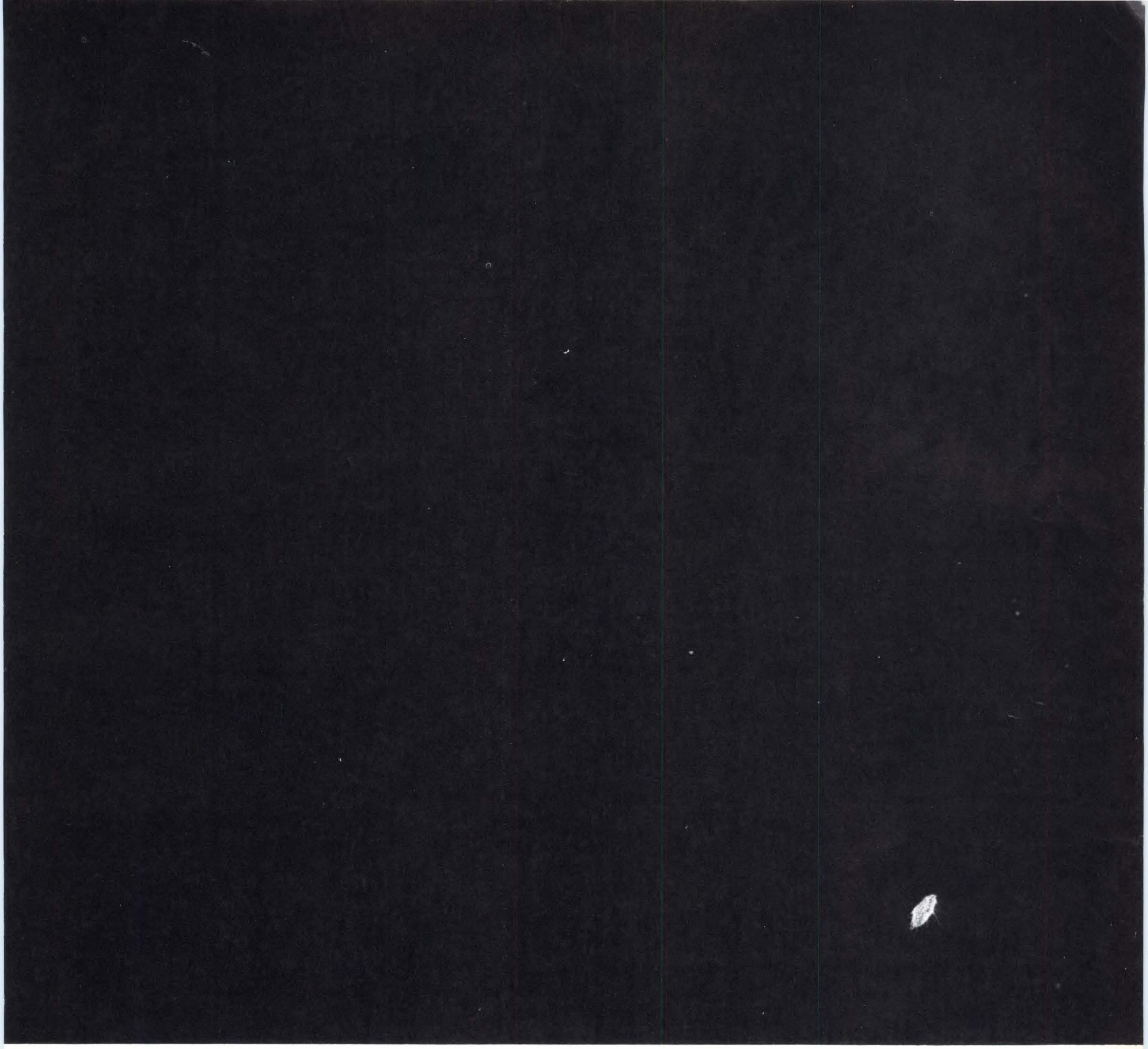
What's ahead in CCDs?

Two-dimensional arrays are now being made with 4-micron wide propagation gates using high-precision optical masking techniques. This procedure results in arrays measuring 16 microns (0.6 mil) per cell. Electron-beam fabrication techniques promise to do better. Lines of 0.5 to 1.0 micron are within the state-of-the-art, and the ultimate capability of E-beam fabrication is probably less than 0.1 micron. These methods may in time yield cell densities approaching 5×10^9 per square inch. As density rises, the cost-per-bit continues to drop. Right now, production estimates indicate a per-bit cost of about 0.05¢. Higher density devices will eventually be delivered for a fraction of that figure.

Author's biography



Dr. Barry T. French is presently group leader of the Special Programs Group, Research and Technology Division of North American Rockwell Electronics Group. Dr. French has a BA degree in liberal arts, a BS in physics and electronics from California State College at Long Beach, and an MA and a PhD in physics from the University of California at Riverside.



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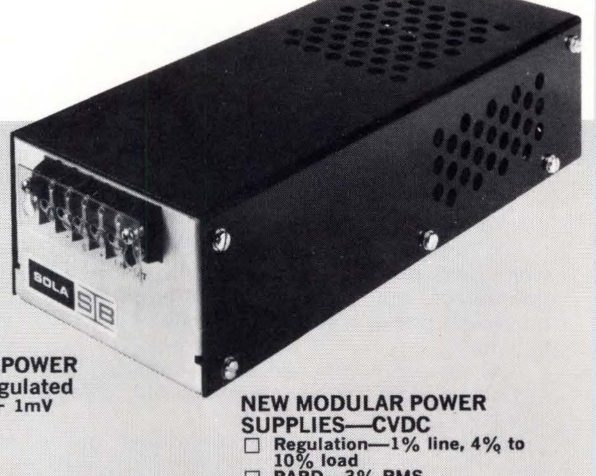
- ☐ Designed for both bench or rack



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Data-sheet dialogues

A chance for you, the reader, to speak out on what's right and wrong with data-sheet specifications.

Specifications and data sheets are as important to the designer as are the components and equipments they represent. Without them it would be impossible to pick and choose wisely from the myriad of similar items on the market today. But, as even the most novice engineer knows, the data sheets are not always what they could or should be. And as a result, countless engineering hours are wasted because of lack of needed data.

Are you one of those often confused by data-sheet specs? Do you feel that some data sheets are loaded with meaningless material and that the really important specs, the ones that will make or break your design, are not even mentioned? Well, here's your chance to sound off and help your fellow designers in the process.

EDN will run this year a series of Data Sheet Dialogues in which you — the data sheet user — can describe problems you've had and pitfalls you've encountered in specifying and designing from data sheets.

The purpose of these dialogues is to get your opinions on what's wrong (or right) with data-sheet specifying practices. In each Dialogue we will print a typical product data sheet that will be representative of other data sheets in that particular product area. Readers' responses — in the form of gripes, suggestions and praises — will be sorted out and published collectively in the next Dialogue, when a different data sheet will appear. We, the editors of EDN, will also include, where appropriate, our own observations gleaned from travels throughout the industry. Mainly, though, these will be dialogues between readers.

To start the series off, we are choosing a typical digital panel meter (DPM) data sheet. Let's hear from you on it. Remember, these Dialogues will only be as useful as you, the participants, make them.

Send your comments to:
EDN Data-Sheet Dialogue Editor
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MODEL XXXX ECONOMY DPM

This economy digital panel meter makes use of analog-type meters obsolete thanks to its low cost of under \$100 (for xx quantities). This 2½ digit instrument is low in cost mainly due to its simple input integration technique that requires very few components. Within the converter is a novel circuit that allows excellent common- and normal-mode rejection and a flutter-free readout.

A panel space of only x square inches is all that is needed for the Model XXXX meter, which mounts from the front of the panel. Servicing it is simple — just pull out the meter's entire chassis from the front. A circularly polarized filter is standard. Options include BCD output, remote hold and special captions.

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1. Top-value high-grade components.
2. Repairable pc boards.
3. Standard overrange of 25%.
4. Takes up less panel space than other DPMs —x square inches.
5. Can be removed completely and quickly, and even replaced with another chassis, in seconds, from the front.
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7. Front window is polarized.
8. Great noise rejection due to input integrator locking in on the line frequency.

SPECIFICATIONS

Ranges:

Volts	Input Resistance
0-199 millivolts	20K
0-1.99 volts	200K
0.19.9 volts	2 meg
0-199 volts	2 meg
001 kilovolts	2 meg
Current:	
0-19.9 microamps	10K
0-199 microamps	1K
0-1.99 milliamps	100 ohms
0-19.9 milliamps	10 ohms
0-199 milliamps	1 ohm

Accuracy:	±0.5% full scale ±1 digit, 25°C ±10°C.
Out-of-Range Indication:	Indicates when unit is below or above standard range.
Extreme Temp. Operating Range:	5°C to45°C
Storage Temp.:	−40°C to +70°C
CMR:	80 dB with 1000 ohm unbalance at 60 Hz
NMR:	35 DB at 60 Hz
Readings/Second:	10
Response Time:	Approximately 1 sec.
Power:	117 volt ±10%, 50 Hz to 400 Hz, about 5 watts
Weight:	Less than 1 lb. (430 grams)

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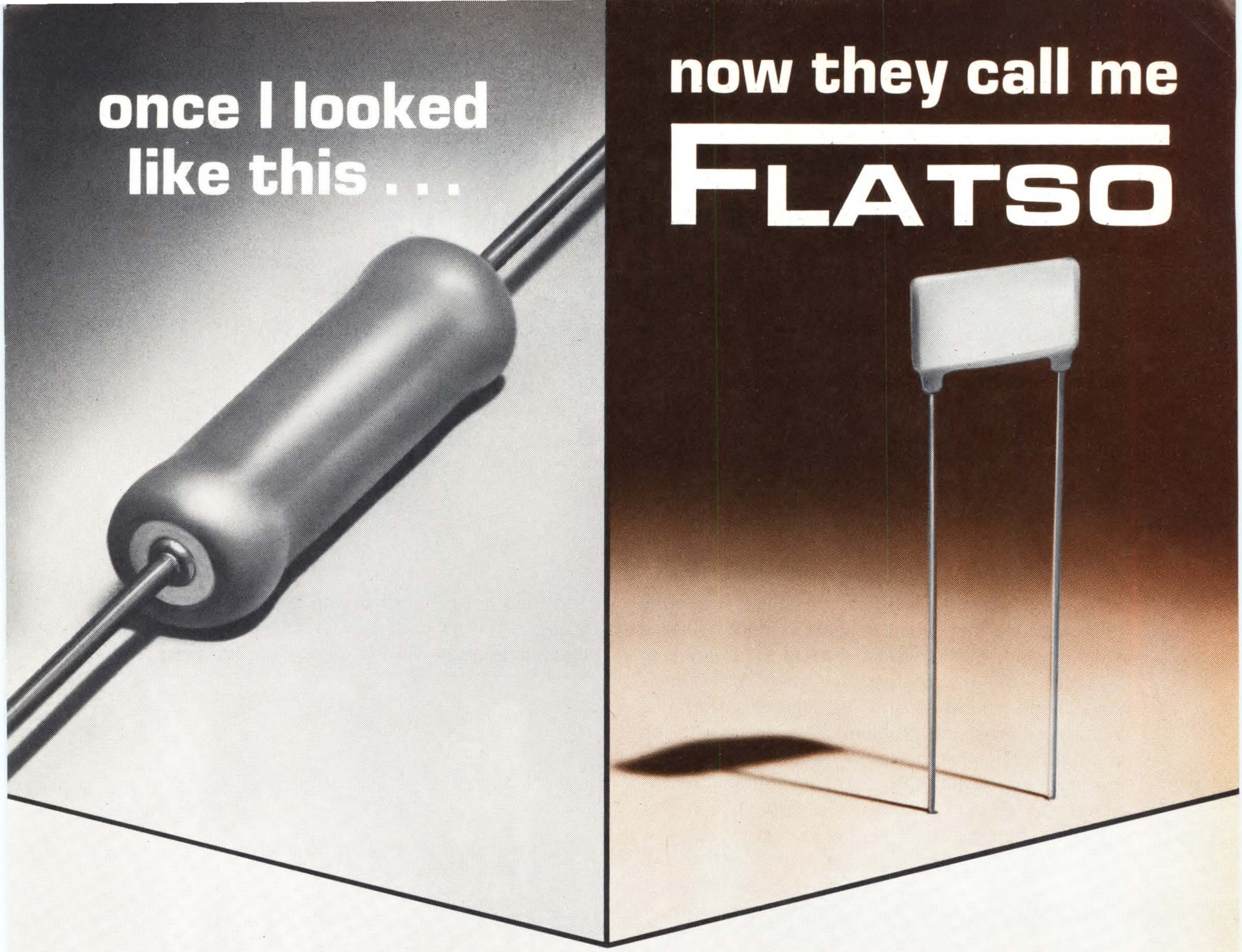

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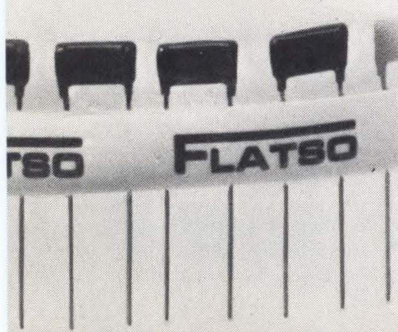
Tolerance: 1%, 2%, 5%, 10% standard
Power Rating: ¼, ½, 1 and 2 Watts
Operating Range: —55°C to +125°C
Temperature Coefficient: ±250 ppm/°C maximum



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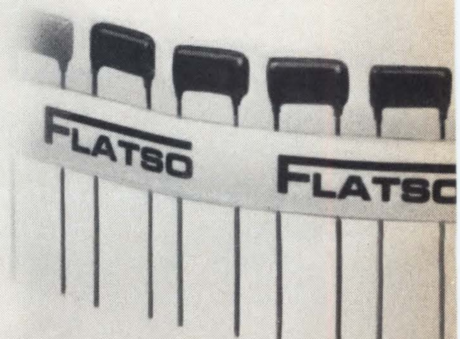
FL ¼	.300	.300	.100	350
FL ½	.525	.300	.125	750
FL 1	1.125	.375	.160	5,000
FL 2	2.125	.375	.175	10,000



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Keep up with the latest in engineering information

The explosive growth of technology is going to continue. But you can still keep current without spending an unreasonable amount of time.

Karen Takle Quinn, IBM Corp.

In his book *Science Since Babylon*, Derek J. de Solla Price reported that it had become evident by about 1830 that no scientist could read all the journals in his field of interest. At that time, some 300 journals were being published and the learned world was already experiencing problems with an information explosion. To solve the problem, the learned world invented a tool called the abstract journal. As the number of scientific journals grew through the years, so did the number of abstracting journals.

Today, it is estimated that there are more than two million scientific and technical papers published annually and over 1000 abstracting journals. In addition to journals and abstracting/indexing sources, there are also technical reports, reprints, preprints, cassette recordings, data bases on magnetic tapes, information analysis centers, information dissemination centers and libraries. All attempt to provide new or additional sources of scientific, technical, environmental and social information.

Since engineers, like scientists, build upon fundamental knowledge, along with the latest experimental laboratory techniques, an engineer must keep up with new technological advances. His slide rule, handbook and computer are necessary but incomplete tools for pursuing innovative work.

Being an updated rather than an outdated engineer means being familiar with the latest available sources of information and knowing how to use them properly. With technology rushing forward, engineers need to review their knowledge of the techniques of keeping current, since these techniques themselves can quickly become outdated. The purpose of this article is to provide such a review.

Communicate your information needs

Personal communication remains one of the most effective ways of keeping up with new developments. Reliance on engineering librarians or other specialists in the field of current information can open the door to a broad variety of information resources, such as published literature, data analysis centers and audio-visual educational aids. It should

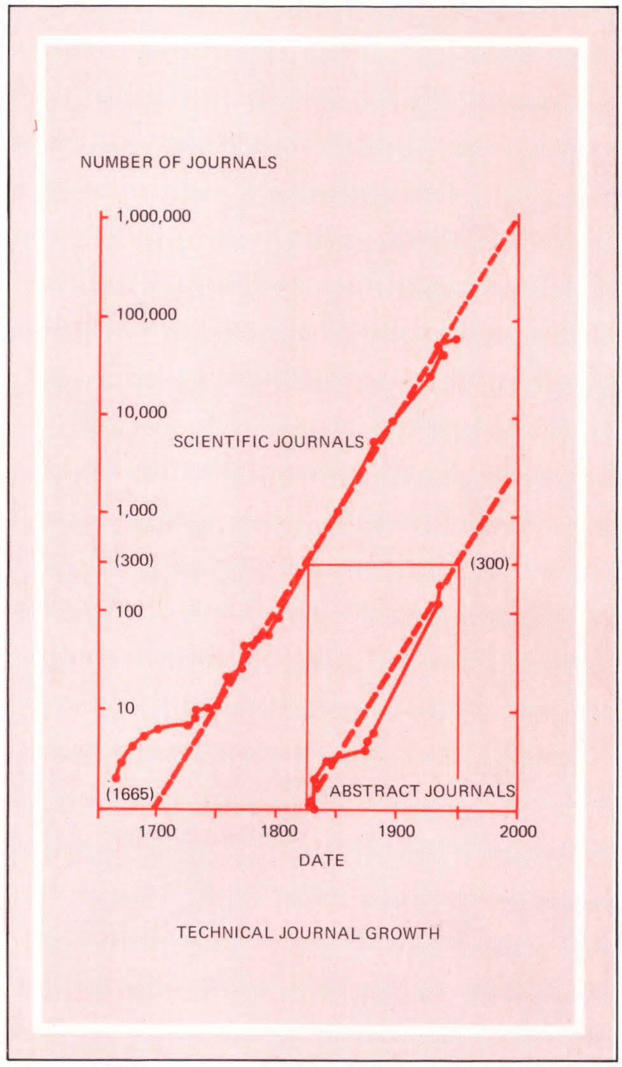
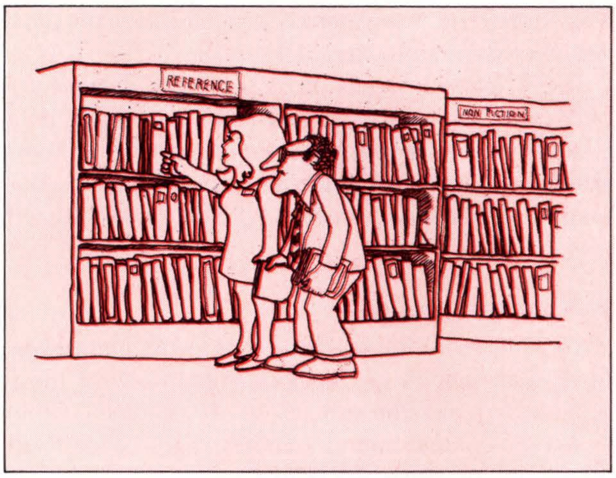


Fig. 1 — The explosive growth in the number of scientific and technical periodicals poses a severe "information" problem for the practicing engineer. (from Science Since Babylon, by Derek J. de Solla Price, Yale University Press, 1961)



Take advantage of librarians' know-how.

be noted, though, that there are inefficient ways of tapping the large information reservoirs a librarian can provide. An engineer accustomed to very specific answers to very specific questions in his specialized work can unwittingly fall into one of the most inefficient ways. He can become so impatient to have quick answers from information retrieval specialists that he blocks or avoids the back-and-forth communication needed to provide the answers.

Technical information-finding is a specialized field, like engineering. Communication of the problem at hand is a separate, initial step toward gaining information from a librarian. A question-answer session is often needed to define the question and the manner in which it can be answered. The answer may overlap several mission-oriented and discipline-oriented search tools. Both the engineer's and librarian's terminology are affected by rapid changes in technology, with new technologies appearing and sometimes dying quickly. Trying to find the latest information about these evasive subjects can be difficult. The search often takes time.

Defining a problem before talking with a librarian and considering different ways to explain it can help speed up communication. Using generally accepted terms and acronymns, along with alternate terminology when applicable, also help. Remember that to find answers to questions, a librarian must often take all of the following basic steps:

- Identify the user's need;
- Interpret questions;
- Identify concept and idea relationships;
- Establish vocabulary (synonyms and related terms);
- Structure the logic;
- Submit search;
- Review results;
- Review user's evaluation of the results.

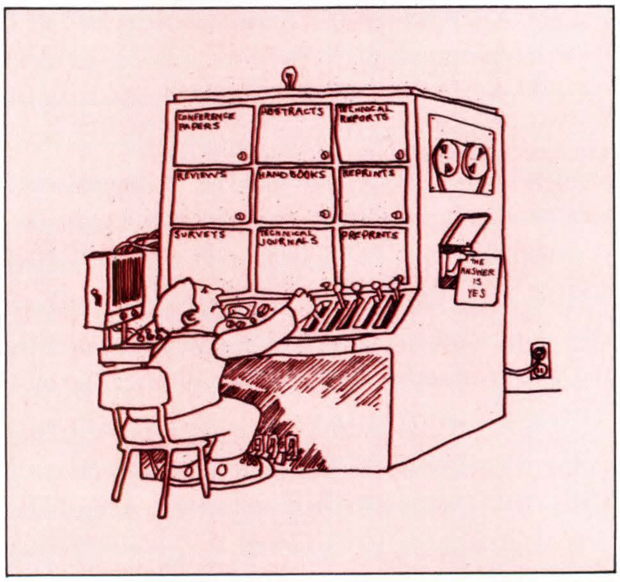
Attend meetings and symposia

There is no substitute for personal contact for keeping up with technology. As a result, conference meetings and symposia offer an excellent means for keeping up to date. More information often comes from casual conversations at these affairs than from formal papers. The formal meetings introduce the people who are making the decisions. The informal discussions often differ greatly from the formal papers, both in content and emphasis, and the give-and-take at the end of a talk will often clarify or crystallize an important point.

Read periodicals regularly

There is too much to read, but keeping up-to-date still requires reading. Selecting 7 to 12 periodicals for regular reading can provide an overview of a specialized field of interest and other related fields.

There are many newsletters and trade magazines. Their informative "half-life" content is short. A stack of magazines will not keep an engineer up-to-date, but reading them on a regular basis will. If some issues are missed because of a business trip or vacation, beginning with the new ones after the absence is advisable. Keeping current means developing the



Use computerized services.

habit of looking at new technology when it is announced.

Selection of periodicals should achieve the dual purpose of keeping up-to-date in a specialized field *and* related fields. Since science and technology are related, developments in the aerospace industry are often applicable to material science, electronics, medicine and mechanical areas.

Read abstract services

Indexing and abstracting services offer another valuable method for keeping up-to-date. If an engineer reads an abstracting service covering the literature of a particular field, he is actually reviewing the literature from several hundred journals. And the literature reflects the developments in the field.

Abstracting services systematically organize the technical literature within disciplines. Many engineers employed by industrial firms have access to internal or commercially-available computerized information services. Others can refer to abstracting services related to their interests. Reviewing an abstracting service on a regular basis can help to keep an engineer informed on recently indexed material. Abstracts will not provide the complete story, but they are a good basis for selecting articles to be read.

Computerized current-awareness services, frequently called SDI (Selected Dissemination of Information), automatically select abstracts or citations from new inputs for users based on interest profiles. The 1972 Engineering Index catalog lists five agencies providing such customized services from COMPENDEX tapes. Sixteen information service centers presently utilize COMPENDEX (Engineering Index) tapes for SDI and searching. When the company affiliations of the authors are indicated within the citation, reprints can be requested. Otherwise, most technical libraries are able to provide copies of requested material in their collections or from other library collections.

In addition to the current awareness capabilities of abstract services, most can be used effectively for retrospective searches and state-of-the-art searches through their cumulative indexes. Computerized searches can be performed on an increasing number of scientific, social, economic and technical data bases. A state-of-the-art search is a good starting point for any project, job or career assignment. Again, this provides a review of past developments and changing technologies which allows a forecast of the future.

The more familiar an engineer is with indexing terminology and its organization, the more efficient these tools become. When requesting a machine search, he will be more familiar with the data base being searched and can better communicate good search logic terminology to a librarian.

Use computerized services

Computerized information centers have grown as rapidly as the scientific journal. ASIDC (Association of Scientific Information Dissemination Center) reports that there are more than 200 data bases available to selected information users. ASIDC recently published a "Survey of Information Center Services" which lists 65 centers offering SDI and retrospective searching capabilities. The survey includes a description of available data bases, along with format options and service costs for each center.

Computerized SDI services are reported in this survey to cost $100-$300 a year, per data base per profile. This is a low price tag for keeping up-to-date. One industrial firm has realized a 94.5% savings in its current awareness program through utilization of a computerized SDI service.[1]

The Science Information Association is presently offering on-line retrieval services for multiple data bases from remote terminals. As the number of computerized data bases increases, so will service bureaus and data service centers with their personalized services.

Follow the reviews

Technical disciplines frequently lend themselves to annual reviews of developments. Many of these appear as magazine articles or as chapters within books or separate bound volumes, often called "Advances in" or "Annual Review".

These reviews as well as annual technical conferences offer very good roundups of developments in a particular field. It is possible for an engineer who uses his intuition to read between the lines and predict, from looking at the past, time frames of future advances. Technological forecasting can be enhanced through analysis of a good review of a particular field.

Investigate guides to literature

In addition to the specialized resources already described, many local libraries have copies of "Guides to Literature" prepared by members of the Engineering School Libraries Division of the American Society for Engineering Education. These guides are 10 to 25 pages long. They list key references, including indexing and abstracting services, bibliographies, yearbooks and surveys, serials, encyclopedias, biographical directories, standards, handbooks and specialized information centers. There are presently fifteen guides available, including:

- Aerospace engineering
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- Bioengineering
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- Computers
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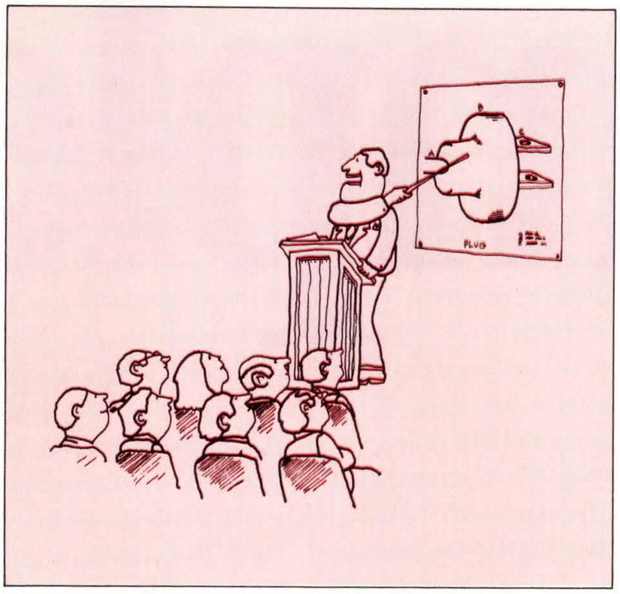

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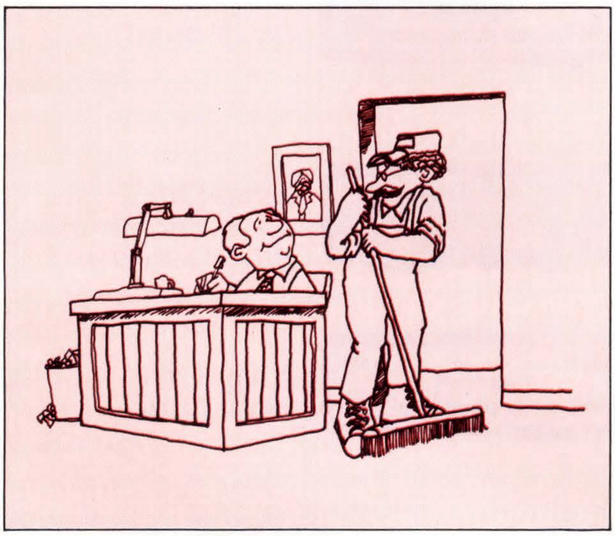

Know company information flow.

gineering societies provide reprint services in hard copy and microfiche formats.

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Know your company

Last, but not least, engineers should be aware of the processes by which information is communicated within their own companies. These include the formal flow process, such as bulletin board notices, company newspapers, company memoranda and reports, as well as the informal flow processes, which are usually relaxed personal contact in which technical and company information is exchanged. Being aware of these patterns and being able to evaluate the relative significance of the information they offer can make the difference between being a progressive member of the firm or an out-of-date office fixture.

Richard S. Rosenbloom and Francis W. Wolek from their survey of technology and information transfer in industrial organizations point out that "If information flow and/or transfer is inefficient, then R &D is inefficient and organizational ability to respond to technological progress is inadequate. This statement applies to the professional ability of individuals as well as companies. ▭

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Author's biography

Karen Takle Quinn is senior librarian at IBM's General Products Div. Library in San Jose, CA. She is also the west coast representative for IBM's Technical Information Retrieval Center. Prior to her 7 years with IBM, Karen held positions of assistant professor, engineering librarian and consultant for the Ford Foundation. Karen holds a BS degree from the Univ. of Wisconsin and an MS in Library Service from Rutgers University.

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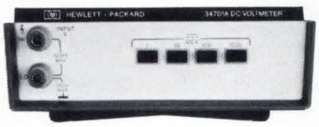

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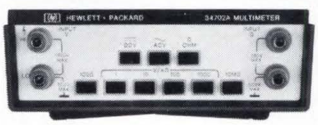

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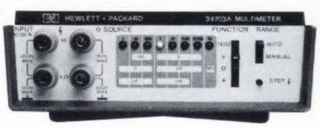

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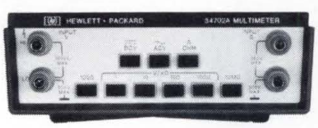

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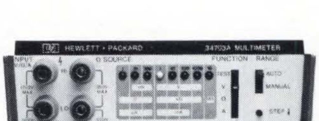

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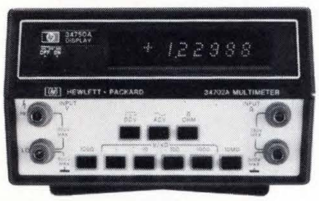

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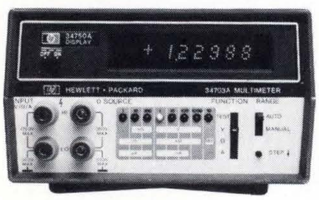

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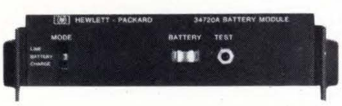

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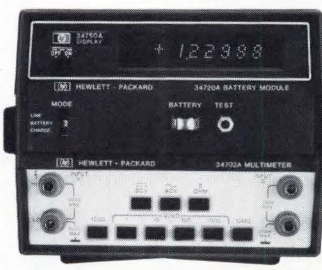

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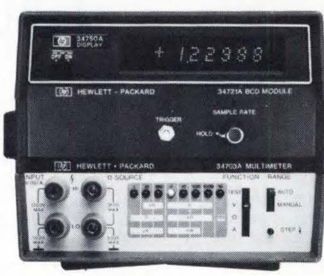

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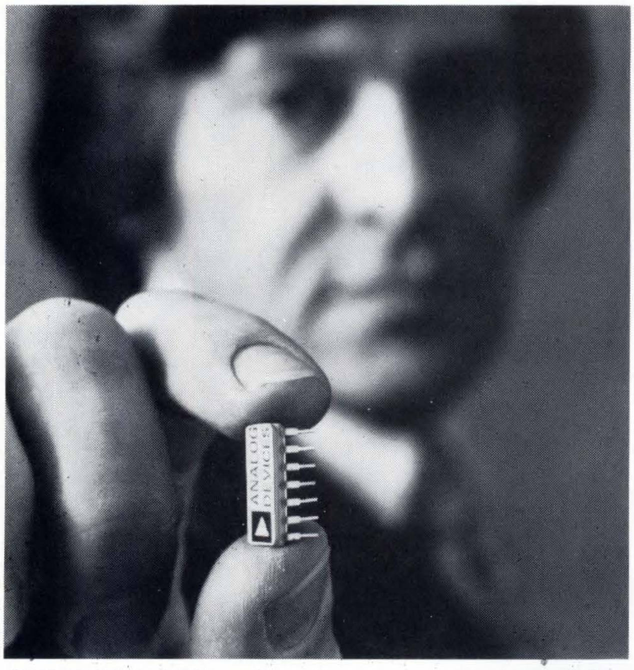

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The advent of low-cost op amps has led to an increasing use of precision logarithmic amplifiers to perform many electronic functions, including the generation of arbitrary functions and the compression and expansion of signals having a wide dynamic range.[1] These amplifiers use the nonlinear I-V relationship of semiconductor p-n junctions. Their output voltages are logarithmic functions of the input voltages, where the use of a diode or a transistor as a feedback element in the op amp circuit provides for logarithmic amplification.

It is well-known that the transfer conductance of a diffused silicon transistor is by far the best exponential feedback element for a precision logarithmic amplifier circuit.[2,3] Indeed, well defined operation over 9 decades (diodes are useful over approximately 6 decades) is not uncommon. In practice, the limiting factor on performance is due to errors associated with the implementation circuitry. A basic understanding of these error sources is necessary to realize the full potential of the logging transistor characteristics.

Fig. 1 shows the basic implementation of a logarithmic amplifier circuit. The ideal functional relationship between input and output is given by

$$V_o = -\alpha \log_e (I_1/I_s) \tag{1a}$$

or

$$V_o = -\alpha \log_e \left(\frac{V_1}{R\, I_s}\right) \tag{1b}$$

where

$\alpha = kT/q$
k = Boltzmann's constant = 1.380×10^{-23} joules/°K
q = charge of an electron = 1.6×10^{-19} coulomb
T = absolute temperature, °K
I_s = emitter saturation current

The components R_o and C_o are used to stabilize the circuit[3,4] and do not affect the dc characteristics

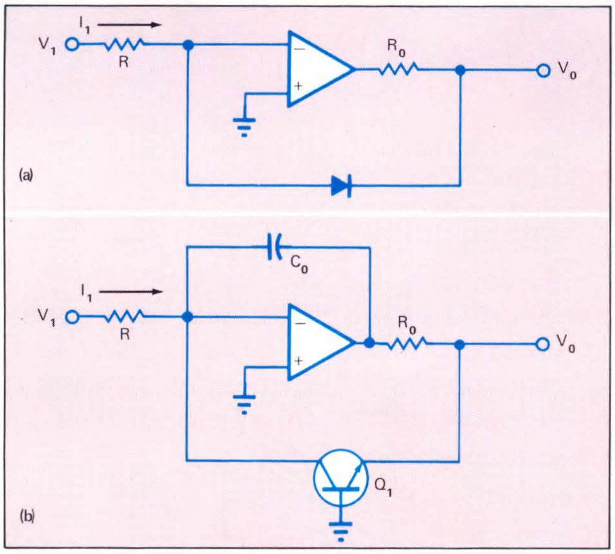

Fig. 1 – Two basic logarithmic amplifier circuit configurations. The top circuit uses a diode as the exponential feedback element and is generally useful over approximately 6 decades. The use of a transistor for the feedback element, as shown in the bottom circuit, increases this to 9 decades of amplifier operation.

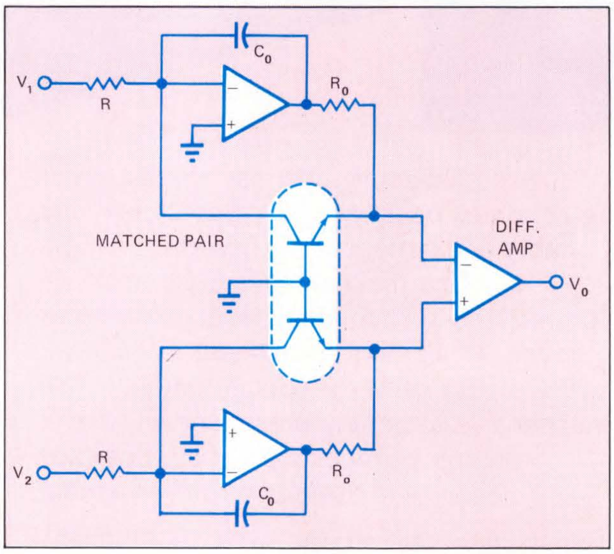

Fig. 2 – To cancel out emitter saturation current for a transistor feedback element in a logarithmic amplifier, matched differential transistor pairs are used. A transistor's emitter saturation current is very dependent on temperature and doubles for approximately every 10°C.

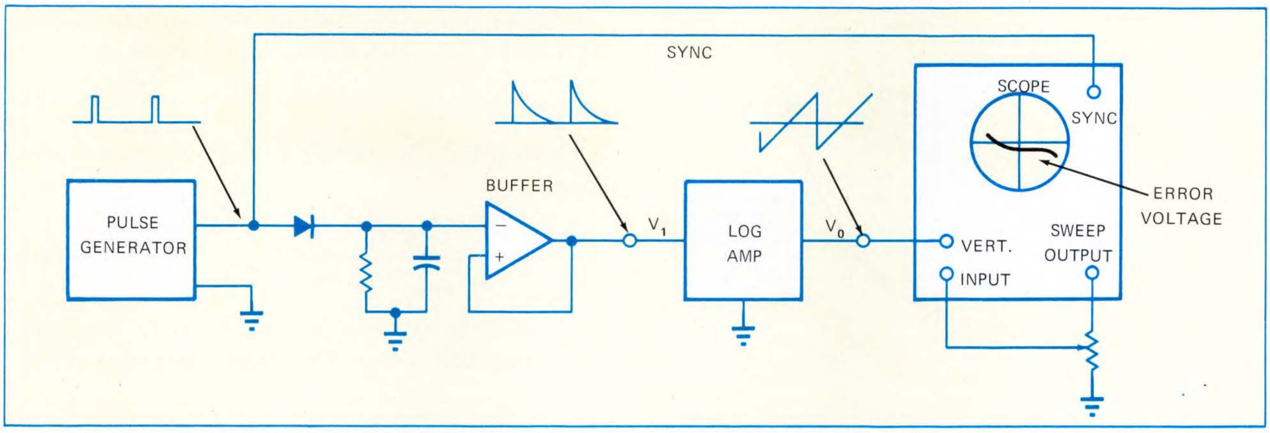

Fig. 3—To measure the feedback transistor's error effects in a logarithmic amplifier, use this circuit arrangement. The exponential decay of an RC network is used as an input to the logarithmic amplifier. The ideal output is then a linear sweep. A portion of the sweep output of the oscilloscope is used to balance out the linear component of the logarithmic amplifier output and the error voltage is then viewed directly on the scope as a function of the amplifier's input level. This measurement is related to the actual normalized fractional input error by **Eq. (6).**

given by **Eq. (1)**. The gain constant α is proportional to absolute temperature and is equal to about 26 mV at room temperature. The emitter saturation current I_s is very temperature dependent (it doubles about every 10°C) and varies from transistor to transistor. For this reason, these circuits are usually used in differential pairs with matched transistors in order to cancel out the I_s term.[1,4,5,6]

One possible matched-transistor configuration is shown in **Fig. 2**. For this arrangement, the output is given by

$$\begin{aligned} V_o &= \alpha \log_e(I_1/I_{s1}) - \alpha \log_e(I_2/I_{s2}) \\ &= \alpha \log_e(I_1/I_2) + \alpha \log_e(I_{s2}/I_{s1}) \end{aligned} \quad \textbf{(2)}$$

If I_{s1} and I_{s2} are perfectly matched and track with temperature, then the second term in **(2)** vanishes and

$$V_o = \alpha \log_e (I_1/I_2) \quad \textbf{(3)}$$

Error analysis

In practice, several important effects cause deviations with the ideal behavior given by **Eq. (1)**. Temperature variations of the parameters in **Eq. (1)** have already been mentioned. Another source of error is the bias current and offset voltage drift of the op amp used. These anamolies directly affect the input current and give rise to a normalized input error of

$$\epsilon_1 = \frac{\Delta V_1}{V_1} = \frac{\Delta V_{offset} + R\,\Delta I_{bias}}{V_1} \quad \textbf{(4)}$$

where V_{offset} and I_{bias} are the offset voltage and bias current variations over the design temperature range, respectively. This expression assumes that V_{offset} and I_{bias} have been trimmed to zero at some nominal temperature. As can be seen, this type of error increases at low input levels.

At high input levels, the bulk semiconductor junction resistance r_b limits the useful range. This term reduces the intrinsic base-emitter junction voltage at high currents and its effect is described by modifying **Eq. (1a)** to read

$$V_o = -\alpha \log_e (I_1/I_s) - r_b I_1 \quad \textbf{(5)}$$

An output error term, ΔV_o, can be referenced to the input by the relationship

$$\frac{\Delta V_1}{V_1} \cong \frac{\Delta V_0}{V_1}\frac{dV_1}{dV_0} \cong -\frac{\Delta V_0}{\alpha} \quad \textbf{(6)}$$

By substituting the output error term of **Eq. (5)** into **Eq. (6)**, the high-level input error can be written

$$\epsilon_2 = I_1 r_b/\alpha = V_1 r_b/\alpha R \quad \textbf{(7)}$$

In contrast to **Eq. (4)**, this type of error increases with input level. Actual error measurements are most conveniently accomplished by the arrangement shown in **Fig. 3**. An actual error curve for a typical transistor is shown in the solid line of **Fig. 5**. This corresponds to a bulk resistance of about 7.5Ω, although the actual effect is somewhat nonlinear.

Dynamic range

For low input levels, the bias current and offset

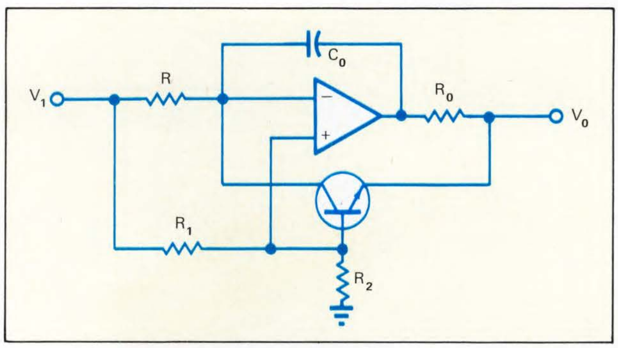

Fig. 4—To control transistor bulk junction resistance, r_b, this modified logarithmic amplifier circuit can be useful. A portion of the input via R_1 and R_2 is substituted for the ground reference and is used to cancel the V_1r_b/R error term. R_1 and R_2 can be chosen such that this error term can be substantially reduced as indicated by **Eq. (12).**

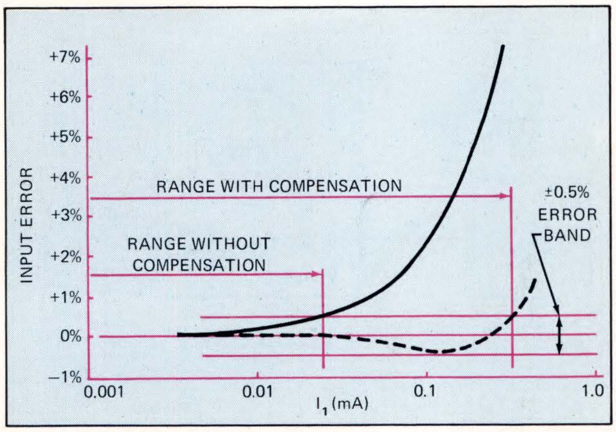

Fig. 5 — Junction bulk resistance error characteristics of a typical transistor. Although the actual error effect is somewhat nonlinear, the bulk resistance here corresponds to about 7.5Ω.

voltage drift of the op amp determine the minimum input for a given accuracy requirement and temperature range. For a given error specification, ϵ, the minimum input is given by **Eq. (4)** as

$$V_{1_{min}} = \frac{\Delta V_{offset} + R\,\Delta I_{bias}}{\epsilon} \qquad \textbf{(8)}$$

At high input levels, the bulk resistance error term given by **Eq. (7)** limits the maximum input to

$$V_{1_{max}} = \epsilon R\alpha / r_b \qquad \textbf{(9)}$$

Combining **Eq. (8)** and **(9)** then gives the dynamic range

$$\frac{V_{1_{max}}}{V_{1_{min}}} = \frac{\alpha R / r_b}{\Delta V_{offset} + R\,\Delta I_{bias}}\,\epsilon^2 \qquad \textbf{(10)}$$

Thus, the dynamic range is proportional to the square of the tolerable error. This expression also shows that for

$$R >> \frac{\Delta V_{offset}}{\Delta I_{bias}}$$

the maximum dynamic range is achieved; however, this condition usually leads to unreasonably high input voltage levels.

Error control

Errors due to the mismatch of I_{s1} and I_{s2} can be minimized by using matched transistor pairs that track closely in temperature. Excellent performance may be realized by using the Fairchild μA726 tem-

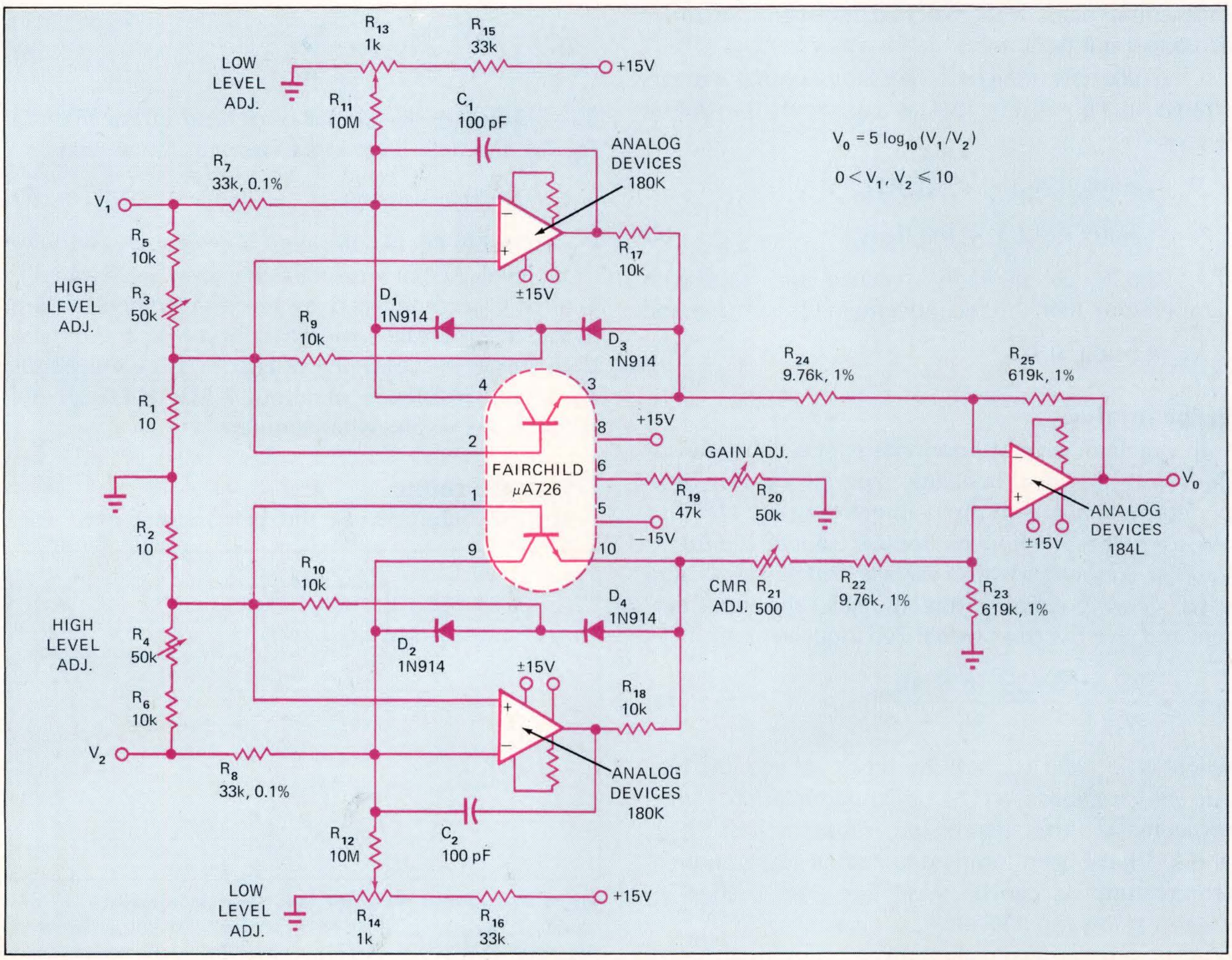

Fig. 6 — Get the most precision and the largest dynamic range from a logarithmic ratio circuit with this configuration. The differential feedback element is a Fairchild μA726 transistor pair which has excellent low differential voltage drift of only 0.2 μV/°C. The transistor's chip is temperature regulated at +125°C. Low-drift op amps also reduce temperature drift.

perature regulated differential pair. This component also has the effect of stabilizing the gain coefficient α. Typical units are specified at 0.2 μV/°C differential voltage drift at a regulated chip temperature of 125°C. Using **Eq. (6)**, this drift corresponds to a normalized input error of

$$\frac{0.2\ \mu V/°C}{35\ mV} = 0.00057\%/°C$$

Therefore, the maximum input error over a 100°C temperature range due to this effect is only about 0.06%.

Low-level errors due to op amp offset voltage and bias current are more difficult to control. Bipolar op amps are available with very low offset voltage drifts but have moderately high offset current drift. On the other hand, FET op amps have low bias current drift but suffer from high offset voltage drift. Chopper stabilized op amps have much lower drift but are limited in bandwidth. In addition, any chopper noise will result in a dc error since the logarithmic amplifier is a nonlinear device. All things considered, a premium bipolar op amp, such as the Analog Devices Model 180K, is probably a good choice. It has a specified offset voltage drift of 0.5 μV/°C and offset current drift of 0.02 nA/°C.

High-level errors due to the bulk junction resistance can be controlled by modifying the circuit of **Fig. 1b** as indicated in **Fig. 4**. A portion of the input via R_1 and R_2 is substituted for the ground reference and is used to cancel the $V_1 r_b/R$ error term. If R_2 is small so that loading is negligible, then the transfer function is accordingly modified to

$$V_o = -\alpha \log_e \left(\frac{V_1}{R\ I_s}\right) + \left(\frac{R_2}{R_1 + R_2} - \frac{r_b}{R}\right) V_1 \qquad \textbf{(11)}$$

If R_1 and R_2 are chosen such that

$$\frac{R_2}{R_1 + R_2} = \frac{r_b}{R} \qquad \textbf{(12)}$$

then the error term is completely cancelled out. In practice, a complete cancellation is not possible since the bulk resistance effect is slightly nonlinear. However, a substantial improvement can still be realized in this manner.

An actual error curve achieved by this method is shown by the dotted line in **Fig. 5**, and is compared with the uncompensated error. As can be seen, a substantial improvement in range is realized. For example, with a ±0.5% error specification, more than an order of magnitude of increased range is achieved by compensation.

A complete circuit

A logarithmic ratio circuit using the techniques described here is shown in **Fig. 6**. Each input is connected to a modified logarithmic amplifier circuit and the outputs are combined by a differential amplifier. A Fairchild μA726 temperature regulated dual transistor is used for the feedback element.

In the upper circuit, R_1, R_3 and R_5 provide the compensation voltage for bulk resistance effects. Resistors R_{11}, R_{13} and R_{15} provide an offset current compensation at low input levels. The network composed of R_9, D_1 and D_3 forms a clamp for negative inputs.

The gain of the differential amplifier is chosen such that the output is ideally,

$$V_o = 5 \log_{10} (V_1/V_2).$$

This expression assumes a gain constant of $\alpha = 35$ mV which corresponds to a chip temperature of 125°C for the μA726. A trimmer, R_{20}, is provided to adjust the gain to this value by varying the control temperature. Trimmer R_{21} is used to balance the differential amplifier and hence maximize the common-mode rejection ratio (CMRR).

In addition to the use of a temperature regulated feedback element, low-drift op amps are used to reduce temperature drift. □

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Author's biography

Dennis Morgan is a senior engineer with the Electronics Laboratory of General Electric Co., where he has been employed for seven years. Dennis received a BSEE from the Univ. of Cincinnati and an MSEE and PhD from Syracuse Univ.

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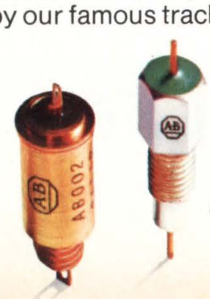
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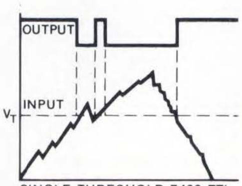

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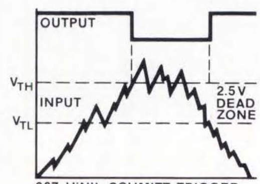

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What do you know about selecting an LED readout?

Once you've decided to use an LED display, you may think your readout decisions are over. They're not. You still have to pick the right LED unit.

Sanford Roth, Dialight Corp.

Proper selection and application of the readout device can play a critical role in the success of an equipment or system design, whether it be a large million dollar system or a simple $200 instrument. And many factors enter into the decision on just what is the best readout in a given circumstance.

Suppose, though, that you've decided that a light-emitting diode (LED) readout is best for your application. How do you choose the type that is most suitable. There are many kinds available; and although they all have most of the same basic solid-state characteristics that led you to use a LED readout in the first place, there are differences between them—some being obvious and others subtle. These differences must be known and carefully considered if the best possible selection is to be made.

Some basic facts

Presently, LED readouts are available in three common versions: a 7-segment display, a 5 × 7 dot matrix, and a 4 × 7 dot matrix. The 7-segment display produces any digit from 0 through 9. The 5 × 7 dot matrix is an alphanumeric readout that provides any letter of the alphabet or any digit from 0 to 9 and the 4 × 7 dot matrix is a hexadecimal readout that provides letters A through F of the alphabet, any digit from 0 to 9 and a decimal.

LEDs are basically monochromatic light sources that provide a glow in only one color. At present they are available in red, green or yellow, but current technology can't produce green or yellow with good efficiencies. Consequently, the cost of LEDs in these colors is high, making them impractical for

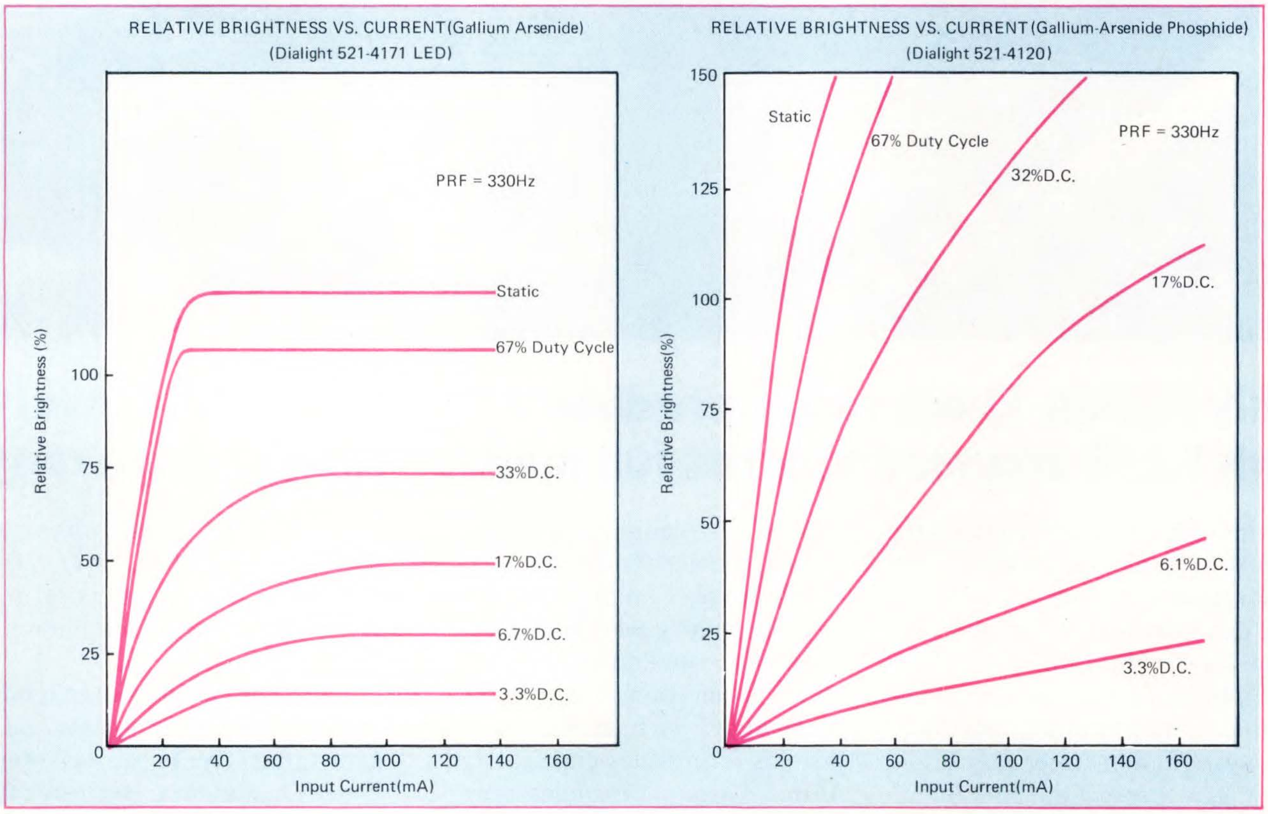


Fig. 1—Gallium-phosphide LEDs saturate at relatively low values of input current (a). Gallium-arsenide phosphide LEDs, on the other hand, deliver a light output that continues to increase with increasing input current (b). As a result, multiplexing which require high pulse current levels can be accomplished with gallium-arsenide phosphide types.

many applications. Thus, it's safe to say that for most practical applications LEDs are available in any color as long as it is red.

In addition to configuration and color, LED readouts come in various sizes. These range from a low of 0.125 in. to about 0.625 in. in height.

Can you read the number?

Before a readout can be of any value to the viewer, he must first be able to see it. Size, brightness and contrast are the most important factors that affect such readability. In essence, the bigger and brighter a display, the more easily it can be seen.

There are many ways in which a brightness measurement can be performed. Unfortunately, no standard has yet been established in the industry for brightness in the visible spectrum.

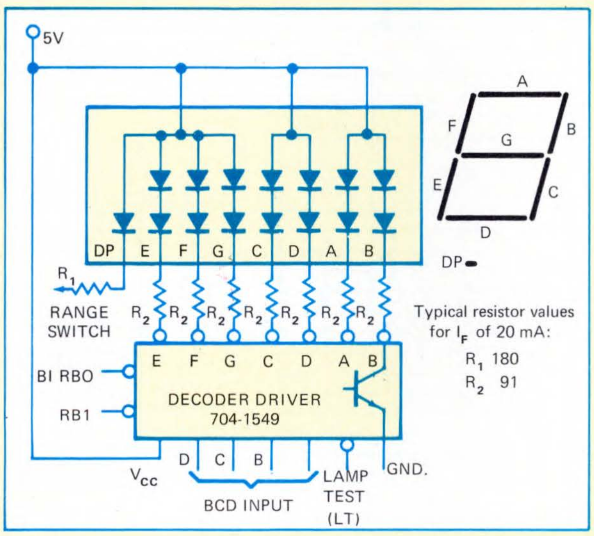
In measuring brightness, the concern is with that portion of the electromagnetic spectrum in which the wavelength of radiation lies between 4×10^{-7} and 7×10^{-7} meters, or 400 to 700 nm. Photometers that measure foot-lamberts (fL) include a color filter that shapes the response to approximate that of the human eye, which is greatest at 555 nm, corresponding to green in wavelength. The response curve of the eye falls to nearly zero at the extreme wavelengths.

Brightness, or luminance as it is sometimes called, is specified in units of fL, which is based on the input current to the LED. Efficiency can be defined as a function of radiated energy at a particular wavelength for a given input electrical energy. However, a more practical unit is fL per mA.

Unfortunately, the fL is a measure of light intensity at a point-source; therefore, the brightness will vary at different distances from the point-source to the area illuminated.

Another way that brightness can be measured is in candelas. Here, the measurement of light is taken over a unit area. Since the brightness is considered uniform over the unit area, the light intensity level could be a smaller number than with the fL, but it will also be more accurate. Milli-candelas per sq cm or milli-candelas per sq ft are the usual practical units.

A quick comparison of the literature available from the different manufacturers shows that each company puts his LEDs in the best light by specifying those parameters that give the highest number. For example, some LED readouts exhibit a brightness that varies markedly from point to point. In these cases, averaging the luminance (in candelas) would give a fairer description than would the commonly specified peak luminance in fL. Similarly, if extremely high luminance occurs over a very narrow segment



Truth Table								
Decimal or function	Inputs						BI/RBO†	NOTE
	LT	RBI	D	C	B	A		
0	H	H	L	L	L	L	H	1
1	H	X	L	L	L	H	H	1
2	H	X	L	L	H	L	H	1
3	H	X	L	L	H	H	H	1
4	H	X	L	H	L	L	H	1
5	H	X	L	H	L	H	H	1
6	H	X	L	H	H	L	H	1
7	H	X	L	H	H	H	H	1
8	H	X	H	L	L	L	H	1
9	H	X	H	L	L	H	H	1
10	H	X	H	L	H	L	H	1
11	H	X	H	L	H	H	H	1
12	H	X	H	H	L	L	H	1
13	H	X	H	H	L	H	H	1
14	H	X	H	H	H	L	H	1
15	H	X	H	H	H	H	H	1
BI	X	X	X	X	X	X	L	2
RBI	H	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	4

H = high level (logical 1 in positive logic), L = low level (logical 0 in positive logic), X = irrelevant.

†BI/RBO is wire-AND logic serving as blanking input (BI) and / or ripple-blanking output (RBO).

NOTE:

1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of any other input.
3. When the ripple blanking input (RBI) and inputs A, B, C, and D are at low logic level with the lamp test input high, all segment outputs are off and the ripple-blanking output (RBO) of the decoder goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segments are illuminated.

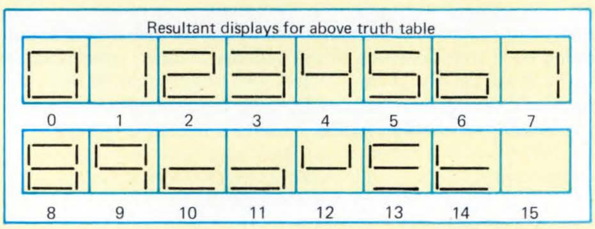
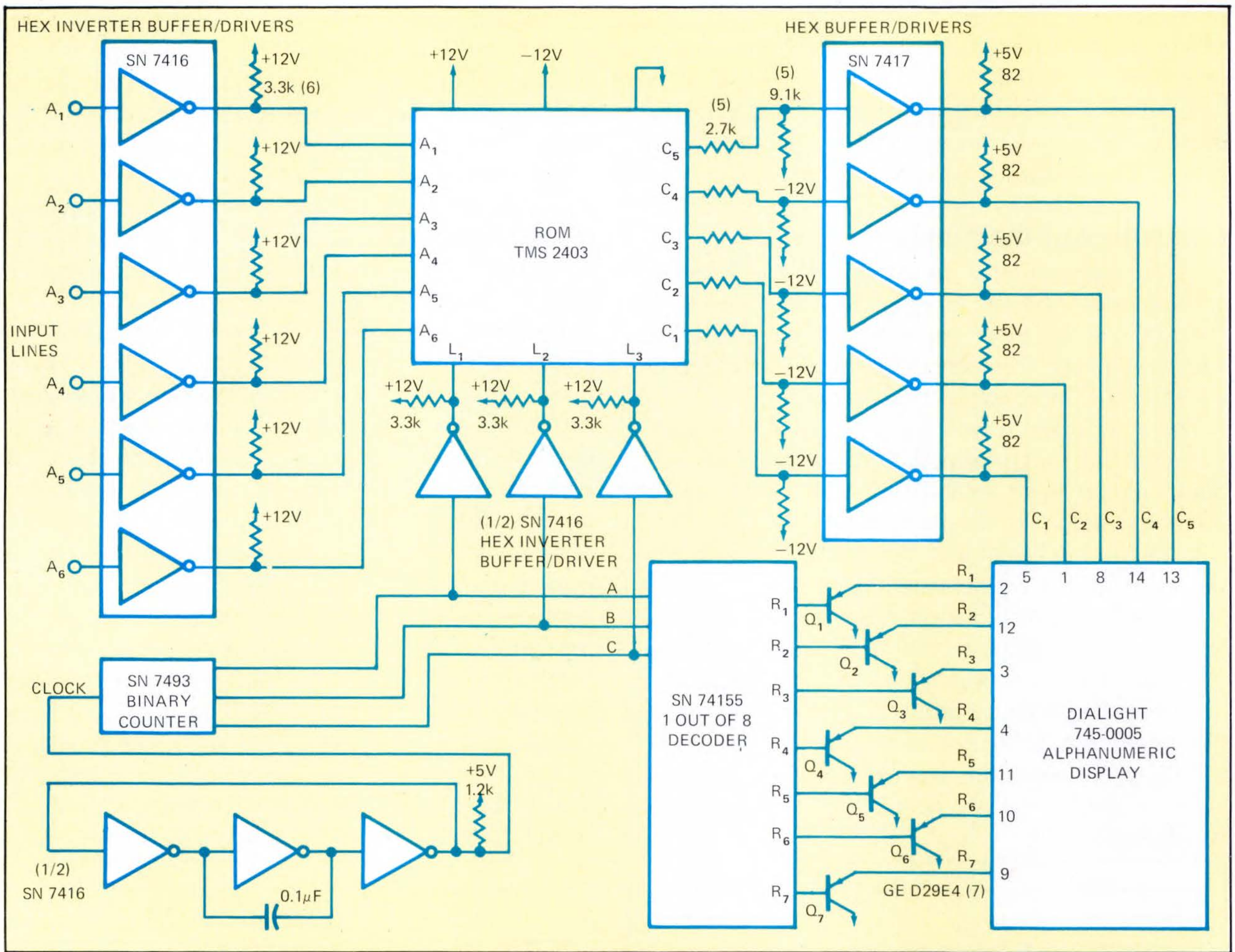
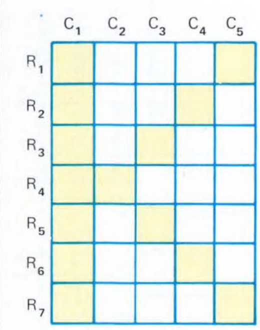


Fig. 2—Readout assemblies like this 5 × 7 dot-matrix alphanumeric unit can be purchased complete with all necessary circuitry, as shown. Or the designer can buy the basic readout and provide his own electronics.



A_6	A_5	A_4	A_3	A_2	A_1	Resultant Display	A_6	A_5	A_4	A_3	A_2	A_1	Resultant Display	A_6	A_5	A_4	A_3	A_2	A_1	Resultant Display
0	0	0	0	0	0	@	0	1	0	1	1	0	V	1	0	1	1	0	0	,
0	0	0	0	0	1	A	0	1	0	1	1	1	W	1	0	1	1	0	1	-
0	0	0	0	1	0	B	0	1	1	0	0	0	X	1	0	1	1	1	0	.
0	0	0	0	1	1	C	0	1	1	0	0	1	Y	1	0	1	1	1	1	/
0	0	0	1	0	0	D	0	1	1	0	0	1	Z	1	1	0	0	0	0	ϕ
0	0	0	1	0	1	E	0	1	1	0	1	1	[	1	1	0	0	0	1	1
0	0	0	1	1	0	F	0	1	1	1	0	0	\	1	1	0	0	1	0	2
0	0	0	1	1	1	G	0	1	1	1	0	1	]	1	1	0	0	1	1	3
0	0	1	0	0	0	H	0	1	1	1	1	0	⌢	1	1	0	1	0	0	4
0	0	1	0	0	1	I	0	1	1	1	1	1	–	1	1	0	1	0	1	5
0	0	1	0	1	0	J	1	0	0	0	0	0		1	1	0	1	1	0	6
0	0	1	0	1	1	K	1	0	0	0	0	1	!	1	1	0	1	1	1	7
0	0	1	1	0	0	L	1	0	0	0	1	0	"	1	1	1	0	0	0	8
0	0	1	1	0	1	M	1	0	0	0	1	1	#	1	1	1	0	0	1	9
0	0	1	1	1	0	N	1	0	0	1	0	0	$	1	1	1	0	1	0	:
0	0	1	1	1	1	O	1	0	0	1	0	1	%	1	1	1	0	1	1	;
0	1	0	0	0	0	P	1	0	0	1	1	0	&	1	1	1	1	0	0	<
0	1	0	0	0	1	Q	1	0	0	1	1	1	'	1	1	1	1	0	1	=
0	1	0	0	1	0	R	1	0	1	0	0	0	(	1	1	1	1	1	0	>
0	1	0	0	1	1	S	1	0	1	0	0	1	)	1	1	1	1	1	1	?
0	1	0	1	0	0	T	1	0	1	0	1	0	*							
0	1	0	1	0	1	U	1	0	1	0	1	1	+							



The character displayed by this alphanumeric display is a function of six input lines A_1 through A_6. The seven rows of the 5 × 7 dot matrix are scanned sequentially one at a time. The timing is controlled by the clock which drives a binary counter, whose outputs ABC control the row to be selected. This ensures that the read-only memory's (ROM) five outputs C_1 – C_5 correspond to the row of dots which are enabled by the 1-out-of-8 decoder. The SN74155 is a dual 2-to-4 line decoder, used here as a 1-out-of-8 decoder.

For example, let's assume that the letter K is to be displayed. K in a 5 × 7 array of dots looks as depicted in b. The ASC11 code $A_1 - A_6$ for selecting K is 001011. The SN7416 inverter buffer/drivers and the SN7417 buffer/driver are used to interface the inputs and outputs of the ROM. The binary counter's outputs ABC continuously cycle from 000 to 111 and back to 000. When ABC equals 000, the ROM outputs C_1 and C_5 will be HIGH and C_2, C_3 and C_4 will be LOW, as shown in b. Simultaneously the 1-out-of-8 decoder drives Q_1 ON, and this enables the first and fifth dots of the first row to be illuminated. On the next clock pulse, the counter advances to .001. C_1 and C_4 will become HIGH, and Q_2 will be driven ON thereby illuminating the first and fourth dots of the second row. This process is continued and repeated rapidly, so that the final result appears to be the letter K.

The 745-0005 in conjunction with any suitable ASC11 ROM will display 64 alphanumeric characters. These are shown in c as a function of the six bit inputs $A_1 - A_6$.

Fig. 3—7-segment readouts of this type are available in sizes up to 0.625 in. in height. The readout is made up of an array of diodes whose light is diffused by seven segmented shaped lenses.

width, the peak luminance reading may not provide a fair comparison.

In addition to brightness, contrast is also an important parameter that affects readability. It relates to the different luminances between the readout character and its background. Contrast diminishes with increased ambient light levels; it is increased by surface treatment to reduce reflection and glare, and by other techniques such as circularly polarized filters and color filtering.

There is also a distinct difference in brightness between LED readouts of different manufacturers. This is caused by the different materials used and the way in which they are placed. Some of them have bright spots in the individual segments of a readout and these can make for uncomfortable viewing and an unattractive display.

Readability is also dependent on such factors as the distance the viewer is from the readout, the brightness of the digits and the width of the bar in a 7-segment display. If the bar is too narrow, the viewer could see an astigmatic distortion in the line, making it difficult to read. It will also be uncomfortable for the viewer to look at this type of image for too long a period.

What about power requirements?

Light-emitting diodes operate from a current rather than from a voltage. To be compatible with IC circuits where 5V is available, series, current limiting resistors must be used to meet the operating voltages of 1.8 to 2.2V for the diodes. The operating current for an LED is usually specified as so many mA per segment. For example, in Dialight's 739 series readouts (0.625 in. character heights) gallium-phosphide lamps are used that require 15 mA per segment. These offer fairly good efficiency as compared with LEDs made from gallium-arsendide phosphide, which use about 27 mA per segment.

Although gallium phosphide is a more efficient material than gallium-arsenide phosphide, requiring less power for the same light output, gallium phosphide saturates at a low-current level while gallium-arsenide phosphide does not (**Fig. 1**). Thus, multiplexing (or strobing) which requires high pulse current levels to maintain brightness, can be accomplished only with gallium-arsenide phosphide. This is an important tradeoff that the designer must take into consideration.

Multiplexing cuts the costs of drive circuitry by using common electronics for a number of readout characters. It also reduces the amount of current required to drive these units. But you can't multiplex gallium phosphide without a large loss of light output. No matter how much more current you put through it after saturation, the LED is not going to put out any more light.

By strobing gallium-arsenide phosphide, you pump in more power and get out more light. In a 10-digit assembly, for example, the unit can be multiplexed at a 10% duty cycle. This means that for 10% of the time power is applied to each digit. However, six is the recommended maximum number of digits for multiplexing.

The make or buy decision

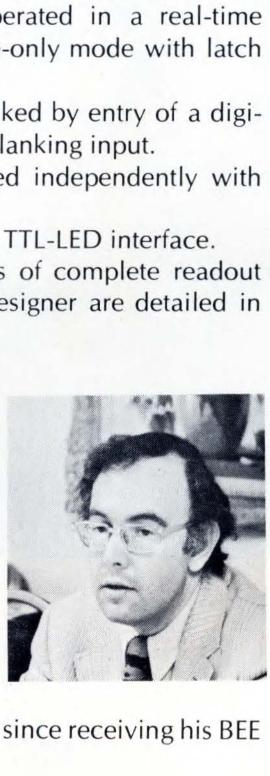
Even after a specific type of LED is decided upon, a choice must be made on whether to buy just the readout and design your own circuitry (driving, decoding, etc.) or to buy a complete readout assembly that includes circuitry. Most engineers like to design their own circuits, which makes sense when the quantities involved or unusual circuit considerations justify it. However, there are many types of complete readout assemblies available off-the-shelf capable of satisfying a wide variety of applications. Assemblies specifically tailored to a customer's needs are also available from various manufacturers. All the user has to do in his equipment is allow for a specific sized readout assembly and wire the output of his circuit to the decoder-driver. This approach can often save both time and money.

Some of the features available in these complete displays are:

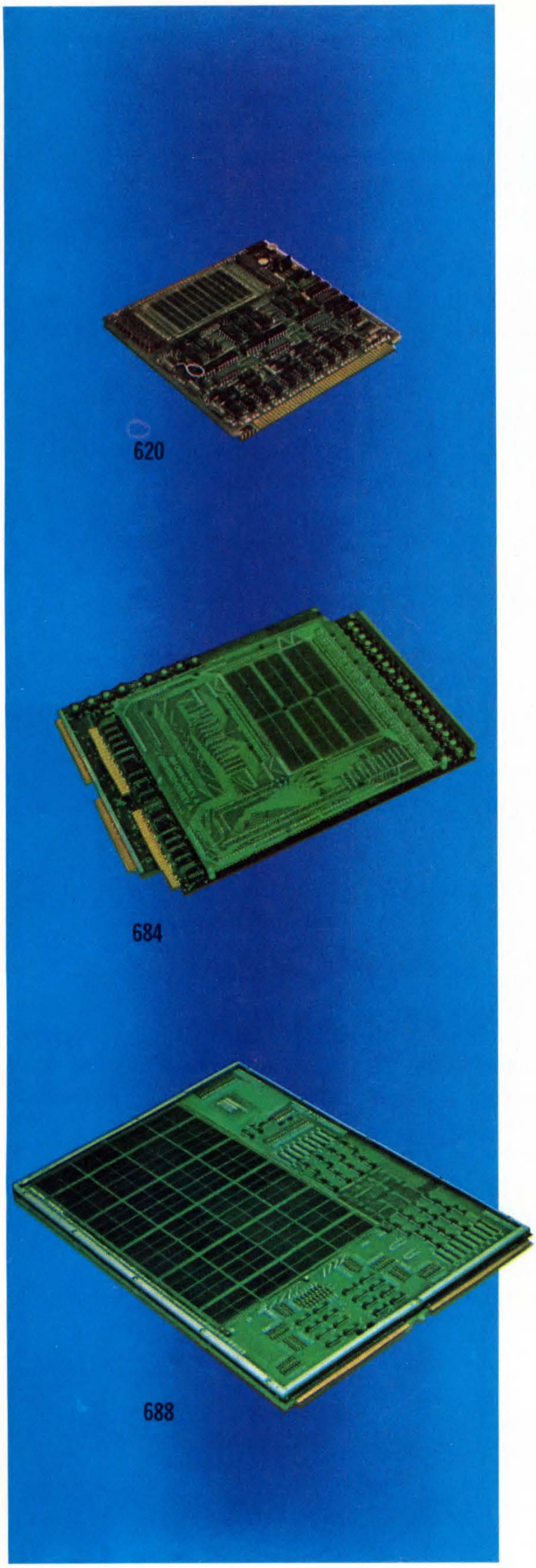
- Latched BCD and decimal-point logic outputs to drive logic processors simultaneously with the displayed data.
- Overriding blanking for suppressing of the entire display or for pulse-modulation of LED brightness.
- A LED test input for simultaneously turning on all display segments and decimal point.
- Capability of being operated in a real-time mode or latched-update-only mode with latch strobe input.
- Capability of being blanked by entry of a digital code or by use of a blanking input.
- Decimal point controlled independently with decimal-point latch.
- Constant-current-source TTL-LED interface.

Two examples of the types of complete readout assemblies available to the designer are detailed in **Fig. 2** and **3**. ▭

Author's biography



Sanford Roth is product marketing manager for Dialight Corp., Inc., Brooklyn, NY. He is responsible for marketing and business development for all new Dialight products and their applications. Prior to going to Dialight one year ago, Roth spent 20 years as an engineer and marketing consultant since receiving his BEE from NYU.



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CHECK NO. 42

Variable limit switch permits hands-off equipment cycling

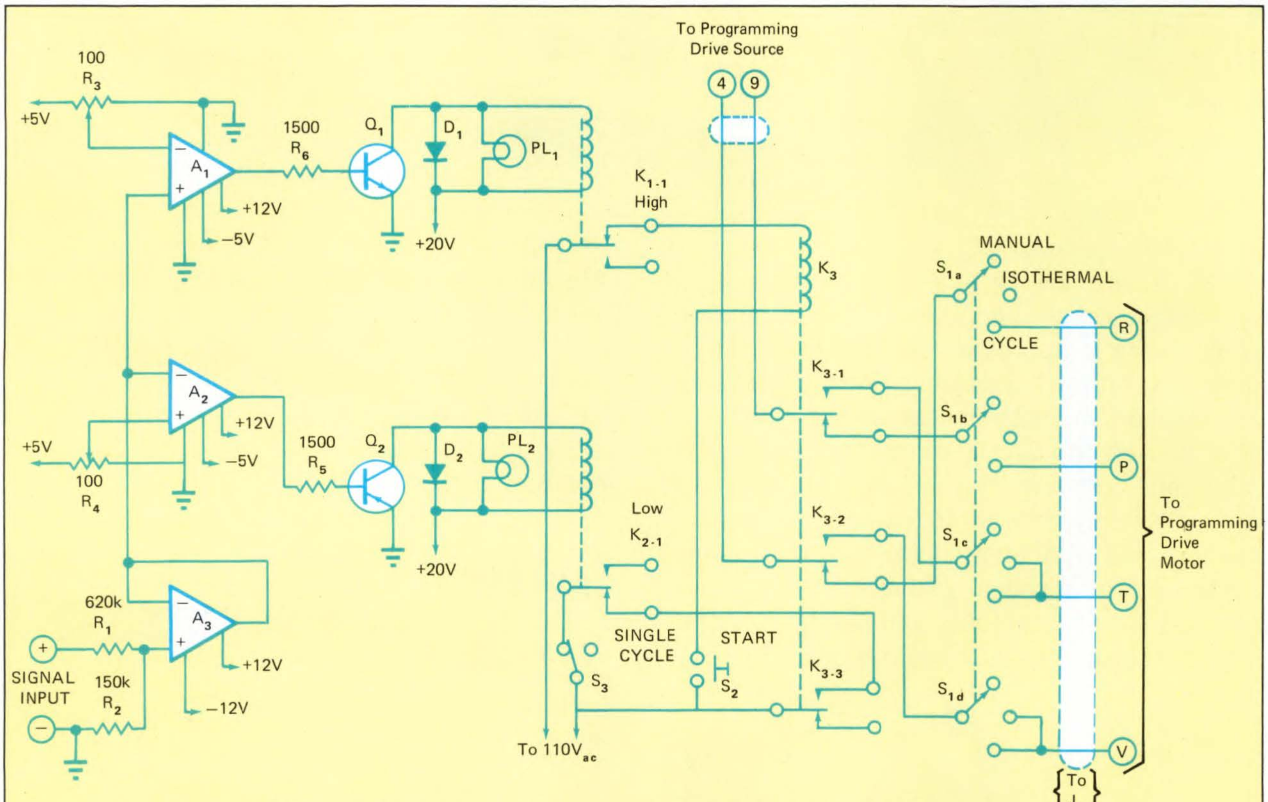
By including end-point detection directly into the controller, continuous cycling operations are more convenient and efficient.

William J. Dobbin, IBM Electronics Systems Center

In the operation of thermal-scanning instruments, many instances occur when it would be desirable to let equipment run unattended. However, the operator must be present at some point to recycle the program (for instance, a maximum temperature limit on the material under investigation). This is especially true in the case of thermal-mechanical experiments where the effect of continuous thermal cycling on material properties is required. While timers can be used to alert the operator, it would be more convenient and efficient to incorporate end point detection directly into the temperature programmer.

Following is a system that permits the operator to pre-select the upper and lower temperature limits for a program. Included is a switching arrangement which allows for any one of several modes, ranging from manual operation to fully-automatic continuous cycling.

While the circuit was specifically designed for a temperature programmer with an output that varies from 0 to +24V dc, it may be readily adapted to other instruments where the output voltage variation is greater than 5V dc. In most cases, the only change required will be in the input resistor network (R_1 and



A_1,A_2 - Voltage Comparator, UA710
A_3 - Semiconductor, HA2602
Q_1,Q_2 - NPN Transistor, 2N2222 or Equivalent
D_1,D_2 - Diodes, 1N4148 or Equivalent
K_1,K_2 - DPDT Relays, 24Vdc Coil
K_3 - 3 PDT Relay, 110Vac Coil

S_1 - 4 Pole - 3 Position Rotary Switch
S_2 - SPST N.O. Momentary Contact Switch
S_3 - SPST Toggle Switch
PL_1,PL_2 - 10V, 14 m Pilot Lights
R_3,R_4 - 100Ω, 10-Turn, Wire-Wound Potentiometers

Fig.—Variable upper and lower limit switch is programmable for four different operating cycles.

R_2 in figure). The wiring and parts placement is not critical, and familiarity with basic electronic circuitry wiring techniques is the only prerequisite to successful assembly.

How the circuit works

The operation of the programming drive motor is controlled by the position of the contacts of relay K_3. When this relay is energized, the motor is driven in a forward direction (increasing temperature); when it is de-energized, the motor is reversed. The condition of K_3 is determined by which of the two limit relays K_1 or K_2 has been most recently activated; energizing K_1 opens the coil circuit of K_3 while energizing K_2 closes it. Relay contact K_{3-3} acts as a " latching" switch—once the programming motor relay circuit has been changed by either of the limit relays, only the other limit relay can affect a change back to the original condition.

Rotary switch S_1 selects the mode of operation. In the "Isothermal" position, the down drive of the programming motor is disabled; in the "Manual" position, both up and down drives are disconnected from automatic control. In the "Cycle" position, both up and down drives are operative. Switch S_3, when turned to "Single Cycle," disables contacts K_{2-1}. In this mode, the low limit is inoperative and the programmer will decrease until its lower stop is reached. Momentary contact switch, S_2, is included to start the cycle.

The high and low limit relays are energized by a control circuit which samples the output of the temperature programmer. The dc input signal is reduced to a 5V maximum by the voltage divider network (R_1-R_2). After passing through the voltage follower A_3, the signal is impressed on both A_1 and A_2, the high and low limit voltage comparators respectively. In these two amplifiers, the input signal level is compared to a reference voltage set by the operator. This voltage is continuously variable from 0 to 5V and is pre-selected by the adjustment of the 10-turn potentiometers R_3 and R_4.

Following the signal through A_1, the high limit amplifier; as long as the input signal level is below the reference voltage, there is no output from the amplifier and transistor Q_1 remains cut off. When the input signal level equals or exceeds the reference voltage, the output of A_1 becomes positive and base current (limited by R_6) flows through A_1. The transistor goes into saturation and the collector current energizes upper-limit relay K_1. The action of the low-limit circuit is similar except that relay K_2 is energized when the input signal level is equal to or less than the reference voltage.

Indicator lamps PL_1 and PL_2 are lit when the relays are energized. They are used in setting the limit potentiometers. Diodes D_1 and D_2 are included to protect the transistors from the back EMF when the respective inductive circuits are opened.

The entire controller is powered by a 32V dc power supply and draws 250 mA.

Setting the cycle

In setting the high- and low-limit potentiometers, switch S_1 is turned to "Manual" and the temperature programmer turned to the highest temperature desired. R_3 is turned until pilot light PL_1 is extinguished, and then slowly backed-off until the light glows. This procedure is repeated using R_4, PL_2 and the programmer set at the low temperature of the cycle. The thermal profile desired is selected through switches S_1 and S_3. The operating modes available are as follows:

- Manual—The limit switch is deactivated and complete control of the programmer is returned to the operator.
- Isothermal—The instrument temperature is programmed up to a pre-selected upper limit and left at this temperature until manually changed.
- Single Cycle—The instrument is programmed up to the upper limit, then programmed down to the lower stop of the programmer and left at this point until manually changed.
- Cycle—The instrument is continuously programmed between the upper and lower limits until the cycle is interrupted manually.

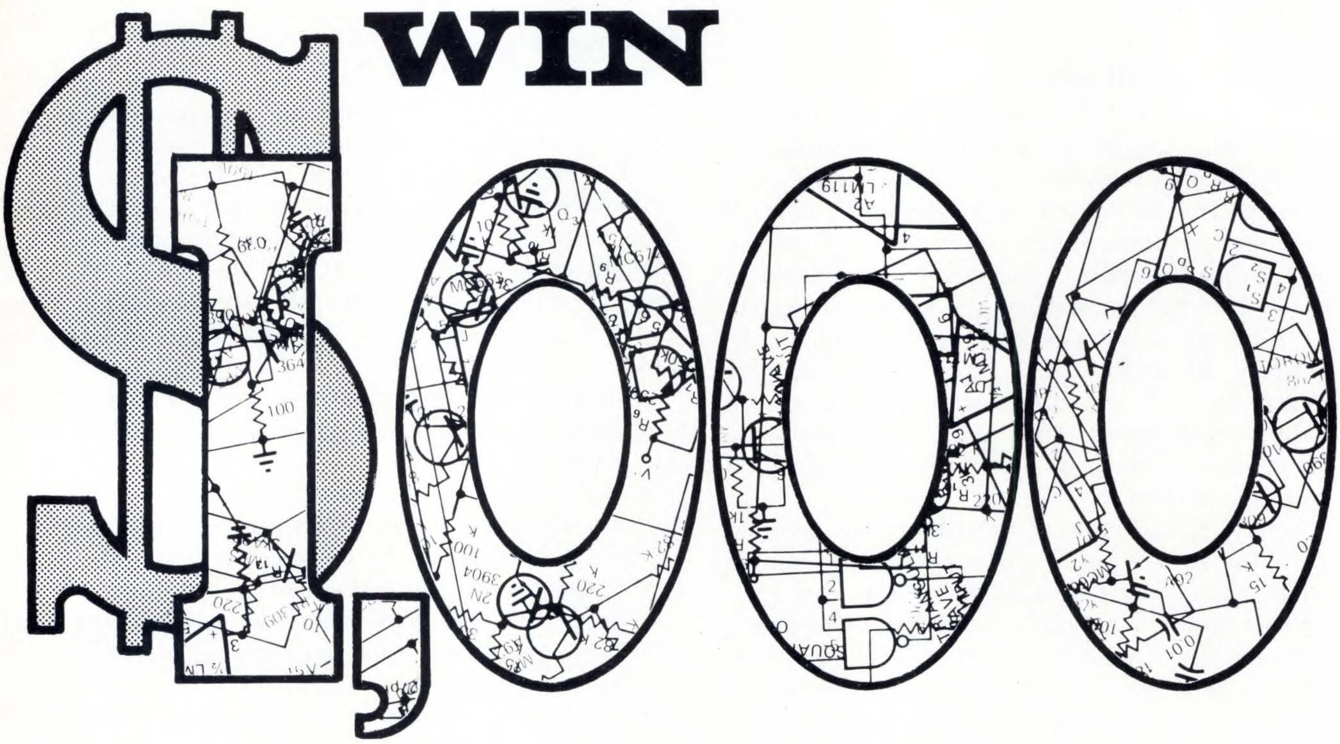
After all adjustments are made, switch S_2 is closed to start the cycle.

It should be noted that while the input impedance of the controller is high, it cannot be assumed that the original temperature programming characteristics are unchanged. While temperature calibration of thermal equipment is routine, it is stressed that the temperature response should be checked with the controller attached.

Finally, the operation of the limit switch is responsive to the voltage output of the programmer and not the temperature of the sample. It is left to the operator to ascertain that the sample temperature is tracking the program temperature through all parts of the cycle where data is required. □

Author's biography

William J. Dobbin is an advisory chemist at the IBM Owego, NY plant and is Coordinator, Analytical Chemistry Group, Materials Engineering. He received his BSChE from Columbia Univ.



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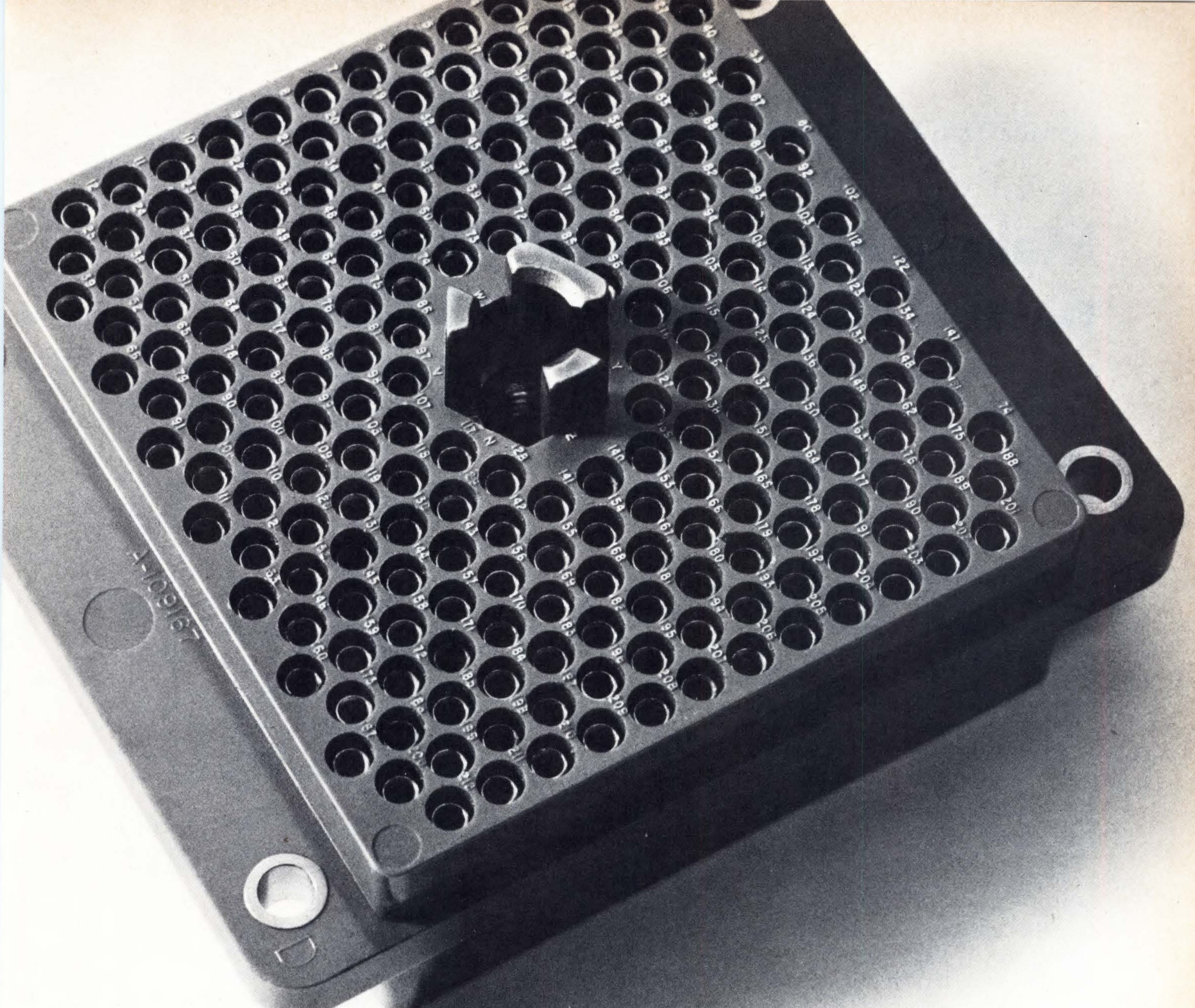

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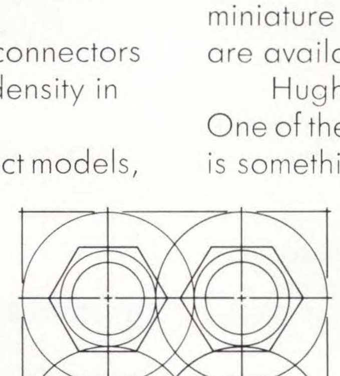

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CHECK NO. 44

Make sure your logic keeps pace with memory cycle times

Now that SC memory speeds are approaching those of today's CPUs, *newer and faster CPUs and control logic are needed. ECL does the trick.*

Dick Brunner, Motorola, Inc.

Memories in present and past computers for the most part have been extremely slow compared with the logic used in the central processor (CPU). However, with the advent of semiconductor memories, the memory speed is approaching that of the CPUs of present-day computers. In order to take advantage of these high-speed semiconductor memories, future CPUs and memory control logic will most likely employ high-speed current-mode logic, such as the MECL 10,000 Series.

Large-scale dynamic MOS memories for mainframe memory have been the first to evolve due to their low power, small size and speed. This article describes the design of a 4k word by 18-bit memory system that is expandable in 4k-word segments. An 1103-type memory (1k-word by 1-bit dynamic MOS) makes up the memory portion of the system, and emitter coupled logic (MECL 10,000 Series) is used to generate the timing and control signals necessary to operate the memory.

The storage building block

A brief description of the operation of the 1103-type memory should be helpful in understanding what control logic is needed to operate and interface the memory with the CPU.

The basic memory device contains 1024 bits of storage organized in a square matrix of 32 rows by 32 columns, together with logic for decoding and gating (**Fig. 1**). The basic storage cell, which consists of three transistors, stores data on the gate capacitance, C, of Q_2. Since data storage is done on this gate capacitance, additional circuitry is required to keep these capacitors charged. The operation of the memory will be explained with the aid of the timing diagram given in **Fig. 2.**

During the time precharge is low, one row is selected by the row decoder. When C enable (chip enable) goes low, all 32 memory cells of the selected row send their data through the read transistor, Q_3, to their respective column refresh buffers. The refresh buffers are also connected to 32 column read/write buffers.

When precharge returns high, the data stored in the 32 refresh buffers is returned to the cells of the selected row by way of write transistor, Q_1, and the dynamic column address decoder selects one column buffer.

At the end of t_{po}, the selected column read/write buffer output is valid. If new data is desired, the read/write amplifier is placed in the write mode at the end of t_{pw}. In the write mode, the new data present on the column input overrides the data previously stored on Q_2. At the end of C enable, Q_1 is turned off and the data is held on the gate of Q_2.

Since the memory cell is a charge-storage type, charge will leak off of the gate of Q_2 over a period of time, and the stored data will be lost. Therefore, the cell must be periodically recharged to retain the data. To insure that data is not lost, the entire memory must be refreshed at least once every 2 msec. In order to reduce the amount of time spent refreshing, the memory is organized so that all 32 memory cells in a row are refreshed during one read cycle. Therefore, only 32 refresh cycles are required every 2 msec to completely refresh the whole memory. This means that a refresh cycle must be initiated every 62.4 μsec, which represents less than 1% of the total available cycle time when the memory is operated at maximum frequency.

Organizing the memory system

The memory system consists of one control card and as many memory cards as are required to give the desired word capacity. The control card generates all of the timing signals to operate the memory, as shown in **Fig. 2.** Additional logic is contained on the card to generate and keep track of refresh cycles,

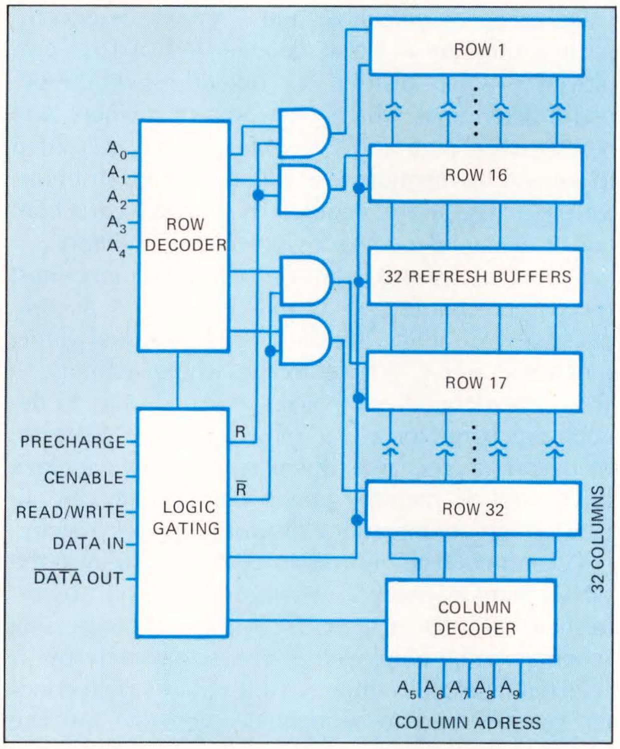


Fig. 1—The dynamic MOS 1k RAM, is organized in a matrix of 32 rows × 32 columns.

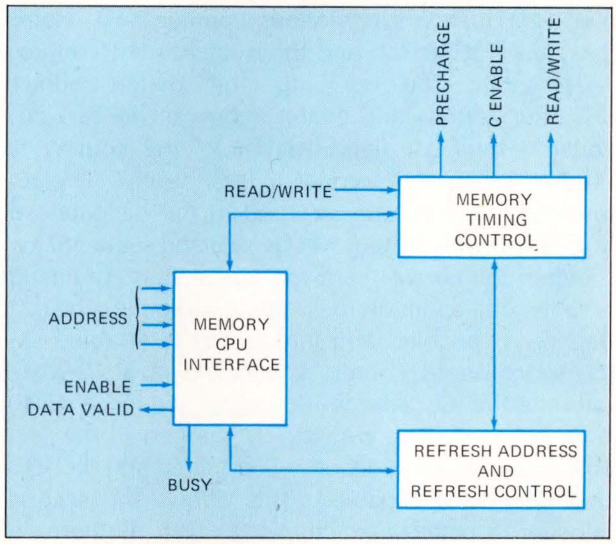


Fig. 3—Memory control card is divided into 3 distinct sections.

as well as to interface the CPU with the memory.

Each memory card contains 4k words × 18-bits of memory organized into four 1k word segments. Precharge and C enable are used for decoding the 1k word segments. The ten address bits from the control card select one 18-bit word from among the selected 1k words.

All translation, MECL-to-MOS and MOS-to-MECL, is performed on each memory card. Although this results in duplication of circuits on each memory card, it does have several distinct advantages:

- The lines connecting the control and the memory cards can be terminated transmission lines. The features gained from using terminated transmission lines are:
  a. There are no reflections to cause overshoot and undershoot.

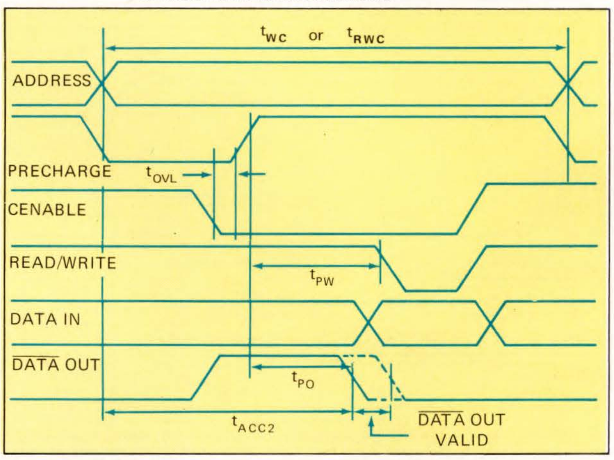


Fig. 2—Timing diagram for operation of 1k MOS RAM.

  b. High fan-out capability is possible with minimum degradation in speed. The output gates on the control card can fan out to as many as 16 memory cards if MECL 10,000 Series gates are used.
  c. By transmitting MECL 10,000 logic level signals rather than MOS level signals, the cross-talk between lines can be greatly reduced.
- The capacitance per translator can be held to a minimum. This reduction in capacitance enhances speed and simplifies the driver design in some cases.
- The data output capacitance of the memory is very small; 3 pF max. However, in a large memory system many data outputs have to be "OR"ed together, which can result in appreciable total capacitance. In turn, such capacitance can slow down the read-access time of the memory due to the low memory output current of 0.5 mA.

By providing MOS-to-MECL translators on each memory card, only four memory outputs are tied to one translator. The memory can be expanded by "OR"ing the outputs of the translators. Since transmission lines are used, little if any speed is lost with this method. This scheme keeps capacitance low and read-access time to a minimum, regardless of the size of the memory.

Control card is partitioned

Fig. 3 shows the interrelationship of these three memory control sections.

Memory timing control. A brief inspection of the detailed diagrams given in **Fig. 4a** and **4b** indicates that the control signals and their overlap could be divided into multiple 20 nsec increments. The scheme illustrated in **Fig. 5** provides the necessary timing pulses in 20 nsec increments when clocking is at a 25 MHz rate. This simple scheme requires one 4-bit binary synchronous counter, two 1-of-8 decoders (MC10162) and three latches with appropriate gating. The four output bits of the counter drive the address and enable inputs of the two decoders. The most significant bit of the counter is used to select the decoder to be enabled. The remaining three bits are attached to the decoders so that the decoder output will be selected sequentially.

When the control card receives a start command (enable), the count on the output is zero, i.e., the first decoder is enabled and the second is disabled. As the synchronous counter is clocked at a 25 MHz rate, the first decoder will output a sequence of 40 nsec pulses starting with D_1. At the end of the seventh count, the first decoder is disabled and the second decoder is enabled. This allows the second decoder to perform exactly as the first. As these 40 nsec pulses propagate down the decoder, they can be picked off at the appropriate times to set and reset latches for generating the desired control signals.

Note from the timing diagram that it becomes necessary to gate the clock pulse with appropriate decoder pulses to get suitable delay and overlap. If a read cycle is desired, the read/write pulse is neglected, the counter is reset to zero and the clock is disabled at the start of D_{12}. For a write cycle, the counter is not reset to zero until the leading edge of D_{15}.

It was mentioned earlier that precharge and C enable were used in decoding 1k out of 4k words of memory. The first 10 address bits from the CPU select one word from a selected 1k words of memory. The remaining address bits from the CPU are used to decode precharge and C enable.

Decoding of precharge and C enable is accomplished through a 1-of-8 decoder (MC10162) employed as a data distributor. The address on the decoder determines which 1k words of memory will receive precharge and C enable. All that is needed to expand the memory is additional data distributors for precharge and C enable. This control card contains sufficient decoding for 8k words of memory.

During a refresh cycle, the whole memory must receive precharge and C enable. This is accomplished by disabling the data distributor, and gating precharge and C enable to the whole memory. It should be pointed out that it is not necessary to decode precharge for a read or write cycle. However, by decoding precharge, it is possible to reduce clock driver and dc memory power comsumption by almost a factor of three for a 4k word memory system.

Refresh control. In order to completely refresh the whole memory every 2 msesc, one row must be refreshed every 62.4 μsec. A sequential addressing scheme can be employed to insure that each row is selected during this time. A 5-bit binary ripple counter can be used to sequentially generate the five address bits necessary to select the 32 rows during refresh (**Fig. 5**). A 16 kHz clock is used to increment this address and initiate the refresh control circuits. Two flip-flops (MC10131) make up the refresh control logic. On the positive edges of the 16 kHz clock, a logic "1" propagates through the two flip-flops. A logic "1" on the last flip-flop enables the 25 MHz clock, forces the read/write control circuit into the read mode, sets the busy flip-flop and switches the external row address coming from the CPU to the

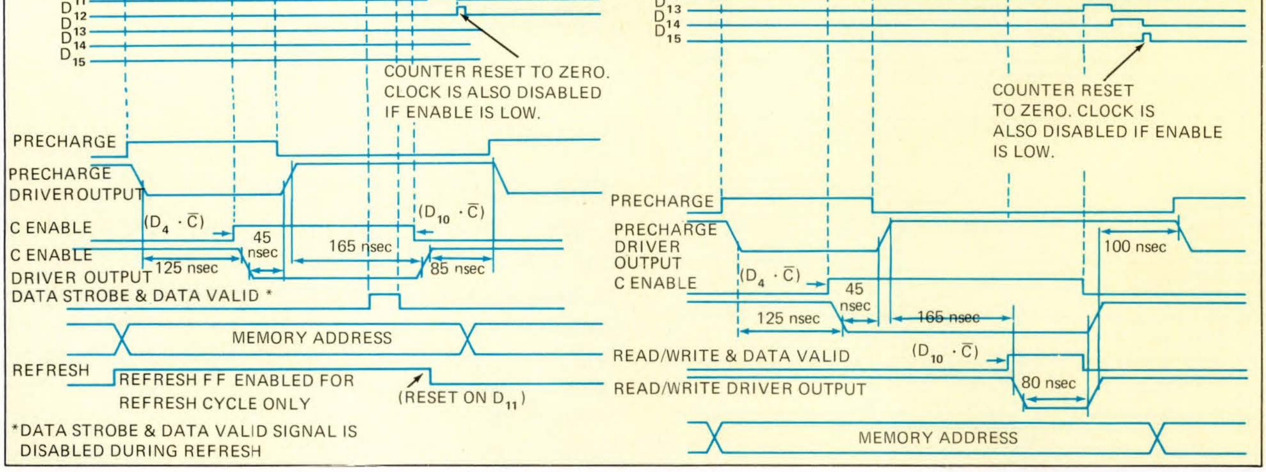


Fig. 4—System timing control for read and/or refresh (**Fig. 4a**) and write (**Fig. 4b**) cycles.

refresh address. This gating of addresses can be accomplished with a multiplexed dual D-latch (MC10134). The refresh control also disables the precharge and C enable decoders so that these signals can be sent to all of the memory devices.

Since the refresh cycle is identical to a read cycle, the counter is reset to zero and the clock disabled at D_{12}. The refresh control flip-flop, however, is preset on memory control pulse D_{11} (**Fig. 4a**), which returns control back to the CPU. If, by chance, a memory cycle is in process when a refresh is requested, the second refresh control flip-flop is prevented from being set until the memory cycle has been completed. At the completion of the memory cycle, the flip-flop is set by the synchronous counter reset pulse, D_{12} or D_{15}, and refresh cycle is initiated.

Memory-CPU interface. There are 13 flip-flop registers for address storage and 18 registers for data storage (**Fig. 5**). Other circuits include the enable latch and the 25 MHz delay-line oscillator.

The major advantage of a delay-line oscillator is that it can be turned on with a definite fixed time delay and turned off within less than half a clock cycle. This is important because turning off a high-speed clock in a closed-loop system can be a problem, especially if the number of gate delays travelled by the reset pulse represents more than half a clock cycle.

Memory card includes translators

The memory card contains seventy-two memory chips arranged in a matrix—in 4 rows by 18 columns. Each row has separate precharge and C enable lines for decoding. The 10 address lines are connected to respective address inputs of the 72 memories and the read/write lines are connected to 9 memories in each of 4 rows. This scheme allows data to be stored in the memory in 9-bit segments as well as in 18-bit segments. The four data inputs are common in each column, as are the four data outputs. Also included on the memory card are 38 MECL-to-MOS translators and 18 MOS-to-MECL translators.

MECL-to-MOS translation

The recommended memory supply voltage for minimum cycle time is that $V_{SS} - V_{DD}$ be + 16V. The memory input logic swing has to be 16V for the supply values given. For maximum memory speed the transition times of the control and address signals should be 20 nsec. For a large memory system, the capacitance on the control and address lines can become appreciable, making it difficult for the translators to meet the transition times specified. By providing translators on each memory card, the capacitance per translator can be held to a minimum. This also makes the translator independent of the size of the memory system.

The maximum capacitance per line for this memory system is:

Precharge	324pF	Read/Write	540pF
C enable	324pF	Data Input	20pF
Address	504pF	Data Output	12pF

Due to the low capacitance and non-critical transition times imposed on the data input lines, the simple driver illustrated in **Fig. 6** can be used. In order to drive the other lines in the time specified, it is necessary to add current boosting as in **Fig. 7.**

MOS-to-MECL translation maintains speed

The output of the memory device is an open-drain MOS device with a minimum capability of 0.5 mA. Note from the timing diagram (**Fig. 2**) that the output always goes HIGH when C enable is brought LOW. At time t_{po}, the output will go LOW if the data bit is a logic "1", or stay HIGH if a logic "O". This means that detection becomes critical on the trailing edge of the data output current, rather than on the leading edge.

The minimum logic swing for MECL 10,000 is 600 mV, and a minimum load resistance of 1.2 kΩ would be required to convert the MOS output to MECL logic levels. Two RC time constants for the maximum memory output capacitance (not including wiring or MECL gate capacitance) is 28.8 nsec. When the wiring, gate capacitance and translator propagation delay times are added, this time can be as high as 50 nsec. It is then obvious that a single load resistor should not be used for translating to MECL if the read access time is to be held to a minimum.

For optimum access time, the impedance seen at the data output should be as small as possible. The MOS-to-MECL translator given in **Fig. 8** has a load resistance of 200Ω and will easily convert the memory output to a MECL level within 10 nsec.

Power supply considerations

The recommended power supply voltages for MECL 10,000 are ground and −5.2V. The output emitter followers of MECL 10,000 require external pulldown resistors to either −5.2V or −2.0V. Due to the large power saving as well as the advantages of a transmission line environment, a −2.0V line was chosen. For example, the average power dissipation of a 510Ω pulldown resistor to −5.2V is 32 mW. This is in contrast to only 9 mW for a 91Ω pulldown resistor to −2.0V. The savings in power is approximately 3.5 to 1, which would more than justify the use of a third power supply in most large systems.

For MECL 10,000, the −5.2V power-supply current drain is essentially independent of the logic state and speed of operation. This constant-current feature results in negligible current variations on the −5.2V line, insuring a quieter, more troublefree system. Although the current drain is nearly constant, bypassing on the supply is recommended. A 1.0 to 10 μF capacitor at the -5.2V supply inputs, and at least a 0.01 to 0.1 μF capacitor for every four or five packages should be adequate for most systems.

Current transients are present on parallel terminated lines; therefore, the -2.0V supply will be subject to considerably more noise than the -5.2V line. To insure adequate bypassing, good RF-type capacitors (0.01 to 0.1 μF) placed every three or four packages, and 1.0 to 10 μF capacitors at the -2.0V supply inputs, are recommended.

Two additional voltages are required for the 1103-type MOS memories. They are +19V (V_{BB}) and +16V (V_{SS}). In the memory, an equivalent silicon junction diode must be reverse biased. If for some reason the V_{BB} line should drop below the V_{SS} line during turn-on or during normal operation, excessive current could flow through this diode and

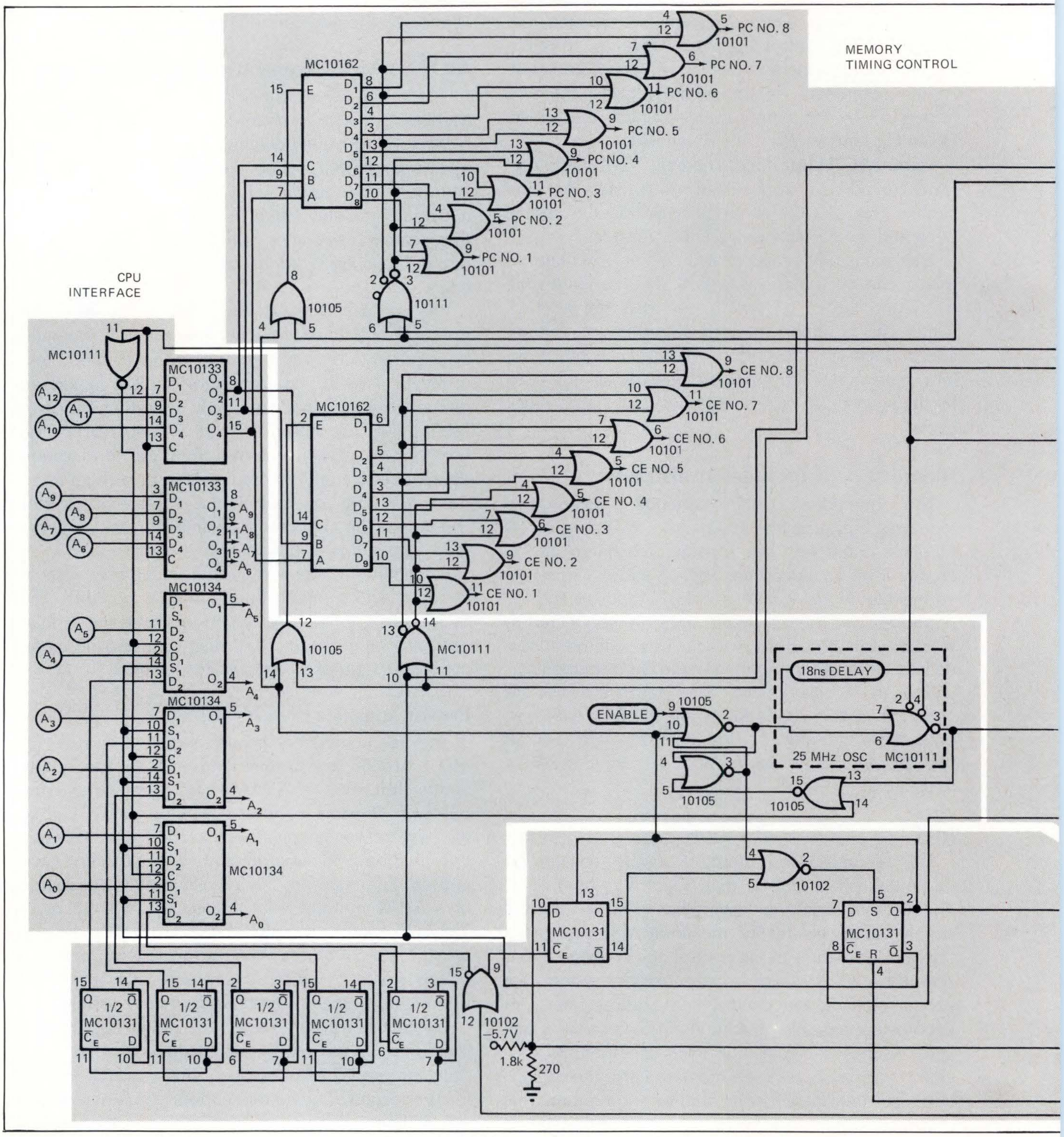
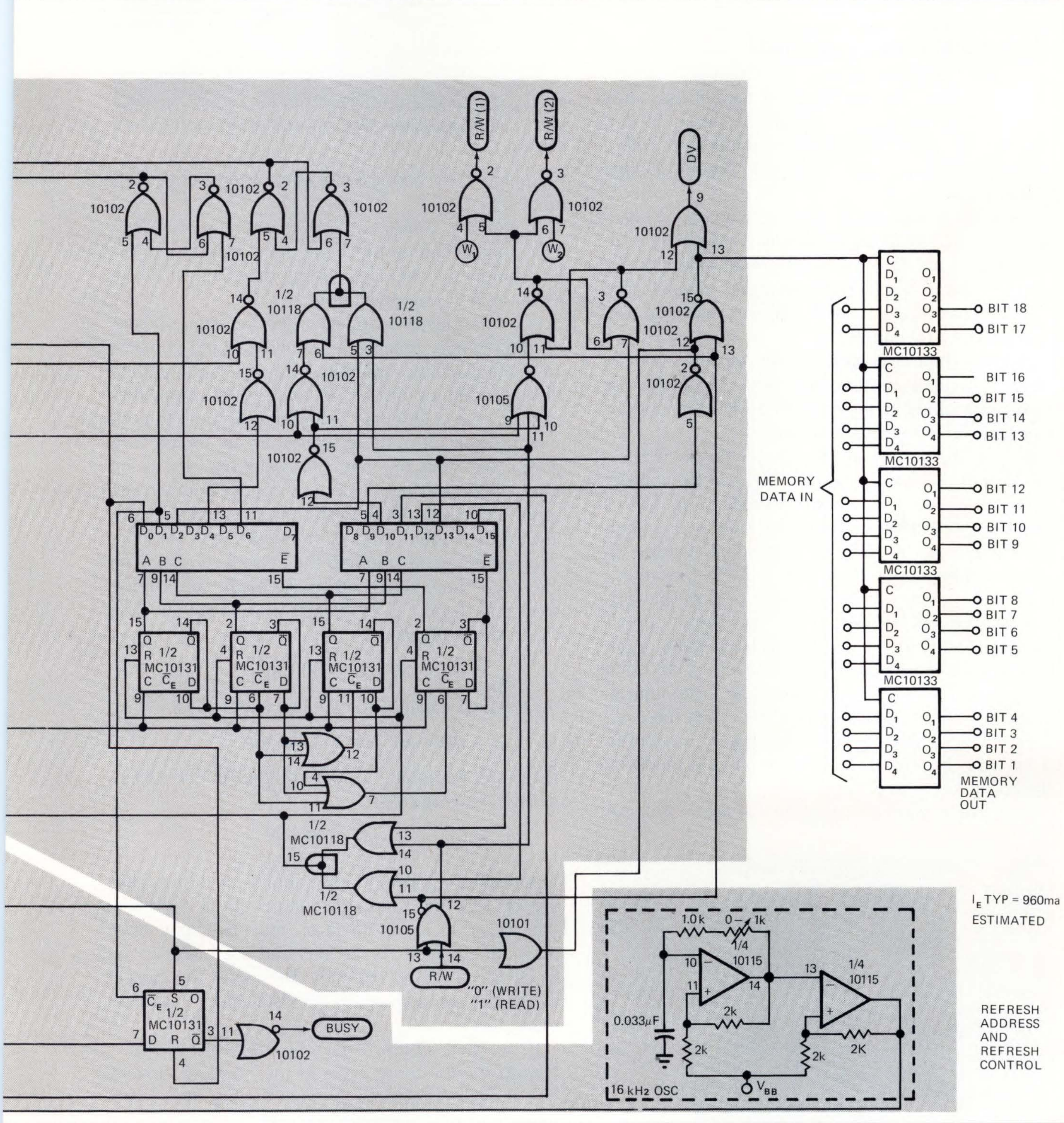


Fig. 5 – Complete logic diagram for the memory control card. The three control sections are shaded in different colors.

permanently damage or destroy the memory. To insure proper turn-on as well as proper V_{BB} voltage regulation, the V_{BB} voltage should either be generated with a 3 to 4V power supply in series with V_{SS}, or the V_{SS} voltage should be regulated 3 to 4V below V_{BB}. Either scheme insures that the V_{BB} line will rise at least as fast as the V_{SS} line during power turn-on.

To further insure that the silicon diode is never forward biased through accidental grounding of V_{BB}, a high-current hot-carrier diode, such as an MBD5300, should be placed across the V_{SS} and V_{BB} lines. The forward voltage drop of the MBD5300 is far less than that of the silicon junction diode of the memory, so all of the current from V_{SS} will be shunted through the hot-carrier diode, rather than through the memory devices.

A 4k word × 18-bit memory array produces large current surges on the V_{SS} supply during normal oper-



ation. To maintain proper voltage levels, adequate bypassing of V_{SS} is essential. At least a 0.5 to 1.0 μF low-inductance capacitor should be used for every 8 or 9 devices and should be placed as close to the devices as possible. Bypassing on the V_{BB} line should be with respect to V_{SS} rather than with respect to V_{DD}. This insures that the V_{BB} line will track the V_{SS} line. To further insure tracking of these supplies, a small impedance (300Ω) can be placed between the two supplies.

How much power is needed?

Memory control board. The memory control board contains sufficient logic to handle 8k words by 18-bits of memory. Thirty-seven MECL 10,000 packages are required to implement this logic with a typical −5.2V current drain of 1.6A. The −2.0V line typically draws 0.8A.

For each additional 8k word of memory expansion, one MC10133 quad latch, two MC10162 1-of-8 decoders and four MC10101 quad gates are required. These additional packages increase the −5.2V current by a total of 330 mA, and add 150 mA to the −2.0V supply.

Memory board power. Power for the memory board is divided into two segments. The first is the power consumed by the memory array itself, and the other is used in the level translators.

For the memory array, the power consumed is a function of the memory cycle used and the number of devices made active during a single cycle. With a memory cycle time of 580 nsec and a precharge pulse width of 190 nsec, the maximum average V_{SS} supply current specified is 25 mA. A close examination of the memory specifications reveals that precharge accounts for over 70% of the memory power for these conditions. Therefore, in large memory systems considerable power can be saved by decoding precharge. For inactive memories the maximum average V_{SS} current specified is 4 mA. With these V_{SS} current values, the maximum average V_{SS} current for a 4k word by 18-bit memory employing precharge decoding is:

$$I_{SS} = 18 \times 25 \text{ mA} + 3 \times 18 \times 4 \text{ mA} = 666 \text{ mA}.$$

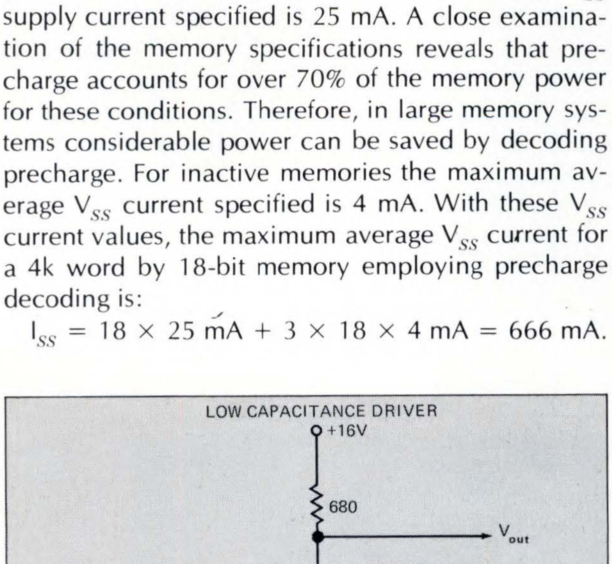


Fig. 6—Low-capacitance MECL-to-MOS driver.

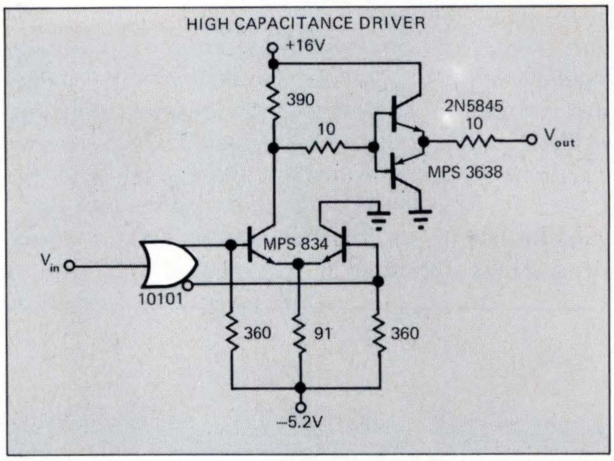


Fig. 7—High-capacitance MECL-to-MOS driver adds current boosting.

If precharge decoding is not employed, then I_{SS} becomes:

$$I_{SS} = 18 \times 25 \text{ mA} + 3 \times 18 \times 21 \text{ mA} = 1580 \text{ mA}.$$

Thus, not decoding precharge for a 4k word × 18-bit memory system results in approximately a 137% increase in V_{SS} supply current.

Level translators account for the remaining power on the memory board. The memory board contains 18 low-capacitance translators for data input, and 20 high-capacitance drivers for address selection, precharge, chip enable and read/write. In order to conserve power, all of these translators are forced high during the time the memory system is not being used. Both the high- and low-capacitance drivers supply constant current to the −5.2V supply, regardless of their logic state or frequency of operation. This feature greatly reduces the current variations on the −5.2V line, which otherwise might cause noise problems. Total −5.2V supply current for the low capacitance drivers is:

$$I_{EE_1} = 18 \times 50 \text{ mA} = 900 \text{ mA}.$$

For the high capacitance drivers, total I_{EE_2} is:

$$I_{EE_2} = 20 \times 67 \text{ mA} = 1340 \text{ mA}.$$

Therefore, the total −5.2V current for the 38 MECL-to-MOS translators is:

$$I_{EE} = I_{EE_1} + I_{EE_2} = 2240 \text{ mA}.$$

As for the V_{SS} line, it only supplies dc current during the time the translator outputs are in the LOW state (V_{DD}). In the LOW state, the low-capacitance driver draws typically 23 mA and the high-capacitance driver draws 40 mA. Therefore, the typical worst-case dc current for 18 data and 10 address translators is:

$$I_{SS} = 18 \times 23 \text{ mA} + 10 \times 40 \text{ mA} = 814 \text{ mA}.$$

Due to the low duty cycle of the 10 clock drivers, their power dissipation is considerably less. Maximum typical I_{SS} for precharge and chip enable is 13 mA and 23 mA, respectively.

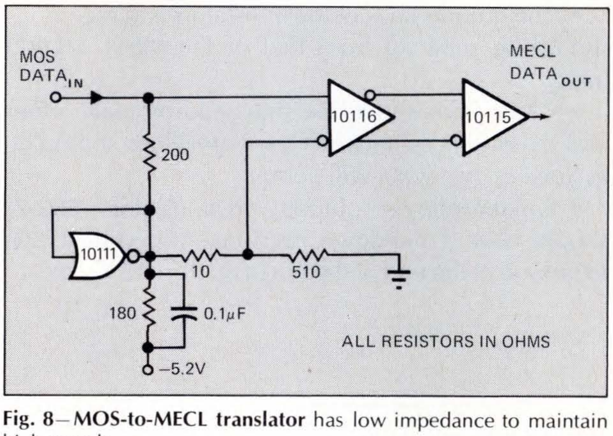


Fig. 8—MOS-to-MECL translator has low impedance to maintain high speeds.

In the high-capacitance level translators, the current-boost transistors dissipate power only when charging and discharging high-capacitance loads. This power can be found from the following relationship: $P = CV^2f$. With a memory cycle time of 645 nsec, the following dynamic translator powers are:

Precharge/Chip Enable:
$P = 324$ pF $(16V)^2$ (1/645 nsec) = 129 mW.
Read/Write:
$P = 540$ pF $(16V)^2$ (1/645 nsec) = 214 mW.
Address:
$P = 504$ pF $(16V)^2$ (1/645 nsec) = 200 mW.

The remaining translators on the board are MOS-to-MECL. These 18 data translators require a total −5.2V current of 210 mA. The −2.0V line requires a typical current of 700 mA.

ECL layout considerations are important.

With large systems, multi-layer boards are preferred. However, double sided boards were used for this system, which added somewhat to layout difficulty. MECL 10,000 is compatible with double sided boards, but for best results the following layout rules should be observed.

Since MECL is most senstive to V_{CC} (Gnd) variations, a good ground plane or bus is one of the most important considerations. Ideally, a ground plane should cover one side of the board, with the interconnections and supplies on the other. However, in most cases the layout will be too complex to permit all interconnects and supply lines to fit on one side. Therefore, on the ground side of the board, the layout should be planned so that interconnecting paths will not cut off a section of the ground plane, or isolate a section so that it is connected to the rest of the ground plane only with a narrow metal strip.

If ground buses have to be used, such as on the memory board, their width should be kept as large as possible, with at least 0.15 in. of width for each 10 packages. A good ground plane or bus will reduce current transients arising in parallel terminated lines, and also eliminate possible high-frequency ground loops.

If possible, the interconnections on one side of the board should run perpendicular to the interconnections on the other side. Since the −5.2V line (V_{EE}) is not as critical as the V_{CC} line, it can be routed as necessary.

The layout of the control board was relatively simple due to the small number of packages. On the other hand, the memory board presents a considerable layout problem because of the large number of devices. A 4k word by 18-bit memory requires 72 memory packages, 38 MECL-to-MOS translators and 18 MOS-to-MECL translators.

In order to insure reasonable success, the following layout rules should be considered. Dynamic MOS memories exhibit two undesirable characteristics: one is high surge current during precharge, and the other is large charging current encountered during switching of the control signals. As mentioned in the power supply section, adequate bypassing is essential to supply peak surge current demands. Also, the fast switching control lines can couple noise to adjacent lines, which can cause the system to fail. To reduce crosstalk and ground current noise, the following guidelines should be followed:

• Clock drivers and address level shifters should be placed as close as possible to the memory array to keep ringing problems to a minimum. For example, assume that the read/write line is 16 in. long and has a measured characteristic impedance (Z_o) of 120Ω. The line, when mounted on G-10 fiber-glass epoxy board, has a width of 0.015 in. and exhibits a propagation delay of 0.15 nsec per in. The high-capacitance driver used is the one given in **Fig. 7.** This driver has a typical output impedance for both the HIGH and LOW states of approximately 10Ω without the damping resistor. Since two read/write translators are used for each 4k words of memory, the maximum capacitance seen by each driver is 540 pF.

Using these values in a computer program designed to calculate the overshoot and undershoot of

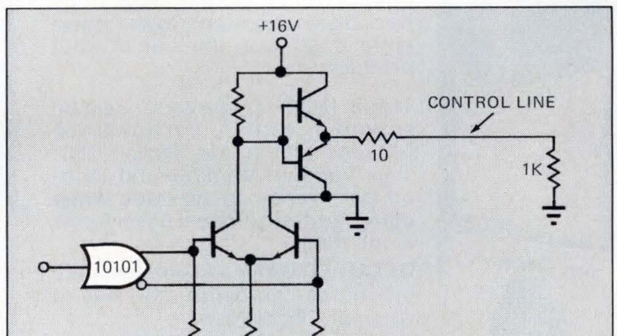


Fig. 9—Output translators use 1k pull down resistors to reduce cross talk and ground current noise.

an unterminated line, reveals that the overshoot will be 41.6% and the undershoot 17.7%. These are the values with zero damping resistance.

The actual ringing encountered at the end of the 16 in. line with zero damping resistance is 51.5% overshoot and 39% undershoot.

Ringing can be greatly reduced by inserting a small damping resistance in series with the line. By adding 10Ω to the line, the calculated overshoot and undershoot become 19.2% and 5.3%, respectively. The actual measured overshoot is 26.6%.

The overshoot is still too high to meet specified limits, but it could be reduced further with a larger damping resistor or by clamping diodes. An increase in damping resistance is undesirable as it will degrade rise and fall times.

Clamping diodes can be avoided if the line length can be greatly reduced. The calculated overshoot for an 8 in. line with a 10Ω damping resistance is 8.2%. Measured overshoot was 6.7%.

- Data-in and data-out lines should be on the opposite side of the board from, and run perpendicular to, the control lines.
- If possible, V_{SS} and V_{DD} should be distributed in a grid fashion to help reduce power supply noise.
- The ground lines of the translators and memories should be separate from that of the MECL 10,000 logic.
- Clock lines should be shielded from each other and the distances between translator lines should be as large as the layout will permit.
- Emitter-follower output-type translators (**Fig. 7**) should have a pulldown resistance (typically 1 kΩ) to ground at the end of the line (**Fig. 9**). □

Author's biography

Dick Brunner is a senior computer applications engineer at the Motorola Semiconductor Products Div., Phoenix, AZ. He received his BSEE from the University of Colorado and is completing his MSEE requirements at Arizona State University.

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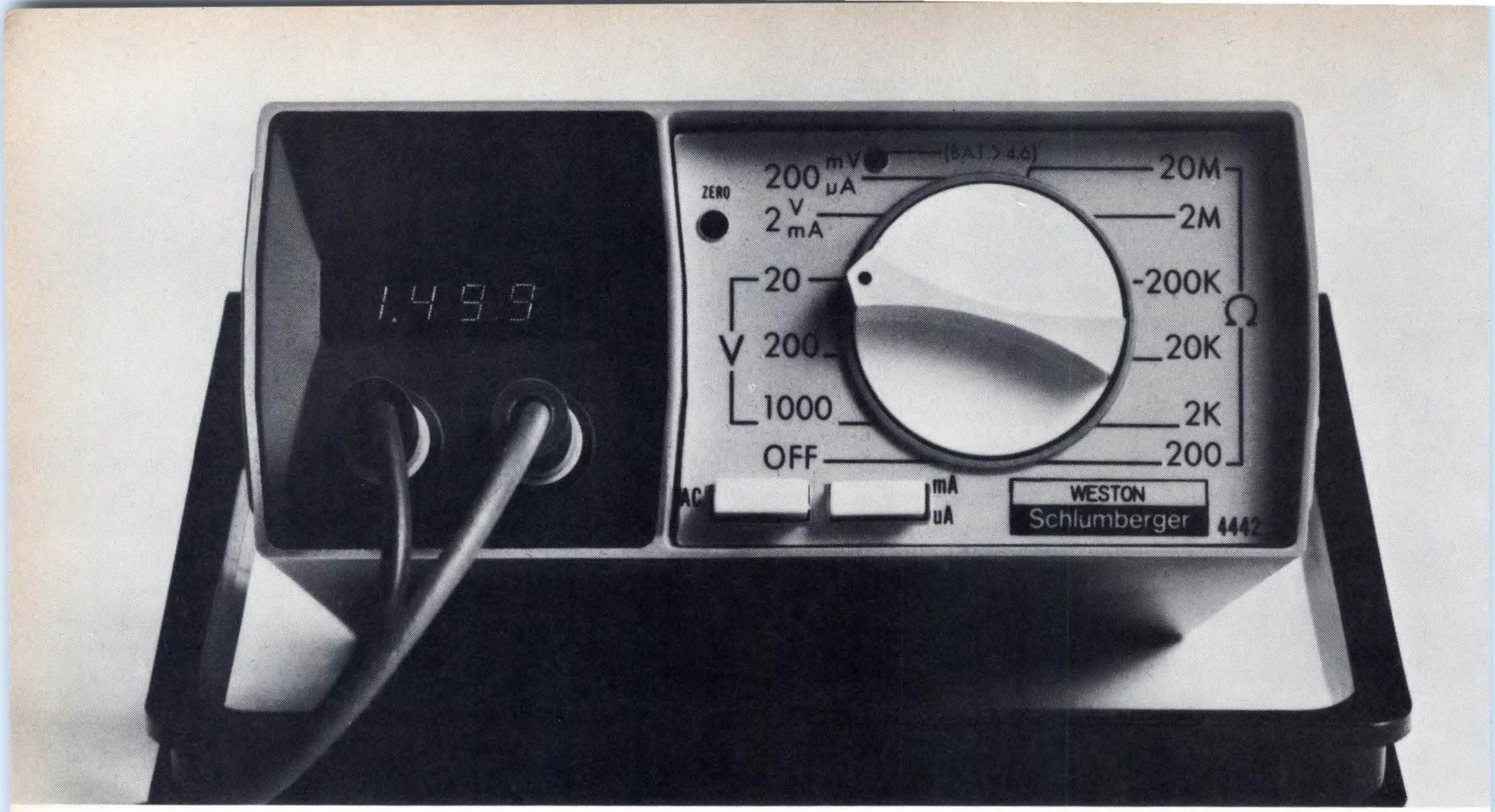

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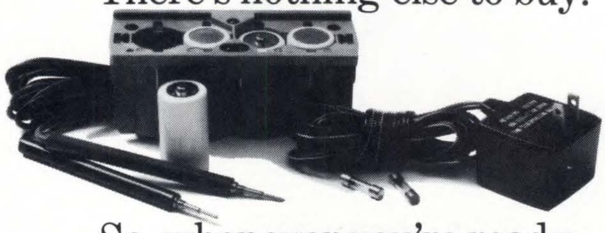

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CHECK NO. 19

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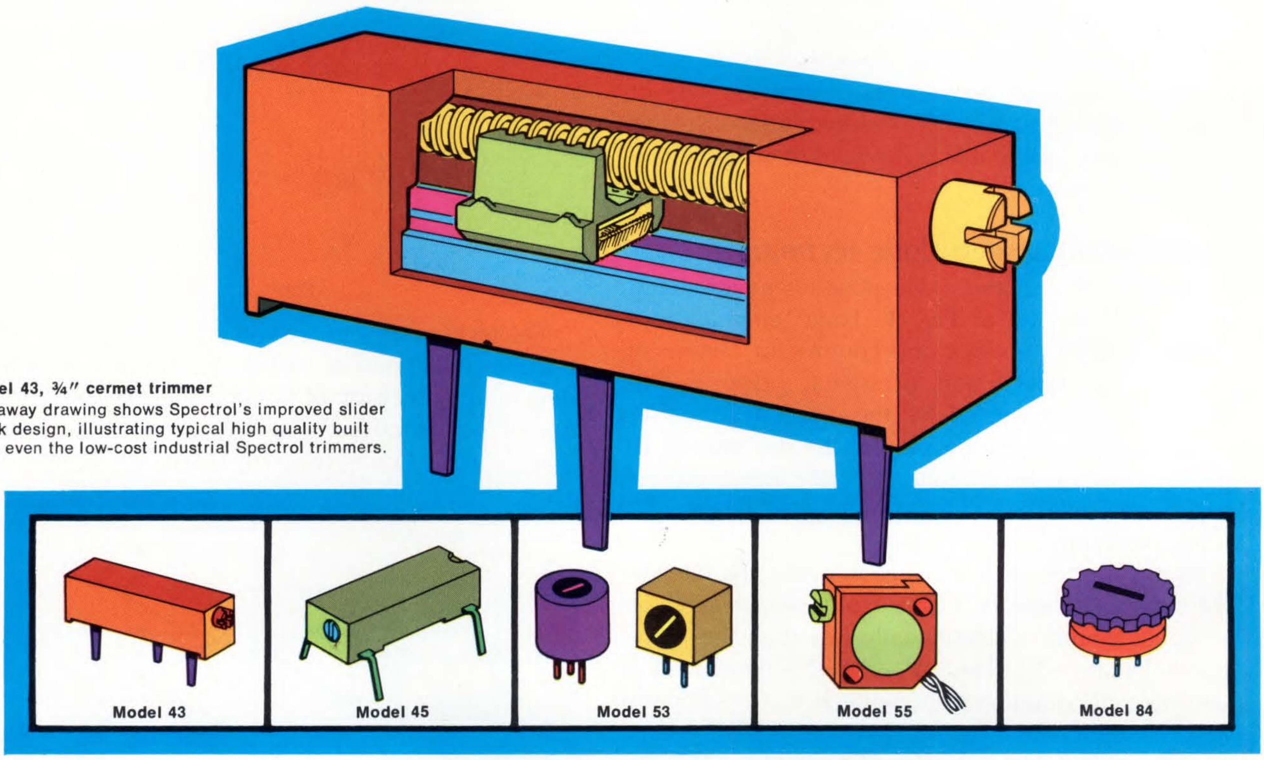

Model 43, ¾" cermet trimmer
Cut-away drawing shows Spectrol's improved slider block design, illustrating typical high quality built in to even the low-cost industrial Spectrol trimmers.

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CHECK NO. 47

Three-phase A/D conversion has high accuracy and low cost

A new conversion technique for those applications not requiring high speed improves integrated slope performance, yet eliminates costly circuits.

Harold S. Goldberg, Data Precision Corp.

In general, there are three main types of analog-to-digital conversion techniques used in digital multimeters: conversion by successsive approximation, conversion by circulating remainder and conversion by integrated slope. The integrated slope technique offers the best accuracy, linearity and immunity to noise, but not the highest speed. However, this is not a handicap for relatively low-speed applications, like in digital multimeters, where the human response in reading data requires more time than is normally needed for accurate conversion. Conversion rates of 2 to 3 per second are easily obtained; greater speeds may produce undesirable flicker and may be difficult to read or interpret.

Updating integrated slope techniques

The early form of the single-slope integrator circuit was configured as in **Fig. 1**. Logic circuitry (not shown) provides a clock and counter for control of the conversion cycle and for driving a display with the developed count. Briefly, the circuit accomplishes the conversion by developing a time interval (t) proportional to the magnitude of the input voltage (V_{IN}) and scaled as a proportional part of the full-scale excursion from $-V_{fs}$ to $+V_{fs}$.

At the start of each conversion cycle, the integrator output voltage (V_A) is at some negative value $-(V_{REF})$, which is algebraically less than the negative full scale $-V_{fs}$. The $-V_{REF}$ level is connected to the integrator input and the voltage V_A rises linearly at a rate determined by the time constant RC, where $R = R_1$. When the value of V_A reaches $-V_{fs}$, the output of A_2 changes polarity and starts the counter. When voltage V_A reaches the value of input V_{IN}, the output of A_3 changes polarity which stops the counter. The timing logic permits the integrator to continue for a planned interval T, sufficient to allow V_A to exceed the positive full-scale range value $+V_{fs}$. Then the logic switches the reference input to $+V_{REF}$ and the discharge of the integrating capacitor C is accomplished at the relatively fast time constant, RC, where R now is $R_2 << R_1$. The cycle then repeats.

In the normal meter applications, the previous counter value is held, or latched, in a buffer storage while the counter is changing, so that the display is updated only after the counter is stopped, and does not reflect the changing values as the counter increments to the next measured result.

The time interval, which determines the counter value, is obtained according to the equation:

$$V_A = \frac{1}{RC}\int_0^t V_{REF}\,dt = V_{IN}$$

$$\text{or } V_A = \frac{1}{RC}\Big[V_{REF}\Big]t - V_{fs}$$

$$\text{and } t = \frac{V_A + V_{fs}}{V_{REF}}RC$$

The technique is truly simple to implement and is relatively inexpensive. However, accuracy is dependent on the precision of R_1 and C, and of the generation of the references V_{fs} and V_{REF}. Moreover, amplifiers 2 and 3 acting as comparators must float and

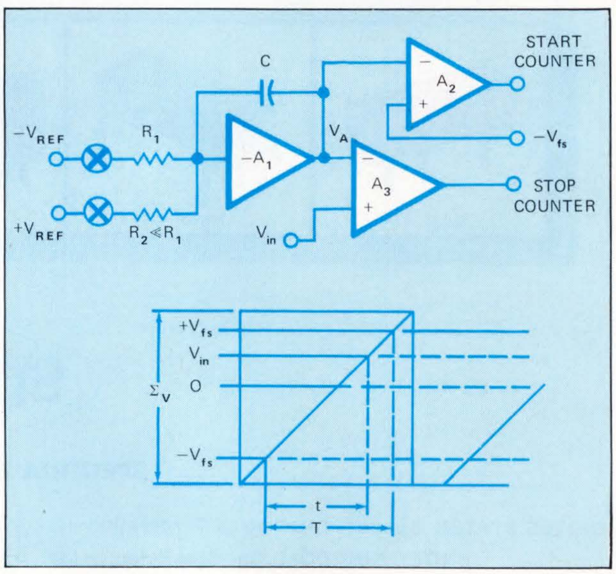


Fig. 1—Single-slope integrating a/d has poor accuracy.

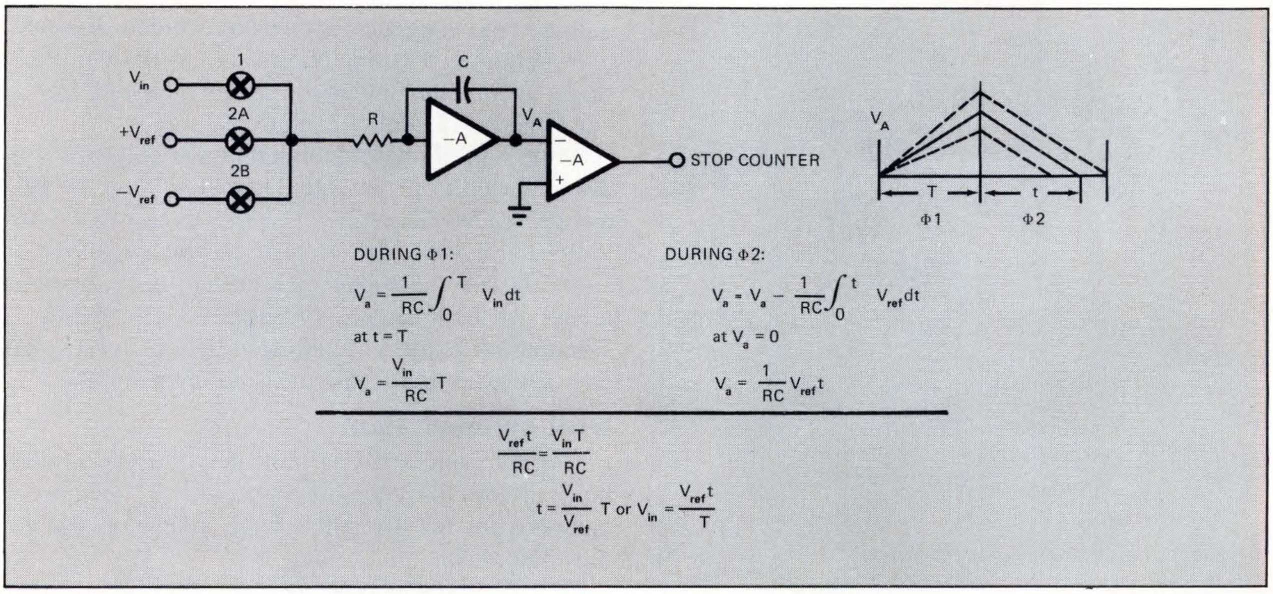


Fig. 2 – Dual-slope integration a/d improves accuracy but suffers from long-term drift.

are subject to common mode voltage problems in determining the cross-over polarity points as they start and stop the counter. In addition, the results are affected by drifts of the reference generating circuit, the comparator amplifiers and the integrator. Digitally, for bipolar operation, the input requires an up/down counter.

Some of the single-slope integration problems are solved by the dual-slope technique. A typical dual-slope circuit is illustrated in **Fig. 2**. Its operation proceeds in two well defined phases, as controlled by digital logic circuitry not shown in the illustration. Briefly, the voltage to be measured is integrated for a constant interval during phase 1, and then the charged integrating capacitor is discharged at a constant rate during phase 2. Because the charge at the end of phase 1 is theoretically proportional to the input unknown voltage, the time to discharge is then proportional to this value. The counter circuit translates the discharge time to a scaled count that represents the input voltage.

At the start of phase 1, the integrator output voltage V_A is zero, and the unknown input is connected to the integrator by switch 1. The integrator acts for a fixed interval T, as controlled by the master clock and digital logic circuitry. At the end of time T, the value of V_A will be proportional to the input V_{IN} and the value of time constant 1/RC.

At the start of phase 2, switch 1 opens removing the unknown input and connecting either $+V_{REF}$ or $-V_{REF}$, depending upon the polarity of the input V_{IN}, so as to reduce the charge on C during phase 2. Phase 2 proceeds until the output of the comparator changes polarity, indicating the zero-crossing (compared to ground). The time (t) to discharge C is then a measure of V_{IN} according to the equation:

$$t = \frac{T}{V_{REF}} V_{IN}, \text{ where T and } V_{REF} \text{ are constants.}$$

Note that this result is independent of the values of R or C, and that the instrumentation utilizes a grounded comparator; both are improvements over the single-slope technique. Also, with this technique a single up counter is all that is needed, rather than an up/down counter, to get both polarities on the display. However, a longer conversion time is required for the two phases instead of one; two voltage references of equal but opposite polarity are required and the performance is still dependent on the long-term drift of integrator and comparator amplifier units.

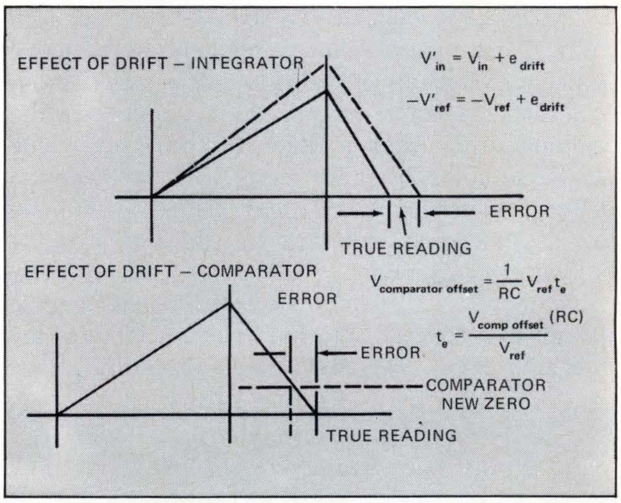


Fig. 3 – Drift components that reduce dual-slope's accuracy.

It may be of interest to indicate the error impact of the integrator drift, as illustrated in **Fig. 3**. The integrator drift introduces an offset input which alters the rate of charge and discharge of the capacitor, and hence the value of V_A reached at the end of interval T, and the time of zero crossover (t).

The comparator drift introduces an offset which affects only time t, at which the zero crossover ending phase 2 may be detected.

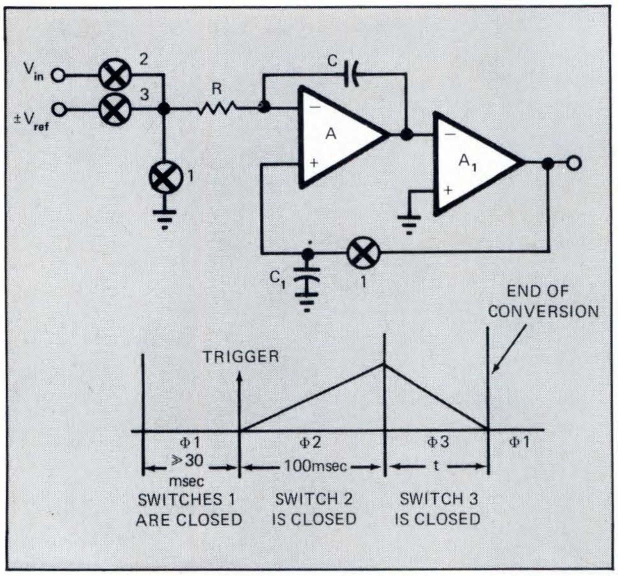


Fig. 4—Self zeroing in Triphasic technique eliminates long-term drift components.

Triphasic conversion eliminates drift

This is similar to the dual-slope technique, but as its name implies, a third phase of operation is incorporated in each conversion cycle, which effectively eliminates the drift impact on accuracy. The TRIPHASIC (TM) circuit is illustrated in **Fig. 4**. The master clock, digital timing and control logic, and counter circuitry are not shown.

During phase 1, the switches marked 1 are closed. These accomplish two functions: first, the integrator input is grounded, presenting zero signal to the input, and second, the integrator-comparator loop is closed, so that any non-zero signal components in the active or passive elements of the loop will be servoed out by the charge stored on capacitor C_1, built up by the servoing action during phase 1. This is the value needed to compensate for "zero drift". At the end of phase 1, switches marked 1 are opened, leaving the stored value of C_1 connected to the non-inverting input of the integrator.

During phase 2, switch 2 is closed, connecting the unknown voltage (V_{IN}) to the inverting input of the integrator. The integrated value, appearing at the output of the integrator, is thus corrected for the zero drifts determined during phase 1. As in normal dual-slope action, the integrator action proceeds for a fixed interval (T), defining phase 2.

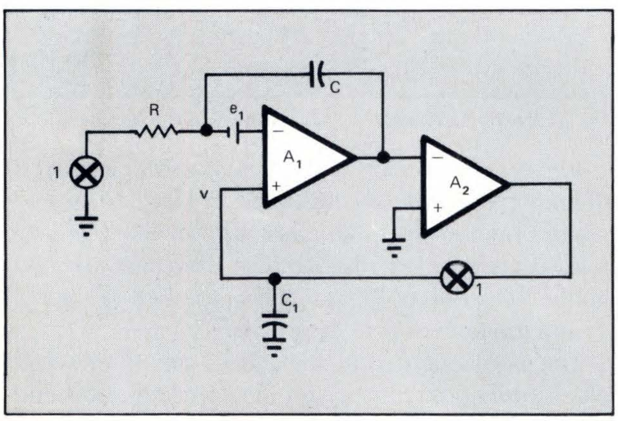


Fig. 5—How to compensate for drift in Triphasic a/d.

At the start of phase 3, the unknown voltage V_{IN} is disconnected from the integrator input, and the reference voltage of proper polarity is connected by switch 3 to drive the voltage on the capacitor to zero. The zero crossover is detected by the ground referenced comparator, and phase 3 is completed. The time for phase 3 is indicated by a counter value and displayed as a scaled measure of the input.

Drift compensation

The following analysis indicates how the charge built up on the memory capacitor C_1 effectively compensates for the drifts of the integrator and for the comparator.

Consider the effects of integrator drift first, and let the drift be represented by an equivalent voltage (e_1)

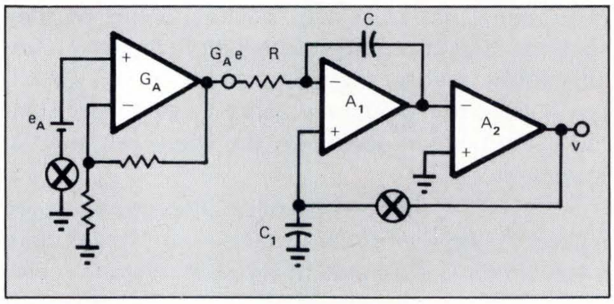


Fig. 6—Input buffer amplifier also adds to drift.

at the inverting input to A_1, as shown in **Fig. 5**. During phase 1, the loop is closed and the servo action continues until the voltage (v) at the non-inverting input to A_1, is equal to the effect of e_1 at the inverting input.

The output of A_1 is $-A_1(e_1 - v)$, which is the input to A_2.

The output of A_2 is $-A_2(-A)(e_1 - v)$, and this is also v.

$$v = A_1A_2(e_1 - v) = A_1A_2e - A_1A_2v$$

$$v = \frac{A_1A_2e_1}{1 + A_1A_2}$$

For high gain values of A_1 and/or A_2,

$A_1A_2 \gg 1$, and

$$v \cong \frac{A_1A_2}{A_1A_2} e_1 \cong e_1.$$

Thus, v self-servos to the e_1 level.

To illustrate the compensation for the effect of comparator A_2 drift, refer again to **Fig. 5**. Let the comparator drift result in an equivalent offset (e_2) introduced at the non-inverting input to the amplifier A_2, and let the closed loop gain of A_1 be represented by G_1.

If δ is the output of A_1 applied to the inverting in-

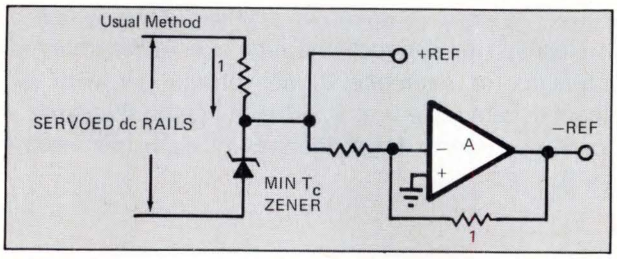


Fig. 7—Typical method for generating voltage reference requires high-cost components.

put of A_2, then the output of A_2 is:

$A_2(e_2 - \delta)$, and this is fed back to A_1, so that the output of A_1 is:

$G_1(A_2)\ (e_2 - \delta)$,

which is also δ. Therefore

$$\delta = G_1A_2e_2 - G_1A_2\delta$$

$$\delta = \frac{G_1A_2}{1 + G_1A_2}\,e_2$$

And for high gains of G_1 and/or A_2, so that $G_1A_2 \gg 1$, $\delta \approx e_2$.

But the error output signal is v, where v is the output of A_2 with δ and e_2 its inputs, thus:

$v = A_2(e_2 - \delta)$, so that using δ from above,

$$v = A_2(e_2 - \frac{G_1A_2}{1 + G_1A_2}\,e_2) = \frac{A_2}{1 + G_1A_2}\,e_2$$

$$v = \frac{1}{\frac{1}{A_2} + G_1}\,e_2 \approx \frac{e_2}{G_1} \text{ for } A_2 \gg 1$$

If a high-impedance input buffer amplifier is used preceding the integrator-comparator circuitry, it is also a source of drift error, and its contribution to the stored compensation in the Triphasic design may be calculated as indicated in **Fig. 6**.

If the zero drift of the amplifier is e_A and its closed loop gain is G_A, then the amplifier output is G_Ae_A, and the input to A_1 is:

$(v - G_Ae_A)$

which is amplified by A_1A_2 and becomes v.

Thus, $v = A_1A_2(v - G_Ae_A)$

$$\text{or } v = G_Ae_A\,\frac{A_1A_2}{A_1A_2 - 1} \approx G_Ae_A \text{ for } A_1A_2 \gg 1$$

Combining all the zero drift components of v in a linear manner including that of a buffer input amplifier,

$$v = G_Ae_A + e_1 + \frac{e_2}{G_1}$$

This indicates the magnitude of offset error which appears at the comparator amplifier output using the Triphasic design. Without this feedback, the open-loop output would be:

$V^1 = G_AA_1A_2e_A + A_1A_2e_1 + A_2e_2$

obviously well into saturation. This is the drift that must be minimized by expensive and exotic amplifier design or by frequent and annoying front-panel adjustments.

In the Triphasic approach, amplifier drifts in the order of 10 to 30 mV referred to input may be tolerated with amplifier gains of $G_A = 8$, $A_1 = 10{,}000$, and $A_2 = 50{,}000$. A minimum of 30 msec is assigned to this self-servo phase between each conversion, assuring continuous correction.

Reference accuracy counts too

The second source of analog-to-digital conversion error arises from the accuracy and drift of the reference source for the down-ramp integration. The accuracy of the reference voltage determines the scaling accuracy of the conversion. Where the reference voltage for the conversion is also used as the reference for the sensor at the origin of the data, maintaining the accuracy is a relatively minor problem, requiring careful attention to the interconnection between source and converter. The generation of equal reference voltages of opposite polarity however, is a converter function and is typically accomplished as shown in **Fig. 7**.

A minimum temperature-sensitive zener diode is usually connected in a servo circuit in order to

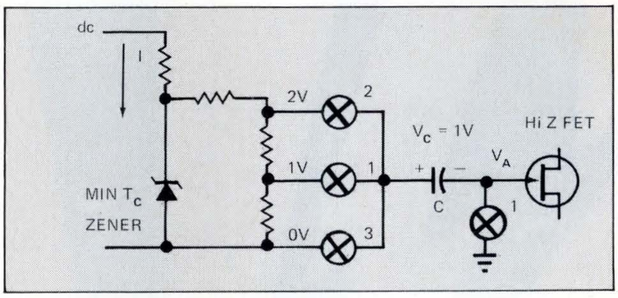


Fig. 8—Isopolar reference generation eliminates costly parts.

maintain a stable voltage as the positive reference. Then a unity-gain inverting amplifier develops the negative polarity of the reference for converter use. The circuit depends for its accuracy on the temperature compensation of the zener and amplifier, and on the zero drift characteristics of the amplier. In addition, the circuitry to develop the opposite polarity represents an added cost and reduced reliability as the source of potential failure.

The three phases of the Triphasic a/d conversion provide a logic control sequence which is used in a passive circuit to generate the equal and opposite polarity reference voltages. This design technique is known as the Isopolar reference generation **Fig. 8**. A minimum T_C zener diode is incorporated in a servoed loop as in the typical design. An improved temperature characteristic is obtained by enclosing the diode in a thermal controlled oven, yielding at least a 10:1 improvement. The servoed constant current in the loop is then directed through a precision resistor divider network to establish precise values of +2V and +1V with respect to reference OV.

During phase 1 of the Triphasic operation, switches designated "1" in the illustration are closed. This charges capacitor C to +1V with the charge polarity as indicated. At the end of phase 1, the "1" switches are opened and the capacitor remains charged, becoming in effect a battery of 1V potential. The FET switch, through which the selected reference value (V_A) will be connected to the a/d integrator comparator circuit, is of very high impedance and no charge of any consequence is conducted from the capacitor in the time sequence of one conversion cycle.

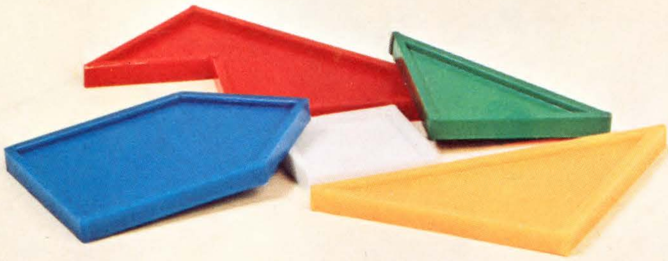
Now, at the end of phase 2, the polarity of the unknown input is sensed, and the reference of the opposite polarity is to be connected at V_A through the Hi-Z FET. If a +1V reference is required (to convert a negative unknown voltage), then switch 2 is closed. This action places the high side of the capacitor at +2V potential, delivering +1V with respect to reference 0 at V_A. If a −1V reference is required (to convert a positive unknown voltage), then switch 3 is closed. This connects the high side of the charged capacitor to reference 0, delivering −1V with respect to reference 0 at V_A. The charge on the capacitor is updated to 1V at the start of each conversion cycle. □

Author's biography

Harold S. Goldberg is president and chief operations officer of Data Precision Corp., Wakefield, MA. He was previously vice-president of Analogic Corp. Mr. Goldberg received his BEE from Cooper Union School of Engineering and MEE from Polytechnical Institute of Brooklyn. Two patents have been granted to Mr. Goldberg.

CHECK NO. 51 →

This problem should take you about 17 minutes to solve.



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Watch for the detailed tour schedule in our next issue.

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DATE	TIME	SITE
January 10 A.M.	Wednesday 9:00-11:00	Honeywell, Inc., 4800 Dry Creek Road, Littleton, Colorado
January 10 P.M.	Wednesday 2:00-4:30	Hewlett-Packard, 815 S.W. 14th Street, Loveland, Colorado
January 11 A.M.-P.M.	Thursday 10:00-2:00	Hewlett-Packard, 1900 Garden of the Gods Road, Colorado Springs, Colorado (Parking: Building "A")
January 12 A.M.-P.M.	Friday 10:00-2:00	IBM, 6300 Diagonal Highway, Boulder, Colorado (Parking: West of Building 021)
January 18 A.M.-P.M.	Thursday 10:00-2:00	Singer, Friden Division, 2350 Washington, San Leandro, Calif.
January 19 A.M.-P.M.	Friday 10:00-2:00	Ampex Corporation, 401 Broadway, Redwood City, California
January 22 A.M.	Monday 9:00-11:00	Precision Instruments, 3170 Porter Drive, Palo Alto California (Parking: Parking Lot)
CO-HOST		S. C.—Marchant Division, 3210 Porter Drive
January 22 P.M.	Monday 1:30-4:30	Philco-Ford, Western Dev. Lab., 3939 Fabian Way, Palo Alto, California
INVITEE INVITEE		Philco-Ford, Electronics Group Varian Associates
January 23 A.M.	Tuesday 9:00-11:30	Sylvania Electric, 100 Ferguson Drive, Mountain View, California
January 23 P.M.	Tuesday 2:00-4:30	Vidar Corporation, 77 Ortega Avenue, Mountain View, California
January 24 A.M.-P.M.	Wednesday 10:00-2:00	Applied Technology, Division of Itek, 645 Almandor Ave., Sunnyvale, California (Parking: Building 849)
January 25 A.M.	Thursday 9:00-11:30	Hewlett-Packard, 11000 Wolfe Road, Cupertino, California
January 25 P.M.	Thursday 2:00-4:30	Information Storage Systems, 10435 North Tantau Avenue, Cupertino, California (Parking: Building 3)
INVITEE		Four-Phase Systems, 10420 North Tantau Avenue
January 26 A.M.	Friday 9:00-11:30	Memorex, Central at San Tomas, Santa Clara, California
January 26 P.M.	Friday 2:00-4:30	IBM, Montry & Cottle Roads, San Jose, California
January 29 A.M.	Monday 9:00-11:30	Burroughs Corporation, 6300 Hollister Avenue, Goleta, California (Parking: North Parking Lot)
INVITEE		Raytheon, 6380 Hollister Avenue
January 29 P.M.	Monday 2:00-4:30	Litton Systems, 5500 Canoga Avenue, Woodland Hills
January 30 A.M.	Tuesday 9:00-11:30	Bunker Ramo, 8433 Fall Brook, Canoga Park, California (Parking: Visitor's Lot)
January 30 P.M.	Tuesday 2:00-4:30	Teledyne Systems, 19601 Nordhoff, Northridge, Cailfornia
January 31 A.M.	Wednesday 9:00-11:30	Electronic Memories & Magnetics, 12621 Chadron, Hawthorne, California (To Be Confirmed)
January 31 P.M.	Wednesday 2:00-4:30	Northrup Aircraft, 2301 West 120th, Hawthorne, California (Parking: East Lot)

FEBRUARY THROUGH MARCH CALENDAR TO BE RELEASED SOON.

Designers' Roundtable

Designers discuss IC op amps: are they as good as they should be?

You've heard all of those "good things" about IC op amps. Here are some of the pitfalls encountered by six engineers.

When EDN asked some local design engineers to participate in a discussion of IC op amps, we were a little hesitant about restricting the conversation to such a limited topic. In fact, during the interview sessions, we discussed their feelings toward most linear modules and ICs, but it turned out that we could actually do several articles on just op amps.

Surprisingly, there were very few beefs about the manufacturers or their hardware, but a great deal of discussion centered around the software deficiencies of op amps.

Spec sheets take it on the chin

If there is one area of unanimous opinion, it must be EEs unhappiness with manufacturers' spec sheets.

Today's designers are as cynical about a manufacturers' spec sheets as they are about last years campaign promises. Here are a few comments:

"The first cardinal rule—don't believe the data sheets—it's pretty hard to beat just plain basic empirical lab results."—*Frank Slater.*

"Because of the competitive situation, a lot of things that should be mentioned on the spec sheets aren't, until the manufacturer has solved his problem. Then the problems are talked about because they have been solved. Offset voltage drift with temperature, for different offset currents, for example, should be better spec'd. If you are using a device that is spec'd at 5 mV offset and a certain temperature drift, and you adjust that down to 1 mV, the drift gets worse. Very few devices are spec'd for this, and maybe it's a rather elaborate parameter to specify for general-purpose devices, but a discussion on the data sheet of what to expect would be very valuable to designers."—*Garrett Myers.*

"There are many specs that just don't show on the spec sheet. My requirements are mostly dc, so speed doesn't mean that much to me. One thing that is important to me is what happens to the input current when you go over the common-mode range. For that matter, what is common-mode range? Is it the voltage at which you begin to see some distortion at the output? That's one manufacturer's definition. I feel that the specified common-mode voltage should be that voltage range over which all of the specifications of the op amp hold—period. If they tell me the bias current is 10 nA, I expect it to be 10 nA over whatever common-mode voltage they specify. That is a spec that is rarely given. Sometimes the input current goes way up when you're up near the positive common-mode limits, especially in FET-input op amps."—*Dick Davis.*

"I'd like to see a good discussion of all interactions on the spec sheet. If there is a pin that I can get my hands on, I want to see it fully characterized. I don't want to be told simply to put a 100k pot between pins x and y; I want to know everything that can happen."—*Ed Merrick.*

"I think we are victims of specsmanship on all spec sheets. If you go to the spec sheet, you'll see some pretty strange tests. Now I don't doubt that if you go back and do the tests the way they did, you'll get the same answers, but the trouble is that it's really not a very valid test. An op amp with a 100Ω input resistor and a 100Ω feedback resistor just doesn't exist in my world. It makes a good looking spec sheet, but I'm sorry, I don't work that way. I have to live with a 1-kΩ input and 10-kΩ feedaround, and I don't get the same performance. Now whether they do that because it's easier to automate under those conditions or they do it to make the spec sheet look better, I don't know. I'm inclined to say it's done because it looks better on paper."—*Frank Slater.*

"Spec-sheet parameters for input currents are only true at zero volts or at narrow common-mode ranges, and if you try to use those input current specs while you're using it at one of the approved parameters, you can't do it; yet the spec sheet doesn't tell you that. It doesn't say that it will, but it doesn't say that it won't. A comprehensive spec that covers everything would be about 20 pages long and make the op amp too expensive, so that's out, but a little bit of discussion on the spec sheet as to what these "tradeoffs are would be very useful."—*Garrett Myers.*

Participants in the EDN Designers Roundtable on IC op amps

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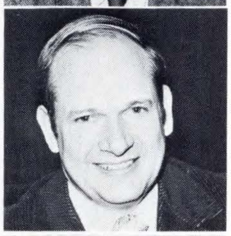

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Medical and research mass spectrometers

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program manager
Military Data Systems
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Nashua, N H
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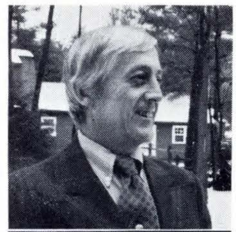

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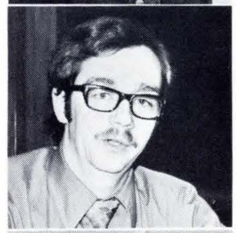

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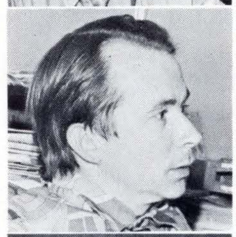
Test systems



Bill Furlow
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Understand the manufacturers' problems

If the designer is quick to criticize all manufacturers' spec sheets, they also have a deep understanding of their problems, for most of them have seen firsthand how data sheets are born. They realize that marketing has more control than engineering and that marketing is not as conservative as engineering.

"Somebody has to start talking about the shortcomings of the devices. Nobody wants to go broke because they have integrity, but I think this would show unusual character on the manufacturer's part, and I would support him". —*Garrett Myers.*

Most of those present concurred in this statement. Incomplete spec sheets do nothing but waste time for everyone. If the part isn't right for the job, a spec sheet won't sell it, but it will create ill will.

Typical values are typically useless

"Typical specifications are of no value to me or any other engineer I've ever talked to. We cannot sell instruments to typical specifications, so we cannot design around anything but guaranteed component performance. Unfortunately a good deal of space is wasted on some of the data sheets touting typical values." —*Paul Levesque.*

"If I'm going to do a selection process and a manufacturer's willing to *guarantee* that a certain percentage of a typical lot will meet his typical specs, then typical would mean something. I could then use the fallout in some less severe application. But typicals are of questionable value unless the manufacturer defines typical." —*Dick Davis.*

Testing is not a luxury

All of the engineers EDN talked to felt that some sort of screening of linear ICs was required.

"Typically, you will experience 1 to 5% rejections against the manufacturer's data sheet. So the guy who's buying linear circuits without testing them must be experiencing a very high failure rate at some other point.

The ICs that pass initial screening seem to do pretty well, especially if you're using metal cans. Field failure rates on properly screened parts are impressively low." —*Garrett Myers.*

What about the equipment involved in testing op amps? Is it something that can be justified? Especially, what can a small company do to screen incoming devices?

"Small \$5-10k testers help but aren't really worth the effort. It takes \$50K to properly test an op amp with all of the interrelated variables to assure that it will work in all of your circuits. The manufacturer cannot be entrusted to final screen for you even though he may have the best equipment and program, because he is prone to logistical errors (shipping the reject bin). A good testing service is the answer for the small user." — *Garrett Mayers.*

Has anyone had problems getting the manufacturers to take back their defective parts? Not one person at the roundtable had. Most manufacturers, they agreed, are eager to back up their guarantees. However, most felt that the manufacturers did not do an adequate analysis of the failed components.

"Only one manufacturer had taken my word that an evaluation part was bad, and bothered to run a study on that part. Most of them will just say, 'ah, ya blew it up'." — *Dick Davis.*

Power aging may be necessary

"If you could see my field failure logs — covering thousands of ICs — and see the difference between off-the-distributor's shelf ICs and those which have been through a burn-in, or power-age you would never again put an IC into your circuit without a complete screening. If you're too small to do it all yourself, you'd better buy 883 or 38510 parts. That means that a 15¢ part may cost \$1.50." — *Frank Slater.*

On this subject there was considerable difference of opinion. Some felt power aging was required for commercial service; some didn't.

"We only power age if we're suspicious of the lot for some initial test result or something. Usually we do thermal cycle them, but not under power, and we experience less than 1% field failures. We're as worried about that as anyone because we guarantee our systems for ten years." — *Dick Davis.*

"Even on commercial units we have to test 100%, at the IC level and perform 100% burn-in, because you can't afford to make a \$400 service call to repair a \$4000 unit in the field" — *Frank Slater.*

"I haven't found, though, for returnable commercial devices, that power aging buys much. It all depends on what level of reliability you want or your customer needs." — *Garrett Myers.*

Popcorn can choke a system

Bear in mind that all of our participants work in areas of the industry where reliability is crucial. Perhaps for this reason, they were more aware of, and concerned with, popcorn noise than would generally be the case.

Popcorn noise is one of those parameters that manufacturers have only recently begun to talk about. How can you test for it?

"Popcorn noise is hard to test for, usually taking one or two seconds, but it can take even minutes in some op amps." — *Dick Davis.*

"The only test that is realistic, at least for our use, is peak-to-peak output voltage as a function of time. I run a chart recorder at 25 mm/sec for at least 20 seconds on every op amp that we use in a popcorn-critical application. Another important thing is that the input must be terminated as it will be in the application, because popcorn noise is predominently a noise current, and sensitive to source impedance. 100 kΩ seems to be about the worst case condition for this noise." — *Paul Levesque.*

What about the op amps themselves?

Several years ago the proponents of both compensated and uncompensated op amps were each out to capture the entire market. Most designers today feel they need both.

"We chose, after a very painful selection process, to go with an uncompensated (301 type) op amp instead of a 741, even though we had to use a capacitor every time. Maybe in 90% of the applications the compensated op amp would have been ok, but it didn't offer that extra degree of flexibility — to make it a little faster or more stable." — *Garrett Myers.*

A few problem areas still exist

It isn't surprising, since there are so many op amps available, but, except for a few small details, most of the designers felt that op amps had taken great strides in the last few years. They had no loud or general complaints about the designs they were presently offered. FET input op amps did receive some rather mild criticisms, though.

"Being a systems house, we don't care to get involved in discrete designs, but last year I needed an FET input amplifier for a mass-spectrometer design. Across the board every FET input op amp — even the modules — went into oscillation in the mode in which I was using them. Capacitive-feedback schemes would stop the oscillations, but then the rise times just wouldn't make it. I went back to the manufacturers and asked what I was doing wrong, and they all said, 'Nothing, you can't stop the oscillation without losing speed' — but when I asked why I couldn't have access to some internal points for compensation, I found out that the marketing groups wouldn't let engineering do it. No one wanted to admit that their amplifiers needed external compensation. So in 1971 I had to design my own amplifier; that's unbelievable! When a salesman comes in now with an FET amplifier, I have him for breakfast. I can't be that unique now, and a lot of FET amplifier users must have run into my problem. Maybe they *can't* bring out the pin I need on a monolithic device, but on the square epoxy modules they could damn well do it." — *Irving Chase.*

"I build my own FET input op amps because I can do it cheaper for one thing, and because I don't want the input and outputs as close, physically, as they are on monolithic op amps." — *Ed Merrick.*

Cans are still the most popular packages

Again, because of their unusually stringent requirement, the designers at the roundtable usually specify metal cans for op amp packaging. They felt that the environmental hermeticity afforded by the metal containers more than offset the slight premium in price. However, none of them was involved with large volume production runs, so automatic insertion was not a factor in their decision. Plastic devices are under evaluation by all of the manufacturers represented, and they all feel that these packages have shown considerable improvement.

"There are plastic encapsulated devices that are extremely rugged. But that's a process that seems to be hard to control. Not everyone knows how to do it. Plastic can be a good heat conductor and should seal the leads very well. Any plastic encapsulated device will receive a very thorough evaluation before we'll use it. There is a dramatic difference from one manufacturer to another in plastic encapsulation." —*Dick Davis*.

Another interesting comment concerned the need for more power handling capability than is presently available in ICs.

"Power ICs are needed—buffers, servo-drivers and consumer circuits—but for that to happen we need a packaging breakthrough. The standard TO-3 can just isn't that attractive, but no one has a better answer yet." —*Garrett Myers*.

What would you like to see?

Are there improvements or new products you'd like to suggest to the manufacturers, we asked the participants of the roundtable.

"When I needed ±60V common-mode range with 10-ppm stability, I had to build it myself.

High-power buffers are another area that need enlarging. And I'd really like to have an overload indication from op amps. Perhaps they could monitor the input stages to know when the amp is out of its linear range. Plus or minus overload indication would be even more valuable. One of the biggest drawbacks to IC op amps has been thermal feedback. About 20-30 msec after you drive the output stage, the chip heats up enough to change the input-offset voltage by as much as 200-300 μV. Attempts to solve this problem have only begun." —*Dick Davis*.

"From what I see, there isn't any JAN IC program for linear devices like there is in the digital lines. They're going to have to get something like that going. Something along those lines would be ideal." —*Irving Chase*.

"Invariably with a high-speed op amp, I have to select the compensation capacitance for a given response. They really don't track too well; lots of times I end up with no capacitance—sometimes 10 pF, sometimes 20. It's a pain in the ____, if you have any volume at all." —*Frank Slater*. □

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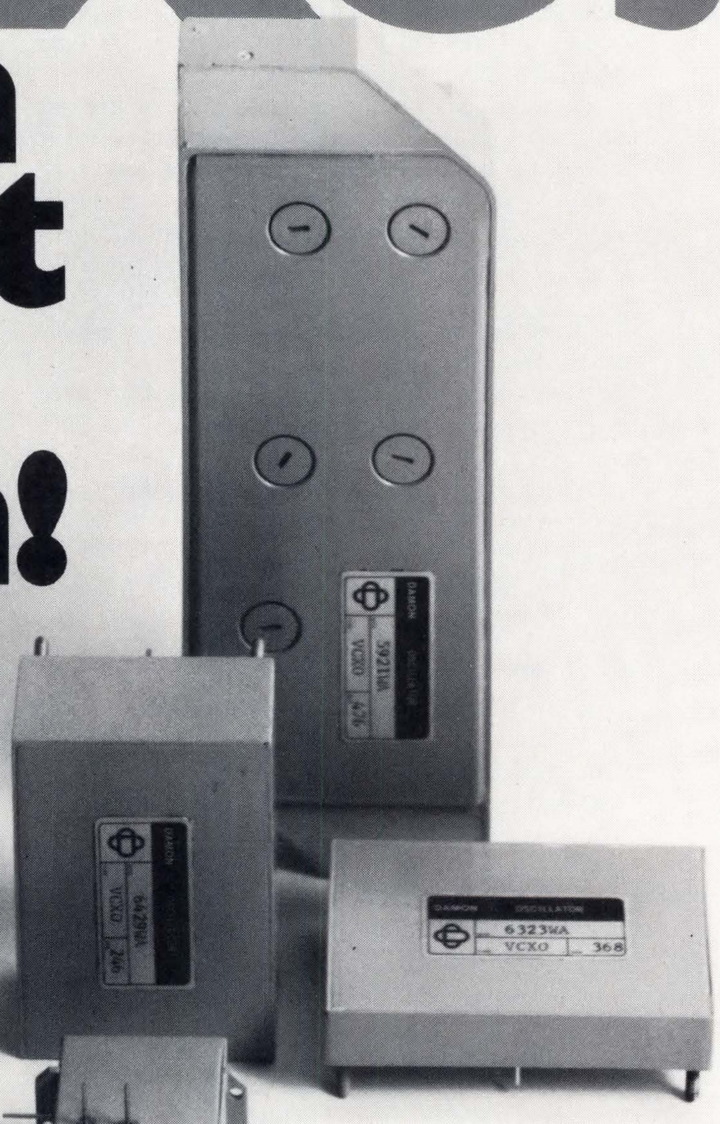

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SPECIFICATION GUIDE*

Parameter	Basic and Multiplier VCXOs	Mixer and Mixer-Multiplier VCXOs
Center Frequency	1 KHz to 300 MHz	100 Hz to 300 MHz
Frequency Deviation	±0.01% to ±0.25% of C.F.	±10 Hz to ±1 MHz
Frequency Stability 24 hr. @ 25°C	±1 to ±10 ppm	±0.5% of peak deviation
0 to 65°C (no oven)	±10 to ±50 ppm	±2% of peak deviation
Linearity	to within 1% of best straight line	to within 1% of best straight line
Minimum Deviation Rate	0 (dc)	0 (dc)
Maximum Deviation Rate	0.2% of C.F. (100 KHz max.)	10 KHz to 100 KHz
Mod. Voltage (Typical)	±5 V peak	±5 V peak
Mod. Input Impedance	>50 K ohms	>50 K ohms
Output Power Available	0.5 mw to 20 mw	0.5 mw to 20 mw
Load Impedance	50 ohms to 10 K ohms	50 ohms to 10 K ohms
Power Requirements (Typical)	−25 V ±1 V @ 30 ma	−25 V ±1 V @ 40-50 ma
C.F. Manual Adjustment Range	±0.01%	±5% of peak deviation

* Obviously, the limits are not absolute. The interrelationship of parameters for VCXOs are of such a nature as to permit optimization of any one or more characteristics to satisfy customer requirements.

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CHECK NO. 101

EDN DESIGN AWARDS

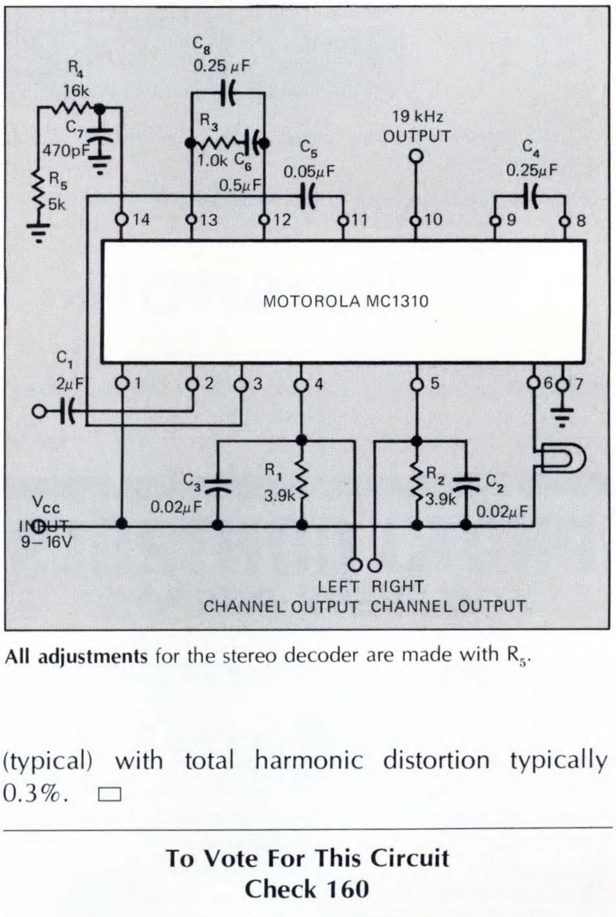
Phase-locked loop stereo decoder is aligned easily

Bruce Korth
Motorola Semiconductor Products, Phoenix, AZ

Stereo decoders normally incorporate LC filters both to provide 19 kHz selectivity and as part of a doubling circuit to generate the required 38 kHz subcarrier. One of the problems with these decoders has been system alignment, since it is necessary to adjust the coils very accurately to obtain maximum stereo separation. Even after obtaining the correct alignment, the problem of aging of the coils and temperature and humidity variations still exists.

A solution to the problem is the phase locked loop stereo decoder shown. The MC1310 requires only one adjustment, which is controlled by a potentiometer. The correct procedure for alignment is to open the input, pin 2, and monitor pin 10 with a frequency counter. The potentiometer is adjusted until a 19.00 kHz frequency reading is obtained.

For those having limited test equipment, a very simple procedure may be followed which will result in separation of within a few dB of optimum. This method consists of simply listening to a stereo broadcast and adjusting the potentiometer until the stereo pilot lamp turns on. Then the center of the lock-in range is found by rotating the potentiometer back and forth until the center of the lamp ON range is found. This method produces separation of 40 dB (typical) with total harmonic distortion typically 0.3%. □



All adjustments for the stereo decoder are made with R_5.

To Vote For This Circuit
Check 160

Convert a CMOS gate to a wide-hysteresis Schmitt trigger

Jim Halligan
Motorola Semiconductor Products, Phoenix, AZ

The threshold level of a CMOS gate can be varied by interconnecting the gate's input terminals. This variation in threshold level can be used to produce the hysteresis effect desired in a Schmitt trigger circuit.

Let us examine the transfer characteristics of a 3-input CMOS NAND gate with V_{DD} = +15V. With two inputs logically HIGH ($+V_{DD}$), the threshold of the third input is approximately 5V. When two inputs are tied together and driven in parallel, the threshold is about 7.5V. When all three inputs are tied together and driven in parallel, the gate threshold is about 8.5V. **Fig. 1** implements a Schmitt trigger with complementary outputs using a Motorola MC14023 triple 3-input CMOS NAND gate. It also shows the hysteresis loop actually obtained with this circuit.

With V_{in} = OV, the outputs of gates A and B are

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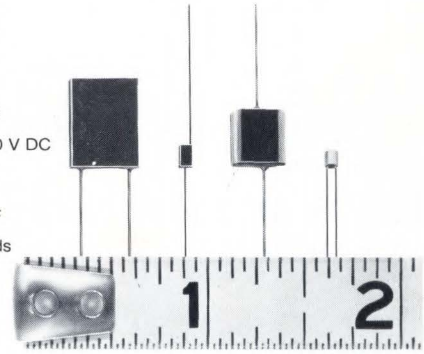

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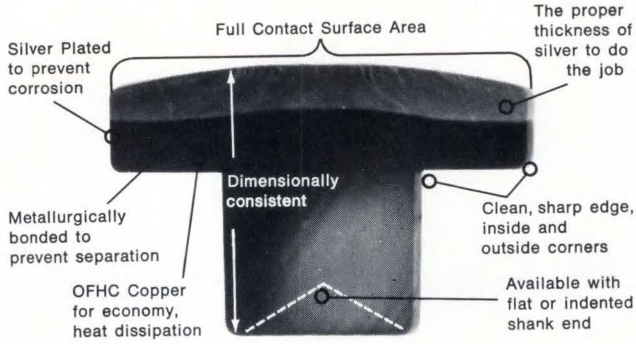

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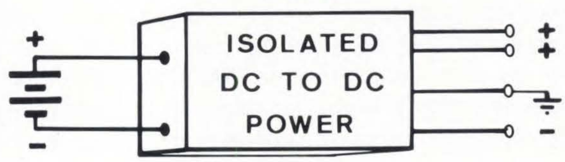

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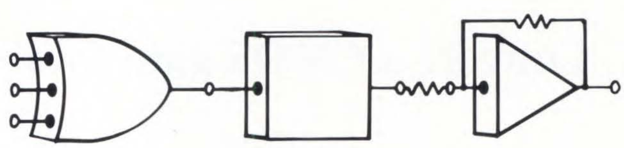

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HIGH, and the output of gate C is LOW. As V_{in} increases in magnitude, the cross-coupling between gates B and C will retain this condition until the input voltage is high enough to switch gate A, changing the state of the flip-flop. Since all of the inputs to gate A are driven in parallel, this occurs at the upper threshold level of 8.5V.

After the state change of the flip-flop, the output of gate C is HIGH. Thus, all but one of the inputs to gate B are held HIGH. As the input voltage decreases, gate A will revert to its original condition (output HIGH) with no effect. When V_{in} decreases to the lower threshold level of 5V, gate B will switch, returning the flip-flop to its original state.

The circuit retains a constant 25 to 30% of V_{DD} hysteresis over a wide range of V_{DD} from 5 to 15V. The lower threshold level is essentially fixed for a given V_{DD}, but the upper level is adjustable. For example, the upper level can be reduced to 7.5V by connecting one input of gate A to $+V_{DD}$ and applying the input signal to the other two gates (dashed curve in **Fig. 1**).

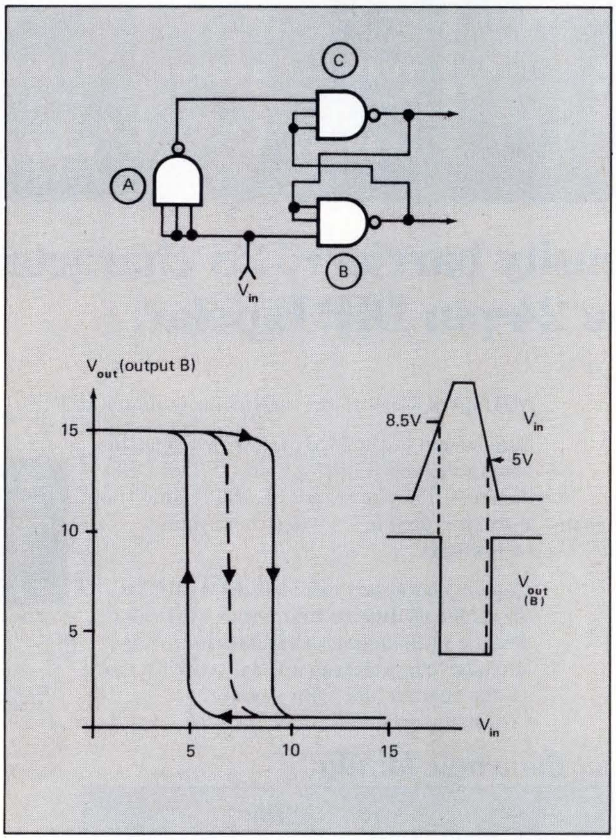


Fig. 1—A triple 3-input CMOS NAND gate connected as a Schmitt trigger (a). The gate is Motorola's MC14023. Its transfer characteristics as a Schmitt trigger (b) are shown. Note the hysteresis loop obtained from +5 to about +8.5V.

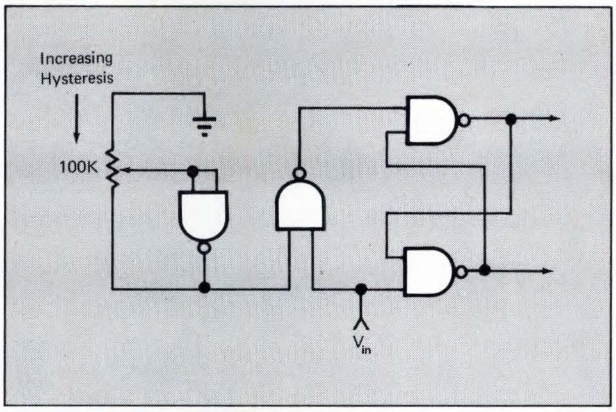


Fig. 2—A continuously variable upper-threshold-level Schmitt trigger can be obtained from a CMOS gate using a Quad 2-input NAND gate (Motorola's MC14011) and a potentiometer. This circuit can be adjusted from zero to approximately 50% V_{DD} hysteresis.

A continuously variable upper threshold level can be obtained using an additional MC14011 Quad 2-input NAND gate and a potentiometer, as shown in **Fig. 2**. This circuit can be adjusted from zero to approximately 50% V_{DD} hysteresis. Note that the value of the potentiometer used here is 100 kΩ. A larger or smaller potentiometer could be used here since absolute resistance value is not critical. However, the potentiometer is the only significant power-drain component in the circuit. Too small a potentiometer could mean an overly large power consumption. On the other hand, if the value of the potentiometer were made grossly larger, the resulting sensitivity of adjustment of hysteresis level would suffer. ▭

To Vote For This Circuit
Check 161

Differentiator circuit produces a relative change

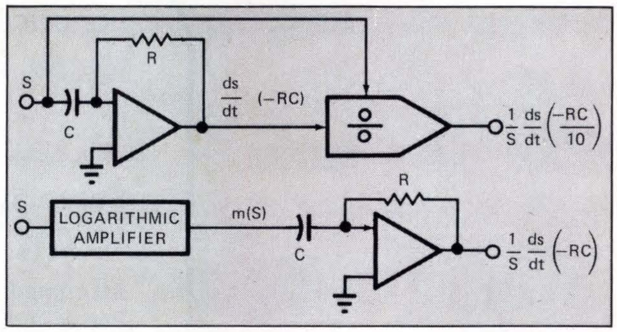
Fred W. Etcheverry
Southwest Regional Laboratory, Los Alamitos, CA

In simple differentiator circuits, a voltage is produced proportional to the absolute change of an input signal. However, it is often desirable to develop a voltage which is proportional to relative change. Such a relative-change circuit can be realized by feeding the input signal to a differentiator and dividing the output of the differentiator by the input signal, as shown (top circuit). This circuit, however, does not have the

accuracy within the dynamic range characteristic of signals with interesting relative change.

With the bottom circuit, the input signal is fed to a logarithmic amplifier. The output of the logarithmic amplifier, ln(s), is then fed to a differentiator. The differentiator's output, l/s (ds/dt) (-RC), is then proportional to relative change.

Logarithmic amplifiers can be purchased in modules or constructed from IC op amps by placing a transistor in the feedback loop. If a high degree of stability and accuracy is desired, transistors, such as Fairchild's μ726, and IC op amps, such as Fairchild's μA727, both fabricated on temperature regulated chips, can be used. □



Relative change from a differentiator circuit can be obtained with either of these two circuits. The top circuit, however, does not have the accuracy within the dynamic range of signals with interesting relative change. By using a logarithmic amplifier, as in the bottom circuit, this problem can be solved.

To Vote For This Circuit
Check 162

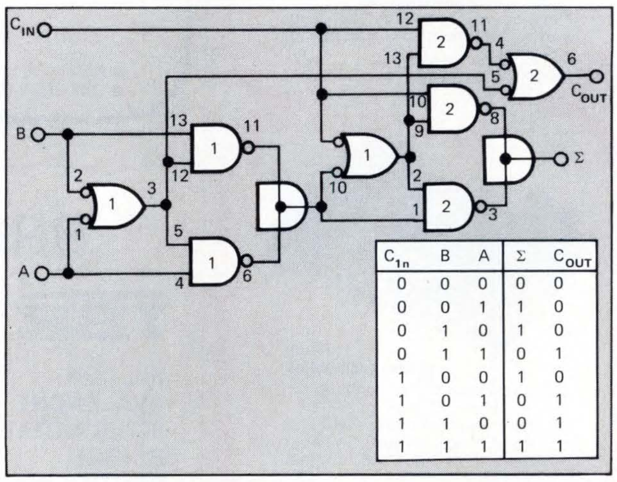
Quad NAND full adder uses two ICs

William Scott Dawson
Computer Science Corp., Huntsville, AL

If in these times of Medium Scale Integration (MSI) a discrete gate circuit can be considered compact, then that is the appeal of this NAND full adder.

Tucked neatly in two DTL packages, such as the MC846P, which is a quad 2-input NAND gate package, the circuit is easily cascaded on a printed circuit board. Two three-gate exclusive NOR's (EZ-1 and EZ-2) generate the sum, which is of course the same as odd parity for the three inputs (AB and C_{in}).

AB is available at EZ1 pin 3 to OR in EZ2-6, and $A\bar{B} + \bar{A}B$ appears at EZ1-8 to NAND in EZ2-11 with the input carry C_{in}. Thus, all inputs and outputs are ones, and no inverters are required for use with MSI counters having only true outputs. Of course, DTL must be used for the wired-AND function. Gates of EZ-1 are designated 1 on drawing and gates of EZ-2 are labeled 2. □



C_{In}	B	A	Σ	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Two DTL NAND-gate packages are all that is required for this full adder.

To Vote For This Circuit
Check 163

Circuit shifts asynchronous high-frequency clock sources

Scott C. Miller
Varian Data Machines, Irvine, CA

Switching between two asynchronous clock sources can be a hazardous event. The circuit shown reduces the hazard by allowing an asynchronous control signal to select between two asynchronous clock sources without producing narrow clocks or glitches and by minimizing the amount of clock time lost during a transfer.

In this circuit, there are three possible states and two possible stable states for flip-flops QA and QB (see Table). Assume that the circuit is in state 1, with the select control HIGH and clock source A enabled

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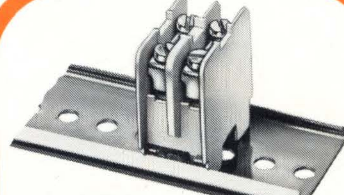

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CHECK NO. 107

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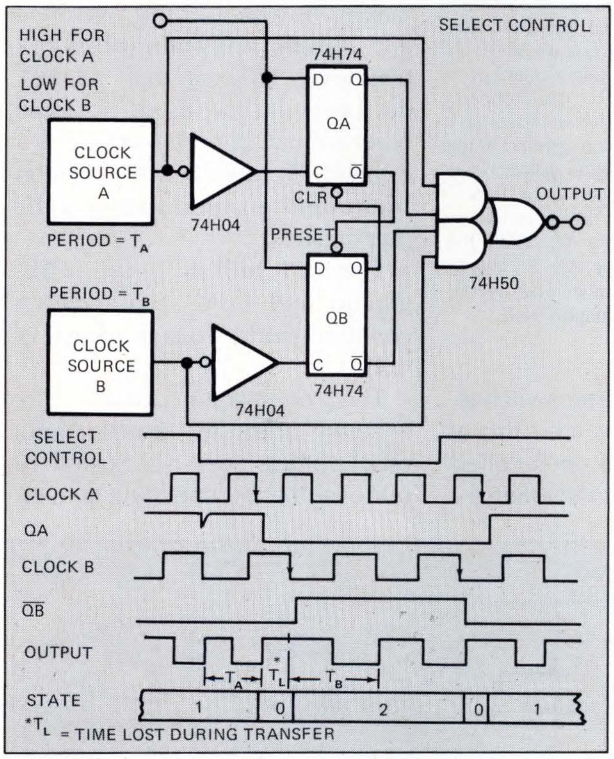
CHECK NO. 61

State	QA	QB	Condition
0	0	0	State during moment of transfer (unstable)
1	1	0	Clock source A selected
2	0	1	Clock source B selected
3	1	1	Illegal state (unstable)

to the output. When the select control transitions to LOW, flip-flop QA will synchronously (with clock A) inhibit clock source A to the output and will release, or enable, the dc preset terminal on flip-flop QB. After flip-flop QA has released flip-flop QB, flip-flop QB will synchronously (with clock B) enable clock source B to the output. Flip-flop QB will now hold flip-flop QA in the reset state. The circuit is now in state 2 and will remain in state 2 until the select control goes HIGH again.



The "select control" signal determines which clock source is delivered to the output. This is done without either glitches or shortening of the output clock pulses.

Flip-flops QA and QB are interlocked in such a manner that one flip-flop must complete a synchronous disable of its clock before the other can perform the synchronous enable of its clock. Returning to state 1 occurs in the same manner as above, establishing a clean, glitch-free transfer between two asynchronous clock sources. The average time lost during a transfer is about one-half clock period of the clock source being selected. □

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Dual, TTL-output voltage comparator combines high speed and excellent input characteristics

PROGRESS IN INTEGRATED CIRCUITS

If you have ever searched for a very fast, high gain transistor, you know the combination does not come easy. In fact, when you scan transistor selection guides, you see that you must usually trade speed for h_{fe}, or visa-versa. A good rule of thumb for finding a fast transistor from a selection guide is to look for the ones with low h_{fe} in that column of the guide. Among the low-gain transistors there are both cheap ones and fast ones.

A similar tradeoff is usually necessary in choosing a high-speed comparator, especially where input performance is critical. Higher speed most often means heavier input currents.

Combining Schottky gating with high-performance linear processing, Signetics Semiconductor Corp. now offers dual comparator ICs that combine good input performance with the lowest propagation delay of any TTL comparator to date. **Fig. 1** shows the new NE521 in action. The 521 has a totem-pole output capable of driving 10 TTL loads directly. Notice the "glitch" in the rising edge of the 521's output in **Fig. 1**; it is evidence of the "active-base pull-down" circuit used to improve the rise time. This pull-down configuration is shown in **Fig. 2**. There is a circuit description with the caption which may be useful as a design idea. The circuit decreases the turn-off storage time of the output transistor. Perhaps this concept might be useful in speeding up discrete transistor switches.

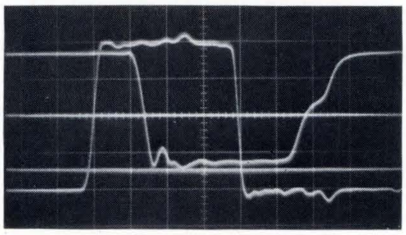


Fig. 1—Here superimposed are drive and response signals for a 521 comparator with a 15-pF load. The drive signal (square positive-going) is ±100 mV on the comparator's inputs. The output trace is shown at 1 volt/div with the reference ground trace also shown. The time base setting is 5 nsec/div. Propagation delay for a 1 to 0 transition is about 7 nsec; the delay for the 0 to 1 transition is about 10. With the open-collector version, the NE522, the 0-to-1 transition time is slower and dependant on the resistive termination used.

Signetics' NE522 is the same as the 521, except it has open-collector outputs to enable AND-tieing.

Performance and versatility

The 521 will operate at 50 MHz; the open-collector 522 can be used at 30 MHz. The 521 and the 522 propagation delay, from comparator inputs to the Schottky gate output, is a mere 10 nsec maximum with 100 mV overdrive and 20 nsec maximum with 5 mV overdrive. To beat that, an ECL device could be used, or some other animal, but the 521/522 is a 10-load TTL device with common strobe and enable inputs on the output gate.

The 521 and 522 use +5V, ground and −5V. That gives a common-mode voltage range of ±3V.

The comparator inputs are Schottky transistor bases. Input offset voltage does not exceed 10 mV over the full operating temper-

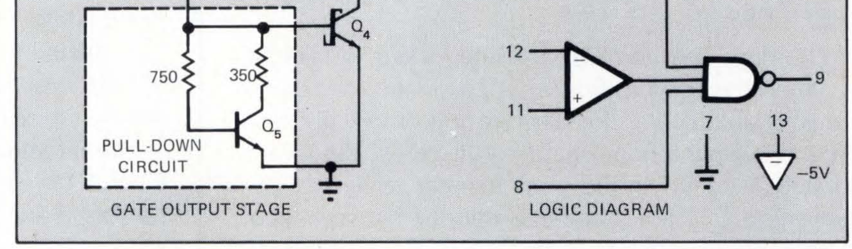


Fig. 2—The circuit is a curious mixture of Schottky and non-Schottky transistors, organized in three basic sections: video amplifier, high-speed level shifter and Schottky gate. Note the "active-base pull-down" transistor, Q_5. It decreases the turn-off time due to charge storage in the base of the output transistor, Q_4. For example, when the output is making a 0-to-1 transition, the base of Q_4 is actively pulled down by Q_5 through the 350 Ω resistor, depleting the stored base charge in Q_4. This speeds Q_4's turn-off time and improves the rise time of the gate.

ature range. Also specified over the full temperature range, input bias current is 40 μA max. and input offset current is at most 12 μA. Typical values of these parameters are, of course, much smaller (if you don't anticipate worst cases happening and don't use the full temperature range).

These performance characteristics make the new dual comparators useful for a host of applications, including MOS memory sense amplifiers (the pin configuration is compatible with the 75107), fast peak detectors, line receivers and many other comparator uses, common and unusual.

Both ceramic and plastic 14-pin DIPs are available. In ceramic, one will cost $5.25, and 1000 will cost $3.45 each. In plastic, one is $4.75 and 1000 are $2.95 each. Information requests on company letterhead only. *Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. Phone (408)739-7700.*

The quad 741 op amp is here in a 14-pin DIP

PROGRESS IN MICROCIRCUITS

Raytheon introduces the quad 741, four independent, high-gain operational amplifiers internally compensated and constructed on a single silicon chip.

Designated the 4136, the unit is a compactly designed, low-cost quad op amp featuring low heat dissipation, low noise and high impedance inputs.

The 741-type amplifier has long been popular because of its good performance record and low cost. The 4136's 14-pin dual in-line package can be used with standard pc board layout techniques and automatic insertion equipment.

The 4136 was conceived to be as simple in design and circuit layout as possible. It has two stages of voltage gain and a class AB complementary emitter follower output stage (**Fig. 2**).

The 4136's input stage is biased by a constant current source, thus stabilizing dc and ac parameters with wide variations in supply voltage. A current source was chosen in place of the usual resistive load for several reasons. First, it provides a method for getting single ended differential voltage gain; and second, the high output impedance of this input stage affords a convenient node for internal frequency compensation with a relatively small capacitor (one end connected to the base of Q_6).

The input bias current is 500 nA maximum. Furthermore, the PNP input configuration shown in **Fig. 2** performs level shifting with a minimum of noise-producing junctions.

The second stage, using Q_{10} as a current source, is Darlington configured to provide a high-gain common emitter stage.

The complementary emitter follower output stage is current protected by resistors R_6, R_7 and R_8.

The 4136 op amp meets or exceeds all specifications for 741 type op amps. It is suitable for applications in low-noise signal processing because of its low-

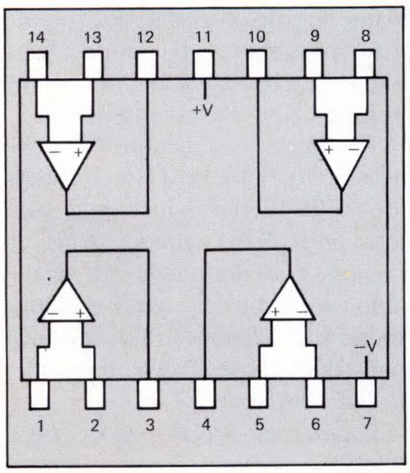


Fig. 1—The 4136 has low noise characteristics, making it suitable for transducer preamps and signal conditioning.

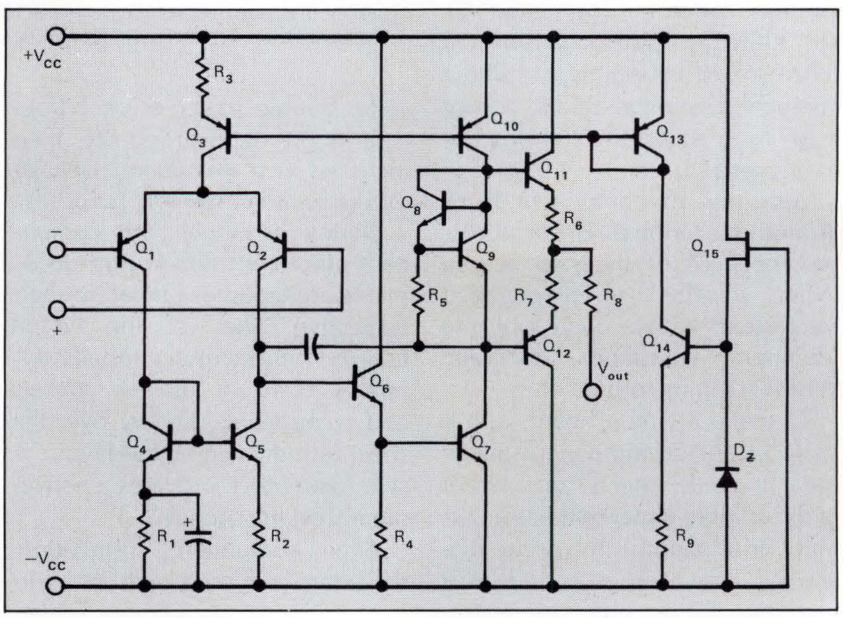


Fig. 2—The PNP emitter coupled pair used as the front end of the op amp has several advantages over the more common NPN pair. Since the lateral PNPs' emitter and collector are formed in processing at the same phase as the NPN base diffusion, breakdown voltages, BV_{ceo} and BV_{ebo}, of these PNPs exceed 90V. This makes it virtually impossible to overstress the input transistors.

noise PNP front end transistor.

Right now Raytheon is the sole manufacturer of the quad 741. Other manufacturers, however, may not choose to second source it with the same pin configuration. For instance, pin 7 is conventionally the negative supply input and pin 14 is the positive supply input. In Raytheon's 4136, pin 11 is the positive power input and pin 7 the negative power input. It is possible that the pin configuration of the Raytheon IC may not be the industrial standard, should the quad package become popular. The semiconductor industry has failed at times in the past to get their pinouts together.

Also, the input currents are opposite in polarity to those of most 741 op amps because PNP transistors are used rather than the usual NPN. This may have some effect on your circuit design.

The 4136 is now available from Raytheon distributors. The RC4136 DP (plastic) runs 1-100 @ \$2.08; 1000 @ \$1.76; 5000 @ \$1.05; 10k @ 98¢; and 100k for 80¢ each. RM136D (ceramic) runs 1-100 @ \$6.75; 1000 @ \$5.40; 5000 @ \$4.04; 10k @ \$3.86; and 100k for \$3.64 each.

Raytheon Semiconductor Div, 350 Ellis St., Mountain View, CA., 94040. Phone(415)968-9211.

For more information, check **169**

Water-soluble paper speeds assembly of printed circuit boards

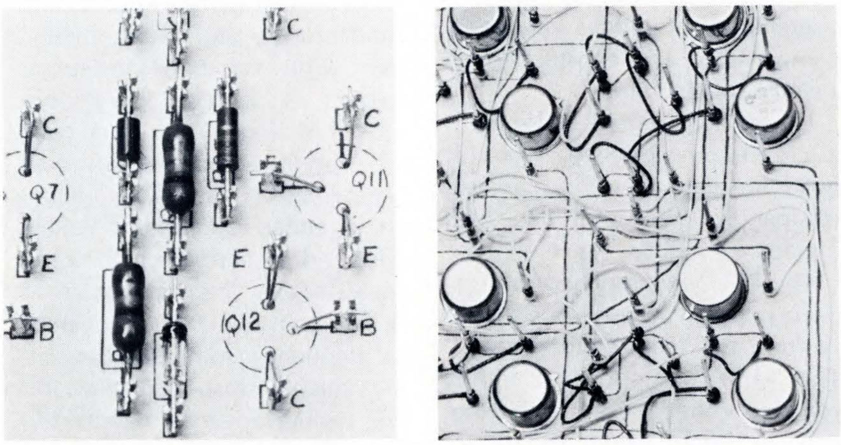
PROGRESS IN PACKAGING

Two new products from Vector Electronic Co. combine with Vector's prepunched tenth-tenth "P" pattern Vectorbord® to provide a novel circuit-board production technique.

One product is a water-soluble paper that can be used for component layout in the design phase and also as an assembly document in production. The other is a new terminal called a "Trifurcated" T-49 Klipwrap that combines a 0.025 square wrapping post with a clip-action terminal able to accept leads from 0.010 to 0.040 inches in diameter.

Wrapping of component leads around the terminal is not necessary because of the clip action. When installed in prepunched Vectorbord with a hand tool, the terminals withstand automatic Wire-Wrapping torque.

To make a circuit board, a full-scale layout of component placement is made directly on a sheet of the soluble paper that has a 0.1-inch grid pattern. A wiring diagram is drawn on a second sheet with the wiring posts in mirror-image relationship to the component layout.



Assembly diagrams printed on water-soluble paper are placed directly on both sides of circuit board to speed assembly and minimize errors.

Copies of the original drawings, made by offset printing on plain water-soluble paper or on Xerox-type 4000 duplicators, are then included in a document package for production assembly purposes.

During assembly, the component placement and wiring documents are taped or pinned to their respective sides of the circuit board. The assembler installs terminals (T-49 or others), sockets and components directly over the sheet as indicated by the layout. A styrofoam block provides a convenient working surface.

After component installation, the board is turned over and wiring is done by wrapping or soldering as indicated by the attached wiring diagram. Because the assembler is looking at the documentation and the work at the same time, fewer errors and greater speed should result.

Finally, the board is rinsed in water to dissolve the document. Any components that are subject to damage by water are, of course, installed after rinsing and drying.

The paper is available in packages of 50, 8-1/2 × 11-inch sheets for \$5.95 with 0.1-inch grid pattern and \$5.50 without grid for copies. T-49 terminals are available with tin or gold plating. Prices are \$20 per 1000 and \$27 per 1000, respectively, in quantities of 1000 to 4000.

Vector Electronic Co., Inc., 12460 Gladstone Ave., Sylmar, CA 91342 Phone(213)365-9661.

For more information, check **168**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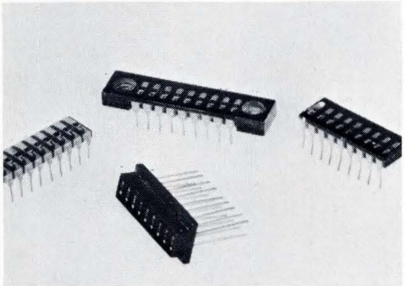


PHOTOTRANSISTOR TAPE READER ARRAYS INTRODUCED. These standard arrays employ 9 optically isolated, high sensitivity phototransistor detectors, encapsulated in clear epoxy resin and mounted on a ceramic substrate. The NSL-2565 array is unique in that mounting/locating holes are provided to assure precise registration between the detector head, its light source and the punched tape. National Semiconductors Ltd., 331 Cornelia St., Plattsburgh, NY 12901. Phone(518)561-3160. **207**

TTL BUS BUFFER GATES OFFERED. Improved versions of 2 TTL quad bus buffer gates have been introduced. They are the SN54/74125 and the SN54/74126. The new TI circuits feature reduced propagation delays and improved output disable times. The average propagation delay time has been reduced 2 nsec. When enabled, the three-state output performs the same as a TTL totem-pole output and provides sharp rise times even when driving highly capacitive loading such as bus lines. The output of the 125 is enabled when the control input is low, and the 126 output is enabled when its control is high. Texas Instruments Inc., 13500 N. Central Expressway, Dallas, TX 75222. Phone(214)238-2011. **208**

SCHOTTKY TTL CLOCK IS STABLE. The CO-238 DIP compatible crystal oscillator is now available at frequencies up to 100 MHz to drive Schottky TTL logic. It operates from 5V dc, drives 10 TTL loads and plugs into a 14-pin DIP socket. The standard CO-238 provides stability of ±0.0025% over 0°C to 70°C. Vectron Labs., Inc., 121 Water St., Norwalk, CT 06854. Phone(203)853-4433. **209**

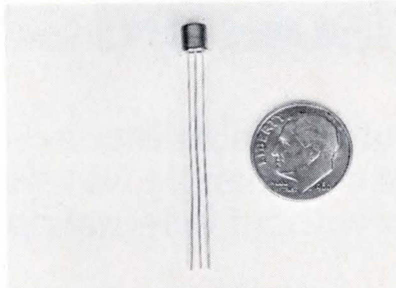
HIGH-SPEED OP AMP IS SUPER STABLE. The Am118, which is pin compatible with the like numbered circuit from National Semiconductor, features (all values are typical): slew rate—70 V/μsec; input offset voltage—2 mV; input bias current—120 nA and offset current—6 nA. The device has a 15 MHz small signal bandwidth and operates over a ±5 to ±120V range. Prices for the amplifiers in the 100-up quantity are: Am118 (TO-5), (−55°C to + 125°C) $19.95 and Am318 (TO-5), (0°C to +70°C) $4.95. Advanced Micro Devices, Inc., 901 Thompson Pl., Sunnyvale, CA 94086. Phone(408) 732-2400. **210**

8-BIT D/A HAS INTERNAL REGISTER. Model MN328B contains an input storage register, monolithic switches, precision ladder network, internal reference and operational amplifiers. The unit is housed in a hermetically sealed 16-pin DIP package and requires only ±15V supplies and a +5V supply. The input circuitry is TTL compatible, and the output voltage is linear to 1/2 LSB over the operating temperature range of 0°C to 70°C. Storage temperature is −55°C to +125°C. The MN328B has an ouput voltage of +5 to −4.91V. Price on the MN328B is $41 each in 100 quantity. Micro Networks Corp., 5 Barbara Lane, Worcester, MA 01604. Phone(617)756-4635. **211**

HEX AND QUAD D-TYPE FLIP-FLOPS TOGGLE AT 110 MHz. S54S/74S174 hex and S54S/74S175 quad flip-flops utilize Schottky TTL technology. All have a direct clear input, and the 175 features complementary outputs from each flip-flop. Pin assignments are identical to the standard TTL versions. Prices are expected to be slightly more than $5 per unit when purchased in lots of 100. Signetics, 811 E. Arques Ave., Sunnyvale, CA 94086. Phone(408)739-7700.

pROMs ASSEMBLE PROGRAMS FOR MICRO COMPUTERS. The 4 pROMs (AO-740, 741, 742 and 743) plug into the prototyping board for the MCS-4 micro computer and perform all the functions of a Fortran IV assembler, eliminating all need for a general-purpose computer. Price is $364 for the set of 4 assembler pROMs. Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051. Phone(408)246-7501. **212**

MOS pROM PROGRAMS 10 TIMES FASTER. Intel Corp. has introduced a 2048-bit erasable static MOS pROM that programs in 2 minutes, 10 times faster than any other MOS pROM on the market. Designated 1702A, the new pROM may be programmed in the field using Intel's Model 7600C tape actuated programmer. It may then be erased like its predecessors by shining ultraviolet light through a transparent quartz cap on the package. The pROM may be erased and reprogrammed as often as desired without impairing its performance. The 1702A has a maximum access time of 1 msec. It may be replaced at any time by a pin-compatible mask programmed ROM, Intel 1301. Price is $45 in 100-piece quantities. Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051. Phone(408)246-7501. **213**



WORLD'S SMALLEST RADIO RECEIVER. The ZN414 dramatically reduces the cost and size of a radio receiver. All that is required to produce a radio receiver capable of covering medium and long wavebands is the ZN414, a battery, an aerial, a speaker, two resistors, a tuning and two fixed capacitors. Ferranti Electric Inc., E. Bethpage Rd., Plainview, NY 11803. Phone(516)293-8383. **214**

10 DEVICES ADDED TO 54C/74C CMOS FAMILY. Following are the 10 new 54C/74C with 100-up pricing in epoxy packages: MM74CO4/MM64CO4/MM/54CO4 Hex Inverter, $1.15; MM/74C73 Dual J-K Master-Slave Flip-Flop, $2.51; 74C76 Dual J-K Master-Slave Flip-Flop, $2.51; 74C74 Dual "D" Flip-Flop, $1.62; 74C107 Dual J-K Master Slave Flip-Flop, $2.51; 74C160 Synchronous Decade Counter, $6.35; 74C161 Synchronous 4-bit Binary Counter, $6.35; 74C162 Fully Synchronous Decade Counter, $6.35; 74C163 Fully Synchronous 4-Bit Binary Counter, $6.35; 74C195 4-Bit Parallel Access Shift Registors, $4.16. Letterhead inquires only. National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051. Phone(408)732-5000. **215**

AMPLIFIERS IMPROVE PERFORMANCE OF MULTIPLIER/MODULATOR. The XR-2208 contains a 4-quadrant multiplier, operational amplifier, buffer amplifier and bias regulator. With a few passive components it performs analog arithmetic computations such as multiplication, division and square-root extraction. As a communications signal processor, it will modulate, demodulate, detect, mix and amplify (or amplify with automatic gain control) over a wide frequency range in AM, double-sideband, supressed-carrier and phase-shift systems. The buffer increases the 3-dB bandwidth of the multiplier to 10 MHz (versus about 1 MHz for conventional multipliers) and decreases output impedance to 50Ω. The supply range is ±4V to ±15V. Input voltage range is ±6V. Exar Integrated Systems, Inc., 750 Palomar Ave., Sunnyvale, CA 94086. Phone(408)732-7970. **216**

SEMICONDUCTORS

MINIATURE SILICON RECTIFIER BRIDGES. This second generation of single phase miniature silicon rectifier bridges boasts a PIV range of from 50 to 1000V. The average dc output of the new Junior Mini-bridge has been upgraded from 8 to 12 A and the peak surge rating from 100 to 150A at no increase in cost. Electronic Devices, Inc., 21 Gray Oaks Ave., Yonkers, NY 10710. Phone(914)965-4400. **217**

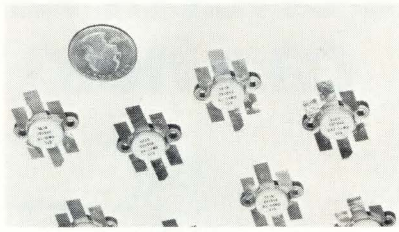
TRIAC SERIES RATED AT 6, 8 AND 10A, AT 85°C. Each of the 3 series is available in 6 voltages (V DRM) 100 to 600V. Half cycle on-state surge current is 66, 88 and 110A, respectively. Gate trigger current is 50 mA at 25°C, gate trigger voltage is 2.0V at 25°C. Prices range from $1.84 to $5.45 in 100 quantity. Sarkes Tarzian, Inc., Semiconductor Div., 415 N. College Ave., Bloomington, IN 47401. Phone(812)332-1435. **218**

4-BIT TTL PRIORITY REGISTER replaces 6 SSI packages. Designated the SN54/74278, this IC consists of 4 input data latches and 5-line priority decoder, in a single package. The fifth priority decoder input permits implementation of cascading circuitry so that a number of these registers can be connected to perform N-line priority decoding. Price of the SN74278N is $2.70 in 100-piece orders. Texas Instruments Inc., Box 5012, Dallas, TX 75222. Phone(214)238-3741. **219**

FIRST SEMICONDUCTOR ABSOLUTE PRESSURE TRANSDUCER replaces electromechanical devices. The LX1600A is expected to have a wide range of applications in fuel metering and ignition controls, heating, refrigeration, automotive safety and diagnostic controls. It is priced at $70 in 1 to 99 quantities and $58 in 100-up quantities. National Semiconductor Inc., (Letterhead inquires only), 2900 Semicondcutor Dr., Santa Clara, CA 95051. Phone(408)732-5000.

RF TRANSISTOR KIT DELIVERS 100W With 20 dB GAIN. This 2-stage kit, in ceramic packages, has a low input Q for better broadband capability. Used in class "C" operation, at 150 MHz, 40V, it will deliver 100W with 20 dB min. gain. This family of devices is also suitable for 28V operations. Nichrome resistors are used for stabilization and durability. Delivery: 6-8 weeks ARO. Dertron Inc., 7516 Central Industrial Dr., Riviera Beach, FL 33404. Phone(305)848-9606. **221**

SEMICONDUCTORS



COMMUNICATIONS TRANSISTOR DELIVERS 75W AT 400 MHz. The devices are specifically designed for operation in Class A, AB, B, or C broadband or narrowband applications covering the frequency range of 200 to 500 MHz. The three transistors in the series are rated at 20, 40 and 75W, all designed for extremely rugged service. An alternate 75W transistor is also available for high power CW or pulsed operation, or as a linear transistor. When operated in a series of one 3W, one 20W and two 75W transistors, an output of 150W can be obtained from a 0.2W input. Prices in quantities of 1 to 99 are: 20W device, $45; 40W device, $90 and 75W device, $135. Communications Transistor Corp., 301 Industrial Way, San Carlos, CA 94070. Phone(415)591-8921. **222**

5-BIT MONOLITHIC SWITCH SAVES COST and space in 10-bit conversion. Model AD552 has been introduced for building precision 5- and 10-bit A/D and D/A converters. Until now designers either graded and selected their own discrete transistor switches or used a matched triplet of 4-bit current switches, such as the AD551, to obtain 10-bit resolution and accuracy. The switch circuitry is geometrically proportioned to attain virtually perfect V_{BE} matching and tracking in the recommended circuit configurations. The AD552 requires complementary binary input coding, features an MSB output current rating of 2.0 mA and settles to 0.05% (±1/2 LSB) in 120 nsec. Analog Devices, Route 1 Industrial Park, P.O. Box 280, Norwood, MA 02062. Phone(617)329-4700. **223**

THE WORLD'S FIRST RADIO TRANSMITTER ON A CHIP, is designated the LP2000 "microtransmitter". The device produces 100 mW pulse modulated, or 50 mW amplitude modulated at 27 MHz from a high stability, regulated monolithic oscillator using external crystal control. The circuit operates from +15 down to +3V supplies. The LP2000 is priced at $12.50 in quantities of 100. Lithic Systems, Inc., P.O. Box 869, Cupertino, CA 95014. Phone(408)257-2004. **224**

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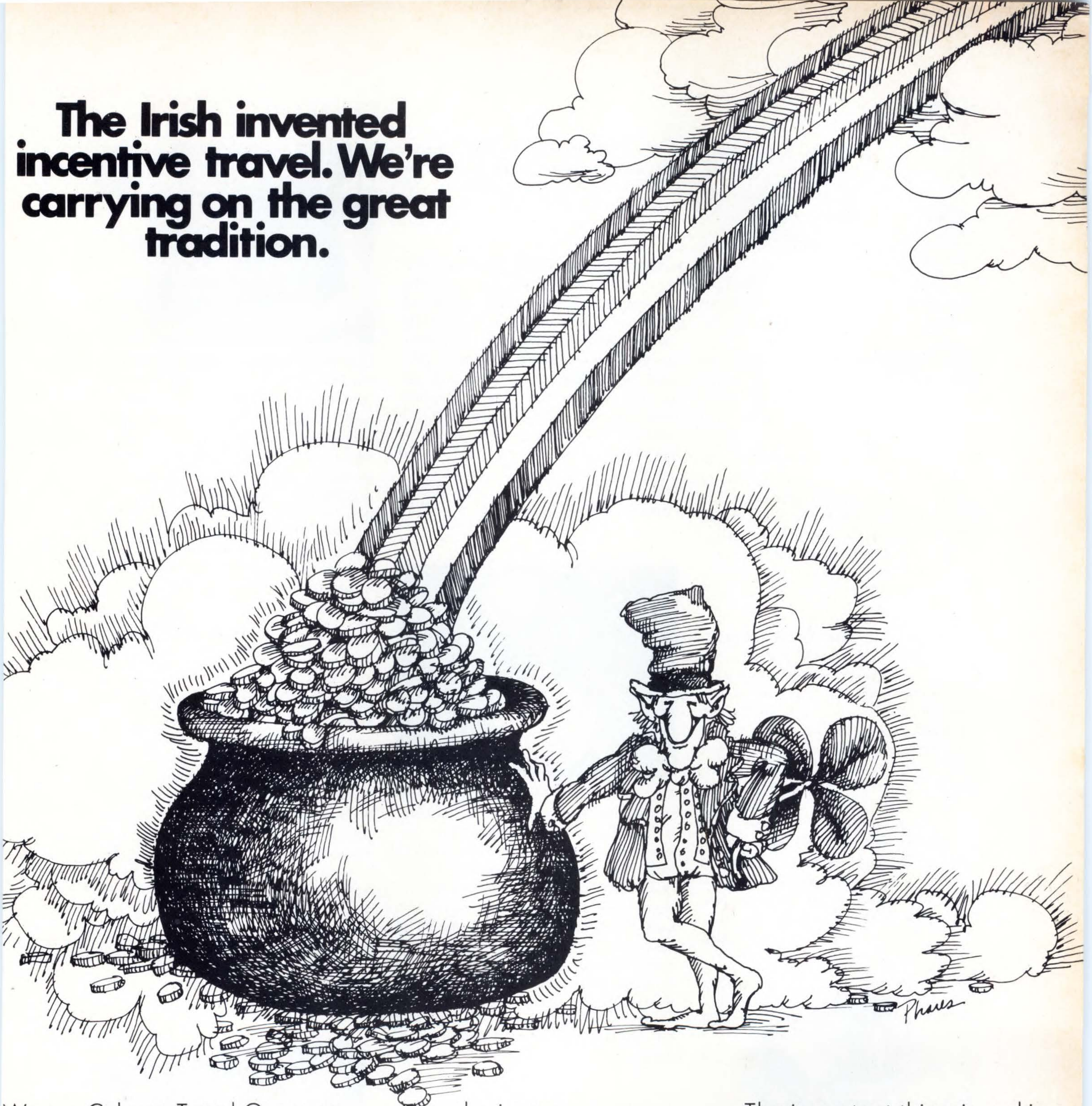

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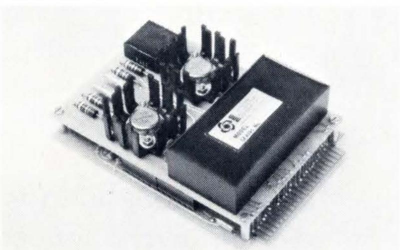
MINIATURIZED MODULAR AMPLIFIER FOR MICROSTRIP CIRCUITRY. The Model AH-52 modular microstrip amplifier operates at a frequency of 10 to 500 MHz and has a nominal gain of 14 dB at 16V dc. A major feature of this modular amplifier is its high reliability—it has an MTBF of 1.44×10^6 hours/MIL-Handbook 217A. Specifications include a noise figure of 5 dB and output power at 1-dB gain compression of +10 dBm. $75. Optimax, Inc., Box 105, Advance Lane, Colmar, PA 18915. Phone(215)822-1311. **225**

16-BIT D/A $350 CONVERTER HAS LINEARITY ERROR OF 0.003%. The DAC45 is a new 16-bit D/A converter which features linearity error of 0.003%, max., drift of only 1 ppm/°C for offset, 1 ppm/°C for linearity and 5 ppm/°C for gain. The current output of this modular unit settles to 0.003% in less than 10 μsec while the voltage output settles in 50 μsec. The linearity error of the DAC45 is only 0.003%. The DAC45 can operate over a ±3°C temperature range with less than one part in 65,000 error and over a ±10°C range with less than one part in 16,000 error. Burr-Brown Research Corp., International Airport Industrial Park, Tucson, AZ 85706. Phone(602)294-1431. **226**

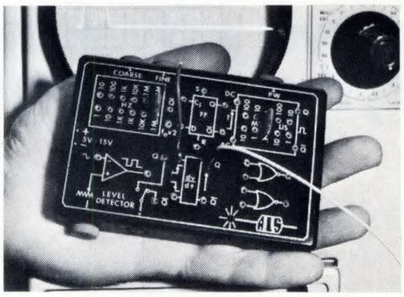


SOLID-STATE LINEAR-ANGLE dc-TO-SYNCHRO CONVERTER. A series of new modular solid-state linear-angle dc-to-synchro converters convert dc information representing angle into 3-wire synchro outputs with a standard accuracy of ±30 minutes of arc. The converters are available with dc inputs of ±10V or ±100V, corresponding to a ±180° of angle. Synchro voltage outputs of 11.8V line-line and 90V line-line at 400 Hz, or 90V line-line at 60 Hz are available. The units can drive loads up to 75Ω line-line at 11.8V, and 4000Ω line-line at 90V. Prices in production quantities are less than $800 each. Computer Conversions Corp., 6 Dunton Ct., E. Northport, NY 11731. Phone(516)261-3300. **227**

FLATPACK SOLID-STATE SWITCH DRIVER. A SPDT switch driver which provides switching input to p-i-n diode switches and is fully compatible with both TTL and DTL circuits is Model SD-2101. The new driver provides 2 outputs from a single input and is used for driving shunt, series and series/shunt switches. It has a total switching time of less than 1000 nsec (from 50% TTL input gate to 90% current output) and operates from +5 and −12, +5 and −15, and ±5 and ±12V inputs. $75. LRC, Inc., 11 Hazelwood Rd., Hudson, NH 03051. Phone(603)883-8001. **229**

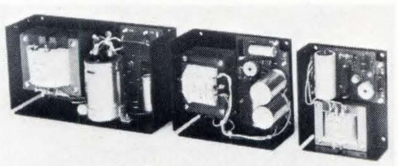
TO-5 SWITCH DRIVER. A miniaturized switch driver, packaged in a TO-5 transistor can, permits any coaxial or waveguide electromechanical switch to be driven from TTL gates. The relay driver (Model SD-1601) drives electromechanical switches by providing either a low-impedance (logic 1) or a high-impedance (logic 0) path to ground for the switch solenoid. Model SD-1601 switch drivers are designed for operating under stringent military environments and over temperatures ranging from −55°C to +125°C. $22. LRC, Inc., 11 Hazelwood Rd., Hudson, NH 03051. Phone(603)883-8001. **228**

SYNCHRO-TO-LINEAR dc CONVERTERS. Series B678 compact solid-state units convert all standard synchro or resolver inputs to a linear dc voltage that is proportional to the input shaft angle. Accuracies of ±6 minutes at 25°C and ±10 minutes over the temperature range of −55°C to +85°C are available. This series offers infinite resolution, does not require adjustment of any kind, is short-circuit proof, is available either for pc-board mounting or connector termination and is fully transformer isolated. All models are hermetically sealed. $595. Transmagnetics, Inc., 210 Adams Blvd., Farmingdale, NY 11735. Phone(516)293-3100. **230**

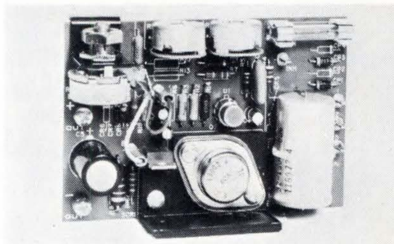


COS/MOS PULSE GENERATOR MODULE. The COS/MOS-compatible pulse generator, Model 727, is a small module that offers frequencies from 1 Hz to 1 MHz and pulse widths from 1 μsec to 100 msec. Additionally, a level detector, a non-capacitive differentiator, a NOR gate, a "D" flip-flop and a pushbutton are provided. Q and $\overline{Q}$ outputs and complementary inputs allow the synthesis of a wide range of digital functions. Powering is either by the circuit under test or from its own supply (3 to 15V) which has up to 50 mA available for powering external circuitry. $125. American Laser Systems, Inc., 3888 State St., Santa Barbara, CA 93105. Phone(805)687-1212. **231**

LOW-COST MINIATURE POWER SUPPLIES. A new line of low-cost, modular power supplies includes single-, dual- and triple-output units available at prices ranging from $16. Fifty four different models are featured, including a miniature series which is packaged into a 2×2×0.4-in. DIP-compatible model. Supplies are offered to include a wide range of input voltage requirements—115, 100 to 230 and 250V ac and 5, 12 and 28V dc. Output voltages of 5, 200 and ±15V at current ratings ranging from 20 to 1000 mA are available. Most models feature regulated outputs. Zeltex, Inc., 1000 Chalomar Rd., Concord, CA 94520. Phone(415)686-6660. **232**



OEM OPEN-FRAME POWER SUPPLIES. The M Series line is initially available in 3 sizes covering 7 voltages, with corresponding current ratings. Standard voltages cover the range of 4.5 to 26V, with currents as high as 12A in lower-voltage ranges. Regulation is by means of ICs, thus minimizing parts required and increasing reliability. OEM unit costs are $29 for the MA size; $45 for the MB size; and $72 for the MC size. Combined quantity discounts are available. Dynage, Inc., 1331 Blue Hills Ave., Bloomfield, CT 06002. Phone(203)243-0315. **233**



SUB-MODULAR POWER SUPPLIES CUT CUSTOM/IN-HOUSE COSTS. A new series of sub-modular dc power supplies, the SM Series, provides the user with a "building-block" concept. The basic building block is a sub-modular supply with an exclusive built-in rectifier, filter, regulator and protective functions. The other building blocks include an ac transformer, wiring harness, heat sink for the sub-module(s) and a mounting chassis or case if desired. Powertec provides any one or all of the "building blocks." Prices are up to 90% lower than other power kits which still require the user to add design, labor and test costs. Powertec, Inc., 9168 DeSoto Ave., Chatsworth, CA 91311. Phone(213)882-0004. **234**

MINIATURE HIGH-PERFORMANCE ac-TO-dc POWER SUPPLY. A new series of miniature ac-to-dc power supplies, the Series 800, come in epoxy cast modules measuring 1.25×2×3 in. and weigh 19 oz. They feature input voltage of 105 to 125V rms (0.75A), 50 to 400 Hz, a single-output voltage of +5, −5, +28, and +30V dc, dual-output voltages of ±6, ±10, ±12 ±15, ±18, and ±24V, accuracy of 0.05V dc, and zero-to-full-load regulation of 0.02%, max. Line regulation is ±0.05%; ripple is 0.5 mV rms max.; and operating temperature is 0°C to +71°C. From $63 for single-output models. Anadyne Div. of California Linear Circuits, 12741 Los Nietos Rd., Santa Fe Springs, CA. Phone(213)698-7991. **235**

TINY HIGH-PERFORMANCE POWER SUPPLY. An output of +5V dc at 1A, 0.05% line regulation, 0.1% load regulation and less than 1 mV rms ripple and noise in less than 11 in.^{3} (2.5×3.5×1.25 in.) are the basic specifications of the Model 21-1000 power supply. The 110/220V ac unit has unregulated power separately available to drive lamps, relays and recorders without loading the regulated power. A specially designed low-profile transformer gives outstanding isolation. $48. Calex, Box 555, Alamo, CA 94507. Phone(415)932-3911. **236**

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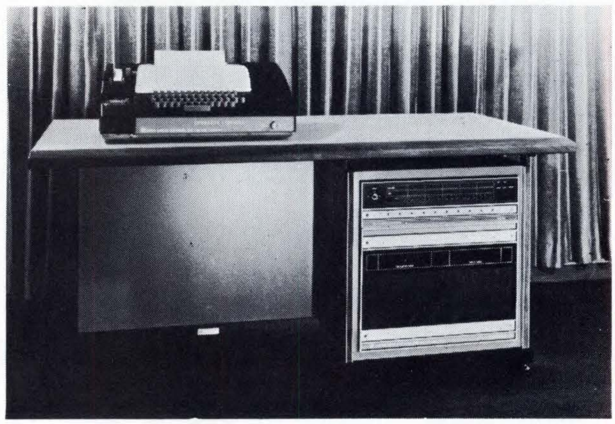

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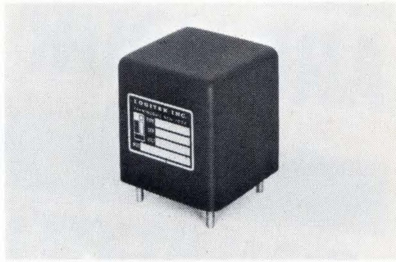
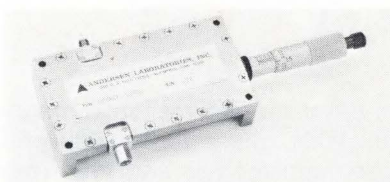
CIRCUITS



Ac POWERED FREQUENCY SENSOR, Type FS, de-energizes electrical systems or activates alarm systems when the power-line frequency varies above or below pre-specified limits. The new sensor is available with ±5% accuracy, an input operating voltage (nominal ac) of 120/208 or 115/200V rms±20%, input operating frequency (nominal) of 60/400 Hz±20% and dpdt or 3 pdt output contacts. Contact rating is 2 to 10A resistive and operating temperature is −55°C to +125°C. Logitek, Inc., 42 Central Dr., Farmingdale, NY 11735. Phone(516)694-3080. **237**

FRACTIONAL-HORSEPOWER MOTOR CONTROL. A new solid-state motor control for use with fractional-horsepower electric motors is Model 4001 which is designed for use with motors up to 1/8 hp and is available in ac and dc models. Built-in feedback sensing of the control operates over its full-wave capability. The unit measures 3-3/8×3-3/4×1-1/4 in. and weighs 7 oz. Circuitry is compatible with either shunt-wound or permanent-magnet motors. Dc models are available in 105 or 210V armature and field. Ac models are available in 115 or 230V, 50 or 60 Hz. Contronics, Inc., 2629 Johnstown Rd., Columbus, OH 43219. Phone(614)471-6466. **238**



LINEAR MICROWAVE PHASE SHIFTER. A new series of linear phase shifters operates at frequencies up to 2.5 GHz. Mechanical phase adjustment is through a unique micrometer on Models 1000 and 2500, with Model 500 using a screwdriver adjustment. All models are fitted with a locking device. Linearity is ±1/2°, and insertion loss is 0.2 dB at 2.5 GHz. Very precise control of phase is provided through the calibrated micrometer, with 5 electrical degrees per mechanical turn. \$500. Andersen Laboratories, Inc., 1280 Blue Hills Ave., Bloomfield, CT 06002. Phone(203)242-0761. **239**

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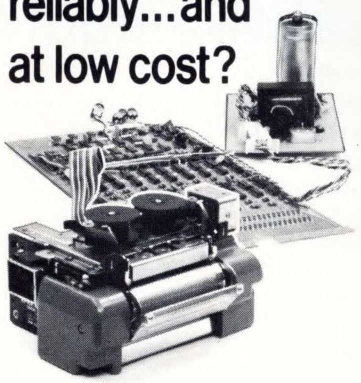

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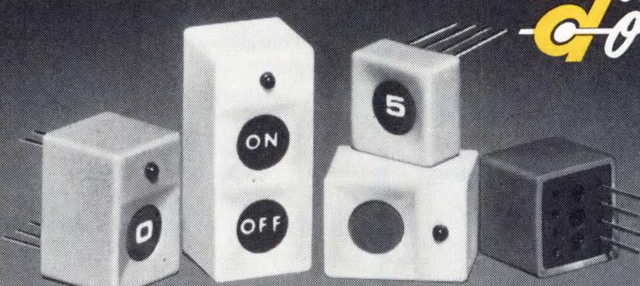

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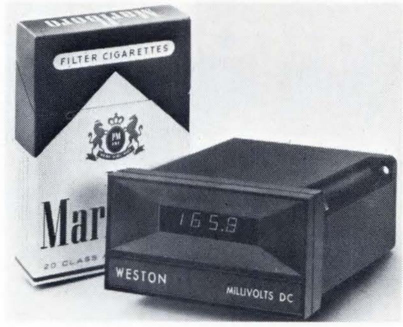
EQUIPMENT

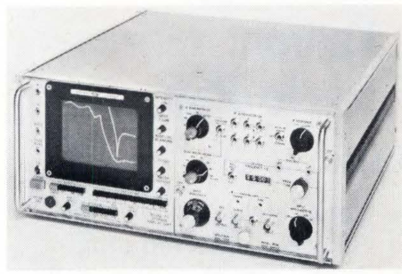


BATTERY POWERED 3-1/2-DIGIT DPM. The new portable Model 1220 DPM is a full bipolar 3-1/2-digit instrument that weighs 4 oz, requires only 4 in.² of panel space and uses only 3/4W of power. The Model 1220 operates from a battery of 5.5V ±10%. Four "C" cells provide 18 hours of continuous operation with all digits fully lit. The DPM uses Weston's patented dual-slope technique and an LSI/MOS plug-in chip for added reliability. Available from stock in ranges of 100 mV to 1000V and 10 μA to 100 mA. Under $100 in OEM quantities. Weston Instruments, Inc., 614 Frelinghuysen Ave., Newark, N J 07114. Phone (201) 243-4700. **170**

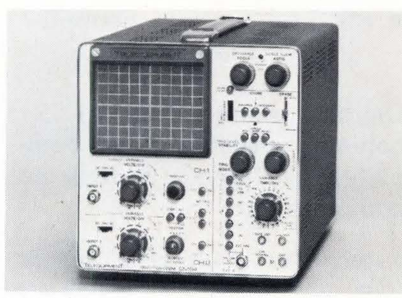
SEVEN-SEGMENT 3-3/4-DIGIT DPM. The AN2534 is a 3-3/4-digit DPM (it can read up to 3999) with a seven-segment Sperry display that offers an accuracy of 0.05%, a resolution of 0.0025% (full scale) and a measurement overrange of 300%. The unit sells for $189 in single-unit quantities, with quantity discounts said to be available. Analogic Corp., Audubon Rd., Wakefield, MA 01880. Phone (617) 246-0300. **171**

A DIGITAL MULTIMETER KIT FOR LESS THAN $100. The IM-1202 is a 2-1/2-digit bipolar multimeter kit, priced at just $79.95, mail order. Assembly time is said to be 2 or 3 evenings. The instrument's accuracy is within 1% on dc volts, 1-1/2% on ac volts and ac/dc current and 2% on ohms. Its 29 selectable ranges measure voltages from 10 mV to 1000V on dc, 10 mV to 700V rms on ac, 10 μA to 2A on ac or dc current and 1Ω to 2 MΩ on resistance. Heath Co., Benton Harbor, MI 49022. Phone (616) 983-3961. **172**

Ac/dc 4-1/2-DIGIT MICROVOLT MULTIMETER. The Model 171 ac/dc digital multimeter offers 1-μV dc resolution and 10-μV ac resolution, ac/dc current and resistance measurements for only $895. As a dc voltmeter, it measures 1 μV to 1000V in 6 full-scale ranges at +0.02% accuracy. On the 5 ac voltage ranges, the 171 permits measurements over 40 Hz to 100 kHz with +0.3% midband accuracy. Keithley Instruments, Inc., 28775 Aurora Rd., Cleveland, OH 44139. Phone (216) 248-0400. **173**

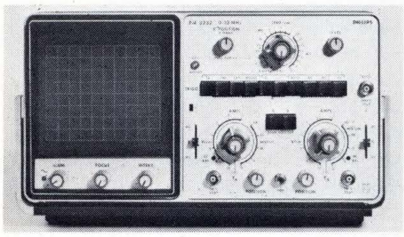


SPECTRUM ANALYZER USES A VARIABLE-PERSISTENCE DISPLAY. The Model 711 variable-persistence display unit offers a persistence range of 300 msec to 100 sec. It can store an image for up to 6 hours or be used in a conventional, nonstore mode, and utilizes plug-in tuning modules covering the audio, video and baseband frequency ranges. $2600. Systron-Donner Corp., Microwave Div., 14844 Oxnard St., Van Nuys, CA 91409. Phone (213) 786-1760. **174**

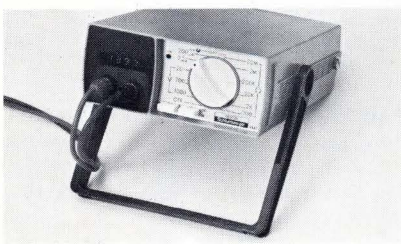


LOW-COST BISTABLE STORAGE SCOPE. The telequipment DM64 10-MHz bistable storage scope is a dual-trace unit that features compactness and light weight. Storage writing speed can be varied from 25 to 250 cm/msec. Sweep speeds from 2 sec/cm to 100 nsec/cm (40 nsec/cm with X5 magnifier), X-Y measurement capability and 5% accuracy make the DM64 ideal for general usages. $1095. Tektronix, Inc., P. O. Box 500, Beaverton, OR 97005. Phone (503) 644-0161. **175**

FREQUENCY COUNTER MEASURES DOWN TO 0.001 Hz IN 1 SEC. A new counter that makes highly accurate direct-reading measurements of audio and low-frequency inputs is the Model 6220, 2-MHz frequency/multiplier counter. The 6220 can resolve 0.001 Hz in 1 sec. Features include AGC, which sets all input adjustments automatically, zero suppression to blank out all leading zeros and an autoranging decimal point. $350. Systron-Donner Corp., 10 Systron Dr., Concord, CA 94520. Phone (415) 682-6161. **176**

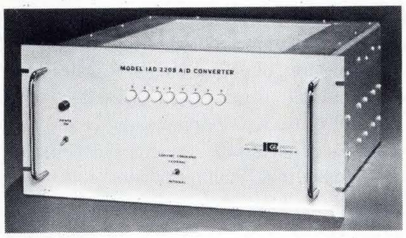


DUAL-BEAM SCOPE HAS 2-mV SENSITIVITY ACROSS 10-MHz BANDWIDTH. Sensitivity of 2 mV/cm across the full 10-MHz bandwidth plus true dual-beam operation characterize the Philips PM3232 general-purpose scope. Offered at approximately $900 as the successor to the Philips PM3230, the PM3232 features dc triggering, automatic leveling, dc coupling and automatic TV line/frame selection. Test & Measuring Instruments, Inc., 224 Duffy Ave., Hicksville, NY 11802. Phone(516) 433-8800. **177**



HIGH-ACCURACY LOW-COST 3-1/2-DIGIT MULTIMETER. Model 4442 digital multimeter for only $325 features dc-voltage accuracy to +0.05% of reading and ac-voltage accuracy to +0.3% of reading (40 Hz to 10 kHz) and +0.6% of reading (10 to 20 kHz). It measures from 199.9 mV to 1000V full scale dc and ac in 5 ranges each. It also measures from 199.9Ω to 19.99 MΩ full scale in 6 ranges with accuracies to ±0.1% of reading. Weston Instruments, Inc., 614 Frelinghuysen Ave., Newark, N J 07114. Phone(201)243-4700. **178**

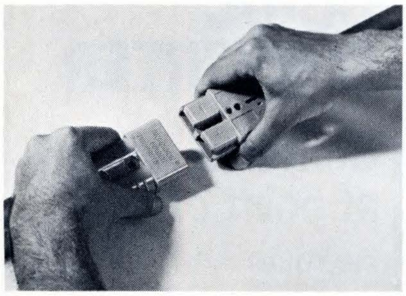
SWEEP GENERATOR FOR IF APPLICATIONS. Model 1202 is a small, low-cost sweep generator that covers the frequency spectrum from 100 kHz to 100 MHz and provides full range sweep with a flatness of ±0.25 dB, 2% linearity and 1V output. The single-chassis, modular construction of the 1200 Series provides a compact size of 8-3/4 × 6-3/4 × 12 in. and ease of maintenance. Plug-in markers (up to 7) and a built-in 102-dB attenuator (1-dB steps) are also available. $895. Telonic Industries, Inc., 21282 Laguna Canyon Rd., Laguna Beach, CA 92652. Phone(714)494-9401. **179**



5-MHz 8-BIT A/D-CONVERTER SYSTEM. Model IAD-2208 A/D-converter system features a 300-psec aperture time, 8-bit resolution at conversion rates up to 5 MHz and an accuracy of ±0.02% of full scale ±1/2 LSB. The IAD-2208 includes a sample-and-hold amplifier, an A/D-encoder system, timing and decoding and power supplies. It operates either asynchronously from an internal clock or synchronously from an external signal source. It is completely modular in design and is rack-mountable. Inter-Computer Electronics, Inc., Box 507, Lansdale, PA 19446. Phone(215)822-2929. **180**

PROGRAMMABLE RFI METER PERFORMS PRECISION AUTOMATIC TESTING. A new programmable EMI/RFI test receiver covering the frequency range of 30 to 1000 MHz in 8 bands is the NM-37/57. With suitable programming, it will perform all automatic and semi-automatic testing required by MIL-STD-461A and MIL-STD-826A. Model NM-37/57 is portable and can operate off ac power or for 8 hours on internally rechargeable batteries. Signal-level range is 0.1 μV to 1V or −20 to +120 dB. Singer Instrumentation, 3211 S. LaCienega Blvd., Los Angeles, CA 90016. Phone(213)870-2761. **181**

CHECK NO. 81



ONE-PIECE CONNECTORS ARE RATED AT 175A. The single-piece structure provides quick and easy assembly of individual contacts. A snapping sound assures that the contact has latched onto the spring. The 175A connectors are also keyed and color coded. The keys form an integral part of the connector and, together with contrasting color coding (gray, blue, orange and yellow), prevent the possibility of connecting nonidentical voltages. The lightweight polycarbonate housings have superior dielectric, heat and arc resistance characteristics. Anderson Power Products Inc., Power Equipment Div., 145 Newton St., Boston, MA 02135. Phone(617)787-5880. **182**

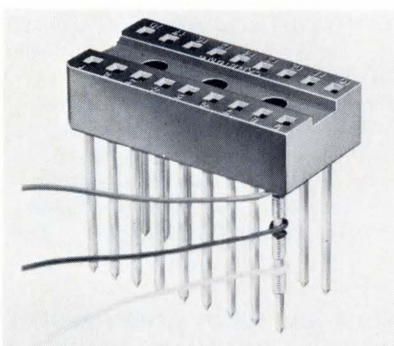
MINIATURE THERMISTORS COVER WIDE RANGE. The Minitherm N40-90002 spans a range of −30°C through −10°C, with a 1° accuracy. 90003 covers −20°C through +25°C with a 2° accuracy. 90004 has a range from +25°C to +100°C. It also has 2° accuracy. The fourth Minitherm (N40-90005) ranges from +100°C through +200°C. Its accuracy margin is from 2-1/2°C on the low side through 3°C on the high side. In quantity, pricing runs 20¢ to 30¢ each. MEPCO/ELECTRA, Inc. Columbia Rd., Morristown, N J 07960. Phone-(201)539-2000. **183**

ALL-PURPOSE ADHESIVE IS WATERPROOF. A new super-strength all-purpose adhesive, called MAGIGRIP, has been developed which makes it possible to bond difficult-to-adhere materials. It will adhere rubber to almost any surface, and it will bond glass, metal, wood and ceramic to almost any surface. The adhesive is merely applied to one surface and placed in contact with the other surface to effect an almost instantaneous bond which continues to grow stronger as the adhesive dries. MAGIGRIP is available in 1- and 5-gal. containers as well as 55-gal. drums. Adhesive Products Corp., 1660 Boone Ave., Bronx, NY 10460. Phone(212)542-4600. **184**

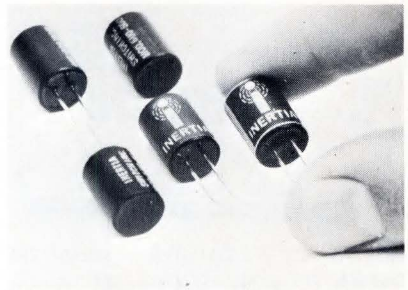
DIP NETWORKS PROVIDE UP TO 23 COMPONENTS. Fourteen- or 16-pin CORDIP resistor networks for pull-up or in-out functions are available combining up to 15 resistors in dual in-line packages. Standard resistance values range from 50Ω to 22 kΩ, with tolerances of ±2% and temperature coefficients of 100 ppm/°C. Custom CORDIP networks can be made with up to 23 resistors, capacitors and diodes interconnected to specifications. Corning Glass Works, Corning, NY 14830. Phone(607)-962-4444. **185**

NONINDUCTIVE POWER RESISTORS. This new power resistor product features an improved dielectric coating and a terminal corona ring for reducing the potential for terminal arcing which may be corona initiated. Increased "voltage-withstand" of up to 50% has been obtained in applications such as capacitor current limiting, impulse generators, X-ray equipment, electronic precipitators, surge limiters with spark gaps and antenna terminations. The No-Arc resistor can be provided for all standard catalog Carborundum AS resistors in ratings from 15 to 150W. The Carborundum Co., Niagara Falls, NY 14302. Phone(716)278-2706. **186**

SCR TRIGGER TRANSFORMER LINE EXPANDED. This 6-pin model is designed for direct pc board mounting with leads spaced on a 0.600-in. diameter circle. Transformers are available open or encapsulated with #20 AWG tinned copper leads. Low interwinding capacitance reduces problems of false triggering. Standard turns ratios include 1:1, 1:1:1, 2:1, 2:1:1, 5:1 and 5:1:1. Models are available for operation from −10°C to 70°C. BH Electronics, 245 E. 6th St., St. Paul, MN 55101. Phone(612)-228-6463. **187**



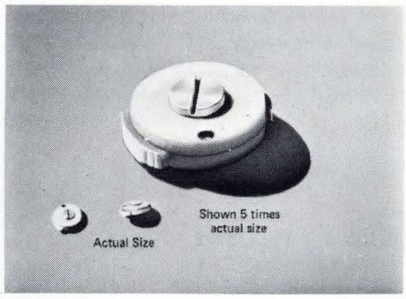
WIRE-WRAP IC SOCKETS USE REPLACEABLE PINS. This replaceable-pin feature is available for 2 and 3-wrap or standard (3-wrap) pins to fit sockets which accept 14, 16, 18, 24, 28, 36, and 40-pin DIPs. These sockets are molded of diallyl phthalate. The Wire-Wrap pins are made of phosphor bronze finished in gold or electro-tin. Terminal size is the standard 0.025-in square. Replacement pins are identical to original equipment. Cambridge Thermionic Corp., 445 Concord Ave., Cambridge, MA 02138. Phone(617)491-5400. **188**



LOW-COST IMPACT SWITCH AVAILABLE FOR WIDE USAGE. An inexpensive, yet reliable unidirectional impact inertia switch with patented magnetic restraint, originally developed for aircraft ELT (Emergency Locator Transmitter), has now been made available for general industrial applications. Model 6U0-600 Impact Switch is $1.80 per unit in volume orders. Its patented magnetic restraint system not only provides an accurate switch, but eliminates the usual resonant frequency problems inherent in the conventional spring-mass system. Model 6U0-600 has unidirectional sensitivity, with a range of 1 to 25 Gs. Operating temperatures are −65°F to +165°F. Switch contacts are SPST, NO, Momentary. Inertia Switch, Inc., 311 W. 43rd St., New York, NY 10036. Phone(212)586-5880. **189**

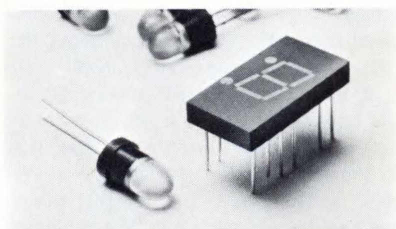
COOLING MODULES FOR POWER SEMICONDUCTORS ARE LIGHTWEIGHT. A simple, compact and highly effective package for cooling 1 to 7 case-common power semiconductor devices has been introduced. Highly effective cooling is provided by air forced through 2 rows of convoluted fin stock. COOL-PAX Wells may be mounted on other systems where cooling air is already available or may be provided in integral assemblies including fan. Where electrical isolation between devices is required, separate Wells may be provided. Thermalloy, 2021 W. Valley View Lane, Dallas, TX 75234. Phone(214)243-4321. **190**

PADDLE-LEVER SWITCHES ARE RATED AT 10A. The MCT-110D-49 and MCT-219N-49 subminiature flat paddle lever switch series is the latest addition to the ALCO-SWITCH family. They are U.L. listed at 10A, 125V ac and 5A, 250V ac and have a pinned lever in a 1/4-in. bushing to prevent lever rotation. Tough, all-metal 1/2 in. diameter construction with high-impact electrical insulation allows use under extreme environmental conditions. Life expectancy is in excess of 150,000 cycles. The single-pole, double-throw MCT-110D-49 is priced at $2.55 in single lots and $1.28 in lots of 500. The double-pole, double-throw MCT-210N-49 is priced at $3.15 in single lots and $1.58 in lots of 500. Alco Electronic Products, Inc., 1551 Osgood St., N. Andover, MA 01845. Phone(617)685-4371. **191**

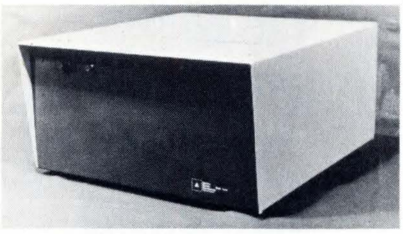


TRIMMER CAPACITORS ARE WAFER THIN. VARI-Thin subminiature trimmers measure 0.221 in. diameter × 0.080 in. thin and have a capacitance range from 5 to 30 pF. The low profile VARI-Thin was designed originally for the quartz-watch industry, and now the advantages of its subminiature size, stability and capacitance range are being utilized in miniature instrument and communication gear. Erie Technological Products, Inc., 644 W. 12th St., Erie, PA 16501. Phone(814)453-5611. **192**

LOWEST VSWR TERMINATION ANNOUNCED. Coaxial SMA termination is said to be the smallest device of its kind available as a standard unit. Maximum VSWR from dc to 18 GHz is 1.15, with readings below 1.10 as typical (VSWR from dc to 10 GHz is 1.05, max.). Maximum power input is 1.0W, with a temperature range from −54°C to +125°C. The unit measures 0.42 in. long with a standard SMA male connector. The device weighs only 0.9 oz. The Model T180M is priced at $15. Engelmann Microwave, Skyline Dr., Montville, N J 07045. Phone(201)334-5700. **193**

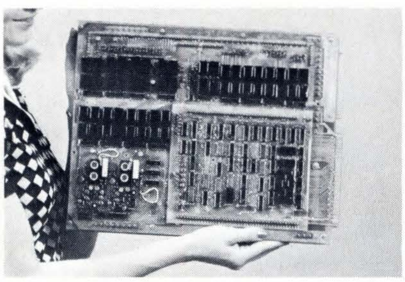


GREEN LEDs AVAILABLE IN DISCRETE OR READOUT FORM. Both the displays and lamps feature reflector design which, when combined with the high electroluminescent efficiency of Gallium Phosphide, gives distinct functional advantages. Evenly lighted segments are achieved in the 0.33-in. displays, resulting in exceptional readability. In lamps, the "pinpoint" effect is overcome, creating a bright, evenly lighted 0.200-in. diameter dome which is visible over a wide angle. The displays may be mounted in a standard 14-pin DIP socket or directly into a pc board and operate with standard IC coder/drivers at IC power levels. Opcoa, Inc. 330 Talmadge Rd., Edison, N J 08817. Phone(201)287-0355. **194**



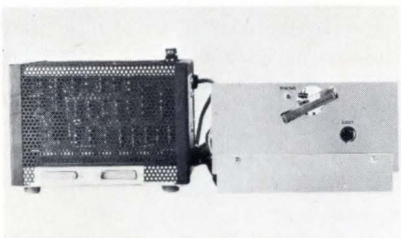
PROGRAMMABLE TERMINAL MULTIPLEXER HAS COMPUTER/TERMINAL COMPATIBILITY. The MultiTerm 2 uses a built-in microprocessor and programmed memory to emulate a computer or terminal to meet a specific application. For example, it can make a video display terminal compatible with a previously noncompatible computer. Or, it permits computers to work with previously noncompatible video display terminals. MultiTerm 2 is programmed in Read-Only rather than Random-Access Memory, preventing program loss in the event system power is cut off. Delta Data Systems Corp., Woodhaven Industrial Park, Cornwells Heights, PA 19020. Phone(215) 639-9400. **245**

ASYNCHRONOUS, SERIAL IMPACT PRINTING TERMINAL operates at a maximum speed of 120 cps and is available in a variety of forms ranging from the basic print mechanism alone to a complete KSR with modem and all-electronic components. The Execuport 1200 prints a full 132-column line from a buffer, producing up to 5 copies and an original on standard perforated paper stock. Spacing can be varied for paper widths from 3-1/2 to 14-7/8 in. Basic character set of the Execuport 1200 is ASCII with generation of the complete 128-character ASCII code. Computer Transceiver Systems, Inc., 66 Midland Ave., Paramus, N J 07652. Phone(201)261-6800. **246**



CORE MEMORIES HAVE CYCLE TIMES OF 900 NSEC AND FASTER. The Series 4000 comes in 40-bit word size and capacities up to 16,384 words per module and costs less than $0.008 per bit in quantity. The new memories use 18-mil Ampex cores in a 3-wire, 3D configuration, spaced in a high-density packaging arrangement. By use of multiple modules, 4000 Series memories may be expanded to a capacity of 131, 072 words of 40 bits each without modification. Power requirements are +5V and −28V. Ampex Corp., 13031 W. Jefferson Blvd., Marina del Rey, CA 90291. Phone(213)821-8933. **247**

DIGITAL TAPE DRIVE OPERATES AT 10 TO 50 IN. PER SEC, has low-maintenance tape tension controls and a mechanical design that reduces the number of moving parts by 25% compared with its predecessor tape drives. The unit uses 10-1/2-in. reels, has standard tape speeds of 12.5, 24, 25, 37.5 and 45 ips and offers packing densities in pairs: 200 and 556 bits per inch, 200 and 800 bpi, and 556 and 800 bpi. Phase encode capability for 1600 bpi also is available. Price is approximately $4000 in OEM quantities. Ampex Corp., 13031 W. Jefferson Blvd., Marina del Rey, CA 90291. Phone(213)821-8933. **248**



DIGITAL CASSETTE MEMORY SUBSYSTEM directly replaces paper-tape-reader/punch units. The TERMI-138E is a character oriented incremental cassette memory for general-purpose store-and-forward applications. It is designed for use with low-speed data terminals or input/output devices, features unique editing capability and control via data encoded commands. The unit operates at switch selectable rates of 10, 15 or 30 cps. Incremental operation is at 30 steps-per-second, with fast forward/reverse at 330 cps. Telex, 9600 Aldrich Ave. S., Minneapolis, MN 55420. Phone (612)884-4051. **249**

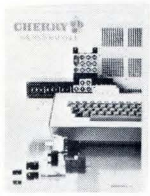
CARD READER READS STANDARD 80-COLUMN CARDS. The Model ZU960HC-3IL is composed of a light sensor matrix (12 × 80), a card slot and light sources. Cards are inserted into the slot, manually, one card at a time, read, then automatically ejected. The TTL compatible output can either be parallel or serial, depending on the scan method. The reader uses incandescent light sources, operating at 5V dc with a power consumption of 12W. Delivery is 4 wks. Panasonic, 200 Park Ave., New York, NY 10017. Phone(212)752-2200. **251**

KEYBOARD MEETS MIL STD 810B. The MK-28M keyboard achieves high reliability through the use of a patented ROM encoder and a crossbar switch with precious alloy contacts. It is currently being delivered with 2-key rollover and data interlock features. N-key rollover can be ordered as an option. The keyboard uses a standard 5-level Baudot code. Optional codes available are FIELDATA and ASCII. Data Electronics Corp., 12 Cambridge St., Burlington, MA 01803. Phone(617)272-7460. **252**

10-1/2-IN. MAGNETIC TAPE TRANSPORT. The Series 10000 tape transport provides for tape speed from 12.5 ips through 45 ips with rewind speeds of 200 ips. Data density is available from 200 CPI through 800 CPI NRZI and 1600 CPI PE. A combination model PE/NRZI 1600/800 CPI is available. Series 10000 tape transports are plug compatible with most other 10-1/2-in. units in the field. Producers Service Corp., 1200 Grand Central Ave., Glendale, CA 91201. Phone(213)245-8424. **253**

TWO VISUAL DISPLAY TERMINALS The Nova Display 6010 display terminal is designed for applications where a faster, quieter and more reliable terminal than a teletypewriter is needed. It has a standard 53-key keyboard and operates in a roll mode, with new text appearing at the bottom of the screen. $2300. The Nova Display 6012 terminal has a movable cursor for hardware editing anywhere on the screen, 3 modes of operation and a hardware protection feature that a programmer can use to format the screen in data entry applications. $2700. Data General Corp., Southboro, MA 01772. Phone(617)485-9100. **254**

FORTRAN IV COMPILER SPEEDS EXECUTION TIME. Users of 16-bit computers now have available an expanded version of ModComp's FORTRAN IV compiler which can reduce execution times up to 50%. The new compiler enables performance to match that of many 32-bit machines. The additions to the existing compiler are designed to optimize both code generation and execution time for users operating under the MODCOMP, MAX II and MAX III operating systems. An optional pass has been added to the compiler which optimizes subscript calculations on data arrays and common subexpressions within a block of FORTRAN IV statements. Modular Computer Systems, 1650 W. McNab Rd., Ft. Lauderdale, FL 33309. Phone(305)974-1380. **255**

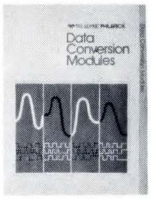


CATALOG OF SWITCHES AND KEYBOARDS contains complete listings, engineering drawings, specifications, operating characteristics and technical data. Included are snap-action switches, leverwheel/ thumbwheel switches, keyboard switches, matrix selector switches and keyboards. Other information on Cherry's plant facilities, equipment, in-house manufacturing capabilities and worldwide sales offices is pictured and described in Catalog C-73. Cherry Electrical Products Corp., P.O. Box 718, Waukegan, IL 60085. **195**

THUMBWHEEL SWITCH BROCHURE DESCRIBES MOST POPULAR TYPES. This 16-pg. short-form catalog describes the features of Type M, H and P thumbwheel switches. It also introduces the industry's latest and smallest thumbwheel switch—the Type L, that measures only 0.71 in. (18mm) high and 0.315 in. (8mm) wide. Included are electrical, mechanical and environmental specifications and a complete description of options available and their application. Interswitch, 770 Airport Blvd., Burlingame, CA 94010. **196**

LITERATURE AVAILABLE ON SOLID STATE LED NUMERIC DISPLAYS. The data sheets cover the specifications on 0.33-in. and 0.77-in. characters using gallium phosphide red light-emitting diodes. The units covered are: SLA-1—7-segment numeric display (decimal point on left); SLA-1R—7-segment numeric display (decimal point on right); SLA-1C—7-segment numeric display with color; SLA-2—numeral one plus and minus signs; SLA-3—7-segment numeric display (decimal point on right); SLA-4—numeral one plus and minus signs (decimal point on right); and SLA-4A—numeral one plus and minus signs (2 decimal points). OPCOA, Inc., 311 Talmadge Rd., Edison, NJ 08817. **197**

POWER SUPPLIES FOR LOGIC AND OP AMPS. Power supplies for IC logic and op amps are described in a 4-page brochure. Single-output 5V supplies with current ratings from 250 mA to 32A and dual-output modules providing ±5, ±12 and ±15V at 25 mA to 8.5A are included in the listings. Acopian Corp., Easton, PA 18042. **198**



DATA-CONVERSION CATALOG from Teledyne Philbrick. A comprehensive fold-out data-conversion short-form catalog features the latest products in a rapidly expanding line of data converters. A/D- and D/A- converter specifications are arranged for quick selection by key parameters. Teledyne Philbrick, Allied Dr. at Rte 128, Dedham, MA 02026. **199**

6-VOLUME SET OF 1973 DATABOOKS AVAILABLE. The SSD-200A 6-vol., 3400-pg. set of DATABOOKS is now available on RCA Solid State's complete commercial line of linear integrated circuits, discrete MOS devices, COS/MOS digital integrated circuits, power transistors, thyristors, rectifiers, RF devices and hybrid circuits. The set contains complete technical data sheets and application notes on all commercial types and has been expanded editorially to include: quick selection guides and charts, cross-reference indexes to show current commercial designations on devices that formerly carried developmental type designations, subject indexes to data and application notes in all volumes so that a user can check the index in any volume to determine which volume he needs. The entire set may be ordered for $12 or volumes may be ordered individually. RCA/Solid State Div., Route 202, Somerville, NJ 08876. **200**

HIGH-VOLTAGE POWER SUPPLIES. A 28-page catalog includes data on module-type and a line of rack mounted high-voltage power supplies for CRTs, photomultipliers, capacitor charging and general high-voltage uses. The line includes unregulated, fully regulated and remotely programmable supplies from 200V to 75 kV. Ac line operated units as well as dc-to-dc converters are described. Advanced High Voltage Co., Inc., 14532 Arminta St., Van Nuys, CA 91402. **201**

REGULATED HIGH-VOLTAGE POWER SUPPLIES. A 2-page data sheet describes a line of regulated, miniature high-voltage dc power supplies. Over 40 models covering 13 output ranges to 30 kV are listed. Detailed specifications are included along with several options. Spellman High Voltage Electronics Corp., 1930 Adee Ave., Bronx, NY 10469. **202**

SHOCK RECORDER FOR SHIPPED PRODUCTS. Shock damage to packages or products being shipped can now be accurately recorded for direct reading by the "Transit Guard" shock recorder, which is detailed in this catalog. The time based, self-contained recorder provides 10 channels for measuring shock magnitude, direction and the number and time of occurrences. Inertia Switch, Inc., 311 W. 43rd St., New York, NY 10036. **203**

SUPPLY BULLETIN DETAILS IC RELIABILITY PROGRAM. A 4-pg. pamphlet, Bulletin 84019, is titled, "Rel II High Reliability Integrated Circuits from TI Supply." It explains that the Rel II program is primarily intended for plastic ICs which fill the need for products more reliable than standard products, yet not as costly as military grade ceramic products. Level I products are baked, 100% tested and then must pass a 0.25% AQL per Mil 105D. The added feature for Level II products in the Rel II program is power burn-in per Mil Std 1015 Condition D. Bulletin 84019 explains that power burn-in is the most widely accepted and positive means of increased reliability. Rel II products are available from stock at TI Supply. Also available are MACH IV and JAN integrated circuits. Texas Instruments Inc., 13500 N. Central Expressway, Dallas, TX 75222. **204**

PORTABLE ELECTRICAL THERMOMETER. Described in a 4-color, 2-page brochure is the RFL Industries' Model 290 electrical thermometer. This unit is a low-cost ($99.95 including general-purpose probe and battery) thermometer with a wide temperature range. The brochure describes typical applications, specifications and lists the 4 different types of probes available for all types of applications. RFL Industries, Inc., Boonton, NJ 07005. **205**

DIGITAL PHOTOMETER. A new bulletin on Pacific Photometric's digital photometer, Model 124, describes the instrument's negative high-voltage power supply (−50 to −2000V), current measuring circuit, dark-current cancellation and scale expansion. Features detailed include 100 pA to 1 mA full scale, 0.1-pA resolution, 100% overranging and rear-panel BCD output for digital data-logging applications. Pacific Photometric Instrumentations, 5745 Peladeau St., Emeryville, CA 94608. **206**

APPLICATION NOTES

APP NOTE EXPLAINS PROBLEM-SOLVING RELAY APPLICATIONS. A 10-pg. booklet, depicting complex electronic interface problems and how they were solved by various dry-reed and mercury wetted relays, has been published by C. P. Clare & Co. Selected applications, each representative of a wide variety of industrial electronic systems, are diagrammed and explained briefly in terms of problem and solution in order to establish a quick understanding of different types of relays and the kind of application for which each is particularly well suited. The booklet, titled "Six Tough Interface Designs," also offers a complete technical dissertation on the design and application of dry-reed and mercury wetted relays, including performance characteristics. C. P. Clare & Co., 3101 W. Pratt Blvd., Chicago, IL 60645. **240**

CMOS ICs IN AUTOMOTIVE APPLICATIONS is the topic of a new technical bulletin issued by Solid State Scientific. AN-103 discusses chip design techniques as applied to automotive requirements and offers data on some of the useful circuits now being implemented in automotive electronic systems. Also detailed are the advantages of using CMOS where high reliability, ultra lower power, wide operating temperature range and high noise immunity are requirements. Necessary configurations as well as a scale drawing of an automobile illustrating various applications have been included. Solid State Scientific, Inc., Montgomeryville, PA 18936. **241**

CATCHING NOISY PRODUCTS IN PRODUCTION BY AUTOMATIC TESTING. Federal Scientific's 12-pg. application note entitled "Quality Evaluation of Automotive Dc Motors" reports on a continuing program by Ford Motor Co. to integrate a Ubiquitous real-time spectrum analyzer into small-motor production for high-speed automatic noise testing. An automatic analyzer/computer system is used to make accept-reject decisions on-line in less than 4 sec. The noise evaluation is based on the frequency spectrum of the motor under test. Federal Scientific Corp., 615 W. 131st St., New York, NY 10027. **242**

SIGNIFICANCE AND TYPES OF TRUE RMS MEASUREMENTS. The application note "True RMS Measurements" is directed to scientists, engineers, technicians and purchasing personnel who are first encountering nonsinusoidal ac waveforms in their measurements. In addition to explaining what true rms is, the note describes how the quantity is measured by various detectors. Limitations and advantages are given for each method. Also critical specifications, such as crest factor, are explained, so that a user and/or buyer can better evaluate instrument purchases. Hickok Electrical Instrument Co., 10514 Dupont Ave., Cleveland, OH 44108. **243**

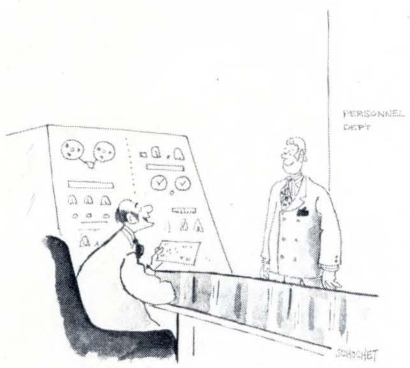
BROADBAND RECEIVER DESIGN TECHNIQUES. A paper entitled "Design of a Communications Security Test Receiver For Maximum Broadband Dynamic Range" is offered by American Electronic Laboratories, Inc. The paper describes the problems associated with detection of broadband signals, offers insight into the solution of those problems and presents the required receiver design technique to maximize broadband sensitivity and linear, instantaneous dynamic range. Charts, graphs and diagrams accompany the text. American Electronic Laboratories, Inc., Box 552, Lansdale, PA 19446. **244**

signals and noise

Want to be an editor?

If you like to write, meet people, be on top of the latest happenings in electronics, why not try technical editing? EDN is looking for a top man to work in the Boston main office.

Send resume and salary requirements to Frank Egan, Editor, Boston, MA.



"WE'VE PUT YOU THROUGH OUR COMPUTER AND IT LIKES THE CUT OF YOUR JIB."

ISSCC to celebrate 20th birthday in '73

New York, NY, November 24—The transistor, which in 1954 had achieved sufficient stature to warrant a national conference at the University of Pennsylvania, will be toasted next year at the 1973 IEEE International Solid-State Circuits Conference, reflecting two decades of spiralling progress.

The occasion will be commemorated on February 14-15-16 by in-depth worldwide reports on advancements in solid-state circuitry, authored by over 150 from here and overseas, including Japan, Holland, Germany, England, France and Belgium.

For the first time, all conference activities will be concentrated at one site, the Philadelphia Marriott Motor Hotel on City Avenue, off the Schuykill Highway.

Programs with registration forms can be obtained from the Moore School or Lewis Winner, 152 West 42nd St., New York, NY 10036.

It's a thought!

Dear Sir:

Re free-lance business-mag writer E. W. Fair's article (EDN, Nov. 1) on how to beat monotony: It sounds great if you own your own business or a hunk of one. I, for example, get bored with engineering sometimes, and so go home and lie down, or maybe mow the lawn or perhaps visit a local bar.

The suggestions of Mr. Fair, who is no engineer nor even a corporate employee, do not, however, ring true. He may understand the mores of big organizations, but if he does, he conceals the fact.

The way to combat boredom in a big organization is limited, because it is closely involved with holding your job. There is only one way in that environment. It is to *appear busy, while getting nothing done*. This is a difficult art. It is not everyone's dish of tea, but I suggest, on the basis of experience (particularly in government funded work), that it is by far the best and safest way.

Part of the technique is strenuous, but not really if you adopt the right frame of mind. Conference telephone conversations, one-day trips to the opposite coast and writing long reports and memoranda are essential parts of the relaxing technique. It may seem that such activities are hard work, but they are hard only if you try to make them good. Once you realize that, in a big organization, nobody will read the reports or remember the conferences or care what was accomplished on the trips, you can fashion these activities in a relaxing manner, secure in the knowledge that you are doing yourself good, and getting ahead in the organization.

Sincerely,
Milburn K. Christopher
V-P
Innes Instrument

To wire-OR not to—Is that the question?

Dear Sir:

Jesse Pipkin ("On Engineers and Profits," EDN, October 1, 1972) spoke out fairly well in his article, but succumbed to "foot-and-mouth" disease (open mouth, insert foot) when belittling the wire-OR. He found "it amusing that such an ill-begotten method of design should also be misnamed!"

Perhaps Mr. Pipkin has never heard of the CTμL (Complementary Transistor Micro Logic) family sold by Fairchild Semiconductor and (to the best of my knowledge) used by Hewlett-Packard. CTμL implements true AND/OR logic and (except for two minor exceptions) provides no OR gates—the wire-OR (and I do not mean wire-AND or wire-NAND or whatever!) provides the OR capability in normal logic design. It was built to function this way and (if I may interject a personal note) is a logic designer's dream to use and also lends itself well to testing <u>if</u> the tester knows his business.

It is the problem of Mr. Pipkin (and others) if he wants to use a wire-AND in place of a wire-OR.

In order to illustrate the effectiveness of the wire-OR, may I refer you to the article "SYMBOL Hardware Debugging Facilities" and the associated bibliography published in Vol. 40 of the AFIPS Conference Proceedings of the 1972 Spring Joint Computer Conference.

There is a wire-OR, Mr. Pipkin; it is alive and doing well. VIVA C TμL!

Sincerely yours,
Myron A. Calhoun
Kansas State University
Department of Computer Science

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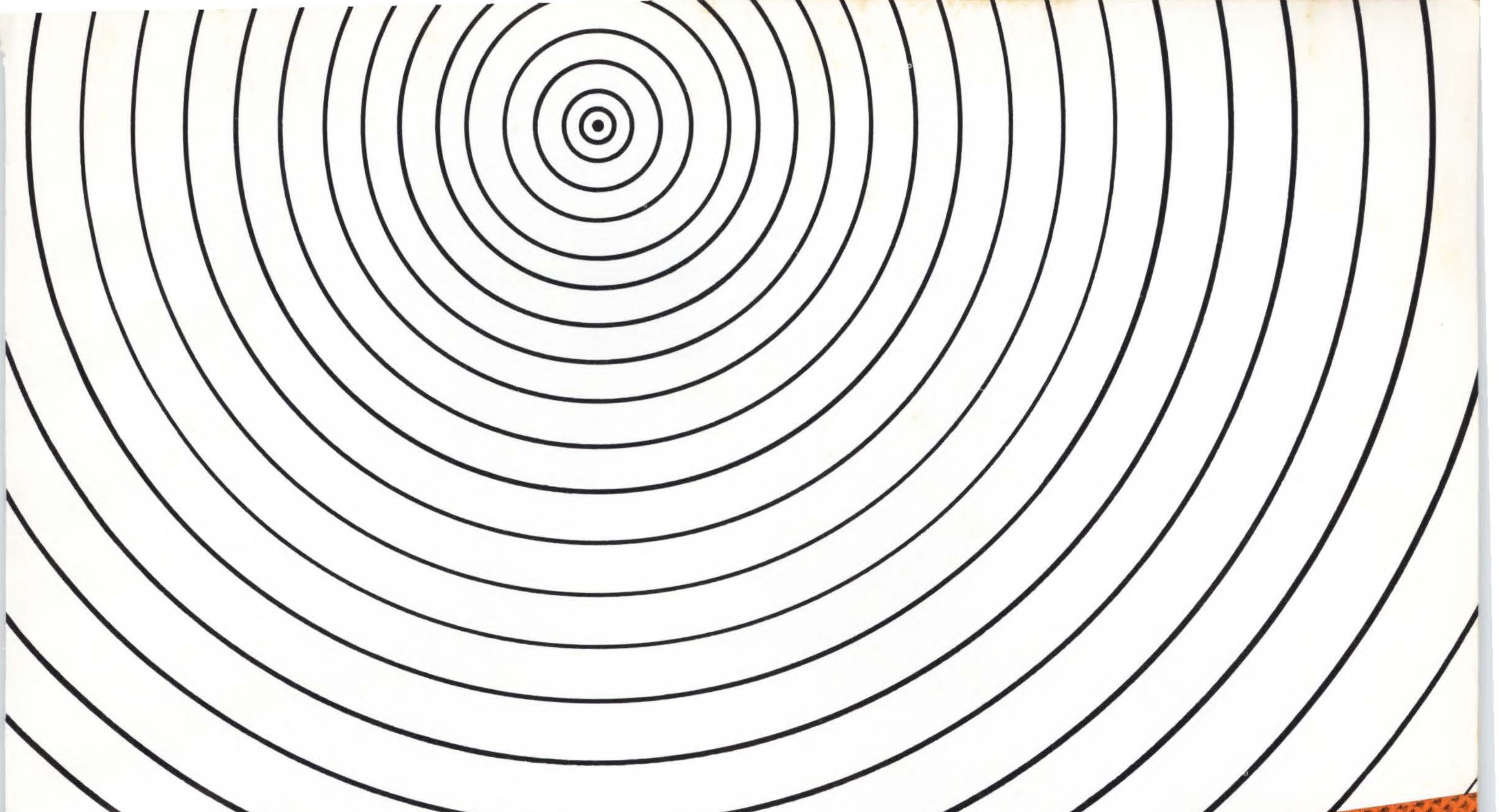

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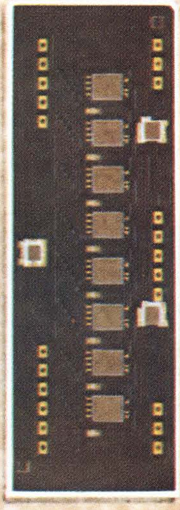

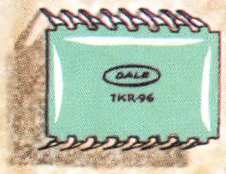

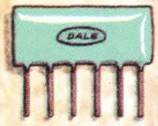

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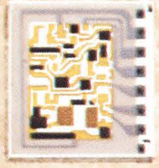

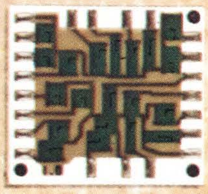

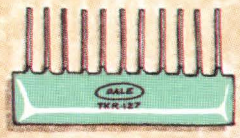

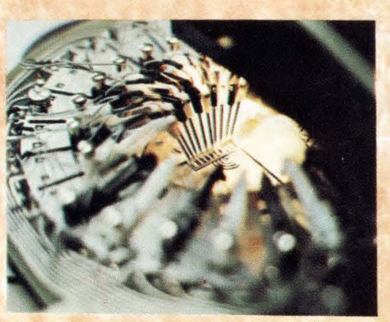

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