EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

EDN

Computer-aided packaging progresses at various levels

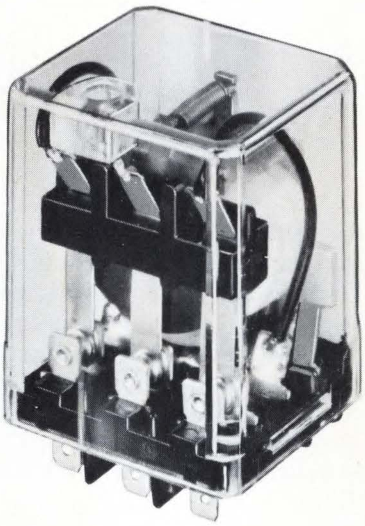
New D/A approach leads to inexpensive converters

Network analyzer uses calculator for control and data analysis

A CAHNERS PUBLICATION

AUGUST 15, 1972

GP



MAGNECRAFT'S NEW CLASS 388

GENERAL PURPOSE RELAY

Magnecraft is pleased to introduce the new Class 388 General Purpose Relay. This inexpensive, high performance line of stock relays offers many quality features found only in custom built versions. Available in either a covered plug-in or open style with a wide choice of AC or DC coil voltages and SPDT, DPDT, or 3PDT 10 amp contacts.

All Class 388 relays have 3-way pierced terminals. While spaced for standard plug-in mounting, the flat terminals (0.187″ x 0.020″) also accept quick-connect receptacles or direct soldering. For plug-in use, three types of chassis mounted sockets are available; quick-connect, solder, or printed circuit terminals. Covered plug-in version has a tough clear polycarbonate plastic cover.

In a highly competitive business, delivery can be a deciding factor. If delivery is important to you, be aware that Magnecraft ships better than 90% of all incoming orders for stock relays, received before noon, THE SAME DAY (substantiated by an independent auditing firm). In addition to our shipping record, most stock items are available off-the-shelf from our local distributor.

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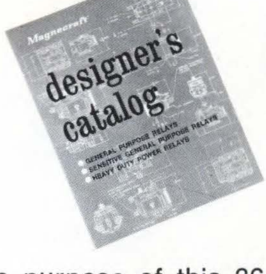

DESIGNER'S CATALOG

The purpose of this 36-page catalog is to assist the design engineer in specifying the proper relay for a given application. The book completely describes General Purpose, Sensitive General Purpose, and Mechanical Power Relays. New products include the complete line of Class 388 General Purpose Relays.

Magnecraft® ELECTRIC COMPANY

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CHECK NO. 2

PACK YOUR CARDS TIGHTER . . . KEEP THEM COOLER . . . with a System that helps you beat the system . . .

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Use Varipak II to pack up to 82 cards and connectors in a row. Even with cards this tight, we've made sure you'll get plenty of air flow between them. To keep components cooler, working longer. For convenience, we mount connectors on the back panel. Makes it easy to cross wire and check out. And Varipak's modular construction lets you design around your needs. Not the limitations of your enclosure. So even special packaging adaptations require little or no tooling costs.

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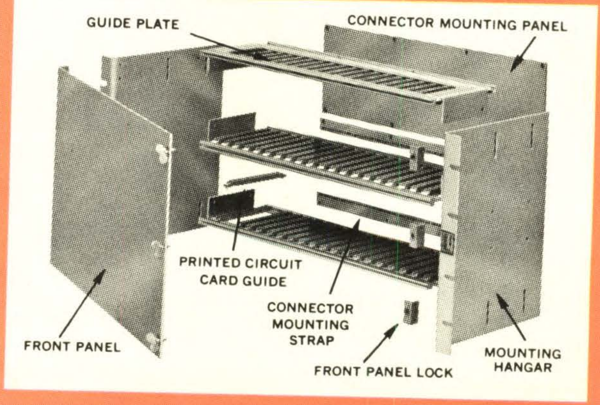

For full details on the Varipak II system from Elco, contact your local Elco representative or distributor, or:

Elco, Willow Grove Division
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(215) 659-7000

Elco, Pacific Division
2200 Park Place
El Segundo, Calif. 90245
(213) 675-3311

Operations in USA, Australia, Belgium, Canada, Denmark, England, France, Germany, Israel and Japan. Sales offices throughout the world. In Europe, Elco Belge, 77 Blancefloerlaan, Antwerp, Belgium, Tel. 03-190064. In the Far East, Elco International, TBR Building, 2-10-2 Nagata-cho, Chiyoda-ku, Tokyo 100, Japan, Tel. 580-2711/5.

If you don't want hybrids. Can't afford high gear-up costs. And need the reliability of discretes.

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CORDIP™ component networks. An entirely new class of low cost, reliable, dual-in-line component networks that give you a flexible new design option.

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CORNING
ELECTRONICS

CHECK NO. 5

AUGUST 15, 1972
VOLUME 17, NUMBER 16

EDN

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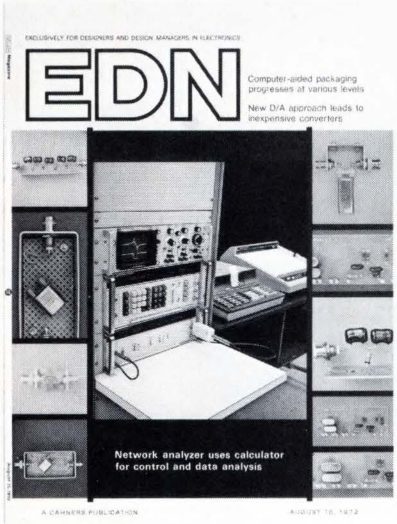
EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS



COVER

The hewlett-Packard Model 3042 Automatic Network Analyzer offers the capability of a computer controlled system at a price approaching that of a manual system. The secret? It operates under programmable calculator control. For details, see page 66.

DESIGN NEWS

DESIGN FEATURES

COMPUTER HARDWARE

PROGRESS IN PRODUCTS

DESIGN PRODUCTS

DESIGN DEPARTMENTS

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But we're doing 6 things to earn it.

1 **Better components.** From ER through industrial, from precision through general purpose – we give you documented reliability. You'll find our metal film resistors outperform other metal films (including glazed), wirewounds and carbon comps. And our Glass-K™ capacitors outdistance monolithic ceramic capacitors on all counts.

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5 **Better new products.** Our CORDIP™ Component Networks let you replace most of the outboard discretes you can't design into an IC. With a pretested, dual-in-line package of up to 23 discrete resistors/capacitors/diodes. Our FAIL-SAFE™ flame proof resistors give you an economical replacement for non-inductive and semi-precision power wirewounds. But ours open – never short – under overload.

6 **Better support.** We've built the largest technically-trained field force in the industry. And have contracted with the 30 most competent and service-oriented distributors in the country to give you in-depth assistance whether your needs are big or small.

Just let us prove it. Write for full details to: Corning Glass Works, Electronic Products Division, Corning New York 14830. Or call: (607) 962-4444. Ext. 8381.

CORNING
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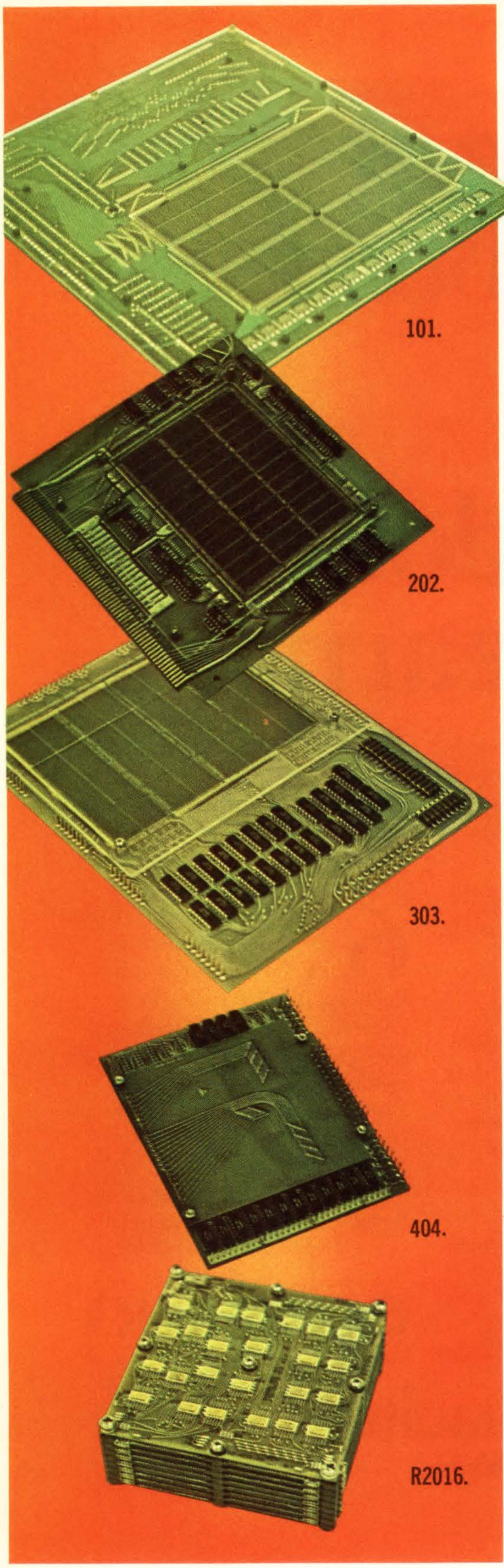
Resistors & Capacitors

for guys who can't stand failures

CHECK NO. 6



Announcing the new

CRUSADER SERIES

the standard high performance core memory stacks from FABRI-TEK.

The best memory systems start with the best stacks. That's why it's so important Fabri-Tek be there at the beginning . . . with Crusader Core memory stacks. The stacks that exemplify the state of the art in memory technology.

Fabri-Tek offers five distinct models within the Crusader Series. Five standard stack designs with the flexibility and assembly ease so necessary for volume production of memory systems.

Crusader Core Model 101. Planar, 3-D, 3-wire stack design construction with a capacity of 147,456 bits of storage (8K by 18 bits). High speed. Typical cycle times of 650 nanoseconds for Read/Write.

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Crusader Core Model 303. Single-sided, 3-D, 3-wire planar design. Storage capacity to 131,072 bits (8K by 16 bits). High speed operation. Typical cycle time, 650 nanoseconds for Read/Write.

Crusader Core Model 404. Compact, folded planar construction in 3-D, 3-wire configuration. Storage capacity is 147,456 bits (8K by 18 bits). Cycle time is typically 650 nanoseconds for Read/Write.

Crusader Core Model R2016. Ruggedized, stack frame, double-sided construction in 3-D, 3-wire or 4-wire. Designed to withstand harsh environments of temperature, vibration, shock and humidity. Storage capacity is 16K, 8K, 4K, 2K by 1 to 80 bits.

For complete performance data on the new series of Crusader Core memory stacks, see your Fabri-Tek Salesman, or contact: Fabri-Tek Inc., 5901 South County Road 18, Minneapolis, Minnesota 55436. Phone 612/935-8811 TWX 910-576-2913.

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CHECK NO. 7

Of cabbages and kings

In lieu of our usual editorial, we offer herewith a collection of opinions, gripes and just plain thoughts we've had lately concerning engineers and the electronics industry:

•We wish everyone would agree on a name for the optical coupler; or is it photo isolator, or photo coupler? The myriad of names used by different manufacturers is not only confusing, but is probably impeding the use of this worthwhile component.

•That old adage about bad times being the right time to get the edge on your competitors has proven right again. Those companies that maintained a respectable R & D program throughout the recent recession have been introducing exciting new products this year at a rapid rate. Those who eliminated development programs as a cost-saving measure are now going as fast as they can to make up for lost time. But significant new products cannot be turned out overnight. And every passing month is a month lost to the competition.

•In a couple of weeks, campaigning for November's election will really begin in earnest. We'd sure like to see engineers everywhere actively campaign for and support the candidate of their choice. Not only would it help put to rest the stereotype image of the disinterested, introspective engineer, but it would show the young voters, many of whom view science and technology with skepticism, that engineers do care how technology is used.

•We heard of a "name" manufacturer who began receiving numerous customer complaints about lack of sensitivity in a certain model stereo receiver. Upon checking, the manufacturer found that the unit, as designed, did indeed fall well short of its specified sensitivity. The solution? A directive from the marketing department to distribute existing stock only to outlets in large metropolitan areas—where lack of sensitivity supposedly is marked by nearness to transmission facilities. Clever? We don't think so.

•Everyone is familiar with that classic poster showing the rather dumb-looking grad who is saying, "Yesterday I couldn't even spell injuneer and today I are one." We'd like to go on record as saying that such a depiction is completely atypical. The overwhelming proportion of the material and correspondence we receive from our engineer readers is highly readable and exhibits good grammar, syntax and spelling. An occasional few do fall short of this quality. But after all, nobody—not even edittors am perfect.

Frank Egan
Editor

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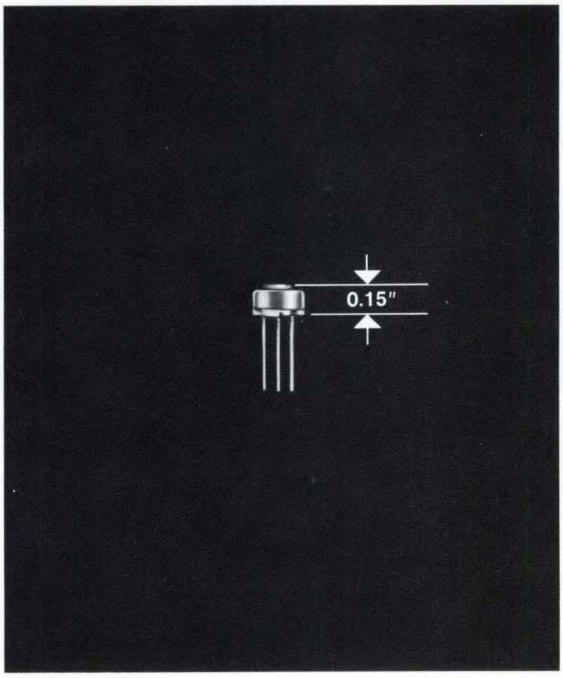
New from Helipot: the lowest trimmer profile in the business.

SHOWN ACTUAL SIZE



You can't do better than our Series 82 Trimmers for small size and low cost . . . and, of course, Helipot dependability. These ¼," single-turn, general-purpose cermet models have the lowest profile in the industry with a proven cermet resistance element that can be set to any voltage ratio within 0.05% of full scale. Sealed metal housings, solid stops, and essentially infinite resolution. They'll save you space—they'll save you money. (Our prices start at $1.40 list.) Two good reasons to write for specs and prices today.

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CHECK NO. 9

5 LINEAR MONOLITHIC SUBSYSTEMS

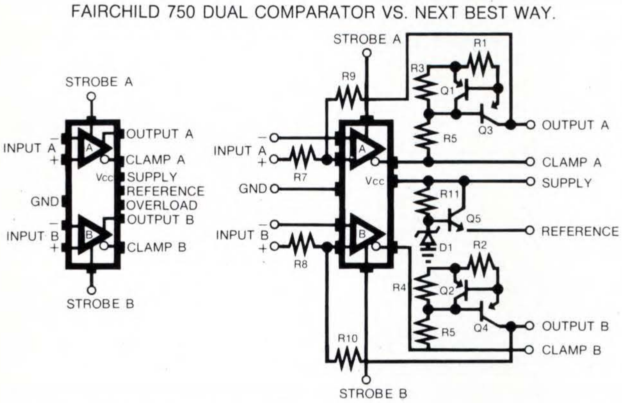
Subsystems: highly complex functions on a single chip. That's where it's happening in linear today. Where Fairchild is. In op amps, voltage regulators and interface.

Look at the facts. In the last 6 months alone 5 new Fairchild monolithic linear subsystems were introduced and are now in volume production.

New 791 High power op amp
Our latest monolithic op amp subsystem has 1 amp output at ±12 volts and automatic circuit protection. Everything is on one chip, so installation's easier. Fewer external connections, testing's easier, less external electronics. Naturally, system costs go down, system reliability goes up. Internally protected against short circuits, power and thermal overloads. 100-piece price: $12.50.

750 Dual comparator

FAIRCHILD 750 DUAL COMPARATOR VS. NEXT BEST WAY.



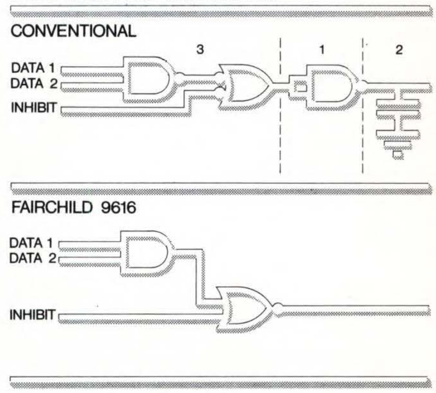
The world's first monolithic comparator subsystem. Eliminates up to 17 discrete components other comparators require for equivalent function and drive capability. A totally-self-contained subsystem consisting of two high-output current, independent comparators on a single chip. Eliminates the external components, board space, and virtually all the engineering calculations necessary to make other comparators function reliably and safely in complex control applications. 100-piece price: $5.95.

776 Programmable op amp
This subsystem is the closest thing to a universal op amp yet devised. Already an industry standard, it's a high quality device that, with the addition of a simple external resistor, can be tailored for optimum performance over an enormous span of applications. The wide range of programmable characteristics make it one of the most versatile and useful op amps to appear in years. Applications range from a nanowatt amplifier to a high-accuracy sample and hold amplifier. 100-piece price: $3.00.

7800 3-terminal voltage regulator
Seven members (5V, 6V, 8V, 12V, 15V, 18V, 24V) compose this family – the first with complete voltage regulation on one chip. The first high quality, sophisticated, versatile, yet simple way of solving VR design problems. At a price so low they can be inventoried in quantity, for use as required. Complete and self-contained in one TO-220 or TO-3 package. And fully self-protected: internal current limiting, thermal shut-down, safe area compensation protect device from current, power, temperature fluctuations. Typical 100-piece price: $1.75.

9616 EIA line driver (& 9617 receiver)
Our 9616 triple line driver subsystem has both internal inhibit and slew rate control. And it's all on one chip. Our 9617 EIA triple line receiver completes the set. They meet all EIA RS-232-C specs. And more. Together, they provide the simplest low-cost solution to problems at the interface in data terminal equipment and data communications. 100-piece price is $4.50 for the 9616; and $3.50 for the 9617.

COMPARISON OF EIA DRIVERS.



Conventional EIA Driver (1) requires external slew rate control capacitor (2) and external gating for inhibit function (3). 9616 EIA Driver requires neither.

93 Linear products in all
Can any other linear-maker make that claim? No way. Whatever your linear needs, the answers are MADE IN FAIRCHILD.

- Industrial controls: 1-Amp op amp; high current comparator, AC control.
- Op amps: general purpose; low input current; high speed; low drift.
- Voltage regulators: general purpose; high current; high and low voltage.
- Interface: drivers/receivers; comparators; D/A conversion; memory.
- Consumer: TV systems; entertainment systems; communications.
- Custom: automotive; consumer; military.

Check us or your friendly Fairchild distributor for products and literature.

MADE IN FAIRCHILD

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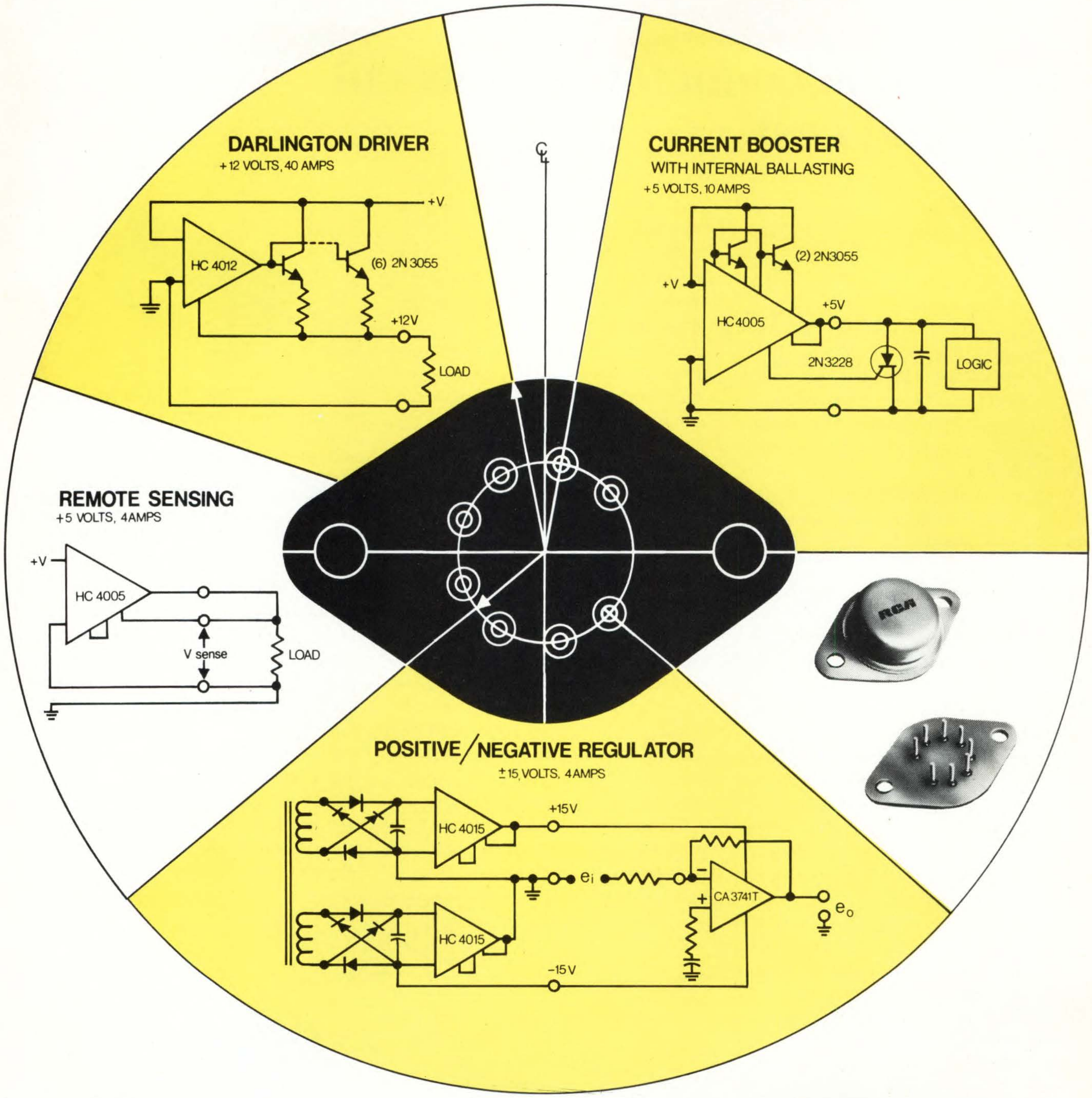
CHECK NO. 10

Why waste time on regulator design? RCA Hybrid Regulators are ready NOW.



Why spend design time on series voltage regulators? When you standardize on RCA power hybrids, you get both performance and flexibility—designed-in, built-in, and tested to cover a broad sweep of your applications requirements. You'll be able to reduce sub-system size, cut design time. And cut your costs, too.

Broad Coverage. RCA series voltage regulators in hermetic steel TO-3 style package can handle a wide range of your regulator requirements from simple slot supplies to computer peripheral equipment. Check these maximum performance highlights:

± 0.6% load or line regulation	HC4005	HC4012	HC4015
± 0.3% load or line regulation	HC4005A	HC4012A	HC4015A
Output voltage	5V	12V	15V
Output current	4A	4A	4A

Versatility. Terminal connections permit you to connect the regulator as a Darlington driver to increase current-regulating capability to 100 amps. The circuit has remote sensing and 40V line-voltage capability. In addition, it uses a series pass element for regulation, and includes both foldback and crowbar-trigger networks.

Pricing. Another big feature. HC4005, 4012, 4015 at $7.50 per unit (1,000 quantity). "A" types at $7.95 per unit (1,000 quantity).

So why be bothered with regulator problems? Check RCA for your series voltage regulator needs. Available now in production quantities.

For more information see your local RCA Representative or your RCA Distributor. For technical data on specific types, write: RCA Solid State Division, Section 50H-15 /UC06, Box 3200, Somerville, N.J. 08876.

RCA Solid State
products that make products pay off

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CHECK NO. 25

New semiconductor mounts cut time and cost

Recently developed connectors and mounting methods for LSI devices hold promise for slashing costs and reducing assembly time. The new developments include:

- Two MOS/LSI leadless, flat mount connectors
- A leadless ceramic package that offers easy device replaceability
- A carrier assembly that permits either plugging in or soldering of the IC

One of the new MOS/LSI leadless flat mount connectors is from Amphenol Industrial Div., and called the Planar-Plug-In (PPI) connector. It boasts the elimination of lead frames, small package and changeability.

American Lava Corp.'s new leadless ceramic package offers package-cost minimization and provides a connector which allows replaceability and a cost reduction in the total system.

Major markets targeted by Amphenol for its new planar-plug-in connectors include business machines, data communications and electronic calculators. The initial product introduction is a 40-lead standard density connector for MOS/LSI circuits.

According to Richard A. Colt, vice president marketing for Amphenol Industrial Div., "the new flat mount planar-plug-in connectors represent a major contribution toward reducing interconnection costs. Essentially, they provide a pluggable system at a cost equal to or less than the cost for a lead frame approach."

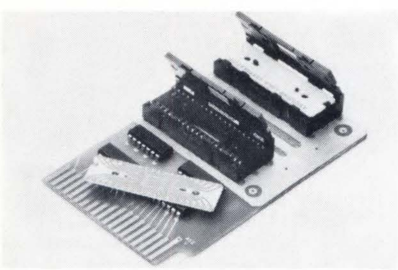


Fig. 1—Amphenol introduces new MOS/LSI leadless connectors. Amphenol Industrial Div.'s new MOS/LSI connector along with American Lava Corp.'s ceramic substrate for the new Planar-Plug-In connector is inserted in typical PC board applications.

Aside from the inherent economic advantages of the PPI connectors, there are several other advantages, according to Colt.

PPI features include: smaller package than other methods, greater packaging density and a tie-down arrangement which requires no screws, but instead has a snap-down lid. Also instead has a snap-down lid. Also provided is positive polarization to prevent the possibility of accidental damage to the circuit through incorrect insertion.

The leadless ceramic package from American Lava Corp. was developed in conjunction with the Amphenol package and is manufactured by the composite technique. This method of construction offers a high reliability package with improved strength and thermal conductivity, and eliminates hermeticity problems. The ceramic is AlSiMag™ 771, a 94% Al_2O_3.

Conductors are refractory metal and exposed areas are overplated with nickel and 60 microinches of gold.

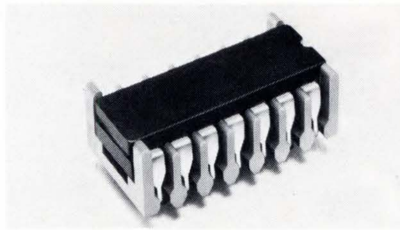
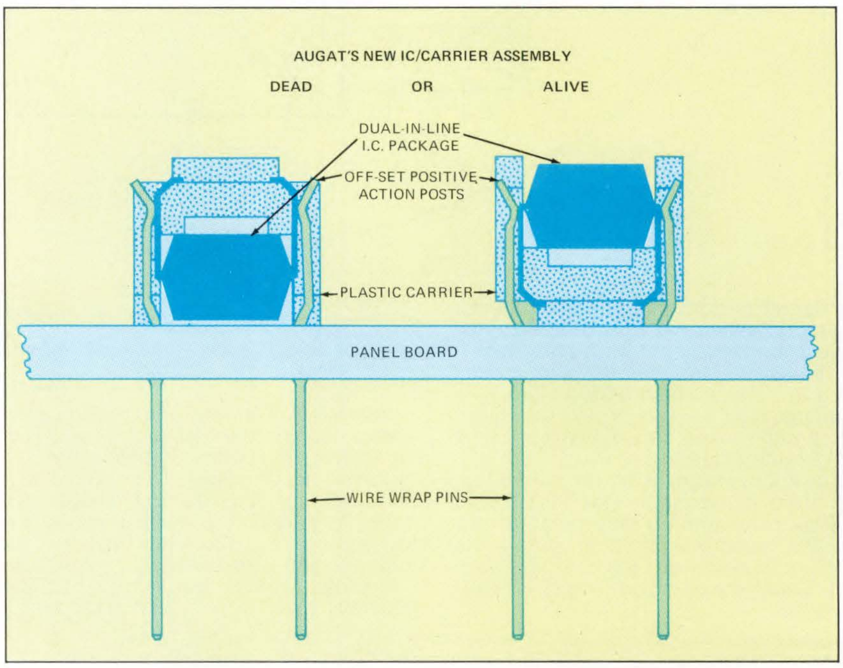


Fig. 2—"Dead or Alive" system IC carrier assembly (alive position with leads down) offers easy snap-in insertion into offset posts of "dead-or-alive" panel. Flexible concept offers design choice of plugging in or soldering of the IC. Plastic carrier also allows frequent changes since it protects leads from insertion and handling damage.

Three versions of the package are available: (1) single place with screened Al_2O_3 insulation layer for maximum economy. This package requires bonding and a cup-shaped lid. Contact pads for connection are on top; (2) three level construction for conventional wire bonding and sealing. Contact pads are on top; and (3) three-level construction as above, but with contact pads on bottom allowing normal orientation of No. 1 lead when placed in the connector.



The second socket for leadless IC's, from Burndy Corp., is a bit like a coffin with a bed of nails at the bottom. The coffin is the box that holds the ceramic substrate for IC or thick film modules. The top of the coffin is a lid that comes down and holds the ceramic against the nails. The bed of nails are tiny spike tips on springs. These penetrate into the solder bumps on the underside of the ceramic—making about 10 mil craters—and this, according to Burndy, forms the same sort of gas-tight highly reliable contact as in wire-wrap or crimp connections.

Additional reductions in packaging cost and time are promised by Augat's new "dead-or-alive" concept, which offers users the design choice of either plugging in or soldering the IC. Either method uses the same basic hardware: IC-carrier assemblies are inserted into the panel board contact patterns, which consist of off-set positive action, Wire-Wrap posts.

The insertion of the IC-carrier assembly with the IC leads down (alive), is the plugged in method. The wave soldering method consists of an IC-carrier assembly with leads upright (dead). This dead or alive operation allows the design engineer to defer a final decision on soldering vs. plug-in until late in the design cycle. The carrier assembly in the dead position does not have to be soldered—it acts as a pluggable socket until soldered.

According to Richard M. Grubb, Augat's Vice President of Marketing, "a large segment of the IC-user market has been favoring PC boards over plug-in panels because of an apparent marginal cost edge, despite the panel's greater flexibility and time and space savings. Since this cost reduction development places Augat in an ever greater competitive position, we expect to make substantial inroads into traditional printed circuit markets.

With Augat's method, the IC leads are crimped around the carrier, allowing electrical contact between the flat surface of the IC lead and the offset pins of the panel, resulting in low contact resistance. When inserted, the IC carrier assembly is firmly held in place and not affected by vibration, shock, and other environmental conditions. The design also permits automatic testing and insertion.

For more information on these developments check the following reader service numbers: Amphenol: check 311; American Lava: check 312; Burndy: check 313 and Augat: check 314. ▭

Microwave power, like the laser, searches for a niche in the market place

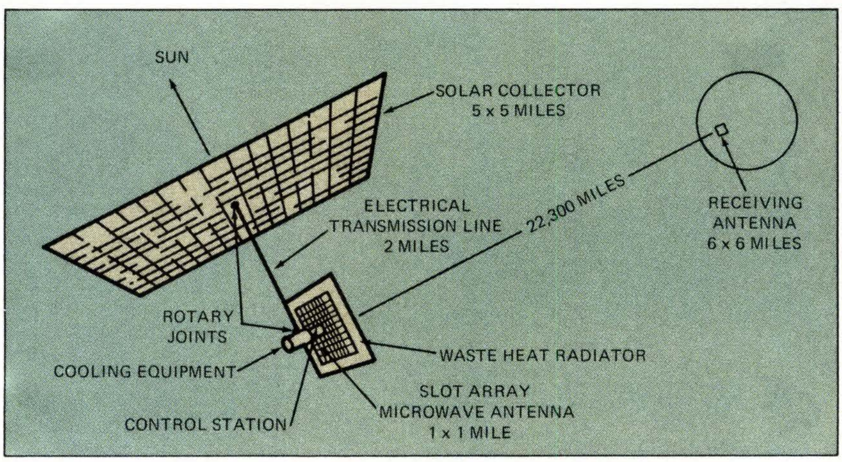
Although it is becoming widely accepted in food processing applications, microwave power is finding it tough to make inroads in other manufacturing applications. Participants at the 1972 Symposium on Microwave Power in Ottawa, Canada indicated that a great deal of work is going on and that some success has been achieved in industrial applications such as curing rubber and foam extrusions, in addition to certain drying applications like edge drying of book bindings and multi-part business forms.

Some other promising areas are in medicine and, for the far future, in the transmission of power from satellites. With regard to the latter application, it looks like 1985 is the magic date when a proper evaluation of free-space transmission of power vs. nuclear power generation can be made. Current astimates show that the cost per kilowatt will be $2100 for microwave and $500 for nuclear, with the largest microwave expense being tied up in the solar cells.

A number of problems have cropped up with microwave power. One deals with microwaves causing cardiac pacemakers to malfunction, and the other deals with the reliability of safety interlock switches in microwave ovens. It seems that some pacemaker manufacturers have failed to compensate for microwave interference with their devices, either through shielding or circuit design. A panel discussion on the topic of microwave interference revealed a lack of communication between oven and pacemaker manufacturers, delaying a speedy solution to the problem.

The interlock switch problem is more basic. Snap-action switches are generally used for this application. Both catastrophic and intermittent failures occur regularly through contamination, contact deformation and welding, and spring malformation. In addition, there is currently no provision to tell when one of the redundant switches has failed, until both fail. Perhaps the solution lies with a clever designer in the semiconductor industry using some of the newer switching and logic techniques.

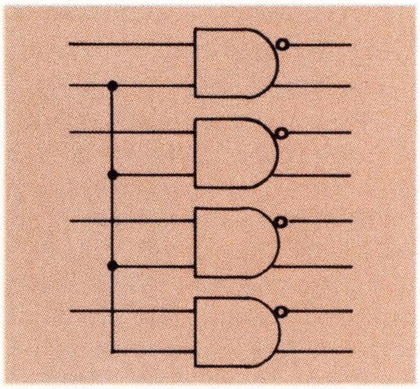
Also of concern to attendees of the symposium are biological effects from exposure to microwave energy. This presented another area of controversy dealing with safe exposure levels. Right now, there are as many different standards as there are government agencies and governments. ▭



Major components of a satellite solar power station designed to produce 10 kW of power.

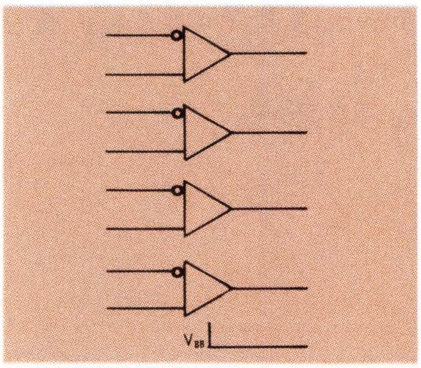
TRANSLATE, MULTIPLEX, INTERFACE, LATCH

Today's designer is faced with the problem of conveying data in the shortest time possible. And this problem is complicated by having to interface low speed TTL sections with high speed ECL systems. Now there is a solution in the form of two new translators that "speak" your language — TTL/MECL or MECL/TTL.



MC10124 MTTL TO MECL TRANSLATOR

A quad translator having TTL compatible inputs and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. High fanout capability (can drive 50 ohm lines), and offers a typical propagation delay of 5.0 ns.

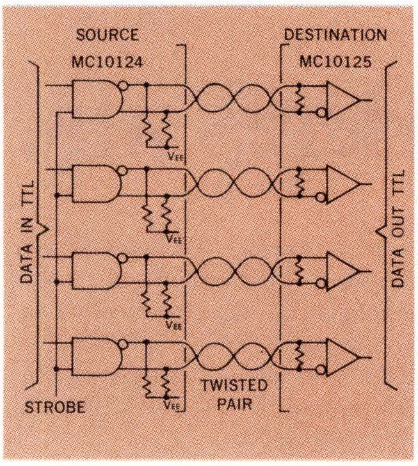


MC10125 MECL TO MTTL TRANSLATOR

A quad translator incorporating differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow use as an inverting/non-inverting translator or as a differential line receiver. A V_{BB} reference voltage is available for Schmitt trigger applications.

TTL/MECL, MECL/TTL OR TTL/TTL

Although usually used to interface between high speed ECL systems and low speed TTL sections, the translators can improve data transmission between two TTL pieces of equipment. A typical example would be a data line for talking between cabinets and/or remote sections of digital machines. The complementary outputs of the MC10124 can drive a differential twisted pair data line which is received by the differential receiver inputs of the MC10125.



This application provides:

- High speed operation with clock rate typically in excess of 75 MHz.
- Excellent noise rejection. The MC-10125 has common mode rejection of ±1 volt specified.
- Quad translators offer minimum package count over conventional duals.
- Strobe capability. The MC10124 has an input common to all four translators to sample input data.

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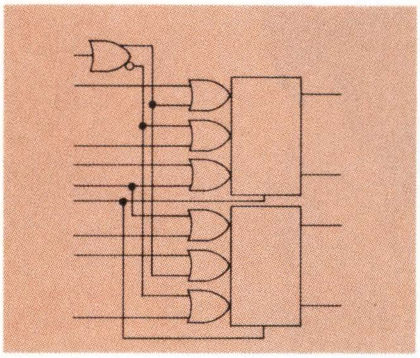
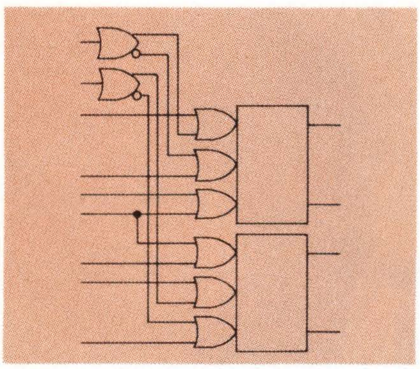
...MECL 10,000 Speaks Your Language

Besides moving data, a designer requires basic storage elements. Two new multiplexer/latches are now available for applications in high speed central processors, accumulators, register files, instrumentation, and high speed digital communication systems.



MC10132 DUAL MULTIPLEXER WITH LATCH AND COMMON RESET

The MC10132 provides a common select input for both latches. Information selected at the inputs is latched on the rising edge of the clock input. A common reset input is provided to reset the latches.

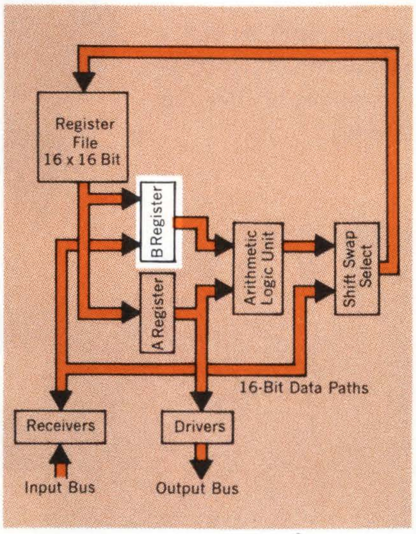


MC10134 DUAL MULTIPLEXER WITH LATCH

The MC10134 offers two latches with separate select inputs for each of the two pairs of data inputs. Each select input determines which information will be provided to the appropriate latch.

MINICOMPUTER STORAGE SIMPLIFIED

One typical application of the MC10134 is temporary



storage in a minicomputer such as the arithmetic section illustrated.

Data may be entered into the "B" register from either the register file or the input bus, requiring a multiplexed input to the register. Eight packages of the dual latch are necessary to construct a 16-bit register. And reset capability is available from the MC10132 if required.

MECL 10,000 APPLICATIONS ASSISTANCE

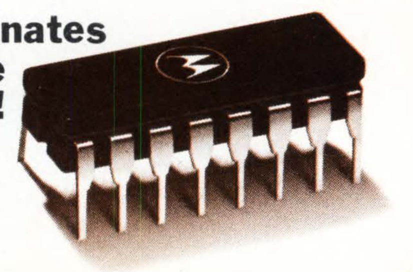
Three new application notes are now available to assist you in applying MECL 10,000. Briefly, these are:

- AN-556: Interconnection Techniques. Describes some of the characteristics of high speed digital signal lines and provides wiring rules for MECL 10,000.
- AN-565: Using Shift Registers As Pulse Delay Networks. The note develops a circuit useful for timing basic computer decisions or for use as an adjustable digital delay line for pulses.
- AN-566: High Speed Binary Multiplication Using The MC10181. With a 4-bit arithmetic unit you can reduce both package count and interconnections in a ripple multiplier and achieve very fast multiplier times.

For complete specifications on these new products and applications information write to Motorola Semiconductor Products Inc., P. O. Box 20912, Phoenix, AZ 85036. And for immediate evaluation call your local Motorola Distributor.

MECL 10,000 is the industry's #1 fastest growing high-speed logic family. Whether your need be applications assistance, system speed, increased performance, or cost reduction — *MECL 10,000 speaks your language.*

MECL 10,000 eliminates the alternatives. Evaluate and compare!



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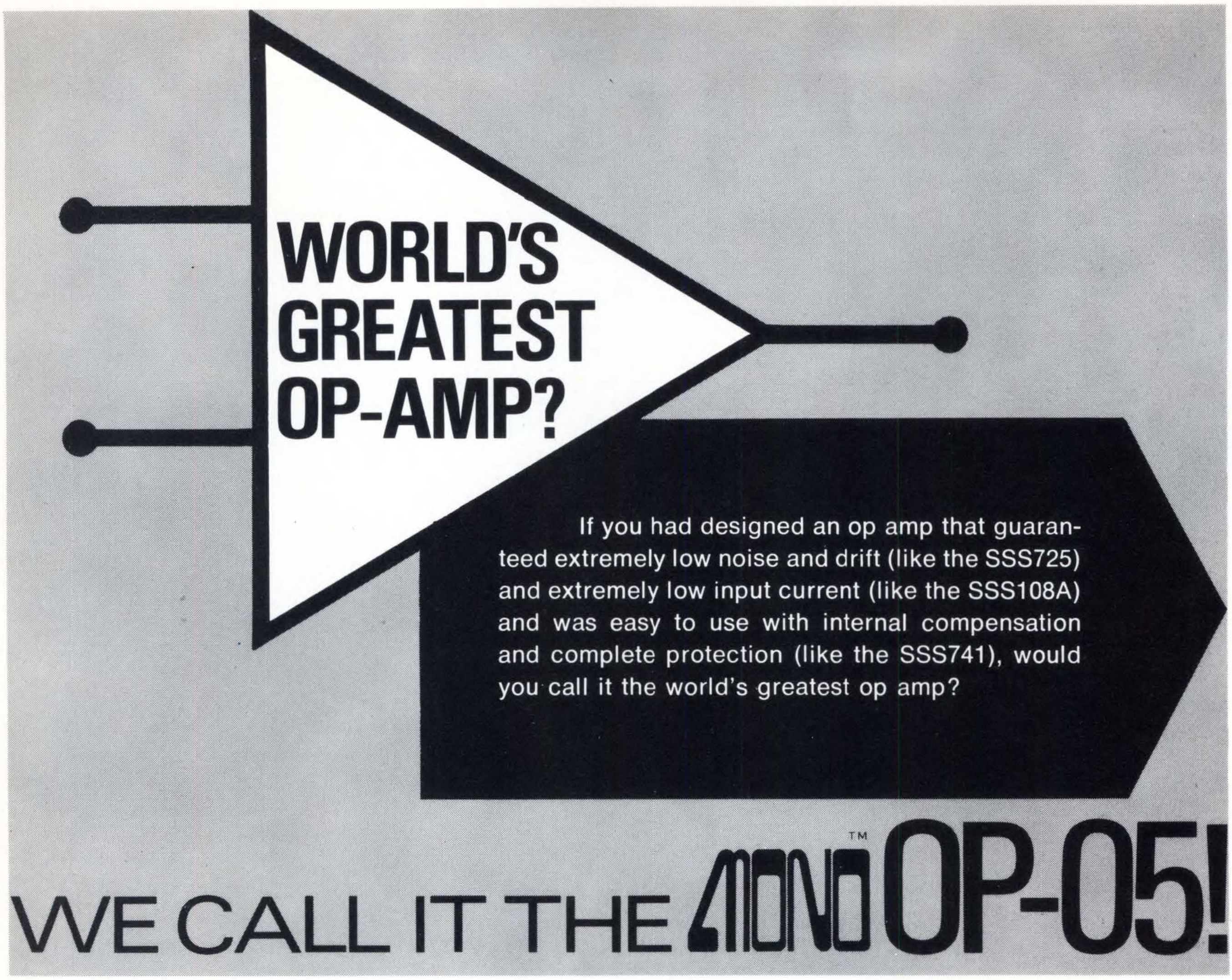

Here are the facts on the new MONO OP-05 *Instrumentation Operational Amplifier:*

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V_{os} Max (mv)	0.5	0.5	1.3
I_B Max (nA)	3.0	4.0	7.0
R_{in} Min (MΩ)	20.0	15.0	8.0
Noise Voltage Max (μVp-p)	0.6	0.6	0.65
TCV_{os} Max (μV/°C)	1.0	0.6	1.5
CMRR Min (db)	114	110	100
Slew Rate (V/μsec)	0.25	0.25	0.25
Price at 100 pcs.	$19.95 (TO-99, −55°C to +125°C)	$14.95 (TO-99, 0° to +70°C)	$6.95 (TO-99, 0° to +70°C)

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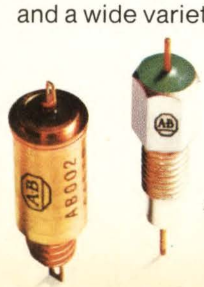
	Circle No.
Publication 5409: type FA, FB, FW, SB, SS ceramic disc capacitors for VHF/UHF.	52
Publication 5410: type FCS, SMFB, SMFO filters for the 50 MHz to 10 GHz range.	53
Publication 5411: type CL multi-layer, coaxial capacitors for connectors.	54
Publication 5414: type MT, MS by-passing capacitors for 50 KHz to 1 GHz.	55
Publication 5416: type BE filters for RFI/EMI suppression.	56
Publication 5417: type SF filters for RFI/EMI suppression.	57
Publication 5418: type AB broad band filters in Pi, T and L configurations.	58
Publication 5419: type DA feed-thru capacitors for VHF/UHF interference.	59
Publication 5421: type SU tubular feed-thru filters for 30 MHz to 10 GHz range.	60



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Use computer aided design to talk to machines in the factory

The steadily-growing use of numerically controlled machines to assemble standard packages into final products cries for design departments to turn to CAD/CAM.

Robert H. Cushman, New York Editor

"Cut out the middleman," has always been good advice for lowering costs and confusion. Production-line automation in the electronics industry is making it possible to cut out a whole group of middlemen between engineering design departments and the factory. The numerically controlled machines that are finding increased acceptance on the factory floor are not only replacing girls on the production lines, but many liason technicians between engineering and the shop as well.

The machines we are talking about are the PC artwork generators, the component inserters, the backplane wirers, the PC drillers, the àutomatic testers, etc. These are the Gardner-Denver Wire-Wrap TM machines, the Gerber plotters and the USM dip inserters that manufacturers so proudly point out on plant tours, and save their pennies to buy more of. With machines like these (and new ones are coming on the market all the time) the manufacturers tell us they can increase production and lower costs without having to add more employees or floor space.

These automation machines have one thing in common. For full exploitation they need numerical input programs. In some other industries, manufacturing engineering departments might prepare these programs for the machines, but in the electronic industry, it seems to make more sense to have the design engineering departments prepare the programs. Not only does this eliminate one historic source of confusion between the two departments, but it gives the engineers a good start in applying CAD/CAM to more of their work.

The abbreviation CAD stands for "computer aided design" and the abbreviation CAM stands for "computer aided manufacturing." We will often put them together as CAD/CAM to emphasize that they are but different ends of what should be one single process flow. CAD is associated with the upstream end of the design-manufacturing process and CAM with the downstream end, as shown in **Fig. 1**.

Those using CAD/CAM tell us that at this point in time, CAM is the most practical. CAD is still in the process of being developed conceptually. They have also indicated that both CAD and CAM are evolutionary processes which take engineering departments years to gradually develop. They can however be bought as an outside service.

Characteristics of some present systems

EDN has not made an exhaustive study of all CAD/CAM

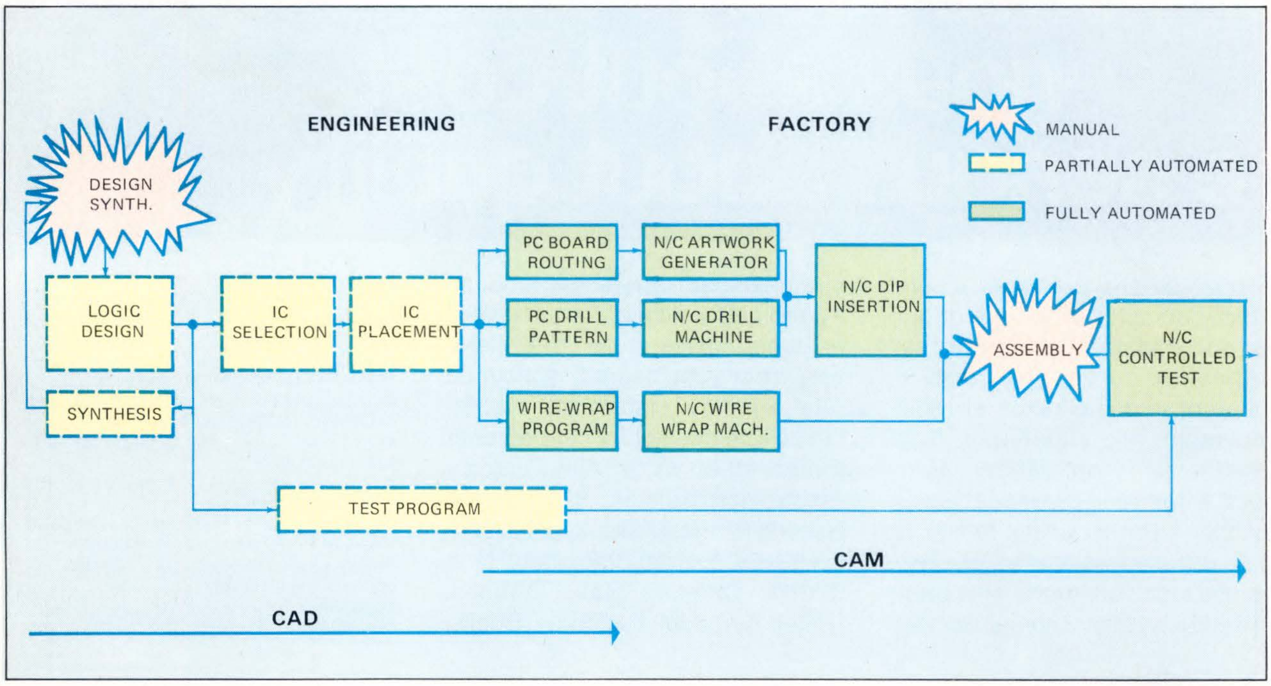

Fig. 1—Flow of the CAD/CAM contribution to electronic design and manufacturing is shown to be overlapped: CAD is most associated with the creative engineering process and CAM is most associated with manufacture. Computers are becoming solidly entrenched in CAM applications, because they are the obvious way for engineers to prepare the instructions for the N/C machines on the factory floor. The paper tapes at the interface between engineering and factory symbolizes this new form of communication that is displacing engineering drawings. Both CAD and CAM are evolutionary processes which take years to develop.

users, just a random sampling as the examples will show. However, we did note some features which we suspect can be extrapolated across all users. First, we saw no indication that any one type of computer installation was becoming most popular. We saw medium sized computers, being used in a dedicated fashion. We saw larger computers being used in a shared fashion. We saw outside timeshare services being used. We saw the computer being used on an on-line interactive mode. We saw computers being used off-line in a batch mode.

About the only common elements were the relatively large assortment of peripherals and the way the data base was the focus of the process. Typical input peripherals would be keypunch stations for preparing card inputs and digitizers for converting points on graphic layout drawings into machine language. A typical bulk-memory add on would be a disc file. Typical output peripherals would be punches for preparing paper tapes for N/C controlled machines and graphic plotters for preparing artwork for PC boards.

The focus on the central data base was evident from the nature of the programs. The computations themselves used at the CAM tend to be rather simple manipulations of the data base. They remind one more of business data processing than sophisticated scientific computation. There is considerable attention paid to housekeeping the data base. Often there will be some error-checking routine between each of the computational steps. The users say that this is not because CAD/CAM generates more errors, but that they want to take advantage of the computer's ability to almost completely weed out the errors that were such a costly fact of life in manual systems. As more MSI and LSI complexity is introduced into electronic products, it will be more essential that the data base be reliable, they say.

Another sort of housekeeping activity was to use the computer as a librarian or file clerk for the data base. Ideally in the future it should be possible for many different engineers, purchasing agents and manufacturing foremen, to have rapid access to the same data base via remote terminals on their desks. Already, this appears to be happening as a by-product with those companies using CAD/CAM.

Hardware company builds on CAM foundation

The fact that an established packaging hardware supplier like EECO, Santa Ana, Calif., can take over an engineer's circuit or logic-level sketch of an electronic system and convert it, via CAM programs, into finished configured packages shows how much progress has been made at the CAM end of CAD/CAM. EECO has "grown into" this form of CAM service as a natural by-product of selling their standard hardware for wire-wrap interconnected DIP packages. Now it seems they are stressing their software and documentation prowess as much as their off-the-shelf packaging hardware.

Apparently, a specialist company like EECO has an edge in building up a CAM process because they have the steady flow of packaging business to justify the many years needed to make CAM fully practical. Most engineering departments that work project by project don't have that luxury.

EECO's approach shows how a service operation can reach back towards the design function and take over all the "clean up details" from the circuit creator. EECO reaches all the way back to a rough pencil sketch of a logic diagram. (It can be a pure logic diagram in the sense that the gates and flip-flops don't have to be assigned to particular IC logic-family packages). However, the diagram should be drawn with a particular logic family in mind. It should conform to the logic rules of that family.

EECO transforms the logic diagram into final hardware in a number of cycles, coming back to check with the customer's engineers between the cycles. On the first cycle, an EECO engineer assigns and jots in circuit identification numbers and Mnemonic signal names on the diagram. These will be used to make the circuit intelligible to the CAM process. The drawing (or rather the reproducible copy EECO works with) is handed over to a keypunch department where four girls are kept busy entering these numbers on punched cards. The girls have been trained to enter the data from the drawings in a format that allows the computer to know what is on each end of each logic signal path. The punched cards are then fed via a high-speed (1000/hr) reader into EECO's General Automation 18/30 computer. This computer has been provided with a look-up table for the characteristics of the gates and flip-flops of the logic family that is to be used. Again, the fact that most designs today are based on relatively few logic families makes it possible for EECO to maintain the pertinent data libraries ready for the computer.

Though the data that has been abstracted from the drawing is rather elementary, EECO has found that it is still enough for them to use in making a number of common-sense checks on the accuracy of the customer's design. One gathers that EECO believes it better to run some validity checks on the customer's design rather than risk the inevitable hassles that occur if mistakes are not caught early. EECO wants the reputation of delivering "correct" results.

EECO's check program has the computer look for signal path strings that have a source, but no loads (don't go to any logic-element inputs), or loads but no source. It will

Fig. 2—Industry standards are the basis of the rapid growth of CAM. Starting with the almost universal acceptance of the DIP IC package, there is now a wide range of DIP support hardware that goes all the way up to the backplane level. This hardware standardization has in turn encouraged the development of expensive but labor-saving N/C machines for automatic handling of these standard parts. And these machines are what encourage the historic graphic language of engineering design to be translated into numeric form and handled by the computers.

print out the numbers for these paths on a "Design Exception Report." It will also look for violations of the design rules for the specified logic family, such as fan-outs that are too large for the gate driving ability. It will add these to the Exception Report.

At this point, EECO shows the Design Exception Report plus the marked-up drawing and some other routine print outs to the customer.

The type of mistakes that EECO's computer has been programmed to look for at this stage are:

- Signal paths that have sources but no loads.
- Signal paths that have loads but no sources.
- Power supplies tied to ground.
- Violations of the logic family loading rules.

These checks are but the application of simple common sense but they invariably uncover mistakes, both possible and outright. The computer prints these out in list form on the "Design Exception Report," and EECO sends this back to the customer along with the marked up drawings. The customer's engineer will look over the exceptions, correct the outright mistakes, and explain to EECO which of the possible mistakes really were mistakes and which were intentional. For example, the computer may have noted a signal line "coming from nowhere" into the diagram, and the designer may explain that this is all right because the signal comes from some other separate system and will be wired in by the customer later. EECO asks the customer to initial these exceptions.

EECO's next cycle is to take the checked and corrected drawings, enter the corrections into the computer, and then run the program that assigns the gates and flip-flops into standard IC packages. EECO has its engineers work along with the computer during this phase because they believe that the logic should be functionally grouped for easier signal-flow tracing during later trouble shooting. Some of the programs that have the computer do all the package assignments tend to produce crazy-quilt arrangements of the logic panels. A shift register may zig-zag all over the place because the computer has picked up one flip-flop here, then jumped over there to pick up another, in its attempt to use up all the elements in the packages.

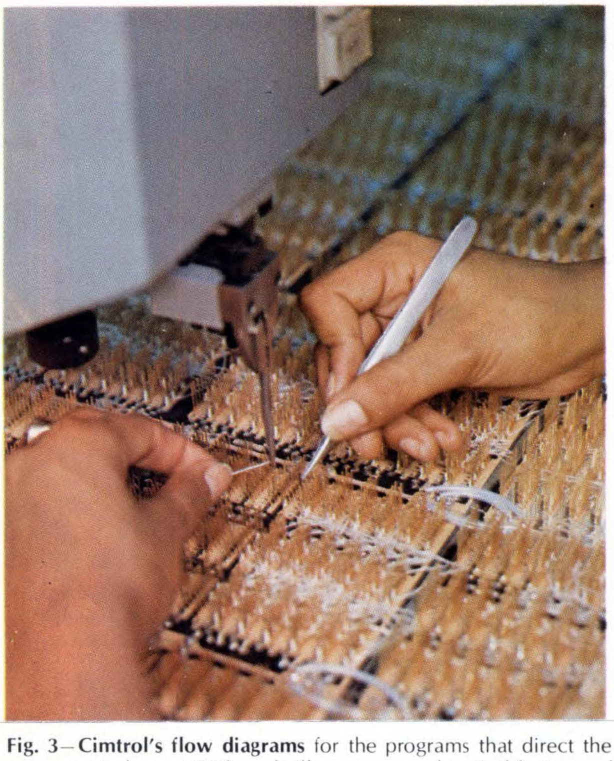

Fig. 3—Cimtrol's flow diagrams for the programs that direct the computer to lay out PC boards illustrate several typical features of today's CAD/CAM: the runs are in a number of separate batches and there is continuous error-checking between steps.

The computer will generate another exception report at the end of this cycle and will print out IC device type lists, pin assignment lists, etc. At this stage, some customers will note the design exceptions but may not make changes in the interest of getting the hardware as soon as possible. They will plan to make the changes later by hand wiring.

EECO finds that some customers will make use of the numbering designations that EECO has developed in performing its CAM processing. They will turn around and enter the EECO numbers for circuit paths as the official numbers on their engineering drawings. Others will incorporate the computer generated lists of IC types, pin lists, string lists, etc. into the service manuals they send out with their products. Though they originally came to EECO just for hardware they end up getting a good deal of the documentation more economically and more accurately than most of their customers.

The value of this documentation by-product of CAM is hard to assess. EECO's Richard Hunter says EECO has had customers who have gone through 20 revisions of products. It seems that just a few are the result of glitches uncovered in the equipment operation; most are the result of customers finding they want more functions. Hunter said that good documentation makes these changes much easier for the designers. For example the designer can go to the "unused logic element" printout that EECO has provided them and find where they can pick up spare gates in the logic packages to to implement the changes. Then they can put out change order instructions and field maintenance can make these changes with a hand gun (going to the spare third level of the wire-wrap posts if they have to).

It seems likely that the ease of modification factor may become much more important now that more computer-type equipment is out on a lease basis. Manufacturer's who lease their product do not like to throw any equipment away. Ideally they would like to keep it on lease with customers forever by a continual series of updating modifications.

N/C company uses its own tools

The CAD/CAM system that the Cimtrol division of the Cincinnati Milling Machine Co., Lebanon, Ohio, has been evolving since 1963 is also an example of working backwards. "Our automation is very shop (or CAM) oriented, as opposed to design (or CAD) oriented," Ed Coodle and Tom Yeager of Cimtrol told EDN. "We saw a need to get the data interfaced between the engineering and manufacturing areas in an automatic manner, so that the shop would receive reliable and consistent information, ready for inserting into their machines."

The Cimtrol system was built around specific machines, such as a Gerber 632 precision drafting table and some of Cincinnati's own numerically controlled drilling and positioning tools. Cimtrol did not use its own minicomputers for the CAD/CAM processing, but does use one of its N/C controllers for automatically positioning wire-wrap guns. The computer used for the CAD/CAM processing is an

IBM 370/145 with a 262k-byte memory.

The Cimtrol engineers say they have reduced their wire-wrap programs to routine and have made strides in similarly reducing IC placement on the PC boards to routine. They have programs to automatically make IC pin assignments after a human has "lightly" partitioned the logic gates into functionally related groups.

But it has proven more difficult to have the computer automatically lay out PC board wiring patterns, Cimtrol engineers say. Their present tack is to use "Lee's Algorithm" and have the program radiate out "waves" from one pin until the wavefront hits a desired second pin, then trace back the path of that point of the wave. (Lee's algorithm is discussed in "Design Automation of Digital Systems," M. A. Breuer, ed., Prentice Hall, Inc. 1972.)

Cimtrol has also worked on some rather sophisticated programs for generating test programs for logic boards. These will be used in conjunction with a N/C controlled board tester of their own manufacture that will incoporate one of their minicomputers. Yeager says that he forsees the need for some large memories in these testers as MSI and LSI systems of sequential logic come along.

Helping the computer with the last 5%

There is a strong vein of common sense to be noted among those who have been using CAD/CAM to earn a living. Harry Keirns, leader of the software design at ATI (Automated Technology Inc.), Champaign, Ill., told EDN that he never worried about not getting the computer to do 100% of the layout routing. "My concern was to have the program adequate for letting the computer route 90% or so of the wires on its own, and then know enough to ask for a human's help," Keirns said.

Design automation was essential for ITA. They were laying out 4 to 6 layer boards containing a thousand interconnection wires for the Univ. of Ill.'s ILLIAC-IV supercomputer. ITA was using a computing system built around a PDP-15 minicomputer with a disc memory. An important peripheral was a high speed Gould electrostatic printer. ITA used this as a low-cost, substitute for a graphic CRT to allow the computer to rapidly and inexpensively tell the human how far it had gotten when the computer called for help. The Gould plotter system could spew out a picture of the routing in one minute at a cost of about one dollar.

"We incorporated criteria into our router program that would allow the computer to know when it was reaching the flat portion of its achievement curve—when it was spending a lot of time in futile attempts to route the last remaining wires of a board," Keirns said. The computer would then stop and activate the Gould plotter to make a proof print. The engineer would take this plot back to his desk, study it, and usually spot the problem right away. Then in ten minutes he'd come back to the computer with some helpful rearrangement that would allow the computer to proceed.

Invariably, the problem that was holding up the "dumb" computer would be ridiculously simple, such as one of the earlier wire routes blocking all subsequent routing attempts from a certain pin. The computer would keep butting up against this obstacle, not seeing that it could not solve it. The engineer would re-route the wire causing the blockage (say to another layer) or shift the pin positions and this would free the computer to continue.

"Perhaps we could have spent a lot of time and come

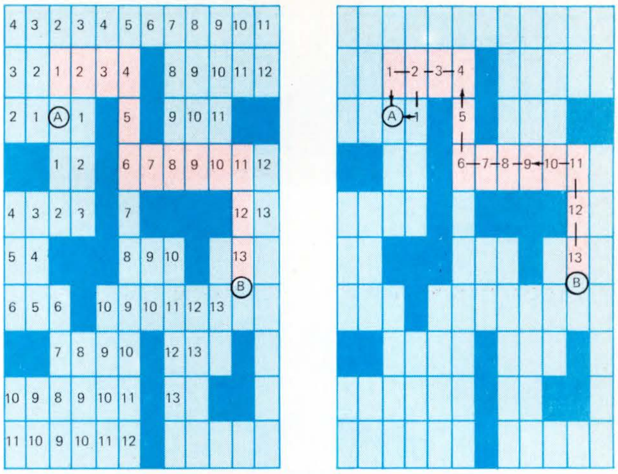

Fig. 4—Lee's algorithm for finding the shortest path between points A and B on a PC board consists of radiating waves or steps out from A, and seeing how many steps it takes to reach B. It is a bit like the way a checkers player thinks out moves in advance.

up with additions to our routing algorithms to take care of these situations, but we did not think it worth the effort," Keirns said. During the first pass, the computer might put down 90% of the wires in ten-minutes running time, then come to a halt, and generate the proof print. In the second pass, after the human had helped it, the computer might reach nearly 100% completing in one minute's time. On subsequent passes if needed, the computer could complete the design within a second's time. A board containing over 100 ICs might only take about a half hour. hour.

"Our Gould plotter cost us about $15K, including interface," said Keirns, which was less than the full graphic CRT, we would have needed to do the same thing. We could scale the display up so instead of having a dense plot of a 6 by 6 in. board, we could have an oversized drawing that would be easier to work with." An advantage of using the high-speed plotter was that the designer would automatically build up a series of hard copy drawings that would show the progress of the routing. ITA still used a pen plotter for the final precision artwork, but this would have been too slow and expensive for the proof plots.

Incidentally, ITA's interest in the Gould plotter caused them to be bought by Gould as the nucleus of Gould's new data-products division. ITA is being moved to the Boston area where they will continue to use their CAD/CAM expertise in developing such products as the interfaces for Gould products. Keirns says that he believes they will be able to make more efficient use of CAD/CAM when they are doing their own work in house, as compared to doing consulting for outsiders. "There were times when we suspected mistakes in the designs we were given, but as consultants we were reluctant to go back and tell our customers we thought they had make mistakes., "Keirns said. "Also, because our CAD/CAM programs were geared to the specific services we were providing, they would not really be capable of uncovering logic-design mistakes from upstream in the design process. We also found ourselves doing layout tasks with the computer, like simple double sided boards that we felt could have been accomplished just as fast with hand taping, simply because a customer wanted them to be done on computer for some reason."

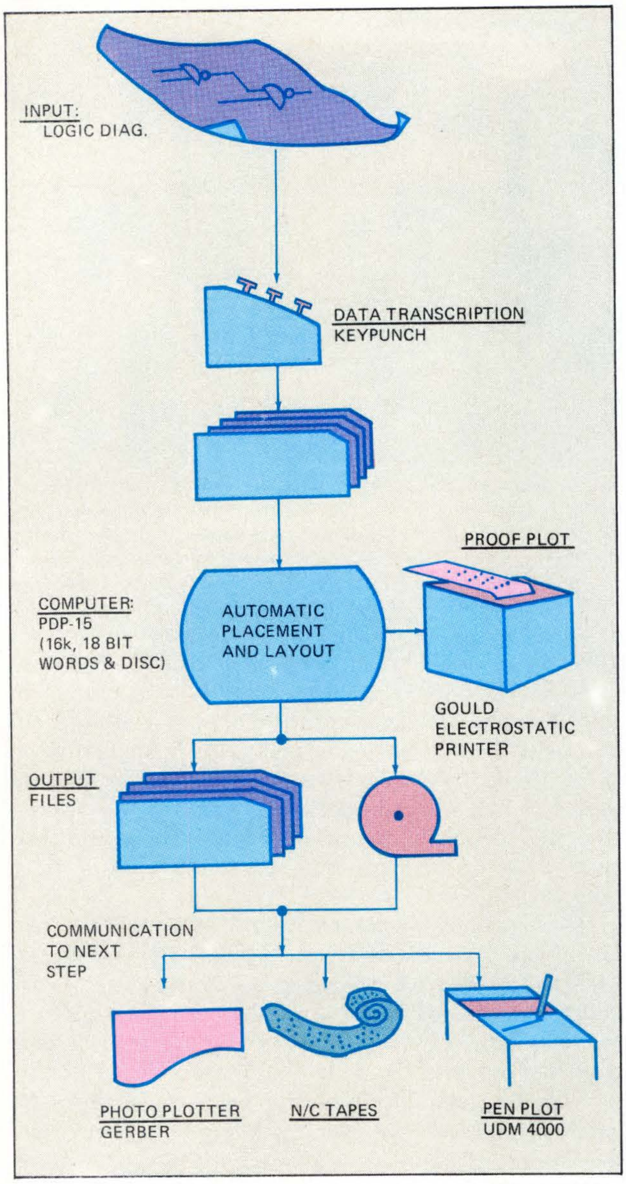

Fig. 5—Overall flow diagram of ITA's CAD/CAM procedure shows how the quick-look Gould plotter was employed in the middle. The rapid proof prints generated by the Gould plotter every time the computer routing program came to an impasse served as low-cost alternatives to an interactive CRT. Actually, in some ways the Gould proof prints were superior to a CRT display because the engineer could take these prints back to his desk, think about them at leisure, write on them, and even overlay several of them on a light table.

Keirns agreed with other CAD/CAM practicioners that one of the weak links in any CAD/CAM system was the initial conversion of data into machine language. "Mistakes would go through and we would find that some of the large, expensive multi-layer boards would have erroneous wiring when completed. Each time we traced back through our CAD/CAM system to locate the culprit it turned out to be some girl at the initial keypunch conversion who had either made a mistake or had misread some handwritten information on a source drawing."

Basic example

We have seen some very basic examples of the principle of working backwards towards automation in many component manufacturing plants. Mostly, they center around the functions of test and inspection, because of the need to generate and communicate quantitative data. One such example comes from a manufacturer of panel meters, Beede of Penacock, N. H.

Beede was having "communication" problems with a customer who was paying a premium price for a 1%-tracking-accuracy, 250° indicator. "We found ourselves involved in a constant back and forth discussion about whether the meters we were shipping were truly meeting their 1% specifications," Beede's Lou Issel told EDN. "We were confident we were, because we were testing them to 1/2% and none of our other customers were having problems. But you don't argue with a customer, you try to communicate better."

To achieve the better communication, Beede engineers developed a semi-automatic checkout station. This gave them a digital printout to 0.01% that they could tear off and ship with each meter. "This tangible indication that we were carefully testing each meter brought the customer's complaints to a halt immediately, Issel said. "The data in this form convinced him he was getting his money's worth."

The Beede tester is an example of "working backwards" because it's need was indirectly suggested by feedback to the engineers from the customer. It is an example of getting the job that counts done with the minimum of automation. An A/D converter that is part of a DPM (digital panel meter), also made by Beede, reads the tracking error and drives a strip printer via the DPM's BDC output. Most important, additional information that identifies the meter, date and meter test position, is also printed.

The woman manning this production test station first sets up the additional information shown to the left of the reading by manual controls. She dials in the meter serial number with thumbswitches, for example. She adjusts the full-scale voltage to put the needle on the full-scale mark, then rotates the large knob at her left to step the input to the meter down through 20% divisions of the adjusted full-scale voltage. These divisions are precisely programmed by the 0.01% resistors on the card plugged into the center of the console.

At each divided down input she notes how far off the needle is from the scale mark it is supposed to be on. She can read this to 1/2% if the meter has a silvered mirror. She then nulls out the small difference with the ten-turn pot on her right, and hits a foot switch to activate the printer. The printer records the bias needed for nudging the needle to the mark as measured by the differential DPM, the DPM being adjusted to read the nulling voltage.

For all their home-brew simplicity, these first steps into automation often have valuable lessons for engineers who are planning ventures into computer aided manufacturing.

•They have solid usefulness. They are the direct opposite of the so called high-power general-purpose do-everything tester that sold to companies for $100,000 only to lie idle because no one felt them quite worth the effort to put to useful work. These home-brew systems are truly application oriented as they were developed in response to real problems.

•They can, like this Beede system, provide the data base that is the foundation of CAM. For example, though Beede does not at this time, they could record the same BDCD that drives the printer of a magnetic tape (a small cassette for example) . . . and store this for later product trends analysis for manufacturing adjustment . . . and even later as input for new design. □

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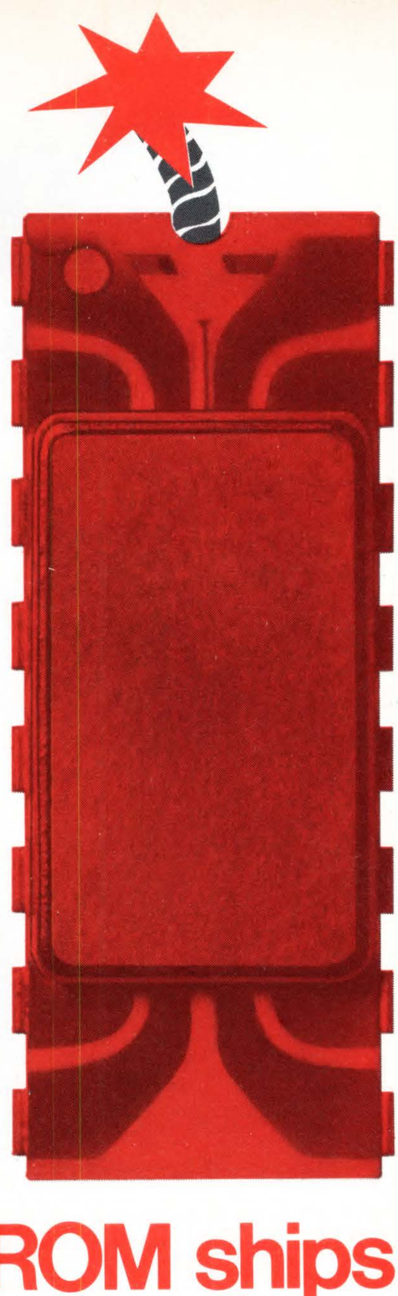

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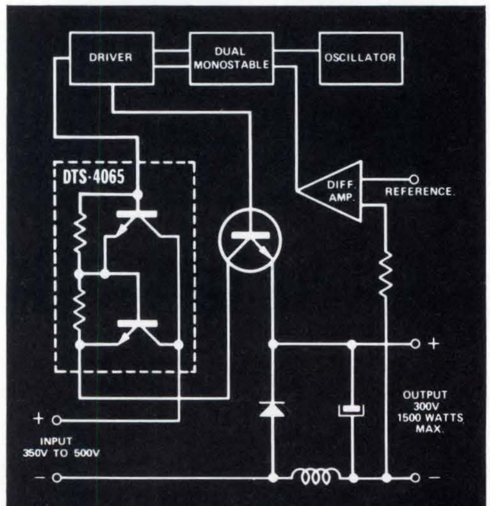

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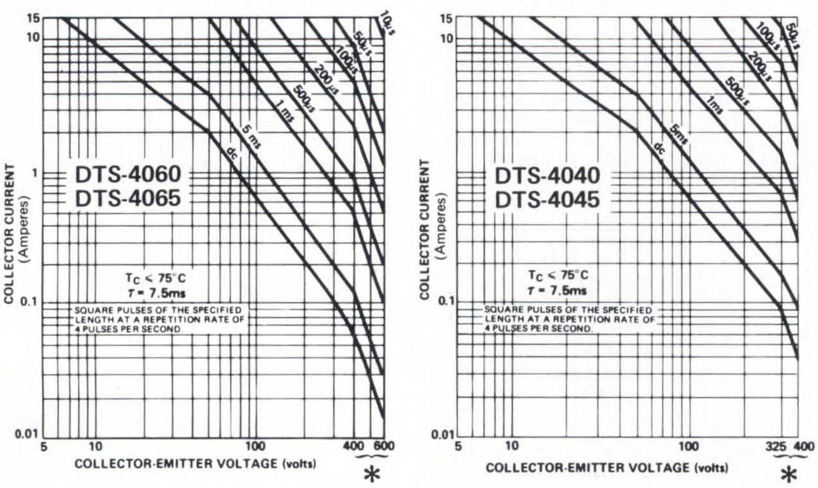

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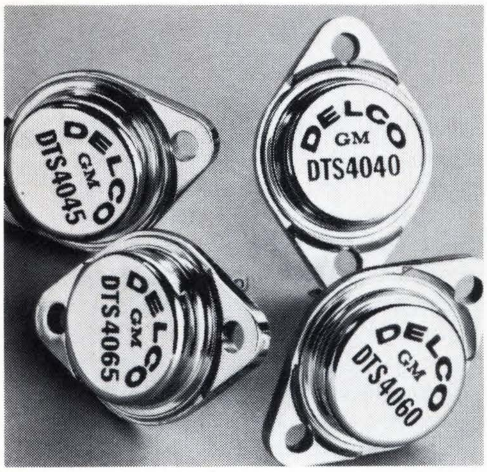

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CHECK NO. 21

New D/A technique leads to an inexpensive converter

Here's an all-digital approach to the D/A conversion problem that eliminates precision-ladder networks and keeps the total component count down.

David J. Guzeman, Teledyne Semiconductor

One of the most common problems occurring in the design of industrial digital-logic systems is that of conversion from digital to analog signals and vice versa. The most common approach to the problem uses voltage comparators and expensive precision-ladder resistor networks. Although this yields extremely accurate converters, it also tends to be very expensive. Here is an all digital approach where the use of MSI components reduces the total component count to a very low number. Cost savings are realized because there are no linear devices used, and hence, the cost of a precision power supply is avoided.

Use two counters and a flip-flop

The basic analog-to-digital conversion technique uses two counters and a flip-flop (**Fig. 1**). In this simplified circuit both counters are the same modulus and both are run from the same clock source. Each of the counters has an output, called the terminal-count output, that delivers one pulse every time the counter reaches the end of the count modulus. A counter that is counting in cycles of 256, for example, would deliver one pulse on every 255th count (zero is the first count). In addition, the inverse of the terminal-count output is provided so that both active HIGH and active LOW terminal counts are available for use.

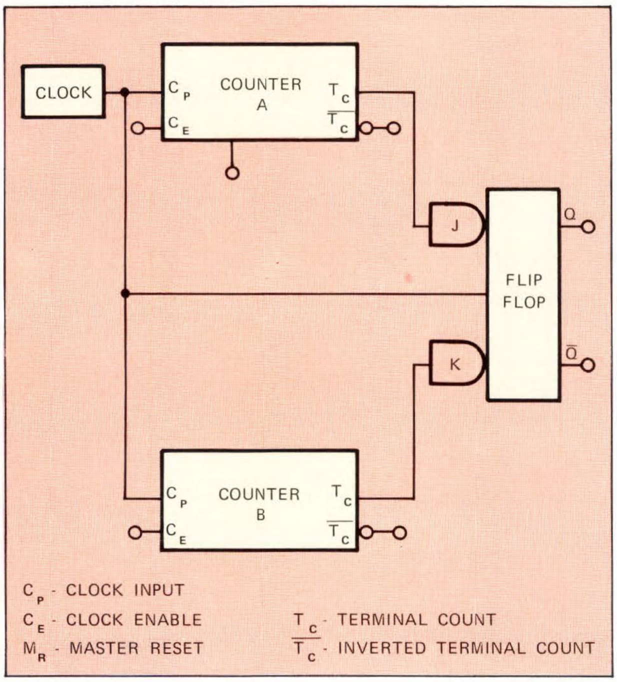

Fig. 1—Two counters and a flip-flop are the basic components for this D/A conversion technique. The duty cycle of the flip-flop depends on the phase relationship of the two counters. Resolution of the duty cycle is controlled by the counting modulus.

When these counters are connected as in **Fig. 1**, the terminal-count output of Counter A sets the flip-flop (the assumption made here is that the counters are out of phase; that is, both terminal count outputs do not deliver pulses simultaneously). For the example shown, the output of the flip-flop follows a 50% duty cycle, going HIGH on every pulse from Counter A and going LOW on every pulse from Counter B (**Fig. 2a**). The 50% duty cycle is due to the fact that these are mod-4 counters that are offset or out of phase by two counts. If the counters were only off by one clock pulse, then the output of the flip-flop would be following a 25% duty cycle (**Fig. 2b**).

It should now be apparent that the duty cycle of the flip-flop is wholly dependent upon the phase relationship of the two counters, and that the resolution of the duty cycle is dependent almost wholly upon the size of the counting modulus. With counters counting to 100, the timing cycle could be controlled to one part in 100, which is 1%.

Before the system can be used there is one complication that must be taken care of. Consider the possibility that the two counters might be in phase. When this occurs the desired state of the flip-flop is for Q to be LOW and stay LOW as long as the counters are in phase. Unfortunately, if both counters are in phase, both of the terminal count outputs will deliver pulses simultaneously. This would normally serve to set the flip-flop into the condition where Q was HIGH (because of the JK nature of the flip-flop). This condition is resolved by using an inverted signal from the terminal count output of Counter B to reset the flip-flop to the condition of Q being LOW.

The principle of using the phase difference between the two counters could be expanded directly into a D-to-A application. The technique would entail periodically resetting the counters, and then setting into Counter A the number that would represent the phase difference. Counter A then becomes the advanced counter. However, when there is a possibility of either one of the counters needing to be the advanced counter, the technique becomes awkward. A better technique is to use the two counters coupled with a signal-conditioning technique that removes the need for one counter to be advanced. This will be developed into a dynamic system that can

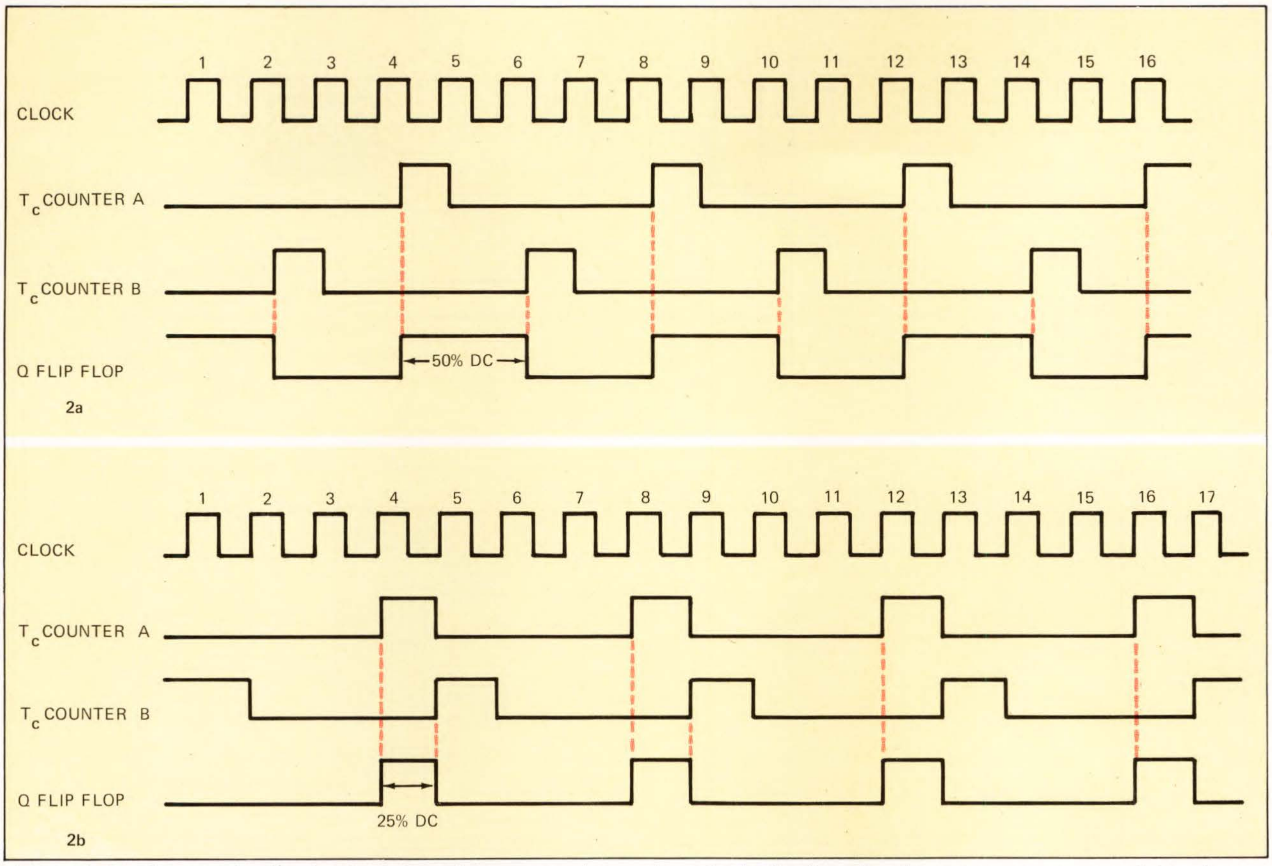

Fig. 2—Timing diagrams for the circuit of Fig. 1 shows a 50% duty cycle (**a**) for the flip-flop when the two counters are out of phase by two counts and a 25% duty cycle (**b**) when the counters are out of phase by one count. Modulus-4 counters are used in the example.

track the digital inputs very closely.

Eliminate counter reset problems

Fig. 3 shows the conditioning circuitry used to detect the pulse on the signal input line. The purpose of the circuit is to disable the counter for one clock pulse each time an input pulse appears on the signal input line. In operation, the first JK flip-flop, A, is supplied with signals that are out of phase (because of the inverter on the K line). With no input signal, flip-flop A will sit with its Q output LOW. The second flip-flop, B, is also conditioned by flip-flop A so that its Q is LOW. Both of these low outputs are fed to gate A, which delivers a logic ONE signal to the enable input of the counter. Thus, with no input signal on the input line the counter is enabled and will count one count every time it sees the rising edge of the clock line.

Consider what happens when a pulse, several clock-pulses long, arrives on the input-signal line. The JK inputs of flip-flop A are conditioned by the signal pulse, and when the next falling edge of the master clock arrives (the JK flip-flops used here are charge-storage devices that trigger on the falling edge of the clock pulse), it toggles into the Q HIGH state. This immediately causes output gate A to switch LOW, which disables the counter. Note that since the counter triggers on the rising edge of the clock pulse, it counted one count when this clock pulse arrived. The counter is disabled for the next clock pulse that arrives, and it is this second clock pulse that is ignored by the counter. Flip-flop B, however, does not ignore it. It switches to the same condition as flip-flop A; that is, with Q HIGH. The output of $\bar{Q}$ of flip-flop B is of course now LOW, and it forces the output of gate A HIGH, which

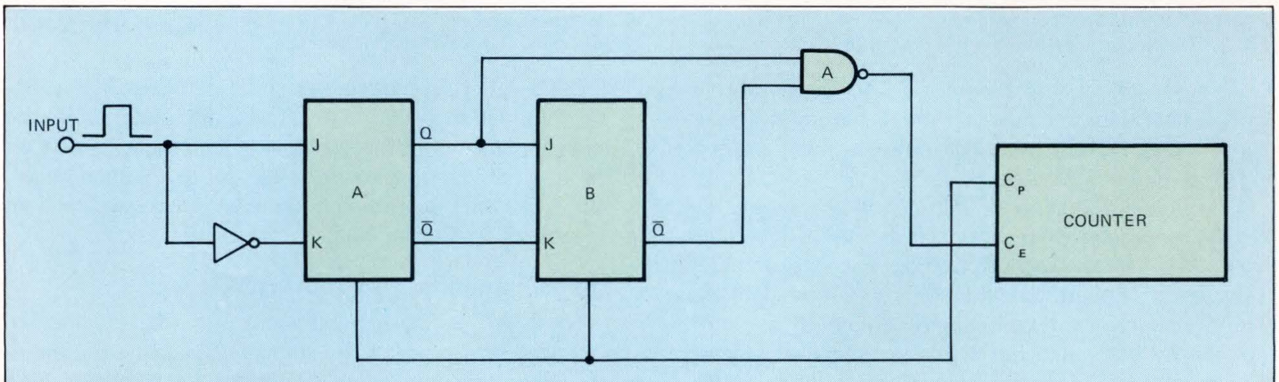

Fig. 3—The input conditioning circuit retards the counter by one count each time the signal input line receives one pulse. This eliminates the need for peridocially resetting the counters.

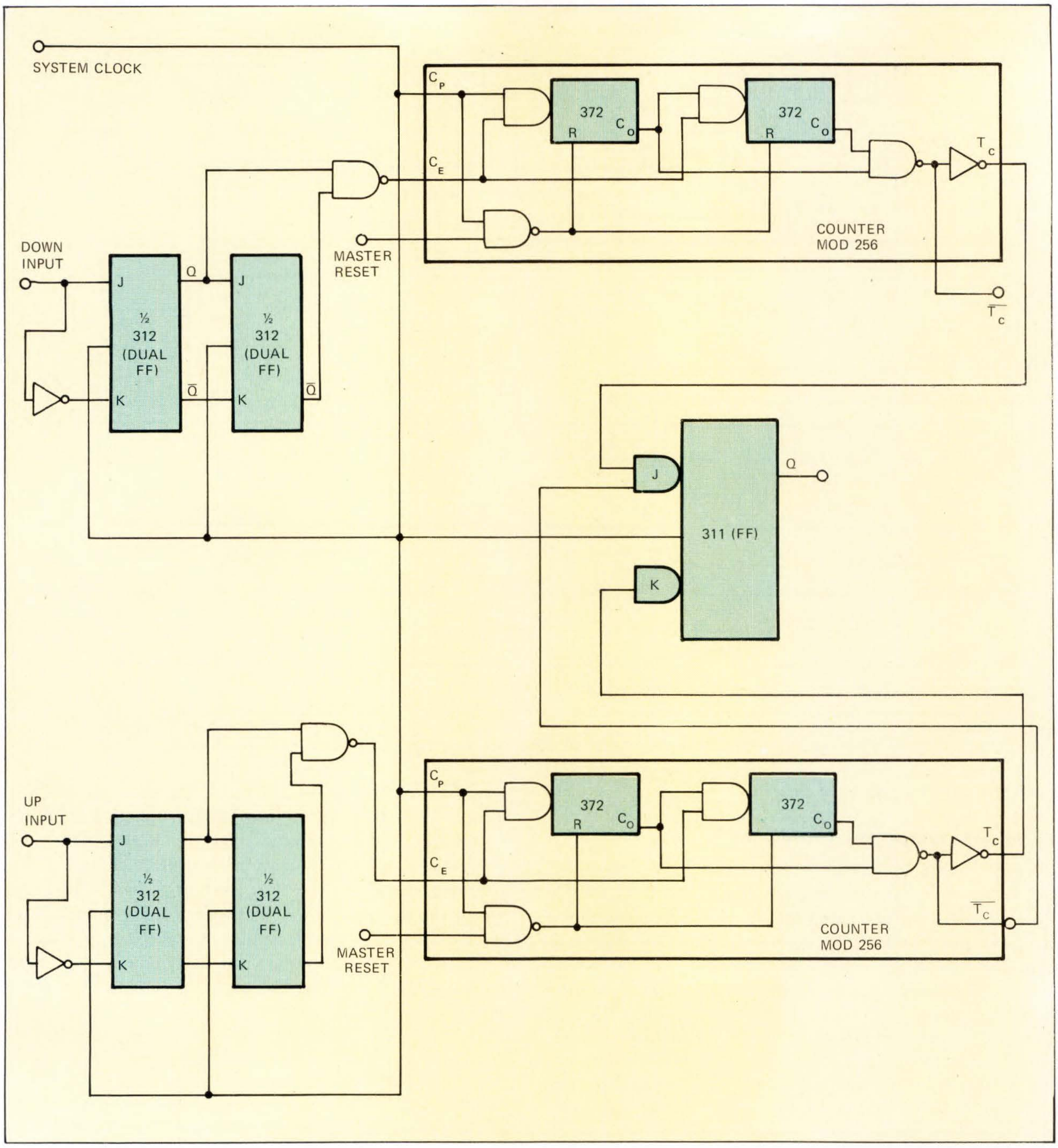

Fig. 4 – The complete converter can be built with a small number of parts. The number depends on the resolution required. In this example, a pair of hexadecimal counters were used to provide a divide-by-256 counter. Note the extra J input to the output flip-flop (not shown in **Fig. 1**). This input resets the flip-flop to the condition of Q being LOW when the two counters are in phase.

once again enables the counter. The flip-flops will remain in this state until the pulse on the signal input line is removed, and the next two clock pulses will then reset both flip-flops to the LOW state.

For proper operation of this circuit the master clock should be at least twice as fast as the input signal pulses. The purpose of the second flip-flop is to ensure that long signal pulses only disable the counter for one clock pulse. The net effect of the conditioning circuit is to retard the counter by one count each time the signal-input line receives one pulse. The complete system is shown in **Fig. 4**. A pair of hexadecimal counters were used to provide a divide-by-256 counter.

While an op amp integrator could demodulate the analog information coded into the flip-flop duty cycle, the ideal application for this conversion technique uses a load that performs the integration itself. All that is then necessary is to buffer the flip-flop output with a power amplifier capable of driving the load.

Simplify multiple D/A converters

There are many useful variations of the basic principle. One is shown in **Fig. 5**. By slightly elaborating on the input-control circuitry, either the counter can be made to skip a count or jump a count. This means that Counter A need no longer have the ability to skip pulses, since advancing

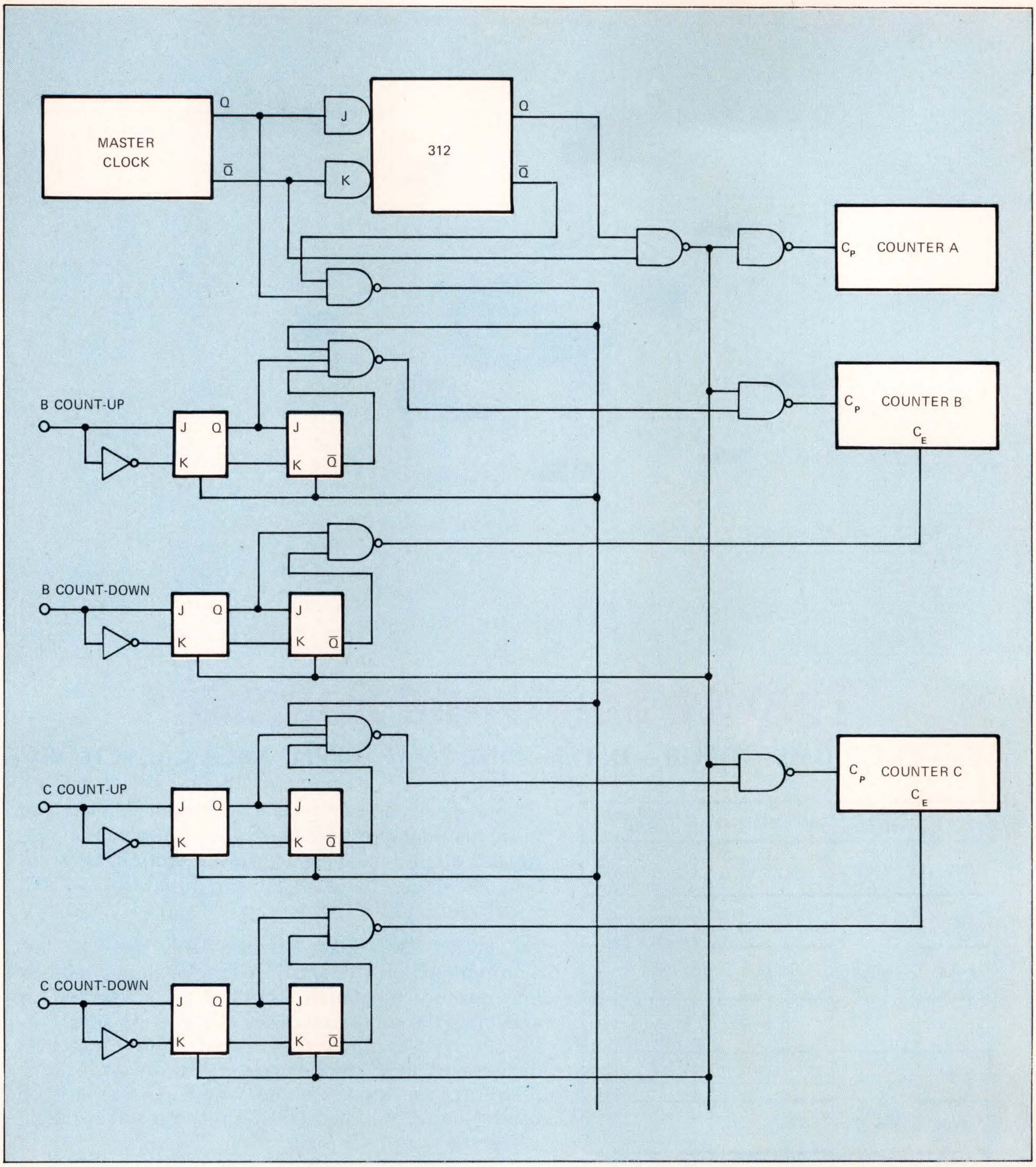

Fig. 5 – Slightly changing the input circuitry allows a single counter A to be used with multiple second counters. This technique requires a two-phase clock for the system.

B by one count has the same effect as retarding A by one count. Since Counter A no longer has to skip counts, it can be used for several other conversion counters. In **Fig. 5**, Counter A is being used as a master for both Counter B and Counter C.

This technique requires the generation of a two-phase clock. The circuit that causes the counter to skip a count remains the same. However, to this circuit is added a similar circuit that causes the counter to count the second out-of-phase clock whenever a signal pulse is added to the count-up signal line. Thus, each of the conversion counters can either increase or decrease its phase difference with the master counter. □

Author's biography

David J. Guzeman is special projects manager at Teledyne Semiconductor in Mountain View, Calif., where he is currently spending most of his time organizing product seminars for Teledyne customers and salesmen. Before joining Teledyne, Dave worked for Sunbeam Corp. for four years. He received a BS in Physics from Aurora College at Aurora, Ill.

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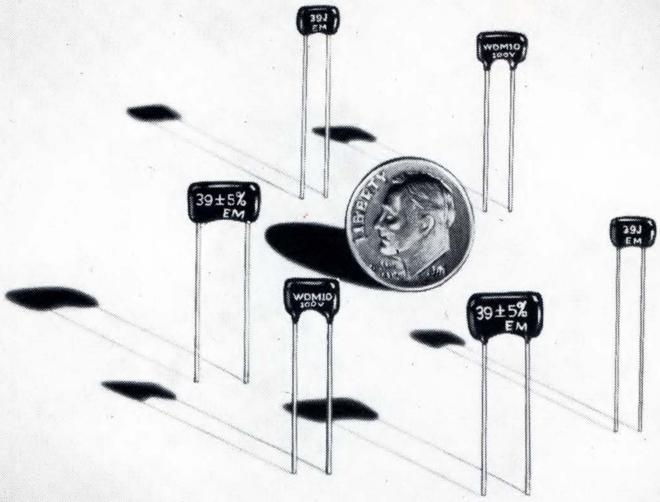

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		D, E	27pF thru 400pF
		F	85pF thru 400pF
DM15		C	1pF thru 1500pF
		D, E	27pF thru 1500pF
		F	85pF thru 1500pF
DM5	300VDC	C	1pF thru 120pF
		D, E	27pF thru 120pF
		F	85pF thru 120pF
DM10		C	1pF thru 300pF
		D, E	27pF thru 300pF
		F	85pF thru 300pF
DM15		C	1pF thru 1200pF
		D, E	27pF thru 1200pF
		F	85pF thru 1200pF
DM10	500VDC	C	1pF thru 250pF
		D, E	27pF thru 250pF
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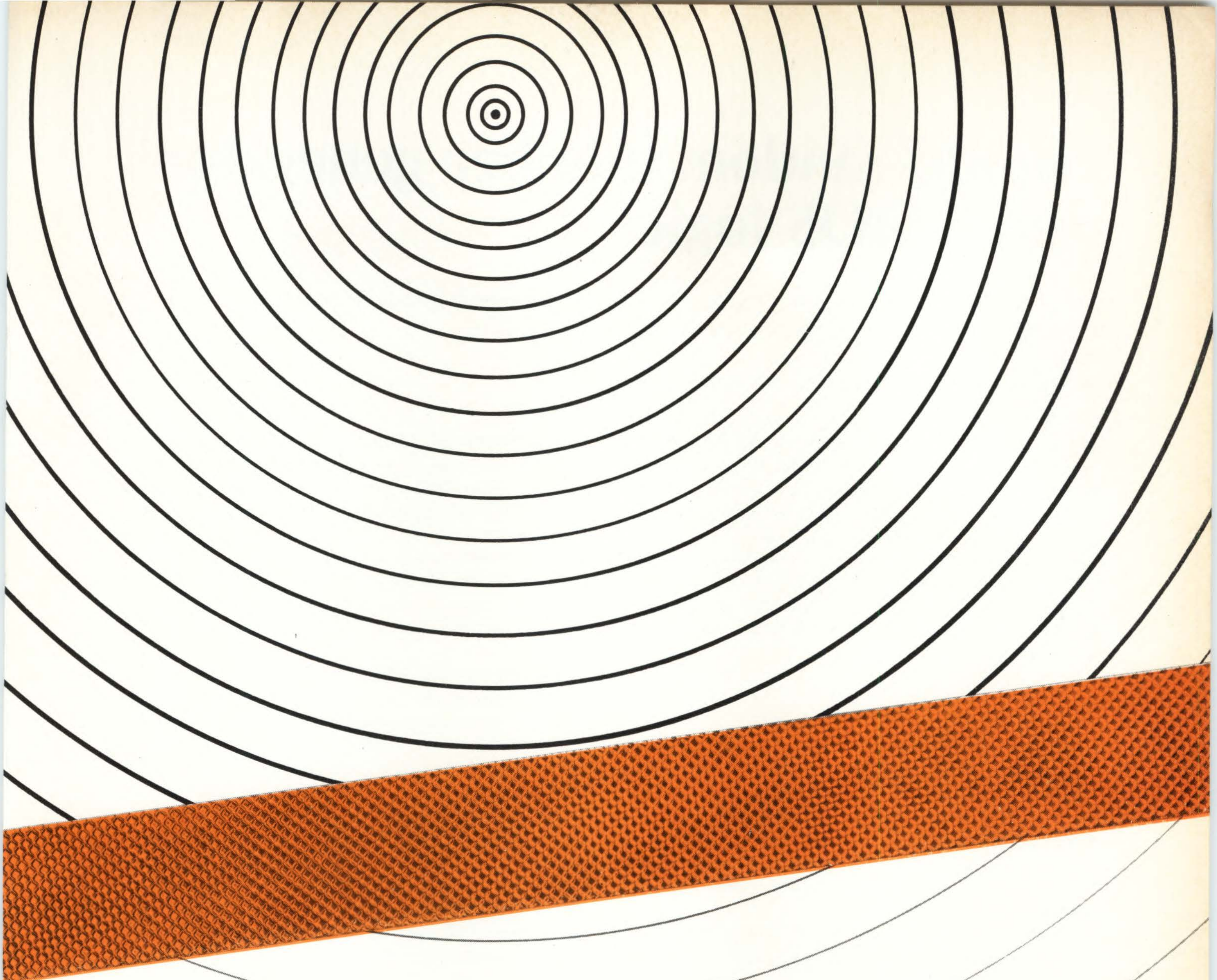

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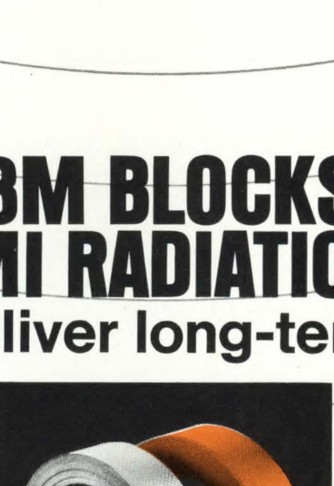

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CHECK NO. 24

Pseudo-random number generator uses CMOS logic

New CMOS MSI packages are making it easier to accomplish special functions like random number generation, with low package counts.

Jim Halligan, Motorola Semiconductor Products Inc.

A pseudo-random digital code generator can be constructed from a shift register and EXCLUSIVE-OR gates. By picking off the outputs of various register stages, performing the Exlusive-OR function, and feeding it back into the register serial input, a digital sequence can be generated which satisfies all of the tests for randomness. The periodicity of the random sequency is $(2^N - 1)$, where N is the number of shift register stages. For example, using an 8-bit shift register, 255 pseudo-random numbers can be continuously generated by Exclusive-ORing the 1st, 6th, 7th and 8th bits:

$$Q_0 = Q_1 \oplus Q_6 \oplus Q_7 \oplus Q_8.$$

The resulting pseudo-random sequence has numerous applications, such as correlation stimuli or test patterns for communications systems. The data scrambling application described here is a particularly useful function which requires only three DIP circuits at each end of a digital communications line to insure message privacy. Most of the devices (or their equivalents) are commercially available from other CMOS supplies.

The eight-bit shift-register MC14021 (device "21" in the multiple-sourced CMOS 4000 family) is used in conjunction with EXCLUSIVE-OR gates MC14507 (also from the 4000 family) to generate the pseudo-random code. The 1st, 6th, 7th and 8th bits are exclusive OR'd and fed back to the shift-register input to develop the code pattern. An all-zeros combination is avoided as it would lock up the circuit.

Only the 6th, 7th and 8th bit outputs are available from the 4021, so it is necessary to simulate the first bit by operating a flip-flop (FF-2) in parallel. This flip-flop is available anyway, because in the CMOS 4000 family the flip-flops come two-to-a-package, and another flip-flop (FF-1) is needed for the system initialization. The simulation is quite literal, because the 4013 package contains the same D-type flip-flops as used in the 4021. The same clock, data and control pulses are applied to FF-2 as are applied to the 4021.

The pattern of 255 bits generated as this logic loop cycles through all its states provides the pseudo-random digital signal. It can be used for a random test signal or carried further as shown and used for protecting messages to be sent out on public channels (or stored in public files). A digital message is scrambled by mixing it with the output of this code generator in an exclusive-OR gate, as shown in **Fig. 1**. The fourth gate in the 14507 package is conveniently available for this. The scrambled data can then be sent out with reasonable certainty that its contents will be unintelligible to others. The 255-bit-long encoding pattern has a sufficient degree of randomness so that it cannot be easily deciphered.

Identical circuit decodes message

A functionally identical 255-bit random-pattern generator is used at the receiving station to unscramble the data

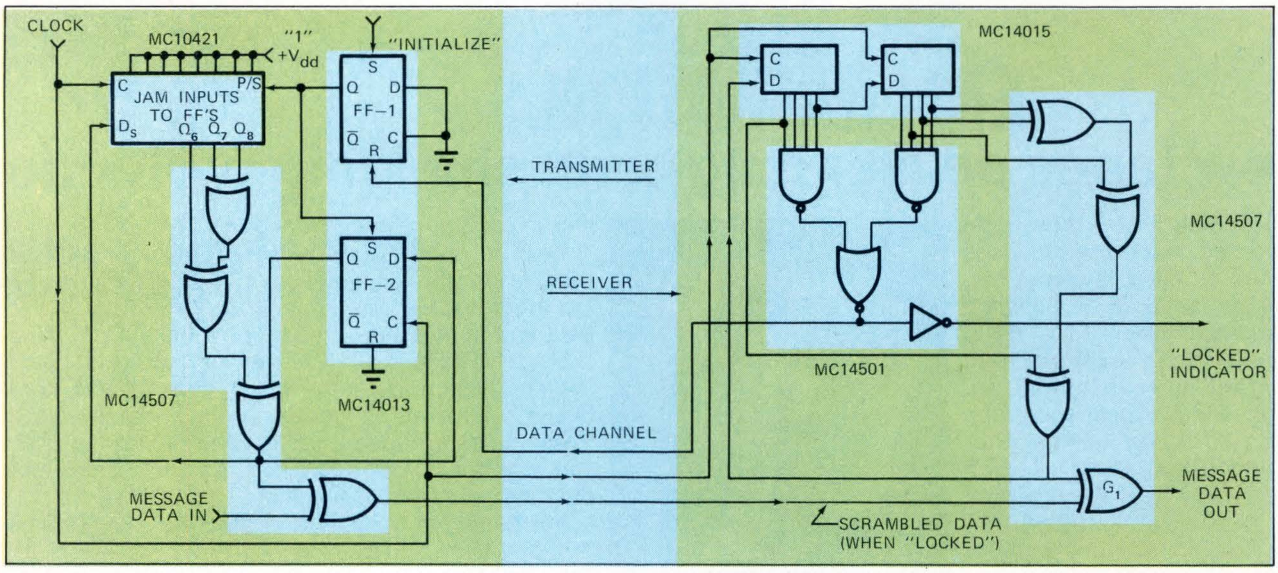


Fig. 1 – Circuits for applying a pseudo-random scrambling code to a message and then removing it. The transmitting station logic (left) is essentially repeated at the receiving station (right). The additional logic is for putting the two shift registers in synchronization at the start of scrambling. Scrambling is accomplished by mixing the digital message with the output of the code generator.

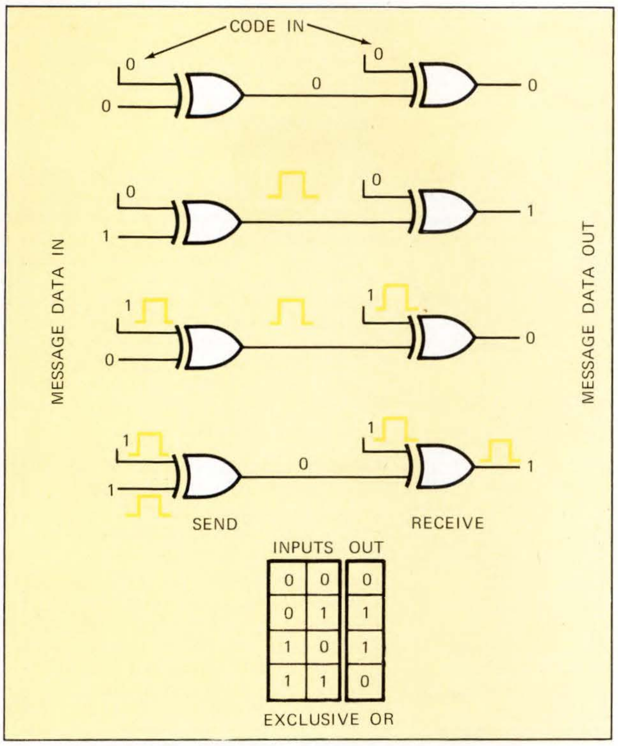


Fig. 2—How the Exclusive-OR at the sending station works with the Exclusive-OR at the receiving station to encode and decode the message. The truth table details how the Exclusive-OR gates add and remove the scrambling code.

message. However, the decoding circuit must have access to the sending clock and a means for synchronizing itself with the coding bit pattern.

The basic duplicate of the random-pattern generator at the receiving station is constructed from two, four-bit registers in the 14015 package that are connected in series. This hardware change is necessary because all the receiving unit shift register outputs must be available for initial synchronization (and the eight parallel jam inputs of the 4021 aren't needed on the receiving end).

Fig. 2, shows the various encoding and decoding signal combinations. If both the data and the scrambling code input to the transmitter exclusive-OR are ZERO, then a ZERO will be transmitted and a ZERO will be decoded. If either the data or the scrambling input at the sending station are ONE, then a ONE will be transmitted. But note that if a "false" ONE has been transmitted by the scrambler, the synchronized decoding ONE at the receiving end will remove it. The "true" ONE from the data will go through. If both the data and scrambling inputs are ONE, then a ZERO will be sent, but a ONE will be reconstructed at the receiving end by the duplicate code.

Synchronizing send and receive

The coding and decoding operations are synchronized by putting both registers into an all-ONE's state. The initialization pulse sets FF-1 which puts the sending register (and FF-2) into the all-ONE's state and then holds the sending register locked in that state until the feedback signal from the receiving registers tells FF-1 that the receiving end has cycled to the all-ONE's state. During this initialization period, data applied at the sending end will be transmitted without scrambling.

The output of FF-1 puts the 4021 into an all-ONE's state

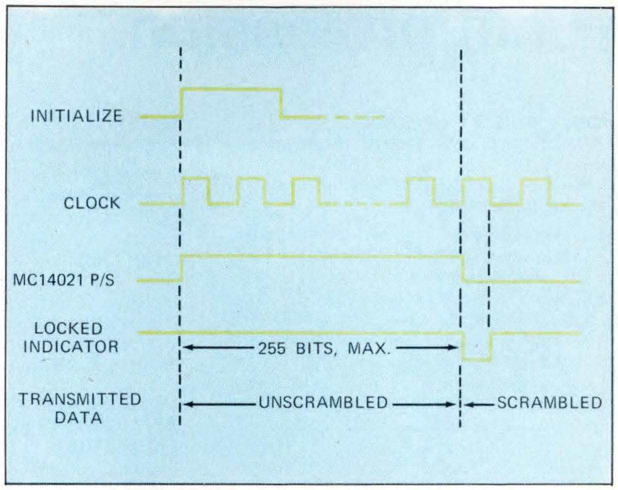


Fig. 3—Timing diagram for the message scrambler shows how the initial synchronization of the transmitting and receiving stations is accomplished.

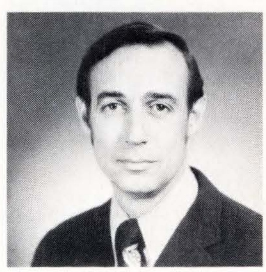
by putting a ONE level into the 4021's parallel/serial control. This causes the 4021 to internally gate all its eight flip-flops to the jam inputs which have been tied to the ONE level. At the same time, FF-2 is also put into the ONE level by a ONE input to its SET control. (see **Fig. 3**.)

The receiving-end register (4015) continues to respond to clock pulses and goes through all its states. Within 255 clock pulses it will have arrived at its all-ONE's state, at which time this condition will be detected by the gates in the 14501 package and they will feed back the signal to the sending unit that will release FF-1 and let the scrambling commence. This signal pulse also tells the receiving end that scrambling has begun. Now, of course, both registers are synchronized because they started from their all-ONE's condition.

This initialization period will never be longer than 255 clock pulses, and it might profitably be used for a preamble of some harmless "housekeeping" information, such as the day's date.

It will be noted that three transmission lines are shown between the sending and receiving unit: one for the clock, one for the message and one for the initialization feedback signal. These signals could be multiplexed so they could be sent on a single telephone line. ▭

Author's biography



Jim Halligan is manager of industrial applications at Motorola's Semiconductor Products Div., Phoenix, Ariz., where he has been employed for one year. Jim previously worked at Philco-Ford and Harris Semiconductor and has a broad background in semiconductor applications, integrated circuit design and automotive electronics. He received his BSEE and MSEE from Drexel University, and is presently attending Arizona State University.

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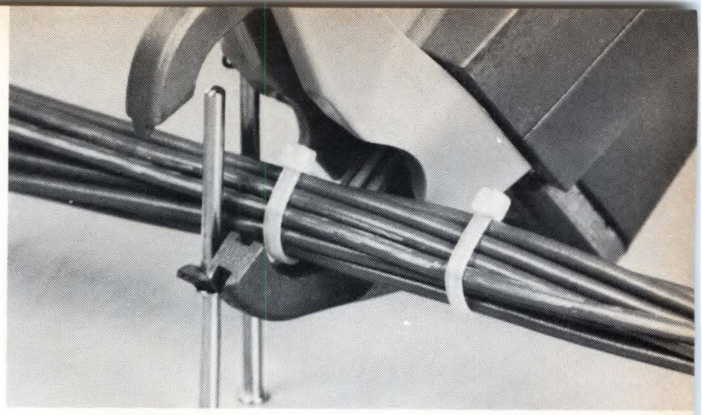

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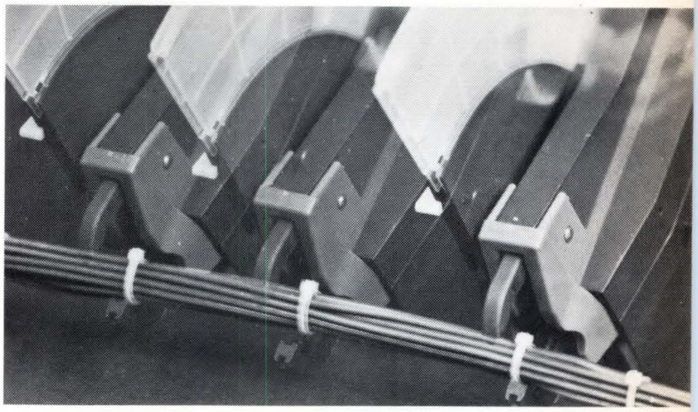

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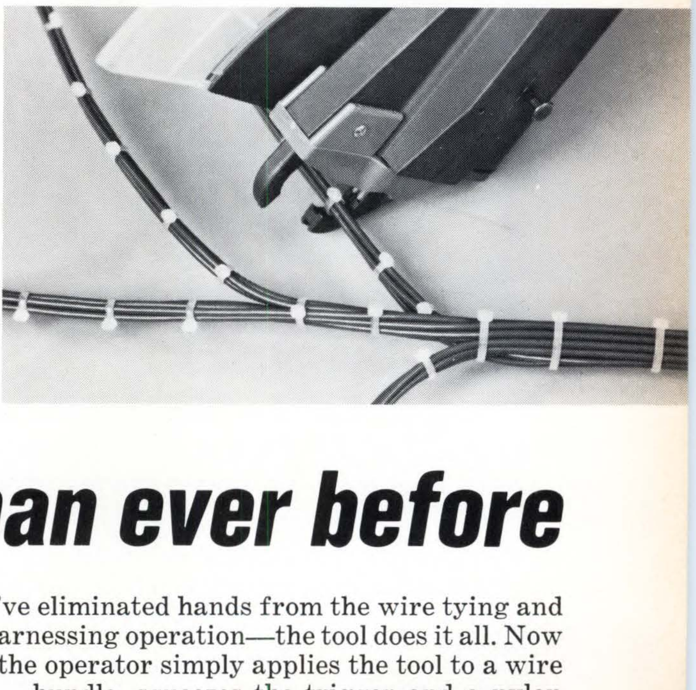

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CHECK NO. 51

Sine-wave synthesizer has low harmonic distortion

Lee J. Mandell
Litton Industries, Van Nuys, Calif.

This circuit is used to synthesize a sinewave with harmonic distortion of less than −50 db. It is basically a transversal-digital filter, whose coefficients are chosen to perform this task. The theory and electrical operation of the circuit are described below.

Theory of operation

A square wave consists of sine waves at the prime frequency and at all odd harmonics and thus is not suitable for data transmission. It is desirable to reduce the amplitude of each harmonic to well below −40 db so as to obtain a single sine wave of the prime frequency with harmonic distortion of less than −40 db. To do this, the square wave is passed through a filter whose resonant frequency is at the prime frequency. This will greatly reduce all harmonics. It is shown that a filter whose impulse response is that of a constant sinusoid will be a resonant filter. This filter can be approximated by using resistors to weight data as it passes through a 16-bit shift register, where the weighting corresponds to the amplitude of a sinusoid at each sampling interval.

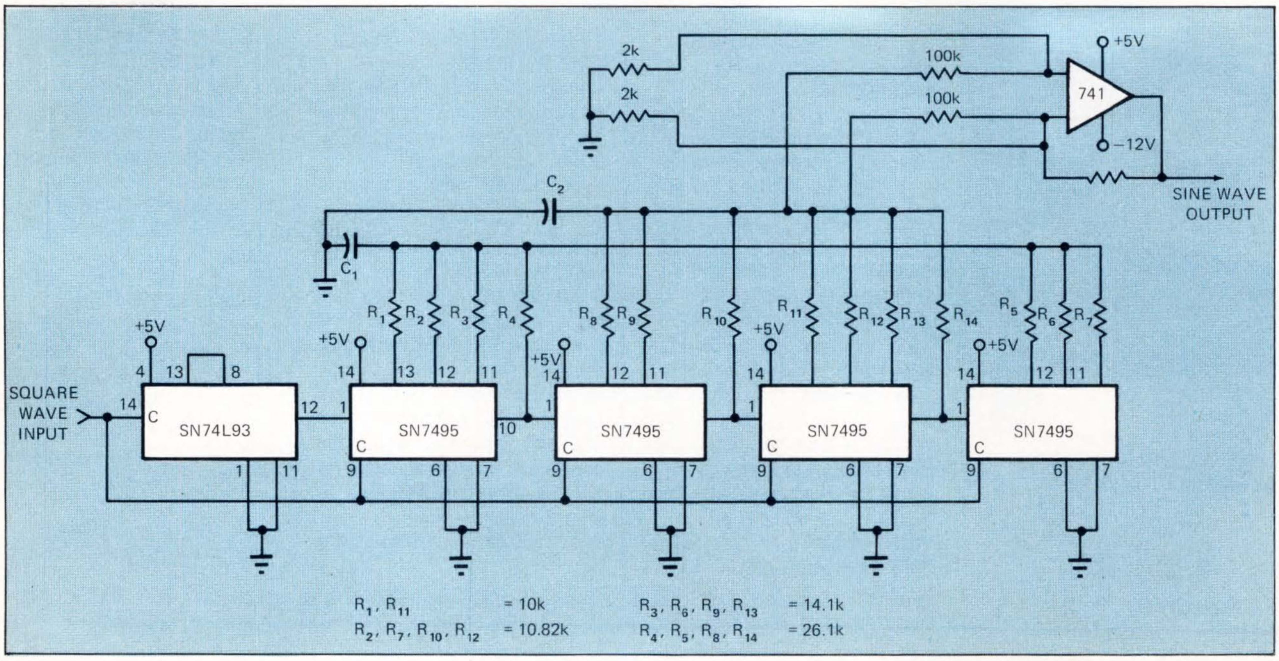
$$W_n = \text{Cos}\frac{2\pi(n-1)}{16} \quad n = 1, 16$$

This results in a sine wave sampled at 16 times its frequency. Thus, it has theoretically no harmonics below the sampling frequency or 16th harmonic. A simple RC filter may now be used to filter out the remaining harmonics.

Electrical operation

A clock whose repetition rate is 16 times the desired frequency is the input to this circuit (any duty cycle will work equally as well). A 4-bit ripple counter (SN 74L93) divides this down to provide a square wave of the desired frequency. This square wave is then sampled 16 times per cycle and shifted down the 16-bit shift register (SN 7495). The value is weighted at each point of the shift register by a resistor whose value is 1/W. (Note that when W = O, the resistor will not be present). The resistors are grouped depending upon whether W is negative or positive and then a 741 is used to obtain the difference which is the sampled sine wave. The feedback resistor may be varied for a 40-db range of output amplitudes. A capacitor (C_1,C_2) value is chosen to eliminate the higher harmonics. The resulting sine wave will have harmonic distortion of less than −50 db. □

To Vote For This Circuit
Circle 150

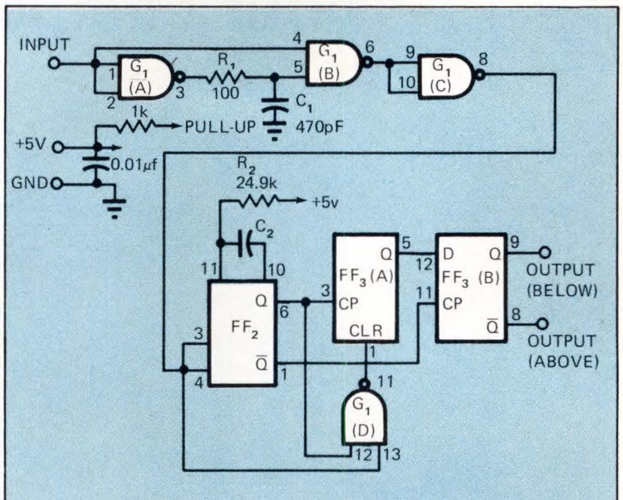


Sine-wave synthesizer is essentially a transversal digital filter with components selected to suppress harmonics present on the input square wave to less than −40 db, obtaining a prime frequency sine wave.

Three IC's accurately sense pulse rate

John W. Poore
General Dynamics Pomona, Calif.

Many applications arise for accurate pulse rate detection where extreme accuracy, such as that of a frequency counter, is not required. The circuit shown indicates when the input pulse rate is above (or below) a set point. The output is high for frequencies above the set point, and low for frequencies below the set point. Set point stability was measured over a 0°F to 200°F range using a mylar capacitor for C_2, and a set point of 10 kHz. The maximum shift in set point frequency over temperature was less than 0.7%. Set point frequency is the reciprocal of the one-shot delay time, i.e. $f_o = 1/(0.32R_2C_2)$. R_1, C_1, G_1(A) and G_1(B) generate a spike at the rising edge of the input signal. The one-shot (FF_2) delay time is affected by pulse width at its input terminal; adding the spike generator makes the circuit virtually insensitive to the input signal on-time or off-time. The rising edge of the input signal causes a spike at FF_2's and G_1(D)'s input. The leading edge of the pulse from the one-shot sets FF_3(A). If another rising edge of the input signal (and thus another spike) occurs during the one-shot delay time, G_1(D) gates a reset pulse to FF_3(A). The trailing edge of the pulse from the one-shot clocks FF_3(B) thus sampling FF_3(A)'s output. This provides a stable output. Two of these circuits can be used to bracket pulse rates. ▭



REF	TYPE	+5V	PULL-UP	GND
G_1	SN7400N	14		7
FF_2	SN54121N	14	5	7
FF_3	SN7474N	14	2, 4, 10, 13	7

Pulse rate of the input signal is accurately sensed using only 3 ICs. Two such circuits, one set to the upper limit and one to the lower can be used for constant frequency monitoring.

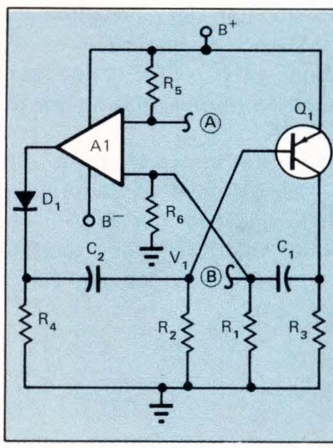
To Vote For This Circuit
Circle 151

Op amp oscillator is voltage or resistance controlled

Kenneth D. Ceola
Honeywell, Hopkins, Minn.

This circuit serves as both a resistance and/or voltage control oscillator. Voltage controlled oscillation is accomplished by commutating voltages at point A, which establishes a threshold on the operational amplifier. Resistance-controlled oscillation is accomplished by commutating resistances at point B. The equations show how the period is dependent on the op amp threshold and/or the resistance at point B to ground.

The circuit is useful in systems where transducers with voltage and resistance outputs are used to monitor desired parameters. The output of the oscillator can be used to modulate a transmitter, rather than having separate resisance and voltage controlled modulators. ▭



Q_1 OFF TIME

$$\cong R_2C_2 \ln \frac{2B^+ - V_{D1}}{B^+ - V_{eb}Q_1}$$

Q_1 ON TIME

$$\cong R_1C_1 \ln \left[(B^+ - V_{EC}SAT\,Q_1)\left(\frac{R_5 + R_6}{B^+R_6}\right)\right]$$

V_{D1} = Diode D_1 voltage drop
V_{eb} = Emitter base drop of Q_1
V_{EC} SAT = Saturated drop of Q_1 emitter to collector

$$\text{OP AMP THRESHOLD} \cong \frac{(B^+)(R_6)}{R_5 + R_6}$$

Voltage/Resistance-controlled oscillator can be frequency controlled by voltage level at input A or resistance value seen at point B or both. Active components A_1 and Q_1 are not identified specifically because they must be selected according to frequency/power requirements of your design.

To Vote For This Circuit
Circle 152

Your vote determines this issue's winner. All circuits published win a $25 U.S. Savings Bond. All issue winners receive an additional $50 U.S. Savings Bond and become eligible for the annual $1000 U.S. Savings Bond Grand Prize.

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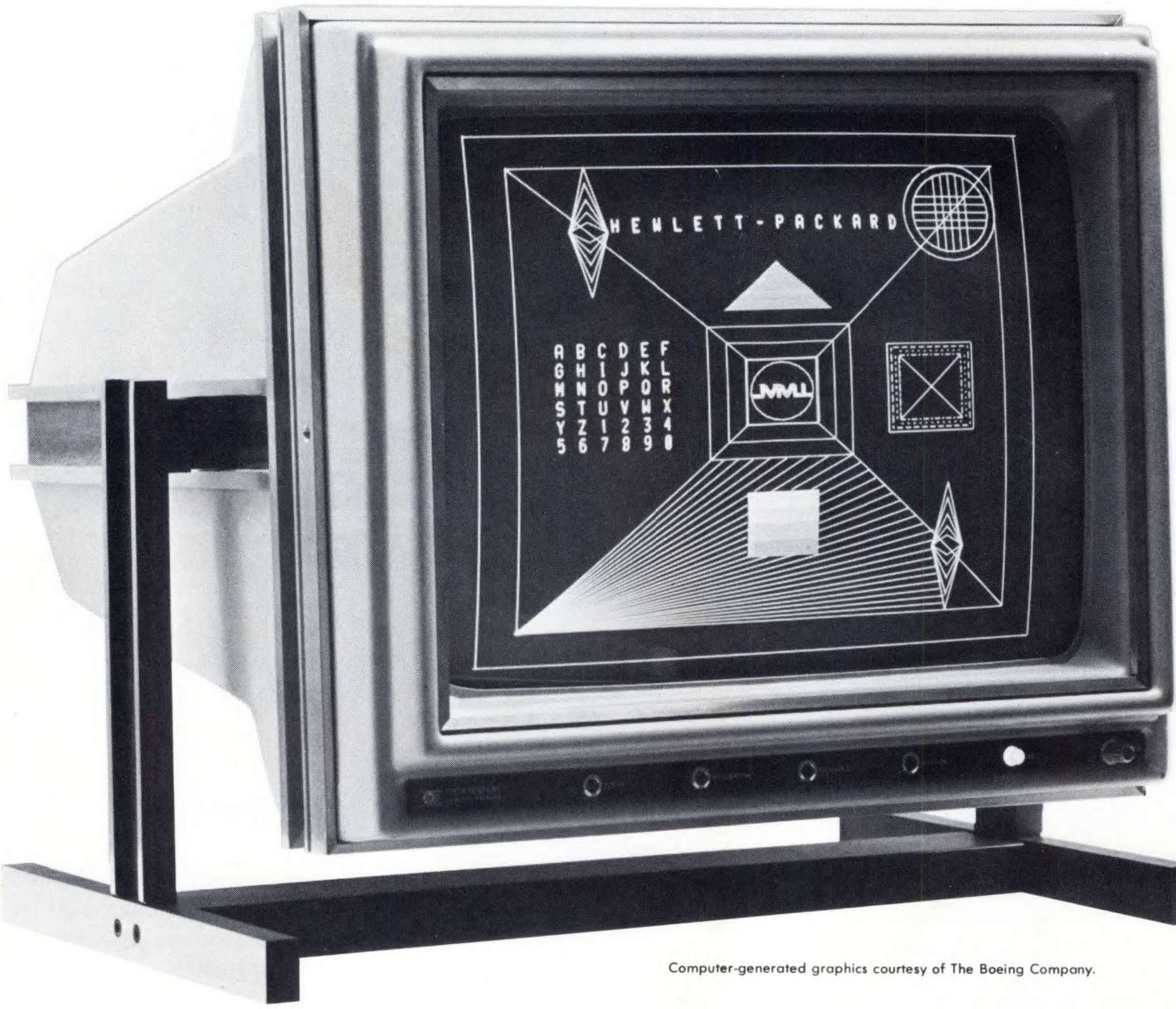
Readers have voted: Helge Mortensen winner of the May 15 Savings Bond Award. His winning circuit is "IC op amps make inexpensive instrumentation amplifiers". Mr. Mortensen is with National Semiconductor Corp., Santa Clara, Calif.

This display writes as fast as your computer can talk.



Computer-generated graphics courtesy of The Boeing Company.

HP's new 1310A 19-inch-diagonal X-Y display is the answer to many an OEM's prayer... because it's the **first display ever that can keep up with the graphic information output of today's high-speed computers.**

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Also as a result of using electrostatic deflection, the 1310A is smaller, lighter, and **requires less power** than any competitive graphic display – only 100 watts. Because it uses the latest, highly rectangular CRT face glass, its display area is equal to that of many 21-inch units. And its **0.020-inch spot size** gives you a crisp, clear image over that entire area.

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Yet, despite all these advantages, the **1310A costs only $3000**—far less than competitive displays (covers and stand, $100 extra). Or, for $2875, you can get all the features of the 1310A, in the new 14-inch-diagonal 1311A. **OEM price schedules are available on both the 1310A and 1311A.**

For further information on both of these new displays, contact your local HP field engineer. Or write Hewlett-Packard, Palo Alto, California, 94304. In Europe: 1217 Meyrin-Geneva, Switzerland.

081/14A

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OSCILLOSCOPE SYSTEMS

The ABC's of A/D and D/A converter specifications

Physical component limitations such as noise and interference can play an important role in a system's design. A thorough understanding is essential for good performance.

Bernard M. Gordon, Analogic Corp.

Most analog-to-digital and digital-to-analog subsystems are generally represented by the block diagrams of **Fig. 1**. As shown, such conversion systems may accept a wide variety of analog input signals and yield various digital outputs for storage transmission or computation. Similarly, stored or transmitted digital or computed data may in turn be utilized to provide a multiplicity of analog display and control signals for subsequent usage.

With the rapid rise of analog-to-digital and digital-to-analog conversion techniques, the tendency by many system designers has been to merely consider subsystems as building blocks. This approach has tended to frustrate them in properly using available building blocks because of a number of factors not necessarily implicit in block-diagram representations.

To have a successful application or installation, the system designer must not only take into consideration the levels of analog signals and types of binary codes desired, but also the "real-life" physical limitations of components, such as noise and interference, which are inherent in all practical situations. Sound-engineering thought and effort directed toward an understanding of some of these limitations, both theoretical and practical, will assist the system designer in anticipating and overcoming problems that can result in poor system performance.

The first thing a designer should have is a thorough understanding of the converter terminology employed by the manufacturer in defining the various specifications. For example, he should understand the difference between absolute and relative accuracies and the difference in errors due to offset drift and scale-factor drift. He should understand the effect of quantization error, monotonicity, and linearity.

Once having understood the terminology employed in analog-to-digital and digital-to-analog converters, multiplexers and sample-and-hold amplifiers, he should make sure that the vendor from whom he is obtaining his equipment has, in fact, specified all of the various parameters required to define proper operation. For example, a sample-and-hold unit without an adequate feedthrough-rejection specification may yield entirely different results with dynamic signals than with static signals.

The user should understand clearly the transfer weighting action of different binary codes. Many users have not taken the time to really understand the difference, however small, between offset binary, one's complement and two's complement codes. Further, many users whose backgrounds have been primarily in digital installations, have not understood the differences between the maximum available resolution allowed by utilizing a given number of bits and the actual accuracy and resolution which may be obtained as limited by other sources of analog error.

The system designer must pay particular attention to analog sources of error. These may be due either to noise generated within the modules he is integrating or due to interference caused by extraneous normal-mode pickup or common-mode signals. It is very important that the user fully understand the sources of and cures for common-mode signal interferences. Many system designers have had a tendency to take common-mode specifications at face value without fully understanding that common-mode rejection is only achieved through an optimum combination of equipment capability matched to anticipated signal-source characteristics. The need for filters must be carefully considered as well as the optimum type of filter for any particular type of anticipated noise or signal interference.

A very common problem encountered in interfacing various analog-to-digital converters, multiplexers, sample-and-hold amplifiers and digital-to-analog modules is simply the resistance of interconnections. The resistance of even short runs of normal-size copper wire and particularly printed-circuit runs is much higher than expected and if

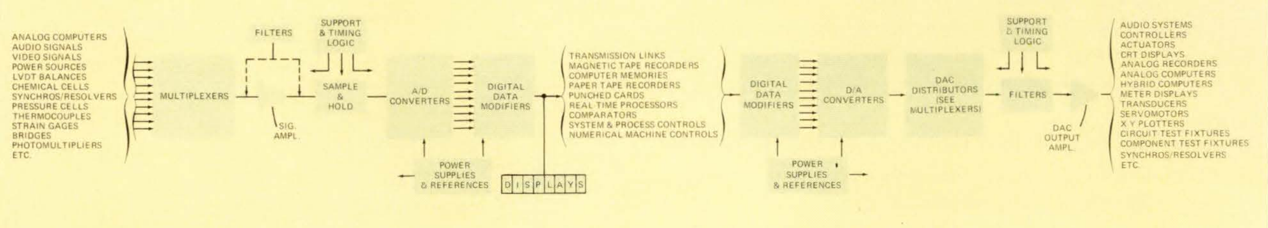

Fig. 1 – All A/D and D/A systems contain some or all of these components.

such wiring is not done carefully and properly, voltage drops and common ground returns can be the biggest sources of error.

Having become familiar with the terminology, types of codes, having studied the resolution and accuracy required, and having given serious consideration to interfacing common-mode and other noise generating factors as well as having considered his interconnection scheme, the system designer is now in a position to thoroughly assess his problem and pick those components best suited technically and economically for the task.

There are a wide variety of applications for analog-to-digital and digital-to-analog converters. Some may best be satisfied with lower-accuracy and lower-speed units while others require the highest accuracy, highest stability and highest speed. The system designer must be aware that all converters which, on the surface have certain similar major specifications, are not identical. He must also realize that it is only through his understanding of the intrinsic capability of the various converters together with their specifications and his understanding of the static and dynamic usage problems, that he may optimize his trade-offs.

Dynamic parameters of amplifiers

Settling time: the maximum time interval between the application of a step function (of specified magnitude—usually end-to-end of the full-scale range) to the input, and the "permanent" entry of the output voltage into a stated voltage band surrounding the theoretical output corresponding to that input. (The term "permanent" is used because the transient behavior of many devices is underdamped; i.e., as shown in **Fig. 2**, the output may pass through the stated settling band one or more times in an oscillatory fashion before remaining within it.)

Maximum slew rate: the fastest rate at which the output of the device can change from one end to the other of its rated range, under stated load conditions. Clearly, this rate is achieved in response to a large step input, as shown in **Fig. 2**.

Maximum small-signal bandwidth: the highest frequency at which an amplifier will track (to within a stated tolerance—usually, to within 3 dB of the low-frequency response) a sinusoidal signal having an amplitude below that value at which the slew-rate limitation is significant.

Full-power bandwidth: the highest frequency at which an amplifier, loaded to maximum rated power output, will track a sinusoidal signal large enough to drive the output to its rated full-scale value at peak input. The nominal relationship between full-power bandwidth and slew rate is:

slew rate $= 2\pi f e_{fs}$ (the maximum slope of a sine wave of e_{fs} peak amplitude),

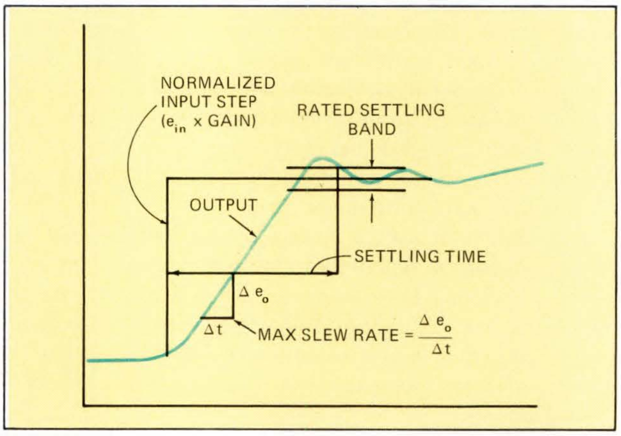

Fig. 2

where f = full-power bandwidth,

and e_{fs} = rated full-scale output.

Note: If the step response of the circuit is nonlinear, f may be somewhat higher than calculated value.

Overload recover time: the time required for the circuit to return to linear operation, within a stated tolerance, after removal of a sustained input that was large enough to drive the circuit into complete saturation—i.e., a condition in which further increase in input did not significantly increase output.

Multiplexer parameters

Transfer accuracy: the agreement between output and input voltage, usually stated as:

$$\text{accuracy} = \frac{e_{in} - e_o}{e_{in}} \times 100\%.$$

This should be given as worst case over the entire rated input voltage range, for a specific signal-source impedance.

Settling time: See Dynamic Parameters of Amplifiers. Better stated as "Switching plus settling time."

Input (leakage) current (OFF mode): the highest current that can flow, at any rated input voltage, into or out of OFF input terminal. The total leakage current of all OFF channels flows through the source impedance, causing an offset error.

Throughput rate: highest rate at which the multiplexer will switch from channel to channel at specified accuracy. The inverse of "Switching plus settling time."

Capacitance/channel, C_c (OFF mode): the capacitive loading (from the common output line to ground) contributed by each OFF channel. In a n-channel multiplexer,

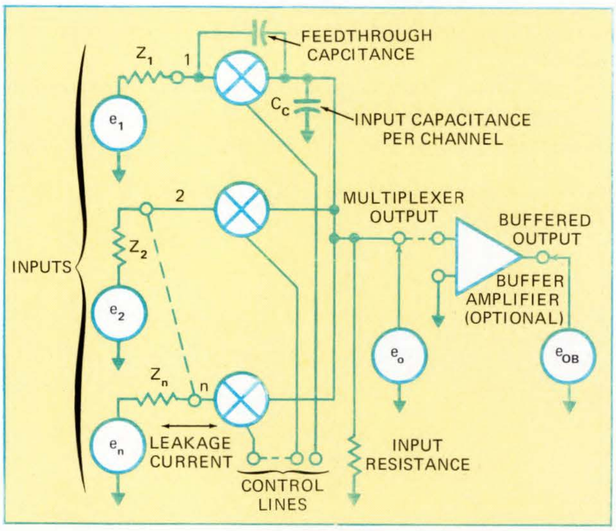

Fig. 3

then, the capacitance (from this source) "seen" by the ON channel signal source is $C = (n - 1)C_c$.

This total capacitance may be a major factor in limiting settling time.

Common-mode rejection: In differential-input multiplexer configurations (2 wires/channel), this is the same as that defined under Common-Mode Rejection.

Crosstalk attenuation: A specific test voltage, at a stated frequency, is applied to all OFF-channel inputs connected in parallel. This ratio (in dB) of the test voltage to the output voltage it induces is:

$$\text{Crosstalk attenuation} = 20 \log_{10} \left[\frac{e_{test}}{e_0}\right].$$

Feedthrough capacitance/channel (OFF mode): The capacitance that couples the input terminal of an OFF channel to the output.

Injected (kickbacks) switching transients: signal components introduced into the source by stray coupling between the switching circuits on the ON channel. In low-level circuits these transients can be very significant. If this transient is signal-level-sensitive, it becomes "Self-modulation," defined under Sample/Hold Parameters.

Sample/hold parameters

Acquisition time: the interval between SAMPLE command and the moment when the output begins to track the input (to within stated accuracy), regardless of the previous state of the output.

Turn-off time: minimum interval between HOLD command and beginning of HOLD mode.

Aperture uncertainty: uncertainty in turn-off time—i.e., uncertainty in transition between SAMPLE and HOLD modes. (Difference between maximum and minimum turn-off times.)

Settling time: maximum time required for the output to track the input within the stated gain accuracy, for a specified step change in input, during sampling or tracking. Usually, step is specified as full-range change.

Decay rate: maximum rate of change of the output voltage to the HOLD mode.

Slew rate: maximum attainable large-signal rate of change of output voltage, in either acquisition or tracking.

Input impedance: resistive and reactive components of load presented to input signal. Two sets of values are given, one for SAMPLE mode and one for HOLD mode. (Alternatively, I_{in} may be specified for SAMPLE mode.)

Gain accuracy: degree to which voltage gain is maintained at nominal value. (Should include effects of gain T.C. and effects of power-supply changes on gain, as well as changes in gain over stated period of time, if significant.)

Voltage gain: nominal ratio of output voltage to input voltage at the instant that the SAMPLE-TO-HOLD transition occurs.

Output offset voltage: maximum value of output when sampling zero input, at a stated temperature (usually 23°C).

Offset drift: worst-case variation in output-offset voltage

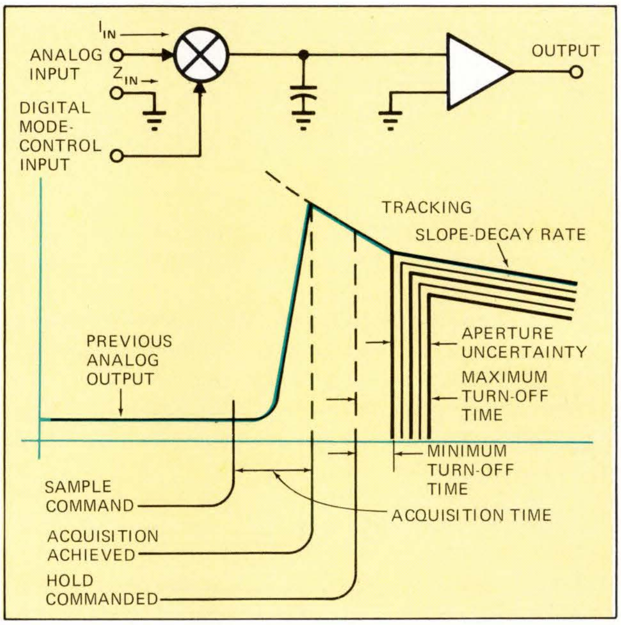

Fig. 4

due to changes in ambient temperature (offset T.C.), power-supply voltage (p.s. rejection), and over stated period of time. Usually, the three drift effects are stated separately.

Feedthrough rejection: ratio (expressed in dB) of a specified input signal to the resultant output signal, during HOLD mode over a stated frequency range.

Self-modulation: maximum variation in output caused by interaction between the signal amplitude and the circuits that accomplish the sample-to-hold mode switching.

Common-mode rejection

Common-mode-rejection ratio (CMRR): the ratio of the CMV to the contribution to the output due to CMV alone—i.e., $CMV/\Delta e_{out}$, where Δe_{out} is referred to the input. This parameter is usually expressed in dB,

$$CMRR = 20 \log_{10} \left[\frac{CMV}{\Delta e_{out}}\right]$$

for the device alone, then:

$$CMRR = 20 \log_{10} \left[\frac{1}{A_1 - A_2}\right].$$

Because A_1 and A_2 are inherently frequency dependent and may be amplitude dependent, the CMRR behavior of a device (such as the amplifier shown in the diagram) is a function of the frequency and sometimes the magnitude of CMV. The effective CMRR of the complete circuit is dependent on both the external and internal impedance balances.

Almost always, the impedances Z_{01} and Z_{02} are high enough (with respect to Z_1 and Z_2 and the reactances of C_1 and C_2) to be ignored. Z_{12} is also usually high enough to prevent significant source loading. Under these conditions,

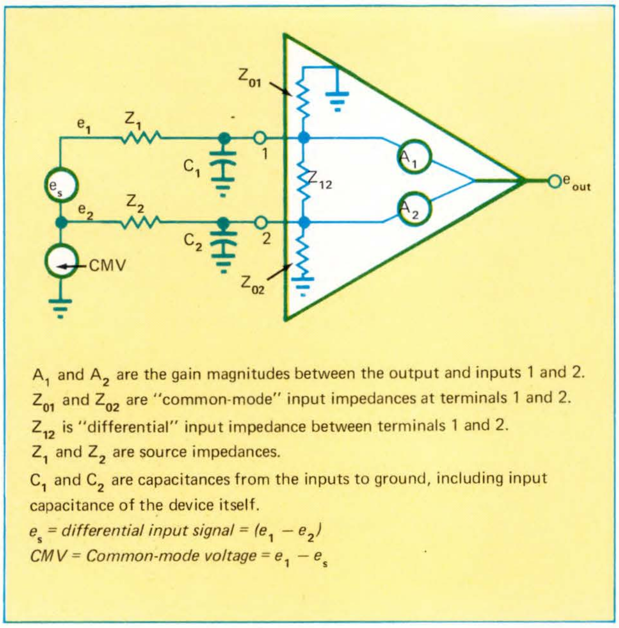

Fig. 5

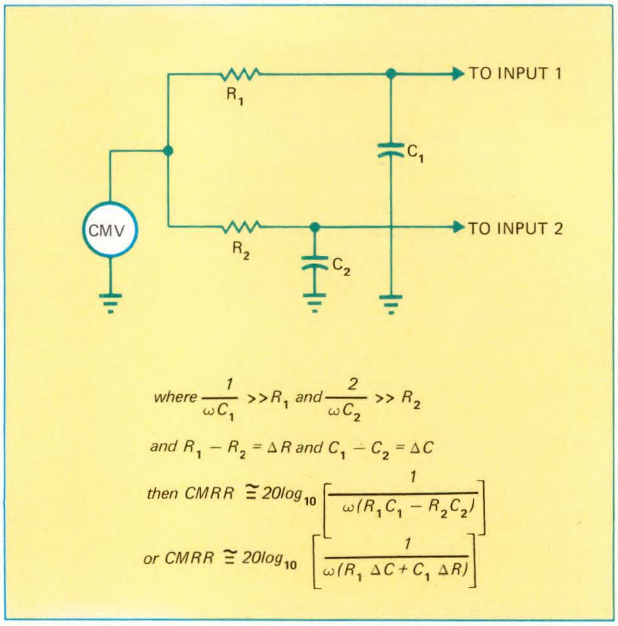

Fig. 6

the external circuit unbalances (including the input capacitances of the device) can cause a significant reduction in the overall CMRR.

To calculate effective external CMRR: CMRR approaches a maximum (for a given C_1 and C_2) when, for a given ΔR, $\Delta R \gg R_1$. When $R_2 = 0$, $R_1 = \Delta R$, and the CMRR is the highest value attainable. Similarly, for a given R_1 and R_2, the CMRR is the highest value attainable when $C_2 = 0$, so that $C_1 = \Delta C$. Under these conditions,

$$CMRR_{(max)} = 20 \log_{10}\left[\frac{1}{2\omega\Delta R\Delta C}\right]$$

and the highest-attainable values are as shown in the chart (**Table 1**). For comparison of these "ideal" figures with the more general case, consider a circuit in which $R_1 = 10^4\Omega$, $C_1 = 100$ pF, $\Delta R = 1000\Omega$ and $\Delta C = 10$ pF. Then at 60 Hz

TABLE 1

Highest attainable CMRR values (at 60Hz)				
ΔR	ΔC = 1pF	ΔC = 10pF	ΔC = 100pF	ΔC = 1000pF
10Ω	162dB	142dB	122dB	102dB
100Ω	142dB	122dB	102dB	82dB
200Ω	136dB	116dB	96dB	76dB
500Ω	129dB	109dB	89dB	69dB
1000Ω	122dB	102dB	82dB	62dB
10,000Ω	102dB	82dB	72dB	42dB

$$CMRR = 20 \log_{10}\left[\frac{1}{\omega(R_1\Delta C + C_1\Delta R)}\right]$$

= 90.4 dB or 11.6 dB lower than the highest-attainable value from the chart.

Normal-mode rejection

(Applies to any analog circuit)

Normal-mode rejection ratio (NMRR) is the ratio of the transfer function (of a circuit or device) for the signal component of interest to the transfer function for unwanted signal components (e.g., noise, line-frequency pickup, etc..) as a function of the frequency of the unwanted components. It is usually expressed in dB:

$$NMRR = 20 \log_{10} \frac{K(f_0)}{K(f)}$$

where $K(f_0)$ is the transfer function $\frac{e_{(out)}}{e_{(in)}}$

at the frequency of the signal of interest. (Note: In an A/D converter, f_0 is usually either zero (dc) or a frequency consistent with the highest rate of change of the analog input that the converter must track.) K(f) is the transfer function for the frequency (above f_0) at which NMRR is calculated.

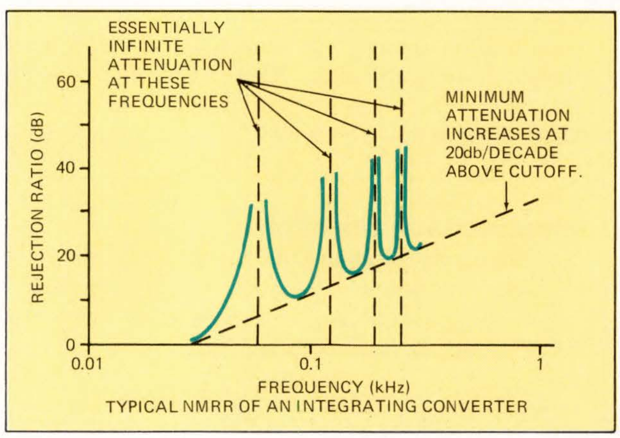

Fig. 7

Any frequency-selective filter will achieve some normal-mode rejection, provided that it exhibits more attenuation above f_0 that it does at f_0. (See Filters discussion.)

An integrating A/D converter provides effective normal-mode rejection for all frequencies above f_0, and essentially infinite NMR at frequencies that are integrally related to the integration period as shown in **Fig. 7**.

For any frequency component having a period that is an integral submultiple of the integration period, the NMRR is essentially infinite. The lowest such frequency, f_1, is:

$$f_1 = (1/T_{int})\ \text{Hz},$$

where T_{int} is the integration period in seconds.

Usually, the integration period is synchronized to the power-line frequency for best rejection of ac pickup. Note that the integrator (which is, after all, a one-pole filter) provides significant attenuation at all frequencies above its low-pass cutoff frequency. This attenuation increases at 20 dB/decade above the cutoff frequency.

Noise calculations

All circuits and devices, active and/or passive, exhibit noise. In a resistor, the Johnson (or thermal) noise is given by:

$$e_n = \sqrt{4KTR\ (\Delta f)}$$

where e_n is the RMS value of the noise energy generated over the bandwidth Δf

R = resistance in ohms,

K = Boltzman's constant, 1.38×10^{-23} Joules/degrees Kelvin

T = Temperature in degrees Kelvin (°C + 273).

The curve (**Fig. 9**) plots the value of e_n against Δf, at 23°C, for various values of R.

Noise sources in series are added by taking the square root of the sum of the squares of the individual noise voltages. Noise sources in parallel are added by converting them into parallel equivalent resistances, and computing the noise generated by the equivalent parallel resistor.

Noise at the analog input and within an A/D converter will cause output-code errors if the peak value of the noise, after filtering and/or integration by the converter (and when added to other uncertainties in the converter error budget), exceeds one least-significant bit. The percentage of time during which a given noise level will exceed the 1-bit threshold may be calculated from a Gaussian-distribution curve (**Fig. 10**) and probability table (**Table 2**).

Table 2 shows that if the 1-bit threshold is greater than the $\pm 3\sigma$ noise level (p-p threshold = 6 × RMS noise level), a 1-bit or greater code error of either polarity will occur less often than 0.3% of the time; or, a unipolar error (for example, n + 1 or more bits instead of n bits of output) will occur less than 0.15% of the time assuming there are no other sources of error.

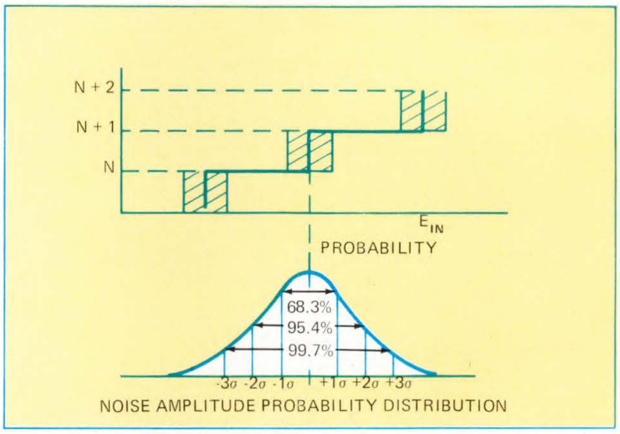

Fig. 9

TABLE 2

Percent of Time RMS Noise Level is Exceeded in Either Direction	Percent of Time RMS Noise Level is Exceeded in One Direction	Peak-to-Peak Noise Level
31.8%	15.9%	±1σ(2 x RMS)
20%	10%	±1.64σ(3.3 x RMS)
4.6%	2.3%	±2σ(4 x RMS)
0.3%	0.15%	±3σ(6 x RMS)
0.02%	0.01%	±3.89σ(7.8 x RMS)

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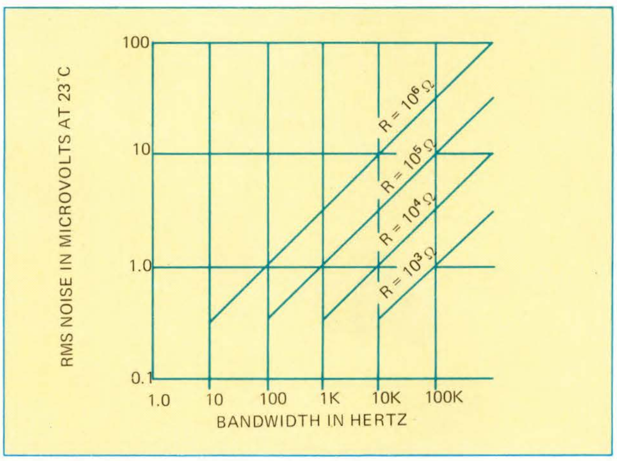

Fig. 8

Author's biography

Bernard M. Gordon is Chairman of the Board and Chief Executive Officer of Analogic Corp. He is also a general partner and technical director of the Gordon Engineering Co., the parent company of Analogic Corp. He is internationally known for his contributions and leadership in the fields of high-speed data handling, computations, digital communications, automatic control and PCM telemetry. His experience with information systems may be traced back from the earliest days of the development of high-speed electronic computers. A holder of an extensive number of patents, Mr. Gordon also holds BSEE and MSEE degrees from MIT.

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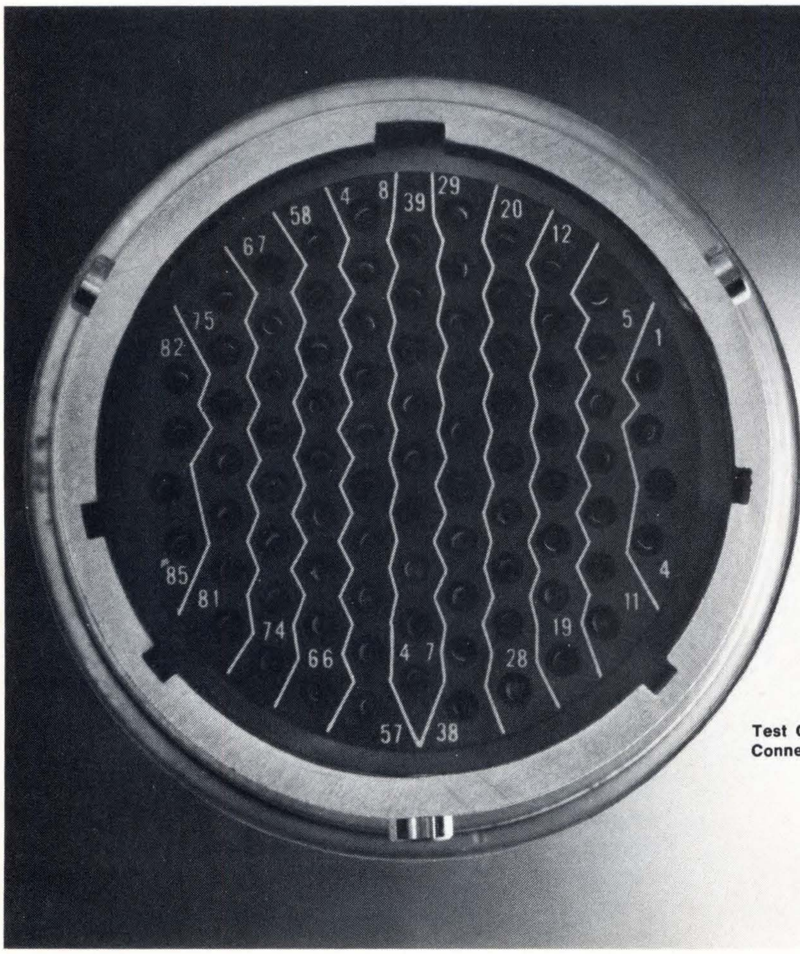

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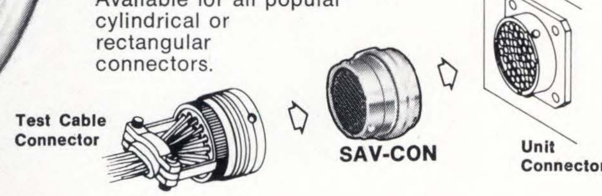

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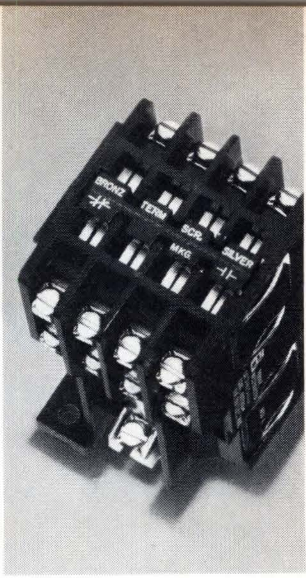

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Get more from your minicomputer with minimum-cost stack memories

Software implementation of memory stacks often slows the memory, while a hardware approach is costly. Here is a way to make existing memory look like a stack.

George Reyling, Jr., National Semiconductor Corp.

Modern programming techniques are making greater use of last-in first-out push-pull stacks. These are very useful for simplifying nested interrupts, and nested and recursive subroutines, as well as compilers and other types of programs.

Many systems implement the stacks with software; however, this limits their usefulness in many situations, since execution time is very slow. Software stacks have some advantages in that the stack size can be quickly modified as memory and stack-allocation requirements change, and several stacks for different purposes are relatively easy to implement once the software for one stack has been provided.

The speed limitation of software stacks may be unacceptable in interrupt service routines, or in systems which require high-speed program execution. In this situation, a high-speed hardware stack may be used. This also has a number of disadvantages. The cost is very high because stacks are not presently available as standard integrated circuits, and thus must be built up from basic components. Size is fixed by the hardware; therefore, a stack must be provided to accommodate the maximum number of words available, even though the maximum capacity may rarely be used.

This article will describe a stack implementation that should provide the advantages of both hardware and software stacks, without the limitations of either.

Make existing memory look like a stack

The principal feature of this implementation is that, rather than providing the hardware to make a complete stack, hardware is provided to make the existing memory *look* like a stack. Since the main memory of a computer usually costs less per bit than a lower-volume hardware stack memory, this approach is very economical. Also, there is likely to be spare memory available since it is purchased in large blocks. Thus, in many systems, the memory words used for the stack may come at virtually no extra cost.

The hardware necessary to implement this stack requires as few as 23 TTL IC packages. It includes registers to hold the stack boundaries and current location pointer, plus the necessary control and buffer logic. Other advantages to this approach are: cycle time is typically only 30 nsec longer than the main-memory cyle time (which can be very short with semiconductor memory), stack size is

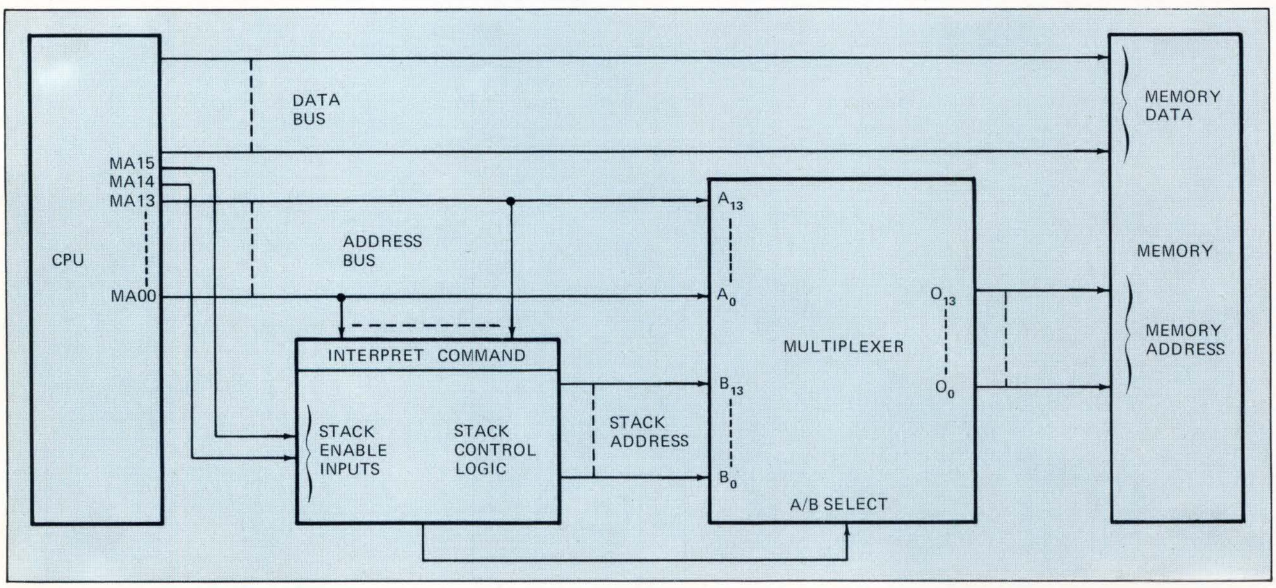


Fig. 1 – Stack memory controller for a 16-bit by 16k minicomputer. The memory address bus can be driven either by the CPU or stack controller.

modifiable under program control, additional stacks can be implemented by adding a duplicate set of hardware, and the memory addressing capability of the stack can be increased to any size by adding more bits to the registers.

Perhaps the most important feature is that the stack controller can be implemented without making any changes in the existing memory and computer, other than the necessity of inserting some tri-state gates in the memory-address lines and, in some systems, increasing the memory-access time by 30-40 nsec.

Implementing the stack memory

This detailed description is for a controller of a programmable-size stack up to 256 words for a 16-bit minicomputer with less than 16k of memory. The stack can be programmed on any 256 word page in the memory. Stack size can be increased to 4096 words by adding 10 additional ICs.

A functional block diagram of the stack controller is shown in **Fig. 1**. The memory address bus is driven either by the CPU or the stack controller, as determined by the select input to the multiplexer. Since the two most significant memory-address bits are not required to form the address of a 16k memory, they are used for commands to the stack controller. If the appropriate command code is placed on bits 14 and 15, the stack control logic will be enabled to place an address on the memory bus for execution of the current stack operation.

TABLE 1 - PARTS COUNT

No. CKTS	Part No.	No. DIPS
MEMORY INTERFACE		
8	DM8093	2
1 (3 SP)	7408	1
1 (5 SP)	7404	1
		SUBTOTAL = 4
LOWER 4 BITS		
2	7475	2
2	DM8563	2
2	DM8200	2
1	DM8123	1
7 (1 SP)	7408	2
10 (2 SP)	7400	3
3	74H10	1
		SUBTOTAL = 13
UPPER 4 BITS		
2	7475	2
2	DM8563	2
2	DM8200	2
1	DM8123	1
4	7408	1
		SUBTOTAL = 8
		LESS COMBINED SPARES = -2
		TOTAL = 23

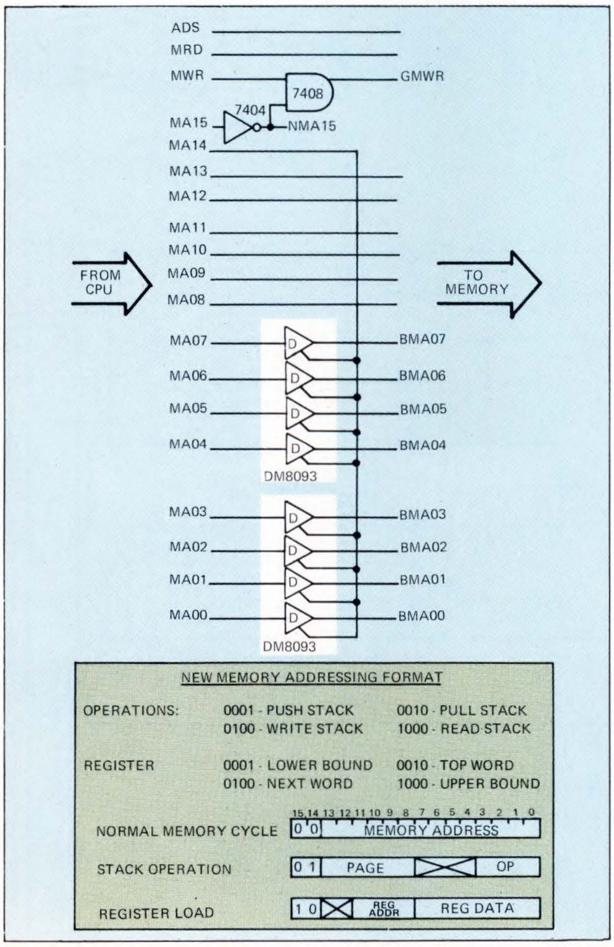


Fig. 2—Memory address bus must be driven by tri-state gates. If not already in use, the gates should be added as shown. New memory addressing formats are also required.

The multiplexer shown is actually implemented by using tri-state logic gates in both the stack control logic outputs and the computer's memory address (MA) bus. If the MA bus is not already driven by tri-state gates, they should be added as shown in **Fig. 2**. If a 4k stack, rather than a 256-word stack is desired, tri-state gates should also be added to MA08-MA11.

The new memory addressing formats are shown at the bottom of **Fig. 2**. Normal memory read and write operations occur when MA14 and 15 are zero. If MA14 is true, a stack operation will occur. The stack will be located on the memory page as specified by MA08-MA13, and stack operation will be specified by bits 0-3. A true bit 0 indicates push-stack, bit 1 a pull-stack, bit 2 a write-stack and bit 3 a read-stack.

When MA15 is true, a register load operation is specified. This allows data to be loaded into any one of the four stack-controller registers. These registers and the associated control logic are shown in **Fig. 3a** and **3b**. The UPPER BOUND register indicates the word on the stack page of memory which is to be the upper boundary, or highest word written into by a stack operation. A stack operation which writes into this word, causes a "stack full" indication (FULL in **Fig. 3a**). A stack operation which writes into a word higher than the upper bound, causes a "stack overflow" indication (NOVF). The TOP WORD register indicates the word on the stack page which contains the last item pushed on the stack. The NEXT WORD register indicates the word to be filled on the next push stack operation. The LOWER BOUND register indicates the lowest word to be read or written by a stack operation. If the TOP WORD and LOWER BOUND registers contain the same value, a "stack empty" indication occurs (EMPTY). If a stack operation occurs on a word below the LOWER

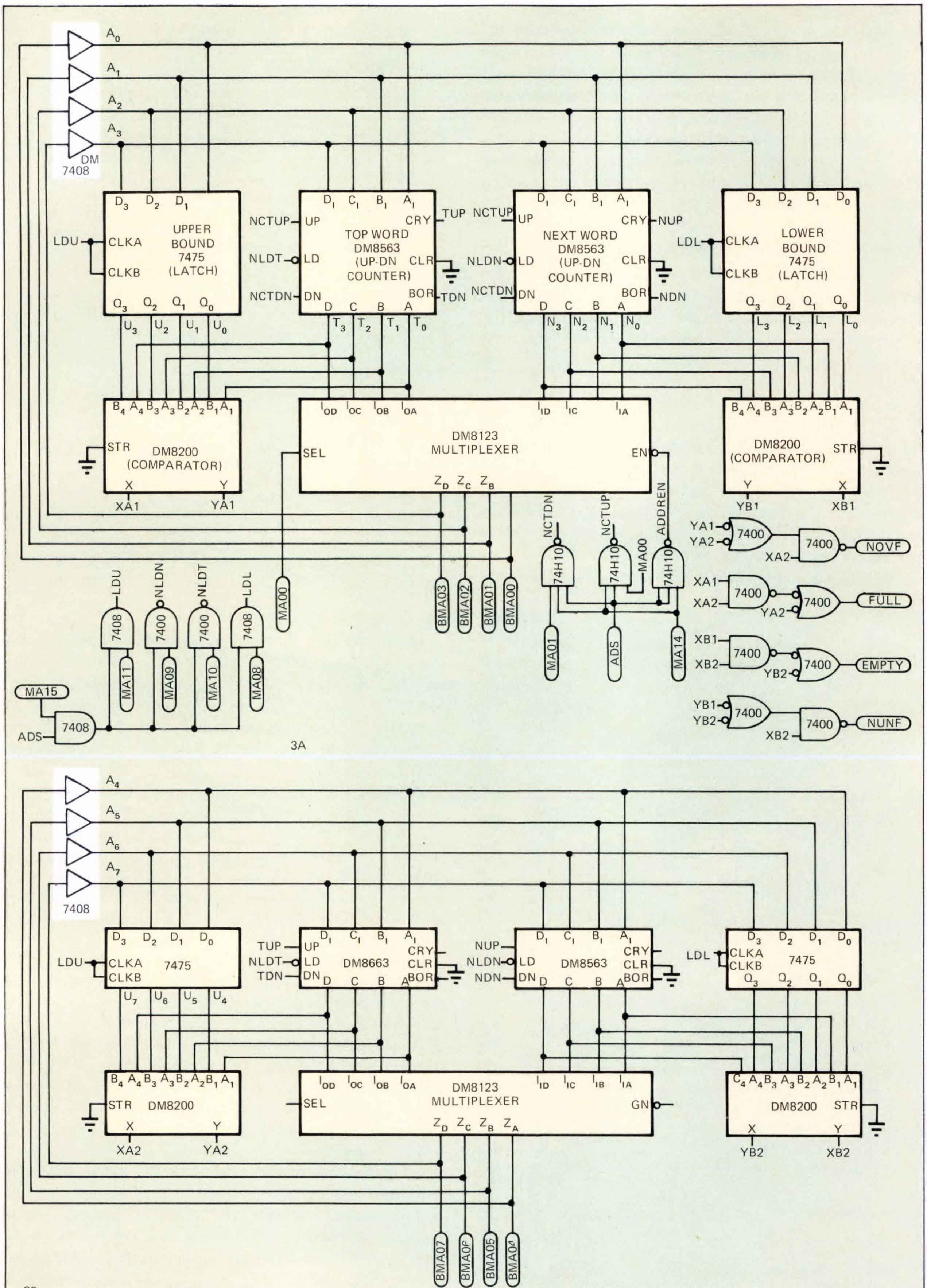


Fig. 3 – Four stack-controller registers are required for a 256-word controller. For a 4k word stack controller, only **3b** has to be duplicated.

BOUND, a "stack underflow" indication occurs (NUNF).

As shown in **Fig. 3a**, both the TOP WORD and NEXT WORD registers can drive the address bus. When a read, write or pull-stack operation occurs, the TOP WORD register drives the address bus. If the operation is a pull-stack, both TOP WORD and NEXT WORD are decremented by one at the end of the operation. Memory address bits 0 and 14 gate the register onto the bus; therefore, the memory access time will be increased by the delay time of the gates if the address is not available prior to the read or write pulse.

The address-data strobe (ADS) prevents decoding spikes when the address lines change state. When a push-stack operation occurs, the NEXT WORD register drives the address bus and, at the end of the operation, both TOP WORD and NEXT WORD are incremented by one.

The load register commands cause a parallel load from address bus bits 0-7 into the register specified by bits 8-11. During this time, the memory write pulse is inhibited (see **Fig. 1**) to prevent any actual memory word from being altered. (If the registers are always loaded using a memory-read, this inhibit is not required).

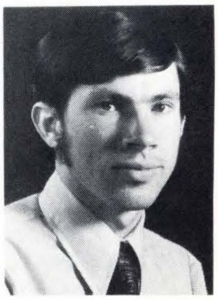
To expand the 256-word stack to a 4096-word stack, only the logic of **Fig. 3b** must be duplicated in addition to buffering 4 more lines. The parts count for a 4096-word stack is therefore, about 32 packages.

Other variations are possible

This example was chosen to demonstrate the simplicity of the memory-controller approach and its use in modifying an existing system with very minor change to the hardware, and no change to the software. Certainly, many variations of the basic idea are possible and useful. A very similar approach could be used for a first-in first-out memory using boundary registers and pointers to the front and back of the queu. In this approach, when a pointer encounters the upper boundary, it would be reset to the lower boundary, and when the pointers are at the same value, the buffer would be either empty of full.

To make hardware stacks and buffers which are not part of main memory, the approach described above is still very attractive. Any available semiconductor, core or other type of memory could be substituted for main memory. A very high-speed version could be built by using bipolar memory. By deriving the control signals from hardware, rather than the address bus, the memory access time would be minimized. ▭

Author's biography



George Reyling is a senior project engineer at National Semiconductor Corp. His principal responsibility is digital systems design. George previously worked at Fairchild Systems Technology and Litton Guidance and Control Systems. He received his MSES from Stanford University and his BSEE from California State Polytechnic College.

Network analyzer uses calculator for control and data analysis

PROGRESS IN INSTRUMENTATION

Network analysis traditionally has been done in one of two ways: either with manually controlled instruments or with totally automatic computer controlled instrumentation. The former has the advantage of relatively low cost, although with definite performance limitations, while the latter offers extremely sophisticated capability, including automatic data analysis, but at a greatly increased cost.

Now, a new Hewlett-Packard network analyzer offers the capability of a computer controlled system at a price approaching that of manually operated instruments. Designated the 3042 Automatic Network Analyzer, the system makes stimulus response measurements of linear networks using the 3330B Automatic Synthesizer as a source and the 3570A Two-Channel Detector as a tracking detector.

Of major significance is the fact that the measurements are made under the control of the 9820 Programmable Calculator. This is what gives the system the automatic control and data analysis capability of computerized systems.

The computational capability of the calculator not only provides simple decision making, such as Hi/Go/Lo limit testing and relative offset measurements, but also provides high-level algebraic manipulations of test data. Data can be stored for a series of tests and minipulated using statistical formulas to obtain the mean and deviation. Measurement results can be printed on the calculator's self-contained printer or recorded on magnetic cards for future use. In addition, plug-in ROMs are available for the calculator for controlling x-y plotters, typewriters or bulk-storage cassette memories. The calculator's 16-character alphanumeric display can even be used as an interactive display between the user and the system.

The calculator can also execute self-calibration programs supplied with the system. This makes possible amplitude measurements having an accuracy approaching that of the source (±0.05 dB). The calculator also makes it possible to easily measure the effects of test fixtures and automatically subtract them from the final results. In essence, the full power and versatility of the 9820A calculator are available to the system user. (See EDN, March 15, 1972, pages 90-91, for details on the 9820A Programmable Calculator.)

Amplitude measurements can be made with the network analyzer over a frequency range of 50 Hz to 13 MHz, and over a dynamic range of 100 dB. The frequency and amplitude resolution of the source are 0.1 Hz and 0.01 dB, respectively. Amplitude measurements can be made of the reference or test channel of the detector or the difference between the two. These frequency selective amplitude measurements can be made with bandwidths of 10 Hz, 100 Hz, or 3 kHz. The amplitude measurements of the detector are displayed on a 4-digit LED display to 0.01 dB resolution.

The phase of the test channel, with respect to the reference channel, is displayed by the tracking detector over a range of ±180° to a resolution of 0.01°.

The detector can optionally make group delay measurements by using the phase readings and the calculator to internally perform calculations on the group delay formula.

Analog outputs of the amplitude and phase readings are available for display on an optional x-y recorder or oscilloscope.

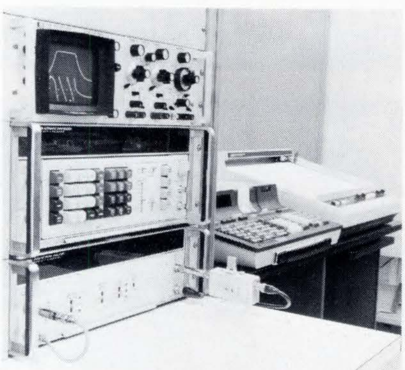
The 3042A Automatic Network Analyzer can be used in both the design lab and in production facilities for performing many measurements. Typical applications are: (1) to measure and adjust transfer functions of amplitude, phase, and delay for filter and amplifier design; (2) to characterize crystals, measuring shunt capacity, Q and phase compression; (3) to measure delay and delay distortion of telecommunications data modules: (4) to test gain-control circuits by using precision amplitude sweeps; (5) for closed-loop crystal-plating processes and; (6) for solid materials and foils testing.

An example of the significant savings in time possible with the 3042A is in the measuring of filter parameters such as insertion loss, stop-band rejection, pass-band ripple, group delay, and delay distortion. Although this often takes half an hour using conventional methods, the 3042A can easily make these tests in less than a minute.

One of the major reasons for the low price of the 3042A is that it uses a standard 15-line interface bus as the means of communications between the test instruments and the calculator.

Price of the 3042A Automatic Network Analyzer is $22,900. Deliveries begin in September. **315**

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. Phone (415) 493-1501. **316**



Automatic control and analysis by programmable calculator give the 3042A Network Analyzer the capability of a computer-controlled system at a price approaching that of a manual system.

Mini-maker bases cassette memory on very simple mechanical transport

PROGRESS IN PERIPHERALS

Data General, the minicomputer maker with a reputation for wise new-product choices, has finally, after two years, come out with a cassette memory system for its Nova family.

"Our search lead us to the simple transport that Redactron Corp. developed for itself two years ago for Redactron's low-cost editing typwriter," said Joe Godbout, engineer in charge of the project. "We liked the way they kept mechanics to the bare minimum and relied upon electronics to give them adequate performance," Godbout said.

The Redactron transport is about as simple a device as will move tape past a head. There is just one oversized garden-variety ac induction motor that drives two spindles that engage the cassette reel hubs. These spindles are rotated in opposite directions and two clutches determine which will be engaged and in which direction the tape will be driven. Clutches may not be the most reliable devices, but two derated clutches represent a lot less complexity than the assortment of solenoid-driven pinch rollers and multiple motors (some with servo speed controls) found in many more elegant cassettes, according to Redactron engineer, Edgar Wolf.

The oversized ac motor provides the transport with a fairly stable speed—even with power-line voltage variations; but as is true with all spindle drives the tape speeds up as it fattens the diameter of the take-up reel. Redactron holds this tape-speed variation down to about 1-1/2:1 by going to special cassettes with over-sized hubs. With regular cassettes the speed variation would be 2-1/2:1.

Ordinarily this speed variation would have forced them to go to some form of dual-track recording (such as ICP has pioneered), but Redactron has developed a clever sort of pseudo phase encoding that allows them to remain with a single track and avoid skew problems thus permitting the packing in of bit densities higher than those found on most other spindle-driven transports. This is important because the oversized hubs reduce the tape length to 200 ft., from the usual 300 ft. found in digital cassettes.

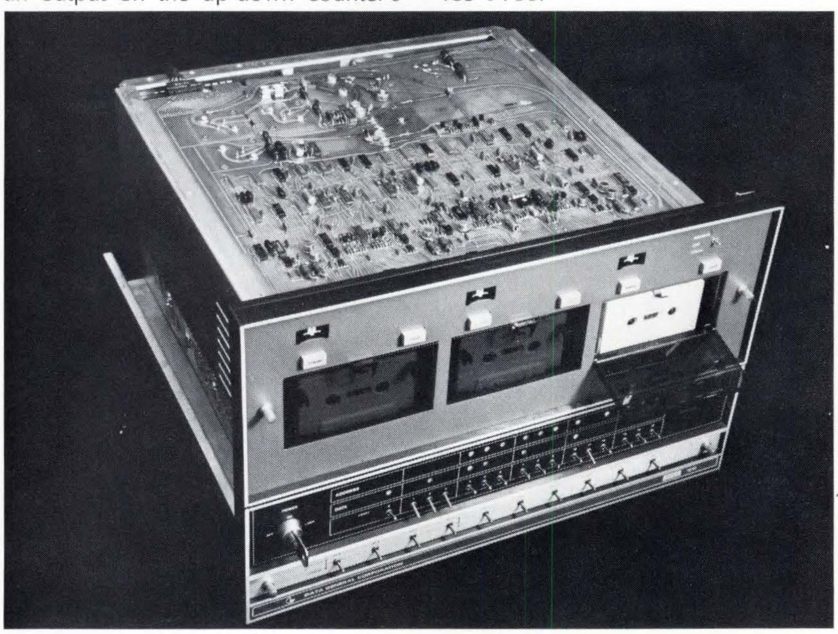
In recording, a three-stage ring counter driven at about 40 kHz divides the data cells on the tape up into three equal parts. The first stage of the ring always causes a positive-polarity flux transition at the beginning of the cell for a clock or reference mark. The second and third stages of the ring can be selectively gated by the data to be recorded to place the negative "return" polarity transition at either the 1/3 point or the 2/3 point in the cell. A ONE will gate the second stage to put the return at 1/3 and a ZERO will gate the third stage to put the return at 2/3.

An up-down counter driven by a higher-frequency clock is all that is needed to recover the data from the tape. The positive flux transition at the beginning of the cell starts the counter counting up, and then either negative-going flux transition will reverse the counter. One only needs to know at the end of the bit cell (which is indicated by the next cell's positive-going transition) whether the up-down counter went through zero or not.

Data General has developed its own TTL circuitry to implement this recording logic and merely looks for an output on the up-down counter's borrow-in pin to indicate whether the counter went through zero. (Redactron implemented the complete record and playback logic in one 40-pin LSI MOS chip).

Data transfer in the Nova cassette unit is 12 kbit/sec and storage capacity is 1 Mbit. Recording speed ranges from 24 to 38 ips.

Data General has priced their system in terms of the transport assembly that holds up to three transports and associated electronics and the interface or controller board that fits into one of the slots in the main Nova minicomputer. The transport assembly costs $2,000, $2,750 and $3,500 with one, two and three transports respectively. The interface control board (which conveniently uses the same software as previous Nova interfaces for large 1/2-in drives) costs $1,500 and controls up to 8 cassette drives. Standard Data General discounts up to 40% are available for quantity orders. The Nova cassette will come with a Data General software package that contains an operating system and cassette handler subroutines, along with capabilities such as assembling, editing, debugging and program storage and retrieval. Data General Corp., Southboro, Mass., 01772. Phone (617) 485-9100.



The three-cassette Nova memory system can be conveniently racked on top of a minicomputer, taking up just 7 in. in additional height. The cassette transport uses a single ordinary shaded-pole ac induction motor to alternately drive two counter-rotating spindles, via slip clutches.

Stable, thick-film fixed resistor has selectable resistance values

PROGRESS IN PASSIVE COMPONENTS

Engineers are frequently faced with circuit designs where the ultimate values of fixed resistors cannot be predetermined exactly during the design stage. A designer has no choice then but to specify a probable resistance value and have the exact value required for each circuit assembly determined empirically during manufacturing. This not only increases manpower requirements but makes it necessary to stock a very wide variety of resistor values.

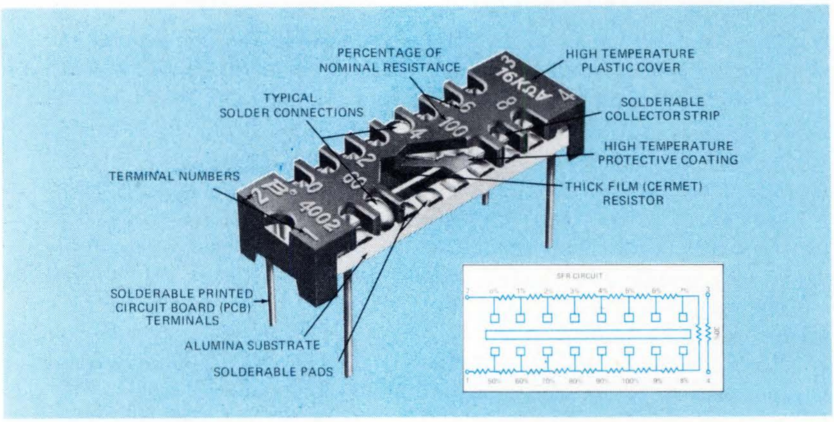
A new component, developed by Bourns and called a selectable fixed resistor, offers an economical alternative to the traditional design approach. Essentially, the Bourns SFR^{TM} Resistor is a thick-film fixed resistive component with the adjustability of a variable resistor. It can be adusted in 1% increments, semipermanently, over a range from 50 to 139% of its nominal value. When the exact resistance requirement is determined, the device is permanently set to that value by a simple soldering operation.

Fifteen standard values of Bourns SFR^{TM} Resistors are available, covering a resistance range from 33Ω to 1,25μΩ in selectable 1% steps. They are designed for PC board mounting and occupy a board area equal to standard 1/2W industrial metal-film resistors. The units meet MIL-R-55182 and have a T.C. of ±50 ppm average. A unique characteristic of the devices is that they provide inherent short-circuit and open-circuit protection for a circuit while they are being adjusted.

The Bourns SFR^{TM} Resistors can also be used in place of "set-and-forget" potentiometers where long-term stability is critical or where future adjustment is to be discouraged.

Prices of the devices are $2.22 in unit quantities, $0.97 for 50-99 and $0.76 for 1000 and over. Availability is factory stock. Distributor availability is scheduled for the end of the year.

Bourns, Inc., 1200 Columbia Ave., Riverside, CA 92507. Phone (714) 684-1700. **317**



The final resistance value is set by applying solder between two of the solderable pads and the adjacent collector strip. This results in a permanent solder connection that shorts the unnecessary resistance segments of the unit.

Storage scope writing speeds continue to take great leaps forward

PROGRESS IN INSTRUMENTATION

In the fast-moving electronics industry glory is very short lived. The most recent example of this was the announcement by Hewlett-Packard of an option for its Model 184A storage oscilloscope that boosts writing speed to 400 cm/μsec. This wrested the speed mantle for storage scopes back from Tektronix, who had just announced its Model 7623 with a writing speed of 200 cm/μsec.

In the HP unit, the 400 cm/μsec writing speed is achieved in the central part of the oscilloscope's graticule, as is common in such scopes. This area is then calibrated into a sub-graticule of 8 × 10 half-divisions. Resolution, however, is not lost. In the high-speed mode, scan is automatically reduced, and so is cathode potential. Spot size is therefore cut, and resolution in the reduced-scan region is as good as it is in normal full-scan operation.

The Tektronix 7623 writes at its 200 cm/μsec speed over the center 4 × 5 divisions of its graticule and at a somewhat slower rate over the full 8 × 10 screen divisions. It uses a special high speed target for capturing the high speed event, and then transfers it to a slower, long-retention target.

Both scope mainframes have a 100 MHz bandwidth. The HP unit accepts plug-ins (2) from the Model 190 Series, and the Tektronix mainframe accepts plug-ins (3) from the Model 7000 Series.

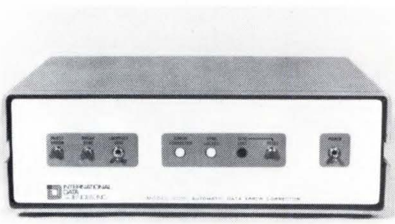
HP's 18A basic mainframe costs $2200 and option 005, which provides the 400 cm/μsec writing speed, adds $500. Tektronix's 7623 mainframe is $2850, and the fast-writing speed CRT, option 12, adds $500 to that price. An accurate price comparison, however, must include the costs of the necessary plug-ins. The HP unit is to be available in September and the Tektronix unit in October.

Hewlett-Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. Phone (415) 493-1501. **318**

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97005. Phone (503) 644-0161. **319**

COMPUTER PRODUCTS

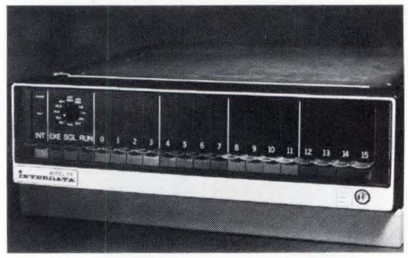
CORE MEMORIES RUGGEDIZED FOR HAZARDOUS USAGE. Models 1865M and 1885M memories meet applicable portions of MIL-E-16400. They are priced from 1.2 to 3.0¢/bit, depending upon size, quantity and configuration. The new memories have cycle times of 650 and 850 nsec and are available in sizes of 4k and 8k words of 9, 12, 16 or 18 bits. Combining modules provides storage capacities up to 65k words of 36 bits. Ampex Corp., 13031 W. Jefferson Blvd., Marina del Rey, CA 90291. Phone (213) 821-8933. **170**



AUTOMATIC DATA ERROR CORRECTOR ELIMINATES TRANSMISSION ERRORS. Validata 9100 finds and corrects 99.999% of all data errors on 4-wire, full duplex, synchronous data channels at operating speeds up to 9600 bps. Errors due to noise, line drop out, and loss of modem sync are corrected in both directions simultaneously. The 9100 installs on-line in seconds and leases for $1 per day per unit. International Data Sciences, Inc., 100 Nashua St., Providence, RI 02904. Phone (401) 274-5100. **171**

TERMINAL INTERFACES FOR MOST COMPUTERS. Interfaces for the company's 4002A graphic computer terminal and 4010 computer display terminal family now include computers manufactured by DEC, Data General, H-P, Varian, Honeywell, Interdata, and Raytheon. The 4010 is a low-cost CRT terminal for business and scientific use. Tektronix, Inc., P.O. Box 500, Beaverton, OR 97005. Phone (503) 292-2611. **172**

DATA MODEM OPERATES FROM 1200 TO 3600 BPS. The modem converts from 1200 asynchronous to either 2400 or 3600 bps synchronous-mode operation. The ADS-412/424/436 operates FSK at 1200 bps, and PSK at the 2400 and 3600 bps speeds. It can operate in a wide variety of system applications, both on dial-up and private line for example, polled operation, reverse channel and Ack-Nack. American Data Systems, 8851 Mason Ave., Canoga Park, CA 91306. Phone (213) 882-0020. **173**



LOW-COST 16-BIT PROCESSOR OFFERS ADVANCED FEATURES. Model 74 includes hardware multiply/divide, 16 general registers, 64k of directly addressable core memory, LSI ROM, up to 255 I/O interrupts with automatic vectoring to service routine, and upward compatibility with all other new series processors. The memory is built around a 4k × 16-bit core module with access time of 300 nsec and cycle time of 1.0 μsec. It is expandable in 8k modules up to 64k. $3600 with 8k or core. Interdata, 2 Crescent Pl., Oceanport, N J 07757. Phone (201) 229-4040. **174**

GE INCREASES SPEED OF TERMINET PRINTERS. The TermiNet ® 1200 can quietly produce hard copy in multiples of seven at a print rate of 120 cps. It has switch-selectable transmission speeds of 10, 30 or 120 cps. Copy appears in upper and lower case alphabetics. The printer is available in three configurations: (RO), (KRS) and (ASR). GE Communication Systems Div., Section P, P.O. 4197, Lynchburg, VA 24502. Phone (703) 846-7311. **175**

MINI-DISC EXPANDS CALCULATOR AND SMALL-COMPUTER MEMORIES. The 8200 Series memory measures 8 × 9 × 9 in, features non-positioning flying heads and read/write electronics. Average access time is 8.5 msec, and data transfer rate is 1.09 MHz. Two models are available; an 8-track, 145k-bit unit and a 16-track, 290k bit-version. Information Data Systems Inc., 7550 Walnut Lake Rd., Walled Lake, MI 48088. Phone (313) 624-5525. **176**

LINE CONDITIONER UPGRADES PHONE FACILITIES FOR DATA TRANSMISSION. Model 66 conditions the amplitude response and envelope delay of voice frequency telephone circuits for data transmission. Units are available with standard 200 Hz equalizer spacing or "proportional spacing" for extended bandwidth equalization. Price is $550. Hekimian Laboratories, Inc., 322 N. Stonestreet Ave., Rockville, MD 20850. Phone (301) 424-3160. **177**

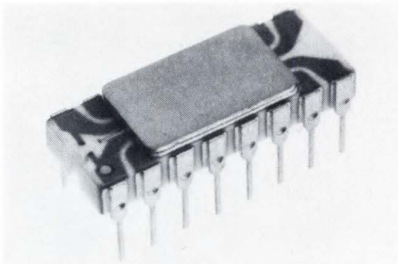
DATA CASSETTE MEETS ANSI, ECMA STANDARDS for digital data recording. The "R" series cassette contains computer-grade tape which is certified for zero drop-outs. Hinged write-lockout tabs can be moved easily to permit re-recording of data. End-of-tape/beginning-of-tape holes are provided. Information Terminals, 1160 Terra Bella Ave., Mountain View, CA 94040. Phone (415) 964-3600. **178**

DEC CUTS PDP-8 PRICES. Price reductions up to 27% on PDP-8 family minicomputer mainframes and up to 45% on typical systems are announced by DEC. A new core memory reduces the price of an 8k-word PDP-8/E from $7740 to $5,650. The price of an 8k-word PDP-8/F is reduced from $6740 to $5150, and PDP-8/M from $6395 to $5150. A 4k-word PDP-8/E price is reduced from $4990 to $4490. The new 8192-word core memory is also being offered in 8k-word add-on increments for $4900. Digital Equipment Corp., 146 Main St., Maynard, MA 01754. Phone (617) 897-5111. **179**

HALL-EFFECT DEVICE IMPROVES CASSETTE HEAD'S ACCURACY. The model RAW-7101 is a dual gap Hall-Effect device which generates an output signal proportional to the recorded magnetic flux and is independent of tape speed. The output tape signal at a recording density of 1600 FRPI is typically 0.4 mV, P-P. $65. Pioneer Electronic Corp., 525 W. Remington Dr., Sunnyvale, CA 94087. **180**

DEDICATED CALCULATORS PROVIDE POWER OF DESK-TOP UNITS. The new machines are the Models 320 Scientist and 340 Statistician, and the programmable Models 322 and 342. Each model has multiple storage registers, calculates with true 13-digit accuracy, and displays 10 digits with sign and 2-digit exponent. The keyboards are fully algebraic and have keys for right and left parentheses, which can be double-nested. Models 322 and 342 feature an 80-step "scratchpad" programmer. Computer Design Corp., 12401 W. Olympic Blvd., Los Angeles, CA 90064. Phone (213) 829-3501. **261**

SEMICONDUCTORS

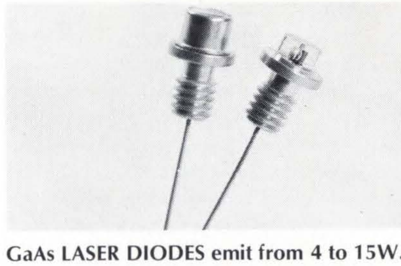


PROM USES FUSIBLE LINKS OF SILICON. This 1024-bit bipolar Prom is programmed by breaking fusible links of silicon imbedded in the matrix of the chip. The silicon fuse separates cleanly and cannot cure or re-link. The 3601 has an access time of 70 nsec. The PROM is pin-compatible with mask-programmed Type 3301A ROMs. Price: $39 each in 100-piece quantities. Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051. Phone (408) 246-7501. **181**

COUNTER TIME BASE REQUIRES LESS POWER AND SPACE THAN TTL. With MK 5009P MOS circuit only one 16-pin package is required, and power requirement is only 80 mW. It is designed to operate with any of three frequency sources: the internal oscillator; an external crystal; or externally applied TTL signal. Frequency division ratios up to 36×10^8 are available. Price is $15 each. Mostek Corp., 1215 W. Crosby Road, Carrollton, TX 75006. Phone (214) 242-0444. **182**

ONE RESISTOR PROGRAMS MICROPOWER OP AMP. At a nominal value of the programming resistor, max input bias current of the LM4250 is 7.5 nA, input offset current is 3 nA, input offset voltage is 3 mV and standby power dissipation 255 μW. Input resistance varies from 2.2 MΩ at high set current to a large as 100 MΩ at low set currents. The LM4250 is pin-compatible with 741 op amps. National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, CA 95051. Phone (408) 732-5000. **183**

4-BIT SYNCHRONOUS UP/DOWN COUNTER PAIR operates at 1/4 regular power yet offers 1/2 the speed of the standard-powered counterparts. These counters offer separate up and down clocks, asynchronous parallel loading and typical operating speeds of 23 MHz with power dissipation of 85 mW. Prices for the counters in the 100 up price range are from $6 to $23 each. Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, CA 94086. Phone (408) 732-2400. **184**

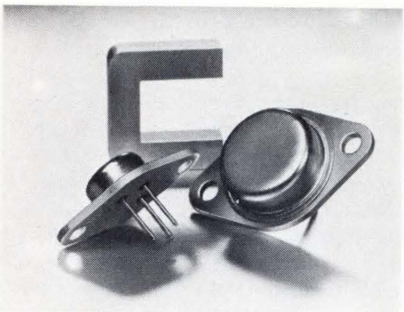


GaAs LASER DIODES emit from 4 to 15W. These diodes will operate at 27°C to duty cycles of 0.1% when biased in the forward direction with up to 200 nsec current pulses. All units are available in either a standard hermetic package or a non-hermetic high thermal conductivity copper package. Peak output is at 905 nM. Priced from $8.00 to $27.60 in quantities of 1000. Laser Diode Labs., Inc., 205 Forrest St., Metuchen, N J 08840. Phone (201) 549-7700. **185**

HYBRID IC INTERFACES TTL CLOCKS WITH MOS SYSTEMS. MHP401 clock driver is capable of sourcing and sinking the large peak currents necessary in order to achieve high clock rates while driving highly capacitive loads. While driving a 500 pF load and operating from +5V and −12V power supplies, the unit can supply clock pulses at rates of up to 5 MHz. In 100-up lots, the MHP401 goes for $3.90. Motorola Inc., Semiconductor Products Div., P.O. Box 20924, Phoenix, AZ 85036. Phone (602) 273-6900. **186**

MONOLITHIC D/A CONVERTER HAS 8 ±1/4-BIT ACCURACY. The DA110 series of devices employs an R-2R ladder network of diffused resistors plus passive PMOS switches. LSB accuracy of the DA110 is rated at ±1/4-bit. All devices have settling time to LSB of 4μsec. Prices in 1-29 quantities range from $31.50 for the DA112 to $15.00 for the DA110. Siliconix Inc., 2201 Laurelwood Road, Santa Clara, CA 95054. Phone (408) 246-8000. **187**

300-A HIGH-CURRENT ARRAY OF INTERCONNECTED SILICON TRANSISTORS, type TA8642 consists of six 50A transistors mounted in a plastic package with a common collector connection. With the six transistors connected in parallel the device features a switching capability of 300A and a dissipation of 1000W. The TA8642 is priced at $99 in quantities of 1-99 units. RCA Solid State Div., Box 3200, Somerville, N J 08876. Phone (201) 722-3200. **188**



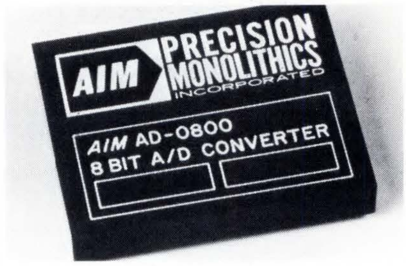
POWER DARLINGTONS FEATURE HIGH VOLTAGE, HIGH GAIN and low saturation voltage. The U2T501/U2T601, a 20 Amp NPN series, offers current gain up to 2000 min. @ 10A and voltage ratings of 80 and 150 V. The series is available in 3-pin TO-3 and TO-66 chassis mounted hermetically sealed metal packages, priced at \$4.30 in 100 quantities. Unitrode Corp., 580 Pleasant St., Watertown, MA 02172. Phone (617) 926-0404. **189**

COMPARATORS HANDLE LONG BINARY NUMBERS. The DM7130/8130 ten-bit comparator determines equality or non-equality between two words while the DM7160/DM8160 compares six-bit words, in about 20 nsec. For longer words, the comparators may be paralleled. Prices in 100-up quantities are DM7130D, \$16.00; DM7160J, \$11.00; DM813ON, \$4.50; DM816ON, \$3.25. National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, CA 95051. Phone (408) 732-5000. **190**

HIGH-SPEED COUNTER PAIR IS PIN COMPATIBLE WITH 54/74192 and 193. These 4-bit synchronous up/down counters offer separate up and down clocks, asynchronous parallel loading and operate at typical speeds of 32 MHz. Prices for the counters in 100-up mix quantity are: Hermetic DIP, (−55°C to 125°C) is \$20.70 each, and Molded DIP, (0°C to 75°C) is \$5.40. Advanced Micro Devices Inc., 901 Thompson Place, Sunnyvale, CA 94086. Phone (408) 732-2400. **191**

SYNCHRONOUS CMOS UP-COUNTERS OFFER 6 MHz OPERATION. The MC14518 provides a dual, BCD function while the MC14520 offers dual binary up-counting. Counter stages are type-D flip-flops that have interchangeable clock and enable lines. This allows counting on either positive- or negative-going clock signal transitions. Prices range from \$7 to \$12.90 in orders of 100. Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85026. Phone (602) 273-6900. **192**

CIRCUITS



A/D CONVERTER ENCODES 8 BITS IN 4.0μSEC MAX! The high speed, small size (2.0 in. × 2.5 in. × 0.4 in.) and accurate performance of the aimADO800 Series is achieved by combining a monolithic aimDAC100 D/A Converter and comparator to form a successive approximation A/D. One option guarantees a minimum of 1,000,000 5-bit conversions per sec. Prices at 100-249 pieces: aimAdO800—$160.00. Precision Monolithics Inc., 1500 Space Park Drive, Santa Clara, CA 95050. Phone (408) 246-92251 **193**

MINIATURE DROP-IN CIRCULATOR COVERS 1.225 TO 1.425 GHz. The tab-lead circulator has an isolation of 20-dB minimum, an insertion loss of only 0.5 dB maximum, and a maximum VSWR of 1.25. Designed for 50Ω microstrip or stripline circuits, Model 1419-1107 has a 1-kW peak, 50W average power rating and will operate from −40 to +71°C. It measures 1 × 1 × 0.3 in. and costs $277. Trak Microwave Corp., 4726 Eisenhower Blvd., Tampa, FL 33614. Phone (813) 884-1411. **194**

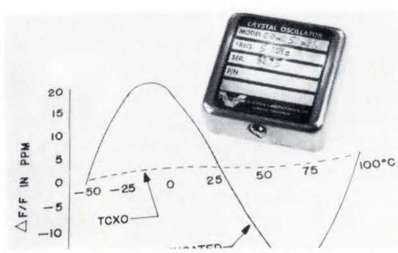
FET OP AMP OFFERS ±5-μV/°C VOLTAGE DRIFT and input bias of ±5 pA maximum. Model 350k also has low input voltage noise of 3 μV pk-pk from 0.01 to 10 Hz and 3 μV rms from 10 Hz to 10 kHz. Input current noise is 0.1 pA pk-pk over 0.01 to 10 Hz and CMRR is 10^4. Output is ±10V at ±5 mA. Cost is $49 ($35 for Model 350J with ±15-μV/°C input voltage drift). Function Modules, Inc., 2441 Campus Dr., Irvine, CA 92664. Phone (714) 833-8314. **195**

7-SEGMENT DECODER/DRIVER-CONNECTOR COMBINATION. Model DD-20 decoder/driver-connector and Model DDL-20 decoder/driver latch connector combination features intensity modulation control, 5V operation, ripple blanking, a lamp-test provision and DTL, TTL and RTL-compatible BCD inputs. Other features include high-current sinking capability for direct display driving and leading/trailing-zero suppression. Pinlites, Box 453, Caldwell, N J 07006. Phone (201) 575-8820. **196**

INDUSTRIAL FREQUENCY SENSOR OFFERS ±2% ACCURACY. The sensor de-energizes power lines when the frequency of a single or 3-phase line exceeds a pre-set limit. The pre-set low-frequency limit is programmed into the device. When the limit is exceeded, the unit de-energizes to operate alarms or shutdown the system. When the line frequency resumes permanently, the sensor automatically re-energizes the system. Price for the LFS-1 is $65. Logitek, Inc., 42 Central Dr., Farmingdale, NY 11735. Phone (516) 694-3080. **197**

TWO-FREQUENCY TONE SQUELCH SS-80J for two-way radio users measures 2-2 /3 × 1 × 5/8 in. The SS-80J employs thick-film microelectronic modules that contain all of the active circuitry used for encoding and decoding. The modules fit into a unique edge connector on a small PC board. Tone frequencies are available from 20.0 to 250.0 Hz. Alpha Electronic Services, Inc., 8431 Monroe Ave., Stanton, CA 90680. Phone (714) 821-4400. **198**

FOUR-QUADRANT MULTIPLYING D/A CONVERTER DAC-MV Series offers output response of dc to 200 kHz and output settling time of 1.5 μsec to 0.01% of fullscale. Requiring only one variable reference input, it can be used as a conventional or multiplying d/a converter. The analog output of the converter is a product of the bipolar reference input and a digital word input. TC is ±30 ppm/°C and fullscale accuracy is ±0.01%. Prices range from $99 to $139. Datel Systems, Inc., 1020 Turnpike St., Canton, MA 02021. Phone (617) 828-6395. **199**



TEMPERATURE-COMPENSATED CRYSTAL OSCILLATOR IS ±10^{-7} STABLE OVER 0 TO +50°C. Model CO-252-3A employs computer-compensation techniques to achieve this stability without the use of an oven. Low-current drain of 5 to 10 mA, 1×10^{-8} per day and 1×10^{-6} per year long-term stabilities and instantaneous "on-frequency" operation are other features. Models are available with sine, TTL or CMOS outputs in the 1-to-20-MHz range. Other models are available to cover 60 Hz through 80 MHz. Vectron Laboratories, Inc., 121 Water St., Norwalk, CT 06854. Phone (203) 853-4433. **200**

X-BAND GUNN-EFFECT OSCILLATOR SSX-12011 which is constructed in conventional wave-guide-flange configuration and requires no additional cavity for normal stability requirements features output power of 20 mW with a varactor tuning range of 50 MHz and 10 mW with 90-MHz tuning. Mechanical tuning range is 1200 MHz. Sperry Electronic Tube Div., Waldo Rd., Gainesville, FL 32601. Phone (904) 372-0411. **204**

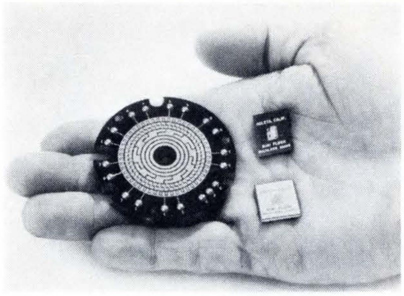
ULTRA-HIGH-SPEED HIGH-PRECISION A/D CONVERTER. Model GMAD-01 has a conversion time which is proportional to resolution and ranges from 100 nsec for 7 or 8 binary digits and sign, to 500 nsec for 12 bits and sign. Conversion speed for 13 bits without sign is 1 μsec. Accuracy is proportional to resolution ($\pm$1/2 LSB). At 13 bits, the specified accuracy is $\pm$0.015%. Sampling aperture time is 1 nsec. Preston Scientific Inc., 805 E. Cerritos Ave., Anaheim, CA 92805. Phone (714) 776-6400. **202**

4-CHANNEL MULTI-SPEED S/D CONVERTER S3313 converts 2-speed, 3-wire synchro data to a decimal display readout. The combined synchro angle is read out from 0 to $\pm$179 degrees 59.9 minutes. This readout is also available as an electrical output in 32-bit serial binary and sign plus 6 digits in serial and parallel BCD. Gap Instrument Corp., 110 Marcus Blvd., Hauppauge, NY 11787. Phone (516) 273-0909. **203**

TWO OPTO-ISOLATOR COUPLERS are the CM4-5010 and CM4-5020 with typical isolation resistances of $10^{11}\Omega$. Breakdown voltage for the latter is 2500V dc and current transfer ratio is 20%. Both units are packaged in standard mini-DIP cases. Costs for the CM4-5010 in 1000 quantities is $1.40 each. The CM4-5020 costs $2.95 each in 1000 quantities. Chicago Miniature Lamp Works, 4433 N. Ravenswood, Chicago, IL 60640. Phone (312) 784-1020. **201**

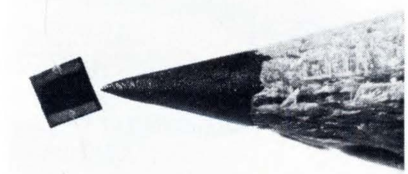
TRANSIENT VOLTAGE-SUPRESSION MODULE for Type S devices contains an RC circuit and is intended for use with Type S coils rated 120V or less. It is designed to limit the transient voltage pulse to 200% of peak line voltage. Suppression components are encapsulated, protecting them from mechanical and environmental damage. Two leads from the module are connected across the suppressor's coil. Square D Co., Milwaukee, WI 53201. Phone (414) 332-2000. **205**

COMPONENTS/MATERIALS



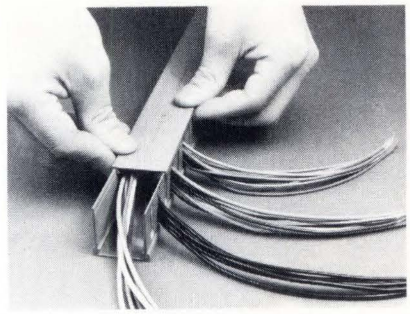
HYBRID SUBSTRATES COSTS CUT 50% BY UNIQUE APPROACH. Utilizing solid-post multilayer printed circuits and precision flush circuits, the technique yields low-cost circuits for mounting beam-lead, flip-chip and other miniature components. Line widths of 2 mils on 10 mil centers are achieved. Boards incorporating these features are available in sizes from 1/4 in. × 1/4 in. to 15 in. × 15 in. Photronics, Inc., 26 Coromar Drive, Goleta, CA 93017. Phone (805) 968-3451. **206**

SOLID STATE AC RELAY SWITCHES 480 WATTS. The GB870 series Reedacs, solid state AC relays, can switch 480 W at 120V ac with packaging so small that two units will fit side by side in a single DIP socket. Price is $2.90 each in orders of 1,000. Grigsby-Barton, Inc., 3800 Industrial Drive, Rolling Meadows, IL 60008. Phone (312) 329-5900. **207**



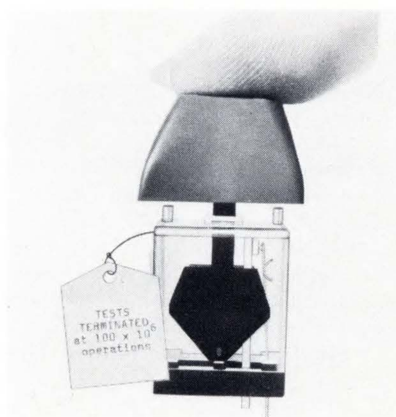
THERMOFLAKE THERMISTORS FOR MICROCIRCUIT APPLICATIONS. The series F40, F80 and F120 consist of thick film thermistors not supported by substrate backings. Depending on the size, thermal time constants range from less than 38 msec to 75 msec. Units are priced from $9.70 to $14.70 each in quantities of 100 to 249. Thermometrics, 15 Jean Pl., Edison, N J 08817. Phone (201) 548-2299. **208**

WIRE INSULATION, KYNAR (R) VINYLIDENE FLOURIDE RESIN, has excellent cut-through resistance. It feeds, cuts and strips smoothly, takes 180° bends without splitting, stands up to automatic wiring machines or semi-automatic hand tools. For samples/literature kit and a list of wire fabricators, write Plastics Dept., Pennwalt Corp., 3 Parkway, Philadelphia, PA 19102. Phone (215) 587-7000. **209**

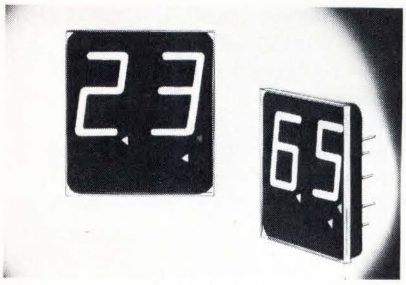


MODULAR PLASTIC WIRING DUCT ASSEMBLES EASILY. Base, cover, and solid (or slotted) side panels of the plastic wiring duct can be assembled quickly to form customized ducts. Available in 1 in., 1 1/2 in., and 3 in. height or width, the 6 ft. long components can be readily cut with snips and punched or drilled for mounting. Wires routed through the slotted sides are completely encircled to prevent slipping. American Pamcor, Inc., Box 1776, Paoli, PA 19301. Phone (215) 647-1000. **210**

SEMICONDUCTOR COOLING PACKAGE DISSIPATES 450W. The hole pattern in each HP3 can be arranged for single or dual semiconductor mounting, allowing the use of up to 8 semiconductors. Cost in a 10-piece quantity is $9.95 each, without fans. International Electronic Research Corp., 135 E. Magnolia Blvd., Burbank, CA 91502. Phone (213) 849-2481. **211**



LONG LIFE KEYBOARD SWITCH COMBINES GOLD CONTACTS with crosspoint configuration, eliminates interference from foreign particles. This single pole, momentary contact switch is not affected by exposure to moisture and thermal shock. Tests were terminated on 12 samples at 100 × 106 operations with all 12 switches functional. The keyboard switch module is available (without key cap) at $0.29 in 250,000 quantity. Cherry Electrical Products Corp., 3600 Sunset Ave., Waukegan, IL 60085. Phone (312) 689-7600. **212**



FASTER ILLUMINATING DISPLAY HAS "KEEP ALIVE" CATHODES. The "keep alive" cathode is an internal ion source that improves the overall operation of these displays in multiplex applications, dark environment, low-temperature environments and applications where suppression or blanking of zeros is a requirement. The 5000 Digit price is $2.30. Sperry, Information Displays Div., P.O. Box 3579, Scottsdale, AZ 85257. Phone (602) 947-8371. **213**

DIP SOCKETS FEATURE POSITIVE CLOSED-ENTRY INSULATORS which prevent damage to socket contacts during IC insertion. IC leads are gripped on ends rather than on sides to assure maximum retentive force. Data sheets as well as FREE SAMPLES for approval are available. Request samples on your company letterhead. Inquiry Processing Dept., JOLO Industries, 11861 Cardinal Circle, Garden Grove, CA 92643. Phone (714) 636-4940. **214**

THUMBWHEEL SWITCH IS AVAILABLE IN ALL STANDARD CODES. It is available with colored wheels, special markings, extra-long PC boards for component mounting, and 240 different binary codes as well as 10- and 11-position decimal outputs. The P switch is designed to deliver dependable operation for more than 1 million detent operations. Type P switch is priced at $2.85 each in quantities of 100 units. Interswitch, 770 Airport Blvd., Burlingame, CA 94010. Phone (415) 347-8217. **215**

METALIZED POLYCARBONATE CAPACITORS OFFER MAJOR SIZE REDUCTION. Mini-Miniature 22 Series now produced in a variety of standard encasements styles and leads, in 50V dc and 100V dc sizes. Ranges are from 0.001 μF. through 50 μF. A typical size in the 22R Series is 10.0 μF, 50V dc, with 0.58 in. O.D. $\times$ 1.16 in. in length. S & El Manufacturing, 18800 Parthenia St., Northridge, CA 91324. Phone (213) 349-4111. **216**

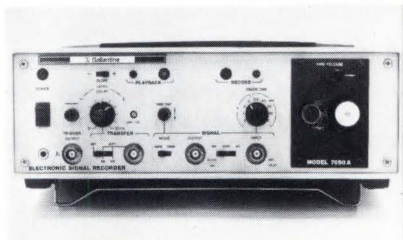
PORTABLE 3-DIGIT DVM, Model 3300, is housed in a ruggedized Lexan case that will withstand dropping and banging. The 3300 operates from 115V ac or Ni-Cd batteries. Exclusive cam rotary switches prohibit the selection of improper combinations of ranges and functions. Five dc, four ac-voltage and five resistance ranges are available in this 7-1/2-lb (with battery) $350 instrument (add $50 for battery pack). Dana Laboratories, Inc., 2401 Campus Dr., Irvine, CA 92664. Phone (714) 833-1234. **219**

512-MHz COUNTER-TIMER, Model 600H, costs only $1095. Its additional measuring modes include period, time interval, frequency ratio, totalizing and stopwatch. A unique input-triggering feature synchronizes the internally controlled gate with the signal frequency. Called Syncrostart, it reduces quantizing error to −1, +0 counts from the usual ±1 count. Model 600 (50-MHz) is available for $750. Newport Laboratories, Inc., 630 E. Young St., Santa Ana, CA 92705. Phone (714) 540-4914. **220**

DIGITAL RADIOMETER/PHOTOMETER SYSTEM, IL600A/IL630, combines digital and analog readout for monitoring optical radiation over the spectral range of from 200 to 1100 nm. Eleven overlapping sensitvity ranges provide an overall dynamic range of 1×10^6 to 1. Maximum full-scale sensitivity is 0.001 μA. The system also has four ranges of cancellation current from 0.005 to 5 μA. It is priced at $1247. International Light, Inc., Dexter Industrial Green, Newburyport, MA 01950. Phone (617) 465-5923. **221**

PROGRAMMER HANDLES FUSIBLE-LINK ROMS. Manual programming of all Signetics fusible-link ROMs is easy on the PR-369 master programmer. It will program five different ROMs of both 32-×-8 and 256-×-4 organizations including the new high speed Schottky devices. Pressing a single pushbutton per output initiates an automatic, internal programming sequence. The instrument is priced at $399. Curtis Electro Devices, Box 4090, Mountain View, CA 94040. Phone (415) 964-3136. **222**

RECORDING MILLIVOLTMETER/MILLIAMMETER single-channel Model 202-100 features a channel width of 100 mm and a unique stylus replaceable by untrained personnel without tools. The instrument permits full-scale ac and dc readings of 0 to 50 mV, 0 to 1 mA or 0 to 50 μA. Recordings are made without ink on a new low cost heat-sensitive paper. Price of the unit is $350. Astro-Med, Div. of Atlan-Tol Industries, Inc., Atlan-Tol Industrial Park, W. Warwick, RI 02893. Phone (401) 828-7010. **223**



ELECTRONIC SIGNAL RECORDER offers signal-storage capabilities with greater flexibility at a fraction of the cost of storage scopes. Model 7050A Electronic Signal Recorder (ESR) uses a continuous magnetic loop. Bandwidth of the carrier system is dc to 100 kHz. The writing speed exceeds 3000 div./msec with a dynamic range greater than 34 dB. The $985 ESR continuously recoras and is triggered to the store mode. Ballantine Laboratories, Inc., Box 97, Boonton, N J 07005. Phone (201) 335-0900. **224**

$285 PULSE GENERATOR features repetition rates from 2 Hz to 20 MHz in 7 overlapping ranges, 5-nsec rise/fall times, variable pulse width from 20 nsec to 200 msec and a variable 5V output into 50Ω (baseline is fixed at 0 ±0.25V. A 40-mA sink current is available. Model 99 unit has fixed 5-nsec delay and 5% pk-pk maximum overshoot at 5V output. Systron-Donner Corp., Datapulse Div., 10150 W. Jefferson Blvd., Culver City, CA 90230. Phone (213) 870-6771. **225**

LITERATURE

TIMER AND COUNTER CATALOG describes a line of time, count, program and step controls and accessories. The catalog includes a selection guide and a glossary of timer and counter terms used. Automatic Timing & Controls, Inc., King of Prussia, PA 19406. **231**

MODEM FACT SHEET. Pulsecom has a new brochure describing their complete line of low speed, Bell compatible data modems. Designated the 4080 Series, the modems are available in a variety of configurations, featuring TTY, EIA, or TLT interfacing, loop back testing and visual diagnostics, and dedicated or dial line operation. Pulsecom, 5714 Columbia Pike, Falls Church, VA 22041. **232**

THE J133 TEST-PACKAGE CATALOG from Teradyne contains a 55-page price list and catalog for the analogical-circuit test instrument. Over 3800 digital ICs that can be tested on the J133 are listed by manufacturers' part numbers, with the stock numbers and prices of the J133 programming boards for each IC. Teradyne, Inc., 183 Essex St., Boston, MA 02111. **233**

MODEMS . . . Bell-compatible 300, 1200 and 2400 bps data sets, plus other specialized data communications products are described in a new 4-page catalog. Full specifications of the modems, as well as Bell equivalency and compatibility are given in chart form. The catalog also describes a multichannel FSK/FDM data transmission system, a speech-plus adapter and a multiline switch. Tele-Dynamics Div. of AMBAC Industries, 525 Virginia Dr., Fort Washington, PA 19034. **235**

THERMISTOR CATALOG, L-4A, covers a broad variety of thermistor sensors and sensor assemblies. Included in this catalog is a sampling of the most commonly used types of FE thermistors and probe assemblies which include Iso-Curve and Uni-Curve, R-T curve matched interchangeable thermistors, FE thermistor beads, probes, discs, washers, rods as well as expanded listing of fast-response glass-probe thermistors and thermistor glass encapsulated diode types. Fenwal Electronics, 63 Fountain St., Framingham, MA 01701. **236**

FREQUENCY SOURCES and accessories including frequency synthesizers, extremely stable signal generators, broadband and tunable power amplifiers and modular amplifiers are described in a new catalog. RF Communications, Inc., 1680 University Ave., Rochester, NY 14610. **237**

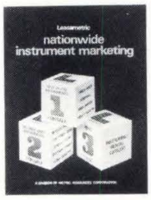
MINICOMPUTER TAPE DRIVE. A new brochure describes operations and specifications of the Model TMY digital tape drive. The TMY is a low-cost, 7-inch-reel tape drive for minicomputers, data terminals, key tape equipment and process-control systems. Request brochure: C-308. Ampex Corp., Marketing Communications, 13031 W. Jefferson Blvd., Marina del Rey, CA 90291. **238**

MINIATURE STRIP-CHART RECORDERS from Amprobe are shown in a new catalog. Also described are ac and dc ammeters and voltmeters, ac volt/ammeters, thermometers, pyrometers, event recorders and time-sharing recorders that record up to 3 variables on the same chart. Amprobe Instrument, 630 Merrick Rd., Lynbrook, NY 11563. **239**

2400 BPS MODEM. The illustrated 8-page data sheet includes features, technical data, as well as typical applications diagrams for Modem 24. The modem uses MOS LSI technology to improve system efficiency and reliability. Other features offered include system error diagnosis from a single site, on-line evaluation of the data communication system, and modem self-test capability. International Communications Corp., 7620 N. W. 36th Ave., Miami, FL 33147. **240**

THE STORY OF COMPUTER GRAPHICS. An amusing 12-page, 11 by 14 booklet tells the story of man's attempts to communicate using graphics. The publication details specifications of the H-P Model 7200A graphic plotter. In easy-to-read cartoon style, "The Story of Computer Graphics" demonstrates advantages of graphical computer output and gives many examples in the fields of business statistics, mathematics and engineering. Hewlett Packard, 1501 Page Mill Rd., Palo Alto, CA 94304. **241**

LITERATURE



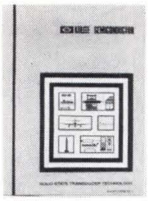
INSTRUMENT MARKETING CATALOG from Leasametric. The 64-page catalog covers three sections: the first contains detailed specification sheets of twelve new DVMs by seven manufacturers; the second covers used Hewlett-Packard and Tektronix equipment that is refurbished and guaranteed by Leasametric's Metricycle Div. It also serves as a "blue-blook" of used prices; while the last section contains rental rates and information on instruments located at the five Leasametric inventory centers. Leasametric, 822 Airport Blvd., Burlingame, CA 94010. **242**

MODULAR OSCILLATORS are described in a new 12-page catalog. Some 18 different models of crystal and tuning-fork controlled oscillators, covering a frequency range of 0.00001 Hz to 40 MHz, are described in detail. Fork Standards, Inc., 205 Main St., W. Chicago, IL 60185. **243**

ACTIVE FILTER FACTS are provided in a 6-page active filter report. It gives the systems engineer data needed for the selection of proper filter characteristics. Plots of phase shift, frequency and step response are provided for 2, 4 and 6-pole lowpass filters with Butterworth, Bessel and Techebyscheff transfer functions. Bandpass and bandreject curves are also covered. Frequency Devices, Inc., 25 Locust St., Haverhill, MA 01830. **244**

SONAR TRANSDUCER CALIBRATION SYSTEMS S-7 from Dranetz Engineering are described in a four-page bulletin. The systems provide transmitting frequency response, receiving response, beam patterns and impedance/admittance plots on underwater transducers. Dranetz Engineering Laboratories, Inc., 2385 S. Clinton Ave., S. Plainfield, N J 07080. **245**

A SERVO CONTROLLER for driving a hydrodynamic actuator in load or position closed-loop servo control is described in a new bulletin. The controller is designed for use with either two-or three-stage servo valves, with signal conditioning for ac and dc transducers. Pegasus Div., Koehring Co., 2890 John R. Rd., Troy, MI 48084. **246**



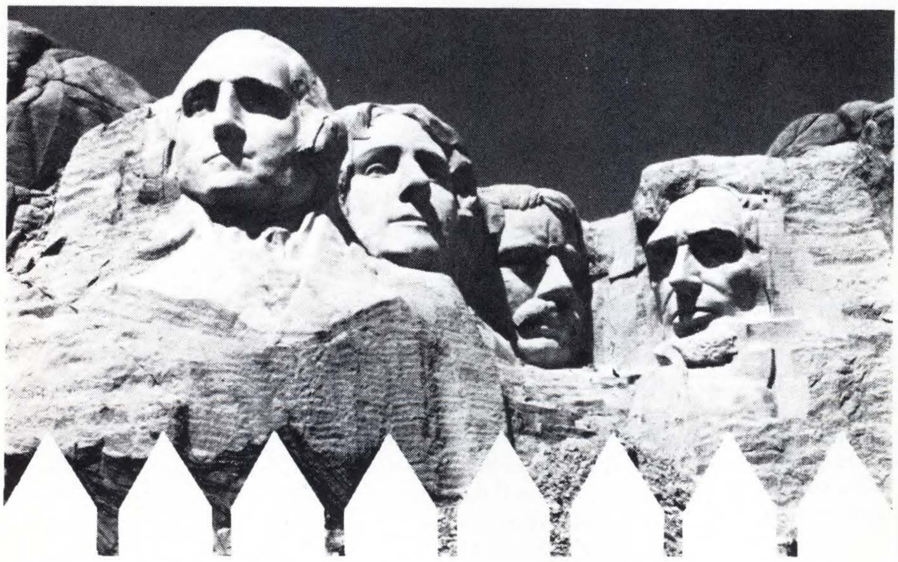
SOLID-STATE TRANSDUCERS are listed in a four-page bulletin. This bulletin describes the principle of operation of these integrated sensor (IS) transducers which are distinguished by their compact size, high output, outstanding dynamic and steady state characteristics and excellent reliability. Kulite Semiconductor Products, Inc., 1039 Hoyt Ave., Ridgefield, N J 07657. **247**

UNIVERSAL CONTROLLER AND DISC SYSTEM—A new eight-page, four color brochure describes the Model 844 universal controller and disc storage system for OEM's and end users. In addition, the brochure describes the design and applications of the new Model 844 and contains a descriptive specification sheet for different disc drives available with the new controller. Cherry Hill Industrial Park, Cherry Hill, N J 08003. **248**

RF LOADS AND WATTMETERS are shown in a new 4-page short-form catalog. The catalog lists all standard and a dozen new coaxial load resistors, absorption wattmeters, directional wattmeters, rf attenuators and coax switches. Bird Electronic Corp., 30303 Aurora Rd., Cleveland, OH 44139. **262**

16-PAGE TRIPLETT TEST-EQUIPMENT CATALOG features the newest digital and FET VOMs, accessories, instrument kits and a VOM selector chart. It includes hand-size portables and general multi-purpose VOMs, FET VOMs with micro-power dissipation, low-power ohms and auto-polarity features. Triplett Corp., Bluffton, OH 45817. **263**

PRECISION ELECTRONIC TEST EQUIPMENT from Rohde and Schwarz are detailed in a short-form catalog. It contains a selection of automated and programmable equipment which includes power, sweep, noise, AM/FM-synthesized and programmable signal generators, precision terminations, fixed-variable and programmable attenuators. Rohde and Schwarz Sales Co. (USA) Inc., 111 Lexington Ave., Passaic, NJ 07055. **264**



ADVERTISER'S INDEX

APPLICATION NOTES

"OPTICAL TECHNIQUES FOR MEASURING FLATNESS" is a FREE 15-page booklet covering the theory of light-wave interference and the use of optical flats. The contact method and two non-contact methods of interference testing are covered along with 3 pages of typical interference patterns and their interpretations. Edmund Scientific Co., Barrington, N J 08007. **249**

24 PAGE APPLICATION MANUAL FOR REED SWITCHES. Included are the operation of magnetic reed switches with permanent magnets and electromagnetic actuation. Physical dimension data, arc suppression and other considerations follow. Contact materials and reasons for each are covered. Last part of brochure includes nearly four pages of explanation of terms and definitions. Ask for Bulletin E00010. Hamlin, Inc., Lake Mills, WI 53551. **250**

APP NOTE SIMPLIFIES OP-AMP NOISE CALCULATIONS. A six-page note simplifies the computation of total equivalent input noise for operational amplifiers. Several examples of the use of the formula are given by its application to the SSS725, a low-noise, low-drift op amp. Also presented is a discussion of the effects of power supply noise and type of frequency compensation used. Precision Monolithics, Inc., 1500 Space Park Dr., Santa Clara, CA 95050. **251**

LSI DESIGN SYSTEM. A 12-page brochure describes the MD-170 "FEDIS" LSI design system. It discusses the need for a modern LSI design system and the "make or buy" alternatives. Complete with photos and charts, it describes the MD-170 operation in detail. Also, four pages are devoted to the "CADIS" software programs that—together with "FEDIS"—provide the designer with a unique and virtually error-free system for checking his LSI designs. Macrodata Co., 20440 Corisco St., Chatsworth, CA 91311. **252**

APPLICATIONS BULLETIN DESCRIBES MAGNETIC DIODES, magnetic-sensitive semiconductor devices, which change their internal resistance as a function of an external magnetic field. By altering the magnetic field, electrical signals may be obtained which allow the conversion of non-electrical into electrical quantities. European Electronic Products Corp., 10180 W. Jefferson Blvd., Culver City, CA 90230. **253**

ANALOG SWITCH APPLICATION NOTES, an 8-page bulletin, No. A004, includes a detailed description of circuit operation and applications of analog switches, with particular emphasis on the utilization of a "compensating FET" to obtain effective $R_{DS(ON)}$ as low as 5Ω. Other sections include a discussion of interfacing the switches with +5V logic, or with +15V open-collector logic. Intersil, 10900 N. Tantau Ave., Cupertino, CA 95014. **254**

N/C NEWSLETTER. Three N/C case-history applications, a look at the use of encoders vs. resolvers, and a discussion of trends in N/C for nonmetalworking applications are among the subjects covered in the Spring 1972 issue of N/C INTERFACE. A special two-page "N/C Application Guide" is included in each issue. Allen-Bradley Co., Systems Div., 747 Alpha Dr., Highland Heights, OH 44143. **255**

GUIDE TO SMALL BUSINESS COMPUTERS. The AUERBACH GUIDE TO SMALL BUSINESS COMPUTERS is addressed to small businessmen who are taking a first look at computers and are trying to relate the capabilities of the many available systems to the actual needs of their daily operations. The guide presents reports and charts that ease the small business computer evaluation and selection task. 139 pages, $19.95. Auerbach, 121 N. Broad St., Philadelphia, PA 19107. **256**

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