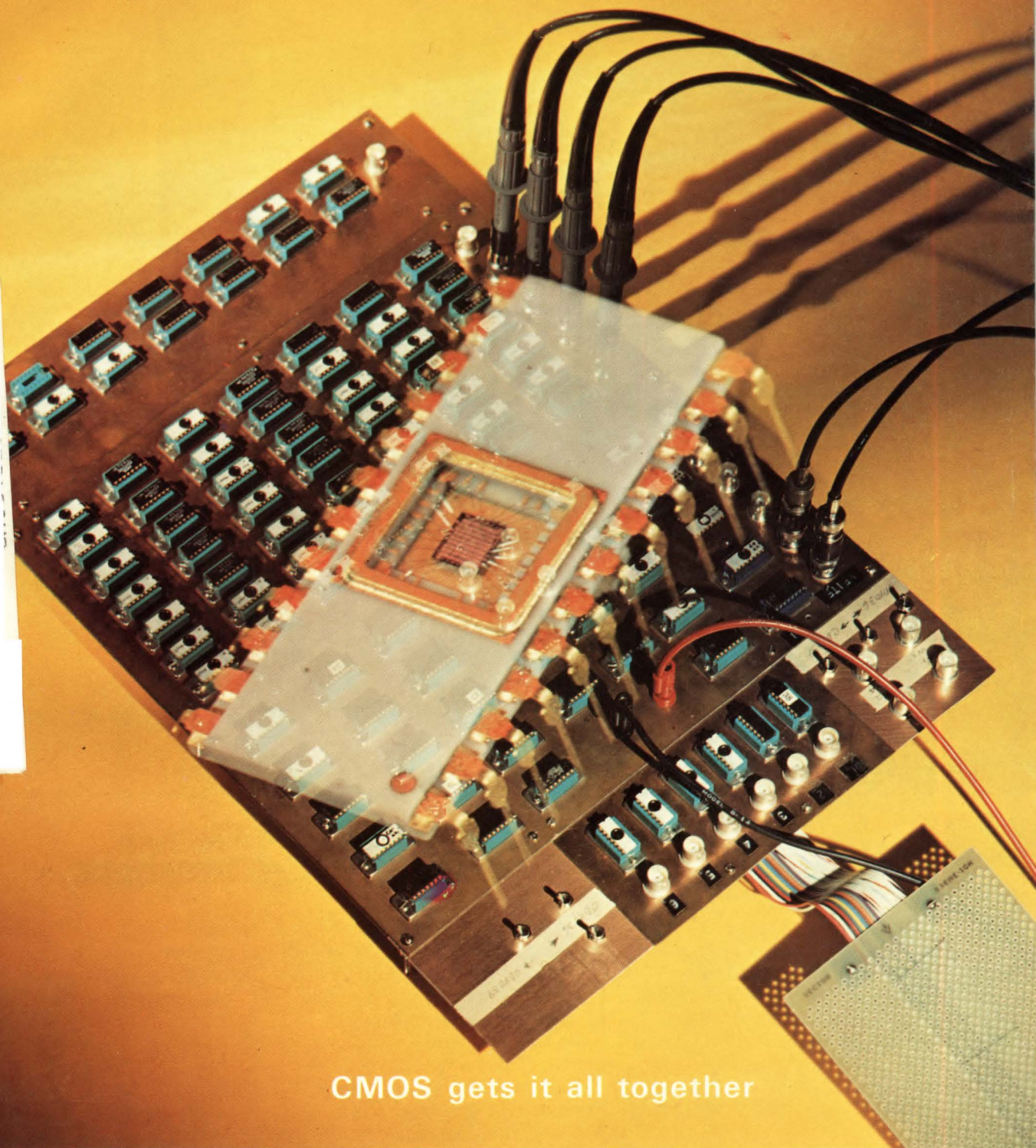


EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

EDN

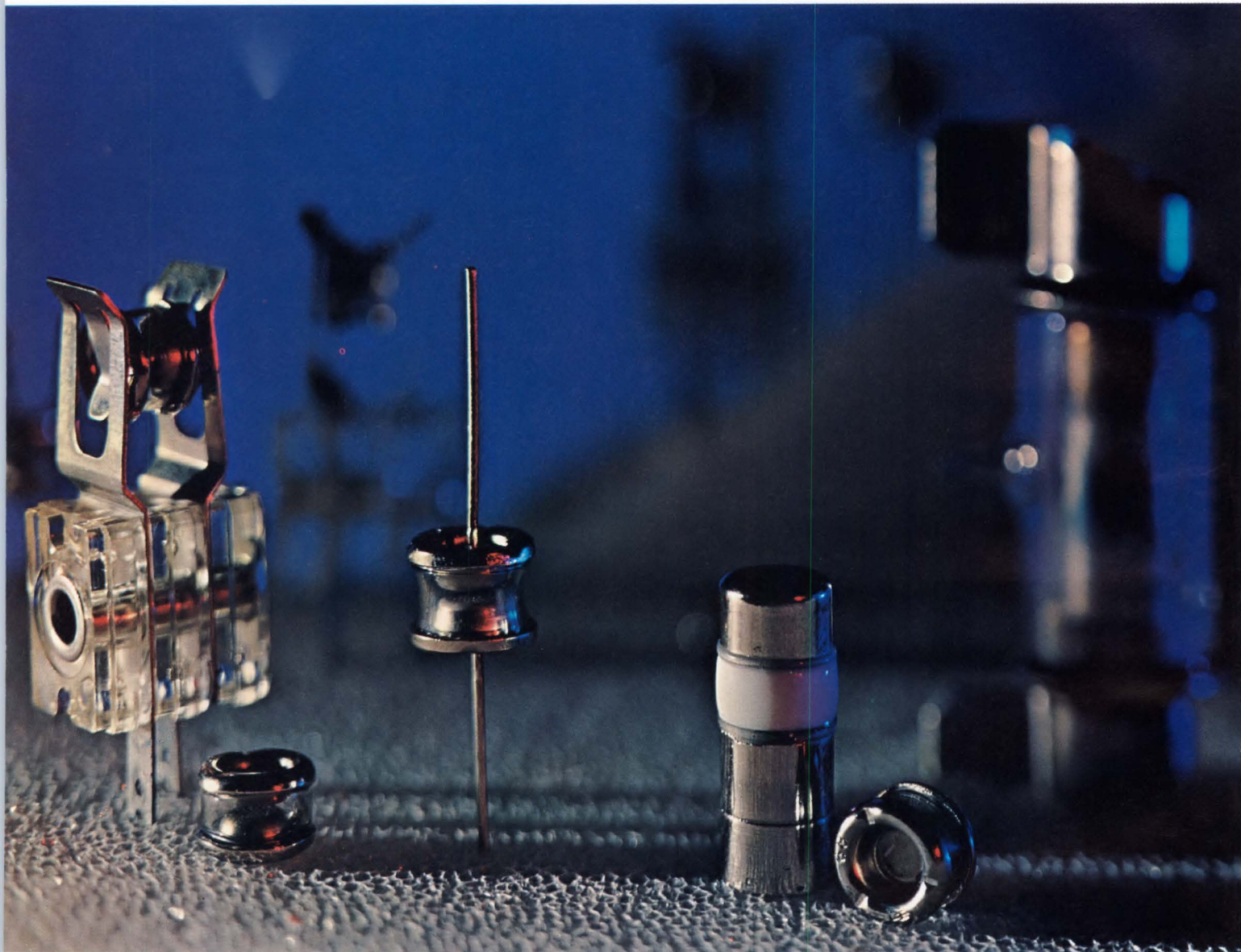
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transmission error checks

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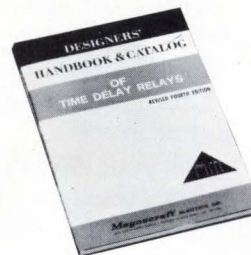
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CIRCLE NO. 2

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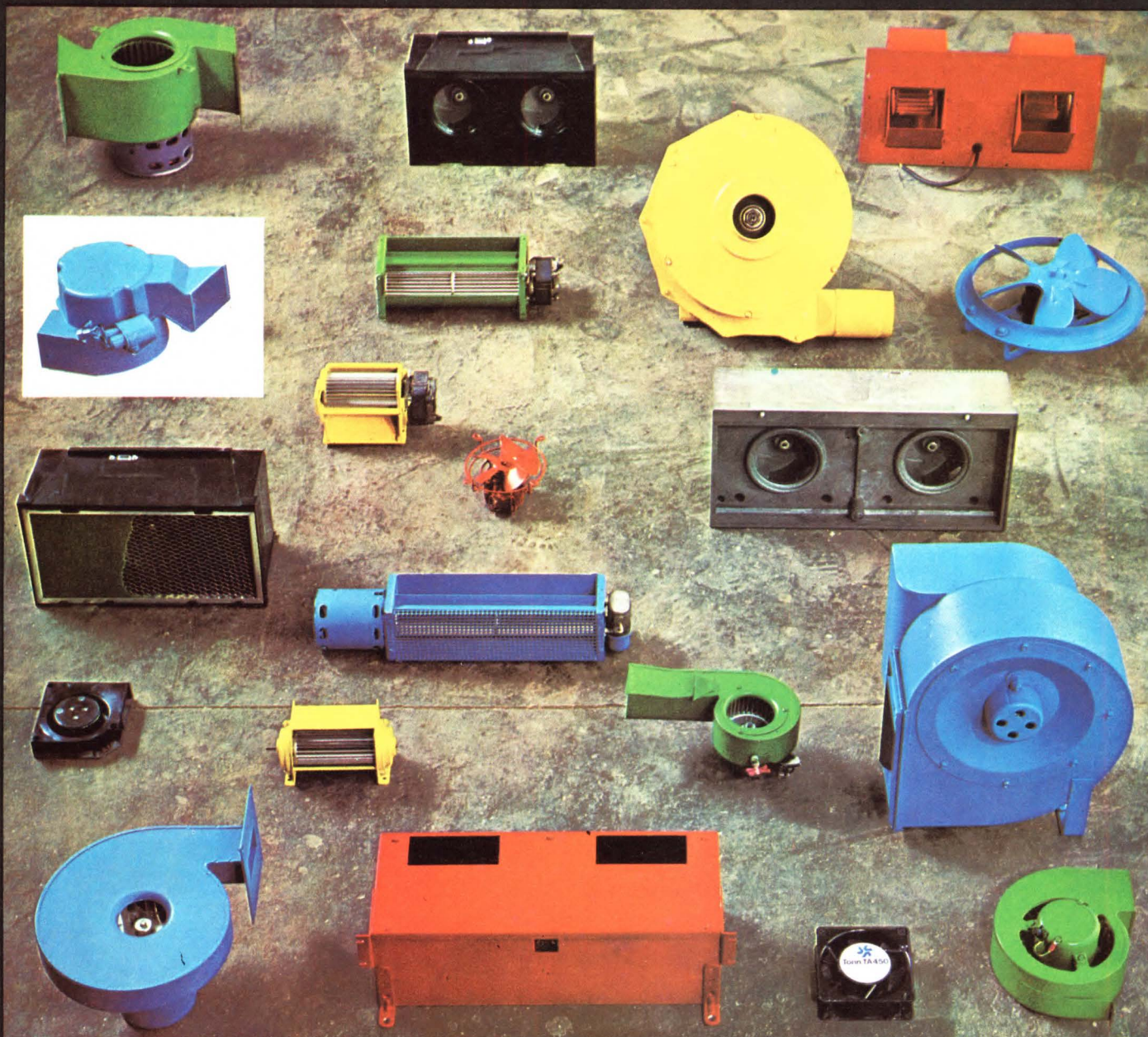
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for your
competitor.
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for you.**

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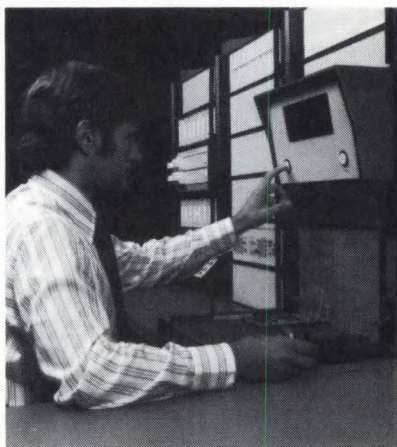
Teradyne's L100 Automatic Circuit Board Test System speaks for itself.

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<pre> MT44 D8 THIS TEST PASSED MTEST ON PINS: M LIMIT :+ 500. MV ACTUAL:+ 248. MV </pre>	<pre> TT39 THIS TEST FAILED TIME FROM PIN 18 TO 21 ACTUAL: 00.195 US TMIN: 00.050 US TMAX: 00.190 US </pre>
<pre> FT35 THIS TEST FAILED <ALARMS>51 FAILING PINS: 20 Z K </pre>	<pre> FT15 THIS TEST FAILED FAILING PINS: S R P N M L J </pre>

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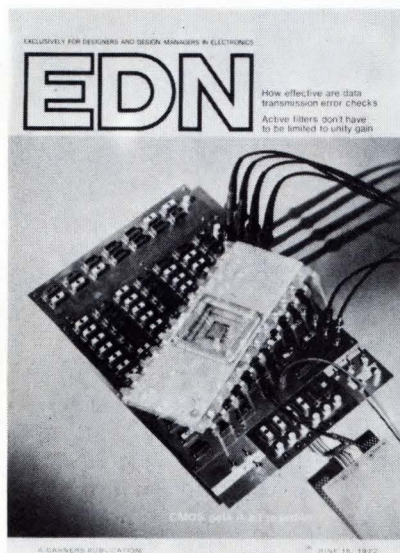


CIRCLE NO. 5

JUNE 15, 1972
VOLUME 17, NUMBER 12

EDN WITH **EEE**

EXCLUSIVELY FOR DESIGNERS AND
DESIGN MANAGERS IN ELECTRONICS



COVER

CMOS circuits like these COSMOS devices of RCA are being used more and more by design engineers. To find out why, see the story on page 28.

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Now designers can begin to trust CMOS. It has the second sources of supply, the steadily-expanding MSI, and a solid promise of lower cost.

Design Butterworth or Chebyshev active filters with gain 40
Gain is often desirable in active filters. Now you can program gain and frequency performance without resorting to a separate amplifier stage.

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CIRCLE NO. 7



Do you read your company's ads?

Did you ever look at an advertisement and not have the foggiest idea as to what is being advertised? Chances are you have. And chances are equally good that you didn't spend much time trying to find out. You just moved on to the next page of whatever it was you were reading.

Sometimes, unfortunately, we don't have this freedom of action. As, for example, when the editors of EDN prepare the product index that appears in each issue. Part of this preparation involves looking at each ad and classifying it according to product category.

You would think that this should be an easy task, and in most cases it is. A glance at or brief scanning of the ad clearly shows the products or services being offered. In some instances, though, and these are not infrequent, all you know after scanning the ad is that something "super-fast" or "extremely-versatile" or "low-in-price" is being featured. The item itself is buried deep within the copy. It's almost as if the manufacturer were either ashamed of the product, or considered it so good that he didn't want just anyone to know about it.

In some cases, and this may be hard to believe unless you are an extremely avid ad reader, even after a complete reading you can't be 100 percent sure of what the item is.

You're probably wondering why we even bring up this subject. If a manufacturer wants to use impenetrable ads, it's his prerogative. Readers will bypass the ads and not buy the company's products. But since no one has a true monopoly these days, similar products are available from others to supply everyone's needs.

What if, though, such ads are used by your company. They affect you in a very direct way. You helped design those products, and if they don't sell, it will have a bearing on your livelihood. So if you don't do it already, start reading your own company's ads. They're aimed at engineers, just like you, so read them in the same way you read everyone else's. But if you find them foggy, or confusing or incomplete, don't just move on to the next page. Tell someone in your marketing department. You may be considered a crank. But on the other hand, you may have a very positive effect on your company's sales.

Frank Egan

Editor



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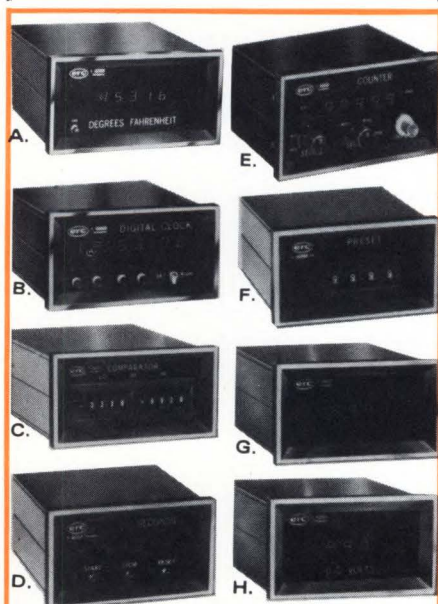
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CIRCLE NO. 8

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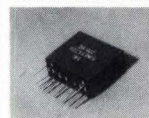
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Ladder Networks

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814 (Binary)	10K	5Ω Bits 1-5	$\pm 30\text{ ppm @ } +25^\circ\text{C and } +61\text{ ppm } -20^\circ\text{C to } +85^\circ\text{C}$	814-D14 90.00
815 (Binary)	10K	None	$\pm 1952\text{ ppm } -55^\circ\text{C to } +125^\circ\text{C}$	815 6.95
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823	10 – 30V	$\pm 26V$	$\frac{30(E_o \text{ max.})}{E_{cc} - E_o \text{ max.} - 1}$	8.95
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CIRCLE NO. 10

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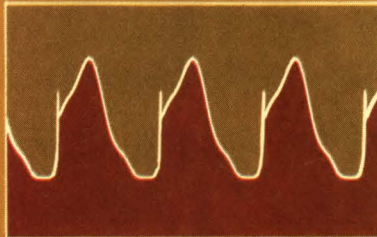
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These new Fluke plug-in options let you add true rms capability to Fluke 8200A and 8400A DVMs. Take the measure of non-sinusoidal waveforms in 500 ms. Get accurate readings from 1 mv to 1000V rms.



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auto ranging on all functions. It features switched input filter, full 1000 volt guarding. Full multimeter and systems options are available. Base price is \$995.

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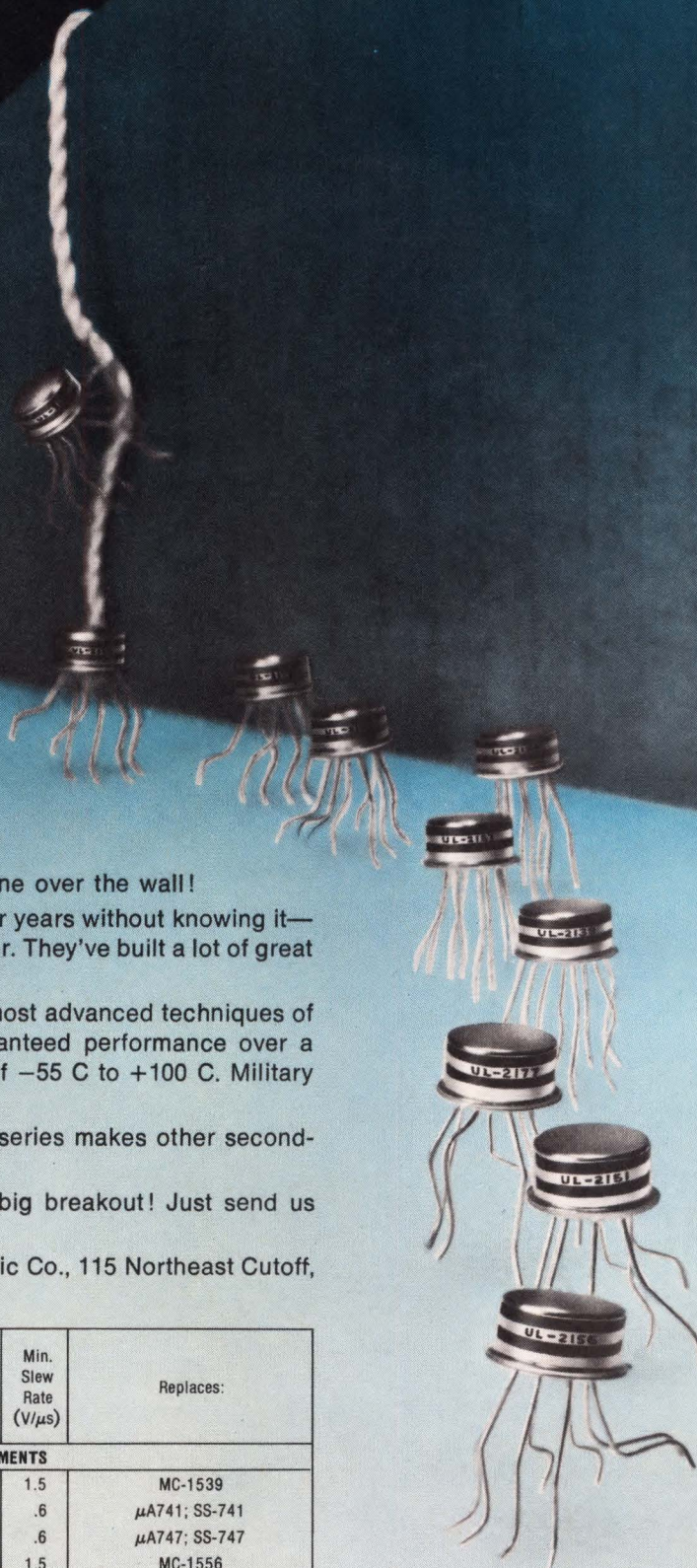
Both DVMs feature 1500V peak overload protection and the ability to meet tough environmental specs.

For full details, call your nearby Fluke sales engineer or contact us directly.

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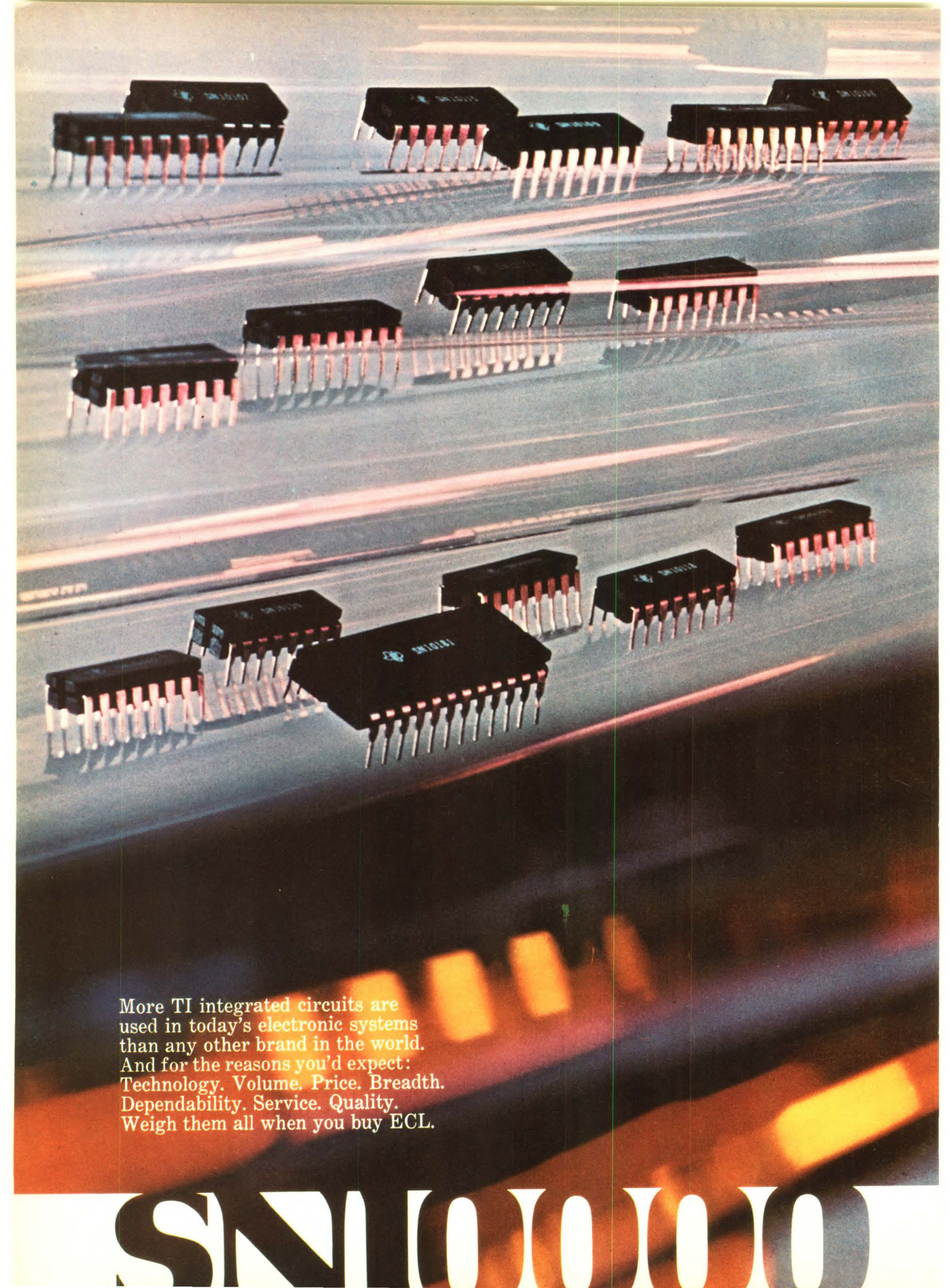
Sprague Series ULS		Max. Input Offset Voltage (mV)	Max. Input Bias Current (nA)	Max. Input Offset Current (nA)	Min. Gain (dB)	Min. Slew Rate (V/ μs)	Replaces:
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IMPROVED PIN-FOR-PIN REPLACEMENTS							
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2151	—	2	50	5	94	.6	$\mu\text{A}741$; SS-741
2157*	—	2	50	5	94	.6	$\mu\text{A}747$; SS-747
2156†	—	4	15	2	100	1.5	MC-1556
—	2158	2	50	5	94	.6	$\mu\text{A}748$; SS-748
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2173	2174	2	3	1.5	100	.25	Similar to SG-118/LM-108, SG-108
2175	2176	2	3	1.5	100	1	Similar to MC-1556, SN-52771/SN-52770
2177	2178*	2	.6	.3	100	.25	Similar to SG-118A/LM-108A, SG-108A

*Dual

† -25 to $+100^{\circ}\text{C}$

SPRAGUE
THE MARK OF RELIABILITY

Analog Products for Signal Processing

A photograph of several Texas Instruments integrated circuits (chips) mounted on a printed circuit board. The chips are black with gold pins. The background is a blurred, warm-toned image of a circuit board with glowing traces. The text is in the lower-left corner, and the large 'SN' logo is at the bottom.

More TI integrated circuits are
used in today's electronic systems
than any other brand in the world.
And for the reasons you'd expect:
Technology. Volume. Price. Breadth.
Dependability. Service. Quality.
Weigh them all when you buy ECL.

SN

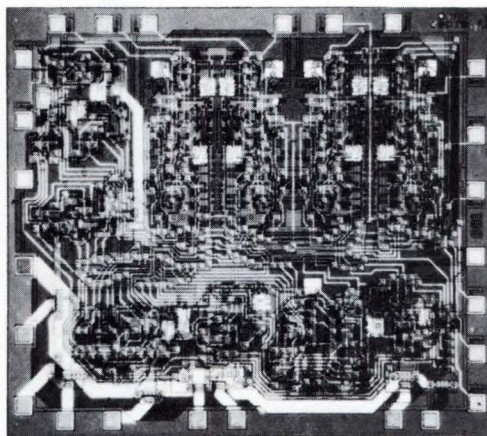
TI announces a new standard line of high-speed, low-power ECL: 2 ns at 25 mW SN10000.

To its capabilities as the major supplier of custom ECL circuits, TI has added a broad new standard family. Series SN10000.

Now, in weighing the long-range pros and cons of designing with emitter-coupled logic, you can add the assurance of TI's technological development and volume-production capability.

TI can deliver now — including MSI

All SN10000 devices listed below are immediately available in evaluation quantities through authorized TI distributors or direct from factory inventories. All are in ceramic dual-inline packages — including the 24-pin ALU circuit — and are pin-for-pin equivalents to the MECL 10,000 series over the 0° to 75°C temperature range. Production quantities can be delivered 6 to 10 weeks after receipt of order.



SN10181 ALU . . . 75 equivalent gates.

nal reference generator which relaxes power supply tolerances and power distribution requirements — thereby reducing overall system costs.

Economical system design

In addition to power supply savings, you can achieve many other important design economies with Series SN10000.

Special PC boards are not required. Switching rise and fall times are slow enough so that conventional, two-sided boards can be used.

Savings in gate and package count are significant because the open emitter outputs and high impedance inputs permit wire-ORing of several gating levels. Data "bussing" and two-way data transfer are also possible with the open emitter outputs, which further make possible great flexibility in terminating schemes and logic interconnects.

Still more reductions in system gate and package count are possible because complementary outputs are readily available from ECL gates.

And now, with the availability of ECL/MSI, you can add the benefits of increased complexity — reduced package count, fewer interconnections, and smaller PC boards. All of which means lower component and system costs per gate.

Much more to come — soon

These devices are only the beginning of a large and complete logic family . . . including memory functions as well as MSI and SSI logic circuits.

Planned, among others, are a quad 2-input AND gate, ECL/TTL level translators, a 12-bit parity checker/generator, an 8-line multiplexer, a quad latch, and a 64 x 1 RAM.

Full specifications available now on all functions

For complete data sheets on TI's Series SN10000, circle 241 on the Reader Service Card. Or write Texas Instruments Incorporated, P. O. Box 5012, M.S. 308, Dallas, Texas 75222.



	DESCRIPTION	100-PIECE PRICE
SN10101	Quad 2-Input OR/NOR Gate (One input common)	1.65
SN10102	Quad 2-Input Gate (3 NOR, 1 OR/NOR)	1.65
SN10103	Quad 2-Input Gate (3 OR, 1 OR/NOR)	1.65
SN10105	Triple OR/NOR Gate (2, 3, 2 inputs)	1.65
SN10106	Triple NOR Gate (4, 3, 3 inputs)	1.65
SN10107	Triple 2-Input Exclusive OR/NOR Gate	2.10
SN10109	Dual OR/NOR Gate (4, 5 inputs)	1.65
SN10115	Quad Line-Receiver	1.65
SN10116	Triple Line-Receiver (Complementary outputs)	1.65
SN10117	Dual 2-Wide 2-3 Input OR-AND/NOR-OR Gate	2.10
SN10118	Dual 2-Wide 3-Input OR-AND Gate	2.10
SN10119	4-Wide 4-3-3-3 Input OR-AND Gate	2.10
SN10130	Dual D-Type Latch	4.45
SN10131	Dual D-Type Master Slave Flip-Flop	5.65
SN10179	Carry Look-Ahead	6.80
SN10181	4-Bit Arithmetic Logic Unit/ Function Generator	20.00

Fast, cool and stable

The new Series SN10000 has a speed/power product of 50 pJ (2 ns at 25 mW per gate). You can take full advantage of the 2-ns speed without cooling problems. What's more, SN10000 offers an improved inter-

TEXAS INSTRUMENTS
INCORPORATED

Ribbon cable breakthrough: crosstalk reduced to under 4%

Flat flexible cabling has come to the fore with the recent invention of a low-crosstalk cable (see Fig. 1). Joseph B. Marshall, engineering director for the Ansley Div. of Thomas & Betts Company, terms his new multi-conductor black-cover cable "Black Magic." It offers a five-fold improvement over conventional flat cable (twisted pairs) in near-end crosstalk and an eight-fold improvement in far-end crosstalk.

Crosstalk is the voltage pulse caused in a quiet signal line when an adjacent line (or lines) is activated. Crosstalk can cause false triggering of logic circuits either at the cable's input (near-end crosstalk) or at its output (far-end crosstalk).

With Schottky clamped TTL and ECL in wide use in high-speed computer systems, performance requirements have become more demanding on the medium carrying these fast logic signals—flat flexible or ribbon cabling. This is especially true with fast-rise-time pulses where crosstalk interference from adjacent signal lines in a cable increases rapidly.

To eliminate crosstalk, flat coaxial cables are generally used. These, however, are more expensive, less flexible and bulkier than flat ribbon cables. In addition, coaxial cables cannot be terminated as easily as can



Fig. 1—Lowest flat flexible cable in crosstalk yet. Designated "Black Magic," it offers better than 5% crosstalk (both far-end and near-end), making it ideal for high-speed-computer interconnections. Note the ease of termination into a multi-conductor PC board with 0.05-in. spacings between conductors. The connectors shown are mounted in adapters for test purposes.

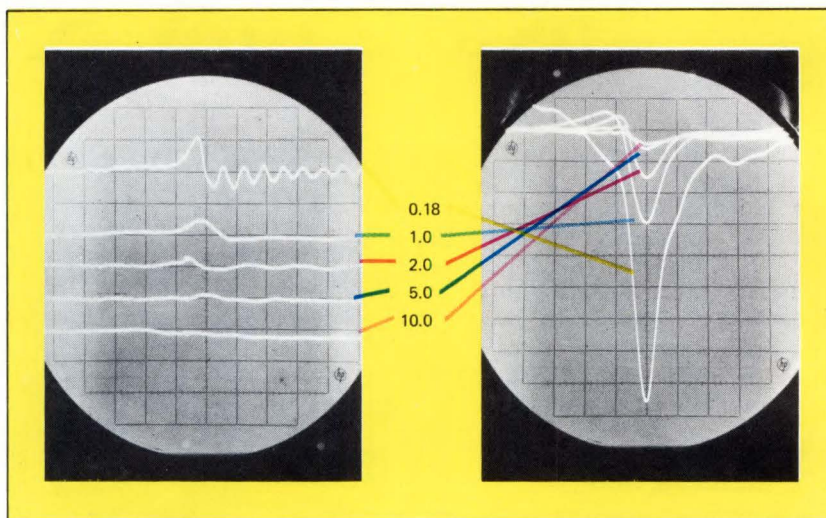


Fig. 2—Comparing crosstalk performances. Photo on left shows oscilloscope crosstalk pulses on a quiet line of a 10-foot "Black Magic" cable for signal risetimes ranging from 0.18 to 10 nsec. The photo on the right shows comparative crosstalk performance of the same length of cable using only a polyethylene core (conventional flat cable construction). Each vertical scale division represents 1% crosstalk. As can be seen, crosstalk is worse at higher frequencies (faster risetimes) and is -8.6% on the conventional cable vs only +1.1% for the "Black Magic" cable for 0.18-nsec risetime signals.

ribbon cables.

The new Black Magic cable is said to offer under 4% crosstalk (see Fig. 2); whereas, most conventional flat cables offer crosstalk performance ranging from 10 to 20%.

In addition, there is only a slight increase in cost over conventional flat flexible cables. For example, a 41-conductor (21 grounds) Black Magic cable (Model PV577-41) costs only 89¢ per foot in 1000-foot quantities. A 21-conductor cable (Model PV715-21) costs 68¢ per foot in the same quantity.

The key to the cable's design is the use of two dielectric mediums—an inner polyethylene cone with a dielectric constant of 2.3 and an outer PVC jacket with a higher dielectric constant of 3.5.

By replacing the traditional outer jacket of air found in conventional flat cables with the PVC jacket, Marshall was able to confine the field of signal electro-magnetic propagation to such

a degree that there was a dramatic improvement in crosstalk.

The attenuation characteristics of the cable were changed very slightly since only 2% of the field propagates within the PVC jacket. At 100 MHz, attenuation is about 1.5 dB per 10 feet.

The use of a PVC outer layer has an additional advantage. It makes the cable flame-retardant, a feature necessary for UL approval, and gives it greater environmental protection for maximum wear.

In the area of traditional computer interconnections, greater uses of this new cable are anticipated, especially where large numbers of multi-conductor cables run atop one another, which can result in severe crosstalk interference.

Marshall also foresees wide use for his new cable in such areas as telephone switching circuits and CATV where coaxial cable has been mostly used. □

Elastomer material holds promise of improving electrical connections

In their search for a low-cost solid-state circuit breaker, researchers at Essex International (a Ft. Wayne, Indiana-based company that manufactures automotive electrical products) have stumbled across a metallo-organic compound with unique properties. The material, which they called Pressex, is a conductive elastomer that conducts electrical current only when compressed. Release of pressure causes it to act as an insulator, even though it is in contact with a live electrical source. The material is not a transducer and is non-linear (see Fig. 1).

Depending on the formulation (it is available in over 100 to date; see Fig. 2) Pressex is said to have three important functional properties: it can act as a switch, as a connector and as a possible overload device or resettable circuit breaker—a property not yet fully understood.

According to company spokesmen, who would not divulge the physical molecular theory of Pressex's charac-

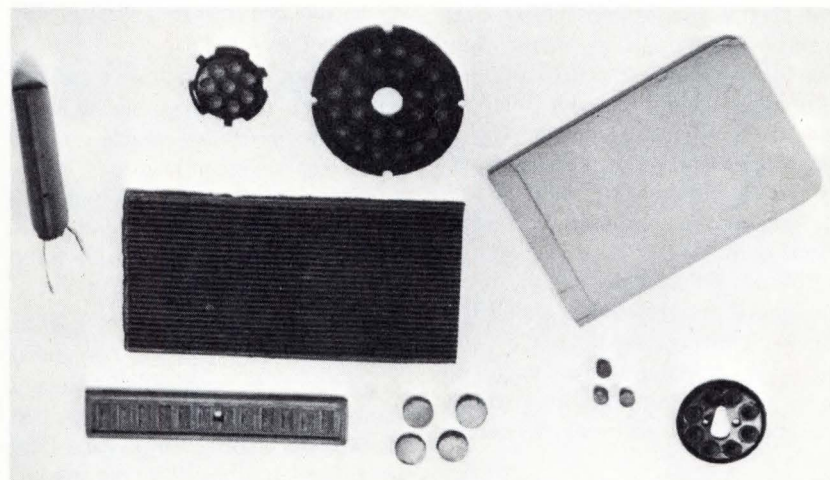


Fig. 2—Various forms of Pressex are available. The new metallo-organic conductive elastomer conducts electric currents only when compressed. Conductivity and activation characteristics depend on material formulation, which can be cast, molded or die cut to nearly any desired shape. It can be made to be spongy, rubber-like, flexible or semi-rigid.

teristics, the material activation distance is a function of formulation.

Several advantages of this new material are claimed over conventional metal conductors. Because it may be

produced in several forms, it can be formulated to meet many specific applications. And because the new material is an elastomer, it provides many more current-carrying paths than metal conductors, thereby lowering the voltage drop in the conduction path and increasing conductor reliability.

Essex officials foresee Pressex's use largely in automobiles, although by no means exclusively. Its application as a switch for lights, gauges, horns, power windows and seats and doorlocks is being forecast, and may be seen in some 1973 automobiles.

When used as a switch, tradeoffs must be made between required activation pressure, travel characteristics (the distance Pressex has to be compressed for activation) and conductivity. The pressure range available at present is said to span 1 oz to 100 lbs of force. Travel characteristics range from 0.001 to 0.125 in. As for conductivity, Pressex ranges from milliohms in the compressed (ON) state to megohms in the free (OFF) state.

There are some limitations, however. Pressex can switch any load (including inductive ones) at voltages only up to 32V. The load capability must be reduced for switching above 32V.

Essex International has made standardized Pressex discs that are available for test purposes. □

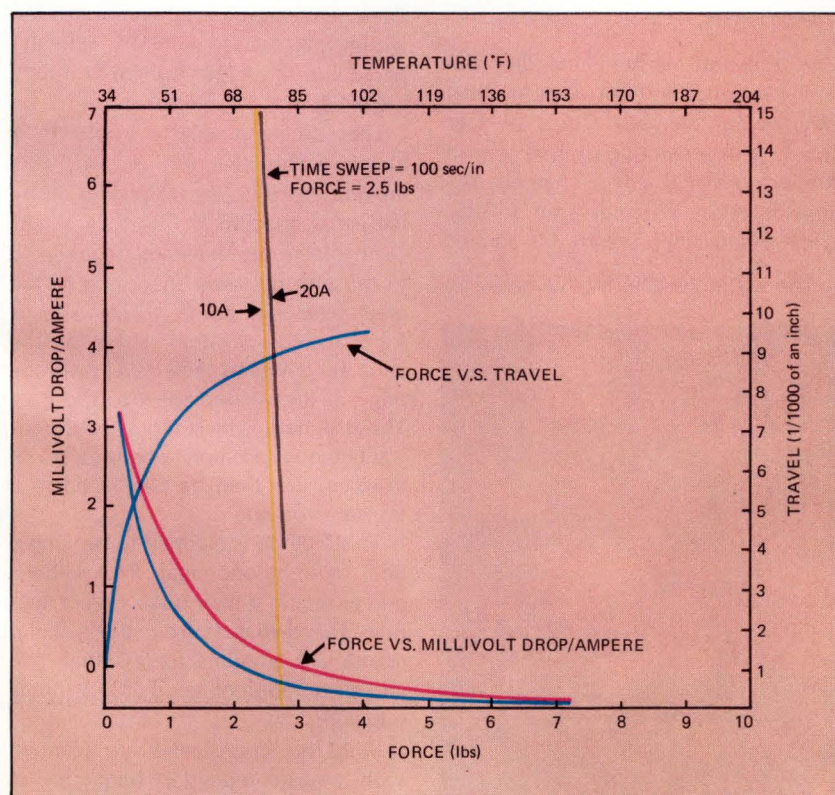


Fig. 1—Characteristics of Pressex as a current-carrying conductor are shown here. Note that the millivolt drop/ampere as a function of force is a square-law function, giving the new conductor material the advantage of positive turn-on and turn-off characteristics.

Acoustic systems allow handwritten data to be sent on phone lines

Two new techniques for transmitting and receiving handwritten graphic and alphanumeric information over ordinary telephone lines in real time have emerged recently. Both of these techniques employ acoustic methods for data sensing and one (see Fig. 1) reconstructs and projects the transmitted digital information onto a large viewing screen, forming a remote blackboard.

The projection technique is an experimental one developed at Bell Telephone Laboratories. It uses a commercially available transmitting pen that is attached to the writing or drawing implement (can be chalk, pen or pencil).

The transmitter is a spark-gap generator that emits a series of 150-kHz pulses as it is moved over the writing surface of a tablet, which is bounded by two microphones. These pinpoint the location of the writing instrument by sensing the pulses and feeding them to a digitizing data set for transmission over telephone lines.

A second data set at the receiving end translates the incoming signals back into pulses to drive two rotating mirrors mounted on a galvanometer. These receive a laser beam from a 3250A UV laser and deflect the laser's beam onto a photosensitive film which is finally projected on a wall or large screen.

The projected film is in step with the handwriting or drawing going on at the transmitting end. This film can

be projected onto any size surface (the projection device is the only limiting factor) and can also be stored for future viewing.

According to Dr. Blake McDowell of Bell Labs, this system can be combined with the 50A portable conference telephone recently introduced by the Bell System to transmit simultaneously both audio as well as video information to classrooms, lecture halls and conference rooms.

Resolution of the system is said to be about 10 bits (1024×1024 points) on a 14×14 in. writing tablet. Recent improvements in the transmitting pen (science Accessories Corp's Graf Pen) are making possible 12-bit resolution.

One major problem that had to be overcome during the designing of the projection system was the poor video quality obtained by using conventional capacitor-type microphones as the pickup heads on the tablet. These microphones have high signal-to-noise ratios. The use of electret-type microphones with superior signal-to-noise characteristics has solved this problem.

A different method for digitizing alphanumerics and drawings has been devised by Siemens Corp. of Germany. The technique utilizes a well-known physical effect, namely that piezoelectric materials emit an electrical signal when pressure is applied.

The writing pad in the Siemens sys-

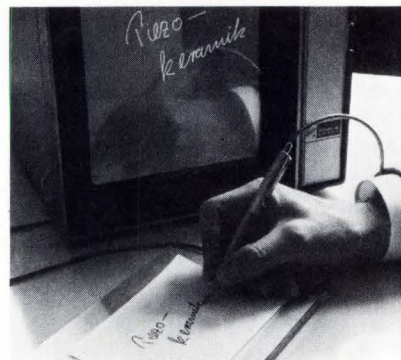


Fig. 2—This Siemens system uses a piezoceramic sheet and a receiving pen that capacitively picks off a moving piezo voltage caused by ultrasonic waves from generators located at the tablet's edges. It is said to offer 0.2-mm resolution and allows alphanumeric and graphic data transmission over telephone lines.

tem (see Fig. 2) is a thin piezoceramic sheet. Unlike the Bell system, the pressure of the pen on the writing pad is not, in itself, used for determining its position. Instead, ultrasonic pulses with a pulse repetition frequency of 500 Hz are generated alternately at the two edges of the writing pad. These acoustic pulses travel across the writing pad with a constant velocity, parallel to the edges from which they are emitted.

They create a voltage front which travels across the writing pad. This moving piezo voltage is picked off by the pens capacitively.

An electronic evaluator, connected to the piezoceramic sheet and to the electronic ball-point forms signals from the propagation times of the acoustic pulses as they travel from the edge of the writing sheet to the pen. These signals, which represent the instantaneous position coordinates of the pen, can then be passed on to a transmission line.

This method is claimed to be simple and more economical than others, and produces a high-quality reproduction. The deviation from the original coordinate amounts to less than 1% and a resolution of less than 0.2 mm is possible.

Since the coordinates are scanned with a pulse repetition frequency of 500 Hz, rapid pen movements (e.g. when somebody is signing a document) can be retransmitted exactly. □

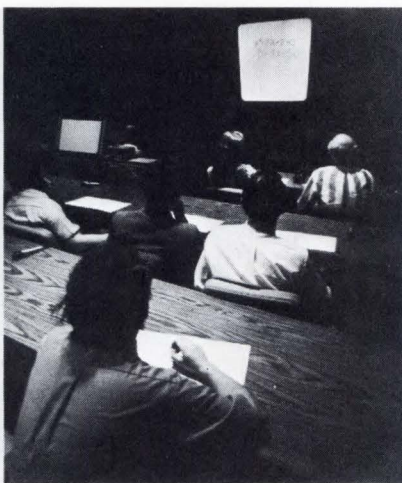
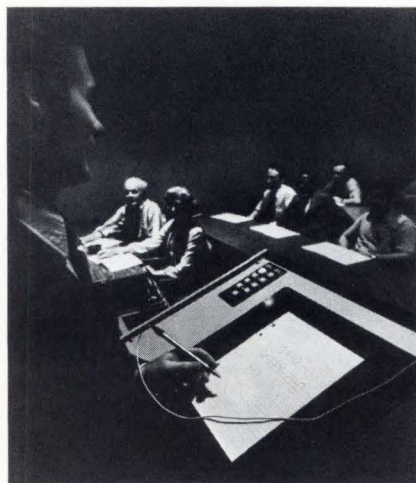
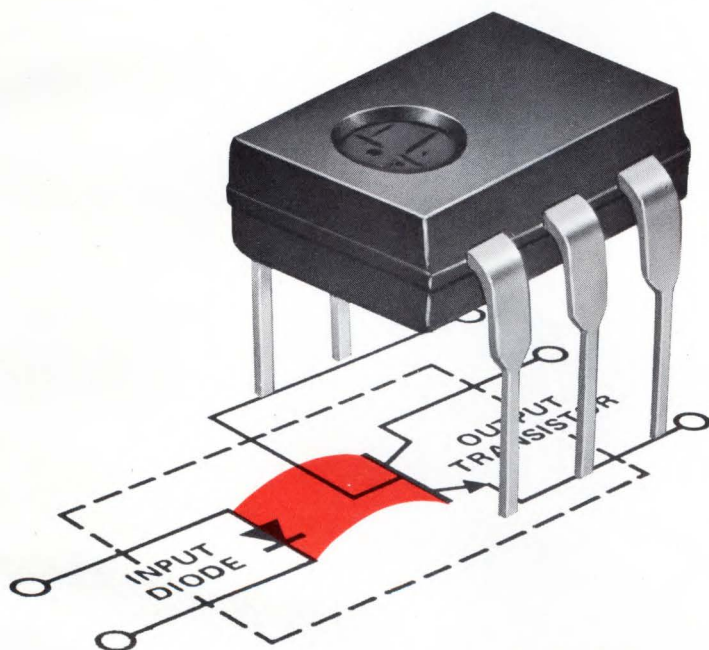


Fig. 1—Algebraic equation is translated into ultrasonic pulses (left) and sent via telephone lines over long distances and projected in real time (right). The Bell developed system can transmit and project alphanumerics and graphics with up to 12-bit resolution.

THE MAGIC COUPLER



Of more than 20,000,000
phototransistors produced by Fairchild MOD,
four million have been used
in optical couplers.

Take a light emitting diode chip. Mount it facing a light sensitive semiconductor detector. Package these two chips in a case with input and output leads. The result is probably the most versatile solid state device available, literally a sub-system that:

- Switches on and off with a speed in the low microsecond range and faster.
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- Relays information from DC to hundreds of KHz.
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- Provides unidirectional operation, with no feedback to the input.
- Interfaces such circuit devices as transistors and integrated circuits.
- Interfaces memory - CPU - I/O Logic.

WHAT IT DOESN'T DO IS ALSO INTERESTING.

For example, it:

- Has no moving parts, no contacts to bounce or arc or erode.
- Is unaffected by magnetic fields.
- Doesn't take up much space, being about 1/3" X 1/4" X 1/3".
- Has no known failure modes to make it fail in our lifetime.
- Doesn't require much current for operation, only a few mA.
- Doesn't cost much. Economical. In fact, downright practical.

The World Beaters	Current Transfer Ratio - % (Typ)	Breakdown Voltage - V Input to Output	Description
FCD 810	25	750	Lowest cost
FCD 811	50	2500	Highest Voltage Plastic DIP
FCD 820	50	1500	The Standard

This device has been called a solid state relay, coupler, isolator and transformer. But think of it simply as the answer to many problems, whether you are in the electronics, control or processing industries; whether you are designing medical instrumentation, processing equipment, transportation systems, etc.

Data sheets describing the characteristics of these remarkable devices and how they operate are yours for the asking from your local Fairchild semiconductor sales engineer. Your stocking Fairchild semiconductor distributor can provide immediate product delivery.

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**The new P&B
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is more than
just a pretty face.**



Our PT times with accurate solid state circuitry...switches with rugged relays. It's the best of both worlds. And it's available now from authorized P&B distributors.

A pretty face? Yes, indeed. But you get more, much more in our new PT Series panel mount time delay. For example:

- Solid state precision plus hard-contact electrical isolation.
- 10-ampere switching capacity.
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- Choice of three timing modes: delay on operate, delay on release, delay on operate with both timed and instantaneous contacts.

- The accuracy, dependability and longevity associated only with solid state circuitry.

Standard models, stocked by leading electronic parts distributors, are available for 24 and 120 volts AC or 12, 24, 48, and 110 volts DC operation. They have a 3-inch diameter Lexan housing designed to be interchangeable with most mechanical timers.

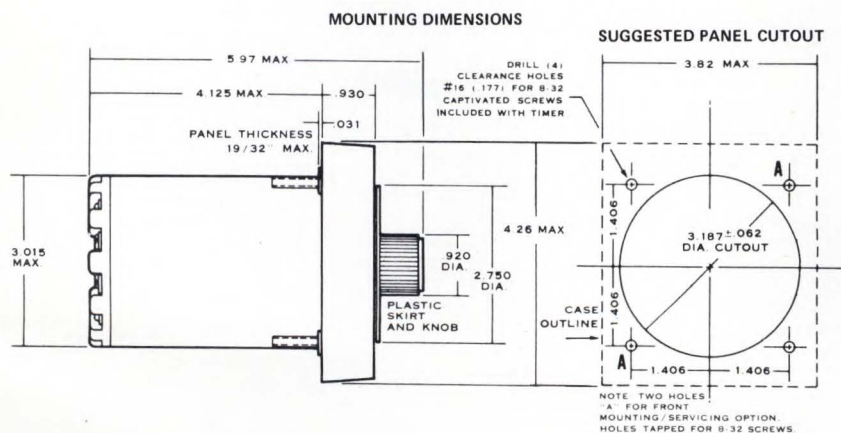
Timing function lights on the face of the PT are available options. A red light indicates timing is being performed and a white light shows tim-

ing has been completed. These lights are available on 110 VDC and 120 VAC models.

The dial is calibrated in seconds and is accurate to within 10% of the full scale. Repeatability is $\pm 1\%$. Typical release time is 45 milliseconds. DC models have polarity protection and AC models withstand transients up to 1000 volts.

Modern in appearance and concept, the panel-mount PT adjustable time delay can add new precision and reliability to your equipment economically.

For full information, call your local P&B representative or write Potter & Brumfield Division of AMF Incorporated, Princeton, Indiana 47670. Telephone 812 385-5251. In Europe, AMF International Limited, Oxford, Oxon, England or S.p.A. Milan, Italy.



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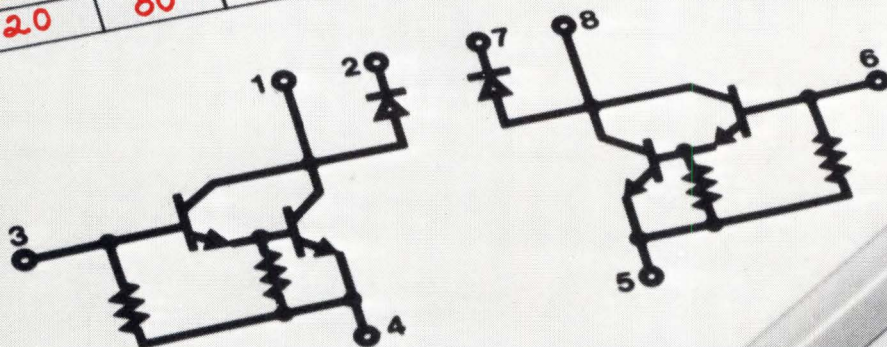
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CIRCLE NO. 15



C-LINE DUAL DARLINGTONS

Type	P _D W	V _{CEO} V	h _{FE}	V _{CE(sat)} V	t _{on} μs	t _{off} μs	Package	Price (100- 999)
PIC500	30	100	2000	1.5	0.55	2.0	T0-3 (8-pin)	\$10.00
PIC501	20	100	1000	2.0	0.65	3.6		6.50
PIC502	20	80	750	2.0	0.65	3.6		4.90

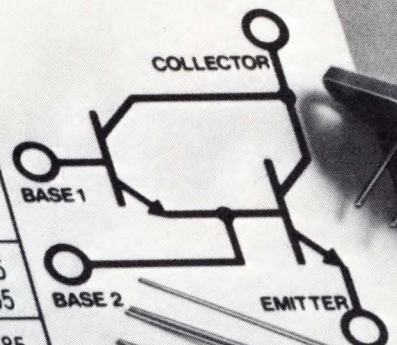


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C-LINE POWER DARLINGTONS

Peak I_c A	Type	Package	V_{CE} V	h_{FE}	$V_{CE(sat)}$ V	t_{on} ns	Price (100- 999)
5	NPN	U2T301 TO-33	60	1000 @ 2A	1.5 @ 2A	300	\$1.25
		U2T401 TO-66					1.50
		U2T305 TO-33	150	1000 @ 2A	2.5 @ 2A	400	1.80
		U2T405 TO-66					2.10
	10	U2T101 TO-33	80	2000 @ 5A	1.5 @ 5A	400	2.25
		U2T201 TO-66					2.55
		U2T105 TO-33	150	1000 @ 5A	2.5 @ 5A	500	2.85
		U2T205 TO-66					3.15
	20	U2T501 TO-66	80	2000 @ 10A	1.5 @ 10A	400	4.30
		U2T601 TO-3					4.30
		U2T505 TO-66	150	1000 @ 10A	2.5 @ 10A	500	5.40
		U2T605 TO-3					5.40
10	NPN	U2T351 TO-33	60	1000 @ 2A	2.0 @ 2A	250	1.50
		U2T451 TO-66					1.80
		U2T355 TO-33	120	1000 @ 2A	2.5 @ 2A	300	2.16
		U2T455 TO-66					2.52
	10	U2T151 TO-33	80	2000 @ 5A	2.5 @ 5A	300	2.70
		U2T251 TO-66					3.06
		U2T155 TO-33	120	1000 @ 5A	3.0 @ 5A	400	3.44
		U2T255 TO-66					3.78
	20						



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Because you can use our high-speed automated terminated machines instead of manual methods. And you have fewer parts to put together because of our one-piece connector housing construction. No need for heat-shrink sleeves; egg-crated cavities in the housing give you the insulation you need.

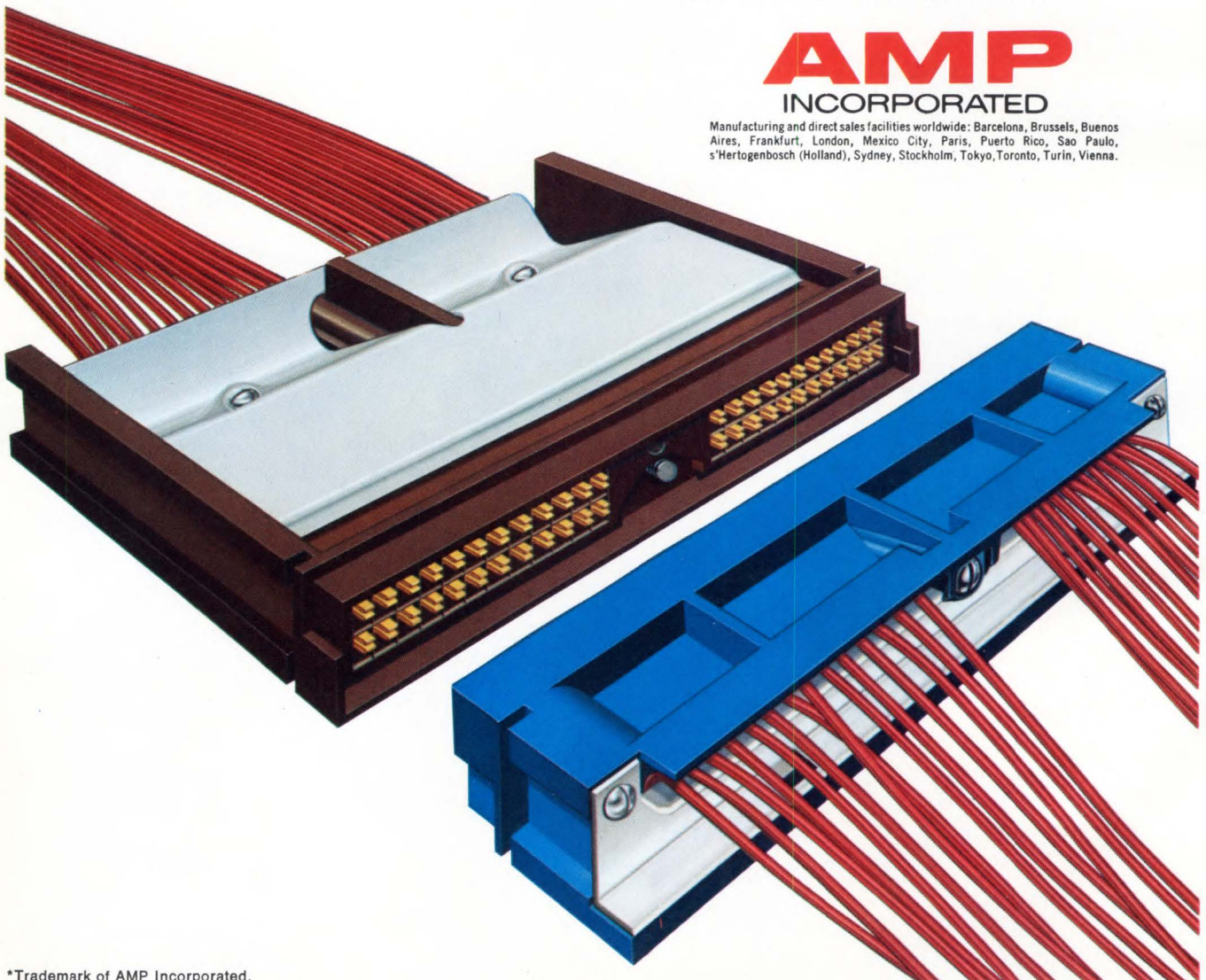
And lest we forget, the AMPLIMATE connector not only mates with itself, but also with a 48-position hermaphroditic connector widely used in the computer industry.

Get the facts on getting together, by writing:

AMP Incorporated,
Industrial Division, Harrisburg, Pa. 17105.

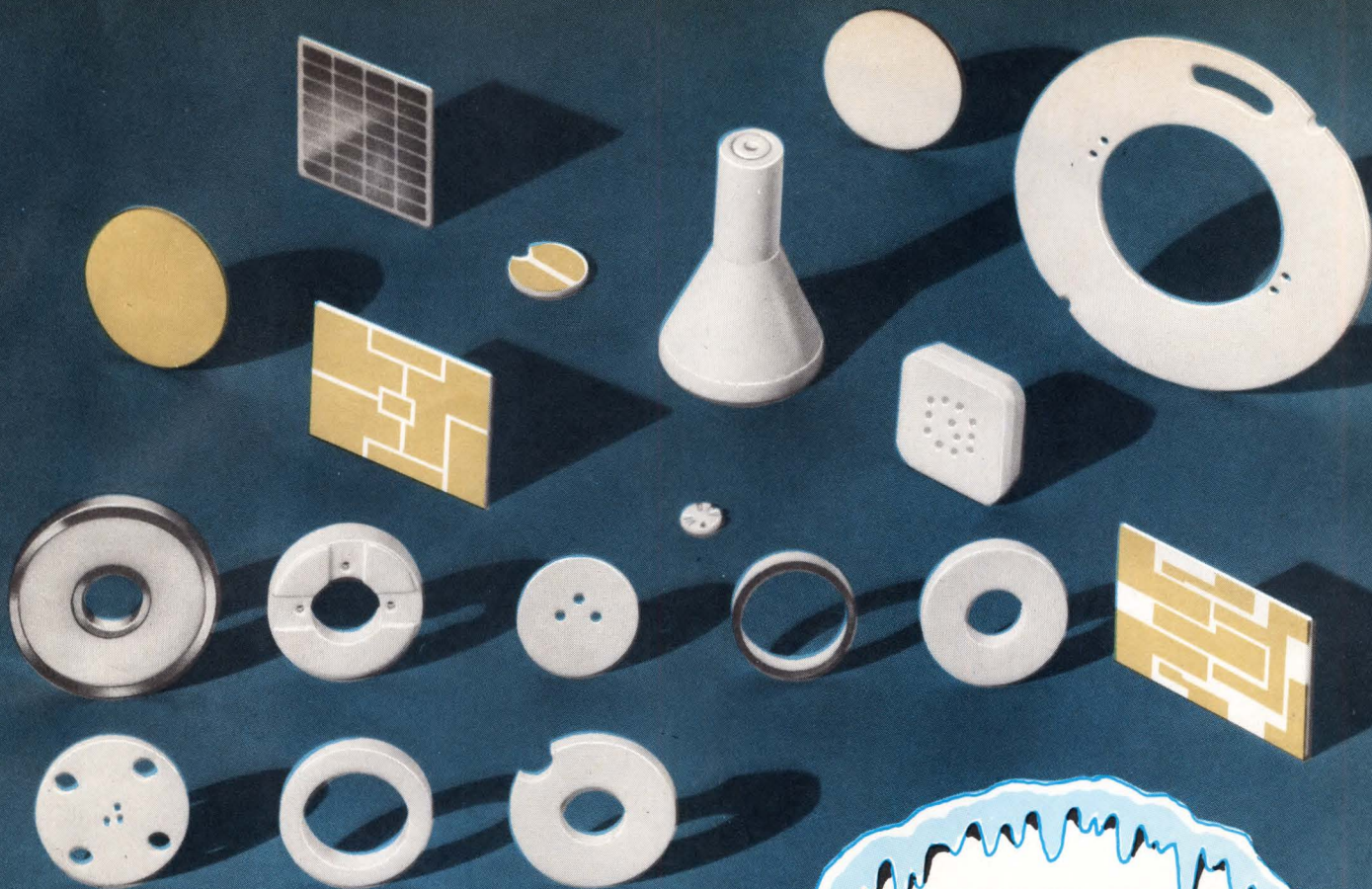
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CIRCLE NO. 24

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New tapes deliver long-term shielding protection

New Scotch Brand tapes with embossed metal foil backings provide an easy, low-cost way to apply lasting EMI shielding in applications up to 12 GHz. Insertion loss levels remain constant in year-long tests. (Applied to a copper substrate, over a $\frac{1}{2}$ " x $2\frac{3}{4}$ " open slot radiating at 143 MHz, Scotch X-1245 tape held the insertion loss level at a steady 65 db.) Insertion losses are equally



Dielectric Materials
& Systems Division **3M**
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CMOS finally gets it all together

Now designers can begin to trust CMOS. It has the second sources of supply, the steadily-expanding MSI, and a solid promise of lower cost.

Robert H. Cushman, New York Editor

Digital logic families have become the backbone of our technology. Their selection is the number one concern for many designers. The right selection of a family will put the designer years ahead of competition; the wrong selection will haunt the designer for years.

CMOS—in the form of the CD4000A family originated by RCA—has finally evolved into a full-fledged, trustworthy logic family. It has enough second sources,—especially since big Motorola has jumped aboard—to get past the cynics in the purchasing department. It has enough gate and MSI functions available off-the-shelf to encourage the designer to give up TTL.

True, present CMOS does not have the speed of TTL, but many of the new application areas don't need speed. For these new markets, like automotive and medical and special-purpose industrial control, CMOS offers designers something far more important than speed: a straightforward, very easy to apply, building-block quality. CMOS is said to be the best logic for product breadboarding and prototyping now available. EDN has heard this from users over and over again. "We like it." "It's the only logic we've tried that works the first time."

This report will introduce some of the CMOS circuits at gate, and hybrid and MSI levels that may make CMOS the "top family" of the 1970's.

An honest gate-level MOS

Unlike most single-channel MOS, that is only really available as discrete devices or full-fledged LSI, CMOS is available in a full-spectrum array of basic gates, flip flops and MSI just like bipolar logic families. Fortunately, because of RCA's eight-year head start in CMOS, RCA's CD4000A family is the dominant de facto standard in CMOS today. Thus, designers are spared the frustrating agonies of choosing between several seemingly equal families, as in the case of DTL and TTL.

Other CMOS families may emerge, such as National's proposed pin-for-pin CMOS replacement for low-powered TTL or a very low-voltage family that might develop from the CMOS circuits used by the watch industry to operate off single 1-1/2V cells. But it will be several years before any new family begins to approach the maturity of the CD4000A family. Besides, for the time being it looks like the 3-15V CD4000A family is suited to the majority of applications. These will be systems that are mostly all-CMOS and not mixtures of TTL and CMOS, many observers feel. Compatibility with TTL will only be an interim requirement, they say, for CMOS will eventually "wipe out" low power TTL, and become the predominant family for gate and MSI-level systems that run under 10 MHz.

The CMOS CD4000A family only needs volume sales to come down to TTL level pricing, these observers feel. Right now gate-level CMOS is 2-3 times the cost of TTL.

First basic element is inverter pair

As is well known, the basic building element for CMOS IC's is a pair of P and N enhancement-mode MOS transistors. This pair is operated push-pull across the supply voltage, using a common gate connection. The very low power comes from the fact that only one of the transistors is on at a time, except when switching. Even when switching, the majority of the dissipation does not come from the resistive flow through the partially ON transistors but from charging and discharging circuit capacitances.

Fig. 1 shows the familiar basic CMOS inverter (a) and its voltage-transfer and load-line characteristics, (b) and (c). There has never been any argument among circuit analysts that the complementary pair is theoretically the best gate for moderate-speed switching. Its "snappy" input-output voltage transfer (curve 2 in **Fig. 1b**) comes closest to the ideal (curve 1). The reason for this switching superiority is easy to understand if you look at the load lines of **Fig. 1c**. Assuming a comparable "downstairs" transistor in each case, one can see that a resistive load upstairs provides a neutral load line (curve 4), making the transistor downstairs do all the work. An enhancement transistor upstairs of the same channel type, as in PMOS, is actually worse than a resistor load, because its sagging characteristic produces a very half-hearted transfer function (curve 6). The depletion transistor upstairs, even though it is of the same channel type, as in DMOS, (curve 3), comes much closer to the ideal characteristics of CMOS. DMOS will be CMOS's closest competitor, for as ex-CMOS enthusiast, Bob Lesniewski, now with MOSTEK, a leader in DMOS says, "it's the poor man's complementary."

CMOS (curve 2) is superior to all these others in performance because the upstairs does not just sit there passively but joins in the switching act. In terms of **Fig. 1b**, the CMOS load line is something like that of the DMOS except that it moves during switching from curve 2a to curve 2b. The push-pull action of the CMOS inverter shows up on **Fig. 1c** like two fencers crossing swords. When the downstairs transistor swings down in going ON, the upstairs transistor swings up in going OFF, and vice-versa. It is hard to beat that switching action.

The TTL transfer curve (no. 5) is included to show how many concessions had to be made in this popular form of bipolar logic to attain high speed. DTL was really superior to TTL in this static respect.

The CMOS characteristics in **Fig. 1** point up some of the

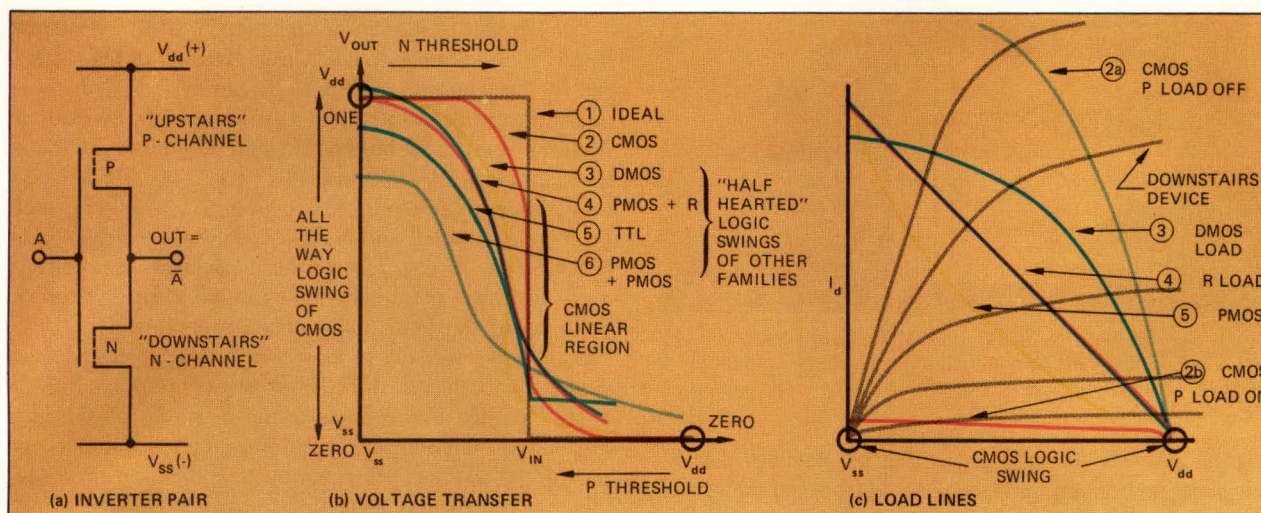


Fig. 1—CMOS is built with pairs of P and N MOS transistors. Most of the time the pairs are driven with a common gate as shown in (a). This pair's switching action comes closest to the

ideal action of any known logic (b), because the active "load" provided by the "upstairs" P device generates a moving load line during switching (c).

basic guidelines for using CMOS properly. If one wants to maintain the micropower capability of CMOS, one should keep the basic pairs at the full ONE-ZERO extremes of the curves as much as possible. As shown in Fig. 1c, practically no current is flowing at these extreme states. If the CMOS passes through the mid-region too often, as will happen with continuous speeds over 1 MHz, then CMOS will not prove any lower in power than other logic (and some of the MSI device package dissipations may be exceeded). Even at lower clock speeds, slow rise and fall waveforms can cause the CMOS to take too long in passing through the mid region, and unnecessarily dissipate

extra power.

Ordinarily, the CMOS itself takes care of these problems, for the regenerative push-pull action of the inverter pairs will cause all the CMOS gates throughout a system to swing briskly hard all the way (within millivolts) of the positive supply or hard all the way towards the negative supply. The exceptional isolation of the inverter pairs—high 10^{12} ohms input impedance and relatively low 1k ohms output impedance—aids this action. There is also a built-in safety margin afforded by the approximately matched 1.7V turn-on thresholds of the P and N devices (in the CD4000A family).

But one can run into trouble when the CMOS is being driven by the many other forms of logic like TTL or PMOS that have sloppy logic swings. As can be seen on Fig. 1b, these logics don't swing all the way to the supplies, and their outputs can put a following CMOS gate into its dissipative region. This might not be obvious because the CMOS with its high noise immunity will continue to function.

A practical problem that bothers engineers when they first use CMOS are gates that have accidentally been left floating. Floating gates can not only waste power but provide headaches for trouble shooters. Designers at one early CMOS user, Monarch Marking Systems, Dayton, Ohio, told us that when they first started working with CMOS they'd occasionally find breadboards acting in a mysterious manner. It invariably turned out to be some input that had been left unconnected and would pick up varying amounts of static charge, causing the gate to erratically shift from one state to the other. It had not been necessary to religiously tie all the gates down when they breadboarded with TTL but they quickly found out that one should make sure that all inputs, even those of unused gates, are tied down to either the positive or negative supply when working with CMOS.

The gate outputs are almost foolproof. The current-limiting characteristics of the P and N devices prevent damaging currents from flowing when the outputs are accidentally shorted to either polarity supply, at least at voltages under 10V. At 5V, all the outputs of most of the gate-level packages can be simultaneously shorted without exceed-

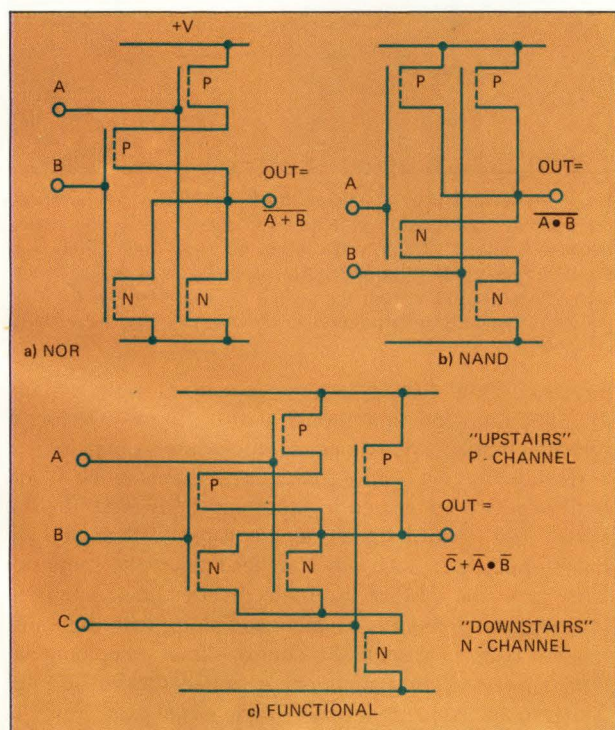


Fig. 2—The pairs of CMOS devices are arranged in series-parallel configurations to produce logic functions. These arrangements can be orderly as the NORs and NANDs of (a) and (b) or mixed as the functional logic of (c). But for every P upstairs there must be an N downstairs sharing the same gate.

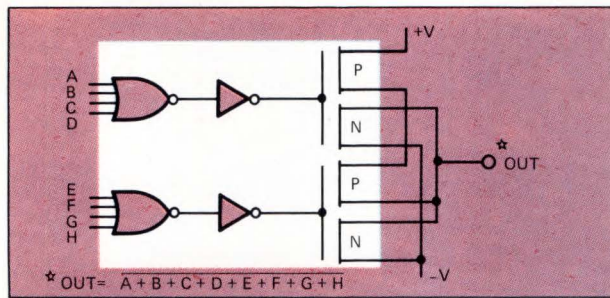


Fig. 3—Second source suppliers to RCA's dominant 4000A CMOS family are adding their own embellishments. Here is a dual four-input NOR from Solid State Scientific that can be wired into a single 8-input NOR.

ing the allowed 200 mW dissipation per package. CMOS suppliers do not recommend it, but EDN noted that many users routinely short the outputs when trouble-shooting.

Five years ago, all MOS systems had bad names because static charges would accumulate on their inputs, create high voltages, and blow the gate oxides. By now, most MOS makers have learned to protect their inputs. RCA has by trial and error made its CMOS family inputs quite rugged. EDN has been using some of the older RCA 6-15V CD4000 series units for over four years now and has not found them especially susceptible to damage from static charge—even when we've occasionally bypassed such advised handling precautions as grounding soldering irons. The inputs of the new 3-15V CD4000A units are said to be even more thoroughly protected by diode-resistor-capacitor networks. About the only precaution needed is not to allow a low-impedance signal whose positive excursion exceeds the CMOS's positive supply to put more than 10 mA into CMOS inputs.

To create logic gates, the CMOS P and N pairs are combined in series-parallel arrangements as shown in Fig. 2. If the P's "upstairs" are put in series while the N's "downstairs" are put in parallel, NOR's are created (a). If on the other hand the P's "upstairs" are put in parallel and the N's "downstairs" are put in series, NANDs are formed (b). Competing single-channel MOS makers say that this need to always operate the CMOS inputs in pairs is a limitation for CMOS at the LSI level, for it means that CMOS can't help but have more metallization runs and oxide window openings than single-channel MOS.

The P's and N's don't have to be in orderly all-series and all-parallel groupings as shown for the NOR and NAND but can be mixtures of series and parallel both "upstairs" and "downstairs" (c). This freedom can be used to efficiently implement boolean equations using the "tree" or functional logic popular with relays, as shown in (c).

CMOS gates are logically just the opposite of DTL and TTL in one important respect. While DTL has large, expandable fan-in and limited fan-out, CMOS has limited fan-in and almost unlimited fan-out. The fan-in to a CMOS gate is limited because a complete PN pair must be added for each input. This is why most of the CS4000A gates have no more than four inputs and these can't be expanded (by diodes, as in DTL). The fan-out on the other hand is limited only by the effect of added wiring capacitance on operating speed. From the dc standpoint, fan-outs much larger than any designer is ever likely to want—in the hundreds—are possible.

One answer to the fan-in limitation of CMOS is offered by SSS (Solid State Scientific) in its 4402 and 4412 gates, Fig. 3. The dual four-input NORs and NANDs in these packages can be paralleled for a fan-in of eight by external wiring on the output buffers. SSS can offer this variation of the standard RCA 4002 and 4012 packages because SSS uses a different internal construction. SSS uses very small geometries on the P and N devices in the actual NOR and NAND gates at the front of these packages and follows these with two progressively larger-geometry inverters to build up to the final output drive capability. (The drive capability is inversely proportional to the device ON resistance and this is directly proportional to the device area.) SSS then leaves some of the terminals on the final inverter pair uncommitted and brings them out to package pins so the user can effect various combinations. SSS says this concept can be expanded to provide fan-ins as high as 16.

Second basic element is transmission pair

The P and N pairs can also be arranged parallel to the power supply, as shown in Fig. 4. This forms the second of the two basic CMOS elements, the transmission switch. It is a rather remarkable element for it can handle analog as well as digital signals and pass these signals in either

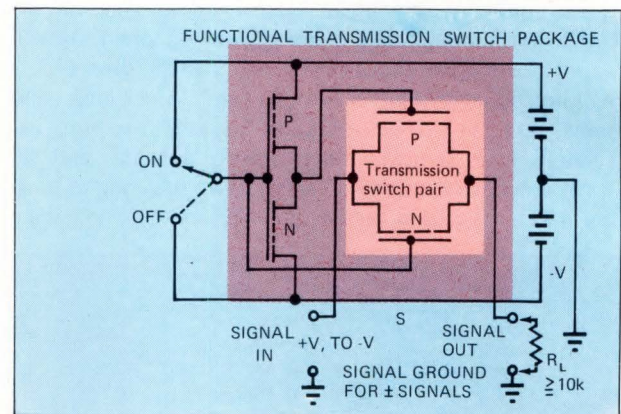


Fig. 4—A second way of pairing the P and N devices produces the versatile transmission switch. It's CMOS's ace up the sleeve because it allows CMOS to do things no other logic family can do. Its a high-grade bi-directional analog switch as well. The inverter (left) needed to turn the switch devices ON and OFF together is typically incorporated inside the IC's that have these switches.

direction. Only CMOS technology can so aptly provide this SPST relay function, though it also can be implemented with complementary pairs of bipolar transistors.

As shown in Fig. 4, the sources and drains of the P and N devices are connected together and "powered" by the signal. The control signals to the gates of this pair are made opposite to each other, rather than of the same polarity as in the case of the basic inverter pair. A built-in inverter pair element is usually used along with the transmission pairs to provide the control signal complementation. Therefore, the pair is either turned ON or OFF together to act like a SPST switch in the signal path.

The advantage of having the opposite-polarity devices in parallel is that neither signal swing will be limited by the gate thresholds and the signal can swing across the whole CMOS supply range. As the sources and drains of these MOS devices are interchangeable, it doesn't matter

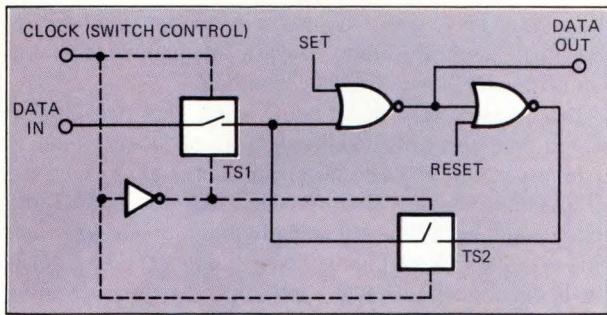


Fig. 5—Transmission switches control the behavior of CMOS flip flops in a most literal manner. The clock works the two transmission switches in opposition. When the clock goes up, TS1 is closed to let data flow into the FF NORs, which is possible because TS2 is open and the NORs are unlatched. Then, when the clock goes back down, TS1 opens, cutting off the data input path, and TS2 closes to hold the data latched in the NORs.

which way the signal flows.

When used to pass or impede digital signals in CMOS logic systems, two or more of these switches are often used to select which of several signals is to be fed to a gate. Only one transmission switch is turned on at a time, and its low impedance—several hundred ohms—will connect one of the signals. The other OFF gates meanwhile have such high impedances—100M Ω —that they might as well be open circuits.

An example of how this is used inside the CD4000A family flip flops is shown in Fig. 5. The control in this case comes from the clock and it alternately turns the two transmission switches ON and OFF in opposition. The first transmission switch is turned ON to enter data into the FF and then the second transmission switch is turned ON to latch the data into the FF. An identical slave FF working on the opposite phase of the clock will usually follow.

Transmission switches can be used to implement three-state logic for common bussing, as will be shown later. There is, however, another way of obtaining the "third," or high-impedance, state on an output. This is to drive the inverter pair in opposition with separate gate inputs so they are both turned OFF. A logic arrangement for this purpose suggested by RCA is shown in Fig. 6. When the control input is LOW, the data will flow through to the output; but when the control input is HIGH, both output devices will be OFF and the output will be disabled. However, this approach does not have either the bidirectionality of the transmission switch.

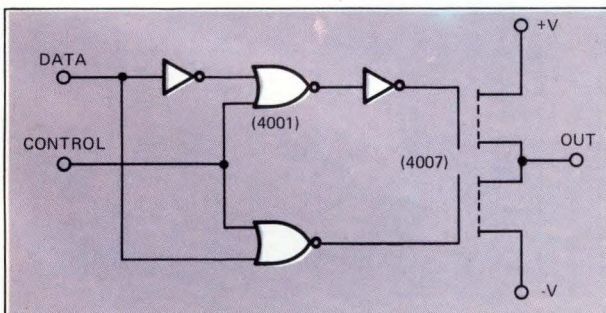


Fig. 6—A third configuration for CMOS pairs is to be put across the supply as in the case of the inverter pair, but to have the gates driven separately. Then they can be either driven together, as in the inverter, or in opposition to produce a "both OFF" state that disconnects the output. This can be used to selectively connect several signal sources to the same party line.

CMOS encourages novel hybrid circuits

Much of the CMOS circuit applications that have been published so far represent fairly routine conversions of popular TTL logic to CMOS. This is as it ought to be for most applications. But there is an important fringe area that CMOS is uniquely qualified to penetrate—the area of hybrid analog-digital functions. CMOS unlike most previous IC logic families, can be made to perform in linear as well as in its basic digital mode. Moreover, CMOS can accomplish nonlinear analog functions such as chopping

While CMOS does not do all of these linear functions as well as they can be done with bipolar linear circuits, and in fact in doing them CMOS often loses its micropower qualities, still it may, at times, be worth having CMOS perform these other functions. There are advantages in having one, unified family make up the whole system. This will be especially true in the future, when complete products will be constructed on one LSI chip.

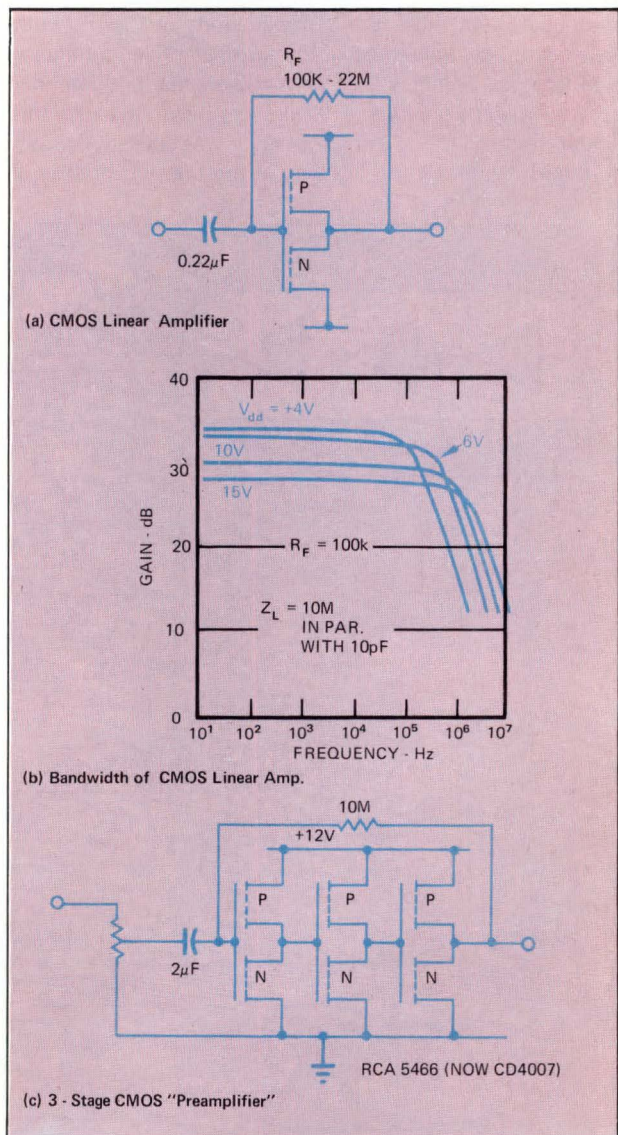


Fig. 7—CMOS inverter pair serves as a linear amplifier. A high-value feedback resistor (a) will cause the inverter pair to self-bias itself in the middle of its linear region, where respectable ac signal amplification for small input voltages will be obtained (b). Odd numbers of pairs can be so self-biased for higher gains (c).

Both the basic pair elements that make up CMOS have linear abilities. It is a bit surprising to find out that the basic inverter pair that is such a perfect logic gate amplifier can also perform credibly as a linear amplifier. Yet, if the inverter pair is self-biased by a feedback resistor from output to input, as in Fig. 7a, it will sit at the middle of its transfer curve where there is a good linear region. The transfer curve is quite steep here (look back to Fig. 1b) so gains of 10-30 are possible for signal swings of a volt or so, with bandwidths up to a MHz, as shown in Fig. 7b. Quite high gains—from 1000 to 10,000—can be obtained by putting three inverter pairs in series with the biasing feedback resistor around all three, as shown in Fig. 7c. Usually the input is ac coupled via a small coupling capacitor, but some experienced CMOS makers say they can now provide enough device stability for straight dc operation.

We suspect that it has been the rapid strides in CMOS processing capabilities at old-timer companies like RCA, SSS and Ragen that has caused them to become more affirmative about these linear applications of CMOS. Four years ago, having learned of the three-amplifier configuration from Joe Tomei of SSS, we made a guitar pre-amplifier for a teenager from RCA 4007 devices just to evaluate this linear mode (Fig. 7c). Its performance was entirely satisfactory and the sharp non-linearity at the top and bottom of

the transfer curve was even useful in optionally producing the "fuzz" type distortion (by not attenuating the input signal) that Rock and Roll musicians like.

The second basic CMOS element, the transmission switch pair, performs equally well in the linear mode. A bipolar version might be faster but that is all. In fact, the CMOS transmission switch is such a superior form of analog-digital switch that it is already finding wide uses outside the CMOS logic family. Some suppliers, such as Harris Semiconductor, Ragen and Siliconix, market these switches as separate analog components.

A practical little circuit we developed using the RCA CD4016A quad transmission switch is shown in Fig. 8. The objective was to multiplex four different signal traces onto a single-channel oscilloscope. The power supply for the CMOS was the same +6V and -6V that we had to have for the 741 op amp summer that combined these circuits into the scope's one channel anyhow. There was no discernable change in the power-supply drain when the CMOS was added, a nice bonus when you add CMOS to existing designs.

The lower 4016 multiplexed four signals on to the scope via the 100 k Ω summing inputs to the 741 op amp. The upper 4016 was for synchronously adding dc bias levels to the op amp summing network so that each of the four signals could be adjusted vertically apart from one another

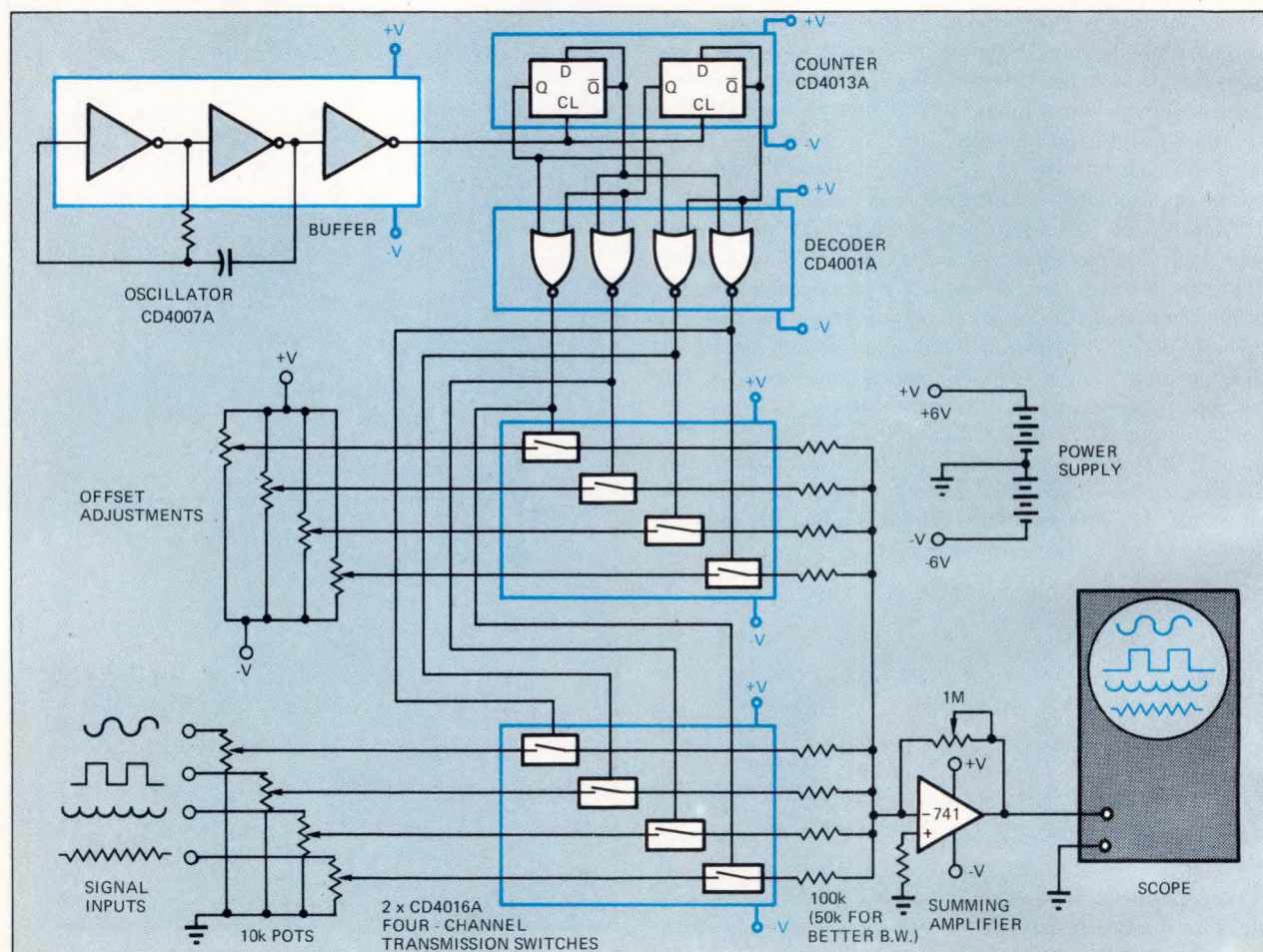


Fig. 8—CMOS transmission switches make excellent analog gates. Here two 4016 quad switches are being used to multiplex four analog signals onto a single-channel oscilloscope. The lower quads open and close the signal paths. The upper quads open and

close dc bias levels. Both quads are driven by the same repeating 1, 2, 3, 4 count from the oscillator-counter-decoder combination above. The 741 op amp adds the signals and biases and presents their sum to the scope.

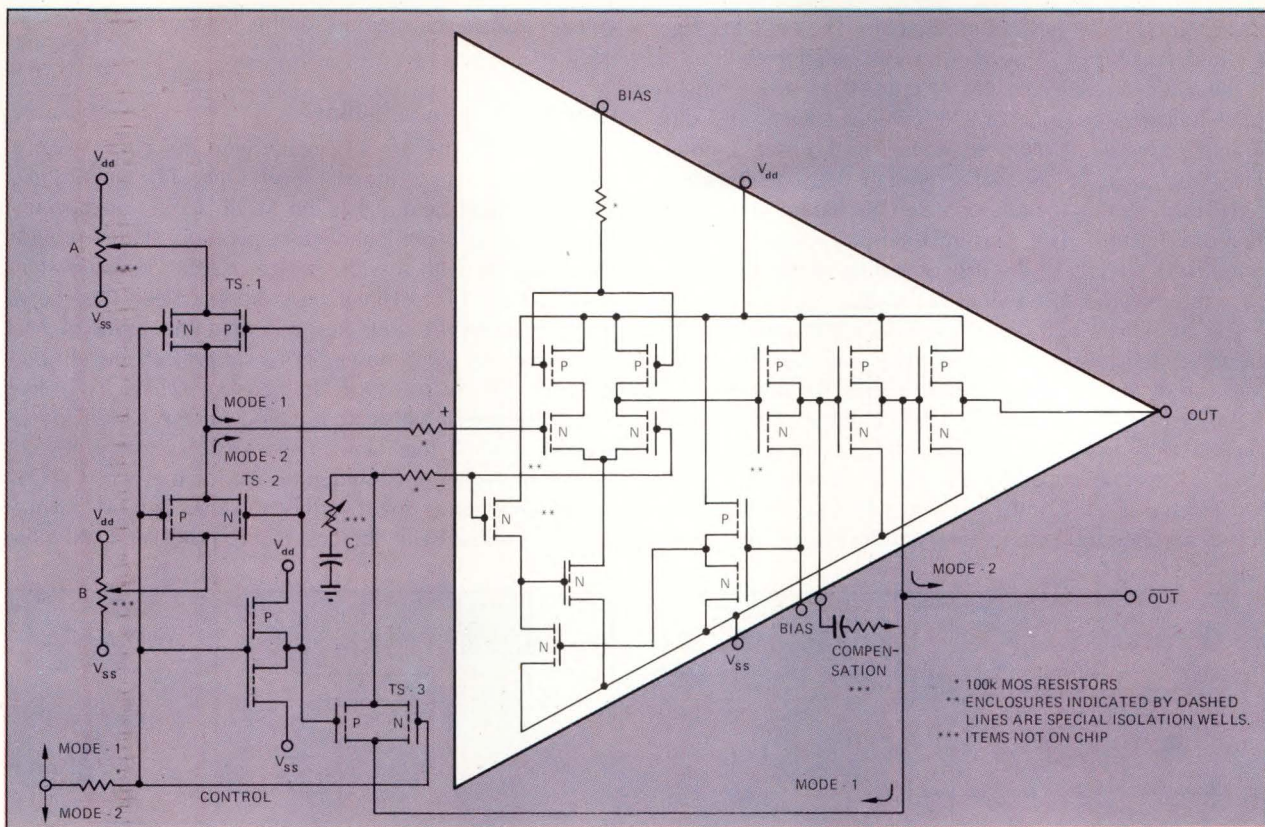


Fig. 9—Sophisticated linear subsystem has been integrated on a CMOS chip by Ragen. A linear-type differential front end has been added to the three CMOS inverter-pair amplifier stages. The transmission switches allow this amplifier to alternately act as an

op amp follower to copy input voltage A on capacitor C, and then as an open-loop comparator to compare voltage on C against input voltage B. This device was developed as a custom device for the military, but is now a commercial item.

on the scope display.

The transmission switches in the 4016 appeared to have all the qualities needed for this analog application. They did not distort the signal when ON and would shut it off adequately when OFF. The transmission bandwidth was into the MHz range and the ON-OFF switching speed more than adequate for the application.

A sophisticated CMOS hybrid

We have touched upon our personal experience with

CMOS in the hybrid mode to emphasize how easy it is to implement some widely-needed but not necessarily digital functions with this flexible, all-purpose "logic" family. An advanced example of this linear aspect of CMOS is shown in **Fig. 9**. It is a multi-mode op amp that comes from a custom circuit developed by Ragen for the military, but now also being sold separately as Ragen's 6023 comparator.

The original LSI A/D converter is a good example of a mostly digital CMOS circuit that incorporates vital linear functions. These linear functions represented 150 devices

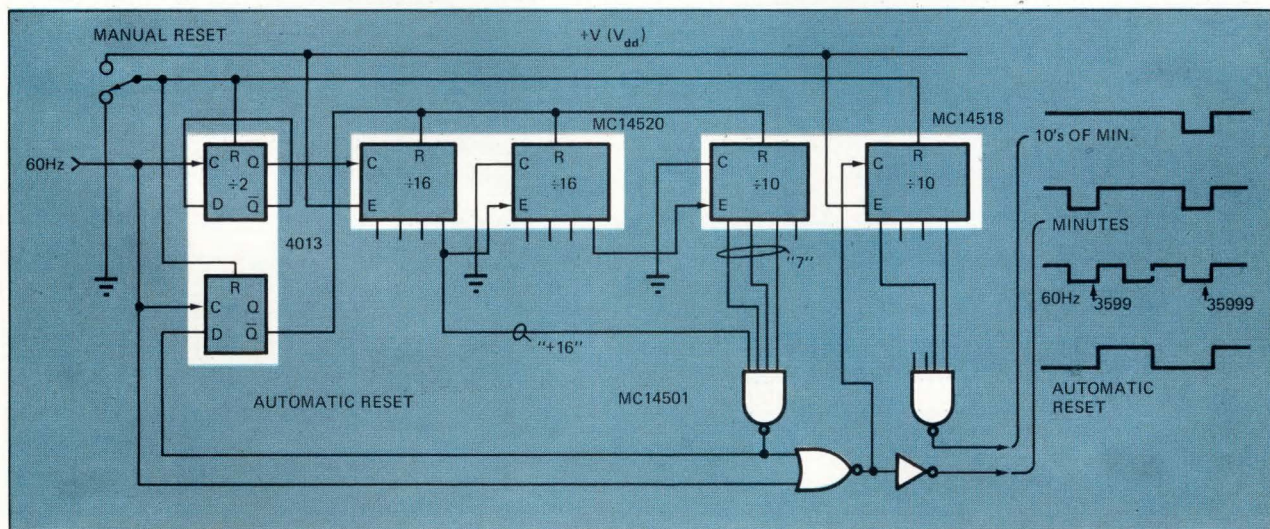


Fig. 10—CMOS MSI is unbeatable for economically performing low-frequency counting. Only a handful of packages are usually needed, and because of the low frequency the power supplies

will cost but a fraction of a dollar. This 60-Hz to minutes and tens of minutes counter could be incorporated as a stand-alone component in consumer appliances, for example.

out of the 600 total devices on the chip. The circuit of Fig. 9, which consists of 25 devices, was repeated three times.

The basic amplifier in Fig. 9 consists of a differential stage followed by four CMOS inverter stages. The differential stage is a CMOS equivalent of the usual bipolar differential stage. Note that it has an unusual constant-current source that includes isolated N-channel devices in their own wells. The four inverter-pair stages operate completely linearly in the first operating mode, but build up to full digital output swings in the other.

The amplifier's two operating modes are controlled by the three transmission switches, in a way that resembles their use in the standard CD4000 family flip-flop (Fig. 5). In the first mode, TS1 and TS3 are closed so that the amplifier acts as an op amp voltage follower and stores the A input voltage on capacitor C. In the second mode, TS1 and TS3 are opened and TS2 is closed. Now the amplifier acts as an open-loop comparator and measures the B input

voltage against the memory of the A input stored on capacitor C.

CMOS MSI is snowballing

It is said that where TTL really won out over previous logic families was at the MSI level. Once TTL families like TI's 7400 (and before that the SUHL family of the now defunct Sylvania semiconductor operation) started providing designers with a wide choice of MSI, designers standardized on TTL, even if they did not need the speed. CMOS CD4000A now has a formidable array of MSI functions and some observers feel it will effectively out-distance TTL before long. It therefore seems likely that many designers will start jumping on the CMOS bandwagon, even if they don't need CMOS's low quiescent power or high noise immunity. And if they do, CMOS prices will come down further towards the TTL level—CMOS is about twice the cost of TTL now—and still more

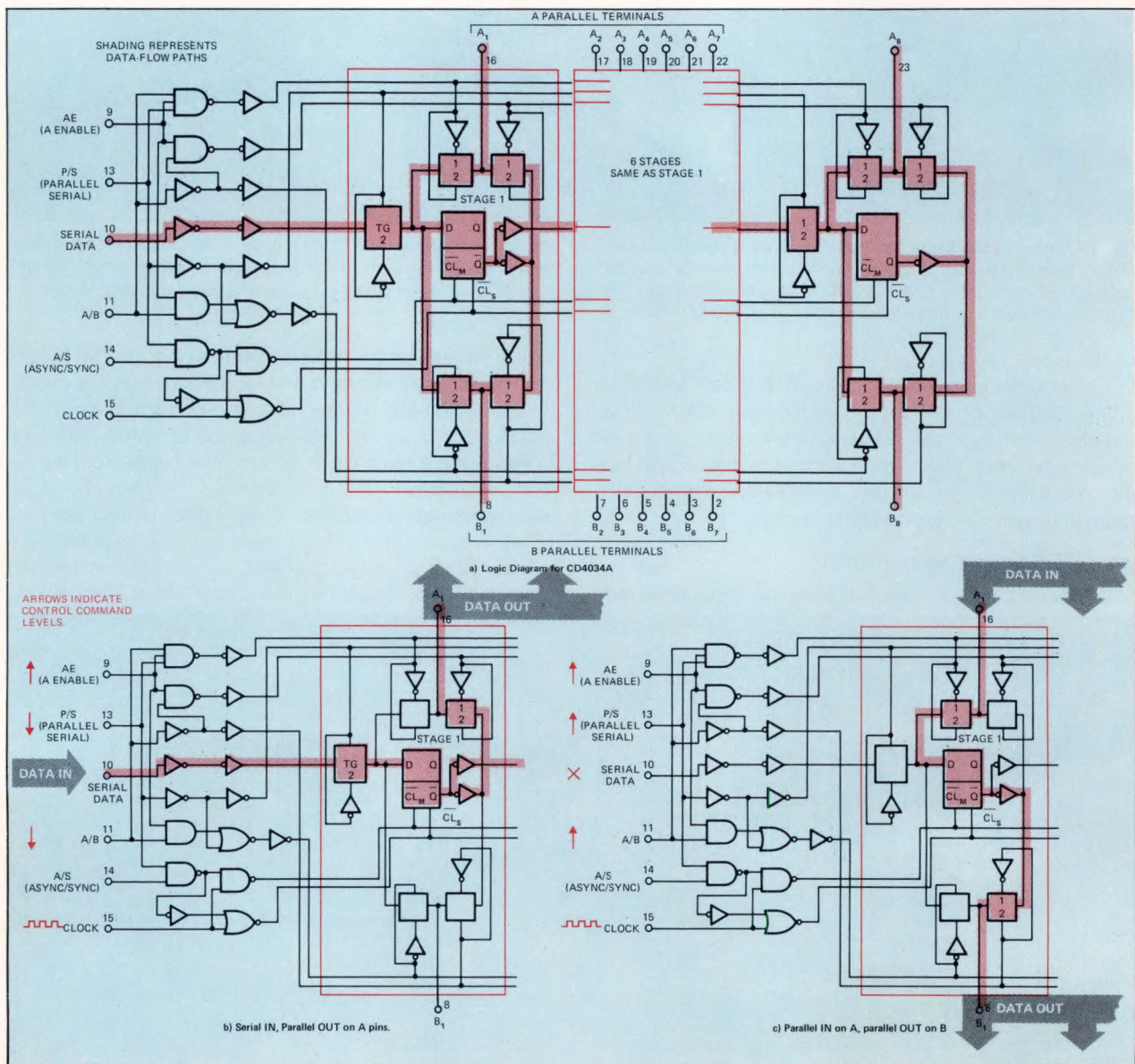


Fig. 11—CMOS MSI is offering some truly universal registers. The 4034 has the built-in control circuitry to do about anything a designer would ever want to do with a register, and it has "three-state" data outputs to boot. The combination of low gate power and

transmission switching allows CMOS to pack more function into small device packages (the 4034 is contained in just a 24 pin DIP). Additional diagrams of left side of 4034 schematic (b) and (c) indicate how control commands to 4034 can change the routing of data.

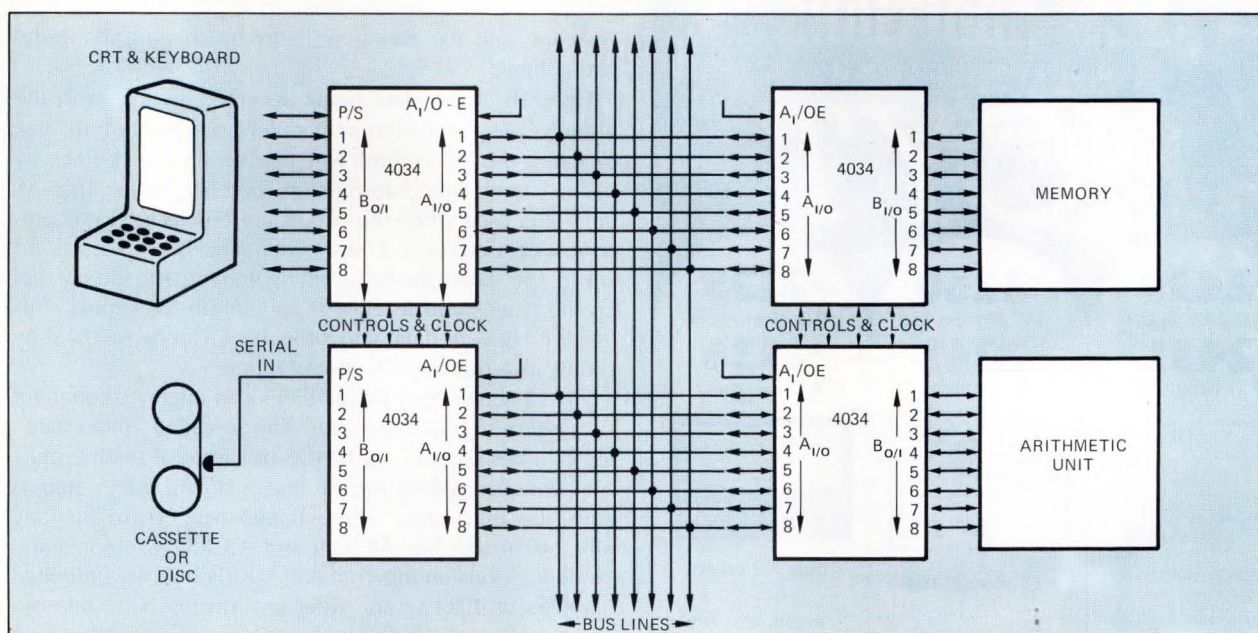


Fig. 12—Common-bus architecture is “child’s play” with the 4034. The user is given all the internal circuitry to accomplish

party-lining, via a minimum number of simple control lines. Here, 4034’s are being used to route 8-bit ASCII characters.

designers will jump aboard.

Then, if suppliers like Harris Semiconductor and RCA start seriously bringing out CD4000 with various forms of dielectric isolation, we will have CMOS fully as fast as TTL and even more designers will jump on the CMOS bandwagon.

What are these CMOS MSI functions that users like the design team at Monarch Marking Systems tell us are so attractive? They are functional groups of the gate-level CMOS building blocks. They are counters and registers and arithmetic arrays. What is nice about CMOS LSI is that it is composed of the same circuits the designer has already become familiar with at gate level, and so are particularly easy to understand and apply.

We will describe just a couple of them . . . some Motorola counters and an RCA “universal” eight-bit register. Each represents a widely needed system function to designers. The Motorola MSI makes timing logic simpler and the RCA register renders common-bussing architecture “child’s play.”

CMOS MSI will dominate timer applications

A routine function in industrial and consumer products is a timer that can count out intervals like minutes and tens of minutes. The circuit in Fig. 10, developed by Motorola CMOS application engineer Jim Halligan, performs this function to the accuracy of the 60-Hz power line, using only four standard CMOS 4000 family packages. Only one of these packages is from RCA’s designs. The other three are Motorola additions to the 4000 family, as indicated by their 4500 numbering (just like the 4400 numbering in Fig. 3 indicated a SSS addition).

The logic of the Motorola counters permits obtaining the full count without having to use decode gates. If the input to these counters is put in on the “E” (enable) pins instead of the “C” (clock) inputs, the counters will respond to the negative edges of the data rather than the normal positive edges. The unused E and C pins are tied to the proper positive or negative supply rails as shown. This arrangement is

used on the input to the second divide-by-sixteen counter and the first divide-by-ten BCD counter. Therefore, these units ignore the positive-going logic level that occurs when the divide-by-sixteens feeding them reach their half-way counts of eight, but do respond to the negative-going logic levels that occur when they reach their final return to 0000 or sixteenth count.

Another trick used by Halligan was to arrive at the divide-by-60 count by first having three of the inputs to the decoding gate, G1, from the first-divide-by-ten sense when the count of $2 \times 16 \times 16 \times 7$ or 3584 is reached, then have the final enable to this NAND come when the output from the first divide-by-sixteen counter indicates that 2×8 , or 16, additional counts have come through. The 3584 plus 16 then equals the desired 3600 counts. Actually, to avoid a race condition, he has his reset anticipated when 3599 counts have been reached and resets the counter on 3600, as shown by the waveform timing. The second divide-by-ten divides the 60 Hz further into ten minute intervals.

A universal bus’able register

RCA is justifiably proud of its new CD4034A “universal” register. This MSI product really “puts it all together” for it incorporates all the control inputs and data steering allowing the designer to do just about anything with a register. You can begin to appreciate the capability of the 4034 by studying Fig. 11a. The 4034’s 24 pins are deceptive, because 16 of them really represent two pins in one. Transmission switches are used to connect these pins bi-directionally to the eight flip flops of the 4034. Thus, the 4034 is the equivalent of a 40-pin device in other technologies, and a good example of how the tricks inherent in CMOS can keep device packaging costs down, while adding to device capability.

Two of the 12 possible data flow combinations for the 4034 are shown in Fig. 11b and 11c. The control inputs are shown by vertical arrows at the left, the states of the transmission switches by shading to indicate closed

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switches, and the data-flow paths by shading along the circuit lines.

Fig. 11b shows data being accepted serially with the outputs being available in parallel from the A pins. Just lowering the AE control will disable all the A lines by making both their transmission switches open. This AE control is used when the A pins are connected to a common system bus as will be shown in Fig. 12.

Fig. 11c shows the data coming into the 4034 in parallel on the A pins and leaving in parallel on the B pins. This "lateral" flow of data across the 4034 can be reversed by simply lowering the A/B control input.

Fig. 12 shows how these 4034's can interface computer subsystems to a common bus. The so-called "three-state" logic comes naturally to CMOS by virtue of the transmission switches. When the AE line is down, the A outputs have the third state,—high impedance. Therefore, any other 4034 that has AE high and AB low will command the logic levels on the common bus. Practically unlimited numbers of 4034's can "listen in" on the party line because of CMOS's high fan out. The control combination for listening in would be AE high, P/S high, and A/S high (for asynchronous reception). The caption indicates how a computer-like system of this architecture could be doing several tasks at one.

Not a bad sort of capability for a 100 by 115-mil chip that is projected to cost \$6 in quantities! It will be devices like the 4034 and a coming four-bit parallel arithmetic processor that will play a significant part in deciding whether CMOS logic families become as important in the 70's as TTL became at the end of the 60's. □

CMOS Suppliers

This list is primarily based on semiconductor manufacturers who now offer the CD4000A family. No attempt has been made to include the many other suppliers of custom CMOS. Readers interested in obtaining quotations on custom CMOS would probably be well advised to contact all MOS makers.

Harris Semiconductor
Melbourne, Fla. 32901
(305) 727-5400

Circle 276

Hughes
Microelectronic Div.
500 Superior Ave.
Newport Beach, Calif.
92663
(714) 548-0671

Circle 277

Inselek
University Park Plaza
743 Alexander Rd.
Princeton, N J 08540
(609) 452-2222

Circle 278

Motorola Semiconductor Products Inc.
5005 E. McDowell Rd.
Phoenix, Ariz. 85008
(602) 273-6900

Circle 279

Semiconductor Corp.
2900 Semiconductor Dr.
Santa Clara, Calif. 95051
(408) 732-5000

Circle 280

Ragen Semiconductor Inc.
53 S. Jefferson Rd.
Whippany, N J 07981
(201) 887-4141

Circle 281

RCA Solid State Div.
Somerville, N J 08876
(201) 722-3200

Circle 282

Silicon Inc.
2201 Laurelwood Rd.
Santa Clara, Calif. 95054
(408) 246-8000

Circle 283

Solid State Scientific Inc.
Montgomeryville, Pa. 18936
(215) 855-8400

Circle 284

Solitron Devices, Inc.
8808 Balboa Ave.
San Diego, Calif. 92123
(714) 278-8780

Circle 275

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Switching, plain and not so plain

The hybrid time delay relay featured below (at d) is a business-like combination of modern electronics with a reliable, inexpensive electromagnetic relay. A single package wraps up the whole deal. It is for places where you want a switching delay of from 1 to 120 sec. repeatably accurate to $\pm 3\%$, fixed or variable; and prefer not to provide the timing elsewhere. The idea is neither original nor recent. Sigma does it more compactly, reliably and *cheaper*.

10,000 volt switching doesn't sound like a subject that belongs on this page. It wouldn't under common circumstances, but item c is an elegant means of grounding the high voltage in an office copier when somebody has to reload it. Would you believe it's an internally illuminated photoconductive element dropping open circuit resistance of 10^{12} ohms to 100k?

Light controlled photoconductor relays in standard packages were brainchildren of a Sigma division specializing in solid state photoconductors. Great merit and flexibility results from use of these Datarels® as we call them; viz. total isolation of input from output or outputs (1 to 4)—with outputs passive and nearly as compatible as resistors. The latest variety was invented by our lady physicist and is imaginatively known as a "Ladybug."

A Ladybug-relay combination solved a recent delayed alarm problem for a Sigma customer. By using a Neon light source for control, the Ladybug imposed *no load* on the timing circuit, operated directly from 120 volts with lock-on alarm. It makes quite a time delay device—up to 60 sec. after *opening* a control circuit. Ladybugs and Datarels® have the flexibility of three alternative internal light sources: Incandescent, Neon and LED.

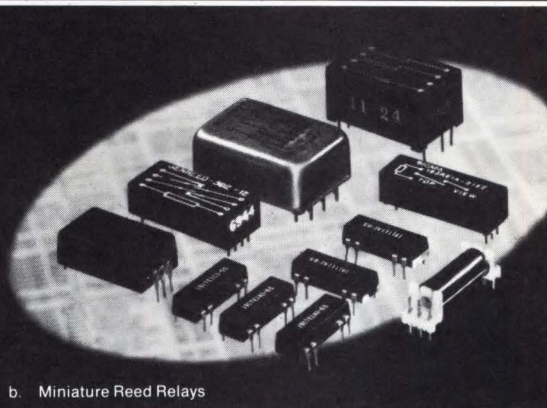
Savvy switching is a worthwhile specialty to know about when you can use it. Sigma has it and has had it since the late thirties.

If you'll circle No. 21 on the beano card, you'll get a fistful of poop. If you write on a specific question, we'll answer it carefully along *with* the poop; and if you make it a personal letter to relay marketing chief, Stu Knapp, with your problem and project laid bare, the action will be sudden and substantial. Write Sigma Instruments, Inc., 170 Pearl St., Braintree, Mass. 02185. Telephone 617-843-5000.

SIGMA
INSTRUMENTS INC



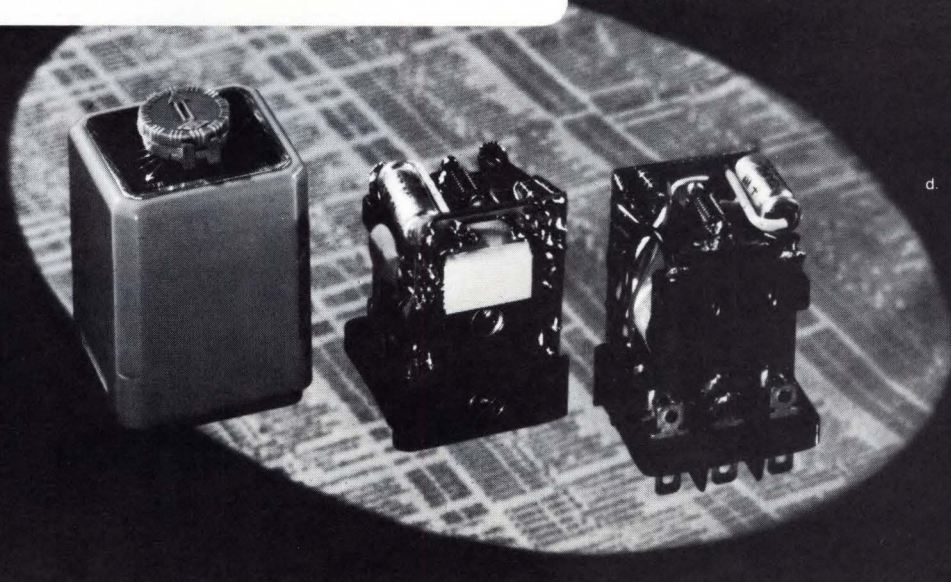
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b. Miniature Reed Relays



c. See text.



d. See text.

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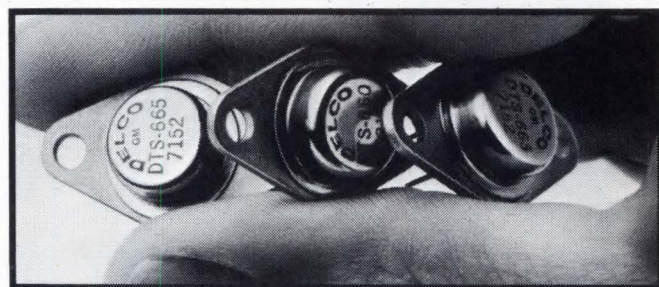
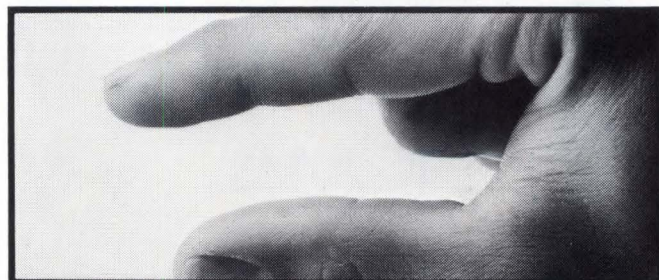
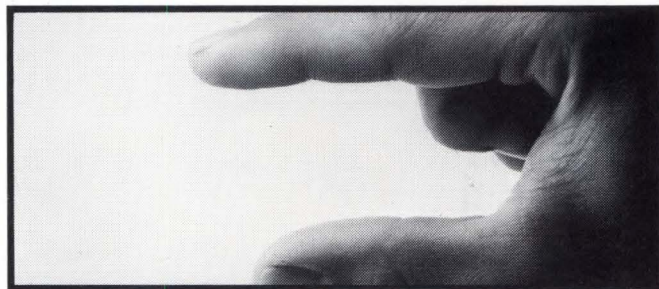
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Type	I_C (Cont) (Peak)	V_{CEO}	h_{FE} @ $I_C=1.0A$ min./max.	$V_{CEO}(SUS)$ min.	P_D min.	Suggested resale price 1-99 quantity
DTS-660	3.5A 10.0A	200V	30 90	200V	60W	\$5.93ea.
DTS-663	3.5A 10.0A	400V	30 90	325V	60W	\$9.57 ea.
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Yes, you can design Butterworth or Chebyshev active filters with gain!

Gain is often desirable in active filters. Now you can program gain and frequency performance without resorting to a separate amplifier stage.

Charles J. Williams, Singer-Kearfott Div.

Design equations for a filter with gain greater than unity are cumbersome and time-consuming to solve without the aid of a digital computer. Even when you have access to a computer, you will find that most computer programs for the design of active filters invariably have the limitation of unity gain. This article describes a computer program which avoids this unity-gain restriction in the design of high-pass, low-pass and multiple-pole active RC filters.

The computer program, written in Tymshare's Superfortran and shown in Fig. 1, may be used to design high-pass and low-pass active filters with gain. It allows the user to specify the passband characteristics of the filter either in the form of maximum allowable ripple or damping factor. The program also provides a summary of the important filter parameters for the purpose of documenting the design.

2-pole low-pass filters

The transfer function for the 2-pole low-pass filter circuit shown in Fig. 2 may be shown to be:

$$T(s) = \frac{K}{\psi^2 + 2d\psi + 1} \quad (1)$$

$$\text{where } \psi = sR_1 C_2 \sqrt{\frac{\beta}{\alpha}}$$

$$\alpha = \frac{C_2}{C_1} \quad (2)$$

$$\beta = \frac{R_2}{R_1} \quad (3)$$

$$= \frac{1}{\alpha} [2d^2 - (1 - K + \alpha) + 2d\sqrt{d^2 - (1 - K + \alpha)}] \quad (4)$$

d = Damping Factor

$$= \frac{1 - K + \alpha + \alpha \beta}{2\sqrt{\alpha \beta}} \quad (5)$$

$$K = \text{gain} \quad (6)$$

and s = Laplace transform operator.

The break frequency (ω_0) of the filter is:

$$\omega_0 = \frac{1}{R_1 C_2} \sqrt{\frac{\alpha}{\beta}} \text{ Rad./Sec.} \quad (7)$$

```

- SFO
> LOAD GRAY
OK
> LIST
1      INTEGER Y, H, D1
2      DATA Y, H, D1/1H, 1H, 1HD/
3      DISPLAY "DAMPING FACTOR (D) OR PASSBAND RIPPLE (P)?"
4      READ (0, 1) L
5      IF (L.EQ. D1) GO TO 11
6      DISPLAY "ENTER THE PASSBAND RIPPLE IN DB (0 FOR BUTTERWORTH)"
7      ACCEPT R
8      E = SQRT(10**(R/10) - 1)
9      D = 0.5*SQRT(2*(1 - (E/(1 + E**2))))
10     GO TO 12
11     DISPLAY "ENTER THE DAMPING FACTOR, D"
12     ACCEPT D
13     IF (D.GE. .707) GO TO 13
14     R = 20*LOG10(1/(2*D*SQRT(1 - D**2)))
15     GO TO 12
16     13
17     DISPLAY "WHAT IS THE CLOSED LOOP GAIN?"
18     ACCEPT AK
19     DISPLAY "WOULD YOU LIKE A HIGH-PASS (H) OR LOW-PASS (L) FILTER?"
20     READ (0, 1)M
21     DISPLAY "ENTER THE CORNER FREQUENCY (KHZ)"
22     ACCEPT F1
23     F = F1*1E3
24     DISPLAY "ENTER C2 (PF)"
25     ACCEPT C2
26     C2 = C2*1E - 12
27     6     DISPLAY "ENTER ALPHA"
28     ACCEPT A
29     D2 = D**2
30     C = 1 - AK + A
31     IF (D2 - C) 4, 5, 5
32     4     DISPLAY "WARNING (D2 - ((1 - K) + A)) < 0"
33     DISPLAY "ALPHA MUST BE LESS THAN", D2 - 1 + AK
34     DISPLAY " "
35     DISPLAY " "
36     DISPLAY "TRY A SMALLER ALPHA"
37     DISPLAY " "
38     GO TO 6
39     5     B = (1/A)*((2*D2) - C + (2*D)*SQRT(D2 - C))
40     R1 = 1/(2*3.14159*F*C2*SQRT(B/A))
41     IF (M.EQ. H) GO TO 9
42     R2 = B*R1; C1 = C2/A
43     DISPLAY " "
44     IF (R.EQ. 0) GO TO 7
45     DISPLAY " "
46     DISPLAY " "
47     DISPLAY "CHEBYSHEV LOW-PASS FILTER"
48     GO TO 8
49     DISPLAY " "
50     7     DISPLAY "BUTTERWORTH LOW-PASS FILTER"
51     GO TO 8
52     9     R2 = (SQRT(B/A))/(2*3.1415926*F*C2)
53     C1 = C2/B
54     R1 = R2*A
55     IF (R.EQ. 0) GO TO 10
56     DISPLAY " "
57     DISPLAY " "
58     DISPLAY "CHEBYSHEV HIGH-PASS FILTER"
59     GO TO 8
60     10    DISPLAY " "
61     DISPLAY " "
62     8     DISPLAY "BUTTERWORTH HIGH-PASS FILTER"
63     DISPLAY "DESIGN REQUIREMENTS"
64     DISPLAY " "
65     DISPLAY "BREAK FREQUENCY = ", F1, "KHZ"
66     DISPLAY "CLOSED LOOP GAIN = ", AK
67     DISPLAY "PASSBAND RIPPLE = ", R, "DB"
68     DISPLAY "DAMPING FACTOR, D = ", D
69     DISPLAY "BETA (B) = ", B
70     DISPLAY "ALPHA (A) = ", A
71     DISPLAY " "
72     R1 = R1/1E3; R2 = R2/1E3
73     C1 = C1*1E + 12; C2 = C2*1E + 12
74     DISPLAY "R1 = ", R1, "KOHMS", "R2 = ", R2, "KOHMS"
75     DISPLAY "C1 = ", C1, "PF", "C2 = ", C2, "PF"
76     DISPLAY " "
77     3     DISPLAY "ANOTHER RUN?"
78     READ (0, 1)N
79     IF (N.EQ.Y) GO TO 2
80     1     FORMAT (A1)
81     END
82

```

Fig. 1 - Computer program, written in Tymshare's "Superfortran" allows the designer to specify critical performance for active filters. Even-order Butterworth filters of up to 12 poles or Chebyshev filters of up to 6 poles can be designed by this technique. Specifying a damping factor of 0.707 (or passband ripple of 0 dB) will result in a Butterworth filter, and a damping factor of less than 0.707 (or passband ripple greater than 0 dB) will give a Chebyshev filter.

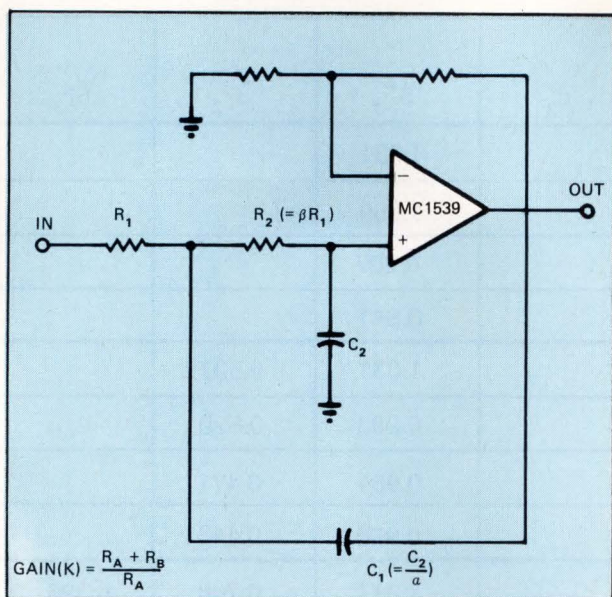


Fig. 2 — This 2-pole, low-pass active filter can be designed quickly, using this program, by specifying the desired damping factor or passband ripple, gain and corner frequency.

2-pole high-pass filters

The transfer function for the 2-pole high-pass filter circuit shown in Fig. 3 is:

$$T(s) = \frac{K}{\psi^2 + 2d\psi + 1} \quad (8)$$

$$\text{where } \psi = \frac{1}{SR_2C_2} \sqrt{\frac{\beta}{\alpha}} \quad (9)$$

$$\alpha = \frac{R_1}{R_2} \quad (10)$$

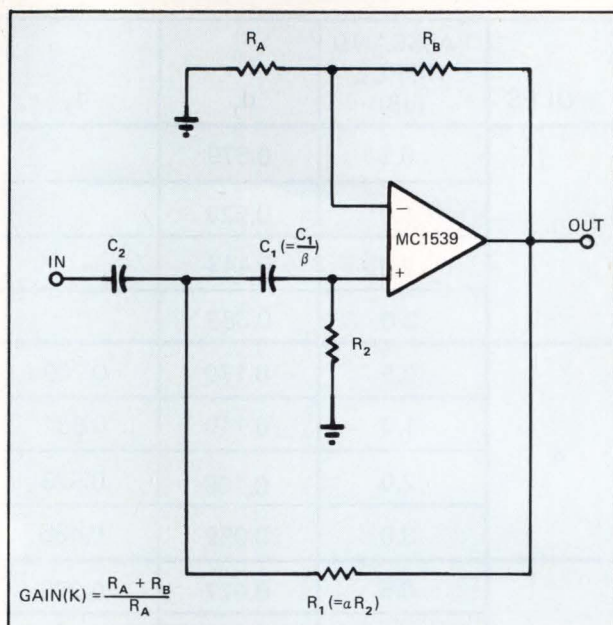


Fig. 3 — 2-pole, high-pass active filters of the configuration shown here can be designed using the same program (shown in Fig. 1) used for low-pass designs.

$$\beta = \frac{C_2}{C_1}$$

$$= \frac{1}{\alpha} [2d^2 - (1 - k + \alpha) + 2d\sqrt{d^2 - (1 - k + \alpha)}] \quad (11)$$

d = Damping Factor

$$= \frac{1 - k + \alpha + \alpha\beta}{2\sqrt{\alpha\beta}} \quad (12)$$

# POLES DAMPING FACTOR	2	4	6	8	10	12
d_1	.7071	.9239	.9659	.9808	.9877	.9914
d_2		.3827	.7071	.8315	.8910	.9239
d_3			.2588	.5556	.7071	.7934
d_4				.1951	.4540	.6088
d_5					.1564	.3827
d_6						.1305

Fig. 4 — Damping factors for even-order Butterworth filters of up to 12 poles are shown. For multiple-pole designs the section with the lowest damping factor should be the last section.

#POLES	PASSBAND RIPPLE (dB)	d ₁	d ₂	d ₃	SF ₁	SF ₂	SF ₃
2	0.5	0.579			1.231		
	1.0	0.523			1.050		
	2.0	0.443			0.907		
	3.0	0.383			0.841		
4	0.5	0.170	0.709		1.031	0.597	
	1.0	0.140	0.637		0.993	0.529	
	2.0	0.109	0.528		0.964	0.471	
	3.0	0.089	0.465		0.950	0.443	
6	0.5	0.077	0.276	0.732	1.011	0.768	0.396
	1.0	0.063	0.228	0.657	0.995	0.747	0.353
	2.0	0.048	0.176	0.505	0.983	0.730	0.316
	3.0	0.039	0.145	0.489	0.977	0.722	0.298

Fig. 5—Damping factors and frequency scale factors for Chebyshev filters of up to 6 poles are shown. Desired corner frequency is multiplied by scaling factor for each low-pass section (divided for high-pass sections), and the result is entered in the program.

K = gain

(13)

and s = Laplace transform operator.

The break frequency of the filter (ω_0) is:

$$\omega_0 = \frac{1}{R_2 C_2} \sqrt{\frac{\beta}{\alpha}} \text{ Rad./Sec.} \quad (14)$$

Multiple-pole filters

Active (even order) filters with more than two poles can be designed using this program by simply cascading several two-pole sections.

To design a higher order Butterworth filter of up to 12

- SFO

```
> LOAD GRAY
OK
> RUN
DAMPING FACTOR (D) OR PASSBAND RIPPLE (P)?
D
ENTER THE DAMPING FACTOR, D
.707
WHAT IS THE CLOSED LOOP GAIN?
5
WOULD YOU LIKE A HIGH-PASS (H) OR LOW-PASS (L) FILTER?
L
ENTER THE CORNER FREQUENCY (KHZ)
10
ENTER C2 (PF)
1000
ENTER ALPHA
1
```

BUTTERWORTH LOW-PASS FILTER
DESIGN REQUIREMENTS

BREAK FREQUENCY = 10 KHZ
CLOSED LOOP GAIN = 5
PASSBAND RIPPLE = 0 DB
DAMPING FACTOR, D = .707
BETA (B) = 6.6449927
ALPHA (A) = 1

R1 = 6.1740941 KOHMS R2 = 41.02681 KOHMS
C1 = 1000 PF C2 = 1000 PF

ANOTHER RUN?
YES

Fig. 6—Sample program run shows step-by-step design of a 10-kHz, low-pass Butterworth filter with a closed-loop gain of 5.

DESIGN SUMMARY

```
> RUN
DAMPING FACTOR (D) OR PASSBAND RIPPLE (P)?
P
ENTER THE PASSBAND RIPPLE IN DB(0 FOR BUTTERWORTH)
.5
WHAT IS THE CLOSED LOOP GAIN?
20
WOULD YOU LIKE A HIGH-PASS (H) OR LOW-PASS (L) FILTER?
H
ENTER THE CORNER FREQUENCY (KHZ)
6
ENTER C2 (PF)
2000
ENTER ALPHA
5
```

CHEBYSHEV HIGH-PASS FILTER
DESIGN REQUIREMENTS

BREAK FREQUENCY = 6 KHZ
CLOSED LOOP GAIN = 20
PASSBAND RIPPLE = .5 DB
DAMPING FACTOR, D = .58680316
BETA (B) = 3.8267166
ALPHA (A) = 5

R1 = 58.014566 KOHMS R2 = 11.602913 KOHMS
C1 = 522.64126 PF C2 = 2000 PF

ANOTHER RUN?
NO

Fig. 7—Computer printout of a sample design for a 6 kHz high-pass Chebyshev filter is shown. Gain of this circuit is 20.

```

> RUN
DAMPING FACTOR (D) OR PASSBAND RIPPLE (P)?
D
ENTER THE DAMPING FACTOR, D
.707
WHAT IS THE CLOSED GAIN?
5.02
WOULD YOU LIKE A HIGH-PASS (H) OR LOW-PASS (L) FILTER?
L
ENTER THE CORNER FREQUENCY (KHZ)
11
ENTER C2 (PF)
1000
ENTER ALPHA
1

BUTTERWORTH LOW-PASS FILTER
DESIGN REQUIREMENTS

BREAK FREQUENCY = 11 KHZ
CLOSED LOOP GAIN = 5.02
PASSBAND RIPPLE = 0 DB
DAMPING FACTOR, D = .707
BETA (B) = 6.6725403
ALPHA (A) = 1
R1 = 5.6012146 KOHMS
R2 = 37.37433 KOHMS
C1 = 1000 PF C2 = 1000 PF

ANOTHER RUN?
YES
ENTER THE DAMPING FACTOR, D
.9659
WHAT IS THE CLOSED LOOP GAIN?
1.402
WOULD YOU LIKE A HIGH-PASS (H) OR LOW-PASS (L) FILTER?
L
ENTER THE CORNER FREQUENCY (KHZ)
11
ENTER C2 (PF)
1000
ENTER ALPHA
1

BUTTERWORTH LOW-PASS FILTER
DESIGN REQUIREMENTS

BREAK FREQUENCY = 11 KHZ
CLOSED LOOP GAIN = 1.402
PASSBAND RIPPLE = 0 DB
DAMPING FACTOR, D = .9659
BETA (B) = 2.3859736
ALPHA (A) = 1
R1 = 9.3668808 KOHMS
R2 = 22.349131 KOHMS
C1 = 1000 PF C2 = 1000 PF

ANOTHER RUN?
YES
ENTER THE DAMPING FACTOR, D
.2588
WHAT IS THE CLOSED LOOP GAIN?
1.402
WOULD YOU LIKE A HIGH-PASS (H) OR LOW-PASS (L) FILTER?
L
ENTER THE CORNER FREQUENCY (KHZ)
11
ENTER C2 (PF)
1000
ENTER ALPHA
.455

CHEBYSHEV LOW-PASS FILTER
DESIGN REQUIREMENTS

BREAK FREQUENCY = 1 KHZ
CLOSED LOOP GAIN = 1.402
PASSBAND RIPPLE = 6.0211932 DB
DAMPING FACTOR, D = .2588
BETA (B) = .31241489
ALPHA (A) = .455
R1 = 17.460941 KOHMS
R2 = 5.455058 KOHMS
C1 = 2197.8022 PF C2 = 1000 PF

ANOTHER RUN?
NO
(@82) >

```

Fig. 8—Six-pole, low-pass Butterworth filter with a gain of 9.87 is designed in just three program passes. Without the assistance of this program, many hours of tedious calculation would be required for a design of this complexity.

poles, see **Fig. 4**, which gives the required damping factors for each section. (To prevent amplifier saturation the section with the lowest damping factor should be the last filter section.)

To design a higher-order Chebyshev filter (up to 6 poles) refer to **Fig. 5**, which gives the required damping factors and corner frequency scaling factors for each section. Simply multiply the desired corner frequency by this scaling factor and enter the resulting frequency for each low-pass filter section or divide by the scaling factor for each high-pass section. The overall filter will then have the required 3-dB corner frequency.

Running the program

The first question asked by the program is whether you would like to specify the passband characteristic in terms of the damping factor (enter a "D") or passband ripple (enter a "P"). Depending on the answer to this question, the computer then requests the required entry. The program then asks for the desired gain and whether a high-pass (enter "H") or low-pass (enter "L") filter is desired. Next, the program asks for the desired corner frequency (in kHz) and the value of C_2 . (See **Fig. 2** for low-pass filter and **Fig. 3** for high-pass filter). Finally, the program requests the desired α (see Eq. 2 for the low-pass filter and Eq. 10 for the high-pass filter). Note that from Eq. 4 (also from Eq. 11) it is necessary that $d^2 - (1 - k + \alpha) > 0$, to avoid taking the square root of a negative number. If, for a given d (damping factor) and K (gain), an invalid value of α has been entered, the program gives a warning, prints the maximum allowable value of α , suggests a smaller value, then

loops back within the program to allow a new α to be entered without re-entering all of the other filter parameters. After a valid α has been entered, the computer prints a summary of the filter parameters and required values of resistors and capacitors.

The computer output shown in **Fig. 6** is an example of the design of a 10-kHz low-pass Butterworth filter, with a gain of 5. A design for a 6-kHz high-pass Chebyshev filter with 0.5-dB passband ripple and a gain of 20 is shown in **Fig. 7** and an 11-kHz, 6 pole Butterworth low-pass filter with a gain of 9.87 in **Fig. 8**. In these examples, the information entered by the user is underlined. □

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1. Ghausi, M., "Principles and Design of Linear Active Circuits," McGraw-Hill (N.Y.) 1965, Chapter 4.
2. "The Op Amp and Active Filter Handbook" Motorola Semiconductor Products, Inc.
3. Ioannides, P.G., "Design Complex Active Filters," EDN/EEE March 15, 1972, pp. 53-54.

Author's biography

Charles Williams is a staff engineer at Singer-Kearfott Div., in Pleasantville, N.Y. He is responsible for circuit design for airborne doppler navigation systems. He received both his BE and MSEE degrees from New York University.



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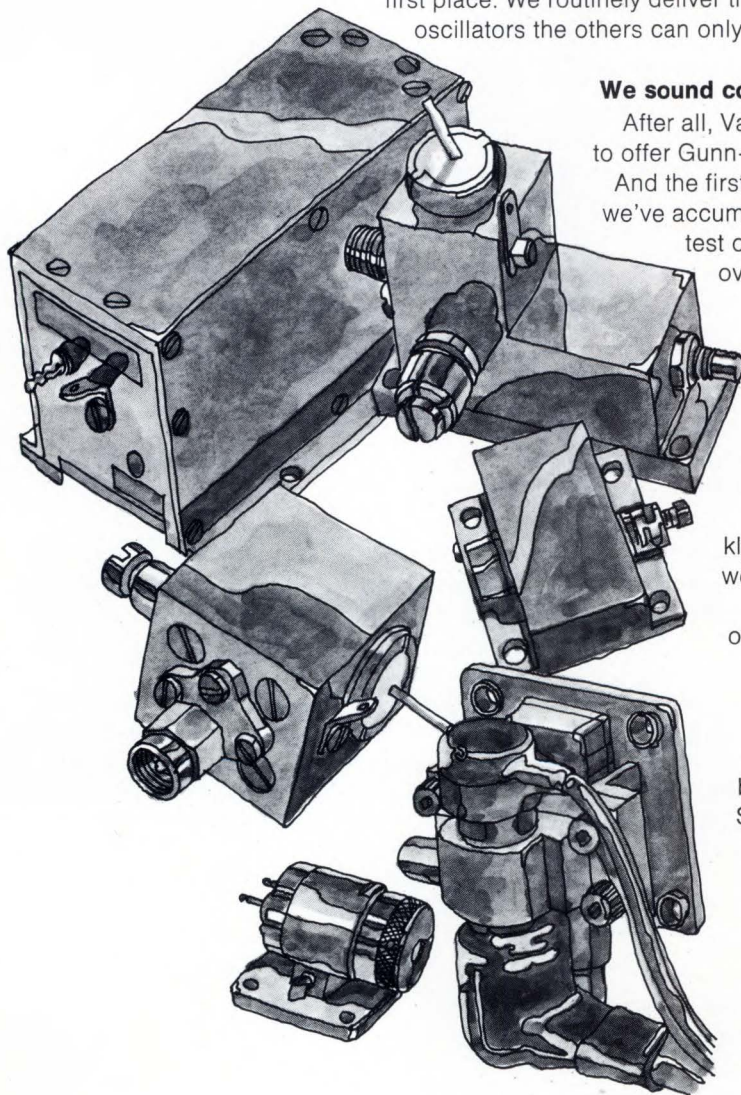
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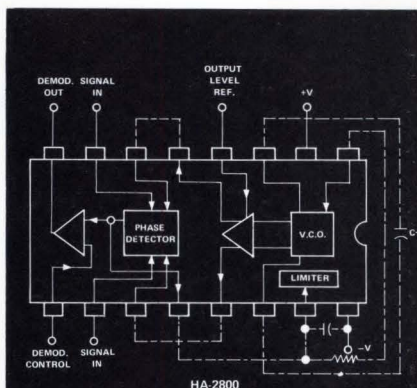
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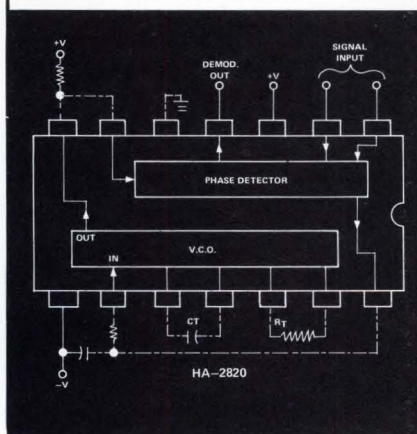
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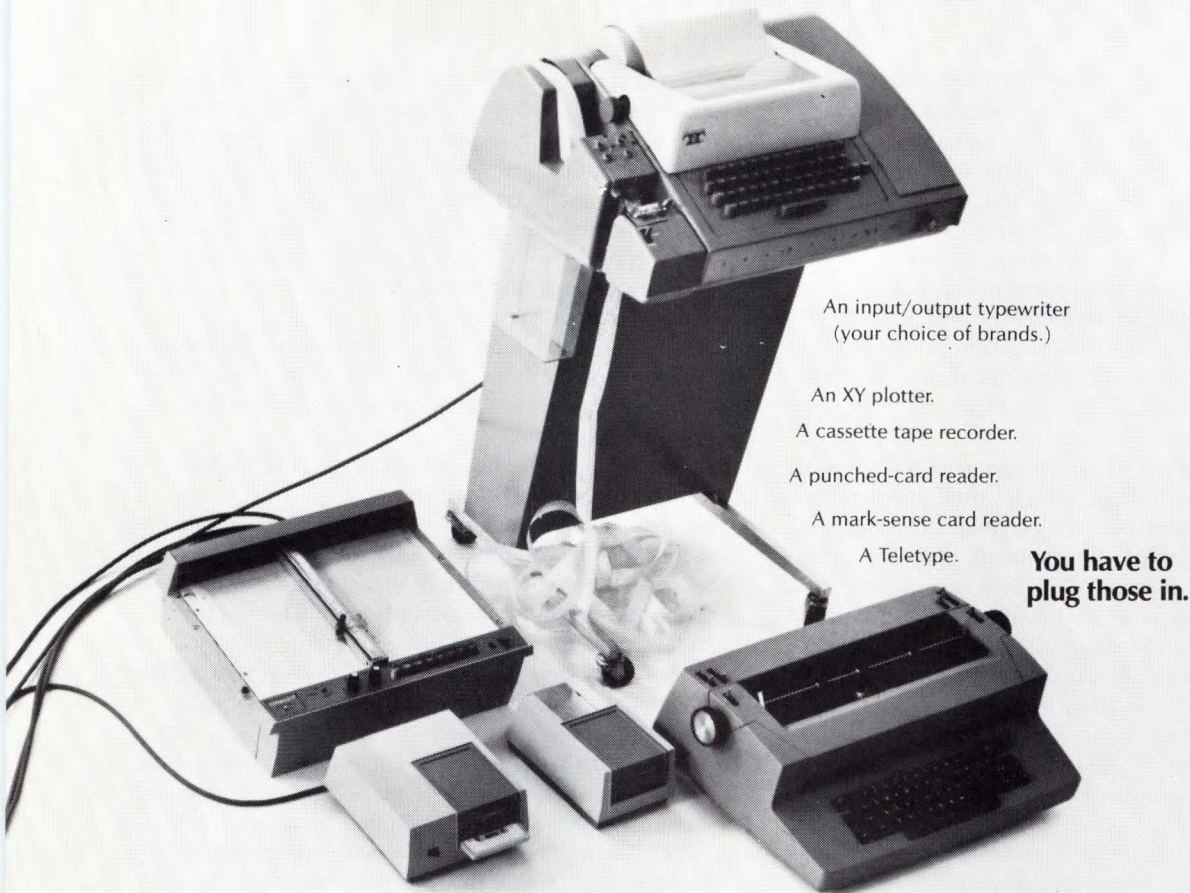
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Quad flip-flop wins National/EDN Tri-State™ logic design contest

For all of you who entered the Tri-State™ logic design contest, sponsored by National Semiconductor and EDN, here are the long awaited results. The winning circuit was submitted by Mr. Vedon Otto of General Dynamics, Fort Worth, Texas. The design he suggested is a quad flip-flop with two Tri-State input/output pins per flip-flop. As promised, Mr. Otto wins a U.S. Tri-State trip, allowing him and a companion to fly to any three states of his choice.

Mr. Otto is presently on assignment in Alaska with General Dynamics and EDN has been unable to contact him to learn his reaction or choice of states that he will visit. His prize-winning design is shown in Fig. 1.

The runners up are:

- Second: Joseph Petit of G.E. in Syracuse, N.Y. for his design "A bipolar data bus switch" used to transmit or receive on a common bus between two data processors.
- Two men tied for third with essentially identical entries: Gary L. Anderson of Trans-A-File System Company, Santa Clara, Calif. and James M. Kasson of Hewlett-Packard in Palo Alto, Calif. who designed "Hex bidirectional bus transfer gates" which result in a 4-to-1 reduction in package counts in bus oriented processors.
- In Fourth place two people had similar circuits: Philip C. Norem of Autotelic Industries in Buffalo, N.Y. and David M. Barton of Develco, Emtel Div., in Mt. View, Calif.

In examining the entries, we became aware of some things we hadn't anticipated. Namely, that Tri-State as a concept was not fully understood by many of the people who entered the contest.

As the functions available inside packages become more complex, the IC part count in digital systems, has dropped steadily. The appropriate use of Tri-State logic

has been a big factor in the reduction of the number of ICs used per system, while still using general-purpose MSI parts. For example, National has done test designs using Tri-State parts that are available or will be coming out soon to functionally duplicate two well known and very similar minicomputers. The total IC part count for the test design was about sixty, which compares to 300 ICs for a three-year old computer design and 130 ICs for an eighteen month old computer design.

Exercises like this help IC companies gain insight into the features which make parts useful. In the light of this type of experience, Mr. Otto's circuit was judged the most useful entry submitted.

In general, those who entered the contest could be placed in one of three categories:

First, those who obviously used Tri-State parts in the past and were suggesting new and better devices.

Second, those who had built digital systems in the past but who did not fully understand how to best apply Tri-State logic to improve their system performance. As a result, they suggested the use of Tri-State in places where conventional TTL would have been perfectly adequate.

And third, those who tried to use Tri-State as a circuit tool rather than a system tool. For example, one entrant used Tri-State in a number of places inside a proposed device to performed what amounted to a simple "OR" function. The part he described would have performed an interesting function, but this was not a good way to apply Tri-State logic.

Characteristics overlooked

The judges also felt that some of the characteristics of Tri-State were being overlooked by prospective users. For

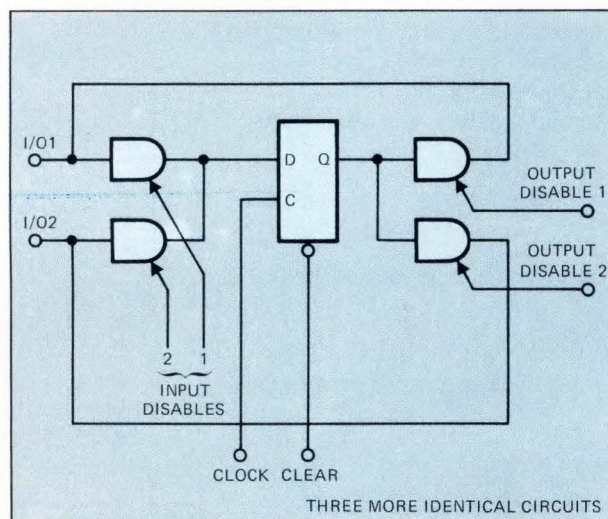


Fig. 1—Winning design in the National Semiconductor/EDN Tri-State™ logic design contest is this quad D-type flip-flop with two Tri-State input/output pins per flip-flop. National plans to produce this device, with slight modifications, as a standard product.

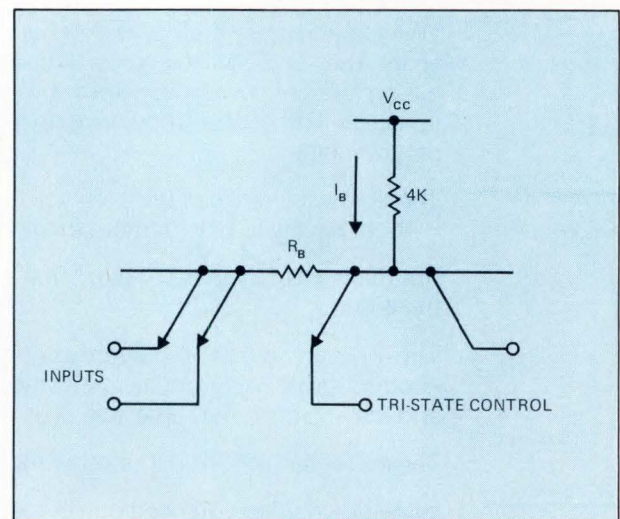


Fig. 2—Tri-State devices, when put into the high-impedance state, exhibit high input, as well as output, impedance due to the multiple emitter input transistor. The Tri-State control will then sink all the base current, while the input pins see only leakage currents.

example, when a Tri-State device is put into the high impedance state, the input becomes a high impedance as well as the output. This is due to the design of the multiple emitter transistor at the input as shown in Fig. 2.

By physically locating the Tri-State control emitter closer to the resistor coming into the base, this emitter will always hog all of the base current, I_B , when it and the data input emitters are in the low state.

Since the base region of this transistor is a semiconductor material with a finite resistance per square, the further away an emitter is from the base resistor contact, the higher the voltage drop from input to base for a given current. The result is that the Tri-State control input sinks all of I_B , while the input pins see only leakage current.

Another feature of Tri-State logic that most people are not aware of is the ability of the output, when in the disabled state, to clamp transmission line undershoots.

Let's say that a Tri-State part is at the end of a fairly long wire (i.e. ten feet) and that it is in the high impedance mode. Let's also say that a signal is being transmitted from the other end of the run to some device near our circuit. There is no termination resistor anywhere on the run. If the signal rings at the end of the line, the disabled Tri-State circuit will clamp undershoots trying to go below -0.4V. A look at the basic Tri-State circuit will show why (see Fig. 3)

Since the output is in the high-impedance state, Q_1 must be "on," with its collector voltage approximately 0.3V, and the base of Q_2 is at about 1.0V. If there is ringing on the line, V_{OUT} can go below ground, but as soon as it goes more negative than two diode drops below the base of Q_2 , both Q_2 and Q_3 turn on. This initial clamping occurs at about 0.4V below ground, with a current of about 50 mA coming from V_{CC} through R_1 . If V_{OUT} still continues more negative, hundreds of milliamps of clamping current are available when V_{OUT} goes more than one diode drop below ground. At this voltage, the collector of Q_4 looks like the cathode of a diode whose anode is the substrate of the chip.

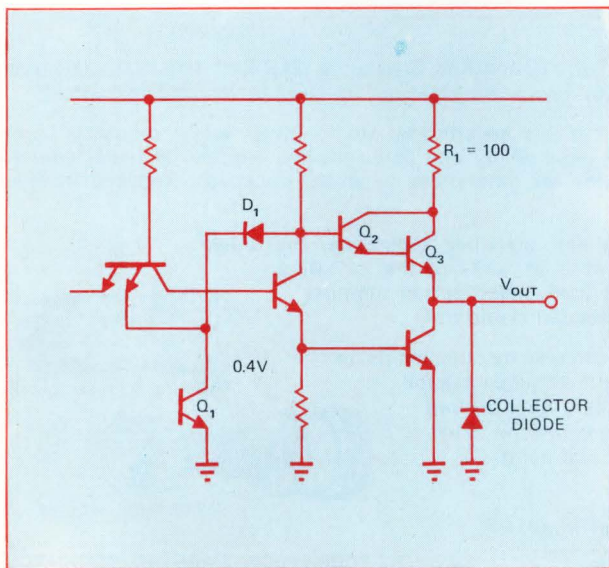


Fig. 3— Bonus feature, often overlooked in Tri-State designs, is the ability of Q_2 and Q_3 to provide current to clamp negative spikes when in the high-impedance state. This permits the use of long, unterminated transmission lines without fear of excess ringing.

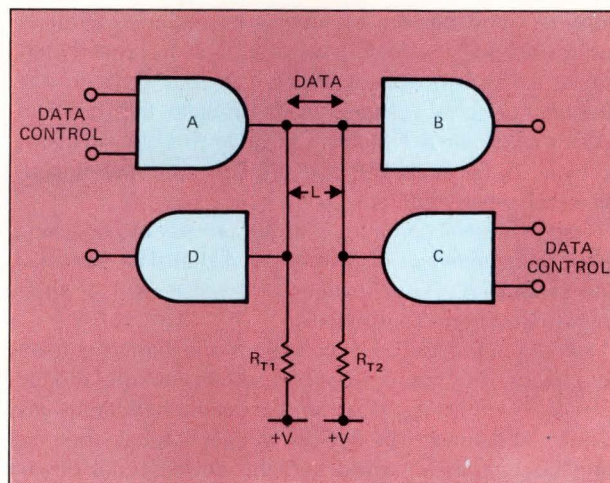


Fig. 4— Bus organized systems, such as the one shown here, require $2(L)$ propagation delays when terminating A-to-B transmission before beginning C-to-D transmission. This is a point which many designers missed in the Tri-State contest.

Long lines can be driven unterminated

While on the subject of data transmission, another feature of Tri-State logic can be discussed. Since Tri-State can absorb transmission line undershoots, fairly long lines can be driven unterminated.

Let's examine a bidirectional line using any transmitter and receiver technique that requires terminating resistors (open collector, for example). This could be the bus in any bus organized system similar to the one in Fig. 4.

Assume that the control signals at both ends of the line which determine the direction of data transfer are coincident and opposite. Assume also that A has been transmitting a "0" to B. At a point in time, the control signals stop the A-to-B transmission and start the C-to-D transmission, with C also transmitting a "0" to D. When can D be sure that it has received C's signal? "Immediately" is not the answer. One propagation delay equal to line length L is not the answer either. Twice the propagation of line length L is the answer.

The reason for the double delay is that when A is inhibited it becomes a high impedance and the voltage at the input to D rises rapidly toward $+V$ due to the termination R_{T1} . At the same instant, C has become a low impedance and its output is at a "0". However, C is doing no work because the signal from A is still holding down C's end of the line.

After one propagation delay, the signal generated by the termination R_{T1} reaches C's end of the line. Then, and only then, does C begin to drive the line. C's "0" now begins to propagate back toward D's end of the line. The effect has been a pulse $+V$ volts in amplitude at D's end of the line lasting for two lines propagation delays. Try it, you'll see it.

This means that, effectively, the propagation delay for that line is twice what it should be for its length. The main source of this problem is, of all things, the termination resistors. With no termination resistors, the distributed capacitance will cause the voltage on the line to change very slowly (relative to the line length) when either end of the line becomes a high impedance. Then, either A or C begins driving the line immediately and the data can be sampled at the other end after only one propagation delay.

However, most bus driving techniques require a termination resistor to set a logic level as well as to properly terminate a line, since most drivers can only drive in one direction (to one voltage). With Tri-State this problem doesn't exist, since Tri-State can drive in both directions (to either of two voltages) and still go into a high-impedance state when required.

(National Semiconductor is in the process of publishing application notes which will cover digital data transmission in general. These features of Tri-State will be thoroughly described in those notes.)

A final point about Tri-State logic is one that is not readily obvious. Tri-State devices can sustain multiple shorted outputs to either V_{CC} or ground indefinitely without any permanent damage. The devices will get hot, but when the short circuits are removed and the devices cool down, they will again perform according to specification. A report on the effects of short circuits on Tri-State devices is available at this time from National Semiconductor Corp.

In conclusion, we would again like to congratulate Mr. Vedon Otto, wherever he may be, for winning the National Semiconductor-EDN Tri-State Design Contest. We would also like to congratulate the runners up and to publically thank all those who took the time to enter this contest. □

The staff of EDN would like to thank Stephen Calebotta of National Semiconductor Corp. for his assistance in judging entries in the Tri-State contest, and especially for preparing this report and analysis.

Winning entry to become standard Product

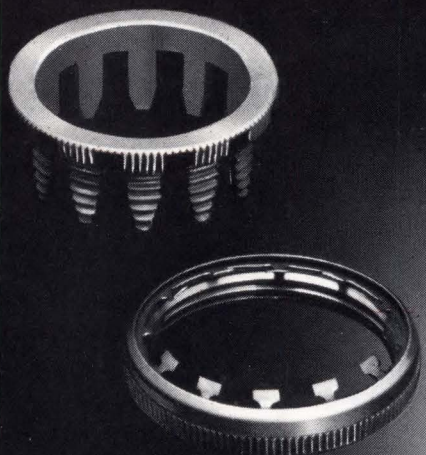
National Semiconductor Corp. is in the process of building the winning circuit with some minor changes. The key change will be the use of gated D flip-flops similar to those used in the DM8551 as opposed to the normal D flip-flops as shown in the logic diagram.

The reason for this change is that the normal D flip-flop stores whatever is at the data input (ignoring setup times) whenever the clock input goes from a logic "0" to a logic "1". In order to retain data in the flip-flop and still be able to change the data on the input line, the clock must be inhibited. Those designers who have tried, are aware of the problems associated with gating a system clock. (Clock skew due to propagation delays, inversion, etc.).

A better idea is to apply system clock all the time and to gate the data instead. With the gated D, there is logic on the chip which permits the signal that would have controlled the clock line on the normal D flip-flop to control the data presented to the input of the gated D flip-flop, either new data or the Q output fed back. There is an increase in the minimum input setup time, however, but this is less of a problem than gating the clock.

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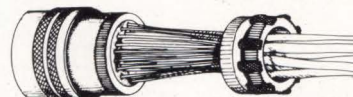
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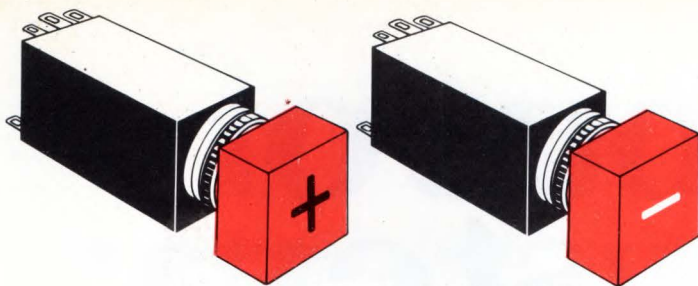
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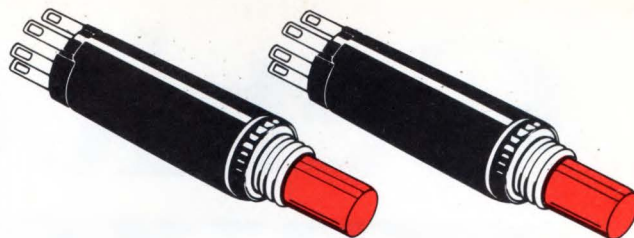
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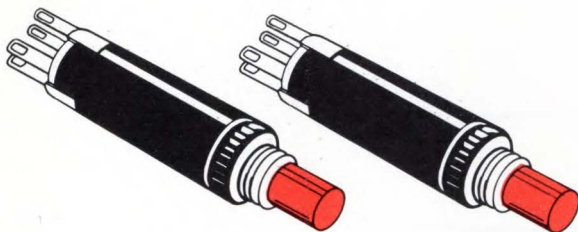
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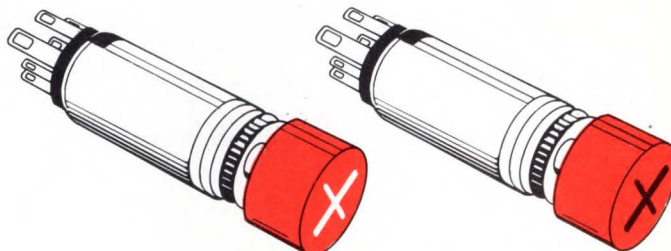
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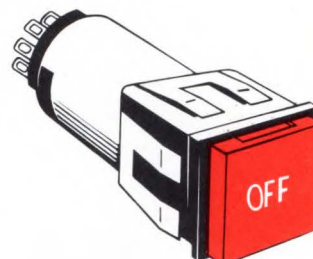
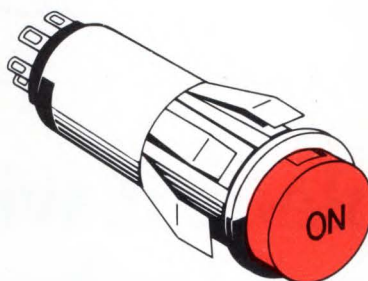
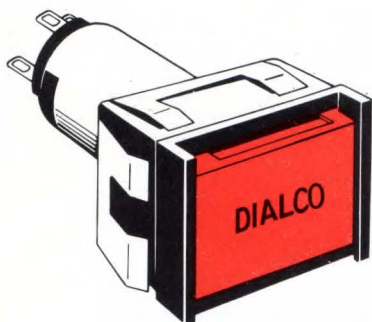
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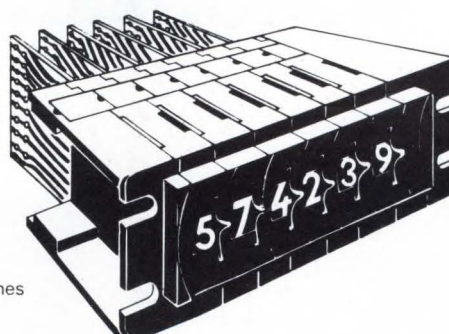
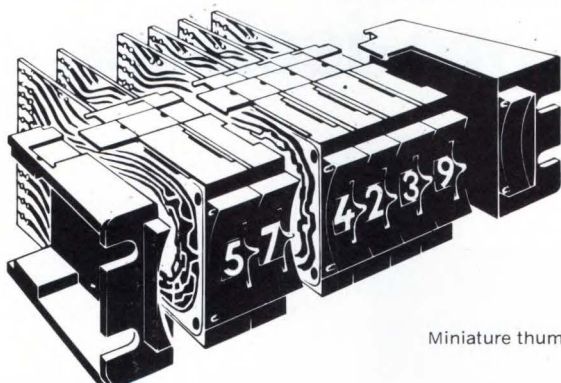
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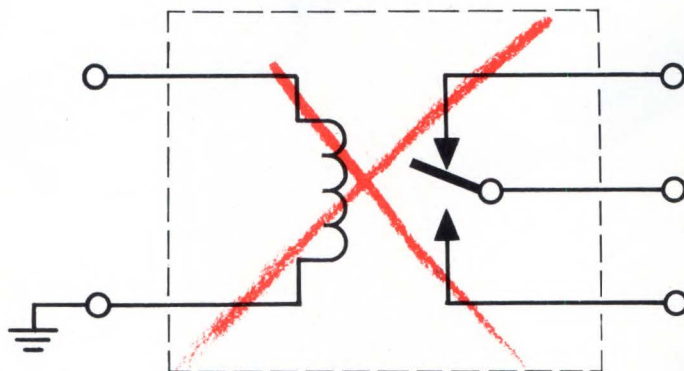
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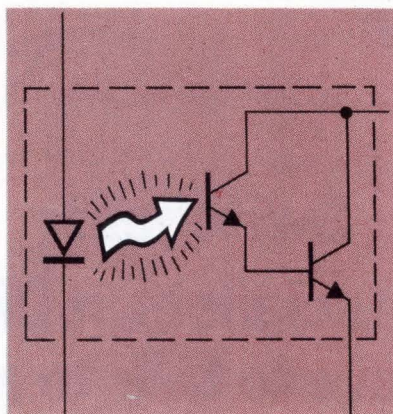


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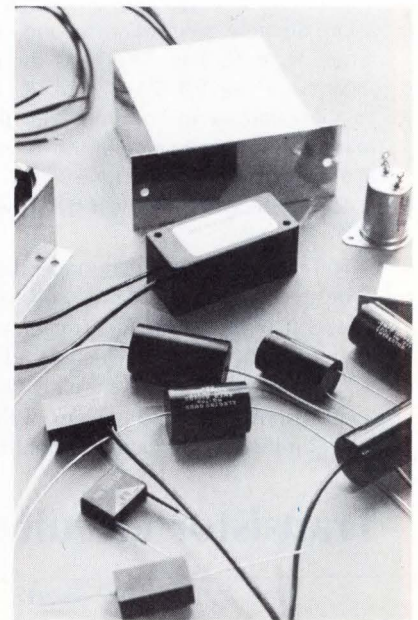
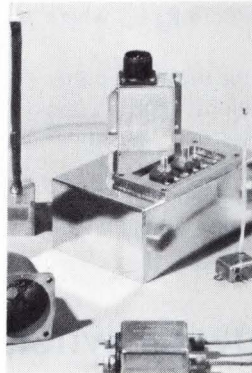
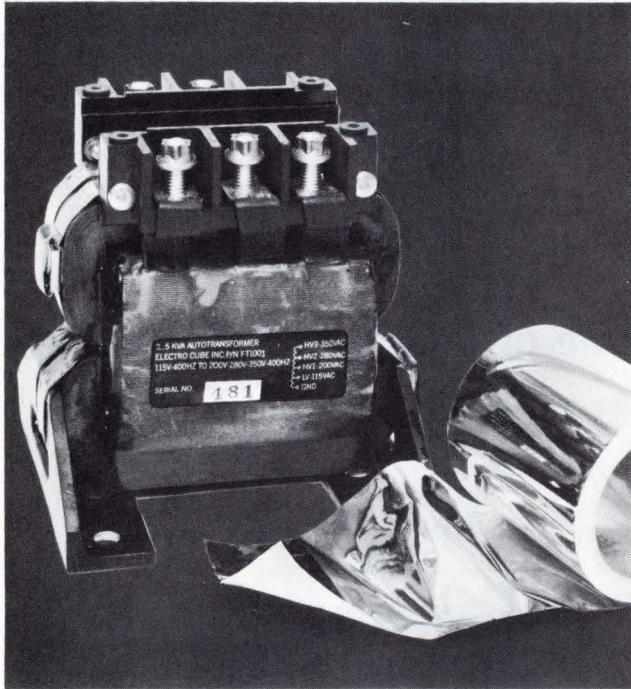
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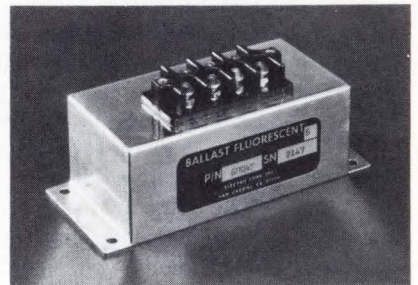
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CIRCLE NO. 19

CIRCUIT DESIGN AWARDS

One shot multivibrator has delayed output

Louis Sims

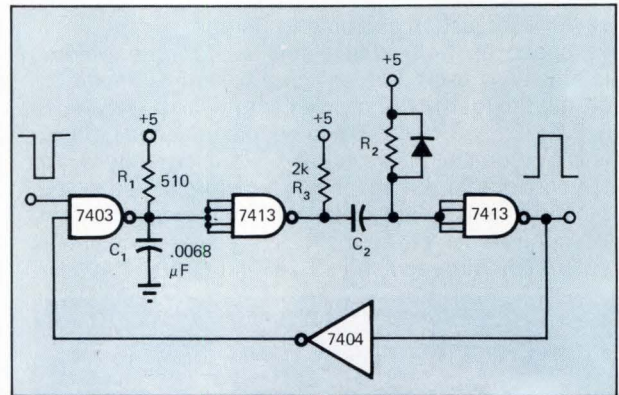
Key Tronic Corp. Spokane, Wash.

This circuit will generate an output pulse after a delay of approximately one microsecond. Delay $\cong 0.36 R_A C_1$, where $R_A = R_1 \parallel 4k$. The 4k is the internal equivalent resistance of the TTL 7413 gate. R_1 may be chosen much smaller than 4k to "swamp" out the effects of the large manufacturing tolerance of the 4k resistance and to arrive at a more accurate delay time.

The pulse width is given by: $T_{pw} \cong 0.36 R_B C_2$, where $R_B = R_2 \parallel 4k$.

This can be made much longer than the triggering pulse, if desired. Again the same considerations apply in the selection of R_2 as for R_1 . Trigger pulses that are shorter than the delay time are rejected and will cause no output.

Recovery of the delay circuit is Beta limited by the 7403 output transistor. Full recovery of the pulse timing circuit is determined by the time constant for $R_3 C_2$. □



Delayed pulse generator, in this case set for approximately 1 μ sec, can be set for other delay times by varying R_A and C_1 . Output pulse width is set by varying R_B and C_2 .

To Vote For This Circuit
Circle 150

Transistor circuit speeds synch time of phase-locked oscillator

J. S. Swartz

IBM Corp., San Jose, Calif.

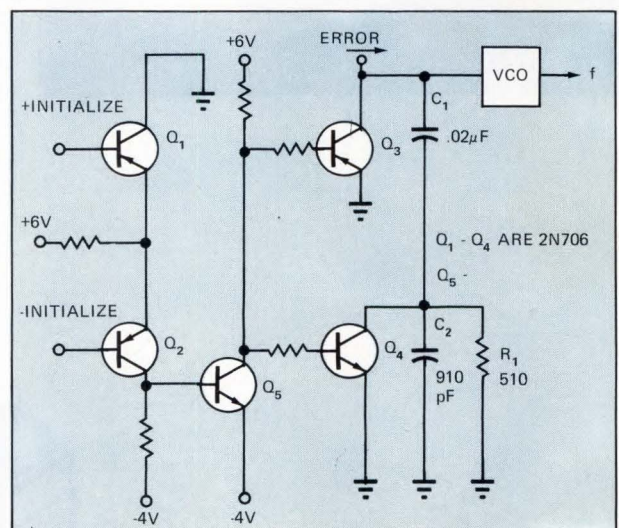
This circuit can reduce maximum synchronization times of a phase-lock oscillator (PLO) by as much as half. For applications where variable data transmission rates are encountered and the PLO must be synchronized rapidly the circuit offers outstanding improvement in performance.

The circuit includes a compensation network consisting of series capacitors C_1 , C_2 and a resistor, R_1 , coupled between the two capacitors and to a reference potential, such as ground. The compensation network serves as a filter for the voltage-controlled oscillator (VCO), which provides a signal of nominal frequency subject to error correction for phase locked operation. The stored voltage on C_1 , C_2 is proportional to the frequency. If a PLO must be switched from an extreme frequency above or below the nominal center frequency to another data source on the opposite side of the center, the switching time can be reduced by initializing the voltage on C_1 , C_2 to the nominal center frequency (OV) before synchronization is attempted. This reduces the maximum time needed to acquire final synchronization.

During operation, an initialization pulse is provided to complementary input transistors Q_1 and Q_2 , causing transistors Q_3 and Q_4 , connected to the capacitors, to saturate. As a result, the capacitors are forced to ground. The initial

frequency deviation of the PLO is thus cut substantially, reducing synchronization time effectively. □

To Vote For This Circuit
Circle 151



Rapid synching of a phase-locked oscillator is enhanced with this switching circuit that provides potential control of the VCO.

Constant-current generator speeds up wired-OR circuits

Peter Alike

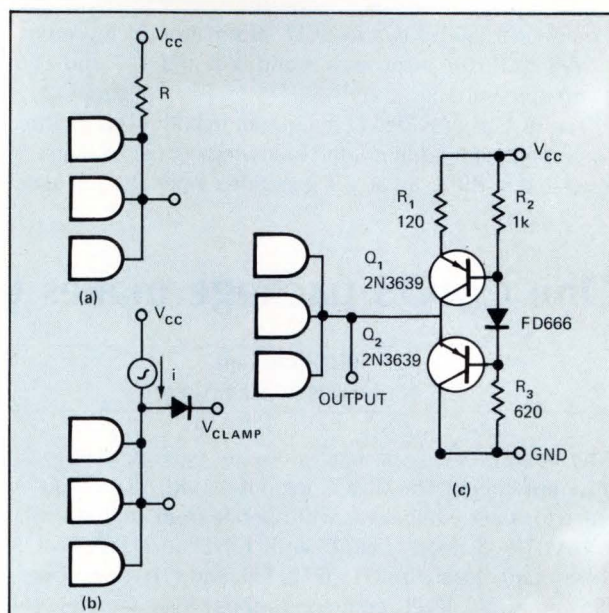
Fairchild Semiconductor Mountain View, Calif.

Open collector outputs allow easy expansion of digital integrated circuits, particularly memories, by facilitating a common bus output interconnection from many devices and allowing the activation of only one device at a time.

The output transistor of the activated device can pull the common bus LOW and a single pull-up resistor can pull it HIGH. For high-speed operation, the value of this resistor should be as low as is consistent with the fan-out (current sinking) capability of each IC, typically 16 mA as shown in Circuit "A".

While a resistor is the most economical pull-up device, it has two drawbacks: The current available to charge the stray and load capacitances decreases as the output rises; and the bus voltage rises exponentially to V_{CC} . This is much higher than necessary to insure proper TTL noise margins.

The ideal pull-up device would be a constant-current generator plus a clamp preventing the output voltage from exceeding +2.4V, as in circuit "B". The circuit shown in "C" implements this concept. Q_1 acts as a constant-current generator (16 mA) and Q_2 acts as a clamp when the output voltage reaches 2.4V. With a light capacitive load of 100 pF the response time is only slightly improved; but with a 500-pF load, rise time is decreased by 11 nsec and the fall time by 24 nsec (measured as a decreased delay at the output of the read gate), which is a significant improvement for the cost of three additional resistors and two PNP transistors. □



Open collector gates in a wired-OR configuration normally use a pull-up resistor, as in circuit A above, bringing the output bus to V_{CC} . Since the required input to subsequent stages is only +2.4V, the clamped constant-current scheme in circuit B will provide faster switching. Circuit C is a practical equivalent of circuit B, providing an 11 nsec improvement of risetime when driving a 500-pF load.

To Vote For This Circuit
Circle 152

2 TTL packages convert BCD up-counter for down counting

Jack Sellers

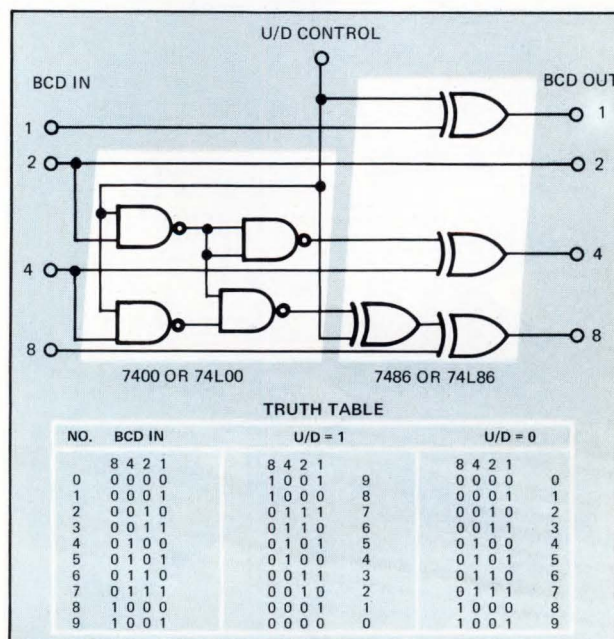
Mostek Corp., Carrollton, Tex.

This circuit illustrates a unique, inexpensive approach to providing a choice of up or down count from a normal up counter. This avoids the requirement of the more expensive up/down counters where a simple down count is desired. The trend to MOS multi-counter circuits makes this circuit a practical means to obtain low-package-count and still provides both up- and down-count capability from the standard up-counter.

The circuit does not provide full up/down counter capability; that is, one cannot count up to a certain count and reverse direction to count back down. However, many applications for up/down counters are such that they are always operated in an up-count or always in a down-count mode. Several applications, including digital voltmeters, require the up/down mode to change on a cyclic basis with this change occurring following a reset condition. It is for these applications that this circuit is intended.

Two packages are all that's required to achieve this conversion of a up-counter (e.g. Mostek's MK 5002 P/MK 5007 P) to a down-counter from the reset condition.

The circuit shown accepts true BCD in and provides the following output dependent on the state of the U/D control:



Standard or low-power TTL can be used to implement this 9's complement BCD generator. The low power versions will be more desirable if you are driving an MOS BCD up-counter. As seen in the truth table, only one control bit is required to set the conversion circuit for up or down counting.

U/D = Logic 0 (LOW) allows the data at the input to appear in the same true logic state at the output also.

U/D = Logic 1 (HIGH) adds the complement of the number 9 (0110) to the BCD information at the input. Adding 0110 transposes a 9 and 0, 8 and 1, 7 and 2, 6 and 3, 5 and 4.

True BCD is provided at the output in both cases. During 9's complement addition, the following is true: No carry is generated in Bit 1; a carry is generated when Bit 2 is logic

1 and the carry is added to Bit 4; a carry from Bit 4 is generated anytime Bit 2 carries or Bit 4 is a logic 1 with this carry added to Bit 8.

A mode change at any time other than reset would not necessarily provide a useable count output. □

To Vote For This Circuit
Circle 153

One CMOS package makes universal logic probe

Phillip Bryant
Nashua, New Hampshire

Why design, or buy, a logic probe for each type of logic you must check? The CMOS logic ICs in RCA's CD4000A series (or their equivalent) will operate from supplies of 3 to 15V. The defined "ZERO" and "ONE" levels for CMOS correspond closely to RTL, DTL, TTL and HTL when operating at the V_{cc} levels common to those logic families, but a level translator will be required for ECL interfaces, or for any logic levels over 15V. One very attractive feature if you're using CMOS for probing around logic circuits is that its input impedance—typically $10^{12}\Omega$ —isn't likely to disturb the circuit under investigation.

The CD4009AE hex buffer costs a little over \$4 in small quantities, and as shown in Fig. 1 only 2 resistors and 2 LEDs are required to convert it into a logic probe. The basic circuit consists of inverters B, F & E in a Schmitt trigger configuration. Resistor R_1 prevents latch-up of the circuit, and its value is somewhat arbitrary. If R_1 is less than

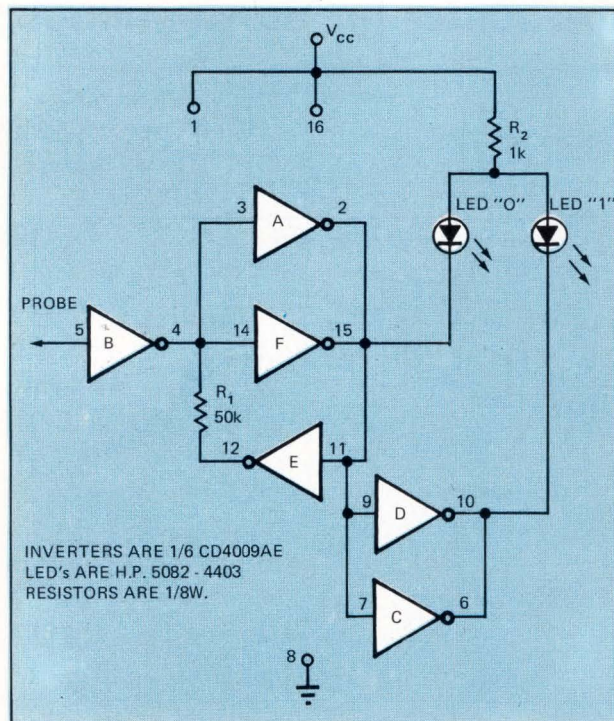


Fig. 1—CMOS logic probe features $10^{12}\Omega$ input impedance and covers 3 to 15V range. While LEDs are visible at all voltages, a 1 k Ω pot in place of R_2 will allow user to increase brightness at lower voltages.

50 k Ω , switching speeds can be increased, but hysteresis will be introduced into the circuit. Inverter D merely provides an output complementary to the Schmitt trigger, and inverters A and C provide extra current sinking capability to drive the LEDs. □

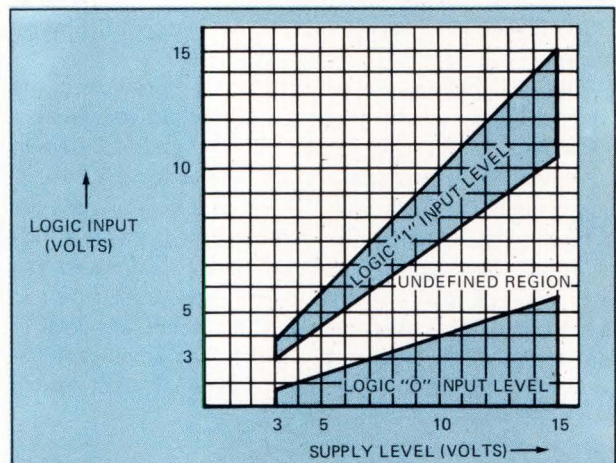


Fig. 2—Logic levels of CMOS gates vary directly with supply voltage. The undefined region shown here for a single gate is greatly reduced in the circuit in Fig. 1 because of the regenerative feedback through inverter E in the Schmitt trigger.

To Vote For This Circuit
Circle 154

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CIRCLE NO. 29

Are your worst-case tests for core memory delta noise valid?

Many "worst-case patterns" are invalid because they ignore the significance of the addressing sequence of the information test pattern

Phil Harding, Electronic Memories

Delta noise is the major nemesis of core memories. It is the penalty of coincident current caused when a matrix of cores is selected by the coincidence of one of many X lines and one of many Y lines. Because of this selection efficiency, there are many unselected cores excited by half current amplitudes. Each of these cores generates a noise, which in sum with other cores, becomes significant.

Memory designers and applications people evaluate core memories by generating an information pattern and addressing sequence which is called "worst-case patterns." Most frequently the tests generated are not truly worst case because they ignore or do not appreciate the significance of the sequence. An appropriate evaluation of a core memory must delve into a number of significant characteristics:

- Hysteresis loop characteristics
- Matrix of core outputs
- Sequence of events
- Delta noise wave shapes

A review of these characteristics will expose the deficiencies of many acceptance tests, and will give a generalized understanding of the problem so that valid tests can be generated.

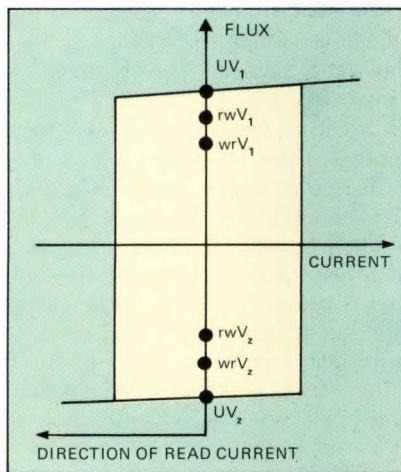


Fig. 1—Six-state model of a core hysteresis loop helps analyze memory behavior.

- uV_1 —Location of core flux prior to a read due to a full write '1' insertion.
- rwV_1 —Location of core flux after a single or many half read ($I_{x'}$, $I_{y'}$, $I_{inhibit}$) pulses followed by half write pulses ($I_{x'}$, $I_{y'}$). The core was initially set into the '1' state.
- wrV_1 —Location of a '1' core flux after a half read disturb.
- rwV_z —Location of a '0' core flux after successive half reads ($I_{x'}$, $I_{y'}$, $I_{inhibit}$), followed by half writes ($I_{x'}$, $I_{y'}$, $I_{inhibit}$).
- wrV_z —Location of a '0' core flux, which was previously write disturbed out of the undisturbed '0' state (UV_z), further displaced by many successive half read disturbs ($I_{x'}$, $I_{y'}$, $I_{inhibit}$).
- UV_z —Location of core flux after a full read.

An analysis of hysteresis loop characteristics

A true hysteresis loop depiction of a memory core involves more than the six states shown in Fig. 1. However, the six-state model is usually sufficient to properly analyze memory behavior. As can readily be seen, the worst X or Y read delta noise will occur if all the positive signal cores excited by the X or Y read current are in the rwV_1 state, while all the negative signal cores are in the wrV_z state, or vice versa.

Lines $X_1, X_2, \dots, X_i, \dots, X_m$ shown in the symbolic mapping of the Kth bit plane of either a 2-1/2D or 3D memory in Fig. 2, represent the mX access lines. Lines $Y_1, Y_2, \dots, Y_j, \dots, Y_n$ represent the nY access lines. The intersection of X_i and Y_j represents the selected address bit. The significance of the quadrants shown are:

Quadrant I—includes the cores on the sense line which intersect X and Y access lines in the direction to produce positive outputs from both X read and Y read current excitations.

Quadrant II—includes cores which intersect in the direction to yield positive outputs from X read and negative outputs from Y read current excitations.

Quadrant III—includes cores which intersect in the direction to yield negative outputs from both X read and Y read.

Quadrant IV—includes cores which intersect in the direction to yield negative outputs from X read and positive outputs from Y read current excitations.

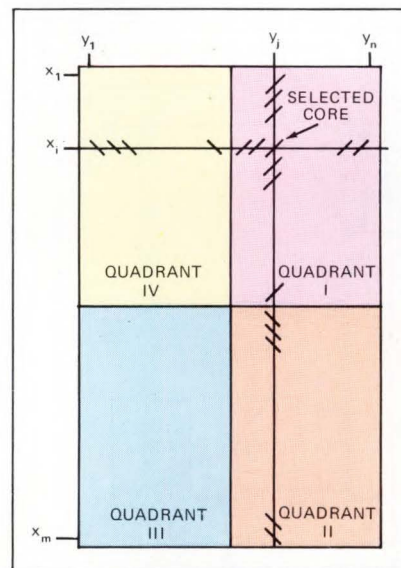


Fig. 2—Matrix of core outputs shows core sense polarities of the Kth bit plane.

The worst-case delta noise occurs if the following is true:

- All cores along selected X_i line in quadrant I are in rwV_1 state.
- All cores along selected Y_j line in quadrant I are in rwV_1 state.
- All cores along selected X_i line in quadrant IV are in rwV_z state.
- All cores along selected Y_j line in quadrant II are in rwV_z state.

An equivalent but opposite in polarity worst-case delta noise occurs if the states in quadrant I are exchanged with quadrants II and IV.

It is difficult to generate the above conditions. Normal sequential addressing cannot be used because the delta noise is eliminated along the selected access line which is being repeatedly selected.

How to generate a worst-case sequence

The following is one example of how the previous analysis can be used to generate a worst-case sequence in a 3D core memory.

- Write "1"s in quadrants II and IV. All cores in these quadrants are left in the rwV_1 state.
- Write "0"s in quadrant I. All cores in quadrant I are left in rwV_z state except for the last X or Y access line. This last line of cores is left in the rwV_z state (approximation). All the cores in quadrant II and IV are left in the rwV_1 state.
- Write "1"s in quadrant III. All cores in quadrants II and IV are left in the rwV_1 state. Cores in quadrant I are unaffected.

This sequence leaves all quadrant I cores in the rwV_z state except for one line of cores. It also leaves all cores in quadrants II and IV in the rwV_1 state. When a core in quadrant I is addressed, the X read current will cause a large negative sense noise in quadrant II, and a small positive noise in quadrant I. Similarly, the Y read current will cause a large negative sense noise in quadrant IV, and a small positive noise in quadrant I. Thus, large negative Y and X delta noise pulses will be generated. Once quadrant I is addressed, the entire sequence must be regenerated to reintroduce the worst-case delta noise.

The delta noise generated from either X or Y read half-

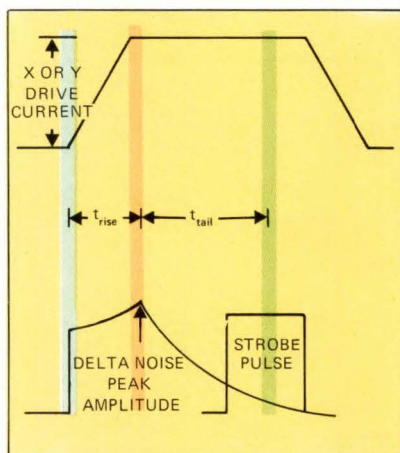


Fig. 3—The important parameters of a delta noise waveshape are t_{rise} and t_{tail} .

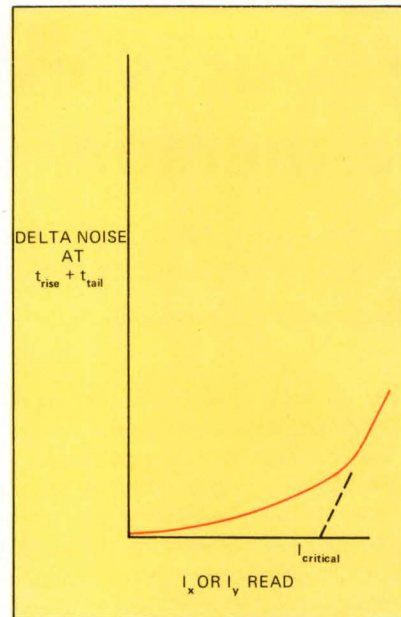


Fig. 4—Delta noise at strobe time stays within bounds if drive current is kept below $I_{critical}$.

select currents are illustrated in Fig. 3. The important parameters to observe are:

- Current rise time (t_{rise}). Maximum delta noise occurs at the end of this time interval.
- Delta noise tail time (t_{tail}). After the current rise time, the delta noise diminishes approximately toward zero exponentially. The amplitude of the delta noise during the strobe interval is the signal which causes decreased memory performance. The delta noise peak amplitude has little influence on performance if the memory lines are properly dampened, and ringing is prohibited.

The amplitude of delta noise during strobe time, or at $t_{rise} + t_{tail}$ after start of current, behaves as shown in Fig. 4. Unless the drive current is above $I_{critical}$, the delta noise during strobe time does not increase significantly as the current is increased. $I_{critical}$ is usually less than the coercive force current for the core. However, the delta noise peak during the current rise time in Fig. 3 does not demonstrate as sharp a change in slope when drive current is increased. Therefore, it is misleading to simply look at the peak delta noise. It is also misleading to look at only the delta noise at one value of current. If the current used to test the cores is below $I_{critical}$, the noise will appear to be lower than it is in actual system performance. Occasionally, cores with higher inductance will have a faster delta noise tail. These cores will have a large peak delta noise, but have a low delta noise during strobe time. □

Author's biography

Phil Harding is director of marketing for commercial products at Electronic Memories, Hawthorne, Calif. He previously worked at Bell Telephone Labs. Phil received his BSEE from Cooper Union College and his MSEE from Columbia University. He has had 15 patents granted with 5 more pending.





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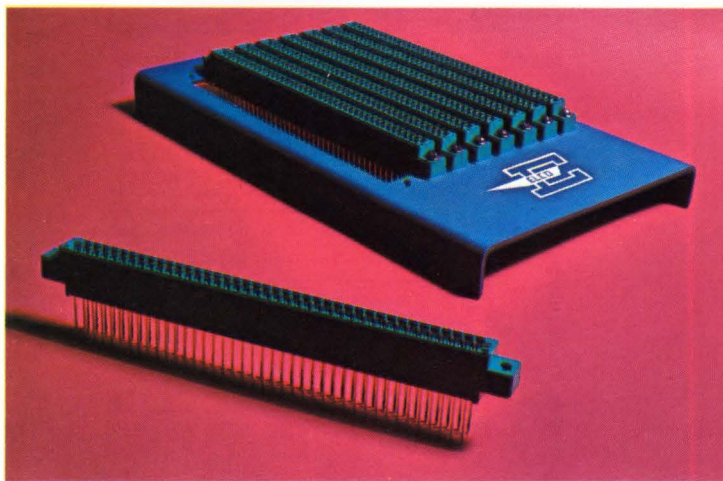
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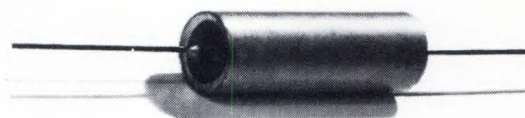
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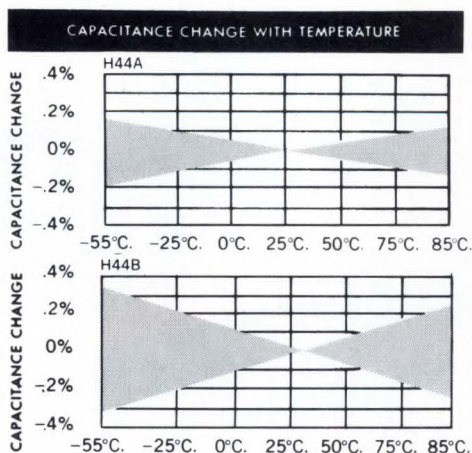
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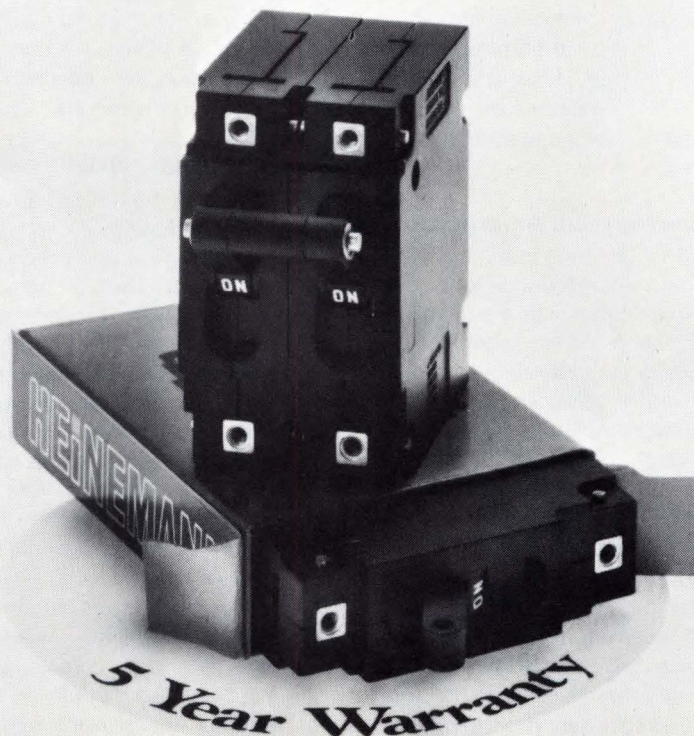
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How effective are data transmission redundance checks?

Vertical and longitudinal redundance check bits are commonly inserted in messages to control errors. Here is a way to determine their effectiveness.

Kenneth N. Larson, Bunker-Ramo Corp.

The number of data processing applications requiring the transmission of digital data from remotely located keyboard-display terminals to centralized computer facilities are rapidly increasing. An inherent problem in all such systems is the interjection of errors into the data as it is traveling between a terminal and the computer. The source of the errors is the relatively noisy environment through which the transmission must propagate. Electrical noise caused by the transmitting equipment, switch boards, nearby electrical machinery and the earth's atmosphere are just a few noise sources which can effect a data transmission. The greater the distance and data rate of the transmissions, the greater the chance of data errors.

Transmission errors which are not detected by the receiving hardware can easily cause accounts to be erroneously altered, reservations canceled, merchandise sent to the wrong destination and so on. Often, system operating personnel do not become aware of such errors until problems arise; that is, until a customer complains about his erroneously canceled reservation or a shipment of goods ends up in the wrong part of the country. A few such errors per month can easily destroy the usefulness of an automated data processing system. Therefore, the effectiveness of the system's error detection hardware should be a primary concern of the system designer.

One commonly used method for controlling data transmission errors is the insertion of vertical and longitudinal redundance check bits into a message. This article will provide a set of equations which will determine the effectiveness of this error control procedure when used in bit-serial data transmission applications.

Detection-retransmission error recovery procedure

The number of vertical and longitudinal redundance bits added to a message by the transmitting terminal is not great enough to allow the receiving terminal to automatically correct a message. Instead, the receiving terminal must send a response message back to the transmitting terminal. The response message is either an acknowledgement (ACK), if the received data contains no errors, or a negative acknowledgement (NAK), if errors are detected in the message. If a NAK response is returned, the sending terminal must retransmit the data.

To improve the efficiency of the detection-retransmission procedure, the transmitting terminal divides its message into blocks. It then transmits the message one block at a time. After a block has been received, the receiving terminal returns a response message. If the response is an ACK, the transmitting terminal sends the next block. If the response is a NAK, only the last block sent must be retransmitted, not the entire message. This procedure continues

until all the blocks of the message have been successfully transmitted.

What makes up a data block?

A data block is the largest collection of bits which must be considered, since one block must be correctly received before transmission of the next can begin. Bit positions within a data block will be more easily described if the block is configured in a matrix form, consisting of I' rows, and J' columns. The j -th column of the matrix will be arbitrarily defined as the j -th word of the block. This will cause the i -th row of the matrix to consist of the i -th bit of every word within the block.

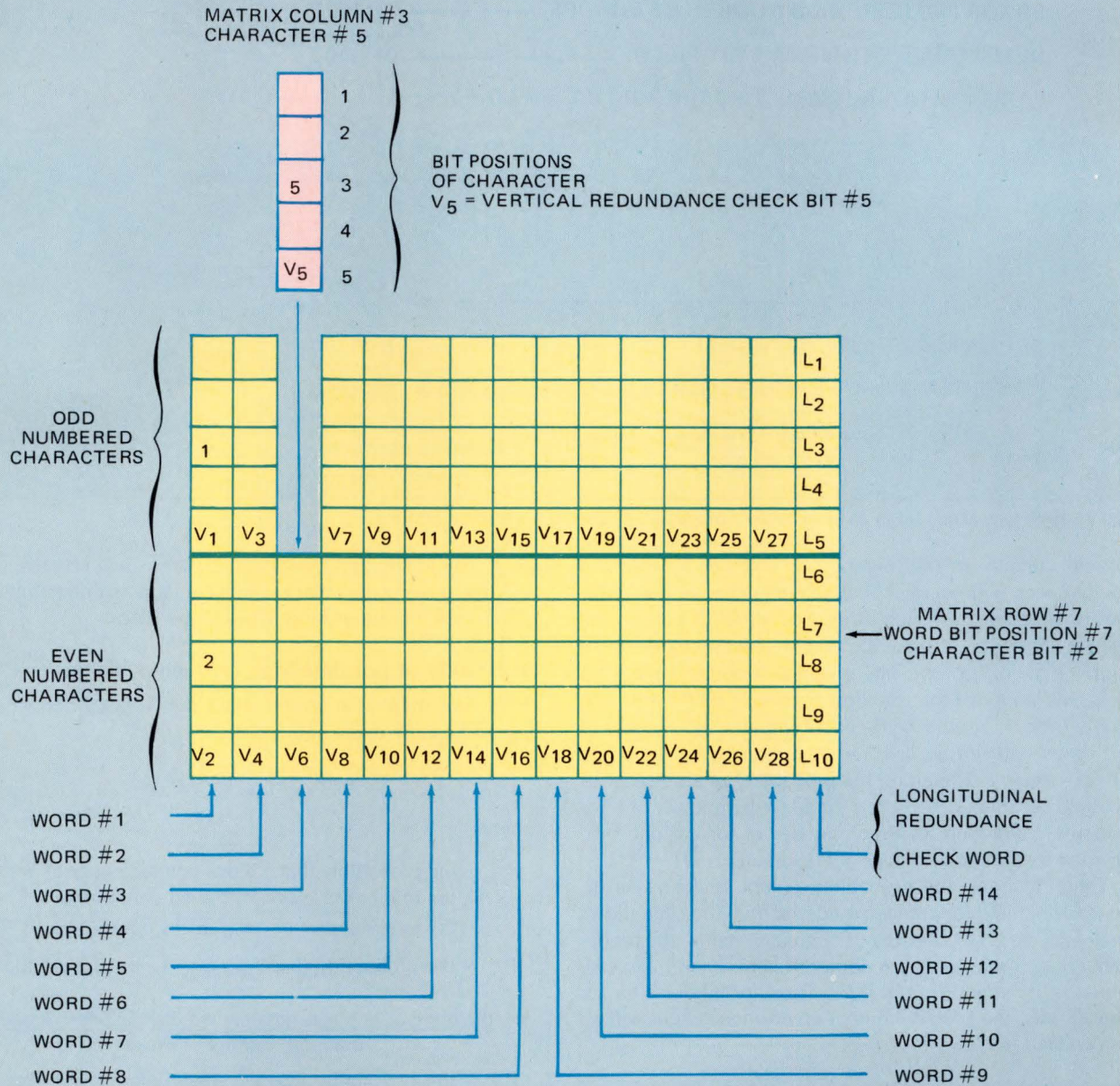
A block consists of W words with C characters per word and B bits per character, where B , C , and W are all positive integers. Therefore, the matrix variable $J' = W$, and $I' = B \times C$. The B -th bit of every data character will be a vertical redundance check bit (VRC). The W -th word of every block will consist of $B \times C$ longitudinal redundance check bits (LRC), and contain no VRC bits. Each vertical redundance check bit will be chosen so that the total number of logical one bits within a character, of which it is part, will either be odd (odd parity) or even (even parity), depending upon which convention has been selected for the system. In a like manner, each longitudinal redundance check bit will be chosen so that the total number of logical one bits in the matrix row, of which it is part, will either be odd or even depending upon the convention selected. The format of a data block is shown in Fig. 1.

Error detection capability of redundance check bits

Let a bit field be defined as a collection of ' m ' bits containing one redundance check bit, either vertical or longitudinal, depending upon the orientation of the field, and $m - 1$ data bits. Thus, a character represents a vertical bit field and a matrix row represents a longitudinal bit field. As the bit field is transmitted through a network, bit errors may be introduced. The introduction of errors into a bit field can be expressed mathematically as the modulo-2 sum of the bit field with an ' m ' bit error pattern. Each logical one bit in the error pattern will thus produce an error in the bit field. Since the all zero pattern does not produce any error in the bit field, there are $2^m - 1$ possible error patterns. For this analysis it will be assumed that all $2^m - 1$ error patterns can occur equally. This assumption is reasonable for systems in which errors tend to occur in bursts, rather than as single isolated events. As an example see Fig. 2.

If an error pattern containing an odd number of logical one bits is added modulo-2 to a bit field, the parity of the resulting erroneous bit field will be incorrect. That is, the field will contain an even number of one bits when it

DATA BLOCK FORMAT
 DATA BLOCK CHARACTERISTICS
 W = 15 WORDS/BLOCK
 C = 2 CHARACTERS/WORD
 B = 5 BITS/CHARACTER
 $C_n B_k$ = BIT k OF CHARACTER n



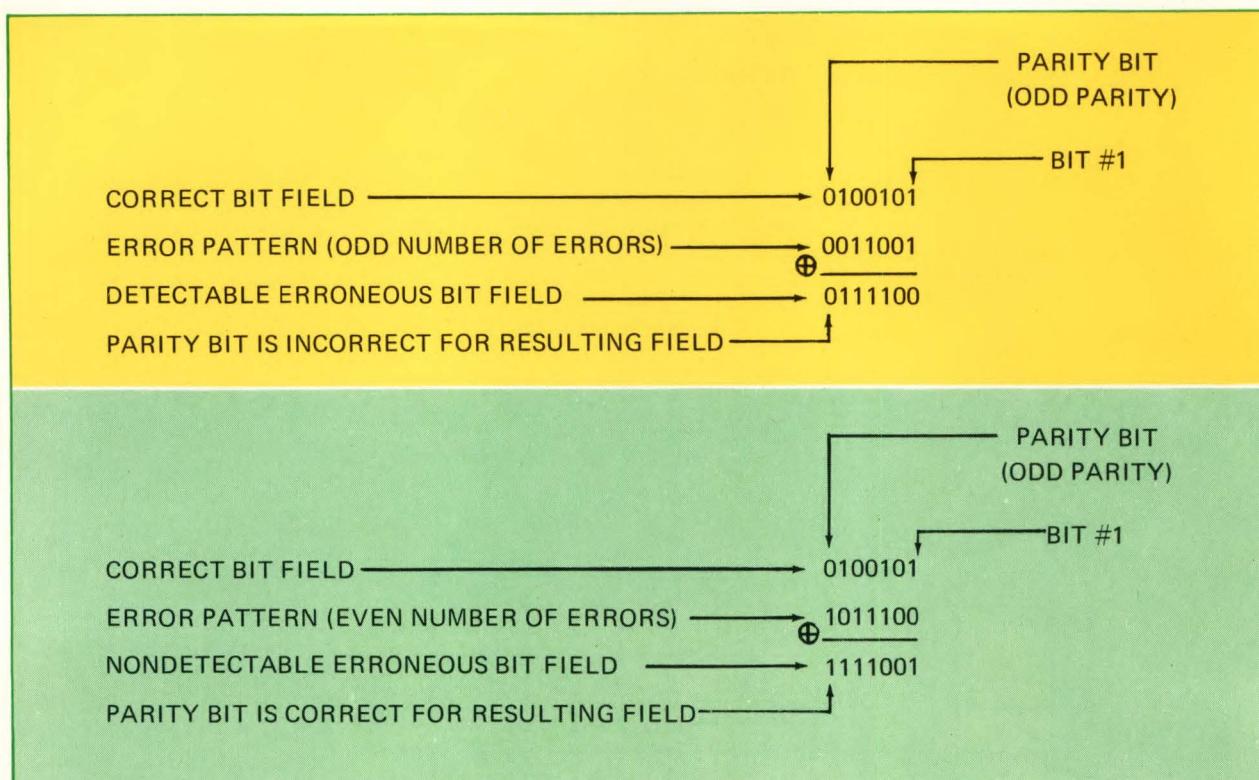


Fig. 2—Each logical one bit in an error pattern produces an error in the original bit field.

should contain an odd number, or visa versa. Since the parity check will fail on a bit field containing an odd number of bit errors, all such erroneous bit fields can be detected. However, if an error pattern containing an even number of logical one bits is added modulo-2 to a bit field, the parity of the resulting erroneous bit field will be correct. Thus, any bit field containing an even number of bit errors will not be detected as erroneous by the parity check circuitry. Therefore, the probability of an erroneous bit field escaping detection is equal to the number of error patterns containing an even number of logical one bits, divided by the total number of error patterns ($2^m - 1$).

Table 1 shows the probability of not detecting an erroneous bit field for different values of 'm.' The table shows that, for values of 'm' equal to or greater than 4, the probability of an undetected erroneous bit field is approximately equal to its upper limit of 0.50. Thus, for bit fields longer than 3 bits, the probability that an erroneous field will go undetected is 1/2.

Error patterns which are always detected

The vertical redundancy check (VRC) will detect any odd number of bit errors within a character. Every block containing an odd number of bit errors must have one or more characters which contain an odd number of bit errors. Therefore, the vertical redundancy checks in a message will cause every block containing an odd number of bit errors to be detected. The vertical redundancy checks will also detect those erroneous blocks containing an even number of bit errors, provided that one of the characters within the block has an odd number of bit errors.

The longitudinal redundancy check (LRC) will detect all erroneous blocks in which the error burst is not greater than one word in length. That is, the number of bits from the first bit in error to the last is less than the number of bits in a

word. The longitudinal redundancy checks will also detect as erroneous any data block which contains an odd number of bit errors in one or more rows of the block.

Probability of not detecting erroneous blocks

The probability that an erroneous data block will not be detected can be expressed as follows:

$$P_E = (P_{EB}) (P_{LB}) (P_{LF}) (P_{VF})$$

where

P_{EB} = the probability that a block contains an error burst
= $\frac{\text{the number of blocks received with errors}}{\text{the total number of data blocks transmitted}}$

P_{LB} = the probability that the error burst is longer than 1 word
= $\frac{\text{the number of bursts greater than } (B \times C) \text{ bits in length}}{\text{the total number of bursts}}$

P_{LF} = the probability that the longitudinal redundancy check failed to detect the error burst

P_{VF} = the probability that the vertical redundancy check failed to detect the error burst.

An error burst shall be defined as an error pattern caused by a single event, such as a noise pulse or fade, occurring on the network and having a length equal to the number of bits from the first error bit to the last, inclusive.

The probability of an erroneous character containing an even number of bit errors, and thus not being detected by the parity check hardware, is less than or equal to 1/2. The probability of all erroneous characters within a block having an even number of bit errors is $(1/2)^n$, where 'n' is the number of erroneous characters in the block. Since the longitudinal redundancy check will detect all error bursts

m	# OF ERROR PATTERNS	# OF ERROR PATTERNS CONTAINING AN EVEN NUMBER OF ONE BITS	PROBABILITY OF NOT DETECTING AN ERRONEOUS BIT FIELD
2	3	1	1/3 = 0.33
3	7	3	3/7 = 0.43
4	15	7	7/15 = 0.47
5	31	15	15/31 = 0.48
m	$2^m - 1$	$(2^{m-1}) - 1$	$((2^{m-1}) - 1) / (2^m - 1) \approx 0.50$

Table I—Probability of not detecting an erroneous bit field of different sizes.

with a length less than or equal to a word ($B \times C$ bits in length), the burst which we are concerned about must be greater than $B \times C$ bits long. Also, a burst must start and end with an error bit, so 'n' must be equal to at least two characters for all bursts of interest. The number of additional characters which may be in error in a burst of length greater than $B \times C$ bits is equal to the probability of a character (other than the first and last) being in error, times the number of characters in the burst other than the first and last character. The probability that a character will contain one or more bit errors is:

$$1 - (1 - p_{be})^B$$

where

p_{be} = the probability of a bit within a burst being in error

$$= \frac{b_w}{b_L}$$

b_w = the number of error bits in an error burst (burst weight)

b_L = the total number of bits in a burst (burst length)

B = the number of bits in a character.

The quantity $(1 - p_{be})^B$ is the probability that all B bits of a character are error free. The number of characters which may be in the error burst, other than the first and last character, is equal to

$$[(b_L/B) - 2]$$

where $[x] = 'x'$ if 'x' is positive, or zero if 'x' is negative. Thus, $n = [(b_L/B) - 2] (1 - (1 - p_{be})^B) + 2$, and the probability of all erroneous characters containing an even number of bit errors (all vertical redundancy checks failing to detect an error burst $B \times C$ bits in length) is

$$P_{VF} = \left(\frac{1}{2}\right)^{2 + [(b_L/B) - 2] (1 - (1 - p_{be})^B)}$$

Since the value of b_L and b_w vary from transmission to transmission, the values used in the above calculations should be mean values for all bursts of length greater than $B \times C$ bits.

Using the same procedure on the longitudinal bit field instead of the vertical bit field, the probability of the longitudinal redundancy checks failing to detect an error burst b_L bits in length will be

$$P_{LF} = \left(\frac{(2^Q - 1) - 1}{2^Q - 1}\right)^{2 + ((B \times C) - 2) (1 - (1 - p_{be})^Q)}$$

where

$$Q = b_L/B \times C$$

In this case the term $1/2$ is not used since the burst may cover less than four bits of any one longitudinal check bit field. For the same reason, the burst length term appears in the exponent of $1 - p_{be}$, instead of as a multiplier of $1 - (1 - p_{be})$. All longitudinal check fields will be covered by bursts $B \times C$ bits or greater, so the multiplier of $1 - (1 - p_{be})$ will simply be the number of longitudinal check fields minus the two fields containing the first and last error bit, $C(B - 2)$, assuming that the first and last bit errors are not in the same field.

Using the equations

Determine the probability of an erroneous data block not being detected for a data transmission, which is bit serial at 1200 bits per second over a switched telephone network. The data is transmitted in 1000 bit blocks with the following parameters:

$B = 8$ bits per character

$C = 1$ character per word

$W = 125$ words per block.

Tables published in an article entitled "High-Speed Voiceband Data Transmission Performance on the Switched Telecommunications Network," written by M. D. Balkovic, H. W. Klancer, S. W. Klare, and W. G. McGruther and printed in the April 1971 **Bell System Technical Journal** provide values for the following terms:

$P_{EB} = 10^{-2}$ at the specified data rate and block size for 91% of all calls

$P_{LB} = 0.18$ (82% of all bursts were less than $B \times C = 8$ bits in length at the specified data rate)

$b_L = 34$ bits (mean value derived from burst length distributions chart for the specified data rate)

$b_w = 8$ bits (mean value derived from burst weight distributions chart for the specified data rate)

From these values the required probability may be calculated as follows:

$$p_{be} = b_w/b_L = 8/34 = 0.236$$

$$1 - p_{be} = 0.764$$

$$(1 - p_{be})^B = (0.764)^8 = 0.116$$

$$1 - (1 - p_{be})^B = 0.884$$

$$(b_L/B) = 34/8 = 4.25$$

$$(b_L/B) - 2 = 4.25 - 2 = 2.25$$

$$((b_L/B) - 2)(1 - (1 - p_{be})^B) = (2.25)(0.884) = 1.99$$

$$2 + ((b_L/B) - 2)(1 - (1 - p_{be})^B) = 2 + 1.99 = 3.99$$

$$P_{VF} = (1/2)^{3.99} = 0.063$$

$$Q = b_L/B \times C = 34/8 \times 1 = 34/8 = 4.25$$

$$(1 - p_{be})^Q = (0.764)^{4.25} = 0.318$$

$$1 - (1 - p_{be})^Q = 0.682$$

$$(B \times C) - 2 = (8 \times 1) - 2 = 6$$

$$((B \times C) - 2)(1 - (1 - p_{be})^Q) = (6)(0.682) = 4.1$$

$$2 + ((B \times C) - 2)(1 - (1 - p_{be})^Q) = 2 + 4.1 = 6.1$$

$$2^Q - 1 = 2^{3.25} = 9.5$$

$$2^Q = 19$$

$$(2^Q - 1) - 1 = 9.5 - 1 = 8.5$$

$$2^Q - 1 = 19 - 1 = 18$$

$$((2^Q - 1) - 1)/(2^Q - 1) = 8.5/18 = 0.472$$

$$P_{LF} = (0.472)^{6.1} = 10^{-2}$$

$$P_E = (P_{EB})(P_{LB})(P_{VF})(P_{LF})$$

$$P_E = (10^{-2})(1.8)(10^{-1})(10^{-2})(6.3)(10^{-2}) = (1.14)10^{-6}$$

$$P_E = (1.14)10^{-6}$$

Therefore it can be expected that one out of every 880,000(1/P_E) data blocks received will contain an error burst which will not be detected by the parity check circuitry of this particular system. It should be noted that this is the typical value and not the worst-case value.

How effective must redundancy checks be?

Vertical and longitudinal redundancy checks cannot detect all erroneous data blocks. The number of undetected erroneous data blocks which a system must expect to receive per time interval is:

$$N = T_B \times P_E$$

where T_B is the number of data blocks transmitted in that time interval. An acceptable value for N must be determined for each individual system.

Assuming that the system used in the example transmitted 5 messages a minute, 40 hours a week, at 1200 bits per second, and each message contained 1250 characters, determine N for a time period of one year.

Number of blocks per message is

$$\frac{1250 \text{ characters}}{125 \text{ characters/block}} = 10 \text{ blocks}$$

Number of blocks per minute is

$$(10 \text{ blocks/message})(5 \text{ messages/minute}) = 50 \text{ blocks/minute}$$

Number of blocks per week is

$$(50 \text{ blocks/min.})(60 \text{ min./hr.})(40 \text{ hr./wk.}) = (1.2)(10^5) \text{ blocks/wk.}$$

Number of blocks per year is

$$T_B = (1.2)(10^5) \text{ (blocks/wk.)}(52 \text{ wk./yr.}) = (6.3)(10^6) \text{ blocks/yr.}$$

The expected number of undetected erroneous blocks received per year should then be

$$N = T_B \times P_E = (6.3)(10^6)(1.14)(10^{-6}) = 7.2$$

$$N = 7.2 \text{ undetected erroneous blocks per year.}$$

Thus, this system should expect to receive 7.2 undetected erroneous blocks per year or about one every month and a half.

The effect of the block parameters on the value of P_E

By making some rough approximations of P_{EB}, P_{LB}, P_{VF} and P_{LF}, the effect of the block parameters (B, C and W) on the value of P_E can be determined. The term 1 - (1 - p_{be})^x can be approximated by xp_{be} by using the first two terms of the binomial expansion of (1 - p_{be})^x. Substituting this result into P_{VF} and P_{LF}, gives the following:

$$P'_{VF} = \frac{1^2 + p_{be}b_L - 2p_{be}b}{2}$$

$$P'_{LF} = \frac{1^2 + p_{be}b_L - 2p_{be}b_L/B \times C}{2}$$

$$(P'_{VF})(P'_{LF}) = \frac{1^2 + p_{be}b_L - p_{be}(B + b_L/B \times C)}{4}$$

The value of P_{EB} can be approximated by

P_{EB} = B × C × W × P_B, where P_B is the probability of an error burst.

The value of P_{LB} can be approximated by

$$P'_{LB} = \frac{K}{B \times C}, \text{ where K is a constant.}$$

Using these approximations, the value of P_E is approximately equal to

$$P'_E = (P'_{EB})(P'_{LB})(P'_{VF})(P'_{LF}) = \frac{W \times K \times P_B}{(4)^2 + p_{be}b_L - p_{be}(B + b_L/B \times C)}$$

The above approximations indicate that the probability of a redundancy check failing (P_{VF} or P_{LF}) is determined to a large extent by the length of the error burst b_L, and the probability of a bit within the burst being in error (p_{be}). As either b_L or p_{be} increases, the probability of a redundancy check failing decreases. Thus, the larger the error burst, the easier it is to detect it.

The probability of an erroneous block escaping detection (P_E) also increases as both the number of words (W) and the number of bits per character (B) within a block increase. However, the above equation indicates that the probability of an undetected erroneous block being received decreases as the number of characters per word (C) increases. What the equation does not show is that as C increases, the number of longitudinal redundancy check bits within the block must also increase. Thus, the time required to transmit a given length message increases. In other words, reducing the probability of an undetected erroneous block also reduces the throughput of the communication system. □

Author's biography

Kenneth N. Larson has been a member of the technical staff at Bunker Ramo Corp, Westlake Village, Calif. for five years. He received his BSEE degree from the University of Michigan and is co-holder of one patent.





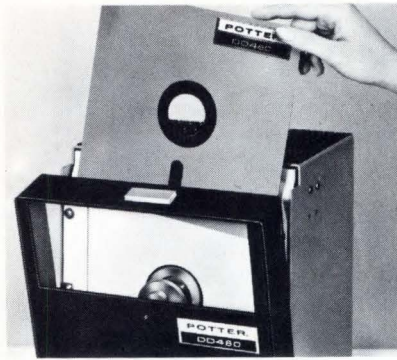
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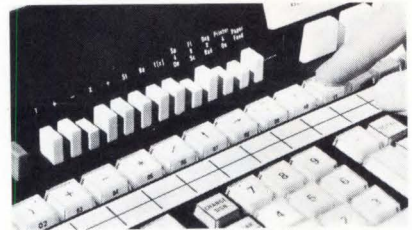
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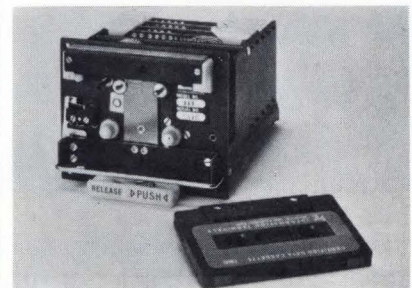
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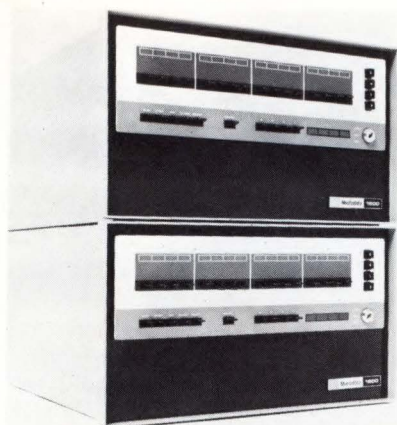


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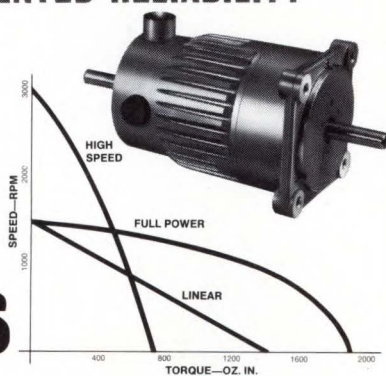
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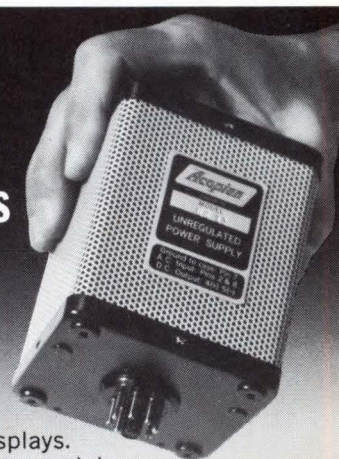
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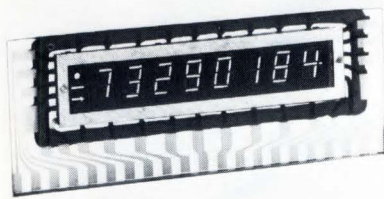
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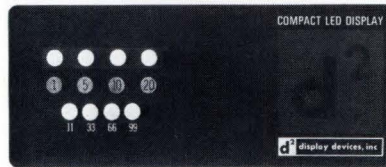
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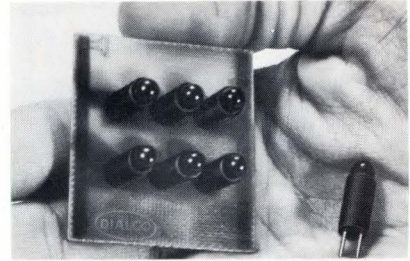
NUMERIC DISPLAY PANEL is an 8-numeral display with decimal points and a left-hand symbol position. The panel is a cold-cathode gas-discharge display. The characters are 7-segment and the symbols are minus, overflow and dot. Character height is 0.255 in. Anode supply voltage is 190V dc and peak cathode current is 0.55 mA. National Electronics, Inc., Geneva, IL 60134. Phone (312) 232-4300. **185**

PUSH-BUTTON ROTARY SWITCHES offered in 6 colors. Designated as Series 2800B, these switches are available in green, red, yellow, blue, white or grey. These push-button rotary switches are bi-

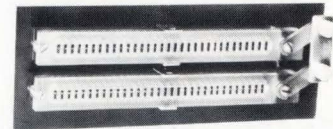
directional. They are available in either 8, 10, or 12 positions in all standard codes. Optional features include RFI shielding, lighted digit positions, and a bezel mount. Janco Corp., 3111 Winona Ave., Burbank, CA 91504. Phone (213) 845-7473. **186**



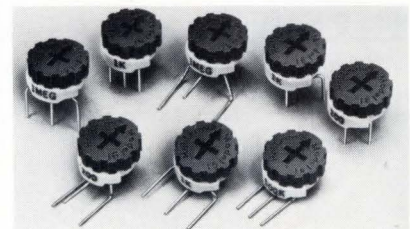
LED DISPLAY PANELS are less than 1/2 inch thick. A unique multilaminate construction technique now makes available low-cost custom fabricated light-emitting-diode display panels up to 30 in. x 40 in. in size. Provisions for switch holes and other panel accessories can be easily provided. Visible graphics may be surface or sub-surface printed. Display Devices, Inc., P.O. Box 667, Encinitas, CA 92024. Phone (714) 753-0113. **187**



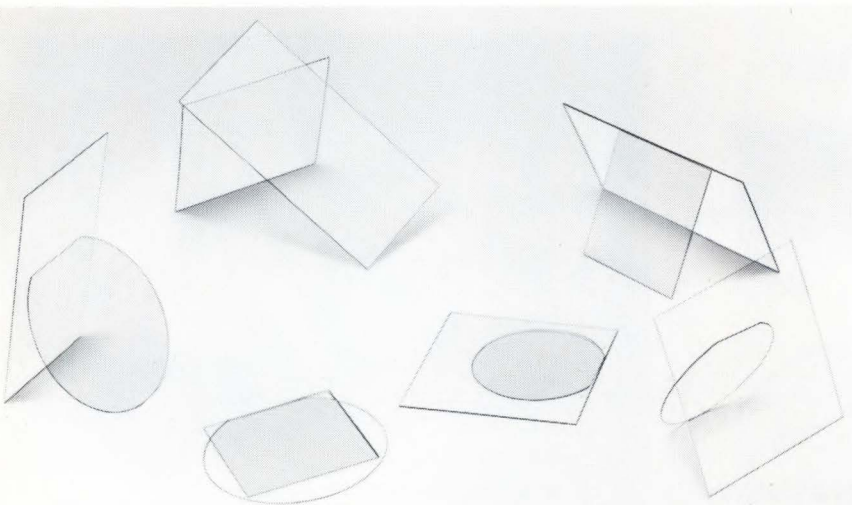
LED LAMPS are directly interchangeable with incandescent. Developed as a direct replacement for the T-1-3/4 incandescent, the Series 549 Bi-Pin lamp is available in voltages from 1.7 to 14V. The LED is made from GaAsP and capped with a red diffused lens. It has a built-in current limiting resistor. In 1000 lot quantities each unit sells for \$0.84. Dialight Corp., 60 Stewart Ave., Brooklyn, NY 11237. Phone (212) 497-7600. **188**



A VERSATILE "ZIP STRIP" (zero insertion pressure) socket which makes it possible to "customize" socket installations for the testing of dual in-line devices with 0.100 in. spaced leads regardless of spacing between rows (0.300 in. min.) may be ganged together for easy mass testing of devices. "Zip Strips" are available in strips of 32 leads on 0.100 spacing. Textool Products, Inc., 1410 W. Pioneer Dr., Irving, TX 75061. Phone (214) 631-5585. **189**



CERMET TRIMMERS provide good stability at low cost. The units typically change less than 0.5% during the first 1000 hours of operation and progressively less per thousand hours thereafter. Temperature coefficient in all 19 standard resistance values, ranging from 10Ω to 2MΩ, is a max. of ±100 ppm/°C over the ambient temperature range of 0° to 85°C. Beckman Instruments, Inc., 2500 Harbor Blvd., Fullerton, CA 92634. Phone (714) 871-4848. **190**



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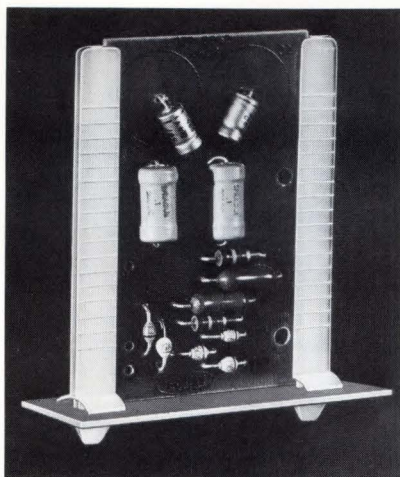
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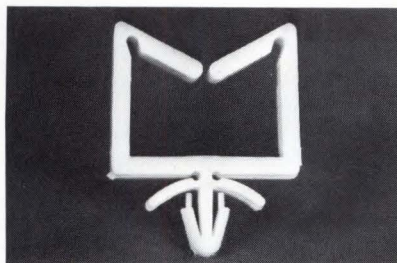
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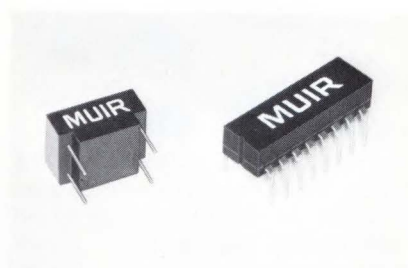
FREE SAMPLES—EDGE GUIDES position printed-circuit boards. Series CBG guides, made of natural color nylon, are available in one, two and three inch effective height. The guides are double channelled to accommodate boards up to 0.075 in. thick. An arrow-type locking head retains the guide in position. The locking head is self-adjusting to fit panel thicknesses from 0.03 in. to 0.09 in. Richco Plastic Co., 5825 N. Tripp Ave., Chicago, IL 60646. Phone (312) 539-4060. **191**

PLUG-IN IC CARDS for wrap-type wiring. EECO 3-D cards are 5.82 in. high, 5.25 in. wide and can hold up to 70 ICs per card. All cards are flame resistant glass epoxy with snaplock position and extraction tabs, 22 test points on top edge of the card, and 120 gold plated etched-type connector-contact fingers. Electronic Engineering Co. of California, Electronic Products Div., 1441 E. Chestnut Ave., Santa Ana, CA 92701. Phone (714) 547-5651. **192**



FREE SAMPLES—WIRE-SADDLE FASTENER installs permanently with ease. WWS-2N wire-saddle fastener features a "Barbed Arrow" insertion tip. Simple finger-tip pressure compresses the tip into a 0.187 in. diameter hole, and once inserted, the tip

expands to lock permanently in position and cannot loosen or fall out. Richlok Corp., 5835 N. Tripp Ave., Chicago, IL 60646. Phone (312) 539-4061. **193**



GENERAL-PURPOSE PULSE TRANSFORMERS, in side egress DIPs and PC mounting Multi-Pacs are available for use in balun and floating switch computer applications. On custom orders, manufacturer will insert additional circuit components, such as diodes, resistors and capacitors in the basic transformer module. In production quantities, prices range from 30c to \$1.50 each. Muir Industries, Inc., 24 Thing Rd., Tecate, CA 92080. Phone (903) 354-1320. **194**

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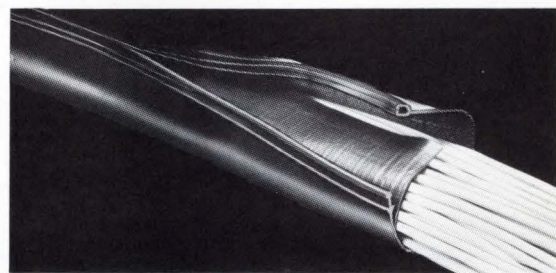


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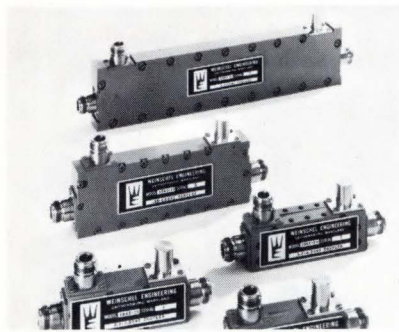
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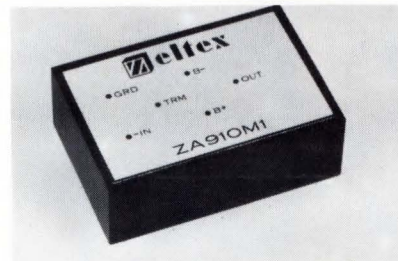
CIRCUITS



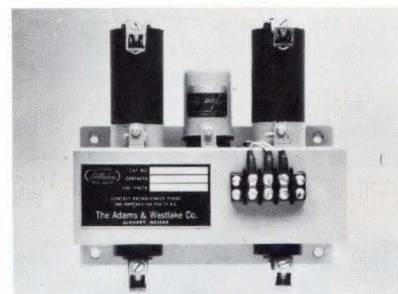
OCTAVE COUPLERS COVER 0.5 TO 12.4 GHz. A series of five octave-band directional couplers are available with both 10 and 20-dB nominal coupling. Three have extended-octave ranges: 0.95 to 2.2 GHz (Model 1541), 1.7 to 4.2 GHz (Model 1542), and 3.7 to 8.3 GHz (Model 1543). The other bands are 0.5 to 1 GHz (Model 1540) and 7 to 12.4 GHz (Model 1544). All five models have a deviation of ± 0.2 dB from average coupling. Prices are \$200 for all models except for Model 1544 with 10-dB coupling, which is \$250. Weinschel Engineering Co., Inc., Clopper Rd., Gaithersburg, MD. Phone (301) 948-3434. **201**

DOUBLE BALANCED MIXERS UP TO 11 GHz. Series FC-304 mixer features coverage from 1.9 to 10.7 GHz. With slightly reduced specifications, Model FC-304SX covers an rf and LO frequency range from 1.2 to 11 GHz. The i-f frequency range is dc to 2 GHz. The unit features a conversion loss of 6 dB, isolation of 26 dB and size of $3/8 \times 9/16 \times 11/16$ in., exclusive of SMA connectors. Lorch Electronics Corp., 105 Cedar Lane, Englewood, N J 07631. Phone (201) 569-8282. **202**

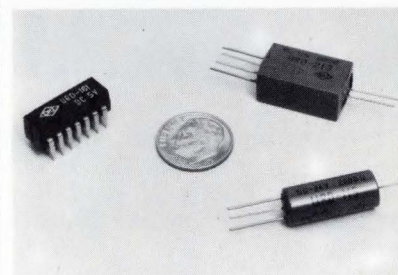
THE TRIM-STEP 225 MOTOR-MOUNTED ENCODER can be readily assembled to a motor by unskilled personnel. The encoder's design provides instant replaceability of its active portions, and eliminates the effect of axial play of the motor shaft. The unit provides square-wave output signals in quadrature and complementary outputs. It is priced at \$100 for single and \$125 for dual-channel models. Trump-Ross Industrial Controls, Inc., 265 Boston Rd., N. Billerica, MA 01862. Phone (617) 663-3451. **203**



ZA910M1 OP AMP SLEWS 2000V/ μ SEC MINIMUM (guaranteed minimum at 100-mA output). It also features a 70-MHz gain-bandwidth product, 30-MHz full-frequency output and 300-nsec settling time to 0.01% of full-scale value. Unit Price is \$99 (1 to 24). Zeltex, Inc., 1000 Chalomar Rd., Concord, CA 94520. Phone (415) 686-6660. **204**



2-POLE POWER-PULSE LATCH SWITCHES 100A AT 120V ac. Series HR-1000 dpst (NO or NC) hermetically sealed solid-state latch can also operate from 230 and 440V ac. Latch-operating voltages are 24 or 48V dc (other voltages available) and switch operation may be continuous (100% duty cycle) or intermittent at up to 6 operations per minute. The Adams & Westlake Co., 1025 N. Michigan St., Elkhart, IN 46514. Phone (219) 264-1141. **205**



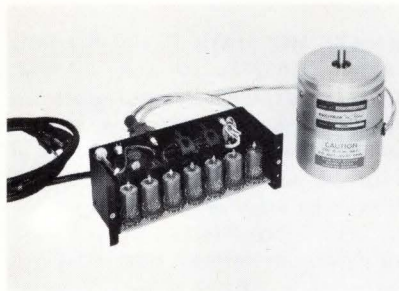
REED RELAYS Series URD are suitable for use with transistorized and integrated circuitry. They are available in several package styles and in 1 Form A and 2 Form A contact arrangements. Breakdown voltage is 100V dc between contacts and 750V dc between terminals. Prices for small quantities start at \$2.50. OKI Electronics of America, 500 S. E. 24th St., Fort Lauderdale, FL 33316. Phone (305) 525-8201. **206**



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CIRCLE NO. 41



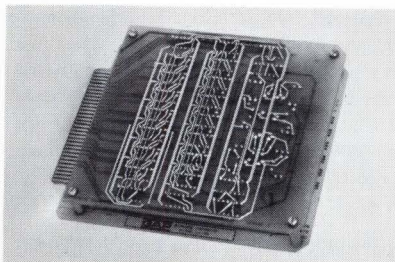
ABSOLUTE ENCODER-DISPLAY PACK-AGE requires only a 115V, 50 or 400 Hz power source to operate. The Decitrak encoder is capable of measurements up to four decades (0 to 9999) with an accuracy of one count. The output drives the associated display and also provides a BCD output at DTL/TTL-compatible levels. The display has seven-segment readouts, an escutcheon and a filter lens. Theta Instrument Corp., Fairfield, N J 07006. Phone (201) 277-1700.

207

SCR TRIGGER TRANSFORMERS IN 3 BASIC SIZES: open or encased for low-cost applications, or encapsulated for special-humidity or military applications are available. Standard units operate from 0 to

+60°C and -10 to +70°C. Turns ratios of 1:1, 1:1:1, 2:1, 2:1:1, 5:1 and 5:1:1 along with primary inductances from 250 μ H to 20 mH are available. Leakage inductance ranges from 5 to 200 μ H and interwinding capacitance from 20 to 50 pF. BH Electronics, 245 E. 6th St., Saint Paul, MN 55101. Phone (612) 228-6463.

208



SOLID-STATE TRACKING S/D CONVERTERS Series 4300 consist of a basic 12-bit s/d converter with an accuracy of 5.2 minutes worst case from all sources. The Series can accept all synchro/resolver input types and continuously present the true angle in digital format. Digital outputs and control signals are TTL/DTL compatible. Price is \$550. Gap Instrument Corp., 110 Marcus Blvd., Hauppauge, NY 11787. Phone (516) 273-0909.

209

FOUR-QUADRANT 13-BIT CONVERTER Model 849 comes in a metal 20-pin package and operates over -55 to +125°C meeting applicable portions of MIL-STD-883. It accepts a serial binary input and has two reference-voltage inputs. External references, command signals, a two-phase clock and power are required externally. References up to ± 10 V dc or 20V ac pk-pk to 2.5 kHz are possible. Cost is \$185. Helipot Div., Beckman Instruments, Inc., 2500 Harbor Blvd., Fullerton, CA 92634. Phone (714) 871-4848.

210

4-POLE HALF-SIZE CRYSTAL-CAN RELAY features high sensitivity. The Model BR52 requires only 500 mW of pull-in power to switch 2A at 28V dc or 115V ac 400 Hz (dry circuit). It withstands shock of 50 g's at 11 msec over a minimum life of 100,000 cycles and is available in coil voltages of 6, 12 and 26V dc (nominal). Operate/release time is 4 msec and temperature range is -65 to +125°C. Babcock Electronics Corp., Sub. of Esterline Corp., 3501 N. Harbor Blvd., Costa Mesa, CA 92626. Phone (714) 540-1234.

211



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CIRCLE NO. 42

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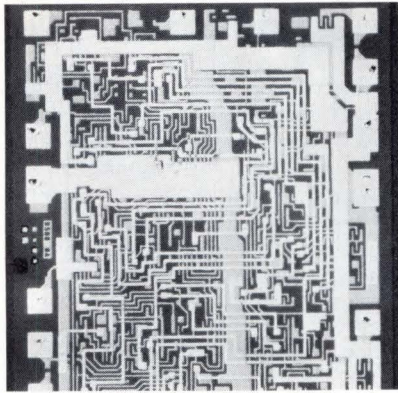
Wakefield Type 180 aluminum cold plates can be used to cool most types of power transistors, rectifiers and high power resistors. Thermal resistance, device case to inlet water, is .3 C/W per device with devices mounted on 1" centers and water flow of 1.5 GPM. These Liquid Cooled Plates may be considered an integral portion of the high current bus work and may be run at higher current densities than open uncooled busing. The use of drawn copper tubing assures a leakproof system which will stand high pressures. 6" and 12" lengths are stocked by Distributors; other lengths up to 6' are available on factory order with or without hole patterns drilled to your specifications. Send for Bulletin 180.



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CIRCLE NO. 43

SEMICONDUCTORS

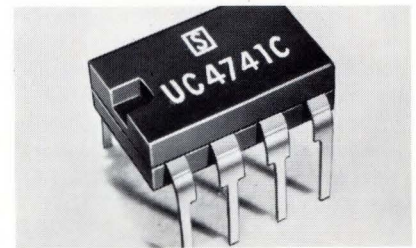


NEW ECL/MSI DEVICES include 200-MHz shift register. Three of the new devices, the 95H00 4-bit shift register, the 95H55 5-bit comparator and the 9580 triple 2-input multiplexer, are the only such functions currently available in ECL logic. The other new device is the 95H28, a high-speed version of the 9528 dual-D flip-flop. Their 100 pc. prices are: 95H00—\$12.50, 9580—\$5.20, 95H55—\$5.20, 95H28—\$5.55, Fairchild Semiconductor Components, 464 Ellis St., Mountain View, CA 94040. Phone (415) 962-3816. **217**

ECL FAMILY has on-chip voltage as well as temperature compensation. With 95100 ECL devices, the design requirement to regulate supply voltages within $\pm 2\%$ can be relaxed to 20% if operating on a nominal 5.2V supply. As a result, the devices are more tolerant of supply voltage variations than standard TTL at 5.0V. The 95100 family is based on Fairchild's 9500 Series temperature-compensated devices. The first devices available are three SSL gates. Pricing of the 95102, 95103 and 95104 dual, triple and quad OR/NOR gates, is \$1.80 for 100-999 quantities. Fairchild Semiconductor, 464 Ellis St., Mountain View, CA 94040. Phone (415) 962-3816. **215**

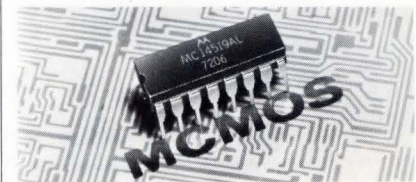
HIGH-VOLTAGE POWER SWITCHING TRANSISTORS, designated JAN and JANTX 2N5660 through 2N5667, feature typical ratings of 2 to 5A. 2N5660-2N5663 have V_{CE} to 400V. The 5A series (2N5664-2N5667) have V_{CE} to 400V; $t_{on} = 250$ nsec, max.; and $t_{off} = 1500$ nsec, max. The transistors are available in TO-5 and TO-66 packages. Prices start at \$10 ea. for 100-unit quantities. Unitrode Corp., 580 Pleasant St., Watertown, MA 02172. Phone (617) 926-0404. **216**

64 × 4 BIT MOS STATIC/DYNAMIC RAMS, UA2264, UA3264, UA2864, UA3864, UA2664, and UA3664, feature regenerative inputs, field-inversion protection, and zener-input protection. The combination of wired OR and multiple chip select lines provides for maximum expansion versatility. Typical access time is $< 1 \mu\text{sec}$. For further information contact Solitron Devices, Inc., 8808 Balboa Ave., San Diego, CA 92123. Phone (714) 278-8780. **218**



OP AMP, Model UC4741C, is now offered in an 8-lead "mini-dip" package. This affords greater package density, since the "mini-dip" occupies 1/2 of the space previously required by the 16-pin DIP, while maintaining the performance standards established with the hermetically sealed UC4741C TØ-99. Solitron Devices, Inc., 8808 Balboa Ave., San Diego, CA 92123. Phone (714) 278-8780. **219**

L-BAND POWER TRANSISTOR delivers a minimum of 20W of rf power at 1500 MHz and 28V with MTBF exceeding 100,000 hours. Reliability is achieved by a proprietary, Auromet[®], gold metalization process which eliminates metal migration inherent in aluminum metalized transistors. Power Hybrids, Inc., 1742 Crenshaw Blvd., Torrance, CA 90501. Phone (213) 320-6160. **220**



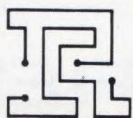
CMOS DEVICE provides data routing control. The MC14519 AL/CL 4-bit and/OR select element provides low power data routing control. Using two control bits, one of two 4-bit information channels can be selected for output distribution. Such an operation is similar to 4-pole, double throw switching. This device can also provide a quad Exclusive-NOR gate function. Price is \$2.10 in 100 quantities. Motorola Inc., Semiconductor Products Div. P.O. Box 20924, Phoenix, AZ 85036. Phone (602) 273-6900. **221**

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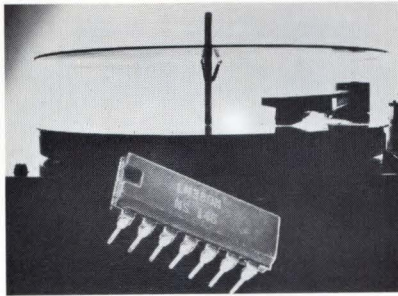
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HIGH-CURRENT TRIACS in press-fit, stud, and isolated-stud packages announced. Nine new 80-A triacs, types 40916, 40917, and 40918 utilize the press-fit package and

have voltage ratings of 200, 400 and 600V, respectively. Types 40919, 40920 and 40921 utilize the stud package and 40922, 40923 and 40924 utilize the isolated-stud package. Prices range from \$14 to \$30 in 100 pc. orders. RCA Solid State Div., Rt. 202, Somerville, N J 08876. Phone (201) 722-3200. **223**

SINGLE-CHIP ANALOG MULTIPLIER with 0.5% accuracy requires no external components. The 8013 provides full-scale accuracy of 0.5%, slew rate of 40V/μsec, output offset of 35 mV and 1 mV/°C output offset drift. It's available in commercial (0° to +70°C) or military (-55° to 125°C) temperature ranges, and is packaged in a 10-pin low-profile TO-100 case. Prices range from \$15 to \$38 in orders of 100-999 pcs. Intersil, 10900 N. Tantau Ave., Cupertino, CA 95014. **224**

1024-BIT P/ROM uses diode programming. The IM5603 is a fully decoded TTL read-only memory organized as 256 words by 4 bits. It has on-chip address decoding, two chip-enable inputs and uncommitted collector outputs. Access time is 60 nsec

and it is packaged in a 16-pin DIP in commercial (0° to +75°C) temperature range. Price in 100-unit quantities for the IM5603 is \$45.00 each. Intersil, 10900 N. Tantau Ave., Cupertino CA 95014. Phone (408) 257-5450. **225**

10-18KV SILICON RECTIFIER features ratings up to 10 mA and 16 kHz with controlled avalanche. Designated Type E10-10, the device can be operated up to 125°C max. junction temperature at low leakage current. Typical applications for the Type E10-10 Series include power supplies, TV, oscilloscopes, air cleaners, electrostatic copying and x-ray equipment. Henley Electronics, Inc., 202 E. 44 St., New York, NY 10017. Phone (212) 986-5544. **226**

VOLTAGE-VARIABLE CAPACITANCE DIODES, designated Series JAN IN5139A-5148A, feature Qs (at -4.0V) as high as 350, 60Vdc ratings, and low leakage. They are available in DO-7 packages. The unit price is \$4.45 in 1-99 quantities, and \$3.00 in 100-499 quantities. JAN-TX versions are available for \$8.40 and \$5.60. Delivery is from stock. Teledyne Crystalonics, 147 Sherman St., Cambridge, MA 02140. Phone (617) 491-1670. **227**

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- positioning
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- smoke detection
- sorting
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- counting
- jam-up
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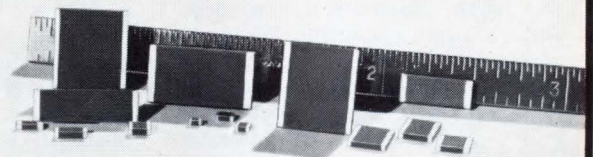
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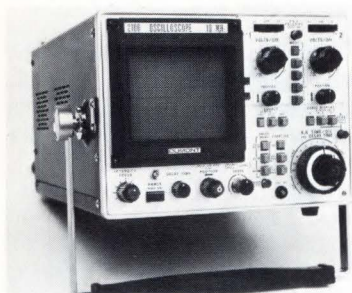
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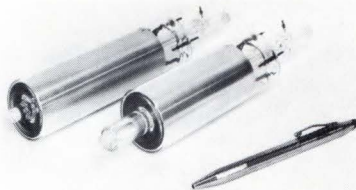
EQUIPMENT



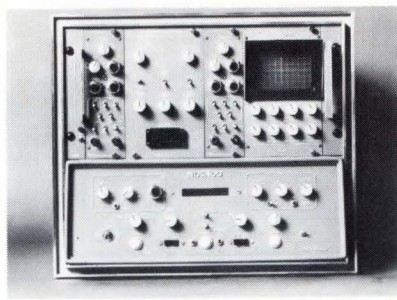
PORTABLE 10-MHZ SCOPE HAS DELAYED SWEEP. The dual-channel Model 2100 has sensitivity of 10 mV/div., sweep speed to 50 nsec/div., an 8-X-10-div. display and weighs only 14 lb. Pushbutton front-panel controls, full auto triggering and AND-gate logic for external triggering as many as four simultaneous inputs are included. Cost is \$995. Dumont Oscilloscope Laboratories, Inc., 40 Fairfield Pl., W. Caldwell, N J 07006. Phone (201) 228-3665. **230**

PORTABLE FET MULTIMETER, Model FE23, dubbed the Little Henry, comes with a D'Arsonval meter that is fully protected to 1000 times overload. A lighted meter allows

the FE23 to be read in the dark. A full range of voltages up to 6 kV, resistance and current, high-voltage readings up to 30 kV and accuracy of 1.5% with a 15-M Ω dc input are additional features of this \$80 instrument. Sencore, Inc., 3200 Sencore Dr., Sioux Falls, SD Phone (605) 339-0100. **231**



FREE SAMPLES OF TINY HE-NE LASERS. Dubbed the "low-fat" lasers, Models 3121 and 3122 cost only \$79.95 (1000 quantities) and carry an 18-month, no-hour-limit OEM warranty. Available in 1 and 2-mV versions with optional polarization, they measure 9-in. long and feature a proprietary non-hydroscopic mirror sealant for environmental protection. The free sample offer is available to any OEM with a valid requirement for laser tubes. Hughes Aircraft Co., Electron Dynamics Div., 3100 W. Lomita Blvd, Torrance, CA 90509. Phone (213) 543-2121. **232**



MULTICHANNEL ANALYZER ND2400 provides automatic spectrum display and analysis of multi-element samples. Three modes of data acquisition are provided with a memory cycle time of only 2 μ sec. A 100-kHz display rate allows flicker-free viewing of sample spectrum. Selection of linear or logarithmic display and sample-spectrum up to a factor of 20 for close inspection are other features. Nuclear Data, Inc., 1330 E. Golf Rd., Palatine, IL 60067. Phone (312) 529-4600. **233**

PEN-SIZE PULSE GENERATOR AND A LOGIC PROBE form a \$190 stimulus-response test set that's only the size of two pens. The pulser, Model 10526T, automatically drives any node to the opposite state for 400 nsec. With its low source impedance of 2 Ω and 0.75A current-delivering ability, it can reverse the state of any node. The probe, Model 10525T, will detect bad levels and open circuits and capture HIGH or LOW pulses as short as 10 nsec while maintaining an input impedance above 25 k Ω . Hewlett-Packard Co., 1501 Page Mill Rd., Palo Alto, CA 94304. Phone (415) 493-1501. **234**

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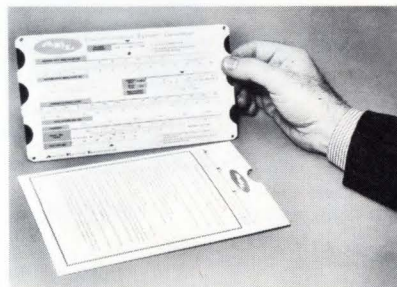
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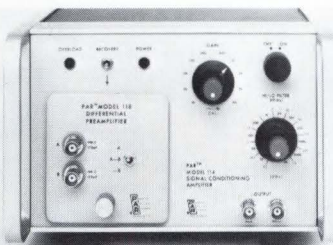
A FREE COMMUNICATIONS SYSTEM CALCULATOR provides a simplified slide rule on fundamental relationships between transmitter power, antenna gain and frequency and receiver parameters. Independent variables incorporated are transmitting frequency, receiver bandwidth, input-noise figure, input signal-to-noise ratio and input, transmitter power output, path loss, total antenna gain, total path distance and horizontal ray altitude. American Electronic Laboratories, Inc., Box 552, Lansdale, PA 19446. Phone (215) 822-2929. **235**



A NEW CONCEPT IN DIGITAL MONITOR AND DISPLAY called VIMAC—Vidar 690 monitor alarm controller—makes it possible for up to seven users to share one data-acquisition system. Operating in conjunction with a digital data-acquisition system such as the Vidar 5400, VIMAC will present up to ten digits of information from any one, or combination of six data devices. Vidar Corp., 77 Ortega Ave., Mountain View, CA 94040. Phone (415) 961-1000. **236**

HIGH-ACCURACY DIGITAL DATA-ACQUISITION and alarm system for dc voltages from 1 μ V to 200V includes thermocouple reference accuracy of $\pm 0.1^\circ\text{F}$, digital conversion to temperature with conformity of $\pm 0.1^\circ\text{F}$ to NBS standards, expand-

ability from 10 to 900 channels and automatic internal programming for up to three thermocouple types and five voltage ranges on a 4-1/2-digit DVM. A 30-channel system costs \$4500. Kay Instruments, Inc., 737 Concord Ave., Cambridge, MA 02138. Phone (617) 868-7080. **237**



GENERAL-PURPOSE AMPLIFIER features a selection of 6 plug-ins that provide low-noise matching to virtually any signal source. Model 114 signal-conditioning amplifier offers switch-selectable gains of up to 2,500,000, switch-selectable 6-dB/octave low and high-frequency roll-offs and overload protection. Price of the 114 is \$595. Preamplifiers range from \$250 to \$525. Princeton Applied Research Corp., Box 2565, Princeton, N J 08540. Phone (609) 452-2111. **238**



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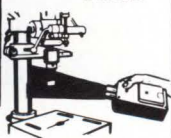
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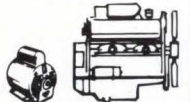
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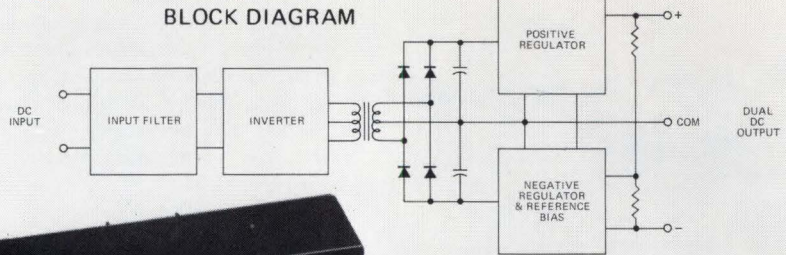
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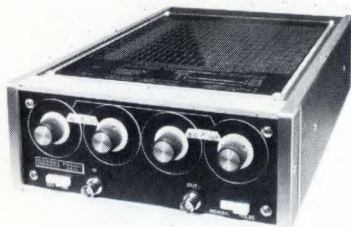
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CIRCLE NO. 50

EQUIPMENT



VARIABLE ELECTRONIC FILTERS Series 4210 cover 0.01 Hz to 1 MHz in 5 models (each model covers six decades). The units use four-pole Butterworth filters in the normal mode and four-pole Bessel filters in the pulse mode. They feature frequency accuracy of $\pm 1\%$, phase shift of $\pm 2^\circ$ and amplitude response of ± 0.2 dB. Ithaco Inc., 735 W. Clinton St., Ithaca, NY 14850. Phone (607) 272-7640. **240**

11-IN.-CRT STORAGE DISPLAY is designed to offer low-cost alphanumeric or graphic computer display. The direct-view storage tube used eliminates costly memory devices required for refreshing the information display and provides high information density with good resolution without flicker or drift. The Model 613 is hard-copy compatible with the Tektronix 4610 hard-copy unit. Catalog price of the 613 is \$2200. Tektronix, Inc., Box 500, Beaverton, OR 97005. Phone (503) 644-0161. **286**

A NEW DIAGNOSTIC TEST SYSTEM is intended for production, inspection and test of PC cards and modules. The system will readily identify most card assembly faults such as missing, wrongly placed, reversed or defective resistors and semiconductors, and checks continuity and isolation of card tracks and reactive devices. An additional feature is a test connection fixture for minimized card-handling times. Marconi Instruments, 111 Cedar Lane, Englewood, N J 07631. Phone (201) 567-0607. **242**



ELECTRIC COUNTER HAS PUSHBUTTON RESET SWITCH OUTPUT. The 4-figure, panel-mounted counter's output may be used to actuate external circuitry. The switch output is a spst FORM C switch and is maintained as long as the counter reset button is depressed. The switch is rated at 4A, 150V ac. The counter operates at up to

1000 counts/minute and is available in most popular ac and dc voltages at less than \$10 in OEM quantities. Durant Digital Instruments, 901 S. 12th St., Watertown, WI 53094. Phone (414) 261-4070. **243**



VTR-1100 1/2-IN. COLOR VIDEOTAPE RECORDER features automatic color lock and automatic gain control. Compatible with the proposed EIAJ Type II and existing Type I tape, its automatic color lock holds even when shifting into the still-frame mode. Resolution is 300 lines (black and white) and 240 lines (color) and signal-to-noise ratio is 40 dB (black and white) and 36 dB (color). User net cost is \$1295. Concord Communications, Systems Div., Benjamin Electronic Sound Co., 40 Smith St., Farmingdale, NY 11735. Phone (516) 694-7960. **244**

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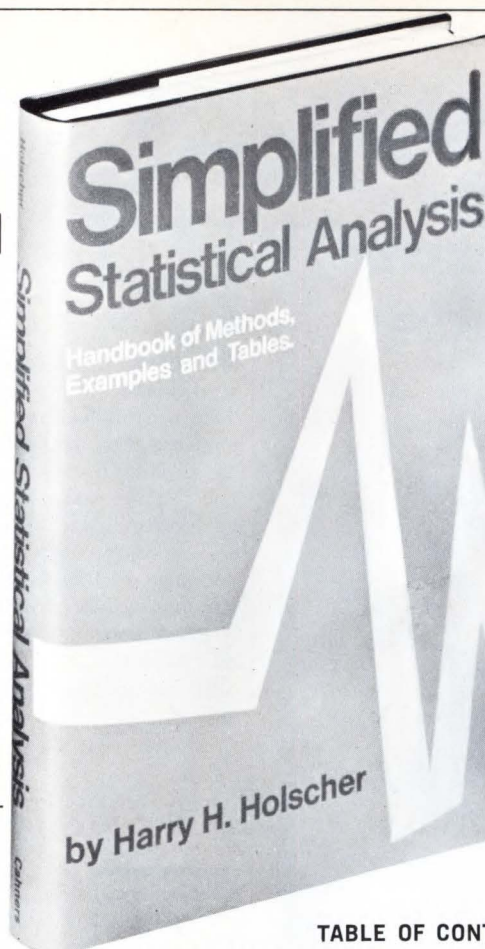


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LITERATURE



LOW-COST D/A CONVERTERS are described in a new four-page brochure. Electrical and mechanical specifications, performance data and application data listed are given for five series of converters. The low cost and moderate performance make the devices attractive for such applications as very low-cost single-channel a/d converters, CRT displays, servo drivers, data transmission via modems, programmed/feedback control systems and digital frequency synthesizers. Datal Systems, Inc., 1020 Turnpike St., Canton, MA 02021.

251



DATA COMMUNICATIONS. The applications and benefits of Intertran, a modular low-cost data set for four-wire twisted pair data communications facilities, are discussed in detail in a new brochure. It examines the capabilities and specs of several models of the Intertran 910 Series data sets used for interfacing any low, medium or high speed terminal devices. Computer Transmission Corp., 1508 Cotner Ave., Los Angeles, CA 90025.

256



OEM CHART RECORDERS for biomedical and industrial applications are shown in a data sheet. Described are a new line of single and two-channel module type recorders which feature pressurized ink writing, rectangular trace presentations, a wide range of sensitivities and chart speed options. Gould, Inc., Instrument Systems Div., 3631 Perkins Ave., Cleveland, OH 44114.

252



MINIATURE POWER MODULES designed for mounting on PC boards and other limited-space applications are described in a four-page brochure. Single- and multiple-output regulated supplies with outputs from 1 to 50V at up to 500 mA are included in the listings. Acopian Corp., Easton, PA 18042.

255



ANGLE-TO-DIGITAL CONVERTERS are described in this eight-page brochure. The series described adapts to either a synchro-resolver-to-digital converter or to a programmable bridge by the use of plug-ins. Singer Instrumentation, Los Angeles Operation, 3211 S. La Cienega Blvd., Los Angeles, CA 90016.

253



CRT TERMINALS. Ten CRT terminal models offering parallel, serial, serial polling and TTY replacement interfaces are described in a new, 8-page, full color brochure. Prices, specifications, options, features and details of modular design are included. Request brochure number 844. TEC, Inc., 9800 N. Oracle Rd., Tucson, AZ 85704.

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TRIPLETT'S MODEL 603 FET VOM is illustrated in a four-page brochure. The VOM is battery operated and has a circuit that permits it to be left on indefinitely without impairing its performance. Triplett Corp., Bluffton, OH 45817. **257**



NEW 20-CHANNEL EVENT RECORDER, Model TR-820 from Gulton Techni-Rite is described in a bulletin. The recorder has eight chart speeds and an internal chart rewind. Gulton Techni-Rite Electronics, Rte 2, E. Greenwich, RI 02818. **258**



INK-JET OSCILLOGRAPHS are described in a new eight-page bulletin. The four basic models detailed offer a frequency response from dc to 1000 Hz, from 2 to 16 measuring channels and Z-fold recording paper. Siemens Corp., 186 Wood Avenue South, Iselin, NJ 08830. **259**



SCR MOTOR SPEED CONTROLS are described in a new brochure. The controls offer speeds from 0.1 to 4140 rpm and torques from 11 in.-oz to 1730 in.-lb. B & B Motor and Control Corp., 96 Spring St., New York, NY 10012. **260**

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SM-102A SPECIFICATIONS — START/STOP INPUT — Input Impedance: 1 megohm shunted by less than 50 pF. **Maximum Input Voltage:** ± 50 V DC referenced to ground for either, or both sides of Input. **Sensitivity:** Zero crossing mode: 100 mV RMS. TTL/relay mode: TTL compatible. **Minimum Pulse Width:** Zero crossing mode: 100 ns at 300 mV pk-pk. TTL/relay mode: 50 ns at TTL levels. **GENERAL — Range:** Time A-B: 0.1 μ s to 10^4 sec. Period Average: 5×10^{-8} sec to 9999.9 sec. Events: 1 to 99999. **Resolution:** Time A-B: 100 ms to 100 ns. Period Average: 100 ns/number of periods averaged. **Accuracy:** ± 1 count, \pm time base accuracy, \pm trigger error (start/stop). **External Oscillator Input Range:** DC to 12.5 MHz. **Time Base:** Frequency: 10 MHz. Aging Rate: less than 5 ppm/year. Line Voltage Stability: less than ± 1 part in 10^4 for 10% line variation. Temperature Stability: ± 5 ppm 10°C to 40°C ambient. Referenced at 25°C . **Readout:** Five 7-segment LED's plus 3 incandescent lamps and 2 decimal points for range indication and overrange. **BCD Output:** Rear panel connector for 5 digits of BCD, Overrange flag, Completion flag, 5-volt reference (1 K Ω impedance), Ground, and Range programming inputs (binary). Maximum cable length, 18". **Power Requirements:** 105-125 volts, 50/60 Hz, 23 watts. (210-250 volts by changing internal switch and fuse). Fuse: 125 volt operation: 1/4 ampere, 125 volt slow blow. 250 volt operation: 1/8 ampere, 250 volt slow blow. **Dimensions:** 9 1/2" deep, 6 3/4" wide, 2 1/4" high. **Net Weight:** 4 1/2 lbs.

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CIRCLE NO. 56

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Application Notes

4A HYBRID VOLTAGE REGULATORS described in new application note. High-current voltage regulators that supply 5, 12, or 15V, with both crowbar-trigger load-protection and foldback self-protection, are described in this 12-page application note, "Application Considerations for Hybrid Series Voltage Regulators," AN-6026, which discusses the design, construction, and use of HC4000 power hybrid circuits. RCA Solid State Div., Box 3200, Somerville, N J 08876. **266**

SOLID STATE CHOPPER application data is available for model NS8000A transformer-isolated microchopper or analog switch. This synchronous amplitude modulator may also be used as a synchronous amplitude demodulator to convert an ac signal to dc. It is capable of linearly switching or chopping voltages over a wide dynamic range which extends down to a fraction of a mV and up to $\pm 10V$. Solid State Electronics Corp., 15321 Rayen St., Sepulveda, CA 91343. Phone (213) 894-2271. **269**

SELECTING A CORONA-DETECTION SYSTEM is simplified with the aid of a new brochure that is designed to assist potential users of corona equipment in choosing a proper system. The components of such a system are discussed along with application factors to consider. James G. Biddle Co., Township Line and Jolly Roads, Plymouth Meeting, PA 19462 **272**

INFORMATION MANUAL ON COMMUNICATIONS SYSTEMS. A new 30-page Communications, Systems General Information Manual is prepared expressly for those faced with the task of implementing a modern data communications system. The new manual begins with an introduction to data communications terms and techniques and then thoroughly discusses methods of integrating computer hardware and software into a total communications system. Request publications #PP-1200-001. EMR Computer, 8001 Bloomington Freeway, Minneapolis, MN 55420. **267**

HYBRID MICROCIRCUITS DESIGN MANUAL. An informative 24-page manual presents useful information for using or designing circuits in hybrid form. It covers thick-film component characteristics, partitioning and design rules, processing, packaging and comparison with monolithic circuits. Numerous schematics and photographs illustrate typical circuits and process information. Airpax Electronics, Control Div., 6801 W. Sunrise Blvd., Fort Lauderdale, FL 33313. **270**

MEASUREMENT OF PHASE JITTER is discussed in a four-page application note entitled "The Effect of Channel Noise and Other Additive Signals on the Measurement of Phase Jitter." The note presents a factual discussion of the various causes of channel noise and "T" carrier quantizing noise and their relationship to the measurement objectives. Hekimian Laboratories, Inc., 322 N. Stonestreet Ave., Rockville, MD 20850. **273**

SEALS AND SEALING TECHNIQUES for sealing hydraulic systems and equipment associated with handling of fluids, including those at cryogenic temperatures, are the subject of a new booklet issued jointly by NASA and the Small Business Administration. Titled *Seals and Sealing Techniques*, NASA SP-5905 (03) contains 34 abstracts. Office of Technology Utilization, Code KT, NASA Headquarters, Washington, DC 20546. **268**

"PHASE AND AMPLITUDE RESPONSE of a variable electronic filter" is the title of a new 16-page application note. A simple, general method for determination of phase and amplitude response of high-pass, low-pass, and bandpass filters is provided for four-pole Butterworth and Bessel filters. Tables and normalized plots of phase and amplitude response of high-pass, low-pass, and commonly used bandpass settings are provided. Ithaco, Inc., 735 W. Clinton St., Ithaca, NY 14850. **271**

TRANSPARENT CONDUCTIVE GLASS for electronic applications is described in a new booklet available from PPG Industries. The 12-page brochure includes product descriptions, performance characteristics and applications for NESA and Nesatron electrically conductive glasses. The custom products booklet, "NESA and Nesatron Glass," is available from PPG Industries, 10 North, 1 Gateway Center, Pittsburgh, PA 15222. **274**

REFERENCE COPIES AVAILABLE

Reference copies of the following articles are available without charge:

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163	Quad flip-flop wins logic design contest	48
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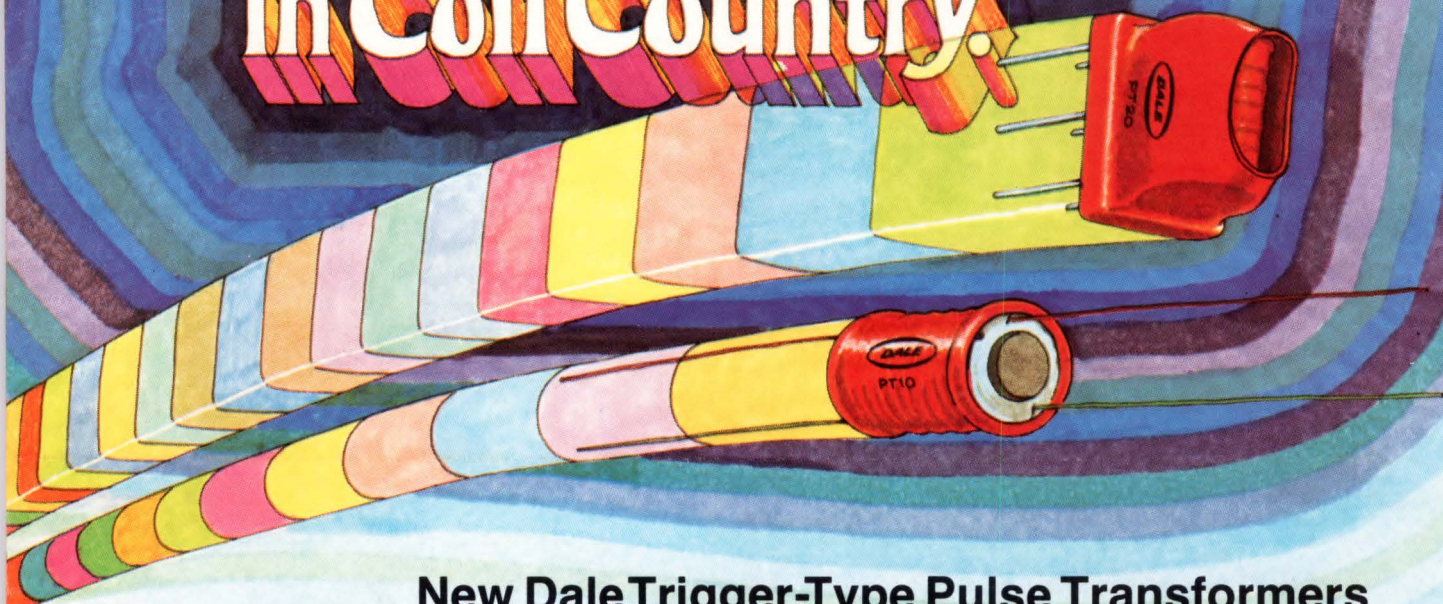
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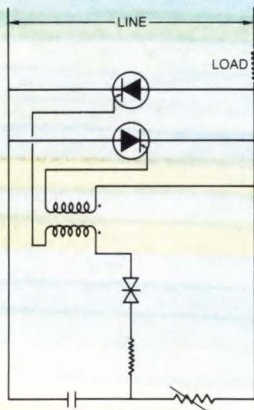
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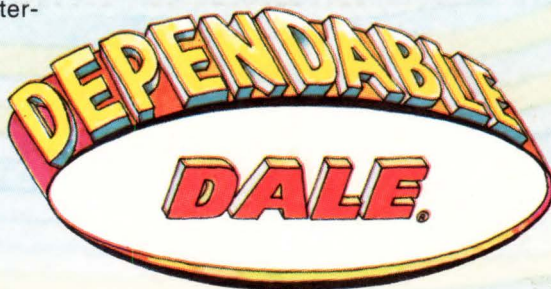
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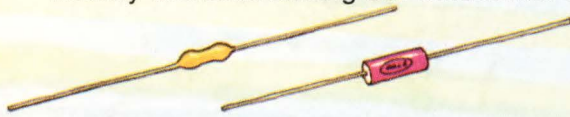
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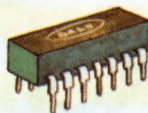


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