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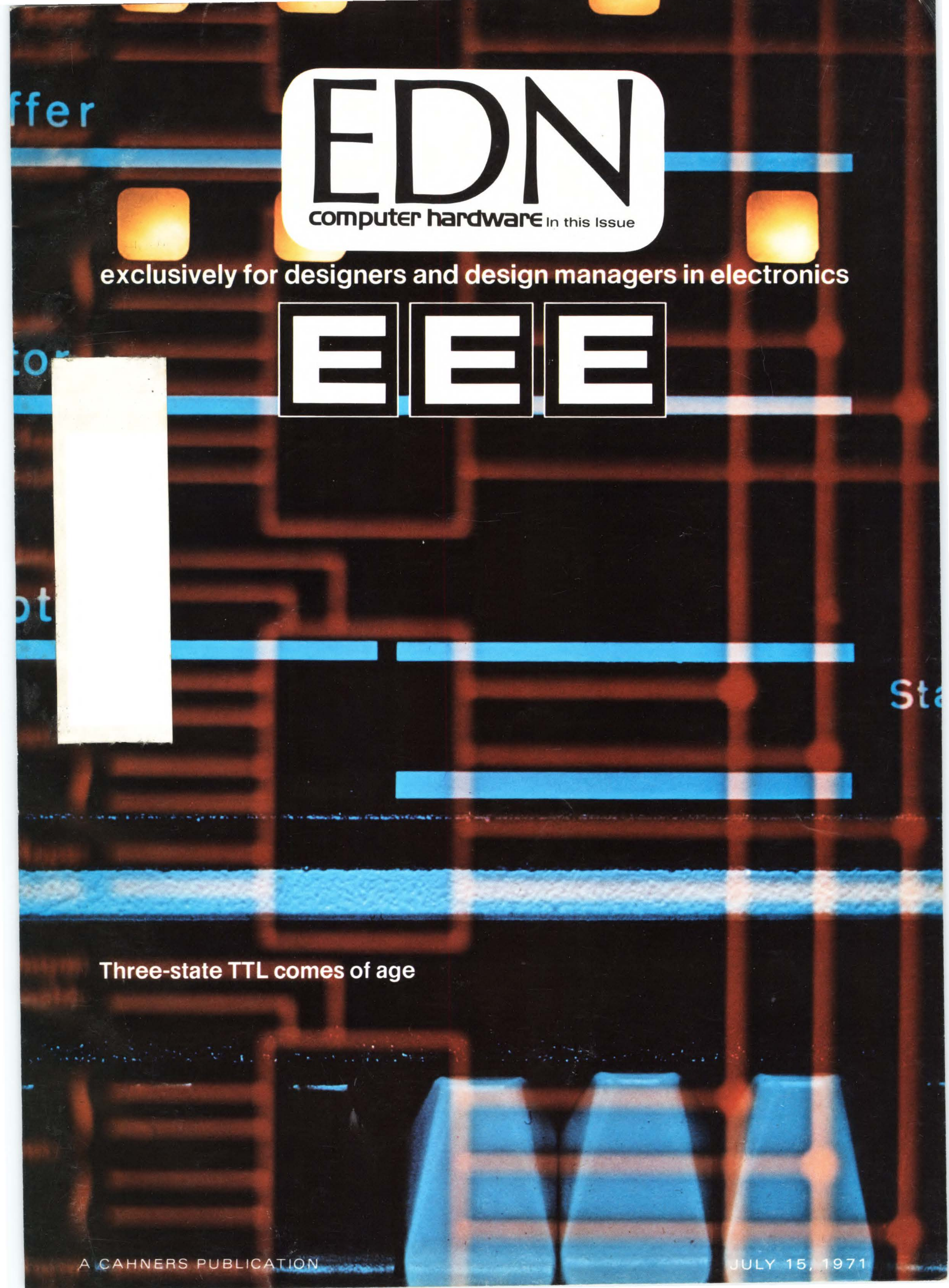
exclusively for designers and design managers in electronics

EEE



Three-state TTL comes of age

A CAHNERS PUBLICATION

JULY 15, 1971

truly remarkable

25-MHz BANDWIDTH

DELAYING SWEEP

3% ACCURACY

10-mV SENSITIVITY

DUAL TRACE &

SIGNAL DELAY LINE

ALL FOR ONLY .....

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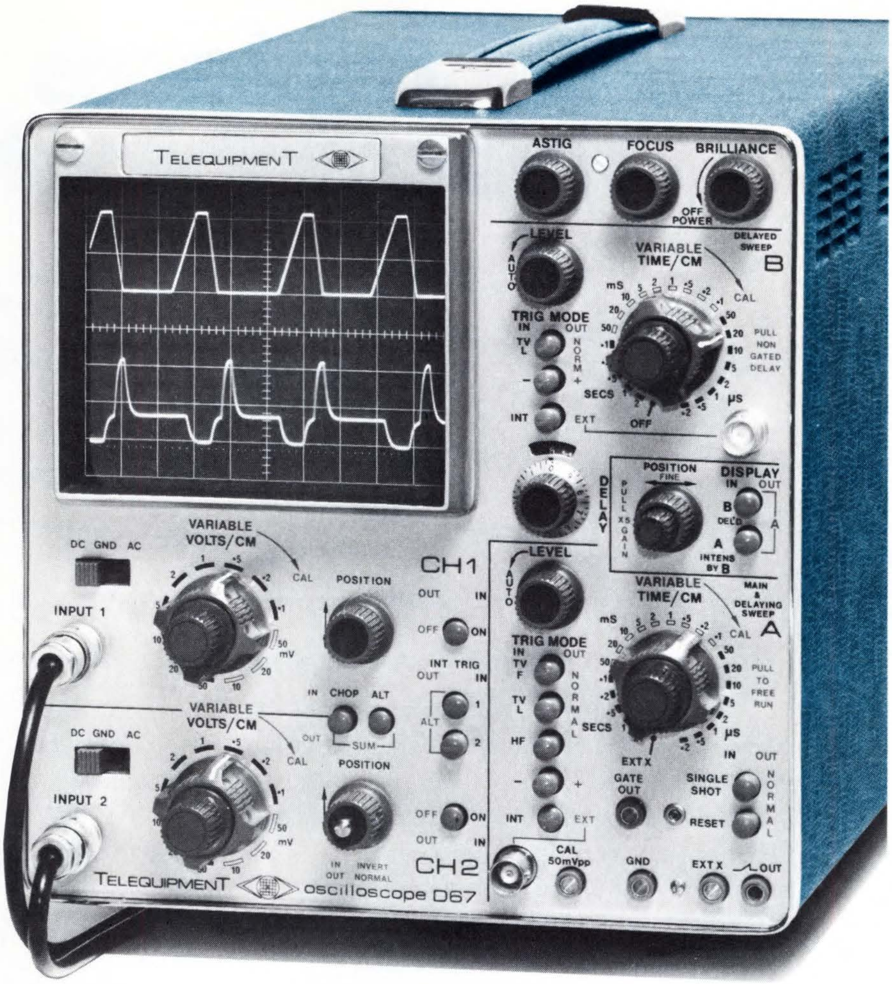


The new Telequipment D67 Oscilloscope offers the performance you have always desired at a price that is several hundred dollars lower than any other comparable model.

In addition to its impressive array of specifications, the D67 has other features not usually found in low-priced scopes: regulated power supplies, FET inputs to keep vertical trace drift to a minimum, fully solid-state design to improve reliability, transistors in sockets to make servicing easier and faster.

Bright displays are obtained by using 10-kV high voltage on the rectangular 5-inch CRT which has a big 8 x 10 cm display area.

A wide range of sweep rates from 2 s/cm to 0.2 μs/cm (40 ns with X5 magnifier), delayed sweep, 3% accuracy and 14-ns risetime, make the D67 ideal for high resolution analysis of pulse sequences. And if some of the pulses are jittery, that won't be a problem because the delayed sweep can be triggered. Those who have a need to view television signals will be pleased with the D67's ability to trigger at TV field and line rates. This feature allows viewing a selected line in a field.

Even if portability is not a prime consideration, you are certain to like the D67's lightweight—it weighs only 25 lbs.

Telequipment Oscilloscopes are marketed and supported in the U.S. through the Tektronix network of 57 Field Offices and 30 Service Centers. The instruments are warranted against defective parts and workmanship for one year. For more information call your nearby Tektronix field engineer or write: P. O. Box 500, Beaverton, Oregon 97005.

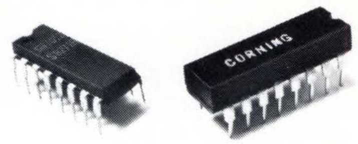
Telequipment Oscilloscope prices start as low as $245.

U.S. Sales Prices FOB Beaverton, Oregon

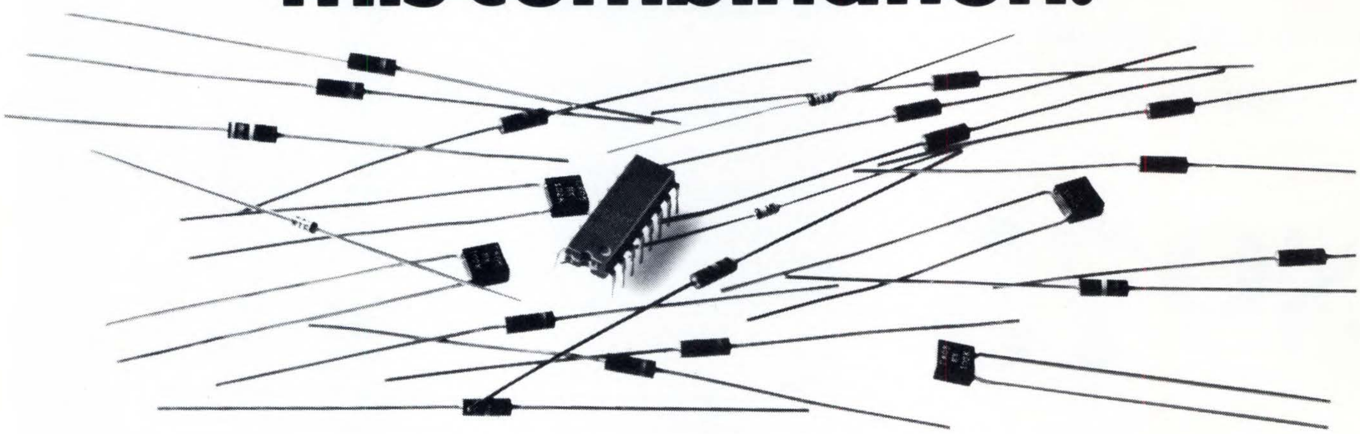
TELEQUIPMENT ® .... a subsidiary of ***Tektronix, Inc.***

CIRCLE NO. 4

This Combination

Integrated circuit  CORDIP™ Component Network

replaces this combination.



Integrated circuit plus 23 discrete resistors, capacitors, and diodes

Corning's new CORDIP™ component networks take in much of what IC's leave out—outboard discretes.

Unlike screened thick/thin film networks, CORDIP component networks give you custom combinations of discrete resistors, capacitors, and diodes in a dual in-line package.

With combinations of up to 20 components in a standard 14-pin package. Up to 23 in a 16-pin package.

With virtually unlimited circuit complexity. With all inter-connections inside the pretested package.

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Combinations of resistors, capacitors and diodes with different tolerances, temperature coefficients and ratings are available in one package.

Which makes it possible to give you almost any custom combination you specify.

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CORDIP component networks are ready to plug in and are fully compatible with IC sequencing and insertion equipment.

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	Resistors	Capacitors	Diodes
Range	10Ω-150K	10-10,000 pF	Low Signal Silicon Planar Types
Tolerance	from 1%	from 5%	
TC	from 50 ppm	+ 2%, −10%	
Ratio	>15,000:1	>1,000:1	

CORDIP™ COMPONENT NETWORKS
From

CORNING
ELECTRONICS

CIRCLE NO. 5

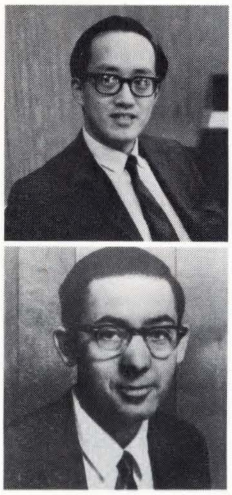
JULY 15, 1971
VOLUME 16, NUMBER 14

EDN/EEE

EXCLUSIVELY FOR DESIGNERS AND DESIGN MANAGERS IN ELECTRONICS

Cover

Cover photo from National Semiconductor shows front panel of DEC PDP-8 minicomputer with logic diagram overlay. Overlay depicts multiple "Tri-State" packages connected to common data bus in a minicomputer application. See p. 18 for "Tri-State" contest rules and introductory article. Photo by Ron Turner.



Speakout—Tom Kwei (top) and Bob Meade of Cogar. See article on p. 29.

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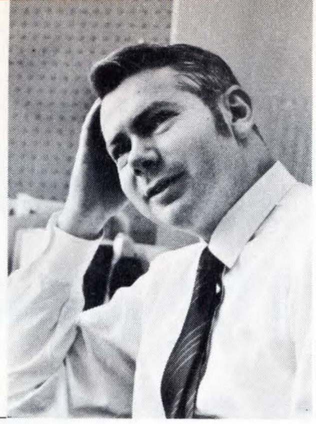

Editorial

The IC Action Will Be in Washington on August 3 and Boston on August 5

As our editors checked with IC manufacturer after manufacturer last month it became increasingly obvious that a new wave of integrated circuits was about to sweep into the marketplace.

Further discussion indicated that both linear and digital ICs including memory LSI were heavily involved and the action would be moving into high gear early in August.

Impressed by all this action, EDN/EEE secured commitments from the IC leaders to reveal their newest IC developments at two EDN/EEE new-IC programs in the East and promptly booked the Shoreham Hotel in Washington, D. C. on Tuesday, Aug. 3, and the Marriott Inn in Newton, Mass., on Thursday, Aug. 5.

So many new ICs are involved that separate rooms have been reserved for the linear and the digital/memory discussions in each hotel. While the wraps will be taken off on many of the ICs for the first time during the Aug. 3 and 5 meetings, we can give you an inkling of what the programs will contain.

At the linear seminar, for example, attendees will hear about the world's fastest operational amplifiers from Ed Fernandez of Harris Semiconductor, Motorola's Don Kesner will include analog-to-digital converters in his talk that cost one-tenth the price of similar devices now on the market, and Julius S. Lemper of RCA will introduce impressive new MOS linear ICs.

On the digital/memory side, General Instrument's Leo Cohen will cover new MOS RAMs built with single-transistor-cell construction, Daniel Baudouin of Texas Instruments will describe the latest concept in LSI complete systems to be available on one, two, or three chips, RCA's Andy Bosso will reveal new advanced complementary-symmetry MOS ICs (both memory and logic devices are involved), and Jack Sellers of Mostek will speak on ion-implanted digital ICs such as four-decade counters.

And these are only openers. Fairchild, National Semiconductor, Signetics, Precision Monolithics, Analog Devices and many other IC companies will also be on hand to talk about what they're doing.

The papers will introduce the new ICs, describe their performance capabilities, show where they fit in the marketplace and, most important, suggest rules and considerations concerning their application.

If you need to know about the new ICs and would like to be there when the devices are described for the first time, send a $25 check to EDN/EEE Seminars, 205 E. 42nd St., New York, N.Y. 10017. You can call 212-689-3250, Ext. 355 to reserve a seat.

The programs will run from 9:00 a.m. to 5:00 p.m. with coffee/Danish at 8:45 a.m., lunch at noon and an afternoon coffee/ Coke break. Extensive IC design manuals have been prepared and in addition supplemental literature will be given to all attendees.

More information and a coupon for registration appear on p. 83 of this issue.

Jerry Eimbinder

Editorial Director

Our new OEM series is the best power supply you can buy for applications that don't need the best power supply you can buy.

Most OEM applications don't need all the special features we build into our best line of power supplies. And most OEM power supply users just won't pay for features they don't need. That's why we've introduced a new power supply designed especially for the OEM user.

We call it our OEM Series power supply.

There are now 89 models in this new series from 4 to 32 volts and in current ranges from 0.9 to 36 amps. There are also ± 12 and ± 15 volt dual output models, with current ranges up to 2.7 amps. The OEM series offers 0.1% regulation instead of our usual 0.01% and comes with open frame construction instead of our usual closed black box. Aside from that, you might never notice any other difference. The OEM series features the same excellent stability, same dependable overload protection, same versatile mounting capability, same "guaranteed forever" performance and same off-the-shelf delivery. The only conspicuous difference is in the price.

So now, when you don't need the best power supply that we sell, we can sell you the best power supply that you need.

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CIRCLE NO. 8

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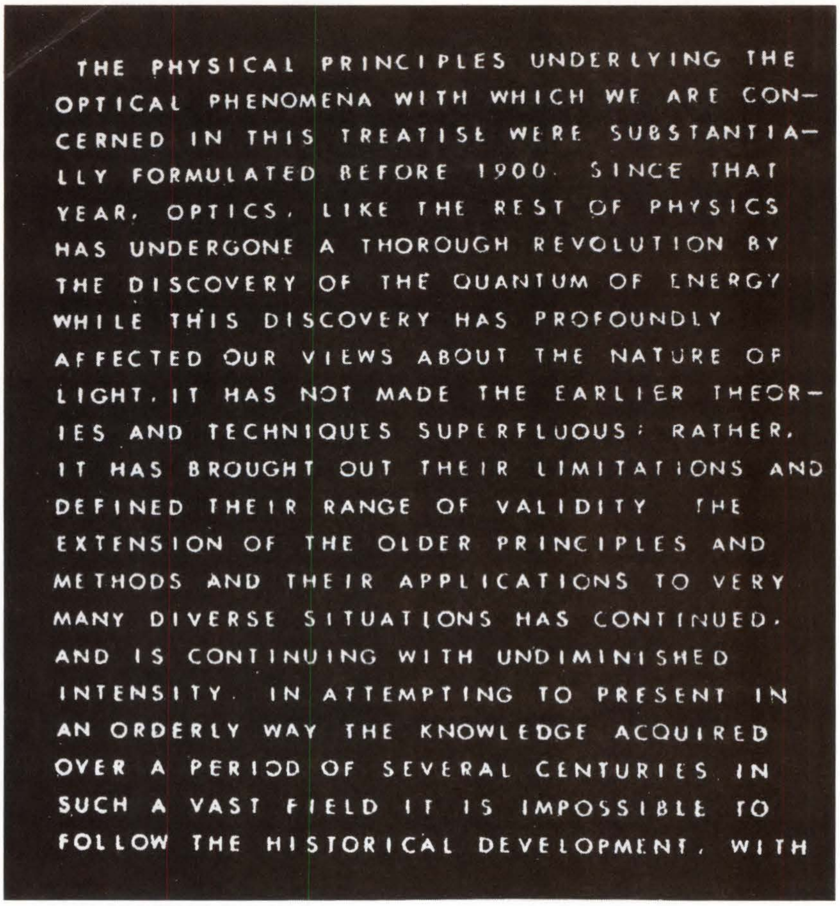


Example of information read out with laser beam. Hologram diameter: 0.5 mm.

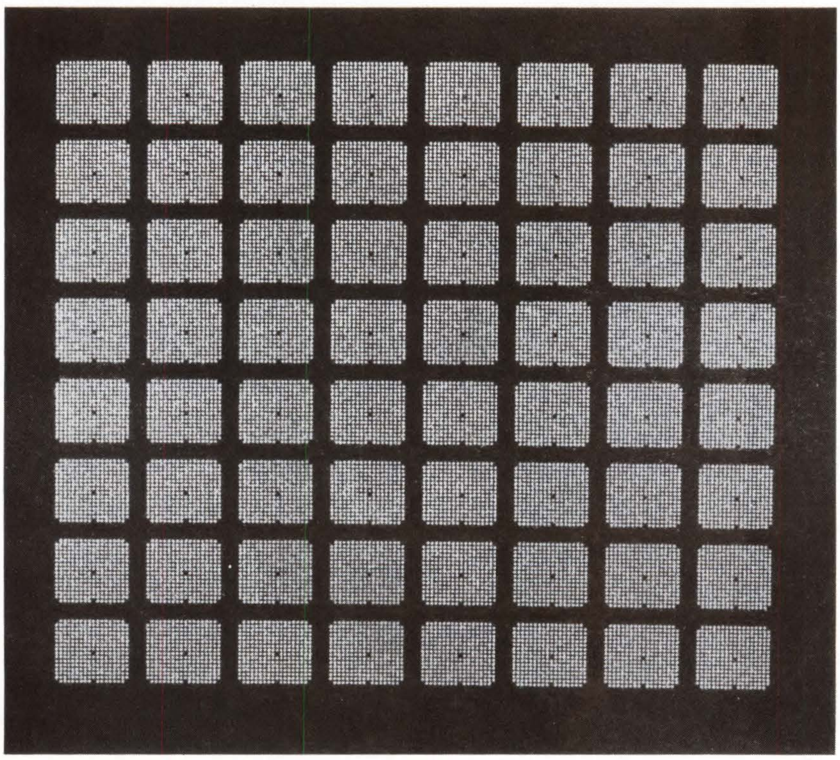


Image from Hologram.

Laser Beam Holographic Memory System Touts Higher Speed, Higher Density

The central research laboratory of Hitachi, Ltd. has reported a major breakthrough in data recording and information retrieval as applied to large capacity information processing.

This high-density holographic memory system is capable of storing 20,000 bits of digital information, equivalent to 2500 characters, in a circular space 1/2-mm in diam.

Memory storage density is 100,000 bits/mm^2. This is about 10 times more than memory devices previously announced and about 1000 times more than integrated circuit memory systems.

To achieve this 100,000/mm^2 density a special optical plate is used. The plate, which evenly diffuses the information-bearing laser beams, is made of multi-layered thin films of cerium oxide evaporated on a glass substratum through several kinds of random-patterned screens. The plate is called a "Random Phase Shifter" since the data carrying laser beams disperse as they pass through.

Among the possible applications are high speed image file memory in information retrieval systems and for large capacity high speed computers. In the latter, for example, a total of 10,000 holographic memories can be placed on a 5- by 5-cm plate. This would provide a storage capacity of 2-billion bits with a read-out speed of a few microseconds.

For more information on this new system, contact the Secretary's Office, Hitachi, Ltd., New Marunouchi Bldg., No. 5-1, 1-chome, Marunouchi, Chiyoda-ku, Tokyo 100, Japan.

Patrol officer reports his location and status to headquarters simply by touching "status" key then pressing point on grid-mounted map which coincides with his vehicle. Color-coded indicator appears immediately at that spot on dispatcher's map.

Base station equipment includes computer, map screen, and keyboard video unit for sending and receiving messages. Color-coded indicator appears at spot on headquarters map (right) when vehicle driver reveals his status and location.

System Permits Instant Vehicle Location

An electronic system that enables a driver to report the location and status of his vehicle in less than 1 sec by touching a pressure-sensitive map has been developed by GTE Sylvania Inc., a subsidiary of General Telephone & Electronics Corp.

Called digimap, the new system reduces radio channel congestion by sending messages in quick tone bursts rather than by voice. It consists of a terminal mounted in a vehicle and base station equipment that includes a computer, a map situation screen, and a keyboard video unit. Each vehicle terminal has a pressure-sensitive map mounted on a grid-coordinate board which the driver merely touches to indicate his position. The vehicle also has a keyboard and small video screen for sending and receiving messages.

The base computer decodes and processes messages, the situation screen illustrates vehicle status and location, and the keyboard video terminal transmits and receives information.

The system also permits patrol cars to send preselected messages such as "send ambulance" simply by pressing a button. In addition, they can transmit numerical and descriptive text by typing on the keyboard. License plate checks can be made from patrol cars directly to computer files in seconds.

First application will be in Oakland, Calif., where the Police Dept. plans to install the system in October.

Computer Detects Cystic Fibrosis in Newborn Babies

One child in 2500 is born with cystic fibrosis, a disabling and eventually fatal disease for which there is no known cure.

Now an IBM computer and a group of Texas A&M scientists have teamed up to spot the illness in newborn babies through analysis of their fingernails. Early detection can add many years to their lives.

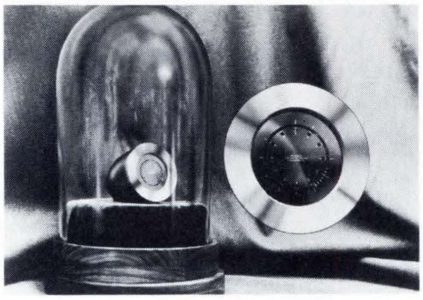
Testing is done in the Activation Analysis Research Lab., headed by Dr. R. E. Wainerdi, under the direction of Dr. L. E. Fite.

Fingernails of normal newborns contain from two to 30 parts per million of copper. Nails of children with cystic fibrosis demonstrate copper concentrations of from 50 to 200 ppm. In general, children with cystic fibrosis have a life expectancy of 5 to 15 years. Early detection and proper treatment can allow them to live three or four times that long.

Fingernail clippings are received from cystic fibrosis centers across the country. The samples and a copper standard are then irradiated, making the various trace elements radioactive. The IBM System/360 Model 65 compares the fingernail radioactivity readings against the reading from the copper sample and reports the parts-per-million copper content of the nail clipping. The entire procedure takes only a few minutes.

Fingernail samples are studied by Drs. Richard E. Wainerdi and Lloyd E. Fite. These samples are exposed to radioactivity in specially designed chambers.

Look Ma—No Hands!



Differing from conventional clocks in three major ways, a unique $25,000 desk clock developed by Motorola has no moving hands. Instead, its face contains 72 light-emitting diodes, arranged in two circles. The outside circle has 60 diodes and marks the seconds and minutes, while the inner circle has 12 diodes to mark the hours.

Inside, moving parts are replaced by ICs. Similarly a quartz crystal timing device takes the place of the conventional circular balance staff or tuning fork.

Laser Megabit Memory

A computer memory that uses laser light to permit writing, storage, readout or erasure of one million bits of data will be built by RCA for NASA. The experimental device will be 6 ft long and telescope shaped. It will be the first full-cycle, all-optical memory, setting the stage for new mass memories with the same storage capacity as disc systems, but 1000 times faster.

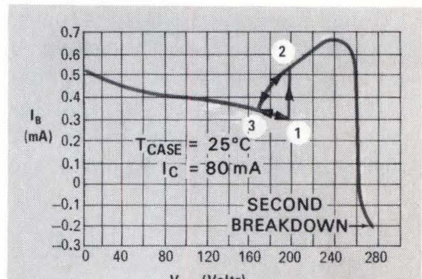
Erasure is nondestructive, so the write, read and erase operations can be repeated as often as desired.

Hotspot Studies Reveal Hysteresis

With the aid of thermosensitive phosphors, NBS scientists have found that some transistors are subject to sustained hot spots even after the operating conditions have been returned to those that previously did not cause such effects. This "hysteresis" effect (shown) may require derating of transistors beyond that needed to avoid second breakdown if reliable operation is to be had.

The phosphors used are excited by UV, and show a dimming of the visible glow as their temperature is increased. Inspection is done using a fibre optic probe. The hotspot temperature is found by comparing the observed brightness with that of an identical surface that has its temperature adjustable and monitored.

By using an observed correlation between the existence of thermal hysteresis and a simultaneous decrease in current gain, the determination of required derating is claimed to be easier than when using the more common approach of measuring thermal resistance.



Radar for the Birds

A British-made 3-cm radar detector is being used in tests that have the eventual aim of minimizing bird-aircraft collisions. Dr. Warren Flock of the Univ. of Colorado is conducting the studies at a reservoir east of Boulder, Colo. where wildlife is plentiful.

His previous studies showed that radar signatures of birds can be distinguished from other radar echoes, and that radar surveillance is superior to other types of observations for detecting potential bird hazards to aircraft.

Design Briefs

Man-Machine Link Improves Efficiency

Public telephone testing will be far nearer automation if an experimental testing device developed by Bell Labs. engineers is adopted for general use in the system. In the operation pictured, a continuous tone indicates that the telephone's coin return mechanism is in proper working order, while a beeping tone signals need for adjustment.

Similar performance checks can be made on other electrical components in the telephone by simply dialing a different series of code numbers for each check.

Microneurosurgery Teams with Color CCTV

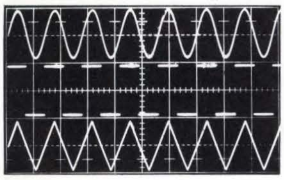
Color images from inside the human body can now be mass-viewed with high detail and excellent color fidelity because CBS Labs. has developed a low-light-level camera. Called the "Minicam", it requires only a 1 footcandle light level instead of the several thousand previously needed.

Pictures as seen on 19-inch color monitors are of studio-monitor quality, thanks to the capabilities of the sensitized SEC vidicon camera tube developed by Westinghouse Corp.

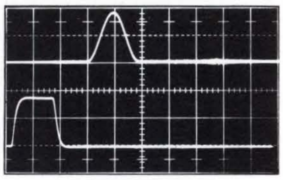
Images are picked up by a specially-devised image fibrescope that attaches to an image port of the operating microscope.

outperforms any signal source from 0.0001 Hz to 11 MHz

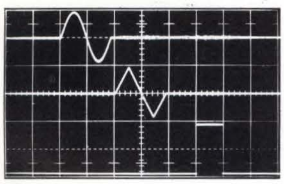
new function generator works harder, operates easier



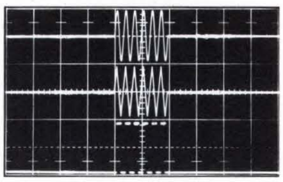
Sine, square and triangle waveforms.



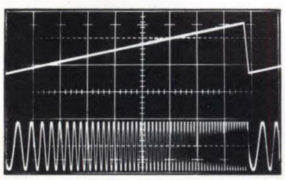
Sine² pulse (top waveform) and 100 ns pulse (bottom waveform).



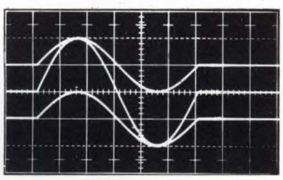
Single shot waveforms.



Burst mode.



Sweeping with internal ramp.



Fixed D.C. offset halves amplitude and offsets waveform positive or negative in relation to ground.

The new Exact Model 7060 Waveform Generator is the first in a series of higher performance instruments designed to be more useful in more test applications.

Its frequency range, from 0.0001 Hz to 11 MHz, expands the versatility of function generators into new areas. For instance, the Model 7060's ability to produce sine² waveforms at 8 MHz now provides a signal source for transmission line testing. Frequency response is flat all the way out to 11 MHz, with high quality waveforms even at the highest frequencies.

For sweep applications, the Model 7060 offers "start" and "stop" frequency controls that let you precisely set starting and stopping frequencies. Accurate Kelvin-Varley dividers tell you exact frequencies without using a counter.

As a pulse generator, the Model 7060 produces pulses with widths variable from 100 ns to 1000 seconds, and repetition rates from 0.0001 Hz to a full 11 MHz. Ramp waveforms with ramp times from 100 ns to 1000 seconds are another first in this instrument.

The Model 7060 sets the pace in D.C. offset, too, with the ability to select either fixed positive or negative or variable ±10 V offset. Offset also can be externally programmed with an analog voltage.

Two complete generators in one, the Model 7060 generates sine, square, triangle, ramp, pulse and sync waveforms, sweeps over a 1000:1 range and has pushbutton control of the operating modes of both generators. The main generator can operate in internal and external trigger modes. In the internal trigger mode, the ramp/pulse generator triggers the main generator. Other features include 80 db attenuation, V:f (voltage proportional to frequency) output, search mode, floating output, sync input for locking to an external frequency or clock and 30V P-P open circuit (15V P-P into 50 ohms) output.

Model 7060 VCF/Sweep Generator. $845.00

Waveform generators from $295

high frequency, low cost

New Model 7030 VCF Generator with 0.0001 Hz to 11 MHz frequency range, 1000:1 VCF/Sweep capability, 80 db attenuation, Kelvin-Varley divider frequency control, variable time symmetry control, search mode, and fixed positive or negative or variable ±10 V D.C. offset. Price $595.00

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CIRCLE NO. 13

TAKE A TRI-STATE TRIP

EDN / EEE and National Semiconductor Corporation are cosponsoring a TRI-STATE* IC idea contest.

The winner, naturally, will be awarded a tri-state trip. Grand prize in the contest will be two round-trip airline tickets from any major U.S. airport with stopovers in any three states the winner chooses, including Alaska and Hawaii. Runners-up will receive kits of TRI-STATE devices from National.

The winner and runners-up also will be named in EDN / EEE.

It's an easy contest to enter. There's no product to buy and no circuit designs are required. All you have to do is come up with an innovative or novel device that uses TRI-STATE circuit outputs to improve a logic design. It's your chance to devise a new TRI-STATE product that could benefit the industry.

Entries will be judged by the editors of EDN/EEE and the applications engineering staff of National Semiconductor Corp., the company that started the TRI-STATE TTL family in 1970.

For complete contest details, write on your company letterhead to National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051 or circle No. 150.

*Trademark, National Semiconductor Corporation. See p. 19 for an article that describes TRI-STATE properties and applications.

BUS-CONNECTABLE TTL ADDS A NEW STATE TO BINARY LOGIC

Only a novelty a year ago, three-state logic (TSL)[1] today offers the designer a unique measure of flexibility and performance in bus-connected logic systems. Creative application of TSL not only might solve a design problem but also might win you an exciting trip for two. (See p. 18 for details).

DALE MRAZEK, National Semiconductor Corp.

Three-state transistor-transistor logic is the first new concept in digital integrated circuitry in recent years. Because of the third stable state—a high-impedance condition that prevents data transfer—large numbers of three-state TTL circuits can communicate reliably with one another via common bus lines, at very high data rates and with excellent noise immunity.

Yet three-state TTL, or TSL for short, is fully compatible with standard TTL, also can be used with DTL, and doesn't require digital system designers to change their techniques of controlling bus-organized systems. These advantages have permitted TSL to grow from a novelty into an accepted logic family in just one short year. At least three manufacturers offer TSL now, and several others are expected to introduce TSL circuits this year. Some of the TSL functions being introduced are not achievable with practical standard TTL.

TSL's compatibility with TTL and DTL results from the characteristic that TSL, when enabled, exhibits the familiar TTL "1" or "0" states. The third, high-impedance disabled state is virtually a monolithic equivalent of an open relay contact at the TSL input or output. The third state allows TSL devices to act as input demultiplexers or output multiplexers when groups of them are operating on a bus line. Logic controls determine which devices receive or transmit the bused data. Standard TTL logic or storage elements are fabricated between the TSL stages to complete the desired IC function.

Breaking away from the TTL mold has brought performance advantages, too. Operating speed is much higher than conventional wire-OR logic with passive pullup—TSL has active pullup. Noise immunity in the "1" state is about 10 times better than TTL. Unlike standard TTL, TSL can drive transmission lines bidirectionally, and TSL drives longer lines than TTL.

TSL Development Goals

"TRI-STATE" logic was conceived as a high-performance replacement for DTL and open-collector TTL in wire-OR designs (it has since found other applications). The goal was a better interface between TTL or DTL and bus lines, rather than a logical wire-AND or wire-OR. In most cases, wire-OR means that several outputs time-share a bus line. All but one output is inhibited to prevent data interference.

Standard TTL can't be wire-OR'ed. Destructive currents may flow through connected TTL outputs. The author and his colleagues at National solved the problem by adding a current switch to the TTL "totem pole" output. This innovation permits the use of active pullup in a bus-connectable output. The undesirable characteristics of previous wire-ORable logic were caused by the passive pullup of the output. The TSL concept also was applied to TTL inputs.

A TSL output is shown on a TTL gate in **Fig. 1**. When the disable input is true, the current switch at the lower left removes output drive current. The output transistors become nonconducting, the output imped-

(Continued)

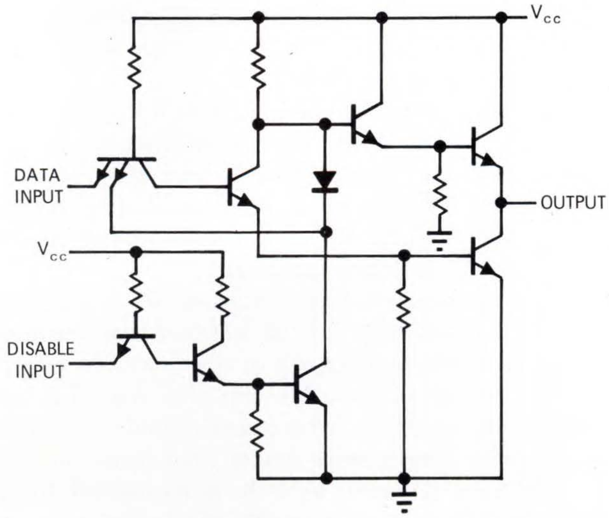


Fig. 1—**Typical gate** with three output states.

1. *The first TSL circuits were introduced by National Semiconductor in 1970. National has trademarked its designs "TRI-STATE", leaving TSL, three-state logic or three-state TTL as the generic names.*

(Continued)

TSL (Cont'd)

ance becomes very high, and at most 40 μA of leakage current will flow in the output. In this condition no definable output logic level can be detected. When the current switch is off, the output has low impedance and the output state is determined by the gate's state. Thus, logical control of the current switch serves the same purpose as strobing wire-OR logic.

The Darlington-connected upper stage seen in **Fig. 1** was added to boost the output source current in the enabled "1" state. The higher than normal source current is responsible for TSL's exceptional "1" state noise immunity and its superior line driving ability. The primary purpose, though, is to permit a driving output to source leakage current for a large number of outputs in the third state on the same bus line. Other design refinements include the use of high-current output transistors and output current limiting. These protect the outputs from being damaged by system malfunctions such as an enabled output being shorted to ground or to V_{CC}. Outputs in the third state are protected by their high impedance.

TSL Bus-Connectability

National's "TRI-STATE" outputs for the commercial version with V_{CC} = 5V ± 5% generally source at least 5.2 mA in the enabled "1" state. The military version however will source only 2 mA because of its wider V_{CC} tolerance of 5V ± 10%. If users employ a tighter tolerance power supply, then the military version will source as much current as the commercial unit. These figures range from 5 to 13 times more than minimum source current, 400 μA, of a standard TTL device with a fanout of 10. The "0" state sink current is 16 mA, the same as TTL.

TSL's higher source current allows it to source leakage into as many as 127 third-state outputs (127 × 40 μA = 5.08 mA) while driving at least three standard TTL loads. That is, up to 128 outputs may be bus-connected. At least 40 can be bused, as indicated in **Fig. 2**, with a military type unit.

Such worst-case leakage demands are rarely found in real designs. First, it is likely fewer than the maximum allowable number will be bus-connected. Second, *typical* leakage at each TSL output is much less than 40 μA. Consequently, extra source current is available to increase fanout, drive longer lines faster, or both.

"TRI-STATE" inputs have the same enabled current specs as TTL — 1.6 mA in the "0" state and 40 μA in "1". They need drive only the internal TTL stages of the IC. High-impedance leakage current is, again, 40 μA

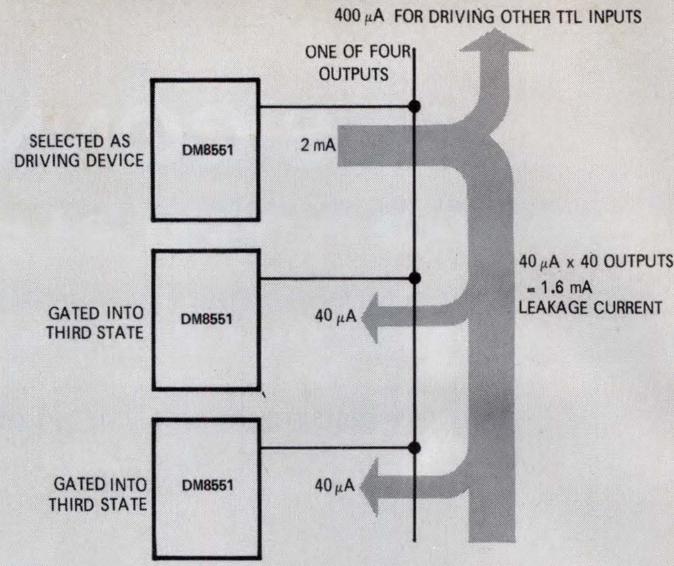
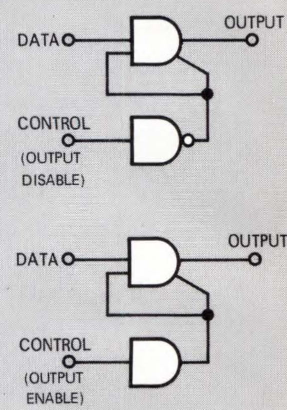


Fig. 2 — **Worst-case output** condition at 125°C.

	DATA	CONTROL	OUTPUT
DM8093	1	0	1
	0	0	0
	1	1	HI-Z
	0	1	HI-Z
DM8094	1	1	1
	0	1	0
	1	0	HI-Z
	0	0	HI-Z



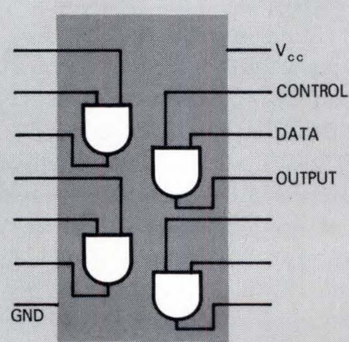


Fig. 3 — **"Tri-State" bus-buffer gate functions** and characteristics.

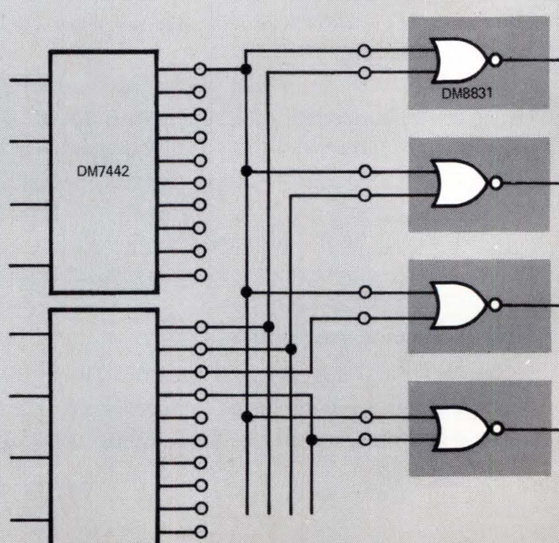


Fig. 4 — **TTL decoder** control of "Tri-State" array.

or less. Like TTL, any number of TSL inputs could be active on the same bus line but generally only 3 to 4 are active at one time.

TSL inputs have much higher effective fan-in than TTL, which means bus drivers have much higher effective fanout. Usually, in a bus-organized system, data is steered or demultiplexed into only one or a few of the inputs connected to a data bus. Suppose 50 TSL inputs are bus-connected and up to five are simultaneously enabled at any given time. The maximum total "1" state current for both enabled and disabled inputs will be 2 mA. The maximum total "0" state current will be (1.6 mA × 5) + (40 μA × 45) = 9.8 mA. This is well within the capability of either TSL outputs or conventional drivers.

Speed and Bus Delays

TSL improves effective system processing rates just as dramatically. The maximum propagation delays in complex TSL devices are generally much less than those in simple open-collector TTL gates. A passive-pullup TTL gate delay is about 30 nsec typical. Even a

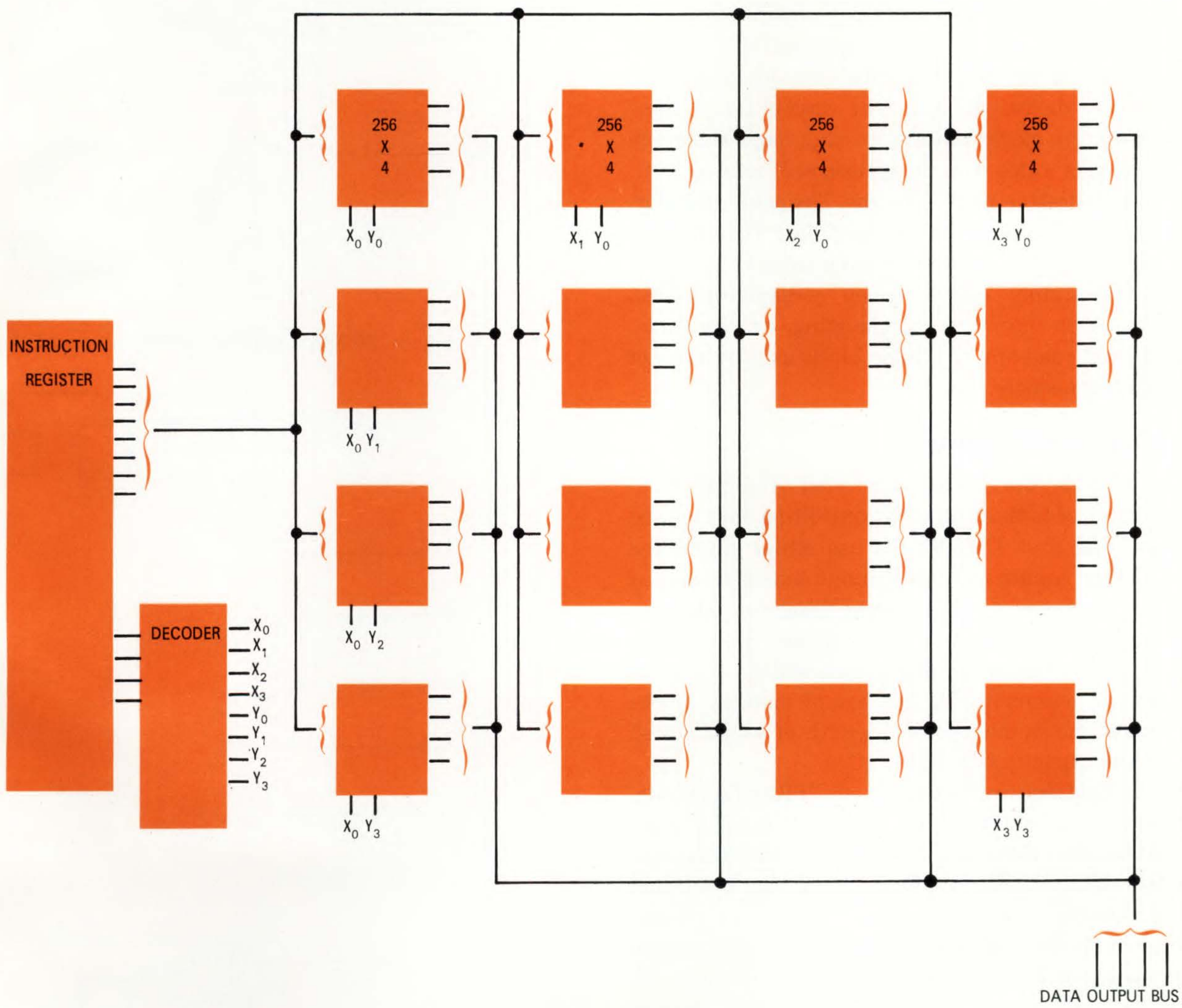


Fig. 5—**Expanded read-only memory organization.**

(Continued)

TSL (Cont'd)

40-mA TSL driver offers maximum delays ranging from 12 to 27 nsec, depending on control and data states, and 6 to 18 nsec typical.

Furthermore, the open-collector delay is specified with nominal load capacitance of 15 pF and load resistance of 4 kΩ. The pullup resistor, which must be varied in size with the logic assembly, may be larger than 4kΩ (see **Table 1**). But capacitance is almost always much higher. To the actual line capacitance, one must add about 5 pF nodal capacitance at each wire junction. Typical bus delays caused by these RC time constants run more than 100 nsec unless output buses are buffered. But buffering output buses has the same drawbacks as buffering input buses.

TSL doesn't use output pullup resistors since outputs have active pullup. Bus delays typically are less than 10 nsec, as the RC time constants are small.

Short bus delays do open the possibility of logic races arising in closed data-processing loops since any odd number of gates in a closed loop will tend to oscillate when operating nearly in sync. The usual transfer-delaying techniques could be used, but TSL offers a solution that allows high processing rates to be maintained. One simply "opens" a loop by disabling a TSL input when an output is transmitting, or vice-versa. Read-in and read-out of a logic block usually are not done simultaneously.

Enable/Disable Controls

"TRI-STATE" devices are controlled by simple techniques, similar to those already controlling data bussed systems. The first TSL devices use either single-line or NOR-type inputs to control input selection, output selection, or memory chip-enable functions. Memory building blocks with chip-enable address decoders, as well as word-address decoders, soon will be available to facilitate assembling a number of memory blocks to increase the number and/or length of words stored beyond the capacity of a single IC.

One control feature built into all "TRI-STATE" devices is a longer delay in switching from disable to enable states than from enable to disable. The difference prevents data interference by insuring that a selected device is enabled a few nanoseconds after the previously selected device is disabled. Single changes in system state variables, such as transition of one memory address bit, will control large arrays of TSL devices reliably.

Single-line control is illustrated by the "TRI-STATE" bus buffers in **Fig. 3**. The two types have opposite

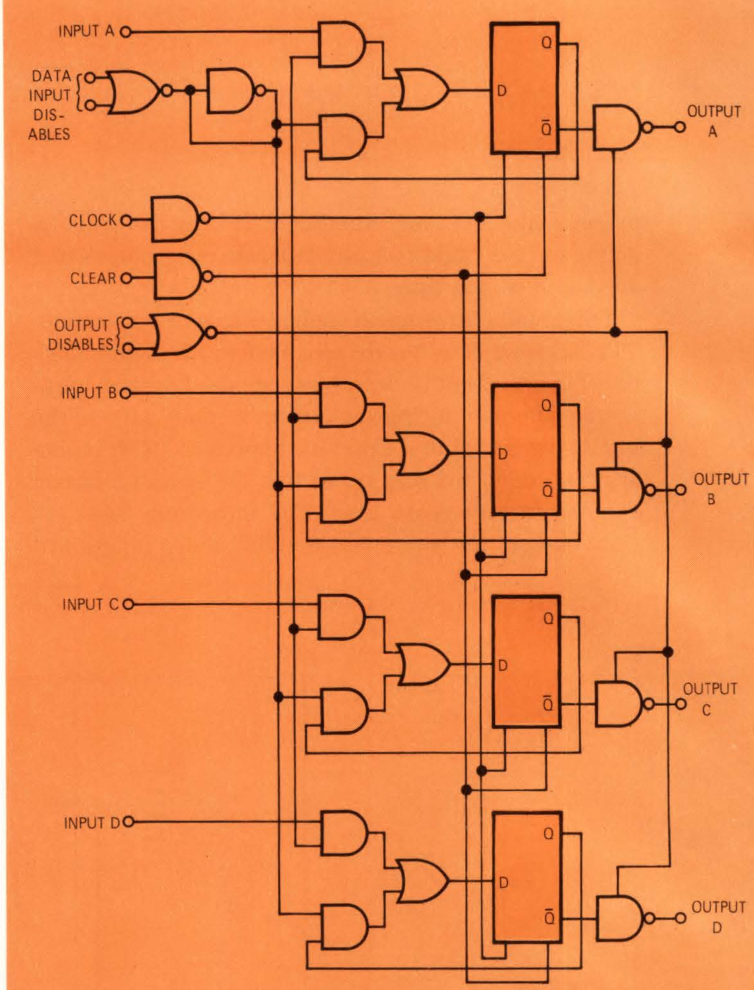


Fig. 6—**DM7551/DM8551 "Tri-State"** qual-D flip-flop.

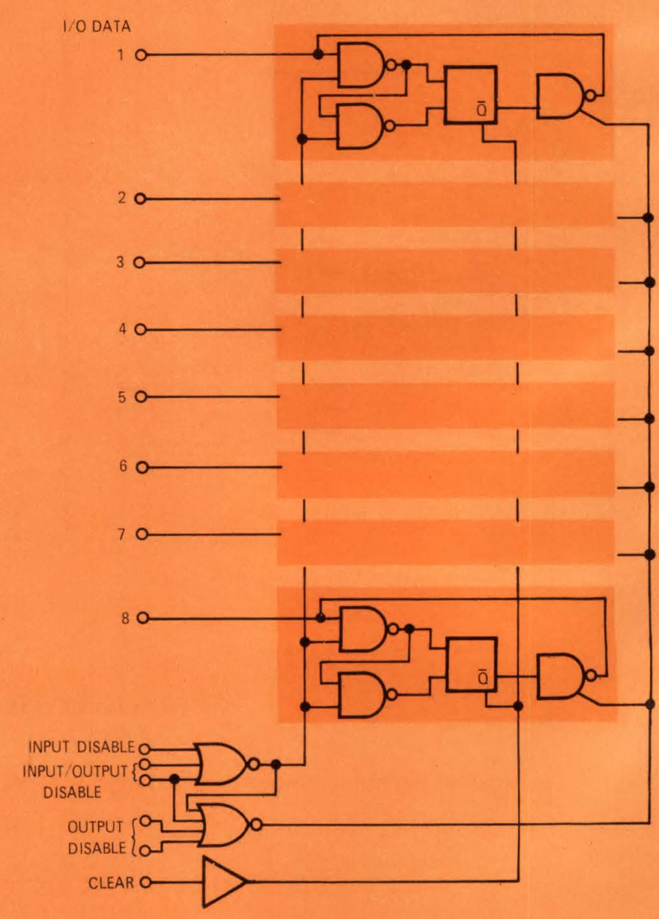


Fig. 7—**DM7553/DM8553 "Tri-State"** 8-bit storage element.

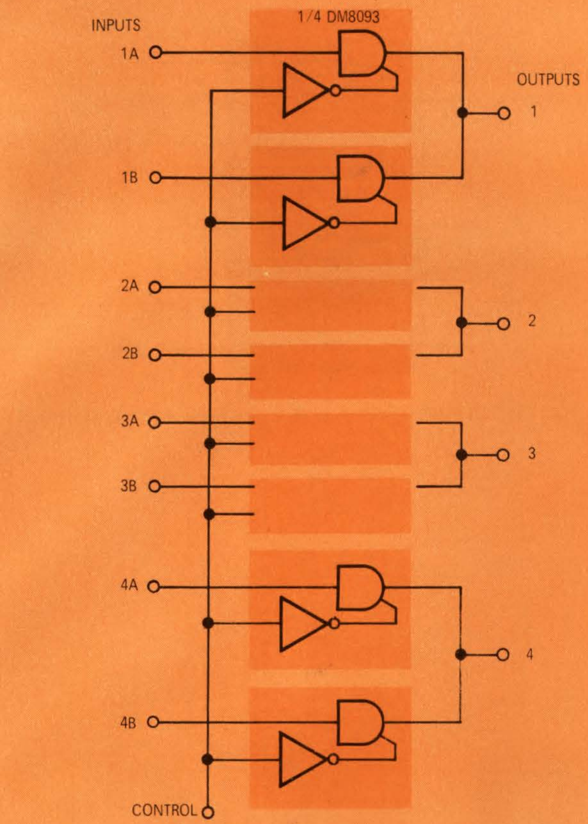


Fig. 8 – **Two-wide, 4-bit multiplexing** with "Tri-State" gates.

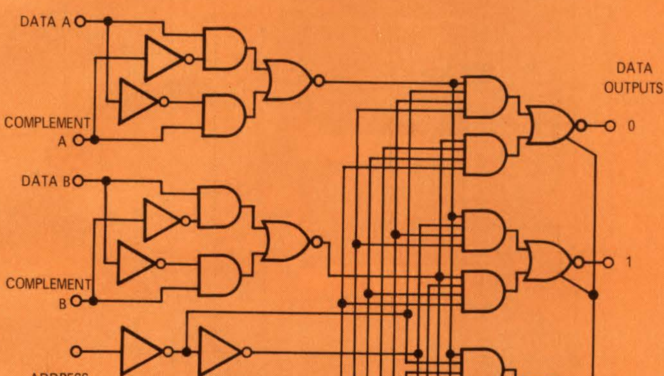


Fig. 9 – **DM7230/DM8230 "Tri-State" demultiplexer.**

DATA A	COMP A	DATA B	COMP B	ADDRESS A 2^0	ADDRESS A 2^1	ADDRESS B 2^0	ADDRESS B 2^1	DIS A	DIS B	OUT 0	OUT 1	OUT 2	OUT 3
0	0	X	X	0	0	X	X	0	1	0	1	1	1
0	1	X	X	0	0	X	X	0	1	1	1	1	1
1	0	X	X	0	0	X	X	0	1	1	1	1	1
1	1	X	X	0	0	X	X	0	1	0	1	1	1
0	0	X	X	0	1	X	X	0	1	1	0	1	1
0	1	X	X	0	1	X	X	0	1	1	1	1	1
1	0	X	X	0	1	X	X	0	1	1	1	1	1
1	1	X	X	0	1	X	X	0	1	1	0	1	1
0	0	X	X	1	0	X	X	0	1	1	1	0	1
0	1	X	X	1	0	X	X	0	1	1	1	1	1
1	0	X	X	1	0	X	X	0	1	1	1	1	1
1	1	X	X	1	0	X	X	0	1	1	1	0	1
0	0	X	X	1	1	X	X	0	1	1	1	1	0
0	1	X	X	1	1	X	X	0	1	1	1	1	1
1	0	X	X	1	1	X	X	0	1	1	1	1	1
1	1	X	X	1	1	X	X	0	1	1	1	1	0
X	X	0	0	X	X	0	0	1	0	0	1	1	1
X	X	0	1	X	X	0	0	1	0	1	1	1	1
X	X	1	0	X	X	0	0	1	0	1	1	1	1
X	X	1	1	X	X	0	0	1	0	0	1	1	1
X	X	0	0	X	X	0	1	1	0	1	0	1	1
X	X	0	1	X	X	0	1	1	0	1	1	1	1
X	X	1	0	X	X	0	1	1	0	1	1	1	1
X	X	1	1	X	X	0	1	1	0	1	0	1	1
X	X	0	0	X	X	1	0	1	0	1	1	0	1
X	X	0	1	X	X	1	0	1	0	1	1	1	1
X	X	1	0	X	X	1	0	1	0	1	1	1	1
X	X	1	1	X	X	1	0	1	0	1	1	0	1
X	X	0	0	X	X	1	1	1	0	1	1	1	0
X	X	0	1	X	X	1	1	1	0	1	1	1	1
X	X	1	0	X	X	1	1	1	0	1	1	1	1
X	X	1	1	X	X	1	1	1	0	1	1	1	0
X	X	X	X	X	X	X	X	1	1	HIZ	HIZ	HIZ	HIZ

control "sexes" and may be switched in pairs, quads, and so on, by one control line in complementary fashion. Prime application is interfacing conventional logic modules with buses, but then "gates" have many switching uses. A pair of quad buffers, for instance, can multiplex two 4-bit sets of bus lines to a main data bus.

NOR-type inputs must both be low to enable a device, which facilitates X-Y selection techniques in large systems. In **Fig. 4**, two TTL BCD decoders with active-low outputs control up to 100 TSL devices. One input may be grounded or tied to the other if single-line select is desired.

TSL Memories

TTL random-access and read-only memory circuits with TSL outputs are more expandable than memory ICs with open-collector outputs. Up to 128 TSL blocks can be connected to an output data bus, making very large, high-speed memories practical without special output buffering. The TSL circuits are pin-compatible with open-collector TTL memory blocks.

New memory designs also have TSL word-address inputs. The inputs as well as the outputs remain in the high-impedance state until the correct chip-enable code is detected by the control inputs. The 16 ROMs in the expanded array of **Fig. 5** have chip-address decoder inputs. The diagram represents a plane of 4096 4-bit words or word segments (four such planes in parallel, for instance, would store 4096 16-bit words in 64 ROM circuits).

Note that each output of the decoder drives only four chip enable inputs in the 4 × 4 plane. Also only one of the 16 ICs has its word-address inputs (register outputs) enabled at any time. TSL register outputs would easily drive the entire plane directly; in fact, they could drive four such planes at high speed. Conventional TTL ROMs would present the register outputs with over 100 mA sink current requirement if addressed in groups of 64, while by the TSL arithmetic previously cited, TSL inputs require only 8.8 mA to drive the selected input in each of four planes.

This is an excellent example of fan-in and fanout improvement. Moreover, the TSL I/O bus delays can total only 10 nsec per access while conventional blocks with buffered inputs and unbuffered outputs exhibit about 115 nsec total bus delays. The TSL blocks will have about the same internal delays as TTL blocks, 50 nsec. In other words, the memory cycle time is halved by TSL.

(Continued)

TSL (Cont'd)

TSL Storage Registers

Another device with TSL inputs and outputs, a quad D flip-flop, is shown in **Fig. 6**. This was the first "TRI-STATE" device produced in quantity. Among its applications are computer registers, variable delay buffer memories, "store and forward" multiplexers, time-sharing of displays, and busing the outputs of MOS ROMs addressed by high-speed, overlapped addressing techniques. MOS outputs lose speed when they are bus-connected; a TSL interface solves that problem, too.

A unique feature of the flip-flops is that all registers may be synchronously clocked. The clock is gated to a module at the same time the TSL inputs are enabled for data read-in. The clock does not have to be multiplexed, unlike conventional D flip-flops, which eliminates false-clocking problems. After the input is disabled, the stored bit in each binary recirculates without changing state. The data is automatically clocked out when the outputs are enabled.

Fig. 7 is another unique design. Each latch has a single I/O pin, allowing the devices to be hung on system I/O buses like appendixes. They will store data and read it out nondestructively like a scratchpad. They also will reformat data. For instance, shuffling data through a series of these 8-bit latches simulates operation of a push-down stack memory. The bits entered last can be read out first. There's no need to transfer data into main memory, the usual way stack operation is obtained.

Data-Switching Devices

Data routing is a natural TSL function. The fact that the two-wide, bidirectional multiplexer of **Fig. 8** uses five fewer gates than a conventional design illustrates the efficiency of TSL in data transfer applications (the "gates" here are the bus buffers of **Fig. 3**).

More complex switching chores are handled by the demultiplexer in **Fig. 9** and the multiplexer in **Fig. 10**. The demultiplexer switches either of two inputs to any of its four outputs. Inputs also may be complemented while being switched. Examples of TSL's bus-interchange applications are shown in **Fig. 11**. Each of the switches actually could be a multichannel assembly of many bus-connected demultiplexers. The multiplexer in **Fig. 10** operates in 8:1 or dual 4:1 modes like a TTL multiplexer. However, the TSL outputs permit multiplexers with as many as 512 channels to be assembled without the usual submultiplexers.

Very long buses and twisted-pair cables are driven

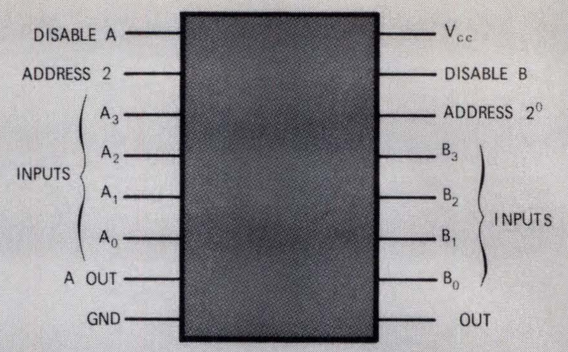


Fig. 10—**DM7214/DM8214 dual 4:1 or single 8:1 multiplexer.**

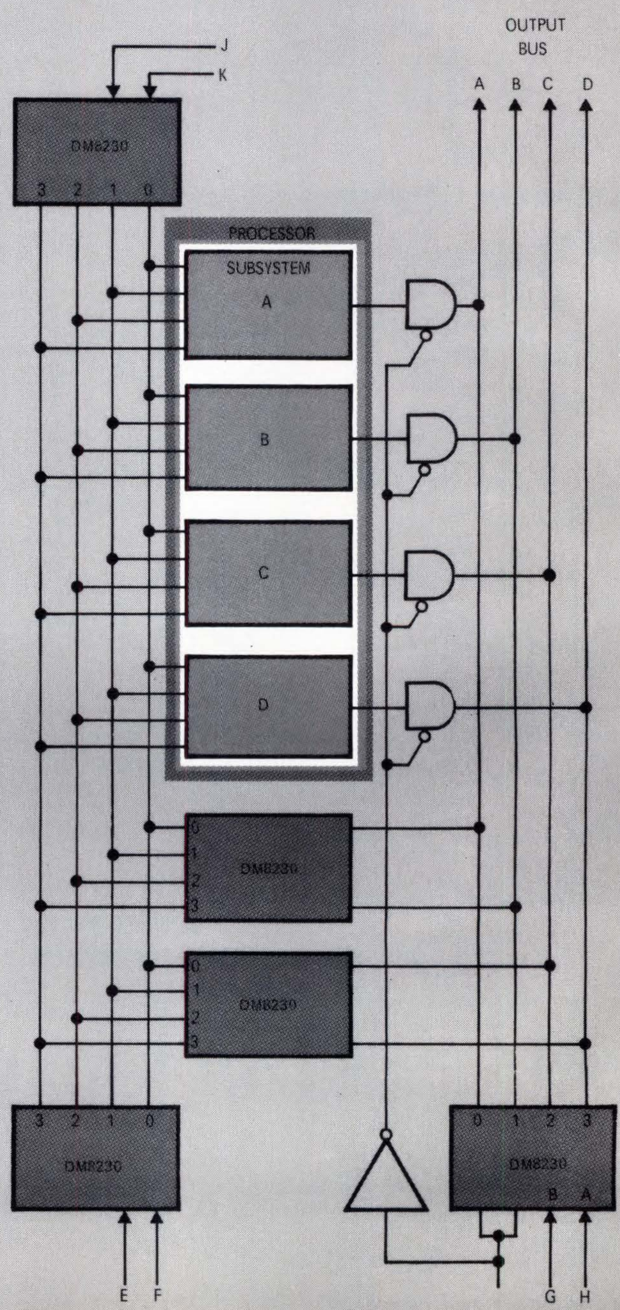
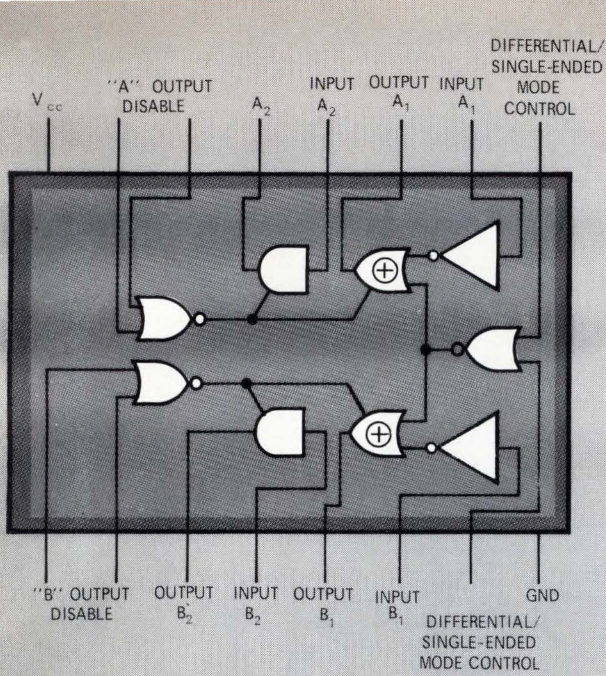


Fig. 11—**Bus interchange examples.**



truth-table (Shown for A Channels Only)

"A" OUTPUT DISABLE	DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL	INPUT A	OUTPUT A_1	INPUT A	OUTPUT A_2
0 0	0 0	Logical "1" or Logical "0"	Same as Input A_1	Logical "1" or Logical "0"	Same as Input A_2
0 0	X 1 1 X	Logical "1" or Logical "0"	Opposite of Input A_1	Logical "1" or Logical "0"	Same as Input A_2
1 X X 1	X X	X	High Impedance State	X ----	High Impedance State

Fig. 12—**DM7821/DM8831 "Tri-State" line driver.**

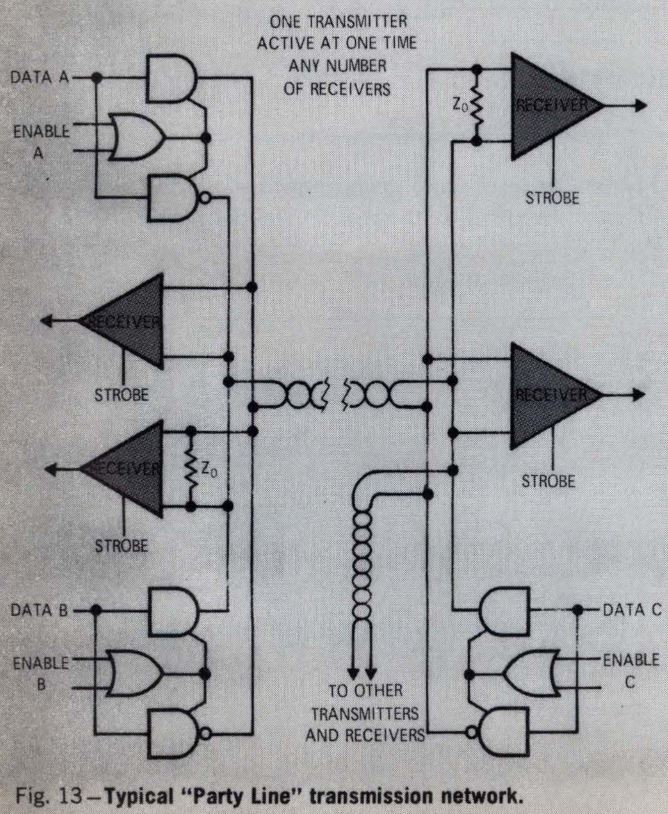


Fig. 13—**Typical "Party Line" transmission network.**

by the drivers in **Fig. 12**. The outputs sink or source 40 mA. The device contains four single-ended drivers or two differential drivers, depending on control inputs to the right-hand NOR. The two NOR inputs at the left control the four TSL outputs. Bidirectional operation of a "party line" cable structure is shown in **Fig. 13**. Don't try this with conventional TTL drivers—they would destroy one another if their outputs faced each other at these high current levels.

Unusual Applications

The device in **Fig. 14** doesn't fit into any single category. It is a 4-bit counter, latch and multiplexer all in one IC. While the counters cascade to 8 bits, 12 bits, etc., the "TRI-STATE" outputs of the latches do the multiplexing. Uses include time-sharing of peripherals such as displays and data loggers.

For instance, in **Fig. 15**, the counters sample control events, transfer their contents on command to their latches, and then resume sampling while the latches await their turn to use the single indicator decoder-driver.

Many recent applications of TSL don't involve buses. Some designers are more interested in the other features. One designer is using TSL to improve the fanout of low-power TTL in systems using a combination of LPTTL, TTL and MOS. The best LPTTL has only a fanout of two at low temperature into standard TTL, and a fanout of one standard TTL load is all the specs guarantee at high temperature. But LPTTL can drive extra TSL inputs when only one input is enabled at a time. Therefore, he puts a device with TSL inputs where storage or switching is needed after a LPTTL function.

Functions such as data "slipping", clock complementing and clock division may be done with the TSL demultiplexer or driver. These devices perform many ordinary—and unusual—logic functions when data, complement and control inputs are cross-connected. Some connections provide an output pulse only when one data input is true and the other false, and some when both data inputs have the same state. This implies that control interlock signals could be generated and distributed by the same device.

It would not make sense to use such complex devices in place of simpler conventional gates for ordinary functions, but it might be worth doing "on the fly" as data is bused. The TSL storage elements already have demonstrated the advantages of one double-barreled operation—storage with multiplexing. Also, it has been

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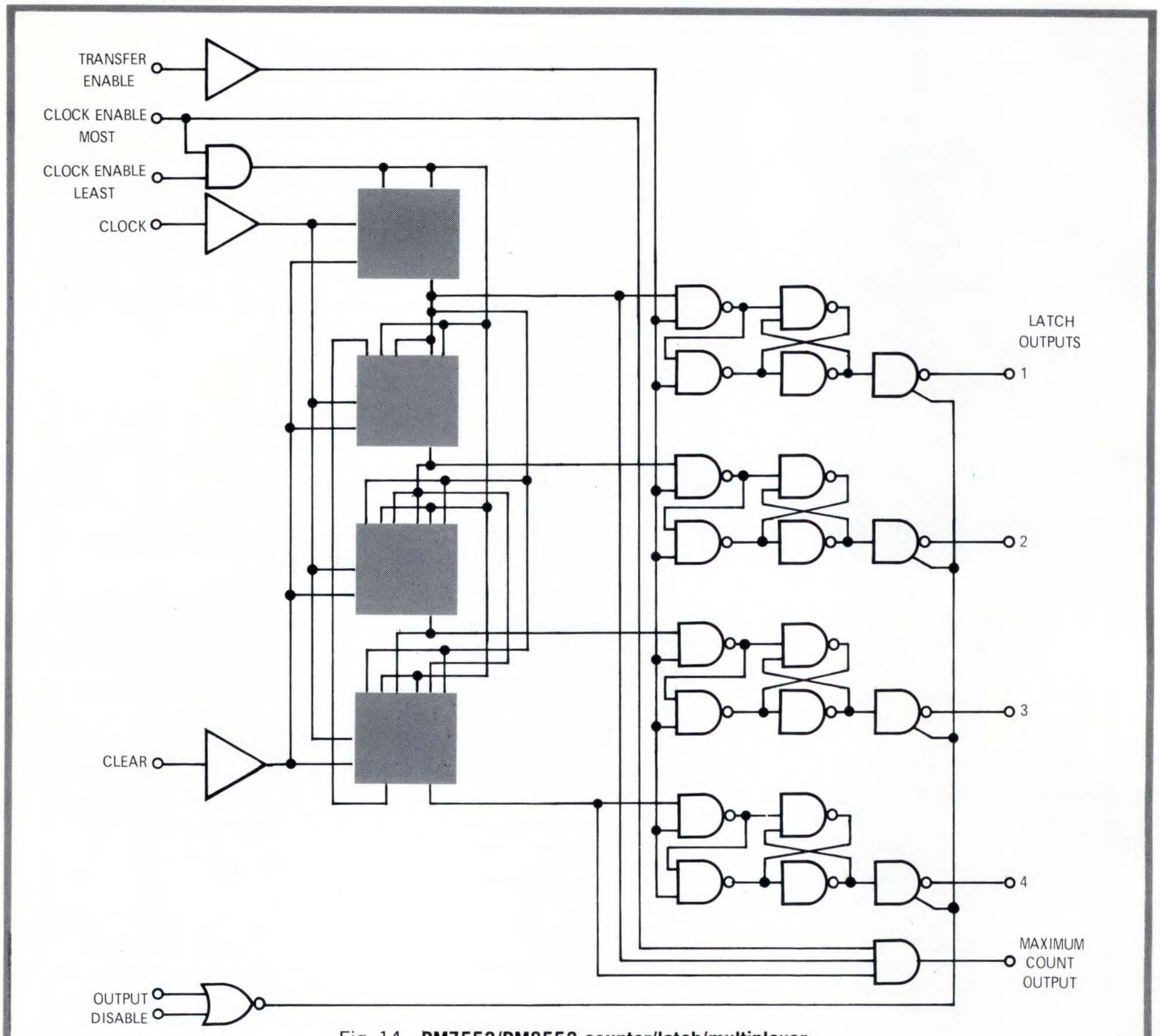

Fig. 14 – **DM7552/DM8552 counter/latch/multiplexer.**

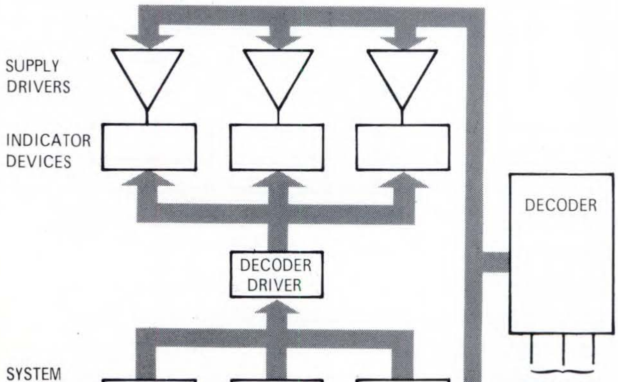

Fig. 15 – **Display system with only one decoder/driver.**

suggested that the third state itself might have a control or information meaning in some applications. The author, though, has not yet seen any practical "trinary" applications of three-state logic. ▭

Dale Mrazek, manager of digital systems applications for National Semiconductor Corp., is the originator of the "Tri-State" concept for which there is a patent application pending. Mrazek has been with the National Semiconductor for 3 years, has been granted two patents with two more pending and holds a B.S.E.E. from Denver University.

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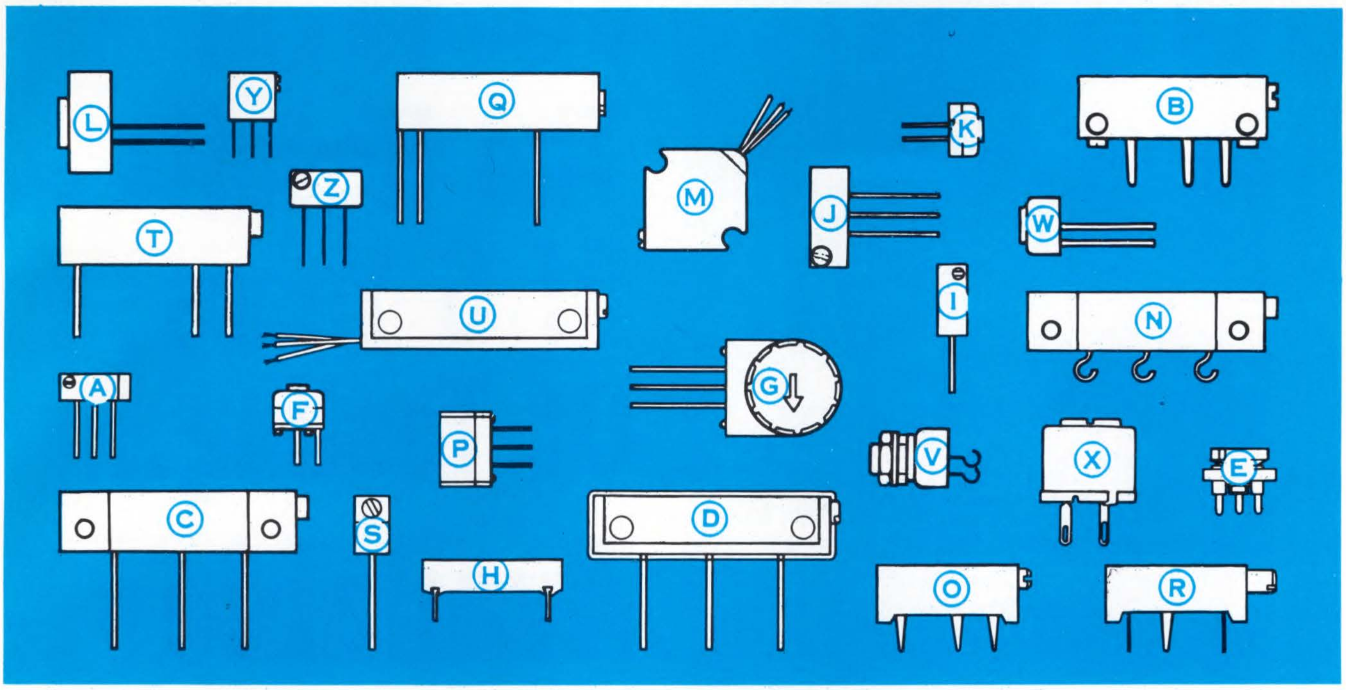

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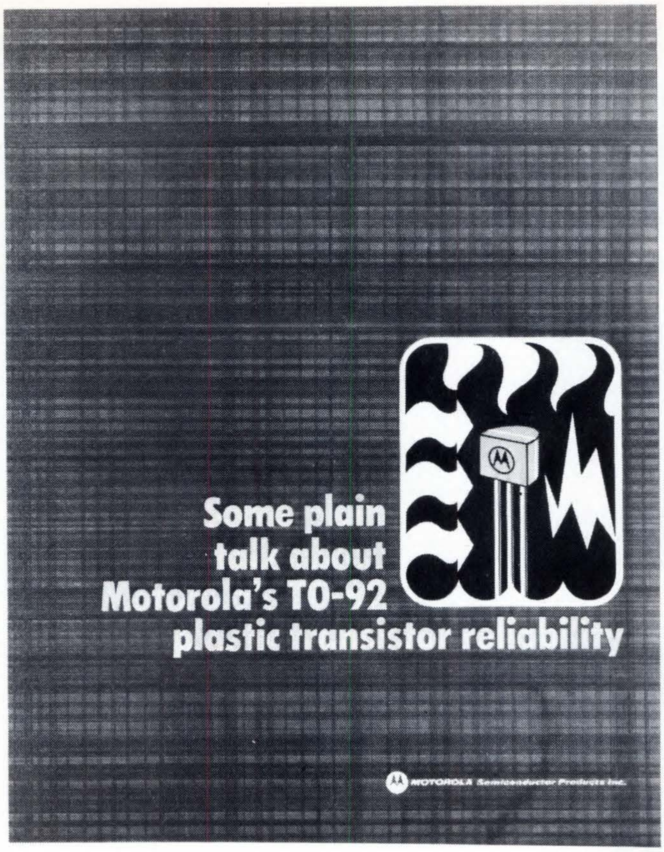

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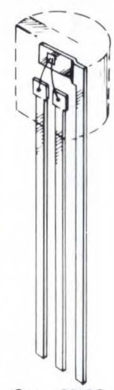

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CIRCLE NO. 50

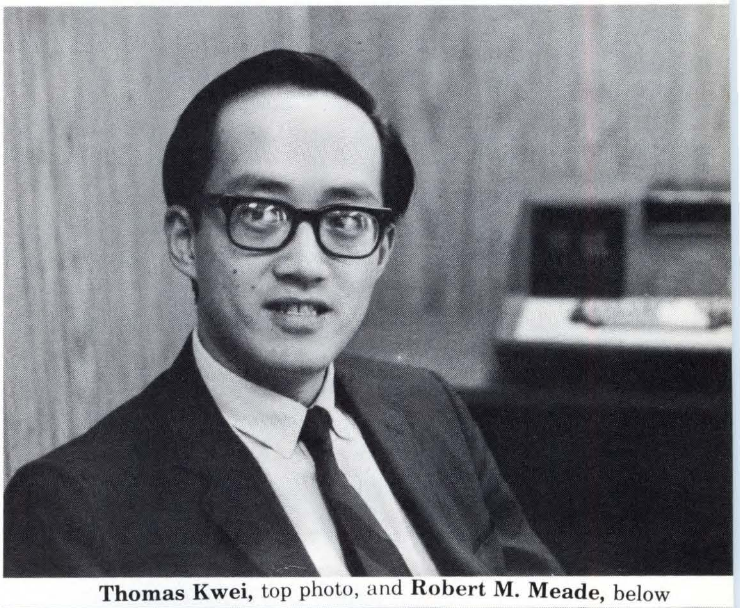
Tom Kwei and Bob Meade Of Cogar Argue The Case for Packaged Semiconductor Memory

Large-scale integration (LSI) has been extensively covered at conferences and in articles for several years now. Nothing since alchemy has been so widely discussed with so little delivered. The slow penetration of LSI can be attributed in part to the number of unique device types that have been designed, their development cost, and the limitation placed on their density by the number of terminals required to communicate between parts.

It has been argued that LSI technology is perhaps best suited for application to computer memories. The regularity of memory structure avoids the mentioned LSI limitations, and allows a single part type to meet the requirements for millions of devices or billions of circuits. It also permits maximum effective topological and electrical design of a large chip to optimize the speed-density/power product. By employing address decoding on the chip, the number of bits in an integrated circuit can be increased to fully use the chip area without being limited by the number of terminals that the chip periphery can carry. Indeed, it is entirely possible that memory is the optimum application for integrated-circuit technology.

With its heralded advantages, it has been anticipated that LSI would have an early and major impact in memories[1]. Certainly, immediate advantages accrue to the user from the intrinsic compatibility of the semiconductor memory with the semiconductor logic of the using system in factors such as signal levels, power supplies and packaging. In a broader sense, however, the acceptance of semiconductor memory by equipment designers also depends upon its compatibility with all the needs of the system design.

Thus, compatibility becomes synonymous with competitiveness. The crucial question a potential user must deal with is not how good semiconductor memories are, but rather, how good must they be to



Thomas Kwei, top photo, and **Robert M. Meade,** below

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meet his needs competitively. And this brings cores into the picture.

The fundamental parameters a system designer traditionally uses to evaluate a product include cost, performance, reliability, and, not to be overlooked, availability. But for memory products, the packing factor or density is an almost equally important parameter.

Other factors such as packaging, cooling requirements, power supplies, maintenance, modularity and volatility are important, but secondary in that they can be evaluated in terms of the fundamental parameters. The user's needs then are an interrelated set of these parameters.

The needs of the system designer are not absolute; they are derived by choosing from the viable alternatives available at the time of decision.

Thus, today the utility of semiconductor memory is still defined by its capability versus that of its principal competition: magnetic memories.

Memory application can be roughly divided into three areas on the basis of performance per unit of cost. These include large capacity (more than one million byte) memories used as an extension of addressable storage, main internal processor memories, and high performance memories that are used in leading edge or prestige systems. The improvement in memory cycle time for each of these three areas is depicted in **Fig. 1** as a function of the year

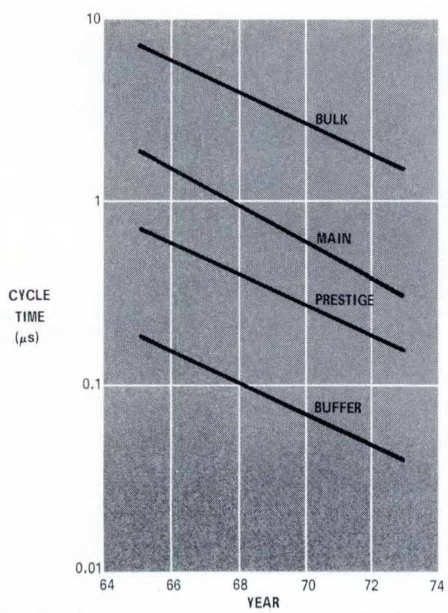

Fig. 1—**Improvement in memory cycle time** for delivered systems from 1965 (actual) to 1973 (projected).

of system shipment. The rate of improvement in the speed of magnetic memories has roughly matched that of logic circuits over the past ten years.

This figure also shows, as a dotted line, the trend of cycle time improvement for semiconductor buffer memories in the 100,000-bit capacity range. In recent years, the use of a hierarchy of memories has been found effective in providing a cost/performance system design[2,3]. By employing the relatively low capacity semiconductor buffer having a cycle matched to that of the processor in a mode transparent to the program, a system can employ a backing main memory that is optimized for low cost. The speed of the backing memory is relatively unimportant provided that the memory has an adequate data transfer rate and the buffer has adequate capacity[4].

Since the speed of the buffer must be matched to the processor's arithmetic speed, there is a strong relationship between its cycle time and the average propagation delay of available logic circuits, as shown in **Fig. 2**.

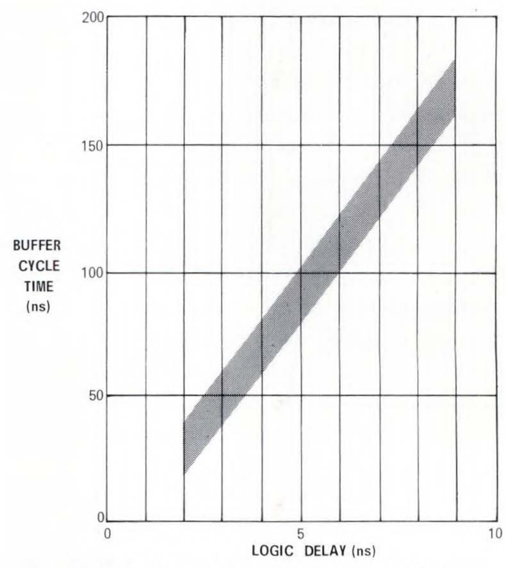

Fig. 2—**Relationship between buffer cycle time** and average propagation delay of logic ICs.

An increase in performance is generally obtained at an increase in price. Cost factors for magnetic memories now in production are illustrated in **Fig. 3**. The prices indicated are based upon quotations for purchases in volume quantities by computer manufacturers. There is a general trend to lower prices at lower performance. No clear relationship can be noted, however, because an important factor implicit in magnetic memory cost and price is the capacity of the basic core stack.

Prices for presently available magnetic memories as a function of their capacity are shown in **Fig. 4**. The relationship between parameters here is stronger. This occurs because larger memory modules employ support circuits, and packaging, construction and testing is more efficient.

For semiconductor memories, the knee of the price/capacity curve occurs at a much lower capacity. This is because semiconductor memory is naturally constructed from IC packages. This leads to a planar plug-in memory module of relatively standard dimensions and to a capacity determined by the point at which minimum cost is achieved. Alternatively, 3-D memory-type packaging could be employed, but this approach tends to increase cost without sufficient improvement in performance[5].

Since 1955, the main memory capacity of systems in a given price class has increased by more than a factor of 4 every 5 years. This trend is continuing.

The improvement in reliability that has been achieved in terms of mean-time-between-failures per megabit of memory as a function of time is shown in **Fig. 5**. At present, magnetic memories are achieving an MTBF of from 2000 to 4000 hours in million-bit arrays. With a continuation of this trend, in about three years, an MTBF of at least 10,000

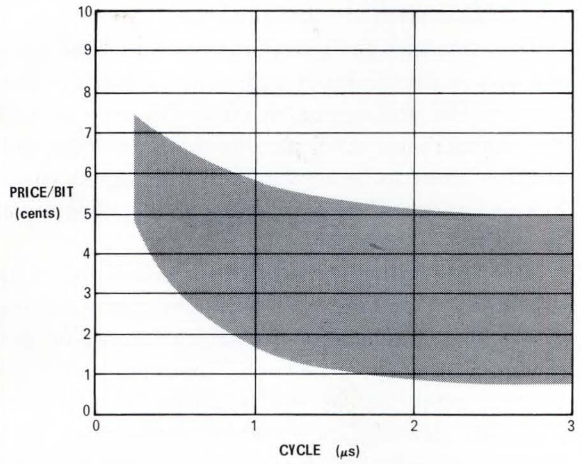

Fig. 3—**Magnetic memory price** per bit vs cycle time in microseconds.

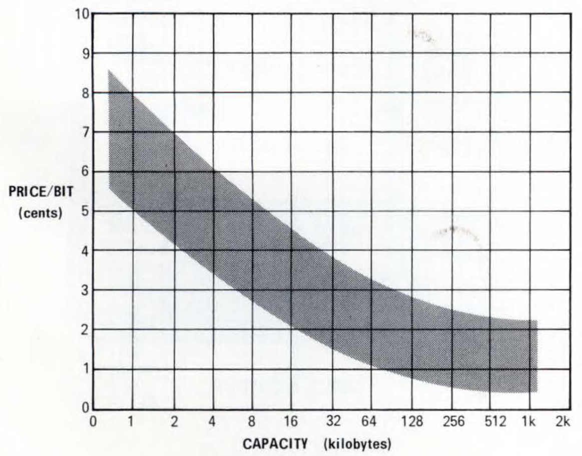

Fig. 4—**Price per bit** for currently available magnetic memories as a function of memory size.

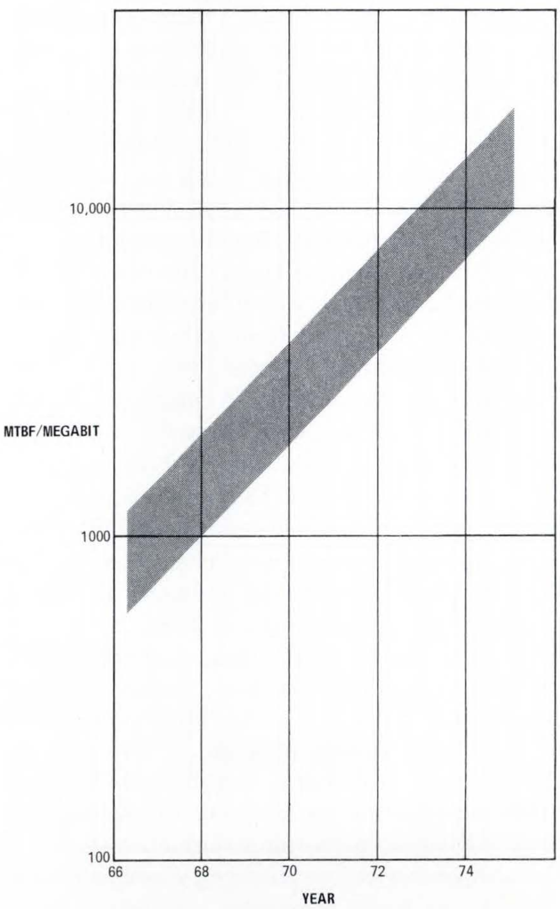

Fig. 5—**Reliability** of main memories expressed in MTBF.

hours per megabit is anticipated and this should be considered a minimum figure.

Poor reliability causes significant out-of-pocket expenditures. For purchase customers, annual maintenance costs typically fall in the range of 10 to 15% of system purchase cost. For computer manufacturers, the cost of maintenance may be as much as 25% of the pricing cost of a rental system.

Historically, reliability has not been the strongest virtue of the component industry. To achieve a goal competitive with magnetic memories, a major commitment is required by the semiconductor industry.

A concerted effort must be made to better identify and understand failure modes and to engineer semiconductor memory products for minimum susceptibility to failure mechanisms.

Techniques of automation and batch fabrication are required not just to produce memory products more efficiently but also to produce them in a more consistent fashion to achieve high reliability.

System memory requirements are now looked at by designers in terms of is it beneficial to go to semiconductor memory instead of using core memory. To make this type of evaluation, both forms of building semiconductor memory should be explored.

One of the two forms is simply the use of an IC package that must be designed into a memory system by the user. The other form is the larger-capacity functional memory system. The latter form usually provides the more valid comparison when semiconductor and magnetic memories are to be evaluated for a given application by a core user.

Let's consider the design of a typical memory system from presently available component products. A list of assumptions and typical characteristics for semiconductor memory devices reflecting the present state of the art is shown in **Table 1**. In this example, it is assumed that a memory of 8192 words by 18 bits is required. The basic storage element chosen for this example is a 1024-bit dynamic MOS chip in a dual in-line package. A dynamic or charge-storage cell design is a good choice because it offers superior cost performance in applications that do not require premium performance alone.

The components can be placed on a card as shown in **Fig. 6** and many companies can supply basic cards of this general approach. This particular example includes a matrix of storage packages together with the support circuit packages needed to do buffering, decoding, powering, output data latching, and termination. For this example, discrete components are needed to perform certain drive functions.

The critical signal path for the card is indicated in the diagram. The input address lines must first be buffered by circuits noted as decoders. These circuits generate true and complement signals from the single line inputs and decode the binary address so that only one row of array packages is selected. They also buffer all address and control lines which permits them to drive a number of cards in parallel, without excessive loading. The address lines, together with necessary control lines, are driven up the column of the card. They are then powered by the driver circuits across the card to select the storage array circuits. The outputs of the storage circuits are sense signals which are routed back down the card toward the connector edge. These are gated and stored in the latch circuits and driven back to the using system via the connector.

This approach to layout provides an effective signal path with the input and output circuits located close to the card connector edge. The flow controls the signal skew and permits both selection and sensing lines to be terminated. The signal wiring can be accomplished with orthogonal conductors on two printed-circuit planes.

The results to be expected from such a design are summarized in **Table 2**. Using the given assumptions, it is practical to package an array of 4096 words of nine bits on a card. This requires an area approximately ten by twelve inches when the circuits are mounted in standard dual in-line packages. To achieve this density, it is necessary to distribute power on internal planes of the card; thus,

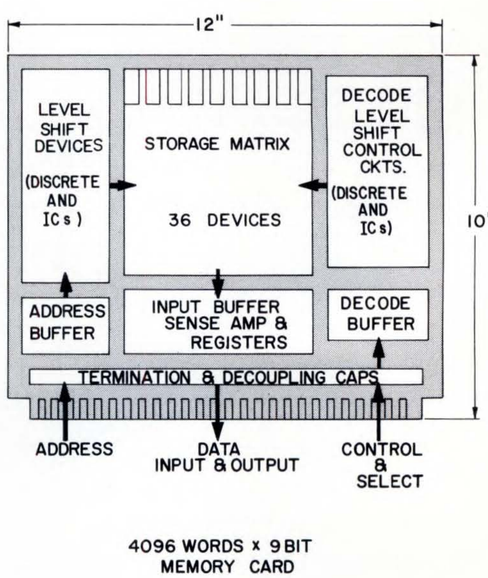

Fig. 6—**Layout** of memory card.

typically, a four-conductor-layer card is needed. The internal voltage distribution also provides ground-plane control for the signal wiring, which may be necessary for noise immunity.

To accomplish the overall memory function, various types of support circuits are required on the card as shown in **Fig. 6**. As the result of the peripheral circuit and card delays, the memory subsystem performance is degraded in access time from the 300 nsec of the storage circuit to approximately 600 nsec at the card level. The general trend is such that as the basic storage circuits are made faster, the percentage degradation in speed at the memory level increases.

Four of these 4096-word cards are required to achieve the specified total memory capacity of 8192 words of 18 bits. This illustrates the convenient horizontal and vertical modularity of semiconductor memory.

As an alternate choice, a user may purchase a complete memory subsystem. For example, today one can buy on a single 8.8 by 7.9-inch card an 8192 word × 18 bit memory packaged with TTL compatible I/O levels. The access time at the system level is 250 nsec, with a 300 nsec cycle time.

Significant hardware costs must be added to those of the basic storage circuits in completing the functional memory. Typical costs for presently available support circuits, cards, and passive components spread over the 36,864 bits of the illustrative card design are shown in **Table 3**. These accumulate to \$0.05 per bit or more. As storage circuit costs are reduced, these additional costs become increasingly significant.

The memory user accumulates program costs in addition to the cost of the basic hardware. A few examples of these include testing, inventory, records and service costs. The magnitude of these depends upon the level of assembly that the user chooses to purchase. The effort involved in obtaining a functional memory can be viewed as a pyramid of endeavor as shown in **Fig. 7**.

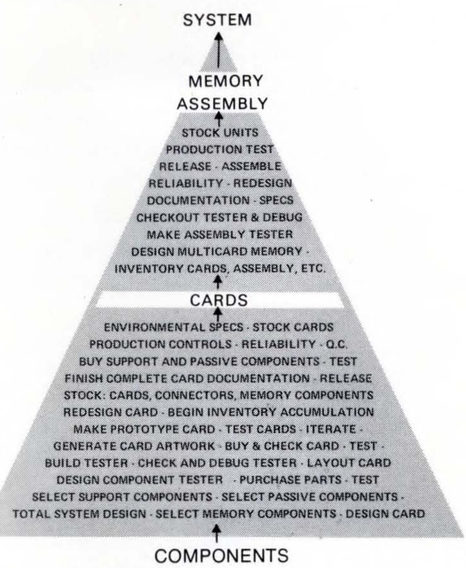

Fig. 7—**Memory pyramid** of endeavor.

Starting at the base provides a user with a maximum value-added[6] but also a maximum expenditure of resources and accumulation of these program costs. It is axiomatic that the utility of a product is a function of the absence of value-that-must-be-added in order to make it useful.

A sample calculation of these supplemental costs[7] is shown in **Table 4**. Using a production volume of 100 megabits per year, these costs accumulate to more than \$0.06 per bit for the user who chooses to enter the assembly pyramid at the component level. Still more significant are his expenditures in capital, factory floor space and personnel. These costs include only production supplementals. The development effort in product design, test equipment procurement, component evaluation, vendor liason, engineering records, etc. must also be assessed. Thus, the system manufacturer must determine whether or not the return on investment required to start at a lower level of assembly is sufficient. In addition, he must decide whether or not

MEMORY REQUIREMENT
8192 words X 18 bits
MEMORY DEVICE ASSUMPTIONS
Capacity = 1024 bits
Access Time = 300 ns
Cycle Time = 500 ns
Dynamic Storage

Table 1

RESULTS OF MEMORY CARD DESIGN
Capacity = 4096 words X 9 bits
Cycle Time = 400 ns
Access Time = 600 ns
Power = 25 W
Card Size = 12 in X 10 in

Table 2

ADDED HARDWARE COSTS	Cents/Bit
Support Circuits	0.29
Card	0.20
Passive	0.01
Total	0.50

Table 3

SUPPLEMENTAL COSTS (at 100 Mbits/year)	Cents/Bit
Testing Dip	0.08
Assembly	0.06
Card Test	0.07
Inventory	0.07 (0.03/bit)
Rejected Dip	0.08
Repair	0.20
QC	0.06
Total	0.62/bit

Table 4

this expenditure has a higher profit potential than the available alternatives.

The example described above was intended to indicate the present compatibility of semiconductor memories with the user's needs, as defined by the available alternatives. By comparison with **Figs. 3** and **4**, it can be seen that the 16k byte semiconductor-memory module is price-competitive in speed, density and power. It can be concluded that at these capacities compatible semiconductor memories are here now.

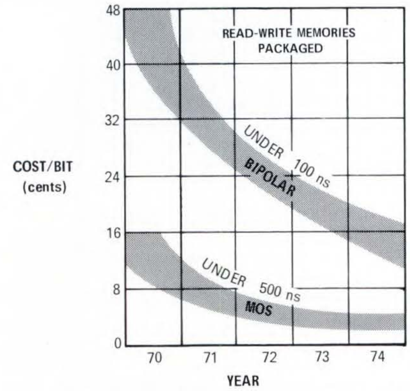

Fig. 8—**Semiconductor memory cost** per bit as a function of year of delivery.

It is apparent as well, that the semiconductor devices of this example could not compete effectively in an application involving multi-million-byte magnetic memories. To project the growth in practical semiconductor-memory application, it is necessary to look closely at the rate of cost reduction. This is shown[8] in **Fig. 8**; such progress is possible because a manufacturing base can be established in areas that are competitive now.

We will see a continuing trend for semiconductor memories to be more and more compatible with the user's needs in ever increasing capacities.

This trend is shown in **Fig. 9**. Semiconductor memories have dominated the scratch-pad area of internal processors in capacities in the order of 1000 bits since 1965. The evolution to capacities of 10,000 bits, a 1k buffer for example, was natural.

The development of memory hierarchy theory has led to the use of high-speed monolithic memories in the 100,000-bit range. The trend is leading to delivery of multimillion dollar bit memories in 1971 and to multimillion byte memories in the near future.

The validity of this trend toward the increasing dominance of semiconductor memory depends upon

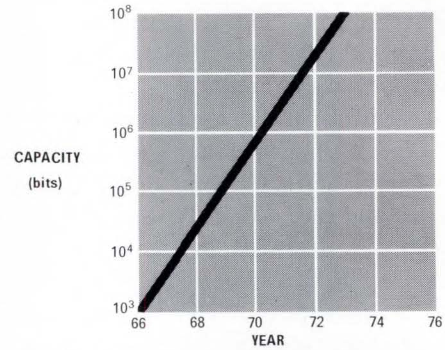

Fig. 9—**Capacity of semiconductor memory** as a function of year of delivery.

a high degree of accomplishment by the semiconductor industry. To reach the expected maturity however, the projected improvements in price will have to be accompanied by progress in reliability. The indications are that high-density semiconductor memory with price and reliability superior to that of cores is a reachable goal. ▭

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Cogar's Kwei and Meade

Both Thomas Kwei and Robert M. Meade joined Cogar in early 1969, a few months after the company was formed.

Kwei is manager of systems applications at Cogar; he was formerly with IBM, where he was mainly involved in the design of random-access and read-only memory systems. He has B.S.E.E. and M.S.E.E. degrees from Yale University.

Meade is manager of product programming and is involved in manufacturing, planning and development efforts for internal information systems. He was with IBM for 14 years and was IBM's manager of memory technical strategy when he joined Cogar. Meade has B.S.E.E. and M.S.E.E. degrees from Rensselaer Polytechnic Institute.

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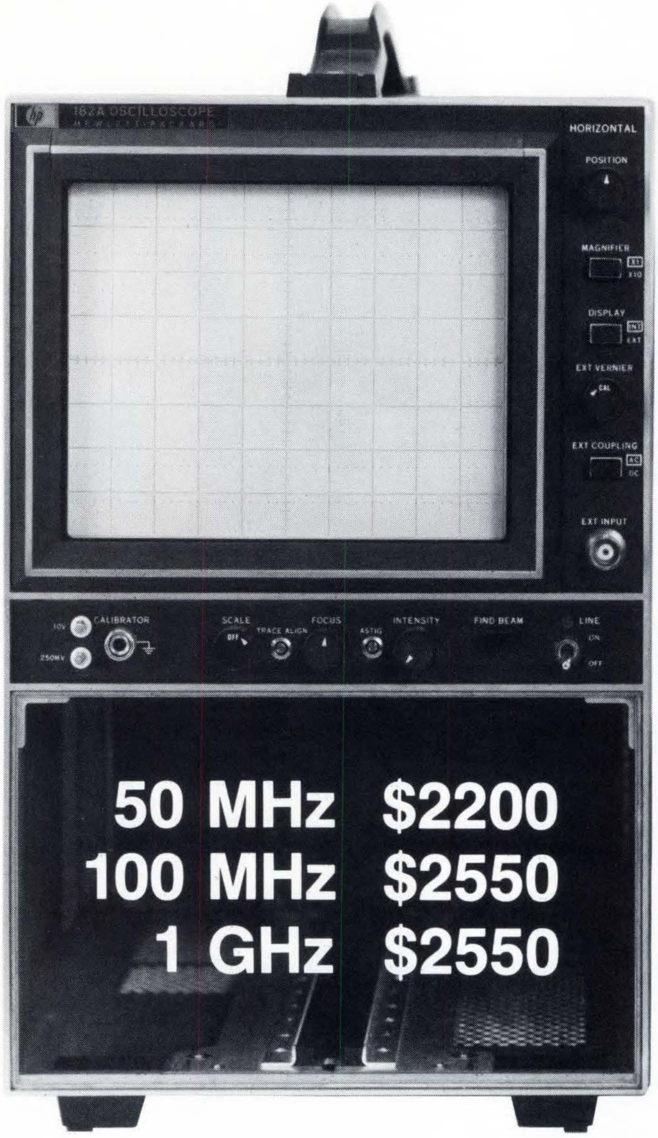

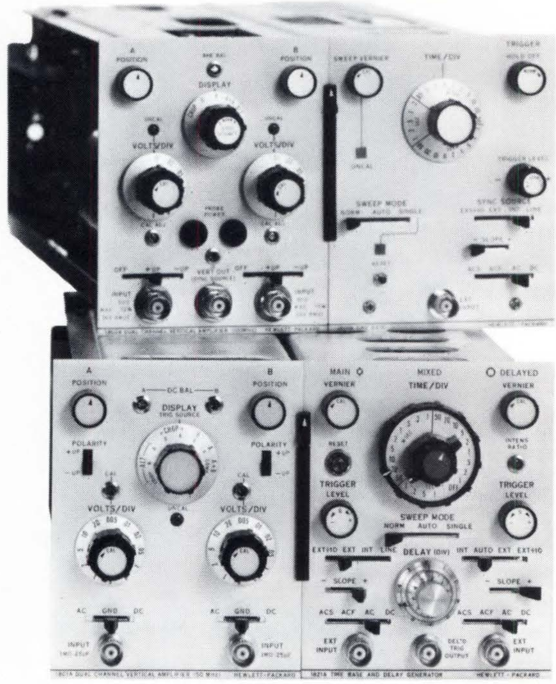

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AIRBORNE POWER SUPPLIES FOR TWTs

If you're designing supplies for TWTs you'll find this a handy guide to the supply types and their merits. Or, if you're buying TWT supplies, this will help you assess the know-how and capability of your source.

STEVE SMITH, Quatt Wunkery

Traveling-wave tubes are used mainly in applications that require a large instantaneous bandwidth, such as communications and electronic counter measures (ECM). For either use the design techniques and standards are about equally stringent.

Instantaneous bandwidths of up to 2:1, at frequencies between 250 MHz and 18 GHz are representative, while power levels range from milliwatts to tens of kilowatts of RF (CW), or hundreds of kilowatts pulsed.

TWT equipment for either communications or ECM is primarily airborne, though much is also shipborne. Design techniques for airborne TWT power will be discussed, and in a concluding article guidelines will be given for selecting an initial design approach based on size, weight, cost, and feasibility factors.

Here we are concerned with only those TWTs with nominal output ratings above 50W CW RF or a few hundred watts pulsed. Typical voltage ranges, power levels, voltage regulation requirements and applications are listed in **Table 1**.

From the schematic (**Fig. 1**), it is apparent that the tightly-regulated helix power supply does not provide the majority of the beam current. It must provide, in fact, only that fraction of the beam current intercepted by the helix. Most of the beam current is supplied by the less tightly-regulated collector supply.

Aircraft Power Systems. Aircraft power has been standardized at 28V dc and 115V, 3 ϕ, 400 Hz ac. Sometimes both are available for operating TWT supplies, sometimes only one. Transients on those sources, of course, become input transients of the TWT supplies that use them. The customary standard to reference for input transients is MIL-STD-704. While this standard was based on conditions that were obtained aboard WW II aircraft, modern aircraft generators are rarely as rough. However, considering that the equipment may be tested in the lab by engineers who can make mistakes, that it operates from generators that can malfunction, and that it may be used in systems that generate transients, it is not unreasonable to ask

APPLICATION	DUTY	PEAK POWER (kW)	HELIX SUPPLY		COLLECTOR SUPPLY		SPECIAL REQUIREMENTS
			V	REG.	V	REG.	
CROSS-SECTION STUDIES	0.001 (TYP)	0.1 - 1	10 kV	0.1%	10 kV	0.1%	Fast rise. Large "On"/"Off" Ratio
ECM	0.005 - 0.2	2 - 50	10 - 30 kV	1%	6-20 kV	10%	Absolutely Reliable
DOPPLER	CW	0.1-up	6-30 kV	0.001-0.1%	5-20 kV	0.01-1%	Noise on helix supply < 1 Part in 10^6
COMMUNICATIONS	CW	0.1 up	3 kV-up	0.01-0.1%	2.5 kV-up	0.1-10%	Noise on helix supply < 1 Part in 10^4

Table 1—**TWT requirements.**

(Continued)

for compliance with this standard. In the higher power systems the cost of compliance may become a significant portion of the total system cost, so it may be wise to question it there.

Conventional Approaches

Table 2 lists some of the more conventional design approaches to power supplies. Each of the following sections is numbered to conform to that same item number in **Table 2**. These sections give a short word picture on each approach.

1) The linear regulator (nonswitching type) is a fine choice if low efficiency is acceptable (expect 50% or so for the whole power supply). For regulator power-output levels to about 100W, the heat sink requirements are reasonable. This approach is also a good choice where the customer doesn't want anything too sophisticated and where there isn't a large budget for the project nor any development dollars. At the 100W level, very few of the problems intrinsic to high power inverters show up, and the inverter design is fairly straightforward. To keep cost and noise down, 20 kHz is a good inverter frequency.

2) If from 100W to a kilowatt or so is needed, and/or power supply efficiency must be above 75%, it's best to plan on a switching regulator. If system efficiency must be around 85%, $100 transistors will be needed instead of $10 types. Finally, if funding is available and the utmost in size and weight reduction is required, plan on some very careful circuit design, a 100-kHz switching regulator, a 50- to 200-kHz inverter, and plan to house all power circuitry in hybrid packages. Better plan on a lot of time too, because while feasible, this design probably will take a man-year or so to learn how to get optimum performance from a 60A, 300V, 20-MHz transistor. If there is no need for a sophisticated design, build a 500W switching regulator that weighs a pound or two, chops at 10 to 20 kHz and gives fairly good regulation.

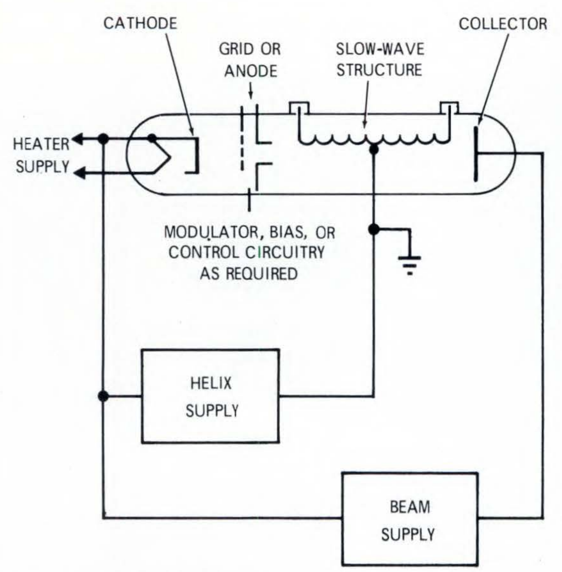


Fig. 1 – **Schematic** showing helix and collector beam power supplies.

At power levels above a few hundred watts, inverters begin to show their fangs. Single transformer types and driven types become somewhat undependable, and much grief can be saved by going directly to a two-transformer Jensen circuit (**Fig. 2**). Starting this circuit under load, or charging a filter capacitor on the secondary, will cause problems, so serious consideration should be given to placing a slow runup circuit in the supply regulator to eliminate current surge. If the full military temperature range of −54 to +71°C must be met (+125°C is not rare), it would be best to have much practical experience or, lacking this experience, plan to spend some R&D dollars. Sometimes the inverter won't start when it's cold, and sometimes, at high junction temperatures, the switching transistors can't take the current transients even though they are "operated within safe operating area ratings".

A 500W, 1-kHz inverter will weigh 5 or 6 lb, and a 500W, 10-kHz inverter will weigh perhaps 2 lb. A 500W at 100-kHz inverter can be designed to weigh 3 to 5 oz with 93% efficiency if there is enough money available. The use of this approach for a helix supply is not too common at high power levels unless it is mandatory to use 28V dc power for the entire system. In this case, a collector supply is needed that can deliver 5 to 10 times more power. If the 28V causes problems, plan on using ac input power, or on having many inverters with their rectified secondaries in series to supply the collector power. This approach uses many components, but can be quite reliable. However, it will be impractical to reduce noise below 1 part in 10^3 or 10^4.

3) This approach is a good choice where power levels are moderate and a switching preregulator can be used to absorb input voltage variations. Let the switching regulator chop at the lowest frequency that permits acceptable size and weight of output choke. Doing so reduces the gain-bandwidth requirements of the linear regulator, which senses the high voltage output directly. Power levels above about 600W are not too practical because of pass transistor dissipation requirements.

4) Unless a great deal of prior design work has been

expended, this approach should have first preference, especially at power levels above a kilowatt. Despite the difficulty in finding beam-power pass tubes with suitable ratings, this approach requires very little knowledge that the average systems engineer doesn't have. Short-circuit immunity is high. The upper limit on power is entirely determined by the availability of pass tubes. Rugged pass tubes that can operate in virtually any environment are available. A relatively low-frequency transformer and filter are necessary, and will be moderately heavy and bulky. Efficiency will be on the order of 50% to 80%, depending on the range of input line voltage variation. Even if it is necessary to finance the development of a special pass tube this still may be preferable to the chance of losing tens or hundreds of kilobucks by embarking on a solid-state regulator/inverter development program.

5.1) One of the most practical conventional all-solid-state approaches is to use an input isolation transformer and rectifier to deliver about 100 to 200V dc to a switching regulator, which then delivers 30 to 120V to a dc-ac inverter and step-up transformer. Available are 60A, 300V high-speed transistors. A pair of these in an inverter will give good performance at 40A line current and a 120V dc input. Similarly, one of these in a switching regulator will deliver 40A from input voltages as high as 250V. Thus we can place an upper power limit of 4.8 kW on this approach. It is possible to parallel several transistors, but care must be taken to allow for inequalities in gain and switching times.

Other techniques should have serious consideration when higher power levels are required. For some reason an inappropriate amount of money gets spent on parallel-transistor techniques as compared to single-transistor ones, especially when fast switching times are required. Size, weight, and efficiency can all be quite good, depending somewhat on packaging expertise. Generally, a 4.8-kW switching regulator or inverter can be packaged in 50 cubic inches for about $40K to $80K, or 200 cubic inches for about $20K to $40K. Input and output transformers are not included in the above estimate. If this looks like a serious strain on your budget, reconsider the decisions that led you here.

5.2) The use of an SCR inverter will remove the limitations on power for that portion of the circuit, but the question of the switching regulator still remains. I suspect that a switching regulator could be built using an SCR as the pass element, therefore it is probably feasible for power levels up to 100 kW or so, and should be seriously considered above 2 or 3 kW. Size and weight advantages will be significant above 10 to 20 kW.

6) In a last-ditch attempt to reduce the projected system weight and size, somebody usually suggests getting rid of the input isolation transformer to permit rectifying the line directly, then feeding the rectified

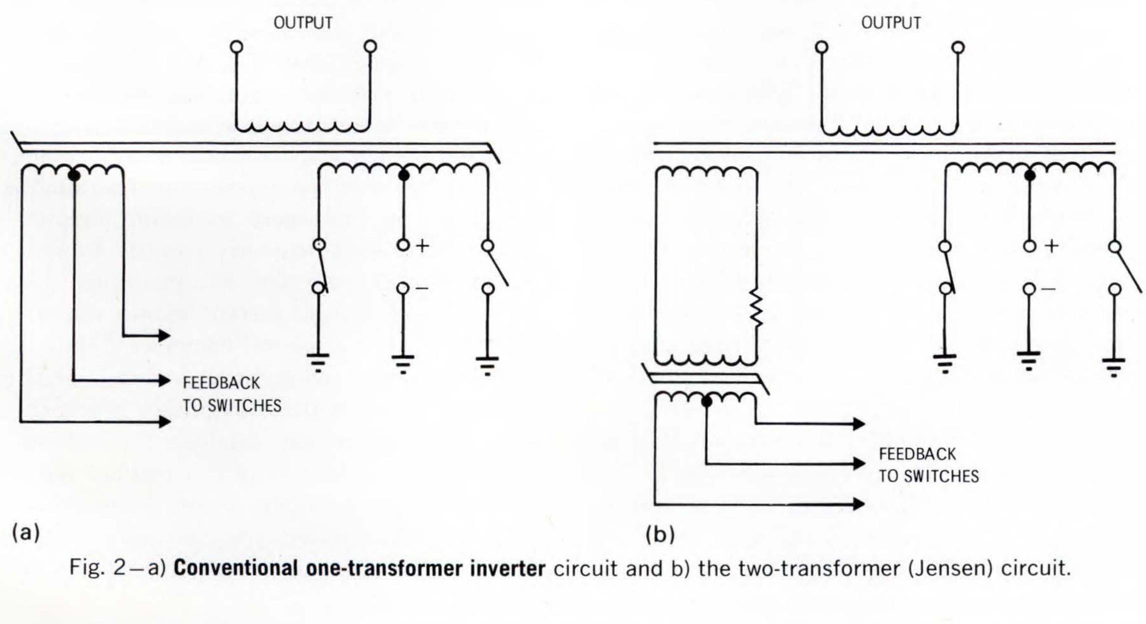


Fig. 2—a) **Conventional one-transformer inverter** circuit and b) the two-transformer (Jensen) circuit.

(Continued)

output into a switching regulator followed by a dc-ac inverter and a step-up transformer. This should be avoided in a helix supply, for equivalent size and weight reduction can often be made in the collector supply with no sacrifice in system performance. Removing the isolation transformer leaves the power line "common" (which is *not* by any means a ground) tied directly to high voltage common (because the dc output must be sensed directly to obtain the regulation usually required of a helix supply). Because the high voltage "common" is connected in the TWT to RF ground, this can put 400 cycle "hum" on the tube, in addition to severe transients. Obviously this is undesirable. The only alternative I have ever become aware of that sidestepped this difficulty was to sense the output with floating sensing circuitry, then use an A/D converter and convey the error information digitally via pulse transformers to the primary side of the step-up transformer. Those familiar with information theory can calculate the theoretical loop gain versus frequency as a function of data rate for this approach, but I do know that data rates well in excess of 1 MHz are required to get moderate regulation of 400-Hz ripple. Another possible technique would be to use analog feedback via a photodiode and a phototransistor. This will have bandwidth and linearity problems.

7) To increase ruggedness and reliability, magnetics should always be considered. The mag-amp and step-up transformer approach results in heavy and bulky components, and generates some RFI, but does have advantages. It is capable of operating at extremely low or high temperatures, and can operate dependably under frequent output short-circuits without power interruption. With two or three stages, reasonably high loop gains are possible. To get around having tens of thousands of turns on the first stage control winding, (using many turns of fine wire offers less reliability than using fewer turns of heavier wire) it would be necessary to allow about 2 to 10 mA of output current for feedback. At very high voltages the power represented by this can be excessive, unless the output power level involved is sufficiently high that this loss becomes insignificant by comparison. Between them, the mag-amp, the step-up transformer, and the high voltage filter, account for a great deal of weight and volume.

Even the size and weight of this heavy, bulky approach may be justified for use as a helix supply. The collector supply, after all, furnishes 70 to 90% of the total dc power requirements, so savings in size and weight can be made there. Further, the magnetic approach is relatively cheap to develop and package.

8) Using SCRs to provide proportional control of the input voltage to a step-up transformer offers a reduction in size, weight, reliability and temperature endurance, and an increase in efficiency and cost over the use of mag-amps. With SCRs, less power is required to sense the output voltage, but considerable active semiconductor circuitry is required instead of a few magnetic amplifiers. This approach is probably preferable over that using mag-amps when the helix supply only furnishes a small portion of the total power. In that case the addition of line filters to minimize RFI from the SCRs is tolerable. Zero-crossing switching can be used to minimize RFI, but getting good regulation requires a high voltage filter with a cutoff frequency on the order of 0.1 to 0.01 Hz, which rapidly becomes impractical.

9) If you consider using a switching regulator/inverter for a collector supply, remember that this supply handles the bulk of the tube's power requirements. If you have chosen this approach, it indicates at least that you are concerned with size and efficiency. How the practical upper power limits are set will now be set forth.

Weight is important, so a fairly high chopping frequency (50 to 150 kHz) should be used to keep down the size and weight of the filter choke and capacitors. Therefore you will require transistors with f_T of at least 15 to 30 MHz. The highest-current transistors in this category are specified for saturation voltage and beta at about 60 to 75A. Experience dictates that such transistors will perform well when derated to 50A. Experience further dictates that with a 28V nominal input, the regulator should not be set for much more than 20 to 22V nominal output. (The regulator should always precede the inverter because inverters are easiest to design and give best performance with a fixed input). We can expect the regulator to deliver about 1 kW to an inverter with an efficiency of at least 90% (if it's much less, something is very wrong).

I have a personal prejudice against paralleling power transistors in high-speed switching circuits. I don't believe that high-frequency current balance can be achieved in any way that will guarantee the transistor's survival. Also, dc current balance requires power-wasting emitter resistors. Therefore, I would use separate regulators and inverters before I would parallel transistors. The multiple regulator approach is practical because you can combine the outputs of two switching regulators in such a manner that the load current is shared equally within a small fraction of a percent. Alternatively, you can use a separate regulator for each inverter, connecting the outputs of the inverters in series.

10) If you are dealing with any application except

Basic Circuit Approach	DC Power Level	Regulation	Comments
HELIX SUPPLIES 28V dc Input			
1) Linear regular, dc-ac inverter, step-up transformer	1 to 100W	0.1% to 0.01%	A practical, easy approach.
2) Switching regulator, dc-ac inverter, step-up transformer	10W to 1 kW	1% to 0.01%	Power levels above 1 kW dc not too practical with 28V dc input.
3) Switching preregulator, linear regulator, dc-ac inverter, step-up transformer	10W to 600W	0.01% to 0.001%	Power levels above 600W not too practical with 28V dc input.
HELIX SUPPLIES 115V/3Φ/400 Hz Input			
4) Step-up transformer, pass-tube regulator	10W up	0.1% to 0.001%	Requires warm up time, less efficient than some solid-state methods.
5) Isolation transformer, switching regulator, dc-ac inverter, step-up transformer	10W to 4000W	1% to 0.01%	One of the better solid-state approaches
6) Full wave diode bridge directly on the ac line (no isolation transformer), switching regulator, dc-ac inverter, step-up transformer	10W to perhaps 10 kW	1% to 0.1%	Gives serious ground-loop problems. Attempt only where weight is critical and no other alternative apparent. Serious problems at high power levels.
7) Magnetic amplifier step-up transformer	10W up	1% to 0.1%	RFI, Size and weight problems
8) SCRs and step-up transformer	10W up	1% to 0.01%	Filter weight and RFI problems. Zero-crossing switching adds more filter problems.
COLLECTOR SUPPLIES 28V dc Input			
9) Switching regulator dc-ac inverter, step-up transformer	10W to 1 kW	1% to 0.01%	(Same as Number 2)
COLLECTOR SUPPLIES 115V/3Φ/400 Hz Input			
10) Step-up transformer, rectifier and filter	10W up	Line	Best bet where line is ±10% and collector need only be held to ±15% of nominal. Reliability far outweighs inverter supplies, weight is somewhat less.
11) No input isolation transformer, switching regulator, dc-ac inverter, step-up transformer	10W to 10 kW	1% to 0.1%	(Same as Number 6)
12) Mag amp and step-up transformer	10W up	1% to 0.01%	A great fraction of the system weight would be used here. Outstanding reliability is the only major advantage. (See also Number 7)
13) SCRs and step-up transformer	10W up	1% to 0.01%	(Same as Number 8)
14) Step-up transformer, pass-tube regulator	10W to 10 kW	0.1% to 0.001%	Great loss of system efficiency in using this approach for a collector supply. (See also Number 4)

Table 2—**Helix and collector supplies.**

(Continued)

doppler ranging or an occasional low-noise communications system, and the tube delivers more than 100W average, the collector will almost always be depressed. Such tubes often can tolerate collector voltage variations of ±15%. If you are lucky enough to have an input line that is regulated within ±10%, then an unregulated collector supply may very well be the best choice. Nothing more than a step-up transformer, rectifier, filter, and bleeder are required. Engineering time and cost are about the lowest, and reliability is about the highest. With good transformer design you can keep the weight comparable to, or lower than, that with any other approach, and the volume will also be among the lowest for any approach.

11) If the collector must be regulated to perhaps 1% or better, and weight is a problem, you can always use the no-isolation-transformer approach that consists of a bridge on the ac line, a switching regulator, and a dc-ac inverter. Power transistors with voltage ratings to 300V, capable of switching 40A are available. A rectified line can supply perhaps 150 to 160V dc loaded. In this approach a regulator should have a nominal output of about 100V dc. Therefore, this approach can provide 4 kW or more with multiple regulators.

Because the ac line common will not be at the same ac potential as RF ground, some ac noise will be coupled through to the collector supply. As an alternate, a dc connection between power common and RF common can be avoided by obtaining the error voltage signal from a floating tertiary winding on the inverter output transformer and compensating for loading variations. Neither approach is recommended for supplies that require ripple or regulation better than 0.1%.

12) If you are primarily concerned with reliability, need fair regulation, have plenty of space available and can tolerate a lot of weight, the magnetic-amplifier step-up transformer approach may be desirable. However, when considered for use as a collector supply handling the bulk of the power in the system, a magnetic frequency multiplier is just as reliable and somewhat less bulky, albeit more expensive.

13) SCRs and a step-up transformer comprise one possible approach to a collector supply. There are two rather serious use problems, however.

First, the nonsinusoidal current waveforms tend to enhance the higher harmonics of most rotary generators at the expense of the fundamental, thus producing RFI. Even if the input contained only the fundamental, the nonsinusoidal current waveforms would still produce RFI. Line filters are electrically and mechanically inefficient at the power levels of the most commonly-encountered collector supplies (1 to 10 kW). I know of no elegant solution. Specific RFI and harmonic distortion levels should be evaluated for each design, and the proper compromises made.

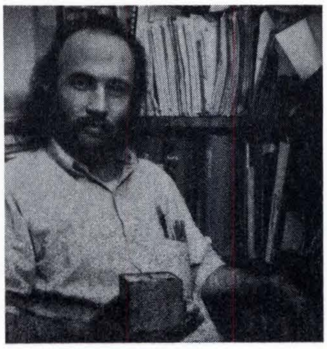
Second, the necessary filter on the high-voltage side of the power transformer must have 30- to 40-dB attenuation at 1200 Hz. This often creates an unanticipated space and weight problem.

On the positive side for this SCR and step-up transformer approach, thermal efficiency will be high. SCRs capable of handling a hundred kilowatt or so are available, and space and weight consumption will be low or moderate. Also, the engineering time required to handle all facets of the design except those relating to the two problems noted previously will be low.

14) The step-up transformer-pass tube regulator approach to a regulated collector supply has many significant advantages. Regulation is excellent. Engineering time is low. Size and weight are moderate. Suitable pass tubes for the particular voltage and current range are not always available, but manufacturers usually can develop a new design or modify an existing one for a reasonable price. Short-circuit immunity is high. Reliability is fair, being mostly dependent on the pass tube.

On the other hand, thermal efficiency is poor. At high power levels, liquid cooling (even though a necessity) becomes a significant space and weight factor, particularly if a heat exchange is involved. Mounting the tubes to meet shock and vibration can also be a problem.

These 14 approaches we have just considered cover most of the conventional design approaches for TWT supplies. A concluding article to be published soon will deal with the factors a systems designer must take into account in choosing the design approach and the building blocks to be used for final design. ▭



Steve Smith is Director of Research for Quatt Wunkery. His duties include development of high performance grid pulse modulators and airborne power conversion modules to handle 200W to 2 kW in a 3-inch cube. He is also a consultant to the aerospace industry. Before joining Quatt Wunkery, Smith was Director of Research for FAM Engineering in Richmond, Calif., and Chief Engineer for Pacific Instrument Company in Oakland. He holds a master's degree in Physics from San Francisco State College.

FOR A FREE REPRINT OF THIS ARTICLE, **CIRCLE NO. L63**

NINE GREAT PLOYS FOR GETTING LEAST FROM ELECTROMECHANICAL COUNTERS

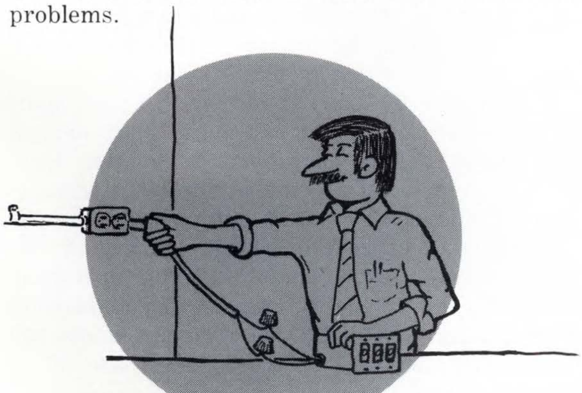
by Eliot Smith

Electromechanical counters have been around a long time—long enough so that almost all their bugs are gone. Yet it's still possible—with a bit of ingenuity and some standard, ready-made specious arguments—to specify them and design with them in ways that are almost certain to assure failure.

Here are a few ploys—along with uncalled-for comments by the spoilsport at the next desk who likes to see things work.

"My operating voltage is close enough to the coil voltage of a standard counter. So I'll use the standard design and avoid the bother, extra cost and delivery delays of a special design."

You might get away with this, but chances are that you're headed for trouble. Counters are designed for a specific ac or dc voltage. If you use too high a voltage, you shorten the life or, maybe, burn out the coil. If you use too low a voltage, you can cause erratic operation or the counter may not operate at all. Generally, your coil voltage should be within 10 percent of the counter's rating to assure no functional problems.



My operating voltage is close enough . . . .

"I know you rate this counter for only 600 counts per minute, but the samples all tested OK at 1000 cpm, so I'll specify this counter for my new high-speed equipment."

This kind of logic invariably leads to future trouble. Most counters are conservatively rated with respect to speed. This allows for normal manufacturing variations and insures that all counters meet minimum specs. It's not uncommon to find 600-cpm counters that can operate intermittently at speeds beyond 1200 cpm. Samples can exceed the spec, but there is no assurance that all units will perform like the samples. You can be certain that if the speed rating could be increased, the counter manufacturer would increase it.

"I've tested this 3000-cpm counter and can't get more than 1800 cpm with it. It's obviously no good."

You often hear that high-speed counters won't go as fast as they should. Often, the problem is pulse timing. Most counters should operate with 50 percent duty cycle. If the voltage and pulse timing are correct, a likely cause of reduced speed is the type of suppression used.

The speed specs for one counter, as an example, are based on a specified dc-voltage input and limited back-spike suppression. But engineers often use diode suppression either for economy or maximum protection of the electronic drive components. Unfortunately, diode suppression slows the decay of stored magnetic energy (which a voltage back spike helps dissipate) and therefore, extends the minimum off-time required. This reduces the counting speed.

Considerations of minimum off time and coil suppression are important in all applications. In high-speed applications these considerations can became primary. In some cases, special coils can be designed to permit high-speed operation with full suppression.

"My special 24-Vdc circuit has 10-ms on and off times. But this 3000-cpm counter won't respond."

Special circuits often mean special pulse

FOR A FREE REPRINT OF THIS ARTICLE, **CIRCLE NO L64** shapes. A capacitor-discharge circuit is ideal for minimizing power drain where counters are used in battery-operated circuits. But here, the pulse shape and duration become important.

If you're going to use anything other than a square wave, it's best to conduct a full test to establish the suitability of counter and circuitry. If circuit changes can't be made, a simple redesign of the counter coil can often result in the desired matching.

"The counters work well on test, but we've had several burn out after we installed them."

Some operating conditions are often overlooked when counters are electrically checked out in the test lab. One example is the black box that develops a temperature of more than 150°F when it's exposed to direct sunlight. Now most commercial counters will operate satisfactorily between 10° and 120°F, though many are designed for operation well beyond these limits. But if you expect extremes in temperature or other environmental conditions, you ought to check with the manufacturer.

"We tapped some holes in the side of this counter so we could mount it on our special adjustable bracket. What could that have to do with the premature failures we're having?"

Just about everything. A counter is, in many respects, a delicate instrument. Foreign particles can cause it to malfunction or fail catastrophically. That's why counters are often totally enclosed to the maximum extent possible.

Adding mounting holes not only provides possible entry for foreign particles but can actually add the damaging particles. Any changes on a counter can affect its operation. Clipping or bending a mounting foot can distort the frame and put critical dimensions out of tolerance. The obvious way around this is to specify the counter with needed modification. Let the manufacturer do it.

We tapped some holes in the side of this counter . . . .

"Even though my count speed is slow, I'm going to specify the more expensive high-speed counter because I need high reliability."

You might think a high-speed counter is necessarily more reliable than a low-speed unit. It ain't necessarily so. A high-speed capability does not mean improved reliability at low speeds. High-speed counters generally do have longer life ratings than low-speed counters. But for the first few million counts at speeds under 600 cpm, a good low-cost counter should be just as reliable as a more expensive, high-speed unit. In fact, because they are more sensitive to short pulses, high-speed counters may overcount if operated from poorly regulated dc supplies.

The point is, speed and reliability don't necessarily go together. Each must be specified individually.

"I checked samples on our test circuit and they worked fine. But they're erratic in production equipment."

There's the problem in a nutshell. If the test circuit doesn't duplicate the production circuit exactly, it's of questionable value. Take the case of a high-speed counter checked out on a recommended test circuit. No problems. In the production circuit, voltage and pulse timing seemed to be the same, but the counter was erratic. The cause? A large solenoid operated in parallel with the counter. Large backspikes from the solenoid swamped the counter coil, causing clapper hangups and undercounting.

"I know these specs aren't exactly what the application requires. But they're what the counter we're using will do, so a new one should be at least as good to be considered."

Here's a case of abusing a Purchasing Department that's committed to getting an economical second source. We should really consider what a counter should do to be satisfactory, rather than what a counter in use can do.

If you take the time to identify all your operating requirements, you can more easily narrow the search for an appropriate counter. Once you've tentatively selected a counter, check its operating requirements. If they differ from your conditions, don't give up yet. It, or your circuit, might be easily modified for optimum operation. But don't ignore the differences either. Carefully matching counters to your requirements can take extra time, but it undoubtedly pays off in the end. ■

Author: Mr. Smith is product manager of electromechanical products at Veeder-Root in Hartford, Conn.

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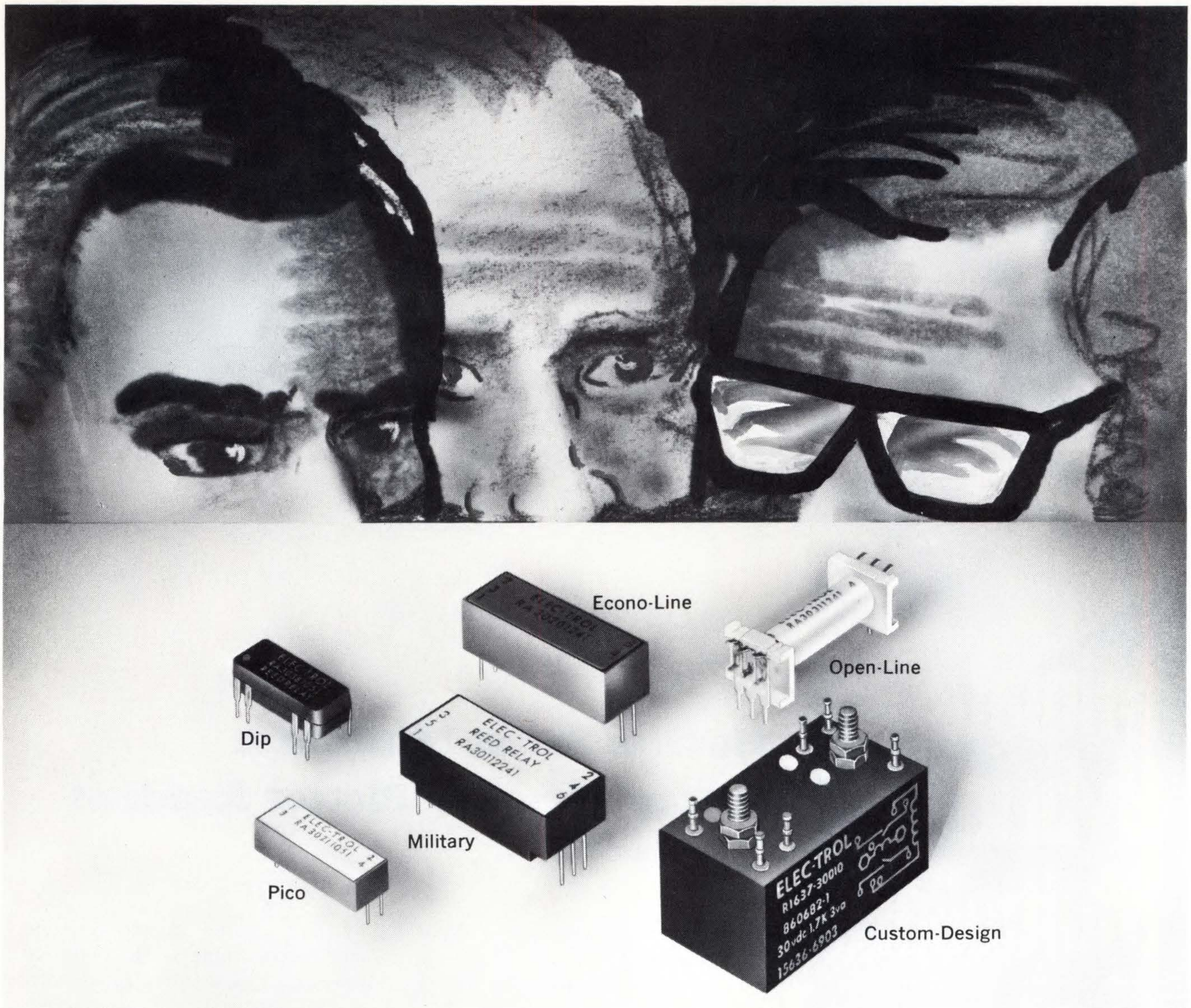

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CIRCLE NO. 17

Measurements File

How to Select Minimum Sweep Time for Plotter Readout

by Bill Mattox

This nomogram presents a rapid and convenient means of determining the optimum total sweep time needed for using an X-Y plotter in spectrum analysis. The nomogram can also be used in automated emi/rfi measurements and other applications that record signal amplitude versus frequency.

Until now there was no convenient method for rapidly determining total sweep time while performing spectrum analysis with a plotter readout. The usual methods of determining sweep time are to reduce the sweep rate until no plotter overshoot is visible and to check steady-state amplitude and frequency measurements against those obtained in the sweep mode. The equation presented here and its nomogram provide a more exact way of determining required sweep time.

Author: Mr. Mattox is radio frequency products manager at Honeywell Test Instruments in Annapolis, Md.

Let's assume a rectangular bandwidth, which is the conservative approach. The bandwidth of the analyzer is assumed to move from f_1 to f_2 in time t. The deflection and slew rate of the plotter govern the time needed to scan the desired portion of the frequency spectrum. Fig. 1 displays the relationship of the various factors. For Fig. 1: t = total time in seconds to scan from f_1 to f_2, $\Delta f = f_2 - f_1$, Δt=time to scan one-half of bandwidth, BW =bandwidth of receiver in Hz and D=desired plotter deflection in inches.

The sweep time is

$$t = \frac{(2D)\ (\Delta f)}{(S)\ (BW)} \qquad (1)$$

However most spectrum-analyzers and sweeping receivers have some nonlinearity of frequency sweep with respect to time. These nonlinearities usually do not exceed a ratio of 2:1. Therefore, the time expressed by Eq. 1. has been arbitrarily doubled to allow sufficient time for the analyzer to

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dwell at a particular frequency regardless of variation in frequency sweep speed. This results in Eq. 2.

$$t = \frac{(4D)\ (\Delta f)}{(S)\ (BW)} \qquad (2)$$

Figure 2 is a nomogram of Eq. 2.

To demonstrate the use of Fig. 2, the following example is provided. Find the optimum scanning time to sweep a 500-kHz band with a 1-kHz bandwidth, using an 8-inch deflection on a plotter having a 30 inch/sec slew rate. The procedure is first to enter the values of Δf(500 kHz) and plotter deflection (8 inches) on the nomogram and connect these entries with a straight line, noting the intersection with the $(4D)\ (\Delta f)$ scale. Then the values of bandwidth and slew rate on the nomogram are connected by a straight line. The intersection with the $(S)(BW)$ line is noted. To solve for t, we drew a straight line connecting the $(4D)(f)$ and $(S)(BW)$ intersections. The resulting intersection on the t scale gives the desired value which is 500 seconds. The calculated value is within 5 percent of the graphical solution.

The nomogram shows that rapid sweep time involves a reduction in plotter deflection and frequency resolution. Typically, if a one-inch deflection is used with the slew rate given above and an analyzer bandwidth of 10 kHz, the sweep time can be reduced to less than 1 second, with a loss of frequency resolution and amplitude.

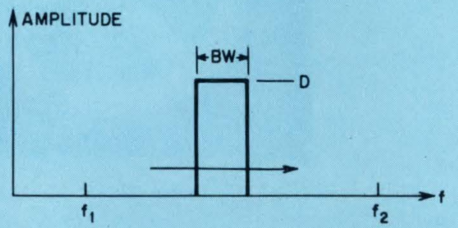

Fig. 1. Sweep time parameters. The dashed line represents the maximum slew rate to reach a deflection (D) in a time (Δt) required to scan half a bandwidth.

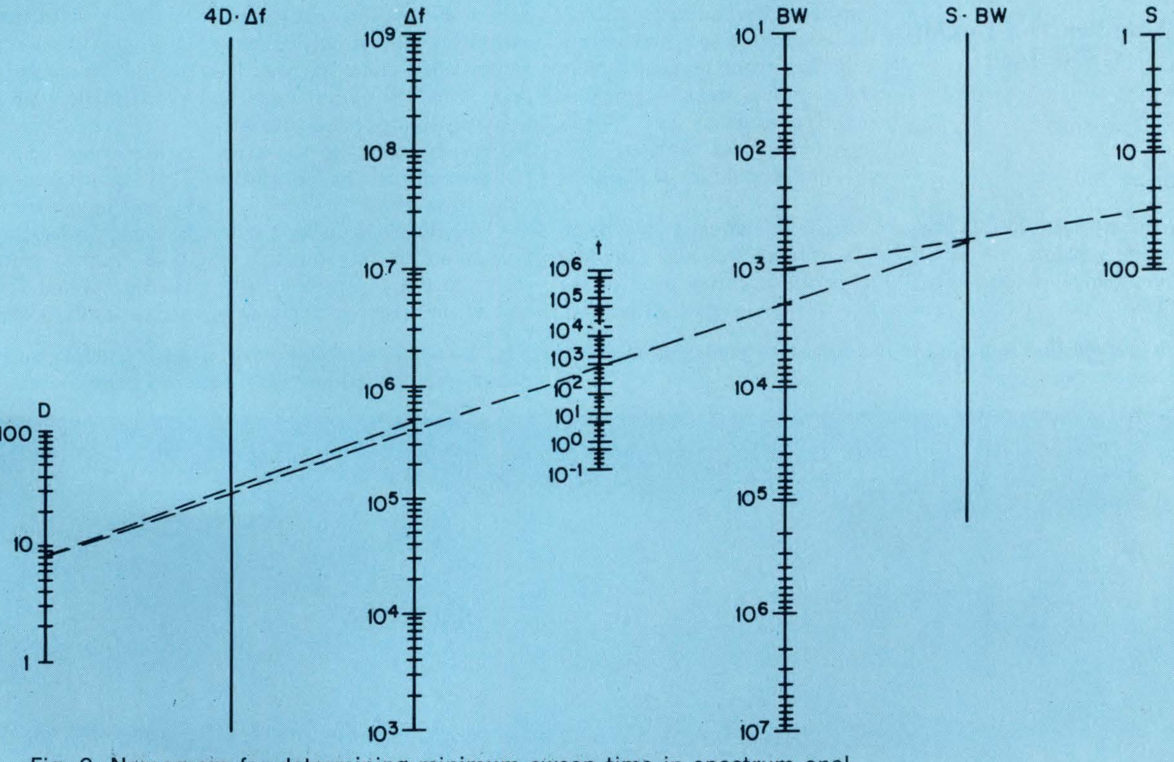

Fig. 2. Nomogram for determining minimum sweep time in spectrum analysis using X-Y plotter readout where: t is (4D)(f)/(S)(BW) in seconds, D is plotter deflection in inches, f is bandwidth to be swept in hertz, BW is analyzer bandwidth in hertz and S is plotter slew rate in inches/seconds.

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An operational approach to sync separation

To Vote For This Circuit Circle 161

by Walter Jung
AAI Corp.
Baltimore, Md.

A useful approach to the video-processing problem of sync separation is shown conceptually in **Fig. 1**. In this circuit, a peak-sensing amplifier automatically biases a control loop to constrain amplifier dynamic range around the negative peaks of sync pulses. The feedback loop follows input bias-level changes, APL changes and hum or baseline ripple.

Diode D_1 charges C_2 to a negative voltage which is forced to track the negative peak of the input video signal. The high gain of the amplifier causes it to saturate at levels only slightly more positive than this negative peak. Thus the output signal is a sharply limited pulse with timing corresponding to the sync-tip portion of the composite video wave-form.

A discrete-component circuit to accomplish this function is shown in **Fig. 2**. Transistors Q_1 and Q_2 form a complementary amplifier with negative feedback applied via CR_1 and C_2. Input video is applied to Q_1 through a 3.58 MHz notch filter (L_t and C_t) to remove color subcarrier components from the waveform. This signal is coupled to Q_1 by C_1, so the level at Q_1's base will be zero. Transistor Q_1 operates as a common-emitter stage for the input signal, turning on with negative going excursions (sync),

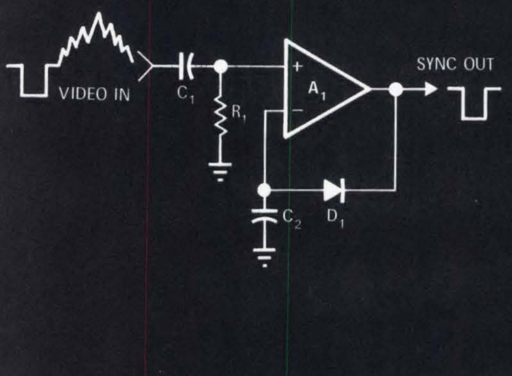


Fig. 1 – Simplified schematic of a negative peak detector for sync separation.

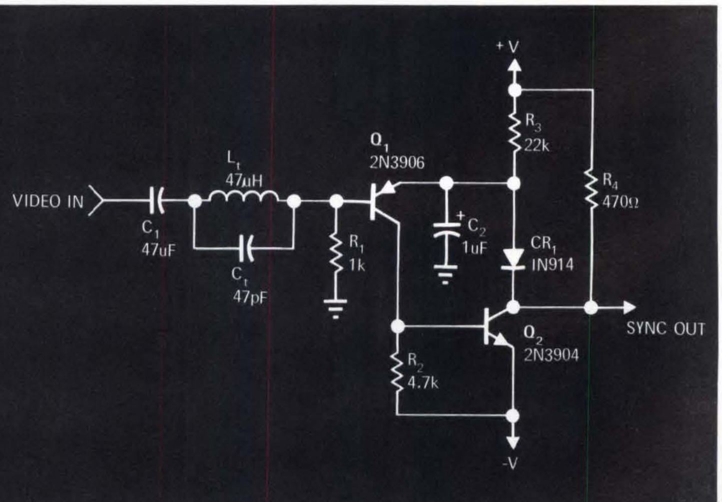


Fig. 2 – Sync removal with negative peak detector. Filter removes color-subcarrier frequency components.

and, in turn, turning on Q_2. When the output signal at Q_2's collector starts going negative, CR_1 conducts, the feedback loop is closed back to Q_1's emitter, and the combination reaches equilibrium.

Since the circuit is set up to conduct only on negative peaks (where Q_1, Q_2 and CR_1 are all on) the feedback is 100 percent at this time, and the negative peaks of the output will follow the input exactly. Capacitor C_2 acts as a memory for negative peaks, storing the level between sync pulses.

As the input signal rises positively from the negative peak, Q_1 turns off because of the charge retained on C_2. This, in turn, switches off Q_2. Diode CR_1 switches off, too, and the collector of Q_2 rises to +V. Though circuit gain is unity for negative peaks, it is extremely high when CR_1 turns off. With the feedback path broken, gain is the product of the gains of the common-emitter stages. Consequently, sync pulses are greatly amplified and sharply limited.

Since the input level rides about the ground and the output tracks this potential, output pulses will have a negative limit close to zero potential. The positive limit is the positive supply line; this can be made +5 volts, and the sync pulses can then directly drive standard logic. The negative supply need only be high enough to keep Q_1 and Q_2 out of saturation and is, otherwise, non-critical. ■

Make-and-break bounceless switching

To Vote For This Circuit Circle 162

By Leo F. Walsh
and Thomas W. Hill
State University of New York
Syracuse, N.Y.

This circuit eliminates switch bounce problems during closing as well as opening. When the switch closes (**Fig. 1**), the Q output from the flip-flop goes to logic-1 state and remains in that state until a period of time after switch release. Turnoff delay is determined by the RC time constant.

When the switch is closed, it immediately causes Q = 1 and $\overline{Q}$ = 0. The $\overline{Q}$ level tries to close the NAND gate but the switch level, although it bounces, holds the NAND gate open and its output remains at logic 0.

Releasing the switch operates the NAND gate causing its output to go to logic 1. This charges capacitor C through resistor R until the reset level is reached. At that time, the flip-flop resets, producing Q = 0 and $\overline{Q}$ = 1. The sequence of operations can be seen by referring to the timing diagram of **Fig. 2**.

Values for components R and C should be chosen according to the bounce duration of the switch used. For a typical spst switch with 1A contact rating, values of R = 10,000 and C = 0.47 μF have proved satisfactory. ■

Fig. 1 – Switch bounce eliminator circuit.

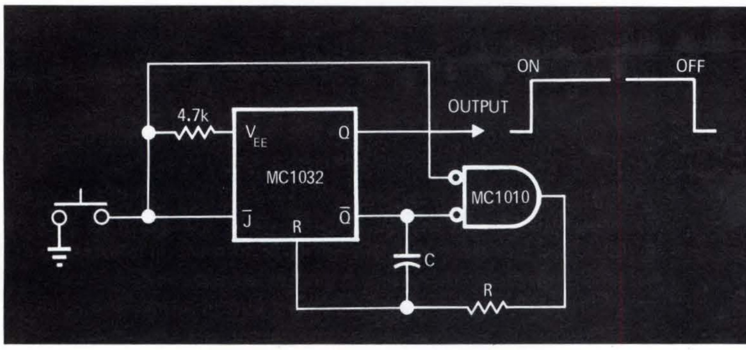
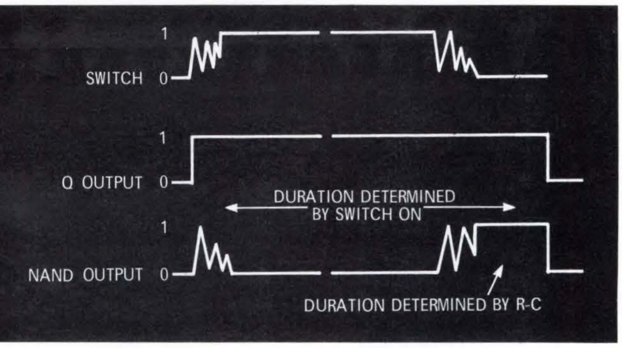


Fig. 2 – Output waveform is free of switch bounce.

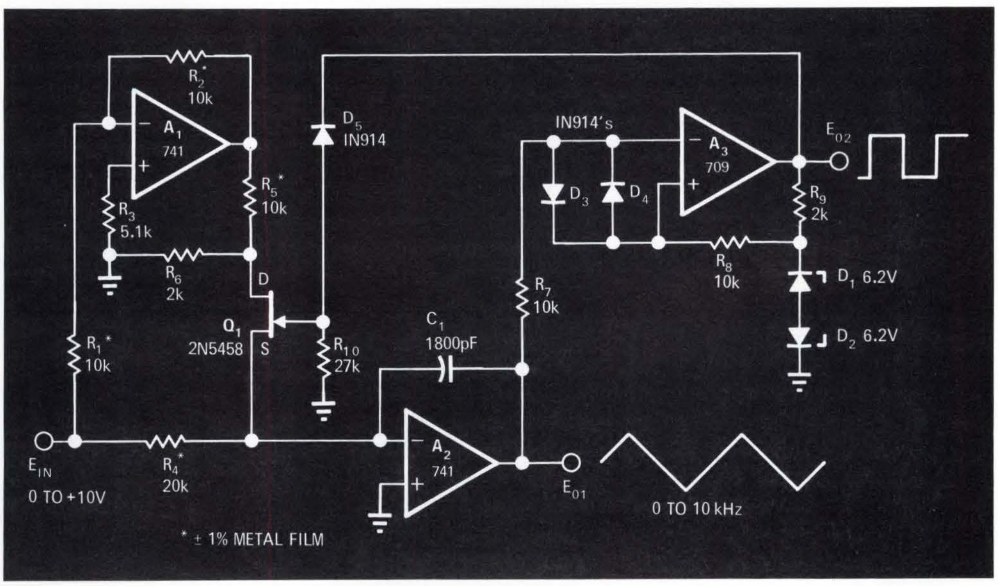


A wideband, linear VCO

To Vote For This Circuit Circle 163

by Gil Bank
Westinghouse Ocean Research
San Diego, Calif.

A voltage-controlled oscillator should have good stability, excellent linearity and a wide range of operation. In addition, a sinusoidal output is frequently desired. This circuit does not have a sine-wave output, but its triangular waveform has only about one third as much third harmonic as a square wave of the same fundamental frequency. This factor makes it relatively easy to convert the



Three IC op amps and a junction FET form a VCO with a 100:1 range and ±0.5% linearity.

triangular wave to a sine wave by filtering.

In the circuit, A1 inverts the positive input signal while Q1 serves as a switch to select the direction of integration. Amplifier A2, with feedback capacitor C1, forms an integrator. Op amp A3, a 709, is used as a comparator. Zener diodes D1 and D2 produce a plus or minus reference voltage with which the output of the integrator is compared.

To follow the circuit through one cycle of operation, neglect R6 and assume Q1 is OFF, which means the output of A3 is negative. The input signal, which must be positive, forces a current through R4 into the summing junction of the integrator, A2, whose output starts slewing negatively at a rate proportional to E_{in}. When the output of A2 reaches approximately −7V, the comparator output goes positive. This action switches Q1 ON, changes the reference voltage of the comparator from −7 to +7V and locks the comparator into a positive output state.

With Q1 ON, a negative current is drawn through R5 that is double the current supplied through R4. The net current to the integrator is equal but opposite to the previous integration current. The integrator output voltage now slews in a positive direction and rises toward +7V. At a 7V input, the comparator output is driven negative which turns Q1 OFF and causes the cycle to repeat.

Resistor R6 attenuates the drain voltage of Q1 so that it will remain completely off (during the appropriate half cycle) for high input voltages. R6 does not affect the magnitude of current injected into the summing junction of A2. Resistors (R7 and R8) and diodes (D3 and D4) are used to prevent latch-up during turn-on transients.

For the values shown and a +15V power supply, the circuit transfer function will be about 1 kHz/V. The circuit will easily operate over a 100:1 frequency range with a linearity error of less than ±0.5%. ■

Circuit Design Entry Blank

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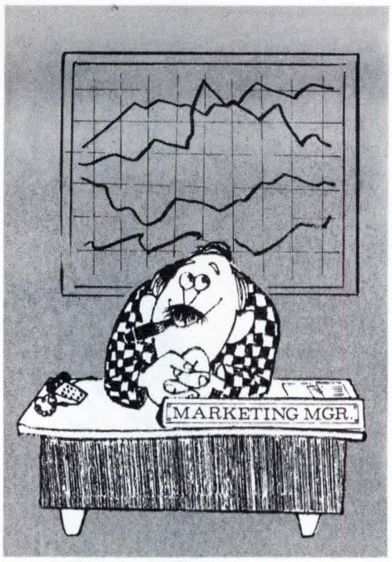
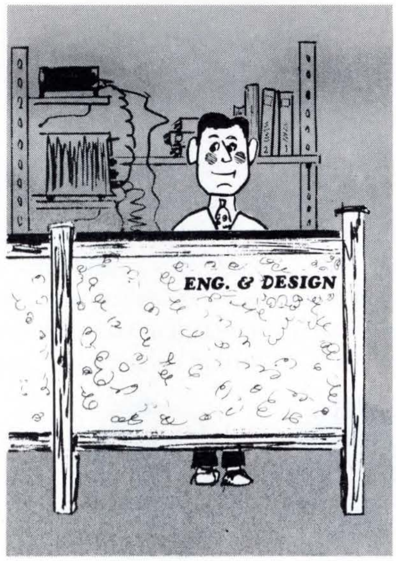




Market Research and Design Can Be Compatible

Engineering and marketing departments are often at odds with each other through lack of mutual understanding. A close look at marketing research can help break down this barrier.

PETER M. ENGSTROM, Pitney-Bowes Fluidic Controls

Doesn't that blankety-blank marketing department ever know what it's doing? How come engineering can't build what we need? Do these and similar statements sound familiar to you? Well, all too often engineering and market researchers go their separate ways without ever getting to meet the other, let alone consult with each other. This attitude can cost a company lots of money and wasted opportunities and is often the cause of product failures in the marketplace. An understanding of just what market research is and how it fits into the overall picture should help clear the air.

What is Market Research?

The American Marketing Association considers marketing research to be "the systematic gathering, recording, and analyzing of data about problems relating to the marketing of goods and services." More broadly speaking, marketing research may be defined as the systematic collection of information for the purpose of enlightened decision making. Marketing research is not an element in the marketing mix such as price structure, product quality, advertising, etc., rather, it is a tool used for the purpose of making decisions about the elements of the marketing mix.

To better understand the concept of marketing research, it helps to take a brief look at its earliest beginnings. Prior to World War II a seller's market existed. The ability to mass-produce goods at steadily declining unit costs as output increased promised profits too attractive to overlook. All effort focused on production, with marketing receiving little attention. Mass production generated great pressures to "move" the product, thus "selling" was emphasized, not marketing.

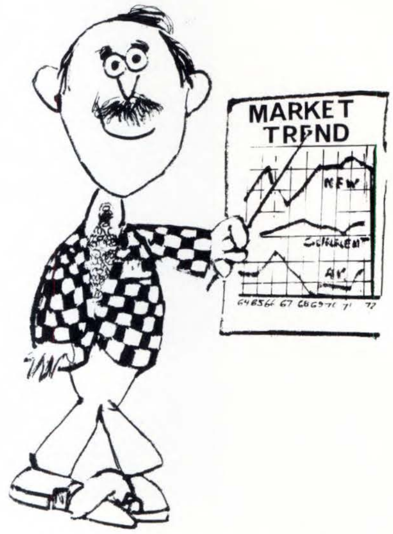
"The difference between selling and marketing is more than semantic," states Theodore Leavitt in the

(Continued)

Harvard Business Review. "Selling focuses on the needs of the seller; marketing on the needs of the buyer. Selling is preoccupied with the seller's need to convert his product into cash; marketing with the idea of satisfying the needs of the customer by means of the product and the whole cluster of things associated with creating, delivering, and finally consuming it."

Rapidly advancing technology in the post-war years has resulted in increased competition and shortened product life cycles. Thus to remain competitive, man-

agement thinking and policy formulation has had to focus on the customer, and information related to customer needs and wants has become an essential basis for management decisions. Under this concept, management's task is to direct the firm's operations toward the product and service requirements of the customer by first learning what his needs are and then determining whether and how the company is able to provide a commodity that can contribute to the customer's satisfaction. What the engineer can do in this light was discussed in EDN, Jan. 15, 1971, "Adaptible



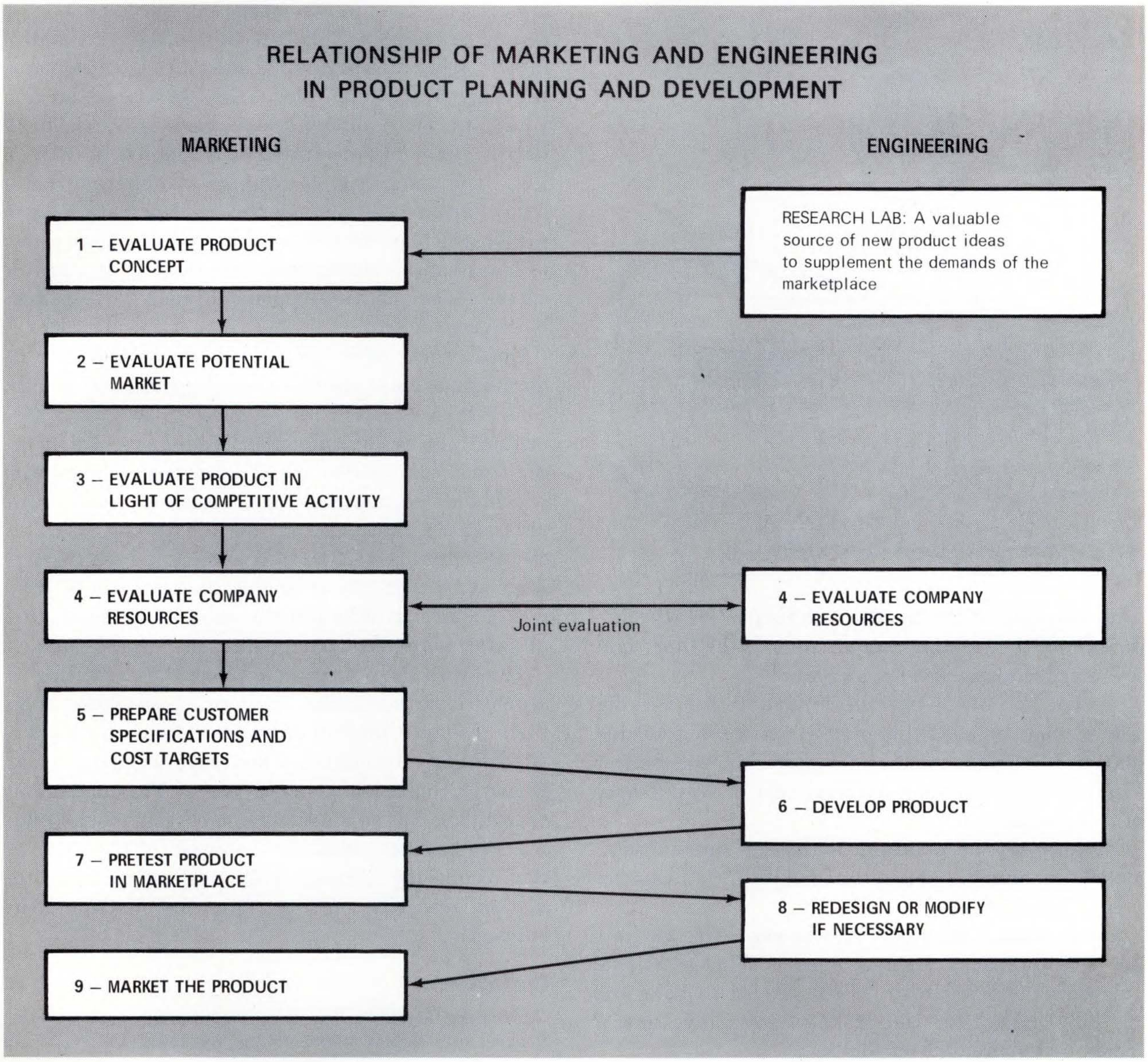
Engineers Will Survive". Marketing research is intended to provide a basis for management decisions related to both potential new activities such as new products or new market areas which offer opportunities for improvement in overall performance, and current activities such as examining and resolving discrepancies between the actual performance and objectives.

In the accomplishment of these ends marketing research may be grouped into four major categories: (1) product research, (2) market research, (3) sales research, and (4) advertising research. *Product research* includes the study of the acceptability of new products, consumer reaction to present products, the study of competitors' lines from both a technical and price standpoint, and product testing. *Market research* relates to facts about the market including size, location, characteristics, and company market share. *Sales research* is utilized to determine sales territories, allocation of sales personnel, compensation programs for salesmen, development of equitable sales quotas, and

WHAT IS MARKETING RESEARCH?

MARKETING RESEARCH; **The systematic collection of information for the purpose of decision making.**

1 – PRODUCT RESEARCH	2 – MARKET RESEARCH	3 – SALES RESEARCH	4 – ADVERTISING RESEARCH
a – New product development	a – Size of market	a – Develop sales territories	a – Select proper media
b – Acceptance of present products	b – Location of market	b – Select channels of distribution	b – Select desirable copy approach
c – Competitive products	c – Market share	c – Allocate sales personnel	c – Determine buying influences
d – Product testing	d – Market characteristics		



for evaluating and selecting appropriate channels of distribution. *Advertising research* concerns itself with media analysis, advertising effectiveness, motivation research and copy research. Of these areas, product research is most closely related to the design engineer, for indeed in many firms it was once largely a function of the engineering department and still is in many companies. Let us take a closer look at this area of marketing research and how it relates to the design engineer in particular.

Product Planning

To remain competitive, manufacturers must frequently adapt or modify their product line to fit their customers' needs, and to be effective, each change must be based on sound information about what the customer requires. Product planning and development is designed to reduce the risk of failure in the marketplace and to avoid the enormous costs associated with such a venture.

Product planning frequently involves anticipation of changing customer product requirements with a carefully planned technical development program. This requires a close dialogue between engineering and marketing. For example, the following steps are not uncommon in the development of a new product:

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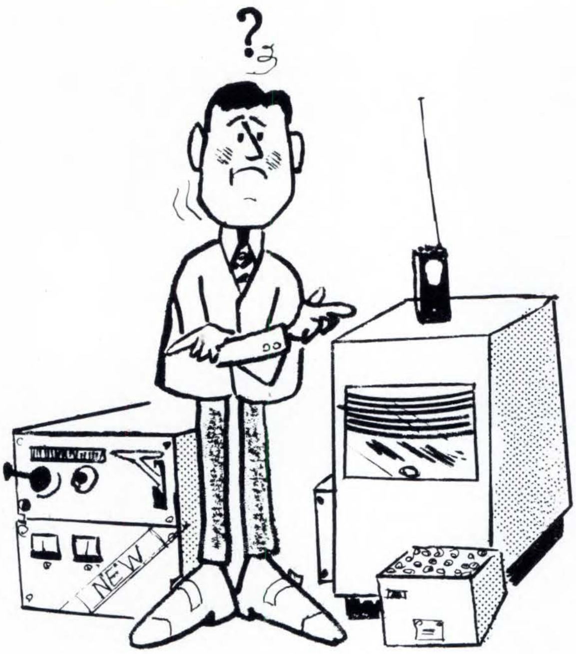


Evaluation of the product concept: Does the product fit in the existing product line? Is the time right for introduction of this product now?

Evaluation of the potential market: Does the consumer want or need this product? Is the market big enough to warrant the investment in time and money? What features influence the consumer in the purchase of this product?

Evaluating the product: Is the new product sufficiently superior to competitive products? Can we offer it at a lower price?

Evaluating Company Resources: Are we in a position to produce the new product? What additional equipment or manpower will be needed to make and market it? How long will it take to recoup investment? Where is the break-even point?

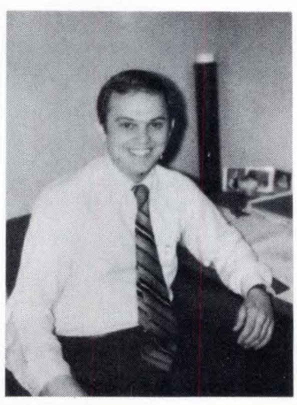
Preparing Customer Specifications: If preliminary evaluation is favorable, what then is it the consumer would like in a product of this kind? What would the consumer not like? What should the product do to meet customer specifications? This is one place in particular where designers and market researchers should work closely together. The engineer should be able to advise the researcher whether certain specs will be so costly to provide that they will defeat other marketing values. The answers to these and other questions reduce the risk attached to the introduction of new products and enable the planning of long-range programs and prevent many false engineering starts. With this information, the engineering department can develop a product which meets marketing specifications as closely as possible. This tack allows specific development targets to replace such generalized developmental research goals as "to advance the state-of-the-art", which are more appropriate to basic research. It allows a rifle to be substituted for a shotgun in R&D efforts, and the payoff is increased results and lower costs. Further, it eliminates the development of a product for which no market exists and reduces the number of opportunities which may be foregone because the company does not have a product to meet the new needs of its customers.

Once armed with the appropriate information regarding customer specifications, cost targets, and the competitive situation in the marketplace, the design engineer can manipulate product designs to satisfy the multitude of requirements. Among the variables over which the designer may have some degree of control are product quality, size, styling and packaging. Where strong patent protection is expected, the investment of large sums of money in product research can be justified and product differentiation can be maximized, thus allowing more freedom in pricing, and larger profits.

Thus with the proper inputs from the marketing research department, the engineering staff can apply their technical know-how to the creation of products which satisfy the needs and desires in the marketplace. However, this is not a one-way street. The engineering department can be a valuable marketing tool by keeping the market researcher abreast of the state of the technology. Armed with this information, the market researcher can perform his function more efficiently. ▭

Databank

"Marketing Myopia", Theodore Leavitt, *Harvard Business Review*, July-August, 1960, Vol. 38, pp. 45-56.



Peter M. Engstrom is an applications engineer in the marketing department at Pitney-Bowes Incorporated. His responsibilities include identification of potential market segments, new product evaluations and sales promotion. Peter earned his B.S.M.E. from Polytechnic Institute of Brooklyn, his M.S.M.E. from Purdue, and expects his M.B.A. from the University of Connecticut in January 1972.

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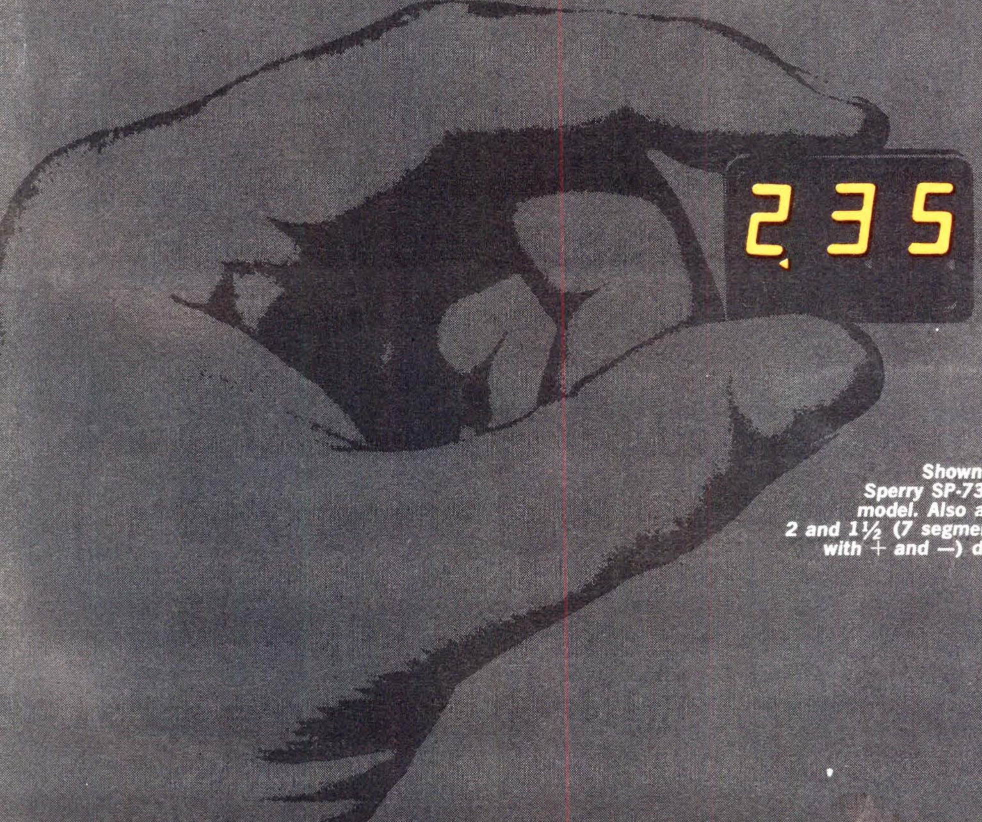

Shown here is the Sperry SP-733, a 3 digit model. Also available are 2 and 1½ (7 segment character with + and —) digit models.

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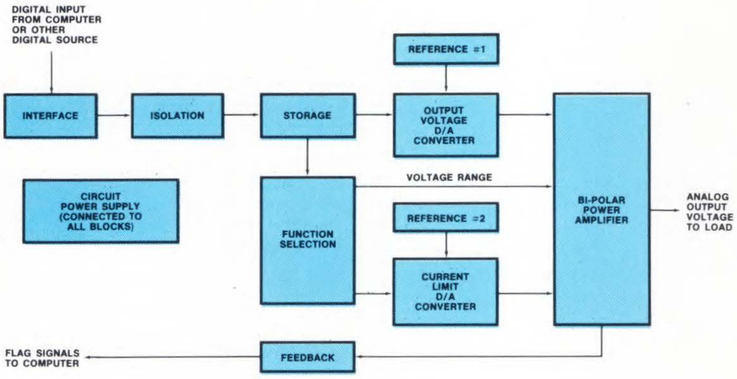

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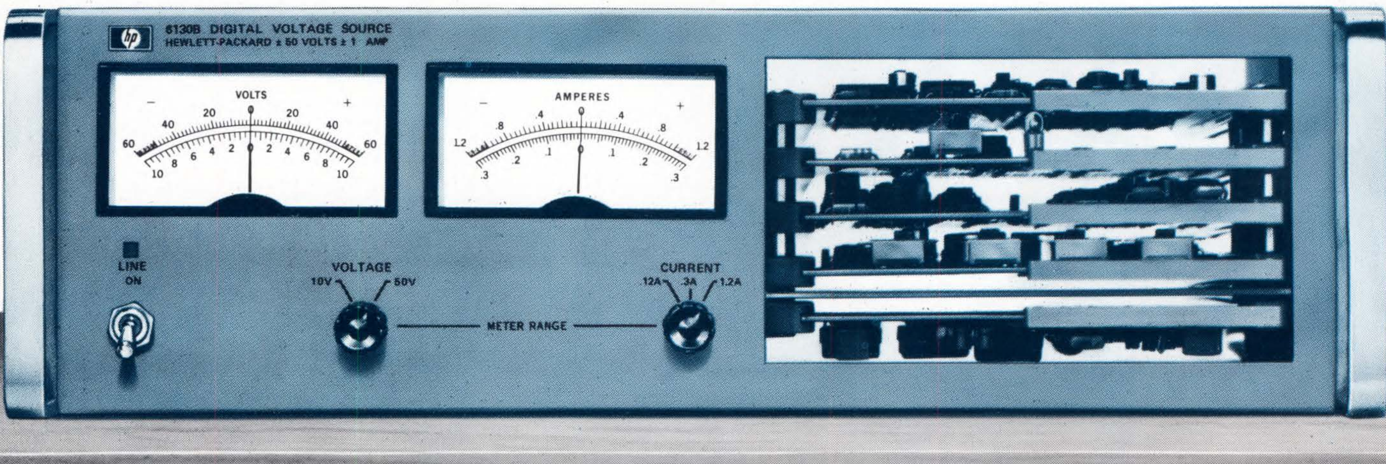

computer hardware

FOR DESIGNERS OF COMPUTER MAINFRAMES, PERIPHERALS AND SYSTEMS

Designing Core Memories Efficiently

A CAHNERS PUBLICATION / JULY 15, 1971

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SIGNAL SOURCES

CIRCLE NO. 402

JULY 15, 1971

computer hardware

EXCLUSIVELY FOR DESIGNERS OF COMPUTER MAINFRAMES, PERIPHERALS AND SYSTEMS

cover

Cover photo by Ray Lewis, EDN/EEE art director, presents an abstract form of the topic "core memories". See article on p. CH 8.

directions

features

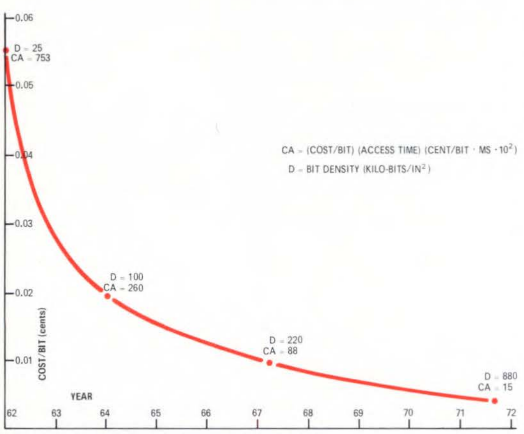
events

"perpetual improvement" regulates memory designs—

The law of "perpetual improvement" has been added to the laws describing "how it happens" in the computer world. The law, conceived by Irving L. Wieselman, vice president of Product Programs at Data Products Corp., is based on the following observations on the analysis of price/performance trends and the changing roles of peripherals.

Consider the memory problem. A basic storage law states that *the cost/bit is inversely proportional to access time.* This is true within a given technology and between technologies. The system designer must select his storage so that the desired capacity is available at a price consistent with the system's usefulness.

Now consider the spectrum of storage devices, with access times ranging from 100 nsec to minutes and costs varying from $0.25 to $0.001/bit. Because of the wide cost range, many designers solve their particular needs by using a set of hierarchy of storage devices with different access times such that the slower and less expensive device handles the larger storage requirements. For example, consider a system requiring 2 billion bits. Assume the price for a main frame core storage to be $0.10/bit with an access time of 1 μsec/word. Thus, the total cost is $200 million for a complete core memory. If a disc file at a cost of $0.01/bit and an access time of 100 msec is used, the cost becomes $200,000. To keep the cost within limits, a storage hierarchy is used where the bulk storage is disc and only a small portion is core.



EFFECT OF TECHNOLOGY ON IBM DISC FILE PRICING

There has been an increase in performance as well as a decrease in cost/bit for disc file systems. A prime measure of performance for a disc file is access time. As a result, a figure of merit, **CA**, is defined as the product of the cost/bit and the access time. Decreasing either the cost/bit, the access time, or both will lower the **CA**. Lower the **CA**, better the storage device.

In order to illustrate the rapid growth of technology and its effect on price/performance, examine the graph. The data represents the disc file products produced by IBM over the last decade, using disc prices excluding the control units. The curve shows the cost/bit decrease as a function of chronological time, indicating a factor of 10 reduction in cost. Increase in recording density with time represents the growth technology and the decrease of **CA** indicates the improvement in price/performance.

Technology changes cannot only alter the mix of peripherals, but can even eliminate certain types. Consider the situation regarding magnetic-card random-access devices such as the IBM 2321 Data Cell. Many systems use this unit as the bulk storage because of low cost (approximately 1/3 the cost of disc storage). However, it is about six times slower. With the introduction of the IBM 3330, system configurations for bulk storage should change. It is close to the cost of the 2321 (20% higher), but is more than 10 times faster and more reliable.

Cost/bit for main frame memories has changed at about the same rate as the disc files. Reduction in cost/bit is mainly dictated by component and manufacturing technique improvements. As the cost/bit decreases, the maximum size of core memories grow. In today's core technology, 500 nsec is the practical speed limit. The emergence of solid-state memories in the 100- to 500-nsec region and with costs comparable to core means that some core main frame memories will be replaced with semiconductor devices. This does not mean, however, that core memories are obsolete. It means that core memories will play a different role in the memory spectrum.

directions

Computer architecture, of course, shifts to take advantage of peripheral changes to improve the price/performance characteristics. The impact among peripherals yields an interesting phenomenon that could be labeled "perpetual improvement". As new peripherals emerge they do not replace the old types because, in the same time span, the old ones are being improved. Thus instead of new peripherals obsoleting old ones, we see a "perpetual improvement" in which the whole technology front seems to be moving forward. Because of this effect, the designer's expectation of a market displacement with a new peripheral turns out instead to be a market modification.

coding standards needed for POS terminals—

Competition is stiffening in the potentially lucrative market for retail point-of-sales (POS) terminals—data terminals which replace conventional cash registers and simultaneously form part of an integrated management information system for a department store. About 10 hardware companies are currently competing for larger shares of this market, and the winners will be those companies that are able to offer more labor-saving

(Continued)

standards (Cont'd)

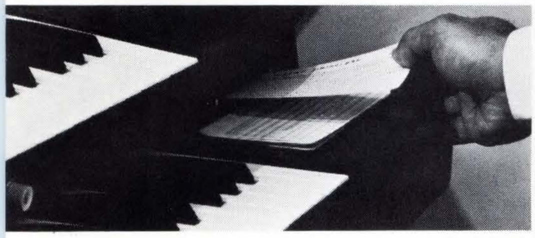
features at lower costs than the competition.

Several manufacturers have achieved cost economies by replacing conventional ICs or discrete-component circuitry with MOS LSI. But the trend towards increased automation in department stores has been stymied by a lack of universal coding standards for credit cards and merchandise tags. Thus, many desirable features – such as provision for automatic entry of customer and merchandise data – are not included in the majority of today's POS terminals, even though these features are technically feasible.

A case in point is a new POS terminal recently introduced by the Uni-Tote Div. General Instrument Corp. This company was one of the first to introduce an electronic cash register, and the new machine, series 300, offers many features that have been included as a result of Uni-Tote's experience in the field. For example, like some other POS terminals, the series 300 has lighted-key signals that guide an operator through transactions, thus minimizing errors and speeding operation and learning time. But the new machine doesn't have a built-in tag reader or card reader. Spokesmen for Uni-Tote say that the series 300 can be interfaced with external tag readers, and the company is currently evaluating several different types of readers with a view to incorporating one of them inside a terminal eventually.

There is hope, though, that some coding standards for merchandise tags will be established soon. The National Retail Merchants Assoc. has task groups working on proposed standards for tag marking and for credit-card specifications. In the credit-card area, however, multiple standards may emerge because various industries – such as banking, air transport and retailing – are all evaluating the problems from different viewpoints.

digital computer controls organ sound—



If Bach were alive today, he might be using an organ with a built-in digital computer. His reasons for doing so could be either aesthetic or economic, because a new line of electronic organs, recently introduced by Allen Organ Company, are said to reproduce the authentic sounds of a quality pipe organ—but at a fraction of the cost.

The unusual new musical instrument was the brainchild of North American Rockwell scientist Ralph Deutsch, who has been granted a U.S. patent for his "Digital Organ." Engineers from NR and Allen Organ worked together to develop a commercial version with the necessary quality and price for the discriminating musical world. Though digital processing requires more circuitry than conventional analog techniques, the engineers were able to meet their cost goals by extensive use of MOS LSI. The organ's musically-dedicated minicomputer contains a total of 22 MOS circuits which perform the equivalent functions of around 2000 conventional ICs or 48,000 discrete transistors.

The purpose of the built-in computer in the new organ design is not to automate organ playing, but, rather, to offer the organist a greater range of sounds to choose from. In addition to the conventional selection of predetermined stops or voices (different tonal qualities) the digital organ can be reprogrammed to produce an almost infinite range of alternative sounds merely by feeding in suitable punched cards.

end of another era—

The end of pencil and pen-pushing where large masses of data are concerned has been forecast by Bunker-Ramo Corp.'s Electronic Systems Division in Westlake, Calif. They made the prediction in reporting application studies for the BR-700 information storage and retrieval system.

Hal Kirsch, Product Marketing Director, pointed out that most data ends up in digital form eventually these days, for storage or handling by computers. "But to get the information into digital form sometimes requires six to eight different persons. Someone writes the original information. Someone else copies it. Someone keypunches it. Someone reviews the keypunching, and perhaps has it repunched to correct errors. And eventually it gets into the computer." Biggest problems with all those steps, Kirsch said, are the large numbers of errors that creep in—as well as the high cost of all the people involved.

In the near future, Kirsch said, the person who originates the information likely will type it directly into an information retrieval system, and then verify it himself. Then it can become permanent information if desired, or with an off-line system it can be called up for review, edited if necessary, returned to temporary storage, eliminated or fed onto a main computer.

"Overspecifying a core memory system is a common and serious problem," states Robert K. Lowry, Vice President of Technology Marketing, Inc. In most cases the engineer is either trying to build in a tolerance or attempting to standardize his unit. But he is going about it the wrong way.... An engineer not only fails to create the extra allowance he is seeking or the design consistency he has in mind, but he complicates the system and increases manufacturing and operating costs. Mr. Lowry explains that well-intentioned errors are generally associated with one or more of four categories: *capacity, speed, temperature and core requirements.* Since volume users let contracts for large numbers of identical systems, even minor cost increments can result in substantial dollar losses later on.

The ensuing discussion of the categories is aimed at commercial uses where the factors are essentially independent of the application (military and space applications are a separate subject) and design goals are cost/performance oriented. As the memory is the highest cost assembly in a computer, those functional needs that can be accommodated by the least expensive, most reliable memory should prevail.

over-specifying core memories can be costly

Memory Capacity The customer's marketing strategy usually dictates the memory capacity. For example, minicomputer manufacturers normally select 4096 words as the basic module. This permits them to advertise a low-cost memory system and provides the superficial convenience of using 4k blocks to assemble 8k, 12k and 16k capacities.

Expanding the total system capacity by plugging in several like modules sounds logical, but it overlooks a basic fact. Most minicomputers available on the current market contain a minimum of 8k storage, and stacking two 4k modules costs more than a single 8k block.

Although the number of cores in an 8k block is double that of a 4k module, there is only one printed circuit board. Electronics accounts for about 30% of the manufactured cost of a 4k block, and the sense and inhibit circuits are identical to those in the 8k version. The number of decoding diodes increases with capacity, but not in direct proportion—a small cost advantage. The additional eight sink switches needed in the typical 8k module add no more than $10 to the cost. By the time the labor to handle additional units and miscellaneous extras are considered, the dollars and cents improvement of an 8k block over two 4k blocks becomes apparent for volume production.

Looking at the other side of the problem, modern design practice can achieve an economical 4k system by substituting a depopulated lower capacity stack in an 8k module. For lowest cost, this stack is a planar array that plugs directly into the electronic motherboard. New techniques permit the electronics to be packaged on a single card, only slightly larger than the stack itself.

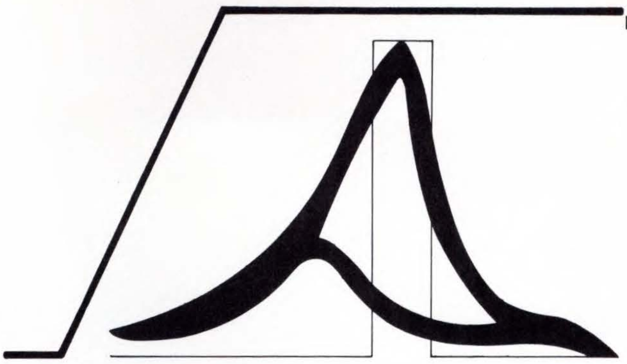
A typical circuitry technique reduces the number of driver switches by 50% in a 3-wire, 3-D organization. The advent of MSI (medium scale integration) components has helped to reduce the size of the electronics package. Items unavailable to designers two or three years ago but that may now be obtained from several manufacturers are:

—Four pulse transformers in a dual in-line package.
—Quad transistors in a dual in-line package.
—A single chip with an eight-bit parity checker.
—A one-of-eight decoder driver that drives a transtransformer directly.

An inexpensive approach to a memory system employs a custom-designed basic module of the most popular capacity. Smaller capacities are realized through a reduction in stack size. Mixing modules containing various stack sizes yields larger capacities. Added savings in inventory, spares stocking and field expansion are a happy consequence.

If a manufacturer needs to advertise a 4k module to meet competition, he must be free to do so. But he should retain the flexibility to save himself and his customer money when he can.

By going to a custom memory in the first place, the manufacturer acknowledges the inherent savings over standard black boxes for large volume production. Units designed for the general market must contain features suitable for a variety of applications. The buyer pays for all of them whether or not they are needed. It is inconsistent to obtain economies by customizing the memory system and then surrendering part of the savings by insisting that the custom unit be rigidly standardized to match an advertising ploy.



Speed The relationship of speed to memory design is often misinterpreted. Engineers seeking operating margins many times specify a higher speed than they actually need. Negative implications of such a tactic are far-reaching.

Maximum margins are attained by increasing pulse widths. Under such conditions, reasonable timing tolerances have no effect on the operating limits of the system. Pushing for speed shrinks allowable tolerances on pulse widths. Continued pursuit of this course ultimately reaches the point where components must be matched and selected to set the pulse widths. Trouble shooting and parts replacement become difficult—at times almost arbitrary.

Larger timing tolerances permit standard components to be employed. The current setting resistor is the only item that may be hand selected. Trouble shooting is then reduced to routine selection and replacement of malfunctioning parts.

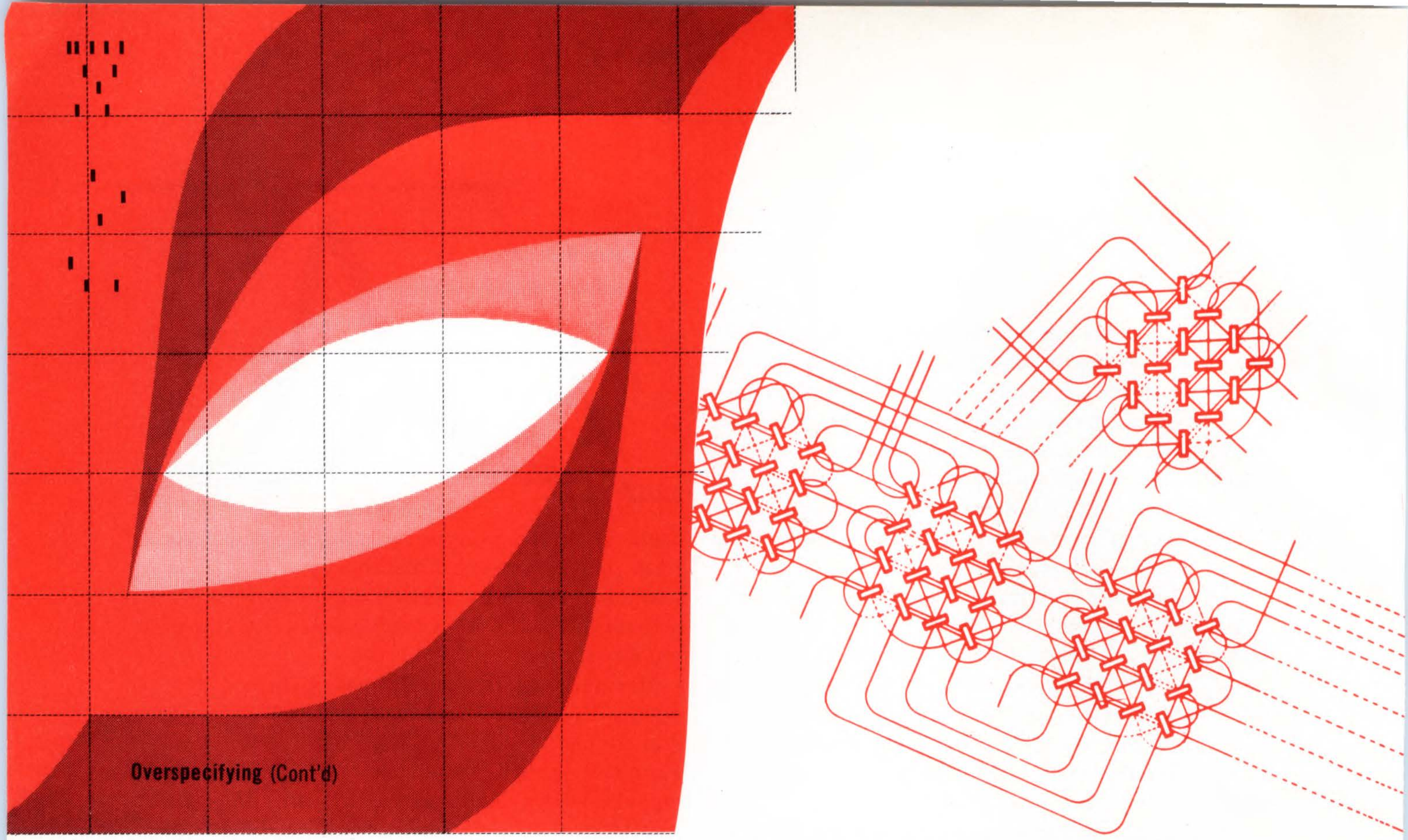
Speed also affects power—a factor often forgotten when an engineer specifies 1.0 μsec but intends to operate at 1.5 or 2.0 μsec. For instance, the inhibit drivers may require 5V in a small 2-μsec design. Designed for 1 μsec but used at 2 μsec, the same system would demand 12V—a power increase of 2.4 times (current remains unchanged). Heat dissipation and reliability problems naturally increase.

Interestingly, core switching times are often not a major factor in system cycling speeds. Various generations of cores are available to the designer, and frequently a superior and faster memory can be achieved using one of the slower cores.

Optimum system speed represents a trade-off of bits/μsec/W. To attain maximum speed with minimum power, core speed and drive current are balanced to the application.

Take, for example, an application using a low-drive core that switches a little slower. The rate of current change is a constant, so with the lower drive requirement, rise times are effectively faster. The result is a memory system with an overall cycle time just as good as if a faster switching core and higher drive current were used—and with better efficiency.

(Continued)



Overspecifying (Cont'd)

Temperature Electrical components limit the operating temperatures, not the core array. Operating temperature range for a typical EDP environment is 0 to 50°C, and these limits can be extended to −10 and 70°C with little cost penalty. But high-temperature requirements increase costs significantly. For example, specially insulated core wire requires chemical stripping. Special capacitors and other nonstandard components are necessary. Few applications call for continuous operation at high temperatures and every effort should be made to hold the specification within the normal range.

Cooling methods are another factor in temperature control. Speeds slower than 2 μsec usually permit convection cooling. Faster speeds require forced air. If forced air is used, the direction of flow becomes important, and where a choice exists, boards should be mounted vertically. This promotes heat dissipation and more efficient cooling.

The understandable urge to economize by using an existing inventory of power supplies may also contribute to the temperature problem. When available voltages exceed those required by the memory system, the wasted power is converted into heat. The power loss increases operating costs and the cooling system may have to be enlarged to accommodate the additional load.

Recent core developments also assist in this area by permitting increased packing density on the board. One example is a new 18-mil core that requires 440 mA for full drive, an almost 50% power reduction over conventional cores of the same size.

Cores and Core Arrays Continuous wired planar arrays are the easiest to build. A simple stack interconnect system may be employed to plug the arrays into the motherboard. Multi-element, double-sided and folded arrays are more complex and generally result in a more expensive system. They belong to the age of the dinosaur if factors other than vibration or minimum package volume are important.

Of course, putting an 8k memory in an 8-inch cube requires some unusual techniques. But in the long run, it may be wiser to design a larger box.

Heat becomes a major problem with complicated arrays in small areas. Even in spacious accommodations there are more small boards, significantly more connectors and more backplane wiring with its attendant problems. The count of interconnect pins goes up and reliability drops proportionately. Complex configurations often require extra testing. For instance, a folded array should be tested both before and after closure. It just makes good sense to avoid trouble and cost wherever possible.

Thanks to MSI components, the packaging of the electronics now approaches the size of the planar stack. Although electronics still represents more square inches, the disparity is closing rapidly and would have been eliminated had not core producers made improvements by stringing on tighter centers.

New, smaller cores provide a double advantage. They switch faster and require less operating power—not necessarily less current, but less overall power because smaller diameter cores need less energy to switch. They also permit mounting on tighter centers and reduce the cost/core of making an array.

In spite of integrated circuits and other heralded advances, modern core packaging is smaller and more compact than anything else in volume production – 500 bpi. This density can be matched or improved with certain optical techniques, but they are not widely produced nor available in the same type of packaging.

In core memory systems, you are dealing with the rate of current change, thus inductance and capacitance become critical. This must be considered in the physical layout of the system to minimize their effect on electrical performance. For instance, through creative planning and design, stack connections can go directly to the required point on the circuit board. This avoids running leads to an edge connector and back through another edge connector.

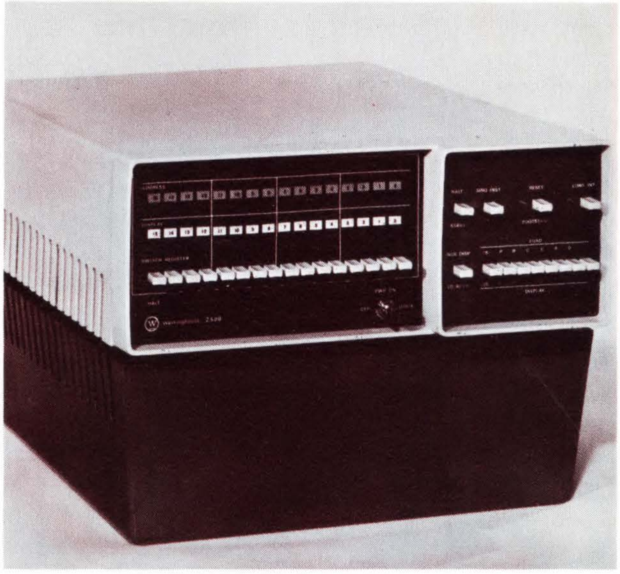
When the objective is low cost, high reliability and good productibility, techniques that permit production uniformity and predictability must be considered. One approach is to strive for a single card memory with minimum hand wiring. The goals are consistent wire paths and a 1:1 identity between the prototype and production units.

Developing the array and interconnect system in concert with the memory electronics also helps. Arrays and electronics designed as an integral unit permit valid determination of minimum path lengths, allow interconnects to proceed directly into the circuitry with the least amount of etch on the board, and avoid running a number of lines around the printed circuit board. As a pleasing fallout, concern over unpredictable items, such as mutual inductance and stray capacitance, is minimized.

Good interconnect techniques make these items highly predictable, and the design appears as straightforward as one from a textbook. Actual operating parameters and wave forms at each point in the circuit can be predetermined with the assurance that the paper design and the operating system will be almost identical.

On core stacks and core memory systems, overly restrictive specifications markedly increase the cost. Specifying drive line resistance, a factor of little significance, is one example. These lines are usually driven by a current source and the IR drop across the line can vary as much as 2:1 without appreciably affecting system performance.

Demanding inductance and capacitance measurements is another instance. A typical figure will usually do.

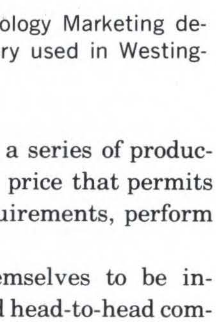


Using the planar array concept, Technology Marketing designed and developed the core memory used in Westinghouse's Model 2500 computer.

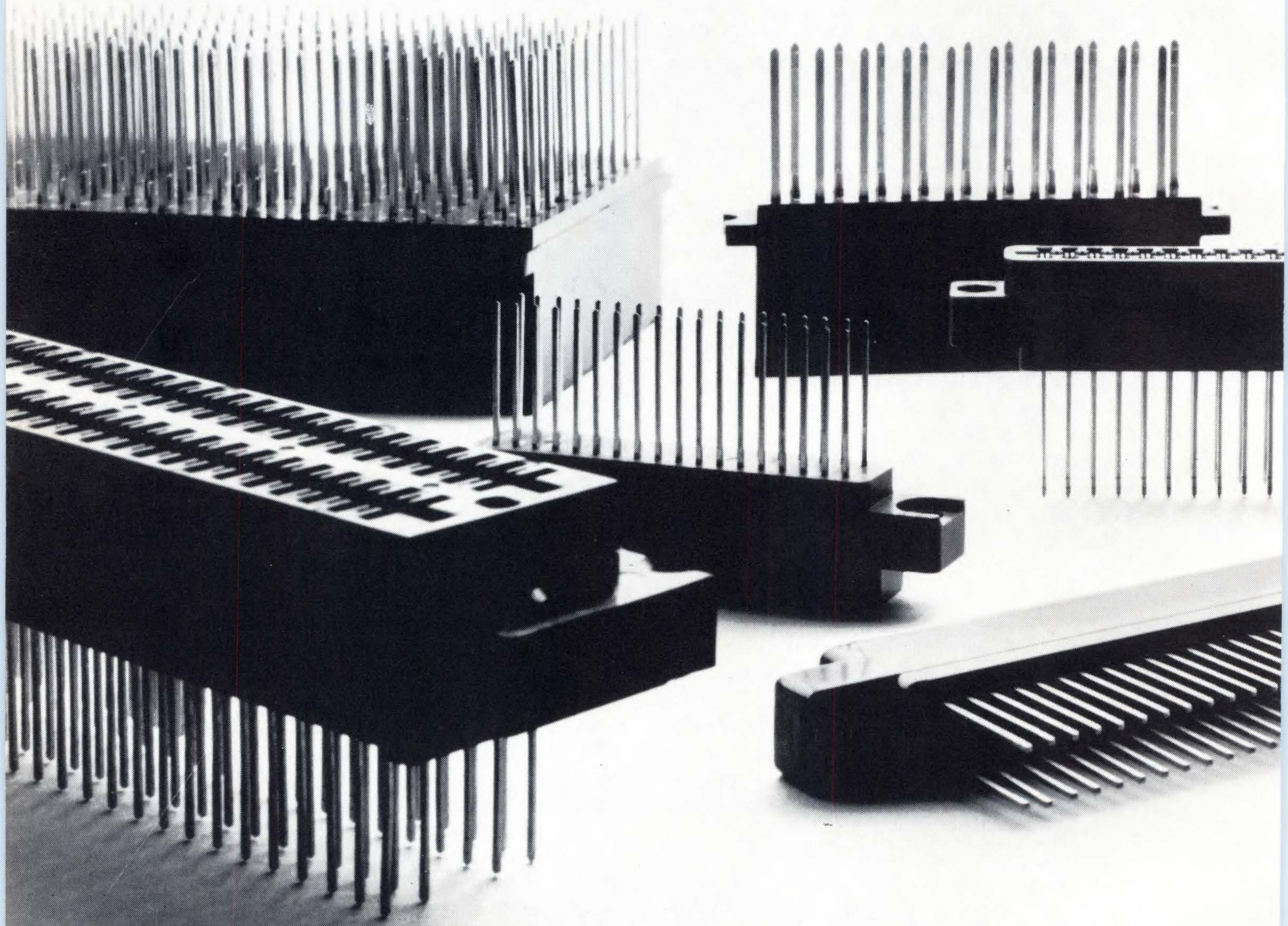
Conditions such as these impose a series of production tests on the vendor. He sets a price that permits his company to guarantee the requirements, perform the tests, and make a profit.

Engineers sometimes allow themselves to be influenced by vendors seeking to avoid head-to-head competition for the core order. Salesmen like to point out special features their product may contain that the opposition's does not. Unless these qualities are needed, their presence adds nothing to the value of the core, but their cost is included.

The engineer in charge should make sure that the specification lists only the required elements. And he should insist that all potential suppliers bid on an identical basis.



Donald T. Jones is a self-employed free lance writer. Presently, Mr. Jones generates technical articles and public relations material including brochures. He was previously employed at North American Rockwell Corp., Autonetics Div., as operations manager, Electro Sensor Systems. He received a B.A. in Business Administration from the University of Redlands and has done graduate work at the University of Southern California.



Some of our private

Most of our off-the-shelf connectors started out as custom designs for specific customers.

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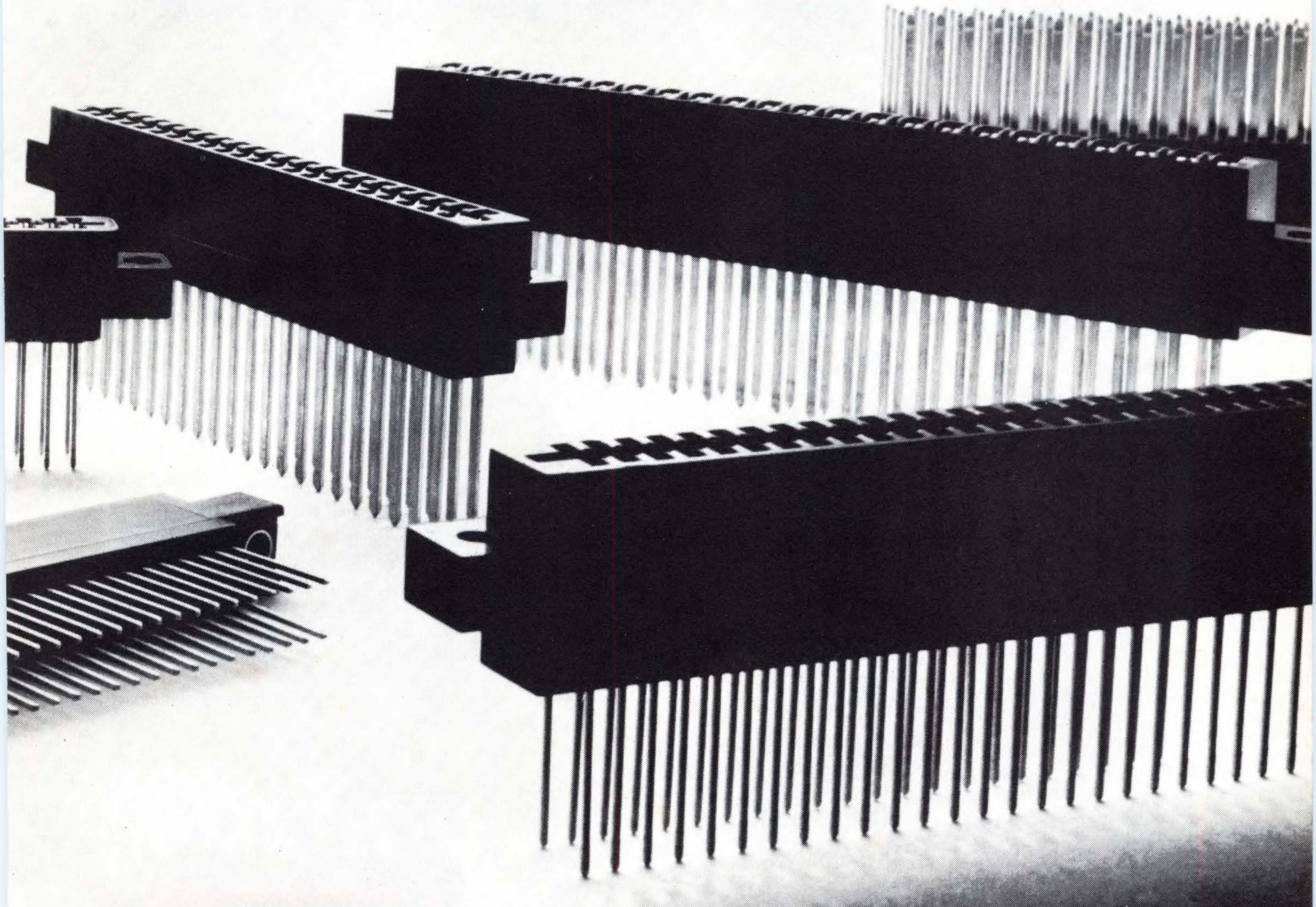
You get a custom connector at off-the-shelf prices—and there's no tooling cost.

For example, our P101 and new P201 circuit-card connectors have custom features such as contact-tail tip locus within .020 inch diameter of true position; our exclusive gold-dot contact system (the dots don't fall off) and a life of at least 500 trouble-free insertions and withdrawals. The P101 is also available with gold-plated bellows contacts.

In addition to these, we've got other connectors coming off the drawing board.

For example, our soon-to-be-ready P108 is a rack-and-



lines have gone public.

panel connector designed for the same tight contact-tail tolerances. It features a solid pin, solid housing construction and a low price.

The P101 is available with 12 to 100 contacts, and the P201 comes in 36, 72 and 100 contact sizes. The P108 has 50 and 104 contacts. Additional sizes can be made available.

They can become public property at low cost.

And, of course, we still have our complete custom facility available.

For those things you just wouldn't want to do in public.

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CIRCLE NO. 409

GTE SYLVANIA

multiplexer generates 9's complement

Generating the 9's complement of a BCD number can be complex. This task becomes easy, however, with an IC multiplexer.

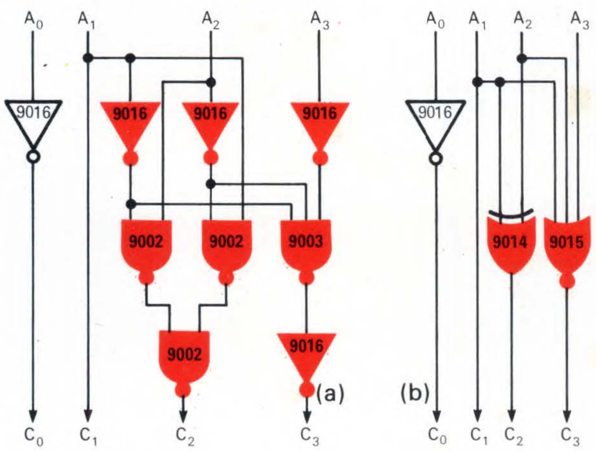
In a computer system, complementary coding of negative numbers is used to perform both addition and subtraction using either an adder or a subtractor, but not necessarily both. One such code is the nine's complement. Many designs, including programmable dividers and decimal adder/subtractors, use the nine's complement of a binary-coded-decimal (BCD) number. As shown in **Fig. 1**, the necessary decoding requires a number of gates or a mixture of gates in different packages—sometimes making circuit layout difficult.

The circuits in **Fig. 1** can be replaced with a dual four-input multiplexer as a function generator plus one inverter, as shown in **Fig. 2**. Logic equations defined by the truth table are:

$$C_0 = \overline{A_0}$$
$$C_1 = A_1$$
$$C_2 = A_1 \oplus A_2$$
$$C_3 = \overline{A_1}\,\overline{A_2}\,\overline{A_3} = \overline{(A_1 + A_2 + A_3)}$$

The inverter that generates the function C_0 is not required if the complement of the variable A_0 is available. One section of the 9309 multiplexer generates the exclusive-OR of A_1 and A_2. This is achieved by selecting a grounded input when A_1 equals A_2 and a high input when inequality exists. The other section of the dual device is used to develop the logic for C_3. Function Z_0 goes high only when A_1, A_2 and A_3 are all low.

Mogens Ravn is a senior applications engineer with Fairchild Semiconductor, Mountain View, Calif. Mr. Ravn is involved in the logic design of proprietary integrated circuits. He received a B.S. from Pennsylvania State Univ. and an M.S. from UCLA.



9's COMPLEMENT TRUTH TABLE

A_0	A_1	A_2	A_3	C_0	C_1	C_2	C_3
0	0	0	0	1	0	0	1
1	0	0	0	0	0	0	1
0	1	0	0	1	1	1	0
1	1	0	0	0	1	1	0
0	0	1	0	1	0	1	0
1	0	1	0	0	0	1	0
0	1	1	0	1	1	0	0
1	1	1	0	0	1	0	0
0	0	0	1	1	0	0	0
1	0	0	1	0	0	0	0

Fig. 1—**Two circuits** generate 9's complement as indicated in the truth table.

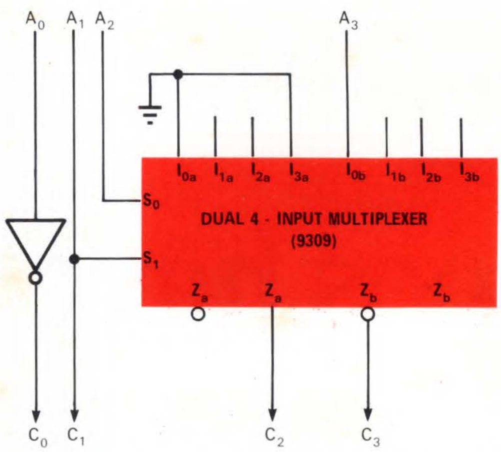


Fig. 2—**Multiplexer** 9309 replaces circuitry, indicated by shading in Fig. 1.

NEW SEMICONDUCTORS FOR

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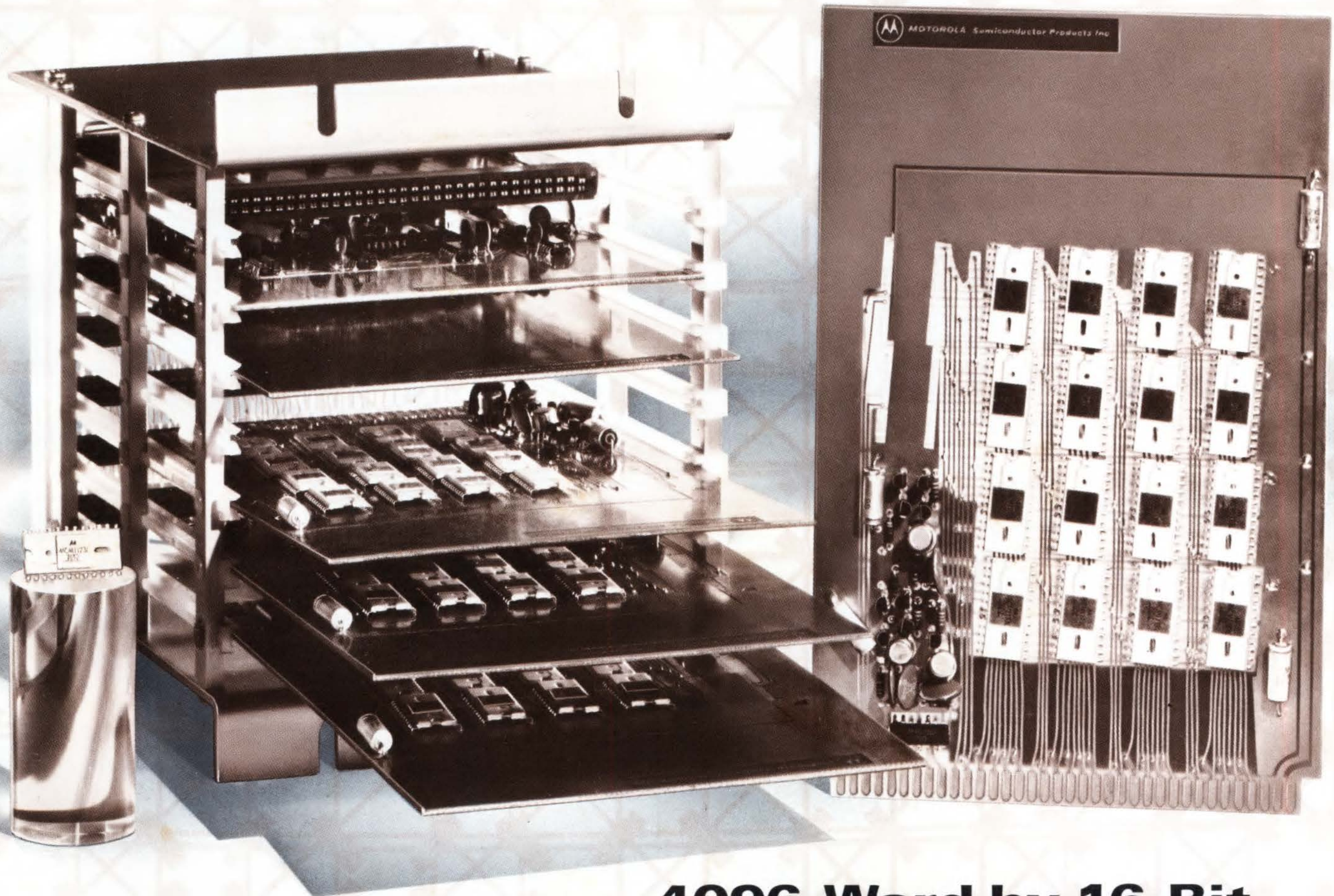


4096-Word by 16-Bit MOS MEMORY SYSTEM

(See Page C)

ALSO FEATURED IN THIS ISSUE:

Beat Cores With MOS In Medium-Speed Stores

Historically inexpensive but slow, cores in mini-computer, main-frame and bulk stores are moving over to make room for the backstretch drive of MOS dynamic storage random access memories. In the race for its logical place in your computer's medium-speed memory system, Motorola's MCM1173L is not merely competitive, but shows its class in the advantages of easy design, savings in space and power, and in the economy it offers.

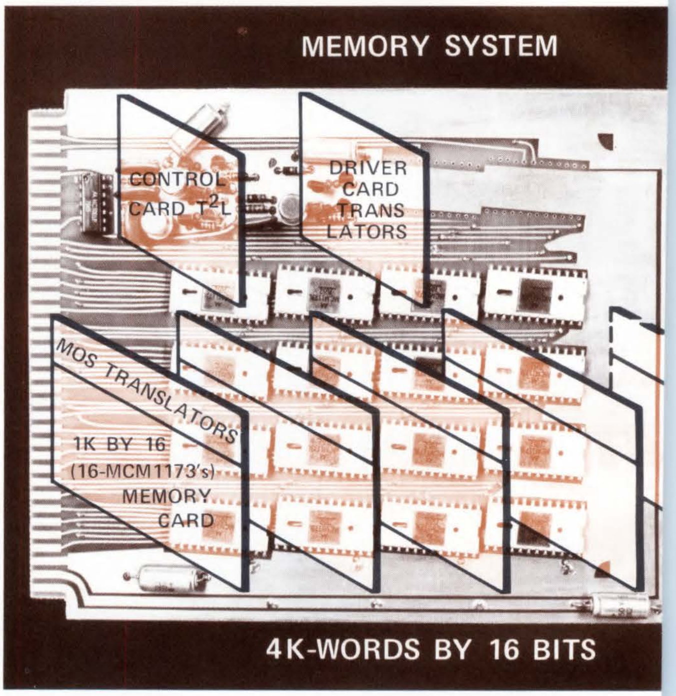
The outstanding advantage the MCM1173L brings to the memory designer is probably its ease of use. An add-on or replacement memory built from this device, for instance, can readily interface with existing system logic. With their low capacitances (address lines typically 2.5 pF), the MCM1173L's inputs are easily driven. Virtually noise free and providing greater than 3.0 mA output current, the MOS memory can drive a TTL gate or flip-flop directly. The need for an expensive, critical design sense amp to sift noise for a weak data pulse is eliminated. And your system layout restrictions are considerably eased.

In stores of certain organizations, the MCM1173L can save significant space. And where you're designing for minimum space, its typical dissipation of 50 μW/bit can reduce power requirements below that of the average core system. Another space-saving feature of this unit is the 22-pin package variation now available.

Dynamic storage of information in the MCM1173L is achieved in a 32 by 32 array of tiny three-transistor cells and associated circuitry. An organization of 1024 one-bit words is provided for maximum flexibility and word capacity. Ample wired-OR capability makes word expansion for larger capacity systems easy and bit expansion is simply a matter of connecting more MCM1173Ls in parallel.

Diode protection is provided on all inputs and a big advantage derives from the fact that you can refresh data without the chip select clock signal. Compared to other MOS devices, you gain design freedom and save the logic used to design around the simultaneous refresh/chip select constraint.

For a peek at a 4k word by 16 bit memory system based on the MCM1173L, see the "Try Dynamic MOS RAMs . . . " story on page C. The MCM1173L comes in a 24-pin, dual in-line ceramic package for the attractive 100-999 price of $28.00. The space-saving 22-pin package is also available. See your nearest Motorola rep or write for details by circling No. 451.



Column And Row Select Character Generators Offer 64 Most Used USASCII Characters

Row Select or Column Select, Motorola offers them both in monolithic MOS 2240-bit USASCII character generators for applications in systems with CRT or optoelectronic displays.

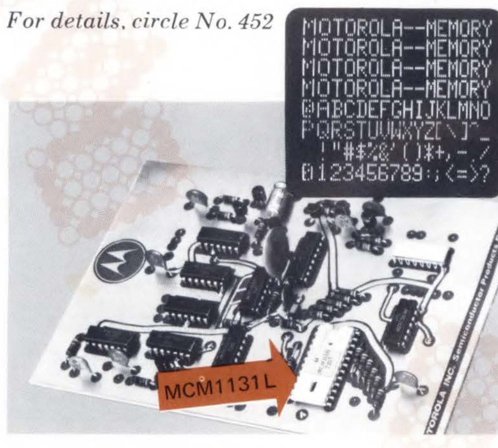
The MCM1131L and MCM1132L are column-select variations of the MCM1130 2240-bit read only memory, while the MCM1121L and MCM1122L are row-select variations of the MCM1120 2240-bit read only memory. Each of the 64 characters is stored as a specific combination of logic "1"s and "0"s in a five by seven cell matrix.

The row select MCM1121L/1122L each use the same type of 28-pin ceramic package. Open-drain output buffers that sink a minimum of 1.6 mA to provide bipolar compatibility are provided on the MCM1122L, while the MCM1121L features push-pull output buffers for MOS compatibility. The MCM1131L is available in the 24-pin ceramic package and the MCM1132L comes in the 28-pin package. All devices have wired OR capability for memory expansion.

A character is generated by applying levels corresponding to the ASCII input code for the desired character to the device address inputs. The select inputs are then used to cause words of five bits (row select devices) or seven bits (column select) to appear at the outputs. In actual operation, the proper logic levels are applied to the row (or column) select inputs in the appropriate selection code sequence. A seven word sequence of five parallel bits per word (five words of seven bits for the column select devices) then appears at the generator outputs.

See your nearest Motorola representative or write direct.

For details, circle No. 452



Try Dynamic MOS RAMs For Main Frame Memory Storage

MOS RAMs now compete successfully with core in the explosive mini-computer market for main memory storage applications. And the breakthrough that made it possible by essentially eliminating dc power dissipation as a factor and greatly reducing physical size requirements is the use of a dynamic storage cell in the MOS memory device. Motorola's MCM1173L 1024-bit dynamic RAM in the following fairly typical 4K word by 16 bit (expandable to 16K) memory system is a good example.

Since the MCM1173 is a 1024 by 1 memory, a logical approach is partitioning the system into 1K word by 16-bit cards. This partitioning scheme also provides easy memory expansion in 1K word increments up to a total of 16K words. The 4K system has four memory cards, one control and one interface driver card. Each memory card contains *16* MCM1173L devices which have all address and control leads paralleled. The control card contains a data distributor which routes the chip select signal to only one of the cards, thus selecting 1K out of 4K words. The ten address bits of the individual memory chips select one word from this 1K.

T²L to MOS Translators

In order to reduce noise and enhance speed, each memory card has its own T²L to MOS translators for reset, ϕ_1, ϕ_2 and chip select. The remaining lower capacitance control signals such as the read/write control, data in/data out and addresses are converted to MOS levels prior to being sent to the four memory cards. The memory control card provides the clocking signals to run the dynamic RAMS and provides the logic interface with the CPU. Refresh cycles, bookkeeping functions, and busy signals are also generated here.

The control unit is illustrated in the control card block diagram. The phase generator provides the clock signals to drive the MOS memories.

Refresh Circuitry

Refresh circuitry has to be included to insure that the memory is completely refreshed at least once every two milliseconds. All 32 bits in a storage column are refreshed at a single time. In order to completely refresh the whole memory every two milliseconds, one column must be refreshed at least once every 62.4 micro-seconds. A sequential address scheme is employed to insure that every column is selected once during this time. A 16 kHz clock is used to increment this address and also to start a memory lock-out and refresh cycle. The address selector section of the control card switches from the external column address coming from the CPU to the refresh address during a refresh cycle.

Logic is necessary to control both the interactions between the refresh and phase circuitry and to inform the CPU when refresh is taking place. This section of the control card is labeled "Refresh control and lockout" in the block diagram.

The shift register clock used for phase generation and the refresh control clock are generated here. The enable input from the CPU starts a read or write cycle by allowing a flip-flop to toggle, supplying a shift register clock. Once the shift register has initiated its cycle, the flip-flop is held in a toggle mode until a cycle is finished and a busy signal is given to the CPU. An exception to this occurs if SPLIT CYCLE is high, stopping the shift register at the second reset pulse until a write command is given. This provides a read-modify-write capability used in some processors.

The 16 KHz refresh clock supplies 62.4 μs periods during which one refresh cycle must occur. A chain of flip-flops controls the locking out of the CPU for a refresh cycle which can occur at any time during the period when the preferential refresh signal comes from the CPU. If no P. R. signal comes by the end of the time period, the circuitry automatically holds the busy signal high after a memory cycle and "steals" the next time period for a refresh cycle. This appears as a normal read cycle at the address selected by the refresh counter.

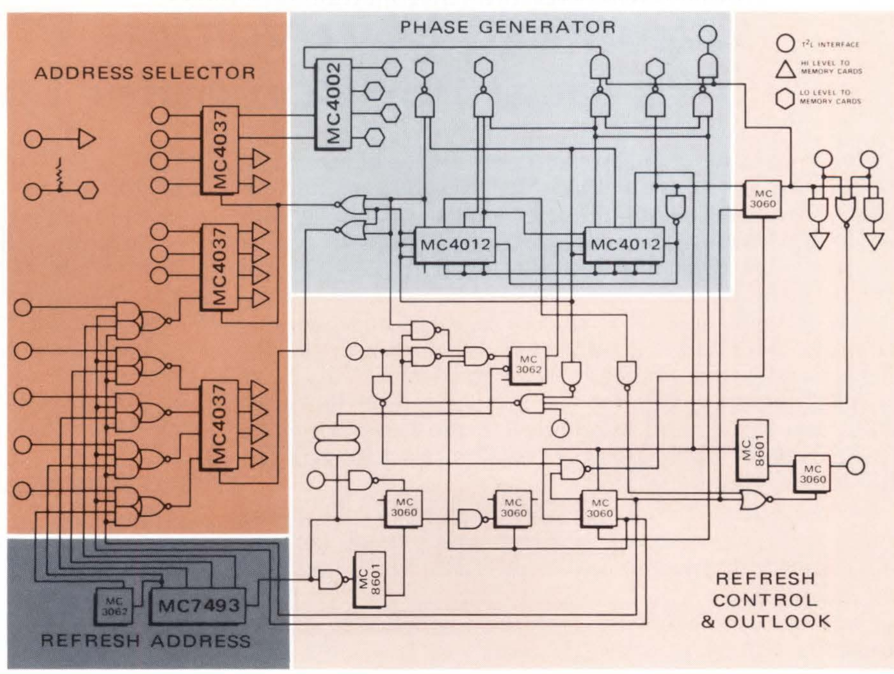
The system includes a variable reset time for the BUSY signal which allows the memory system to be "tweaked" into the CPU operating cycle.

Electrical Characteristics

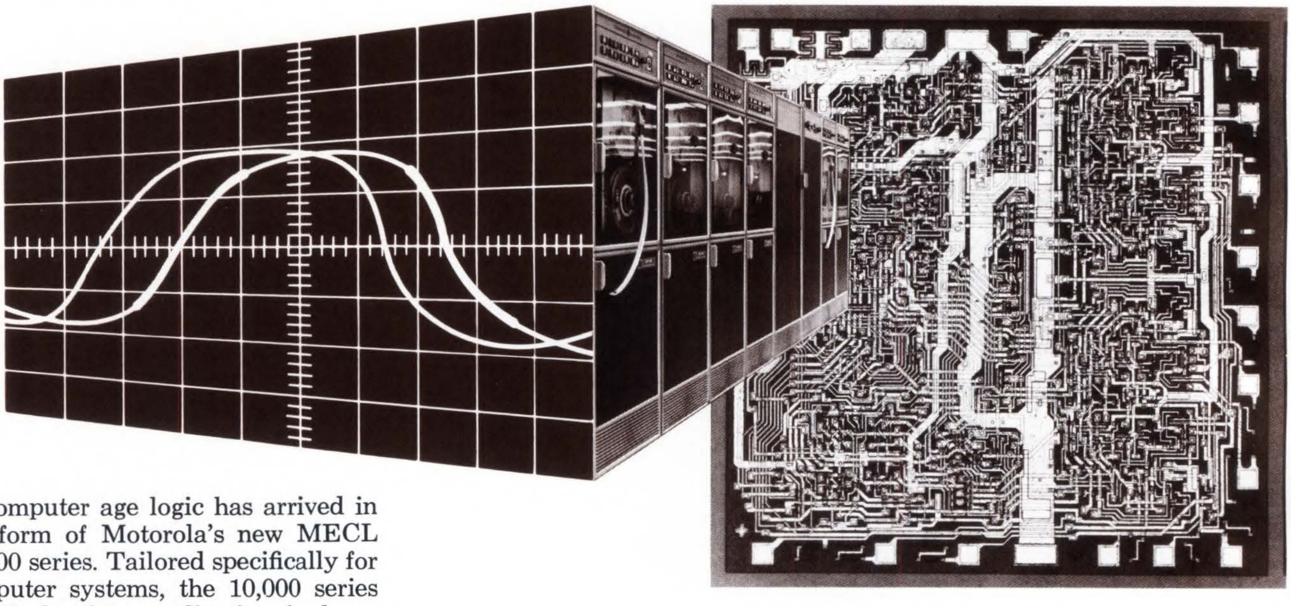
Recommended voltage difference between V_{SS} and V_{DD} is 18 volts for operation at a cycle time of 800 ns. For this memory system V_{DD} is at ground potential and V_{SS} is +18 volts. The memory device input logic swing for these supplies is 18 volts, so trans-

Continued — Page I

COMPLETE SCHEMATIC FOR CONTROL LOGIC



High-Speed, Low-Power Logic Family Specially Designed For Computer Systems



Computer age logic has arrived in the form of Motorola's new MECL 10,000 series. Tailored specifically for computer systems, the 10,000 series will find prime application in large and small central processing units, high speed peripherals such as discs, and high speed memories.

From a speed-power standpoint, the MECL 10,000 series provides a decided improvement on the latest Schottky-clamped TTL lines, and functionally, it has a great many operating advantages over TTL designs. For example, MECL 10,000 is characterized by high speed (typically 2 ns propagation delay per gate), low power (25 mW dissipation per gate), and toggle frequency to 150 MHz. Couple this with logic design flexibility, constant power dissipation, and ease of driving various transmission line configurations and you have the ultimate logic family for computer systems.

These MECL 10,000 functions are now available:

Series	Characteristics	Unit Price (100-up)
MC10109L	Dual 4-5 Input OR/NOR Gate	$ 2.00
MC10110L	Dual OR 3-Output Gate	2.50
MC10111L	Dual NOR 3-Output Gate	2.50
MC10119L	3-3-3-4 Input OR-AND Gate	2.50
MC10131L	Dual D Flip-Flop	7.00
MC10181P	4-Bit Arithmetic Unit	20.00

Planned to be strong in complex functions, the family will add in 1971: 11 gate functions, 2 line receivers, 5 complex functions and memory elements such as a dual D latch, a dual J-K Master-Slave flip-flop, a 64-Bit RAM, a 256-Bit fusible link ROM plus others.

Contact your nearby Motorola distributor for evaluation devices now. Computer designs deserve computer logic — MECL 10,000 is the answer for optimum system performance.

For details, circle No. 454

Ultra-Fast, Low-Voltage PNP Switches Are Ideal For Computer Logic Circuits

If you're among the many designers who need very high-speed switching at low voltages for special computer circuits, your requirements can now be fully satisfied by four new PNP silicon switching transistors offering both similar and improved capabilities of the standard 2N4208 and 2N4209 devices.

Two of these new PNP silicon Annular transistors — called the MM4208 and MM4209 — are spec'd like the 2N4208 and 9 but provide a lower minimum $V_{BE(sat)}$ of 0.7 Vdc versus 0.8 Vdc for the 2N parts. And the MM-4208A and MM4209A, in addition to the lower minimum $V_{BE(sat)}$, offer a higher BV_{CEO} of 15 V to give you considerably greater design latitude.

Switching times for all four transistors, @ $I_C = 50$ mAdc, are $t_{on} = 15$ ns (max), $t_{off} = 20$ ns (max). Their current-gain bandwidth product is a high 1300 MHz (typ) @ $I_C = 10$ mAdc.

The four new devices also feature a low collector-emitter saturation voltage of 0.18 Vdc (max) @ $I_C = 10$ mAdc, thus providing a high level of operating efficiency.

Collector current-continuous, with a maximum rating of 200 mAdc, also fills high-performance needs such as efficient display driving and other logic circuit applications.

Both the MM4208 and its "A" version have h_{FE} min/max ratings of 30/120 @ $I_C = 10$ mA, $V_{CE} = 0.3$ V, and the MM4209 and its "A" version have corresponding min/max h_{FE} ratings of 50/120.

These new switches are supplied in the rugged TO-18 metal case for the following 100-up prices: MM4208 — $2.50; MM4209 — $4.50; MM4208A — $3.00, and MM-4209A — $5.00.

For details, circle No. 455

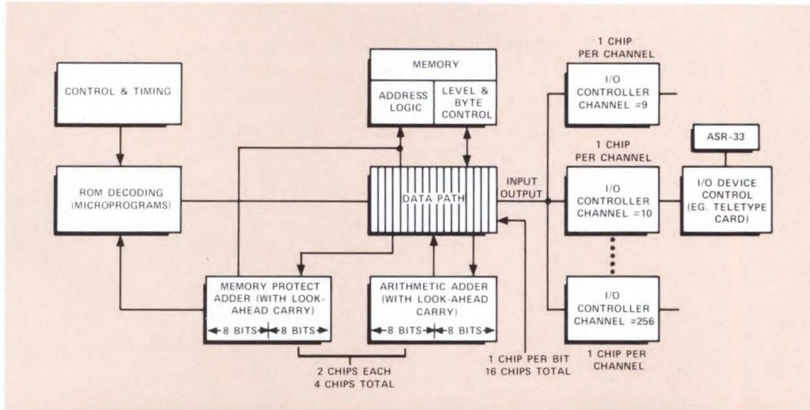
SWITCHING CHARACTERISTICS	Symbol	Typ	Max	Unit
Turn-on time ($V_{CC} = 3.0$ Vdc, $I = 50$ mAdc, $I_{B1} = 5.0$ mAdc)	t_{on}	—	15	ns
Turn-off time ($V_{CC} = 3.0$ Vdc, $I_C = 50$ mAdc, $I_{B1} = I_{B2} = 5.0$ mAdc)	t_{off}	—	20	ns
Storage time ($V_{CC} = 3.0$ Vdc, $I_C \approx 10$ mAdc, $I_{B1} = I_{B2} \approx 10$ mAdc)	t_s	17	20	ns

Array-Derived TTL/LSI Increases Mini-Computer Speed/Capability

The availability of TTL-LSI provides the computer system designer with a powerful tool. An example of one of the types of systems that can benefit from the use of the TTL-LSI tool is a mini-processor designed by the Motorola Control Systems Product Operation. In developing the TTL-LSI functions needed for the prcoessor, the advantages offered by Motorola Semiconductor Products' 112-gate array were significant factors in the decision to use this technology rather than full custom design.

Design Objectives

The mini-processor is used by Motorola to process data entering a system from communication channels. The design objective was to build a mini-processor with a sophisticated, high speed, high capacity, input-output structure.



(FIGURE 1) MINI-PROCESSOR SYSTEM ARCHITECTURE

System Architecture

The new mini-processor is controlled by a microprogrammed read-only memory (ROM), as shown in Figure 1. Designed for powerful input output (I/O) data control, its internal structure provides complete byte manipulation capability.

The processor is organized to take advantage of techniques which reduce the programming burden associated with information transfers. The programmer, for example, can set up a data block transfer to or from any or all peripherals and this block transfer will be completed without further program interference. To achieve this data transfer strength and still keep cost in line with the mini-processor philosophy, the pointers and control words associated with the 256 I/O transfer channels are contained in the main memory rather than in dedicated hardware registers resident in the I/O section. High speed information transfers thus rely upon the use of very high speed main memory and very low processor propagation delay times.

The speed requirements of the central processor were satisfied by turning to available TTL-LSI technology. Use of Motorola's 112-gate array led to physical compression of the logic and lower, more consistent delays.

To take advantage of the continuing improvement in the price/performance ratio offered by semiconductor memory technology, the processor is designed to function with memories of various speeds.

The three separate processor functions implemented with the 112-gate array are the adder, the data path, and the I/O channel controls.

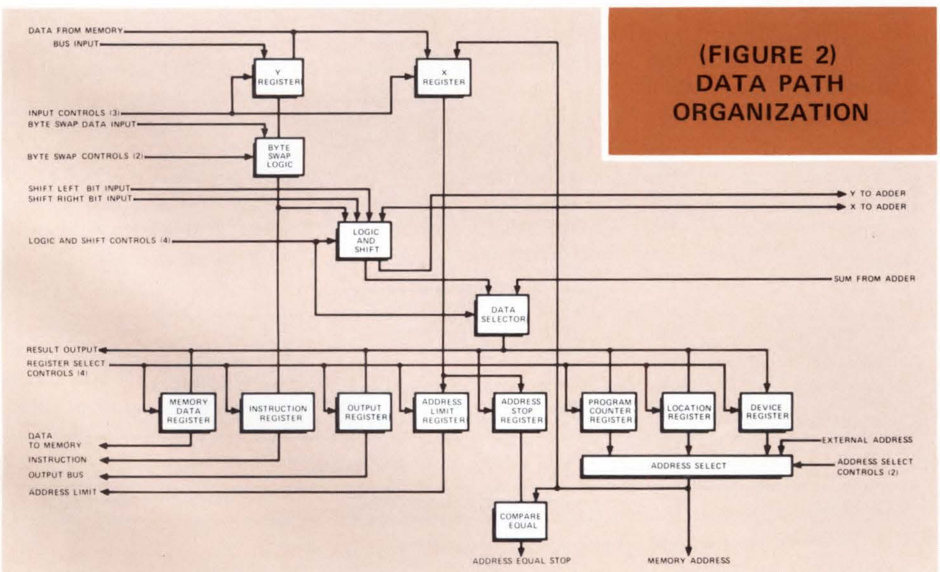
The two sixteen-bit adder functions, i.e., the arithmetic function and the memory protect function, are each contained on two identical chips of eight bits each. The propagation delay through a full 16-bit adder function is calculated to be 50 ns typical, 68 ns maximum.

112-Gate Array Cuts Board Requirements

The data path function shown in Figure 2 contains the registers, logic and data buss connections necessary to implement the data manipulation portion of the mini-processor. Partitioning the function so that the corresponding bit in each register is contained on the same chip offers greater system speed because most of the data path is on a single chip. Sixteen identical circuits are used to build the complete data path function.

The use of the 112-gate array permitted the processor data manipulation circuitry to be built on two identical 5 x 7-inch printed circuit boards, each composed of 8 data-path chips, 1 adder chip performing the arithmetic function, 1 adder chip performing the memory-protect function, and 3 additional logic chips.

The I/O controller channel represents an application in which speed/propagation delay was not the major concern. Rather, the need was for a highly repetitive function, up to 256 identical high gate-count chips per processor. The low design charge and fast turn-around time offered by the 112-gate array were advantages here.



(FIGURE 2) DATA PATH ORGANIZATION

Advantages of theTTL-LSI Approach

Most of the performance advantages of TTL-LSI are derived from the reduction in drive required of

Continued Next Page

ARRAY DERIVED TTL/LSI
Continued from Page E

individual elements within the LSI function. Simply stated, logic elements drive very short leads that have little capacitance. Internal gates can function without the totem-pole output needed for off-chip driving. What results is smaller gates with higher speed using less power.

Systems benefit directly in terms of higher speed and lowered power requirements. The more efficient utilization of silicon by LSI results in several indirect system benefits including reduced size, construction cost and total cost.

Building TTL/LSI Using the Array Concept

A customizable array consists of a silicon chip containing a pattern of cells completely processed except for metalization. The array is transformed into a custom circuit by designing metalization patterns that connect the cells into gates and the gates into the desired functions.

Compared to a fully custom design, there are three telling advantages in the array approach.

First, the customer is working with a proven design, except for the interconnections whose logical integrity can be established. Therefore the probability of a successful part from the first design effort is high.

Second, turn-around time is low for delivery of production quantities because of commonality in the diffusion processes with standard TTL. Turn-around time is also low because the array's predesigned cells make the use of Computer Aided Design easy. Metalization patterns for various gates, for example, are already available and may be called for by the customer/designer as required.

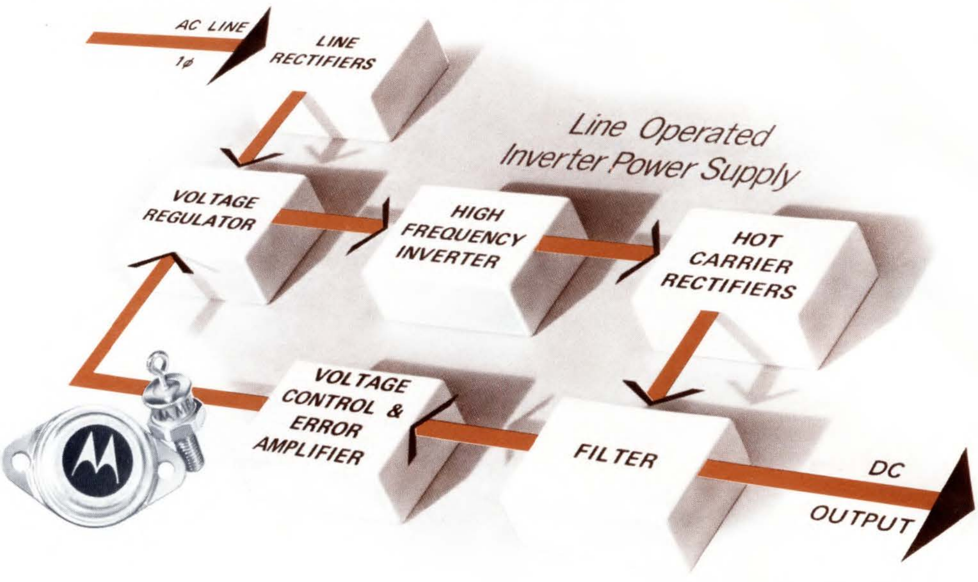
Finally, custom design costs are lower since only metalization patterns need be determined.

Patterns of uncommitted elementary cells such as Motorola's 112-gate array offer the customer/designer greater flexibility than arrays of fixed gates such as AOI's. In the 112-gate array each cell can be connected at the first metal layer as high-level, low-level or buss gates. And, if needed, AOI's or totem-poles can be implemented.

Conclusion

Allowing great design freedom and the option of drawing upon computer aids, the use of Motorola's 112-gate array offers a practical method of implementing a system in TTL-LSI. The array concept can provide circuits in minimum time at low cost. In the hands of a computer system designer, it is, indeed, a powerful tool.

Reduce Power Supply Size & Weight With High-Frequency Inverter Techniques



A line-operated inverter power system capable of delivering 225 watts may now be fabricated in a space as small as 3″ x 6″ x 6″ (108 cu. in.) and weighing only 2 pounds.

A dissipative regulator of the kind ordinarily used in computers would require a transformer by itself weighing about 15 pounds and would have a volume requirement far in excess of 108 cubic inches!

This tremendous volume and weight savings is accomplished by using a high-frequency inverter preceded by a regulator which is fed directly from the rectified AC line. Since the inverter operates at approximately 20 kHz, hot carrier rectifiers (four MBD5400's) are utilized to efficiently produce the low-voltage, high-current DC output.

Voltage Regulation

Output voltage regulation is accomplished by a feedback network between the DC output and the line voltage regulator. The latter uses high voltage silicon power transistors.

Besides size and weight advantages, system efficiencies are relatively high at about 60%. Heat and volume required for heat dissipation are drastically cut as a result.

50% Less Power Loss

The MBD5400 hot carrier rectifiers provide a 25 A current capability with less than half the forward voltage — and consequent 50% less power loss — as compared to conventional silicon devices. Their majority carrier operation provides no stored charge and extremely fast recovery times.

Either the MJ9000 or 2N5241 power transistor may be used in the voltage regulator. Both feature 10 A I_C, 325 V sustaining voltage capability and excellent safe operating area. Switching times for the 2N5241 are included on the data sheet: 2.5 μs maximum @ 2.5 A I_C. Saturation voltage is 0.7 V @ 2.5 A.

Write for data including a start-to-finish application note completely describing inverter circuitry!

For details, circle No. 456

HOT CARRIER RECTIFIERS

Series	Outstanding Characteristics	Price 100-Up
MBD5300 MBD5400 MBD5500/A MBD5550/A	50% less power loss (½ the V_F) flat rectification efficiency to 50 KHz, low stored charge and high surge capability from Schottky barrier principle.	$3.60 6.00 8.50 9.10

HIGH VOLTAGE SILICON POWER

Series	Outstanding Characteristics	Price 100-Up
MJ431 MJ9000 2N5241	5 to 10A, 325 $V_{CEO(SUS)}$ capability, 0.7 to 2 V $V_{CE(SAT)}$ range for high voltage operation in inverters, converters, regulators and switches.	$11.50 10.80 15.56

Hybrids Extend IC Capabilities, Lower Costs In Computer Systems

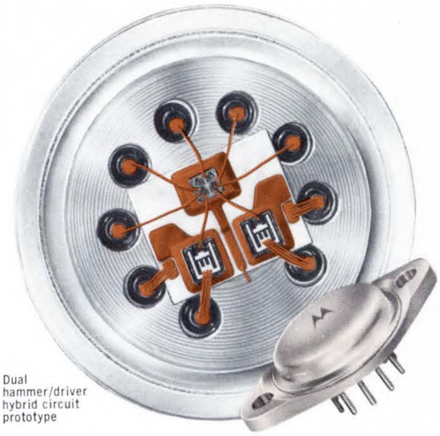
As the state of the monolithic IC art advances, so too does the understanding of the very substantial place and contribution of the hybrid circuit.

Hybrid circuits extend the monolithic integrated circuit capability into areas of high current, high voltage, and precision components. They provide performance and the total function in a compact package for simplified equipment design and construction, and smoother component procurement.

As one of the world's major discrete and IC semiconductor suppliers, Motorola has the broadest possible in-house base of product and product knowledge handsomely complemented by the latest in complete thick and thin film production facilities, using specially-developed assembly techniques.

One Motorola hybrid circuit of particular interest to designers of computer peripheral equipment is the new MCH2890 Dual Hammer Driver for which a 10-pin TO-3 package is used because of its power handling capability, rugged hermetic construction, and acceptance as an industry standard.

This dual power-driver has a breakdown voltage of 120 V and is designed for 6 amp pulse operation with 8 amp surge capability. The circuit has a thermal resistance of 5.0° C/W for single channel operation and 7.5° C/W for dual channel operation. Samples are available with formal product announcement planned in the very near future.



Dual hammer/driver hybrid circuit prototype

New Computer Hybrid Development

Several other computer hybrids are currently in production but not yet released. One is a 32 V clock driver for shift register memories with loads up to 2,000 pf and typical switching times of 100 ns total on and 100 ns total off. A Quad MOS TTL level translator converts from 0 to −10 V MOS levels to standard TTL levels. For driving 500 mA into a .5 μH load with current switching times of 50 ns on and 40 ns off, a 40 V TTL compatible core driver has also been developed. With diode arrays of considerable interest, the introduction of a 60 V dual eight-diode array and a 60 V dual sixteen-diode array is notable. V_f range at 500 mA is .8 to 1.3 V, and t_{rr} is less than 5 ns @ 10 mA.

If you have a specific hybrid circuit application, write directly to Hybrid Marketing, Mail Drop A140, Motorola Semiconductor Products Inc., P.O. Box 20932, Phoenix, Arizona 85036.

Silicon Gate Technology Increases MOS Appeal And Productivity

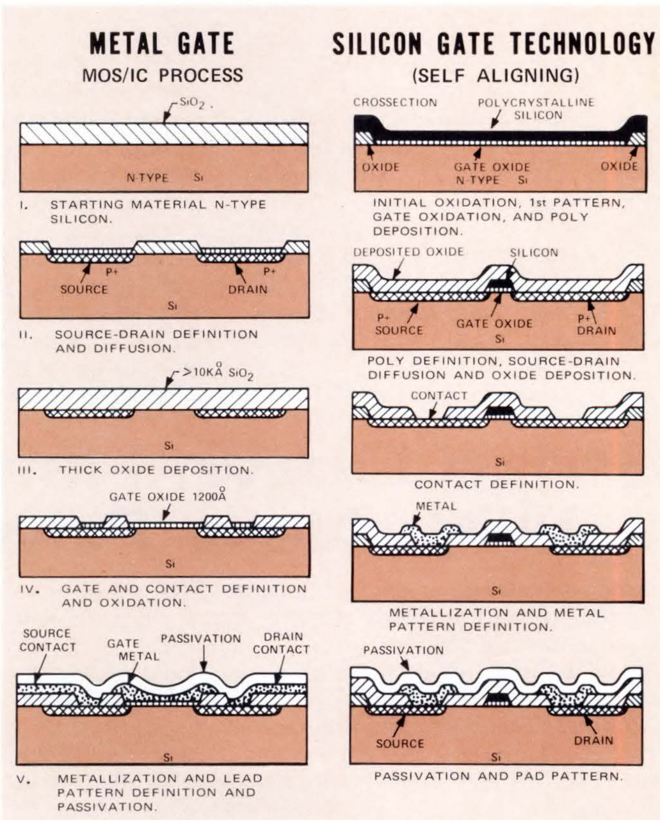
Early predictions of high yields and low costs for MOS/LSI were several years premature.

Now Silicon Gate MOS/LSI technology is a production reality finally leading to fulfillment of those early expectations. And the use of a polycrystalline silicon layer as the gate electrode is the key to this success.

The most important benefit in silicon gate processing is the self aligning feature inherent in the process. The gate electrode itself acts as the diffusion mask that defines the source and drain regions during processing, providing precise alignment of these regions. Extension of the gate from the source completely to the drain regions insures formation of the channel during device operation. In conventional processing alignment must be maintained through successive masking operations. Overlap must be provided in the mask set to compensate for misalignment in the manual mask alignment procedure. This overlap wastes chip area and causes relatively large parasitic capacitances that tend to limit device performance.

One of the major advantages of this self-aligned gate structure is that it limits any overlap to that caused by side diffusion and therefore minimizes the effect of parasitic capacitances.

The key silicon gate feature that allows reduced die size is the additional interconnection flexibility provided by the polycrystalline silicon. Diffused conductors are available in the substrate with this technology as with other MOS structures. The polycrystalline silicon is separated from the substrate by an insulating oxide layer (see diagram) and is used (with some restrictions) as an interconnecting layer of diffused conductors. Another oxide layer separates the polycrystalline silicon from the aluminum metalization which also provides the usual interconnection capability.



Since almost three layers of interconnection flexibility are available with silicon gate processing the device geometrics can be reduced to — Continued Page I

Noise Immune Logic Functions Expand Designer's Choice

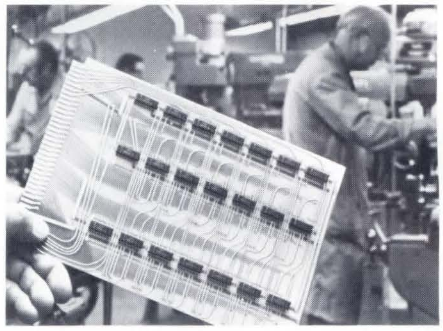
Designers of industrial control systems or computer systems that must operate in high-noise environments now have three new logic tools. A quad latch, a quad exclusive-OR and a dual pulse stretcher have been added to Motorola's high-threshold MHTL line, which now totals 23 functions.

High threshold circuits are relatively immune to false switching triggered by electrical noise because the voltage required to drive a device input from the MHTL "1" or "0" level to the switching threshold is much larger than for any other bipolar logic type — in fact, 5 volts on either side of the threshold.

The MC682 quad latch is useful in monitoring and storage applications. The quad configuration can temporarily store a four-bit binary coded decimal digit, or four bits of a binary number.

The quad Exclusive-OR, MC683, consists of four gate arrays. Each array accepts two inputs, and generates the Exclusive-OR output.

The dual pulse stretcher, MC675, generates an output pulse, whose width is the sum of the input pulse width and an externally determined interval.

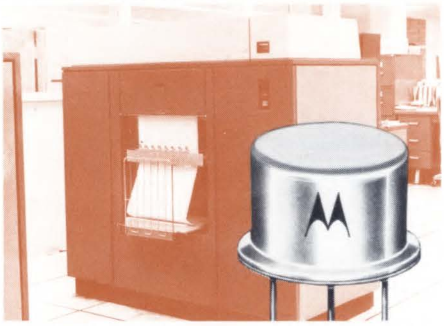


Each of the three functions is in a 16-pin dual in-line package.

Type		Quantity/Price 100-999
MC675P MC682P MC683P	Plastic Package	$1.86 2.20 2.05
MC675L MC682L MC683L	Ceramic Package	2.16 2.75 2.55

For details, circle No. 457

4-Amp Silicon Power Switch Offers Nanosecond Nimbleness



Here's a quick answer to your needs for a rugged printer/hammer-driver offering top performance in a tiny (TO-39) package — the 2N4877, 4 A, 60 V, 10 W device. *It provides 60* $V_{CEO(sus)}$, 20 to 100 h_{FE} range at 4 A/4 V, an f_T of 30 MHz and rise and fall times of 100 and 500 nanoseconds, respectively.

Saturation is a miniscule 1 V at 4 A and leakage current measures in the low microamperes. Design it into your critical, space-limited applications for an economical 100-up price of $2.50.

For details, circle No. 458

New Germanium Family Wins Power-Package-Price Crown

57 W power-dissipation in a TO-66 case! . . . at prices that start at 49¢ 100-up!

That's the new 2N5887-5901 series with gain-spec levels at 0.5, 3 and 7 amperes and with 20 to 75 volt BV_{CES} ratings to enhance your low-frequency design possibilities in computer power supply applications.

Of course, all the other germanium advantages are there too; saturation voltage of only 0.4 V @ 7 A, low 10 mA leakage @ 100°C and . . . low price! 100-ups start at a low, low 49¢ and top out at $1.15 for the 75 V unit. The series offers the reliable, compact

TO-66, cold-weld, all-aluminum case and is electrically similar to the 2N3611.

For details, circle No. 459

Strike Down Hammer-Driver Costs With New Power Darlingtons!

Now you can cut the cost of hammer-driven designs — and other computer-related circuitry, too — with six new silicon power Darlington transistor families!

The 4 to 16 A units eliminate conventional power circuits in printers requiring separate, "one-for-one" driver and output transistors and emitter-base resistors.

Each device in a series has its complement: in TO-3's, there are the 4 A MJ4000/4010, 5 A MJ900/1000, 10 A MJ2500/3000 and the 16 A MJ4030/4033 series. In plastic, there is the 4 A MJE700/800 and 5 A MJE1090/1100 Thermopad series.

Because of their high gain, you can drive Darlingtons with ICs and go directly from milliamperes to amperes. Their complementary capability makes possible both positive and negative-based systems and, because they require a single heat sink, space and component needs are lessened, reliability rises and costs decrease.

Initial cost is low — a complementary 4 A, 75 W, TO-3 pair costs just $3.20, 100-up — and six families let you choose the exact degree of cost/performance you need!

Darlington Series		I_c (cont.) A	V_{CEO} (sus) V	h_{FE} (min) @ I_c	Price (100-Up) Range	
PNP	NPN				PNP	NPN
*MJE700-703	*MJE800-803	4	60/80	750 @ 1.5/2 A	$1.42 to 2.02	$1.20 to 1.68
MJ4010/4011	MJ4000/4001	4	60/80	1,000 @ 1.5 A	1.85/2.30	1.35/1.80
MJ900/901	MJ1000/1001	5	60/80	1,000 @ 3 A	2.28/2.71	1.57/2.14
*MJE1092/1093	*MJE1090/1091	5	60/80	750 @ 3 A/4 A	2.40/2.65	2.05/2.03
MJ2500/2501	MJ3000/3001	10	60/80	1,000 @ 5 A	3.65/4.05	3.05/3.45
MJ4030/4031	MJ4033/4034	16	60/80/100	1,000 @ 10 A	4.35/4.85	4.15/4.55

*Plastic Thermopad Package

For details, circle No. 464

Core-Driver Trio Stars In Total Memory-Driving Role

With the introduction of three discrete, hermetic core-drivers, designers of driver circuits for core memories are afforded considerably increased design latitude. Two of the new NPN silicon transistors — the 2N5859 and the 2N5860 — are made specifically for high-current, high-speed switching applications, and the third device — the 2N5861 — is designed for medium-current, high-speed switching.

All three parts — supplied in the popular TO-39 metal can — are ideally suited for ferrite core and plated wire memory-driver or MOS translator applications.

The 2N5859 and 2N5860 memory drivers feature maximum turn-on and turn-off times (@ I_C = 1.0 Adc) of 35 ns and 60 ns, respectively. And the 2N5861 also demonstrates fast turn-on times of only 25 ns and turn-off times of 60 ns @ I_C = 500 mAdc.

100-999 prices, at your nearest Motorola distributor are: 2N5859 — $.65, 2N5860 — $.90, 2N5861 — $1.00.

For details, circle No. 460

Dynamic MOS RAMs — Continued from Page C

lators are used. Although the individual address and phase input capacitances are small, the paralleling of devices can result in considerably higher loads. Individual phase drivers are used here for each card, resulting in a load of 16 inputs or typically 300 pF including wiring. Addresses are common to all 64 devices for a similar total capacitance. The data inputs are only four parallel loads for a total of 25 pF and do not require high drive capability. The simple translators used in this system are MTTL high voltage gates such as the MC7407 with current boost complementary emitter followers. These translators can safely drive in *excess of 500 pF in less than 20 ns* and easily fulfill the drive requirements of the memory systems.

Memory Output

Output of the memory devices consists of open drain MOS devices with 3 mA minimum drive capability. Bipolar interface is easy with the resulting high on/off output current ratio of the MCM1173. One technique uses the high output current, typically 5 mA, to develop sufficient voltage across 1 K load resistors to drive the D input of a flip-flop (or gate) to a logic "1" state. During the time the memory output is valid, the trailing edge of the Data Valid signal transfers the data into *a quad latch.* If the lead length from the memory system to the CPU is very short, the output of the MCM1173 devices could be connected directly to the CPU without a data latch.

Conclusion

Design of a minicomputer mainframe system such as the one briefly described here points out the versatility of dynamic random access memories. It should also kill the myth that these RAMs are hard to use and require expensive external circuitry to drive them.

For details, circle No. 453

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P.O. Box 20924
Phoenix, Arizona 85036

FOLD HERE

NPN Memory-Driver Quads Gain Higher Power Ratings, Increased Temperature Range

Originally introduced as 600 mW devices, the MPQ3725 and MPQ3303 Quad Memory-Drivers, in the dual-in-line TO-116 plastic package with a copper lead frame, now offer higher power ratings of 2.5 watts for four devices, or 1.0 watt for each device.

A new increased operating and storage temperature range for both quads of −55° to +150°C, together with their high-speed high-current and low-saturation voltages are just a couple of the superior memory-driving parameters you've been looking for.

Their high-speed switching characteristics are:

MPQ3725 — t_{on} = 20 ns (typ) @ I_C = 500 mAdc
t_{off} = 50 ns (typ) @ I_C = 500 mAdc

MPQ3303 — t_{on} = 15 ns (max) @ I_C = 1.0 Adc
t_{off} = 20 ns (max) @ I_C = 1.0 Adc

Warehouses are fully stocked and the 100-up price for both devices is only $3.75 each.

For details, circle No. 465

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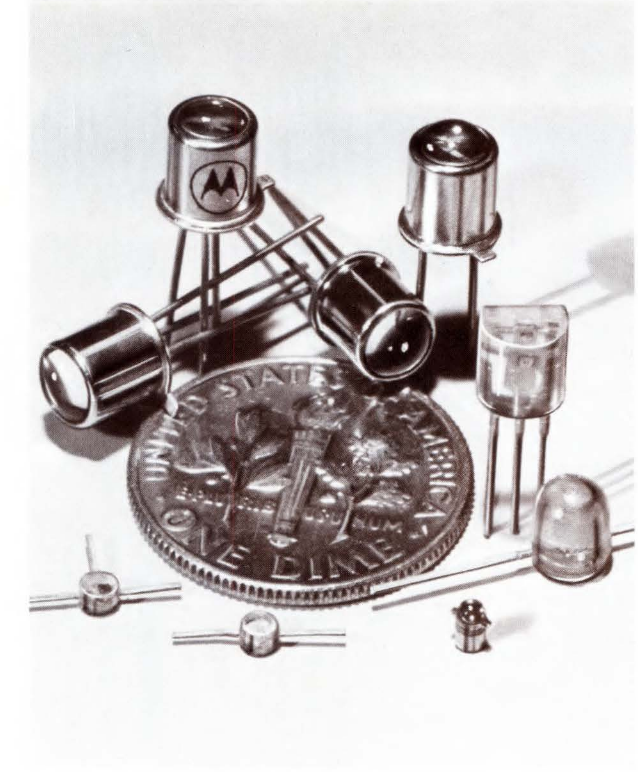
Silicon Gate Technology — Continued from Page G

minimum size. This provides reductions in chip area of up to 50 percent over equivalent parts built using conventional technology. These smaller devices provide higher component density and represent more die per wafer and, eventual lower costs to the user.

With the improvements in interconnection flexibility, smaller die size, and the elimination of parasitic effects, device performance improves, too. Higher frequency operation is possible, and as a result of improved work functions between materials, the voltage required to establish the conducting channel (threshold voltage) can be made low enough to insure complete bipolar compatibility. In fact, threshold voltages below one volt are now readily obtained.

Silicon gate processing can be used with P-channel, N-channel or complementary MOS structures and offers significant improvements over conventional processing for each type. It is apparent, then, that this new silicon gate technology offers a combination of advantages that is unmatched by other manufacturing techniques.



New LEDs Brighten Card/Tape Reader Picture

Meet the new REDHEAD on your block for a buck! The MLED630 offers 1,100 fL typical brightness at 50 mA input current and a wide, 120° field of view. It's cased in the popular, TO-18 type package with a unique, molded plastic lens for durability and long-life, and . . . it's very low cost — only $1.00, 100-up. Use it compatibly with integrated circuits for low-drive current (200 fL typ @ 10 mA) data-read applications requiring high visibility, low drive power, fast response . . . and economy.

Tiny, Micro-T red LED shows big performance! For space-limited, panel and circuit condition indicators, punched card readers, light modulators, shaft or position encoders, optical switching and logic circuits you can't get a mightier light than this: 750 fL at 20 mils, or 330 fL at 10 mA. You also get nano-amp leakage, and a molded plastic lens for wide viewing angle plus easy insertion into PC boards and custom designs. It's the MLED 50 . . . a 6,600 angstrom Atlas in a pinhead package!

Do invisible things with 9,000 A, infra-red LEDs! Narrow beam light emission is the keynote of these two new plastic infra-red LEDs — MLED60/90 — lensed for high, on-axis power output (either 550 or 350 μW (typ) at 50 mA input) providing a greater signal to coupled silicon detectors.

Our Micro-T size equals your high density application need.

Turn red reliably with a tiny LED pill! Only 50 mils turns the MLED610 up to 1,100 fL brightness — high enough for most designs requiring metal-package reliability for high density mounting — PC boards, for example, that demand the ultimate in shock, thermal and moisture resistance.

It's the only red LED in the tiny rugged "pill" — use it in space-limited designs that need exacting, IC-compatibility. And use it in custom arrays where your need is close-tolerance spacing.

The gallium-arsenide-phosphide die is passivated for more reliability. **Turn red today.**

LED	PERFORMANCE ADVANTAGE	PRICE 100-Up
MLED50	Low-cost, subminiature plastic red LED for space-limited designs	70¢
MLED60/90	Narrow-beam, infra-red LED with 2 power output choices	$1.15/1.00
MLED610	Unique red LED in pill package with IC-compatibility	$2.60
MLED630	Low-cost, TO-18 with high brightness, 120° field-of-view	$1.00

For details, circle No. 461

LATEST COMPUTER-RELATED APPLICATION NOTES

AN-519 — USING MDTL LOGIC BLOCKS — Typical applications of MDTL gates and flip-flops, with emphasis on the positive logic AND, OR, NOR, NAND, and Exclusive-OR functions. Methods of interfacing MDTL with other popular logic families are also discussed.

AN-528 — BINARY-TO-BCD AND BCD-TO-BINARY CONVERSION WITH COMPLEX IC FUNCTIONS — Complex function integrated circuits reduce the cost of performing conversion from binary to the BCD code or from the BCD code to binary. Four methods of performing each conversion are discussed and compared.

AN-530 — THE MC7491A EIGHT-BIT SERIAL SHIFT REGISTER AND THE MC7495 FOUR-BIT SHIFT REGISTER — Operation of the MC5491A/7491A 8-bit shift register and the MC5495/7495 4-bit universal shift register are discussed. The use of the two devices in a data transmission system is illustrated.

AN-533 — SEMICONDUCTORS FOR PLATED-WIRE MEMORIES — An introduction to the operation and electrical characteristics of plated-wire memories with discussion of memory interface devices—including drivers, sense amplifiers and decoders and related plated-wire applications.

AN-536 — MICRO-T PACKAGED TRANSISTORS FOR HIGH SPEED LOGIC SYSTEMS — For specialized needs such as extremely high speed with minimum power dissipation, or unusual logic functions, discrete transistors in the ultra-small Micro-T package may prove advantageous.

AN-538 — MOTOROLA COMPLEMENTARY MOS IC's — The properties of N-channel and P-channel MOSFETs and how they are used to construct complementary MOS integrated circuits. Some MCMOS logic functions are discussed, and the design of a MCMOS programmable binary up-counter is given.

AN-539 — INTERFACING WITH MOS IC's — The problem of interfacing MOS integrated circuits with the logic levels of MECL, MDTL, MTTL and MRTL. Emphasis is placed on the use of other integrated circuits to achieve this interfacing.

LITERATURE REQUEST FORM

NOTICE: Requests for literature on items described in New Semiconductors for COMPUTER SYSTEMS cannot be honored after Oct. 15, 1971.

Please circle the Reader Service number for item(s) you wish to receive:

451 452 453 454 455 456 457
458 459 460 461 462 463 464 465

List below the numbers of the Applications Notes desired:

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New Semiconductors for **COMPUTER SYSTEMS**

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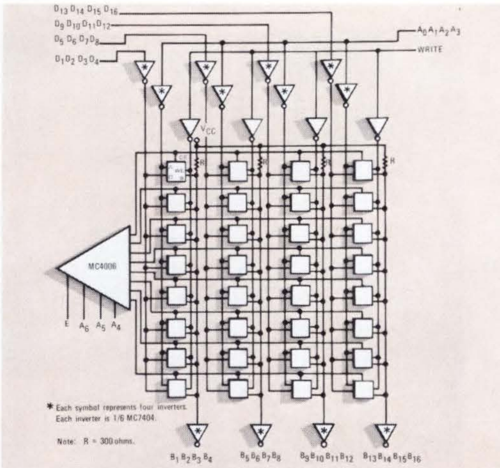
MCM4064 64-Bit RAM Offers High-Speed System Capabilities

Computer designers looking for speed advantages have a new ally in the MCM4064L 64-Bit Random Access Memory. Organized as a 16-word by 4-bit array, the MCM4064L utilizes Schottky-diode-clamped transistors to obtain fast switching speeds. Minimum access time is 15 ns and maximum is specified at 60 ns.

Address decoding is incorporated in the MCM4064L and provides 1-of-16 decoding from the four address lines. Separate data in and data out lines, together with a Chip Enable input, provide for easy expansion of memory capacity. A Write Enable control enters data presented to the data lines in the addressed storage cells. When writing, the data out level is the complement of data in.



128-WORD BY 16-BIT HIGH SPEED BUFFER MEMORY

128 × 16-Bit Memory Cycles in 85 Nanoseconds

Let's take a look at a typical system using TTL logic and the MCM-4064 as a main frame store of 128-words by 16-bits. The following devices are required:

32 MCM4064	64-bit memories
1 MC4006	1 of 8 decoder
9 MC7404	Hex inverters

To directly address the 128 words of memory in this system would require seven address inputs. Since the MCM4064 basic building block has but four, the Chip Enable control is used along with an auxiliary device to accomplish the full seven bit addressing needed.

Address lines A0 through A3 are each brought to all memory devices in address drivers using a TTL fan-out of 8. In the diagram, each inverter/driver represents four, one for each bit A0 through A3. Thus sixteen inverters are required for the address lines. The same scheme is used to represent the data input and output buffers. The four address bits A0 through A3 are common to each memory device in the system and are used to address the corresponding word in each MCM4064.

The necessary address expansion is achieved by connecting the Chip Enable inputs of each device in a row, treating the system as an 8 row by 4 column array, and driving the 8 row lines with a 1 of 8 decoder (MC4006). This method provides the three additional word address inputs required.

The output bit lines in each column are wire-ORed because the devices chosen by the Chip Enable signal are dominant. Lines B1 through B4 in the left-most column are brought out to 4 inverter/buffers as are the four data lines of the other three columns.

Other organizations can be used but in wire-ORing MCM4064L outputs, eight was chosen as an optimum trade-off of decreasing decoding versus increasing access time because of output capacitance. The eight outputs at 8.0 pF each, plus an average of 5.0 pF for board capacitance give a total of slightly more than 100 pF for a total system access time of less than 100 ns typical. Interestingly, cycle time is less than 85 ns typical.

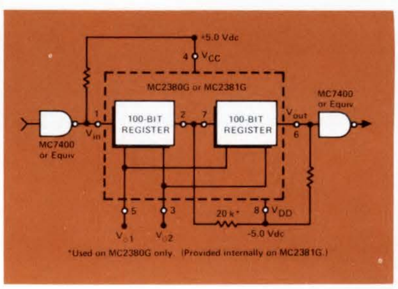
Data is written into the memory by selecting one memory device in each row with the Chip Enable as was done for the read operation.

Further details on the MCM4064 and a 512-word by 8-bit memory are given on the data sheet. The MCM4064L is available in the 16-pin dual in-line ceramic package and its 100-up price is $11.55. For evaluation samples call your local Motorola distributor.

For details, circle No. 462

Low-Power Dual 100-Bit Silicon Gate Registers Interface With Bipolar Logic

Silicon Gate MOS offers far more than the manufacturer advantages of simplified fabrication and improved yields. It provides the significant user benefits of direct bipolar interfacing, lower power requirements and ultimate space requirement reduction per system. When you accept these facts as Motorola most emphatically has, the only question remaining is where to start with standard product.

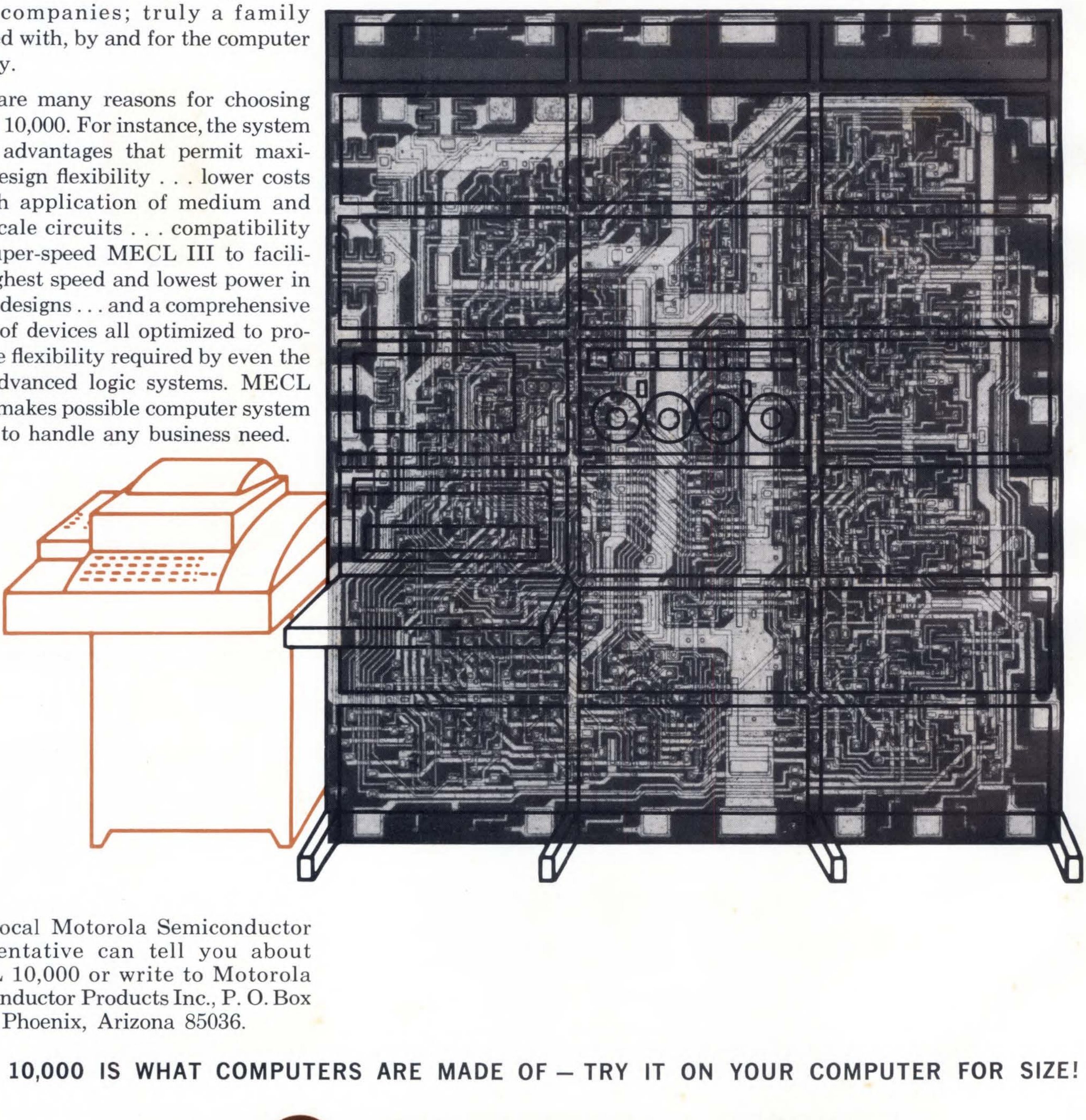


The MC2380G and MC2381G, two variations of a dual 100-bit dynamic shift register, were chosen as the harbingers of Motorola's Silicon Gate MOS product because of the flexibility and general popularity of the dual 100-bit organization in sequential digital applications. Both devices provide bipolar compatibility at inputs and outputs and both utilize low-voltage circuitry and a two-phase clock for minimum power dissipation. The MC-2380G has open-drain outputs for high drive capability and the MC2381G achieves direct MOS output compatibility with a pulldown resistor on the output.

Performance features include 3 MHz operating frequency, 0.4 mW/bit power dissipation @ 1.0 MHz (typ), operating temperature range of −55°C to +125°C, 40 pF clock input capacitance, and typical output impedance of 400 ohms.

Quad 256, dual 512, and 1024-bit dynamic shift register types are all set to join these first Motorola silicon gate shift registers with formal introductions and availability soon. Dual 250 and dual 256-bit silicon gate static shift registers are approaching the introductory stage. Watch for announcements throughout the balance of 1971. Meantime — contact your nearest Motorola distributor where the 100-up price is $3.95 for either device.

For details, circle No. 463



high-speed translators simplify ECL/TTL interface

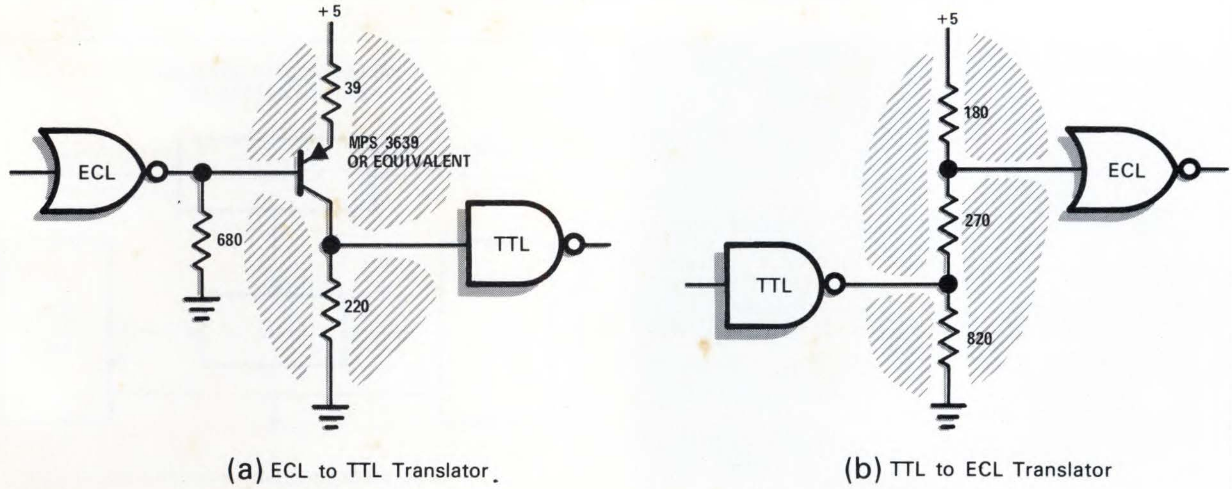
Two high-speed ECL/TTL translators, built with inexpensive discrete components, permit operation of both logic families from a common 5V supply.

As system speeds increase, it becomes desirable to take advantage of the low-propagation delays and fast toggle rates of the emitter-coupled logic (ECL) circuits. However, the designer often faces the dilemma of interfacing saturated logic levels with ECL levels. Existing integrated circuit translators require different power supplies for the ECL and TTL circuits. The circuits shown permit operation of both families from a common supply.

For ECL-to-TTL conversion (circuit (a)), a high-speed pnp switching transistor is connected as a low gain amplifier. The 39Ω resistor biases the transistor around the ECL output levels. Propagation delay for the translator shown in (**a**) is <5 nsec and is dependent on the speed of the transistor. Fanout is limited to two if speed and noise immunity are to be retained.

Propagation delay of the TTL-to-ECL translator (**b**) is limited by the stray capacitance within the circuit. With compact packaging, delay times are <2 nsec. Fanouts of 10 are possible with high input impedance ECL circuits. When using ECL with 2 kΩ input resistors, fanout should be limited to one or adjust the translator resistor values to compensate for the input current. The translator may be used with both active pull-up and open collector TTL. ➔

Bill Blood is a computer applications engineer for Motorola Inc., Semiconductor Products Div., in Phoenix, Ariz. Bill previously worked for R. J. Communication Products, Inc. and Motorola Control Systems Div. He received a B.S.E.E. from the University of Florida.



(a) ECL to TTL Translator.

(b) TTL to ECL Translator

walking-bit generator tests semiconductor memories

A popular test pattern for semiconductor memories has become known as a "Walking-Bit Pattern". This pattern has the property that during any pass through the memory, the pattern length matches the memory length.

A search for a worst-case pattern for semiconductor memories has been underway for some time. A number of people have proposed the "Walking-Bit Pattern" which has the characteristics that make the isolation of decoder faults (single or multiple), as opposed to memory cell faults, extremely easy. Because of the long test times encountered, it may be impractical to employ this pattern in a high volume production environment. However, it is a very valuable tool for laboratory analysis, especially during the troubleshooting phase of device evaluation.

The Pattern The "Walking-Bit Pattern" is characterized by a single bit of information (**1** or **0**) contained in a field of opposite information characters (**0**s or **1**s). This bit is cycled through the memory until every cell has been tested. For example, a 256-bit memory would be exercised as follows:

1. The memory is loaded with **0**s except for cell number 1 which contains a **1**.
2. The memory is read.
3. The memory is loaded with **0**s except for cell number 2 which contains a **1**.
4. The memory is read.
5. Repeat steps 1 to 4 until cell number 256 has been tested.
6. Repeat the entire process, however, interchange **1** and **0**.

This sequence is illustrated in **Fig. 1**. To completely exercise the memory, 1024 passes are required. If the cycle time is 1 μsec, the test time will be approximately 1/4 sec. As memory size increases, this time will increase accordingly.

The Generator A block diagram of the generator (designed and built at Intel) is shown in **Fig. 2**, with a complete functional logic diagram shown in **Fig. 3**. A description of the operation of the generator follows:

The outputs of two 12-bit binary counters are compared. When they match, the comparator generates a **1**. The bit counter is clocked at the address rate of the memory under test, while the pass counter is incremented once after the bit counter has gone through two passes (the memory is loaded during the first pass and

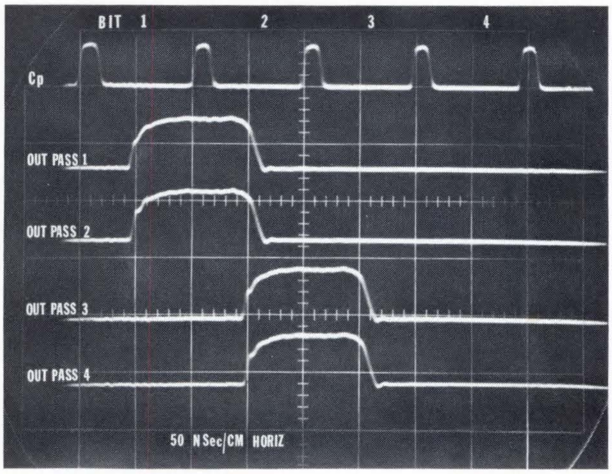


Fig. 1—**Oscilloscope** presentation illustrates "Walking-Bit Pattern" sequence.

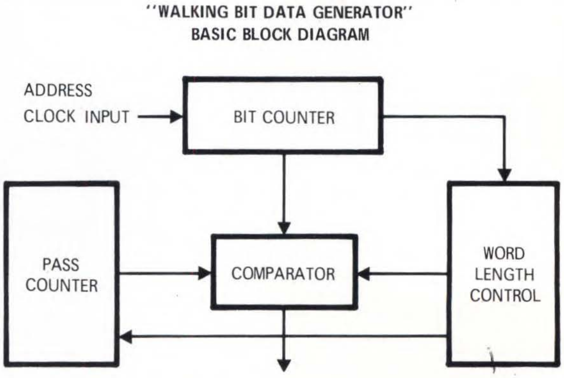


Fig. 2—**Basic block diagram** shows the signal flow of the "Walking-Bit Generator" shown in Fig. 3.

read out during the second). Only one match will exist per pass so it can be seen that the pattern produced will be the "Walking-Bit Pattern" described above.

The length of the bit counter is variable between 8 and 12 stages. This allows for word lengths from 256 to 4096 bits in binary increments. The word length control is accomplished manually through a 4-deck, 2-pole, 6-position rotary switch that can be mounted on the front panel.

The output of the comparator (**A**) is wired to an AND-OR-INVERT gate that permits automatic complementing of the data. Thus after a **1** has been completely "walked" through the memory, the data is complemented and a **0** is "walked" through. Output of the AND-OR-INVERT gate (**B**) goes to a noninverting driver that is capable of driving coaxial cable terminated in 50Ω (**Fig. 4**).

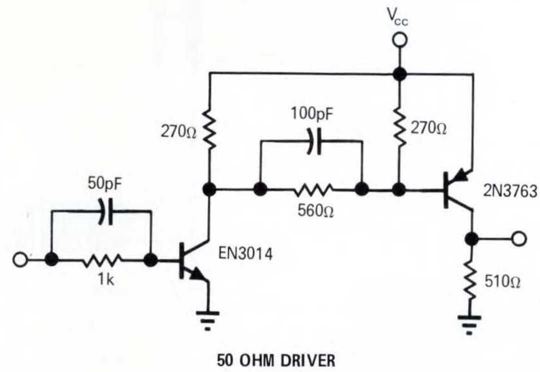


Fig. 4—**This noninverting driver** interfaces the AND-OR-INVERT gate output with a coaxial cable terminated in 50Ω.

CHARACTERISTICS OF THE "WALKING BIT GENERATOR" (Fig. 3)	
DATA OUTPUT: NRZ Format	**CLOCK AND RESET INPUTS:**
LOGIC '1' = +4.5V	MAX FREQ = 10 MHz
LOGIC '0' = 0.0V	POSITIVE GOING PULSE—TTL COMPATIBLE
OUTPUT Z = 50Ω	
MAX FREQ = 10MHz	PULSE WIDTH = 25 to 400 nsec
MIN FREQ = DC	RISE/FALL TIME = 100 nsec (max)
WORD LENGTH: (Variable) 256, 512, 1024, 2048, 4096 bits	
POWER REQUIREMENTS: +5V dc at 1-1/2A	

Coauthors **Joel Karp** and **Paul Metrovich** are employed by Intel Corp, Mountain View, Calif. Joel, a member of IEEE, is an MOS design engineer and he has project responsibility for a RAM exerciser. Paul's responsibilities include the design and building of test equipment for semiconductor memories.

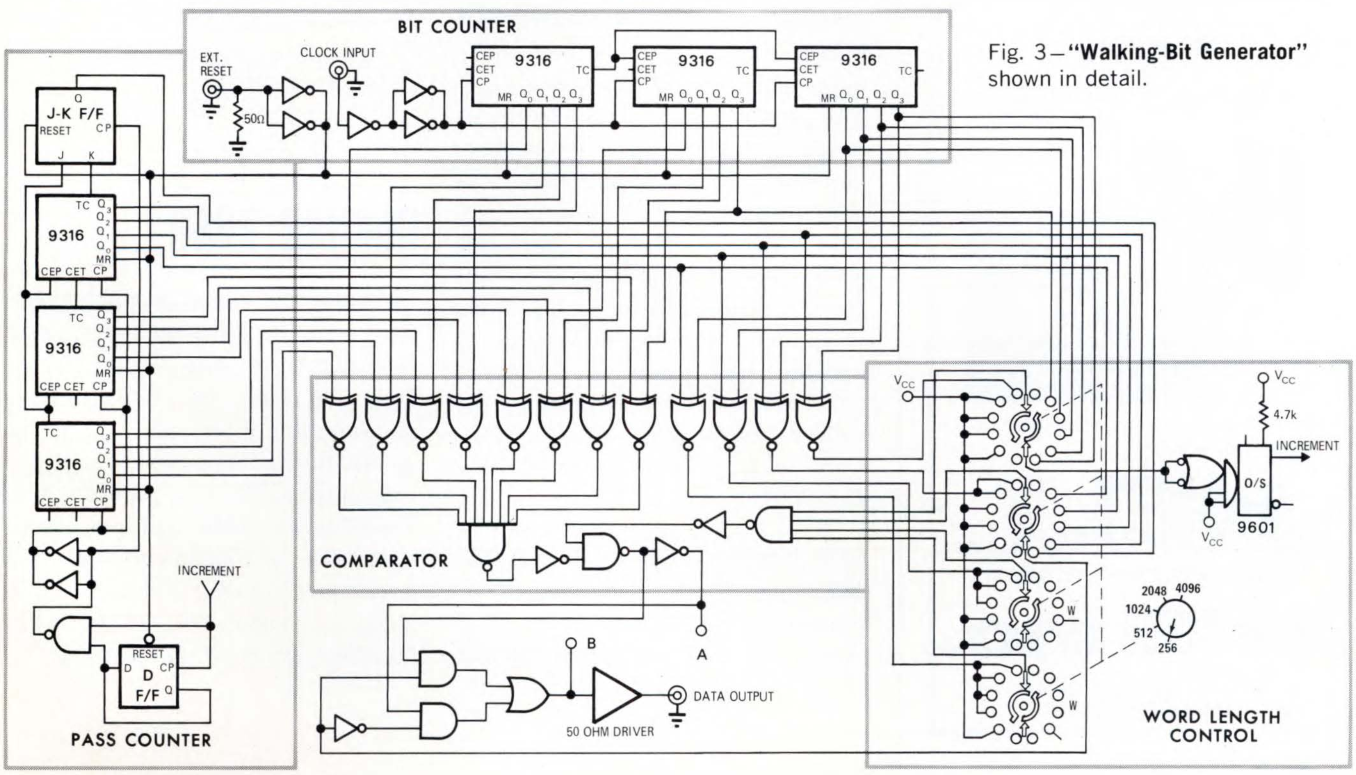


Fig. 3—**"Walking-Bit Generator"** shown in detail.

coming courses...

EVALUATION AND ANALYSIS OF TIME-SHARING SYSTEMS, New York, N.Y., August 11-13, Washington, D. C., September 20-22. This course is for management and technical personnel involved with the selection of time-sharing systems. Course objective is to place each attendee in position to best evaluate: (1) a time-sharing service to meet his individual needs, (2) a time-sharing system to meet his company's requirements for providing internal and external time-sharing services, and (3) the problems associated with operating an in-house time-sharing service, from both a technical and financial point of view. For more information, contact: *REGISTRAR, The Institute of Advanced Technology, Control Data Corp., 5272 River Rd., Washington, D C 20016.*

ADVANCED EDP SYSTEMS DESIGN/TECHNIQUES, August 4-6, New York, N.Y., September 8-10, Washington, D. C. This seminar will discuss recent information processing development and concepts, and portray some new approaches to the solution of problems. Also, the latest information processing techniques will be surveyed with a discussion on how to develop them and the difficulties associated with their use. Contact: *REGISTRAR, The Institute for Advanced Technology, Control Data Corp., 5272 River Rd., Washington, D C 20016.*

DATA COMMUNICATIONS SYSTEMS SEMINAR, July 26-28, New York, N.Y., September 8-10, Washington, D. C. An introductory seminar for the individual preparing for on-line, real time or other system that involves data communications. It is designed as an overview to orient the potential user in system design aspects, hardware considerations and software organization. For more information contact: *REGISTRAR, The Institute for Advanced Technology, Control Data Corp., 5272 River Rd., Washington, D C 20016.*

MINICOMPUTERS: THEIR STRUCTURE, CHARACTERISTICS AND APPLICATIONS, July 26-30. With increasing frequency, small computers are being used in research, engineering and manufacturing. This course discusses the relevant characteristics and application techniques of these computers to scientists and engineers. Tuition is $250. For information contact: *Continuing Engineering Education, Chrysler Center—North Campus, The Univ. of Michigan, Ann Arbor, MI 48105.*

coming soon...

THE OPERATOR, ENGINEER AND MANAGEMENT INTERFACES WITH THE PROCESS CONTROL COMPUTER, August 3-6, Purdue Univ., Lafayette, Ind. The problems of man-machine interaction will be discussed during this symposium. Registration fee is $50. Proceedings will be available. For additional information write: *Div. of Conferences and Continuation Services, Purdue Univ., Memorial Center, Rm. 116, Lafayette, IN 47907, Phone (317) 749-2533.*

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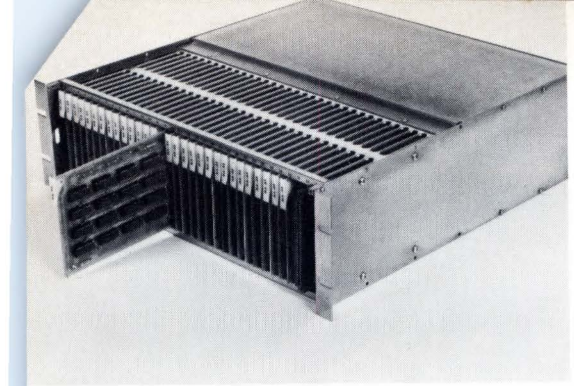

semiconductor memory systems offer low-cost flexibility

A family of low-cost general purpose semiconductor memory systems organized around a 1024-word by 1-bit dynamic storage cell has been developed by Monolithic Systems Corp., Englewood, Colo., for the individual desiring speed and flexibility. Designated Monostore III, these systems provide an excellent vehicle for minicomputer designers who need a readily available unit to test new organizational structures.

Monostore III is packaged in a 5.25- by 19- by 18-inch rack mount chassis. This unit provides up to 393,216 bits of storage and a self-contained power supply. The modular design of Monostore III permits economical expansion beginning at 1k words and extending to 65k words. Bit lengths (8 to 96 bits) can be arranged to meet the user's needs.

Four types of printed circuit boards make up the system – memory array, timing and control, address buffer and address register. Memory array cards (4.5 by 8 inches) have a storage capacity of 16,384 bits and can be organized as 1k × 4, 2k × 4 or 4k × 4 to form 1-, 2- or 4k word systems. These boards reduce spare parts cost and allow a minimum time for fault isolation. Systems of 8k and 16k are developed by paralleling (wired-OR) cards. A printed circuit power plane and wire-wrapped edge connector interconnect the cards. Signals to and from the unit are carried via twisted pair or coaxial cable terminated in characteristic impedance at the receiving end. Burndy MS type connectors are used and they allow twisted pair or coaxial leads to be carried through one pin location – an excellent interconnect medium between high-speed units and additional memory modules.

Systems built with multiple units use twisted pair or coaxial cable for communication between units and the system. When using a bus arrangement, the address (binary form) is strobed into the addressed module. Data may then be either strobed or entered as a level onto the bus. This is determined when the system is specified and the timing card is connected accordingly.

The 16-bit address register can act as a random set register or switch to a sequential mode of operation. In sequential mode, the control permits half, split or full cycle operation of the address register. For resetting the register to zero, a clear line is available. Upon request, an increment and decrement line can be made available for address control.

Normally access time is 450 nsec from receipt of a "read" command, and valid data output is indicated. However, the characteristics of dynamic semiconductor memory cells require a refresh cycle approximately every 2 msec. The refresh operation requires a 650 nsec read cycle. Monostore III delays the access time if a "read" command is coincident with the refresh operation. If the refresh cycle is in process, the "read" command is accepted and then processed upon completion of the refresh cycle. As a result, the read access for a 650 nsec operation is extended less than 1% on the average.

To load a word requires 650 nsec from receipt of "write command". However, as in the case of a read, if a refresh cycle is in process, the write operation may require up to 1 μsec. This occurs <1% of the time and does not significantly affect the average write time. Special handling of the refresh technique makes systems with no refresh delay available.

A built-in addressing capability permits up to 64k words to be addressed. Four units tied to a common address, data and command bus provide addressing up to 64k × 24.

Three modes of operation are available – full cycle, split cycle and read-modify-write. In full cycle, a read or write cycle is initiated by a read or write command, respectively. During the read cycle, a data register holds the output data until the next read or write cycle. For split cycle operation, the cycle complete pulse appears only on the write cycle. In the read-modify-write mode, the memory performs a read operation in 450 nsec and allows a modify time that is equal to the width of the data available pulse. The data is written back in the last 100 nsec of the cycle. The old data is then in the data register and the new data is stored in memory. A 650-nsec read-modify-write cycle has an access time of 450 nsec with a 50-nsec modify time.

Input signals are TTL compatible. All input lines are terminated at the memory with a 330Ω resistor to ground and a 270Ω resistor to 5V dc. Required rise and fall times for the read and write commands is 15 nsec. Write and read command pulses (both negative giving signals) require 70 nsec minimum duration, 200 nsec maximum. Power requirement for the 35-lb unit is 115/230V ac ±10%, single phase, 48 to 63 Hz. The unit weighs 25 lb without the power supply and requires +5V dc and +19.5V dc. Battery back-up is available for use in real-time or where nonvolatility is required.

The Monostore III is available off the shelf for 2.5 cents/bit in quantity. Complete system price is expected to be significantly less than 2 cents/bit in 1972. Monolithic Systems Corp., 2700 S. Shoshone St., Englewood, CO 80110. **420**

feature products

computer interface for programmable instruments

A new computer interface package drives programmable waveform generators and other programmable instruments.

Model 67 interface package includes an interface card compatible with Hewlett-Packard and Raytheon computers, cable, connectors and softwear (paper tape), everything required to operate the system. It will work with programmable instruments that take information from the computer such as signal generators but not with instruments that feed information back into the computer.

Model 67 interface functions simply by putting a statement in the calling program for the desired frequency, waveform, and a control word that sets amplitude, triggering, gating, dc offset and phase.

Price of the Model 67 interface package is $445 including software to drive the Models 605 and 606. Stock delivery. Exact Electronics, Inc., Box 160, Hillsboro, OR 97123.
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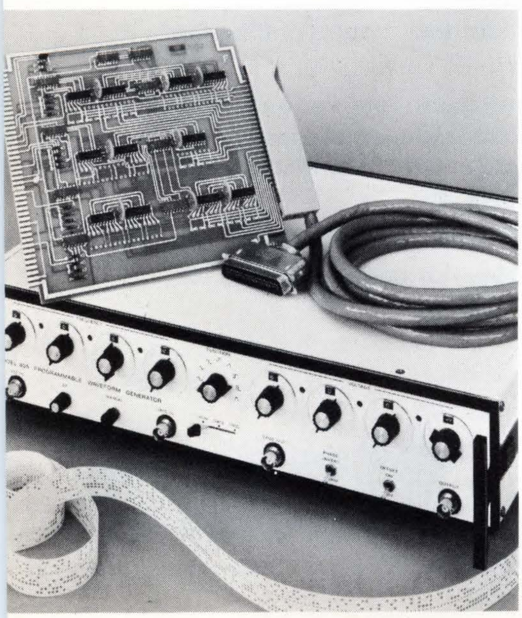

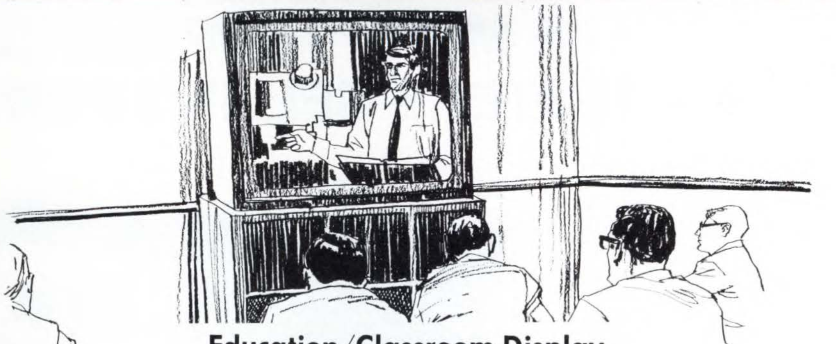

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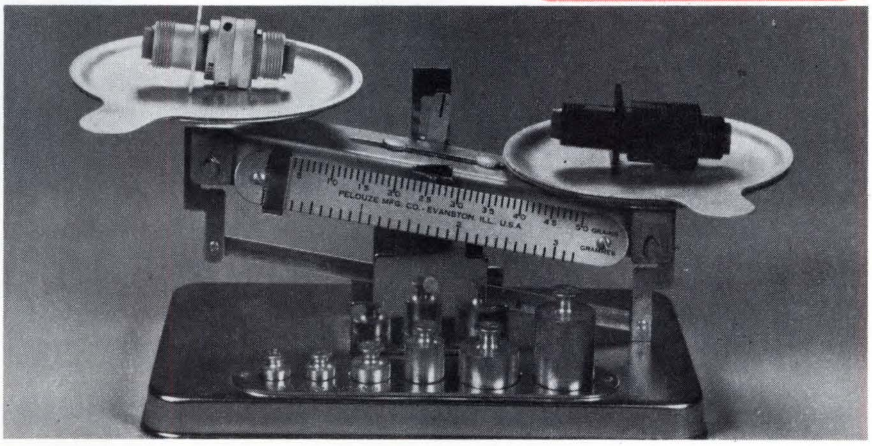
Amphenol introduces rear-release challenger

PROGRESS IN CONNECTORS

A new line of general-purpose circular multiconductor connectors from Bunker-Ramo's Amphenol Connector Div. may help the company to acquire a share of the rear-release market comparable to it's existing share of the front-release market. Among the many important competitive advantages claimed for Amphenol's new Merlin I series are reduced weight, size and cost—all resulting from a simplified mechanical design.

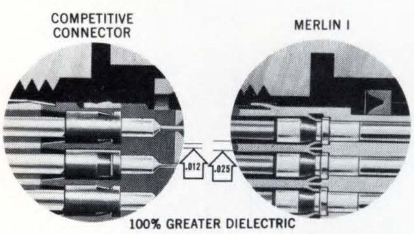


Amphenol's new Merlin I connector (in the left pan of the scale) is lighter and shorter than a typical competing connector (in the right pan).

Latecomer in rear-release

Amphenol's decision to introduce a line of rear-release connectors at this late stage of the game is somewhat surprising. For years Amphenol has placed major emphasis on front-release connectors, thus allowing the bulk of the rear-release market to go to competing companies such as ITT Cannon and Deutsch.

Recent events, however, have changed the market situation. The Navy has now issued a revision to its MIL-C-26482 specification for high-contact-density connectors. The new revision F to the military spec embraces a high-temperature, rear-release, design (NAS1599) which the Navy had originally refused to accept when the industrial spec was first introduced in 1963. Both the Air Force and the Navy have released design specifications on a new connector that will intermate



Most rear-release connectors (left-hand cross section) include metal contact-retention clips which occupy valuable space, thus allowing little room for a dielectric wall between conductors. The Merlin I (right-hand cross section) has a special plastic disk with molded contact retainers, thus allowing a thicker dielectric wall.

with existing MIL-C-26482/NAS1599 connectors. Also, new international specs have been issued covering the same basic design in England, France and Germany, making it apparent that the NAS1599 style will become a European standard.

Because of its increasing acceptance by various standards authorities, the NAS-1599-style connector is growing in popularity. In this country, the airframes for the F-105 retrofit, the S3A and the F-15 are all scheduled to use the connectors. Overseas, the connectors will be used for the MRCA, Concorde, Viggen and Harrier.

Last but not least

Amphenol's decision to introduce the Merlin I series was prompted by the growing market acceptance of rear-release connectors. But, though it's fully compatible with existing MIL-C-26482/NAS1599 connectors, the Merlin I isn't just a "me-too" item. Thanks to a special plastic contact-retention disk, the new connector doesn't need individual metal retention clips for each contact. The result is a connector that is inherently lighter (up to 40%) and more reliable than competing connectors. Though the Merlin I can intermate with other NAS1599 connectors and has the same mounting dimensions, it is physically shorter than other versions.

The retention disk is made from the 3-M Company's Astrel 360—the same material that Amphenol uses in its popular MIL-C-81511 connectors. This material is stable up to 500°F and can easily meet the temperature requirements of MIL-C-26482, while retaining its strength, resilience and dimensional tolerances. The absence of individual retaining clips allowed the retention plate to be designed with thicker dielectric walls, thus minimizing outgassing and weight loss that can occur during prolonged exposure to high temperatures and high altitudes.

Eight popular versions

Initially Amphenol will produce the new connectors in eight configurations—which will meet 75% of current market requirements. These versions range from a size-10 shell with 6 contact positions to a size-24 shell with 61 contacts. Other configurations will be introduced soon.

Prices depend, of course, on the configuration and quantity ordered. Because of the simplified mechanical design, Amphenol's production costs are lower than those of companies whose connectors require individual retention clips. This will allow Amphenol to underbid other companies for large orders. For small quantities, Amphenol's prices will be roughly the same as those of competing companies, though the total cost to the user should be lower because of reduced assembly and repair costs. Amphenol Connector Div., Bunker-Ramo Corp., 2801 South 25th Ave., Broadview, IL 60153. **170**

Shirt-pocket DVM

PROGRESS IN INSTRUMENTATION

Soon an engineer will have to start wearing shirts with two pockets. He will need one pocket for the usual paraphernalia such as a slide rule (or, perhaps, an electronic calculator), logic probe, screwdrivers, trimming tools, pencils, etc. And he will need a second pocket for his digital voltmeter.

Kruger–Eckels (South Pasadena, Calif.) has introduced what is probably the first commercial pocket-sized DVM. But the Kruger–Eckels Model 20 isn't the smallest DVM on the market. Some existing digital panel meters are smaller (though one could argue that a DPM isn't really a DVM if it doesn't include range switching).

With a height of only 1.2 inches and a width of 3.2 inches, the Model 20 should fit most shirt pockets. But its length of 7.6 inches may cause a few engineers to bump their chins on it, and its weight of 1.1 lbs may ruin a few shirts. The manufacturer achieved the small height by using incandescent readouts–which have the advantage that they're brighter than LED's but the disadvantage that they're less rugged.

The Model 20 has a three-digit display and can measure voltages from 1 mV (999 mV FS) to 999V. It features autoranging (with decimal-point indication) and automatic polarity switching (with sign indication). Specified accuracy is 0.1% ±1 digit.

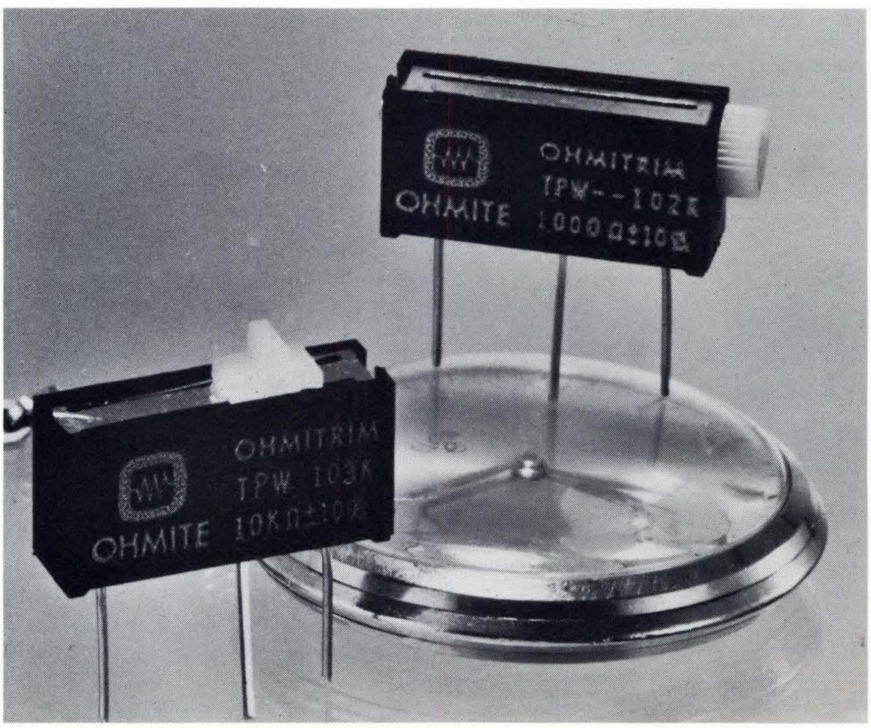
The unit's nickel-cadmium batteries allow 8 hrs of continuous operation without recharging. A plug-in power supply permits continuous operation from an ac line and also allows the internal batteries to be recharged overnight. When operated solely from its batteries, the unit is completely isolated from ground and, therefore, has excellent common-mode rejection. When powered from an ac line, its common-mode rejection is 100 dB. Its normal-mode rejection at 60 Hz is 60 dB. The Model 20's isolation from ground and its 10-MΩ input impedance make it especially useful in the medical field.

Of course, the Model 20 can be worn on the belt or hand-held instead of being carried in a pocket. Also, the pocket clip can be easily removed for stacking.

In unit quantity the DVM costs $750 complete with power supply. A plastic carrying case with belt strap is $32, a probe lead costs $7.50 and leads with hook clips are $8 a pair. Kruger–Eckels, Box 681, South Pasadena, CA 91030. **171**

Versatile trimmer pots for PC boards

PROGRESS IN POTENTIOMETERS

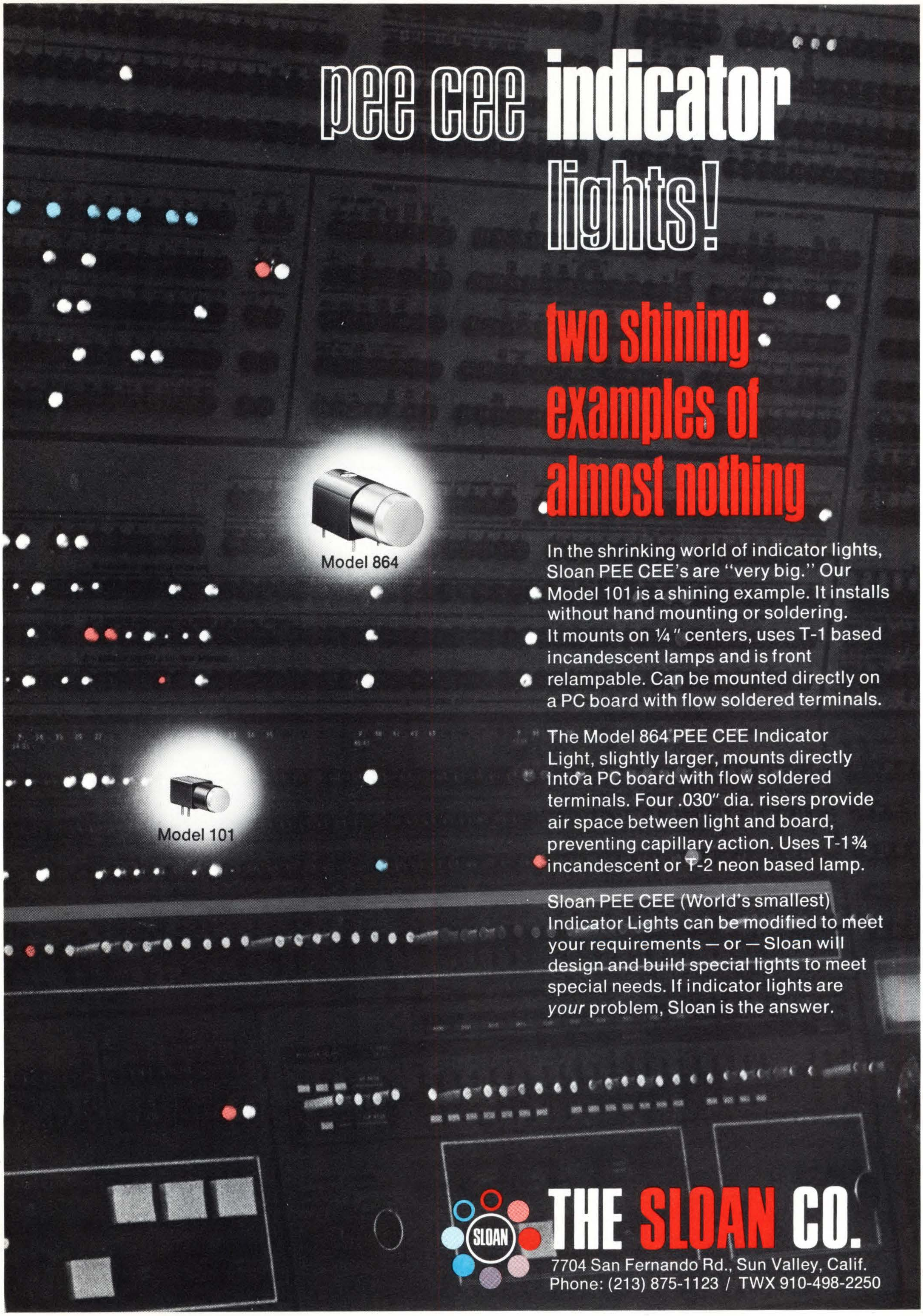


Wirewound trimmer potentiometers, models TPW-100 and TPS-100, have a nominal 1.0W rating and are offered in resistance values ranging from 10 to 20,000Ω. Leads are spaced on a 0.1-inch grid pattern for ready PC board insertion and are gold plated to facilitate soldering.

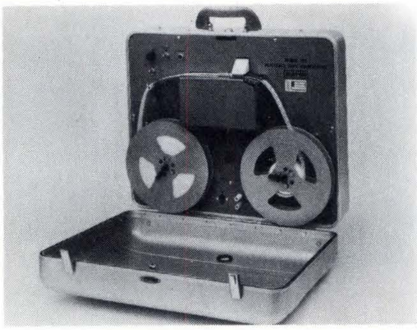
Model TPW-100 is lead-screw actuated (approximately 35 turns of the lead screw will cover the complete winding) and is designed to provide "clutching action" at either end of the winding.

Model TPS-100 is slide actuated. It permits fast, approximate placement of the slide actuator to a predetermined position.

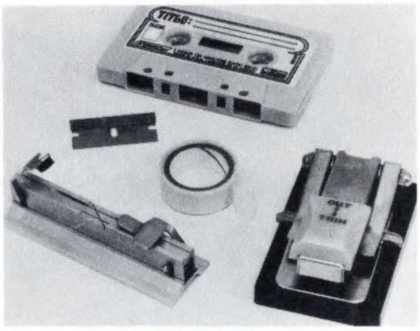
Lead-screw actuated model TPW-100 will meet the requirements outlined in EIA Standard RS-345, "Resistors, Variable, Wirewound (Lead Screw Actuated)" for characteristic "A". Slide actuated model TPS-100 will also meet the same requirements of EIA Standard RS-345, where applicable. Ohmite Mfg. Co., 3601 Howard St., Skokie, IL 60076. **172**


pee cee indicator lights!
two shining examples of almost nothing
Model 864
Model 101
In the shrinking world of indicator lights, Sloan PEE CEE's are "very big." Our Model 101 is a shining example. It installs without hand mounting or soldering. It mounts on ¼" centers, uses T-1 based incandescent lamps and is front relampable. Can be mounted directly on a PC board with flow soldered terminals.
The Model 864 PEE CEE Indicator Light, slightly larger, mounts directly into a PC board with flow soldered terminals. Four .030" dia. risers provide air space between light and board, preventing capillary action. Uses T-1¾ incandescent or T-2 neon based lamp.
Sloan PEE CEE (World's smallest) Indicator Lights can be modified to meet your requirements — or — Sloan will design and build special lights to meet special needs. If indicator lights are your problem, Sloan is the answer.
SLOAN
THE SLOAN CO.
7704 San Fernando Rd., Sun Valley, Calif.
Phone: (213) 875-1123 / TWX 910-498-2250

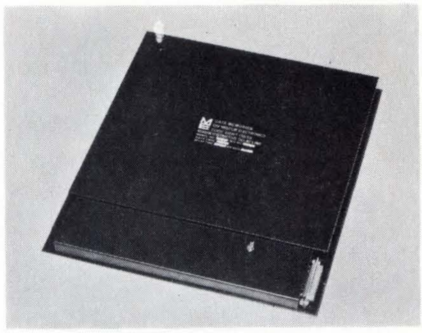
CIRCLE NO. 20



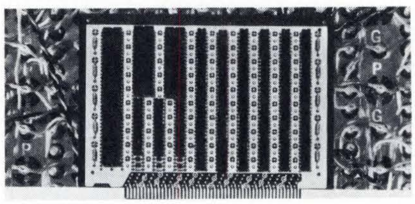
Portable tape perforator, Model 701, housed in a light-weight aluminum suitcase, requires only 48V dc power source and a 2-wire signal input. Model 701 converts 8-level, 11-bit code into an 8-level parallel form for driving 8 punch solenoids in sequence. Power is consumed only during punching. Conrac Corp., Alston Div., 1724 S. Mountain Ave., Duarte, CA 91010. **173**



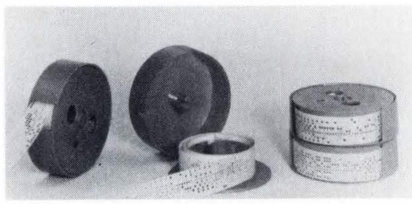
Cassette tape splicers handle 1/8-inch wide tape. Manual model 30-652, priced at $2.95, consists of a splicing block with felt-tipped tape hold-down clamps. A semi-automatic model 30-650 (priced at $4.95) has a built-in blade for diagonal cutting and an intergral pair of cutting blades for after splice trimming. GC Electronics Div., Hydrometals, Inc., 400 S. Wyman St., Rockford, IL 61101. **176**



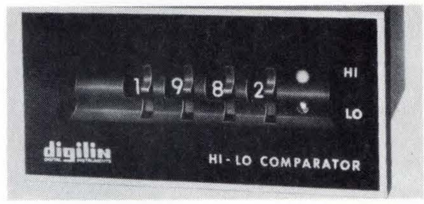
Magnetostrictive delay lines, 545 Series, have delay times of up to 10 msec with delay adjustment ranges of up to ±1 μsec. Delay adjustment ranges of up to ±4 μsec are available by special request. Units come complete with TTL compatible input/output circuitry. Storage capacity is 20,000 bits (2 MHz bit rate). Melcor Electronics Corp., 1750 New Hwy., Farmingdale, L.I., NY 11735. **179**



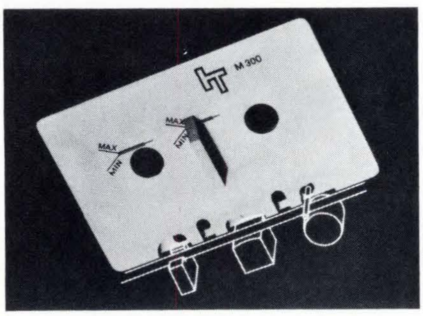
Logic board can be used for 100-MHz operation. To achieve maximum power and ground distribution, 95% of the board surface is covered with 2-oz copper. A unique interconnecting technique allows the user to package up to 50, 14-pin DIPs or any combination of 14-, 16-, 24- or 36-pin ICs on a single 5- by 7.5-inch board. Micro Technology, 5388 Sterling Center Dr., Westlake Village, CA 91361. **174**



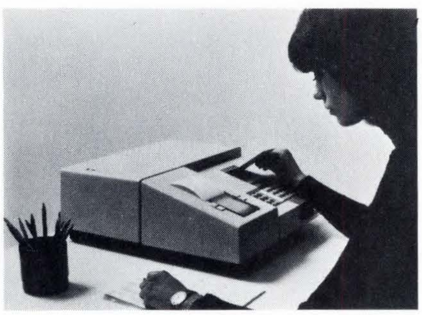
Paper tape winder/container, called Speedy-Reel, holds up to 125 ft of 1-inch computer tape. Operator simply pulls the unit apart, inserts the tape, snaps it shut and winds up the tape. Once inside, the reel becomes a container that protects the tape from damage. Unwinding is just as easy. Price is $2.98 per unit. Computer Accessories Corp., 211 New York Ave., Huntington, NY 11743. **177**



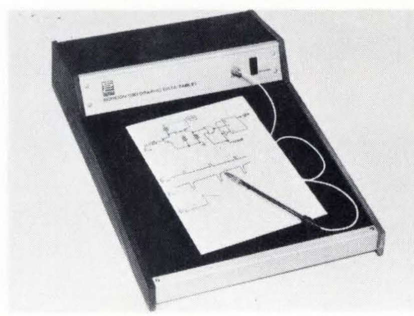
Limit set comparator, Type 2370, accepts DTL/TTL compatible BCD data from either a digital panel meter or other source. Continuous comparison is made on the preset level of the four thumbwheel switches. Front panel LEDs and rear panel logic indicate the input state – either high or low. Price is $125/unit. Digilin, Inc., 1007 Air Way, Glendale, CA 91201. **180**



Cassette head and guide gage M-300 permits cassette users to accurately position guides, heads and pinch rollers. The gage accurately locates the tape path with reference to the mid-point dimensions of all cassettes meeting ANSI, ECMA and audio standards. The device has graduation marks that indicate head insertion distance. Information Terminals Corp., 1160 Terra Bella Ave., Mountain View, CA 94040. **175**



Microcomputer P602 can be operated either in a manual mode as a calculator or in a program mode as a digital computer. Main memory consists of 16 registers, three of which are operating registers, four are program registers for 128-step program and nine for storage. The unit can be integrated into a sophisticated system through peripheral input/output units. Olivetti Corp. of America, 500 Park Ave., New York, NY 10022. **178**



Graphic data tablet, Model 520, operates on a newly patented principle and has a writing surface of 11-inch square (other sizes are available). Measuring 15-1/4 by 4-5/8 by 20-13/16 inches, the unit simultaneously generates both digital and analog signals of the pen's coordinates. Analog bandwidth is 20 Hz and digital outputs are 10-bits parallel for both X and Y. Shintron Co., Inc., 144 Rogers St., Cambridge, MA 02142. **181**

Instrument Specialties new inlay-overlay technique

improves contact reliability, preserves spring characteristics.

A new technique from Instrument Specialties, employing beryllium copper spring material inlaid or overlaid with precious metal alloys, solves many critical contact spring problems in a better, more economical way. You can improve surface conductivity at low voltage levels without electroplating. And, in high-current applications, you can obtain thicker contact sections without the added production cost of assembled contacts.

Using this technique, Instrument Specialties can also furnish springs with a stripe of non-solderable material, creating an effective solder barrier for fast, clean connections.

This cost-saving process can provide many combinations of precious metals with spring materials, either as individual springs or in convenient strip form.

In volume production, it could be your most economical way to combine superior contact characteristics with optimum spring performance. Or, depending upon your needs, an Instrument Specialties spring specialist may recommend one of our other proved techniques—Contips,® selective plating, riveted or welded contacts, etc.—to solve your problem. Write today for more information. There's no obligation. Address: Dept. EDN-64.

INSTRUMENT SPECIALTIES CO., INC.
Little Falls, New Jersey 07424
Phone 201-256-3500

CIRCLE NO. 27

Computer Products

Voltage monitoring unit, PowerGuard "B", is specifically for "brownouts" detection. A digital clock displays the time of erroneous condition and a light indicates the limit that was exceeded. International Data Terminals Inc., 2995 N. Dixie Hwy., Oakland Park, Fort Lauderdale, FL 33308. **182**

Core memory, Model 3600, accommodates more than 1000 bits/inch^3. Priced at <$0.20/bit, it offers 650- and 900-nsec cycle times in sizes ranging from 16,384 to 131,962, 36-bit words. Ampex Corp., 9937 W. Jefferson Blvd., Culver City, CA 90230. **183**

Photoelectric punched tape reader/spooler, TRS-8000, exhibits read rates up to 750 characters/sec and stop-on-character capability at all speeds. The 8-inch spooler accommodates up to 1200 ft of tape. Electronic Engineering Co. of California, 1441 E. Chestnut Ave., Santa Ana, CA 92701. **184**

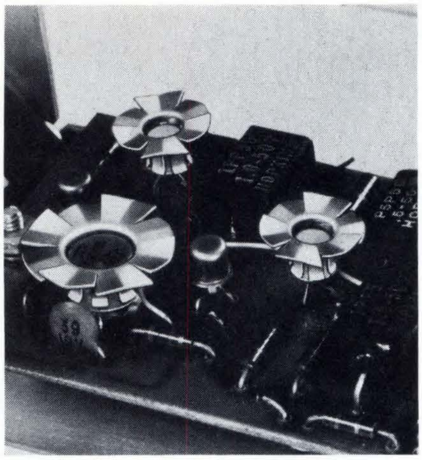
Two modems, Models 320 and 324, are 2000-bps and 2400-bps synchronous units, respectively. Type 320 is for unconditioned private lines and the 324 is for conditioned private lines. Astrocom Corp., 293 Commercial St., St. Paul, MN 55106. **185**

Add-on core memory 360/CORE is plug compatible with IBM System/360, Models 30, 40 and 50. Memory is expandable from 8192 to 524,000 bytes. Cambridge Memories, Inc. 285 Newtonville Ave., Newtonville, MA 02160. **186**

Digital cassette DC-630 uses fully certified 1/4-inch computer tape and operates at speeds >50 ips. Other features include bit densities of 1600 bpi and start/stop time of ≥15 msec. BASF Systems Inc., Crosby Dr., Bedford, MA 01730. **187**

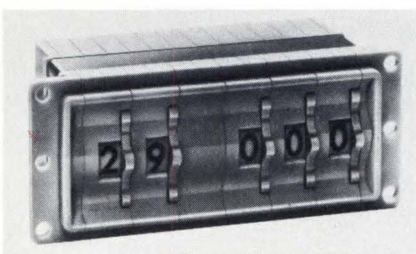
Photoelectric tape reader, type TRP500, has a reading rate of 0 to 500 cps. Tape handling is either loop type or fanfold with trays for up to 200 feet of tape. The Superior Electric Co., 83 Laurel St., Bristol, CT 06010. **188**

Disc drive 215, compatible with IBM 360 and 370, features two spindles/drawer and provides 116.7 million bytes of storage. California Computer Products, Inc., 2411 W. La Palma Ave., Anaheim, CA 92801. **189**

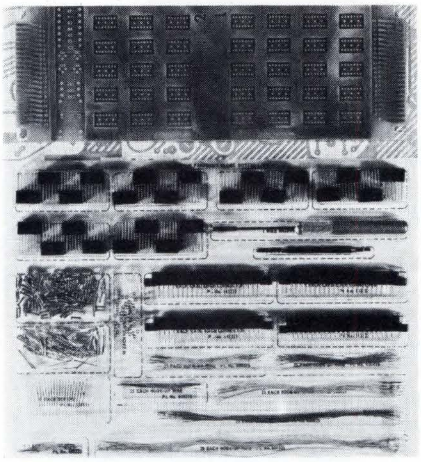


Heat dissipators for semiconductors are made of brass and priced from $0.04 each in OEM quantities. Models are available for TO-18, TO-5, TO-8 and TO-66 devices. These "fan-top" devices install without tools. IERC, 135 W. Magnolia Blvd., Burbank, CA 91504. **190**

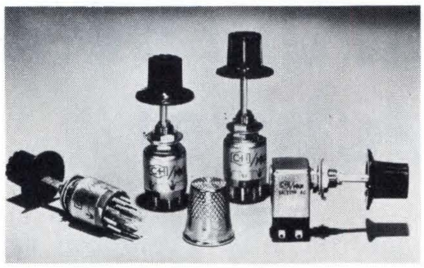
Sonic sensor cell operates with 5- to 10-mW excitation and has projected lifetime of 50 years. Six models are available with operating frequencies that range from 16 to 500 kHz. Prices are competitive with photoelectric applications. Instrumentation Div. of Gulton Industries, 1644 Whittier Ave., Costa Mesa, CA 92627. **191**



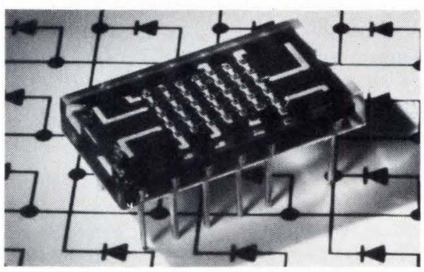
Thumbwheel switches of the 29000 Series have a 0.2-inch high character display and offer a selection of codes including BCD, BCO, BCD with complement, single-pole decimal and single-pole double-throw repeating. Prices fit a "rotary switch" budget. The Digitran Co., 855 S. Arroyo Pkwy., Pasadena, CA 91105. **192**



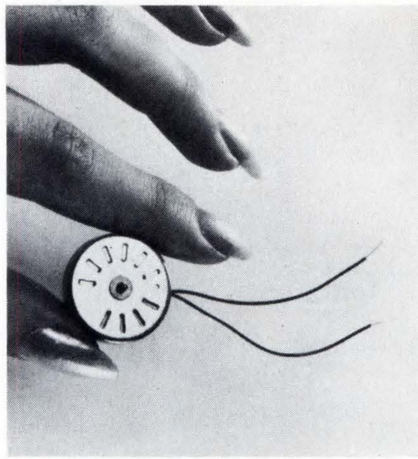
Breadboard kit for designing circuit prototypes uses "Wire-Wrap" connections and includes all necessary hardware components. The board material is 0.062-inch flame retardant G-10 material. Kit price is $148. HMW Enterprises, Inc., 15 Walnut St., Steelton, PA 17113. **193**



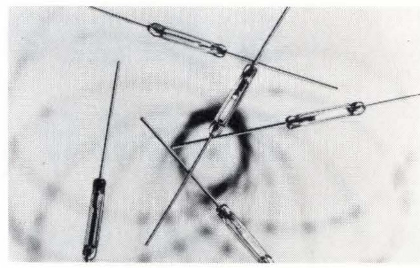
Rotary switches are thimble-sized and available in 1-, 2- and 4-pole configurations with a progressive "On" circuit arrangement and nonshorting, break before-make contacts. Rating is 2A, 125V ac for the 2- and 4-pole versions. Prices range from $4.45 list to $1.45 each in large quantities. Cutler-Hammer, Inc., 4201 N. 27th St., Milwaukee, WI 53216. **194**



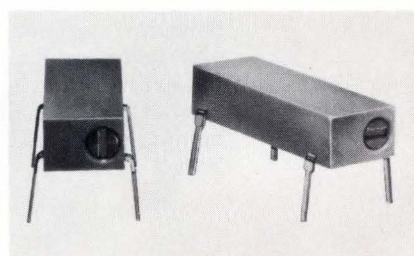
Five by seven matrix alphanumeric LED display, Model TIL305, provides 0.3-inch characters for a $10 per digit price tag in 1000 quantities. Photometric brightness is typically 300 fL at 10 mA. Texas Instruments Incorporated, Inquiry Answering Service, Box 5012, M/S 308, Dallas, TX 75222. **195**



Subminiature synchronous motor is only 1/4-inch thick by 7/8-inch diam. The Model AMY 6 contains a hardened shaft and sintered bronze bearings. Shaft speed is 300 rpm with 24V, 60 Hz, 0.3 VA input. Landis & Gyr, Inc., 4 Westchester Plaza, Elmsford, NY 10523. **196**



Reed switch with stable contact resistance and no contact bounce, Model MTHG-2, has operate time of 0.4 msec and operates in any position. Maximum ratings are 10V dc/0.1A with breakdown voltage of 500V dc minimum. A minute amount of captive mercury permits the bounceless contacting. Price is $2 each in 1000 lots. Hamlin, Inc., Lake Mills, WI 53551. **197**



Rectilinear dual-in-line trimmer, Series 125, has Cermet element. Units are 3/4-inch long, have 20-turn adjustment, are rated at 3/4W at 25°C and have sealed construction. Pin spacing is TO-116. Price is $1.66 each in 10,000 quantities (for standard ±20% tolerance). CTS of Berne, Inc., 406 Parr Rd., Berne, IN 46711. **198**

From 3M...

Flammability protection

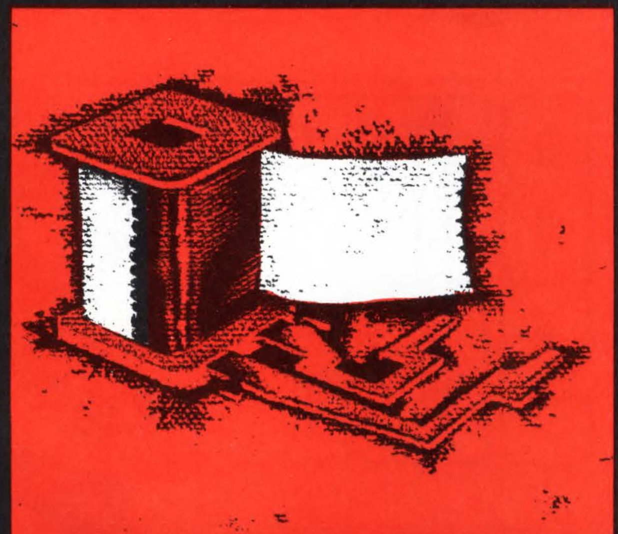
New flame retardant materials for insulation safety.

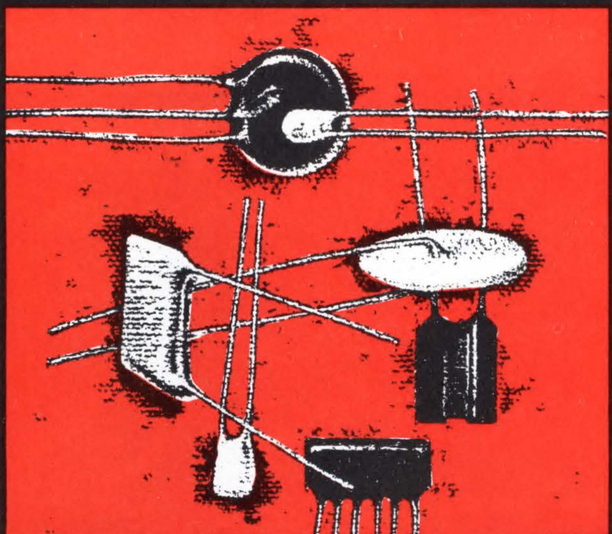
"SCOTCH" BRAND FLAME RETARDANT TAPE NO. X-1266.

Resin-fiber construction with flame-retardant pressure-sensitive thermosetting adhesive for 130°C use. Excellent conformability. Handles like conventional paper or acetate cloth tapes. Flame-out in 3 seconds or less (ASTM-D1000-70 test). Meets UL flame retardancy requirements for SE-O materials, as well as UL Standard 492.

"SCOTCHCAST" BRAND FLAME RETARDANT RESIN NO. XR-5217.

For radial and axial lead components — thermistors, resistors, RC networks, film foil, ceramic, tantalum, diced chip and mica capacitors. Suited for semi-automatic or automated production equipment. Coats at 300°-350°F. Fast cure time: 2 min. at 350° to 30 min. at 275°F. Meets flame retardancy requirements of UL Standard 492.





Check these other flame retardant materials.

"SCOTCH" BRAND TAPES.

No. 69 — glass cloth, thermosetting silicone adhesive.
No. 66 — vinyl, UL recognized 105°C meets MIL-1-7798-A.
No. X-1264 — epoxy web solvent-resistant wire and cable ID tape.
"Temflex" Brand No. 2585 — non-adhesive vinyl plastic, flexible, self-extinguishing.

"SCOTCHCAST" BRAND RESINS.

No. XR-5192 — arc and track-resistant 130°C, liquid epoxy.
No. XR-5126 — room-curing two-part epoxy, 130°C, semi-flexible.
No. 255 — thermal and mechanical shock-resistant, 130°C, meets MIL-1-16923E.

TUBINGS.

"3M" Brand 3001, 3002, 3003, 3008 — extruded vinyl, general purpose, 105°C rated.
"Scotchtite" No. 3028 — heat shrinkable, clear or colors, thin wall. UL recognized 105°C, meets MIL-1-631 and MIL-1-23053B.

COPPER CLAD.

"Cuflex" Brand Flexible Laminate 6540 — copper-clad epoxy polyester web for printed wiring.

MICA.

"Isomica" Brand — silicone bonded mica for high temperature use.

For complete information, write: 3M Co., DM&S Div., 224-64, St. Paul, Minn. 55101.

Dielectric Materials & Systems Division 3M COMPANY

CIRCLE NO. 31

Wideband transformers packaged in TO-5 and 1/3 DIP are available in both balanced and unbalanced types and with various impedances. Typical frequency range is 0.1 to 1000 MHz and typical power handling ability is 1W. The Vari-L Co., 3883 Monaco Pkwy., Denver, CO 80207. **199**

Copper-filled conductive resin system, the BLISS-BOND 300, replaces or complements conventional silver-based resin systems in many applications. It adheres to ceramics, metals, plastics and most other materials, and its viscosities can be varied by the user. Gulf+Western Industrial Products Co., R&D Center, 101 Chester Rd., Swarthmore, PA 19081. **200**

Tubular capacitor only 0.15-inch long by 0.055-inch in diam is offered from 100 pF through 0.012 μF with BX characteristics, ±15%ΔC over the temperature range of −55 through +125°C. Republic Electronics Corp., Dept. K, 176 E. 7th St., Paterson, N. J. 07524. **201**

Metallized ceramic boards of the IB Series use chrome-copper metallization to reduce cost and microwave loss. Standard sizes are 1 by 1, 2 by 2 and 1 by 2 inches. Film Microelectronics Inc., 17 A St., Highland Industrial Park, Burlington, MA 01803. **202**

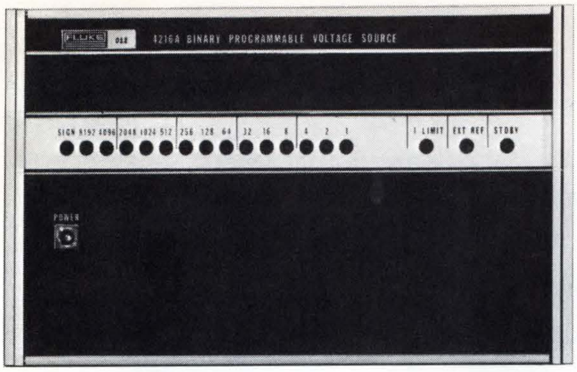
Optically-coupled isolator with 25,000V breakdown rating between input and output consists of a GaAs input diode driving a silicon photodetector. Several models are available for various transfer efficiency and speed requirements. Price is $10 each in single lots. Optron, Inc., 1201 Tappan Circle, Carrollton, TX 75006. **203**

Notched pot cores, Type RM, have square mounting configuration and consist of only five parts. First available in RM-6 (14 mm) size, they are offered in five different materials and with various gaps. Ferroxcube Corp., Saugerties, NY 12477. **204**

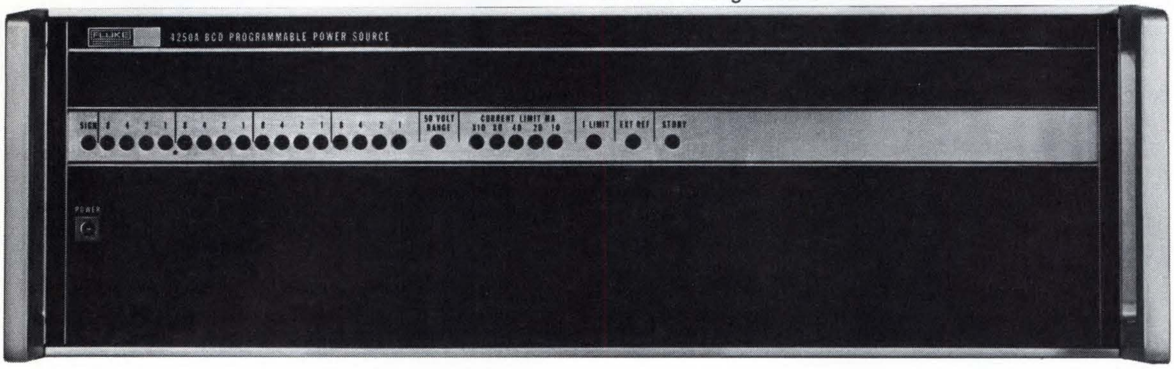
Heat gun provides three temperatures by using quick-change color-coded nozzles. Temperatures to 1200°F are produced. A shaded-pole brushless motor permits quiet, maintenance-free continuous operation. Ideal Industries, Inc., Sycamore, IL 60178. **205**

Ceramic feed-through capacitors in both round and square shapes with capacitance values to 5.5 μF are designed for ac/dc application in RFI/EMI filters. Versions are available with NPO, K500, K1700 and K4700 materials. Typical prices range from $0.75 to $2 in production quantities. The Potter Co., 500 W. Florence Ave., Inglewood, CA 90301. **206**

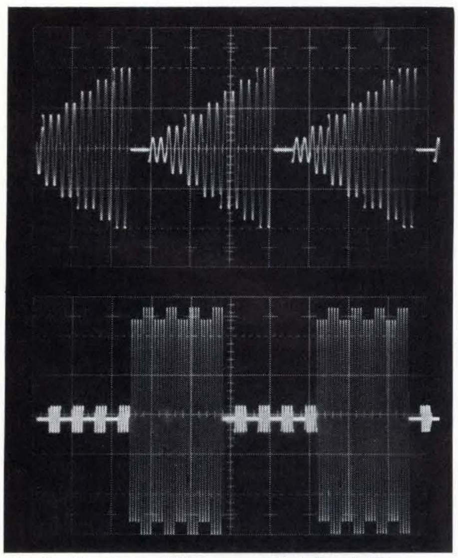
Reed relays, the sealed contact dry Model MRB, mount on 0.1- by 1-inch grid centers and offer typical response time of 200 to 650 μsec. Rating is for 10 million operations at 28V dc, 125 mA. C. P. Clare & Co., 3101 Pratt Ave., Chicago, IL 60645. **207**



Instrument photos show Model 4216A Binary Programmable Voltage Source in half-rack version at top and Model 4250A BCD Programmable Power Source in full rack configuration.



New Fluke programmable power sources put it all together. One instrument does the work of a whole rack of equipment.



An indication of the powerful flexibility of the Series 4200 can be inferred from the scope photos.

This family of systems instrumentation represents an entirely new approach to automatic test and process control equipment. They serve as husky power supplies, fast digital-to-analog converters, programmable attenuators, power amplifiers, and even dynamic loads.

Either BCD or binary programming with internal memory is offered. Accuracy is 0.01% throughout. All models feature dc or ac external reference capability programmable in or out, 50mv peak programming noise, isolated control logic to eliminate digital noise, and complete digital display.

Brief specs of the first four models:

	4210A	4216A	4250A	4265A
V_o	10v	16v	65v	
I_o	100ma		1a	
Settling Time	30μs		100 μs	
Basic Unit*	$995		$1295	

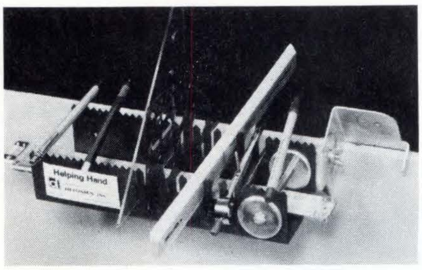
*Options extra

More data. Full data sheets and complete applications information are available from your Fluke Sales Engineer who will also be happy to arrange a demonstration at your convenience. Or you may address us directly if it's more convenient.

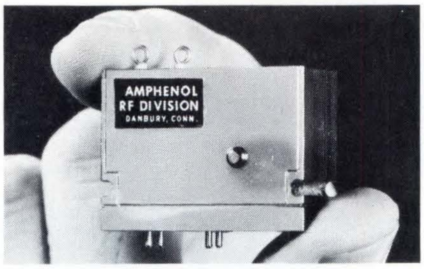
FLUKE®

Fluke, Box 7428, Seattle, Washington 98133. Phone: (206) 774-2211. TWX: 910-449-2850/ In Europe, address Fluke Nederland (N.V.), P.O. Box 5053, Tilburg, Holland. Phone: (04250) 70130. Telex: 884-50237 / In the U.K. address Fluke International Corp., Garnett Close, Watford, WD2 4TT. Phone: Watford, 27769. Telex: 934583.

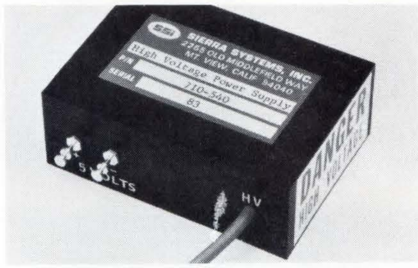
CIRCLE NO. 33



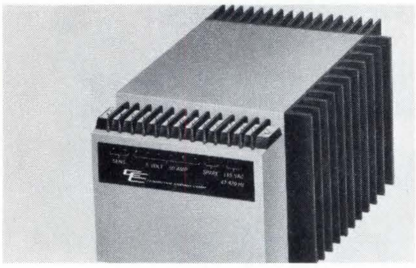
Instrument holder for tilted drafting boards, the "Helping Hand", holds drawing instruments at any board angle from horizontal to vertical with no rolling or sliding. Capacity is 17 instruments and price is $12.50. Devonics, Inc., Box 7158, San Diego, CA 92107. **208**



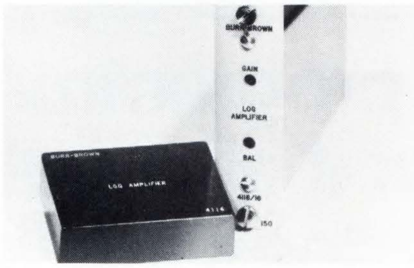
Microwave coaxial switches of the 303 Series are subminiature, perform through 6 GHz and handle up to 150W. Amphenol RF Div., The Bunker-Ramo Corp., 33 E. Franklin St., Danbury, CT 06810. **209**



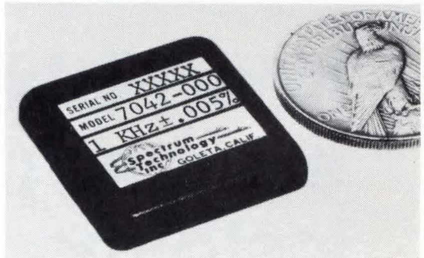
HV supply for CRTs, Series 710, operates from 5V dc input. Output voltages from 300 to 3000V with better than 1% regulation are available to provide up to 2 mA output. Price is $49 each in quantity. Sierra Systems, Inc., 2255 Old Middlefield Way, Mountain View, CA 94040. **210**



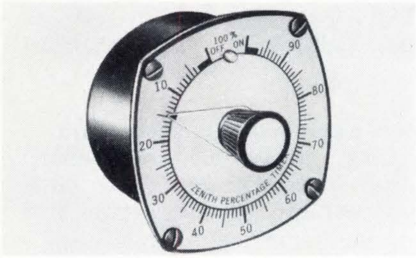
Power supply provides 5V at 50A in a 5- by 6- by 7-inch package. Combining 75% efficiency with freedom from RFI, the supply gives ±1% regulation (line and load), and recovers within 50 μsec from a 10A step load. Operating temperature range is −30 to +71°C and the price each is $525. Computer Energy Corp., 399 Smith St., Farmingdale, NY 11735. **211**



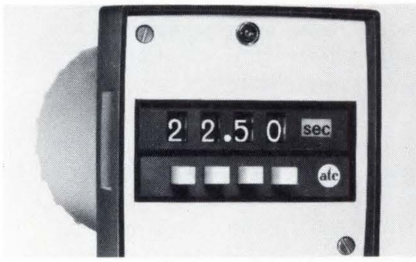
DC log amp, Model 4116, is capable of logging voltage over an 80-dB range and current over a 120-dB range. The output voltage is proportional to the logarithm of the input. Accuracy is ±1% over the ranges stated. Unit price is $95. Burr-Brown Research Corp., International Airport Industrial Park, Tucson, AZ 85706. **212**



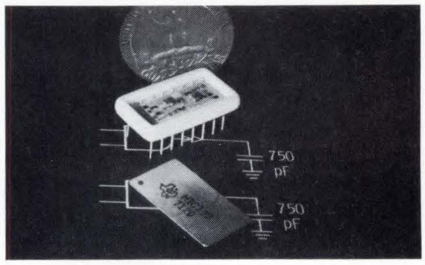
Crystal oscillator/logic clock is available at frequencies from 4 kHz to 20 MHz with ±10 PPM accuracy at 25°C. Temperature range is −55 to +125°C with stability of ±0.05%/°C. Output is +0.5V maximum (sink 5 mA) for logic "0" and +4V (source 1 mA) for logic "1". Case height for the Series 7042 unit is only 1/4 inch and size is 1.5 inch². Spectrum Technology, Inc., Box 948, Goleta, CA 93017. **213**



Percentage timers of the CP Series provide continuous ON-OFF cycling of electrical circuits where a percentage of the primary fixed total cycle time is necessary. Electrical rating is 15A, 250V (resistive load). Time ranges of 4, 15, 30 or 60 sec; 5, 15, 30 or 60 min; and 2, 6, 12 or 24 hrs are offered. Zenith Controls, Inc., 830 W. 40th St., Chicago, IL 60609. **214**

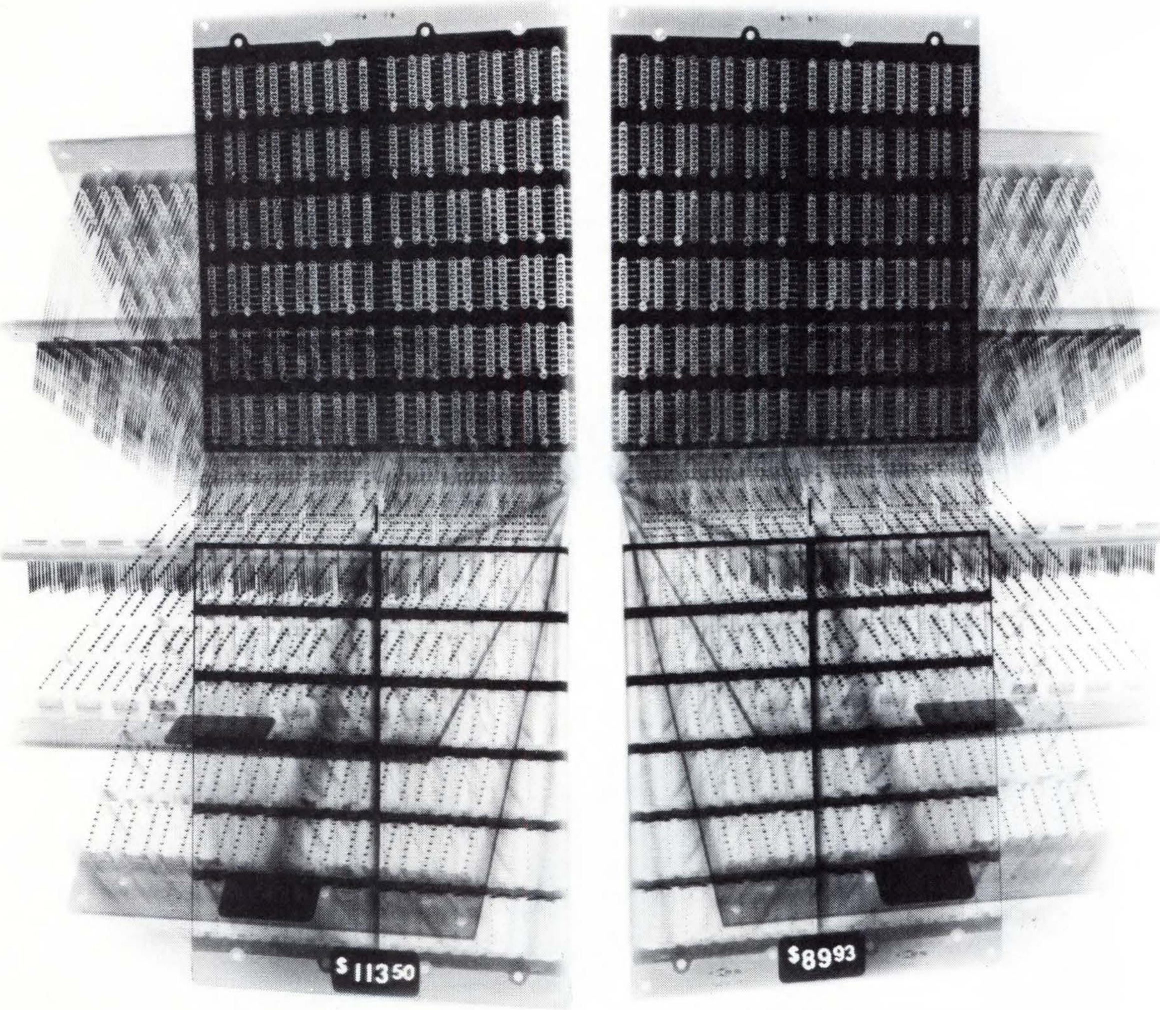


Solid-state timer, the all-digital Series 335, has 10-msec repeat accuracy on all settings from 1/100 sec to 1-2/3 hrs. Both DPDT instantaneous contacts and DPDT delayed contacts are provided. Available ranges are 99.99 min and 99.99 sec with settability to 0.6 sec and 0.01 sec, respectively. List price is $79. Automatic Timing & Controls, Inc., 201 S. Gulph Rd., King of Prussia, PA 19406. **215**



Hybrid IC dual MOS clock driver has 50 nsec or less switching speed into a 750-pF load. Model HIC138 is intended as an interface circuit between TTL logic levels and MOS logic levels. Standby power required is 30 mW/driver and supply voltages are +5 and −12V. Price of the 16-pin dual-in-line version is $21.30 in 100-piece lots. Texas Instruments Incorporated, Inquiry Answering Service, Box 5012, M/S 308, Dallas, TX 75222. **216**

Turn 'em upside down and they all look alike...



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Our new brochure details 70 of these models along with the competitive units that they replace. Our logic panels are 20% less. Our brochure is free. Write for it today.

STANFORD APPLIED ENGINEERING, 340 MARTIN AVE., SANTA CLARA, CAL. 95050 (408) 243-9200 TWX 910-338-0132

CIRCLE NO. 34

Circuits

Log video amplifiers have dynamic ranges in excess of 90 dB and video bandwidths >35 MHz. Twelve standard models are offered. Scientific Technology Inc., 655 Sky Way, San Carlos, CA 94070. **217**

Modular temperature controls of the "Action Pak 2000" Series are offered in two proportional control modes and with a self-contained triac power stack. Package size is 2 by 3 by 3 inches and prices range from $50. Action Instruments Co., 3928 Mt. Ainsworth Ave., San Diego, CA 92111. **218**

Time-proportional controller that fires at zero voltage has control accuracy to ±0.1°C. Model 72 requires 117V, 208V or 230V ac, 50/60 Hz at 15A maximum. Price is $60 for 115V operation and $62.50 for other voltages. RFL Industries, Inc., Boonton, N J 07005. **219**

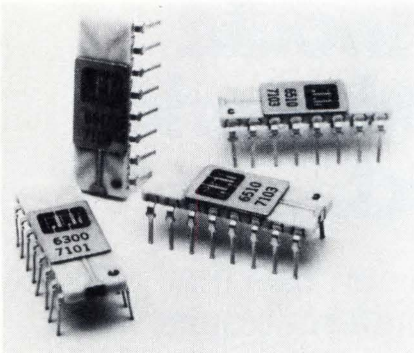
Triple power supply, Model 1051, delivers + and −15V at 0.5A and with 0.05% output regulation, and +5V at 1.25A with output regulation of 0.1%. Price, with 2-year warranty, is $75 each in moderate quantities. Pacific Instrument Co., 4926 E. 12th St., Oakland, CA 94601. **220**

DC motor controller for low-inertia servo motors, Model NC101, has servo bandwidth to 1000 Hz and can be used to achieve speed ranges greater than 6000:1. Control Systems Research, Inc., 335 Fifth Ave., Pittsburgh, PA 15222. **221**

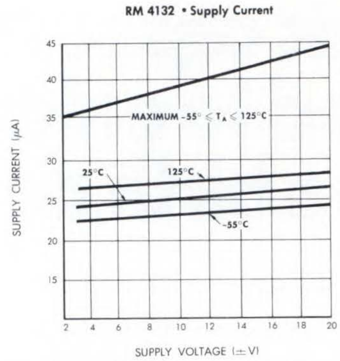
Events counter, a microminiature 4-digit totalizing unit only 37/64 inch^2 by 1-1/4 inch deep, has count rate of 1200 cpm. Models of the 49500 Series are available for 50, 60 or 400 Hz or dc operation with nominal power consumption of 2.5W. The A. W. Haydon Co., 323 N. Elm St., Waterbury, CT 06720. **222**

Millivolt/thermocouple alarm module, Model 18-141, receives a signal from a thermocouple and controls one hermetically-sealed 5A relay to signal a Hi or Lo alarm condition. Price is $145. Bell & Howell Co., Control Prods. Div., 706 Bostwick Ave., Bridgeport, CT 06605. **223**

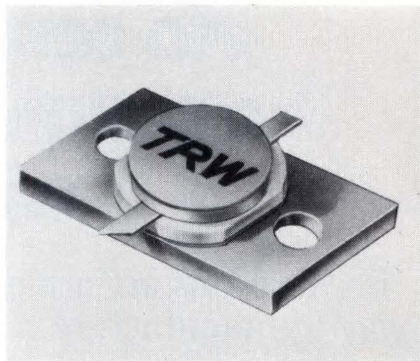
High-voltage electronic chopper handles from 1 mV to ±150V and operates between 270 Hz and 30 kHz. Model 150 plugs into a standard 7-pin miniature tube socket and can be used between −55 and +150°C. Small quantity price is $98 each. Solid State Electronics Corp., 15321 Rayen St., Sepulveda, CA 91343. **224**



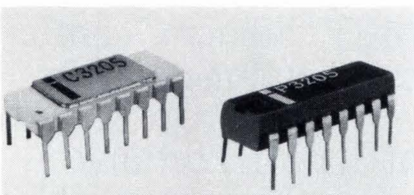
Random-access memory MM6510 is a 256-bit bipolar unit that is nonvolatile. If system power drops anywhere between 5 and 2V, memory information is guaranteed intact. If a complete 5V power failure occurs, the memory holds the information for 10 msec. Enable access time is 70 nsec, and in lots of 100 to 999, the 0-to-70°C unit is priced at $27 each. Monolithic Memories, 1165 E. Arques Ave., Sunnyvale, CA 94086. **225**



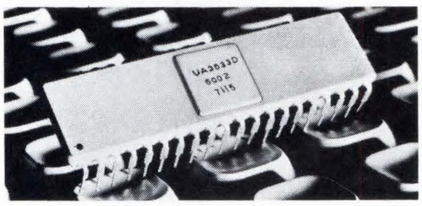
IC op amps, RM4131 (high gain) and RM4132 (micropower), are available. RM-4131 features 1.6 mA max current drain at 20V, slew rate of 2V/μsec and unity gain bandwidth of 4 MHz. Large signal voltage gain is 160V/mV. The 4132 features 35 μA max current drain between ±3 and ±20V, input offset of 2 nA and unity gain bandwidth of 150 kHz. Raytheon Semiconductor, 350 Ellis St., Mountain View, CA 94040. **228**



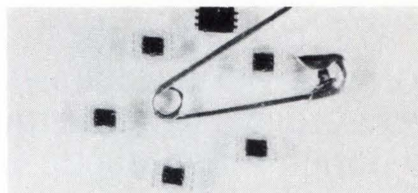
Broadband microwave power functions, designated "MICroAMP", include a series of silicon amplifiers that offer power levels of 12W to 6W in four increments of 1 to 2.3 GHz. Power gain is from 10 dB to 6 dB depending on power level and bandwidth. At the 100-quantity level, price is $240 each for the high power units and $100 each for low power devices. TRW Semiconductor Div., 14520 Aviation Blvd., Lawndale, CA 90260. **231**



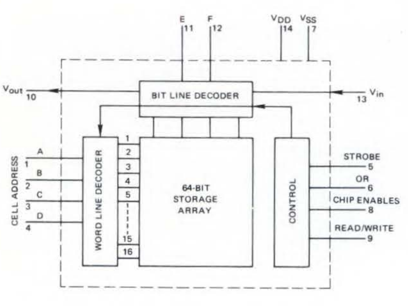
High-speed 1-of-8 decoder 3205, converts a binary code to a signal on 1-of-8 output leads. Input-to-output delay is only 18 nsec max. Price in lots of 100 items is $4.35 each (silicone) and $5.40 each (ceramic). Intel Corp., 365 Middlefield Rd., Mountain View, CA 94040. **226**



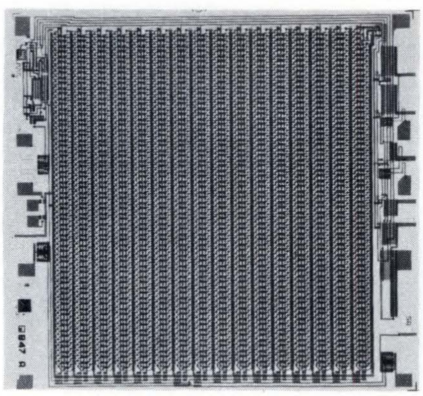
IC ROM UA3533, universal encoder can be programmed for codes with 9 bits/word or less. The unit translates signals from up to 128 keys into any of four different modes providing a total of 512 9-bit word possibilities. Unisem Corp., Box 11569, Philadelphia, PA 19116. **229**



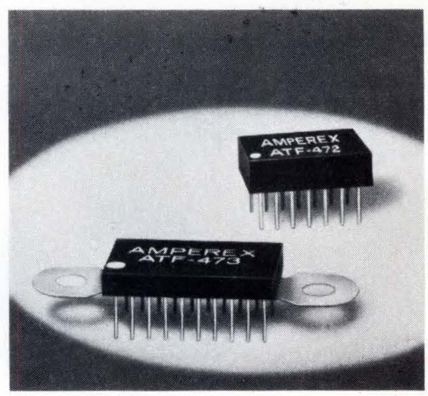
Operational amplifiers in LIDs include such items as the μA741 and LM 101. They are available in 8- or 14-post LIDs, and prices range from $2 to $5.50 each. Computer Components International, Inc., 3804 Burns Rd., Palm Beach Gardens, FL 33403. **232**



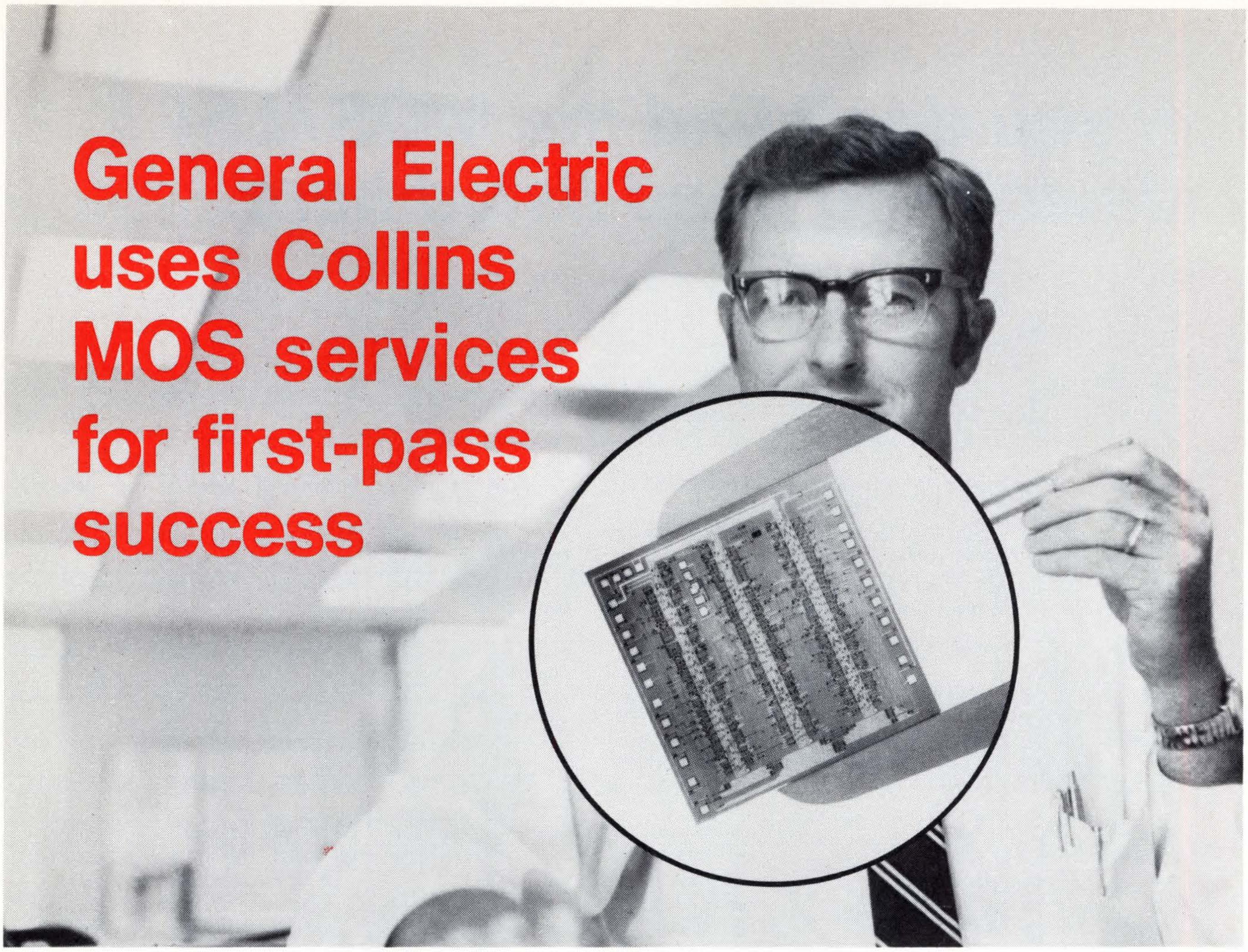
Complementary metal oxide semiconductors (CMOS) feature eight new logic circuits. Units include a 64-bit RAM, dual 4-bit shift register, dual "D" flip-flop, quad exclusive-OR gate, quad 2-input NOR gate, dual 4-input NOR gate, quad 2-input NAND gate and a dual 4-input NAND gate. Technical Information Center, Motorola Semiconductor Products Div., Box 20924, Phoenix, AZ 85036. **227**



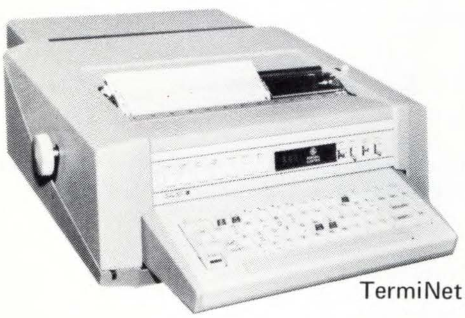
MOS dynamic shift registers with recirculating logic include the 2505, a 512-bit version and the 2512, a 1024-bit unit. Both registers operate with a typical clock rate of 5 MHz, power dissipation is 150 μW/bit at 1 MHz, and prices, in lots of 100 to 999, are $4.60 and $10.60 each, respectively. Signetics Corp., 811 E. Arques Ave., Sunnyvale, CA 94086. **230**



Dual Hybrid IC clock driver ATF473, is capable of driving two-phase clock lines for 35,000 bit MOS arrays at 1 MHz. The unit can source and sink up to ±2A in each circuit at output swings up to ±30V. Maximum rise or fall time into a 7000-pF load is only 40 nsec and delay time is only 10 nsec. Price is $16.50 each. Amperex Electronic Corp., Hybrid ICs, Cranston, RI 02920. **233**



GE's TermiNet 300 Teleprinter is whisper quiet and twice as fast as conventional printers. Advanced MOS circuitry minimizes size, maximizes versatility, reliability, and maintainability. Inset shows automated layout of GE's random logic MOS/LSI array.



TermiNet 300 Teleprinter

General Electric engineers used Collins automated services to design a random logic chip for GE's new TermiNet* 300 Teleprinter.

After a two-week familiarization course, they followed the step-by-step computer transactions to translate their design logic into the digital data which directs the highly-automated teleprocessing and teleproduction operations.

Utilizing predesigned cells, Collins teleprocessing (design) services executed the logic simulation, automated layout and routing, and test generation programs. The teleproduction (build) services digitally generated the photomasks, controlled the wafer fabrication, produced the test tooling and characterization sequences, and packaged the MOS/LSI prototypes.

The 150- x 160-mil chip performed as predicted, and yielded 39 percent at wafer level in initial test. This first-pass success is typical of the fast turnaround time, low cost, and predictable results of Collins C-System automated MOS/LSI design and processing services.

*Trademark General Electric Company, U.S.A.

COLLINS

COMMUNICATION / COMPUTATION / CONTROL

CIRCLE NO. 38

If you don't find the MOS/LSI device you need listed here,

	TYPE NUMBER	DESCRIPTION	CIRCUITRY	POWER SUPPLY	POWER DISS	PACKAGE (DIP/FP)	OPERATING TEMP (°C)
SHIFT REGISTERS	CRC1501	1024-Bit Shift Register	high threshold dyn 4ϕ	V_{DD}= −12	0.29 mw/bit	14-lead	−25 to +85*
	CRC1502	32-Bit Quad Gated Shift Register	low threshold dyn 2ϕ	V_{CC}= +5, V_{DD}=gnd	0.7 mw/bit	24-lead	−25 to +85*
	CRC1503	32-Bit Quad Gated Shift Register	low threshold dyn 2ϕ	V_{CC}= +5, V_{DD}=gnd	0.7 mw/bit	40-ld/34-ld	−25 to +85*
	CRC1504	16-Bit Quad Gated Shift Register	low threshold dyn 2ϕ	V_{CC}= +5, V_{DD}=gnd	0.7 mw/bit	24-lead	−25 to +85*
	CRC1505	198-Bit (Triple 66) Shift Register	high threshold dyn 2ϕ	V_{DD}= −14	0.075 mw/bit	14-lead or 10-lead TO-100	0 to +70
MEMORIES	CRC3001	1024-Bit 128-Word ROM (Custom pattern)	high threshold static	V_{GG}=V_S= −27, V_{DD}= −13	0.130 mw/bit	24-lead	0 to +70
	CRC3003	1024-Bit 128-Word ROM (sine look-up)					
	CRC3002	2048-Bit 256 & 512-Word ROM (custom)	high threshold static	V_{SS}= +12, V_{GG}= −12, V_{DD}=0.0	0.150 mw/bit	24-ld/22-ld	0 to +70
	CRC3004	2048-Bit 256-Word ROM (4 x 4 Multiplier)					
	CRC3501	2560-Bit 256 & 512-Word ROM (custom)	low threshold dyn with static outputs	V_{SS}= +5, V_{GG}= −12, V_{DD}=gnd	0.200 mw/bit	28-ld/34-ld	−25 to +85*
	CRC3502	2560-Bit 256-Word ROM ASCII/EBCDIC Converter					
	CRC3503	2560-Bit 256-Word ROM EBCDIC/ASCII Converter	low threshold dyn with static outputs	V_{SS}= +5, V_{GG}= −12, V_{DD}=gnd	0.200 mw/bit	28-ld/34-ld	−25 to +85*
	CRC3504	2560-Bit 512-Word ROM Row Character Generator ASCII Upper Case	low threshold dyn with static outputs	V_{SS}= +5, V_{GG}= −12, V_{DD}=gnd	0.200 mw/bit	28-ld/34-ld	−25 to +85*
	CRC3505	2560-Bit 512-Word ROM Row Character Generator ASCII LC & Special Characters	low threshold dyn with static outputs	V_{SS}= +5, V_{GG}= −12, V_{DD}=gnd	0.200 mw/bit	28-ld/34-ld	−25 to +85*
	CRC4001	64-Bit (16 x 4) RAM	high threshold static	V_{SS}=0.0, V_{GG}= −27, V_{DD}= −15	3.9 mw/bit	14-lead	0 to +70
	CRC4002	128-Bit (64 x 2) RAM	low threshold static	V_{SS}= +12, V_{DD}=gnd	0.9 mw/bit	24-lead	−25 to +85*
	CRC4003	256-Bit (64 x 4) RAM	low threshold static	V_{SS}= +12, V_{DD}=gnd	0.9 mw/bit	28-ld/34-ld	−25 to +85*
FUNCTIONAL LOGIC	CRC2001	16-Channel Multiplexer	high threshold static	V_{DD}= −28	150 mw	40-ld/34-ld	0 to +70
	CRC9501	8-Bit Plus Sign A/D Converter	high threshold dyn 2ϕ	V_{DD}= −12, V_{GG}= −28	100 mw	24-lead	−25 to +85*
	CRC9502	8-Bit Plus Sign D/A Converter	high threshold dyn 2ϕ	V_{DD}= −12, V_{GG}= −28	120 mw	24-lead	−25 to +85*
	CRC9503	R-Adder	low threshold dyn 2ϕ	V_{CC}= +5, V_{DD}=0	120 mw	40-ld/34-ld	−25 to +85*
	CRC9504	Quad Serial Summer	low threshold dyn 2ϕ	V_{CC}= +5, V_{DD}=gnd	90 mw	24-ld/22-ld	−25 to +85*
	CRC9505	Analog Switch	high threshold static	V_{SS}= +12, V_{CC}= +5, V_{GG}= −28, gnd	95 mw	14-lead	−25 to +85*
	—	Recursive Digital Filters System	high threshold dyn 4ϕ	V_{DD}= −12, V_{GG}= −28 & gnd	—	24-lead	−25 to +85*

These MOS devices are fabricated using a proven P-channel enhancement mode technology. Electrical characteristics are measured at t_{case}= + 25°C. Most of the devices are also available for operation over MIL temp range −55°C to +125°C.

design it yourself.

Collins new MOS/LSI shift register, memory and functional logic standard products are available for your equipment/systems designs today. For your custom designs, we invite you to use Collins automated MOS/LSI design & processing services. The complete cycle—from input of logic equations to tested prototype—typically takes 60 days: 30 days to design, 30 days to assemble and fabricate prototypes. Standard product data sheets are available from Collins MOS/LSI distributors and representatives, or directly from Collins Radio Company. MOS/LSI Marketing, Dept. 600, Newport Beach, California 92663. Telephone 714-833-0600.

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COMMUNICATION / COMPUTATION / CONTROL

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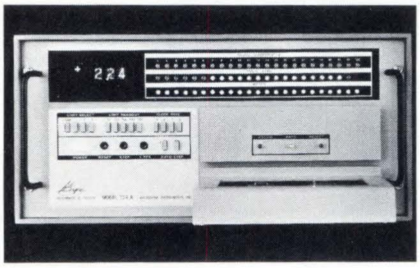
CIRCLE NO. 50

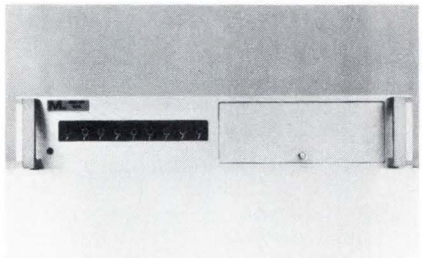


Automatic IC tester, Model 724, performs full functional and parametric analysis. Faster than many computer controlled systems, the 724 requires approximately 20 msec to check contact to the DUT, perform all possible function tests and verify dc parameters to within 1.5%. Price is $8850. Microdyne Instruments, Inc., 203 Middlesex Turnpike, Burlington, MA 01803. **243**

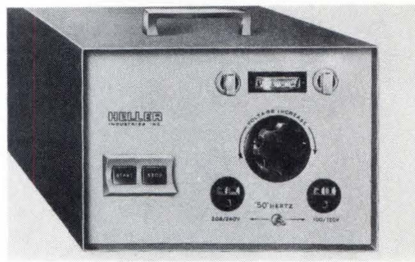
Function generator with simultaneous AM and FM capability, Model F231, covers from 0.005 Hz to 3 MHz. Signals generated are sine, squarewave, triangle, ramp, sawtooth, pulse, sweep, tone burst, FM and AM, and suppressed-carrier AM. A built-in notched-T filter permits self-calibration of frequency. Price is $1195 each. Microdot Inc., Instrumentation Div., 19535 E. Walnut Dr., City of Industry, CA 91744. **246**

Digital ratiometer—the 3-1/2-digit type 2330-570—displays the ratio of 2 dc voltages over a 10:1 change in the reference voltage. Accuracy is ±0.1% of reading ±1 digit over a reference voltage range of +0.5 to +2.0V dc. DTL/TTL-compatible BCD output and display hold are standard. Price is $199 each. Digilin Inc., 1007 Air Way, Glendale, CA 91201. **249**

ASCII message generators are priced at $595. Model 400 generates the full 94 ASCII printable characters in sequence and Model 401 generates a "Quick Brown Fox. . ." message. Crystal controlled clock rates are selectable in eight steps from 110 to 9600 baud. Wavetek, Instrument Sales Mgr., Box 651, San Diego, CA 92112. **244**

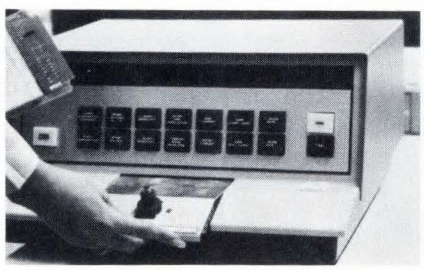


Digital clocks are available in 4-, 6-, 7-, 8- and 9-digit versions. An errorless hold-off circuit delays an output change for up to 0.8 sec. Output storage data can be held indefinitely while the clock continues to count. Prices for the new series 3100 clocks start at $575. Monitor Labs. Inc., 10451 Roselle St., San Diego, CA 92121. **247**

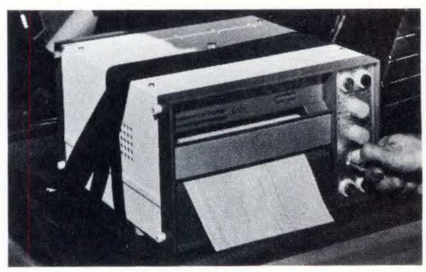


50-Hz power source, Model SK-1, converts 208/230V three-phase, 60-Hz input to 0 to 120 and 0 to 240V single phase, 50-Hz output at 750 VA. Outputs are individually fused and metered, and are well suited for both lab use and the testing of export equipment. Price is $795. Heller Industries, Inc., 18 Microlab Rd., Livingston, NJ 07039.

Frequency counters with automatic ranging, Model cf-251 and cf-252, have measuring range to 100 MHz. They automatically select both the correct measuring range and the decimal point position, depending upon the operator's choice of highest accuracy or fastest measuring speed. Prices are $695 and $895, respectively. Dixson, Inc., Box 1449, Grand Junction, CO 81501. **245**



Program board for checking sense amplifiers on the Signetics 1420 linear IC tester accommodates all standard IC packages that have 16 pins or less. Two versions are available, one that tests for operation within 5% (priced at $375) and one that tests for 1% performance (priced at $575). Signetics Measurement/Data, 341 Moffett Blvd., Mountain View, CA 94040. **248**



Portable recording oscillograph, Model 5-130, is a direct print-out multichannel recorder for use at altitudes to 25,000 ft—useful in virtually any attitude and under acceleration levels of up to 5G. Writing speed is over 50,000 inches/sec. Power required is 12V dc at 75W. Bell & Howell, Electronics & Instruments Group, 360 Sierra Madre Villa, Pasadena, CA 91109. **251**

Low-level data acquisition systems for extracting microvolt signals from "real world" industrial environments, the 200 Series, feature accuracy of 0.1% of full scale ±1/2 LSB, 140 dB CMR from dc to 1 kHz with 1 kΩ source imbalance, up to 1000V CM, <1 nA input current and 0.2 μV/°C zero stability. Multitech Automation Products, 583 Monterey Pass Rd., Monterey Park, CA 91754. **252**

Solid-state dipper, Type 90652, provides improved performance as compared to vacuum-tube versions. Frequency coverage is 1.7 to 300 MHz in seven ranges. Price, complete with carrying case, coils and 9V alkaline battery, is $110 each. James Millen Mfg. Co., Inc., 150 Exchange St., Malden, MA 02148. **253**

Break-out boxes that interface with "D" subminiature connectors have standard 3/4-inch banana jack spacing. Price ranges from $86 to $320. Technical Assistance Labs., 12701 S. Van Ness Ave., Hawthorne, CA 90250. **254**

High-voltage power supplies with up to 30 kV dc output have digital readout with 200 mV resolution. Models of the Series 205 include 1 kV at 30 mA, 3 kV at 10 mA, 5 kV at 5 mA, 10 kV at 2 mA, 20 kV at 1 mA and 30 kV at 0.5 mA. Voltage is adjustable from 0 to maximum in each unit. Prices start at $450 each. Bertan Associates, Inc., 15 Newtown Rd., Plainview, NY 11803. **255**

Ribbon bonder can produce 200 to 300 finished pieces an hour. The Model 1360 has automatic feed and break, and ultrasonically bonds either aluminum or gold ribbon of up to 20 mil² cross-sectional area. Price is $4470. Hugle Industries Inc., 625 N. Pastoria Ave., Sunnyvale, CA 94086. **256**

Coax contact assembly machine for subminiature connectors can cut assembly time by approximately 90%. The "CATS" unit requires only ac power and 100 psi air for operation. Burndy Corp., Norwalk, CT 06852. **257**

Ten-bit A/D converter is capable of word conversion rates from dc to 2 MHz when triggered externally, and can operate on internal clocks at 100 Hz and 2 MHz. The LAB 210, when combined with options, can also serve as a 100-word memory, a transient detector or a D/A converter. Base price is $4900. Computer Labs., 1109 S. Chapman St., Greensboro, NC 27403. **258**

Relay evaluation instrument, Model K147, continuously monitors the dynamic contact performance of signal or switching relays. The basic $7000 instrument simultaneously tests up to 28 Form A or B contacts or 14 Form C contacts. Teradyne, Inc., 183 Essex St., Boston, MA 02111. **259**

Lead bond pull tester, Model 2300, is semiautomatic and will handle a wide variety of packages including TO-5, TO-18, flat packs and plastic strips. Price complete is $229. R & G Enterprises, Box 2111, Santa Clara, CA 95051. **260**

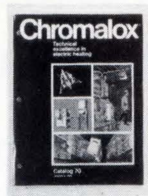
"Capsule Listing of Data Converters" is the title of this six-page summary that lists the salient specifications of a wide range of data converters and related accessories. ILC Data Device Corp., 100 Tec St., Hicksville, NY 11801. **276**

Circuit breaker panel boards are the subject of this 20-page design and application guide that details five types of panel boards that meet over 80% of all requirements. I-T-E Imperial Corp., 233 E. Lancaster Pike, Ardmore, PA 19003. **280**

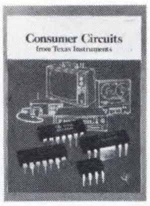
Rotary switch technical bulletin SP-395 contains eight pages of complete design information for using rotary switches in thousands of design variations. Oak Mfg. Co., Div. of Oak Electro/Netics Corp., Crystal Lake, IL 60014. **284**

NPL 112-page looseleaf catalog offers information on an entire line of altitude reporting displays, solid-state data converters, servosystems and indicators, digital transducers and displays, encoders, commutators and switch assemblies, and tandem assemblies. Northern Precision Labs., Inc., 202 Fairfield Rd., Fairfield, N J 07006. **277**

Digital Counters, eight-page bulletin 71-OEC-1, illustrates and describes approximately 50 standard digital counters. Included are electrically activated, rotary and ratchet mechanically activated and predetermining counters, elapsed time indicators, engine hour meters and special devices. ENM Co., 5342 Northwest Hwy., Chicago, IL 60630. **281**

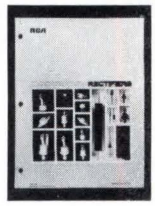


Electric heating elements and other electric heating equipment and controls for industrial process applications are covered in 132-page catalog 70. Included are sections on applying electric heat, helpful hints and circuitry and the selection of control equipment. Emerson Electric Co., Edwin L. Wiegand Div., 7500 Thomas Blvd., Pittsburgh, PA 15208. **285**

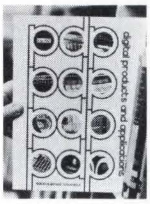


Consumer IC Bulletin CB-134, is a four-page brochure that provides a selection of 39 ICs ideal for use in the various sections of AM/FM radio-phonograph and color TV systems. Texas Instruments Incorporated, Inquiry Answering Service, Box 5012, M/S 308, Dallas, TX 75222. **275**

Low-cost conversion products are included in this four-page brochure that describes a complete line of low-cost D/A (from $19) to A/D converters (8-, 10- and 12-bit models). Zeltex, Inc., a Subsidiary of Redcor Corp., 1000 Chalomar Rd., Concord, CA 94520. **279**

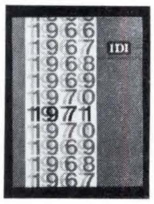


Thyristors and Rectifiers, 28-page catalog THC-500A, contains a wide selection of thyristors (triacs and SCRs), rectifiers and diacs. Data for each type of device are arranged by series and in order of ascending current. RCA Commercial Engrg., Harrison, N J 07029. **283**



Digital products and applications is a 158-page catalog that details a computer line, from the smallest PDP-16 functional computer to the largest PDP-10 computer system. About 25% of the catalog describes the way computers are used. Digital Equipment Corp., 146 Main St., MA 01754. **278**

"Track-Type Limit Switches" is the title of 28-page publication GEA-8394. These switches are designed to control the motion of machine tools, conveyors, turntables, elevators, cranes and mining equipment. General Electric Co., General Purpose Control Dept., Box 913, Bloomington, IL 61701. **282**



Digital readout catalog contains six pages of information on a product line that includes decode displays with and without memory, counter displays with and without memory, bidirectional counters and digital clocks. Instrument Displays, Inc., 223 Crescent St., Waltham, MA 02154. **286**

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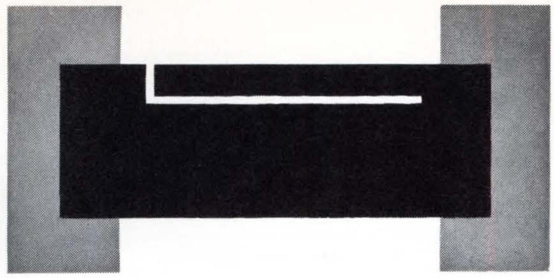
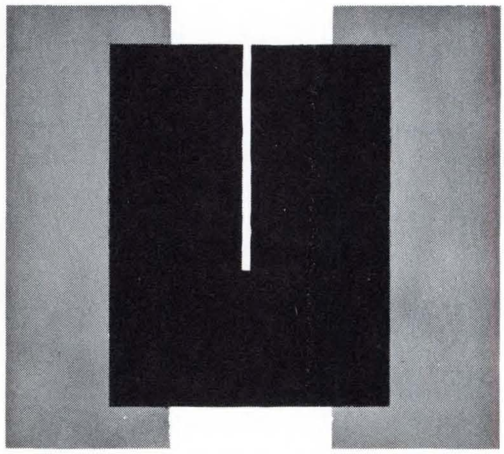
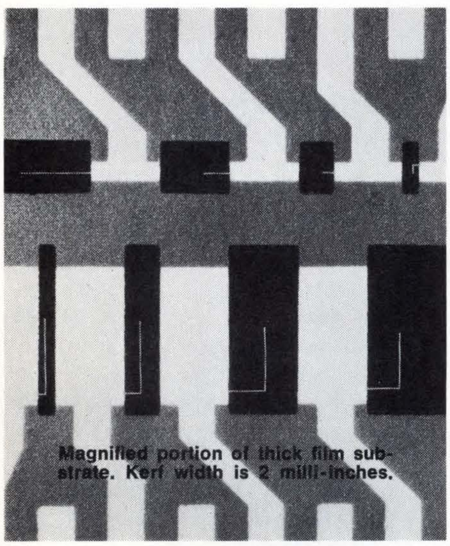
Being crooked usually beats going straight





...when it comes to laser trimming.

ESI offers the only debugged total system that makes the optimum cut automatically, whether it's straight into the resistor or an "L" cut (at no sacrifice in speed.)



Magnified portion of thick film substrate. Kerf width is 2 milli-inches.

Speed is the prime consideration in trimming resistors with a laser beam, but your desired rate must be achieved without sacrificing *quality* of the cut and *final accuracy.* Automatic L-cutting offers the best answer to controlling these factors, because after the laser beam has reduced the deviation from nominal value by approximately 15% it turns and completes the trim by running with the current lines instead of across the resistor, maximizing final accuracy. Highest quality is assured since the largest possible resistor area remains for maximum power dissipation and lowest current noise.

Our Model 20A system decides for each resistor exactly how much deviation must be removed before turning. Yet it still processes up to 10,000 resistors per hour at one station (depending upon hybrid chip parameters). Prices for complete laser trimming systems (installed, less freight) range from $22,000 to $85,000. This covers options from computer-control through semi-automatic and manual operation, at final accuracies specified from 0.1% to 0.01%.

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CIRCLE NO. 47

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Index to Ads, Products and Literature

Application Notes

"Application Notes" is a 13-page treatise on the current industry trend toward solid-state controllers. Covered are general switching, markets for solid-state devices, triac operation, solid-state switching possibilities and a list of potential applications. Hamlin Electronics, Inc., 3066 W. Clarendon Ave., Phoenix, AZ 85017. **290**

Thyristor control of incandescent traffic-signal lamps is an eight-page application note AN-4537. It indicates the major problems faced by the traffic-control designer and offers insight into solutions for these problems. RCA Commercial Engrg., Harrison, N J 07029. **291**

"Variac Catalog and Applications Handbook" is the title of this 24-page handbook that starts with a general discussion of the selection and application of "Variacs", proceeds through a complete listing of single-phase, three-phase, 400-Hz, and portable models, and concludes with a special section on how to "Get More Out of Your Variac." General Radio, 300 Baker Ave., Concord, MA 01742. **292**

"X-Band D-F Receiver Using Microwave Integrated Techniques" is the title of a paper that covers the development of a small two-channel hand-held receiver for use in determining the direction of an RF emitter operating in the 9- to 10-GHz frequency range. American Electronic Labs., Inc., M/S 1123-BKM, Box 552, Lansdale, PA 19446. **293**

"What Happens When Unused Input Design Rules Are Not Observed" is the title of eight-page engineering bulletin 25636-3. This note discusses degradation in device performance as a result of leaving unused inputs open. Sprague Electric Co., North Adams, MA 01247. **294**

"Universal Active Filter—Theory and Application" is a 54-page book that outlines the operating characteristics and performance advantages of the universal active filter. Specific applications in the communications, secure speech, avionics, radar and audio analysis fields are included. Kinetic Technology Inc., 3393 De La Cruz Blvd., Santa Clara, CA 95050. **295**

"Don't Fight It, Burn It" is the title of a 12-page booklet on how to pyrolyze obstinate samples for direct infrared analysis. It shows how polymers, carbon filled rubber and other intractable samples are volatized in seconds by the pyrolysis process for quick and reproducible results. Barnes Engineering Co., 30 Commerce Rd., Stamford, CT 06902. **296**

Design and fabrication of RF and microwave communications transistors is the subject of a brochure that includes sections on chip design, chip process, packaging, and reliability studies. Communications Transistor Corp., 301 Industrial Way, San Carlos, CA 94070. **297**

Emergency systems for handling power failures is a 20-page book that tells why the need for emergency power has grown, why it will become even more essential as the demand for electricity increases, where emergency power is needed, why it must be operated automatically, and what makes an automatic system reliable. Automatic Switch Co., Florham Park, N J 07932. **298**

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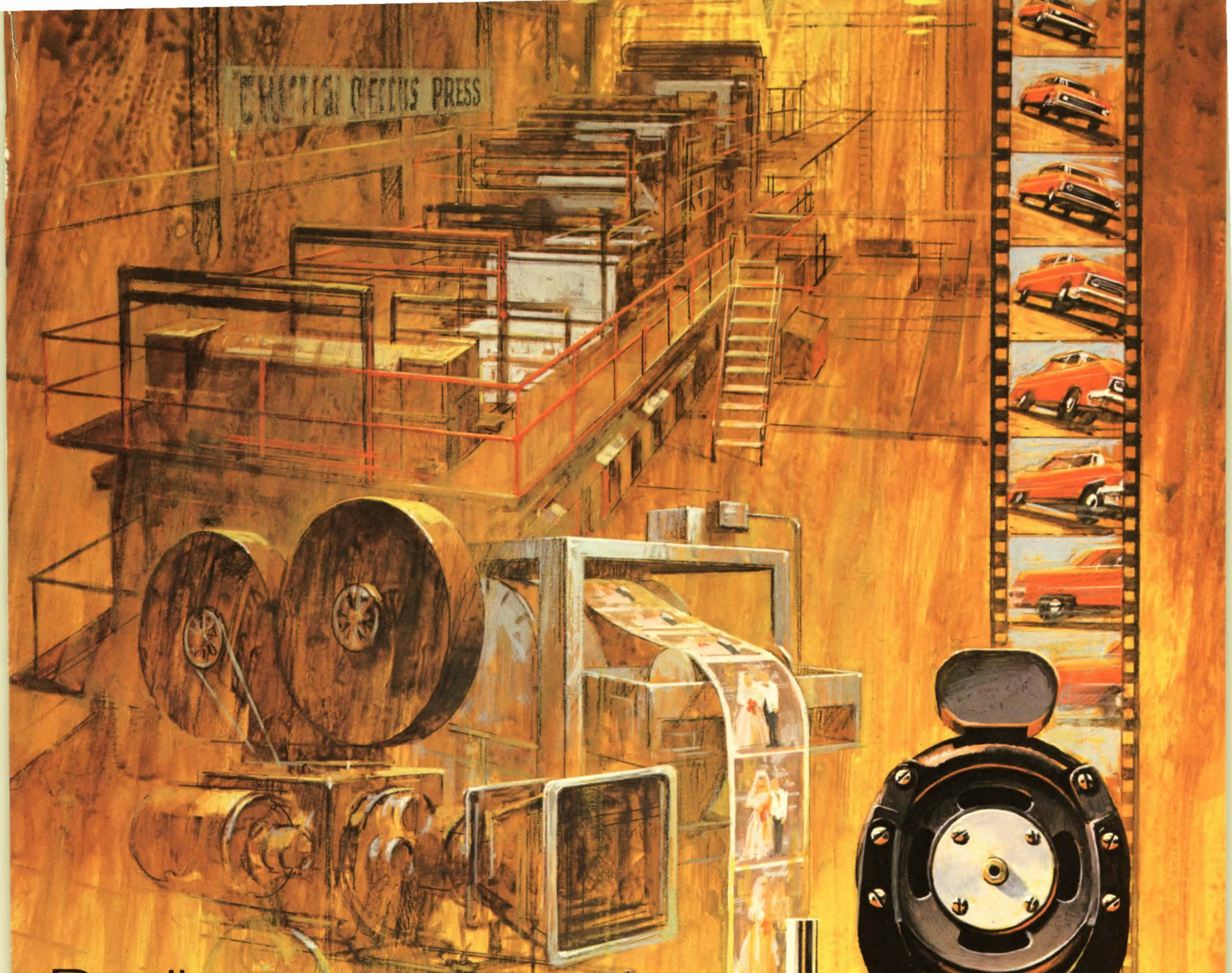

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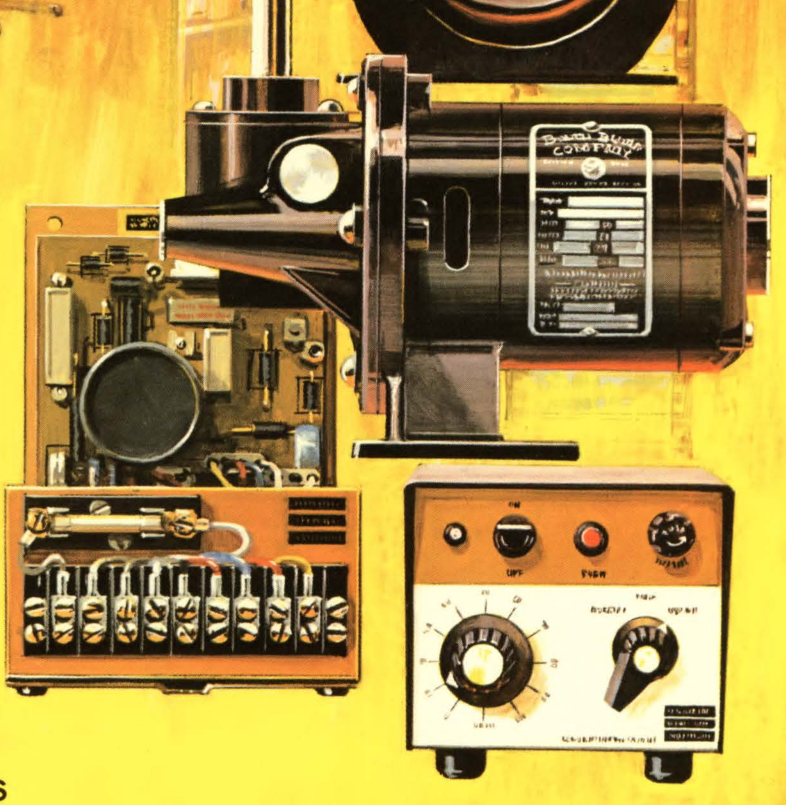

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