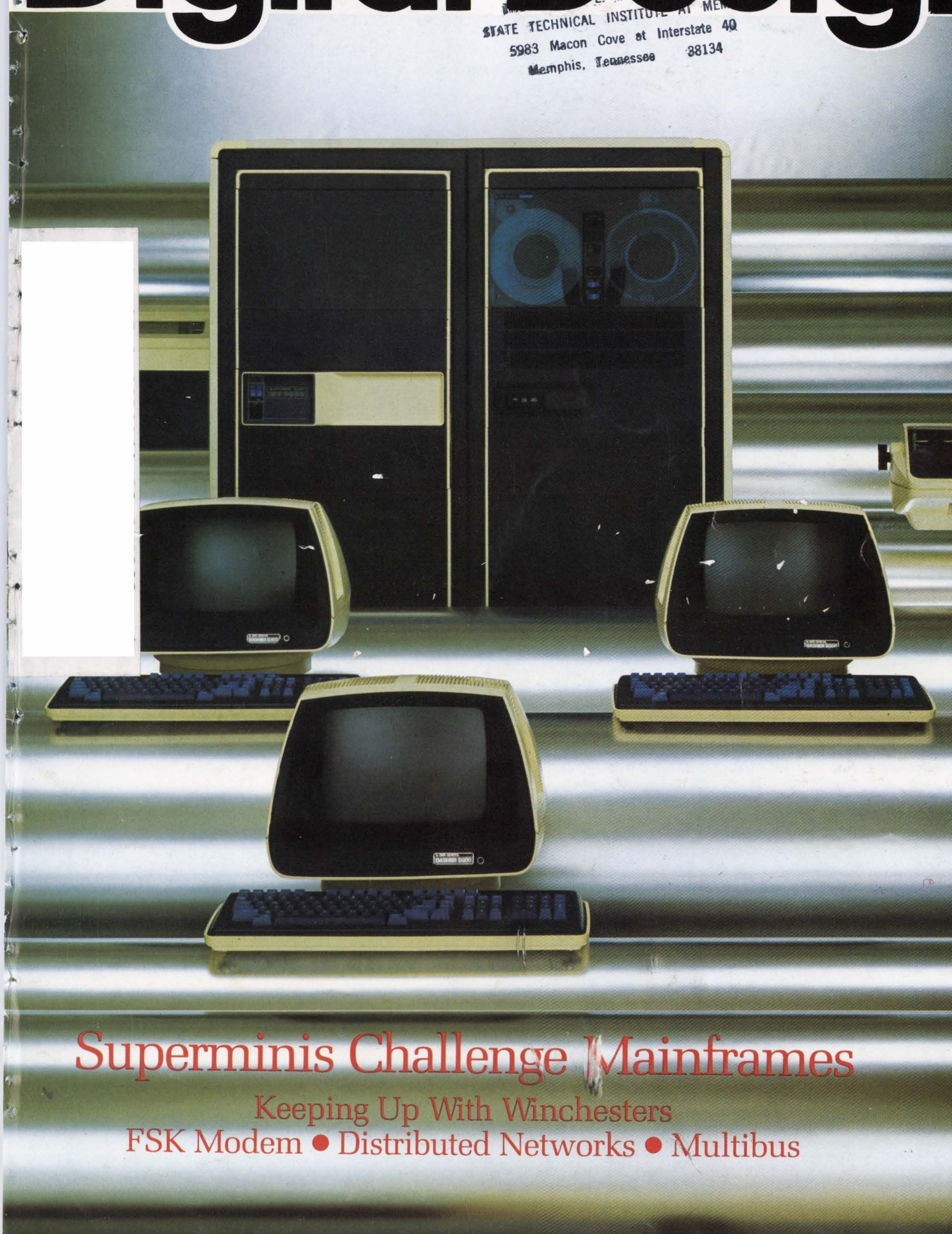
A MORGAN-GRAMPIAN PUBLICATION

Digital Design

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 10/82



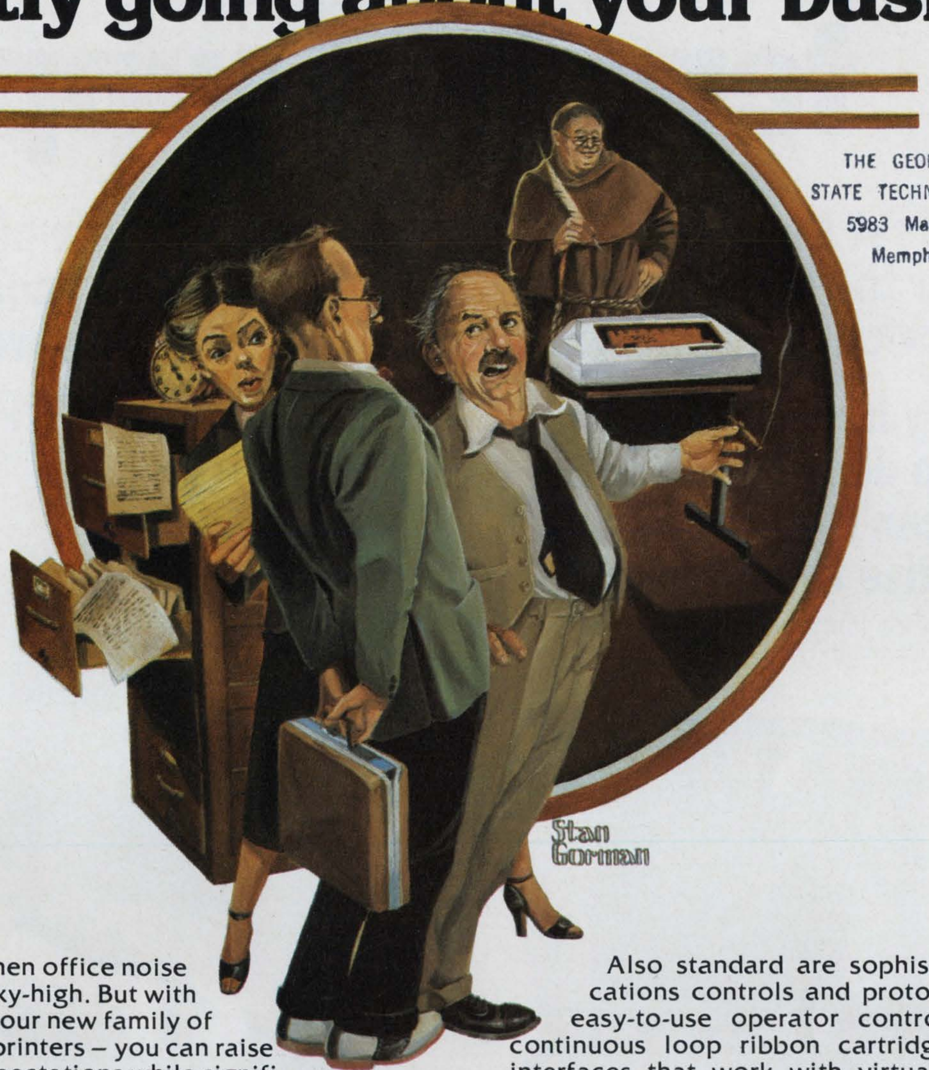
Superminis Challenge Mainframes

Keeping Up With Winchesters

FSK Modem • Distributed Networks • Multibus

VOL. 12
NO. 10

Anadex SILENT/SCRIBE™ printers. Quietly going about your business.



Now and then office noise levels can go sky-high. But with Silent/Scribe – our new family of matrix impact printers – you can raise your printer expectations while significantly lowering your office noise level.

How quiet is "silent"? Silent/Scribe operates at less than 55 dBA, which means that in the average office you may have to look at it to determine whether it's printing.

SILENT/SCRIBE MODELS

Standard Features	Char. per Inch	DP-9000A	DP-9500A	DP-9001A	DP-9501A	DP-9620A
Printing Speed (Char. per Sec.)	10	150	150	120	120	200
	12	180	180	—	—	120
	12.5	—	—	150	150	—
	13.3	200	200	—	—	—
	15	—	—	180	180	150
	16.4	—	—	200	200	164
Enhanced	10	—	—	—	—	100
Expanded Print (Double Width)		Yes	Yes	Yes	Yes	Yes
Dot Addressable Graphics (Dot/In., H/V)		60/72	60/72	75/72	75/72	72/72
Max. Line Width (In.)		8.0	13.2	8.0	13.2	13.2
Audible Alarm		Opt.	Opt.	Opt.	Opt.	Yes
Out-of-Paper Sense		Yes	Yes	Yes	Yes	Yes
Ribbon, Continuous Loop Cartridge (Yds)		30	30	30	30	30
Interfacing: Parallel Cent. Comp.		Yes	Yes	Yes	Yes	Yes
RS-232-C Serial		Yes	Yes	Yes	Yes	Yes

And Silent/Scribe is as easy to buy as it is to live with. You can select a variety of printing speeds, fonts and line widths. Some models provide both draft and enhanced quality copy. All models have superb dot-addressable graphics at no extra cost.

Also standard are sophisticated communications controls and protocols, flexible and easy-to-use operator controls, quick-change continuous loop ribbon cartridge, and universal interfaces that work with virtually any computer system.

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DP-9000A

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Steve Olla, Purchasing Manager
Millennium Systems Inc.

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Tom Peters, Engineer
Gould Inc.

We don't satisfy our OEM customers by making the best promises. Instead, we make the best terminals for the money, and deliver them the way they want them —when they want them. A concept so simple, you'd think everyone would have caught on.

But apparently not. Our value, performance and service were so exceptional that when we entered the end-user market in 1979, we were able to become the No. 1 independent manufacturer of smart terminals in just two years. An accomplishment that prompted *Computer Systems News* to say "...TeleVideo is one of the most amazing success stories in the computer industry."

It doesn't amaze us, however. Once we found a way to beat the leaders on price and quality, finding customers was easy.

In fact, it was OEMs who first contacted *us* after our success in the general-purpose market, with the idea of modifying terminals. And now we're totally committed to the OEM market.

Here's what we can offer.

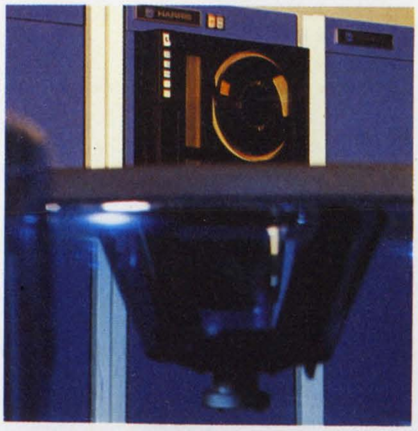
Uniqueness: We'll work closely with you all the way down the line to insure the right color, keyboard design, logo; and a code structure to interface with your software.

Fast delivery: We always have inventory ready for modification, so our turn-around on key operations begins the day you place your order.

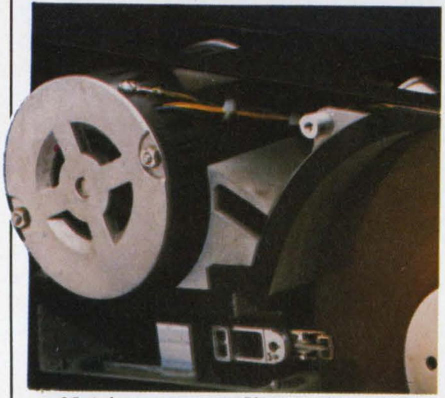
Price/Performance: Nothing outperforms our terminals on the job, and no one beats our price for value. Our rigid testing and use of high quality components have made our record of customer service,

OCTOBER 1982
VOL. 12, NO. 10

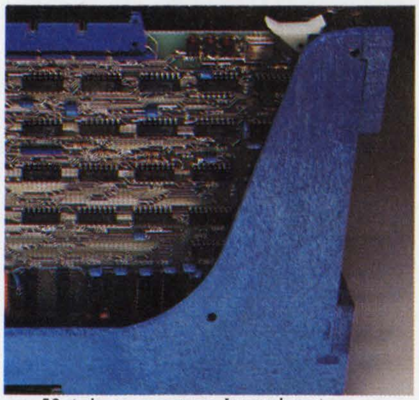
Digital Design



p. 44 (photo courtesy Harris)



p. 28 (photo courtesy Shugart Assoc.)



p. 52 (photo courtesy Interphase)

Cover

This month's cover depicts Data General's line of superminicomputers, which are reviewed in our supermini feature beginning on p. 44 (photo courtesy of Data General).

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Smart Graphics™ GX-100 We Have Only Just Begun.

The **GX-100** Graphics Terminal is only the beginning of a family of Computer/Graphics products from Modgraph. The Modgraph **GX-100** is a dual purpose expandable computer terminal. High resolution graphics, 8085 processor, 144K RAM, independent high speed alphanumeric overlay, and a wide range of performance characteristics unmatched in the graphics industry.

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OTHER FEATURES

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VT-100 Trademark Digital Equip. Corp.

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Calendar

November 1–2

Data Processing & Telecommunications Seminar. Newton Howard Johnson, Boston, MA. New York, NY, November 15–16. Contact: National Institute for Management Research, PO Box 3727, Santa Monica, CA. (213) 450-0500.

November 1–3

Online '82. Atlanta Hilton, Atlanta, GA. 4th Annual Conference and Exposition for users of online databases. Contact: Jean-Paul Emard, Online Inc., 11 Tannery Lane, Weston, CT 06883. (203) 227-8466.

November 3

Invitational Computer Conference. Palo Alto, CA. November 8, Denver, CO. Directed to the quantity buyer—OEMs, systems houses and "sophisticated" end users. Contact: B.J. Johnson Associates, 3151 Airway Ave., #C-2, Costa Mesa, CA 92626. (714) 957-0171.

November 7–10

Data Training '82. Adam's Mark Hotel, Houston, TX. Third Annual Conference for Data Processing and Office Automation Trainers. Contact: Loretta Lillios, Conference Coordinator, Data Training '82, 176 Federal St., Boston, MA 02110. (617) 542-0146.

November 8–11

COMDEX/Europe '82. The RAI Exhibition Center, Amsterdam, The Netherlands. Contact: The Interface Group, 160 Speen St., PO Box 927, Framingham, MA 01701. (617) 879-4502, outside MA toll free (800) 225-4620.

November 8–10

VLSI Design Seminar. Washington, DC. A structured approach to custom IC design, presented by Prof. Carlo H. Séquin. Contact: Hellman Associates, 299 S. California Ave., Palo Alto, CA 94306. (415) 328-4091.

November 9–13

Electronica '82. Trade Fair Center, Munich, W. Germany. 10th Annual Trade Fair for Components and Assemblies in Electronics. Contact: Kallman Associates, US Representatives, 5 Maple Ct., Ridgewood, NJ 07540. (201) 652-7070.

November 10–12

Compsac '82. 6th Annual International Computer Software & Applications Conference and Technical Show. Hotel Palmer House, Chicago, IL. Contact: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. (301) 589-3386.

November 15–17

ISHM '82. International Society for Hybrid Microelectronics. MGM Grand Hotel, Reno, NV. Contact: ISHM, PO Box 3255, Montgomery, AL 36109. (205) 272-3191.

November 15–17

National Systems Executive Forum. Washington, DC. "Managing Software Development." Contact: US Professional Development Institute, 12611 Davan Dr., Silver Spring, MD 20904. (301) 622-5696.

November 16–18

Cherry Hill '82. National Test Conference. Franklin Plaza Hotel, Philadelphia, PA. Contact: David Kirk, McKinney/Public Relations, Independence Mall West, Philadelphia, PA 19106. (215) 922-3945.

November 23–25

The 2nd International Conference on Semi-custom ICs. The West Center, London, England. Contact: Conference Secretary, Prodex Limited, 79 High St., Turnbridge, Wells, Kent, TN1 1XZ, England. 0892 39664/5.

November 29–December 2

Globecom '82. Global Telecommunications Conference. Sheraton Bal Harbour Hotel, Miami, FL. Contact: Dr. Thomas J. Harrison, Registration Chairman, IBM Dept. 2K1, PO Box 1328, Boca Raton, FL 33432. (305) 998-2734.

November 29–December 2

COMDEX/Fall '82. The 4th Annual National Conference and Exposition for Independent Sales Organizations. Las Vegas Convention Center, Las Vegas, NV. Contact: The Interface Group, 160 Speen St., PO Box 927, Framingham, MA 01701. (617) 879-4502, outside MA, (800) 225-4620.

November 30–December 2

Autofact 4. Conference and Exposition. Philadelphia Civic Center, Philadelphia, PA. Contact: Society of Manufacturing Engineers, One SME Dr., PO Box 930, Dearborn, MI 48128. (313) 271-1500.

November 30–December 2

MIDCON '82. Dallas Convention Center, Dallas, TX. High-Technology Electronics Exhibition and Convention. Contact: Eileen Algaze, Electronic Conventions, 999 N. Sepulveda Blvd., El Segundo, CA 90245. (213) 772-2965.

November 30–December 3

NATA. The North American Telephone Association 13th Annual Convention and Exhibition Showcase. Washington Hilton Hotel, Washington, DC. Contact: NATA, 511 2nd St., NE, Washington, DC 20002. (202) 547-4450.


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News Update

Inmos Moves Price On Static RAMs

Inmos has announced price reductions on its fast 16K MOS static RAMs. One hundred-piece prices for the 55ns IMS1400-55 and 45ns IMS1400S-45 16K × 1 MOS static RAMs were quoted as $18.00 and $21.60 each, respectively (reduced from $20.00 and $24.00). The 55ns IMS1420S-55 4K × 4 static RAM was reduced from $23.60 to $19.45 each (100's).

Agreement On Gate Arrays

Thomson-EFCIS (a subsidiary of Thomas-CSF), and Applied Micro Circuits Corporation (AMCC) have signed an alternate source agreement regarding AMCC's high-performance, bipolar Q700 series of gate arrays.

Computer Aided Engineering

Kamran Elahian has established Computer Aided Engineering in Sunnyvale, CA, to develop computer-aided IC design systems. The initial $2.5 million funding package was obtained from sources including Bay Partners, Mountain View, CA, Harvest Ventures, NY, and Hambrecht & Quist, San Francisco, CA.

Industry Standard For Micro-Floppy

Xidex Corporation has joined the group established in June 1982, to develop an industry standard for the next generation of sub-4″ computer disks. The group, consisting of manufacturers of floppy disk drives and media, plans to recommend a media standard to the American National Standards Institute (ANSI) by the end of September. Other members of the group are Dysan Corporation, Olivetti Peripheral Equipment, Inc., Shugart Corporation, Tabor Corporation, and Verbatim Corporation.

Intel To Serve Datacom Industry

Intel Corp. has established a Data Communications Business Unit to develop and market new datacom systems products. The new business unit is managed by Philip L. Arst, previously the head of Intel's Ethernet program. The unit reports to Leslie L. Vadasz, senior vice president and director, Corporate Strategic Staff.

8″ Winchester Contract

Micropolis Corp. has received an OEM contract for 8″ Winchester disk drives, valued at $5 million to $10 million, from Siemens AG, Munich, West Germany. The 5-year agreement calls for all Siemens divisions worldwide to purchase all six models of the Micropolis 1200/1220 Series drives with Micropolis Intelligent Interface, offering a maximum storage capacity of 45 Mbytes.

Discount On Add-In Memories

Texas Instruments has announced average price reductions of 20% effective immediately on most members of its series of add-in memory boards for LSI-11, PDP-11, VAX-11/780, and iSBC/Multibus computer systems. The company also announced an introductory discount offer to encourage evaluation by first-time users of TI add-in memory boards, effective through December 31, 1982.

Zilog, AMD Sign New Second-Source Agreement

Zilog and AMD have signed a new cross-licensing agreement for the Z8000 μP component family, extending an alternate-source relationship that has existed since 1978. Under the terms of the new agreement, AMD will manufacture both the original Z8000 family of 16-bit CPUs and peripheral circuits, and the recently-released Z8003/4 virtual-memory processors. In return, Zilog will obtain a number of AMD-developed peripheral circuits compatible with the Z8000 family, as well as certain AMD proprietary communications devices.

Digital To Market BBN Software

Digital Equipment Corporation has added RS/1, the Research System to its Laboratory Data Products (LDP) Group. RS/1, a software product of BBN Research Systems, will now be available to Digital's scientific customers.

Price Of EPROMs Drops

Intel Corp. has announced a 20% price reduction on its high-density 27128 EPROM. The new price is $45 per device for orders of

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MARS-232 Array Processors Support the User
who needs:

Signal Processing
with programmable high-speed arithmetic, logical, and decision-oriented operations for real-time applications.

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directly into the processor at sample rates up to 20 MHz via a prioritized multi-port bus structure.

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where, as a development system, the MARS-232 supports low-cost ROM-based MARS-132's or customized user-defined VLSI implementations.

MARS-232 Array Processor Features Include:

- 1K Complex FFT Performance
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In today's world it is not enough to have outstanding hardware. Our interactive software system, GSP, allows hands-on assembly/disassembly, loading, debugging, and diagnostic services – with multiple processor support built-in. For the real-time environment, we use ESP, a host-resident executive. It provides intelligent supervision for host programs that call applications library or user-defined subroutines, without compromising the speed of MARS.

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With its high computational capacity and low cost, the MARS family provides solutions for a broad range of application areas – on-line video inspection and image analysis; front-end data acquisition, compression, and formatting; spectral analysis, filtering and thresholding.

MARS- a new world of performance for medical, seismic, radar, sonar, and communications systems.

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For additional information on the MARS Family of High Speed Array Processors, write or call:
Numerix Corp., 320 Needham Street, Newton, MA 02161 Tel. 617-964-2500

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10,000 units, down from $57 per device. In addition, Intel projects further price reductions of the 27128 EPROM to less than $20 per device for quantity orders in the second half of 1983.

$4.5 Million Systems Pact

Computer Aided Engineering has signed a $4.5 million contract with Apollo Computer, Chelmsford, MA for Domain Computers which will be used in Computer Aided Engineering's LSI and VLSI computer-aided design systems. Deliveries on the two-year contract began in June.

Standard For μPs

The IEC, Geneva, Switzerland has published a standard (IEC559) for next generation μP systems to perform binary floating-point arithmetic. The standard specifies floating-point number formats, the results for arithmetic operations, conversions between different formats, and conversion between floating-point numbers and integers or decimal strings.

Price Reductions

Gould Inc, SEL Computer Systems Division has announced price reductions for memory and peripherals used with the Gould CONCEPT/32 computers. Memory prices have been reduced as much as 23% for some models of the Integrated Memory Module (IMM). The new prices for single 256 Kbytes, 512 Kbytes, and 1 Mbyte IMMs are $7,000, $9,000 and $14,000, respectively. Packages of two, three or four IMMs are available. Typical of these is the package of four 1 Mbyte IMMs for $39,000. Price reductions of up to 25% were announced for selected 80 Mbytes, 300 Mbytes, and 600 Mbytes disk drive units and disk subsystems.

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Xylogics Storage Cells: A totally new way to solve data storage problems on VAX*, PDP-11*, LSI-11, Nova/Eclipse** and Multibus*** compatible systems. We start with the proven performance, reliability and economy of our Peripheral Processors for 100% software compatible control. Then we add state-of-the-art peripherals like high-performance fixed disk and removable cartridge Winchesters, ¼″ cartridge tapes, and reel-to-reel tapes for start-stop or streaming operation. And we wrap everything up in a series of modular cabinets that integrate perfectly with your computer packaging.

Storage Cells: They give you more choices, more capacity and more convenience in less space, and at lower cost than any other data storage subsystem on the market.

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Now you can forget about data storage limitations. With Storage Cells you can get the perfect combination of capacity and application-oriented features in an incredibly compact package. Consider the XSC100 for VAX and PDP-11 systems. In a single bay cabinet only 40″ high, this Storage Cell gives you up to two 160MB disks plus a reel-to-reel streaming tape with emulation of DEC's RK07's or RM02's and TS04 peripherals.

The XSC200 for Q-bus, Unibus,* Multibus, or Data General I/O bus** systems is equally versatile. In one 5¼ inch high cabinet you can combine fixed and removable Winchester disks. Or you can have two 34MB or up to two 70MB Winchesters in the same 5¼″ space. For Q-bus only, the XSC200 features up to 70MB of Winchester storage plus a 17MB cartridge tape drive.

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When we took the title "The Capacity Leaders," we knew we could never rest on our laurels. If you'd like complete technical information on the new Computer Memories 40 Mbyte 5¼" Winchester disk drive, call or write us today at the address below.

And still the Capacity Leader...

Computer Memories, Inc.

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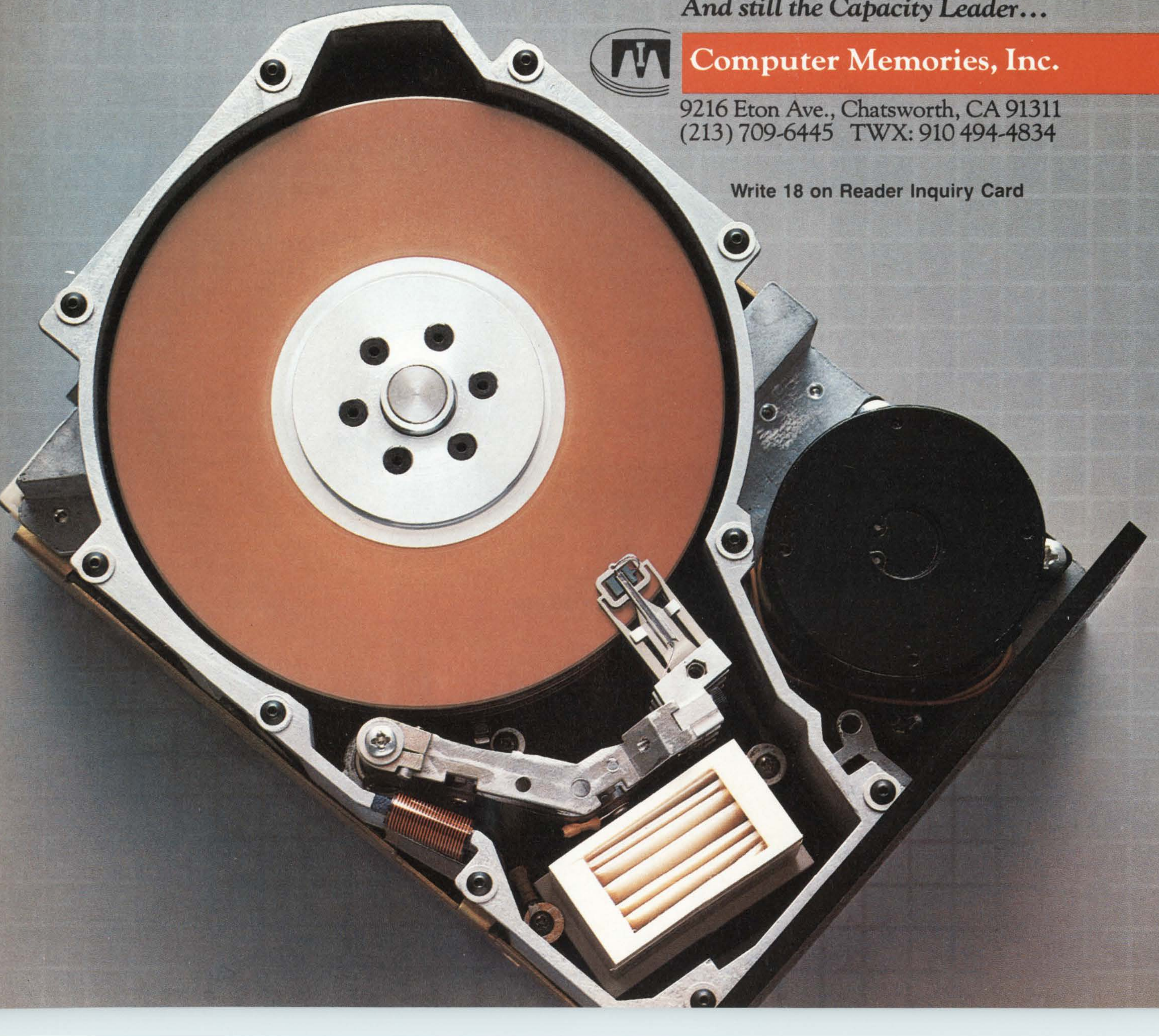

Display Technology Provides Local Hidden Surface Removal and Surface Shading

A new product from Lexidata Corp (Billerica, MA) reduces from minutes to seconds the average time it takes to display a solid image. The new display system, called SOLIDVIEW, can display the construction of a solid object incrementally without sequentially repainting the entire screen in scan line order. SOLIDVIEW incorporates local hidden surface removal and visible surface shading to accelerate the shaded image generation process. This new approach, according to David A. Luther, industry marketing manager, "provides the fastest, most cost-effective capability for viewing solid models anywhere."

Lexidata predicts SOLIDVIEW will broaden the market for solid modeling by bringing the technology to applications where its use has been prohibitively slow.

"The standard approach to generating a solid image is just too slow and tedious," says Luther. "Traditionally, a host computer must transform and clip an object into a viewing volume, remove hidden surfaces and calculate pixel values for each visible surface. The entire image must be created at the host computer before pixel data can be sent to the display processor. The image then appears in scan line order from top to bottom. There is an inordinate waiting period from the time an image is requested to the appearance of the first visible scan line, and once the drawing starts, the host must send every pixel to the display processor, tying up expensive host computer time."

SOLIDVIEW processes three-dimensional primitives such as polygons, lines, and points, as well as two-dimensional data. The system performs piercing and contouring functions and features both constant and smooth shading techniques.

"In the new approach," Luther explains, "hidden surface removal, visible surface shading, and pixel drawing functions are performed locally by SOLIDVIEW, drastically reducing host computer use. Full geometric representations, not individual pixels, pass from the host to SOLIDVIEW. Once the host has transformed and clipped one geometric figure, it is sent to SOLIDVIEW, providing immediate feedback to the user. The picture is contructed quickly and incrementally, providing the first interactive solid modeling capability."

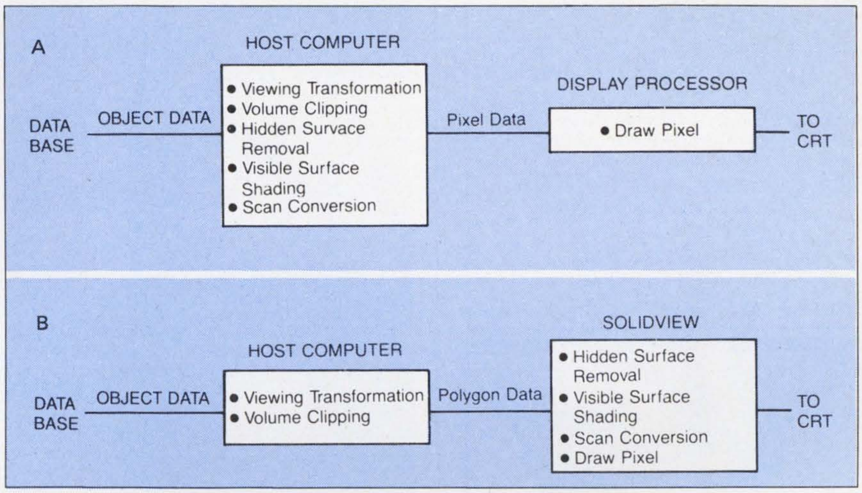

Figure 1: A) Typical solid modeling systems are host intensive, as opposed to B) SOLIDVIEW, which off-loads the host and balances the workload.

Price for a 640×512 resolution SOLIDVIEW system is $29,000, including monitor. An expanded version incorporating pan/zoom and interactive features is priced at $37,000 including monitor (delivery is 90 days).

Interface Package For Development Systems

The Design Automation Division of Tektronix has just announced the first package in its Vendor Interface Program, a long-range plan to integrate Tektronix μC design tools with the development systems of other vendors. The program will focus on the large customer and equipment installed bases that development system vendors such as Intel, Motorola and Zilog have created. In its introductory package Tektronix will offer a general purpose interface for its 8500 Series of Microcomputer Development Labs and Intel's Intellec Series II and III.

The introductory package provides full file transfer and interface capability between Intel's Intellec Series II and III systems and the Tektronix 8540, 8550 and 8560. Priced at $500, the package is scheduled for availability this month. It will allow Intel systems to be used with Tektronix software development tools, while providing a bridge to multi-vendor chip support.

For example, 8086 load modules can be transferred to the Tektronix system and executed using Tektronix 8086 emulation and debug system. This gives the

Continued on pg. 18

Technology Trends

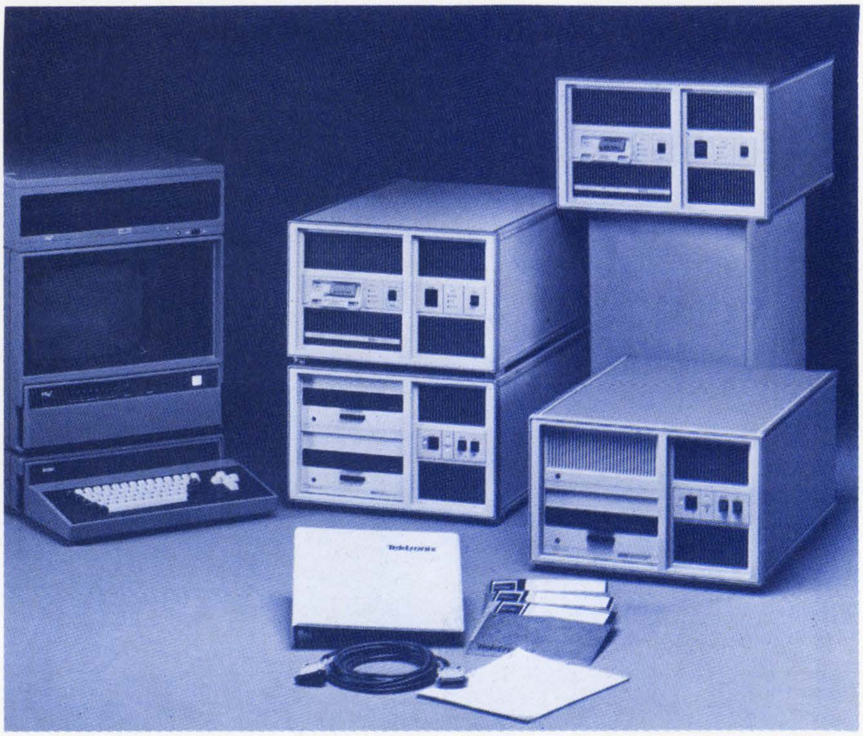

Figure 1: In its introductory package, Tektronix has introduced a general purpose interface for its 8500 series and Intel's Intellec series II and III.

Continued from pg. 17

designer access to emulator features such as real-time execution from emulation memory, or simulation of prototype I/O which are features not available with the Intel system.

Load modules can also be transferred from the Tektronix system and executed on the Intel emulators. This configuration allows Tektronix to offer a complete software development environment for processors like the Intel 8051, with access to Intel emulation if it is needed. This approach is useful in bridging the development tool gap where support for multiple vendor processors is required, such as a design containing both an Intel 8051 and Motorola 68000.

In addition, the interface package allows a number of stand-alone Intel development systems to become team-oriented work stations linked via the Tektronix 8560 multi-user mainframe and the TNIX operating system. This increases the capability of each stand-alone Intel system by adding more file and directory space, and also creates a complete team-oriented development environment to support today's larger design projects. Through TNIX, the designer has access to built-in functions such as on-line "mail" for inter-user communication plus a complete set of documentation tools that increase productivity. Traditional μP software tools like editors, assemblers and compilers are also available on the 8560 to support Intel chips, so the designer can off-load tasks that may have been constrained on the stand-alone system.

Future interface packages will bring Tektronix multi-chip design tools to the systems of other major development system vendors, such as Motorola and Zilog. Also, Tektronix design tools will be introduced into the traditional host computer market in the form of compilers and assemblers, integration tools and interfaces and optimized to a particular host machine.

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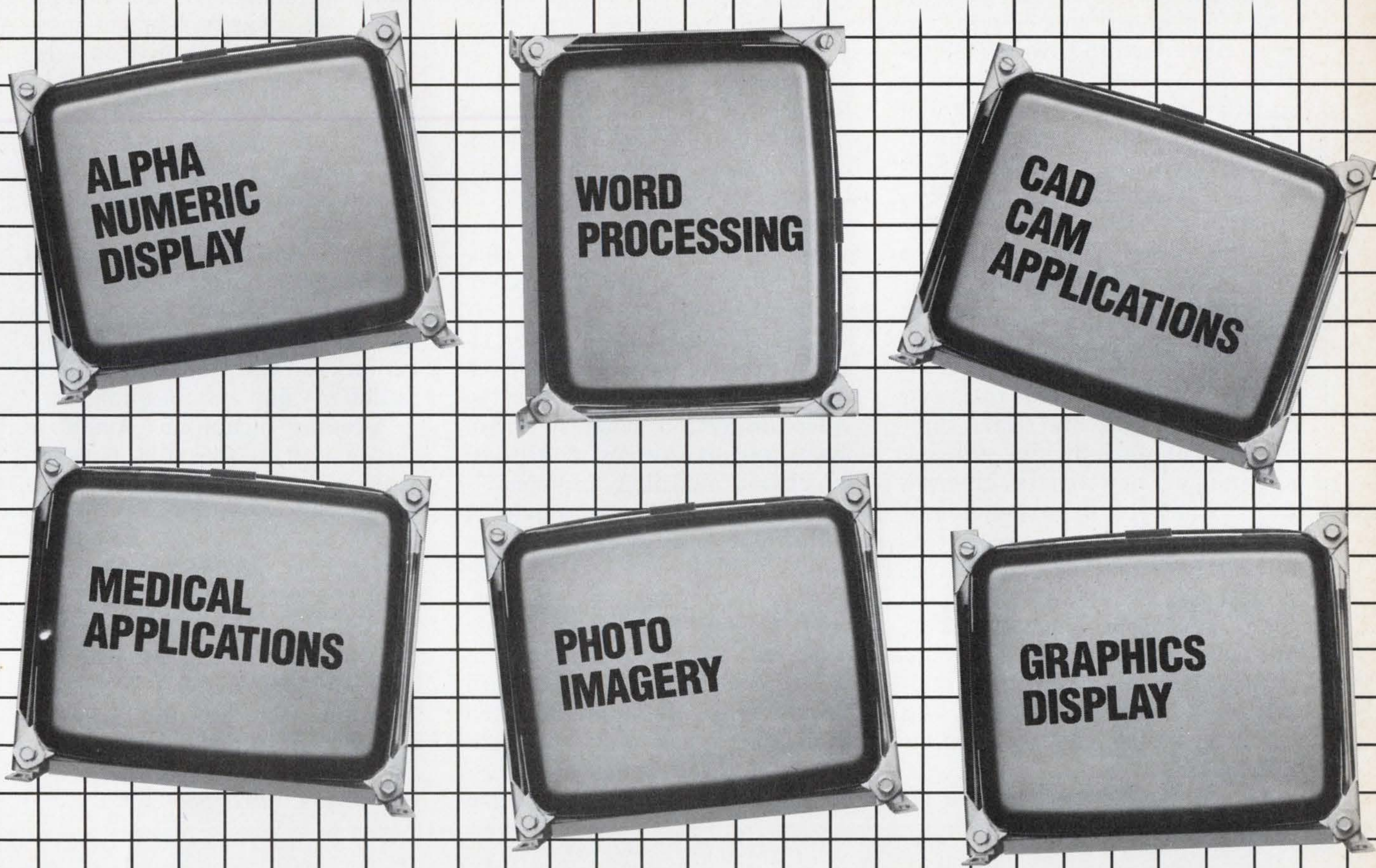

Yesterday's ideas might not be good enough for today or tomorrow, and selecting the proper data display has never been more significant. Recent studies in the computer marketplace indicate the CRT display has become the single-most important element in today's computer systems. An easy-to-read, jitter-free display is of course a dynamic part of this critical man/machine interface.

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Vision Comes Of Age

Machine vision has emerged from a long infancy, according to a study by Insight Associates, a Carson City, NV consulting firm. The US installed base of non-captivity manufactured vision systems grew by *83%* in 1981, increasing to 1,031 units from a 1980 total of 562 units. Shipment value rose to an estimated $29.4 million in 1981 and will top $1 billion in 1991, growing at an average annual rate of 44%. These market figures do not include shipments of vision-directed wirebonders or image analyzers.

The emergence of vision technology in the last two years is evidenced not only by rising shipments, but also by the growing number of newcomers entering the business. Only a handful of companies produced vision systems a few years ago; today, vision manufacturers totaling 66 firms routinely announce new products. Venture capitalists and shareholders have put more than $40 million into eight start-up companies that make robotic vision systems.

Two forces are driving the vision market: higher productivity and improved product quality. Offering payback periods as short as three months and performance unmarred by fatigue and boredom, vision systems excel in tedious, labor-intensive work. But technological factors also drive the market. More robust algorithms, faster operating speeds, higher resolution, greater use of gray-scale processing, and increased "user-friendliness" contribute to a growing acceptance of machine vision.

Diversity keynotes the seven vision system market segments. Three different product types — video inspection systems, micromeasurement systems, and printed circuit metrology systems — are used in *off-line* measurement and inspection applications. Two *on-line*, general purpose types — robotic vision systems and IDC vision sytems — find use in a wide array of inspection, detection, and control applications. A third on-line type, the vision-directed wirebonder, has only one end-user — the semiconductor industry. A final system, the off-line image analyzer, only marginally qualifies to be called a vision system, since it performs limited *automatic* analysis of scene data.

In 1981, vision systems going to on-line applications had an edge over off-line system usage, their share amounting to 54% of the number of units installed. By dollar value, however, on-line uses trailed, taking $14.3 million of the $29.4 million in total shipments, or 49%. When the 1980s end, it will be no contest at all; on-line systems — paced by their teaming up with robots in assembly applications — will predominate both in dollar value and unit volume.

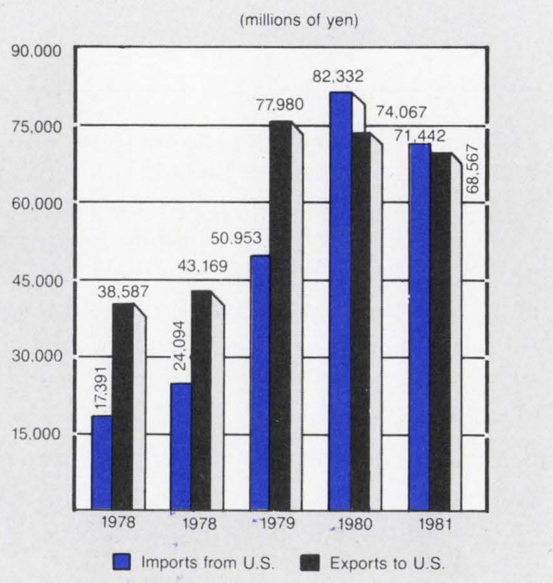
Another dichotomy found in the market is the split between custom and standard products. Although the custom type dominated the 1981 market for on-line systems, accounting for $8.8 million or a hefty 62% of the $14.3 million total, the standard product will prevail in both dollars and units after 1983.

Further details of the study are available from Insight Associates, PO Box 2829, Carson City, NV 89702. Tel. (702) 882-8893.

US Invades Japan

To balance the harsh criticism leveled at Japan over the years, for "invading" US markets for automobiles, household appliances, audio and video products, and semiconductors (among others), a recent report written from the Japanese point of view indicates concern on their part about US competition in the Japanese semiconductor industry.

Entitled "Semiconductor/Microelectronic Industry in Japan," it addresses the issue of US-Japanese competition by pointing out that US companies have steadily increased their market presence in Japan over the past 14 years. Beginning in 1968 with the establishment of Texas Instruments Japan Ltd. as a joint venture with



Source: Japanese Government Statistics on Foreign Trade

Figure 1: US-Japan balance of trade in semiconductors indicates a large market for American companies in Japan.

Sony Corporation, US companies determined to reciprocate Japanese moves into the US have begun to explore the Japanese semiconductor market. Other than TI, companies which have established Japanese affiliations include such heavyweights as American Microsystems, Fairchild, Motorola, AMD, Signetics, ITT, Intel, Zilog, and Mostek. Other companies such as Analog Devices, General Instrument, Teledyne, Rockwell, Harris Semiconductor, National Semiconductor, and Monolithic Memories have established branch offices in Japan. To date, however, TI (independent of Sony since 1971) is the only US-capitalized company actually manufacturing ICs in Japan. IBM has announced plans to build a manufacturing facility and start mass production in 1983. Intel plans to make ICs in Japan sometime after 1983, and Motorola (presently affiliated with the Japanese firm Aizu Toko) is expected to build its own production plant as well.

As the world's second largest consumer of semiconductor products, as well as the second largest producer, there is clearly a large market for American companies in Japan. With mutually-agreed-upon tariff rates of 4.2% to be in effect starting in January 1983, the friction between the two countries should lessen, and both should benefit from the large markets each has to offer. Nontariff barriers still remain, however, and these are discussed in the report as well.

"Semiconductor/Microelectronic Industry in Japan," a 200-page study prepared by Yano Economic Research Company, Ltd., takes an in-depth look at the present state of the semiconductor industry in Japan. Coverage includes: the structure of the industry; manufacturers' market shares and characteristics; technology trends; market forecasts by end-use application; and detailed profiles of 30 major Japanese semiconductor manufacturers.

Further information can be obtained from Mary O'Connor, Venture Development Corporation, One Washington Street, Wellesley, MA, 02181. Tel: (617) 237-5080.

Sevenfold Market Increase Projected For Voice Digitizing By 1985

Voice digitizing, previously limited to overseas channels and very long distance circuits, is becoming a commonly encountered network device, according to a new market report by Frost and Sullivan, Inc.

A market for 30,000 devices through 1985 is forecast by the 170-page study, entitled, "The Emerging Market for Voice Digitizers." From $8.5 million in 1981, the market will expand nearly sevenfold to more than $60 million in 1985.

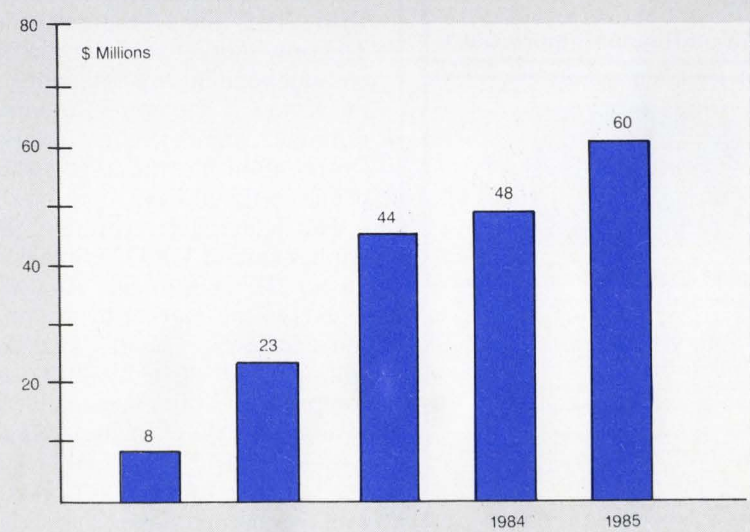
Recognizing this, many firms, especially the modem makers, will soon introduce voice digitizing products.

Some key factors underlie the optimistic projections:

- *Economics*: This includes the recent abolition of bulk rate discounts on TELPAK tariffs coupled with rate increases on private line and switched network services. Indeed, TELPAK users now pay between three and five times more for each circuit than was the case under the discounted tariff.
- *Semiconductors*: This technology will erode voice digitizer prices significantly. The digitizing algorithm in a device represents a large percentage of a unit's total cost, but with VLSI, costs will be cut in half.

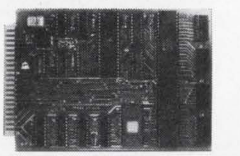
The net result of such developments: More than 20% of all major intercity connections will become suitable for voice/data integration via voice digitizing.

Other technology to provide a market impetus includes linear predictive coding. LPC simplifies the digitizing process, significantly reduces bandwidth requirements, and lends itself to secure voice



Source: Frost & Sullivan Inc.
(Report No. 1015)

Figure 1: The emerging market for voice digitizers could double sales in the near future.



implementation.

The development of standardized output protocols will also facilitate the integration of voice digitizers into both existing and planned data networks. X.25 compatibility, for example, will encourage the use of digitizers on packet switching networks.

Such a network application in fact, "represents a potential market that could easily double the sales of voice digitizers. Typical voice conversation generates lull periods that account for as much as 75% of a phone call's duration.

Still another favorable trend is the storage of digitized voice in computer systems. Voice digitizing permits "store and forward" messages, thereby opening up a new concept for linking offices of the future.

For further information, contact Customer Service, Frost & Sullivan, 106 Fulton Street, New York, NY 10038.

Tel: (212) 233-1080. Report #A1015.

Alphanumeric CRT Terminal Shipments To Exceed 3 Million Units In 1986

According to Venture Development Corporation's latest study on the alphanumeric CRT terminal industry, shipments will exceed 3 million units in 1986. Over 65% of these terminals will be shipped to the open market rather than sold to "captive" system purchasers. Although open market shipments will have a larger share of the shipments in 1986, they will grow at a slower rate than captive market shipments.

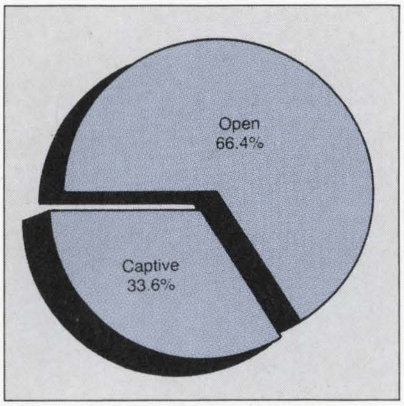


Figure 1: 1986 Market share by captive vs. open market segments.

Industry leaders in today's alphanumeric CRT terminal market are systems manufacturers such as IBM, DEC and Hewlett-Packard. The only market segment that has an independent manufacturer as the leader is the non-3270 editing terminal area where Teletype Corporation has the largest share of the installed base.

The VDC study entitled "The Alphanumeric CRT Terminal Industry III: A Strategic Analysis" segments the market by "dumb"/ conversational, "smart"/ non-3270 editing and "smart"/3270 and compatible editing terminals. According to VDC analyst Wendy Abramowitz, "The dumb terminal segment of the CRT market will continue to lose share over the next five years. Most dumb terminal manufacturers will be upgrading their products and producing more smart terminals. These two market segments will eventually merge into one."

In addition to discussing conversational, non-3270 editing and 3270 and compatible editing terminals, the study segments shipments by captive and open markets, distribution channel, applications and industry participants. There are detailed analyses of industry structure, the impact of graphics on the alphanumeric CRT terminal market, emerging plug-compatible markets, foreign competition, vertical integration, pricing and ergonomics.

Further information can be obtained from Wendy Abramowitz, Market Research Analyst, Venture Development Corporation, One Washington Street, Wellesley, MA, 02181. Tel: (617) 237-5080.

Bus Switches Ease Peripheral Costs

In many existing systems, peripherals such as tape and disk drives are often more expensive than the CPU.

One alternative to the costly approach of simply buying more peripherals, recently introduced by MDB, is to switch whole sections of the CPU bus (complete with all attached peripherals and memory) between the processors.

The MLSI-DB11-S family of bus switch modules uses standard Q-bus backplanes. They can share a single peripheral between two CPU's or multiple peripherals and memories between several CPU's in various combinations.

When the family is divided into its respective categories, it can be seen that there are a number of modules in each: MLSI-DB11-SA (5 boards), SB(2 boards), SC(4 boards), SG(1 board). Depending on the sort of system switch the user intends to configure, he will distribute these modules among

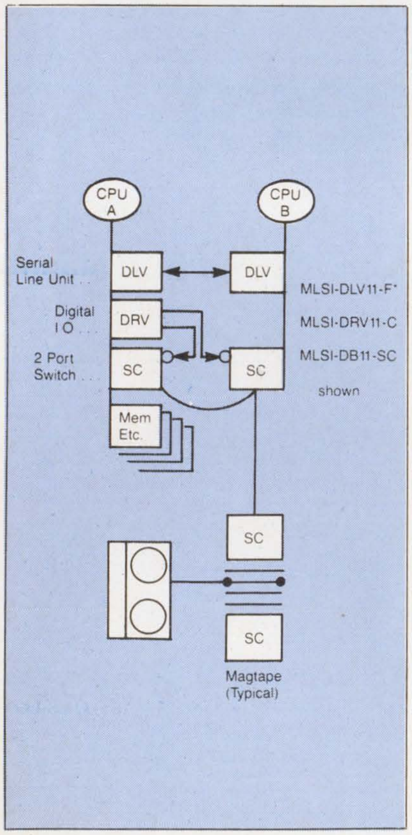


Figure 1: Program control from one CPU.

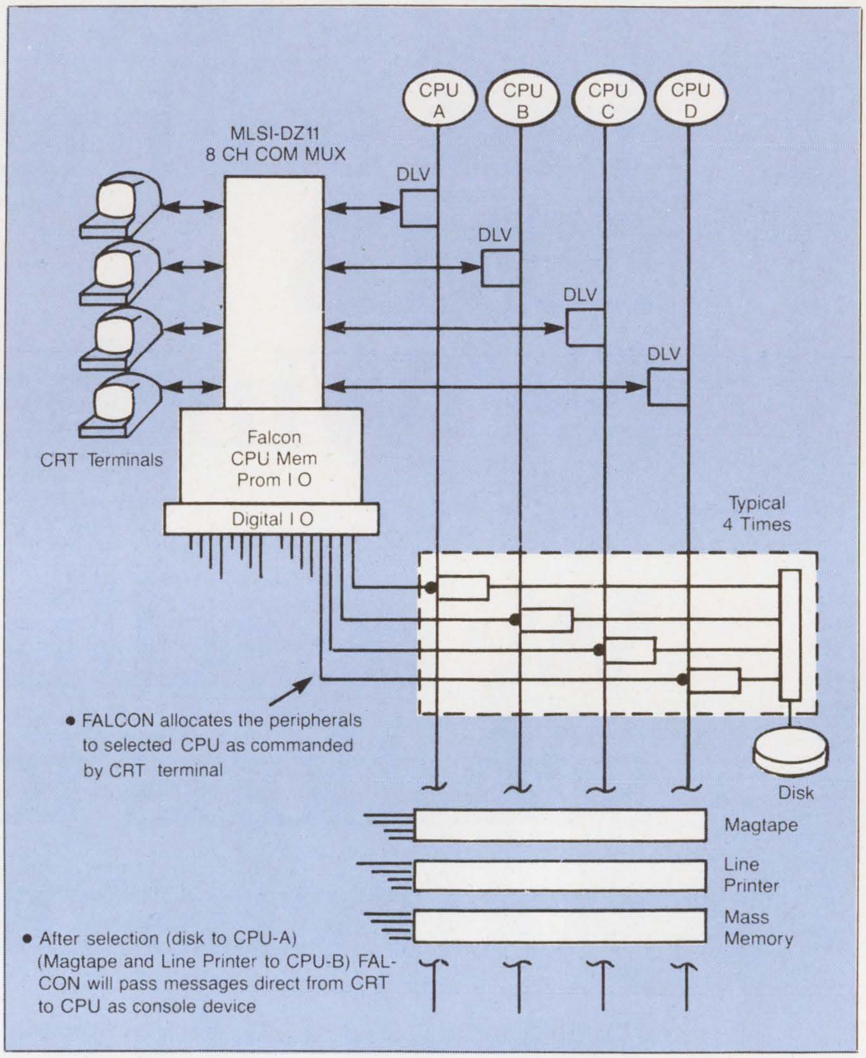


Figure 2: Transparent switch control through CRT terminals.

the various computers of this multiprocessor system.

In documenting the product line, MDB has highlighted a number of design examples. The two configurations illustrated here outline both the method for switching the shared bus from one CPU to another and transparent control through CRT terminals.

Figure 1 shows how one processor in the system can provide system switch control through a digital I/O module. A dual processor system is shown using the MLSI-DB11-SC. A MLSI-DRV11-C digital I/O module is used for control.

Upon power up, CPU-A will be connected to the shared bus. CPU-B can request the shared bus through the serial link (MLSI DLV11-F). When CPU-A is finished using the shared bus it will switch the bus to CPU-B and inform it through the serial link. CPU-A will not switch the shared bus back to itself until it makes sure CPU-B is free to release it by dialogue through the DLV link. This approach requires some software but can be handled through standard drives (DLV, DRV11C).

Figure 2 shows a control system which allows any of the system CPU's to be powered-down. The system user can select any of the

available CPU's with any combination of available switched resources through a CRT terminal. The key to this system is a minimal stand alone control processor (such as a Falcon) and a communications multiplexer (such as an MLSI-DZ11).

When a terminal sends a message to the Falcon, the software looks for a special character and a request to obtain a CPU and a particular set of peripherals. The Falcon sends back messages to the terminal as it grants or rejects the requests and configures the system. When the user is satisfied, the user asks to be connected to the CPU. The Falcon then passes through messages from the terminal to the CPU and vice versa. In this way the CRT becomes the console device for its chosen CPU with peripherals selected for the task.

> *These examples are only two of numerous configurations and applications explained in the MLSI-DB11-S users' guide, available from MDB.*

Several CRT's can be requesting at a time. The Falcon can allocate devices based upon priority established in a look-up table in its memory. The software to support the activity described above can be stored in Falcon PROM and message storage in the RAM.

This would be an ideal control system for the 4CPU × 4 shared bus system shown above. It would include virtual terminals and an assignable peripheral CPU pool. *MDB Systems, 1995 N. Batavia St, Orange, CA 92665.* **Write 198.**

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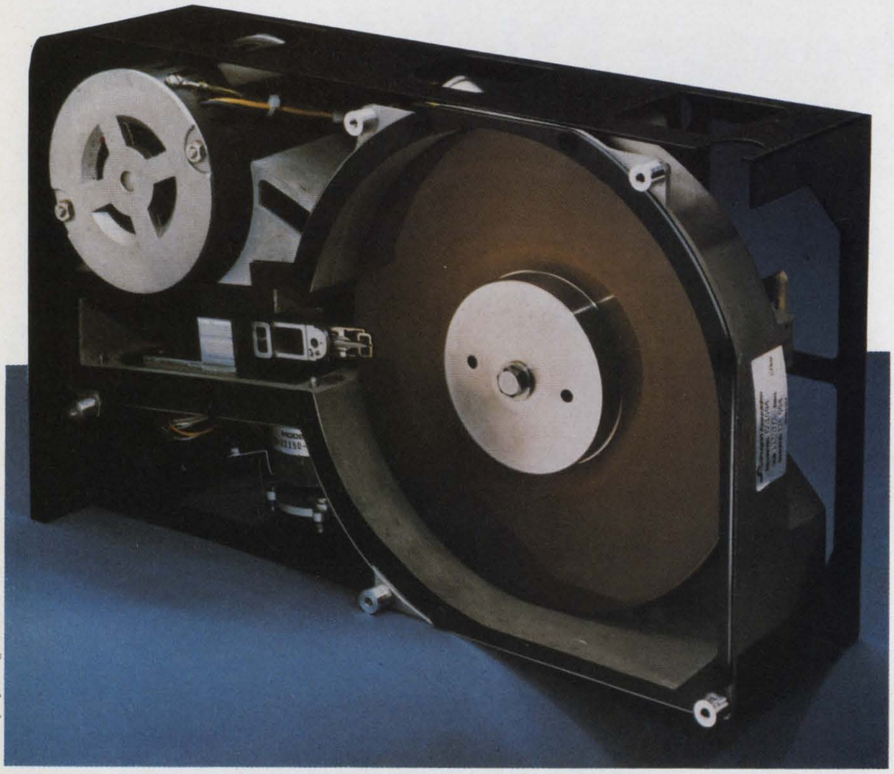

Courtesy of Shugart Associates

Growth of the small systems market has spawned a wave of new companies and innovative technologies.

Keeping Up With Winchesters

by Bob Hirshon

Keeping pace with Winchester technology is fast becoming a hopeless endeavor. First of all, there's the sheer number of new companies entering the field. Then there are the established companies moving into new areas of disk drive manufacture—as well as other companies moving out of new areas. The technology itself is changing, with thin film media and read/write (R/W) heads making a prolonged debut, and new twists in head positioning being announced on a seemingly daily basis. And market forecasters invariably make it a point to mention off-handedly that it won't be long before optical and holographic storage techniques will eclipse Winchesters altogether.

The reason for all this activity is the growth of the small computer systems market. Market research firms, such as Frost & Sullivan (New York, NY) expect $50 billion will be spent during the 1980s on small business computers (the largest segment of the small computer market). Many of these will either incorporate Winchester drives from the start, or upgrade to them as the small businesses grow into larger ones. The same will be true of small computers used at home and as engineering tools. Using predictions such as these, start-up Winchester companies have convinced venture capital firms that small Winchesters are a sure-thing investment. The result is a proliferation of well-financed small-Winchester manufacturers hoping to ride the coattails of the small computer market.

Head Positioning

To survive in this competitive market, these companies are offering improved performance and capacity specs. This increased performance hinges directly on quick, accurate R/W head positioning. Companies have focused their R&D in this area, and, as a result, head positioning techniques have become the chief distinguishing feature among the new crop of small Winchester drives.

The two major categories of R/W head positioning are *closed-loop* (meaning the heads sense their location from reference data stored on the disk surface and feed this information back to the actuator for more precise positioning) and *open-loop* (which operate blindly, relying on the mechanical accuracy of the actuator mechanism to find the proper track.)

Open-loop systems are inexpensive, reliable, simple and generally use older, proven components—the entire positioning system may consist merely of a stepper control, amplifier, and a stepper motor connected to the R/W heads by a radial armature. However, because the R/W heads are not position-sensing, they are limited by the accuracy of the stepper motor and the precision of the mechanical components moving the heads. In addition, they are prone to physical and environmental effects, such as vibration and thermal expansion. Consequently, open-loop positioning systems are limited to lower capacity drives with lower track densities (200 to 300 tracks per inch).

The term "closed-loop system" is synonymous with "servo" or "feedback system": a servo head

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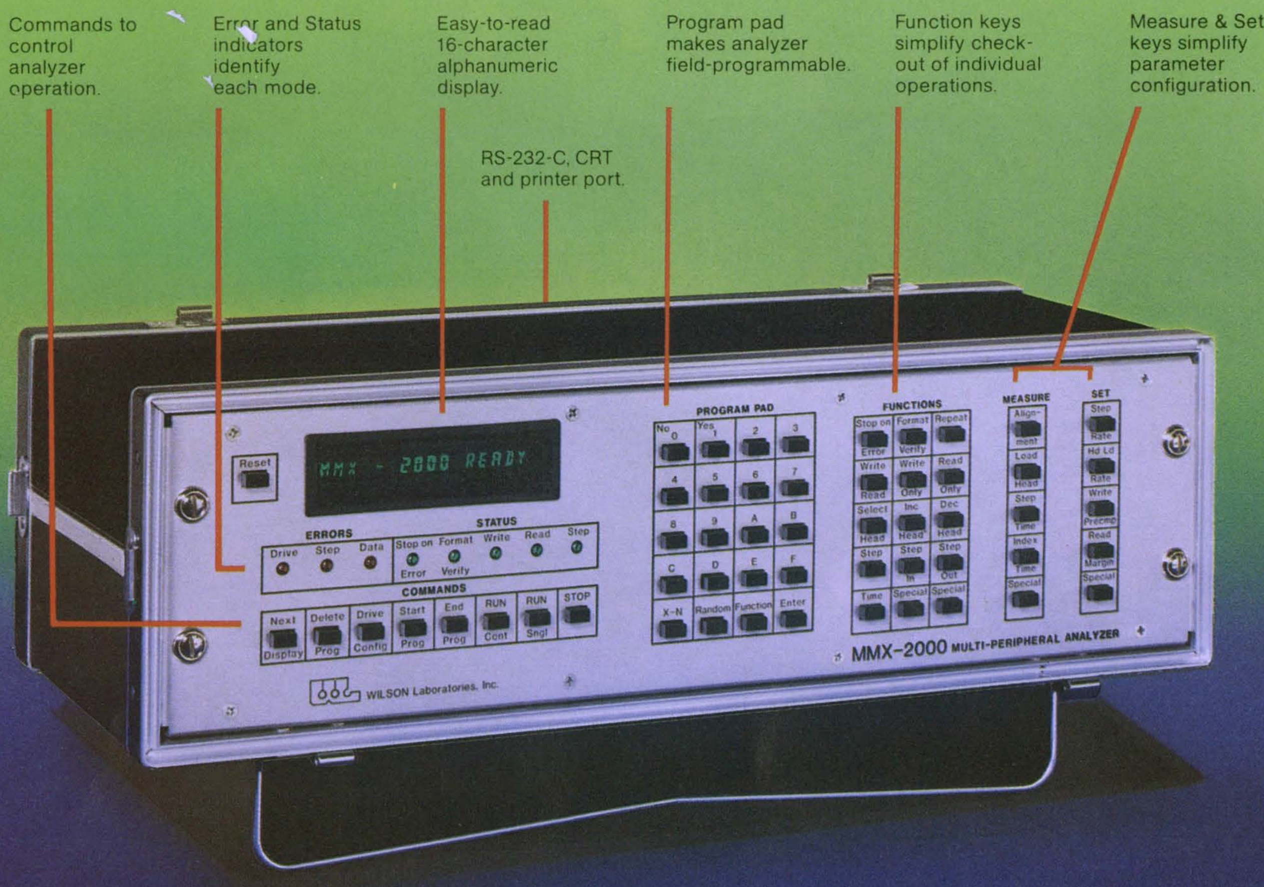

Cartridge Tape Drive Myth No. 4:

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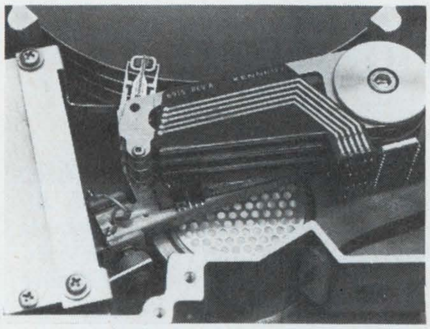


Figure 1: Kennedy's positioning system is a voice coil rotary actuator with the voice coil placed near the read/write heads (instead of behind the arm pivot).

reads reference information that was permanently written onto the disk's surface during manufacture. The servo head then feeds back this positioning information to the actuator that controls head movement. This feedback loop keeps the heads on-track, compensating for any mechanical off-tracking.

Closed-loop systems may be either *dedicated* servo systems or *embedded* servo systems. Dedicated systems reserve one disk surface solely for reference data. A servo head, flying over the surface, positions itself according to this reference data. Physically attached to the R/W heads operating on the other disk surface(s), the servo head thereby leads the R/W heads to their proper track. The main drawback of dedicated systems is that one entire disk surface must be devoted to reference data, and is therefore unavailable for regular data storage. In addition, because the servo head is mechanically attached to the R/W heads, mechanical and environmental factors may introduce some off-tracking. For example, the servo head may be perfectly on-track, but under extreme thermal stress, the attached R/W heads may be slightly off.

Embedded servo systems overcome these problems by embedding positioning data right onto the data storage tracks; the R/W heads act as the servo heads. While this eliminates off-tracking problems, there is some loss of performance, since the heads must perform double-duty.

R/W head positioning may be accomplished by either stepper motor or voice coil. Stepper motor positioning—the more common method—limits track density by virtue of the size and precision of the motor's steps. Voice coil actuators allow continuous R/W head movement, and therefore increased accuracy and track density.

Thin Film's Long Debut

Thin film media and R/W heads allow greatly increased data densities, and have been available for well over a year. Still, while some companies use them (notably, Seagate Technologies and Datapoint), most do not. This is because Win-

SASI Defined

by Gilbert Shepherd, V.P. of Marketing, Cynthia Peripherals, Inc., Palo Alto, CA.

SASI is an acronym for Shugart Associates Systems Interface. It is a developing industry and ANSI standard (ref. ANSI document X3T9.3 dated 4/2/82) interface for connecting disk drives to a host computer system. Its primary objective is to provide host computers with device independence, within a type of device. Thus, disk drives, tape drives, printers and even communication devices, of different type, can be added to the host computer without requiring modifications to generic system hardware or software.

SASI basically defines a hardware specification, i.e. numbers of pins and connectors; and a software specification, i.e. the command structure through which information will be transmitted. It differs from many industry-available controllers in that it is an intelligent interface. Many of the functions currently incorporated in a controller are now included on the drive side of the SASI interface. For this reason it is called an intelligent interface.

A typical SASI interface will have the following features:

- 50 pin connector at end port
- Up to 8 Bus Ports
- 9 Data Lines—9 Signal Lines per Port
- Timing of Signal Lines on Each Port
- Command and Message Protocol
- Logical Interface
- Open Collector or Differential Drivers and Receivers

Up to 8 SASI devices can be supported by the SASI bus. They can be any combination of host CPUs and intelligent controllers. This is shown in **Figure 1** which is a SASI Complex System, and is illustrated with 5 Control Units and 3 Computers with Host Adaptors (8 devices total).

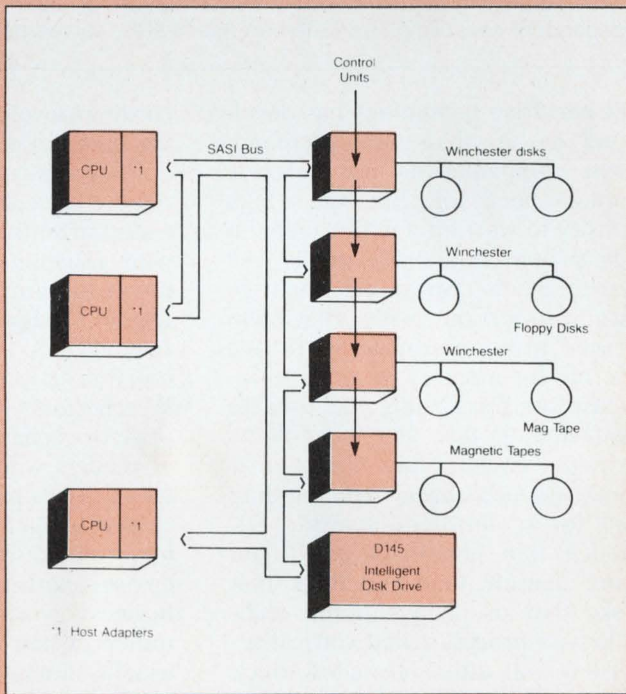


Figure 1: The SASI bus supports up to eight SASI devices, which can be any combination of host CPUs and intelligent controllers.

Back-Up Standards And Non-Standards

Explosive as the small Winchester market is, Winchester back-up is even more so, with floppy drives, tape drives, and Winchester cartridges all vying for market share.

Floppy disk drive manufacturers are trying to grow out of their low-capacity pigeonhole. Currently they are perceived as low-end Winchester back-up; however, much of the action in the Winchester market is in high-capacity small Winchesters. To take advantage of this growing, new market, floppy drive manufacturers are moving towards higher data densities using improved media. Iomega (Ogden, UT) gets ultra-high density on their floppy disk by encasing it within a protective cartridge. Although the cartridge is far heavier and more unwieldy than a standard floppy disk, it provides 10 Mbytes of removable memory on a single disk. Furthermore, the drive is highly insensitive to shock and atmospheric contaminants. Amlyn (San Jose, CA) provides high capacity by using a cartridge of five high-density flexible disks.

Winchester manufacturers are incorporating cartridges of their own as integral back-up. Removable Winchesters are currently offered by Cynthia Peripherals, Control Data Corp, DMA Systems, Data Peripherals, New World Computer, Seagate Technology, SyQuest, and Western Dynex.

Tape drive manufacturers aim to take the lion's share of the high-capacity Winchester back-up market, but to do so they must standardize both their interface and their recording format, so that OEMs will be assured of device compatibility and ready second-sources. In the area of quarter-inch cartridge drives, manufacturers put aside their differences this summer and formed the Working Group for Quarter-Inch Cartridge Drive Compatibility (with the somewhat perplexing acronym "QIC"). Ray Freeman, of the independent consulting firm Freeman Associates, served as mediator for the working group, which consisted of fifteen manufacturers: Adaptive Data and Energy Systems, Archive, Basic-4, BNR, Cipher Data Products, Computer Peripherals, Inc., Data Electronics, Kennedy, Memorex, Moya, Qantex, Sankyo-Seiki, Tandberg Data (Innovative Data Technology, American distributor), 3M, and Western Digital. The group submitted their proposed interface to the American National Standards Institute (ANSI) and the European Computer Manufacturers' Association (ECMA) for consideration. They are now working on recording standards.

The Winchester back-up arena has also attracted a number of non-standard tape technologies. Rosscomp Corp (Cerritos, CA), for example, recently introduced a tape system that stores 160 Mbytes on a 4″ reel holding 600′ of ½″ computer grade tape. The system has a dump/restore time of 20 minutes for 160 Mbytes and a 140 Kbyte/sec transfer rate. The device will be available by year's end, and will cost under $1000 (with quarter inch cartridge interface) in OEM quantities (intelligent interfaces and intelligent disk/ tape controllers are available as options).

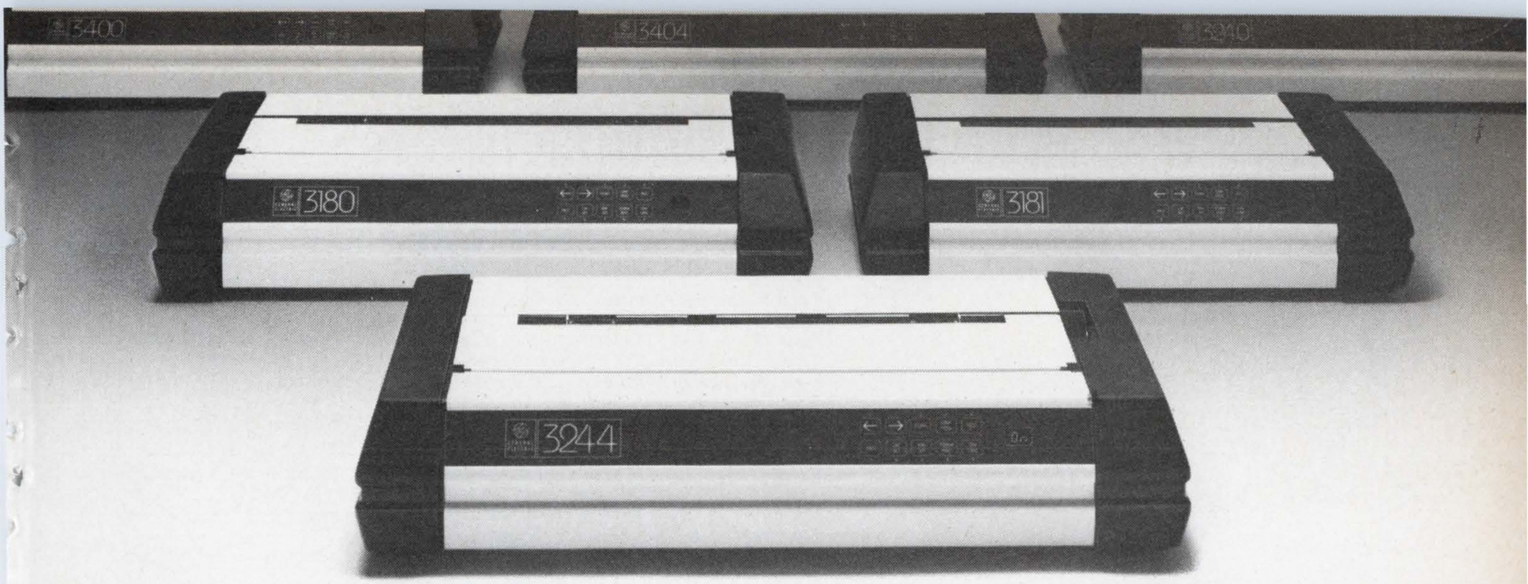
Pragma Data Systems (Sunnyvale, CA) is another company that uses standard ½″ tape in a non-standard manner. Their Model 2000 Direct Access Cartridge System uses ½″ tape cartridges measuring 4.87″ × 4.87″ × 1″ to store 80 Mbytes (formatted) with a read/write data frequency of 625 Kbytes/sec, and an 80 Mbyte formatted dump time of 7.4 minutes. The key feature of the design is that the tape is held stationary while the R/W heads are rotated within a loop of tape. Mass production difficulties have delayed the Model 2000's release, but it should be available by December. OEM price is $1985.

chester drive technology has developed faster than user demand. Most companies do not perceive enough need for thin film's high density to warrant a major technology switch from oxide media and ferrite heads. So rather than go into production with thin film drives now, manufacturers are waiting for memory demand to increase, and are using the time to perfect their thin film technology.

In the case of thin film media, some manufacturers are holding out for a different reason. Although thin film disks pack data more densely than can thick film disks that use conventional technology, a process called vertical recording will ultimately allow thick film media to store more data than thin film. Therefore, some manufacturers are staying with thick film, concentrating on vertical recording development, and bypassing thin-film disks altogether.

Conservatism may be a wise policy, since both OEMs and end users currently are more concerned with reliability than with performance or price. A June survey of **Digital Design** readers showed that reliability is their most important consideration when purchasing Winchesters—more important than price or capacity. Typical responses of readers who indicated that they chose drives based on reliability included: "Maintenance costs are a major marketing problem with otherwise relatively inexpensive small business systems"; "For our customers, when a disk goes down, it usually shuts down their whole system"; and "Reliability is what keeps the customers coming back." Some of the responses, apparently from OEMs who had been burned on Winchester deals in the past, had an almost militant tone: "If it doesn't work, I don't need it"; "Sooner or later a unit must be serviced, but it should be later than sooner"; and finally "Other criteria make no difference if you buy a piece of junk." In addition, a sizeable portion of our surveyed readers (61%) said that manufacturer's reputation is important.

This new conservatism seems to stem both from bad experiences our readers have had in the past with Winchesters, as well as a concern for today's enormous cost of servicing. This may make things difficult for all but the most heavily-backed of the new start-up firms, most of whom are banking on OEMs leaning towards new technologies and improved specs, rather than a long history and proven reputation.



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GENERAL ELECTRIC

Write 22 on Reader Inquiry Card

5¼" Winchester Manufacturers

MANUFACTURER	MODEL	CAPACITY (UNFORMATTED)	AVERAGE ACCESS TIME (MSECS)	TRACK-TO-TRACK ACCESS TIME	DATA TRANSFER RATE
Ampex Corp. El Segundo, CA Write 315	Pyxis 7	6.7 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	Pyxis 13	13.3 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	Pyxis 20	20.0 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	Pyxis 27	26.7 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
Atasi San Jose, CA Write 316	3020	19.84 Mbytes	30 msecs	3 msecs	5 Mbits/sec
	3033	33.07 Mbytes	30 msecs	3 msecs	5 Mbits/sec
	3046	46.3 Mbytes	30 msecs	3 msecs	5 Mbits/sec
Computer Memories, Inc. Chatsworth, CA Write 317	CM 5206	6.38 Mbytes	80 msecs	2 msecs	5 Mbits/sec
	CM 5412	12.76 Mbytes	80 msecs	2 msecs	5 Mbits/sec
	CM 5619	19.14 Mbytes	80 msecs	2 msecs	5 Mbits/sec
Corvus Systems San Jose, CA Write 318	6 MB Winchester Disk System	6.7 Mbytes	125 msecs		7.68 Mbits/sec
DMA Systems Goleta, CA Write 319	Micro-Magnum 5/5	13.50 Mbytes	40 msecs	3 msecs	5 Mbits/sec
	Micro-Magnum 5	6.75 Mbytes	40 msecs	3 msecs	5 Mbits/sec
Evotek Fremont, CA Write 320	ET-5810	12.90 Mbytes	49 msecs	3 msecs	8.2 Mbits/sec
	ET-5820	25.83 Mbytes	49 msecs	3 msecs	8.2 Mbits/sec
	ET-5830	38.75 Mbytes	49 msecs	3 msecs	8.2 Mbits/sec
	ET-5840	51.68 Mbytes	49 msecs	3 msecs	8.2 Mbits/sec
	ET-5510	7.81 Mbytes	49 msecs	3 msecs	5.0 Mbits/sec
	ET-5520	15.62 Mbytes	49 msecs	3 msecs	5.0 Mbits/sec
	ET-5530	23.43 Mbytes	49 msecs	3 msecs	5.0 Mbits/sec
	ET-5540	31.24 Mbytes	49 msecs	3 msecs	5.0 Mbits/sec
Fujitsu America Santa Clara, CA Write 321	M2231	6.6 Mbytes	95 msecs	18 msecs	625 Kbytes/sec
	M2232	10 Mbytes	95 msecs	18 msecs	625 Kbytes/sec
International Memories, Inc. Cupertino, CA Write 322	5006 H	6.38 Mbytes	85 msecs	3 msecs	625 Kbytes/sec
	5012 H	12.76 Mbytes	85 msecs	3 msecs	625 Kbytes/sec
	5018 H	19.14 Mbytes	85 msecs	3 msecs	625 Kbytes/sec
	5007 H	7.01 Mbytes	85 msecs	3 msecs	687.5 Kbytes/sec
	5014 H	14.03 Mbytes	85 msecs	3 msecs	687.5 Kbytes/sec
	5021 H	21.04 Mbytes	85 msecs	3 msecs	687.5 Kbytes/sec
Irwin Olivetti Ann Arbor, MI Write 323	510	12.3 Mbytes	33.32 msecs (w/settling time)	10 msecs (w/settling time)	5.4 Mbits/sec
	516	16.0 Mbytes	34 msecs (w/settling time)	10 msecs (w/settling time)	5.4 Mbits/sec
	416	16.0 Mbytes	34 msecs (w/settling time)	10 msecs (w/settling time)	5.4 Mbits/sec
	HD562/11	3.75 Mbytes	66 msecs	1.1 msecs	5 Mbits/sec
	HD562/12	7.5 Mbytes	66 msecs	1.1 msecs	5 Mbits/sec
	HD562/13	11.25 Mbytes	66 msecs	1.1 msecs	5 Mbits/sec
	HD561/2	7.5 Mbytes	120 msecs	2 msecs	5 Mbits/sec
Memorex Corp. Santa Clara, CA Write 324	306	6.7 Mbytes	170 msecs (95 msecs optional)	18 msecs	5 Mbits/sec
	310	10 Mbytes	170 msecs (95 msecs optional)	18 msecs	5 Mbits/sec
Micropolis Corp. Chatsworth, CA Write 325	1302	17.3 Mbytes	38 msecs	8 msecs	5 Mbits/sec
	1303	34.6 Mbytes	38 msecs	8 msecs	5 Mbits/sec
	1304	51.9 Mbytes	38 msecs	8 msecs	5 Mbits/sec
Miniscribe Corp. Longmont, CO Write 326	2006	6.4 Mbytes	85 msecs (w/settling time)	3.0 msecs	5.0 Mbits/sec
	2012	12.8 Mbytes	85 msecs (w/settling time)	3.0 msecs	5.0 Mbits/sec
	4010	10.0 Mbytes	120 msecs (w/settling time)	3.0 msecs	5.0 Mbits/sec
	4020	20.0 Mbytes	120 msecs (w/settling time)	3.0 msecs	5.0 Mbits/sec
Mitsubishi Electronics Compton, CA Write 327	M4863 1	3.33 Mbytes		3 msecs	5 Mbits/sec
	M4863 2	6.66 Mbytes	75 msecs (w/settling time)	3 msecs	5 Mbits/sec
	M4863 3	10.0 Mbytes	75 msecs (w/settling time)	3 msecs	5 Mbits/sec

From only a handful of manufacturers last year, the 5¼" Winchester disk drive arena now contains 25 companies, and is growing every day. To obtain more information about these companies, write in the appropriate Write numbers on the *Digital Design* reader inquiry card.

RECORDING SURFACES	TRACK DENSITY	MTBF	INTERFACE	DIMENSIONS	PRICE (QTY)	COMMENTS
2	360 tracks/inch	12,000 hours	ST506	8"×5.75"×3.25"		
4	360 tracks/inch	12,000 hours	ST506	8"×5.75"×3.25"		
6	360 tracks/inch	12,000 hours	ST506	8"×5.75"×3.25"		
8	360 tracks/inch	12,000 hours	ST506	8"×5.75"×3.25"	$1135 (1000)	
3	800 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$1470 (1000)	
5	800 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$1800 (1000)	
7	800 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
2	345 tracks/inch	8,000 hours	ST506	8"×5.75"×3.25"	$1050 (500)	
4	345 tracks/inch	8,000 hours	ST506	8"×5.75"×3.25"		
6	345 tracks/inch	8,000 hours	ST506	8"×5.75"×3.25"		
4			S-100 and other personal computers	15"×12"×5.75"	$3195 (1)	
4	454 tracks/inch	8000 hours	ST506	10.5"×5.75"×3.25"	$1275	Uses one fixed and one removable disk.
2	454 tracks/inch	8000 hours	ST506	10.5"×5.75"×3.25"	$995	Uses one removable disk cartridge
2	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
4	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
6	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
8	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$2225 (1000)	
2	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
4	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
6	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
8	367 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
4	254 tracks/inch	10,000 hours	ST506 (SA4000 available)	8"×5.7"×3.3"		
6	254 tracks/inch	10,000 hours	ST506 (SA4000 available)	8"×5.7"×3.3"	$1050 (1000)	
2	303 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
4	303 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$740 (1000)	
6	303 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
2	303 tracks/inch	10,000 hours	IMI	8"×5.75"×3.25"		
4	303 tracks/inch	10,000 hours	IMI	8"×5.75"×3.25"		
6	303 tracks/inch	10,000 hours	IMI	8"×5.75"×3.25"		
2	900 tracks/inch	8,000 hours	Unique interface accommodates	8"×5.75"×3.25"	$1650 (500)	Available w/S-100 and Multibus host adapters and CP/M software package
2	900 tracks/inch	8,000 hours	disks and integral tape drive	8"×5.75"×3.25"	$1794 (500)	
2	900 tracks/inch	11,000 hours	compatible w/Irwin 510 or 516 for system expansion	8"×5.75"×3.25"	$1140 (500)	
2	254 tracks/inch	8,000 hours	ST506	8"×5.75"×3.25"		
4	254 tracks/inch	8,000 hours	ST506	8"×5.75"×3.25"		
6	254 tracks/inch	8,000 hours	ST506	8"×5.75"×3.25"		
4	254 tracks/inch	8,000 hours	SA1000	8"×5.75"×3.25"		
4	254 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
6	254 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"		
2	960 tracks/inch		ST506	8"×5.75"×3.25"	$900 (1000)	
4	960 tracks/inch		ST506	8"×5.75"×3.25"		
6	960 tracks/inch		ST506	8"×5.75"×3.25"	$1400 (1000)	
2	402 tracks/inch	8,000 hours	ST412 (or ST506)	8"×5.75"×3.25"	$600 (1000)	
4	402 tracks/inch	8,000 hours	ST412 (or ST506)	8"×5.75"×3.25"	$675 (1000)	
2	588 tracks/inch	8,000 hours	ST412 (or ST506)	8"×5.75"×3.25"	$625 (1000)	
4	588 tracks/inch	8,000 hours	ST412 (or ST506)	8"×5.75"×3.25"	$750 (1000)	
2	256 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$740 (500)	
4	256 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$900 (500)	
6	256 tracks/inch	10,000 hours	ST506	8"×5.75"×3.25"	$1100 (500)	

MANUFACTURER	MODEL	CAPACITY (UNFOR-MATTED)	AVERAGE ACCESS TIME (MSECS)	TRACK-TO-TRACK ACCESS TIME	DATA TRANSFER RATE
New World Computer Irvine, CA Write 328	2/0 Microdisk V	2 Mbytes	19 msecs	3 msecs	6.25 Mbits/sec
	4/0	4 Mbytes	19 msecs	3 msecs	6.25 Mbits/sec
	2/2	2 Mbytes fixed, 2 Mbytes removable	19 msecs	3 msecs	6.25 Mbits/sec
	4/2	4 Mbytes fixed, 2 Mbytes removable	19 msecs	3 msecs	6.25 Mbits/sec
	4/4	4 Mbytes fixed, 4 Mbytes removable	19 msecs	3 msecs	6.25 Mbits/sec
Nippon Peripherals Kanagawa, Japan Write 329	NP05-6	6.67 Mbytes	175 (w/settling)	18 msecs	5 Mbits/sec
	NP05-10	10.0 Mbytes	175 (w/settling)	18 msecs	5 Mbits/sec
NEC Lexington, MA Write 330	5210	6.38 Mbytes	102 msec (w/settling time)	17 msecs	625 Kbytes/sec
Nissei-Sangyo America Write 331	DK501-1	6.7 Mbytes	78 msecs (w/settling time)	17 msecs	5 Mbits/sec
	2	10.0 Mbytes	78 msecs (w/settling time)	17 msecs	5 Mbits/sec
	3	13.1 Mbytes	78 msecs (w/settling time)	17 msecs	5 Mbits/sec
Priam Corp. San Jose, CA Write 332	Diskos 502	50 Mbytes	35 msecs	10 msecs	625 Kbytes/sec
Rodime Ltd. Mission Viejo, CA Write 333	RO 201	6.67 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	RO 202	13.33 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	RO 203	20.00 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	RO 204	26.67 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	RO 206	40.00 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
	RO 208	53.34 Mbytes	90 msecs (w/settling time)	18 msecs	5 Mbits/sec
Rotating Memory Systems Milpitas, CA Write 334	RMS 504	4.5 Mbytes	70 msecs	2 msecs	5.0 Mbits/sec
	RMS 507	6.38 Mbytes	77 msecs	2 msecs	5.0 Mbits/sec
	RMS 509	9.0 Mbytes	70 msecs	2 msecs	5.0 Mbits/sec
	RMS 513	13.5 Mbytes	70 msecs	2 msecs	5.0 Mbits/sec
	RMS 514	12.75 Mbytes	77 msecs	2 msecs	5.0 Mbits/sec
	RMS 518	18 Mbytes	70 msecs	2 msecs	5.0 Mbits/sec
	RMS 519	19.13 Mbytes	77 msecs	2 msecs	5.0 Mbits/sec
	RMS 526	25.5 Mbytes	77 msecs	2 msecs	5.0 Mbits/sec
Seagate Technology Scotts Valley, CA Write 335	ST 506	6.38 Mbytes	170 msecs (reducible to 95 msecs)	3 msecs	5.0 Mbits/sec
	ST 406	6.38 Mbytes	85 msecs (including settling)	3 msecs	5.0 Mbits/sec
	ST 412	12.76 Mbytes	85 msecs (including settling)	3 msecs	5.0 Mbits/sec
	ST 419	19.14 Mbytes	85 msecs (including settling)	3 msecs	5.0 Mbits/sec
	ST 706	6.38 Mbytes	85 msecs (including settling)	3 msecs	5.0 Mbits/sec
Shugart Associates Sunnyvale, CA Write 336	SA 602	3.33 Mbytes	84 msecs	3 msecs	5.0 Mbits/sec
	SA 604	6.66 Mbytes	84 msecs	3 msecs	5.0 Mbits/sec
	SA 606	10.0 Mbytes	84 msecs	3 msecs	5.0 Mbits/sec
Tandon Corp. Chatsworth, CA Write 337	TM 602	6.38 Mbytes	98 msecs	3 msecs	5.0 Mbits/sec
	TM 603	9.57 Mbytes	98 msecs	3 msecs	5.0 Mbits/sec
	TM 603 E	14.4 Mbytes	137 msecs	3 msecs	5.0 Mbits/sec
	TM501	6.4 Mbytes	110 msecs	2 msecs	5.0 Mbits/sec
	TM502	12.8 Mbytes	110 msecs	2 msecs	5.0 Mbits/sec
	TM503	19.1 Mbytes	110 msecs	2 msecs	5.0 Mbits/sec
	TM703	31.0 Mbytes	39 msecs	5 msecs	5.0 Mbits/sec
Texas Instruments Houston, TX Write 338	525/61	6.38 Mbytes	100 msecs	3 msecs	5 Mbits/sec
	525/122	12.76 Mbytes	100 msecs	3 msecs	5 Mbits/sec
Western Dynex Phoenix, AZ Write 339	WD 505	6.38 Mbytes	35 msecs	3 msecs	5.0 Mbits/sec

RECORDING SURFACES	TRACK DENSITY	MTBF	INTERFACE	DIMENSIONS	PRICE (QTY)	COMMENTS
1	250 tracks/inch	10,000 hours	ST506, S-100, universal	8.0″ × 5.75″ × 2.125″	$496 (500)	
2	250 tracks/inch	10,000 hours	same as above	8.0″ × 5.75″ × 2.125″	$756 (500)	
1 fixed, 1 removable	250 tracks/inch	10,000 hours	same as above	8.0″ × 5.75″ × 1.125″	$836 (500)	
2 fixed, 1 removable	250 tracks/inch	10,000 hours	same as above	8.0″ × 5.75″ × 3.25″	$996 (500)	
2 fixed, 2 removable	250 tracks/inch	10,000 hours	same as above	8.0″ × 5.75″ × 3.25″	$1196 (500)	
4	254 tracks/inch	10,000	ST506	8″ × 5.75″ × 3.25″		
6	254 tracks/inch	10,000	ST506	8″ × 5.75″ × 3.25″		
4	200 tracks/inch		ST506	8″ × 5.75″ × 3.25″		
4	254 tracks/inch	20,000 hours	ST506	8″ × 5.75″ × 3.25″		
6	254 tracks/inch	20,000 hours	ST506	8″ × 5.75″ × 3.25″		
8	254 tracks/inch	20,000 hours	ST506	8″ × 5.75″ × 3.25″		
8	960 tracks/inch	8,000 hours	ST506 (PRIAM and ANSI available later)	10″ × 5.75″ × 3.25″	$2000 (500)	
2	600 tracks/inch		ST506	8″ × 5.75″ × 3.25″	$720 (100)	
4	600 tracks/inch		ST506	8″ × 5.75″ × 3.25″	$890 (100)	
6	600 tracks/inch		ST506	8″ × 5.75″ × 3.25″	$1,060 (100)	
8	600 tracks/inch		ST506	8″ × 5.75″ × 3.25″	$1285 (100)	
10	600 tracks/inch		ST506	8″ × 5.75″ × 3.25″	$1735 (100)	
12	600 tracks/inch		ST506	8″ × 5.75″ × z3.25″	$2050 (100)	
2	270 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
2	383 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
4	270 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
6	270 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
4	383 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
8	270 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
6	383 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
8	383 tracks/inch	10,000 hours	ST506	8″ × 5.75″ × 3.25″		
4	255 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$875 (500)	
2	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″		
4	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$1050 (500)	
6	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″		
2	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″		Removable cartridge disk
2			SA 1000	8″ × 5.75″ × 3.25″		
4			SA 1000	8″ × 5.75″ × 3.25″		
6			SA 1000	8″ × 5.75″ × 3.25″		
4	255 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$545 (1000)	
6	255 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$680 (1000)	
6	255 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$795 (1000)	
2	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$545 (1000)	
4	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$680 (1000)	
6	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$795 (1000)	
6	600 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	— —	
2	417 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$1225 (1)	
4	417 tracks/inch	11,000 hours	ST412	8″ × 5.75″ × 3.25″	$1575 (1)	
2	345 tracks/inch	11,000 hours	ST506	8″ × 5.75″ × 3.25″	$495	Removable cartridge disk

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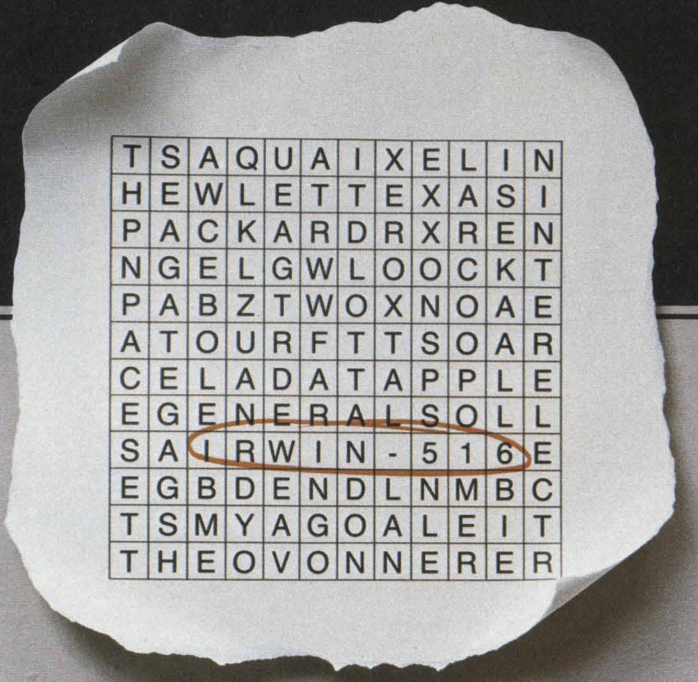

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μCs In Distributed Control Environments

by Martin B. Pawloski

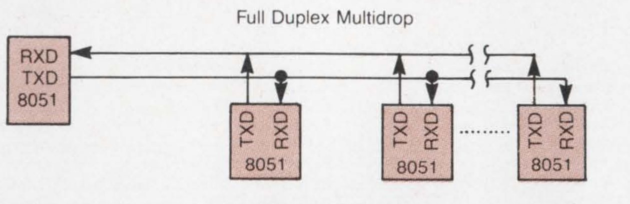

Figure 1: A full duplex, multidrop network.

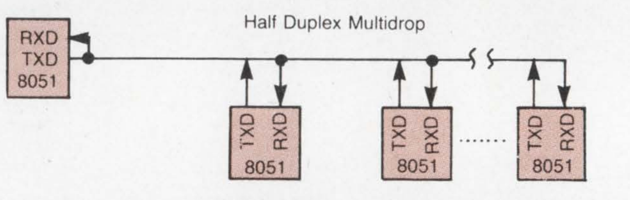

Figure 2: A half duplex, multidrop network.

The dramatic trend in recent years toward distributed control has clearly followed, and largely been a result of, the technology drive of the semiconductor industry. Historically, when computing power was very expensive—compared to the cost of interconnect—massive cabling harnesses and large backplanes tied the central computer to the various points of control. But now, due to the emergence of powerful and highly integrated μCs, the economics of system design has changed drastically. The inexpensive μC has made interconnect expensive relative to computing power. Current distributed control system architectures use numerous μCs within the system, while every effort is made to minimize the interconnect by using, for example, bit serial communications.

But there are reasons other than cost for using distributed control. Distributed control can also ensure higher system reliability by being able to isolate a failing control loop, or a node can be used to insulate the system from the noise encountered in various hostile surroundings. Another advantage of distributed control is that it enforces modular design methodology. By functionally partitioning the system and assigning individual nodes to particular tasks, hardware and software designs of large, complex systems are simplified, productivity is increased, and the debugging phase of the project is facilitated. This modular approach can also be used to allow system expandibility with little or no cost burden added to a base product. System expandability by means of serially interconnected distributed control can be used to greatly simplify field installation of options.

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The attributes of a distributed control system include independency of tasks (e.g., control of individual machines in automated factory environments, or the control of various sensors and actuators in process control environments). The μCs in distributed control systems are loosely coupled (i.e., they do not share a common memory), requiring a local memory store in each node. Again, to minimize interconnect, the internode communication is accomplished by a bit serial stream. A bit serial stream, though low in bandwidth, is sufficient due to the node's high level of intelligence.

Distributed Control Networks

A full duplex, multidrop network using 8051s is shown in **Figure 1.** This network architecture is useful when the master is required to know the complete state of the system, such as the command node of an energy-security system. The master 8051 initializes, monitors and can forward messages on the network. The master, after interrogating each slave 8051, which has a unique software-recognized address, would transmit appropriate control and/or data. Using the MCS-51 interprocessor communication protocol, up to 256 slave 8051s can be addressed in a single frame. Larger numbers of slaves can be addressed using multiframe addressing.

The μC is offering control system designers some new inexpensive alternatives.

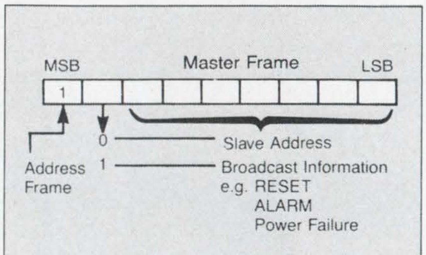


Figure 3: Network efficiency can be increased by defining software-recognized control bits in the address frame.

Distributed Control—The μC Emerges

The emergence of the μC has been implemented in the economic considerations of the control system designer, and the battle between centralized and distributed intelligent systems is now well under way.

Often, the smaller less publicized firms take up the ideas of the IC houses to build board and system level products.

One perfect example is from the Inconix Corp, Natick, MA. Its product, "CinchPac" **(Figure 1)**, is an intelligent measurement and control system based around the Intel MCS-51 family (in fact an 8031 with 2 Kbytes of RAM). One CinchPac board also includes conditioned interfaces for process and machine signals, and a serial interface for communications.

Single CinchPacs can operate independently or can be networked over long distances and high speeds as the lowest element in a distributed network, simplifying the process to computer interface and unburdening the host computer. Networked CinchPacs can also operate without the need for a host computer.

Supporting the network concept, Inconix's Cinchnet is designed to meet the EIA standard RS-485. Any unit at any node in the network can initiate messages automatically, without polling and without some other intelligent devices allocating communications time.

Cinchnet supports up to 124 nodes on the network, plus a "host" node. At any node, including the host address there can be "Gateways", (or entry points to the local area network) to terminals to computers for communications using standard RS-232-C units.

Cinchnet is a contention network, using ordinary twisted pair cable, not coax. Modems are not required. It operates at 57,600 baud at 4000 ft. The protocol which is built into every Gateway and into the CinchPac Operating System (CPOS) is called Carrier Sense Multiple Access/Collision Detection (CSMA/CD). The name resolves the question of how several units on the same lines can initiate messages at the same time. Two of the four wires carry a "busy" signal or carrier. A unit senses the carrier to determine whether it can initiate a message, via the other two wires. If the network is not busy, it turns the carrier or busy signal prior to transmitting. Given the speed and nature of 11MHz computers, there is a small but finite possibility that two or more units can detect that the line is not busy and attempt to transmit simultaneously. This is called a collision, which, as the name implies, is detected. Any transmitting unit listens to its own messages and determines whether they are transmitted properly. Each has to do so, to detect collisions. For a collision, CinchPacs and Gateways automatically calculate a small random delay for retransmission.

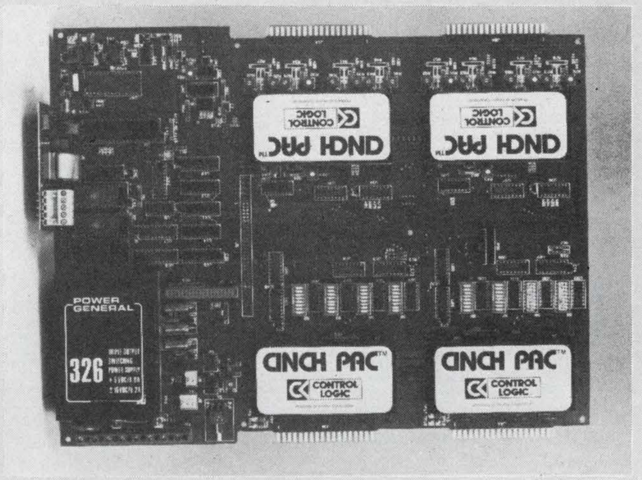


Figure 1: Iconix Corp.'s Cinch Pac is an intelligent measurement and control system based around the MCS-51 family.

These delays are based on each unit's Cinchnet address and therefore differ for different units.

CinchPacs may be commanded via Cinchnet to report certain values automatically as routine reports, on demand in reply to inquiries, or automatically as exception reports as for warning and alarm limit violations. These values are identified when the application programs are programmed. In the case of preprogrammed CinchPac Model 20, Warnings and Alarms, the reported values are the analog input channel values, in engineering units. For Model 30, PID Loop Control, the reported values are the current value for each loop update and the resulting output value. (There are two pairs of such values for cascaded loops). These models are preprogrammed. All the user/host has to do is issue the command to enable such automated reporting of important values for each program. The value identified for each application program is called its "principle value", the routine or on-demand reports of such principle values are regarded as "information channels" to the host. Once programmed, the host user can issue commands to selective-

A half-duplex network organization is shown in **Figure 2.** Though its instantaneous peak bandwidth is only one-half that of a full-duplex network, a half-duplex network offers two major advantages. First, it minimizes interconnect and thus is the lowest-cost network architecture. Secondly, it is possible for any two 8051s to communicate directly to each other without going through an intermediate node. In many real-time control applications where one distributed control node must quicky react to the data supplied by another node, the effective bandwidth of this network architecture can actually be greater than that of a full duplex architecture.

There are two basic methods for managing access and ownership of the serial channel. One way is for one of the 8051s in the network to be programmed as the network master. This master 8051 continually polls the slave 8051 nodes. Upon receiving a transmit request from a slave, the master passes ownership of the network to the requesting 8051, which can then transmit to any other 8051 in the network. Once the communication is completed, ownership is then passed back to the master, which in lieu of a pending transmission of its own, will continue to poll the slave 8051s.

Another method is to create a

ly control reporting on the information channels.

The range of tasks handled by CinchPac, illustrated in **Figure 2** go from on/off control (bit or Boolean manipulation) to very sophisticated continuous calculation and control (byte manipulation); this choice between bit and byte operation provides CinchPac's decision approach appropriate for the industrial task at hand.

For motion control, CinchPac compares present location (accurate to less than 0.00075″ in a foot of travel) to desired location and actuates a drive system to move in the fastest yet optimum (using the built in PID algorithm) speed. Control of speed is enhanced because CinchPac can respond to varying loads, again using the PID routine. Movement of parts and sequencing of operations is achieved in CinchPac by virtue of the 8031's programming capability. Batch operations involving recipe choice, ramp and soak sequences, and control of process variables are easily handled within one CinchPac. Then there is three mode (PID) and cascade, feedforward, feedback, etc. control of temperature, pressure, flow, level and force for process control oriented applications; limit checking provides alarm signals. Quality analysis involves high accuracy measurement of instrument signals; comparing to quality limits and reporting to a central data collection point are common CinchPac activities.

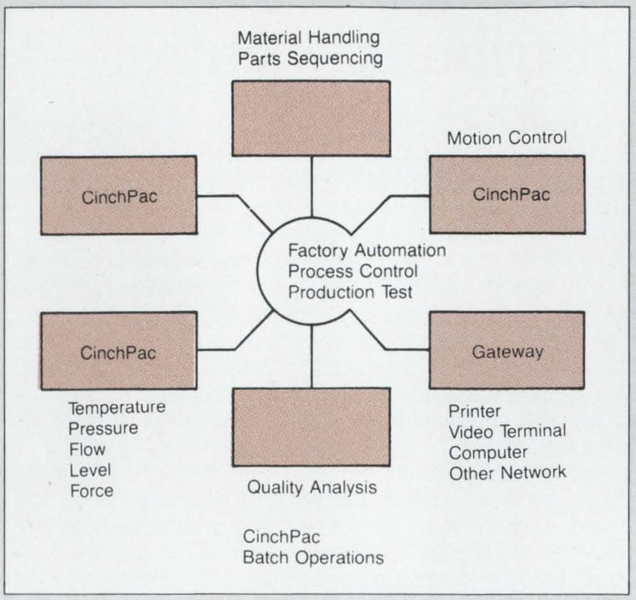


Figure 2: CinchPac with individual assignments interconnected with Cinchnet industrial network.

virtual ring and pass ownership of the serial channel around the ring. Ownership goes to the node that currently has the baton or token. When finished with the serial channel, the token is passed to the next node on the ring. The new owner of the channel will execute a transmission, request data to be sent to it, or not having any pending serial channel transactions, it will forward the token to the next node on the ring. At power up, one 8051 is programmed to assume mastership of the ring. From then on, mastership continually rotates around the ring. Averaged over time, every node has equal use of the common serial channel resource.

Network efficiency can be increased by defining software-recognized control bits in the address frame. An example of this is the ability to broadcast information to all nodes at the same time instead of transmitting the information to each node individually. For networks with a small number (‹128) of broadcast bits, see **Figure 3**. For larger networks, a specific address can be reserved for broadcast. In this case, upon notification that an address frame has been received, the 8051 would do two compares before enabling further data frame reception. One compare would be

```
PARITY INSERTION AND VALIDATION

;THIS ROUTINE INSERTS AN EVEN PARITY BIT
;IN THE OUTGOING DATA STREAM
;
PAR_INS;  MOV  ACC.7,P      ;MOVE EVEN PARITY INTO MSB OF DATA
          CLR  TI           ;CLEAR TRANSMIT INTERRUPT FLAG
          MOV  SBUF,A       ;LOAD TRANSMITTER BUFFER WITH DATA
          RET               ;RETURN TO CALLING ROUTINE

;
;PAR_VAL VALIDATES THE PARITY OF THE BYTE RECEIVED AND SETS THE
          CARRY IF THERE IS AN EVEN PARITY ERROR
;
PAR_VAL;  CLR  RI           ;CLEAR RECEIVER INTERRUPT FLAG
          MOV  A,SBUF       ;LOAD DATA JUST RECEIVED INTO ACCUMULATOR
          MOV  C,P          ;LOAD PARITY FLAG INTO CARRY. IF THE BYTE
                            ;IN THE ACCUMULATOR IS NOT EVEN PARITY, THE
                            ;PARITY FLAG WILL EQUAL 1
          RET               ;RETURN TO CALLING ROUTINE

CHECKSUM CALCULATION AND VALIDATION

;THIS ROUTINE CALCULATES THE CHECKSUM OF THE OUTGOING BYTES
;THE CURRENT VALUE OF THE CHECKSUM RESIDES IN THE ACCUMULATOR
;
CS_CALC:  XRL  A,@RO        ;XOR OUTGOING BYTE WITH ACCUMULATOR
          MOV  SBUF,@RO     ;LOAD TRANSMITTER BUFFER WITH DATA
          RET               ;RETURN TO CALLING ROUTINE
;
;WHEN ALL DATA HAS BE TRANSMITTED, THE CHECKSUM HAS TO BE SENT
;
SEND_CS;  MOV  SBUF,A       ;TRANSMIT CHECKSUM

;
;THIS ROUTINE VALIDATES THE CHECKSUM OF THE DATA RECEIVED
;AGAIN THE ACCUMULATOR CONTAINS THE CURRENT VALUE OF THE
CHECKSUM
;
CS_VAL:   XRL  A,SBUF       ;XOR BYE RECEIVED WITH ACCUMULATOR
;
;WHEN THE MESSAGE HAS BEEN COMPLETELY RECEIVED, THE CHECKSUM IS
CHECKED
;
CS_CHK;   JNZ  CS_ERR       ;IF ACCUMULATOR IS NOT ZERO, THERE IS
                            ;A CHECKSUM ERROR
```

Table 1: Programming examples for the 8051.

for the broadcast address (typically all 1s or all 0s); the other compare would be for the node's own unique ID. Upon recognition of an impending broadcast transmission, each 8051 node would enable itself to receive the complete transmission. Power up reset, system reset, power failure, alarm or time of day are examples of control information that would be broadcast to all nodes.

The integrity of the data being transmitted over the network can be ensured in a number of ways. Using the parity bit in the MCS-51 PSW, parity can be software inserted in outgoing bytes, or software validated on incoming bytes.

Another method that can be used independently or in conjunction with parity is calculating the check sum and inserting it as the last frame of the message. For the highest level of data integrity possible, at the expense of network bandwidth, a receiving MCS-51 node can echo all frames received from the transmitting node for its validation. **Table 1** shows programming examples of the possibilities discussed above.

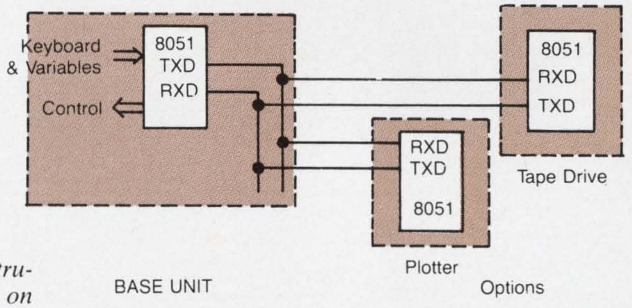


Figure 4: An instrument design based on the 8051.

Distributed Control

Figure 4 shows a sophisticated instrument design based on the 8051. The master resides in the base unit and is the instrument's controller. Additional options that can be bought with the unit, or purchased at a later date and connected to the unit, could include a plotter, a printer, a terminal, or a floppy or tape cartridge. These options can be simply added by just connecting them to the base system. Each different option would have its own unique node address. Upon power-up, the master would poll all possible node addresses to see what options are connected to the instrument and be able to automatically configure the system. □

Courtesy of Harris

Superminis Give Mainframes A Run For Their Money

by Nicolas Mokhoff

The price/performance of mainframe minicomputers has been blurring for several years to the extent that, in some applications a superminicomputer, like Gould's Concept 32/8780, can now effectively compete with high-end mainframes such as IBM's 3081 and 3083, high-end Cybers, and supercomputers like the Cray 1. This bold assertion is specifically made by minicomputer manufacturers who tout their products as super minicomputers.

The term "superminicomputer" is not clearly defined. According to a market study on "Superminicomputers in the 1980's" that was compiled by International Resource Development (IRD) Inc, a Norwalk, CT research firm, every computer industry supplier and research firm has formulated their own definition. IRD came out with a consensus definition: Superminicomputers usually have word-length architectures designed around 32 bits, but can include 24-bit and 48-bit systems, too. Certain high-end 16-bit minicomputers are also in this group. Other features that define super minicomputers include their ability to support at

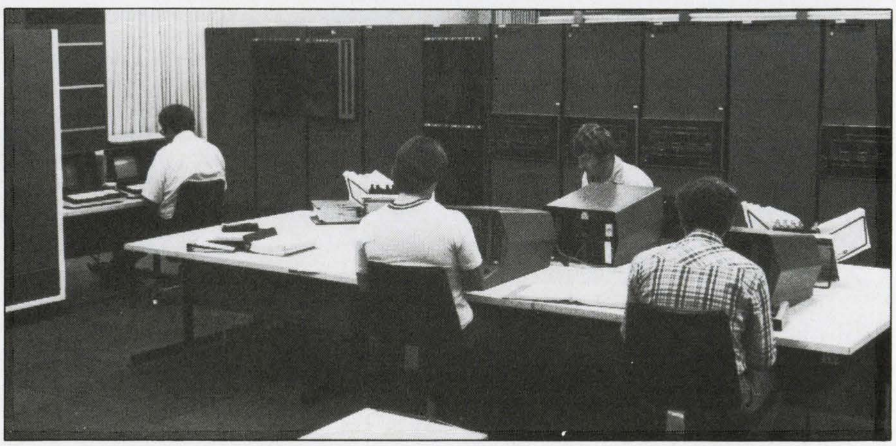


Figure 1: Harris places the performance of the 800 at twice that of a VAX 11/780.

SPECIFICATIONS	IBM 4341-2	P-E 3250	DG MV/8000	DEC VAX-11/780	DEC VAX-11/782	HARRIS H800	PRIME 850	GOULD 32/87	GOULD 32/8780
Approximate Whetstone performance in M.I.P.S.	1.5	1.2	1.3	1.2	2.0	1.5	2.2	3.7	6.6
Optimized Whetstone performance in M.I.P.S.	N/A	3.0	N/A	N/A	N/A	N/A	N/A	9.4	17.4
Average System Approximate Price (2MB, 300MB disc, tape unit, software)	$430,000	$249,150	$273,760	$319,040	$485,340	$294,650	$379,500	$264,900	$395,000
Maximum Main Memory	16MB	16MB	12MB	8MB	8MB	12MB	8MB	16MB	16MB
Storage Interleaving	Standard	Standard, up to 4-way	Standard, up to 4-way	Optional 2-way	Optional 2-way	Up to 4-way	Standard, up to 2-way	Standard, up to 4-way	Standard, up to 4-way
I/O Throughput	14MB/Sec	10MB/Sec/Bus	18.2MB/Sec	13.3MB/Sec	13.3MB/Sec	19MB/Sec	8MB/Sec	26.67MB/Sec	26.67MB/Sec
Maximum Cache Size	16KB	8KB	16KB	8KB	8KB	6KB	32KB	64KB	128KB
Cache Organization	N/A	Write-through 4-way set associative	Write Back, direct mapped	Write-through 2-way set associative	Write through 2-way set associative	2 block partitions	2x16KB 2-way set associative	Write-through 4-or 8-way set associative	Write-through 4-or 8-way set associative
Effective Memory Access time w/cache	120-240ns	250ns	264ns	280ns	280ns	180ns	130ns	94.5-153ns	94.5-153ns

Table 1: Comparing high-performance superminicomputers. (Source: Gould SEL)

least 16 remote terminals and have a minimum memory configuration of at least 1 Mbyte, with most current machines configured for 16 Mbytes.

Gould's Concept 32/8780 certainly fits this definition. Its 32-bit architecture places the machine in direct competition with a number of similar high-end superminicomputers whose manufacturers have addressed the same price/performance features.

George Teixeira, a competitive analyst with Gould's SEL Computer Systems Division in Fort Lauderdale, FL. has compiled a chart of six competitive superminicomputers that are geared for similar applications: seismic prediction, oil exploration, aircraft simulation, image processing, and energy management (**Table 1**). Listed are approximate Whetstone performance numbers and optimized Whetstone numbers, both expressed as MIPS (million instructions per second), a common performance value used in the minicomputer industry. (See accompanying "The Whetstone Benchmark"). Optimized Whetstones are calculated because according to Teixeira, "Perkin-Elmer developed a special program that optimizes its computers to operate faster when a special Whetstone performance program is run on its machines." Thus to compare apples with apples, Teixeira lists two figures for Whetstone calculations.

Included in the chart are the maximum main memory and the cache memory sizes, the I/O throughput, the type of storage interleaving used, the cache organization, and the memory access time with cache. Prices for an average system vary from Perkin-Elmer's 3250 listing for $249,150 to Digital's VAX-11/782 that is priced at $485,340. The prices take into account different system configurations that are reflected by different hardware and software available from each company. While some minicomputer manufacturers may take exception to the choices of computers in this table, the chart reflects the top of the line of supermini computers that are being used in similar applications. Overall, according to the IRD report, there will be about 13 times the number of superminicomputers installed in 1990 than in the beginning of this decade (**Table 3**).

The following illustrates some salient features of the six companies highest performance machines. *Data General's Eclipse MV/8000* is their top of the line 32-bit machine and is the company's only computer that is classified as a supermini. From more than 90,000 minicomputers shipped by Data General since its inception only about 50 MV/8000 have been delivered — a testimony to the exclusivety of the supermini.

The machine is an upward extension of the company's main line offering—the Eclipse series. The

	H800	PE 3250	SEL 32/87	VAX 11/780	PRIME 750
Approximate Whetstones performance in M.I.P.S.	1.0	0.8	2.0	0.8	0.8
Architecture	48 bits	32	32	32	32
Virtual Memory	Yes	No	No	Yes	Yes
Physical Memory	12MB	16MB	16MB	8MB + 4MB (shared)	8MB
Shared Memory	Yes	No	Yes, but not cached	Yes	No
Cache Memory	Yes	Yes	Yes	Yes	Yes
BUS Throughput/sec	19MB	40MB	13.3MB read 26.6MB write	13.3MB	8MB
MAP Features	Yes	No	Yes	Yes	No
No. of Terminals	128	64	64	96	96

Table 2: Harris's systems comparison.

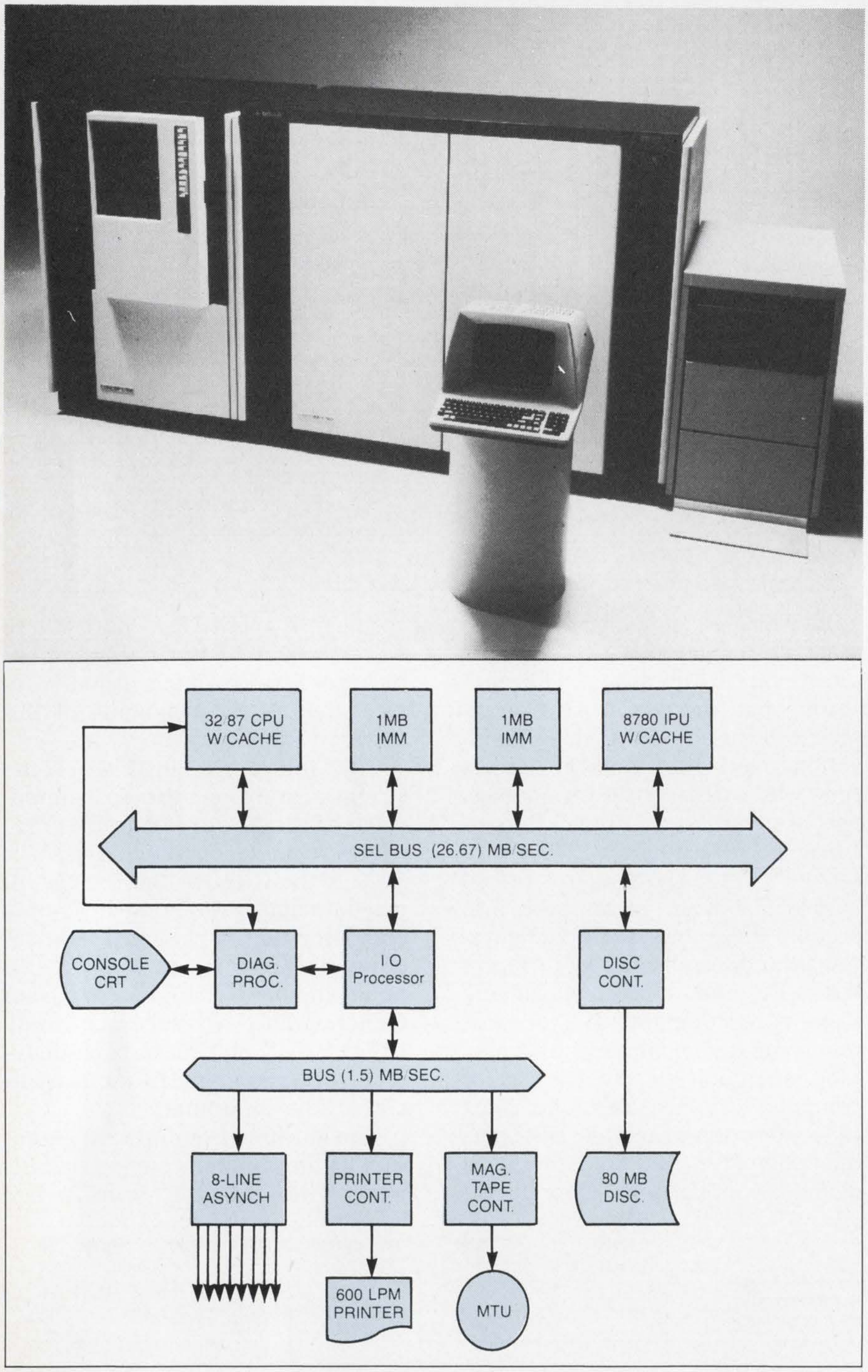


Figure 2: Gould's Concept 32/8780.

MV/8000 uses only five boards to house a virtual address space totalling some 4.3 billion bytes, end-user address spaces of up to 512 Mbytes each, a built-in diagnostic processor, a hardware-supported eight-ring security and file protection mechanism and three 32-bit software languages. The MV/8000 can execute both 16-bit and 32-bit programs simultaneously and program instructions of both lengths can be intermixed in a single program.

Similar to some other superminicomputers, this system encompasses four major subsystems: CPU, memory unit, systems control processor and the Input/Output system. The architecture is one of a multiprocessor made up of 3 processors which allows placement and management of intelligence as close to the actual process as possible. An optional fourth processor, a date control unit, acts as a communications controller, handling up to 8 synchronous lines. Up to four of these data control units can be configured around a single MV/8000.

The MV/8000 has a unique multiprogramming operating system known as AOS/VS and Fortran, PL/1 and BASIC compilers. Any of the AOS compilers used on the other Eclipse systems can also be used with the AOS/VS operating systems.

Digital's VAX 11/780 accounts for the basis of much, if not most, of the company's 1980–1990 product development efforts. More than 2000 VAX 11/780's have been shipped since their introduction in 1977. VAX systems are the predominant computers in the university research environment, especially among physical science departments. In many universities, centralized "computation" centers had been developed to pool computing resources to be used by the various science departments for their computer-based R & D educational programs. Typically, such centers were jointly funded, and were often equipped with large centralized mainframes from CDC, Univac and IBM. As the VAX series became available, the apparent price/performance characteristics—showing significant improvement over the centralized computing approach—enabled individual department heads to justify acquiring their own department—level VAX systems. Thus, where mainframes had previously been installed to serve the university's computation needs, there may now be installed 2 or 3 or 4 VAX systems—or a mix of Digital and other superminicomputer systems.

The company's 11/750 that offers "60% of the performance of the VAX-11/780 at 40% of the cost" uses gate-array technology. This allows the computer to be assembled in a smaller package (because a single gate array chip can provide

The Whetstone Benchmark

To have some degree of comparison between different computer architectures a majority of computer manufacturers (especially in the scientific area) have adopted Whetstone numbers to rate their machines.

The Whetstone values are based on how well the computer performs when using a standard Whetstone benchmark program. There are two versions of the program, one using single-precision numbers and the other double-precision numbers.

The larger the Whetstone value obtained, the greater the performance. Since the early 1960's single benchmarks have served to rate computer performance; however, new techniques must be employed to thoroughly compare today's machines. While the Whetstone is still valuable as a basic measurement, recent technologies such as cache memory, writable control store and software optimizers have added new variables to an already debatable rating method.

Why the Whetstone? During the early 1970's the British government requested the Central Computer Agency to develop a tool for measuring computer performance. Originally, the Whetstone program was intended to compare different language processors on the same computer. But it quickly became apparent that the impact of the source language processor was dwarfed by the impact of the translation technique employed. For example, an interpreter did not stand a chance against a compiler, and optimizing compilers (such as that of IBM's FORTRAN-Level H) clearly outperformed their less intelligent counterparts.

To counter the optimization challenge, a new benchmark was sought that would force any compiler, no matter how smart, to execute every logic path and perform every function. This new benchmark became known as the Whetstone benchmark.

The Whetstone benchmark, as developed, consists of 10 program modules each of which exercises a group of high-level language facilities. Each module is placed in a loop and the number of times it is executed is determined by the statistical frequencies of those elements contained in the module. Features such as simple variable and array addressing, fixed and floating point arithmetic, subroutine calls and parameter passing, and standard mathematical functions are exercised.

The speed of the machine is expressed in KWIPS (thousands of Whetstone instructions per second) and is calculated from a number of runs of the benchmark with varying values of the loop counter.

To date the Whetstone benchmark program has been designed to run under various high-level languages including FORTRAN, ALGOL, and BASIC.

What are some problems with the Whetstone benchmark? First and foremost it must be remembered that the benchmark measures processor speed, not throughput. Thus, all throughput factors such as the efficiency of the operating system, the configuration, and the channel speeds are ignored. On systems with cache memory, the relatively small program can fit snugly inside the cache and thus only measures its ability to number crunch out of the cache.

Writable control store, a feature that allows the user to provide microcoded versions of critical routines and can result in a 60% speed improvement, can boost the Whetstone ratings numbers by as much as 20%. Likewise, floating-point processors can improve Whetstone ratings considerably.

Finally, software optimization techniques have doubled the ratings of some computers, and programmers use of subprograms and structured programming methods have also helped to undermine the original purpose of the Whetstone program.

How do Whetstone numbers differ from MIPS? MIPS (millions of instruction per second) figures are approximate indexes, and manufacturers vary as to the methods used to derive them. IBM and other mainframe vendors frequently take the average of a number of runs with a multiplicity of job types, usually predominantly COBOL batch programs, some of which are compute-bound and some of which are I/O-bound. Supermini vendors, on the other hand, frequently run standard FORTRAN-based Whetstone benchmarks that tend to do especially well on systems with fast floating-point processors and cache memory. In view of these inconsistencies, one cannot compare mainframe MIPS with supermini MIPS since there is no common denominator.

Thus in conclusion, Whetstone numbers should only serve as a rough guideline to narrow system comparisions to a set of most-likely comparable systems. However, no factor affects system throughput more than the customer's intended use and application. Therefore, Whetstone numbers should never be used as absolute definitions of system performance.

— George Teixeira
Gould SEL
Computer Systems Div.
Fort Lauderdale, FL.

the equivalent logic of about 25 standard ICs) as well as cutting power consumption in half. Thirdly, circuit reliability is greatly improved and, fourthly, the cost per equivalent logic using gate arrays is about one-half the cost of using ICs, according to Digital.

Harris's 800 **(Figure 1)** is publicized as the most powerful virtual memory superminicomputer available today. Harris places this system's performance at a level almost twice that achievable by DEC's VAX-11/780. While many features of the 800 system are similar to those found in the smaller 500, this model also provides decimal arithmetic, has an integrated floating point, incorporates a 48-bit word-length architecture, and supports up to 128 concurrent users. The system architecture also features "pipeline" and parallel processing, with three separate processors used in this design. The instruction processor maintains the instruction and operating code and streams these to the execution processor, which decodes the incoming instruction and prepares the initialization and execution of the code. Working together, these two processors enable up to 7 instructions to be in the pipe-line simultaneously, either being fetched, prepared,

	1981	1983	1985	1990	Cumulative (1981–1990)
Units Shipped	2000	4400	7400	23,700	102,200
Value of Shipments.	$300M	$660M	$890M	$1,775M	$10,013M
Unit Value (x)	$150K	$150K	$120K	$ 75K	—
Source: IRD, Norwalk, CT.					

Table 3: Shipments of 32-bit superminicomputers.

decoded, processed or executed. The processor provides 11 decimal digits of precision which is beyond the degree of precision attained by many other superminis. The 800 can be configured around a shared memory unit in configurations of up to six processors.

Recently Harris enhanced their H-800 series with up to 12 Mbytes of real memory and 48 Mbytes of virtual memory. These features are included in two new computers: the H-800-1A and H-800-1B. The new models can execute programs up to 6 Mbytes in size and use Harris's recently introduced VOS operating system.

Like the H-800, the new models support up to 128 concurrent users doing interactive program development, time-sharing, multi-stream batch, multiple remote job entry and real-time processing. Included also is a 6 Kbyte bipolar cache memory, an integral hardware floating point processor and the same 48-bit architecture as in the H-800, which features pipeline and parallel processing that allows up to seven instructions to be processed simultaneously. The system bus is capable of an aggregate transfer rate of 19 Mbytes per second, and up to 31 I/O channels are available including from 16 to 72 priority interrupts. Languages offered with the H800-1A and H800-1B include FORTRAN 77, PASCAL, APL, BASIC, COBAL, RPG, ASSEMBLER, SNOBOL and FORGO. The H800-1A with 768 Kbytes of high density memory, expandable to 12 Mbytes, is priced at $192,400. The H800-1B has 1536 Kbytes of high density memory, also expandable to 12 Mbytes, and is priced at $199,600. This includes a system console terminal with programmed I/O channel and a maintenance aide processor terminal. Harris 800 users can upgrade to the H800-1A and 1B with a field package that costs $18,000.

Every supermini manufacturer compares his machine with other competing computers in a unique way. When Harris compared H800-1 specifications to what they consider four leading contenders (**Table 2**) the results illustrate that there is no standard way to evaluate superminicomputer performance.

The basic 32/8780 computer configuration contains the largest cache of any superminicomputer on the market today.

In 1974, *Perkin-Elmer* and *Gould's SEL* division were the first computer manufacturers to develop, and market a true 32-bit minicomputer.

Perkin-Elmer reviewed the then current technology to determine if a large-word machine (i.e. 32-bit) could be developed and marketed as a cost-effective alternative for those sophisticated minicomputer users who had about exhausted the potential of the 16-bit machines. The answer in 1974 was the Model 7/32, the industry's first 32-bit minicomputer. This event, along with Gould's then Systems' concurrent activities, launched the superminicomputer industry. According to IRD Perkin-Elmer accounts for about 36% of the 32-bit superminicomputers installed worldwide. IRD predicts that shipping rates of Digital and Prime, Data General and perhaps one or two others are soon going to eat into the 36% share currently held by PE. The combined number of installations for the Perkin-Elmer's Series 3200 models is in the 2000-unit range. The company refers to its line of superminicomputers as Megaminis, with the top-of-the-line model being the 3250.

The company's machines, unlike DEC's, use real memory-based architecture. Megamini usage patterns are clustered around real-time-oriented applications (like industrial process control and

System	Gould 32/8705	Gould 32/8780	Prime 850
2MB Main Memory	X	X	X
8-Line Async	X	X	X
CRT Control Console	X	X	X
300MB Disk Subsystem	X	X	X
75IPS, 800/1600BPI Tape Subsystem	X	X	X
Floating Point Accelerator	X	X	X
600 LPM Printer	X	X	X
Operating System	X	X	X
Fortran	X	X	X
Total Price	$264,900	$395,000	$379,500
Performance in Whetstone MIPS	3.7	6.6	2.2
Optimized Whetsone MIPS	9.4	17.4	N/A
Source: Gould SEL			

Table 4: Comparing top-of-the-line superminis from Gould SEL, and Prime.

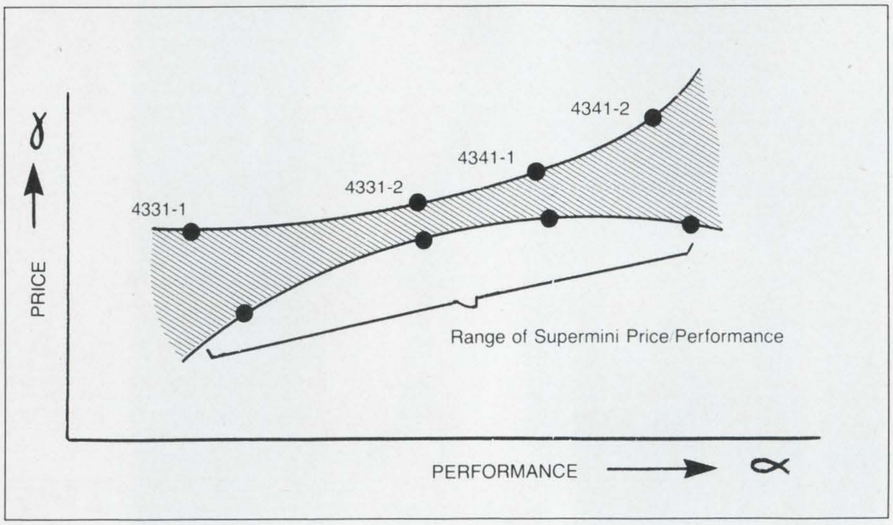


Figure 3: A look at how suppliers perceive the price/performance of superminis (source: IRD).

SCADA); interactive applications (for multi-user time-sharing); transaction processing applications (in which market Megaminis are sometimes found being benchmarked against Tandem's "Non-Stop" machines), and in other applications where real-time computation and response is vital to the effectiveness of the system.

According to Perkin-Elmer one unique feature in the 3200 series is the floating point processor capability, designed in accordance with some internal standards promulgated by the National Bureau of Standards. The reasons for the decision to standardize the floating point format were two-fold: to meet the demands of the Government agency user community (an important PE volume customer); and to make it easier for users to swap programs among 32-bit computer systems. With the increased application of 32-bit superminicomputers to mathematical modeling, methods of notation for various mathematical precision levels is going to become more important.

Prime's 850 unit incorporates multistream instruction processing architecture and uses 1-Mbyte memory boards consisting of 64k RAM chips. The 850 is being configured with from 2 to 8 Mbytes of main memory, enabling a 512 Mbyte virtual addressing space per user. The processor can support up to 128 terminals.

When comparing this machine to Gould's 32/8705 or /8780 the Prime 850 does not fare as well in performance while being relatively higher priced (**Table 4**), according to Gould's Teixeira.

At its recent announcement of the 32/8780 Gould SEL's Cal Shoemaker, VP marketing and sales said: "The 32/8780 is the fastest machine around, and is priced very aggressively—we fully expect to dominate the high end of the 32-bit minicomputer market with this product."

Every supermini manufacturer compares his machine with other competing computers in a unique way.

The 32/8780 makes use of architectural concepts in the earlier 32/8780 and 32/87 but is more than five times faster than its closest price competitor. Its optimized Whetstone performance was measured at 17,477 MIPS. The system achieves its extraordinary processing power from a unique combination of parallel processors with high-speed, ECL technology, and very large cache memories.

The parallel processors, designated as the Central Processing Unit (CPU) and the Internal Processing Unit (IPU), work together to share the load in a multi-stream environment. Under control of a single operating system (MPX-32), the CPU handles all I/O and interrupt processing, while the IPU handles compute-bound tasks. Both processors have their own floating point hardware. The basic 32/8780 computer configuration consists of 32 Kbytes of 75-nanosecond cache memory in both the CPU and the IPU, which is the largest cache of any superminicomputer on the market today. This can be upgraded to provide a total of 128 Kbytes of cache memory.

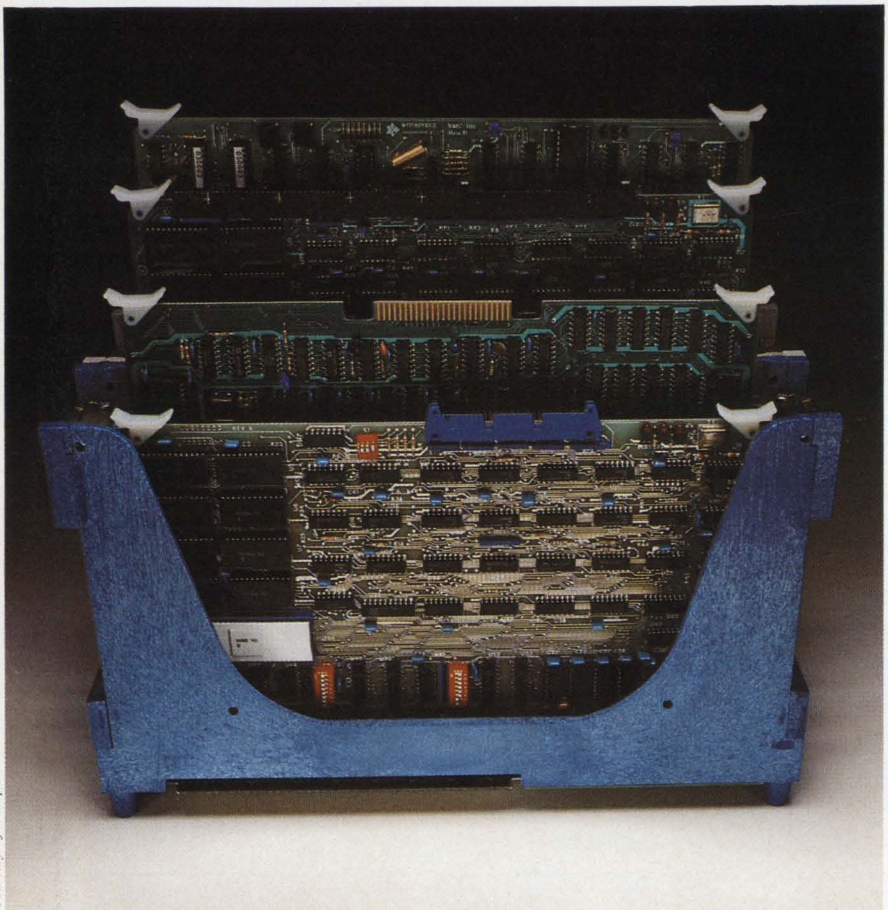
The Whetstone I benchmark industry standard was given to evaluate the 32/8780. The standard unoptimized code produced by the Gould SEL Fortran 77+ compiler resulted in a processing rate of 6.659 million Whetstone instructions per second (M Whets/sec), which is approximately twice the processing power of its closest competitor.

The basic configuration of the new Gould Concept 32/8780 (**Figure 2**) includes a 32-bit ECL-based CPU and IPU each having its own 32 Kbyte cache memory, 2 Mbyte main memory, built-in floating-point processors, a diagnostic processor, I/O processor, line printer/floppy disk controller, dual floppy disk, CRT control console, and all required chassis, power supplies and cabinet. The price for the basic 32/8780 computer is $395,000.

The benchmark supermini that most minicomputer companies compare their machines to is the IBM 4300 series. A look at how, in general according to IRD, suppliers perceive the price/performance of the superminis vis-a-vis the 4300 series machines can be seen in **Figure 3**.

While this report is far from an exhaustive survey of the minicomputer industry it attempts to highlight the top-of-the-line supermini machines that are invading the mainframe computer turf. ☐

Designers' Guide To The Multibus



Courtesy of Interphase

by Paul Snigier, Contributing Ed.

Today's economic climate may dictate the choice of bus to the OEM designer. Many useful applications requiring dedicated controllers are suited to the STD bus and its compatible products, since they are positioned below the Multibus in price. However, those applications that require an upward growth path may do better with the Multibus than with the STD bus. Many low-end industrial applications will still use the more costly Multibus, with the designers leaving much of the board capabilities unused.

Low-end applications require the flexibility and bit capabilities of the Multibus, in areas such as multiprocessing. The Multibus is known to support multiple single board computers, letting one of these SBCs handle bus control and arbitration, which certainly is not possible with the STD bus.

Recession Boosts Bus

In these recessionary times, with products tied up in inventory considered to be a liability to a firm's cash flow, the Multibus has an advantage: a smaller card inventory is possible, tying up less capital. The argument that certain features will go unused — an argument aimed at the Multibus by the S-100 and STD compatible makers — though accurate, does not tell the entire story. A perfect fit may even be detrimental in today's bad times, with many OEM vendors either laying off some of their design workforces, cutting back on inventory even more, and cutting capital expenditures for design tools and development aids. Although many functions and board sections may go unused, the boards are more universal, and make designing in easier.

By providing system flexibility, the Multibus is assured of success in an unstable market environment.

STD makers seem somewhat chagrined by the turn of events. Some predict that when the upturn occurs, the Multibus flexibility and overkill will once again become a greater liability.

Despite the criticisms, leveled by the STD bus makers against the Multibus and its compatible boards and cards, the trend in the Multibus cards is toward enhancement of exisiting features, as well as new ones. This trend can be seen in the MLZ-91A micro from Heurikon, a Z80A-based single board computer that has a broad list of significant features that include 64KB of RAM on-card, a direct memory access controller, and double-density floppy disk drive controller. It also has interfaces for hard disk drive, streamer tape backup, GPIB, RS-232C/422/423, as well as memory and I/O mapping and a lot more on-card functions. Then there's the iSBC 88/40 measurement and control micro (that is 8088-based) with its 5-MHz CPU rate. The 88/40 has 32 single-ended analog input channels, 16 differential channels particularly suited to ultra-noisy analog lines, as well as an on-card DAC and optional analog output. Three connectors permit analog, digital and even other I/O expan-

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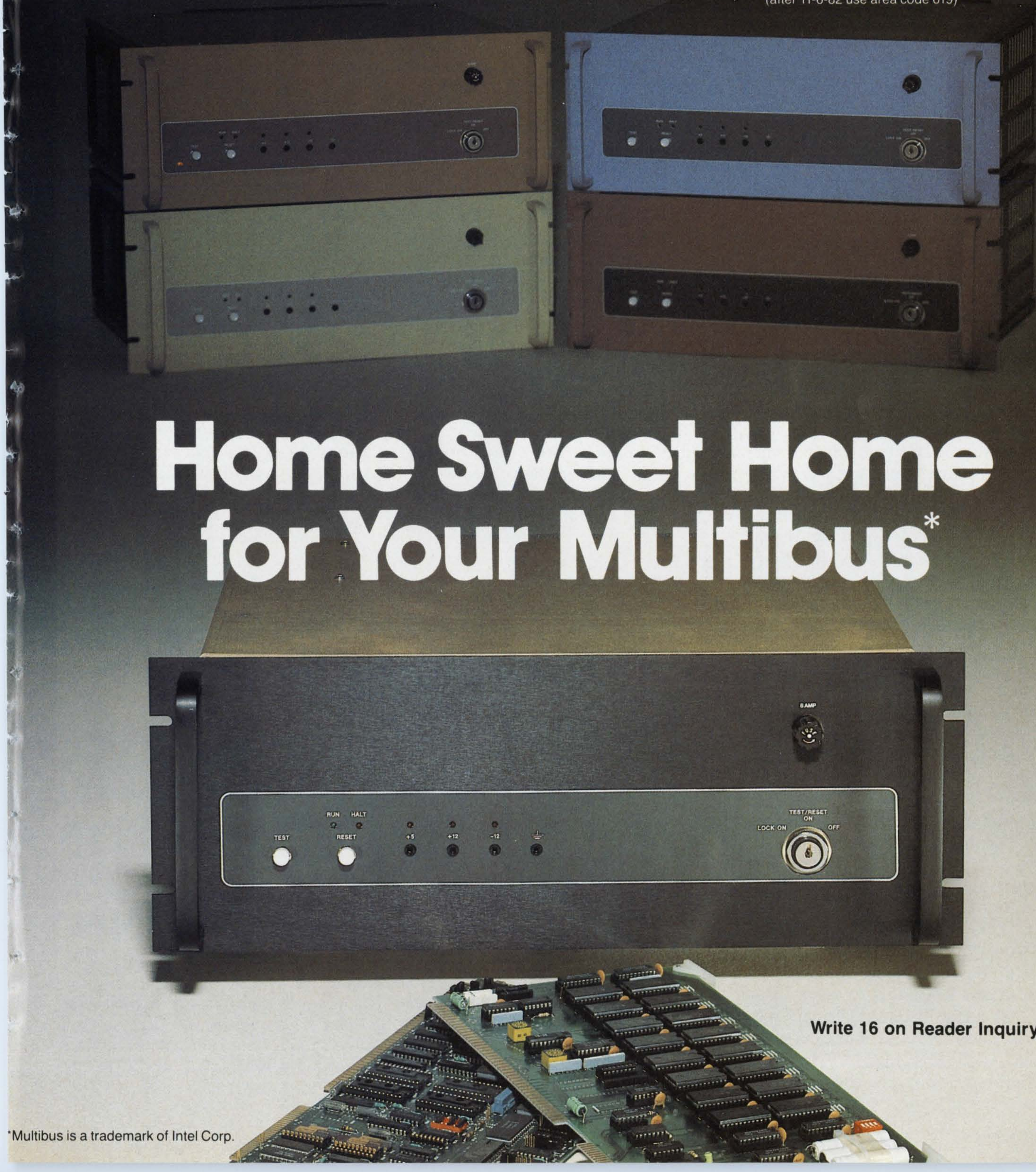
Home Sweet Home for Your Multibus*



Write 16 on Reader Inquiry Card

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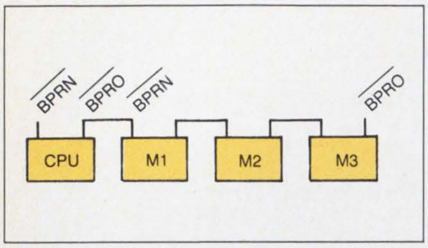

Figure 1: Priority in and out lines are used for determining priority resolution and are connected in this daisychained fashion. M1, master 1, is the highest priority module; M3, the lowest. Both signals are tristate with a 5 mA minimum driver current and −2 and −1.6 mA maximum receiver current, respectively (in L to R sequence above)

sion. The board concurrently processes and updates 16 control loops in under 200 ms.

Expansion modules for Multibus board-level computers are extensive. Just a few functions include: speech synthesis, disk controllers, analog inputs and outputs, analog I/O expansion, floating point math processors, Centronics parallel printer interface, parallel I/O expansion, prototyping expansion modules, GPIB controllers, cassette and cartridge interface, VDT interface (both alphanumeric and graphics), DMA channel interface, static and dynamic memory expansion, real time clock, and ancilliary Multibus compatible products, such as backplanes, card cages, and extender cards. Multibus has over 50 compatible sources of system modules. It was first on the market with a workable and fully documented interconnect system, and it supports both 8- and 16-bit μPs, and did so from the start, not through modifications as with other buses.

Familiarity may breed contempt, but for the Multibus this hasn't been true, since OEM system designers prefer to remain with proven systems, cards, products and the like. This is particularly true in recessionary times, so experimentation or buying of new bus cards or products is less likely to occur. Under economic pressures to survive, OEM designers and marketers are unlikely in this time to go with something unproven; they become very "design conservative."

Technical Details

Let us look at some of the technical aspects of the Multibus. This bus quickly interconnects SBCs, digital I/O boards, memory boards, and peripheral controllers and other devices. It was originally developed, designed and specified by Intel, and subsequently became an industry-wide de facto and new IEEE standard. In the construction of a system, the designer selects the proper mix of components to satisfy application requirements. Power supplies, card cages, extender cards and the like are offered by Intel and many other firms.

Multibus has five signal categories — a 22-line address bus, 16-line bidirectional data bus, 8-multilevel interrupt lines, power distribution lines and control and timing lines. The address and data bus are tristate, but interrupt lines are open collector. The signal category breakdowns, represented in a functional breakdown in **Table 1**, illustrate the very direct nature of the Multibus pin assignments for these categories.

Bus modules are either masters or slaves, and operate as either. A master module transmits commands and designates addresses on the bus. It controls the bus. This is distinct from the slave, which cannot control the bus. To avoid conflict, built in arbitration handles requests from multiple masters on a priority basis. Data transfer speed is not bus clock synchronous, so higher rates are possible. The controlling factors, however, are the master and slave data rates. A slow master can just as easily gain bus access as a faster one. Once it does gain bus control, either multiple- or single-word transfers are permitted. As listed in **Table 1**, Multibus signals are assigned to pins in the P1 primary connector or P2 secondary connector. The P1 signals include data, address control, interrupt and power lines. P2 signals in the auxilliary connectors are optional and used for battery backup, mostly for memory data protection. Most bus signals use negative logic (TRUE when LOW), thus decreasing the chance of an incorrect instruction, as bipolar devices produce HIGH outputs when undriven. As a consequence, when one bus master takes control from another, invalid TRUE outputs are not issued.

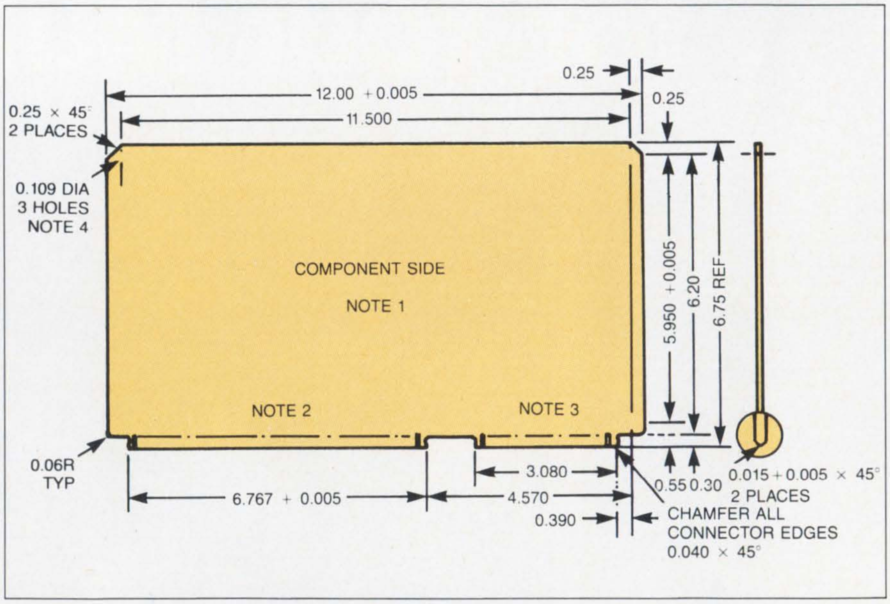

Figure 2: Multibus mechanical board dimensions, 12" by 6.45" by 0.062", are larger than the S-100—10" by 5.125". The edge connector (bottom) side is asymmetrical, with the 2 × 43 edge connector (0.156" spacing) at left and the auxilliary 2 × 30 connector (0.1" spacing) at right. These connectors are available from many firms, such as TI, Amp, and Viking. Other mechanical specs include: 0.6" board spacing, 0.435" component height, 0.050" clearance on conductor near edges. Ejectors are not shown, but may be Seanbe-type S203s.

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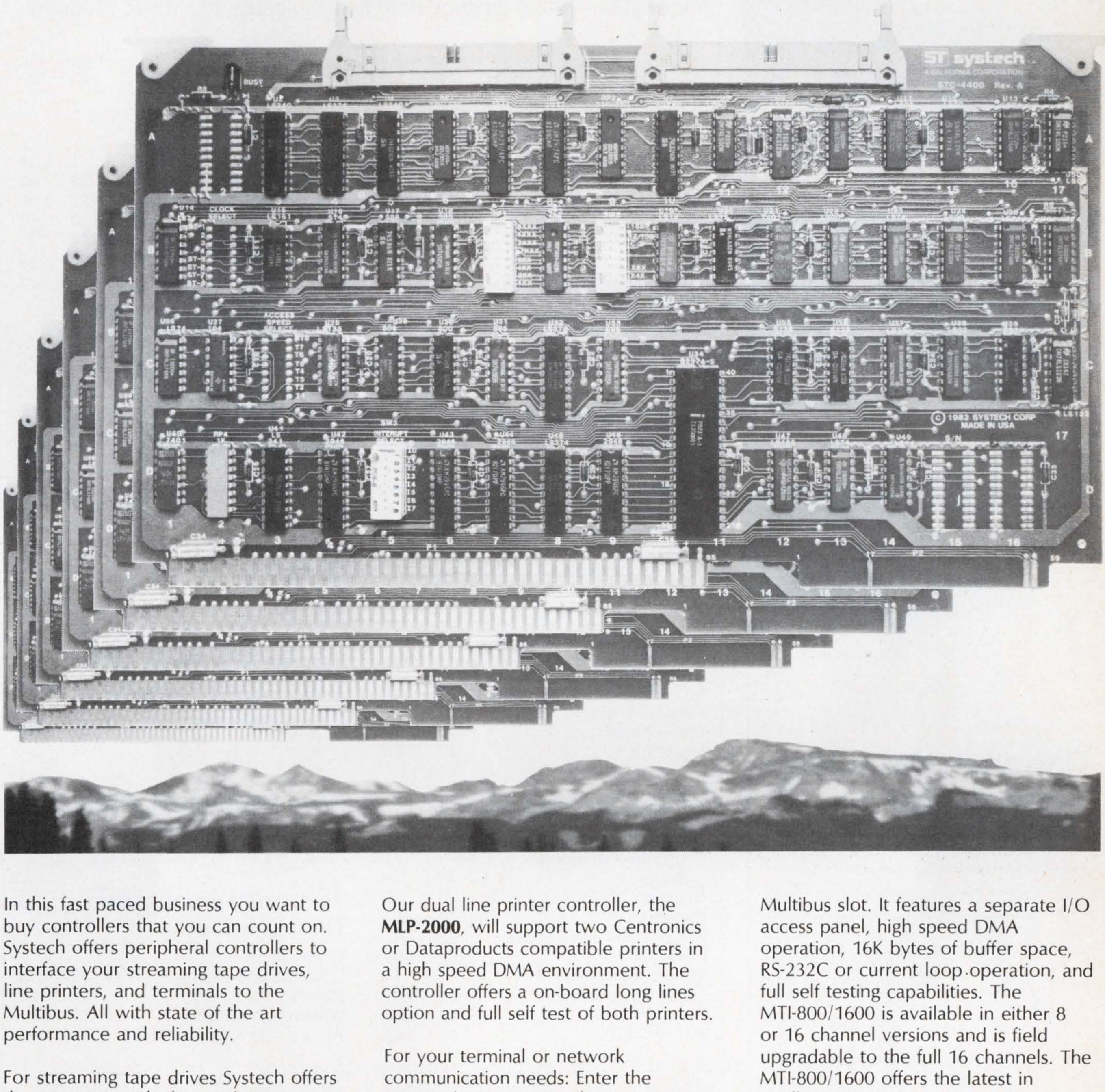

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Multibus Board for Numerical Control

The industrial marketplace is now under heavy fire from both the semiconductor and computer industries. Virtually every day, a new device, board level product or system is announced specifically targeted towards the automated factory, robotics or process control areas. As more emphasis is placed on these applications, the designer will see a plethora of Multibus boards specifically dedicated to interfacing existing computer systems with the outside world.

One company that is already making inroads is Toko America, Skokie, IL. Its product, the NCB 102, is a numerical control board based around a Z80A, and KM3701/3702, two chips designed at Toko Semiconductor in Japan. Tukihiro Asami, Senior Design Engineer, Toko Japan, and Douglas Yumoto, Products Engineer in Skokie, shared with us some design philosophy behind the board, together with some applications.

Looking at the design example in **Figure 1** is perhaps the best way to gain insight into the function of the board. The NCB 102 receives data from a host computer via the Multibus and produces drive signals for servo and stepping motors. A closer look shows an on-board Z80 that processes ASCII code from the host computer and converts it to a 24-bit number that the KM3701 uses to produce an interpolation pulse form.

For precise motor control, the KM3702 compares the interpolation pulse with the feedback pulse from a shaft encoder on the motor.

Although the KM3701 communicates with the Z80 through an 8-bit data bus, the internal operation is done in a 24-bit parallel mode, because 8- or 16-bit arithmetic operations were not enough to provide precise tooling.

One interface to the NCB102 is for the Multibus; another allows communication with an additional module. The combination of the control module and the additional module allows four axis positioning, three axis linear interpolation, two axis circular interpolation and helical interpolation to be performed.

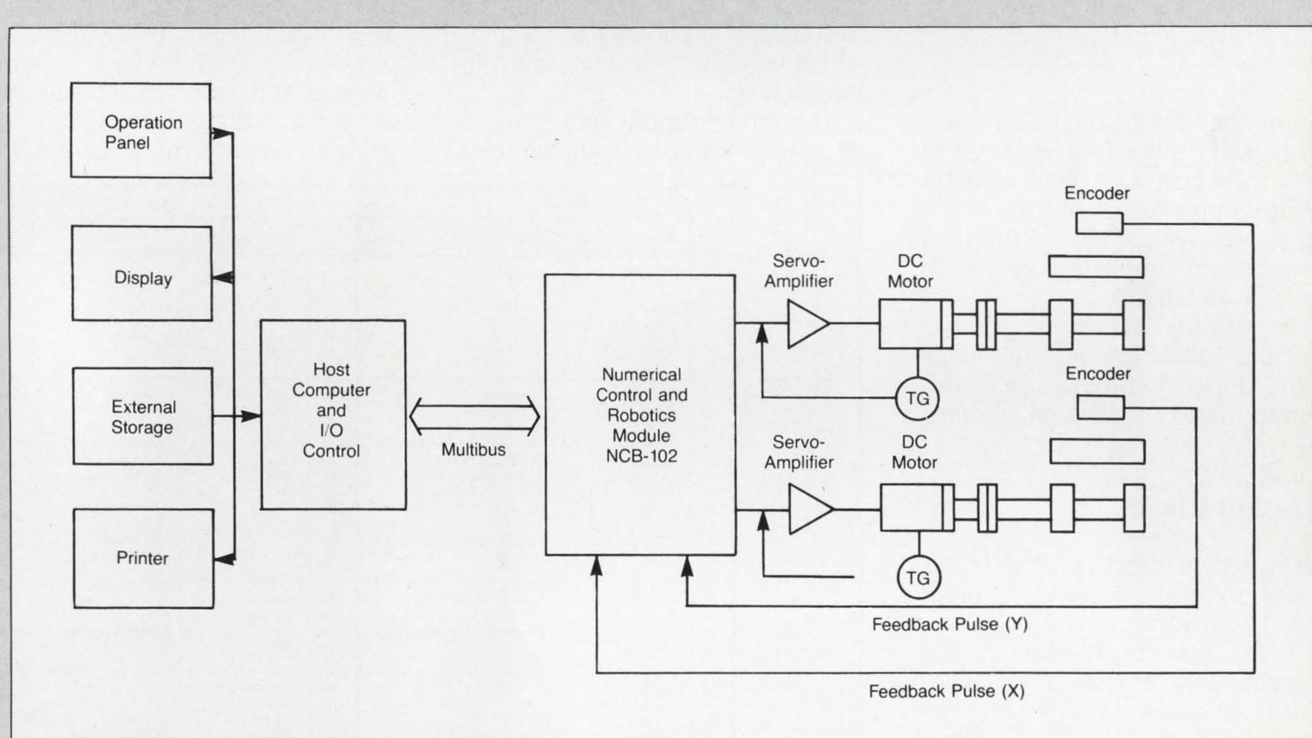

Figure 1: The NCB 102 numercial control and robotics module shown in a typical application.

As for primary signal lines, the initialization signal is the reset instruction. Obviously, it is used primarily in startups, but can be used otherwise. Just as in most other single board computers and systems, pushing a button initiates initialization,but is also hardwired in. A manual reset, obviously, is only one use.

The address bus has 20 lines. If using an 8-bit μP,the OEM would use 16; since the Multibus also handles 16-bit μPs, in this case all 20 address lines are used for referencing memory. Also, 12 lines are used for I/O port designation. Inhibit lines permit both RAM and ROM to be assigned identical memory addresses. The inhibit RAM signal inhibits response and vice versa. These two signals permit the sharing of memory, to also allow for an auxilliary ROM at the same addresses as the primary ROM, or to permit memory mapped I/O ports to override ROM.

Data travelling between the CPU and memory or I/O port trav-

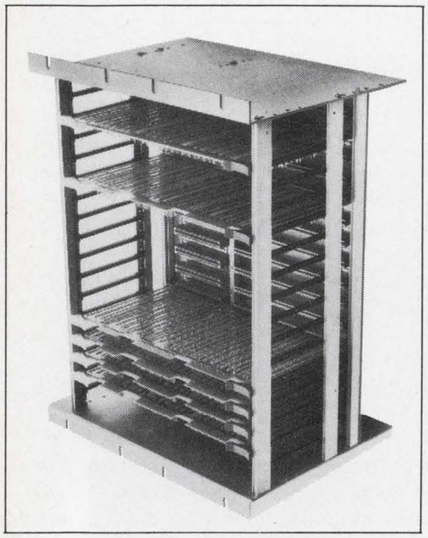

Figure 3: Designed for high speeds and low crosstalk, Multibus backplane card frame boards, such as this Hybricon 8010, are widely available. Wire wrap boards permit high density, using TTL, ECL, analog.

el over the bidirectional data lines, or permit memory-mapped I/O ports to override ROM. The 8-bit μPs use only the eight LSBs. When the upper eight MSBs of the data bus are used, the byte high enable signal is TRUE.

For priority resolution, 7 bus lines are used. The negative edge of the clock synchronizes bus arbitration, priority resolution circuits.

Constant Clock

The constant clock period is for general-purpose devices or modules. The priority in and out lines, used for priority resolution, are daisychained. In this daisychain, priority of a given master is given by physical card location. When the given master obtains bus control, it uses a "busy" signal to indicate the bus is in use. However, if the bus is not busy, a module requesting control uses the "bus request" signal to indicate this. On the other hand, if a master has control, and another attempts to gain control, it can indicate this through the "common request" signal to the controlling bus. The bus control group does, among other things, coordinate information transfer. Two sets of R/W signals exist — one for memory operations and the other for I/O devices. The memory "memory read" and "memory write" signals are used in conjunction with strobing memory. The "memory read" places the address of the memory location to be read on the address bus. The "memory write" signal places the memory location to be written to on the address bus. The I/O "read command" places the address of an input port to be read on the address bus, while the "I/O write" command places the address of an output port being written on the address bus. When completing the read or write operation, it sends a transfer acknowledgement. The slave makes interrupt requests by using the multilevel lines; these are granted by the CPU sending the "interrupt acknowledge" signal, which requests transfer of interrupt information.

The power supply lines, pins 75-86, carry voltage to all modules. Each board must provide bulk decoupling capacitors on-board to prevent power bus current surges. It is recommended that high-frequency decoupling also be used. Typically, values used are 22 μF for +5V and +12V pins, and 10 μF for −5V and −12V pins. The other pin designations for the power supply group are straightforward, as determined from **Table 1**.

As for optional signal lines,the P2 signals are not bussed to the backplane. Thus, a separate connector is required for each board using these signals. Let us look at some of these lines. The AC low power fail interrupt signifies that the AC input voltage is too low, warning of a power supply failure. Normally, this signal becomes TRUE 3 ms before the DC power will fall below acceptable levels. This signal is disabled when the power rises again to 95% or more of rated voltage. An external power source, such as battery back-up, provides voltage to interrupt the

	(Component Side)			(Circuit Side)		
	Pin	Mnemonic	Description	Pin	Mnemonic	Descripton
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5	+5 VDC	4	+5	+5 VDC
	5	+5	+5 VDC	6	+5	+5 VDC
	7	+12	+12 VDC	8	+12	+12 VDC
	9	−5	−5 VDC	10	−5	−5 VDC
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK/	Bus Clock	14	INIT	Initialize
	15	BPRN/	Bus Priority In	16	BPRO/	Bus Priority Out
	17	BUSY/	Bus Busy	18	BREQ/	Bus Request
	19	MRDC/	Memory Read Command	20	MWTC/	Memory Write Command
	21	IORC/	I/O Read Command	22	IOWC/	I/O Write Command
	23	XACK/	XFER Acknowledge	24	INH1/	Inhibit 1 Disable RAM
	25	AACK/	Advance Acknowledge	26	INH2/	Inhibit 2 Disable ROM
	27		Reserved	28		Reserved
	29		Reserved	30		Reserved
	31	CCLK/	Constant Clk	32		Reserved
	33		Reserved	34		Reserved
Interrupts	35	INT6/		36	INT7/	
	37	INT4/		38	INT5/	
	39	INT2/	Parallel Interrupt Requests	40	INT3/	Parallel Interrupt Requests
	41	INT0/		42	INT1/	
Address	43	ADRE/		44	ADRF/	
	45	ADRC/		46	ADRD/	
	47	ADRA/		48	ADRB/	
	49	ADR8/	Address Bus	50	ADR9/	Address Bus
	51	ADR6/		52	ADR7/	
	53	ADR4/		54	ADR5/	
	55	ADR2/		56	ADR3/	
	57	ADR0/		58	ADR1/	
Data	59	DATE/		60	DATF/	
	61	DATC/		62	DATD/	
	63	DATA/		64	DATB/	
	65	DAT8/		66	DAT9/	
	67	DAT6/	Data Bus	68	DAT7/	Data Bus
	69	DAT4/		70	DAT5/	
	71	DAT2/		72	DAT3/	
	73	DAT0/		74	DAT1/	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77	−10	−10 VDC	78	−10	−10 VDC
	79	−12	−12 VDC	80	−12	−12 VDC
	81	+5	+5 VDC	82	+5	+5 VDC
	83	+5	+5 VDC	84	+5	+5 VDC
	85	GND	Signal GND	86	GND	Signal GND

Table 1: Multibus groupings and pin assignments.

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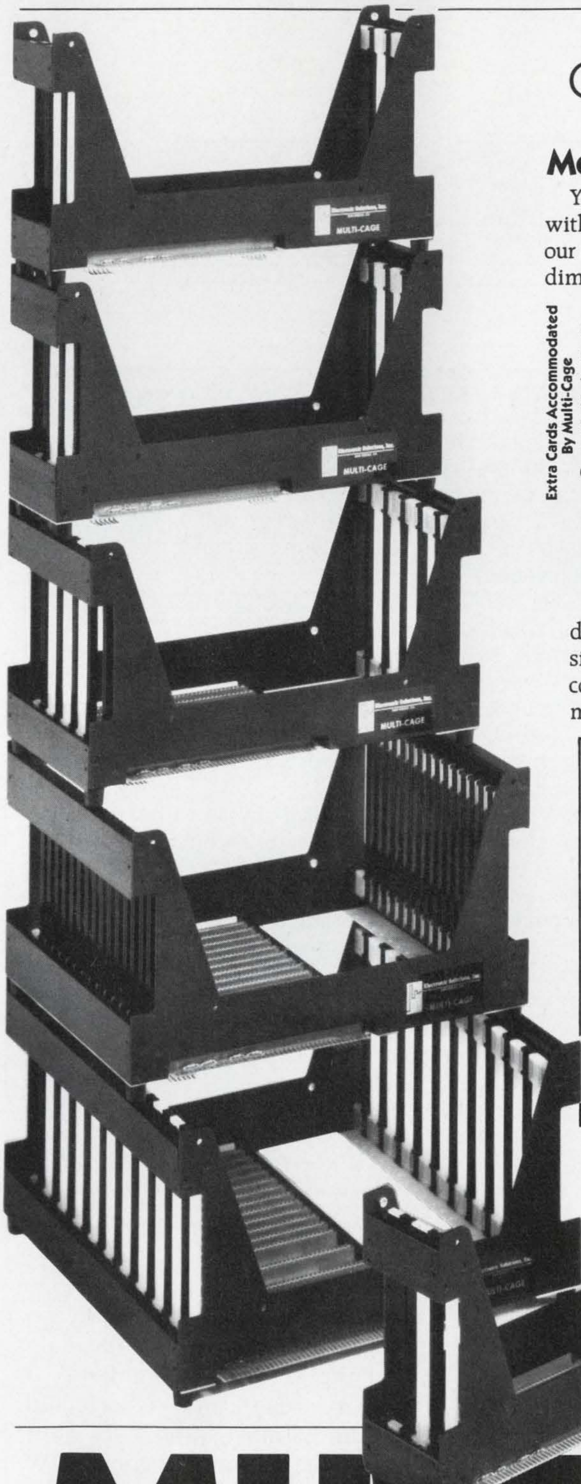

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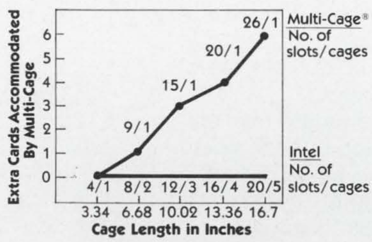

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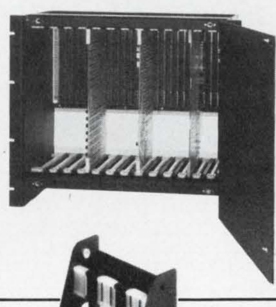

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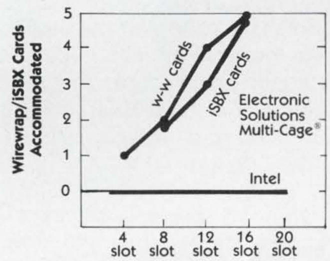

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Write 28 on Reader Inquiry Card

Graphics Board Gets Intelligent

Of the many Multibus compatible graphics boards on show at this year's Siggraph, the one that drew the greatest amount of interest was the system from Matrox Electronic Systems in Canada.

The system consists of two boards; VGM-1000 (Virtual Graphics Machine) and RMB-1000 (Refresh Memory Board). The VGM-1000 generates all of the video timing signals and provides local intelligence with an on-board graphics interpreter executed by an 8088 CPU. The RMB-1000 contains 512 Kbytes of high speed RAM for four bit plane storage. The memory is organized as 1024 × 1024 × 4 pixels. The system has also been designed to accommodate 256K RAMs. When these parts become available a single RMB-1000 memory board can hold 2 Mbytes of RAM organized as 2048 × 2048 × 4 pixels.

The VGM-1000 and the RMB-1000 boards are connected via three 50 pin ribbon cables at the top of each board (Metabus). Both boards require only +5V power from the Multibus. The VGM-1000 board appears to the system bus as an 8088 master CPU with full bus arbitration logic.

The user can configure the RMB-1000 memory board for a variety of different display formats and memory configurations through a combination of software programming, jumper changes, and crystal clock changes.

A minimal configuration consists of two boards; one VGM-1000 and one RMB-1000. This system can be structured for any display format within 1 Mega pixels, with each pixel being 4 bits deep. Examples are 1024 × 1024, 1024 × 768, 640 × 480, 800 × 600 landscape and portrait displays.

For displays requiring more bits per pixel (up to 16 bits per pixel) or more resolution (up to 2K × 2K) additional RMB-1000 memory boards can be used. A maximum of four RMB-1000s can be "stacked" together with one VGM-1000. For example, a display of 1600 × 1200 × 4 requires two RMB memory boards configured for serial operation. A display of 1024 × 768 × 16 requires four RMBs configured to operate in parallel.

Virtual Graphics Machine

The GXB-1000 design incorporates the concept of pipelined distributed processors. The four GXB-1000 processors represent the lowest level of the pipeline (as far as the actual picture generation is concerned). The higher level CPU (on-bus or off-bus via a data link) loads a display file containing the picture description (data and instructions) into off-board RAM memory on the Multibus (there can be multiple display files in the off-board RAM). The display file can be up to 16 million bytes long. Multiple display files can also exist anywhere in the 24-bit Multibus address space.

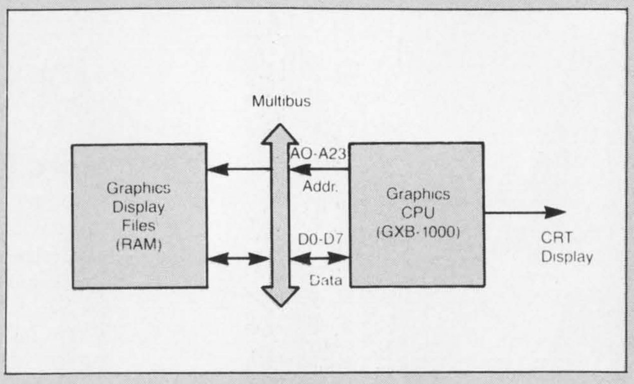

Figure 1: Display file/Graphics CPU architecture.

The user can think of the GXB-1000 board set as a graphics processor which executes its own instruction set. The internal CPU together with local resources (ROM, RAM, graphics processor, VIP, PIP, refresh memory, etc.) can be thought of as a single graphics CPU with microcode stored in on-board ROM. A particular graphics instruction is performed by executing microcode (actually 8088 machine language).

The starting address of the display file to be executed (VGM program) is loaded by an external host via the VGM I/O port, in 3 byte transfers (the I/O port address is user selectable). The host then issues a RUN DISPLAY FILE command after which the VGM fetches the first byte of instruction from the starting address.

The local CPU executes instructions using on-board resources; vector generator, VIP, and PIP. The instruction execution time varies from slow (milliseconds) for long vectors, clear screen, area fills, etc. to very fast (nanoseconds) for control instructions. During execution the Multibus is not used, thereby freeing it for higher level CPU communications. After execution of the complete display file, the local CPU (8088) sends an interrupt signal to the host, notifying it that the display file has been finished.

CPU with a "power fail interrupt" signal to indicate power failure. The "power fail interrupt" interrupts the CPU, with the "power fail sense" indicating that power has failed. The "power fail sense" remains TRUE until reset by "power fail reset."

If "memory protect" is LOW, memory contents cannot be altered. This prevents memory operation when power is uncertain. An auxilliary power latch, "address latch enable", is available for 8085 or 8086 micros. From either of these micros, it is used as an auxilliary latch. This signal produces a LOW on the halt line when the CPU halts. A "wait state" signal indicates the master processor is in the wait state. In "auxilliary reset" a reset signal initiates the power-up sequence. As for data transfer, reading and writing is limited to a maximum rate, but is typically lower to allow for bus arbitration and memory access time. Depending upon whether a memory device or input device is supplying the data, either the "I/O read command" or "memory read" line is selected. The address must stablize for 50 ns before either command goes LOW. The slave then replies by placing data on the bus and pulls the acknowledged signal LOW.

The rate timing resembles read timing in a number of ways. Data is applied to the bus simultaneously

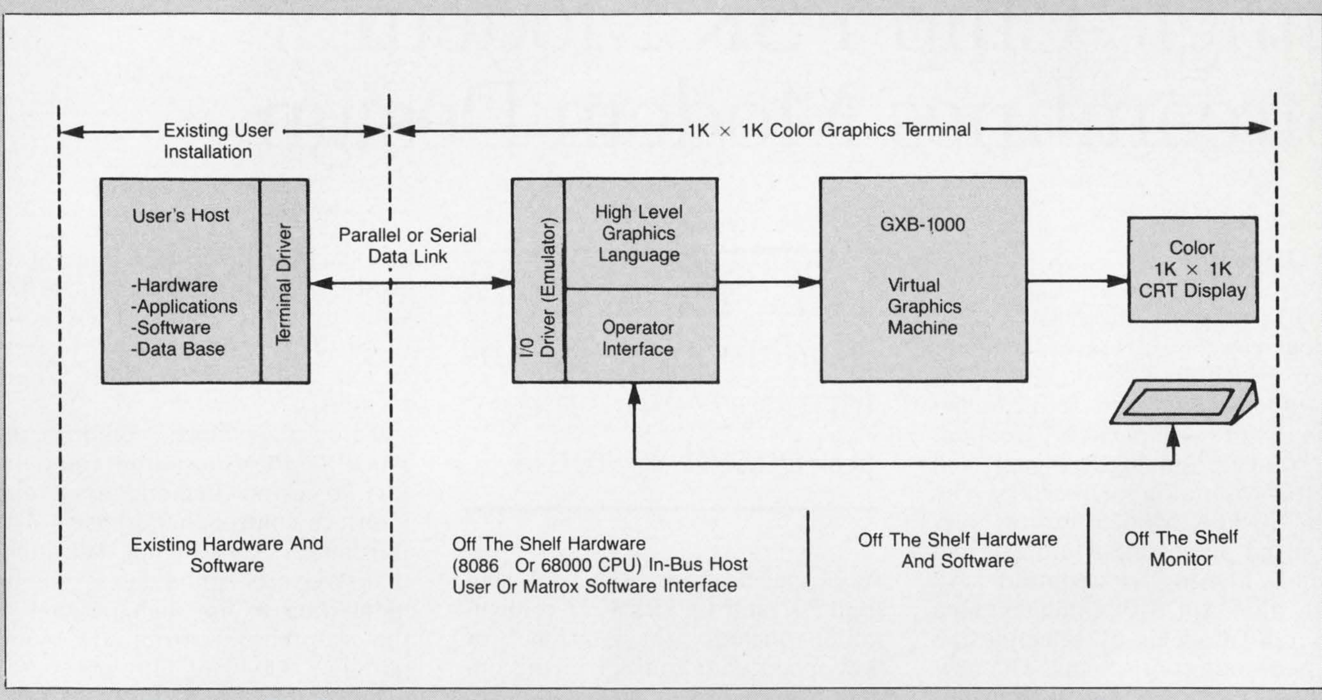

Figure 2: 1K × 1K color graphics terminal implementation.

Alternately, multiple display files can be linked so that at the completion of one file the on-board 8088 will jump to the beginning of the next file. Nesting of display files is also supported.

The same byte (fetched from off-board RAM) can be interpreted by the 8088 as either 8088 instruction opcode or as graphics instruction opcode. The mode is determined by executing the instructions "Switch to Graphics Mode" or "Switch to 8088 Mode." This feature enables the programmer to combine the full 8088 instruction set (at full speed) with Matrox graphics instructions, in the same or different files.

By writing the terminal's high level graphics software in a high level language (C, Fortan, Pascal), executed by the in-bus user CPU, any graphics terminal can be designed (Matrox offers both 8086/87 or 68000 based Multibus CPU cards as in-bus host processors). The Matrox graphics commands are treated as user macrocommands and are defined as such to the user's high level language assembler. The programmer does not have to be concerned with the display hardware, and can therefore write high level terminal programs on the CPU of his choice to generate display files. These display files are in turn executed by the Virtual Graphics Machine in a pipelined fashion, providing the high throughput required for interactive graphics.

This approach significantly simplifies the design of a graphics terminal and enables the user to construct a custom terminal or emulate and upgrade any existing terminal in the shortest possible time. All of the existing user application software and hardware can be used without any change.

As an example of this philosophy, Matrox has developed a Tektronix 4113 emulator software package in "C" which runs on the Matrox MBC-86/12 (8086/87) Multibus CPU board. The package uses a real-time kernel, written in "C," which supports multitasking.

The software is available in "C" source code for the user wanting to add special functions.

Jerry Sullivan, Marketing Manager, told **Digital Design** to expect a terminal based around the board set around the end of the year.

with the address. After the data is sampled, the slave signals over the bus with "transfer acknowledge."

INT0-INT7 (inv), pins 35-42, are the parallel interrupt requests. The interrupt lines permit a slave to interrupt a processor. Two interrupting schemes exist. Bus vectored interrupts transfer the vector address over the Multibus address lines to the slave with the master using the "interrupt acknowledge" instruction for synchronization. The alternate vectored interrupt requires the interrupt controller with the master module to generate the vector address transfer to the processor over the local bus, so that no address appears on the Multibus itself.

As for electrical specifications, all drives on the bus must be in the levels of 2.0 to 5.25V for a HIGH, with 0.0V to 0.45V for a LOW. Receivers accept a 2.0V to 5.5V range as HIGH and −0.5V to 0.8V for LOW. Most bused signals are tristate. Power supply voltage tolerance is ±1%, with ripple at or beneath 25mV(p-p). For obvious reasons, drivers and receivers are proximally close to their pin connections. As for mechanical aspects, the motherboard supports the 86-pin receptacles that mate with the plug on each board. The motherboard contains 86 pin connectors to mate with each individual board. □

Single-Chip FSK Modem Streamlines Modem Design

By D.M. Taylor

A new chip utilizing NMOS technology has transformed modems from black boxes or, at best, board-level products to a single-chip, 28-pin DIP package. Containing on-chip analog-to-digital and digital-to-analog converters, the Am7910 FSK Modem utilizes digital signal processing so no external analog filtering is required. All told, the Am7910 emulates nine different modems by selecting the proper mode control pins. The new modem from AMD meets Bell 103, Bell 202, CCITT V.21, and CCITT V.23 specifications. The 1200-baud Bell 202 and CCITT V.23 configurations include a back channel for low-speed data transfer in the opposite direction of the main channel. The automatic answer process is assisted by outputting the period of silence and then the answer tone. Full analog and digital loopback modes are available for testing purposes by enabling MC4, the loopback mode control pin. Standard modem handshake signals like data terminal ready ($\overline{DTR}$), request to send ($\overline{RTS}$), clear to send ($\overline{CTS}$), and carrier detect ($\overline{CD}$) are included.

David M. Taylor is with Advanced Micro Devices, 901 Thompson Place, Sunnyvale, CA 94086.

This single-chip modem may be interfaced to many µP-based systems.

Three main blocks comprise the Am7910: the transmitter (modulator), receiver (demodulator), and interface control (handshake). The transmitter has a digital data input that converts (modulates) digital input data to an analog signal at the transmitted carrier (TC) output. For 300-baud full-duplex and main-channel 1200-baud half-duplex operation the digital data is presented to the main transmitted data (TD) pin. For back-channel half-duplex operation, the back transmitted data (BTD) pin is used as the digital data input. Similarly,

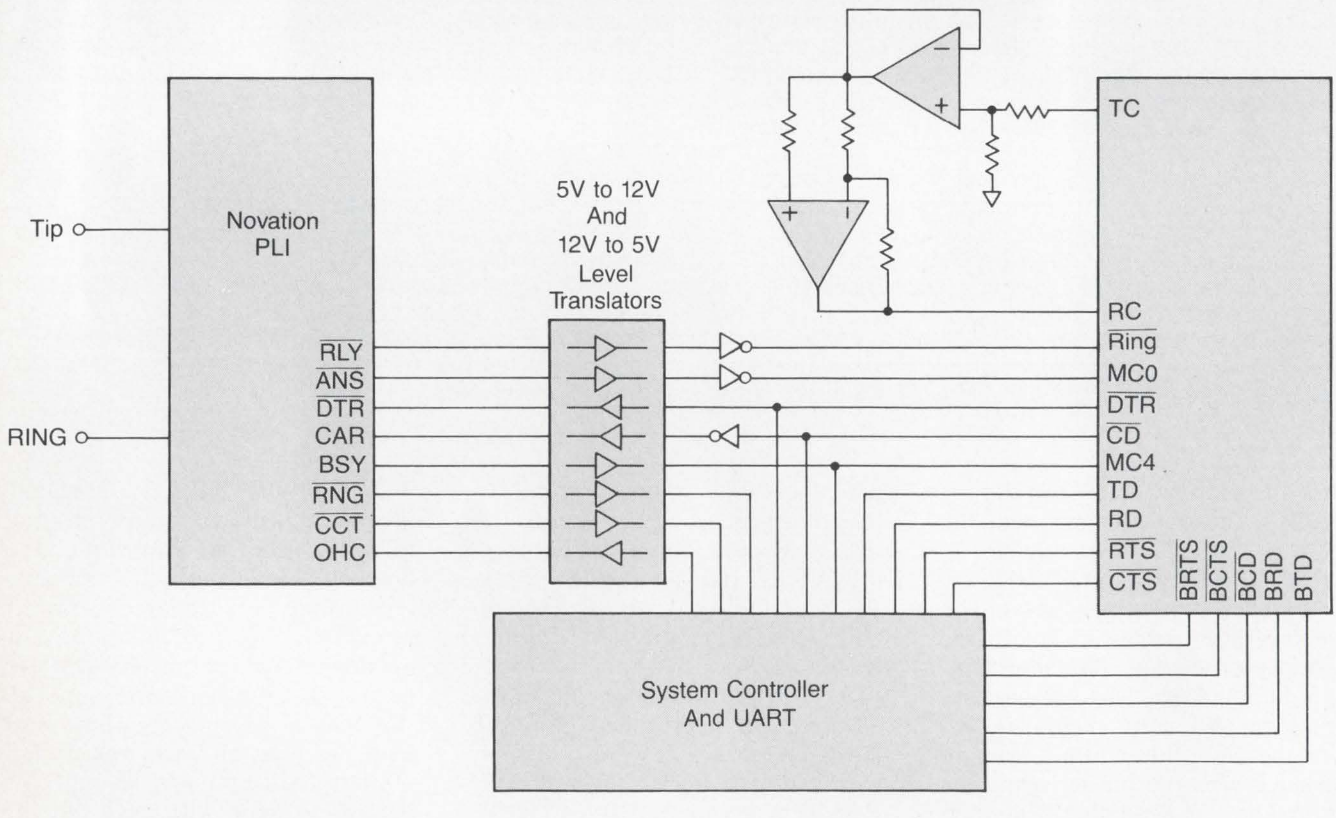

Figure 1a: Am7910 interfaced with Novation PLI

the receiver demodulates the analog signal present at the received carrier (RC) input into digital data at the received data outputs. Again, for 300-baud full-duplex and main channel 1200-baud half-duplex operation, the received digital data is available at the main received data (RD) output while 1200-baud back-channel data is available at the back received data (BRD) pin. In the 1200-baud Bell 202 and CCITT V.23 configurations, the RTS line controls whether the Am7910 is transmitting or receiving on the main or back channel. When RTS is low, the transmitter is set to transmit on the main channel and the receiver is conditioned to receive on the back channel. When RTS is high, the modem will receive on the main channel and transmit on the back channel.

The interface control controls the operation of the modem. The four mode control pins (MCO-MC3) select which modem is to be implemented: Bell 103, Bell 202, CCITT V.21, or CCITT V.23. MC4 provides loopback capability for testing each modem. Asserting MC4 high sets both the transmitter and receiver filters to the same frequency band. This allows looping back either the received data (RD) output to the transmitted data (TD) input (digital loopback) or the transmitted carrier (TC) output to the received carrier (RC) input (analog loopback). A full set of handshake signals are provided for main and back channel operation: request-to-send (RTS), clear-to-send (CTS), and carrier detect (CD). Data terminal ready (DTR) is a status signal from the data terminal to the modem signifying that the data terminal is ready to transmit and/or receive data. A low on the RING input informs the modem that there is an incoming call that must be answered. The Am7910 answer sequence consists of outputting a period of silence and then an answer tone on the TC output. The period of silence is required by the phone company to allow automatic billing machines to record the call. The length of time for the silence and the answer tone intervals and the frequency of the answer tone are determined by the modem configuration selected on the mode control inputs.

Coupling To The Line

The only external device required to connect the Am7910 to the phone line is a data coupler. Either a direct connect data coupler or an acoustic coupler may be used. A direct connect data coupler (also known as a data access arrangement or phone line interface) does not use the telephone handset but connects directly to the phone line,

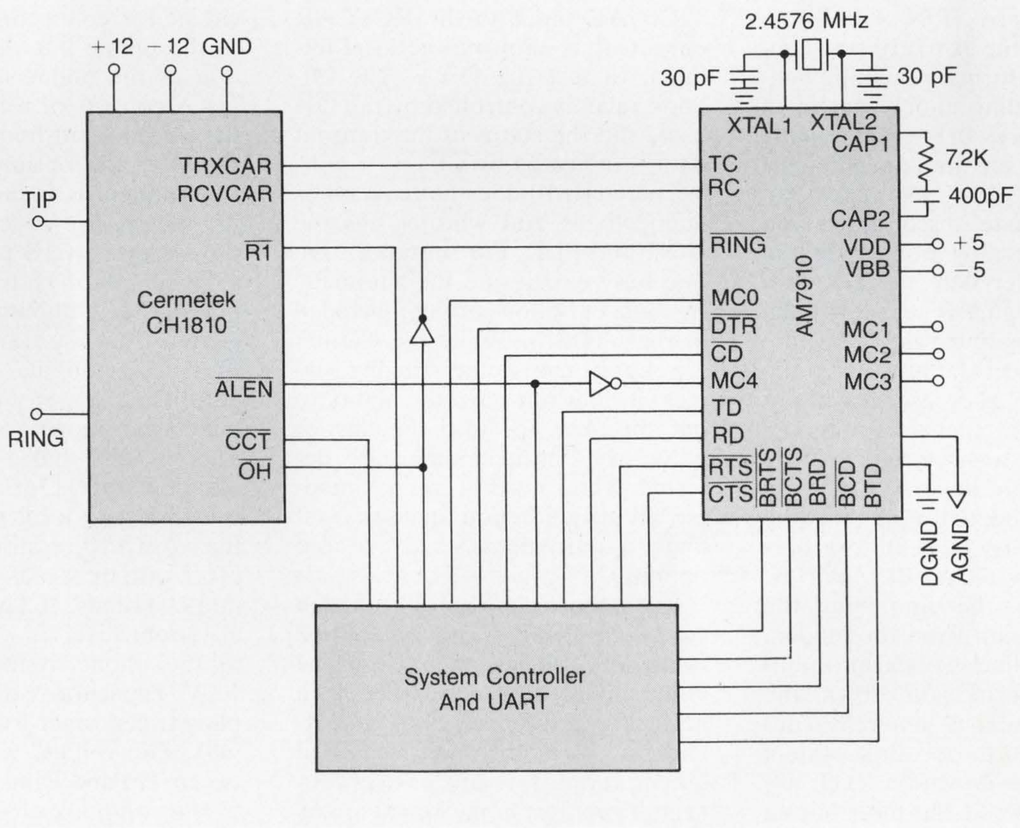

Figure 1b: AM7910 interfaced with Cermetek CH1810.

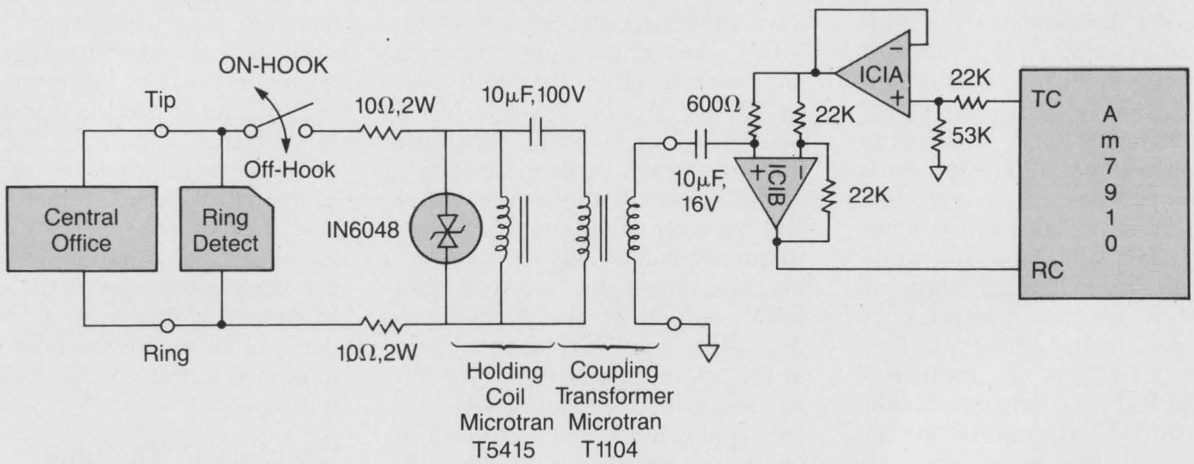

Figure 2: Am7910 Data access arrangement.

usually through a coupling transformer. An acoustic coupler, on the other hand, uses the telephone handset transmitter and receiver to send and receive signals.

A data coupler can be designed by the user or one can be purchased that has already been certified by the FCC. Recently there have been some module DAA devices introduced. When a Novation Phone Interface (P/N 490278) is connected to the Am7910, the configuration performs automatic calling (pulse dialing under control of the host processor) or automatic answering for any modem configuration **(Figure 1a)**. The Novation PLI can initiate disconnect upon loss of carrier by monitoring the Am7910 carrier detect ($\overline{\text{CD}}$) lead. If a ringing signal is sensed by the PLI on the Tip and Ring leads, the PLI will connect the modem to the line, drop the $\overline{\text{ANS}}$ lead low to put the Am7910 in the answer mode, and start the answer sequence by dropping $\overline{\text{RNG}}$ low. A line busy circuit is included for making the line appear busy to remote callers during testing. The PLI will be connected to the line, but the transmission path from the modem to the phone line is open, prohibiting data transmission down the line. The system is generally controlled by a μP or other system controller. The Novation levels are +12V and 0V, so the modem and the system controller logic levels must be buffered to the PLI as shown.

The Cermetek CH 1810 DAA module and a system controller are also easily interfaced to the Am7910 **(Figure 1b)**. Note that no duplexor is required with the Cermetek DAA because one is contained in the module. The input/output logic levels are standard 5V TTL levels. The CH1810 allows analog loopback by asserting $\overline{\text{ALEN}}$ low. This connects the TRXCAR input to the RCVCAR output, thus allowing the local terminal to test the DAA. The off-hook relay is controlled by the $\overline{\text{OH}}$ lead, and the status of the transmit path is indicated by $\overline{\text{CCT}}$.

The CH1810 does not contain as many "bells and whistles" as the Novation PLI. For instance, the line busy circuit and the automatic disconnect options are not included in the CH1810. While the Cermetek DAA can detect ringing signals, it does not have the ability to put the Am7910 into the answer mode when an incoming call is detected. The choice of a DAA module will depend upon the user's systems requirements and desired options.

If it is more economical to design your own DAA, a copy of Part 68 of the FCC rules available from the Government Printing Office is a necessary reference. Part 68 outlines the electrical and mechanical specifications for any device connected to the phone line. Part 68 does not contain any technical engineering information on how to design DAA's, but instead outlines certain specifications that may not be violated by equipment connected to the telephone network. If a DAA has been certified by the FCC (like the Novation PLI and Cermetek modules discussed previously), the modem connected to the DAA does not normally need to be approved by the FCC in addition.

Figure 2 shows a simple DAA circuit for connecting the Am7910 to the phone line. The major portion of the phone line side of the DAA consists of a holding coil for the on-hook/off-hook status and a ring detector for automatic answer. The modem is inductively coupled to the phone line through the transformer. IC1B provides 3dB of gain for the received signal and provides a minimum of 6dB of rejection from the transmit output to the receive input. The maximum permissive power that may be input to the phone system is -9dBm. This ensures that a maximum signal level of -12dBm will be received at the local office. Because the Am7910 transmitted carrier (TC) output signal level is 0dBm into 600 ohms, IC1A sets the proper output level at -9dBm for input to the phone system. The 10μF, 100V capacitor isolates the coupling transformer from the nominal -48V DC voltage which exists between Tip and Ring.

The on-hook/off-hook relay is controlled manually by the DATA/TALK button on the telephone, or by the automatic calling and auto-

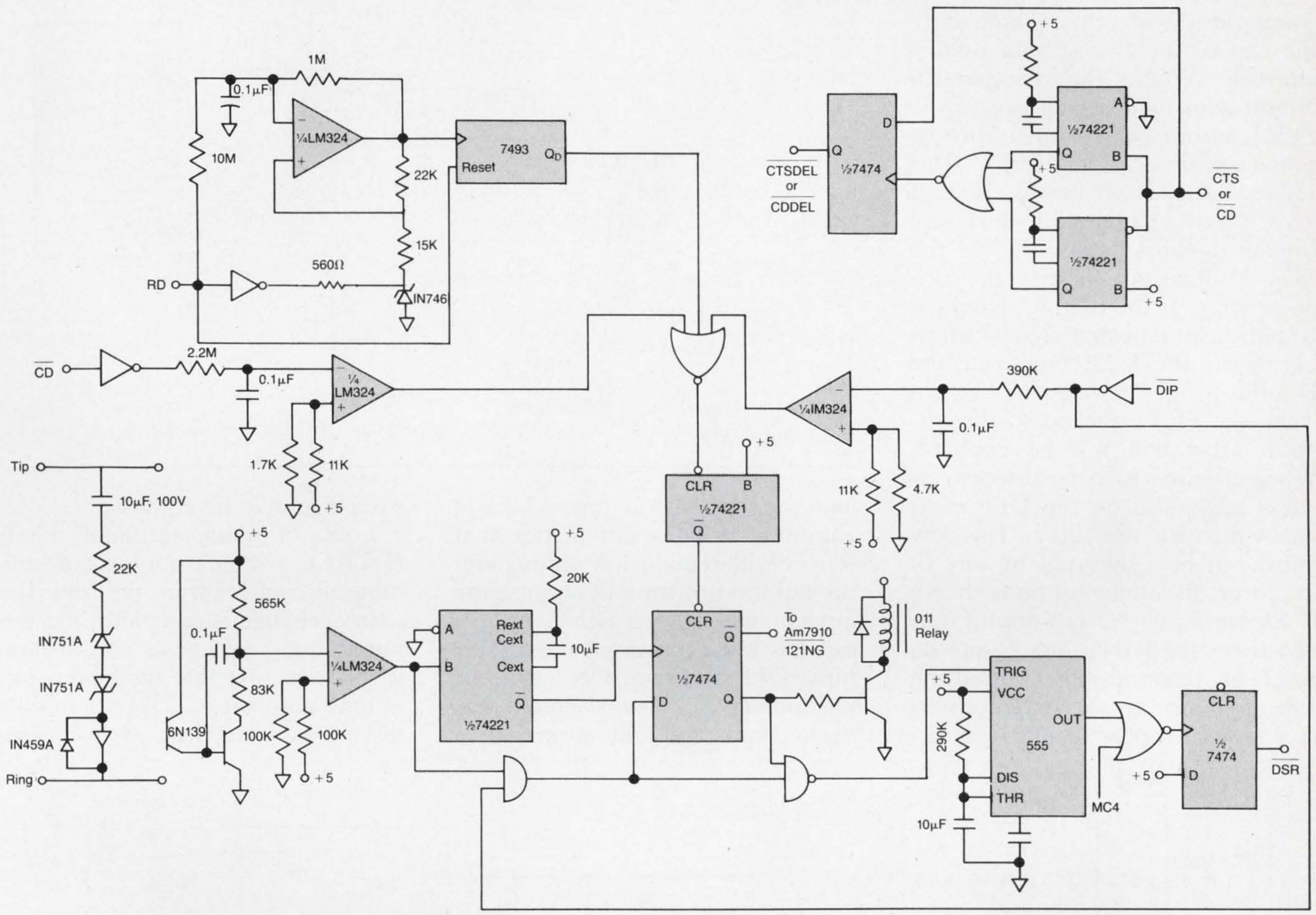

Figure 3: Customising the Am7910 to user's requirements.

matic answering circuitry associated with the modem. "On-hook" refers to the disconnected state; i.e., the phone is sitting on its cradle. "OFF-hook" means the DAA is connected to the line. When the phone line is off-hook, a DC current flows through the holding coil. By monitoring this holding current the phone company knows that somebody is connected to the line. The telephone company provides lightning protection for transients above about 1500V, but any protection below this must be provided by the user. The IN6048 is a transient suppression diode that turns into a low impedance device during a lightning hit. Because the circuitry in **Figure 2** has not been submitted to the FCC, for approval, it must be approved as outlined in Part 68 before being used.

Discrete Options

Discrete options may be included to completely customize the Am7910 to the user's requirements **(Figure 3)**. The automatic answer sequence may be utilized by incorporating a ring detection circuit; in this case it is also advantageous to have automatic disconnect circuitry to eliminate requiring a person to manually disconnect the line. For certain specific applications, the internal Am7910 handshake delays ($\overline{CTS}$ ON or OFF or $\overline{CD}$ ON or OFF) may need to be extended to meet the user's system requirements. In certain applications the user may want to include the modem status signal data set ready ($\overline{DSR}$).

Figure 3 shows the discrete options which may be included to completely customize the Am7910 to the user's requirements. It needs to be emphasized that none of the circuitry shown in **Figure 3** is required, but the circuits shown may be mixed and matched depending upon the system requirements. The circuitry shown includes ringing detection, generation of data set ready ($\overline{DSR}$), handshake delay extensions, and three disconnect options: loss of data terminal ready ($\overline{DTR}$), loss of carrier detect ($\overline{CD}$), and receive space.

The ringing detection circuitry **(Figure 3)** expands the ring detector circuitry shown in a block in **Figure 2**. Part 68 of the FCC rules discusses the US ringing signal characteristics; they can vary from 40V RMS to 150V RMS around 20Hz. When an AC signal greater than 7.0 V exists between tip and ring, the LED in opto-isolator 6N139 will just turn on the phototransistor.•Unless this signal reaches 40V RMS and at least 15.3Hz, the integrator voltage at V_c will not drop enough to change the state of the comparator high. If a valid ringing signal toggles the output of the comparator high, the comparator will remain high until the end of the two second ringing interval. When the comparator output goes high, it will trigger the 74221 monostable multivibrator which is timed for 138ms. This 138ms delay is to ensure that at least 2 and ½ cycles (at 20Hz) of ringing signal is present before the 7474 D flip-flop enables the off-hook relay. If the ringing signal (or a spuriously detected signal) drops out before the 74221 times out, the D input to the flip-flop will be zero when the FF is clocked so the off-hook relay will not be enabled. When the line is to be disconnected, a low pulse on the DFF clear line will open the relay. This low pulse can be generated by any of the three disconnect options shown in **Figure 3**. The D flip-flop $\overline{Q}$ output drives the $\overline{RING}$ input, and the Am7910 responds by outputting 1.3s of silence in US configurations (1.9 s in European configurations) and 1.9 s of answer tone (3.0 s in Europe). It does not matter that $\overline{RING}$ will remain low throughout the duration of the call because the modem will ignore $\overline{RING}$ once a call has been answered until $\overline{DTR}$ turns OFF and then ON again. At this point, call establishment has been completed and normal data exchange may take place.

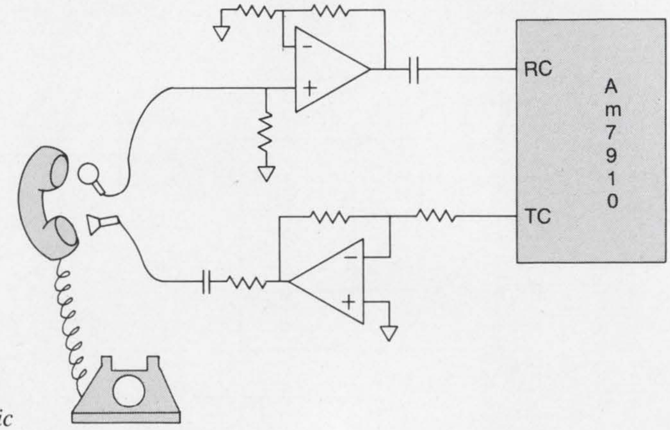

Figure 4: Acoustic Coupling Circuit.

Loss of data terminal ready ($\overline{DTR}$) is a standard means of initiating disconnect from the line. If a data exchange is complete, the terminals may exchange end-of-message codes. At this time both terminals may raise $\overline{DTR}$ to initiate disconnect. The loss of $\overline{DTR}$ dis-

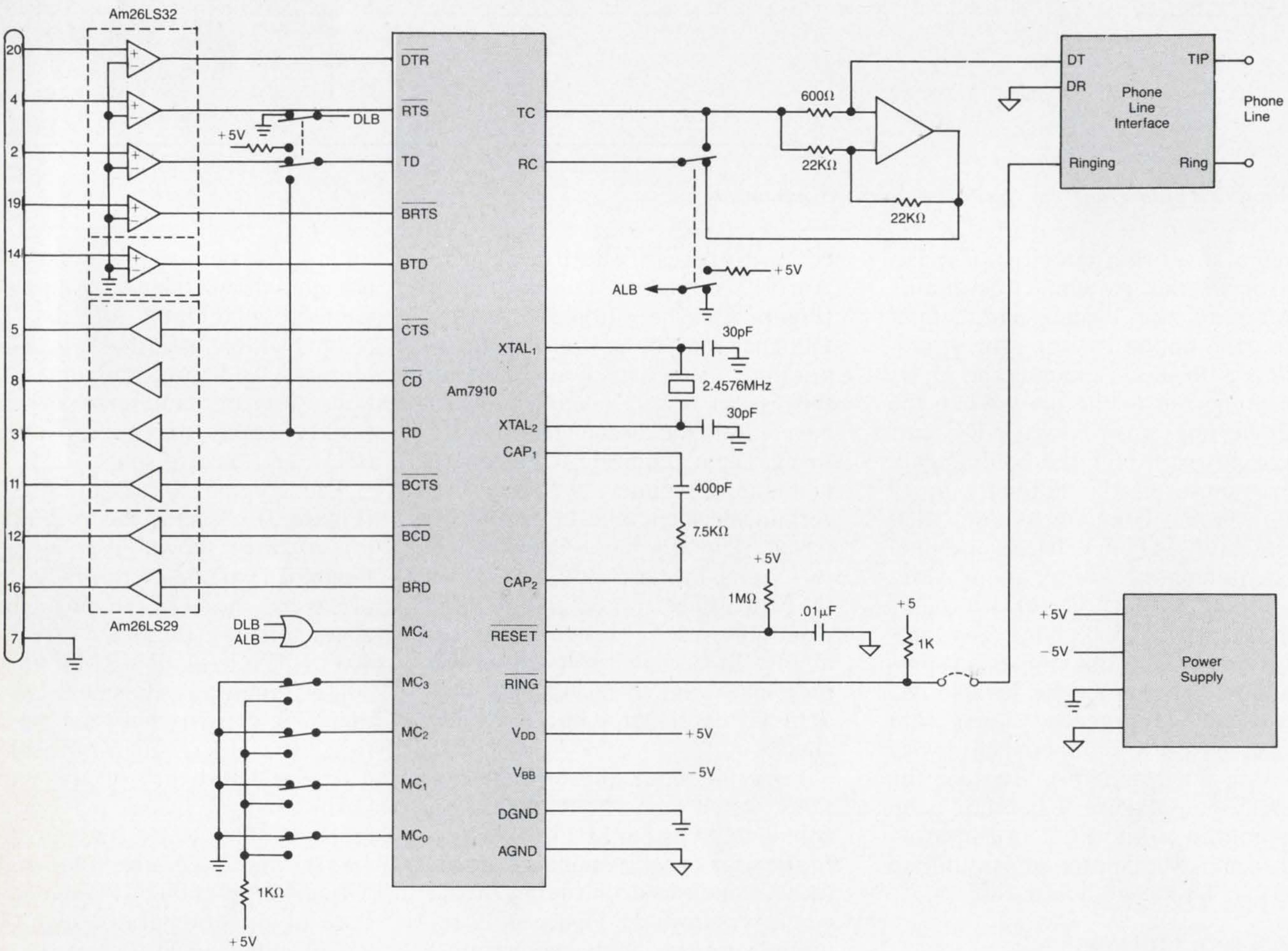

Figure 5: Am7910 FSK Modem.

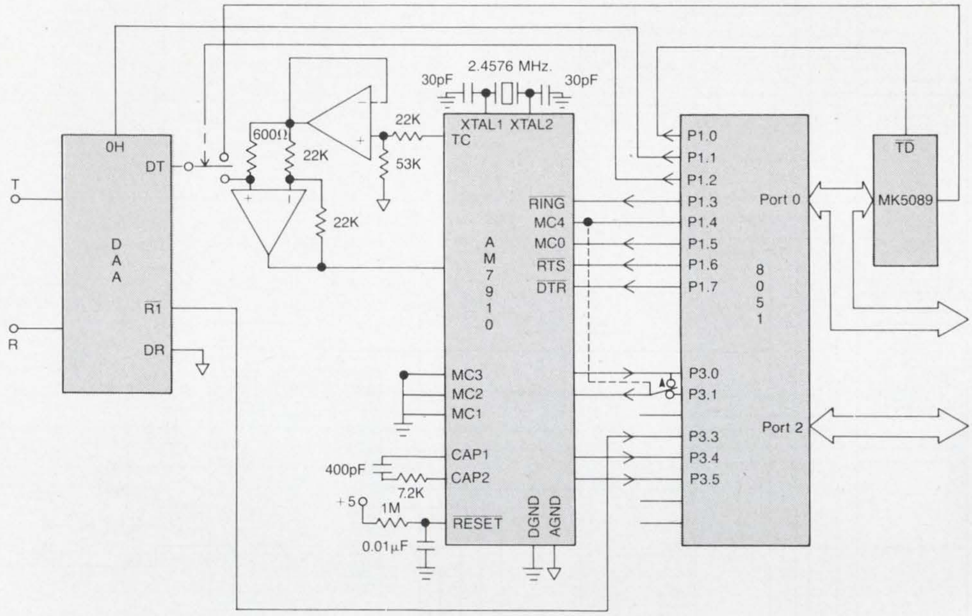

Figure 6: 8051 Single chip μP interfaced to Am7910

connect circuitry **(Figure 3)** initiates disconnect if $\overline{DTR}$ is raised for a time ≥50ms. The comparator output trips high, which will generate one pulse from the 474221 monostable multivibrator.

The loss of carrier detect ($\overline{CD}$) disconnect circuitry works exactly the same as the loss of $\overline{DTR}$ disconnect circuitry; the only difference is the loss of $\overline{CD}$ circuitry must have $\overline{CD}$ off (high) for ≥30ms **(Figure 3)** before disconnect is initiated. The loss of $\overline{CD}$ disconnect should only be used with 300-baud modems, because the $\overline{CD}$ pin for the 1200-baud configurations is only low when receiving data; hence, disconnect would be initiated 300ms after the remote modem ended its transmission. This feature is desirable in the 300-baud cases, however. For example if one of the data terminals decides that transmission is complete, its terminal may raise $\overline{DTR}$ to disconnect it from the line. Then 300ms after the local disconnect, the remote terminal would initiate loss of $\overline{CD}$ disconnect in response to the loss of carrier.

The receive-space disconnect option is available for both the 300-baud or 1200-baud configurations. If a space or binary "0" is received for 2.0s, the 7493 ripple counter counts to 8, which triggers the 74221 monostable multivibrator. The op-amp acts as an oscillator enabled by RD LOW; as long as RD is LOW, the 7493 will count. If a "1" is received on the RD line before the two seconds are up, the 7493 will be reset before the count of 8 is reached and the oscillator will stop. The next "0" received enables the oscillator and starts the 7493 counting again. With this disconnect option, a terminal that dominates the "conversation" may disconnect the other modem from the line by sending a stream of zeros. After sending zeros to disconnect the remote end, the local terminal would disconnect itself from the line by initiating a loss of $\overline{DTR}$ disconnect.

The disconnect option enables a terminal that dominates the "conversation" to disconnect the other modem from the line by sending a stream of zeroes.

Data Set Ready is a status line from the modem to the data terminal equipment in response to $\overline{DTR}$ LOW informing the DTE that the modem is ready for data transmission. $\overline{DSR}$ ON (low) indicates that the modem is in one of the following modes:

(1) Connected to the line
(2) Not in the TEST, TALK, or CALL modes.
(3) Completed the answer tone or CALL sequence

The Am7910 does not provide $\overline{DSR}$; however, $\overline{DSR}$ can be easily implemented in hardware for any modem configuration when required (**Figure 3**). When the DAA connects the modem to the line in an auto answer configuration, the

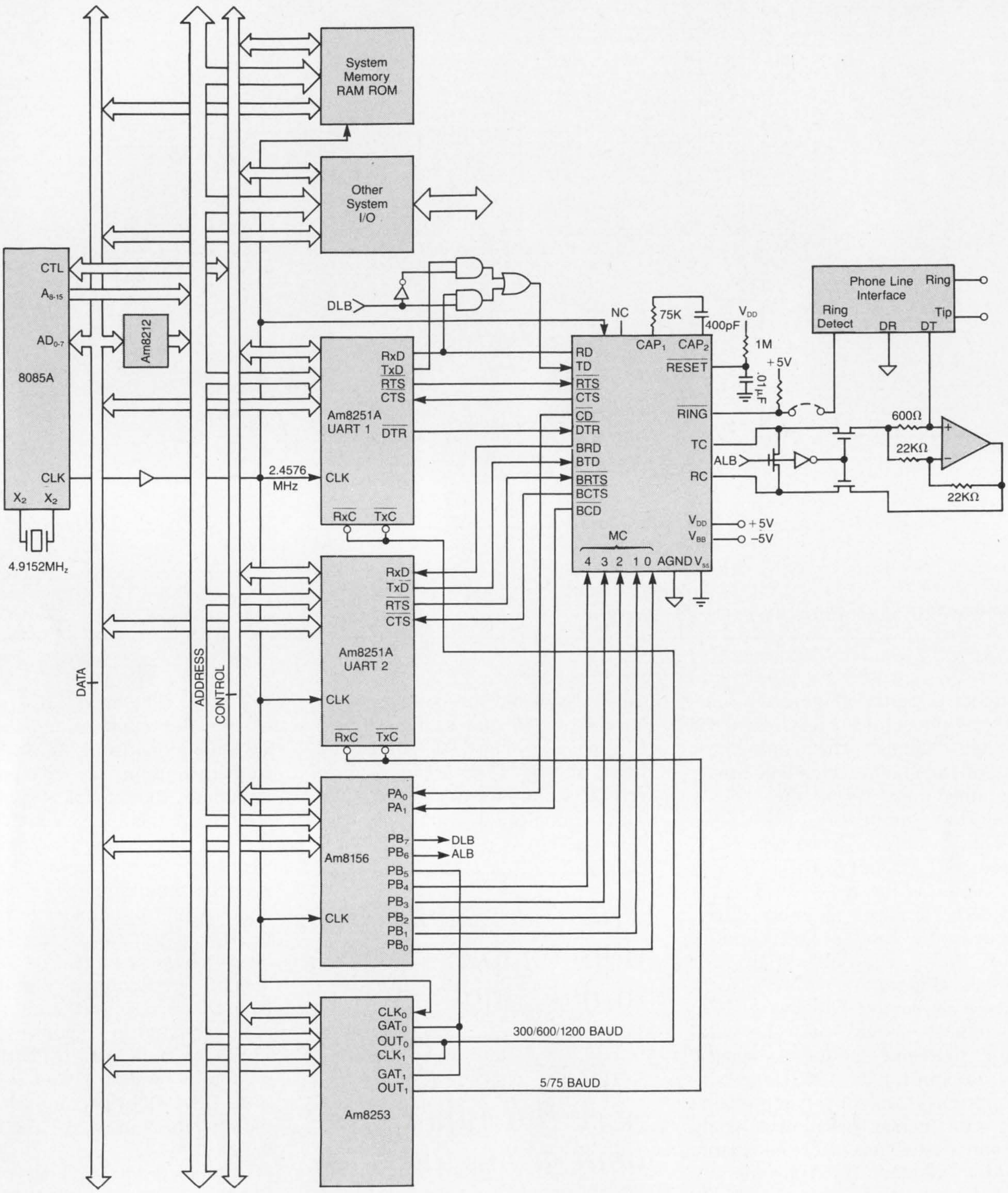

Figure 7: Am7910 in an expanded 8085 system.

555 is triggered by the AND condition of DTR on, the detection of a valid answer tone, and the off-hook relay being enabled. The 555 delays the triggering of the DSR flip-flop for 3.2s in the US or 4.9s in Europe to allow completion of the auto-answer sequence. Note that if the TEST mode is enabled (MC4 = 1), the DSR flip-flop will never be clocked ($\overline{Q}$ will remain high). This allows the phone to auto-answer a call, but DSR will never be enabled. This is consistent with condition 2 above.

The Am7910 handshake delays (RTS ON or OFF to CTS ON or OFF and receive carrier ON or

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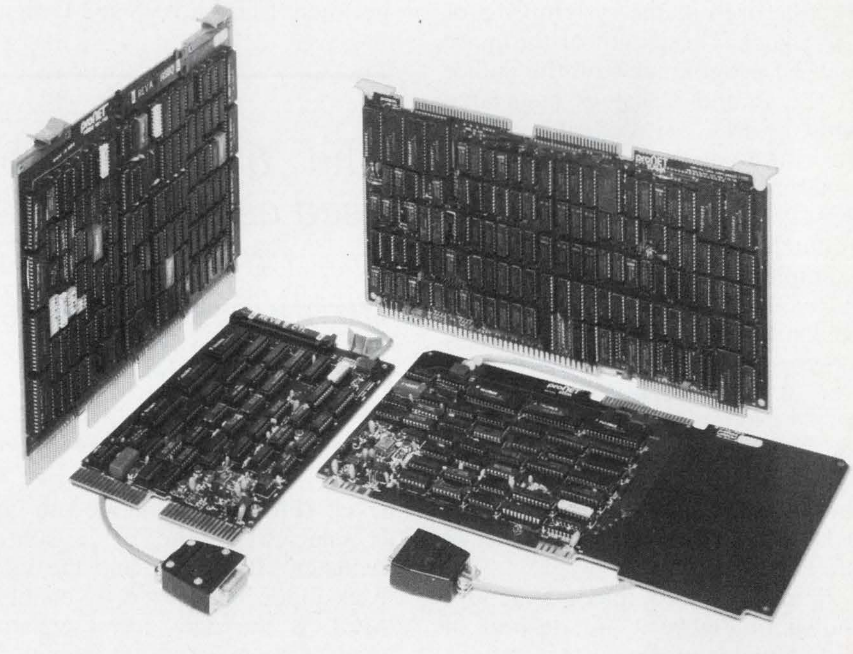

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OFF to $\overline{CD}$ ON or OFF) are fixed for the shortest delays allowable for switched network configurations. These delays may not be long enough for certain applications, but they can easily be increased if needed (**Figure 3**). The $\overline{CTS}$ or $\overline{CD}$ output from the Am7910 is connected to the 74221 monostable multivibrators as shown. A LOW on $\overline{CTS}$ or $\overline{CD}$ will enable the lower MV. On the trailing edge of the one-shot pulse, the DFF will clock the $\overline{CTS}$ or $\overline{CD}$ LOW value present at the input to the output. The DFF output may then be used as the system $\overline{CTS}$ or $\overline{CD}$ signal. The length of the pulse may be programmed by the choice of the R and C values associated with the MV. By the same token, the rising edge of $\overline{CTS}$ or $\overline{CD}$ will generate a pulse from the upper MV; its pulse length should be programmed in the same way. As an example, if a 1.0s total delay from $\overline{RTS}$ ON to $\overline{CTS}$ ON for the V.21 configuration is desired, the pulse length should be 1.0s minus 400ms. (the internal Am7910 $\overline{RTS}$ ON to $\overline{CTS}$ ON delay) equals 600ms for the lower MV delay. A proper choice of the R and C values for the MV will generate the required delay for $\overline{CTS}$ ON at the output of the DFF.

If many of the analog functions shown in **Figure 2** are desired, it would make more sense to use a μP or other system controller to generate the timing functions as opposed to using so much discrete hardware. However, if a single disconnect option is desired, for instance, it would probably be more cost effective to use the discrete hardware implementation.

Acoustic Coupler

With an acoustic coupler circuit, the Am7910 transmitter output passes through a gain stage to set the proper level to the speaker **(Figure 4).** The speaker then drives the mouthpiece in the telephone handset. The telephone earpiece output drives the microphone. The amplifier stage then sets the proper signal level for the Am7910 receive carrier input. Note that the telephone earpiece and mouthpiece are typically set in rubber cups to isolate the microphones and speakers from room noise. (Reference 1 provides additional information for designing acoustic coupling circuits. For instance, Reference 1 has two figures which help characterize the telephone handset speaker in the earpiece and the carbon microphone in the mouthpiece.)

System Applications

The Am7910 is used in standalone configurations simply by using standard RS-232-C line drivers and receivers to perform level translation between TTL and RS-232-C signal levels **(Figure 5)**. The modem type is selected by the mode control switches MC0-MC3, and the loopback mode is selected by enabling MC4. If the data access arrangement detects a ringing signal for automatic answer, the Am7910 $\overline{RING}$ input can be strapped to the DAA's ringing signal. If ring detection is not desired, simply trying $\overline{RING}$ high will disable the auto-answer sequence.

The 8501 can be used as an automatic calling unit through either pulse or tone dialing.

When configured with an 8051 single-chip μC, **(Figure 6)** the Am7910 takes advantage of the on-chip UART aboard the 8051. Full duplex 300-baud operation is available by programming the UART in the 8051 for the proper baud rate. The 8051 can be used as an automatic calling unit through either pulse or tone dialing. Pulse dialing is performed by pulsing the off-hook (OH) lead of the DAA. Tone dialing can be performed by incorporating a tone dialer chip like the Mostek 5089.

If tone dialing is desired, P1.2 would connect the MK5089 to the line by enabling its relay. (Specifications on pulse and tone dialing are given in References 2 and 3). If remote, or digital, loopback is desired, the 8051 can enable MC4 to put the Am7910 in the loopback mode while connecting the received data (RD) line to the transmitted data (TD) line. When loopback is selected, the Am7910 sets the transmit and receive filters to the same frequency band so that either the transmit carrier output can be directly connected to the receive carrier input (analog loopback) or the received data output can be directly connected to the transmit data input (digital loopback). The mode control pins are shown connected for the Bell 103 configuration, however, the CCITT V.21 configuration may be used in exactly the same way by simply tying MC2 to +5V instead of ground.

Normally both the transmit and receive side of the 8051 UART operate at the same speed, so if a half-duplex 1200-baud configuration is used with the 8051, some extra software would be required to "fool" one side of the 8051 UART into thinking that it is operating at 1200BPS. For instance, in the Bell 202 configuration, one side is transmitting or receiving at 1200-baud while the other transmits or receives at 5 baud. Programming the 8051 baud rate at 1200-baud would take care of the main channel, but the 8051 UART also tries to force the back channel to operate at 1200-baud. To get around this problem, assume the Am7910 is receiving on the main channel at 1200-baud. This also means the Am7910 is transmitting at 5 baud on the back channel. The modem receives 1200/5 = 240 bits for every one that is transmitted. When a low-speed bit pattern is to be sent down the line, the 8051 should output a new character for every 30 bytes (240 bits) demodulated by the receiver. Thirty bytes can be detected by counting the receiver interrupt flag which is generated each time a full byte is received. By the same token, low speed data may be read by the 8051 by modifying the software to account for

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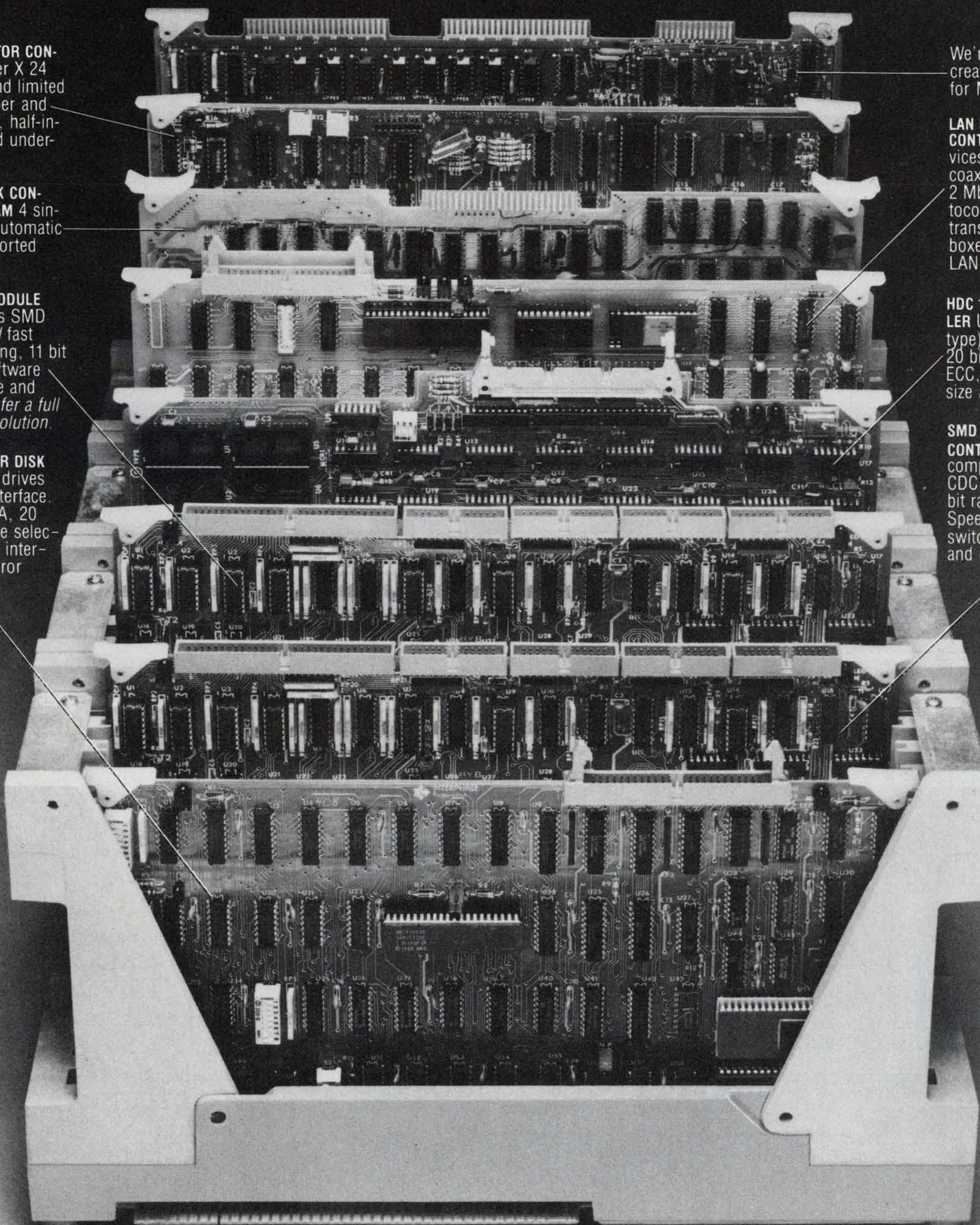

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reading one bit for every 240 bits transmitted.

Many of the analog circuit functions **(Figure 2)** may be performed digitally by the 8051. For instance, two of the disconnect options discussed earlier may be implemented easily by the 8051. By monitoring the $\overline{CD}$ or RD lines, the 8051 can initiate loss of carrier detect disconnect or receive-space disconnect by disabling the off-hook lead to the DAA relay.

The Am7910 becomes a powerful addition when connected to any μP-based system **(Figure 7)**. The 8085-based system requires two UARTs for half-duplex operation although only one if required for full-duplex operation. The Am8253 programmable interval timer generates the baud rate frequencies for the UARTs. The Am8156 RAM/IO/timer chip controls the mode settings of the Am7910 and provides loopback control. When digital loopback is selected, the data received by the modem on the RD line is passed through the and-or circuitry back into the TD input for retransmission over the phone line. When analog loopback is selected, the 8085 can test the modem by sending out a digital data stream. The analog carrier output on the TC lead is looped back into the received carrier input and demodulated back into the original digital data stream at the RD output. The small parts count required enables the modem to be put on the same PC board as the other digital circuitry.

References

(1) "Acoustic and Inductive Coupling for Data and Voice Transmission," October 1972, Bell System Technical Reference PUB 41803.

(2) "Data Communications Using the Switched Telecommunications Network," Revised May 1971, Bell System Technical Reference PUB 41005.

(3) "Data Couplers CBS and CBT for Automatic Terminals," May 1974, Bell System Technical Reference PUB 41802.

(4) Conversation with Edward DeWath, Standard Technologies Corporation, Berkeley, CA. □

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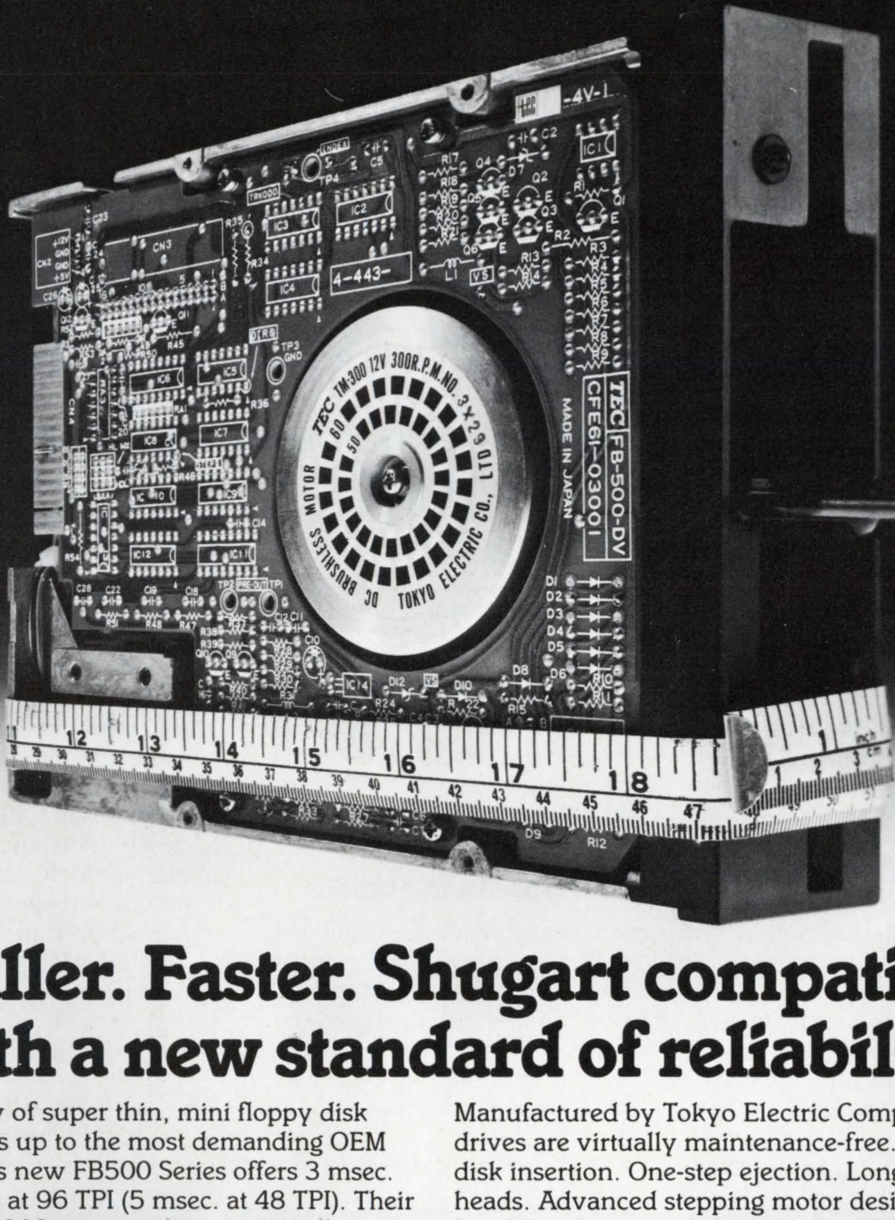

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ALU Speeds Image Processing For Q-Bus Or Multibus Systems

Real time image processing can now be done inexpensively, thanks to the new ALU-512 pipeline arithmetic logic unit introduced by Imaging Technology as the latest addition to their IP-512 image processing system. The IP-512 family consists of board-level products that combine with either a Multibus- or Q-bus-based host processor to create an image processing or computer graphics system. The minimum configuration consists of a frame buffer (FB-512) and an analog processor (AP-512).

The frame buffer contains 262 Kbytes of on-board RAM for the storage of a 512 × 512 pixel image. Each individual pixel has 8 bits of digital data, translating to 256 levels of grey-scale or color. The display memory can be treated as 8 binary planes of 512 × 512 × 1 images.

Any combination of bit planes can be write protected from the CPU or the AP-512's digitizer access. Bit plane 0 can also be selected as pixel write protect mask. Once set, the pixel has been masked, and can not be written to.

Read/Write access to the display memory while an image is being acquired is allowed. Pixel data can be transferred from the display memory to the host processor at up to 1.25 Mbytes/sec. Eight directions of auto-increment data transfer are supported. Digitized data transfer from the AP-512 requires only 1/30 sec to fill the FB-512's entire display memory at a 10 Mhz rate.

The analog processor utilizes precision offset from 0V to 2V, with 256 increments. Sample and hold circuitry assures DC restoration at each horizontal scan line at proper black level. The conditioned signal is then digitized via either 4, 6 or 8 bit flash A/D converter at 5 or 10 million samples per second. The digital output of the A/D is then passed through 256 bytes of look-up table (LUT) for pixel transformation. Finally, the output of the LUT is downloaded to the FB-512 for CPU or ALU processing. The video data from FB-512 is reconstructed by the AP-512, via 3 sets of LUT & D/As, to drive B/W or RGB color monitors. All LUTs are software programmable.

This system's subtraction capabilities make it ideal for assembly line inspection.

ALU Speeds Operations

The arithmetic logic unit (ALU-512) pipeline processor incorporates 5 stages of logic functions:

- 4:1 input operand selection; FB-512, AP-512, or constant.
- 8 bit multiplier
- 16 bit ALU
- 16 bit shifter
- 2:1 resultant data selector

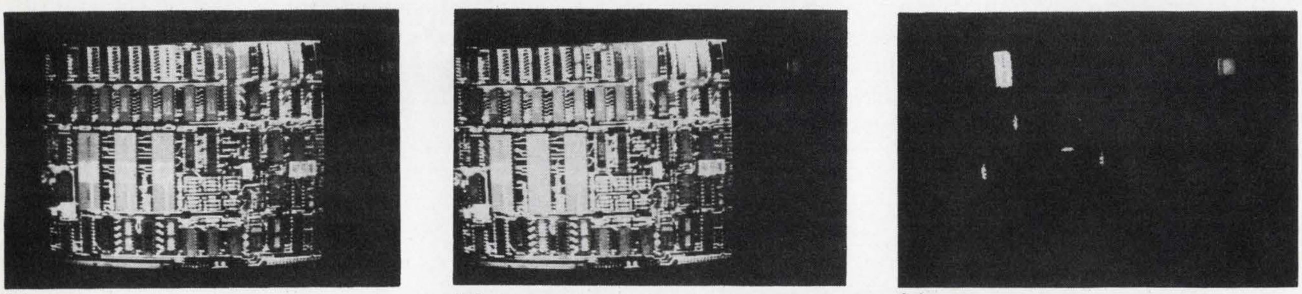
4:1 frame buffer data selector. The ALU-512 architecture will support up to four, byte wide FB-512 I/O channels, via four high speed video buses. Each FB-512 I/O channel can support multiple FB-512 image modules, out of which a 512 × 480 display window is selected.

A byte-wide I/O channel is dedicated to the AP-512 module, for digitized image input and video display output. Each byte-wide channel can be routed to different internal ALU data paths from the five 4:1 input operand selectors. The 4:1 data selector can be used to select 8 or 16 bit operands. The five sets of 2:1 selectors choose either the selected 4:1 frame buffer data, a programmed constant, or the A/D digitized input data. The selected constant can be set to zero for null operand, or it can be a kernel element for the convolution process. The A/D data can be entered via the 2:1 selector. A fifth 2:1 selector is dedicated for the output display channel.

8 bit multiplier. The 8 bit multiplier stage multiplies two selected 8 bit pixels and is used in image convolution and scaling. The entire multiple stage can be bypassed for operations not requiring multiplication to occur.

16 bit ALU. The 16 bit ALU operates on two 16 bit operands, A and B. The standard arithmetic and logic functions are:

B MINUS A
A MINUS B
A PLUS B



(a) (b) (c)

Figure 1: The image subtraction capabilities of the ALU-512 make it ideal for inspection applications. In the application shown above, the image of a printed circuit board under inspection (b) is subtracted from a "correct" circuit board (a) and the difference—a missing IC and some resistors—is shown in C.

A XOR B
A OR B
A AND B

When overflow or underflow occurs, the user has the option to force the resulting 16 bit output to be high.

16 bit shifter. The 16 bit shifter is used to either shift or rotate the 16 bit ALU output data. The resultant effect is multiplication or division of the 16 bit data by powers of 2. This function is required for image averaging.

2:1 resultant data selector. For sets of 2:1 16 bit data selectors route the final data back to any selected frame buffer for storage of data.

Quality Control

Real-time inspection is one application to which the IP-512, with the optional ALU, is particularly well-suited. This application can be useful in quality control situations, where items on an assembly line must be visually examined for conformity.

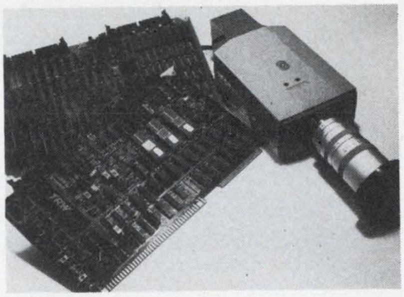
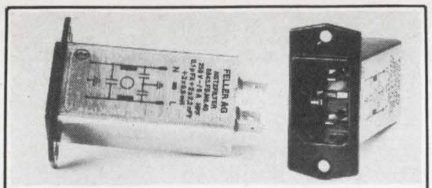


Figure 2: The IP-512 image processor and graphic controller features the unique combination of modular frame buffer (FB-512), analog processor (AP-512) and pipeline processor (ALU-512), for flexible digital image processing. Combined with a Multibus or Q-bus based computer, the IP-512 becomes a complete Image Processing system.

The ALU-512 subtraction abilities make this application possible. A video camera may scan printed circuit boards, for example, for image intensity and shape at a rate of 30 to 60 times/sec. The analog processor converts this scanned data into digital form, in a 512 × 512 or 256 × 256 area, with each matrix element having up to 256 levels of grey. The frame buffer then stores 512 × 512 × 8 bits of digital data. Finally, the ALU-512 performs a subtraction, determining the difference between the image of the PCB under inspection and that of a correct PCB stored in memory. As shown in **Figure 1C,** the system can readily detect missing components.

Price of the ALU-512 is $2995; the FB-512 frame buffer sells for $3995; and the AP-512 analog processor ranges in price from $2395 to $3995, depending on number of A/D and D/A converters. **Imaging Technology, Inc,** 400 W. Cummings Park, Suite 4350, Woburn, MA 01801. **Write 200**



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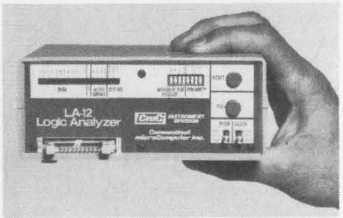

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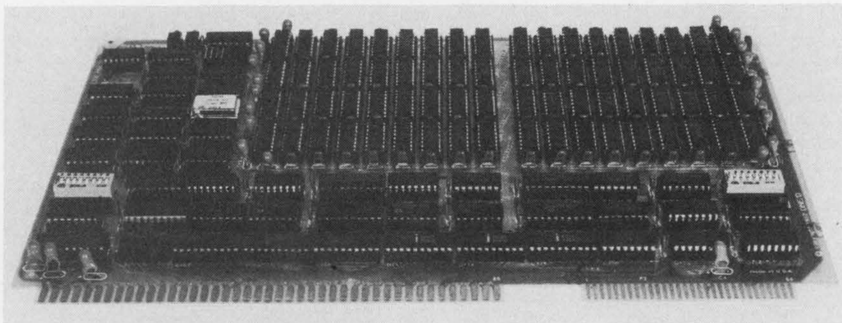

According to Terry Doone, President of One/D, the fundamental concept underlying his product line is to offload as much intelligence and functions as possible from the CPU module, pushing them out to peripherals and memories, resulting in a more distributed overall system.

Not surprisingly then, the company's "Smart RAM" memory series has incorporated memory management capability, whose traditional place has been on a CPU board.

This memory management feature takes a 16-bit address and maps it into a 20-bit address space, thus expanding a 64 Kbyte space into a 1 Mbyte space. The scheme implemented is flexible enough that the popular "page register" method turns out to be a subset of its capabilities. When the mapping is disabled, the card reverts back to a standard "dumb" memory card responding to all 20 Multibus address bits. Switching between smart and dumb modes is accomplished dynamically under software control.

There are other advantages resulting from the memory management feature being on the memory card.

- An existing 64 Kbyte system can be expanded to directly address more memory without having to redesign or replace the CPU module. Furthermore, existing software can run in unmapped mode as is, while new software going beyond 64 Kbyte can run in mapped mode. Both software and hardware investments are thereby protected. A system upgrade is therefore possible with virtually no disturbance to the existing configuration.
- In a multiprocessor system, the memory manager is common to all CPU modules, and even non CPU master modules such as intelligent peripherals capable of DMA. This uniformity eliminates the complication arising from having to communicate the different mapping states of various CPU modules amongst each other.
- In a multi-user/multi-tasking system, the dynamic mapping provides fast context switching through only a handful of output commands.
- Even used as plain "dumb" memory, it protects against future unforeseen expansion requirements.

All the above are possible with standard off the shelf 8-bit as well as 16-bit CPU cards with no special addressing designs.

Smart RAM is available in several sizes, from 32 Kbyte to 512 Kbyte, all with parity error checking and logging as a standard feature. The various model numbers are tabulated below:

Model No.	Memory Size
SRM 032	32 Kbytes
SRM 064	64 Kbytes
SRM 128	128 Kbytes
SRM 256	256 Kbytes
SRM 512	512 Kbytes

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Write 197

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GRAPHICS

From Andromeda

THE CONTROLLERS: The VDC11 family of dual-width, Q-Bus resident Video Display Controllers provides the basis for building your own graphic display subsystem, or . . .

THE TERMINALS: The VDT11 family of complete Video Display Terminals combines the appropriate VDC11 controller with an attractive 12″ video monitor, separate serial keyboard, and interconnecting cables

FEATURES

- 512H x 256V Physical Display Resolution
- Display processor emulates popular terminals for software compatibility
  - ADM-3A or VT52 in Alpha mode, Tek 4010 in Graphic mode
- Q-Bus resident, dual-width controller
  - Emulates DLV11, may be system console device
- Controller includes extra, independent, RS232 serial interface
  - May be used for serial printer, modem, another terminal, or any RS232 device
- Many enhancements including: Smooth scrolling, selective erase, screen readback, and multiple display pages (optional)
- Low cost: Controllers start at $1200 each and complete graphic terminal subsystems at $1700 each

The VDC11/VDT11 is also available in a standalone version that does not require a Q-Bus based system. In this configuration, the VDC11 communicates with the host system via the RS232 serial interface. Andromeda also offers a variety of other graphics related hardware and software. Call or write for details.

ADM-3A is a product of Lear Siegler, Inc.
VT-52 is a product of the Digital Equipment Corp.
Tek 4010 is a product of the Tektronix Corp.

Prices are domestic U.S.A. only

ANDROMEDA SYSTEMS INC.
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CANOGA PARK, CA 91304
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TWX: [910] 494-1248

VLSI CAD/CAM SYSTEM

For IC Mask Design And Manufacturing Applications

The Series 100 features a multiple CPU system architecture together with field proven CAD/CAM software. It interfaces directly with other IC design systems' data and can be used either as a standalone design system or linked in distributed networks with other VIA Systems and/or larger machines. It includes a DEC LSI-11/23 minicomputer with 256 Kbytes of main memory, a high-speed 35 Mbyte Winchester disk drive and a 17 Mbyte 6400 bpi tape cartridge; a design station including an alphanumeric terminal with user-programmable function keys, an 11″ x 11″ data tablet for online design, and a graphics sub-system containing a graphics processor, video controller, and a 19″ high resolution, 60 Hz, flicker-free, color monitor. From $90,000. **VIA Systems Inc,** 11 Concord St, Nashua, NH 03060. **Write 146**

TURNKEY CAD SYSTEM

Comprehensive 2D Drafting System

ANVIL-3000D Advanced Interactive Drafting package interactively instructs users in the procedures to become productive in computer-aided design and drafting. It incorporates a menu-driven interactive language that provides computer-aided instruction (CAI) on the major areas of CAD and examples of how those areas are used to produce drawings. The built-in instruction, when coupled with the ANVIL-3000D Training Manual, eliminates the requirement for classroom training. It supports between 6 and 8 terminals on most 16-bit computers. In concert with any of the ANVIL IID (Intelligent Interactive Display) series graphics devices, this

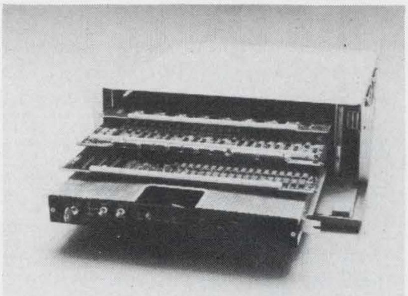
software will support 30 to 80 terminals on an appropriately configured 24-bit-word or larger computer. Offered either as a turnkey system or as an unbundled software package for use on 16-bit and larger computers.

As a turnkey system, ANVIL-3000D equipment will be offered initially with a Hewlett-Packard 1000 minicomputer and ANVIL-1200 IID interactive display with keyboard, joystick and ANVIL Workplane with drafting overlays for data entry at the touch of a stylus. With display workstation this system is $90,000. ANVIL-3000D software can be leased for $1750 per month for a package that can support up to two workstations. **Manufacturing and Consulting Services Inc,** 17942 Cowan Ave, Irvine, CA 92714. **Write 150**

NOVA PROCESSORS

Alternatives To Nova 4X Computers

Series 200 processors, available in 5- and 11-slot versions, offer 200 ns microcycle performance with full Nova 3 and Nova 4 memory mapping capabilities including 4- or 8-way memory interleaving. A variable microcycle feature allows reduction of microcycle



times of 120 ns increasing performance even more. Standard MOS memory is available in 128 Kbyte increments, packaged on 15″ boards containing up to 256 Kbytes each, and expandable to 512 Kbytes. Features include micro diagnostics for self test on power-up, built-in debugging aids and memory diagnostics, extended stack facility, an integral RS-232 compatible port with resident auto-load boots, a real-time clock, and support for full byte parity. Processors also include full battery backup logic, and off-the-shelf 240- or 550-Watt power supplies. **Digidyne Corp,** 2625 Ariane Dr, San Diego, CA 92117. **Write 143**

RESEARCH SYSTEM

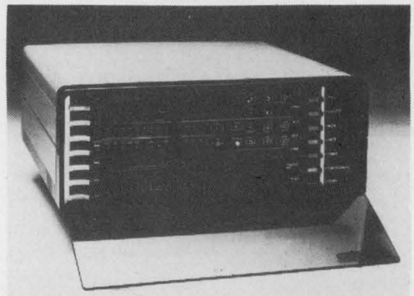
New VAX Capabilities

A complete reimplementation of RS/1 for the VAX, RS/1-PLUS features extensive improvements to the "Electronic Lab Notebook." This includes enhanced graphics support, table control, and programming tools, as well as full utilization of the VAX environment. RS/1-PLUS runs in VAX native mode under VMS and UNIX. Full VMS and UNIX support includes: sharable task image (reduced memory, disk I/O requirements); full use of VAX instruction set with long integers and double precision floating point; and improved execution and compilation speed. Presentation-quality graphs, bargraphs and pie charts can be created with simple commands. **Bolt Beranek and Newman Inc,** 10 Moulton St, Cambridge, MA 02238. **Write 140**

MODEM

With 6 Port Multiplexer Option

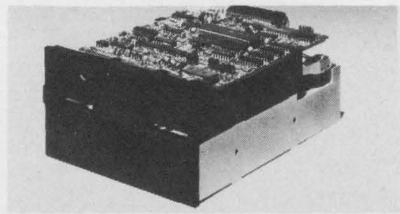
MP-14.4 provides 50% more throughput per voice grade circuit than was previously possible. The 6 port multiplexer option integrates several slower data signals, up to a maximum of 14,400 bps, onto one composite VF signal. In this way the modem, acting as a master (or tandem master modem at a remote location), eliminates the need for multiple parallel telephone circuits. It accumulates channel impairment data on a continuous basis and permits evaluation of modem performance and line degradation. Addition of Paradyne's ANALYSIS Network Management System adds immediate and predictive diagnostics. **Paradyne Corp,** PO Box 1347, 8550 Ulmerton Rd, Largo, FL 33540. **Write 160**



2 MBYTE 5¼" FLOPPY

Exceeds 8" Disk Drive Capacities

The µP-controlled TM102 is designed as a real-time, RAM memory for small business systems and word processing systems. Users can expand capacity 2, 4, or even 8 times with no



change in cabinet size of power supply. It features a 96 tpi configuration and a fast track-to-track access time of 3 ms. Average access time is 95 ms, including head settle time. Density is 11,754 bpi and data transfer is 500 Kbytes/sec. A µP provides microstepped head positioning for improved 96 tpi track accuracy. $325 in OEM/qty. **Tandon Corp.** 20320 Prairie St, Chatsworth, CA 91311. **Write 162**

LEVEL METER

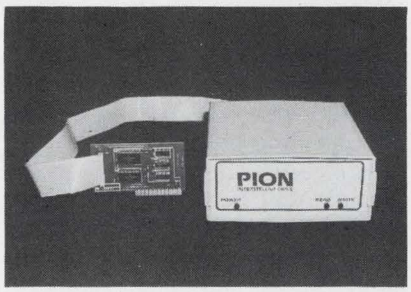
Fills Requirements Of Both Bench And Systems Engineers

The 5002 combines new analog measurement techniques with existing digital voltmeter technology. It uses 3 AC detection techniques (Peak, Rectified Mean, and True RMS) for total versatility and accurate measurements from DC to 20 MHz. Front panel selection of any of the 3 detectors—in addition to the choice of either a voltage or power measurement—makes this instrument ideal for work on complex and random noise waveforms. AC or DC coupling and the ability to perform the measurement over selectable periods of time from 100 ms to 100 sec further add to its versatility. **Racal-Dana Instruments Inc,** 18912 Von Karman Ave, PO Box C-19541, Irvine, CA 92713. **Write 161**

DISK DRIVE EMULATOR

64K DRAM Technology

The basic unit consists of 256 Kbytes of storage, user expandable to 1 Mbyte, an appropriate interface card, and all necessary cabling. Automatic power failure detect is combined with battery backup to eliminate data loss due to power failures and to retain data after the computer is powered down. Interstellar Drive comes with



its own independently regulated power supply to prevent power drain to the host microcomputer. Drivers, diagnostics, and utilities software are all provided as part of the basic package. **Pion Inc,** 74 Appleton St, Arlington, MA 02174. **Write 159**

CARTRIDGE TAPE SYSTEM

Stand Alone Intelligent Unit

The 1200S is an ideal companion product to off-the-shelf RS-232C data loggers and data acquisition devices, as well as a program loader and data storage system. It features simple manual operation and a flexible software package that facilitates remote control via ASCII control characters. The ANSI compatible, 4 Mbyte 1200S features automatic telephone answering, line monitoring and control, plus a standard power fail recovery system. Interfacing and software can be tailored to customer's applications. $2245. **ALGO Inc,** 10336 Nightmist Ct, Columbia, MD 21044. **Write 169**

APL TERMINAL

Expanded Overstrike And Edit Features

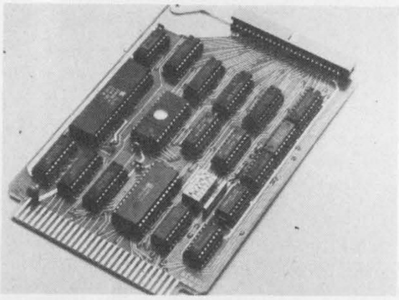
The AJ 520/A video display terminal recognizes 70 standard and up to 128 user-defined overstrike characters. It is an ANSI standard, 132/80-column display with detachable keyboard, extra large letters on a 15" screen, 4 pages of set-up menus in plain English, and 24 user-programmable function keys. The terminal also offers a range of features important in many APL applications. These include memory expansion to 21K, bi-directional scrolling, optical filter for added glare reduction, video output connection for external monitor, and a

printer port connection. **Anderson Jacobson Inc,** 521 Charcot Ave, San Jose, CA 95131. **Write 154**

INTELLIGENT PIO

Combines Multi-LS TTL Level Input With Data Acquisition

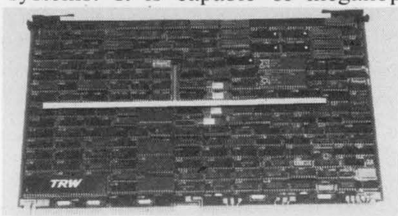
The ST 4394 single board Intelligent I/O processor monitors 32 LS TTL level inputs and incorporates onboard Z80A CPU, Z80A CTC, 2 Kbyte EPROM and 1 Kbyte RAM. Eight bits of LS TTL level output for control or status functions are also provided. Communication with the host processor may be accomplished via interrupt or parallel polling structure. The board occupies 4 consecutive, switch selectable I/O locations within the host processor's address space. The onboard processor can execute the Monitor/Control program, while leaving the host processor free to perform system level tasks. The ST4394 $275, qty and OEM discounts avail. **Applied Micro Technology Inc,** PO Box 3042, Tucson, AZ 85702. **Write 177**



ARRAY PROCESSOR

For M68000 Versabus μC Systems

SKYMNK-V is a full 32-bit floating-point array processor. This fully programmable unit is contained on one Versamodule and comes complete with software to support signal processing and other number crunching tasks on M68000-based Versabus systems. It is capable of megaflop



speed (one million floating point operations per second) for numerically intensive applications. Features include: 32-bit floating-point arithmetic with IEEE standard format; 48-bit extended precision for selected operations; real, complex and integer arithmetic instructions; and shared memory with host. **Sky Computers Inc,** Foot of John St, Lowell, MA 01852. **Write 187**

TAPE DRIVE CONTROLLERS

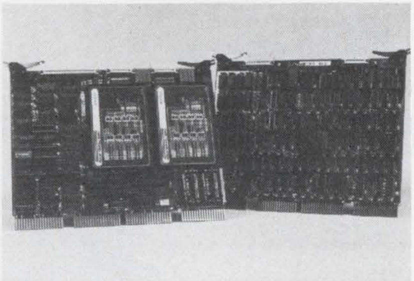
Link IBM Compatible Tape Drives to Variety of μP Buses

The ITS Family is a line of intelligent 8085-based controllers that link IBM compatible 9-track formatted tape drives, such as the Cipher Microstreamer, to the S-100, SS-50, and TRS-80 Buses. Unburdening the main processor of the tape drive control task, they are ideal for multi-processor and multi-user systems. Featuring software selectable ASCII to EBCDIC code conversion in firmware, they currently include the ITS-100 (for S-100), ITS-50 (for SS-50), and ITS-80 (for TRS-80). Software is supported under CP/M, MP/M, DPC/OS, OS-9, and TRSDOS. $850. **Alloy Engineering Co,** 12 Mercer Rd, Natick, MA 01760. **Write 175**

ANALOG OUTPUT BOARD

With Dual Ported RAM Board Achieves 800 KHz Operation

This LSI-11 Bus compatible digital to analog converter interface features data transfer rates from memory at up to 800 KHz, an advanced on-board multiplexer RAM channel list, and simultaneous output capabilities. The DT3366 Analog Output System

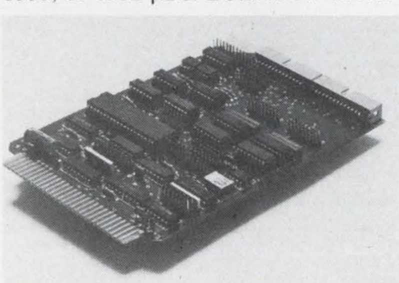


allows the user to drive up to eight 12-bit D/A channels directly from memory at up to a 400KHz transfer rate without processor intervention. When used with the DT3369 Dual Port RAM board, the DT3366 can transfer data from memory at an 800KHz rate via an external bus, without halting the processor requiring use of the procesor bus. The DT3366 may be optionally expanded with the DT3376 8 channel expander board. Up to 3 DT3376 interfaces can be connected to a single DT3366 for a total system capability of up to 32 D/A channels. The DT3366 is $2195 for the 4 channel version in 1-9 qty. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Write 179**

SERIAL I/O CARDS

Provide RS-232 And RS-422 For STD Bus

Capable of supporting all forms of serial communication for STD Bus systems, SB8422 and SB8412 cards contain two independent, full duplex channels. The SB8412 accommodates STD-Z80 bus systems; the SB8422 is for STD Bus systems based on the 8080, 8085, 8088, 9995, 6800, or 6502 μPs. Both allow the ad-

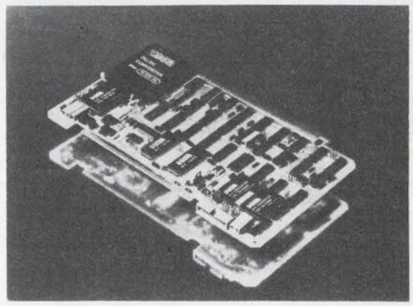


dition of serial peripherals to STD Bus systems. Each of the two card versions supports serial communication in async, bite sync (BISYNC), and bit sync (SDLC, HDLC, ADCCP) protocols. On-board baud rate generation provides 50 to 19.2K baud in the async mode, 800 to 307.2K baud in the sync mode, or DC to 500K baud using externally supplied clocks. They support both RS-232 and RS-422 interfaces. In qty 25, the 2.5 MHz version of the SB8412 is $195, the 4 MHz version is $235; a 4-MHz SB8422 is $245. **Micro/Sys,** 1367 Foothill Blvd, La Canada, CA 91011. **Write 183**

A/D–D/A BOARD

For Motorola's Exorciser And Rockwell's System 65

The SineTrac ST-6832 A/D–D/A Board interfaces both analog input and output signals, plugs directly into any card slot, and is fully compatible with any other microcomputer modules that are bus compatible with either the EXORciser or System 65. It



accepts up to 32 single-ended or 16 differential analog input channels. Under program control from the microcomputer, particular analog channels are selected and digitized. The digitized data is then stored in user selected memory locations so that it may be further processed. Also, 2 D/A channels may be included for data distribution. It is a memory-mapped device that is organized around 8 basic registers. These 8 consecutively addressed registers have a user selectable base address. Starts at $689 for 32 A/D channels, and gains of X1, 2, 4 and 8 only in qty 1-4. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048. **Write 180**

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Siemans Corporation
SONY Corporation
Tandberg Data, Inc.
TEC, Inc.
TECSTOR, Inc.
TRILOG
Universal Data Systems
XYLOGICS

Date	*Location*
1982	
Sept. 8	**Newton, MA**
Sept. 28	**Chicago, IL**
Oct. 11	**Westchester, NY**
Nov. 3	**Palo Alto, CA**
Nov. 8	**Denver, CO**
1983	
Jan. 20	**Orange County, CA**
Feb. 1	**Dallas, TX**
Feb. 3	**Houston, TX**
Feb. 28	**Atlanta, GA**
Mar. 29	**Ft. Lauderdale, FL**

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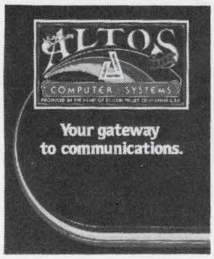
Shouldn't You Be Among Them?

New Literature

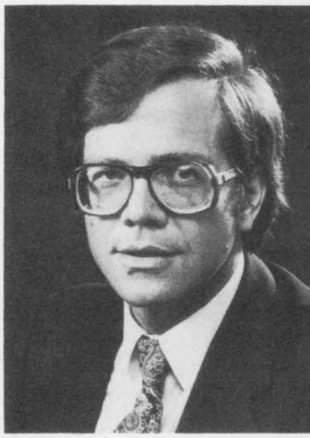
Power Supply Catalog. A line of 6 new high-efficiency AC/DC power supplies and 12 new low-profile DC/DC converters are featured in this 12-pp. Power Supply Catalog. Included is information on 4 new triple output supplies and 2 new single logic output supplies. The supplies are available in PC Mount or Chassis Mount versions; prices start at $106 in quantities of 1–4.
Analog Devices **Write 252**

Disk Tech Data. A technical data sheet details the STC 8675 high-performance disk subsystem. Designed specifically for the 4341 CPU user, the 8675 consists of two storage directors and four disk drive units. Subsystem capacities range from 2,540 megabytes with eight single-density spindles, to 5,080 megabytes with eight double-density spindles.
Storage Technology **Write 251**

Local Networking. A new full-color brochure describes the Altos Computer Systems approach to local and long distance networking as well as mainframe communications (2780/3780, 3270). The 6-pp. fold-out brochure, entitled "Altos—Your Gateway to Communications," describes the Altos-Net software for the networking of Altos 16-bit microcomputers, and software for communications protocols.
Altos Computer Systems **Write 254**



Full-Line Suppliers Offer Advantages



by George Sollman, Vice President, Marketing
Shugart Associates, Sunnyvale, CA

Buying rigid disk drives from a full-line supplier saves OEMs considerable time and money over buying from several one-product companies. We estimate, for example, that it costs an OEM approximately $500,000 to do business with each separate drive vendor. This figure includes such factors as the selection and qualification process, maintenance training and spare parts inventories.

Choosing a full-line supplier offers other advantages as well, including customer-driven marketing, greater depth of marketing, manufacturing and engineering personnel, and the financial strength to develop follow-on products as well as survive an economic downturn.

First, the full-line supplier is customer driven rather than product oriented. This means a company producing 5.25, 8 and 14-inch rigid disk drives is committed to selling you the drive you need instead of the only product in the sample case.

Also, building a good rapport between the respective customer and vendor management staffs is an essential ingredient for a mutually successful OEM business relationship. Such a relationship takes time to establish, and that investment in time is multiplied by the number of vendors utilized. A customer buying drives from two or three different companies must communicate with two or three different sets of engineering, quality assurance, technical support, marketing and executive staffs.

The time spent building a good business relationship is not wasted when dealing with a full-line supplier since customers can purchase products of different size and performance, depending on his different system needs.

Supported by revenues from mature products, a full-line supplier also has the greater financial depth to survive a business slump as well as fund the research and development effort necessary to produce follow-on products. Shugart, for example, will spend more than $20 million in 1982 to develop floppy and rigid disk drive technologies, and future generations of laser-based optical disk drives. This demonstrates a long-term commitment to serving customer needs tomorrow as well as today.

Since buying from a full-line supplier offers numerous time, cost and resource benefits over one-product firms, buyers should consider the company behind the product as well as the product itself when shopping for rigid disk drives.

Another 5¼-Inch Winchester Start-Up Company?

by George Brennan, President
Evotek Corporation, Fremont, CA

There has been a lot of discussion, in the trade press and elsewhere, about the sudden spate of start-up companies entering the disk drive industry. Why, it is asked, do these new-comers think they can be successful in a field where larger, more established companies might more reasonably be expected to succeed?

The thing that separates the small,single-product start-up firms from the diversified established companies is the concept of "strategic focus." Firms like Evotek admittedly have limited focus: bringing to the market what we think is the best 5-¼-inch Winchester disk drive possible. But that focus is total; it occupies 100% of our efforts. We devote all of our resources, both financial and technical, to the successful completion of that project.

Large companies, on the other hand, have competing programs in-house that vie for the finite resources available. And, in addition, new product development has to compete with efforts to improve existing products.

The strategic focus of a start-up company, therefore, often compensates for the size and resources of the larger, more established firm.

Another charge put up to new companies is that — without track record — they are financially weak. What shouldn't be overlooked is that there are venture capitalists with "deep pockets" standing behind these start-ups. That is,the successful start-up is often backed by people with significant financial resources available when problems arise.

If a program still has merit, the knowledgeable venture capitalist won't walk away from it at the first sign of trouble; additional resources will be brought to bear on the problem.

Besides, support from a parent corporation can be pulled away from an in-house program in a large organization, as well. In fact, a smaller organization may have more determination to see a single project through than will a larger company, with a dozen or more competing projects.

Another item for consideration — from the point of view of an OEM — is what criteria should be used in selecting a vendor as a partner? What will separate the few, successful drive manufacturers from the large number of start-ups today?

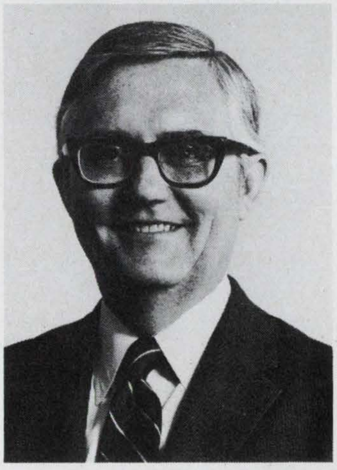
As I see it, success will come to those companies which have the manufacturing capability and skill to build a high-volume, low-cost, reliable peripheral.

The capability of successfully making the transition from an engineering workbench prototype to full-scale production units will be the determining factor in the success of the peripheral manufacturers: whether start-up or established.

In addition to that consideration, an OEM should look for a product family that shows long-term chance of success, plus an organization with the financial resources needed to support the operation.

OEMs who discover these qualities in a vendor will have found for themselves a partner who will be around and be successful in the years ahead.

Atasi: Why Another Disk Drive Company?



by Donald Pate, Vice President, Marketing
ATASI Corp., San Jose, CA

With nearly 40 disk drive companies already competing intensely for sales, we're often asked why Atasi Corp. founders decided to enter this market. People who ask this perhaps are overlooking that the disk drive industry is highly segmented. It is not just one but actually several markets. Consequently, a start-up disk drive company that carefully examines the market and selects a relatively unpopulated niche has excellent chances for success.

Using this approach, Atasi targeted users of high performance 5¼-inch Winchester disk drives, and developed a high capacity, low access time product to meet their special requirements. Among our first products is a 33 Mbyte 30 ms access time disk drive. As a result of this highly focused market approach, Atasi directly competes with only four — not 40 — companies.

Our selection of the high performance 5¼-inch market segment was based on a thorough understanding of the history of the industry. In the early days of μP-based personal and home computers, 5¼-inch Winchester disk drives with storage capacities of 5 Mbytes and access times of 80 to 100 ms were more than adequate to meet users' needs. Recently, though, microcomputer manufacturers have introduced extremely powerful small systems — we call them "supermicrocomputers" — with sophisticated operating systems. These systems are now suitable for applications previously reserved

Viewpoint

for larger systems, but they require greater disk drive capacity and more rapid access to data to support these new applications. Some of these applications now open to smaller, yet powerful systems, are CAD/CAM three dimensional interactive graphics, local area computer networking and voice synthesis.

Atasi's founders knew that just choosing the right market opportunity does not guarantee success. So, the company set some additional objectives designed to position Atasi as a strong contender in its market.

First, we assembled a management team with a nearly unequaled track record in the design, manufacture and marketing of high performance disk drive products.

Second, we designed a product that places technology proven in 8-inch and 14-inch disk drives into a 5¼-inch disk drive, which required a very innovative packaging approach. Atasi's disk drives use a closed-loop servo positioning system instead of the traditional open-loop stepper motor positioning technique found in most 5¼-inch drives. The use of this closed-loop system is the key to Atasi's achievement of *both* high capacity and low access time.

Equally important, even though Atasi is using proven technology in our first products, we are prepared to incorporate new technologies into future products to further increase capacity while maintaining access times well below the industry average. Among these new technologies are run-length-limited (RLL) coding and thin film head/media.

Third, Atasi places great emphasis on manufacturability and reliability in our products, a problem our predecessors frankly have struggled with for some time. Our approach was to consider manufacturability and reliability as design criteria, not a function of production line band-aids or endless testing.

Fourth, Atasi was determined not to announce a product until we were confident we could deliver it soon and on time. Even with this self-imposed restriction, Atasi is the only company shipping high performance 5¼-inch disk drives this year.

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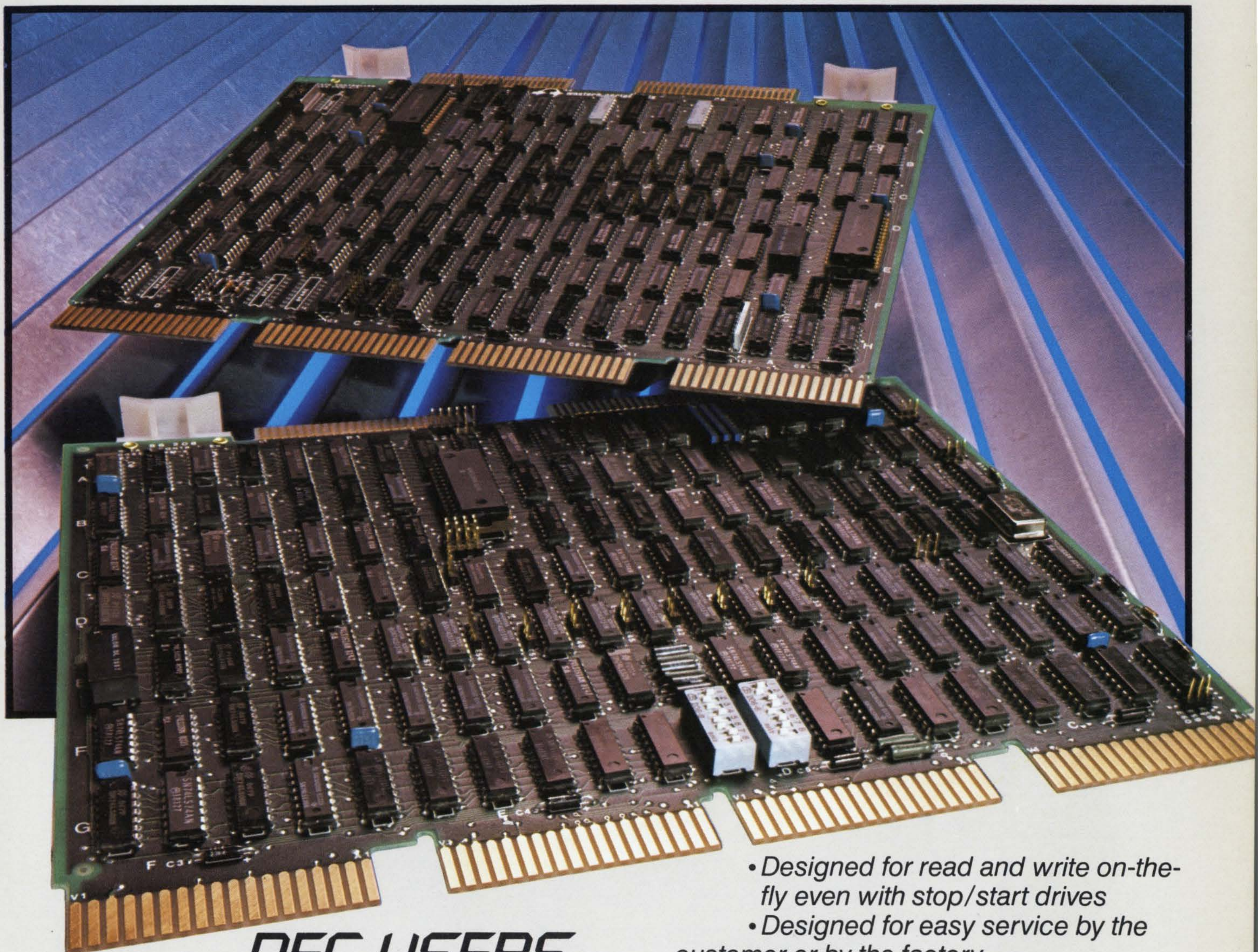

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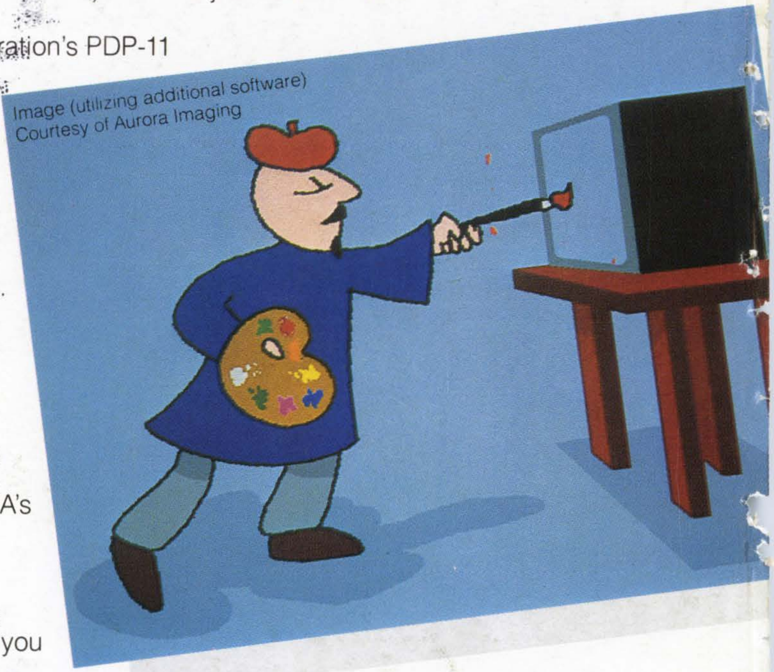
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