VOLUME 10, NO. 12 DECEMBER 1980

Digital Design

Computers • Peripherals • Systems

TECHNOLOGY FORECAST

Minicomputers
Microprocessors & Microcomputers
Microprocessors
MOS RAMs
Bubble Memory Systems
Cartridge Tape Drives
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TWIN DISPLAY is designed to fill the missing link in computerized pre-printing processes. It eliminates time-consuming conventional film stripping and retouching, and allows the operator to utilize digital computer equipment without the usual delays. Full page composition and make-up is quick and easy. Linked to any color scanning device, the basic information containing original art, transparencies and keyline material is the input source for Comtal's Twin Display System. All routine operations are done at a rate faster than traditional studio crafts can achieve. Page assembly is done at the operator's convenience. Color matching and masking by the stylus method gains time of a new order compared to conventional handling, thanks to the exclusive Reference Screen built-in to Comtal's Twin Display. Errors are caught and quickly erased without the "original" being lost. After approval, the completed page is returned to the output scanner unit and converted into film separations or gravure cylinders to suit the particular printing operation required. Comtal's Twin Display is the new dimension in image information providing a display screen showing an exact replica of a finished page without the need for chemical, mechanical or photo-optical procedures.

DIGITAL VIDEO INPUT PROCESSOR by Comtal is a system that digitizes original film imagery as seen on an illuminated light table by a video camera. The DVIP adjusts for variations to provide very high quality digital images on a B&W monitor as an adjunct for the Vision One/20. Its applications include military or telecommunications use as well as non-destructive testing procedures. A further Comtal choice allows transfer of the image to a host computer.

8000-R, a newly redesigned, random real-time peripheral device, provides a superior image when used in conjunction with a data base host or applied to a Vision One/20. Ideal for pipeline processing and color image enhancement, the 8000-R solid state processor is a standard in the industry.

MAPPER, Comtal's interactive spatial warp system, provides point by point image registration under the control of the operator via an interactive procedure. Often applied to Landsat imagery or graphic arts, the Mapper is typically linked to a Vision One/20 and has 6 or 12 degrees of freedom — applicable to a broad range of imaging and cartographic projections. The concept includes simple linear effects that achieve translation, rotation and scaling as well as more advanced warping characteristics of "rubber sheet" distortion such as in second order warp or advanced cubic warp visuals.

COZO (Continuous Zoom) by Comtal gives the convenience of magnification from same size to macro imagery (up to 512 times) as a tool for medical, graphic or industrial fields. Its key features include replication, bi-linear and cubic interpolation, with zoom in steps of .002 magnification.

HIGH RESOLUTION PROCESSOR is special-purpose Comtal hardware used in conjunction with the Twin Display to produce high spatial and color brightness resolution output such as that essential for pre-printing operations. The HRP aids in page make-up allowing interactive composition to be achieved by the operator at relatively high speed.

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Computers • Peripherals • Systems

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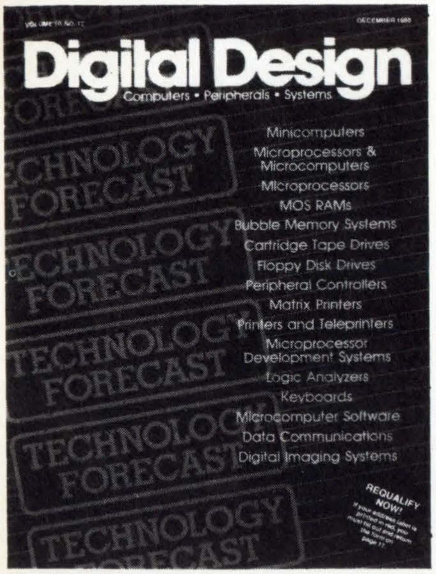

ON OUR COVER

1981 promises even faster technological changes than in 1980. The cost of miscalculation could prove catastrophic. To aid you in making the best possible product and technology choices in 1981, this year's "Technology Forecast" predicts which technologies are likely winners.

Departments

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Letters

Education

Dear Editor:

I read your September editorial on declining U.S. productivity and its impact on the computer industry. You define the problem quite well. But perhaps there is a more fundamental reason why things are going bad in public schools. I strongly suspect that if we were to compare yesterday's to today's schools, many would rate rather low — except for the amount of violence today. I received a good education not because I was exceptional; in those days parents gave more meaning to getting a good education: they emphasized reading and learning over entertainment.

Richard Foy
Redondo Beach, CA

Recursive Programming

Dear Editor:

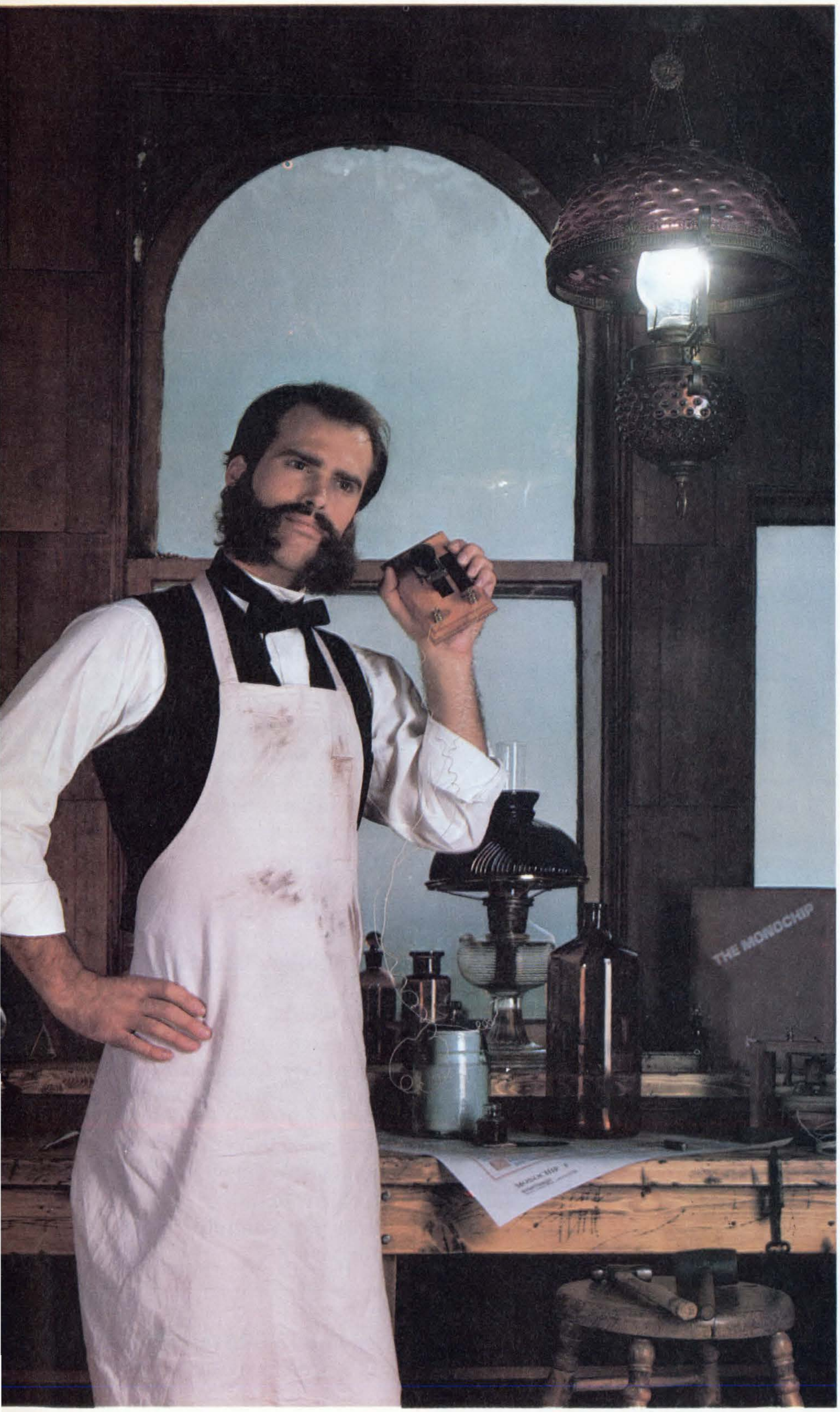
In "Recursive Programming in Basic" (July 1980, pg. 20), Dr. Dershem indicates that a recursive algorithm for N! is a classic example. However, he states that an iterative algorithm is as good. Actually, the optimum organization for computing N! in minimum time, assuming a "data flow computer" with a large number of available arithmetic units, employs a recursion formula, where the HOL expression (DIV means positive integer division with no remainder) is as follows:

```
FACN := FFAC (1,N) WHERE
FFAC (X,Y) := IF X=Y THEN Y
ELSE FFAC (X, (X+Y) DIV 2) *
((X+Y) DIV 2 + 1,Y);
```

FFAC (X,Y) may be viewed as routine or computer organization which recursively calls or replicates itself until a "divide and conquer" type algorithm has been organized to compute N! The attached three part figure is, I hope, self explanatory. It shows 4! reduced to simultaneous multiplication of 4 x 3 and 2 x 1, followed by a final multiplication of the two products. If there are at least N/2 multipliers available, operating in parallel, the recursive approach can, by setting up a "pipelined" or "binary tree" organization, compute

continued on p. 8

With Monochips,™ Alexander Graham Bell might have invented the picture phone.



"Mr. Watson, come here — I want you." With this simple statement telecommunications technology was born.

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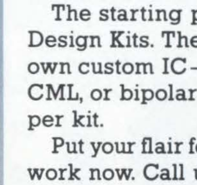

Monochip:™ the semi-custom IC.

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Letters

continued from p. 6

N! in the time to perform $\log_2 N$ multiplies.

Of course, optimizing the time taken for the "computer" to organize itself and the means for doing so are interesting problems that are currently being investigated at various universities and research laboratories.

Edwin M. Drogin
Eaton Corp.
Deer Park, NY

Free To Choose

Dear Editor:

Your September Speakout on the decline of U.S. productivity is timely. Contact over many years with people in several States knowledgeable about our public school system and its schools convinces me that the situation is deplorable. Rather than preparing our young people to solve problems, our public schools cause these problems.

Government must establish and regulate minimal educational standards. With a voucher system, parents will be free to educate their children in a school of their choice. Private schools would increase, competition would develop and the quality of education would improve. Funds could be transferred from a tax base, and directly to the school of one's choice. With the passage of time, survival of the public schools would demand that we elevate our standards. As it is, competition is nonexistent, inadequate standards are deteriorating, and time is running out.

R. A. Gange
P.O. Box 304
Princeton, NJ 08540

Technology Giveaway

Dear Editor:

I strongly object to "giving" our technology to anyone – especially to the Red Chinese (reference pg. 22 in the March issue). Why is IEEE aiding them by helping them to get our electronics and computer technology?

Robert J. Borton
Bridgeport Controls
Horsham, PA

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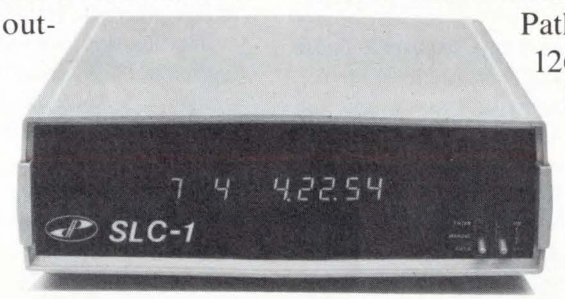


GET INTO THE TIME MACHINE.

DIGITAL PATHWAYS

Circle 64 on Reader Inquiry Card

Paul Snigier, *Editor*

Computers Kill Jobs

A "boomerang effect" is about to spur microcomputer/minicomputer growth. It is a backlash phenomenon not yet noticed by the computer industry. Even among those few economists who first predicted it, it's not recognized as the precursor that will bootstrap U.S. industry and society into a four-day workweek.

From 1976 to 1980, American firms substituted labor for capital: rather than improve productivity with more efficient machinery or computers, U.S. companies preferred to merely increase their work force. To meet increased industrial and consumer demands, the companies increased their labor force and added more shifts. These decisions were often made without deliberation, let alone consideration, of future impact. This was done for several reasons. Much money was being invested in non-productive equipment or products that met environmental, safety and anti-pollution requirements. A slide in net income since the 1969-70 recession, from which (non-computer) corporate profits never really recovered, left less for new equipment. Firms, fearing a recession in 1978-80, were reluctant to allocate too much money for new equipment or for increased plant size. This fear of over-capitalization and expansion extended to high-growth industries, which didn't want to repeat 1974-75. Their fears were groundless.

This all adds up to bad news for the general labor force – but even greater growth than anticipated for our computer industry. With the economy expected to break out of its recessionary turn in 1981, inflation (now about 12.5%) is expected to edge upwards again. However, this time, firms will not follow the 1976-80 scenario of substituting labor for capital. Instead, with improved computer-based systems now available, 1981 economics will dictate that computer-based systems replace more labor functions.

For the computer/electronics industry, for its employees and for its employers, this spells good news; for the unskilled and semi-skilled workers, it spells trouble. What is about to happen has no historical precedent. Most assembly jobs will vanish in eight years. Volvo (to use only one example) says it can design a plant using μP-driven assembly equipment that is run by only 12 people; it replaces 1,200 workers. "Blue collar robots" are about to replace many job functions that don't require too many "smarts". These jobs require less human judgment and exist in clearly definable steps. They'll go first; middle management jobs will go next as computer-based systems take over more decision-making. The impact on office automation and production lines will hit blacks, women and Hispanics very hard. This alone could spawn some tough anti-computer legislation when reformers like Ralph Nader get hold of the computer industry. At all levels, robots and computers offer advantages: they rarely make mistakes, are tireless and faster workers, and don't belong to unions – nor do they file grievances. Computers have already begun to throw workers onto unemployment; the replacement process is subtle, and most firms don't make the process visible.

We must honestly face up to and accept a fact: computers kill jobs. And, jobs created by computers no longer make up for eliminated jobs. Estimates vary, but it's quite possible that by 1986 that 15% of today's workers will be replaced. Perhaps more.

By the way, programmers shouldn't be too smug; they will also become victims – only a bit later. Computer programming jobs will be eliminated in great quantities starting in the late 1980s. Self-programming, user-friendly computers will play their role in this "great extinction" of programmers, as will the shift to fabricating existing mainframe/minicomputer CPUs onto single chips. For example, what IBM recently did with its 370, and as Intel and Motorola are doing, will open up enormous software bases. Tons of low-cost IBM 370 programs exist; they will become accessible to the 32-bit μP users. This will accelerate as "TRS-370", 32-bit desktop computers become available in 1983. This, in turn, will decrease the need for programmers. The massive buildup of libraries and programs will also play its part. The analogy I use is that of U.S. railroad building: there was a limit to how much track was needed; once a certain point was reached, track-laying tapered off. This also occured in U.S. highway building in the 1950s and 1960s.

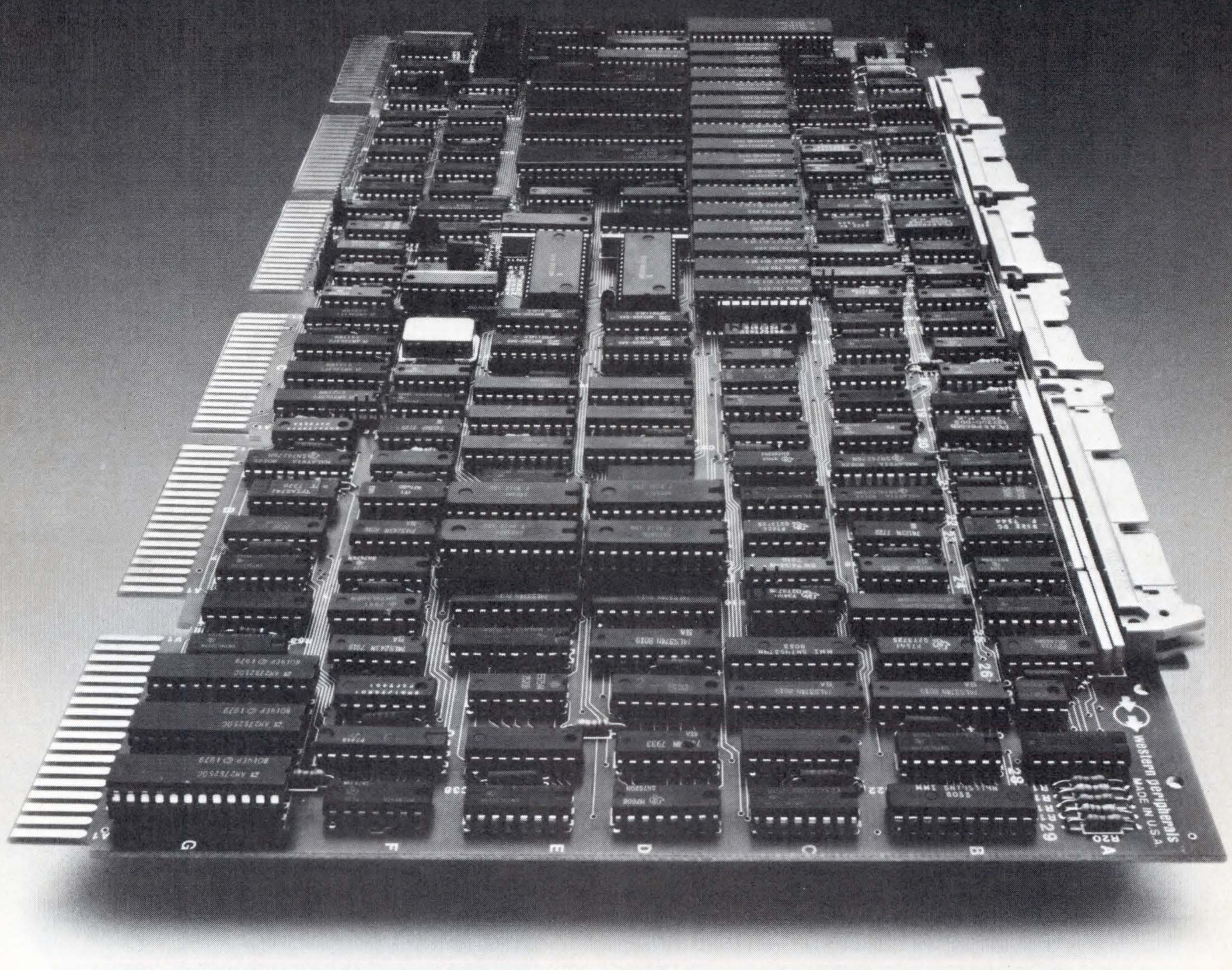
Nothing can stop the revolution. In Europe, trade unions are trying to limit computers; some have formed groups. All such attempts are doomed. If any nation bans imports or creates barriers against more efficient nations, the less-efficient nation will suffer a lowered standard of living. The British motorbike industry is a good example. It fell victim to the more productive Japanese bike industry, which then proceeded to destroy the British industry by using superior technology and assembly plants. The Japanese, it might be noted, were pioneers in applying robots.

But we must not haphazardly remove workers and deposit them onto swelling unemployment and welfare rolls. If handled this way, the dangerous social situation that will emerge will create public outrage and a political backlash that could hinder our computer industry. Just as environmental regulations have strangled other industries, Federal regulations will be written and enforced to slow down the computer industry. These anti-computer regulations will come unless we take action now.

Rather than act when the deteriorating situation has antagonized U.S. society and labor unions, we must educate our leading lawmakers. What we need *now* are "early warnings" for workers whose jobs are in jeopardy. Some might suggest retraining. It's rubbish. Retraining for what? Jobs are already vanishing. Besides, after investigation and interviews with participants in existing retraining programs, my conclusion is that most retraining is a cruel joke. Retraining is a non-solution. "Work sharing" with four-day workweeks is the only way out of this disaster.

Computers need not be job killers and ruin lives; if we, the IEEE, leading industry leaders and our lawmakers act soon, we may all benefit in the transition. Work sharing is needed, with same-salary, four-day workweeks. The alternative is frightening.

Introducing the DC-231 universal single board SMD disc controller.



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Innovative Design

Smart Servo-Positioning Enhances Micro Winnie

In September, Sam Irwin, founder and ex-president of Sycor, Inc., announced simultaneously the formation of his new company, Irwin International, and his namesake's first product, the Irwin 510 micro-Winchester drive.

Irwin's 5.25″ Winchester boasts a number of impressive features, including:

- 10MB formatted capacity (12.3MB unformatted)
- 25 msec average access time
- integral tape backup
- 12.2 cents per KB price

All of these features result in large part from a single design advancement: replacement of the stepper motor head positioner with a smart servo positioner. This μP-controlled, closed loop servo finds tracks by reading location information *pre-embedded* into the disk. In contrast, conventional stepper motor positioners find tracks mechanically – more slowly and less accurately.

Increased head positioning accuracy means more information can be squeezed onto a disk. With a track density of 900 tracks per inch (tpi) and a recording density of 8000 bits per inch (bpi), Irwin's 5.25″ disk drive actually has a capacity greater than many 8″ Winchesters.

Rapid access times result from the quick, μP-controlled servo arm and the virtual elimination of settling time, since the servo positioner has no seek error. In addition, average latency dropped to 7.5 ms, thanks to a disk rotation speed of 4000 rpm (3600 rpm is standard). This increase in rpm was made possible, once again, by use of high speed servo positioning.

Elimination of the bulky stepper motor gave Irwin designers some wide open spaces to play with inside the 3.25″ × 5.75″ × 8″ industry-standard minifloppy-sized housing. Just enough space, in fact, to incorporate a streaming cartridge tape backup system, which runs off the same motor as the disk spindle.

Like the disk drive, the tape drive achieves high accuracy and capacity from an embedded servo approach. Rather than using off-the-shelf tape cartridges, the drive uses cartridges (3M DC100A or Verbatim TC-150) prerecorded with servo location information, allowing a bit density of 10,000 bpi and a capacity of over 10 MB. This high bit density, along with a 60 inch per second (ips) tape speed, allows the drive to dump or restore 10 MB in only four minutes, all on one cartridge.

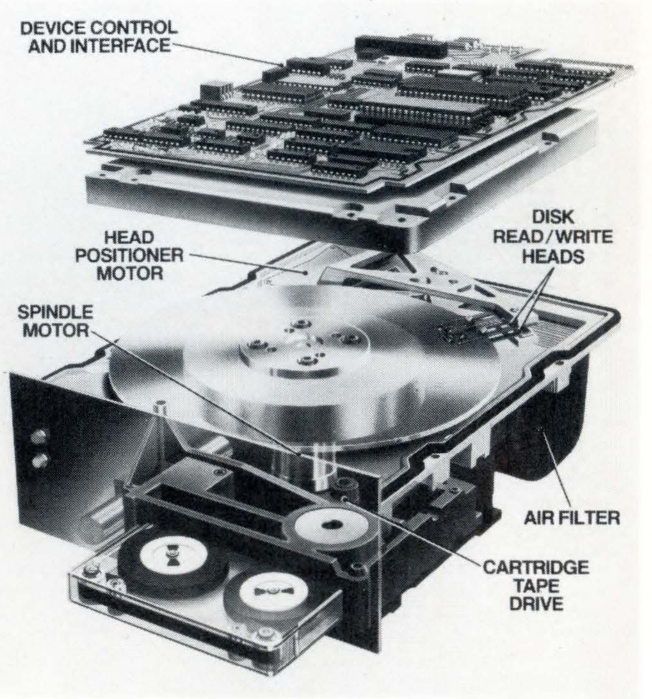
At $1500 each (in quantities of 500), the 510 is considerably more expensive than the other micro-Winnie, Shugart Technology's ST506, even when including minifloppy backup for the 506. But because of Irwin's greater capacity – nearly double Shugart Technology's – their cost per KB remains far lower: 12.2¢ for Irwin, 19.6¢ for Shugart Technology.

Aside from the servo positioner, the 510's key design feature involves regulation of spindle speed. All-effects switching of the DC brushless monodirectional motor regulates both the disk spindle and tape capstan drive speed to 0.1% accuracy. Exactly how this is accomplished Irwin engineers won't even hint at, except to say that it's a controller function.

Irwin International's micro-Winchester is targeted at the growing customer demand for less expensive and more compact storage devices – a market that could reach $500 million within the next three years. The 5.25″ Winchester offers advantages over the 8″ Winchester: it is more compact, less expensive and consumes less power. It will sell well in word processing, POS terminals and small business systems. Unlike the 8″ hard disk drive, where backup uncertainties confused OEM customers, the 5.25″ disk lends itself to the high-capacity minifloppy drives. Product standardization will also produce faster industry acceptance. Mini-Winchesters will provide higher storage capacity to systems that formerly were floppy-based, providing greater data bases with the reliability of a Winchester in the small size of a minifloppy.

Executive vice-president Paul Cochlan says that Irwin will be building 100 units for customer evaluation in January-February 1981, with volume production beginning in May. By the end of 1981, Cochlan expects the company to produce and ship 7500 micro-Winnies.

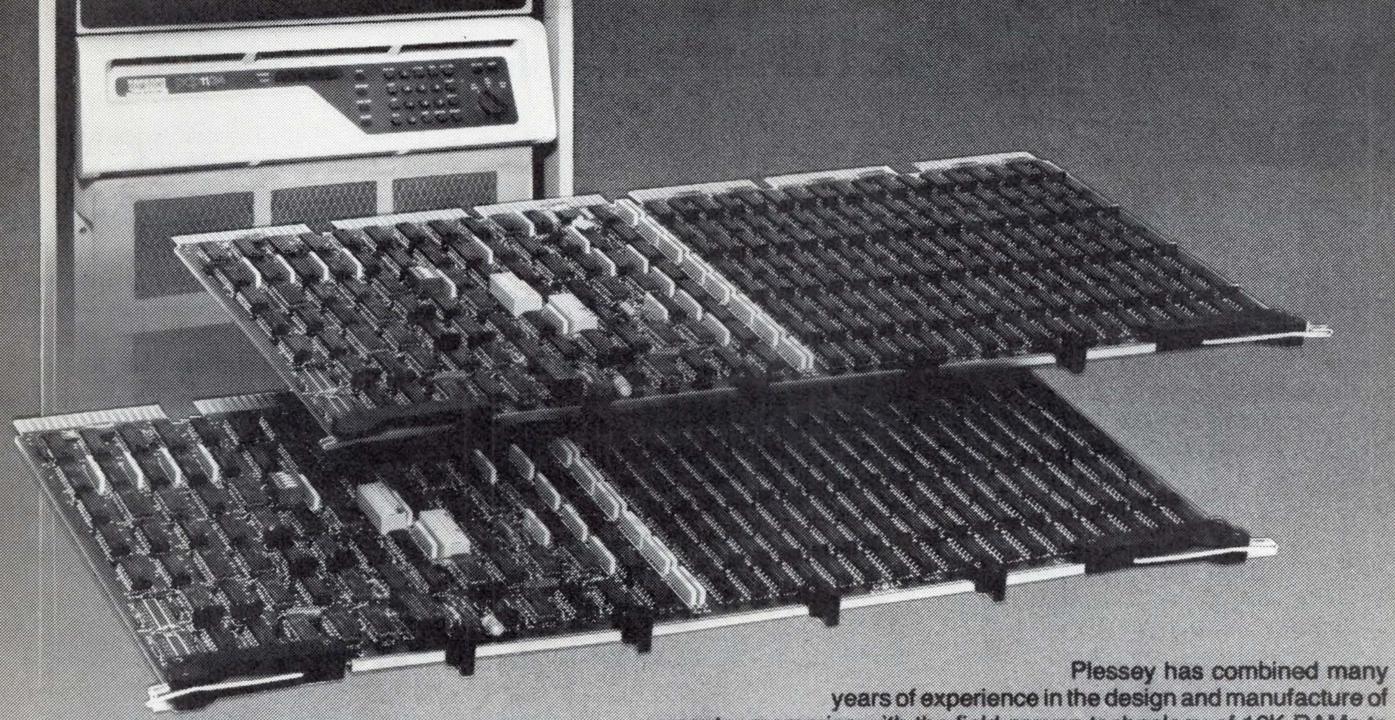
–Bob Hirshon



Exploded view of Irwin International 510 5 1/4″ Micro-Winchester disk drive details unit's component layout.

Plessey's 256 Kbyte Add-In MOS Memories for the PDP-11*

PM-S11L Memory Series



Plessey has combined many years of experience in the design and manufacture of computer memories with the field-proven technology of 16K RAMs to produce the reliable PM-S11L Memory Series for the PDP-11. The SINGLE hex board 256 Kbyte MOS memories are compatible with DEC's* operating systems and diagnostics and are completely hardware, voltage, signal and pin-to-pin compatible with Unibus* backplanes. These memories offer refresh cycling and can be supported by battery backup. All electronic components of the PM-S11L Memory Series are mounted on a stable, rugged base that is reinforced with a metallic brace to ensure safe shipment and ease of installation and maintenance in any systems environment.

Plessey's PM-S11L Series is designed to replace DEC's MS11L. The PM-S11L and PM-S11L/F are available in 256, 192, 128, and 64 Kbyte versions, with or without on-board parity controller. Variable switch settings allow starting and stopping on any 8 Kbyte boundary within the extended addressing range of 0 to 4 Mbytes. LED indicators are included for visual display of parity error.

The PM-S11L has a cycle time of 500ns and read/write (R/W) access time of 385/235ns. Model PM-S11L/F is configured for a cycle time of 425ns and R/W access time of 300/200ns for improved PDP-11 performance.

Plessey's reputation for quality, service, delivery, competitive prices, and worldwide support has made us the largest independent producer of DEC-compatible equipment. All Plessey products withstand strict quality control procedures of the highest commercial standards. Add-in memories are subjected to dynamic "burn-in" at elevated temperature, and inspected for error-free operation in the user's environment via bench tests and computer diagnostic procedures.

Plessey's product line includes add-in/add-on core and semiconductor memories; cartridge, disc pack, floppy, mag tape controllers and subsystems; microcomputer and minicomputer systems; DEC-compatible software; and a wide variety of backplanes, expansion chassis and other accessories. All Plessey products include applicable hardware and software documentation, plus warranty with maintenance/installation options.

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Technology Trends

Will I/O Biochips Create Computer Peripherals Revolution?

Dr. J. R. Barker, *Dept of Physics, U. of Warwick, England*

The *biochip* promises direct and sophisticated interface between the human nervous system and computers. By the mid- to late-1980s, such a chip could revolutionize the computer industry.

Semiconductor technology has brought microelectronics down to the stage where the size of individual transistors on a chip approaches that of large molecules in cellular material. The scale will soon be small enough for us to design circuits capable of organizing themselves into simple forms of artificial intelligence. Coupled with newly-developed techniques for implanting probes in living material, they could minimize the slow and awkward interface barrier now existing between operator and computer. Initially, biochip interfaces would create new market niches – not replace existing peripherals.

Electrode array needed

The idea of implanting electronic systems into living tissue is not new. Several labs are working on microelectronic hearing devices that by-pass a defective inner ear by directly exciting a small part of the nerve bundle forming the auditory nerve. These devices use tiny electrodes, several μm in diameter, which are made by photolithography. Similarly, it is possible to stimulate a precise part of the optic nerve, or visual cortex, to produce bright spots in the field of vision. By adding a microprocessor to a multi-electrode system, it might be possible to pre-process and use them to build up rudimentary images of the visible world. Other work being done includes the electrical stimulation or control of defective neural units in people who are paralyzed in the lower parts of their bodies or down one side. Research of the nervous system, including the brain, has substantially benefited from electronic techniques for exciting and probing.

But all these developments have been severely restricted by the lack of large arrays of ultra-small electrodes and miniature processing systems capable of exciting and probing in a fine mesh over a large enough portion of the neural networks, and of doing so without causing damage. So far, sensors are either too coarse or too few in number to cope with the complexity of individual cells or neural systems.

Although these problems could be overcome by borrowing from the microfabrication techniques used in making silicon chips, there remains the problem of transmitting information from, say, a 100,000-electrode array to the experimenter. Since extensive sorting and pre-processing are necessary, this requires a versatile, high-density μP. Such an "intelligent" implantable sensor for monitoring and controlling is termed a "biochip".

Tissue repair possible?

If advanced medical instrumentation were to be developed along biochip lines, it could significantly improve our knowledge of the electrical signals (and chemical ones, if chemically-sensitive ultra-small devices were used) that govern learning, memory and behavior. From this knowledge, and by reversing the job of a sensing biochip to that of control, it would become possible for neural tissue to be partly repaired. It would be possible to bypass nerves – perhaps even to one day bypass the spine to partially mobilize quadraplegics.

Part of our research program in advanced microelectronics is to study the feasibility of such biochip instrumentation. In collaboration with certain U.S. labs, we are exploring problems with electronic process in ultra-small devices, complex system design and bio-compatible materials important to future biochip technology. The silicon-chip revolution is now reaching a stage where further miniaturization and circuit cleverness will call for extensive changes in the way devices are made, in the design of computer architectures and even in the scientific basis for understanding and exploiting electronic processes.

VLSI spurs novel approaches

Industry is now getting to the end of the LSI era, where, typically, a μP is manufactured as an array of some 64,000 transistors interconnected on a silicon chip about 4 mm^2 in area and sizes of the smallest features are about $2 - 4$ μm. Biochip developments will mean VLSI circuits comprising many millions of components packed onto a single chip. Individual circuit elements as small as 200 A (20 nm or 0.02 μm) will be used. This is about the size of large molecules in cellular matter. Many of the ideas and techniques of bulk solid-state physics which have held for the last three decades of electronics will no longer work on this ultra-small scale.

Conventional computer systems will be difficult to incorporate on VLSI chips because of the very high proportion of interconnect paths, which take up a lot of space. This "wiring" problem is brought about because sequential processing architectures are in use. Parallel or concurrent architectures offer better space-filling pathways but are not as well developed. Choosing the computer architecture to use in the VLSI chips will mean considerable re-thinking of basic computer science; constraints imposed by the economies of design and fabrication of the equivalent electrical circuits will not be the least of the problems to be solved.

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becomes a dominant factor when the size of the silicon approaches the 100-A region, for the electron waves can then escape from the device and may overlap into adjacent devices. This is known as the tunnelling phenomenon. Conduction still goes on, but to understand what is happening requires the full theory of quantum mechanics.

Superlattices give us a good example of the sort of quantum effects which can be exploited in ultra-small systems. In a perfect crystal, the electronic properties of the material are fixed by a periodic array of atomic potentials, which diffract the electron waves as they propagate through the crystal lattice. An artificial 1-D lattice, known as a superlattice, can be superimposed on the crystal lattice by growing alternate layers of various materials on a semiconductor substrate, separated by a few hundred angstroms. By varying the composition and separation of the layers, it is possible to control the electron dynamics in a direction perpendicular to the layers.

Superlattice effects have been demonstrated by a number of laboratories, particularly Dr. Ray Dingle's group at U.S. Bell Telephone Labs. The superlattice proposed by TI's Dr. R. T. Bate could be made by using one of the advanced lithography techniques. Applying a voltage V to the upper aluminium electrode induces a periodic electrical potential at the silicon/silicon-dioxide interface in the vicinity of the buried periodic array of polycrystalline-silicon electrodes. If the electrode spacing d is made comparable to the average electron wavelength at the interface, these electrons see an artificial, periodic lattice superposed on the natural, silicon lattice. By altering V and d, the dynamical properties of electrons flowing between the source and drain electrodes could be drastically altered. *Generalizations of this type of VLSI structure,* in which various voltages are applied over different regions of the buried superlattice, *are of considerable interest in our investigation of co-operative electronic phenomena to do with biochip design.*

Co-operative networks

When the separation between devices approaches molecular size, it is more difficult to isolate any particular device from its neighbors. In a similar way to the superlattice example, overall architecture of the VLSI system of devices may become more important than the host semiconductor in fixing the electrical properties of the array. Unexpected interactions appear between circuit elements. For example, "crosstalk" between memory cells in high-density LSI memory chips is a reliability problem. Exploiting such behavior between devices would create versatile electronic networks which would not need the high proportion of space-consuming wiring patterns that are now used in μPs. The behavior of an orthodox logic system is fixed once the pattern of devices and their interconnecting pathways has been established. A different behavior might be imparted by re-ordering the devices, but this is normally impossible in IC systems. We are studying an alternative approach. We have built theoretical models to simulate arrays of electronic devices which are only partially isolated from each other. The arrays are intended to undergo spontaneous self-organizing, or co-operative transitions between differently- ordered electrical structures.

Information is received at the input in the form of coded electrical signals which are processed and passed to the output as additionally-coded signals. At the lowest input-signal strengths, the array behaves according to the built-in architecture. At some higher level of input signal, cross-interactions between the devices arise through, for example, tunnelling of electrons. Competition between these new channels of communication and the original built-in coupling gives rise to a differently-ordered electrical architecture. The new architecture, and new processing function, is sustained as long as the input signal stays strong enough. This type of system must have a great deal of freedom in coupling between devices, a small number of which control the others, so many parallel paths are necessary.

Co-operative behavior of this kind is termed "synergetic phenomena" for systems comprising many interacting subsystems which are able to reorganize themselves and lock themselves into differently-ordered structures when driven very far from their normal equilibrium.

Preliminary studies are encouraging enough for us to foresee many applications for biochips embodying co-operative VLSI networks. For example, they might be used in self-healing logic arrays that would be capable of repairing a certain amount of radiation damage. They might form the basis of memory systems capable of sorting and relating data, and of "artificial intelligence" units to assist in processes such as pattern recognition.

Implantable electronics

Many problems, to do with the materials used, must be solved before high-intelligence, implantable electronic systems succeed. First, the biochip must be effectively insulated against saline fluids so that it is not penetrated by unwanted dopant ions, such as sodium, which destroy semiconductor devices. The insulating layer, from a few hundred A to several μm thick, must be chemically bonded to the chip as a conventional wrapping is incapable of preventing saline penetration to at least a few μm. Second, the biochip must be compatible with the host biological material, so outer layers must be of chemically inert materials, such as plastics. This poses problems with the interface between the outer, inert layer and relatively active electronic chip layers, which must stick together well enough to prevent unpeeling. Third, electrolysis, which might cause metal micro-electrodes dissolving in electrolytic surroundings when currents flow, poses long-term corrosion problems and make it difficult to obviate toxic by-products. Though a number of new materials show promise, solving the problem of passivating the biochip implants will require greater research efforts.

When the human nervous system can be connected to implanted or external computers in a sophisticated manner, the man-machine interface will take on a new meaning. Bionic chip applications could conceivably alter the computer industry, business world and society.

Color Graphic Display Terminals

Richard A. Pendergrass
Interpretation Systems Inc.

Ask a LANDSAT image analyst why the "standard" full-color composite of orbital MSS (multispectral scanner) data always incorporates bands 4, 5 and 7. He will answer, with a tolerant smile, that it is because only three primary colors are used in digital image processing systems, as in many photographic processing techniques.

It is not an uncommon or unreasonable answer. But it is not an unreasonable question, either. Since LANDSAT data consist of four, rather than three, MSS bands, shouldn't it be expected that the information contained in all four bands will be of some use to the analyst?

Of course. But LANDSAT data certainly isn't the only type of imagery seemingly limited by the three-color industry standards for electronic processing and display systems. Other types of satellite imagery incorporate more than three bands. Certain types of image processing tasks begin with four or more original image arrays, either multispectral, multitemporal or multisensor.

Some digital image analysis and processing techniques allow for this multiplicity of arrays, but still limit display and processing parameters to the three primary colors, simply adding quantities of refresh memory to accommodate the increased data load.

It is demonstrable, however, that the primary colors used in most raster scan display systems – red, green and blue (RGB) – still can be used to drive the three guns of an ordinary color CRT, but be incorporated merely as a display subfunction, not as a data processing dictate. One must first abandon the notion that linear encoding of digital data for raster scan color display is necessary because of technological limitations of CRTs.

These parameters are labeled intensity, hue and saturation (IHS). Incorporating IHS as descriptive measures, the human eye/brain combination can place any object or point of light within a three-dimensional coordinate system encompassing visual perception space **(Fig 2)**. If this model of perception space can be numerically partitioned, so that the cylinder represents a grid of X, Y and Z axes of given value ranges, then any combination of intensity, hue and saturation can be placed according to the XYZ coordinates, and be given a corresponding, invariable value. Furthermore, if this perception space can be modeled mathematically and graphically, complete with numerical values for any point within, then a digital image processing system can be designed to incorporate those parameters.

Not only does the resulting display conform to perception space, but it then can be manipulated for enhancement along those same parameters, an absolute requirement for a truly interactive system.

The necessity to combine four or more image displays is one reason, though it may be a technically trivial one, for encoding non-red, green, blue. The main reason for adopting different parameters is that RGB does not define the perception vectors of human vision. It displays a number of objects of varying appearance. To describe the objects, in their relation to one another, the human observer will be forced to describe them in perceptual terms: How bright are they? What hue is each object? How much color does each object contain, or how much white is mixed with the hue of a particular object?

In digital image processing systems, the problem and the solution are more complex. Unlike the analog home TV, digital systems display *information* as pixel arrays, typically 512 pixels wide X 512 rows deep. Each digital pixel represents a certain bit precision, again typically 8 bits for a monochrome display. In the traditional RGB processing system, a "full color" image displays these pixels with 24 bits of precision each – 8 bits for red, 8 bits for green and 8 bits for blue. The resultant display, therefore, represents 256 red levels (8 binary bits = 256), 256 blue levels and 256 green levels, or more than 16 million possible combinations per pixel. Unfortunately, the human eye cannot distinguish 16 million distinct combinations of intesity, hue and saturation. In fact, due to the nature of additive color, most of those 16 million combinations of red, green and blue will be visually redundant, with the effect of degrading the visual information presented because the information is perceptually confusing.

Once such images are separated into distinct, manageable components for processing, an almost unlimited number of options are available to the operator. In this example, not only were the data available as multispectral components, but they were available also as multitemporal components. In an attempt to determine quantitatively and qualitatively the effects of soil treatments on the crops during the month of growth between the photographs, a ratio of the red filter of one date to the red filter of the second date was executed. Ratios also were created between the two dates for the blue and green filters. The resulting ratios were compared, and based on ground truth, the green filter ratio was selected for the greatest apparent amount and range of information. Encoding data into IHS space, the green filter ratio was assigned as 8 bits of color data, with the original (first date) red filter component assigned as the intensity component, displayed as 6 bits of data. Thus the intensity component of the combined image gives the observer spatial reference information, while the color component displays the effects of soil treatments, showing clearly where simulated industrial pollution caused crop stress and where controlled row pairs maintained health growth patterns. In this simple linear combination, a fundamental use of IHS encoding is established.

In a more complex multispectral combination, a fundamental use of IHS encoding is established.

In a more complex multispectral combination of data, a LANDSAT image was easily constructed from the and Bands 6 and 7 in two bandwidths of the infrared spectrum. The resulting composite is visually compatible with

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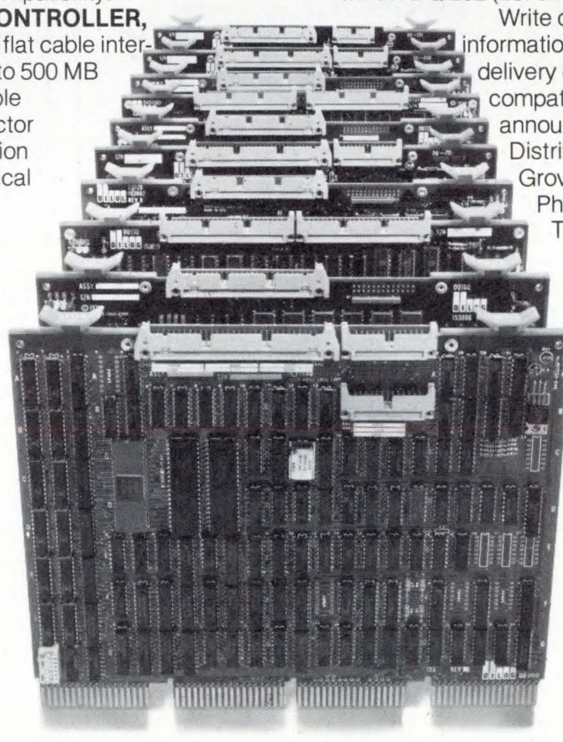

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the standard RGB-combined version, but the data now exists as the three components of intensity, hue and saturation. Since these three data components are independent, it is possible to remove the intensity component, a result of reflectivity normalization of the four images, for further processing, leaving the color components unchanged. In this example, the intensity component was sharpened using a Fourier filter, and recombined linearly with the original color components. The apparent visual resolution is thus greatly enhanced through a manipulation of the data representing reflectivity, while the spectral information remains unaltered.

Since IHS encoding, user-defined processing algorithms and fast computational speed are combined into the same stand-alone system, it becomes obvious that such a system is appropriate for *any* existing image processing and analysis requirements, but also for most conceivable requirements, establishing such a system as a powerful development tool. And since digital imagery is becoming established as the technological state of the art for the 1980s, it is apparent that such a design philosophy will become the standard for the coming decade in fields ranging from remote sensing to medicine, from nondestructive test to meteorology, from microbiology to military surveillance, and from computer graphics to cartography.

IBM Threatens "Giant Killers"

A leader in hardware technology but a stumbling giant in applications software development in that uncomfortable realm of putting its own creations to use. This IBM sterotype is changing. With this change in marketing strategy that is unfolding, IBM has begun to build a software business with the same seriousness it used to attack the stored program, computer industry just two decades ago.

With heftier profits going to the software side, IBM is not about to give it away to the independents. Instead, independents are in for some rough competition in the 1980s. IBM will increasingly use software to generate revenues and profits, which will maintain system differentiation, beat competitors, absorb dp hardware power, create new communications standards, re-enter the transaction-related services business and remain the dominant industry giant. IBM also will become more active in the network service field.

The upcoming 32-bit microprocessor will signal a shift in IBM strategy. Since 32-bit micros are ultimately mainframe-killers, expect mainframes to fade from much of the marketplace. Present 32-bit minis, such as Data General's MV/8000 and DEC's VAX, will penetrate commercial markets during the first half of the 1980's, now that the scientific market has more or less saturated. These super minis are now positioned in the market niche occupied by low-end mainframes. These 32-bit minis, in turn, will come under attack from the 32-bit micros by 1985. It's certain that IBM will enter the microcomputer realm by 1983.

Minicomputers

Paul Snigier, *Editor*

Minis will stay ahead of micros and make inroads on mainframe markets – only the definition of what is a mini will undergo radical alteration starting in 1981. Traditional dividing lines between micros and minis and mainframes will erode further in 1982. Some micros today rival minis. Traditionally, the mini is a computer taken to a problem; whereas, mainframes stay in one place and the problems come to them. Minis, being smaller and cost-effective for smaller jobs, are dispersed to applications throughout an installation. They may even extend throughout locations of larger multi-location plants.

Mainframes operate with large amounts of data while "batch processing" programs. Several programs simultaneously loaded are executed portion by portion. All data needed are entered before execution starts. Minis process programs interactively, with data entering from external devices or computers, terminals or data-acquisition systems. The mini can then process the data under severe time constraints. Other 32-bit minis, rather than performing high-speed data transfers, interact with numerous remote data terminals. These terminals exist in centralized manufacturing and control environments. 32-bit minis have adopted techniques that already have been pioneered by mainframe makers. These techniques include cache memories and interleaved main memories (and combinations of these two).

Changing definitions

What is a mini? The definitions are changing. A small business user doesn't really care whether his computer uses a Z9000 or 32-bit μP, or standard LSI-11-type mini or VAX, or downgraded mainframe from IBM. The computer industry is moving from selling minicomputers to selling solutions.

Will we call a mini a mini, yet call a micro that's far more powerful still a micro? Or, upcoming minis that outperform many mainframes, still minis? Already, micros exist that can equal or beat some high-end minis. And, some minis exist that can beat some mainframes. The single-chip IBM 370 is almost here; and by 1983, desktop TRS-370/135 computers will sell for $15,000, with expansion memory under $8,000/MB. A μP interest group, "Group/380", already exists in preparation for the Intel, Motorola and IBM μP product introductions. With tons of free software for the 360, 370, 303X and 4300s available in the public domain, we will soon see emulators for these and other large mainframes put on chips. What does this mean for minis? VAX and MV/8000 minis won't enjoy the long product lifetimes that the PDP-8 and PDP-11 families enjoyed.

As an example of the blurring boundaries is Zilog's Z9000. Virtual memory, first used on the IBM 370 in 1974, is used on the Z9000. This second-generation 16-bit micro allegedly benchmarks one-on-one with the PDP-11/70. With its memory management unit to better implement virtual memory, Z9000-based microcomputers will pose competition to many present minis. These second generation 16-bit μPs will compete against existing 16-bit minis.

Higher profile in 1981

Mini makers were forced into a low profile during the 1970s. Mainframes went into dp application – typically high-visibility applications. Minis were sold to OEMs and went into systems that reduced production costs in the tool control industries and manufacturing industries. The result? Mini makers (DEC, H-P, DG, P-E, etc) also suffered from lower visibility. Now, with mini makers implementing their minis into micros, and selling to the medium and small business market, and also selling 32-bit minis to mainframe users, minis will grow in visibility in machine tool controls, ATE, factory data collection, process controls, design analysis, and dedicated department applications. They will function as network elements in distributed data processing, data communications nets, and serve as business computers in small businesses or banks.

Mainframe/micro makers counterattack

Mainframe makers aren't taking the invasion of their territory by mini makers lying down: they have counterattacked by introducing mainframes that compete in power and price with the new minis. IBM's 4300 series is one example. IBM, incidentally, is becoming more of a communications company and will grow less susceptible to the inroads of mini and micro makers in the mid 1980s.

But, expect IBM to become more aggressive in pricing. IBM's upper management is allegedly upset with IBM's financial performance. This guarantees the prospect of a real war shaping up between the mini makers and IBM. Although IBM will compete more in the communications business, it will also be going head-on with mini makers. 1981 will mark the real transition.

On the other side, mini makers are about to feel the full pressure from micro makers, who are offering 16-bit (and soon 32-bit) word micros for desk-top units. Mini makers accuse the micro makers (with perhaps the exception of TI) of being weak in upward compatibility, with certain manufacturers such as Intel with its 8080 family as being archaic. The 32-bit micros, however, will borrow much from existing 370 applications software. It will become increasingly difficult to distinguish between micros and minis by 1983.

Spearheading the attack against IBM is DEC's flagship

VAX. The recent VAX-11/750 announcements confirm suspicions that the 1980s will be "the VAX decade." DEC's VAX-11/750 offers 256 kB to 2 MB of main memory. It is the first 32-bit mini to use custom LSI gate array chip technology. It is positioned between the VAX-11/780 and PDP-11/70, and fills a niche in price and performance, making it easier for those OEMs and end users seeking to make the jump from 16- to 32-bit minis. Physically, it's one-third the 780's size; price wise, it's 40% of the 780's \$210k to \$225K price tag – at 60% of its performance. The 750 will hurt sales of DG's MV/8000, as well as other 32-bit minis from Prime, H-P and Wang. For 1981, VAX-11/750 won't make more than a dent; by 1982, it should start to eat at the top end of the 11/70 market, much like the 11/44 did from the low end. For OEM system integrators, the 11/750 creates more work, since it doesn't support many PDP-11 software products. OEMs won't be running PDP-11 code on the 11/750.

To be sure, there will be other 32-bit minis. Hewlett-Packard's 32-bit mini, the Vision family, will be downward compatible with its 3000 line, which Vision will replace. In late 1981, DEC should unveil its Nebula, a 32-bit VLSI μC LSI-11/780, with the full VAX-11/780 architecture running at one-third the mini's speed. DEC's upcoming "Super VAX," termed Nova, will beat the existing VAX-11/780 and provide twice its speed for high-end users. This will enroach further into mainframe territory. Data General is not sitting by idle, and rumors say DG will also unveil a 32-bit machine above its MV/8000.

Software improves

Sophisticated software, previously available for mainframes only, is now available on minis. The independent software houses transported software down to minis. The 1980s, however, will see a maturing in which the mini makers will custom tailor DBM systems specifically for their interactive minis. To take the load off programmers, mini makers will offer improved query and report writer utilities to enable unknowledgeable end-users and executives to query the data base – all with minimal training. Developments will concentrate on code reduction and improved code-generation utility. Programmers are too often wasted on mundane activities; in the 1980s, they will be used more efficiently on development and maintenance, thus improving programmer productivity. The combination of computer-illiterate end users and the scarcity of programmers will force mini makers to "humanize" their minicomputers with English structure languages that enable end users to make simple information requests – without becoming programmers. The end users have the money to buy the computers, and they're not about to learn programming.

Another sign of this "coming of age" is the upward compatibility of mini systems; as users upgrade, their investment in applications software, which is taking a larger bite out of the total systems cost, will be (hopefully, but not always) protected better.

Reliability improves

To minimize downtime, mini makers are taking innovative approaches. DG in its MV/8000 can operate in a degraded or subnormal mode, bypassing its cache memory until repairs are made. The MV/8000 monitors itself, looking for potential troubles, which it immediately flags and then does everything to keep operating (in a degraded mode) after the fault condition occurs. Rather than an "all or nothing" operating mode, the 8000 limps along at degraded levels until repaired – conditions under which other minis would crash. The purchasers of 32-bit minis are commercial organizations that cannot afford downtime. This is a strong selling point.

A subsystem with its OS and I/O is dedicated to maintenance and diagnostics, a procedure pioneered by IBM on its mainframes. The subsystem detects troubles (high temperatures, abnormal power, parity errors); and if serious, notifies the operator, logs in time and nature of event, and may even stop the CPU. With control store in RAM, and loaded each time the 8000 is powered up from a 1.26-MB disk (rather than in PROM), updating microcode is easy. Upon a hardware fault, the subsystem overlays the alterable control store with micro-diagnostic routines or "system maintenance instructions" also stored on diskette. Fault isolation begins by verification of a portion of the hardware and expanding this base. Faults are then isolated within minutes and the field repair unit is replaced and subsystem diagnostics verify the repair. Unlike traditional error checking, which is done only when an address is referenced, the 8000 ECC technique prevents accumulation of single-bit errors than can eventually grow into uncorrectable double-bit errors. DG's "sniffing" technique every two seconds corrects the entire contents of main memory. Intermittents, a particularly annoying problem, are brought out by stressing to failure with power margining; i.e., varying voltage +5% to −10%. If desired, clock speed can be dropped by 20ns; this also stresses intermittents, but also permits operating the 8000 with boards on extenders for diagnostics, and permits the 8000 to operate at a slower speed should a part degrade. In degrade-mode performance, the system bypasses the system cache, instruction cache or address cache.

Add-in/-on growth stronger in 1981

The minicomputer-compatible add-in/-on market, after suffering (partly initiated by IBM's aggressive price-cutting), is recovering. Sales for existing 16-bit minis will remain strong, particularly for DEC-11 compatible equipment. They should begin to taper off by 1982. By then, the 16-bit micros from semi and mini makers will be taking over sales. The overall demand for add-ins/-ons will rise, but the increasing share of market (SOM) will go to the 32-bit minis. DEC minis will take the lion's share.

Rentals/trade-ins to rise

Monthly rental of high-end 32-bit minicomputers could become commonplace in the mid-1980s. Certainly, service for minis (something that was once less than desirable) has improved to the point where it is matching that on the mainframes. With the growth in the minicomputer field, the used-minicomputer market will also grow. End-users wishing to upgrade will trade in their older minis in great numbers. Mini makers will find it lucrative to refurbish and upgrade these older minis and sell them back with a warranty. In the 1970s, the residual value of minis was not that great. This will begin to change in 1981.

Networking to grow

Many systems are using multiple μPs, further removing boundary lines. The development and maintenance and troubleshooting of such systems, however, will present a growing challenge in 1981. Networking will grow in sophistication. Inter-system transfer of data blocks will give way to complete resource sharing. The widespread compliance and acceptance of communication/networking standards will improve inter-system applications software transportability.

Market outlook

Although forcasting is risky, let's make some "guesstimates." We know the mini market expansion is not at maturity and continues to grow at a rate exceeding 15% in the U.S. The commercial side will grow faster than the OEM side. Worldwide mini sales will grow 25% or so (depending upon the industry prognosticator). The most quickly expanding areas include distributed business data processing. DEC, as expected, holds about a quarter of the market; Data General, only less-than-a-tenth, and expected to decline in its share of market (SOM). Honeywell and Hewlett-Packard, both in the DG SOM ballpark percentagewise, will probably increase their SOM in 1981. IBM will also increase its SOM, but DEC will remain unchanged. Expanding areas for mini purchases will fall in small systems. IBM is already the number two mini maker, and only a distant second to DEC. Part of this IBM SOM is due to its small business systems mini sales, where it beats even DEC and HP. As expected, in the OEM and systems market, DEC is the leader by far, beating out HP, Honeywell, IBM and Data General.

What are mini purchasers looking for in 1981? To unsophisticated small business users, reputation of the mini/micro maker are (and will be) the number one criterion. Executives in these businesses have little minicomputer savvy and go by the only criterion that exists for them. IBM and DEC stand to win out on name alone in these markets. The little guys will lose out in the 1980s, since the new and expanding markets for minis (and micros) lie in businesses populated by unsophisticated purchasers. Unlike the late 1970s, where purchasers had the know-how to pick and choose, these purchasers won't do this. The big mini and micro makers will get bigger; the smaller ones will get smaller (in terms of SOM).

For OEMs, as well as users, the implications of switching vendors is today no longer a matter to be taken as lightly as it once was in light of the growing minicomputer and system complexity. For these two reasons, a growing trend to mini vendor loyalty surfaced in 1979-1980; it will expand throughout the 1980s.

These factors will reinforce a trend to purchasing miniperipherals from the system supplier. Sole-sourced purchases will grow. What this means for independent miniperipheral makers will be lost sales; but, for the mini makers, it means added revenue. Mini makers will become more involved in designing and manufacturing peripherals in the 1980s – despite their denials. There is a positive note. With the exception of low-speed serial printers, the miniperipheral market will be so strong that the increased growth may offset any sales lost to the mini makers. The greatest increase in the miniperipherals SOM growth will come in graphic display terminals. Other miniperipheral areas will do well, and the minicomputer makers will want a share of this expanding market. DEC spokesmen were recently careful to say that DEC's decision to manufacture Winchesters was made only because they couldn't find what they wanted on the market; we wonder if mini makers won't jump headlong into competition with independents. As for printers, mainframe makers will get more into this market. Unlike the mainframes, with their 600- to 2000-lpm printers, minicomputer printers operate at 100 to 600 lpm. They also cost less, but are where the sales are now. Independent printer makers should take note: mini growth signals demand for matrix line printers; indeed, IBM got into the market and will expand its activities there. ■

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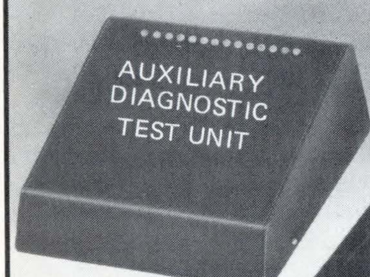

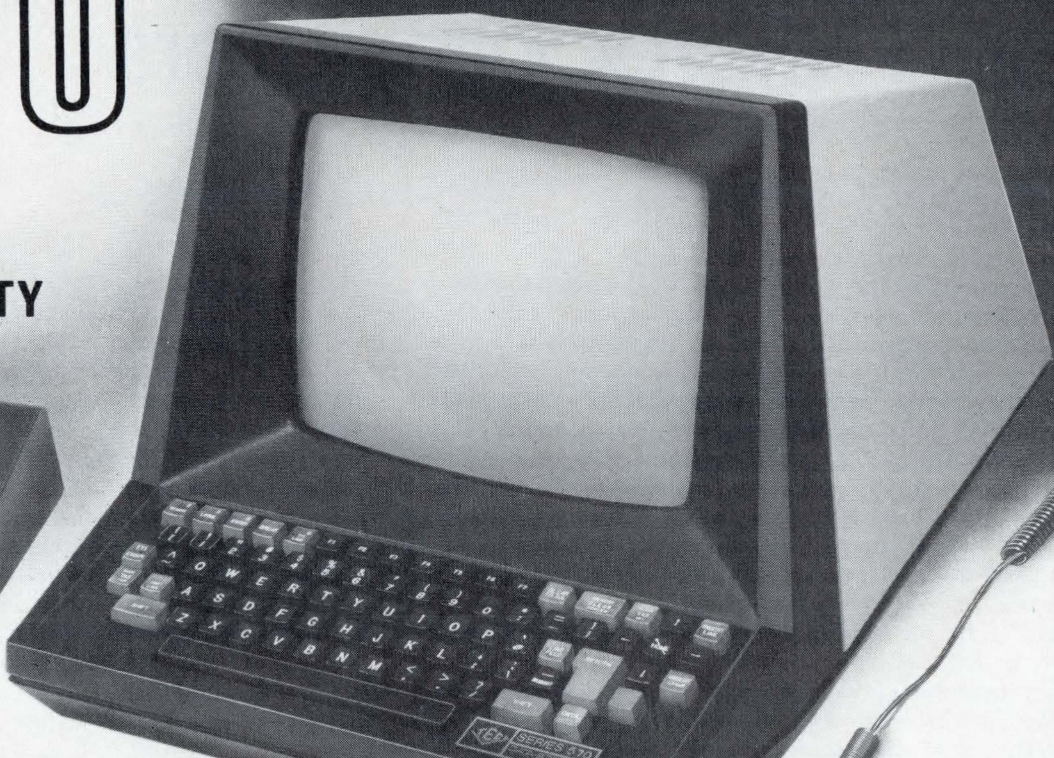

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Microprocessors and Microcomputers

Ian LeMair *Motorola Semiconductor Group, Phoenix, AZ*

The year 1980 has witnessed the rapid acceleration of the use of microprocessors in many applications. These μPs fall into three categories and will be discussed as such in this article. The first category is the microprocessing unit or MPU. The MPU is the "central processing unit" of a multichip system made up of the MPU chip and memory and I/O chips. Typically the MPU has no, or very limited, on-chip memory or I/O. Typically devices that characterize the term MPU are the 6800 and 8085. The second category of microprocessor devices are microcomputing units or MCUs. These devices contain on-chip RAM, ROM or I/O functions. These devices can be either "stand alone"; that is, the total "system" is on the chip, or expandable; where additional memory or I/O is added external to the MCU to enhance the on-chip functions. Typical MCUs are the 6801, 8048 and 3870. The third category of μP device is the μC. This term refers to the board and box products that contain MPUs or MCUs as the processing unit. The term will refer to any or all of these three categories.

In 1980, looking backward to 1974, several generations of MPUs, MCUs and Microcomputers are visible. In that timeframe, microprocessor devices have progressed from very simple controllers, designed for and used as random logic replacement devices, to devices that are viewed as very sophisticated controllers and computer-like devices. The period prior to 1978 was a time of hectic product introductions by semiconductor manufacturers and prototyping of designs based on these new products by the potential users.

During 1978 and 1979 manufacturers of products began delivering in volume quantities, and were at the same time starting to enhance their product offerings to match the requirements of the marketplace. At the same time, the marketplace was more clearly able to express its needs and gained confidence in the semiconductor manufacturer's ability to meet those needs on silicon chips. It was in this timeframe that a new terminology became widespread when referring to microprocessors. Devices were classed as Low Range, Mid Range or High Range devices. The term Low Range corresponded closely to devices with the cost and performance of 4-bit microprocessors while the Mid Range corresponded to the cost and performance of 8-bit microprocessors. The High Range was characterized by 16-bit microprocessor products.

Today in 1980-1981 we have high volume, low cost μPs and μCs associated with consumer oriented applications. These devices are 4- or 8-bit units in instrumentation, process control and other commercial applications. Associated with medium-to-high-volume applications are 8-bit MPUs, MCUs and μCs. These devices range across a wide variety of applications from games to computers. The newest 8-bit MPUs are structured to better support high level languages such as PASCAL, and as such are becoming better suited to computer-like applications. The evolution of μPs now includes 16-bit units that, for all practical purposes, are "minis on a chip". It is with these devices (plus the newer 8-bit devices' that software becomes of major importance. The programs tend to be large and complex in nature and often will require the support of an operating system plus support software such as assemblers, simulators and high level complete with minis for many of the same applications and do so by offering lower cost and modern software capability coupled with innovative architectures.

Microprocessing computing units

During 1980, the trend to MCUs increased with the introduction of many new products. These new product introductions spanned the 4- and 16-bit word lengths and performance ranges previously noted as low, medium and high performance. Examples of these are National's COPS family, Motorola's M6805 family, and Zilog's Z8 products. During 1980 it became obvious that MCUs offer the right amount of ROM, RAM and I/O for the most cost effective solution to many applications. With increasing memory and I/O functions appearing on the chip as well as performance level increases, the MCUs offer significant competition to the traditional multi-chip MPU approach to applications by offering improved cost/performance over the multichip approach.

At the lower-performance market end, the standard approach is to consider the MCU as a function-on-a-chip, and MCU as a non-expandable device and stand-alone unit. As we move up in performance, applications require more flexibility or features and MCUs start offering expandability so that off-chip memory and I/O can be added around the MCU. This is similar to the multichip MPU approach but the package count is reduced by utilizing MCU on-chip features, offering a lower cost approach.

In 1981, the trend to use MCUs, as opposed to MPUs, in new applications will increase as potential users become more familiar with the many MCUs that are available. Also the manufacturers will be moving from the sampling to the production phase on these new devices.

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Microprocessing units

The major emphasis in the introductions of MPUs during 1980 has been on the 16-bit MPUs and their support products such as software, peripheral controllers and development tools.

The emphasis in MPUs in general during 1980 has been on either higher performance (16-bit or high performance 8-bit MPUs such as the Motorola MC6809 or Intel 8088) or lower power (MPUs based on advanced CMOS technologies). Increasing gate density on the chip has aided the evolution to wider word lengths and higher performing MPUs while the environmental and power factors have opened up new opportunities for MPUs (and MCUs) in CMOS. Typical μPs available in CMOS are the RCA 1802, Motorola MC146805, and the National NSC800. It is expected that this trend to CMOS MPUs will continue, since the performance levels of the CMOS devices are compatible to the NMOS devices while offering the added advantage of higher noise immunity, wider operating voltage ranges and lower power consumption.

It must be recognized that most of the demand for the traditional 8-bit MPUs is in products designed prior to 1980. These products in 1981 and beyond will be redesigned or upgraded with either the newer generation 8-bit products, such as MCUs, or 16-bit MPUs, putting more pressure on the semiconductor manufacturers to de-emphasize the 8-bit MPU products in favor of 8-bit MCU products to service the requirements of the 8-bit MPU marketplace. Except for 8-bit MPU products in CMOS, 1981 will see very limited announcements of new 8-bit MPUs, and the 4-bit MPU may disappear completely, a fate that is still several years away for the 8-bit MPU and at least a decade off for the 16-bit MPU.

Microcomputers

During 1980 the 8-bit board families of products were filled out and new 16-bit entries started to appear on the marketplace. While the 8-bit board level products have been around for some time and several defacto bus standards exist for these products, the introduction of the 16-bit units has caused a new cry for bus standardization, as potential 32-bit μP products loom on the horizon. In contrast to what users can count on in MPUs and MCUs, they still can hope that a fairly high degree of standardization may yet occur at the board level. The market during 1980 appeared to move toward some industry-wide bus standards that allowed users to obtain CPU, I/O and memory boards from multiple sources. However, the adoption of standards for 16-bit and 32-bit bus structures is moving slowly and it will be well into 1981 before standards exist for these products. The market forces at work could result in several "standards", such as one for industrial applications, another for computer applications, etc. Use by the commercial/industrial market of μC products is being driven by a rapidly growing class of specialized OEM manufacturers who assemble μP based systems intended for relatively low volume, fast market penetration applications and whose expertise is not in the "board stuffing" business. These value added manufacturers (or systems integrators) have expertise in the applications and/or software for that application. It is this particular marketplace that semiconductor manufacturers and mini houses compete head on for the same application. The advent of the 16-bit MPU as it is applied to μC products will intensify this competition. Many software houses are now making available μP software packages that are very similar to those available from minis. ■

Microprocessors

Bob Greene
Intel Corp., Santa Clara, CA

In the mid 1980s, software implications of the μP will cause us to approach a "crisis" with respect to software development. There are not enough programmers. To successfully avert the impending crisis, designers must use functionally integrated software.

In the same period, software – to allow efficient use of micros – will approach "a crisis level". Many factories will have 10 processors per employee on the floor for automated assembly and robotics. High-speed communications networks will be popular, combined computer and communication systems for communications world wide will be in all-electronic offices and computer mail systems. System requirements are also far more sophisticated. Fault tolerant computing will be a must. Multiprocessing and transparent multiprocessing will come to the forefront. Operating systems will be distributed, network system architectures will be common. Families of programming languages will be required – languages that address specific application problems so that each area or type of problem may be addressed in the most efficient manner. Processing power available will exceed that of the largest computers we have today. Therefore, sophistication of μP usage will exceed the sophistication we have available for our largest computers today! The use of CAD and performance/density of the silicon proved that the hardware is at hand today; the problem is that of generating the application software.

The software crisis

Problems must be overcome to design and use micro systems in the 80s. Software costs will become totally dominant. As application complexity increases, design costs increase drastically. Use of processors and support components, peripherals and tools must address design implementation costs directly or fail in solving the μP crisis. Manufacturing costs continue to rise due to labor, increasing sophistication and larger systems. Integrity and reliability of the system become more important than in the past. Integrity in this context is the guarantee that a fault is not designed into the system. Reliability is the ability to decrease the random failures due to component and/or software malfunctions. Investments required for hardware, and especially for software, will be large and will absolutely demand preservation for the future. No longer will a designer create and ship a product, then completely scrap the design for the next generation and start anew.

Solutions for the eighties

Solutions μP makers will follow are threefold. First, complete solutions will be required. A compatible, wide range of processors must offer performance from the lowest to the highest level. Migration paths among these levels will be changeable depending on the applications requirements. Second, peripheral or I/O support should be extremely broad, extremely well integrated, and compatible with both the processors and available media for mass storage, communications, memories, etc. Third, software will be provided as the basis for the customer system. The system will then be tailored by the customer for specific requirements in terms of management of resources, communication media, protection, and systems structure. Languages will be passed through to the end customer as well as provided for the designer of the application to write the code needed in the base system.

Although assembly programming will survive, most programming will be done with higher level languages. Each type of application (scientific, mathematics oriented, business oriented, etc.,) will be supported with a specific language as well as a system implementation language. This arrangement will allow the designer direct access to his particular computer system with a high degree of efficiency. The languages will be compatible with respect to standards to provide migration among processors. They will also be compatible in output to allow part of the system's software to be written in assembly language, part in system implementation languages, and specific portions in particular applications language. Software costs will dominate system development and long term system usage. Many μC users realize that development of an OEM design is dominated (60-70%) by software; what they fail to realize is that total software cost during development of a new product is only 30% of the total software cost for that product long term. *The remaining 70% is incurred in applications, debug, and maintenance costs after the product has been put into production.*

Because of this extremely high cost of software, preservation of investment in software development is a must. The only way to preserve this investment is to develop a set of standard languages that are both modular and structured. These languages will provide upward mobility to allow compatibility with VLSI (specifically constructed to be compatible with these languages.) Software **must** provide migration from the single module logic replacement of the 70s through multimodule and multiprocess applications of the early 80s, to multiprocessor, multiprocess and distributed processing applications of the 80s. Only modern languages that provide *both structure, modularity and additional advanced programming concepts* will provide these kinds of transitions. Moreover, processors that support these languages will also have specific provisions for the resources that languages themselves require. ■

MOS RAMs

Staff Report
National Semiconductor
Santa Clara, CA

In the past decade an entirely new industry has emerged whose sales have gone from zero to $2.5 billion – unprecedented in the history of the industrial world. During this same period, changes in the marketplace, user and designer sophistication have produced an explosion of applications in appliances, telephones, automobiles, and toys. What do all of these changes mean for the future? Let's take a look at major product areas.

Dynamic RAMs

For several years designers have been holding their breath while a dozen or so manufacturers have kept us posted on their progress in single (5V) power supply 16-k amd 64-k dynamic RAMs. During 1980, both products finally arrived in the marketplace from several manufcturers with the rest of the pack following closely on their heels. As expected, the 16-k single supply devices led the 64-k devices by six months; but both are now available in quantity. At the moment, both products are in their infancy with little availability and few suppliers. Prices therefore, are still high. Cost per bit for a single power supply 16-k device is twice that of 3 power supply devices; while cost per bit for the 64-k device is 2-3 times as high. An economic cross-over with the 3 power supply 16-k device is expected within one year for the single power supply 16-k device and within 2 to 3 years for the 64-k device. With typical design lead-times of a year or more, the system designer is behind schedule if he hasn't already begun designs using these new devices. Even if he is on schedule, he can't forget that the 256 k and 1M dynamic RAM's will be coming along next, at three year intervals.

The layout

Once a designer makes the commitment of using these new 5 volt 16-k and 64-k devices, he has the task of evaluating various devices and suppliers in the marketplace. These devices all look the same, but there are characteristics which are critically important to the designer. Devices differ significantly in die layout and size. Each manufacturer picks a layout that promises to produce the best performing and lowest cost part. Die size is dependent on selected layout and skill of the manufacturers skill in "scaling" this layout to a produceable size.

Alpha particles

Another factor the system designer must face when using modern, high density dynamic RAMs is possible susceptibility to alpha particle errors, (sometimes called soft bit errors). With previous, lower density generations of dynamic RAMs, operating margins were greater.

This was due, in part, to larger memory cell capacitors, higher supply voltages and lower speeds. These factors resulted in larger charges being stored and less opportunity for error. With modern high density devices, operating margins are much narrower because of smaller capacitors, lower supply voltages, and higher speeds. Some of the new designs therefore, become susceptible to "hits" from high energy ionizing radiation (alpha particles) which generally arise from radioactive decay of trace contaminants in the devices' packaging material.

Dynamic RAMs

Several other trends are becoming clear as more manufacturers commit their production to future designs. One such trend is a dynamic RAM with on-chip refresh circuitry-pseudostatic RAM. With all necessary refresh circuitry on the chip capable of refreshing in any one of three or four modes, the designer will be able to treat this part almost as if it were a static RAM. He will achieve the economy and low power consumption of dynamic memory array with the application simplicity of the static RAM. These devices will be available in 8-k×8 and 4-k×8 configurations within the next year. They will be competitive with static RAMs in applications which require byte wide, relatively slow, low cost memory such as intelligent terminals and personal computers.

Beyond the certain trend to pseudostatic devices, other dynamic RAM trends move quickly into the speculative "maybe" category. These trends include on-chip redundancy to inprove device yields, ECC circuitry to eliminate soft bit errors of all kinds, lower supply voltage, and CMOS peripheral circuitry coupled with NMOS memory arrays to provide lower-power, higher-performance devices.

Performance/availability

Performance ranges from fast, high power devices to slower, low power devices. There has been a steady trend toward a lower speed-power. Since speed-power product is one widely-used figure of merit for static RAMs, this indicates that products in the market place have been steadily improving. Recently, many devices have been introduced with a power-down feature which typically reduces power consumption by a factor of 8-10 when the device is deselected.

Where's the Action?

Currently the greatest speed selections and product availability for NMOS and CMOS static RAMs are in 1K×4 and 4K×1 configurations. Also, the CMOS devices are most suited for ultra-low power or battery-baked applications. These advantages, however, must be weighed against current speed and price disadvantages with respect to NMOS devices. Several manufacturers are already involved with NMOS 1 k×8, 2 k×8 and 16 k×1 devices. Availability and suppliers are limited but will improve soon.

In spite of current static RAM evolution into 8-k×1 and 16-k×1 devices, the real trend is toward 8-bit wide or byte-wide (byte-wyde?) static RAMs. The reason for this is the proliferation of μP-based applications which require byte-wide memory systems and limited depth. These applications, ranging from 1-k to 16-k bytes, are ideally suited by cost and speed requirements to the medium speed byte-wide static RAMs in configurations like 1 k×8, 2 k×8, and even 4 k×8. Devices with these configurations are now in the plans at several suppliers.

At the 4 k×8 size, byte-wide static RAMs will become competitive (functionally and economically) with previously described 4 k×8 and 8 k×8 pseudostatic devices. As a result, pseudostatic competition could inhibit development of large, medium speed byte-wide static RAMs beyond 2 k×8 or 4 k×8 configurations. Instead, static RAM development will concentrate on fast bit-wide configurations for improved cache and control store memories.

Design and process technology are currently being pushed by static rather than dynamic RAMs, primarily because of the larger size dynamic RAM storage cell. Die size of a 16 k static RAM memory array is roughly equivalent or slightly greater than that of a 64-k dynamic RAM. Size increases beyond 16 k instatic RAMs will, therefore, be as difficult to achieve as increases beyond 64 k in dynamic RAMs.

EPROMs

Fastest growing segment of today's MOS memory market is the non-volatile memory. For the next five years this market will be primarily served by the ultra-violet-erasable PROM (UV PROM or EPROM for short). A growing segment, however, will be captured by a new product, the electrically-erasable PROM (EEPROM). Today, EEPROMs are widely available in the 2 k×8 configuration, and just this year have become available in 4 k×8 and even 8 k×8 configurations. Supplies and suppliers for these new devices are still very limited.

In addition to these higher density devices, process technology improvements (such as the "arsenic process") have led to faster access times, ranging downward from the standard 450ns to 300ns and even 250 ns. During the next five years densities should increase to 128K and possibly 256K, while access times should increase marginally over the same period as well.

MOS RAMs *continued on p. 96*

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Bubble Memory Systems

Leonard M. Call
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Bubble memory systems are like a three-legged stool: very functional, but you need all parts. With bubble memory systems, the three parts – include the bubble memory device, LSI peripheral circuits and controller.

1980 saw the arrival of the bubble memory system. Few designers would prefer to wrestle directly with a bubble memory device if they can have a simple interface to a controller situation. Ease of use is what will propel bubble memory systems into many applications and insure dynamic growth in 1981 and the years beyond.

Bubble memory systems, in addition to the bubble memory itself, consist of the LSI peripheral circuits and controller. Peripheral circuits are the sense amplifier, operational driver and coil pre-driver and coil drivers. The sense amplifier senses bubble output signals and serializes them for input to the controller. The operational driver generates bubbles, transfers bubbles into the storage area, replicates bubbles in storage for output operations and transfers bubbles out of storage. The coil pre-driver and coil drivers generate triangular current waveforms for rotating magnetic field coils and provide power fail sensing and control.

The controller is the single most complex component in the bubble memory system – it embodies the system's personality. Control functions depend on the architecture of the bubble memory component. Control timings depend on bubble memory gate design.

The controller usually performs system timing and control, bus management, redundant loop management, error correction, address conversion, data security and maintenance aids.

Before specifying, consider the bubble memory's architecture and performance, component parts counts of peripheral circuits, availability of a controller and ease of interfacing.

What's available?

Five manufacturers have bubble memories on the market. Here is a summary:

Texas Instruments • 92-kbit (TIB0203) with 4-ms access time • 512-kbit (TIB0500) with 11.2-ms access time, has boot loop and swap gates introduced in 1979. • 1-Mbit (TIB1000) with 11.2-ms access time, has boot loop and swap gates.

Rockwell International • 256-kbit (RBM256) with 4-ms access time, redundant loop map stored off chip on PROM. • 1-Mbit (RBM411) with 8-ms access time, redundant loop map stored off chip on PROM, introduced in 1980.

Intel Magnetics • 1-Mbit (7110) with 40-ms access time, has boot loop and swap gates introduced in 1979. Controller available.

National Semiconductor • 256-kbit (NBM 2256) with 10-ms access time, has boot loop and swap gates, introduced in 1980.

Fujitsu • 74-kbit (FMB31DB) with 370-ms access time, serial loop device. • 81-kbit (FBM32DB) with 4.5-ms access time, major/minor loop. • 256-kbit (FBM43DA) with 6-ms access time, announced in 1980.

1981 will see new product announcements and entry of Motorola as a bubble memory supplier. We will see: *Texas Instruments* 256-kbit (TIB0250) with 5.6-ms access time, previously announced. *Rockwell International* 1-Mbit (RBM413) with 8-ms access time, boot loop and swap gates. *Intel Magnetics* 1-Mbit (7112) with 20-ms access time, faster version of 7110. *National Semiconductor* 1-Mbit (NBMXXXX) with estimated 10-ms access time. *Motorola* 256K bit (MBM0256) with 4-ms access time, second source of Rockwell RBM256. 1 M bit (MBM1000) with estimated 10-ms access time, boot loop and swap gates. All manufacturers should have full sets of LSI peripheral circuits and controllers available in 1981; controllers will lag.

1980 saw progress in developing applications for bubble memory systems in a number of different areas. They include: numerical machine tool controllers, communications, portable terminals, word processing, POS terminals, voice synthesis, aerospace and defense and other applications. 1980 applications found bubble memory systems not really impacting floppy disks significantly. Fixed head disks retained their immunity, which their lower cost/bit provided. Multimegabyte box-level memory products remain in the future.

Currently prices for bubble memory systems are roughly 100 millicents a bit. Costs should drop by a factor of two every year for bubble memory devices as manufacturers move down the experience curve. Intel Magnetics has advertised price projections for bubble memory systems at just under 60 millicents a bit in mid 1981 and "guaranteed" less than 30 millicents a bit in mid 1982 (in each case, for significant order quantities).

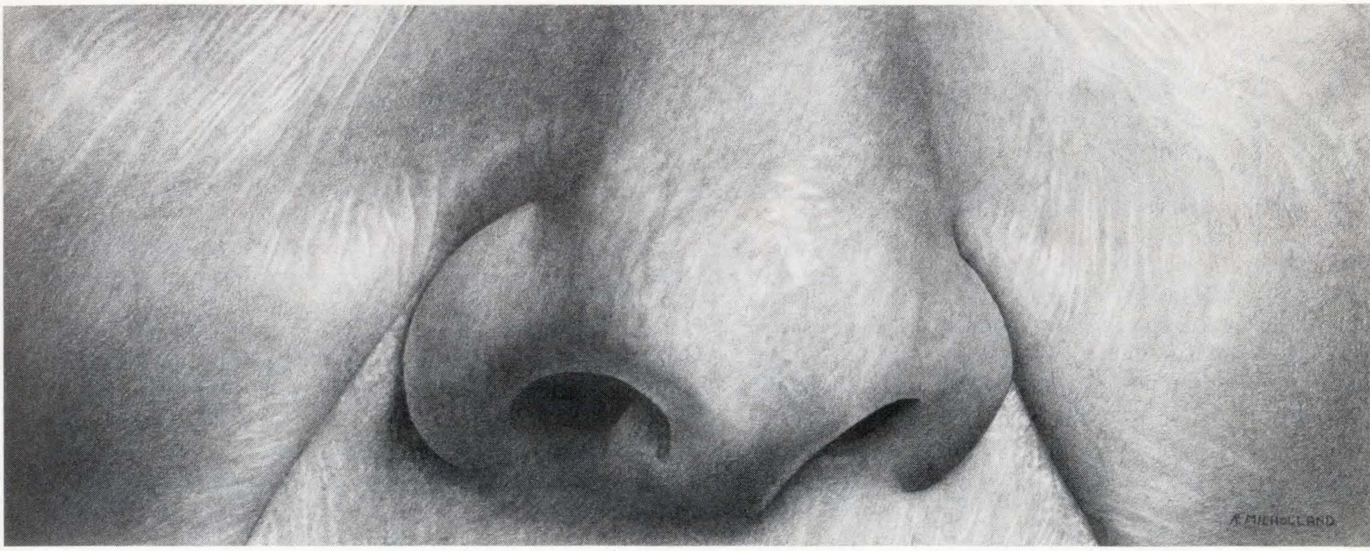
While the 10 millicents a bit price which was widely discussed and forecast a year or more ago continues to elude us, it is coming, but won't be here in 1981. It could arrive in 1983 or sooner if volume usage takes off.

How rapidly are bubble memory systems becoming accepted and applied by electronic systems designers? Available facts seem to indicate that the market is below the expectations of these early years. Lack of LSI support circuits and single chip controllers from most suppliers kept bubble memories from achieving the promised ease of use for many designs. Lower volumes delayed progress down the experience curve and prices have not reached levels projected earlier. Estimates from several sources place total world market shipments of bubble memory systems at about \$20 million in 1980. In November, Venture Development Corp of Wellesley, MA, released a study forecasting market growth from \$18.4 million in 1980 to \$226 million in 1985. Others have spoken publicly of forecasted 1985 volumes which significantly exceed the projection just mentioned. More manufacturers will be in the marketplace – most or all offering a complete set of peripheral circuits, as well as controllers. Prices will drop. 1981 should be the first year of startling growth. ■

Costs Must Be Cut

Bubble memory system users are concerned with costs for bubble memory, peripheral circuits and controllers. There are several factors that influence manufacturing costs. The Gadolinium Gallium Garnet substrate is expensive compared to silicon. In quantity amounts a 3″ GGG wafer with a thin-film EPI layer costs approximately \$300, but under \$20 for a 3″ silicon wafer (also with an EPI layer). In a bubble memory device, substrate cost (GGG plus EPI) dominates; it is greater than wafer fabrication, assembly, packaging or testing. It is 35% of total device cost. Chip size for a 1-Mbit device is usually 400 × 400 mils. Yields are good because: (1) bubble memory architecture with 8-10% redundant minor loops permit meeting specs even with defects which cause some unusable storage loops and (2) there are only two metal masks – the aluminum-copper or copper circuit and permalloy asymmetric chevron layers. Assembly and packaging cost are high because of device operation complexities. The chip must be mounted on a chip carry – resembling a small PC board. Two copper wire coils provide the rotating magnetic field. Permanent magnets top and bottom provide bias field for non-volatility. All must be contained in a molded body inside a metal shield. Testing is costly. Testers are expensive and slow. Testing at device level for a 1-Mbit memory exceeds 1 min. and approaches several minutes – a situation that must be improved. In a bubble memory system, the device is the greatest cost item, and is 40% of system cost with peripheral circuits, controller, bus interface, PCB and system assembly and test comprising remaining system costs. Manufacturers will cut these costs drastically starting in 1981.

Nosey, nosey, nosey.



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Cartridge Tape Drives

William Valliant, *Data Electronics, Inc., San Diego, CA*

A closely-watched computer peripheral of 1980 was the 1/4-in. digital cartridge tape drive. The main application was Winchester-disk back-up. As the low-cost fixed Winchester disk drives started to ramp up their deliveries, the need for fast, reliable, low-cost back-up became obvious. The 1/4-in. cartridge drive was a clear answer for the need. As a result, 1/4-in. digital cartridge tape drive deliveries have increased substantially.

Technology background

Eight years ago, the first 1/4-in. data cartridge was announced. All of the tape drive and guidance mechanics resided in the cartridge. Only a single drive wheel turned to move tape. Development efforts began in several places, applying the new low-cost media to various tape-based applications. Successful applications have shown up in telecommunications, data logging, program loading and fixed-disk back-up.

Inventor of the 1/4-in. cartridge, 3M, was joined by Verbatim (then called ITC) in 1975. The market needed at least two sources for the media to be viable. Initial cartridges held 300 ft. of tape. In 1976, tape capacity increased by 50% with the introduction of the 450-ft. cartridge; This year, cartridges went up to 600 ft.

Disk back-up

While many applications flourish for digital cartridge tape drives, disk back-up promises to be the largest single market. Over 25,000 digital cartridge tape drives went into disk back-up applications during the 1970s – the 1980s will be significantly greater.

To meet the demand for more capacity, disk drives require both an increase in track and linear density. Stepping up the density requires a decrease in the distance between the head and the disk surface (the head must fly closer to the rotating surface). Data reliability demands that the disk be sealed. Such protection prevents ambient dirt from destroying the media or the heads. Since the fixed disk drive still must be loaded and its data removed for most applications, it needs removable-media back-up.

A good choice for back-up is a device that can match the capacity of the disk drive in a single compact package, at a cost that is significantly lower than the cost of the fixed disk drive.

The 1/4-in. data cartridge capacity fulfills these back-up requirements. As seen in **Fig 2**, the drive cost per megabyte has significantly decreased over the past 6 years, allowing cartridge drives to meet the challenge of low-cost large-volume small computer applications. Cartridge-drive cost has essentially tracked the decreasing disk drive cost. In addition, the current back-up cartridge drive is only about half the cost of the disk drive it is backing. This is a key factor to its acceptance.

Interchangeability vs. IBM compatibility

A commonly misused term today is "industry standard media." Literally, this means that the media must be manufactured in accordance with some standard. The 1/4-in. data cartridge has been covered by an ANSI standard for several years. Therefore, it is "industry standard media." Because it must meet this standard, it will be mechanically and magnetically usable in any cartridge drive designed to accept it. To meet the further requirement of transferring data from one drive to another, a recorded standard must be adopted. Two such ANSI standards exist for standard density and work has begun to produce a high-density recorded standard.

IBM-compatibility is another case. Here, the data must be recorded in a prescribed form, so that it can be played back on an IBM system. Cartridge drives do not record data in an IBM-compatible manner as no such standard exists for disk back-up applications.

At times the term "industry standard media" is taken to mean IBM-compatible media. This is not the case for cartridges.

Cartridges continue to gain widening acceptance because they are easy to handle, can accept data from an entire disk onto a single cartridge, can operate unattended, and can allow for file restructuring during the save operation.

1980 saw breakthroughs

In 1980, the conventional number of tracks was increased to 7 and 16, allowing for commensurate increase in capacity. Linear bit density was increased to 7500 and 10,000 bpi. Encoding schemes included group encoding methods for the first time. Stream-

TABLE I

1/4-INCH HIGH DENSITY DIGITAL CARTRIDGE TAPE DRIVES

SUPPLIER MODEL NO.	CAPACITY MBYTES UNFORMATTED	XFR RATE MBYTES/SEC	# TRACKS	LINEAR DEN. BPI	$ COST OEM/1K	*INTERFACE	*TYPE STR/BLK
Kennedy							
640	17.3	24	4	6400	840	Kennedy	Blk
Qantex							
400	17.3	24	4	6400	995/500	DEI-F	Blk
410	110	80	16	7200	1095	Qantex	Str
DEI							
1130/1190	10	29.3/87.9	2	7500	415	DEI-S	Str
1230/1290	20	29.3/87.9	4	7500	525	DEI-S	Str
7130/7190	10	29.3/87.9	2	7500	746	DEI-S	Str
7230/7290	20	29.3/87.9	4	7500	788	DEI-S	Str
Funnel	17.3	24	4	6400	1075	DEI-F	Blk
Archive							
9010	10	87.9	2	7500	823	DEI-S	Str
9020	20	87.9	4	7500	954	DEI-S	Str
IDT							
TDC 3210	10	36	8	6400	NA	IDT	Str
TDC 3220	20	63	8	11,200	NA	IDT	Str
TDC 3164	17.3	24	4	6400	NA	DEI-F	Blk
3M							
HCD-75	67.1	17.5	16	10,000 FRPI	2338	3M	Str
Sintrom/Perex							
HD6400	17.3	24	4	6400	NA	DEI-F	Blk
EPI	17.3	24	4	6400	900/500	EPI	Blk

**DEI-F = Funnel*
DEI-S = Streamer/Streaker (1130-7290)
Str = Streaming
Blk = Blocking

ing drives, allowing for back-up times of 1 min. per 5 MB became available. A range of capacities to match the various system requirements also became available (10, 17, 20, 35 and 67 MB). The 600-ft. cartridge appeared. Controller development continued and numerous firms announced common disk and 1/4-in. cartridge drive controllers for most popular computers. New, efficient servo systems saved system power and reduced local heat generation. Moving head technology included digital positioners and edge-seeking types. Error rates were improved by one and two orders. The extensive use of μPs in drives permitted higher-level interfaces and easier system integration. New tape formats were proposed to take advantage of the streaming technology. The integrated cost met the system designer's objectives at various performance levels.

1981: a boom year

Many companies are now entering the 1/4-in. digital cartridge drive market place. Plug compatible, and/or media compatible positions are being taken by many companies, and the industry should rapidly mature.

Interface standardization will possibly advance through ANSI efforts. (discussion is underway to produce an ANSI tape back-up interface standard.)

While streaming as an optimum disk back-up technology occurred in 1980, the continued existence and high demand for blocking, or start/stop drives, indicate the future will not belong to streamers only. The advantages and general versatility of a start/stop device will attract systems developers.

Further into the future, drive cost and integrated system cost will fall with the development of controller chips and inclusion of more LSI within drives. As drives' cost effectiveness rises, disk markets will benefit in this synergistic tape/disk cost performance improvement.

Contemplating future capacities, a simple analysis of current product features reveals that 115 MB is the upper limit. However, advances in heads (thin film, for example) and media could continue to extend the useful range of the cartridge beyond this limit. Error correction schemes must be used to make these exceedingly large capacities sufficiently reliable.

The 1/4-in. digital cartridge tape drive will continue its prominent place in the system architectures of 1981 and beyond. ■

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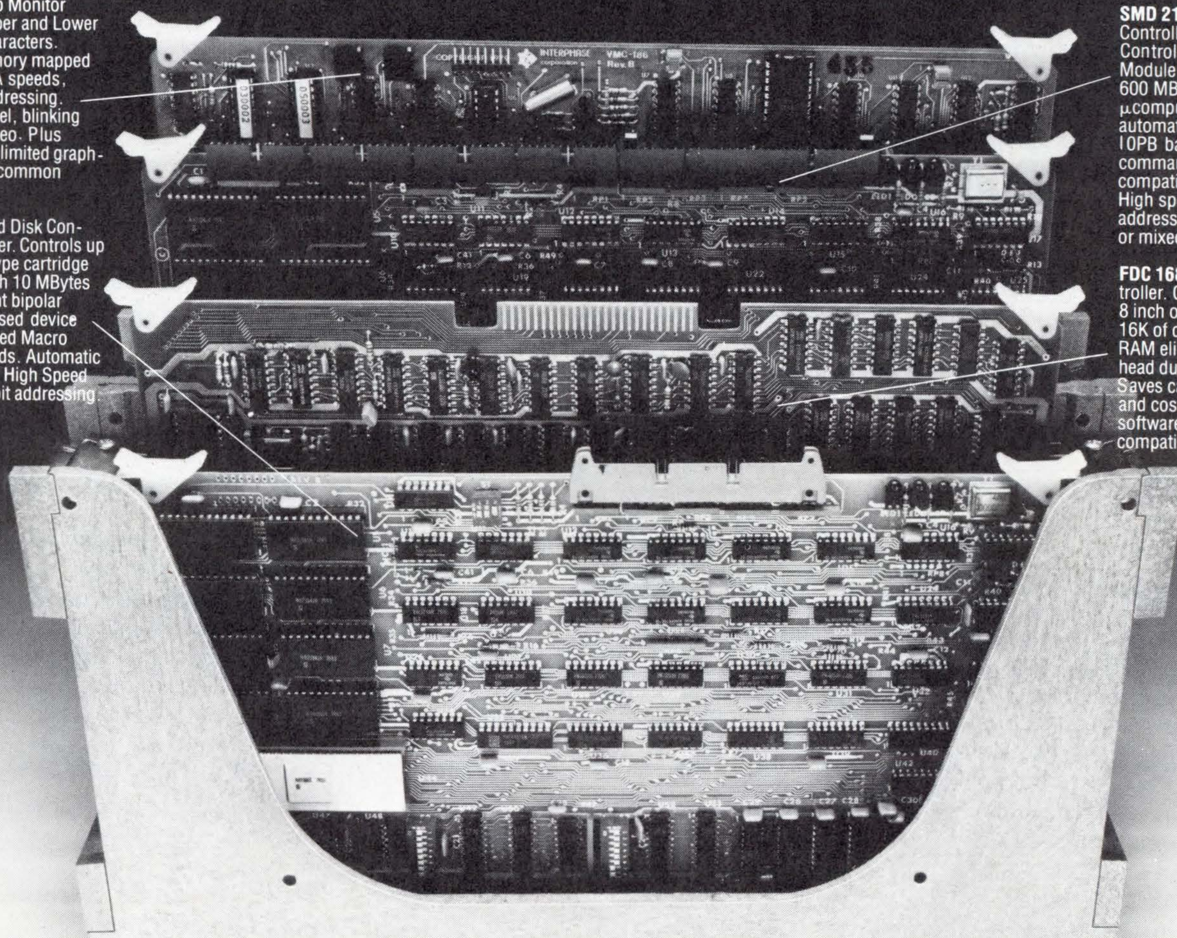

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Floppy Disk Drives

E. Chuck Ouellette
Remex Div.
Ex-Cell-O Corp.

1980 was the year the dual-sided floppy disk came of age technologically. The media wear problem which made the dual-sided floppy disk drive a highly-questionable product in the minds of potential buyers, has been resolved by enough manufacturers to assure product viability. With this solution, the industry has seen the major vendors commit to supply large quantities of dual-sided drives to the marketplace. Large OEM buyers – those who take about 80% of the floppy disk drives produced – are also now committed to dual-head drives. Single-head drives have reached their peak sales, and as vendors begin to supply the dual-sided drives in large quantities, shipments of the single-head drives can be expected to decline sharply and then disappear.

Wear problems solved

Excessive media wear in dual-sided drives was caused by head design problems and too much force during delivery of the head to the point of contact with the media, causing scoring and gouging of the recording surface. Both problems were solved in 1980. Head delivery improved due to carriage/head-moving system refinements. Each mafacturer has its own scheme for better head delivery; these techniques include electrical, mechanical and electromechanical methods to bring the head down flat, without bouncing to avoid scoring or gouging the media.

Subtle but important changes have been made i.. head design. Fine points that were not even considered potential problems two years ago have been recognized as important to media life in the dual-sided environment. Head curvature, materials and the bevel of the edges have all been changed to reflect the industry's greater understanding of head design requirements. Head production techniques and design now yield heads of high quality more consistently. Combined with soft delivery of the heads and improvement in magnetic coating of the media, this has reduced diskette wear significantly.

Not all head delivery systems are created equal, however. The art of head load system design lies in delivering head to media in a controlled way without decreasing overall performance (i.e., increasing head load time, settle time, etc.). Some manufacturers did this successfully – some have not. One which has dealt effectively with this problem uses an electro-mechanical approach that delivers the head to the media very fast, but slows it down just before contact; the head is delivered in a controlled fashion without increasing delivery time or impairing drive performance.

Volume production

Having a viable dual-head design is only half the battle. Vendors must still produce drives cost effectively and in high volume, without reducing product quality. It won't be easy. Dual-head drives made the industry reconsider the floppy disk drive as a manufacturing problem: no longer is it a cheap disk to be produced with low, non-critical tolerances. The floppy is a high-technology electro-mechanical product with tolerances comparable to those of all precision instruments; the ability to produce these devices with prices under $500 for OEMs is a feat.

The addition of the second head added another tolerance dimension. Radial track alignment becomes significant with increased data densities and the isotropic characteristic of media. As a result, preset alignments performed at the factory became highly critical. Also, bit shift which results in data errors is now known as a function of parallelism between the two heads (azimuth). Head compliance, too, is a delicate balance; too much head force results in media wear, while too little produces R/W problems due to lack of head/media compliance. Changes in tolerances in the dual-head design make the relationship between temperature, humidity and alignment highly significant with respect to media. Industry is now aware that floppy disk drives must be treated with the same care as hard disk drives; this understanding is helping to change the way drives are handled in shipment and at the customer site.

For example, it has long been accepted in hard disk handling that, prior to making an alignment, the alignment diskette is inserted and a specified warm up period is allowed so that both device and media reach a stable temperature. This complimentary temperature is important to a correct alignment. Today this same practice is required for floppies; 30 minutes is the usual minimum warm up time. Adherence to warm up parameters will prevent users from misaligning a properly aligned drive or even rejecting a good drive, as has happened in the past. To aid users in understanding these important drive parameters, many manufacturers now supply, as part of documentation, correction factor charts. These correction factors aim to produce drives that will operate reliably within a range of ±30%

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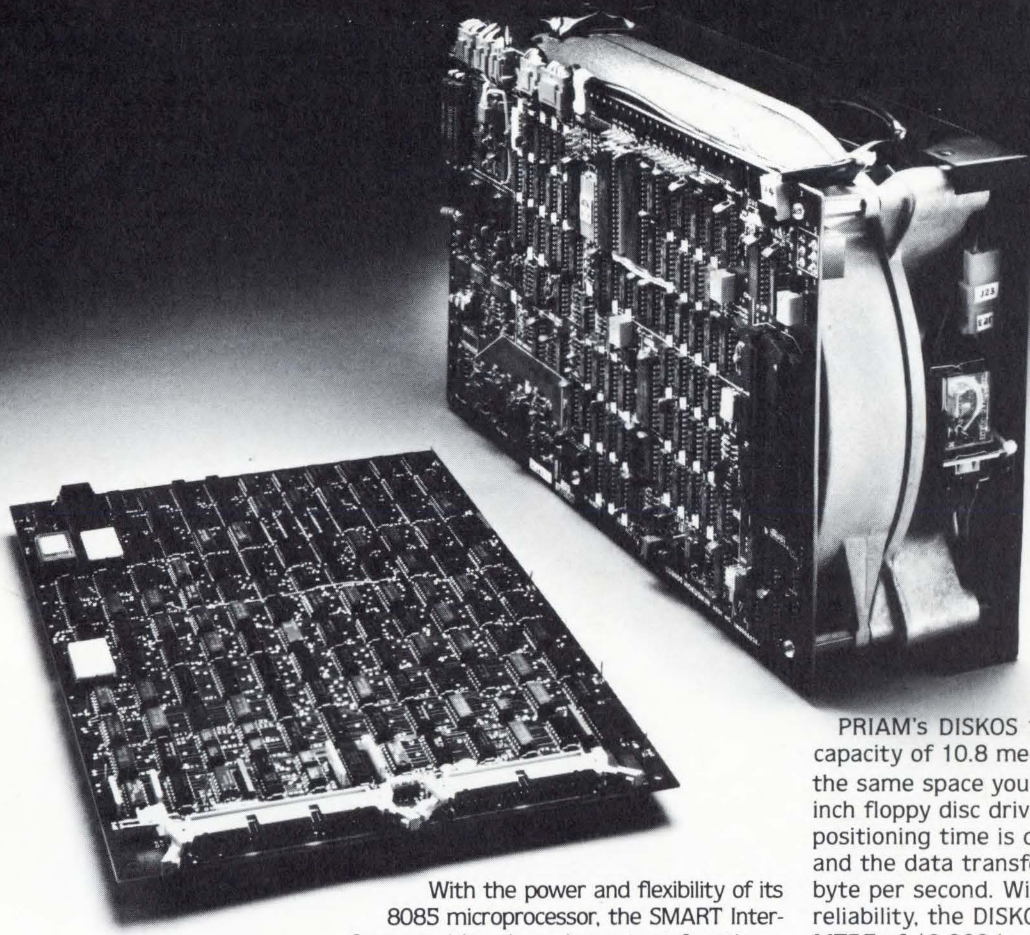

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alignment drift (resulting from the isotropic characteristics of media and other tolerance build-up due to temperature and humidity change).

It may seem strange that these problems have not surfaced until now, considering the long history of floppy disk production and the documentation of these problems in the hard disk industry. However, single-sided drives, which dominated the market in its early years, had much lower tolerances than dual-sided drives, and were much more forgiving of slight misalignment. Also, although these problems were well-understood in hard disk production, transference of this understanding to floppy disk drive manufacturers has been slow.

Manufacturers face numerous internal production challenges beyond those of head alignment and proper handling. The first concern is that quality must not decline with increased volume production. The accepted functional failure rate for units shipped to the field is about 5% to 8%; to compensate for damage that occurs in shipping and handling, vendors are attempting to achieve a 95% yield rate in production.

Maintaining product quality in high-volume production requires skilled personnel. In early floppy disk production, it was thought that skill was needed only at the testing stage. However, since precise alignments have to be performed at almost every work position on the production line, workers assembling the drives must have relatively high skill levels – in excess of what is usually required in PCB production, for example.

Vendors must also include more controls on the production line to maintain consistent quality. Some manufacturers now use in-process inspections that are a scheduled part of the production process. Also, drive suppliers can reduce production errors by using more sophisticated tooling and assembly aids.

All the factors required to maintain product quality in volume production (skilled labor, in-process inspection and additional assembly aids), as well as the fact that some manufacturers require significant retooling to implement their dual head designs, points to yet another factor to be considered in 1981: increasing manufacturing costs. Because of these increased costs, vendor financing is also a vital consideration in determining whether a manufacturer can become a viable supplier to the industry. This, then brings us to the 1981 business decision.

Long-term considerations

In 1981, buyers will care about supplier production capability; in 1982, production capability considerations will continue, but with volume production soaring, price/performance will become the issue. 1982 will also see interest in high data capacities. 1983 should bring a major shake-out. In 1984 and 1985, buyers will shop for suppliers who will provide higher capacities and new technologies.

Future technology

The dual-head floppy disk drive's design problems were largely solved in 1980. Also, 96-tpi drives were introduced in 1980 for acceptance. As yet, the 96-tpi density proved viable only on the 5.25-in. drives, and large scale production of those products will be limited by available head supply and by industry indecision over the relative performance of the band head positioner versus lead screw design.

Eight-in. drives should also achieve higher densities by

FLOPPY DISK DRIVES *continued on p. 96*

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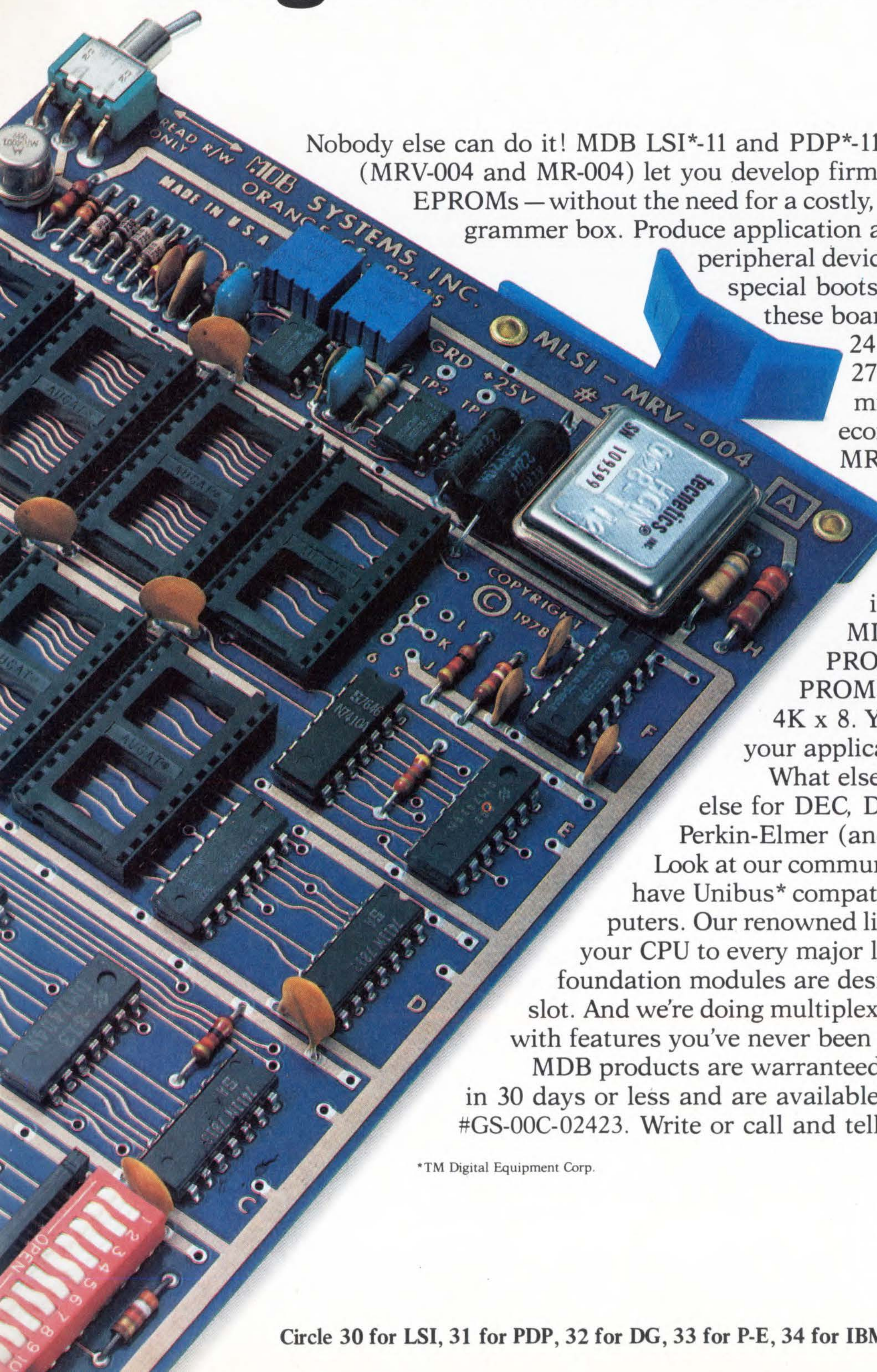

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Peripheral Controllers

Fred B. Cox
Emulex Corp.

Peripheral controller design has undergone significant changes in recent years. Single most significant factor underlying these changes is the widespread application of microprocessor technology. There will be continuing advancements in this area, and the "how" of these advancements will be based on more sophisticated use of intelligence now implanted in controller architecture. The "whats" and "whens" are dependent on several factors and are not yet completely clear. Let's examine the transition of controller designs over the past few years, outline advantages and benefits of most recent technology, and speculate on what direction future controller products may take in 1981 and beyond.

Controller markets

A controller makes physical, logical and electrical connections between a computer I/O facility (bus) and independent peripheral device, such as disk drive, tape transport, line printer, etc. Need for such a device arises from the general-purpose nature of the interfaces the CPU and peripheral manufacturers must, of necessity, build into their products. The controller must, as a minimum, interface to the CPU I/O bus on one side, to the peripheral(s) on the other, and translate the flow of data, control and status signals between the two. What else the controller does depends on factors like software requirements, peripheral complexity, data transfer rates, CPU internal I/O capability, etc.

These factors translate into different controller design requirements, depending on kind of organization involved. They fall into three broad categories: CPU manufacturers, OEMs/users and independent supplier.

Controller implementation

Historically, controllers were implemented with discrete, parallel circuitry performing all data transfer and control functions. For sophisticated peripherals, such as a large capacity system disk, design complexity and circuit element count of the controller can exceed that of the CPU. For example, DEC's RP11E controller, which handles 20 and 40 MByte disk pack drives, occupied a stand-alone 6-foot-high cabinet, complete with blower and supply. Later designs, using more MSI/LSI circuitry, reduced large disk controllers to a group of several circuit boards, some of which are mounted in the CPU (or an expander box) and the rest in the drive cabinet.

Despite such design improvements, controllers by discrete circuitry are specialized and relatively inflexible devices. Extra functions require extra hardware which consumes space and power and adds cost to both controller and system. For installation and maintenance, one must rely on software diagnostics because there is no practical way to perform automatic hardware tests, in a "dumb" controller. Such controllers can seldom handle more than one kind of peripheral without major change or redesign. These limitations arising from discrete circuit implementation are bad enough for the CPU manufacturer and OEM, but they are significantly greater problems for the independent supplier. By clever design, cost can be kept down to make the product price competitive. But software transparency is difficult, if not impossible to achieve in a complex controller. Flexibility is usually achieved by combining a basic general-purpose controller element with specialized adapters for different host CPU's and/or peripherals.

In the mid 1970s, μPs began to appear in several controller designs. The μP-based controller incorporates a basic ALU sequenced by a micro-coded program in a control memory.

For simple, low-performance controllers, MOS technology may be used, but in most controllers, bipolar bit-slice oriented elements are usually required because of performance requirements. These basic elements are supplemented with additional storage (RAM), data buses, and dedicated circuitry to handle specialized functions required in the controller.

In some early designs, the μP was used mainly to perform certain auxiliary functions, such as generating status conditions, with dedicated discrete circuitry used to handle most or all high speed control and data transfer functions. Current designs use the μP to handle most basic functions.

Independent controller suppliers have been more aggressive in using technology than have CPU manufacturers and OEMs. This helps solve the basic set of problems . . . .

1. Packaging. By using sequential, stored logic component count is reduced over a discrete implementation which saves board real estate. The ultimate objective is to reduce

circuitry to fit on one (or few) boards which can be mounted inside the host CPU.

2. Cost. Lower cost is a direct benefit from improved packaging. Use of fewer circuits and boards is a direct cost reduction. Because the controller can be mounted in already available board slots and consume already available power, extra system overhead costs are eliminated.

3. Transparency. By proper microcode design, the controller can emulate a pre-defined architecture. Since complete emulation is a complex task requiring much testing, bugs can be fixed by changing code rather than hardware. This is important where the board density is too high to add more parts because of packaging contraints. Transparency can extend to execution manufacturer-supplied diagnostics as well as functional software, although some designs do not go that far because of cost or other considerations.

4. Flexibility. A programmable device can perform multiple applications much easier than a fixed logic unit. This is more applicable to the peripheral side than the CPU. A wide range of different disk drives can then be supported by one, or perhaps a few, microcode versions. It is also possible to emulate different controller architectures which have been developed for a common CPU I/O structure without changing controller hardware.

5. Extra Features. Any left-over speed and/or program space in the micro-processor can be used to give some extra benefits; usually these will be "optional" or "transparent" to the user if the controller is designed for transparency with existing software. Examples include self test, media formatting, bootstrap, alternate error control and design commonality. These are the important benefits now being realized by controller manufacturers and users. In the area of more sophisticated peripheral controllers, such as for disk and tape, μP design technology began to appear in 1977 in the form of cartridge disk (2314/5440) controllers. The DEC RK11 controller designed for the 5-MB RK05 disk drive, for example, occupies four PCBs, mounted in an auxiliary chassis. Early equivalent controllers supplied by third parties were a little better, but were also configured in about the same package.

6. Self Test. The microprocessor in the peripheral can, and should, be used for extensive testing of the device itself. This function (which cannot be done well by the external controller,) requires no change to existing interface and necessary impact on existing software.

7. Error Control. It should be possible to present an apparent "error-free" medium to the outside world by incorporating error correction, bad block mapping, etc. inside the peripheral. Presumably the peripheral manufacturer would use an optimum strategy for his particular design which would be acceptable to users. Again, this could be done transparently, or at least with minor impact, on existing controllers and/or software.

8. Remote Diagnostics. This is an extension of self testing whereby a remote diagnostic could run via a communication line, with the microprocessor handling communications and testing tasks.

9. Simplified Interface. A simple, parallel data type interface complete with timing and control signals can be provided. This would change the peripheral interface side of the controller, but the controller μP should be readily adaptable to the new, and simpler, interfaces. This possibility has, in fact, been recognized in the proposed ANSI interface standard for 8″disk drives.

Beyond these (and perhaps a few other obvious functions), widespread application of really smart peripherals will depend upon development of system hardware and/or software architectures to make use of them. Given these definitions, the functions to be performed by the controller will follow.

Smart (or intelligent) disk drives incorporate a high degree of μP-based sophistication in the peripheral. The success or failure in promoting this concept into new system designs may give an early indication of the future direction of the "smart peripherals" market.

On the CPU side, manufacturers presently have large investments in hardware and software built around current controller/peripheral designs. Enormous user bases already established will require a long time to make radical changes – at least ones which are not relatively transparent to the user. New concepts are coming; but the timing, considering financial investments and organizational inertias, is unclear. In the meantime, will controllers change much (get any "smarter") in application? There are limits on the controller designer – unless he wants to pioneer a whole new system architecture and develop a lot of new hardware and software to go with his controllers.

The future

The nature of future controller designs depends upon what they are required to do and where they are physically located. In the long term, these definitions depend primarily on what the CPU and peripheral manufacturers (sometimes the same) to to their product architectures and hardware/ software interfaces.

Until 1983-84, most independent peripherals will at least continue to incorporate relatively basic, and hopefully standard, interfaces. If so, the controller definition on the peripheral side will remain unchanged for a while. Large disks, for example, today mainly offer the so-called Pertec standard interface. These standards will probably continue for a few years. The 8″ Winchester disk market is a jungle now, with 20 or more different interfaces. Hopefully ANSI will finalize their standard soon and many manufacturers will at least offer it as an option. Once established, this standard will be followed for many years. To be sure, peripherals either now, or in the future, will incorporate internal μPs for a variety of purposes. This will give the peripheral itself a basic intelligence. The question of how best to use this capability is still open. The following functions make a lot of sense and will probably become commonplace soon:

Combined controllers. Designs have already emerged which combine controller functions for more than one type of peripheral; e.g., tape and disk. These are most applicable to smaller disk and tape capacities but will undoubtedly grow upward in capability and types of peripherals supported.

Network interfaces. Direct peripheral interfaces to various network definitions can be expected as various standards emerge. In these cases, the controllers will handle network protocols rather than interfacing to a CPU bus.

Looking ahead

A few pioneering controller designs are coming which could have major overall impact. Exactly when and what are unclear. New peripheral designs and CPU hardware/software architecture must be developed to take advantage of the inherent capability of external μP-based controllers. Exactly what these changes will be and when they will appear is less clear, although expanded use of the total potential of μP-based controller will be a major factor to future improvements in computer system cost and performance. ■

Matrix Printers

Peter Craig
Printronix, Inc.

It's no secret that 1980 has been a banner year for matrix printers of all categories. Company after company has posted record shipment levels despite an overall economic slowdown. For 1981, we can certainly look forward to continued explosive demand for mini's, micro's and, of course, output devices, (in particular, the ubiquitous versatile matrix printer).

Perhaps the most significant aspect and the greatest benefit of matrix technology, and certainly, the single most dramatic cause of growth for these devices is versatility. As minis and μPs reach all areas and levels and information processing becomes intertwined with corporate and personal lives, we need appropriate output forms. Whether large symbols, small symbols, machine readable, human readable or graphic representation of events and data, the system designer of the '80s must produce meaningful, readily interpreted output. Matrix printing is the only moderate-price and high-performance hard-copy technology that can meet this challenge.

Why will the 1980s be "the decade of matrix printers"? For several reasons. Matrix printers, by virtue of their ability to place a dot anywhere on a page as well as totally "saturate" a page to an all black condition when under computer control, can create virtually any size or shape symbol desired. The system designer is no longer shackled to artificially fixed print output, but has new resources to tailor systems to user applications. In practical terms, this means designers can produce large characters for labels in warehouse applications, readable from 20′ to 30′ away, or can produce small characters compressing a business report to 8-1/2″ × 11″ format. Machine-readable bar codes and human-readable alphanumerics – combined on the same document – can be produced. The designer can reduce tabulated lists of numerical data to charts and graphs, thus enhancing comprehension and increasing user productivity. Graphics capability is not limited to data representation, because applications specialists now produce both forms and data simultaneously by electronically storing a forms image, merging variable data into the form, and single-pass-printing of the composite image. This is desirable in distributed networks where different transactions require uniform forms, and terminals are often unattended. Finally, advances in print quality discussed above have paved the way for matrix printers to establish an entry into WP. Although presently limited to casual WP use on multi-function small business systems, the direction is clear and the evolution to aesthically stylized fonts will greatly expand the role of the matrix printer in offices.

Looking ahead

Superior multi-part copy, outstanding print quality, economic cost of ownership, and solution oriented versatility continue as the major factors in the matrix printer field. Developments will not slow in 1981. We anticipate new milestones in matrix printer evolution for both serial and line printers. Here are our predictions . . . .

First, versatility will continue to expand as greater intelligence is incorporated into the printers, thus providing more functions in terms of alternate dot densities, dynamic speed/print quality trade-offs under software control, down-line font loading, more extensive selftest and diagnostics, and simpler host software.

Second, expect continued refinement in print quality as dot densities increase and multiple-pass, incremental-dot offset capabilities emerge.

Third, acoustic noise, product size, and weight will all be optimized with new products. The installation of terminal units and systems in today's offices demands quieter, esthetically pleasing units.

Fourth, mean time between service calls for both preventive and remedial maintenance will stretch out toward the 1000-hr. mark for aggregate operating hours. Device simplification and improved self test/diagnostic capabilities will facilitate both test and cleaning functions at the operator level. Leading edge, high quality printer manufacturers offer one year warranties on their devices as evidence of enhanced product reliability.

In serial printers, new performance levels will occur in 1981 with the expected introduction of a 400 cps ballistic head printer. Increased differentiation between suppliers will also become evident; e.g., the unsophisticated, low-price, commodity-type units and the highly versatile, high-value units from other suppliers. To the serial printer user, this means alternative sources, with more suppliers selling through more distribution channels than ever before.

For line printers, the user alternatives will also likely increase. More vendors will introduce higher speed products and new levels of price performance will be established at the low speed end of the range. Low-speed matrix line printers will vie for user selection with high-speed serial units in terms of throughput. Meanwhile, the extended durability and tolerance to high duty cycle applications will underscore a key value edge for the line printer. At the 300 lpm level and above, this durability and the versatility of matrix printers will apply increasing pressure on bank printers, and will broaden user acceptance at higher performance levels. IBM's participation and "blessing" of this technology will undoubtably prove to be a major factor in the recognition and growth of application oriented output.

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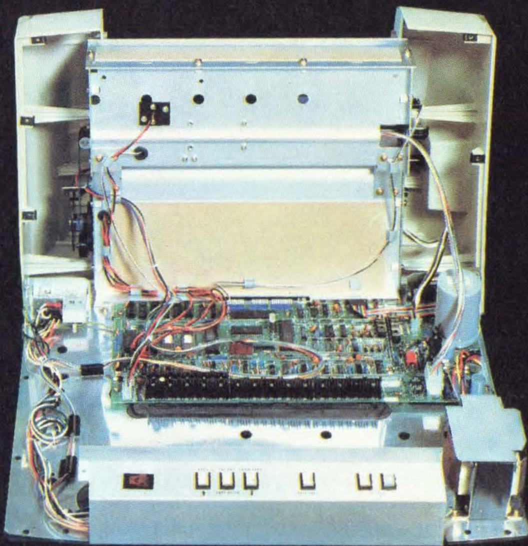

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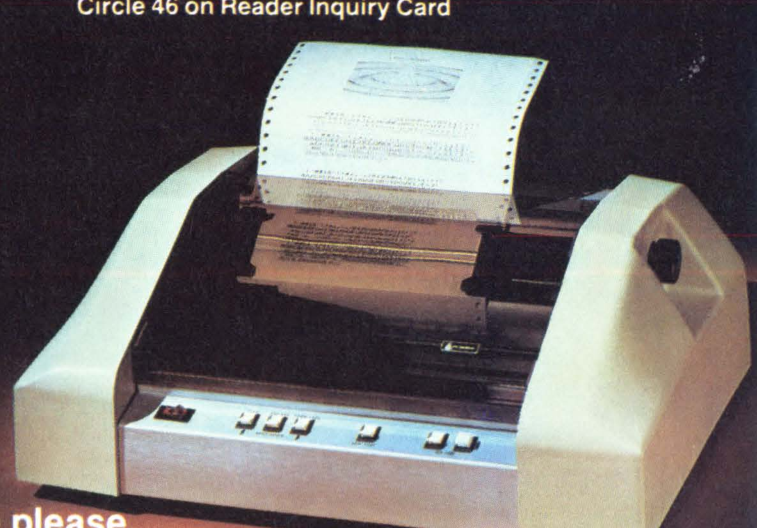

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Printers And Teleprinters

David Glidewell
Mannesmann Tally, Kent, WA

In 1982, total, world wide, non-captive demand for serial matrix RO printers is expected to exceed 300,000 units. The estimated average-annual-growth-rate from 1978 to 1982, by speed class, is 34% for 30-119 cps. 22% for 120-200 cps; and, 71% for over 200cps. Higher print quality is approaching correspondence quality through multipass printing and denser needle arrays. Several vendors have announced products with 12-24 print elements in single head. More entries above 200 cps are expected in 1980-1981 to compete with Dataproducts. Higher reliability (100 million character head life) is now typical; the trend is toward 250+ million characters.

Increased functionality takes full advantage of the inherent ability of matrix to produce multilingual character sets and full graphical images. Products to compete with the IBM 3287 (4-color printer) should appear in 1981. Environmental improvements will come with reduction in size, weight, power and acoustical noise.

As for vendors, the supplier list is long and still growing. Traditionals like, Centronics, Logabax and Mannesmann Tally, are broadening their lines to compete in all performance ranges. Major diversified companies, (DEC, G.E. and T.I.,) have entered the general OEM market. Although the product entrance barriers are relatively low, major computer companies have elected to purchase rather than manufacture (IBM, Dataproducts, Univac, Mannesmann).

Teleprinters

The total, world wide, non-captive market for serial matrix KSR teleprinters is expected to exceed 120,000 units in 1982. The anticipated average-annual-growth-rate from 1978 to 1982, by speed class, is 8.4% for 300/600 baud and 83% for 1200 baud with a 1200 baud-share increase from 13% (1978) to 54% (1982).

Standardization of block mode transmission in data terminal equipment is also expected. Implications of X.25 are being planned as additional non-volatile memory within the terminal, small removable memory and "window into working space memory." RS449/423 adaptation will be planned for as higher transfer rates of packets are used. Integral modems should become available.

The list of suppliers is short but growing. Traditionals, such as Centronics, DEC, G.E., Mannesmann Tally and Teletype, are broadening lines to compete in all ranges. Major diversified companies (Siemens, Texas Instruments) have entered the OEM market. No start up company has yet entered this market.

Serial solid printers

The "daisy wheel" and "thimbles", have supplanted the IBM selectric in WP and "correspondence" quality.

The total, worldwide, non-captive market for serial solid printers is expected to exceed 550,000 units in 1982. The average annual growth rate from 1978 to 1983 will be 25% (Europe higher than U.S.). The trends indicate lower-priced OEM products (sub $1000 in qty at 45 cps, possibly $500 in OEM qty. at 25 cps; improvements to daisy wheel life; more forms handlers.)

Qume leads, with Diablo in second place. NEC and Dataproducts (Plessey acquisition) are present. New products were introduced by Japanese companies at 1980's NCC. Exxon (Qyx Div.) is using daisy wheels in its typewriters. Some vertical integration will occur in 1981 by system manufacturers.

Solid line printers

A shift in product line-speed range to 300-1200 lpm is coming. Most vendors now use μP-based electronics and may add more diagnostics. Expect new product lines before 1982 at higher prices, speeds and with more features. More improvements are expected in the areas of acoustic noise and electrostatic discharge.

Dataproducts has the largest OEM share of solid impact line printers. Data Printer, CDC Centronics and others participate in the OEM market. Technical entrance barriers are high, allowing only large mainframe manufacturers – such as IBM, Univac and Burroughs to produce their own. More licensing is expected between the independents and mainframe houses.

Matrix line printers

Band and matrix printers are price and performance competitive for normal printing functions. Matrix functionality is improving with higher print quality, higher reliability, increased electronics and reduced mechanics. New functions include graphics, color, diagnostics, programmable fonts, etc. Print speed range will shift to 300-900 lpm, with 600 lpm optimum. Expect multiple-speed machines capable of near letter-quality at low speeds as well as normal printing at rated speeds. Environmental improvements will be made in size, weight, power and acoustical noise.

Printers and Teleprinters *continued on p. 94*

μP Development Systems

Bob Hunter, *Tektronix, Beaverton, OR*

1980 was a year mixed with both consolidation and progress for the μP development industry. Previously promised advances, such as 16-bit support, became realities at a pace somewhat slower than anticipated.

In spite of a trend toward multi-user systems, the demand for single-user systems remained strong throughout the year. A single-user system is usually comprised of a CRT terminal, CPU/controller, floppy disk storage, single or multiple emulators and the software necessary for code generation and debugging during hardware/software integration.

This continued demand is traceable to the growing number of manufacturers entering the μP-based product market for the first time. To accommodate the eventual move of these customers into the multi-user realm, one development system manufacturer has announced an entire μP development "family," which allows a user to transport his single-user hardware and software into a multi-user version or a host-oriented version, if desired.

Several factors converged during 1980 to spark a major move toward multi-user development systems. One is the anticipated code volume required for upcoming 16-bit products. Most 8-bit applications have stayed within the 64-k address range directly serviceable by an 8-bit processor. With 16-bit applications, code volumes will quickly leap into the megabyte range. Each software project will demand a modular approach that consumes the full-time output of an entire programming team.

In response to this multi-magnitude jump in software requirements, multi-user systems feature mass storage and sophisticated operating systems to enhance project organization and management. The acceptance of these advanced development tools has been helped by a growing number of computer engineers entering the μC design field, and who are already acclimated to the use of software-oriented design procedures.

Two types of multi-user architectures are offered in today's market but neither is, as yet, dominant. One type is the timeshared CPU approach, (a single CPU, backed by mass storage, services a number of low-cost CRT terminals and integration stations.) The other type is the distributed processing approach, (centralized mass storage services a number of intelligent terminals, each with its own μP development hardware.) The latter approach has two problems yet to be solved. One problem is the high cost of expansion. In effect, a whole new set of development hardware must be supplied to add a new work station. The second problem is in the limitations of processing. Often, such processing does not allow the use of "background" tasks like operation of a line printer, or a compilation, etc.

During the past year, major manufacturers of multi-user systems introduced only a few new products. Instead, they concentrated on the improvement of existing products, or belatedly introduced previously promised models. As software requirements of 16-bit development push the market further into the multi-user camp, this lull will quickly end.

The other major approach to expanding μC software development requirements is the host approach, where μC design tasks are timeshared on a general-purpose computer. This approach uses independently purchased μC software development tools; peripheral hardware/software integration stations handle emulation and debugging. The host solution has continued to gain acceptance because it uses existing computer resources while allowing multiple users and centralized management control. The growth of the host market has continued to stimulate the demand for μC software development packages, including cross-assemblers, compilers, editors and the like. This growth has also quickened the trend toward "unbundled" emulation among major μC development system manufacturers.

Emulation retains its crown

Although software simulation is still offered by several suppliers, emulation is by far the most prevalent means of installing and debugging code into the prototype. ICE uses an emulator processor to exercise code eventually destined for use by an identical or very similar processor, (that will eventually run the prototype.) During emulation, the code is executed under control of debugging software. This function allows the user to observe effects on the

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processor architecture and bus.

The major trend has been toward unbundling ICE. In effect, this means splitting the two major μC design tasks into two separate packages: software development and software/hardware integration. Until recently, most manufacturers supplied tools for both tasks in a single unit, and emulation was accomplished only through control by development system software. Now the μC code can be transferred to a separate system containing the emulators and independent debugging software.

Throughout 1980, there has been a growing demand for unbundled emulation. Part of the push in this direction comes from growth of the host approach to μC development. Since most host systems already have multiple user terminals and adequate mass storage, no additional hardware is needed to support μC software development. However, there is a need for both emulation hardware and debugging software specific to the processor targeted for the prototype. The answer is an emulator system that is linked to the host through an RS-232C connection. This bus allows μC code to be transferred to the emulator system where it can undergo emulation and debugging. There is an added advantage to this approach: no additional timesharing burden is placed on the host computer during debugging operations.

A significant practice observed in 1980 was the continued hesitation to introduce 16-bit real-time emulation. One reason has been delayed chip availability and the "wait and see" attitude concerning the Z8000 and 68000 in relation to the 8086. Another problem has been the technical challenge presented by 16-bit emulation.

A questionable area for ICE is its use in debugging multiprocessor systems, termed "multi-ICE". This method uses two or more emulator processors run simultaneously while connected to their respective processor sockets on the prototype. Multi-ICE is currently accomplished in several ways. One such method emulates a single processor in a multi-processor system while the others run free. Several suppliers currently offer modular emulators that function in a multiple emulator configuration. In some cases, this is a by-product of the development system architecture. In a distributed processing system, for example, each station is capable of independent emulation while several terminals can join to emulate the various processors in the prototype. In other cases, multi-ICE is accomplished through control options to a multiple emulator system. In any case, there is no coordination of trace information presented by the various emulators, and therefore no way to verify that they are interacting properly.

In another approach, the multiple emulators have joint control of the user through a software interface provided by the development system. The user then controls the operation of each emulator and combination of emulators. The development system software can now present a coordinated set of trace information for each emulator. At present, this approach is offered in limited form for no more than two processors. It also creates a very different kind of problem, one involving human interpretations: to trace the parallel interaction of several processors in terms of individual shifts in the working registers. This task becomes extremely difficult because of the sheer volume of information presented to the user.

Real-time prototype analysis is a development system feature that will probably grow more important. Many μP applications continue to be interrupt-driven and dedicated to real-time control functions, where a prototype system must ultimately be debugged at full operating speed. Real-time analysis uses a high-speed trace buffer to capture prototype bus activity and selected hardware status at a breakpoint specified by the user. Data is triggered into the buffer by configuring various combinations of built-in word recognizers and counters.

High level languages move ahead

High level languages for μC development is currently the subject of increased use and interest. Languages such as PASCAL, PLM/X, FORTRAN, MDL/μ, and COBOL have become increasingly available for a wide number of chips. Part of the reason for this accelerated activity in languages is the anticipation of the large code volumes that will be required by 16-bit chips, making μC development more software-intensive than ever. Another factor is the number of technical improvements and modifications that are making such languages more suitable for μC software development.

A good example is PASCAL. As a structured language, it automatically provides modularity that is conducive to a team-oriented software effort. A megabyte-size program can be broken down into modules small enough to be handled by individual programmers and then linked into executable code as a project proceeds. To make PASCAL work at the machine level, a number of enhancements have been added that allow the programmer control of certain operations like interrupts, register access, and I/O. A number of current versions of the language now make allowances for manipulation at the micro level.

In the case of PASCAL, a major breakthrough was the condensation of a PASCAL compiler into a 64-k address space. This is the largest space directly addressable by an 8-bit processor, which is still the language processor in most development systems. Previously, it was necessary to first compile PASCAL source code into psuedo-machine language called P-code, and then use an interpreter to convert the P-code into object code specific to the processor being programmed. Interpreters usually execute at a slower rate than compiled programs, so the move to a PASCAL compiler has had significant impact on μC software development. A similar evolution has occurred with BASIC, including the addition of micro extensions and the development of compilers. Other languages, such as FORTRAN and PL/M have now been adapted for use by nearly all major development system manufacturers.

Assembly language still remains a vital programming tool since it brings the programmer face to face with the particular machine he is coding. This gives him the greatest opportunity to create low-volume, fast-running code. Most assemblers now include macro capability and conditional assembly as standard features. Software development loads have increased, alongside a corresponding rise in concern over the execution times of both assemblers and compilers. Complex programs can eat up several hours of computer time during code conversion, and processing time is a significant factor in programming productivity.

1981 and beyond

Here is the long-term picture for μC development systems. Single-user systems will continue to play a vital role. The demand for multi-user systems will accelerate. Sophisticated logic analysis will become a vital part of μC development systems. ICE will continue to have a place in the μC development picture. The pressure for intersystem communication will continue. Fewer manufacturers will stay in the development system market.

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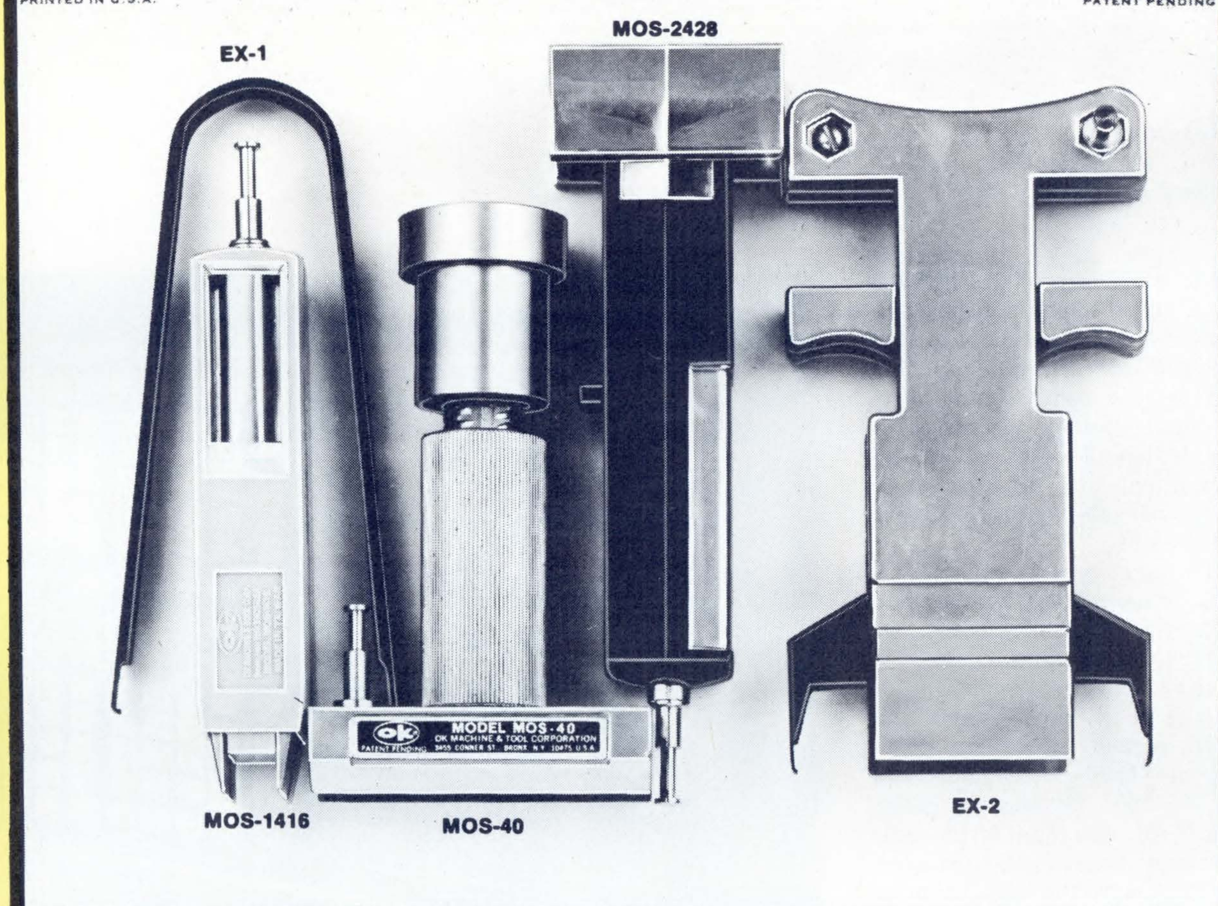

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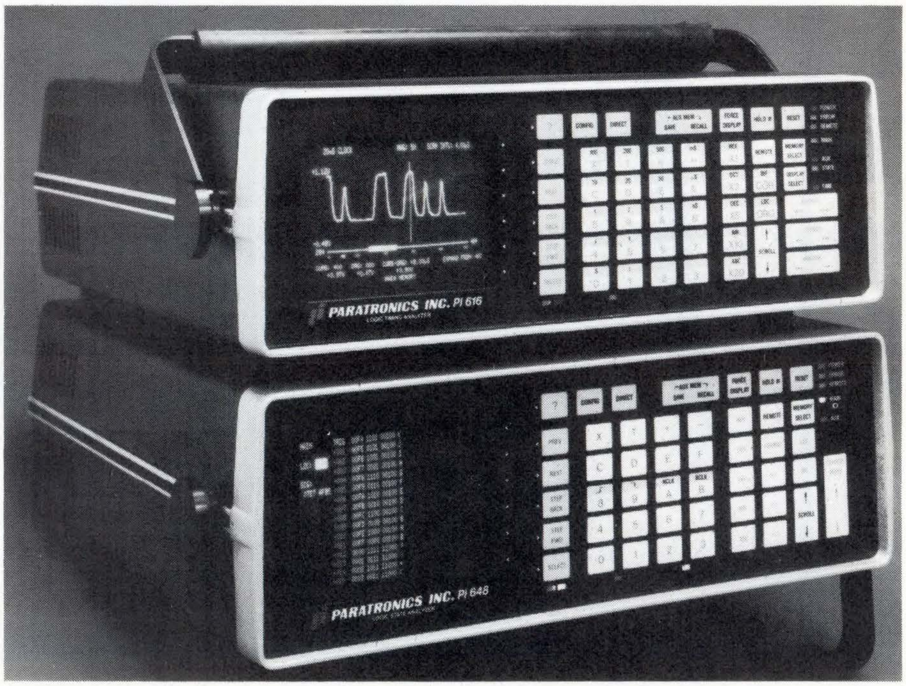
Logic Analyzers

Staff Report
Gould Inc., Biomation Div.,
Santa Clara, CA 95050

New logic analyzer products in 1980 showed both an application diversification and, at the same time, a specialization. The diversification took the form of various manufacturers introducing input probing accessories or probe pods that allowed a general purpose mainframe logic analyzer to be used for a wide range of different analysis applications.

Specialization to a specific task requires many more input channels than conventionally available. Today we have logic analyzers with 32-, 48-, 64- and 96-input channels specifically for the analysis of μP-based systems with wide input capacity slow in maximum clocking rate. They generally don't run beyond 10 MHz because the design constraints for wide input instruments require clever design to keep channel-to-channel skew to a manageable number. Typically, the channel-to-channel skew limits the maximum rate at which the instrument can clock data into its memories.



Logic Analyzers, like the PI 616 (shown with a PI 648 companion data domain unit) and the Model PI 540, both have a real time A/D converter built in for single-shot waveform diagnosis.

Along with the many new product introductions in 1980 – spanning a price range from $750 to more than $15,000 – has arrived the game of specsmanship: all timing analyzers that were introduced in 1979 and 1980 can capture glitches to 5 ns; in spite of the fact that these instruments have input impedances ranging from 5 pF to 15 pF.

The other half of the glitch capture performance specification is the overdrive required for the instrument to detect a given pulse width. One aspect of this whole question is, how long are the leads from the user's test point to the first active circuit element of the logic analyzer? You can't beat the laws of physics: The longer these passive leads are, the more capacitance and inductance they introduce to the incoming signal, and reflect back into the user's circuit.

This is generally not a problem with lower speed logic analyzers (circa 20 MHz). For those logic analyzers with very fast clock rates, say greater than 50 MHz, input probe design considerations are of upmost importance to insure integrity of the signal passing to the logic analyzer detection circuitry, and also the reflection of that circuit impedance back into the user's system.

Human interface

Early logic analyzers without μP control had front panels that basically consisted of switches and knobs. The number of functions available on the instruments were typically modest. Now, with current third generation machines having a keyboard, and an interactive CRT display, the number of features and capabilities have multiplied.

The manufacturer is challanged to develop products in which the features and capabilities of the analyzer are easy to use. The user should very carefully evaluate the human interface of a given instrument to determine how easy it is to program trigger events, delay settings, etc., and also determine how "friendly" the instrument is. This assessment will be particularly important in the future as the logic analyzer gains more complex features, such as sequential trigger events, etc.

Another aspect of the "friendly" nature of the instrument is that a logic analyzer tends to be a casually used instrument. Whereas the engineer might use his oscilloscope every day while developing a μP-based system, he may only use the logic analyzer during a particular part of the development program. From one project to the next, he may not use his logic analyzer at all. When he takes it down from the shelf to apply it to a new problem, the human interface is important to him. Therefore it is necessary for him to be able to set up the instrument and use it in a minimal period of time. A good part of the success of a new product in the next two years will depend on how easy the features are to address, program, and use.

Input probing

There have been recent introductions of various kinds of specific input probing arrangements. These take the form of either a special hard-wired probe for a specific μP (which usually includes disassembly or mnemonics of that processor), and probes that allow interface to a specific bus-oriented system, such as IEEE 488 or RS-232C. These probing arrangements give the user an extra dimension in convenience at the expense of versatility, since the probes are dedicated to a specific function. The probes relieve the user of the tedium of connecting probes to a μP, or to his bus-oriented system.

This trend is expected to continue, since there are several different bus-oriented systems that can be specifically addressed; for people using these systems, the probes are really convenient.

One problem the user must face in the future is support. The manufacturer must decide which μP chips he is willing or able to support with hardware and software. The manufacturer must select, for support, those chips that have the most popularity or applicability and ignore the also-rans. Also, as discussed above, high performance logic analyzers require input probing arrangements that are appropriate to the speed of the mainframe. If the mainframe is capable of resolving signals in the time domain down to 10 ns, the input probes must be capable of passing data with rise times on the order of 1 to 2 ns.

Wither field service?

Another trend in 1980, not yet highly significant, is the orientation of logic analyzers to remote diagnosis. This is characterized in the Dolch, Paratronics, and BP Instruments logic analyzers by an RS-232C data link. This allows the logic analyzer to transmit trapped data from a remotely located system to a central facility such as the factory, for experts located there to diagnose the problem.

Other logic analyzers, such as the Biomation K100-D and Hewlett Packard 1602, have IEEE 488 I/O interfaces. This extends versatility of controlling the logic analyzer through the 488 interface via a suitable controller, but does require some kind of conversion device between IEEE 488 and RS-232C.

The concept of using logic analyzers in remote diagnosis has been crystallizing over the last couple of years. Most mainframe computer manufacturers have extensive remote diagnostic capabilities in place now. The idea of mating logic analyzers to a system of this kind has great appeal, since it gives the remote diagnostic link a time domain analysis capability.

Most logic analyzer manufacturers will be disappointed to learn that a logic analyzer is not a suitable instrument for general field service use. Its very nature prevents this: the logic analyzer collects simultaneously occurring data on many different lines, either with respect to its own internal clock for timing analysis, or with respect to the system clock for data domain analysis. Diagnosing a large, complex system with the information provided by the logic analyzer requires someone with intimate knowledge of that system. Most computer companies find it difficult and prohibitively expensive to find qualified people capable of making such analyses, or training lower level people to become qualified. Thus, the difficult and sticky problems that are best diagnosed with a logic analyzer will continue to be handled by those factory-level support people who have intimate knowledge of the system being diagnosed. These people exist, and are in place. Remote diagnosis helps them to leverage their time more effectively so that they need not travel to all remote locations experiencing trouble.

A case can be made for an analyzer preprogrammed with known good data. Then, it can trap suspected data and compare the two data sets to provide clues to the serviceman. This tends to be a simplistic approach, since system level problems are much better approached with self-diagnostics. Experience has shown that logic analyzers are better used in the hands of experts.

A second aspect of the preprogrammed logic analyzer is that of programming: it takes a good bit of effort to develop a library of reference data from which to troubleshoot faults. Invariably, the specific fault being observed in the field has not yet been programmed at the factory.

A more promising tool for routine service maintenance and troubleshooting is comprehensive self-diagnostics in the system being examined. Comprehensive and clever diagnostic routines built into the product or system can help to rapidly isolate problems to a PC board or sub-system level. Remember, the bottom line in field service support is minimizing downtime for the customer. In most cases, troubleshooting to the PC board level, and swapping that board out, is still the fastest way to get back on line.

Another potential time-saving device for field service troubleshooting is signature analysis. However, this concept still seems to be having trouble finding a home in the electronics industry. There is not a lot of evidence of this approach being used for system-level diagnosis.

Bear in mind that, when considering signature analysis as a logic analyzer feature, there are currently two implementations available: the classical H-P approach, which is a measurement based on transition counting and time; and a check-sum approach, which is a measurement based on data trapped in the logic analyzer's memory. The two measurement techniques are not compatible.

Self test diagnostics

Since we earlier mentioned self-test diagnostics, let's consider them in context of the logic analyzer.

Virtually all manufacturers of third generation logic analyzers (those analyzers that use a μC for instrument control) utilize some form of self-test diagnostics. When the instrument is powered up, the microprocessor checks

various aspects of the instrument's functioning. Certainly, these diagnostics are not absolutely necessary for the functioning of the instrument. On the other hand, the diagnostics give the user a high degree of on-the-spot assurance that the instrument is operating correctly. Depending on how these diagnostics are structured, they can also be used for troubleshooting problems down to the component level.

The efficacy of self-test diagnostics runs the gamut from a pure sales feature to an extensive component-level diagnostic package. Clearly, the potential buyer should evaluate these diagnostics as part of his evaluation procedure of several different instruments. This tends to be tricky, since no manufacturer puts a figure of merit on his diagnostic package. Perhaps a good rule of thumb to evaluate diagnostics is by examining how long it takes to run the diagnostics during power-up, and what secondary operations are available to the user to perform component level troubleshooting.

1980 trends

We expect the trend towards fitting logic analyzers into μP development and debugging tasks to continue at an evolutionary rate. Instruments will get faster and have more channels. The user must realize that, as the instruments get wider and faster, they also get more expensive, even though memory costs continue to come down. The cost of high speed memory is still not a real bargain. In addition, as speeds go up, input circuitry becomes considerably more sophisticated and must be designed for much wider bandwidths (to pass faster signals) than most analyzers presently have.

As a practical matter, a 100-MHz timing analysis capability for use on microprocessor systems is probably a realistic and useable clock rate. In the next two years, we will probably see microprocessors that can clock at rates from 15 to 20 MHz. Thus, a 10-ns timing capability is a reasonable compromise between having better time resolution and cost.

Logic analyzers will no doubt get more intelligent in the future, with better human interface, and there will probably be more offerings of disassembly of stored data into opcodes or mnemonics.

On the other hand, disassembly is not always the best route to follow. For instance, consider the designer working with a high level language, such as PLM or PASCAL. For this caliber of user, expected to increase in the future, disassembly does not help his analysis task. Compilers translate a specific higher level language into machine language which is binary, or more conveniently, hex.

Thus, when working with a high level language during the development phase, it tends to be more convenient to use a machine-code-oriented analyzer, rather than mnemonics, since the high level language typically does not generate assembled code. If you don't have an assembly language listing of your program, an analyzer with a disassembler does not help you. On the other hand, it's too soon to tell which approach will be the favorite among designers, high level language or assembly language. Each approach has specific advantages.

Some recent trends that are expected to continue on a small scale are the marriage of analysis (digital trouble-shooting) and scopes or waveform recorders (analog debugging). In the end analysis, when time domain problems are encountered, they are generally a result of analog problems: Address or data line ringing, glitches, noise, etc. Thus, having a scope triggered by a logic analyzer (or in the same box) or having a waveform storage device in the logic analysis system, makes sense. Unfortunately, many problems are random in nature. So, to use a scope for this kind of troubleshooting tends not to be effective. This defines the need for a waveform capture and storage device, either a storage scope or the so-called waveform recorder.

In a few years, analyzers and ICEs will grow alike. Disassembly is one analyzer aspect that tends to make it look more like an emulator.

Perhaps analyzers and emulators may not coalesce into one kind of a device. Perhaps we should make emulation totally software oriented, i.e., the user simulates his system totally in software. Once he has completely debugged all his code, and is now ready to begin the software/hardware integration task, he uses a stand-alone transparent analyzer to diagnose system level problems. This addresses the fact that emulators, at least in their present form, tend not to be truly transparent. Because of this, the emulator interferes with normal target system operation.

The world of μPs is not the only application area of logic analyzers, even though it is a large percentage of the total logic analyzer business. Logic analyzers are used as design and production test tools and in field service, as discussed earlier with respect to remote diagnosis. This customer base tends to rely more on the timing analysis capability of the logic analyzer, rather than data domain. The reason is that large systems tend to have sophisticated software diagnostic routines and datatraps in situ. The designer or troubleshooter of such large systems is faced more and more with critical timing requirements. Mainframe speeds continue to increase, with 9-M instruction/sec. computers a deliverable reality today. Timing relationships at the systems level, and especially within the CPU, continue to become more critical. When these problems become aperiodic, or random in nature, the use of a logic analyzer with fast clocking capability (beyond 100 MHz) becomes important in the troubleshooting task.

The major conundrum in designing ultra high-speed analyzers to test ultra high-speed logic is that the chips available for the design of such analyzers is the same logic that is going to be tested. Obviously, from a classical instrumentation measurement point of view, this is an untenable position.

On the other hand, various clever design approaches, such as multiplexing available memory chips to achieve a faster array speed, and designing front ends with GHz transistors, tend to ameliorate this kind of a problem. Reaching for ultra-high speeds in this fashion, however, is very expensive from a manufacturing standpoint. Thus, don't look for 16-channel 500-MHz logic analyzers, at prices less than $8,000, in the near future.

Market shakeout

During 1981 and 1982, we will no doubt see a shakeout of logic analyzer suppliers. In addition to the failure of various suppliers, or their getting out of the business, we will have new suppliers attracted to the market. The reason is the high growth rates in this market segment – 30 to 40% annual rate, compounded.

Is this of little importance to you, the user? Yes. Ask yourself: Who is going to maintain this new product that I just bought two years from now? Will the company still be in business, and will I be able to get parts from them? Will I be able to secure warranty repairs on this instrument? Thus, along with technical features and versatility, you must evaluate the staying power of your logic analyzer supplier. ■

Keyboards

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1981 will see the keyboard/terminal industry compare the cost of keyboards and switch technologies where no strong relationships exist. Manufacturers are advertising the \$75 keyboard, \$50 keyboard and \$25 keyboard. If everyone used the same keyboard, keytop layout and electronic configuration, it would mean a lot. Today's keyboard business will remain, in 1981, a custom business. OEMs will continue to ask for non-standard features.

Synergism cuts costs

Until now, a terminal manufacturer first designed the entire system and then discovered what he wanted the keyboard to look like. The result? An expensive, custom keyboard. 1980 saw more terminal designers and the keyboard manufacturers working together – from the beginning. 1981 will see the trend grow.

The real cost influencers

Keyboards will not continue to be an increasing percentage of terminal cost. The more customizing in the design, and the more components used, the higher will be the manufacturing cost.

So what are all these price announcements saying? More than saying anything, they are confusing the real issues and hiding the real price influencers. Some insist that the real cost of a keyboard is determined by the technology. Not true. Let's look at switch costs.

The highest cost is reed. Even though this is the most expensive switch technology, it has its place and will probably always have its market. It uses a hermetically sealed reed at each key position and is an absolute necessity in hostile environments. Price is usually not the main issue in selecting this technology. Second is the Hall effect switch; cost per station runs about \$0.10. Third is inductive technology which drops significantly in cost to \$0.03 per key station. The mechanical switch is fourth and costs \$0.02 per key station. Finally, capacitance switches are least costly and cost \$0.01; they have no precious metals and require no soldering. Prediction: the future effect of different switch technologies on keyboard costs will be small, especially with the two lowest-cost technologies.

The real influencers in a specific keyboard's cost are the electronic design, mechanical design (key layout, mounting method, connector) and keyboard manufacturer's commitment to vertical integration and automation.

Electronics

There is a definite trend towards a detachable keyboard in applications that require a CRT at which operators must spend a good portion of time. A detachable keyboard is moveable by the operator to a position most comfortable for him. This requires that the keyboard be attached to the terminal by a flexible cable which contains a minimum number of wires. Also, the keyboard must output data in serial fashion. This method reduces the number of lines to four or five: serial data output, power, ground, and optional serial data input (used for addressing LED indicators or change keyboard functions.) Such keyboards use inexpensive μPs to produce their serial output. A μP like the 8051, handles switch matrix scanning, key-down validation, code look-up tables and data serialization. Buffering the keyboard μP's serial output by a standard TTL device is most common and sufficient for driving the short cables.

The minimum interface

Established standards exist for two of the three major types of keyboard electronic interfaces. Parallel data output from a keyboard usually involves a 7-bit ASCII code, a strobe (data ready signal), power and ground (ten lines total). Serial data usually involves one serial line with a start bit, 7 data bits, and a stop bit, along with power and ground; 3 lines at 5-V levels or 4 lines for RS-232C. The problem arises with the "wired only" keyboard, especially with the increasing popularity of the capacitive keyboards. Hard contact keyboards lend themselves easily to the wired-only approach, but designing an interface strictly for them most often negates the possibility of utilizing a capacitive keyboard. A capacitive keyboard requires some A/D circuitry, which must be installed on the same printed circuit board. Such a keyboard, however does not require precious metal contact plating or a diode for each key to achieve n-key rollover. Therefore, it would benefit every terminal manufacturer to consider the advantages of reliability and low cost of a capacitive keyboard.

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Microcomputing Software

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From micros to mainframes, the cost, availability, and quality of software continued to dominate the computer world in 1980 with more computer power offered at a lower price. This development was emphasized by Intel's recent announcement of a 32-bit μP which will provide mainframe power at micro cost. No comparable breakthrough in software was announced, nor is one expected in the near future. Programs continue to grow larger and more complex at all levels. The number of programmers increases (although not at the rate industry would like). The sophistication of the user community grows. Yet, software productivity and reliability remain serious problems and only slow, evolutionary solutions appear likely.

At the μC level, two late (but long-rumored) announcements dominated the software news: (1) Intel's adoption of ADA (the Department of Defense standard language) as its systems programming language for the new 432 μP, (2) Microsoft's (Bellevue, WA) adoption of UNIX (the Bell Labs and Western Electric time-sharing operating system) as its standard OS for 16-bit μPs.

What can ADA do?

ADA is the latest effort to bring features from many earlier languages into a single general language. PL/I, an earlier attempt at the same goal, has adherents but lacked the wide acceptance that IBM anticipated. ADA, however, starts with the backing of the DOD. This language has been under development for about 5 years and is close to final form. The next two years should see the emergence of standard and actual compilers for the language, although preliminary packages are already in limited use. ADA's goals are as follows. . .

1) To continue the trend toward modular programming, structured programming, and top-down design that was embodied in PASCAL. The emergence of structured assembly languages and structured versions of BASIC and PASCAL shows the popularity of these techniques.

2) To provide a single language capable of handling applications ranging from business data processing to real-time, embedded control systems. A single language obviously eases the problems of training, project management, control, maintenance, and documentation.

3) To combine a general, applications-oriented language with a systems programming language. The result should be useful both for writing applications software and for writing operating systems, compilers, communications packages, and interactive systems. The combination eases the problem of developing programs that fall partly in both categories, such as the software for a piece of programmable test equipment or a programmable signal processor.

4) To support specialized areas such as real-time applications, interactive systems, and parallel processors.

5) To help with what have become the most expensive and most time-consuming stages of software development: debugging, testing, documentation, and maintenance. The language should have features that aid in the development of reliable, modifiable programs that are easy to debug, test, and document.

6) To provide a complete, unambiguous definition that can serve as a standard for implementation on a variety of machines.

7) To allow use of the special techniques necessary for large systems; such as separate compilation of modules or entire subsystems, levels of access allowing large teams to work together without interference, and automated software tools.

8) To provide efficient representation of a variety of data structures and operations on those structures without demanding awkward, stilted efforts from the programmer. The compiler should handle details of the implementations.

9) To provide separate environments for various user levels; such as, systems programmers, applications programmers, package developers, end users, central operators, remote users, teachers and students. Programs and data created in one environment may have to be protected partially or completely from users working in other environments.

10) To handle special situations, such as custom input/output, or the need to include routines in other languages, or the invariably required exceptions to general rules.

Obviously, these goals are hard to achieve with any language. Individually, there is considerable argument about what they mean and how they can best be reached. Furthermore, any language must meet the more traditional goals of ease of use, object program efficiency, small size, portability, ease of implementation, and compatibility with languages previously used in a particular application area. One can hardly expect that ADA will be the ultimate solution to all programming needs and problems.

Here are ADA's key features . . . .

1) Type declarations. Not only must the programmer declare the type of each variable (as in ALGOL and PASCAL), but he/she may also declare new types. The traditional types (Boolean, integer, real, record, etc.) are, of course, supported. The user may, however, declare new types such as a grade level (an integer with values 0 to 12), an employee record (with certain fields), or a node in a communications network. This ability allows the programmer to work at a more natural level (particularly simplifying documentation), and also allows the compiler to check syntax and to inform the programmer about improper specification and use of data.

2) Package declarations. A package can be an entire set of types, functions, procedures, and other resources. It can have its own independent existence, regardless of other parts of the program with which it is combined. Obviously, package facility simplifies the use of standard programs such as floating point packages or communications packages as pieces of larger systems.

3) Tasks. A task is a program that can be executed concurrently with other programs and can also be started, suspended, or interrupted independently. Multitasking is essential for the development and operation of real-time and parallel systems.

4) Access rights define the ability of one program to utilize facilities inside another program. A program may specify that only certain variables, structures, or functions are available externally to certain users. Details of an implementation may then be hidden within a program, easing debugging, testing, and maintenance.

5) Protection levels determine which programs have the rights to read, write, and perform other functions on particular data or programs. For example, a user program running on a piece of programmable test equipment must not interfere with the operating system or translator programs. It may, however, be able to use some systems programs, such as I/O drivers or timing routines. A diagnostic program, on the other hand, may need more general rights while a debugging program used at the operating system level must have more general rights to use and change facilities at a variety of levels.

Thus, ADA is a higher high-level language with many of the features of systems programming languages (used in developing operating systems and other systems software), simulation languages (used in simulating systems made up of complex structures), string-handling or information-processing languages, and other special-purpose languages. What is ADA's future? The next decade will tell the story. There will surely be much resistance from users, programmers, and analysts with large investments in older languages. For many, the older languages have done the job and they see little reason for change. The continued use of FORTRAN and COBOL is ample evidence of the cost and difficulty of change.

But many factors will promote the spread of ADA. The DOD will insist on its use in many defense-related applications to provide ADA with a base. A large community of new computer users has no software investment to guard; this community could be converted to ADA. Intel's selection of ADA is a large boost toward its widespread use. Intel is a major force in μPs, but it is almost entirely non-defense-related. Thus Intel has given ADA new respectability *outside* the military/defense establishment and among newer users. Why did Intel make this choice? Some of the reasons: (1) Existence of the ADA base in the military/defense market. (2) A strong, universal definition that will be maintained and extended, as compared to the narrow definition and use of most system programming languages. (3) ADA's features for supporting real-time applications, multiprocessing, parallel processing, and separate environments. (4) The need for a more powerful and more general systems language for mainframe-level micros such as the 432. However, Intel appears to be still hedging its bets – the 8086 and its successors (the 186 and 286) will use PL6M and PASCAL as their systems programming languages. ADA will be added later if the market will support it (and demands it).

What can UNIX do?

UNIX is a time-sharing operating system from Bell Labs, originally developed for the PDP-11 about ten years ago. It is the PASCAL of operating systems, the favorite of a large number of sophisticated users despite lack of support from its developer or from any of the computer manufacturers. UNIX has thus become almost a cult item, particularly in academic and research circles.

Microsoft, however, plans to make it more than a fashion. The company intends to promote UNIX (or XENIX as Microsoft calls its version) as their central product of the 1980s, much as their widely used BASIC interpreters in the 1970's. Microsoft has obtained a special license from Western Electric, with rights to appoint distributors and sublicense other users. The plan is to have XENIX available with support on the DEC PDP-11, Zilog Z-8000, Motorola 68000, and Intel 8086 by the end of 1981.

Reasons why Microsoft made this choice: (1) The immense amount of time and effort required to design and implement a completely new operating system. (2) The numerous specialized software tools already available for UNIX, such as the Programmer's Workbench and the YACC compiler-compiler (used in writing language compilers). (3) Ten years of field experience and debugging UNIX. Field experience is considered the only method to locate the subtle problems in a large operating system. (4) The generally high regard in which UNIX is held in the computer community. (5) The availability of the C programming languages for system development.

Of course, Microsoft has a lot of work turning UNIX into a popular, general-purpose operating system. Most current UNIX installations are sophisticated users who can handle problems. Few users are involved with specialized applications and few have to worry about problems like commitment of code to ROM, real-time applications, or embedded systems. But UNIX certainly offers Microsoft a strong base from which to work.

Other developments

Here, briefly, are other software developments: (1) Extension of the popular CP/M operating system to the 8086. (Whether the limited, single-user CP/M can compete with the far more powerful UNIX is open to question.) (2) A new assembly language standard for μPs. (Surely we need a great deal more work in the software standards area.) (3) Increased availability of multitasking real-time operating systems for μCs. (These systems are rapidly becoming more

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Data Communications for Minicomputers

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This past year was noteworthy because of the development of a new range of data communications products designed specially for use with minicomputers and dumb terminals. Mini data communications requirements differ from those of large mainframes. Communication is over shorter (50-100 mi.) distances – not 2,000 mi. Minis have only one or two discrete data communication "links" to remote offices – not a complex multinode "network." The big difference is that the mini only supports, with few exceptions, asynchronous "dumb" terminals, whereas the mainframe user typically expects his terminals to benefit from some kind of built-in "communication protocol."

Communication protocol

Communication protocol is a set of rules governing information flow in a communication system. Rules include a definition of the block format or 'message envelope' (used to "packetize" each message transmitted.) The 'message envelope usually contains special "control characters" to mark its beginning and end, along with an address which directs messages to selected terminals. It may also include a sequence number and/or block check character so that the receiving terminal may check the incoming message for errors. The protocol rules also define how a terminal "acknowledges" a message or, in the event it detects an error, how a terminal requests a retransmission.

One of the most widely used communication protocols is IBM's Binary Synchronous Communications Protocol, known as BISYNC. BISYNC was first introduced in 1960.

The overall format of a typical BISYNC message has the message preceded by the SYN (synchronization) character necessary for correct operation of synchronous terminals. The header information begins with the special control character SOH (Start of Header) and ends with STX (Start of Text). The text portion of the message is variable in length and terminated by ETB (End of Transmission Block) if more messages follow, or ETX (End of Text) if no more messages are to be sent. The message is terminated with BCC (Block Check Character).

If a terminal conforms to one of the defined communication protocols, such as IBM's BISYNC, it operates error-free because it has the benefit of automatic retransmission-on-error; it can also be 'multidropped', either individually or in clusters, with other terminals on a single line because it can be selectively addressed or 'polled' by the host computer.

Polling

"Polling" involves the addressing by the host computer of each terminal on the line, one after the other. In a typical application, the computer polls the first terminal which responds "NAK" if it has nothing to transmit, or "ACK," followed by its message if it has a message to transmit. The computer then polls the next terminal in sequence. If any terminal does not respond, the computer will "time out" and proceed to poll the next terminal. Polling takes place constantly, in round-robin fashion. Outbound messages from the computer are also transmitted to each terminal when it is due to be polled. Typically, the ACK-NAK protocol is also used to verify correct receipt of messages or request transmission.

Terminal polling is only possible if three criteria are satisfied:

(a) The terminal must be 'small' enough to have an 'address' and be able to respond when it reads its address in a message received on the line.

(b) The terminal must be 'buffered,' since it only has access to the line at the discretion of the computer. Such a system is only efficient if the message has been entered at the terminal and is ready for transmission in the terminal's buffer when the terminal is polled.

(c) The host computer must have software available to perform the polling procedure and support the particular communication protocol which the terminals are designed to use.

Typically, these criteria are only satisfied in terminals and data communication systems supplied by the large mainframe manufacturers or designed to be compatible with the product offerings of the mainframe manufacturers. The minicomputer user is typically forced to use so-called "dumb" terminals and configure his terminals one per computer port, thus losing the cost advantages of being able to put multiple terminals on one line and also losing the benefits of retransmission-on-error.

Before reviewing the data communications implications of dumb terminals in detail, it should be clarified that *all* of the minicomputer manufacturers do offer software support for one or more communication protocols, especially the popular IBM BISYNC protocol. In addition, DEC, for example, supports its own DDCMP, and Data General offers support for the international standard packet-network access protocol, CCITT X.25. But the software support is *not* designed for communication with terminals. It is designed for distributed processing applications to permit the minicomputer to be connected to a large mainframe host, emulating an IBM BISYNC terminal, for example, or it is designed to facilitate computer-to-computer communication using packet-switched networks (in the case of

Data General) or DEC's own "DECnet" network architecture.

Dumb terminal

A dumb terminal is a protocol-less terminal. It may incorporate a micro and a very extensive control program which permits it to do very intelligent local screen formatting, prompting, data field validation and range checking, but such a terminal is still 'dumb' if it is Teletype®-compatible. Without a protocol, a terminal cannot be addressed, so it cannot be clustered or multidropped with other terminals on the same telephone line, and it has no means of assuring error-free data over real-world telephone circuits. As a data communication device, such a terminal is indeed dumb.

The reason why such terminals are the rule in the minicomputer world and the exception in the mainframe world is twofold:

First, whereas terminals in the batch-oriented world of the mainframe computer are normally remote from the computer site, the interactive, transaction-processing design philosophy of the minicomputer manufacturers means that terminals are the sole means of computer access to local users, as well as remote users. Most of these terminals are hard-wired to the minicomputer, not connected over telephone lines, so they do not need sophisticated retransmission-on-error or line-sharing capabilities.

Second, there is no standard communication protocol. The communication protocols used in the mainframe world are the inventions of IBM, Univac, Burroughs, and others. Each protocol was defined by a single manufacturer so that terminals and computer software could be developed to support it. With such a large percentage of their terminals attached locally to the host minicomputer, minicomputer manufacturers have not felt the need to develop and aggressively market a protocol of their own, except to enhance computer-to-computer communication. Furthermore, with so many of their users satisfied with the present arrangement, and so many of their OEM's and system houses anxious to preserve the freedom of choice which the Telprinter-compatible industry standard provides, the manufacturers are not strongly motivated to invest in a protocol of their own inventions. Instead, they will wait for an international standard to materialize, perhaps based on the CCITT X.25 protocol defined for access to international packet-switched networks. But such a standard will only evolve very slowly.

In the meantime, the dumb terminal will continue to thrive. But, for the increasing number of minicomputer users who cannot tolerate the risk of undetected data transmission errors and the telephone costs associated with using multiple 'dumb' terminals at a single office remote from the computer, the new data communications products introduced in 1980 offer a new era of reliable, cost-effective data communications.

The data concentrator

The data concentrator uses statistical multiplexing techniques, so several "dumb terminals" share a single telephone line, with one concentrator unit installed at each end of the line. The device operates extremely efficiently with interactive CRT terminals, since it allocates the shared telephone line to each terminal dynamically, as needed, rather than on a predefined basis. As a result, for example, it can allow four CRT's each operating at 2400 bps to share a single 2400 bps line. In addition, the protocol used between the concentrators incorporates the same retransmission facility provided for single terminals by the Error Controller. Thus, the Data Concentrator acts as both an error controller and cluster controller for as few as two terminals, without requiring any changes to the existing dumb terminals hardware and mini software. Incidentally, it also allows the asynchronous terminals to be used with high-speed synchronous modems.

Multidrop concentrator

The multidrop concentrator uses the same statistical multiplexing techniques as the Data Concentrator, but since it can be configured in a multipoint configuration it allows individual dumb terminals and dumb terminal clusters to be multidropped at different locations to share a single multipoint phone line.

In operation, the master concentrator polls the remote Node units at high speed, accepting multiplexed inbound data from terminals at each site and delivering multiplexed outbound data addressed to individual terminals at each site. The multipoint data link operates synchronously at speeds to 9600 bps, but speeds of 2400 or 4800 bps are most typical. The individual 'dumb' terminals multiplexed by the Node Concentrator at each site may operate at virtually any asynchronous data rate to 4800 bps.

Port concentrator

All other products require no changes to existing hardware and software. They preserve the one-to-one relationship between each terminal and its associated port on the mini. But in some configurations ports may be limited. Some type of port-sharing device may be desirable.

The benefit of the true communication protocol, supported in software on the host computer, is that it allows multiple terminals to be polled using a single computer port as well as a single telephone line. But unless special software resides in the host computer, it is not possible to support multiple terminals on a single port. The purpose of the Port Concentrator is to simplify the special software required.

Port selector

The Port Selector controls and coordinates terminal access to a computer facility, integrating dedicated terminal connection with dial-up access, if required, and providing the advantages of both without the disadvantages of either.

The port selector is installed between the computer and the terminals. Like the phone rotary, the Port Selector provides first-come-first-served contention between a large number of terminals for a smaller number of computer ports. But, unlike the telephone rotary, this facility is offered to all terminals whether access is dial-up or dedicated. In the simplest type of application, all terminals are in contention for all ports. The port selectro provides the same contention and port selection facilities provided by the dial-up phone rotary, without the speed restrictions and high cost of dial-up access.

The future

Looking forward to 1981, it appears likely that additional products will have integral modems to cut costs and simplify system design and installation. High-speed modems will provide a built-in error controller and concentrator modems will package a data concentrator with a high-speed modem family in single units. 1981 will see growing data communications sophistication for mini and "dumb" terminal users. This will increase data communications applications.

Digital Image Processing

Ted Driscoll and Chris Walker
Staff Report
International Imaging Systems Div.
Stanford Technology Corp.
Sunnyvale, CA

Digital line processing, in the past decade, has gone from an exotic research field to real world application. The area of activity has been in a variety of professions, notably remote sensing, medical imaging, non-destructive testing and meteorological prediction. This growth was assisted by advances in microelectronics, minicomputer manufacturing and video technology. At the beginning of the 1970s, large mainframes performed the necessary image processing operations. Primitive displays allowed examination of the results, but these displays were limited in their capabilities. As image processing enters the 1980s the situation is changing. A number of manufacturers now offer sophisticated "image display-computers" that allow the user to see the image being worked on, and also perform complex processing, internally, at high speed. This development has allowed the host computer in an image processing facility to become smaller and cheaper. It has also made possible new ways of approaching classic image processing problems.

The new generation of image display-computers can be described as limited-precision array processors. Limited precision means that the processing is generally limited to 16-bit integers and typically the input data has only 8-bit precision or less. This is the dilemma that faced image processing a decade ago: how to process copious, low precision image data. Image display-computers were developed to provide this processing capability. Their integer precision permits high speed sequential computation in pipelines. They also offer the additional advantage of maintaining spatial, two-dimensional distribution of data. They are "image" processors where the word "image" refers to any regularly distributed, two-dimensional form of data. This spatial data is not limited to imagery; it includes radio astronomical data, topographic and cartographic data, graphic arts printing masters, and synthetic aperture radar. This generation of image display-computers can both process and display their data. Furthermore, the latest examples of these devices are not limited to simple processing tasks. These display-computers have made possible the implementation of a variety of complex algorithms for image classification, transformation and enhancement, running in real time under interactive control by the user.

To see what's happened and will happen, let's examine one of these image display-computers. It consists of an expandable pool of refresh memory channels which are directed through lookup tables (LUTs), then scroll, splitscreen and zoom hardware into any of three high-speed processing pipelines. These pipelines allow full precision summing of any or all data streams from the refresh memories and then lookup-table-like scaling or transformation of the results in the Output Function Memories (OFMs). The resulting three data streams can then be directed to two places: either to D/A converters which drive the red, green and blue inputs of a color display monitor; or back through a feedback path to a higher precision processing unit (ALU) and on to the refresh memories again. Older designs provided only a linear flow of data from image memory to the display monitor. Transformations performed along the way could not be saved for further processing. The loop architecture described can iteratively or recursively process image data. Specifically, the output of a given operation can be directed back to refresh memory for further processing by the same algorithm or a different one. In addition, the later stages of the loop at the ALU can handle higher precision data streams so that iterative operations overflowing the pipeline precision can still be handled. This 16-bit data stream can be stored in a pair of 8-bit refresh memory channels by merging them together as a 16-bit "accumulator" channel.

Such an architecture is oriented to complete images, not pixels ("picture elements"). A feedback operation involves the return of 262,144 (512X512) pixels in sequential order to a selected refresh memory. Transformations, pipeline addtions, etc., are applied to entire images or regions of interest in entire images. The basic module of data in this device is the "image", not the individual pixel. This global processing simplifies description of algorithms (when we refer to a subtraction we mean a pixel by pixel subraction of two complete images.) Pipeline processing is performed as a single step, and can be executed so quickly and exactly that in many cases, the results are not kept. They are merely used to refresh a video monitor and then recomputed during the next video refresh cycle. The results are saved only when a "feedback" is executed. In this case an entire image is passed through the rest of the loop and directed to a selected refresh memory channel. Conceptually, this is similar to parallel processing; in fact it is accomplished sequentially at high speed.

The new generation of image display-computers can be used for very complex processing. They are, nevertheless, general purpose devices within the context of image processing. Such flexibility has led to a second major change in image processing. This is the movement of complex processing from software running in the host computer to the hardware of the display-computer running under host control. This is known as "implementation in hardware" because the actual computation for the algorithms is accomplished in the pipeline. However, as with any other hardware device, some software control is necessary. In the case of the architecture and algorithms described here, this software control consists of small DMA transfers to various subunits, usually to load tables and enable data paths. Such transfers never approach the number of words of data in the subject image that would have to be read or written in a software multispectral classifier. The computation necessary to generate the tables is simple compared to the classification computation. Also, when the host is simply controlling hardware, there is a major improvement in speed. This makes possible the interactive use of new algorithms that once took too long to consider in an interactive process. A cluster classifier requires no input other than the image itself. Cluster classifiers are "unsupervised." Figuratively, a supervised classifier "demands" that the image return information about certain given landcovers. On the other hand, an unsupervised classifier takes a less biased approach by "requesting" the image to return those classes that are most differentiable. Again, such an algorithm has been implemented in the display-computer. Typically, cluster classifiers are among the slowest and most CPU-intensive image processing functions. Execution times can easily run into hours and as a consequence of this, some implementation of cluster classification has dramatically improved execution time while still acting on a full 512 by 512 image. This has been accomplished using a classification algorithm and features of the display processor that allow rapid collection of image-wide statistics. The results, after interpretation and merging of similar classes, would look like figure 4. As before, this implementation is limited to ten channel data and 255 classes. It allows the user to control the size of a class, the separation between classes, and number of iterations performed. The resulting high-speed, unsupervised classifier permits the user to probe an image. Rather than being forced to rely on a one-time cluster classification, the user can interactively explore different parameters and learn enough about the scene to eventually perform a supervised classification. Speed of operation translates to more interactive processing, greater knowledge of the study area and, consequently improved accuracy.

Bivariate histogramming

This function plots a bivariate frequency distribution function. A 256 x 256 graph is produced in which the value of each cell represents the number of pixels that have those values in the two input channels. This requires large data areas and enormous input/output requirements in any software implementation. Hardware histogramming capabilities dramatically simplify this operation. The software needs only to read and write 256 histogram values 256 times to plot this scattergram. Since these histograms are taken in one fifteenth of a second in the hardware, the function cosumes approximately twenty seconds in a worst-case situation. The output graph can be very useful in interpreting the distribution of data values and identifying distinct classes or clusters.

Median filtering

This filter algorithm is similar to convolution except that the output value for each pixel is the median of the neighborhood values in the input image. The resulting image has reduced the high-frequency noise without a corresponding loss of edge definition. The implementation involves a sort of approximately (p**2)/2 comparisons to find the neighborhood median, where "p" is the number of pixels in that neighborhood. Using the capabilities of the display-computer architecture that allow an entire image to be processed in one pass, and the two summing stages available in the pipeline and the ALU, it is possible to implement such a sort in the hardware.

Image rotation

Spatial deformations such as rotation or magnification are time-consuming image processing algorithms. Implemented in a host computer they require large data storage areas or large amounts of image I/O. The display-computer can be used to significantly speed first-order spatial transforms because of its capabilities of selective feedback and independent horizontal and vertical scroll. In rotations or magnifications, a hardware implementation can take advantage of the fact that large groups of pixels move together in a predictable manner. We have utilizied these features in a hardware rotation function that is substantially faster than previous software implementations. At present it is limited to "nearest neighbor" pixel sampling but will soon be extended to include bilinear interpolation. It is also limited to 512 x 512 images by the display architecture, but within these limitations the results are indistinguishable from software-generated rotations.

Topographic rotations

Image display-computers are not limited to image data. Other two-dimensional spatial data can be effectively processed with startling improvements in speed or capability. As an example, topographic data is available for the continental United States and the display computer can perform a number of complex operations on this data. Formerly, this was only possible in software. Topographic data is in a gridded form with a value in each pixel corresponding to that pixel's central or average elevation above sea level. When displayed as imagery, low elevations appear dark and high elevations appear light.

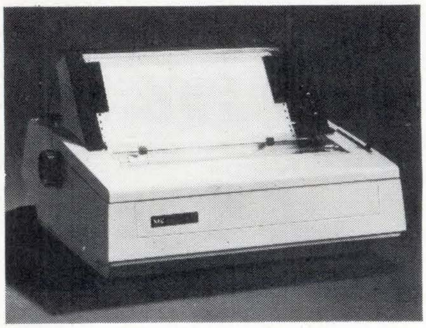
Conclusion

Execution speed improvements range from 3.25:1 to an estimated 230:1. More important, hardware implementations are now all running in seconds, or what could be referred to as "interactively." If a function takes longer than a couple of minutes to finish, the user will generally use it differently; i.e., in a batch mode. This kind of use discourages refinement, cross-fertilization, and exploration. On the other hand, if a function finishes quickly, it encourages the user to experiment with different parameters. The end result is that hardware implementation improves the utility of an

Digital Image *continued on p. 94*

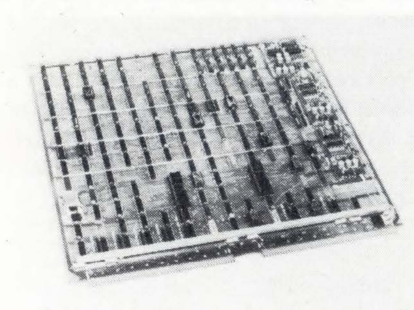
New Products

OEM PRINTER. This fully formed character printer offers a reliability standard of 3,000 hours MTBF, and requires OEMs to stock only 3 major parts to affect repairs. It is the size of a standard office typewriter, with print speed of 30 cps and is lightweight and quiet, with a low 58 Dba sound rating when used with an op-



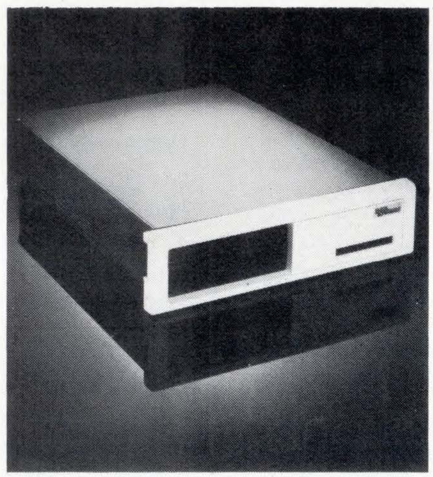
sound rating when used with an op-tional cover set. All electronics, including 3 μPs, are mounted on a single circuit card. A new swaging technique eliminates more than 100 parts while producing a more rigid and durable printer frame. The Spinwriter 3500Q is $1430/100. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173 **Circle 184**

GRAPHICS/IMAGING POST-PROCESSOR features a 256 × 13 video lookup table (VLT) which accommodates color and monochrome images requiring 256 selections per pixel and/or multi-level, high resolution graphics such as detailed CAD/CAM type applications. It provides 13 VLT bits in parallel. In monochrome, the VLT can be used to drive 2 monitors and provides one 8-bit output (256 grayshades)



and one 4-bit output (16 grayshades) with one bit for blink. Up to 8 full bit map memory planes may be software selectably gated into the VLT. The GCT-3032-8 is also equipped with two RS-232 ports for interfacing interactive devices. $4,700/unit. **Genisco Computers,** 3545 Cadillac Ave, Costa Mesa, CA 92626 **Circle 178**

WINCHESTER/FLOPPY. This DEC-compatible system combines an 8″ Winchester disk and an 8″ floppy disk in a 5 1/4″ high rack mountable unit, with 8.8MB of total capacity. LSI-11 and PDP-11 interfaces are also available. Features of the DSD 880 include a control panel for selection of operating modes, off-line functions and "hyperdiagnostics." Off-line functions include copying the contents of the Winchester to and from the floppies.



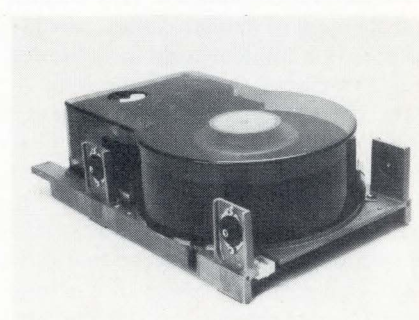
Off-line diskette formatting and error reporting, by two 7-segment LED displays, are also provided. The hyperdiagnostics is a package of microprogrammed routines that enable users to trouble-shoot a DSD 880 without a host CPU, and rapidly identify faulty models. ($7495). **Data Systems Design, Inc,** 3130 Coronado Dr, Santa Clara, CA 95051 **Circle 172**

DC POWER SUPPLIES. These 40 and 60 watt open-frame switching D.C. power supplies come in 2 package sizes with single and multiple output versions. All units have an extended range AC input of 90-132/180 VAC. The single output models 5A5 and 5B5 deliver 5V @ 7A and 12A at full load. This 5A and 5B series is $45 and $75/unit. The 40w multiple output 5AXMP delivers 5V @ 4A, ±12V @ 0.5A, −5V @ 0.5A and +15V @ 1.0A for $59/unit. The 60W multiple output 5BXMP delivers 5V @ 7A, +12V @ 1.5A, -12V @ 0.5A and −5V @ 0.25A for $89/unit. **Sierracin/Power Systems,** 20500 Plummer St, Chatsworth, CA 91311 **Circle 181**

APPLE DRAWING TABLET. Using a menu on the Apple's screen, the user can select from 6 colors for lines or 106 colors for fill-in areas, width of drawing line, and magnification size. Straight lines can be drawn automatically. Images can be stored on disk and called up later for changes or incorporation into another picture. VersaWriter comes with 2 disks, which include a set of common electronic schematic and logic symbols. Software includes: automatic color fill; Textwriter which lets the user add text to an image for titling, etc.; calculation of distance or area; and Shape Tables for recall of images in any program and for animation by storing a sequence of images. A 32K or larger Apple computer with disk and Applesoft in ROM, or Apple II Plus is required. $252. **Peripherals Plus,** 119 Maple Ave, Morristown, NJ 07960 **Circle 142**

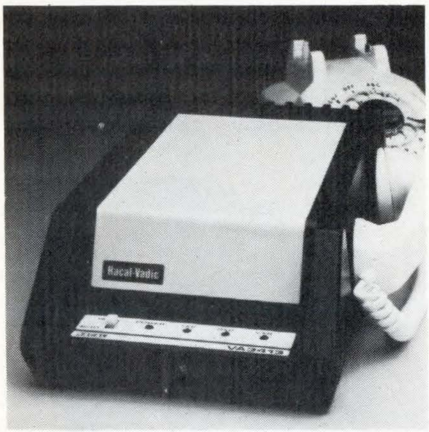
MEMORY BOARD. These modules are completely compatible with WANG MVP, VP and LVP memory boards. The SMS3515 detects parity errors on incoming and outgoing data. Parity errors are stored in the memory array and are indicated by card edge LED indicators which can be manually reset. **Automated Control Systems, Inc,** 1801 – 130th NE, Bellevue, WA 98005 **Circle 138**

8″ DISK DRIVES feature a high speed average access time and high capacity. Enhanced Winchester 3350 type technology contact-start/stop heads and media are used at densities of 9550 bpi and 720 tracks/inch. The direct drive DC spindle motor rotates at 3,600 RPM which yields a data transfer rate of 1.229 MB/sec. Model 2311 stores 48 MB on 2 platters and the model 2312 stores 84 MB on 4 platters, utilizing 589 cylinders at 20,480 bytes/track. An industry standard SMD



interface is no extra cost on the 2311/2312 family of drives with data separation circuitry included. Other interfaces are optional. Model 2311 is $3195/100, model 2312 is $3795. Lower cost models include the 2301 (11.7 MB) at $1660/100, and the 2302 (23.4 MB) at $2095/100. **Fujitsu America, Inc.,** 2945 Oakmead Village Ct, Santa Clara, CA 95051 **Circle 129**

DUAL ACOUSTIC COUPLER provides both 1200 bps and 0 to 300 bps full duplex async operation and is fully compatible with VA3400 and Bell 103/113 type modems. Using μP control, it employs a scheme for automatic detection of the called modem. Another feature is automatic 9 or 10

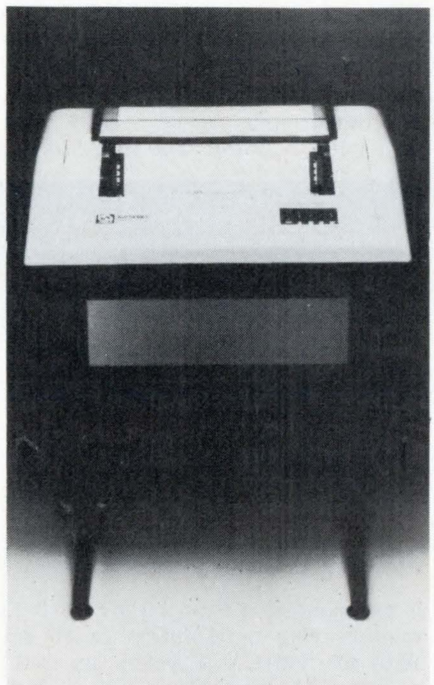


bit character length recognition in the VA3400 mode so the user can communicate with either 9 bit (primarily IBM) or 10 bit systems without any physical changes to the modem. The VA3413 is \$895, OEM discounts available. **Racal-Vadic**, 222 Caspian Dr, Sunnyvale, CA 94086 **Circle 192**

2 MHz FUNCTION GENERATORS. Both feature $\leqslant$ 0.25% sine distortion and $\leqslant$ 25 ns pulse rise time. The FG 507, a TM 500 plug-in, has mathematically accurate log and linear sweep capabilities. The FG 501A contains the same high performance and low distortion sine waves but without the sweep capabilities. It replaces the FG 501. New features include increased frequency, output voltage and offset; output step attenuator; variable symmetry; and trigger mode. Both generate 5 basic waveforms – sine, square, triangle, ramp and pulse – at output levels up to 30V peak-to-peak with up to ± 13.0V of offset from a 50-ohm source. The FG 507 is \$1250; the FG 501A is \$680. **Tektronix, Inc**, Box 1700, Beaverton, OR 97075 **Circle 195**

PHONE LINE MODEMS. The first of these data communications products is a μP modem operating at 14400 bps. It offers greater speed, lower communications costs and increased data throughput. It is designed to communicate with Analysis network management systems. Also available is a 9600 bps multipoint modem which operates at its rated speed both inbound and outbound and trains in 20 ms. The third product is Datalyzer which provides computer system data traffic measurement capabilities in conjunction with the communications network measurement capabilities provided by Analysis. The Vertical and Horizontal Coordinates Program for Analysis automatically determines the least-cost configuration for each multipoint line within a communications network. The final two products are a 2400 bps diagnostic modem for operation in IBM 3600 loop networks, and MP-4800/208B Bell-compatible modem. **Paradyne Corp**, 8550 Ulmerton Rd, Largo, FL 33541 **Circle 185**

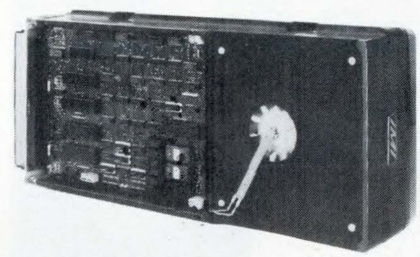
TERMINAL ENCLOSURE. The new Intermediate Terminal model features an ergonomic enclosure with a detachable keyboard to allow independent positioning of keyboard and display with extended keyboard housing to provide a hand rest. It can accommodate extra circuit boards for added features or customization. The μP-based ADM-32 includes two full



1920 character pages of memory, function keys, complete editing capabilities, block mode transmission, visual attributes, business graphics, a numeric keypad, full or half duplex conversation modes, self-test and typewriter tab stops. Available in early 1981. **Lear Siegler, Inc.**, 714 N. Brookhurst, Anaheim, CA 92803 **Circle 174**

SOFTWARE PACKAGES. The MRX-PRINT package allows the printing of computer output on IBM 3284, 3286, 3288, Memorex 2089 and equivalent printers at local or remote sites. Output can be queued from TSO terminals, from JES2 and from user-written programs. Flexible control of the printing network is achieved through commands from operator consoles and TSO terminals (\$7500). The Direct Access Space Manager (MRXDASM) is a dump/restore package that provides back-up, recovery and space management functions for high-capacity disc drives including disc-to-disc copy, data set control by group name, and disc-to-tape or tape-to-disc compress. It also includes device independent copy/restore, and an archiving facility. (\$8500). Also available are Quantitative Computer Management (QCM), Shared Tape Allocation Manager (STAM) and Shared Data Set Integrity (SDSI). **Memorex Corp**, MS 12-16, San Tomas at Central Expwy, Santa Clara, CA 95052 **Circle 191**

8″ WINCHESTER WITH SBC. The embedded controller fits within the 10 and 20MB drives to provide an average access time of 35 ms and power re-



quirement of 75 W. It provides a high-performance, async, parallel interface between the 8″ drive and CPU. Many cumbersome software routines previously executed by the CPU can now be handled in controller firmware. The 7710 and 7720 drives with controller are \$2195 in OEM qty. **International Memories Inc**, 10381 Bandley Dr, Cupertino, CA 95014 **Circle 140**

PROGRAMMING SLAVE. This unit, an addition to the SMARTY PROM Programming System, allows programming of 16 EPROMS to 32K bits. Up to 15 SWEET 16s can be daisy chained to the SMARTY for programming of 240 EPROMS simultaneously. The SMARTY system includes keypad selectable device types, LED indicators to confirm correct selection, LED

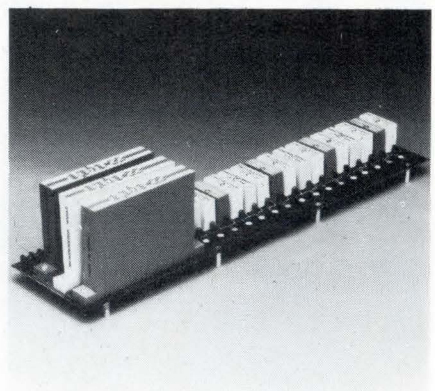
device error indicators, editor, serial and parallel I/O, switch selectable baud rates to 9600, PPTR interface and PROM simulator. The SMARTY is \$1995; the SWEET 16 is \$2250; and an optional built-in Micro Cassette Data Storage unit to upload or download programs from RAM is \$695. **Sunrise Electronics**, 524 S. Vermont Ave, Glendora, CA 91740 **Circle 139**

New Products

DEVELOPMENT SUPPORT TOOLS. With BSO assemblers, any Data General computer can be converted into a multi-user, μP development system for Intel, Motorola, Zilog and TI 16-bit μPs. Other assemblers can be added creating a universal development system supporting 30 different μPs and up to 128 users. Additional products permit a DG development system to interface to μP in-circuit emulators, dedicated μP development systems, PROM burners and universal emulators. Assemblers start at $1200 (3 or more). **Boston Systems Office, Inc,** 469 Moody St, Waltham, MA 02154

Circle 187

REMOTE I/O WITH TIME DELAY. Programming of the timed mode and time duration is accomplished by command from the host computer. The timed mode can be either a delay or a pulse function. The time interval



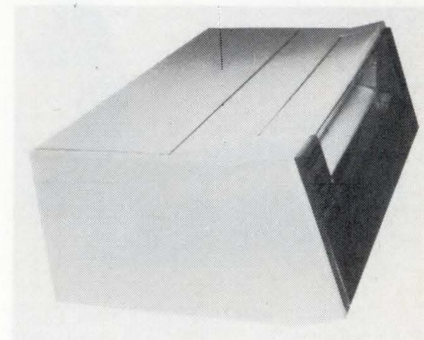
is programmable from 10 ms to 10.92 minutes with a resolution of 10 ms. With the SAMUX II system, up to 32 of the 192 I/O modules can be programmed to function in the timed mode. **Opto 22,** 15461 Springdale St, Huntington Beach, CA 92649

Circle 161

IMAGE PROCESSING SOFTWARE. This Library of Image Processing Software (LIPS) package has programs for 2 or 3-dimensional convolution operations with selectable FIR kernels; contrast enhancements; adding, subtracting, multiplying and dividing images; as well as histogram computation and display. Written in PASCAL, FORTRAN, and MACRO-11, LIPS also includes programs for tape archival and directory; flexible image and data file formats; direct or inverse Fourier transformations; complex image display aspects of amplitude, square amplitude and real or imaginary part in addition to a complete documentation maintenance program. Disk paging support subroutines enable random or sequential access, single or multiple (up to 16) buffered I/O, optional look ahead buffering and up to 32 kB transfers at the maximum channel rate. **DeAnza Systems,** 118 Charcot Ave., San Jose, CA 95131

Circle 126

INTELLIGENT PLOTTER. This 36″ intelligent digital drum plotter has a speed of 35 ips, rapid acceleration (4G), fine resolution (0.0125 mm) and continuous paper feed. It uses a proprietary servo-motor drive system and two 16-bit μPs. Plot time is indicated on an LCD display also used to report



the results of an automatic self-diagnosis sequence. Other diagnostic tools include built-in test patterns and a single vector operation mode in which vectors can be processed and plotted one at a time. The 3620 is $27,900, optional integral controller is $29,900. **Nicolet Zeta Corp,** 2300 Stanwell Dr, Concord, CA 94520 **Circle 131**

MULTI-CHANNEL VIDEO CONTROLLER. This Multibus-compatible device offers graphics capability as well as alphanumeric character generation on 2 independent displays. Onboard μP performs control and logic functions, including: intermixable text and graphics display, 3 software-selectable character fonts, user-defined custom characters, an addressable cursor, an independently addressed status line, and an on-board date and time clock. With various text-oriented commands, the user may intermix characters of differing sizes on the screen. Communication between the MCV-1023 and the user's system is by a combination of programmed I/O and a shared 2kB block of addressable RAM. Introductory single channel version is $995. **Metacomp, Inc.,** 7290 Engineer Rd, San Diego, CA 92111

Circle 143

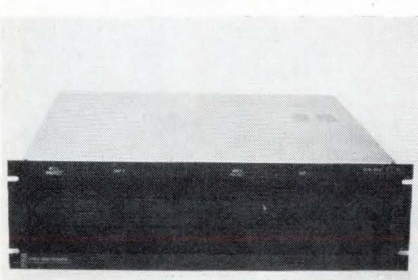
DC POWER SYSTEM. The CS series of multiple output DC power systems provide 425W of power in a 5×6×14″ package. A typical unit provides +5VDC @ 60 AMPS, +12VDC @ 4AMPS, −5VDC @ 1AMP at 50°C and is impervious to overvoltage, overtemperature, overcurrent and brownout conditions. **Switching Power Inc,** 4835 Veterans Hwy, Holbrook, NY 11741

Circle 132

PASCAL COMPILER is based on the ISO standard, has extensions for real-time and multi-tasking operations and can communicate with modules written in other languages. Designed for the Naked Mini 4 (NM4) series of minicomputers, it produces fast-running native machine code that executes under both the NM OS4 and RTX4 (real-time executive) operating systems. It offers local and global variables, floating point, integer and Boolean arithmetic, user data types, structured data types, scalers, multi-dimensional arrays, sets, recursive procedures and functions, dynamic storage allocation and all Pascal loop and control structures. Additions to standard Pascal file I/O include block I/O and random access of disk files. The software and documentation for NM4 Pascal is \$2500/copy. **Computer Automation,** Inc, 2181 Dupont Dr, Irvine, CA 92713 **Circle 175**

REMOTE VIDEO DISPLAY TERMINAL features a commercial keyboard designed to facilitate rapid numeric data entry. The unit includes a 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions, and protect mode. The IQ-120-C uses a Lear Siegler compatible code structure. Expansion options include block mode and hard copy capability with printer interface. Switchable options include parity odd/even, 10- or 11-bit word, and mark/space parity. **SOROC Technology, Inc.,** 165 Freedom Ave, Anaheim, CA 92801 **Circle 128**

FLEXIBLE DISK SYSTEM, for DEC LSI 11/02 and 11/23 based microcomputers, holds up to 1MB of online random storage on each of 2 diskettes. A single dual wide controller contains an on-board bootstrap. Housed in a 5 1/4" rack mount chassis, the Dualdrive is available in the single sided

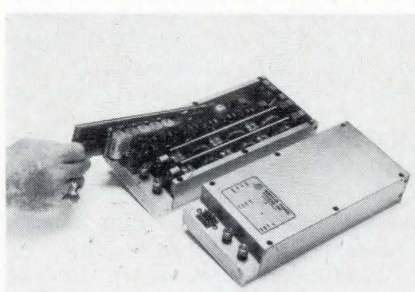


800-1 version with capacity of 1MB (\$3295), or the double sided 800-2 with capacity of 2MB (\$3995). **General Digital Industries, Inc,** 500 Wynn Dr, Huntsville, AL 35805 **Circle 134**

CPU BUFFER CIRCUIT provides elastic buffering between asynchronous CPUs in a parallel-processing network, or between CPU and peripheral circuits. An I/O interface unit, operating with both Zilog Z-Bus- and non-Z-Bus-compatible CPUs, it synchronizes devices that operate independently or at different data rates. The Z-FIO can operate in interlocked or IEEE-488 handshake port mode with empty, full, and wait/request lines for high-speed data transfer. Its 128-byte by 8-bit organization is expandable to any width and cascadable to any depth. The unit generates 7 sources of vectored/nonvectored interrupts. It can manage DMA transfers of up to 1MB/sec and can transfer data to or from memory during every machine cycle. \$39 each/100. **Zilog,** 10340 Bubb Rd, Cupertino, CA 95014 **Circle 144**

300 MB DISK PACK for the Century Data Systems Trident T-300, Ampex DM9300 and other compatible drives is now available. The Scotch 947/300 disk pack, with 10 disks, has 15,352 primary and 133 alternate recording tracks. A pre-recorded servo surface defines track location at 384 tracks/in. Total data capacity is 300 MB. The 20 lb. pack is 7" high. **3M,** Dept. DR80-21, Box 33600, St. Paul, MN 55133 **Circle 133**

SWITCHERS. Using special modules, power densities of 4.5W/in^3 are achieved with MTBFs of 100,000 hr. Sparing of modules rather than power supplies reduce spare parts costs and



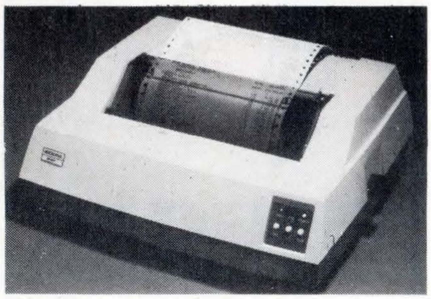
reduce the MTTR. Single or multiple outputs are offered in a wide range of voltages and currents. **Modular Power Systems, Inc,** 8900 Shoal Creek Blvd, #127, Austin, TX 78758 **Circle 179**

CRT CONTROLLER interfaces an 8-bit μP to CRT raster scan video displays. RAM can be addressed in either straight binary or by row or column. It provides refresh alphanumeric information which allow up to 16K characters, with 32 scan lines/character, to be addressed. Other features include up and down scrolling by page, line, or character; programmable vertical sync width; fully programmable display of rows, columns and character matrix; and fully programmable cursor. The R6545-1 is housed in a 40-pin ceramic or plastic DIP, and replaces up to 20 individual TTL components. \$12.70/100. **Rockwell Int'l,** 3310 Miraloma Ave, Anaheim, CA 92803 **Circle 193**

New Products

GRAPHICS FOR TX-80 With bit plot mode each bit arriving at the parallel interface individually controls one of 7 print wires. Utilizing a PROM, GRAFTRAX enables the TX-80 to perform programmable Universal Forms Handling functions. The length of a line feed is software definable in 255 steps of .007″ each. Form lengths are adjustable from one to 255 lines. The size of the print field can be adjusted from one line up to a full page. GRAFTRAX also counts the dots being printed so that if a safe duty cycle is exceeded, it slows the printer down. **Epson America, Inc**, 23844 Hawthorne Blvd, Torrance, CA 90505 **Circle 162**

MATRIX PRINTER/PLOTTER. This unit provides program control up to 240 full 40-character lpm utilizing a graphic 280 × n dot matrix. It takes only 14 seconds to produce full 280-line CRT display in hard copy. Interfaces include parallel; 7-bit ASCII, STROBE, BUSY, ACK and serial; RS



232 with selectable baud rates of 110, 150, 300, 600, 1200, 2400, 4800, and 9600. The print mode is forty 5 × 7 dot matrix characters per line with 96 ASCII upper and lower case characters. Sprinter 40 can be connected with TRS80, Apple II, Atari 800, Commodore Pet and other computers using standard interfaces. **Alphacom, Inc.**, 3031 Tisch Way, San Jose, CA 95128 **Circle 217**

LINKAGE EDITOR AND PASCAL COMPILER are 2 enhancements to the Perkin-Elmer family of 32-bit computers. The OS/32 LINK provides improved response, throughput and speed. It fully exploits the memory architecture of the computer systems permitting programs of up to 16MB to be created in up to 256 individually protected, relocatable segments. An automatic overlay scheme dynamically manages the loading of overlays at run-time without placing constraints on the programmers. An optimizing Pascal compiler is also available. Up to 64 users can share access to the compiler for development and testing of Pascal programs. The Pascal package is $5250 including documentation and 1 year software maintenance. Right-of-copy fee is $525. **Perkin-Elmer**, 2 Crescent Place, Oceanport, NJ 07757 **Circle 189**

LSI-11 TAPE CONTROLLER. The unit provides 9-track NRZ format on a single quad board. PE or dual density is also available with a dual width board. Boards fit into a standard Q-BUS. The TC-151 can mix 9-track NRZ, PE, or dual density tape units in any combination of up to 8 units. A 33-word buffer provides greater flexibility in assigning priorities to the computer. R/W on the fly, for automatic non-stop operation when doing consecutive R/W operations, is accomplished without special software. The TC-151N, with NRZ only, is $2,450. The TC-151P, for PE and NRZ, is $3,150. **Western Peripherals**, Div. of Wespercorp, 14321 Myford Rd., Tustin, CA 92680. **Circle 190**

UNDER $1000 PRINTERS. These 125 cps, 80- and 132-column bidirectional printers support the full upper and lower case 96-character ASCII set in software selectable fonts of 5, 10 and 16.5 cpi on original plus 3 copies. The μP-controlled printers contain a 240 character buffer, with additional data buffers to 3K optionally available in 1K increments. A comprehensive self-diagnostic program in automatically run on power up. The MT-80P Centronics-compatible parallel interface version is $795. The MT-80S serial (RS-232) version is $895. **Micro-tek, Inc**, 9514 Chesapeake Dr, San Diego, CA 92123 **Circle 167**

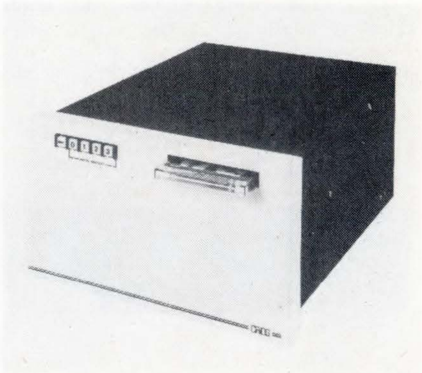
CHANNEL MULTIPLEXER. This family of isolated input expander boards pass microvolt-level input signals while withstanding common mode voltage input levels to ± 250V. The DT1748-EX features 8-, 16- and 24-channel differential input models in which each channel utilizes a reed relay/flying capacitor design for high isolation and low level signal handling capability. These single-card expansion sub-systems are intended for multiple use in expanding the channel capacity of Data Translation's Multibus-compatible isolated analog input systems. In 1-9 qty, the 8-channel model is $595, 16-channel is $995, and 24-channel is $1395. **Data Translation**, 4 Strathmore Rd, Natick, MA 01760 **Circle 186**

LINE CONDITIONERS. A combination noise filter/voltage regulator has been added to the LCC Series of solid state AC Power Supplies. The series is available in ratings from 1KVA to 75KVA with single and 3 phase versions available in all standard power line voltages at 50 or 60 Hz nominal frequencies. They provide ±2% line voltage regulation for +10 −20% input variations as well as common and transverse mode noise attenuation of greater than 80dB. The Conditioners feature internal energy storage adequate to maintain output power for a complete utility outage of one-half cycle (8ms). From $400. **Elgar**, 8225 Mercury Ct, San Diego, CA 92111 **Circle 127**

2K × 8 CMOS RAM is pin compatible with byte organized industry standard EPROMS. It features HMOS speed, NMOS high-bit densities, and CMOS low power dissipation. The HM6116 has an address access time of 120ns. Power dissipation during operation is 180mW, and 100uW during complete standby. **Hitachi America, Ltd.**, 1800 Bering Dr, San Jose, CA 95112 **Circle 176**

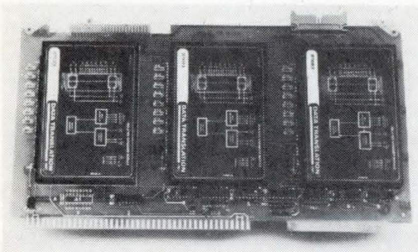
DAISY WHEEL PRINTER, for word processing and small business systems, improves price/performance standards. It incorporates a μP to perform self-test and other control functions. Its modular construction allows instant service through onsite swap of any of the 5 modules. The Stylist 360 can accommodate 100 characters in several sizes, fonts and languages, operates at 17 cps with bi-directional logic seeking, and has a character-wheel with a life of over 50 million strokes. In OEM qty. 100 the Stylist 360 is $820/unit, available in second quarter 1981. **Pertec**, 12910 Culver Blvd, Los Angeles, CA 90066 **Circle 171**

CARTRIDGE TAPE BACKUP. A 17MB cartridge tape backup option is available for the RL01 equivalent HD-11 20.8MB Winchester disk system. The Data Electronics Inc. tape option also facilitates transferability of software between systems. All data is read while writing is still in progress. With its separate read and write heads, and



separate data paths, data is immediately verified. A 32 bit CRC is used for error detection. An ECC circuit allows for reconstruction of an entire block of data, or up to 25″ of tape. **Charles River Data Systems, Inc**, 4 Tech Circle, Natick, MA 01760 **Circle 136**

MATRIX LINE PRINTERS provide optional hard copy output for TI's DS990 computer family. Both use raster/dot-matrix technology to produce high-resolution characters on a 9 × 7 matrix. They print at speeds of 300 and 600 lpm using a 96 character ASCII, 132 column format. They may be used in plotting applications with user-developed software. Model LP 300 is $9,750, LP 600 is $13,750.



Quantity discounts, lease and maintenance rates are available. Deliver in first quarter 1981. **Texas Instruments Inc**, Box 1444, M/S 7784, Houston, TX 77001 **Circle 135**

NEW DESK TOP MICROCOMPUTER. Though smaller and weighing less than a standard office typewriter this new micro contains 64K RAM, 2K Phantom ROM, an 8085A-2 microprocessor and four RS232 asynchronous interface ports. The unit employs most current technology throughout using two BASF mini (5.25″) floppy disk drives (with optional expansion capabilities) having 300K bytes capability of on line storage. The operating systems available with this Micro 210 are fully compatible with the company's current line of microcomputers. When used with the wide range of DTC or other terminals, the Micro 210 is a powerful general purpose microcomputer. $3295. Delivery, 45 days ARO. **DTC**, 590 Division St., Campbell, CA 95008. **Circle 223**

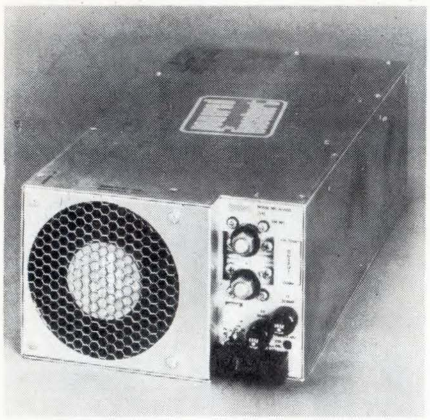
BUS CARD RACKS. Two new Standard Bus Card Racks with Motherboards are designed to accept all STD BUS cards. The QR-8 (accepts 8 cards) and the QR-16 (accepts 16 cards). The fully assembled bus card racks are of cost-effective compact design with low-noise glass epoxy motherboards and printed circuit board connectors. Card spacing on 1/2″ centers with molded card guides containing vents for air circulation provides for a compact card frame with superior mechanical and electrical characteristics and virtually eliminates the possibility of shorts. **Quasitronics, Inc.**, 19 West Water St., Canonsburg, PA 15317. **Circle 208**

THE CP/M HANDBOOK WITH MP/M, by Rodnay Zaks, has been written for all users of the CP/M operating system from clerical personnel who use a computer to enter data or execute specific programs to experienced programmers who want to develop their own programs. The book contains a comprehensive description of all CP/M facilities and resources, instructions for advanced operations, and complete discussions of all versions of CP/M including 2.2, CDOS and MP/M (Multiprogramming Control Program for Microprocessors, an operating system that allows several terminals to be used simultaneously). This 321 pp. book with illustrations is $13.95. **SYBEX, INC**, 2344 Sixth St, Berkeley, CA 94710 **(Inquire directly)**

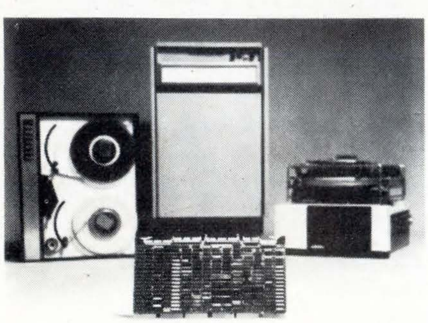
DATA COMMUNICATIONS INTERFACE. This double-buffered program-interrupt interface couples an LSI-11 bus with a serial synchronous modem using EIA RS232-C or RS423 interface standards. Protocols are DDCMP, HDLC, and BISYNC. It enables users to develop X.25 links between LSI-bus-based systems and public packet-switched networks. The DPV11 can be used in both full or half duplex operation. Transmission speed is software dependent and can achieve rates as high as 56 kB/sec. From $550. **Digital Equipment Corp**, Maynard, MA 01754 **Circle 160**

New Products

1500W POWER SUPPLY fits into a standard 5 X 8″ slot in the mainframe cabinet which will allow continued growth without changes in system housing. The first model in the HL series is a +5V, 300A model. The new design reduces cost per watt up to 15% compared to 750W and 1000W switching supplies. It also improves power density: 2.5W/in.^{3} at 5.0V and 2.8W/in.^{3} at 5.75V. The HL 1500 controls output voltage within 1% during a 25% change in load and recovers to "flat" output in 0.5ms. Up to 4 supplies, linked with a control cable, can share up to 1200A for a total power output of 6 kW. The HL 1500 is $1220/unit, $960/100. **Boschert, Inc**, 384 Santa Trinita Ave, Sunnyvale, CA 94086 **Circle 173**

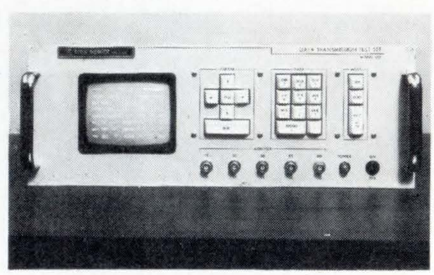


DISK/TAPE CONTROLLER. These multifunction disk and tape controllers attach removable pack or fixed Winchester SMD disk drives and "start/stop" or "streaming" 1/2″ formatted tape drives. They support 2MB/sec disk transfer rates and 320 kB/sec tape transfer rates. They attach up to 4 SMD disk drives and up to 8 formatted tape drives without modifying the operating system software. A dual bipolar μP design simultaneously controls the CPU, disk, and tape interfaces. Separate buffering for disk (3 sector) and tape (64 byte) allows simultaneous disk and tape transfers at full speed. The Spectra 20 (for DGs NOVA and ECLIPSE) is $5100/unit, $3900/25. The Spectra 21 (for the PDP-11) is $5800/unit, $4500/25. **Spectra Logic Corp**, 2316 Walsh Ave, Santa Clara, CA 95051 **Circle 183**

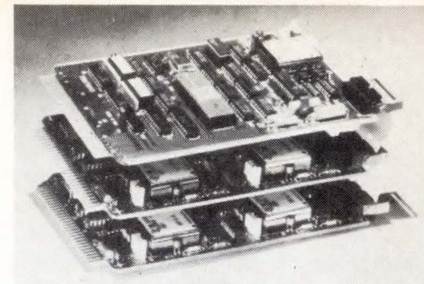


UNIT PROCESSORS. Two new unit processors with cache memory have been added to the 1100/60 family. The 1100/60 systems are the first large-scale general purpose computers to implement instruction execution with multiple μPs. Both the new models have 8 kB of cache memory and are field upgradable to model H1 and H2 unit processors. The 1100/60 E1 central processing complex with 2MB of main storage, 8 kB of buffer storage, one I/O processor and one System Support Processor with system and maintenance consoles is $518,975. Five year lease is $11,342/month including maintenance. The 1100/61 E2 is $555,545. Lease price is $12,139/month including maintenance. Delivery in first quarter 1981. **Sperry Univac,** Box 500, Blue Bell, PA 19424 **Circle 141**

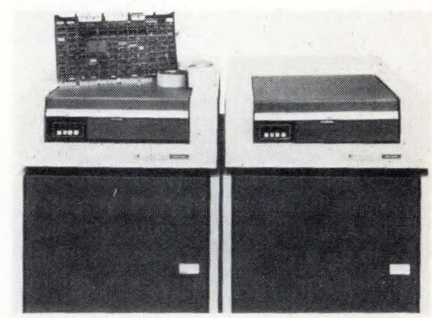
DATA TRANSMISSION TEST SET tests and evaluates systems operating from 10 bps to 100 Mbps. Model 607 measures bit errors, bit error rate, block errors, second errors, block and second thru-put and presents the results on a formatted 5″ CRT display. A printer may be connected to this bus for hard copy of test results and unit setup parameters. Self diagnostic capability tests the data paths and verifies the proper operation of all control and operator functions. **Aydin Monitor Systems,** 502 Office Center Dr, Ft. Washington, PA 19034 **Circle 180**



MAGNETIC BUBBLE MEMORY. The single-board memory systems are supplied with 1, 2, 3 or 4 92K-bit TIB0203 bubble memories for 11.5K, 23K, 34.5K or 46K bytes of storage. The TBB7090 contains all necessary support circuits including custom controller. The TBB7091 is an expansion system. Two TBB7091 boards can be used with one TBB7090 board. Both are available in two temperature ranges, 0°C to 50°C and 0°C to 70°C. They are bus and timing compatible with Pro-Log and Mostek STD-BUS series. They feature lower power operation, 4 ms access time, and 50K bits/sec data transfer rate. From $610 to $1580. Also available are two kits which provide the magnetic bubble memory and custom integrated circuits required to layout and assemble a complete 92K-bit bubble memory system. The TIBK091 and the TIBK090 kits are from $151 to $191. **Texas Instruments Inc**, Box 225012, M/S 308, Dallas, TX 75265 **Circle 182**

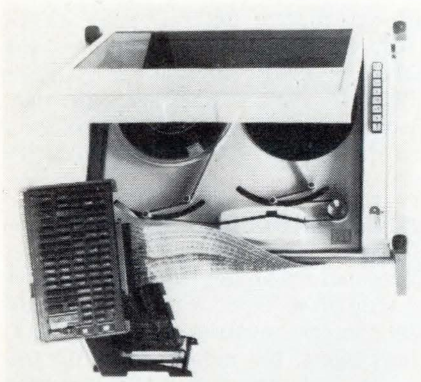


MULTIFUNCTIONAL SMD CONTROLLER. An array of computer subsystems feature a high transfer rate, transparent ECC, and multiword transfers. The PM-DC1100 is a single hex-wide, μP-based controller that supports a variety of drives with SMD-type interfaces. When combined with the PM-FD11/G Winchester disk drive, it becomes the PM-FS11/G Winchester disk subsystem. Using a multidrive interface chassis, a single PM-DC1100 controller supports up to eight 25.3MB drives for over 200MB of data storage. The PM-FS11/G is $7442/unit. The PM-DC1100 is also an integral system component in the family of PM-DSA11 removable disk cartridge and disk pack subsystems which provide unlimited off-line storage. **Plessey Peripheral Systems,** 17466 Daimler Ave, Irvine, CA 92714 **Circle 194**



23Mbit TAPE SYSTEM is designed for severe environment industrial, military and aerospace applications. The basic unit consists of a compact drive module coupled to a sealed removable tape module. It has 23 Mbit of storage at 1600 bpi on 300 feet of 1/4″ magnetic tape. The unit has bidirectional R/W capability on 4 tracks with a 192K bps transfer rate. Operating temperature is −40°C to +71°C. The SETS-1 recorder is $7200 in quantity. **EMM Sesco,** 20630 Plummer St, Chatsworth, CA 91311 **Circle 158**

DIGITAL RECORDER. This IBM/ANSI compatible magnetic tape system is plug-compatible with the Intel Multibus. INTL-1050 consists of a single card tape controller which connects to the IDT Model 1050 formatted tape transport. The complete subsystem uses a dual-density 9-track, 45 ips, tape transport for either 800 cpi (NRZI) or 1600 cpi (PE) providing over 40 MB of data storage. Error recovery, interrupts, status and diagnostic primitives are resident in 4K on-board EPROM. The INTL-1050 master



system consisting of the Intel Multibus compatible tape controller, a dual (NRZI and PE) formatter and the Model 1050, 1/2″ magnetic tape transport, is $7,750 with additional slave daisy-chain drives available at $4,250 each. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117 **Circle 177**

SINGLE CHIP μP WITH BASIC. This bus-oriented single-chip 8-bit microcomputer executes a high-level language called NSC Tiny BASIC directly on-chip. The 40-pin INS8073 incorporates both on-chip RAM (64 bytes of scratchpad memory) and on-chip ROM (2.5 kB on which the Tiny BASIC interpreter is stored). It contains an 8-bit arithmetic logic unit, an 8-bit accumulator, an 8-bit extension register, plus 4 internal 16-bit registers. It has 16 address lines and 8 data lines, and separate Read and Write strobe outputs. The INS8073 is $26/100, $40 in single quantity. **National Semiconductor,** 2900 Semiconductor Dr, Santa Clara, CA 85051 **Circle 130**

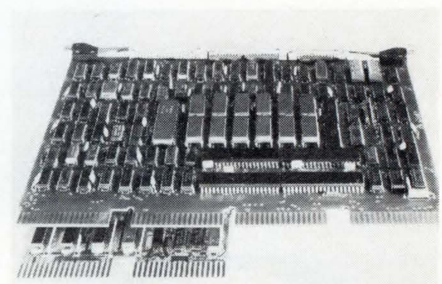
NEW 6800/6809 μP DEVELOPMENT SYSTEMS. This development system series for 6800/6809 microprocessors, provides up to 64KB of RAM and 2MB of disk storage. Configured with a 1920-character CRT and either dual 5 1/4″ or 8″ disk drives, the new "Scoutsystem" line incorporates Smoke Signal's "Hunter" shortcut debug package allowing memory, register and stack contents to be inspected and changed. A MacroAssembler uses standard Motorola assembler directives, and provides a relocatable code for assembling several modules separately. An additional conversion package permits files generated under MDOS to be read by SSB's DOS68 or DOS69 and vice versa. A text editor and text processor are also available. Prices for the "Scoutsystem" range from $5,700 to $7,745 including CRT and standard software. Delivery, 30 days ARO. **Smoke Signal Broadcasting,** 31336 Via Colinas, Westlake Village, CA 91362 **Circle 196**

SWITCH PRODUCT GUIDE. This 6-page brochure (# 1-0074C) describes Digitran's commercial and industrial digital switches. It contains pictures, descriptions and basic data of 10 thumbwheel and lever switches. A table shows the availablity of 30 features or options for each model. **Digitran Co.,** 855 S. Arroyo Pkwy, Pasadena, CA 91105. **Circle 188**

10 BIT D/A CONVERTER. The unit has a high speed, μP compatible input register, designed for interfacing with even the fastest μPs. It guarantees monotonicity and ±1/2 LSB linearity over the 0°C to +70°C or –55°C to +125°C operating temperature range.

Most available monolithic 10 bit D/A's have slow CMOS latches and are incomplete, requiring external references and external output op amps for normal operation. The MN3040 has a fast TTL latch with internal reference and output on amp. $65/100, 4 weeks ARO. **Micro Networks Co,** 324 Clark St, Worcester, MA 01606. **Circle 204**

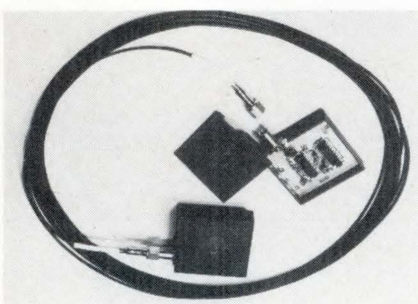
LSI-11/PDP-11 TAPE CONTROLLERS operate with standard tape drives and support any combination of 7- or 9-track, NRZI, or dual density drives. Up to 4 drives can be daisy-chained to one controller. They provide 64 bytes of data buffering. In the NRZI mode, 7-track drives operate with the controllers at 200, 556 or 800 bpi, and 9-track drives at 800 bpi in NRZI or at 1600 bpi in the PE mode. They incorporate an integral 16-bit bipolar μP with tape drive speeds to 125 ips. For NRZI mode one quad board is required, and for PE mode, a dual size board is added. The



single quad T04 or T34 is $2600, the dual density version (a quad plus a dual board) is $3300. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512 **Circle 170**

New Products

μP-CONTROLLED INTERACTIVE TERMINAL replays up to 7680 characters (4 full pages) of previously-displayed data. The Model 14 features trailing-space and -line suppression, and limited block-mode capability. Transmit and print terminator codes may be selected, stored and transmitted to the computer or printer at the desired points. Transmission stop codes may also be selected. Other features include a function memory of 1920 characters reserved for up to 32 programmable functions (24 on dedicated keys), programmable I/O and peripheral data rates, programmable tabs and cursor symbol selection. Model 14 is $1890, quantity discounts available. **Teleray,** Div. of Research Inc, Box 24064, Minneapolis, MN 55424 **Circle 145**



FIBER OPTIC COMMUNICATION LINK. The kit provides TTL transmitter and receiver modules which permit installation of a simplex link in excess of 1000 meters. The component contents of the LINK II kit are: a transmitter module, the MFOL02T; a receiver module, the MFOL02R; and, 10 meters of fiber cable, pre-terminated with appropriate matching AMP connectors, to demonstrate fiber optics capabilities. These components are supplemented by complete component specifications and extensive applications literature. Features of this system include: efficient die to fiber coupling; field replaceability; RFI/EMI shielding; elimination of ground loops; electrical isolation; and, noise immunity. The LINK II kit is $124.99. **Motorola,** Semiconductor Products Inc, Box 20912, Phoenix, AZ, 85036 **Circle 166**

SOFTWARE DIRECTORY. This 80 pp. booklet is available at no charge to computer users interested in the extensive range of available software for Harris 24 and 48 bit computers. It features over 150 different software items. **Harris Computer Systems,** 2101 West Cypress Creek Rd, Ft. Lauderdale, FL 33309 **Circle 157**

MESSAGE SWITCH for DGs Nova line of minicomputers is designed for line concentration and/or front ending larger communication systems. Its throughput is over 20 messages/sec sustained for messages averaging 500 characters. Its software modularity allows the SC/80 switch to accommodate expanded protocol support and expanded throughput capacity. The stand alone operating system supports a variety of disks and can be configured for 16-128 async or sync lines. The total system including hardware is from $40,000 to $60,000. **Conversational Systems Corp,** 132 W. 31 St, New York, NY 10001 **Circle 169**

CHANNEL ADAPTER. This IBM Graphics Front End Processor, based on the LSI-11, can exchange data with both raster and vector graphic systems at data rates up to 1MB/sec. It appears as any of the standard IBM peripherals by control unit emulation software. It can interface with any graphics system that has a PDP-11 or LSI-11 interface capability, or an 8/16-bit parallel DMA interface or serial interfaces are available for non-DEC systems. Interfaces are also available for optional control devices. Each device attached to the 8911 can be assigned one or more of the 256 possible subchannel addresses. Its internal LSI-11/02 or optional LSI-11/32 CPUs can perform message switching, data manipulation and command translation. **Austron Data Systems,** 1915 Kramer Lane, Austin, TX 78758 **Circle 213**

APPLE II VIDEO TAPE CONTROLLER. The system hardware/software permits precise video tape positioning. The interface contains a video/audio switcher to allow alternate display of computer-generated or taped video on a single monitor. The system will control industrial type VHS, Beta, and 3/4″ video recorder/players. No modifications to the computer or VTR are required. The C.A.V.I. (Computer Assisted Video Interface) is applicable to "Interactive Video Instruction". A student views lesson segments on video tape, then responds to questions asked by the computer. The C.A.V.I. Model 400 Interface is $495. A Computer Assisted Instruction (C.A.I.) software system is available on a separate disk for $295. **BCD Assoc, Inc,** 1216 N. Blackwelder Ave, Oklahoma City, OK 73106 **Circle 149**

ROM STIMULATOR, residing in the Apple II-based development system, consists of a hand wire wrapped plug in a 2.75″ x 7″ card. This card contains 2 kB of static RAM memory located in Hex C800 of CFFF in the Apple II memory map. It also contains the logic necessary to automatically switch control of the address and data bus from the Apple II to the Lamar SuperKim (target) ROM sockets. $395. **Lamar Instruments,** 2107 Artesia Blvd, Redondo Beach, CA 90278 **Circle 153**

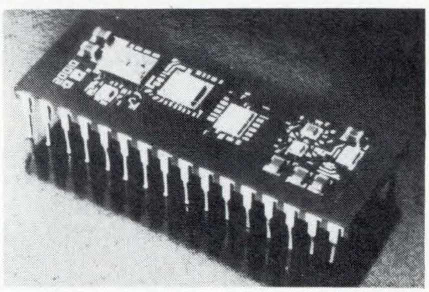
BAR CODE LIGHT PEN reads low density bar code labels, including dot matrix printed labels. Scan velocity can be up to 30 ips. A low power LED light source above the ball irradiates the label. The LED provides good signal-to-noise ratio when reading non-carbon based inks. Low density source printed UPC/EAN symbols also can be read successfully. Output is an analog signal with a free air to white paper differential of approximately 125 mV. The Model 1241 Ruby Wand is available in OEM quantities from $160 to $286. **Interface Mechanisms, Inc.,** Box N, Lynnwood, WA 98036 **Circle 148**

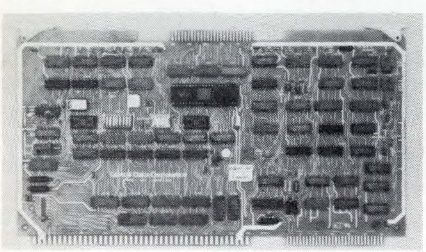
FLOPPY DISK CONTROLLER is compatible with the DEC RX02 floppy disk system. All circuitry is contained on one dual height card which plugs directly into a standard LSI-11 backplane and interfaces through a 50 conductor ribbon cable to any Shugart compatible drive. The card features a transparent firmware bootstrap which automatically loads either single or double density diskettes, IBM 3740 formatting capability, alternate address and vector selection, jumper selectable four-level device interrupt priority, power fail protection, write current control signal, double sided control signal, and write precompensation for reduced error rates. The MXV21 is $1260/unit. **Micro Development Assoc**, 2192 Martin, #210, Irvine, CA 92715

Circle 210

12-BIT A/D CONVERTER. Various models of this unit convert in 6, 4.5 and 3 μs. Key specifications for all grades include no missing codes over the operating temperature range of 0° to +70°C, maximum non-linearity if ±0.012% low gain temperature coefficient of ±30ppm/°C maximum, and a typical power dissipation fo 775mW. Power requirements are ±15V and +5V, ±10%; a "Z" model is also available for ±12V supplies. The AD578 requires no external components. Input scaling resistors allowing input voltage ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Short cycling is possible for applications requiring faster conversion speeds at lower resolutions. From $85/100. **Analog Devices Semiconductor,** 804 Woburn St, Wilmington, MA 01887

Circle 163





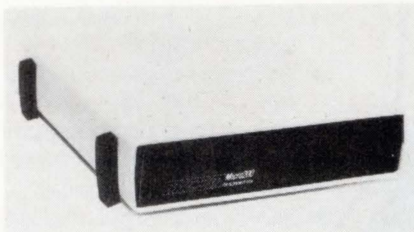
FLOPPY CONTROLLER. This Multibus double-density floppy disk controller board allows the user to hook from 1 to 4 double-density standard-size floppy drives to a Multibus system. It uses the industry standard FD1791 controller and is adaptable to single- and double-sided drives. All write data is pre-compensated for reliability. All data transfers to and from memory are done by DMA and logic is included for full multi-master capabilities. **Central Data Corp,** 713 Edgebrook Dr, Champaign, IL 61820 **Circle 146**

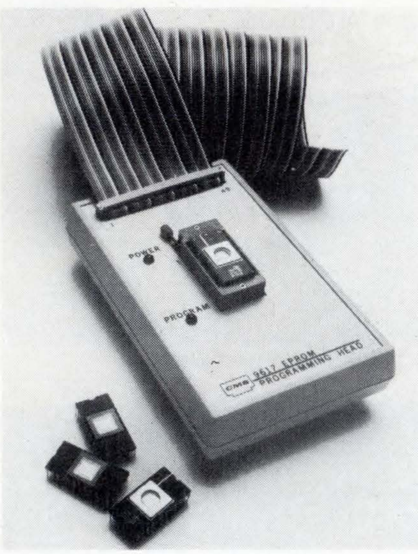
A/D MODULE digitizes up to 8 separate differential analog inputs from devices such as pressure and temperature transducers. The A/D module complements G&L's 6800-based GL868 microcomputer product line. Card size is the standard 4.5 × 6.5". The module features 12-bit resolution and a variable gain from 2 to 1000. The conversion time is 25 μs for low gains and up to 320 μs for high gains. Sockets are provided for additional filtering, gain, or attenuation. Four to 20 ma signals are easily handled by the module. **Giddings & Lewis Electronics,** 666 S. Military Rd, Fond du Lac, WI 54935

Circle 156

New Products

PORT CONCENTRATOR allows one computer port to communicate with up to 16 channels on a remote Micro-800 Data Concentrator using a simple async or sync protocol. Some user programming is required to communicate with the Port Concentrator, but the Micro 200 offers a simpler interface. $1,000/unit, 60 days ARO. Quantity and OEM discounts available. **Micom Systems, Inc.,** 9551 Irondale Ave, Chatsworth, CA 91311 **Circle 152**





EPROM PROGRAMMING HEAD, with Support Firmware, is a utility module for use with M6800 systems. It programs single-voltage EPROMS from data resident in the system memory. The 9617 is designed to derive all signals and power directly from the parallel I/O connector, P3, of any CMS single board microcomputer. It can also be interfaced to any system which provides two unbuffered MC6821 Parallel Interface Adapters and a source of +5 VDC. The 9617 is intended for tabletop use and is connected to the system I/O port by a 50 conductor flat cable. Single voltage EPROMS of either 2K by 8 or 4K by 8 configuration can be read, tested from erased condition, programmed and verified. Data in memory can be inspected and changed prior to programming. ($250). **Creative Micro Systems,** 11642-8 Knott St, Garden Groven, CA 92641 **Circle 164**

LARGE SCREEN DISPLAY. The 15″ diagonal screen displays 33 lines of 132-column text, (4,356 characters). This represents a full-width, half-page in length ot line printer output. An optional screen buffer memory stores an extra 33 lines of text or a full page, and also provides both up and down scrolling. Other display features include direct cursor positioning, 7 cursor control functions, line erase, screen erase and character repeat keys. The 5210 has 96 upper and lower case ASCII characters plus 32 special graphics characters. The detached keyboard has integral 15-key data entry pad and 18 function keys. The display's communications interface has 8 switch-selectable speeds, from 300 to 38,400 bps. The display also has an RS-232-C port so it can be interfaced to a slave printer. The 5210 is $4500, 150 days ARO. **Data General,** Rte. 9, Westboro, MA 01581 **Circle 151**

EXPANDABLE μC SYSTEM. This Z80A-based microcomputer system features two 8″ double density, floppy disk drives with 6 status indicators each to verify major functions, while aiding operation, programming, and debugging. Disk capacity is 1MB (IBM format, double density), and main memory provides 64kB. Each drive has a write protect switch, and 2 additional disk drives can be added. Model 6100 is compatible with the CP/M version operating system, IBM 3740 single-density format, IBM 2D double-density format, S100 BUS, and RS232C. Four slots in the backplane can accept Modems, graphics, additional I/O and memory. Model 6100 is $4950. **Innotronics Corp,** Brooks Rd, Lincoln, MA 01773 **Circle 216**

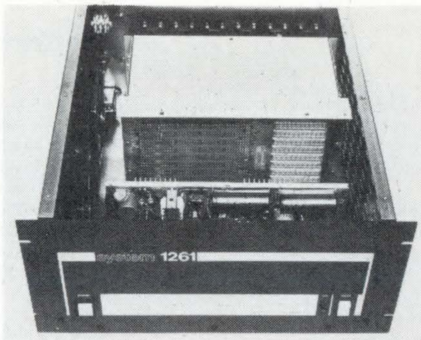
EPROM PROGRAMMER. The unit provides 16kB of RAM, a Z-80 microcomputer, a 16 digit 7 segment LED display, and a keyboard with 15 command and 20 data keys. Capabilities include loading contents of master ROM into the RAM buffer, programming the contents of RAM into EPROM, displaying content of EPROM and/or RAM, block updating RAM, and block transfer of data between RAM sections. Users may execute or debug machine language programs in Z-80 or 8080 code, display the contents of registers, update register contents, designate up to two breakpoints, and activate a built in "micro-speaker" under software control. Model PKW-5000 is $1595. **Energy Electronic Products Corp,** 6060 Manchester Ave, Los Angeles, CA 90045 **Circle 165**

UNIVERSAL μP DEVELOPMENT STATION. The Phoenix 1 comes with a μP-based computer and 48K RAM, a 12″ CRT, full ASCII keyboard and keypad, three 5 1/4″ minidisk drives (306 kB total), two RS232C interfaces for peripherals, and assemblers for a variety of μPs. ($5495). Software support includes a Pascal Compiler which runs under the AMIX operating system. It includes extensions for business programming as well as system level work. Separate modules written in assembly or Fortran-77 can be linked with AMI-Pascal programs. It requires 48K memory, dual floppy disks and a CRT terminal on the host system. AMI-Pascal on floppy diskette is $275 including a reference manual and 6 month software maintenance. **American Microsystems, Inc.,** 3800 Homestead Rd., Santa Clara, CA 95051 **Circle 218**

CRT TERMINAL features full-screen editing capability. It contains a 24 line by 80 character/line display plus integral 73-character ASCII keyboard and 14 dedicated full-screen edit function keys. It has an RS232C interface with 7 selectable baud rates from 300 to 19.2K, and provides instant screen verification of text editing changes. Features include cursor positioning, 2-speed auto-repeat cursor movement, overtype, character or line insertion/deletion, scrolling and windowing. The CDP18S040 COSMAC Data Terminal is $1195 in 2 versions: 115V, 60 Hz or 220V, 50 Hz. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876 **Circle 150**

DATA-COMM PRODUCTS. This new product line includes a variety of sync and async limited distance modems; terminal, port, and modem sharing devices; and modem eliminators. Designed to reduce network costs, the 6000 Series provides the user with reliable, ruggedly constructed products. A free catalog is available. **International Data Sciences, Inc.,** 7 Wellington Rd, Lincoln, RI 02865. **Circle 159**

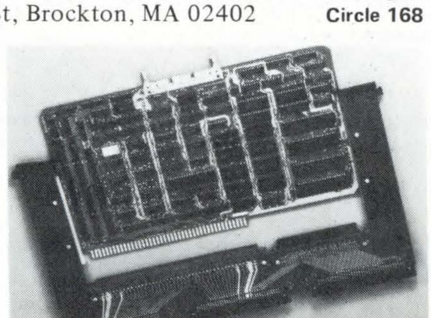
MULTIBUS COMPATIBLE CHASSIS. Through the segmented part number the user specifies a keylock or alternate action front panel power switch, connector cut-out or blank back panel, 4 output switching regulator power supply, 11 slot card cage, and rack mount or stand alone chassis. Completely assembled, the System 1261 OEM chassis starts at $1,600 for a 175W power supply and vary with power supply output requirements. **Prototek, Inc., Box 46512, Cincinnati,** OH 45246 **Circle 155**



BIT-DRIVER MODEM. This metallic-conductor Bit-Driver short-haul modem is part of an RS-232C-compatible standalone data transmission system. It provides asynchronous simplex and duplex data transmission at speeds from dc to 56K bps. Recommended for use in clean electrical environments, its operating range extends from 5000 to 15,000 ft. Model 9338 is $195. **Belden Corp.,** 2000 S. Batavia Ave., Geneva, IL 60134 **Circle 147**

CARD RACK which holds up to 24 STD BUS cards, bolts into an EIA standard 19″ rack. It provides 16 card slots on 1/2″ centers and 8 card slots on 1″ centers. Its improved motherboard reduces cross-talk and reduces noise on signal lines. The motherboard will operate at a free air temperature range of −15°C to +125°C. The CR24A is $220 to $295 depending on quantity. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940 **Circle 154**

INTERFACE PANEL allows adaption of a Multibus compatible board to the 326 Class Vertical or Horizontal Racks. This gives the flexibility to add extra logic on the wire wrappable panels designed for the rack selected. Packaging problems are solved with a wide selection of different size racks and a variety of backplanes. $99.50 each, 1-24. **Mupac Corp,** 646 Summer St, Brockton, MA 02402 **Circle 168**



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Product Index

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New Products

NEW CRT CONTROLLER. A low-priced CRT controller has many features. These include: dual row buffers, on-chip attribute generation and fully programmable screen and character formats. New chip reduces number of ICs usually required for a CRT display subsystem from more than 100 to less than 20. CRT displays are found in a wide range of systems, but the most cost-sensitive applications are those for small systems, such as "dumb" terminals. It is this applications area for which Intel has designed the 8276. Samples of the 40-pin 8276 now available. Production quantities available first quarter of 1981. $15 each in quantities of 100. **Intel Corp.**, 2625 Walsh Ave., Santa Clara, CA 95051. **Circle 214**

GRAPHICS FOR TI 810 PRINTER. This graphics board provides graphics and custom character print capability in addition to the 910 printing, format and forms control features. It plugs into the printer's line buffer option slot, contains a RAM buffer and ROM that controls the 810 processor for bi-directional printing and plotting functions. Two plot modes are available for hardcopy of raster scan data or information mapped in dot-matrix memory. Users may also define and program a 75 character software font for custom uses. Data is transmitted on the RS232 serial or optional TI parallel interface at 9600 baud. **Analog Technology Corp**, 15859 E. Edna Place, Irwindale, CA 91706 **Circle 224**

TELETYPE EMULATOR, PROGRAMMER UTILITIES FOR HP MICROS. Important new software, including utilities for data communication and teletype emulation is now offered for HP's Series 80 personal computers. Enhanced functions and commands, with the emphasis on statistics, math and string manupulation, are also available as programmer utilities. Other utilities let the programmer redefine the CRT, keyboard, and internal printer operation. Teletype emulation and other utilities are available now for the HP-85, and will be usable on other HP Series 80 personal computers when they are introduced. The teletype emulator and other programmer utilities come individually on a tape cartridge or disk. Price for one tape cartridge is $29; $12 for subsequent units. Disks are $21 for first one; $12 for others. Prices include literature that explains what the program does and how to call it. INQUIRIES MANAGER, **Hewlett-Packard Co.**, 1507 Page Mill Rd., Palo Alto, CA. 94301. **Circle 209**

MOSTEK'S 64K DYNAMIC RAM. Mostek has entered the 64K Dynamic RAM market, with its MK4164. The Mostek 64K incorporates several new design and fabrication technologies which make it different from a scaled version of the 16K RAM design.

For example, use of polysilicon instead of diffused bit lines allows a 50% increase in signal to the sense amplifier. By relocating the bit lines to a different level, the distance between adjacent capacitors is reduced to 3 microns, a savings of 6 microns compared to the diffused bit line approach. This space savings permits an increase of the storage capacitor size to 75% of the total cell area. Multiplexed address inputs, pioneered by Mostek, permit the MK4164 to be packaged in a JEDEC-approved 16-pin plastic DIP. The device features single +5 volt supply operation, maximun power of 300mW active and 20mW standby, and 150ns access time. The price for the MK4164-20 in 100-piece lots is $59.99. **Mostek Corp.**, 1215 W. Crosby Rd., Carrollton, TX 75006 **Circle 234**

METRIC ELECTROSTATIC PRINTER/PLOTTER. New printer/plotter produces a resolution of 100 dots/cm (254 dots per inch) compared to the conventional 200 dots per inch. Quadramet 9424 Model plots at 2.45 cm/sec (1.0 inch) at a plot width of 59.51 cm/sec (23.43 inches); the Quadramet 9436 plots at 1.27 cm/sec (0.5 inch) across an 89.59 cm (35.27 inches) plot width. Metric electrostatic printer/plotters, elimanate costly and time consuming process of metric conversion to English dimensions. Deliveries scheduled for January, 1981. Quadramet 9424 is $29,500; the 9436, $39,800. **Benson-Varian, Inc.** 385 Ravendale Dr., Mountain View, CA 94043. **Circle 244**

INTERACTIVE GRAPHICS TERMINAL. Dynagraphic Series II has a bright, high-resolution (2048 X 2048), 19" vector refresh display. For CAD/CAM and engineering applications, the stroke-drawn display terminal offers a cost competitive alternative to lower-resolution raster displays. It generates legible displays of complex engineering designs. Local terminal processing permits rapid, dynamic user interaction, such as selective erasure/continuous on-screen dragging of complex images.$8,840. Imlac Corp, 150 A St, Needham, MA 02194. **Circle 203**

WIRE STRIPPER. ST-300 has adjustable stop for consistancy in wire strip lengths. Strips 14 to 22 AWG solid/stranded wire cleanly and quickly. Strips Kynar, vinyl, polyethylene, rubber, neoprene, and irradiated vinyls. $9.95. **O.K. Machine And Tool Corp**, 3455 Conner St., Bronx, N.Y. **Circle 200**

μP-CONTROLLED CASSETTE RECORDER. The μP-based control system continuously monitors and regulates tape speed, tension, and assures uniform start/stop profiles. Sensing is provided for tape leader, load point, early warning, cassette in place, side A/B, and write protect. Specifications include: 5.6 X 10^6 bits, unformatted storage capacity; 24,00 bps data transfer rate; 800 bpi packing density; serial NRZ and clock data interface; 30 ips, 60 ips search, 120 ips slew tape speed. Options include read-after-write, 8-bit parallel ANSI formatter, RS-232C async interface and IEEE-488 parallel interface. The 6440 Raycorder II is $545/unit; $335 in OEM qty. **Raymond Engineering Inc**, 217 Smith St, Middletown, CT 06457 **Circle 225**

6800 DIAGNOSTICS AND DISK REPAIR. The memory diagnostics contain zeroes and ones test, random pattern test, walking bit tests, dynamic *ram* dropout test and convergence test. Disk repair contains utilities which operate on a FLEX-formatted diskette. Included are 3 diagnostic utilities which report unreadable sectors and structural inconsistencies among the files on the diskette, 2 utilities for recovering data when the directory on the diskette is not readable and a utility to remove bad or intermittant sectors from the free space. $75.00. 5" or 8" diskette. A comparable package for the 6809 is available. **Technical Systems Consultants, Inc.**, Box 2570, W Lafayette, Indiana, 47906. **Circle 201**

SINGLE BOARD MULTIPLEXER The MX-4 multiplexer is offered as an economical and highly reliable microprocessor based multiplexer. It permits up to 4 asynchronous data links to be transmitted over a single synchronous composite channel with asynchronous option.

The MX-4's single board design includes switch programmable character formats for fast and easy installation, character-oriented line protocol, immediate character transmission and a composite channel loopback switch for easy self-testing. The full duplex channel can operate at speeds up to 9600 bps. **Gandalf Data, Inc.**, 1019 S. Noel Ave. Wheeling, IL 60090. **Circle 207**

NEW SBCs. A powerful microcomputer card (QCB-9) based on the 6809 8 bit microprocessor. Includes the following on-board features: Floppy Disc Controller, RS-232C Serial Communication Interface, two eight bit parallel ports, up to 24K bytes of EPROM space, or 6 K bytes of RAM, flexible I/O port addressing, S-100 Bus structure, on board power regulation. **Logical Devices Inc.,** 1525 NE 26th St., Ft. Lauderdale, FL 33305. **Circle 233**

NEW I/O PROCESSOR. This new I/O Processor (Model IOP) provides multiprocessor capability for Cromemco's S-100 bus, microcomputer systems. The new IOP is a true single-card computer with a fast Z-80A μP, 16K bytes of RAM and up to 32K bytes of PROM. The IOP can be used either alone or with other IOP cards as a satellite processor on the S-100 bus. The IOP can also be used to interface the S-100 bus processor and a set of peripherals. These peripherals are controlled over a new bus, called the C bus, which operates independently of the S-100 bus. Devices such as Cromemco's QUADART serial I/O card can be interfaced through the C-bus connector on the top edge of the IOP card. The Model IOP card is available assembled and tested for $695. **Cromemco, Inc.,** 280 Bernardo Ave., Mountain View, CA 94043. **Circle 212**

SWITCHER 500-V/200-V HEXFETs provide designers of switchers destined for Europe (210-220V line input). The 450-V devices offer designers of switching supplies an extra voltage margin over 400V devices for use in equipment subject to noisier electrical environments. **International Rectifier,** 233 Kansas St., El Segundo, CA 90245. **Circle 215**

1.6 MBYTE OPTION FOR THIS MICRO. GNAT Computers is offering 1.6 MB of on-board disk storage for its SYSTEM 10 microcomputer. This extended storage is achieved through addition of a double tracking feature to its double-sided, double-density, 5 1/4 inch disk drives. Other features: a Z80 μP; 65KB RAM; DMA controller; interrupt controller and three serial I/O channels. The system can be optionally configured with an AM9511 or AM-9512 arithmetic processor, Real Time Clock and IEEE 488 GPIB interface. The OEM quantity 12 price of System 10 with the 1.6 MB option is $5770. Delivery is stock to 60 days. **GNAT Computers Inc.,** 7895 Convoy Ct., Bldg. 6, San Diego, CA 92111. **Circle 228**

MULTI-FUNCTION LSI MODEM. This multi capability modem can communicate on a variety of networks. It can operate at various baud rates (0 to 1200 characters per second) and functional modes. These modems are implemented with custom LSI chips into a single 2 1/4″ X 2 3/4″ module with full communications capability. The modular modems, used for building block applications, can be mounted directly on printed circuit boards or to any flat surface within most computers or terminals. Seven functional modules that offer complete LSI based receiver and transmitter functions are available. **Novation Inc.,** 18664 Oxnard St., Tarzana, CA 91356. **Circle 206**

WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60/S4 STANDS ALONE.

Magnavox combines the superior display and control features of the plasma-panel-based Orion-60 terminals with the powerful S4 Micro-Computer System.

The result is a stand alone graphics system that allows you the freedom to develop a wide variety of graphics application and development programs—while maintaining complete control over program storage, program-generated data, library routines and other facilities.

The Orion-60 display terminal offers full graphics with floppy-disc storage, as well as optional rear-projection functions. It lets you create your own displays and enter data by simply touching the screen with your finger. So you can program your own character sets and generate vectors of any length to absolute coordinates. And because the Orion-60 is plasma-based, you'll get bright, high-contrast images free of jitter or distortion.

The S4 Micro-Computer has system software with development capabilities that are as good or better than those found in many larger computer systems.

Features include CP/M* 8080 system utilities, Fortran with 32K RAM, and a full range of graphic utility routines including window, zoom, sub-image movement and rotation.

The Orion-60/S4.

For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 South Coliseum Boulevard, Fort Wayne, Indiana 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

**CP/M is a trademark of Digital Research.*

Circle 53 on Reader Inquiry Card

New Products

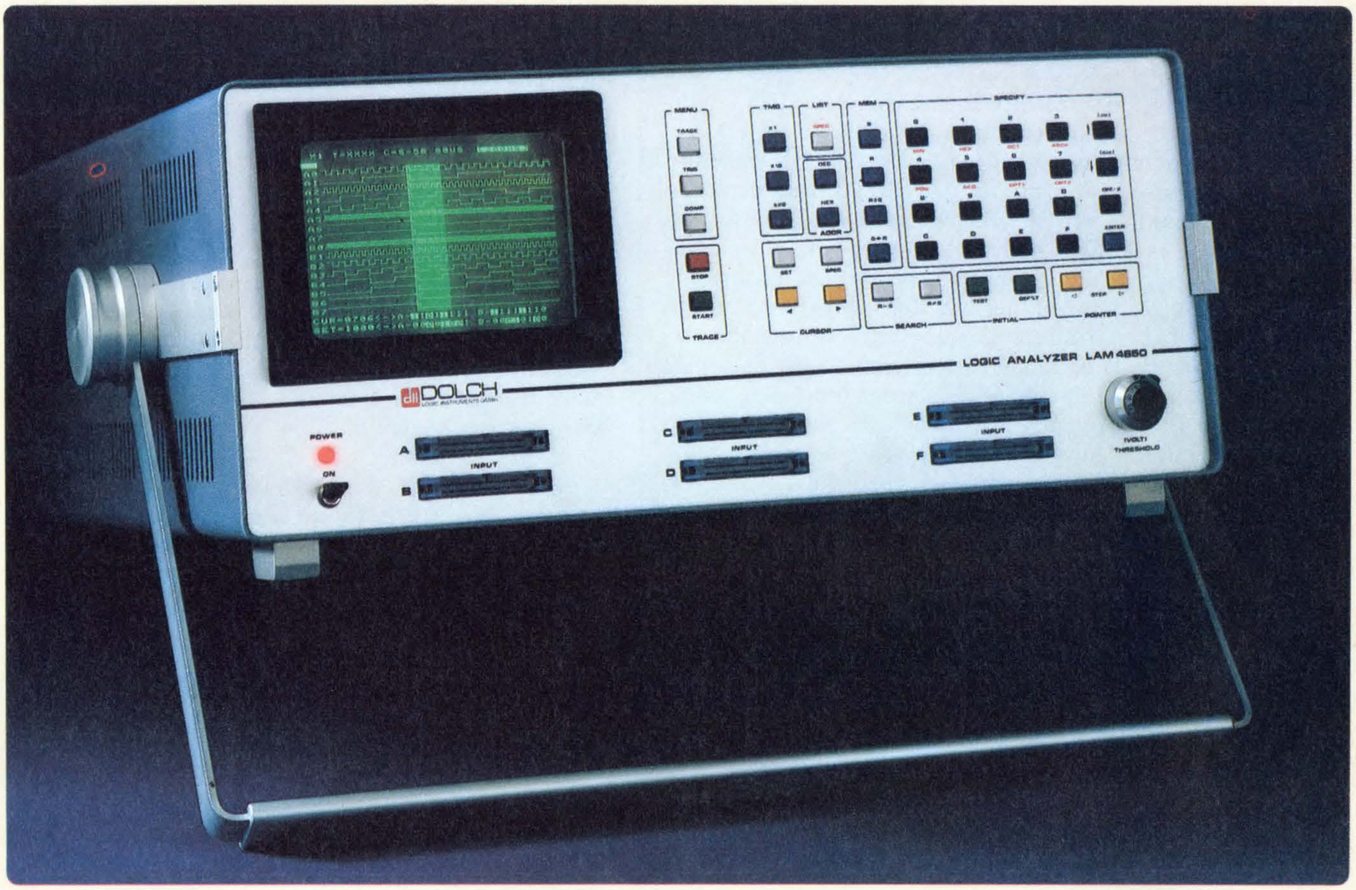
MODCOMP INTRODUCES PASCAL – Modular Computer Systems, Inc. (MODCOMP) has added PASCAL to its standard offering of high level software products. MODCOMP/PASCAL is designed to meet the latest proposed International Standards Organization (ISO) standard. Fully integrated with MODCOMP's MAX IV software family it takes complete advantage of the powerful CLASSIC architecture. The compiler and the optimized code produced by the compiler are sharable by many users simultaneously in developing and testing MODCOMP/PASCAL programs. Available 30 days ARO. Single use licensing agreement fee is $3500 per computer. The package includes complete documentation (User and Reference Manuals) and six-month warranty. **MODCOMP Inc.,** P.O. Box 6099, 1650 West McNab Rd., Ft. Lauderadatle, FL. 33310 **Circle 281**

CATALOG OF STANDARD LINE CONNECTORS. Cannon Electric has a new 1980-81 catalog of standard line connectors used in commercial, industrial, military and aerospace markets. The 233-page catalog features 225 black-and-white photographs, 250 drawings and 13 cutaways of 20 different connector lines. Included in the new catalog are connector applications, contact arrangements, electrical and mechanical data, materials and finishes, dimensions, performance test results and cross-reference guides. **ITT Cannon Electric,** 666 E. Dyer Rd., Santa Ana, CA 92702. **Circle 220**

INTELLIGENT MODEMS. These new modems offer greatly increased capabilities compared with ordinary "dumb" modems. The 1030 Series combines low error rate modem with an automatic calling unit (ACU) and custom BIZ-080 microcomputer into a compact FCC-registered unit with auto-answer, auto-dial and auto-repeat dial features. The key to this enhanced performance is BIZCOMP's Code-Multiplexed Design which allows Intelligent Modem control using the same terminal as that for data communication. The top-of-the-line 1031 adds command-selectable dial pulse or tone dialing, and self-test for ensuring full functionality. Availability is stock to six weeks. Prices: Model 1030 – $395; Model 1031 – $495. Discounts available. **BIZCOMP Corp.,** P.O. Box 7498, Menlo Park, CA 94025. **Circle 219**

NEW APPLICATION NOTES FOR LOGIC ANALYZER. Four free new application notes describe uses of the Biomation K100-D logic analyzer. Two of the brochures show use of the K100-D logic analyzer to trace program flow on the Z-80 and 8085 μPs. One brochure shows use of a HP Model 7245A printer to extract status parameters and to obtain hard copy of stored data in memory output. The fourth describes extension of the trigger capability of the K100-D using the 10-TC. **Gould Inc.** Biomation Operation, 4600 Old Ironsides Dr., Santa Clara, CA 95050. **Circle 221**

POWERFUL SINGLE-BOARD MICROCOMPUTER SYSTEM is suitable for small-scale industrial automation tasks. In addition to the central processor and a real-time clock, the new 210 D SBC offers programmable serial and parallel interfaces for I/O transfers, 12 interrupt inputs for real-time applications and memory space up to 20 KB CMOS-RAM and EPROM. The memory can be expanded to 64KB by means of various expansion modules. A single module can contain up to 8KB CMOS-RAM and 32KB of EPROM or up to 4KB CMOS-RAM and 16KB or EPROM. **Siemens Corp.,** Mr. Martin Weitzner, 186 Wood Ave., S., Iselin, NJ 08830. **Circle 222**



48 TO 96 Channels in One Logic Analyzer

Our LAM 4850 is the only logic analyzer that won't force you to buy, borrow or add-on to expand your analyzing capability to 96 channels. The power is already there. The flexibility is there. With a new channel expansion probe, the world's first 48-channel logic analyzer can be easily extended to an unrivaled 96 channels.

Plus multi-level clocking flexibility.

With three individual memory blocks of 16 channels by 1000 bits, the LAM 4850 allows simultaneous sampling with up to three separate clocks. This gives you a bus demultiplexing capability to independently monitor addresses and data. You can also disassemble program execution of a microprocessor into mnemonic code with this high performance instrument.

Plus sequential trigger power

The LAM 4850 has a 4 level nested recognition capability easily programmed through a separate menu. This feature simplifies debugging a faulty piece of software among several nested routines. And the LAM 4850 has the unique Dolch trigger trace monitor that gives you a real time read out of the completed routines.

Plus many other features:

- 1000 bits of recording and reference memory per channel
- Clock rate to 50 MHz
- With 96 channels—500 bits of recording and reference memory and 10 MHz clock rate
- Separate menus to set trace, trigger and compare parameters
- 5 ns glich catching
- Binary, hex, octal, ASCII, and timing display
- Programmability via GPIB and RS-232 interfaces
- Disassemblers and personality probes for all popular microprocessors

Plus sales and service nationwide.

For more information, contact your nearest representative or our manufacturing facility. Dolch Logic Instruments, Inc., 2180 Bering Drive, San Jose, CA 95131. (800) 538-7506. Inside Calif.: (408) 946-6044. TWX 910 338 3023.

dli DOLCH
LOGIC INSTRUMENTS

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Circle 63 on Reader Inquiry Card

Digital Imaging

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image processing system more than is implied by time comparisons. This is only a sampling of sophisticated image processing algorithms recently implemented on this representative image display-computer. In addition to a basic library of functions, we now have hardware implementations of spatial FFTs, contouring, dynamic pseudocoloration, and a multicolored, generalized version of the mathematical game of LIFE. Under development are automatic map digitization, stereo photo interpretation, watershed mapping, and a variety of other functions applicable to nondestructive testing, medical imaging and printing industry. Hardware available today is clearly ahead of the application software. Few, if any, generic image processing problems appear to be presently insoluble in the available image display-computers. However, our experience has shown that some algorithms, which at first seem impossible, can be reformulated to make their implementation in hardware straightforward. While host-computer-software approaches generally perform the entire algorithm on each pixel before considering the next pixel, the hardware approach in an image display-computer generally involves a stepwise completion of the algorithm.

The challenge in the next decade will be to overtake and fully utilize the capabilities of these new devices. Fortunately, hardware developments have curiously assisted new software development because as devices become more powerful, they also become cheaper. Their power has also reduced the need for expensive hosts. These two factors alone are leading to an expanding market. ■

Microcomputer Software

continued from p. 66

capable, more sophisticated, and larger. Intel's RMX/86, for example, occupies 90 bytes in its full configuration!). (4) Increased concern with company-level policy on software development and reliability.

Some problems ahead

As for the future, here are trouble spots . . . .

1) The μP/μC manufacturers have now borrowed almost all the languages, operating systems, and other stock-in-trade available from the world of larger computers. If they make further advances, they must do their own research, sponsor work in universities, or combine forces with mini and mainframe manufacturers. Perhaps the combined Intel-Xerox-DEC Ethernet communications effort will lead to cooperative work on software.

2) μC development systems remain characterized by low-quality, inadequate software. Few high-level languages are available, software tools are inconsistent as well as difficult to use, and too few tools are available to aid in debugging, documentation and maintenance.

3) The level of expertise among manufacturers varies greatly. While some talk about multitasking, concurrency, exportation, access rights, and hierarchical memory protection; – others are still discussing macroassemblers, small variations in instruction sets and minor coding problems! The level of expertise among users shows a similar variation. The trend toward rapid obsolescence of devices, programs, methods training, engineers and even companies shows no signs of stopping. ■

Keyboards

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Mechanical features

Lowering keyboard cost through mechanical design considerations includes decreasing the number of keys by using the μC (whether on or off the keyboard) to increase the functions of keys or combinations of keys. Electronic alternative-action and shift-lock keys with LED indicators eliminate expensive switches and increase keyboard reliability. If the keyboard has a mounting frame, reducing the number of bends helps. Minimizing the size and complexity of the printed circuit board, allowing the use of acceptable material substitutes for G10FR4, and using single-sided boards can also significantly reduce costs. Gold-plated card-edge connectors are definitely out, with flat cable and pin headers common.

Standardizing key layouts is becoming an important factor as keyboard manufacturers become automated and as single-piece keyboard modules are used to reduce cost.

Manufacturing capability

The two most critical factors in keyboard production are plastic molding capability (especially keytops) and ability to meet demand. Control over molding keytops and necessary tooling support is important in providing lower costs, quality and delivery. Key tops will remain the most persistant problem in the keyboard industry. Few manufacturers have enough experience or sufficient facilities to efficiently produce the number of shapes, sizes, legends and color combinations. It may all change by 1983. ■

Printers and Teleprinters

continued from p. 53

Mannesmann Tally and Printronix are primary OEM sources for shuttle matrix products. H-P and IBM announced products in the 200-600 lpm range. Okidata, Phillips and others have offerings of other impact matrix line printer products. The list is short and the market continues in a normal OEM mode.

Page printers

Non-impact matrix is dominated by electrophotographic products. Performance ranges from 10 to 200+ pages/min. Current products are polarized with "super printers", such at the Xerox 9700, IBM 3800 and Honeywell page printer, over 100 pages/min. and priced above $250,000 at one end of the spectrum. The intelligent copier/printers (ICP's) are at the low end – from 10 to 50 ppm currently and priced from $15,000 to $75,000. These ICP's, such as the IBM 6670, Wang 41F and Canon LBP products, are typically copier based and subject to similar service requirements. Advantages are speed, print quality and graphics capability. Disadvantages are single copy and high maintenance.

Expect emerging technologies such as magnetographics, large array ink jets and perhaps, eventually, impact matrix arrays. Several participants, including the Japanese copier manufacturers, should stimulate improvements in cost and maintainability. Expect more mid-range offerings by 1983. ■

Designers' Notebook

Programmable Gain Changing Provisions

Only after it has been determined that a single, optimum gain setting does not satisfactorily resolve any and all inputs within the resolution of the given system should programmable gain be considered. Not only is it expensive to incorporate software programmable gain into a DAS, but it almost always ends up becoming the greatest single source of errors within the system.

In a fixed-gain, high-input impedance differential amplifier (**Fig A**), the actual differential amplifier is made up of two LF156s for input buffers and one LF157 to produce a better CMRR (common mode rejection ratio) for the differential stage. Since a CMRR of 80 dB needs a better than 0.005% ratio matching of the gain resistors, a potentiometer is used to fine-tune the CMRR at low frequencies. The high frequency CMRR depends entirely on the op amp selected for the differential stage; the LF157 provides an excellent high frequency response of 90 dB at 1kHz.

Because it is difficult to maintain a high degree of common mode rejection, the programmable gain feature should not be placed within the differential amplifier stage itself; rather it should be placed in a separate stage following the differential amplifier (**Fig B**). This particular programmable gain circuit employs a CD4051 CMOS analog multiplexer as a two-to-four line decoder with appropriate FET drive to switch between feedback resistors and to program the gain in any one of four values.

The problems associated with a circuit of this type are rather obvious. First, as previously noted, one offset adjustment for the entire DAS would be advantageous. Not only does the programmable gain stage require offset adjustment, but the offset of the gain op amp and the offset of the differential stage must be nulled out to prevent the offset error of the system, up to this point, from becoming a function of the programmed gain.

Probably the biggest disadvantage in using a programmable gain stage is the initial calibration required. Besides the two offset adjustments, four gain adjustments must be carefully made by selecting FETs and feedback resistors. The calibration of this gain stage is not only troublesome, but very time consuming and not very appealing for high-volume production.

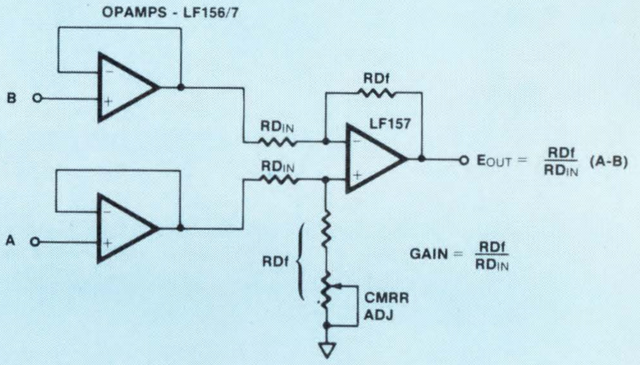

Fig A Differential amplifier with CMMR fine adjustment provides fixed gain high impedance input.

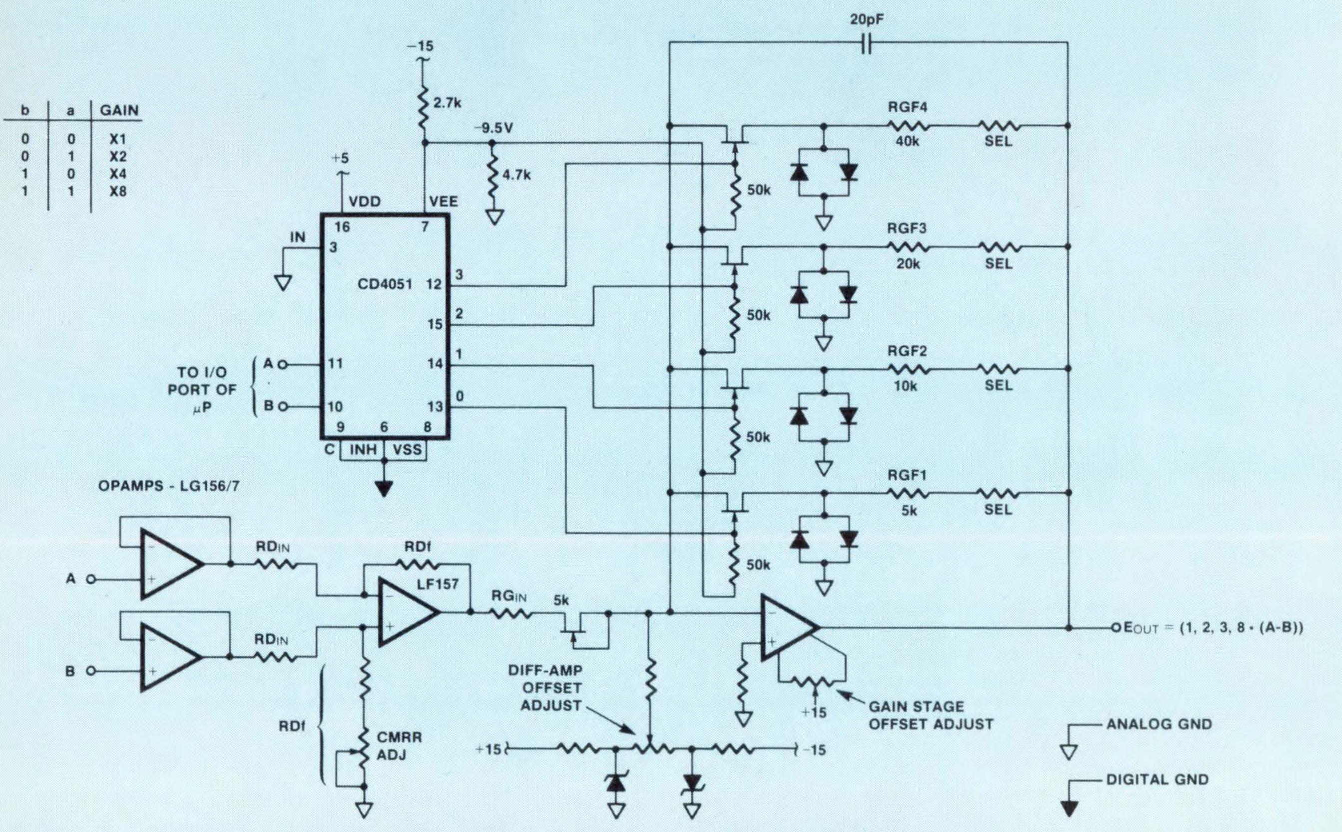

Fig B Software programmable gain differential amplifier produces four gains of 1, 2, 4 and 8X.

MOS RAMs

continued from p. 36

The designer should be aware of a dual JEDEC pinout standard for 32-k and 64-k EPROMs, which suggests a functional controversy among several manufacturers. One manufacturer includes an on-chip output enable function, while another manufacturer requires an external chip select buffer. The designer can sidestep this controversy by including a chip select buffer, which allows either device to be used with simple board jumpering. At least one manufacturer is planning to offer 32-k and 64-k devices with both pinouts to solve the designer's second sourcing problems in yet another way.

Future developments

Several other significant developments are likely to emerge in the next five years. At least one manufacturer is building an EPROM with the conventional NMOS memory array, but with CMOS peripheral circuitry. This approach will produce devices that use less power and provide better noise immunity. First of these devices, in a 2-k×8 configuration, is being sampled now with production scheduled for early next year.

The other significant development expected over the next five years is the EEPROM. Currently, several manufacturers have announced devices with a 2-k×8 configuration and are either sampling or are about to go into production with them. Other manufacturers are planning similar devices which should be in the marketplace within a year. ■

Floppy Disk Drives

continued from p. 46

1982. When closed loop positioners can be produced cost-effectively, track densities beyond 96-tpi and storage capacities of 2-Mbytes or more will become realistic.

Before we reach higher storage capacities, we need media that can keep pace with drive technology. This sets the stage for introduction of the true 5-Mbyte drive. While some high capacity drives currently exist, the lack of compatibility in media, form, fit and function between these units and industry standards makes wide acceptance unlikely.

5.25-in. drives will find increasing application in WP and intelligent terminals where small size counts; these drive designs will become even more compact. Lowering power consumption by a projected 25 to 30% will result in smaller, quieter cooling fans, helping to minimize drive size.

1981's floppies will use more μPs to provide more intelgent drives. Intelligent on-board controllers will unload the CPU by providing local file management systems.

Will thin film technology help reach higher recording densities? Yes. But, thin film in Floppies will probably appear after 1981.

What about smaller (2.5 to 3 in.) disks? They are too costly to develop and manufacture to be candidates for future production. Bubble memory may be used where the smaller disks would otherwise be useful, especially since offices of the future would be the most likely area for using smaller disks. This application requires a minimum of 1-Mbyte of storage, which is not now feasible on smaller disks. ■

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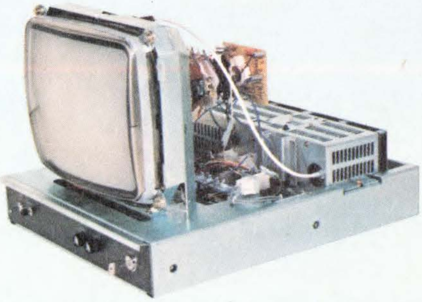

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