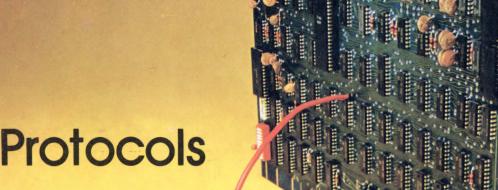
VOLUME 10, NO. 7

JULY 1980

Digital Des Computers • Peripherals • Systems

System Designers' Guide to Printers Recursive Programming





Protocols

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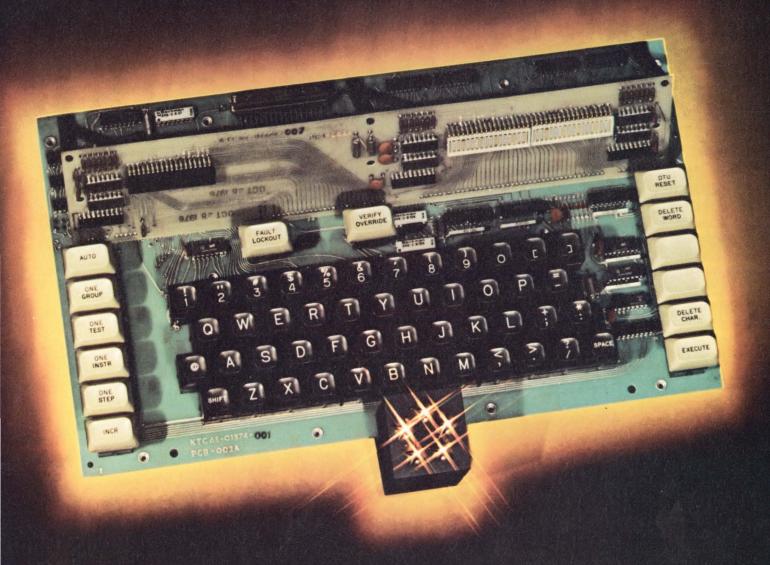
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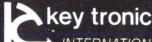
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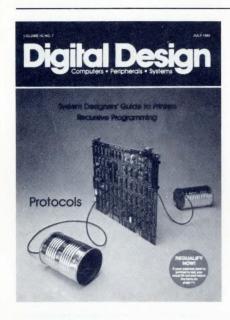
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Microcomputer programmers too often dislike recursive algorithms because they believe recursion requires a large computer and fancy language implementation. This is false. Here's how to use recursion in microcomputers using Basic.

26 System Designers' Guide to Hard Copy/Printers

This technology overview of printers covers computer output printing technologies, hardcopy techniques in Western Europe, optimum design high-speed non-impact printers, tactical hard copy image generation systems and synchronous jet ink droplet generator mechanisms.

40 Communicating Data With Protocols

This article describes protocol types, basic formats and information provided and required by each protocol to communicate with the computer.

ON OUR COVER

This month's cover symbolically exemplifies the use of protocols for intercomputer communication. (*Photograph courtesy of MDB Systems of Orange, CA*).

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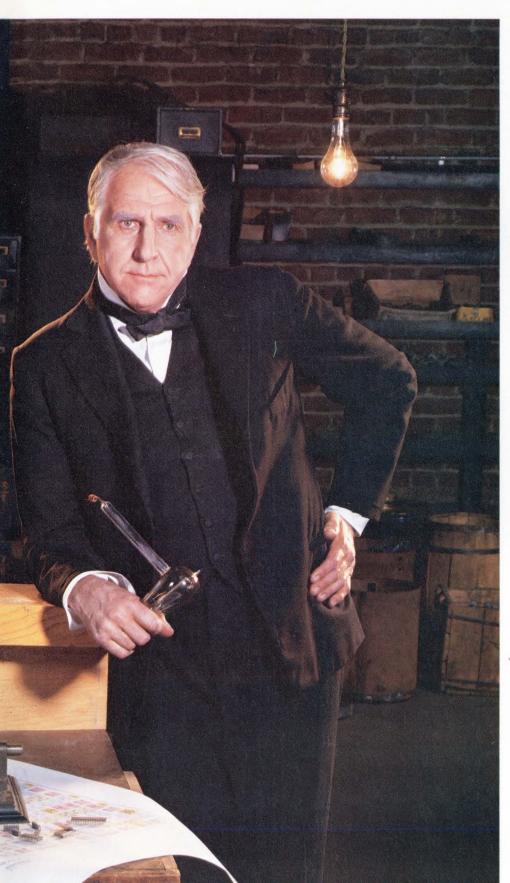
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Speakout

Paul Snigier, Editor

Continued Growth Ahead

Last May (1979), we asked you what you wanted to see more and less of. The results were overwhelming; and as a result, we made several changes you asked for. For example, when you voted one column, Viewpoint, as low-interest, we responded by replacing it with a regular monthly column, Designers' Notebook that had run twice before as a trial balloon. Since then, your letters and comments on Designers' Notebook have been overwhelmingly favorable.

Once again, we would like to ask you to do us a favor: please take a moment and participate in planning Digital Design's engineering editorial coverage. This is *your* magazine; and only by serving you better and providing you with top-quality material and categories that you want to see do we make our advertisers happy (who pay our bills, making us happy) — not to mention helping *Digital Design* provide

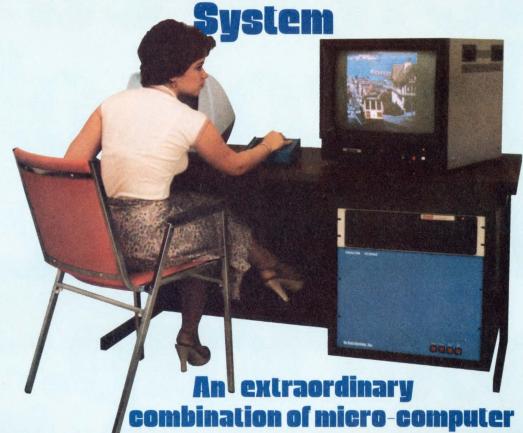
a vehicle for disseminating useful and practical educational and product information free of charge to you. As an engineer in industry, this editor, like other EEs, found *Digital Design* and other electronics/computer publications the only really good source of an abundance of up-to-date information that costly (and all-too-often, impractical) texts could not carry.

Once again, please tell us more about what you want to see — or not see — by rating the topics below. Rate subjects A through E. "A" is "most preferred" and "E" indicates "least preferred." Then tear this page out and mail it to me. Address it: Paul Snigier, Editor, Digital Design, 1050 Commonwealth Ave., Boston, MA 02215. Once again, thanks for helping us plan our editorial coverage and for your letters, comments and phone calls.

1. Computers/Memories 1. Minicomputers 2. 16-bit micros 3. 8-bit micros 4. Array processors 5. Signal processors 6. Floppies 7. Winchesters 8. Tape streaming 9. Tape/cassettes 10. Add-in/on memory 11. Controllers 12. EPROM programmers	A B C D E	6. Types of articles 1. Feature-length tutorials 2. Feature-length equipment surveys 3. Application notes from users 4. Cases from users 5. Users' equipment designs 6. Literature 7. Book reviews 8. Equipment vendor applications 9. Letters 10. Speakout 11. Software Deisgn Series 12. Special Reports (as Jan. 80	A B C D E
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3. Data Communications/Interfacing 1. Communications interfaces 2. Communications monitors 3. Modems/Data sets 4. Fiber optics 5. Data acquisition 6. Time sharing/distributed processing	A B C D E	3. Include schematics 4. Include printout 5. Include equations 6. Include vendor equipment photos 7. Quote test industry personnel 8. Your Function 1. Incoming inspection	
4. Software 1. Pascal 2. Ada 3. Basic 4. Assembly 5. Calculator	A B C D E	 Production testing QA/QC/reliability Prototype evaluation μP development Test design Field service Standards/calibration 	
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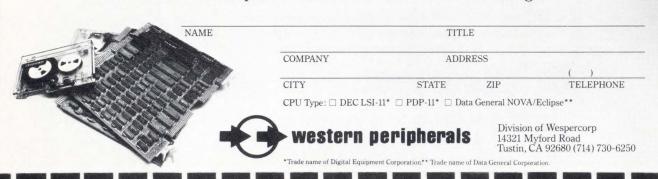
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DIGITAL PATHWAYS

Technology Trends

Inventor of Core Memory Lectures To DEC Engineers

Digital Equipment Corporation sponsors a computer museum at Marlborough, Mass. Housed in a two-story building with gold-tinted windows are some of the fascinating tools that science has used in its continuing efforts to create a working electronic model of the human brain. The displayed collection starts with a yellowing, ivory set of Napier's Bones (1614) and runs chronologically to DEC's 1969 PDP-12, (an offspring from MIT's LINC-8 computer). Highlighting the museum's collection are selections of MIT's Whirlwind computer. Whirlwind differed from other early pioneers in computers in being the first, and fastest general-purpose computer. The ENIAC (later to become the Sperry Univac) was not a general purpose machine. Its primary goal was to construct a series of artillary-firing-tables for the Aberdeen Proving Grounds. MARK I at Harvard was a slow-moving electromechanical device that was quickly left behind by the high speed of allelectronic computers. Bell Telephone's Relay Computer was designed to facilitate transmission of rapidly-growing communications circuits. The general-purpose Whirlwind became the flower seed from which has sprouted most of the computer hardware as it stands today. The transition of Whirlwind from a laboratory machine at MIT to a marketable commercial device was made by Ken Olsen. He had worked on the computer at the Institute and when the Whirlwind project was finally phased out in 1959 he, and other scientists, started Digital Equipment Corporation in 1961. The PDP-1 was launched that same year.

The single most important ingredient of Whirlwind was the invention of the random-access magnetic-core storage feature. It replaced unreliable vacuum tubes and made possible the rapid development of computers.

Inventor of this ferrite-core memory, after four years of research, was J. Forrester, who had struggled with electrostatic storage tubes since the concept of Whirlwind was first sketched on paper. On June 2, 1980,

J. Forrester came to DEC's Computer Museum in Marlborough to deliver the third in a series of "Computer Pioneer" lectures (lectures delivered by the pioneers of computer development). For an hour-and-a-half, before an excited, wide-eyed group of young DEC engineers, Dr. Forrester presented a slide/talk show. He recounted many of the problems he had faced with the Whirlwind project. An early design requirement for the computer, he revealed, was building it high enough in the room so that no person would ever tower over it. It was important that it be huge enough to reflect all the research money being invested by the government. Because he himself is well over six feet tall, the computer stood

close to seven feet high.

"How did you happen to become involved in computer science in the first place?" one of DEC's young engineers wanted to know during the concluding question and answer period. "Because I always wanted to be where the action was, I guess," answered Dr. Forrester. "I found you always had to be in the right place. If you got too far away from the action you would be lost in the crowd. If you got too near the edge you could fall over the cliff. You just had to be in the right place." His contributions to the Whirlwind project and to computer technology in general proves that he had always been in the right place at the right time.

-Harry Shershow

U.S. Computers Rebound

The U.S. computer industry is emerging from relatively flat growth last year and revenues are improving. But problems could surface, and the industry must adapt to an increasingly competitive environment. Otherwise, shifts in product demand, protectionism overseas, and outmoded pricing policies and cost structures will persist as long-term problems.

A newly completed Arthur D. Little Impact Services five-year outlook pegs last year's combined data processing revenues at \$29.4 billion for the seven largest U.S.-based computer vendors and plug-compatible mainframe vendors (PCMVs), who comprise more than 80% of the domestic industry. They estimate that IBM is experienc-

ing a 4.5% decline in dp revenues and only a 3% growth in shipments — a situation due to the firm's customers for larger computers who are currently opting to lease rather than make major investments in the purchase of equipment they may soon wish to replace with newer models. While that is causing a temporary revenue problem, IBM will soon experience a surge in shipments of its new smaller systems.

ADL believes that the industry must continue the trend to separate pricing of software and services and that U.S. vendors need to readjust their internal cost structures in a period of declining component costs, increasing personnel costs, and economic uncertainty.

Proliferation of Electronics Distributors

The emergence of the Industrial Electronics Distributor — not the Department Store — will be the significant new force in the sale of small business computers. True or false? Apparently, it's true. According to Strategic Business Services (San Jose, CA), com-

puter stores and retail electronics stores which handle more than 80% of the current retail trade, will account for only 50% of the business by 1984. Retail department stores, other mass merchandisers, specialty stores, electronics stores will have 12% of sales.

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Technology Trends

Engineering Office Of The Future Will Improve Productivity

Is industry spending more time in designing sophisticated electronic systems for secretaries than for design engineers? According to G. J. Lorenz of United Computing Systems of Kansas City, MO, the situation is intolerable.

The engineering work station, or engineering office of the future, is in many senses as important as, or more important than, the office of the future as a means of enhancing workforce productivity. This is especially so given the chronic shortage of design engineers during every boom period. An obvious way to mitigate the effects of too few engineers is to improve the efficiency of the available manpower. But manufacturers have not created sufficient demand for systems which could realize such a goal, so progress has lagged.

It seems especially ironic that designers have been kept busy creating systems to support the office worker, while the engineer's own needs have been all but overlooked.

A lot has already been accomplished in this direction, claims Lorenz. "A number of firms offer significant tools of use to engineers; for example, an extensive software library and other support. But industry has just scratched the surface with respect to the engineering support that will be provided in a few short years."

In fact, technology already exists today which is making design engineers, researchers, architects, city planners and even tax assessors, more efficient and effective. Various interactive graphic systems and software packages are prime examples of such design aids. They greatly simplify such diverse tasks as preparing engineering drawings, laying out ICs, creating and revising maps, and maintaining pipeline locations and associated data for entire utilities. The ability to remotely tie in with mainframes, including a Cray-1, and an extensive array of UCS software and data bases, is an important asset to the designer and is a trend which will see future refinement and expansion.

The problem is that while sophisticated design tools for engineers and scientists have existed for some time.

and continue to improve, we have a long way to go in order to achieve a well organized 'engineering work station' that meets each designer's specialized needs.

The typical engineer today still works at a conventional desk or drawing board, making pencil sketches and writing out equations in longhand. He may have access to a computer or a timeshare terminal, and if he's fortunate there may be a graphic plotter he can use. But only a small percentage of

designers today have access to an interactive system even though studies have shown enormous cost/benefit advantages for such investments.

The full-fledged Engineering Office of the Future will include an interactive computer terminal, graphic CRT display with 3D capability, comprehensive data base management systems, printer, plotter — perhaps shared between eight or ten engineers — and access to a variety of software, data bases, and large host computers.

Computers Aid In Search For Unified Field Theory

Mark E. Canney University of Minnesota

A mine shaft 2,000' deep and five million gallons of water are the props University of Minnesota researchers will need to conduct a test that may shed light on the nature of all matter. The research project, which combines the efforts of physics researchers from the University of Minnesota, the University of Wisconsin, and Harvard and Purdue Universities, will test a part of the unification theory of physics, according to Marvin Marshak, Associate Professor of Physics at the University of Minnesota.

Albert Einstein spent the latter part of his career working on the unification theory, but was unable to complete the work before he died. The basic premise of the unification theory is that the four forces in nature — gravity, electromagnetism, the nuclear or strong force that holds the nuclei of atoms together, and the weak force, which is responsible for some radioactive decay — are all governed by one fundamental interaction.

In the last decade, partial unification of the electromagnetic and weak forces has been verified experimentally. Gravity and the strong force, however, have yet to be "unified," and the Minnesota project will be an attempt to prove that the strong force fits into the unification scheme.

"This experiment is of such importance to the world-wide physics

community that three independent experiments are currently planned, one in Minnesota, one in a salt mine in Ohio, and one in a tunnel under the Franco-Italian Alps," Marshak said.

Supported by the U.S. Department of Energy, the Minnesota experiments will be conducted in the Tower-Soudan mine, now a state park near the southern shore of Lake Vermilion. Planning for the experiment is well underway, and Marshak expects testing to begin sometime this winter.

If the researchers can find empirical evidence that the strong force is part of the unified whole, they will be one step closer to providing that all matter, at some time, breaks down spontaneously and converts to energy.

Observing this breakdown is the key to this experiment.

The researchers hope to observe the protons contained in the atoms that make up water as they decay, that is, change from matter to energy. Such transformations are extremely rare, happening only once every 10^{30} to 10^{34} years. The experiment can be performed either by observing a small amount of matter for a long time or by observing a large amount of matter for a short time.

The physicists have opted for the second choice. Five million gallons of water, the amount that contains 10³⁴ protons, will be piped from nearby Lake Vermilion to a point 2,000' below the earth's surface in the mine shaft.

Continued on next page

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Technology Trends

Continued from previous page

Into the water-filled shaft, the researchers will place photoreceptors sensitive enough to pick up and record minute quantities of light.

When a proton decays, the resultant energy is measurable as a tiny burst of light. The light burst is so minute that the photoreceptors must be extremely sensitive to detect it.

Because of the hypersensitivity of the photoreceptors, the experiment must be done deep underground. If the testing were done on the earth's surface, the radiation that bombards the earth daily would overload the photoreceptors.

Some forms of radiation, however, will penetrate the earth and reach the photoreceptors, Marshak said. This radiation will not be significant

enough to disrupt the experiment, and will be used to test the effectiveness of the equipment.

Beyond its attempt to include the strong force in the unification scheme, the experiment, which will last for at least five years, will shed light on the origins of the universe and may provide clues to the nature of its demise.

Could such interactions between gravitational and electromagnetic fields be used to create a new type of space drive propulsion system and spacecraft and aircraft of revolutionary design? And, could such interactions be used to create silicon crystals with perfect lattice structures? Or, super-strong metals totally free from impurities? Or used in the fabrication of semiconductor devices with densities and capacity undreamed of today? At this stage, any such implications remain in the speculative stage, and it won't be known for awhile.

Software Copyright Woes Continue

Unauthorized copies of Nestar Systems' Basic Programmer's Toolkit are apparently being marketed in Europe. The unauthorized copies of the ROM-based Toolkit are being sold on tapes and diskettes. This raises the legal and ethical issues of software protection, even though the distribution form has been changed from ROM to magnetic media.

"We believe there is direct violation of our international copyrights for the Basic Programmer's Toolkit", commented Dr. Harry J. Saal, Nestar's president. "The sale of unauthorized copies of our product concerns us: it is bad for Nestar in particular and for the microcomputer industry in general."

The unauthorized copy of Nestar's code has additional ramifications: since it has been *incorrectly* relocated to a RAM memory location, there are certain operating conditions under which the running program would malfunction and alter or lose the user's data. In addition, one of the Nestar Toolkit commands no longer functions correctly. The only other change is the replacement of the Nestar Systems, Inc. copyright notice with the name of the company offering the unauthorized copies.

"Nestar Systems," Dr. Saal stressed, "is taking immediate action to prevent this unfair and illegal practice from continuing. We will pursue all remedies available to us under our international copyrights and trade agreements to stop the sale of any unauthorized Toolkit copy. Moreover, we encourage other manufacturers and dealers to join us in aggressively pursuing firms engaged in similar acts."

The recent, spectacular growth in microcomputer sales makes issues of firmware, software, and hardware quality very critical. "Right now, product integrity and dependability are essential: suppliers' reputations and their sales success will depend on products performing as promised. Dealers and users are unknowingly taking risks with their programs when they use an unauthorized copy. In addition, the substantial investment necessary to produce quality software will not be made if illegal pirating becomes widespread in this industry."

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Recursive Programming in BASIC

Herbert L. Dershem Hope College, MI

R ecursion can be a valuable tool on microcomputers using BASIC. For this reason, it should be in every programmer's repertoire.

What is recursion?

Anything is recursive if it is defined in terms of itself. In programming, a recursive subroutine calls on itself.

Don't confuse recursion with iteration, since both often can solve the same problem. The distinction is clear: a procedure is iterative if the same process is performed, begun and completed repeatedly; a procedure is recursive if, in the middle of its execution, it calls upon itself. Therefore, a recursive procedure begins another execution of itself before the original execution is finished. Such a procedure has more than one execution in progress at a given time, whereas an iterative procedure never has more than one in progress.

Testing for recursion

Not every language implementation permits recursion. In BASIC, recursion is only possible if it is permissible to call a subroutine from itself and still retain the ability of the original execution to return to the proper point. To test your BASIC for recursion capability use the following program:

- 10 REM TEST FOR THE ABILITY OF THE BASIC TO PERFORM RECURSION
- 20 N=1
- 30 I=0
- 40 GOSUB 100
- 50 IF I<> 2*N-1 THEN 170
- 60 PRINT "RECURSIVE"; N-1; "TIMES."
- 70 N=N+1
- 80 GOTO 30
- 100 I=I+1
- 110 IF I<N THEN 130
- 120 RETURN
- 130 GOSUB 100
- 140 IF I > 2*N-1 THEN 170
- 150 I = I + 1
- 160 RETURN
- 170 PRINT "NOT RECURSIVE"; N-1; "TIMES."
- 180 END

Every call of subroutine 100 increments 1 by one. The Nth call results in the setting of I to N and a return with-

out a recursive call. This return to each of the previous levels increments I by one. On the final return, I should equal 2*N-1, if the process was carried out correctly. Thus, if this program runs for a given value of N, this version of BASIC allows N-1 recursive calls. Many versions of BASIC virtually set no limit on the number of such calls possible.

If the BASIC is not recursive to the appropriate level for some value of N, it usually responds with some type of diagnostic message rather than arriving at statement 170.

Writing recursive subroutines

If you have found that your computer's BASIC does allow recursive subroutines, you are now faced with the problem of writing them. Then follow this general outline of recursive subroutine in BASIC:

- 1. If the first call, initialize the stack pointer.
- 2. If termination condition, compute result, decrement stack pointer, return.
- 3. Do computation.
- 4. Save necessary values in stack.
- 5. Increment stack pointer.
- 6. Recursively call this subroutine.
- 7. Restore saved values from the stack.
- 8. Do any remaining computation.
- 9. Decrement stack pointer.
- 10. Return.

When you recursively call a subroutine from itself, the variables in the called execution destroy the variables of the same name in the calling execution. To preserve the original values of these variables, save in a dimensioned variable (called a stack) those variables you need to recall later. Suppose your subroutine has three variables -X, Y and Z—that it wishes to save for recall, when it returns from a recursive call. The format of the stacks for these variables, which are introduced by three subscripted variables of the same names, uses the following representation:

- X(1) X from execution 1
- Y(1) Y from execution 1
- Z(1) Z from execution 1
- X(2) X from execution 2
- Y(2) Y from execution 2
- Z(2) Z from execution 2

To keep track of the position in the stack where the current execution saves its values, use a pointer. Every recursive call increments this pointer by one. Likewise, each return decrements the pointer by one.

The general recursive procedure just outlined shows only one recursive call in the subroutine. In general, steps 3 to 8 may be repeated several times before returning to steps 9

An example: calculating N!

Let's take a recursive subroutine and follow these steps. Let's use the classic example of factorial recursion. Unfortunately, it's also a problem because recursion is not the best way to obtain a solution; however, it is the most familiar and simplest of all examples, so why break tradition?

The common definition of N factorial (N!) is iterative and given by: N! = N*(N-1)*(N-2)* ... *2*1 for N = 1, $2, \ldots$ (where 0! = 1). But there is also this recursive definition of N factorial: N! = N*(N-1)! for N = 1, 2, ...(where 0! = 1). Notice that the factorial is defined in terms of itself, but with one escape clause which occurs at 0!. The recursive form of a subroutine to compute N! is exemplified by this sample calling program:

960	REM THIS SUBROUTINE COMPUTES N FAC-
	TORIAL RECURSIVELY AND
970	REM STORES THE RESULT IN F. THE FIRST
	CALL IS TO 990.
980	REM SUBSEQUENT CALLS ARE TO 1000.
990	S = 1
1000	IF N<>0 THEN 1040
1010	F = 1
1020	S = S-1
1030	RETURN
1040	N(S) = N
1050	S = S+1
1060	N = N-1
1070	GOSUB 1000
1080	N = N(S)
1090	F = N * F
1100	S = S-1
1110	RETURN

- 10 REM SAMPLE CALLING PROGRAM FOR RE-**CURSIVE FACTORIALS**
- 20 DIM N (100)
- 30 INPUT N
- 40 GOSUB 990
- 50 PRINT F
- 60 GOTO 30

In this program, statement 990 corresponds to step 1 in the general algorithm given earlier. Statements 1000-1030 correspond to step 2, in which the termination condition is N = 0. No computations in this program correspond to step 3 of the general algorithm. The remaining steps correspond to statements as follows:

Step	Statement(s)
4	1040
5	1050
6	1060-1070
7	1080
8	1090
9	1100
10	1110

Of course, the iterative version of the factorial subroutine is much simpler and executes much faster. This is an iterative version of a sample calling program:

```
970
       REM ITERATIVE SUBROUTINE TO COM-
       PUTE N FACTORIAL
980
       REM AND STORE IT IN F.
1000
1010
       IF N<= 1 THEN 1050
1020
       FOR I = 2 TO N
         F = F*I
1030
1040
       NEXT I
1050
       RETURN
```

REM CALLING PROGRAM 10 TO COMPUTE FACTORIALS **ITERATIVELY**

20 INPUT N

30 **GOSUB 1000**

40 PRINT F

50 GOTO 20

Computing Fibonacci Series

Another example of recursion is calculating the Fibonacci sequence of numbers. The Nth number in the Fibonacci sequence, F(N), is defined in terms of its two predecessors.

F(0) = 0F(1) = 1F(N) = F(N-1) + F(N-2) for N + 2, 3, ...

The BASIC version of this algorithm and its calling program are:

970 REM SUBROUTINE 990 CALCULATES THE NTH FIBONACCI NUMBER

980 REM RECURSIVELY AND RETURNS IT IN F.

990 S = 1

1000 IF N = 0 THEN 1020

1010 IF N <> 1 THEN 1050

1020 F = N

1030 S = S-1

1040 RETURN

1050 N(S) = N

1060 S = S+1

1070 N = N-1

1080 **GOSUB 1000**

1090 N = N(S)

1100 F(S) = F

1110 S = S+1

1120 N = N-2

1130 **GOSUB 1000**

1140 N = N(S)

1150 F = F(S) + F

1160 S = S-1

1170 RETURN

10 REM CALLING PROGRAM TO COMPUTE FIBONACCI NOS. RECURSIVELY

20 DIM N(50), F(50)

30 INPUT N

40 **GOSUB** 990

50 PRINT F

GOTO 30

Again, just as in the case of the factorial, iteration gives a more efficient solution to this problem.

970	REM SUBROUTINE 1000 CALCULATES TI	HE
210	NTH FIBONACCI NUMBER	11.
980	REM ITERATIVELY AND RETURNS IT IN F.	
1000	F = 1	
1010	P = 0	
1020	FOR $I = 1$ TO $N-1$	
1030	Q = F	
1040	F = F + P	
1050	P = Q	
1060	NEXT I	
1070	RETURN	
10	REM CALLING PROGRAM TO ITERATIVE	LY

- COMPUTE FIBONACCI NOS.
- 20 INPUT N
- 30 **GOSUB 1000**
- 40 PRINT F
- 50 GOTO 20

Although iteration gives better answers in both of the first two examples of recursion, recursion is the desired technique for many problems because it greatly simplifies the solution algorithm and its implementation in a BASIC program.

Tower of Hanoi

Let's consider two such problems. The first is the Tower of Hanoi, a well-known problem nicely treated in a recursive manner. This problem consists of three pegs, called pegs 1, 2 and 3, and D disks, all of different radius, and are to be stacked on the pegs. Initially, the disks are stacked on peg 1 in order of decreasing size, with the largest disk on the bottom. In this problem, you must move the disks from peg 1 to peg 2 under the restriction that you can only move them one at a time from one peg to another, and that you may never stack a larger disk on top of a smaller one. The recursive solution, which generalizes the problem of moving D disks from a peg called E to peg F, moves the top D-1 disks on peg E to a third peg, then moves the one remaining disk on peg E to peg F, and then moves all of the disks on the third peg to peg F. In this way, the problem of moving D disks is reduced to making two moves of D-1 disks. Therefore, the recursive algorithm for moving the top D disks from peg E to peg F is:

- 1. If D = 1, move top disk from E to F and return.
- 2. Let G be the number of the peg which is not E or F.
- 3. Recursively call this procedure to move the top D-1 disk from E to G.
- 4. Move the disk on E to F.
- 5. Recursively call this procedure to move the top D-1 disk from G to F.
- 6. Return.

In the implementation, store the number of disks on peg I in T(I), for I = 1, 2, 3. When a recursive call is made, the values that need saving are E, F and D. Then, the BASIC version of this algorithm is:

- REM TOWER OF HANOI SUBROUTINE TO 960 MOVE THE TOP D(S) DISKS
- 970 REM FROM PEG E(S) TO PEG F(S). T(I) CON-TAINS THE NUMBER
- 980 REM OF DISKS ON PEG 1. INITIAL CALL IS TO 990.
- 990 S = 1
- 1000 IF D(S) <> 1 THEN 1050
- 1010 T(E(S)) = T(E(S)) - 1

- 1020 T(F(S)) = T(F(S)) + 11030 PRINT "MOVE"; E(S); "TO"; F(S)
- 1040 GOTO 1190
- 1050 G = 6 - (E(S) + F(S))
- 1060 S = S + 1
- 1070 D(S) = D(S-1) - 1
- 1080 F(S) = G
- 1090 E(S) = E(S-1)
- 1100 **GOSUB 1000**
- 1110 T(E(S)) = T(E(S)) - 1
- 1120 T(F(S)) = T(F(S)) + 1
- 1130 PRINT "MOVE"; E(S); "TO"; F(S)
- 1140 S = S + 1
- 1150 D(S) = D(S-1) - 1
- 1160 E(S) = 6 - (E(S-1) + F(S-1))
- 1170 F(S) = F(S-1)
- 1180 **GOSUB 1000**
- 1190 S = S-1
- 1200 RETURN
- 10 REM CALLING PROGRAM TO SOLVE TOWER OF HANOI PUZZLE.
- 20 REM T(1) CONTAINS THE NUMBER OF DISKS ON TOWER I.
- 30 REM D(1) IS THE TOTAL NUMBER OF DISKS.
- 40 REM E(1) AND F(1) ARE THE SOURCE AND DES-TINATION TOWERS.
- 50 DIM E(20), F(20), T(3)
- 60 INPUT T(1)
- 70 T(2) = 0
- T(3) = 080
- 90 E(1) = 1
- 100 F(1) = 2
- 110 D(1) = T(1)120 GOSUB 990
- 130 GOTO 60

Quicksort algorithm

Let's now consider a final useful application of recursion, the quicksort algorithm. You can easily program these efficient and widely-used sorting algorithms recursively.

Suppose that you have stored values in $A(L), \ldots, A(H)$ and wish to place them in ascending order in the same storage locations. The basic quicksort algorithm chooses some arbitrary value from this list, say X = A(K), and then rearranges the values so that all values smaller than X are located before it in the list and all values larger than X are located after it. Then X will be located at its correct sorted position in the list of, say, A(I). The same algorithm is then recursively applied with L and I-1 in place of L and H, and then again applied, with I+1 and H. When calling the algorithm with L = H, it simply returns.

The only part of the algorithm that needs some additional attention is the process of rearranging the list so that X is in its proper position and all other values lie on the proper side of X. By keeping two pointers, I and J, you rearrange the list. I starts by pointing at the first position in the list, L. J points to H. Then as pointer I moves down the list, it encounters a value no smaller than X. This value of A(I) should, therefore, lie below X in the list. Next, pointer J moves up the list until it encounters a number no larger than X. That number is exchanged with A(I); both are then in the proper part of the list relative to the eventual position of X. Repeat the process until I and J cross. At that point, the rearrangement is complete, as the following example of the process shows:

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average of 128 times each month.² For users of computer-based equipment, power disturbances can and do create a variety of costly problems.

Effects upon data processing computers.

When these power disturbances occur in your data processing center they can cause entry errors, program changes or loss, head crash, data loss, the generation of false or garbled data, the need to rerun programs, and computer downtime.

Effects upon computerized process control equipment.

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References:

- 1. U.S. Department of Commerce, "The Effects of Electrical Power Variation Upon Computers: an Overview."
- George W. Allen and Donald Segall, IBM Systems Development Div., "Monitoring of Computer Installations for Power Line Disturbances," presented to the IEEE Power Engineering Society.



Topaz peripherals solve the power paradox by conditioning normal ac power for your computer and computer-based equipment.

I-	>12	12	12	12	12	12	12
	75	I->75	3	3	3	3	3
	60	60	I->60	I->60	44	44	44
	13	13	13	13	I->13	13	J->13
X-	>46	X->46	X->46	X->46	JX->46	JX->46	X->46
	44	44	44	J->44	60	60	I->60
	94	94	94	94	94	94	94
	49	49	49	49	49	49	49
	95	95	J->95	95	95	95	95
	J->3	J->3	75	75	75	75	75

The following program implements this process:

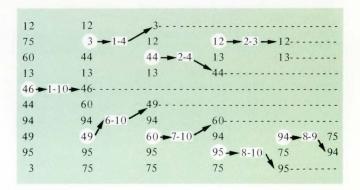
950	REM	QUICKSORT-SUBROUTINE	TO	REAR-
	RANG	E A(L(S)) THRU A(H(S))		

- 960 REM SO THAT ALL VALUES <= X LIE BE-FORE X AND ALL VALUES
- 970 REM > = X LIE AFTER X WHERE X = A (INT ((L(S) + H(S))/2)).
- 980 REM INITIAL CALL TO 990 SORTS A(1) THRU A(N).
- 990 S = 1
- 994 L(1) = 1
- 997 H(1) = N
- 1000 IF L(S) >= H(S) THEN 1270
- 1010 M = INT((L(S) + H(S))/2)
- 1020 X = A(M)
- 1030 I = L(S)
- 1040 J = H(S)
- 1050 IF A(I) > = X THEN 1080
- 1060 I = I + 1
- 1070 GOTO 1050
- 1080 IF $A(J) \le X$ THEN 1110
- 1090 J = J-1
- 1100 GOTO 1080
- 1110 IF I > J THEN 1170
- 1120 T = A(I)
- 1130 A(I) = A(J)
- 1140 A(J) = T
- 1150 I = I + 1
- 1160 J = J 1
- 1170 IF I <= J THEN 1050
- 1180 I(S) = I
- 1190 S = S + 1
- 1200 L(S) = L(S-1)
- 1210 H(S) = J
- 1220 GOSUB 1000
- 1230 S = S + 1
- 1240 L(S) = I(S-1)
- 1250 H(S) = H(S-1)
- 1260 GOSUB 1000
- 1270 S = S 1
- 1280 RETURN
- 10 REM CALLING PROGRAM FOR OUICKSORT.
- 20 REM A(1) THROUGH A(N) CONTAIN NUMBERS TO BE SORTED.
- 30 DIM A(100), L(20), H(20), I(20)
- 40 INPUT N
- 50 FOR I = 1 TO N
- 60 A(I) = RND(0)
- 70 NEXT I
- 80 GOSUB 990
- 90 FOR I = 1 TO N
- 100 PRINT A(I);
- 110 NEXT I
- 120 GOTO 40

Statement 1000 in this program is the test for termination. Statements 1010-1170 perform the partitioning of the list into those values smaller than X and those larger than X. Two recursive calls follow the partitioning. Only three values, I, L and H, are saved during the recursive call.

Quicksort example

An illustration of an execution of the quicksort algorithm appears as follows. The far left column contains the original list of ten numbers. The circled numbers are the values used for X, and the number-pairs in rectangles are the values of L and H used to partition the list. Note that the procedure begins with L=1, H=10, X=46. Partitioning in the fifth position then places X. Next the process is called for X=3, L=1, H=4, and X=49, L=6, H=10. The process continues in this way until all values are correctly sorted.



Tree searching

These few examples indicate the ease and convenience of doing recursion in BASIC. Another larger area of application for recursion involves tree searching. This application is especially useful for searching game trees or for other applications that need a strategy to be determined through a choice between alternatives.

ABOUT THE AUTHOR



Herbert Dershem is Chairman of the Department of Computer Science at Hope College, Holland, Michigan. He has a Ph.D. in Computer Science from Purdue University.

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System Designers' Guide to Hard Copy/Printers

R ecent advances in technology have brought new methods to produce and handle hard copies. The introduction of copying, wp and dp has brought us a new style of handling this information. It is just a matter of time until these new technologies will be implemented into a system called electronic desk. Everyday paperwork can then be produced electronically by a word processor which, in general, consists of a keyboard terminal, a display monitor and a printer. Memos, reports and documents are produced and edited on the display screen and stored in memory devices such as mag tape, card or disk, etc. The electronically-stored information can be readily converted into hard copy via a printer whenever needed. With these recent advances in technology, system design is changing; and our perception of how it will change - that is, our design philosophy - will alter radically. The following five excerpts of articles presented at the 1980 Society of Information Display symposium different, but important, aspect of printer cover technology.

Currently, the printer can be of the impact type (daisy-

wheel is common) or the non-impact type (ink jet or laser beam). Both impact and non-impact printers have improved their quality and speed during the past decade. In non-impact printing, technologies such as laser beam and fiber optic CRT techniques have matured and been commercialized. These printers can be located near the work — wp station and can be used to print out information from a magnetic media which is known as an *intelligent copier*. The printer can also be located in a remote place. Magneticallystored information can be transmitted via telephone lines to produce hard copies at these remote locations. This will result in rapid cost/effective communication and in effect, create an *electronic mail* system.

Upcoming services by new commercial satellites and microwave systems will greatly accelerate information transmission, In the near future, the copying machines and computer printers that generate hard copies, the display screens that generate soft copies, the word processors and the data processors will be integrated into a big family — the *information society*.

Computer Output Printing Technologies Donald S. Swatik

Computer Peripherals, Inc., Rochester, MI

This article presents an overview of the trends in computer printer imaging technologies. Widely varying technologies are employed in printers, depending on performance, print quality and cost considerations. These requirements vary by orders of magnitude over the spectrum of printer applications tied to computer systems. Printer performance can be subdivided into three categories based on the character generation sequence utilized. The lowest speed devices are serial printers operating in a character-at-a-time mode at speeds from 60 to 200 cps (20-70 lpm equivalent). Line printers span the medium-speed range and print an entire line at a time in a random-character sequence at speeds from 75 to 3,800 lpm. Finally, the highest speed printers are page printers which instantaneously print in a line-at-a-time mode but can only be stopped and re-started on a page basis. These units operate at speeds from 4,000 to over 20,000 lpm. Each speed range can be further subdivided with respect to the imaging technologies employed as (1) impact or non-impact; (2) matrix or solid-stroke character generation and

(3) plain or special paper. The vast majority of printers in widespread use today print on plain paper and this discussion will be limited to technologies that are capable of imaging on plain paper.

The present serial printer market is dominated by the impact matrix printer. These devices are very cost effective at low speeds due to the simplicity of their design, but are limited by their low print quality capability, high acoustic noise and the high duty cycle to which the mechanical matrix head is subjected. The line printer market has been served by serveral technologies, with drum printers predominately at the lower speeds from 300 to 900 lpm and train printers at the higher speeds from 1,000 to 2,000 lpm. Train printers offer superior print quality and operator changeable font at the expense of higher product cost. New products using interchangeable print bands are available now to bring the advantage of train printer technology to the 300 to 1,200 lpm market. These band printers also have the capability of printing full-length lines on letter-size sheets for paper savings besides printing on standard size EDP forms.

Presently, non-impact printers are receiving much attention; and it is, therefore, useful to review their capabilities

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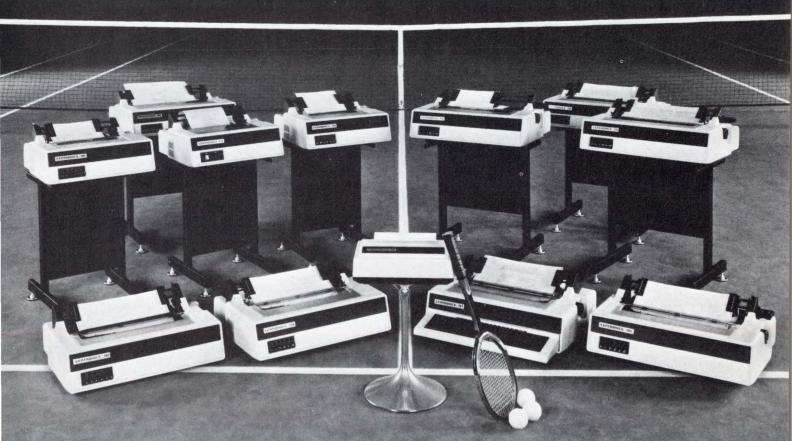
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with respect to impact printers. A major advantage of non-impact technology is the ability to print high resolution images in a very dense dot matrix format at relatively high speeds. This capability combines the high print quality obtained with solid-stroke impact printers with the font versatility of the matrix format, thus allowing for the electronic selection of character set size, style and pitch and maintaining constant printer through-put independent of character set size. In addition, forms printing can be accomplished in parallel with the variable data, reducing the need for special pre-printed forms.

A fundamental difference of non-impact from impact printers is the lack of simultaneous, multiple copy capability. On the positive side for non-impact printers, singlepart paper is less expensive than an equivalent quantity of multi-part forms; and all copies are of uniform "first copy" print quality. On the negative side, a means of producing sets of multiple copies must be provided in many applications. This can be accomplished by buffering an entire job either by spooling at the system level or by storing the job within the printer. Alternately, the program can be re-run "N" times for "N" copies. To maintain equivalent throughput with impact printers, a non-impact printer must, therefore, be "N" times faster than its impact printer counterpart typically by a factor of two to one.

A trend-setting plain paper imaging technology for each class of printer is reviewed; namely, (1) Ink Jet Serial Printers; (2) Band Impact Line Printers; and (3) Laser Electrophotographic Page Printers.

Tactical Hard Copy Image Generation System Larry E. Hand, R. E. Davis and R. J. Straayer Harris Government Systems Group, Melbourne, FL

The hard copy image generator is part of an overall system that we developed for satellite imagery recording in a tactical environment. The system is designed to provide current weather information via real-time, high-resolution film transparencies and includes an antenna, computer-controlled data processing hardware, user terminal, disk drives

for image storage, high speed magnetic tape recorder for satellite signal recording, soft copy display and high-resolution hard copy display.

A significant feature is system processing at a rate of 200K 6-bit samples/sec. These rates permit real-time hard copy recording of a complete satellite pass in less than 15 min. and playback speeds of less than 5 min.

Image generation subsystem

The image generation subsystem (Fig 1) provides wow/

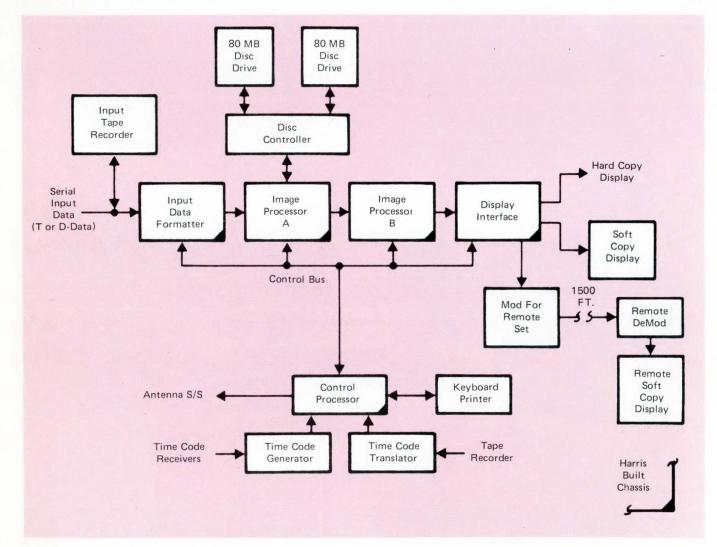


Fig 1 Image generation subsystem block diagram.

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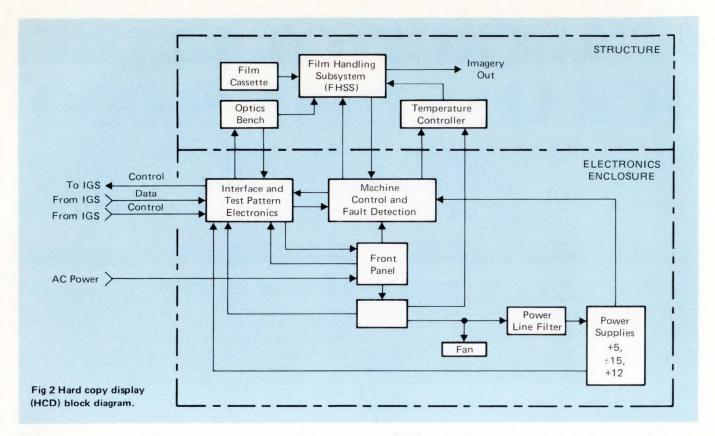
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flutter correction, curvature correction, image contrast enhancement, edge enhancement processing, scaling or magnification, latitude/longitude gridding, and image statistic gathering.

The input data formatter (IDF) corrects for wow/flutter variations of the satellite scanner, performs earth curvature correction and generates a standard image line of 5520 pixels (picture elements) per line. This module also performs rate buffering of the data for subsequenct pipeline processing.

Image Processor A (IPA) stores real-time satellite data on two 80 Mbyte Winchester technology disc drives for later replay. The gray scale values may be remapped to achieve contrast enhancement and the data is separated into two pipelines which subsequently drive the hard copy and soft copy displays. The soft copy data is derived by averaging pixels in the full resolution data to generate a lower resolution data set which matches the physical display resolution. Following this operation, both data streams are processed for edge enhancement using a 3 × 3 Laplacian mask technique. The IPA also scales the data for 2× and 4× magnification.

Image Processor B (IPB) gathers statistics on the data to provide histogram plots, single point digital values, or single line values. The IPB also overlays the data with latitude and longitude grid lines and calculates the next satellite transmission time and coordinates for tracking purposes.

The display interface (DI) appends the top and side annotation for both the soft and hard copy displays. The data is rate buffered to the hard copy display. The soft copy data is stored in a refresh memory, 128 Kbytes in size. The soft copy is displayed on a CRT monitor as a raster scan display of 480 lines by 504 pixels. The weather image is 345 × 352 samples with top and side annotation filling the remaining area. The system can also overlay the weather image with text strings and weather symbols. The image area can be scrolled up or down as required for the satellite pass.

The four pipeline processors are each connected to the control processor (CP) through a redundant 256 Kbit synchronous data link control (SDLC) serial bus. The CP interfaces directly with the operator, accepts operator commands, and responds by issuing commands to each of the pipeline processors as required.

Hard Copy Display

The hard copy display (HCD) (Fig 2) receives a video input from the image generation subsystem (IGS) and generates a high resolution output image. The image is recorded as a film transparency 11-in. wide and 4- to 40-in. long, using laser scanning of dry process media. This combination permits real-time recording of imagery at 686 lpi and 64 gray shades in a tactical environment. Conventional silver films require wet chemical processing and, as a result, are not well suited to tactical use.

Scanning of coherent laser light offers several major advantages for high resolution image recording. Laser beams can be focused into highly intense spots that are easily controlled in both intensity and position. Coherent, diffraction-limited laser optics offer a longer depth of focus than incoherent systems which have large apertures for light collection.

The optical bench which performs this laser scanning is a fully aligned assembly containing all functions and components required for operation. The output of a rugged 5 mW Helium-Neon laser is split into two separately controlled scan beams: The first is an exposing beam and the second is a unique scan position feedback beam, called the grating beam. The intensity of the exposing beam is modulated by highly efficient acousto-optic device of Harris manufacture. This modulator is operated in a closed loop mode where a portion of the modulated beam is compared to the desired value and the appropriate correction applied to achieve a linear dynamic range of 30 dB at 100 kHz. The exposure and grating beams pass through a beam forming assembly and are scanned by a moving core galvanometer.

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This galvanometer is capable of linear angular sweeps at cycle times down to 20 msec. These scanning beams are, in turn, imaged onto a common flat image plane at slightly separated vertical positions by a flat field scan lens. The exposing beam proceeds out front of the optics bench, through a deviation prism which provides a seal against contamination, and up to the exposing capstan. The grating beam scans in synchronism with the exposure beam, slightly displaced. This beam is folded at the front of the bench and returned to a transparent Ronchi ruling which is located at a position equivalent to the image plane. The intensity modulation imposed by the grating provides scan

beam location information which in turn, permits the exposed pixels to be placed accurately along the scan line.

Up to 300 ft. of unexposed dry silver film is stored in a light tight film cassette. The cassette is easily removable for loadings of rolls of the SM 7869 dry silver film. The film is threaded over exposure capstan rollers and on to the dry rollers. During exposure the copy is driven line by line asynchronously across the exposed platen. Exposed copy is held prior to development in a slack box. When exposure is complete, the copy is cut and driven through the heat developing film processor. The copy is processed at 12 ipm and emerges dry and developed at a catch box.

Optimum Design pF High-Speed Non-Impact Printers Isao Fujimoto

NTT Yokusuka Electrical Communication Lab Kanagawa, Japan

A high speed (15,000 lpm) laser printer was developed for computer peripheral equipment. The printer was designed to use the abilities of the electrophotographic process effectively. The printer prints out kanji characters and has various functions such as variable character size, vertical to horizontal conversion, etc. This article presents an outline of this printer and its components.

A printer for a peripheral has to print out a large number of pages in a definite time and thus must use forms of low-priced plain paper. Therefore, electrophotographic process is applied. Electrophotographic printing techniques naturally suited to high speed printing seem to exist, but the capabilities of each element in the printing process must be improved in order to realize a high speed printer.

As printing speed is increased, printing throughput

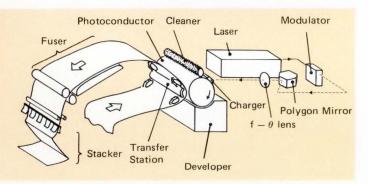


Fig 1 Configuration of the printer.

Table 1. Printer specs

Item	Characteristics
printing speed	. 15,000 lpm (line spacing 3.2 mm)
dot density	. 9.4 dot/mm
printing width	
paper speed	
character size	
	38.5, 77.1 points*
line spacing	. max. 1.1, min.
	33.8 mm
	* 1 point = 0.3514 mm

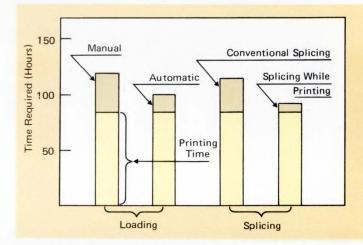


Fig 2 The time required for paper handling (printing speed: 15,000 lpm; sheets printed: 1,000,000 pages).

becomes an important problem. This problem is solved by adopting self-loading forms and splicing during printing.

Configuration

Each element (optical system, developer, forms stacker, etc.) was investigated to improve overall performance and a high printing speed (15,000 lpm) was achieved.

The configuration of the high speed non-impact printer is shown in Fig 1. The optical system is composed of a 30 mw He-Cd laser, a TeO₂ acousto-optical light modulator, a beam correcting f-0 lens and a 12 facets polygonal mirror. These elements of the optical system are fixed on one base in order to keep the optical path steady. The developer has two magnetic rolls. The fuser is composed of fuser rolls and a preheating stage.

The performance shown in **Table 1** is supported by the following technical considerations.

High speed printing

The polygonal mirror rotates at 42,000 rpm on dynamic air bearings and a magnetic floating bearing. Tilting error between facets is less than 5 sec during rotation. Therefore, beam error on the photoconductor surface is less than 0.02 mm with no optical compensation.

The developer, with two magnetic rolls, can handle the printing speed of 89 cm/sec. Temperature fluctuation of the paper at the front of the fuser rolls is less than 5°C because of adequate tension to paper. Fins in the stacker swing forms continuously and refold them without error.

Paper handling facility

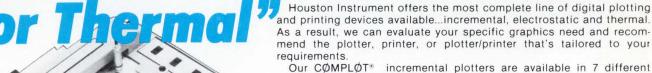
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heavier and handling time comes to be a significant part of printing time. Two methods, therefore, are adopted to overcome this problem.

One is to splice the last sheet of the old box and the first sheet of the new box during printing. The other is to load the first sheet automatically from the transfer station to the stacker through the fuser stage, where high temperature is dangerous. The latter is used for loading the first forms of a job, or when different size forms are used. Fig 2 shows that these techniques reduce handling time by more

than half, a sizeable savings when print speed is 15,000 lpm.

Functions

In Japan, Kanji (Chinese character) are usually used. Thus it is desired that output devices for a data processing system are able to print out Kanji character. The printer has memory for up to 8,000 Kanji character sets and has the following functions; (I) variable character size and variable spacing; (II) vertical to horizontal conversion; (III) printing characters between lines; and others.

Synchronous Jet Ink Droplet Generator Mechanism Richard A. Hein and David E. Lundquist

Computer Peripherals, Inc., Rochester, MI

The synchronous droplet generator is the mechanism used in the ink jet printing to provide a continous flow of ink drops of consistent size and at uniform rate for accurate placement on a suitable recording media, such as paper. This study examines desirable drop generator performance; namely a stable ink stream that forms droplets free of satellites (secondary droplets).

Description

The droplet generator, shown in Fig 1, consists of the following basic elements: ink chamber, piezoelectric crystal, orifice holder and orifice. Pressurized ink supplied to the ink chamber provides a continous stream from the orifice at a velocity determined by pressure in the ink chamber. Stream breakup and droplet formation are enhanced by electrical excitation of the piezoelectric crystal which propagates a pressure wave through the chamber and along the stream axis. Excitation of the piezoelectric crystal at a given frequency causes the stream to break into discrete drops at a unique distance from the orifice exit at the frequency of piezo excitation, provided that the stream velocity is maintained within certain well defined limits.

Using a measurement microscope and stroboscopic illumination phased with the piezoelectric crystal pulses, stream breakup has been observed over a range of piezoelectric drive conditions, while maintaining stream velocity within limits related to orifice size and frequency of droplet formation.

Typically one of the five patterns shown in Fig 2 can be observed at stream breakup. A satellite-free ink stream is

shown in Patterns 1, 2, and 3. Patterns 4 and 5 are not satellite-free. By controlled change in piezoelectric excitation, as shown in Figures 3 and 4, each of the patterns of Figure 2 predominantly occur in the zones indicated.

The most desirable operating zone is satellite-free zone 1. In this zone, variations in piezo drive parameters have minimum influence on stream backup and drop stability. With this objective, piezo drive parameters have been varied

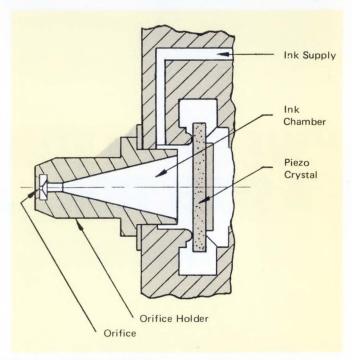


Fig 1 Ink jet droplet generator.

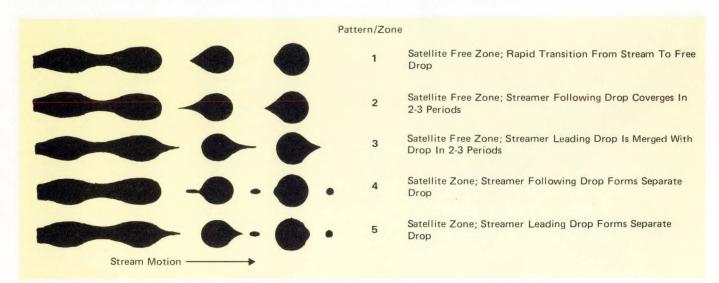
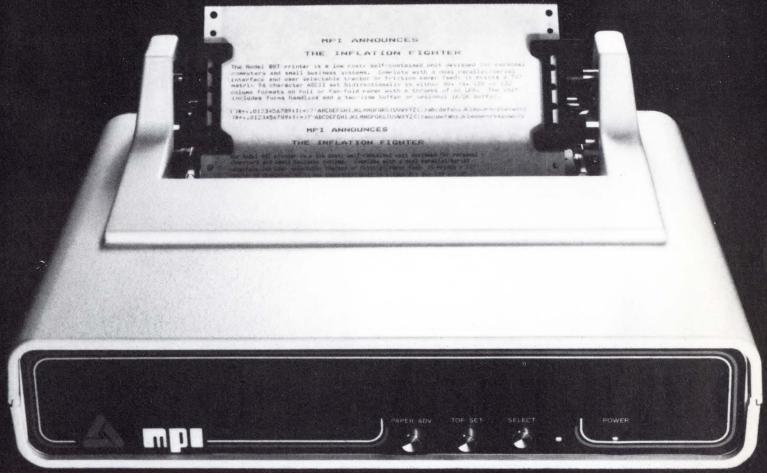


Fig 2 Droplet patterns at stream breakup.

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over a broad range on a number of droplet generator geometries to identify characteristics that yield the largest satellite free operating zone.

Results

Ideally, each generator is expected to follow the solid line curve producing minimum change in stream breakoff distance with changes in piezoelectric excitation. Stream breakup on some droplet generators followed the dashed curves of Figures 3 and 4. Stream observation also confirmed reduced regions of satellite free performance. Detailed inspection of these cases disclosed geometric defects, predomin-

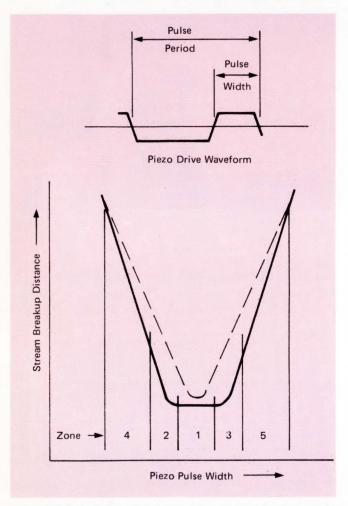


Fig 3 Variation of stream breakup distance with change in piezo pulse width, at constant voltage.

antly interior surface imperfections of the orifice holder and/or non concentricity of the orifice to generator axis as major contributors to non-satellite-free operation. Both defects caused a small angular deviation of the stream from the generator axis, which in turn disturbed the droplet formation process.

A strong correlation exists between drop generator geometric details and stable droplet formation. Performance tests, with observation of stream breakup over a range of piezo crystal drive parameters, has proven to be a valuable tool in the design of a reliable droplet generator for ink jet printing.

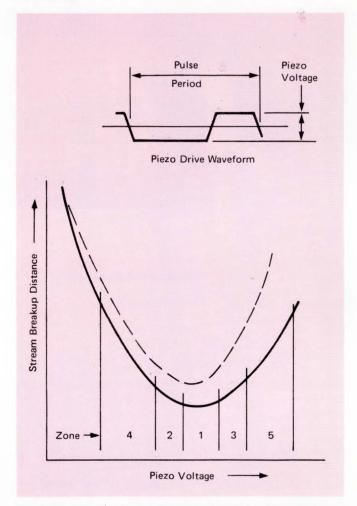


Fig 4 Variation of stream breakup distance with change in piezo pulse amplitude, at constant pulse width.

Hardcopy Techniques in Western Europe Ulf Rothgordt

Philips Lab, Hamburg, W.G.

Softcopy and hardcopy are complementary methods for representing information to the human being. Although in many cases a softcopy will be sufficient for conveying the information, a hardcopy can be advantageous as a short-term storage medium. New services like Videotex are more efficient if a hardcopy unit is connected to the system. For other new services like Telex and Telefax hardcopy output is a must.

Merging of data processing and telecommunications as well as the "Integrated Electronic Office" will lead to a variety of new requirements and technologies for hardcopy output, which may be described with terms like "intelligent copier" or "printer/plotter". There is a world-wide trend to versatile hardcopy devices with high output quality which can be observed in Europe, too.

The technologies for achieving these targets do not differ very much from those used in other parts of the world. There may exist, however, a few specific European contributions that have to be mentioned in the course of the survey on hardcopy technologies.

Impact printers

As for closed-font printers, there is almost no activity in mechanical high-speed printers in Western Europe. In the early '60ies, Siemens developed a drum printer with a unique solution for driving the hammers, which got its

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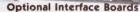
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printing energy from springs on a rotating wheel. These electro-mechanical devices were not reliable.

Today, closed-font printing is restricted to low-speed serial printers used as terminal printers, teleprinters and in wp. The required quality for these applications has resulted in a shake-out of principles, with the "Daisy-Wheel"-printer remaining as the winner. Main part of such a printer is a wheel consisting of up to about 100 spokes, each carrying one character. Printing is accomplished by positioning this wheel and then striking the type face onto the paper by a solenoid-driven hammer. The printing speed of these devices ranges from 15 to 50 character(s), their print quality is excellent.

There is an important European contribution to all these printers in the world since most of the daisy wheels as such are produced in Switzerland by the firms Caracteres SA (\sim 55%) and Tout Pour l'Informatique (\sim 15%). Complete devices are manufactured by a number of companies, among them we find Daisy Systems Holland BV (M 50), Olivetti (TES 401, TES 501), Olympia (ESW 100) and Siemens (Teleprinter 1000).

As for matrix printers, an increased printing speed together with a large number of different characters can be achieved by using a matrix-printing technique. Solenoids are driving needles that are arranged in vertical lines or even in a complete 2-D matrix. The first mechanical matrix printer appeared on the European market in the late '60ies. It was used in the desk-top calculator Philips P251. The characters were composed of a matrix with 7×5 dots. This rather low resolution resulted in a poor printing quality. Main aim of the development in the following years was to increase print quality and speed. Philips is now offering a number of matrix printers with different concepts. A line printer for

400 lpm employs a shuttling bar that carries the needle-driving solenoids for a 9×9 character matrix. Other printheads (PACT 200, PER 3100) for serial operation consist of 7 or 9 vertically arranged needles. The most advanced model is the MPR 18 with 18 needles for the vertical strokes. This printhead is capable of printing in correspondence quality. Highest quality is achieved by a two-pass mode.

Similar principles and qualities can be found in printers from Binder (4132 kP), whereas Facit uses in their 4540 a somewhat different approach. A printhead with a full matrix of 35 needles is manufactured by RENA.

Non-impact recording techniques

The variety of principles used for non-impact hardcopy generation is much higher than for impact printing. A more detailed description of these techniques is given below. Starting from lower speed techniques like ink jet and thermal recording up to laser beam printers, most of the known principles can be found in European equipment. Only two of these methods deliver a hardcopy on plain paper, i.e. the ink jet and the electrophotographic systems. Most of the non-impact recording techniques are employing paper that is adapted to the specific process, like heat-sensitive paper for thermal printing, etc.

Ink-Jet Techniques. Ink-jet printer development started in Europe already in the early '60ies with a low-pressure x-y-deflection systems. Later on high-pressure systems with special modulation techniques as well as a droplet-on-demand system have been invented in Sweden. The work of Hertz resulted in color plotters of excellent quality. Stemme's approach of a low-pressure droplet-on-demand system has been taken over and modified by several indus-



trail companies, among them, e.g., Matsushita.

Other droplet-on-demand systems have been developed by Siemens and Olympia. In its PT 80 Siemens has combined 12 tubular piezo-electric transducers in a printhead, the nozzles being arranged in two vertical lines. The latest development of Siemens is a color printer especially for Videotex applications. Olympia, too, offers an ink-jet printer with 12 nozzles, but with flat transducers.

Thermal Printing. Thermal printers become more popular, especially those with a comb-like printhead as opposed to those with a moving one. There is a trend to hybrid structures with thickfilm resistors as thermal writing elements and driving transistors on the same ceramic substrate. This technique is not only used for printers but also for plotters and for telecopiers (facsimile devices). Asea Hafo in Sweden is one of the most prominent manufacturers of thermal printheads. Philips has announced their "Copy 80", a thermal printer for 80 characters/line.

Electrosensitive recording. In the electrosensitive or "burn-off" recording process the white or metallic surface of a paper is removed in response to a voltage applied through a wire stylus, revealing a dense black underlayer. There are several European manufacturers of such papers. In Germany, Robert Bosch GmgH is producting its Al-coated RMP-paper, used in devices from Walther (DE 100), Olympia (NMD 40) and others. The low voltage of 10 to 40 V necessary for marking this kind of paper makes it possible to arrange a large number of styli in a comb-like structure and to control these styli individually. In the U.K., Nig Banda is manufacturing an electrosensitive paper with a white surface that is mainly used in drum-type facsimile equipment, e.g. the Hell-Fax HF 1048.

Electrostatic recording. Electrostatic recording is a two or

three step process, where in the first step a change image is produced on a dielectric coated paper by means of some kind of electrode array. The second and third steps make a visible image of the latent charge image by applying dry or liquid toner. There are several European manufacturers developing printers and telecopiers based on the electrostatic process. Philips is offering desk-top transceivers (P-FAX 2002 and 2003) that correspond to the CCITT group 2 and group 3 recommendations, respectively. Application of this technique for hardcopy output from CRT display terminals or Videotex systems seems possible. Advantages of this recording technique are its high speed and the high printing quality on a paper which looks like plain paper.

Some resemblance to the electrostatic printing process can be found in the electrophoretic recording technique, which allows a real continuous-tone reproduction, a feature not available with most other non-impact recording techniques.

Electrophotographic printing. Electrophotographic printers, sometimes called laser printers, are one of the latest high-speed printer developments. Based on the principle of plain-paper copiers, the exposure of the electrophotographic drum is being done by an electronically modulated and mechanically deflected laser beam. Siemens has developed such a printer which is now sold as 3352/ND 2 Laser Printer. New developments aim at replacing the laser beam by other illuminating means like solid-state lasers, CRTs and light-modulating arrays.

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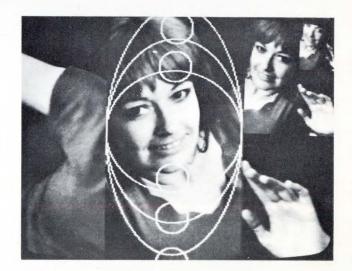
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Communicating Data With Protocols

n the increasingly sophisticated world of data communications, the use of protocols to establish data format is becoming more important and prevalent. While communications from a "dumb" peripheral to a processor can easily be conducted by a simple UART (Universal Asynchronous Receiver/Transmitter) or USRT (Universal Synchronous Receiver/Transmitter), for long distance links between intelligent devices (processors, etc.), an error checking protocol which can relieve some of the host software requirements is necessary. This article describes types of protocols, their basic formats and the information provided and required by each protocol to communicate with the computer. There is also some discussion of advantages and disadvantages of the protocols and the types of error checking used with each protocol.

First, some definitions

Before further discussion of what protocols are, a few words on what they aren't. Data communications protocols do not specify what method is used to transfer data (i.e., RS232, RS422, CCITT, etc). These methods are specified by standards set by the Electronic Industries Association or Comite' Consultatif Internationale de Telegraph et Telephonie. Protocols also do not control data rate. Serial data transfer rates, which are generally between dc to 19.2 kbaud, and modems less than or equal to 9600 baud are often selectable

by software. What data communications protocols do specify is the format in which data is transferred.

Two main ways of transferring data are serial data transfer and parallel data transfer. Parallel data transfers are easily handled by direct memory access (DMA), are typically asynchronous and do not require error detection. Serial data transfers are handled under interrupt control with some exceptions, are typically synchronous, and use some type of error detection.

Protocols are used to transfer data serially across a data communications link (Fig 1). Serial data transmission is particularly advantageous as the distance of data transfer increases. Although parallel transfers are obviously faster and may be desirable over short distances, serial transmission is not as likely to fail and is often less complicated for the programmer. For short distances, you do not typically use error detection; protocols typically used in longer distances provide a way to solve error problems encountered.

One problem found in transmitting serial data asynchronously is the clock skew encountered between the transmitting station and the receiving station. Data transmission of this type can be generated by a UART (Fig 2). A USRT may be used to prevent skewing problems by generating a clock signal, which is used by the receiving station to decode the message, along with the data message.

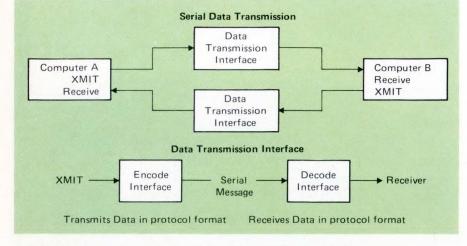


Fig 1 Protocols transfer data serially across a data communications link.

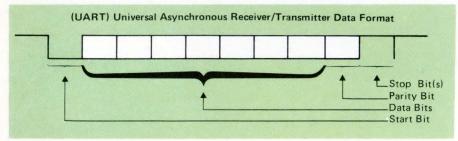


Fig 2 Serial data transmitted asynchronously can be generated by a UART.

Two groups: BOP and BCP

Generally, protocols are divided into two basic groups — bit oriented protocols (BOP) and byte control oriented protocols (BCP). Some BOP examples are:

SDLC - Synchronous data link control

ADCCP – Advanced data communication control procedures

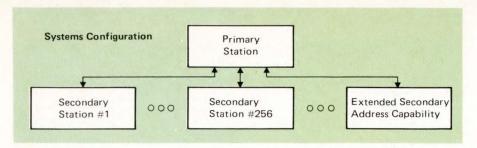


Fig 3 Bit-oriented protocols are transmitted in frames as shown here in this system configuration.

HDLC – High-Level data link control

BDLC - Burroughs data link control

BCPs include:

DDCMP — Digital data communications message protocol

BISYNC – Binary synchronous communications

Protocol-oriented interfaces are often required to handle both bit- and byte-oriented protocols, thus providing maximum system flexibility. Bitoriented protocols are transmitted in frames (Fig 3). The system configuration using BOP consists of a primary station with up to 256 secondary stations. Some protocols, such as ADCCP or HDLC, can increase the number of secondary stations to exceed 256 secondary stations by using an extended address. This is accomplished by using a 16-bit address field instead of an 8bit address field. Each frame (Fig 4) starts with a flag of 8 bits (01111110).

A frame may be followed by another frame, another flag or idle. When a frame is immediately followed by another frame, the ending flag of the first frame is also the starting flag of the next frame.

To prevent an unintended flag from occurring in the middle of a frame, a method of "zero" insertion and deletion is used. Anytime five contiguous "ones" are in a data stream, a "zero" is inserted after the fifth "one."

Following the flag is the address field, which is used by the primary station to designate the secondary station for which the frame is intended. Therefore, it is necessary for each secondary station to be able to decode the address field in order to determine if the frame is intended for that station. The address field is also used by the primary station to determine which secondary station generated a frame. In this case, the secondary station must place its address in the address field when sending a frame to the primary station.

Following the address field is the control field. The control field represents one of three types of format:

- 1. Information Transfer Format
- 2. Supervisory Format
- 3. Nonsequenced Format

The information format is the frame sequence number of the data. Each frame is numbered sequentially so that the station may determine if any previous messages are missing and request retransmission if required.

A Send Sequence Frame Count and a Receive Sequence Frame Count are used to determine how many frames are in a transmission. A Poll/Final bit is set by the primary station to authorize transmission. The Poll/Final bit is set by the secondary station in response to the sequence completion. Each frame sent to the secondary station

from the primary station has a sequence number and the Poll/Final bit is set to zero. When the primary station is finished and ready for the secondary station to respond, the Poll/Final bit is set to one. The secondary station then responds with a number of frames in which the Poll/Final bit is set to zero. When the secondary station is finished, the Poll/Final bit is set to one. Therefore, the Poll/Final bit is used to determine when data transmission from a station is finished.

In the supervisory format, the first two bits determine that the format is indeed the supervisory format. The next two bits indicate the type of command. After the type of command, a Poll/Final bit is sent, followed by a receive sequence frame count. Three basic commands are used:

Receive Ready (RR) is sent by a station to indicate that all sequence frames up through the receive sequence count minus one are correct and the station is now ready to receive more.

Receive Not Ready (RNR) indicates a temporary busy condition; no additional frames that require buffer space can be accepted.

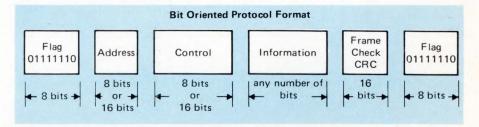


Fig 4 Each bit in this bit-oriented format starts with a flag that has 8 bits in a binary sequence 01111110.

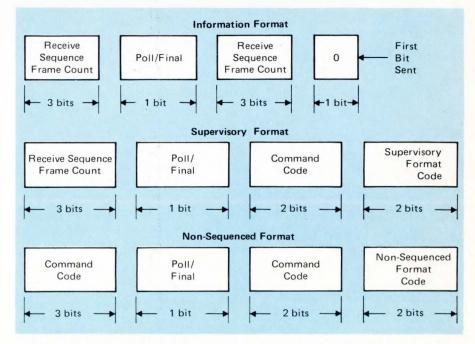


Fig 5 Messages are transmitted in a format that consists of a hearer, a body and trailer field.

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Reject (REJ) is used to request transmission or retransmission. Reject is also used to acknowledge receipt of a receive sequence frame count minus one, indicating the station is ready for more.

In the nonsequenced format, the first two bits determine that the type of format is the nonsequenced format. Following the format is a Poll/Final bit and five bits which are used for the command code; up to 32 commands and 32 responses are possible.

Following the control field is the information field. The information field varies in length and may include a number of sequential frames to complete a transmission. Data can be configured in any code structures such as binary, binary coded decimal (BCD), EBCDIC, ASCII, etc.

Following the information field is the frame check sequence (FCS), which is used to detect errors which may occur during transmission. The content of the FCS field is determined by the cyclic redundancy check, CRC-CCITT, which is based on the polynomial $G(X) = X^{1.6} + X^{1.2} + X^5 + 1$.

The transmitted data is divided by the generator polynomial and the FCS is the complemented remainder. All the data transmitted after the flag is used to calculate the CRC, excluding zero bits inserted to prevent an unintended flag. The closing flag indicates that the previous 16 bits were the frame check code. The FCS is followed by a closing flag sequence 01111110.

A primary advantage of using a BOP is that there are no restrictions on the data codes used. In addition, a BOP does not require any special set of characters for control, is not concerned about peripheral control and is operable with full duplex or half duplex. Also, error checking and correction is available on a complete frame.

But there are disadvantages as well. The header of a BOP is relatively short and a buffer of appropriate size must be made ready by the operating system on relatively short notice. It may become necessary to limit the message length to a maximum number of characters. In addition, the transmitting station cannot transmit an idle in the middle of a message because it will cause an incorrect character count and produce a bad CRC check.

Byte-control oriented protocols (BCP)

IBM "BISYNC" provides an example of a character-oriented Binary Synchronous Communications Protocol. Messages are transmitted in a format consisting of a header or control field, a body or text field and a Trailer or Error checking field (Fig 6).

Bisync requires two sync characters to assure proper sync at the start of the message. Each sync character consists of 8 bits. Following the sync characters is the header, which starts with an 8-bit Start Of Header (SOH) command. Following SOH is the header, or control, field. The header field starts with the address of the station receiving the information or source. Following the address is the block sequence number or job number, and following the job number are the concharacters which determine whether the following message is data or a control action. The acknowledgment following the control character insures error free reception of messages received previously. Control information is sent using special characters or character sequences.

Following the header is Start of Text (STX), the text field which contains data information or control information, and End of Text (ETX) followed by the block check used for erfor checking. Some of the communication characters are:

End of Transmission Block (ETB): Used to indicate the end of the text field. ETB is followed by the block check code.

Intermediate Transmission Block (ITB): Used as the end of the block; block check to follow.

End of Text (ETX): Used to indicate the end of the text field; no more data blocks.

Negative Acknowledgment (NAK): Indicates that the previous block received was in error. This informs the program that it will have to retransmit.

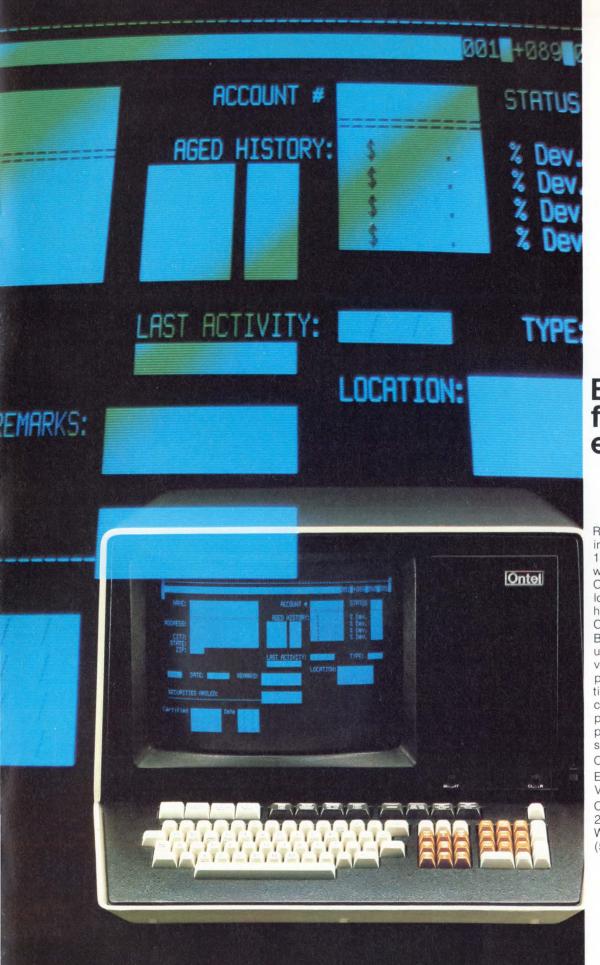
Data Link Escape (DLE): Used during transparent text transmissions for control purposes.

Affirmative Acknowledgment (ACKO or ACK1): Indicates that the block was received error free. ACKO is for an even number of blocks and ACK1 is for an odd number of blocks.

Types of codes supported by Bisync are ASCII, EBCDIC, and SIX BIT TRANSCODE. Error checking used with Bisync are Vertical Redundancy Check/Logitudinal Redundancy Check (VRC/LRC) or Cyclic Redundancy Check (CRC). VRC is used with the ASCII code on each character and LRC is used on the entire message.

The EBCDIC code uses CRC for the entire message; CRC-16, a 16-bit CRC consisting of two 8-bit character transfers, is used.

The six bit transcode code also uses



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CRC for the entire message; in this case, CRC-12 which is a 12-bit CRC consisting of two 6-bit transcode transfers, is used.

If an error is detected, NAK is generated. If an error occurs, Bisync requires retransmission of the blocks. A positive acknowledgment, ACKO or ACK1, is generated if no error is detected.

Bisync requires stripping SYNC characters so that the CRC will not compute SYNC characters along with the message. Control characters are also excluded from the CRC.

Transparent text distinguishes between the control characters (as listed above), the peripheral control characters such as carriage return (CR), line feed (LF), back space (BS), and graphic characters, such as alpha characters, numeric characters, and special characters and symbols, which are normally used with terminals. Transparent mode sequence is distinguished by inserting DLE characters at the start of the transparent mode sequence; type of characters to follow is defined

as one of the group previously specified.

Sync characters are sent when no data characters are sent. In the transparent data mode, the sync characters can be confused as data characters; to prevent this, DLE is inserted in front of the sync characters. This implies that something special is coming and both DLE and the sync character are disregarded.

One of the advantages of Bisync is that you can transmit idle characters, impossible using other protocols.

On the other hand, Bisync can only transmit in half-duplex, not full duplex; and the protocol is continually acknowledging which results in wasted time. Also, Bisync requires more time to generate individual control characters than BOP.

Another byte-count-oriented protocol is DDCMP (Fig 7). In DDCMP the messages are transmitted by means of a header field, information field and error checking.

Two sync characters are required at the beginning of a message to assure proper sync. Following the sync characters is a header. At the beginning of the header is an eight bit start of header character (SOH). The control data following SOH is a 14 bit field which can be used to indicate the number of characters that will follow in the information part of the message or can be used as control. When used as control, the first eight bits are used to indicate the type of control message and the last six bits (usually all zeroes) are used to specify the reason for NAK.

Following the count or control field are two flag bits which are used as quick sync and select flags. The quick sync is used to inform the receiving station that the message will be followed by sync characters, allowing time to engage a sync stripping capability.

The select flags indicate the last message, enabling the station addressed to transmit. This is useful in a half-duplex or multipoint where transmitters need to be turned on and off.

Following the flag bits is the response field. These bits are used in data messages to indicate the number of the last message correctly received for positive or negative acknowledgment of types of control messages.

Next comes the sequence field, the bits of which are used as data messages where the sequence bits indicate the number of messages assigned by the transmitter. They can also be used with REP to specify that all messages up to a number specified have been received.

The address field which follows the sequence field is the address of the station receiving the information.

Error checking using the CRC-16 cyclic redundancy check follows the address field. DDCMP does not require acknowledgment for each message. Special NAK or ACK characters can be used to specify the sequence number of the last good message received.

DDCMP can be used in full or half duplex. When a message is sent out of sequence, an REP message is sent containing the sequence number of the most recent unacknowledged message sent to the station. The receiving station acknowledges the REP message. An NAK is sent if the REP is not received. DDCMP allows up to 255 unacknowledged messages.

Protocol oriented interface

The data transmission block is used to interface the computer to the serial transmission lines. Data comes from the computer bus in parallel form and is converted by the interface into serial

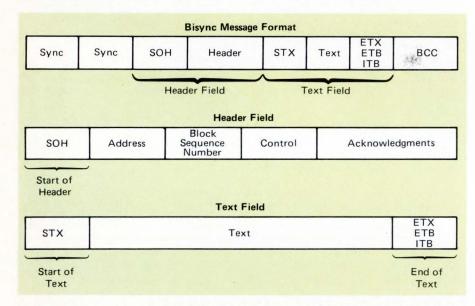


Fig 6 Bysync transmits only in half-duplex, and the protocol is constantly acknowledging, thus wasting time.

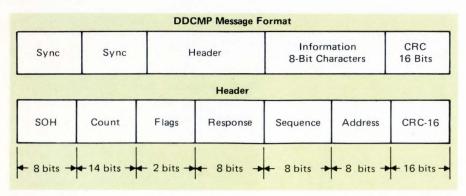
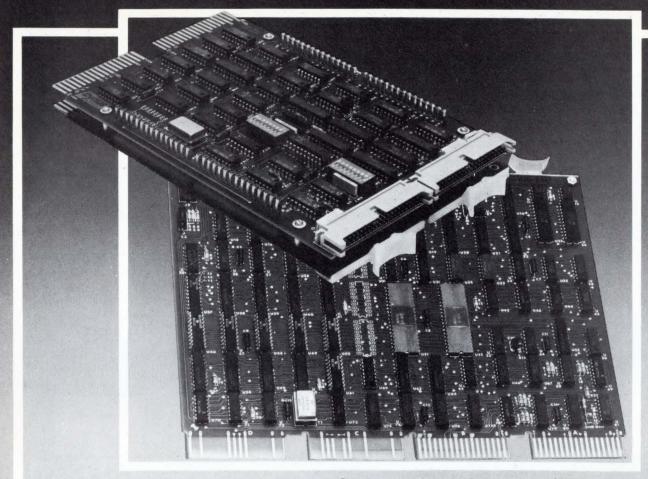


Fig 7 DDCMP is a byte-count-oriented protocol, with messages transmitted by means of the header field, (as shown), information and field and error checking.



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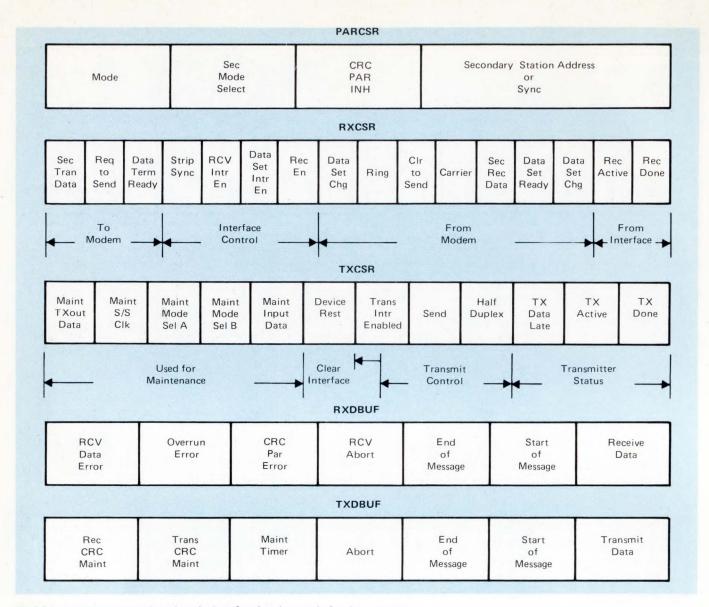


Fig 8 Status registers determine when the interface has data ready for the computer.

form, based on a specified protocol. Data is converted in the format which the computer expects to receive.

The computer must provide the interface with the information necessary to send and receive messages. One means of accomplishing this is the use of basic I/O registers associated with the interface device address. Although there are many ways to program interfaces and various types of interfaces to accomplish this task, one example will be discussed.

Let's examine a typical synchronous communications interface designed for Unibus computers. The principles can be applied to other interfaces. The interface provides parallel-to-serial and serial-to-parallel data conversion, EIA level conversion, modem control for full or half-duplex operation, protocol management and bus interface. As noted above, the interface will accommodate bit and byte oriented protocols.

The interface consists of five registers; a receiver control status register (RXCSR) which is a read or write register, a receiver data buffer register (RXDBUF) which is read only, a parameter control status register (PARCSR) which is write only, a transmitter control status register (TXCSR) which is a read or write register, and a transmitter data buffer register (TXDBUF) which is a read or write register.

The computer is informed by the interface under interrupt control when the interface is ready to transmit data or when the interface has data ready for the computer. This information can also be obtained by reading the appropriate status registers (Fig 8).

The first thing necessary when using a protocol interface is to set up the PARCSR. This register is used to tell the interface which protocol is desired, whether CRC is wanted or not, if a secondary address mode is selected

and to define the secondary station address or sync character (depending on which protocol is selected; BOPs use a secondary station address and BCPs use a sync character).

The RXCSR and TXCSR registers are used to set up control conditions and report status conditions.

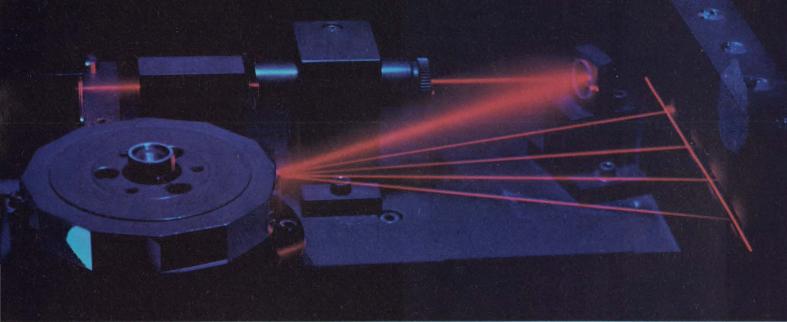
All control signals sent to the RXCSR can also be read from the RXCSR. The RXCSR is also used to provide modem status information and interface status.

The RXDBUF is used to report error conditions and control information, and also contains the data received.

The TXDBUF register is used in maintenance, control messages and the data to be transmitted.

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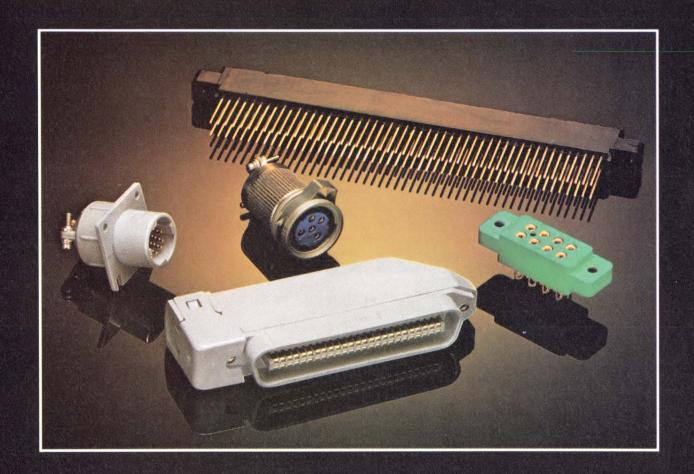
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Product Close-Up

Printer/Plotter Captures Color Graphics on Plain Paper

Bob Hirshon, Assistant Editor

Each new advance in systems electronics begs the invention of another: new low-cost, high resolution color graphics displays seemed somehow incomplete without a means to make hard copy of the images.

One answer, introduced at last year's NCC, is Trilog's Colorplot-100 plotter/printer, providing color hard copy from graphics terminals quickly (3 min/copy) and inexpensively (25-40 cents/copy, including ribbon cost). Colorplot's image quality isn't on a par with that of photographic hard copy units produced by Dunn and Matrix. However, lower cost per copy — less than one tenth that of phototechniques — plus added versatility of printing capabilities have given Trilog's entry a ready market.

To keep pace with that market, Trilog recently introduced a second model of the Colorplot (which can now properly be called a series), the Colorplot-144. The C-144 is a C-100 specifically adapted for use with a Chromatics color graphics terminal.

Both of Trilog's Colorplots use raster scan impact technology. The printing head is a horizontal bar 13.2" long equipped with 44 leaf spring printing hammers, spaced at 0.3" intervals. This bar shuttles back and forth on a 0.3" path, printing a line of dots, at 100 dots per inch, with each sweep. Printing is bidirectional; when the printing head reaches the right, the paper advances one plot row and the bar prints the next line of dots right to left. Each horizontal line takes 40 msec.

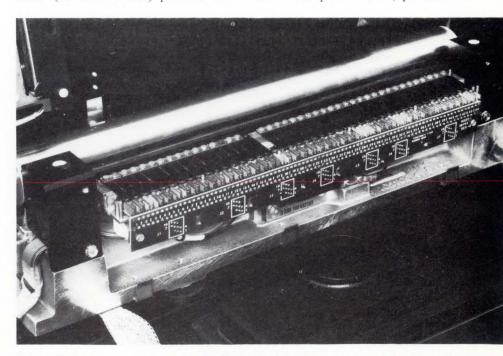
Colorplots use a three-color ribbon, consisting of twenty-yard lengths of

yellow, magenta and cyan (aqua), the three reflective primary colors, laid end-to-end. Each twenty-yard strip is coded with a pattern of perforations, so the software can go into a search mode to find whatever color is indicated.

Trilog's plotters print one color at a time: first, the print head lays down all the yellow on the page; then, tractors back the paper up to the start, and the print head plots all the magenta; finally, the cyan is printed. Alternating dots of any two of these colors yields three more colors (red, green and blue). Adding white (no ink) and black (all three colors) provides the

machine with eight-color capability. For regular printing applications, a standard — and less expensive — black nylon ribbon may be substituted.

Backing the edge-punched, fanfold paper up accurately enough so that dot rows could be overlaid was the biggest difficulty in designing the system. With dot rows a scant 0.01" apart, each dot had to be delivered within 0.005" of its mark to produce a clear image. This meant keeping the paper tight, but not so tight that the edge perforations were elongated. Two adjustable tractors, one above and one below the print station, provide this



Bank of 44 leaf spring printing hammers. Spring-tensioned hammers are held by a permanent magnet; a single dot is impacted by electromagnetically releasing one leaf spring.

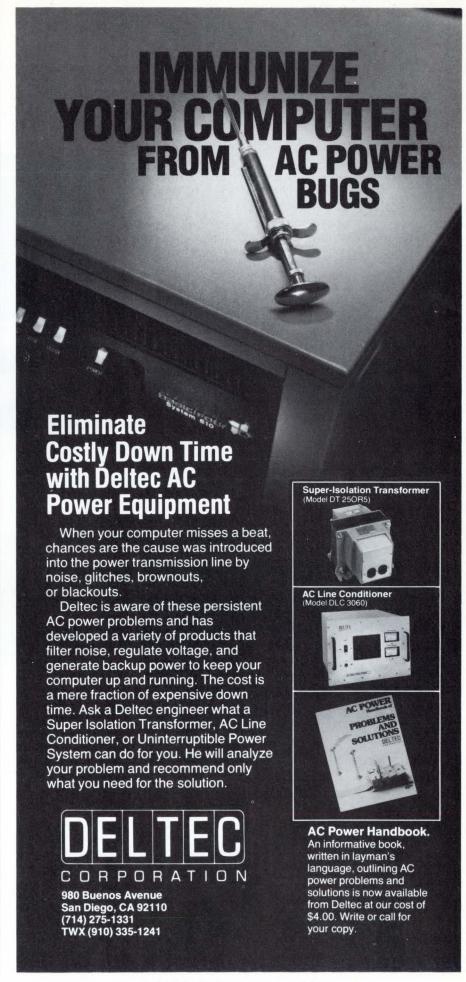
capability. Driving the top tractor is a bidirectional stepper motor. The lower tractor, run by a VC motor, is logic controlled to provide proper torque at all times, maintaining optimum paper tension.

Resolution of the C-100 is 100 dots per inch vertically as well as horizontally. Unfortunately, the Chromatics terminal that Trilog wanted to handshake produced a 512 × 512 pixel rectangular image; translating that signal straight through a C-100 would result in a distorted, stretched-out image on the hard copy. To match the aspect ratio of the Chromatics terminal, Trilog needed a unit with a resolution of 144 dots per vertical inch, and designed the new C-144 to meet that need.

Designing the C-144 required alterations of the paper-handling electronics to step the paper at 1/144" intervals rather than 1/100" intervals. Then, since this is a printer as well as a plotter, a new font had to be designed to accomodate this new spacing. For the C-144, Trilog retained the same 7 × 9 font matrix used in the C-100, but reduced the resolution to 72 dots per vertical inch. In the print mode then, the C-144 uses only every other plot row. Although this lower vertical resolution results in lower quality characters, it allows the C-144 to print at a brisk 190 lines per minute. Printing on all 144 plot rows would cut this speed in half.

Dots are 1/50" in diameter, so there's considerable overlap, even at 72 dots per inch. In print mode, this results in smoother characters, with less of the scalloping characteristic of dot matrix printers. In the plot mode, however, this overlap must be taken into account when comparing Trilog image clarity with that of other image reproduction techniques. For example, a 100 dots per inch Colorplot image can't be expected to provide the sharpness of a 100 dots per inch magazine illustration. Since resolution figures give only a vague idea of actual image clarity, comparisons should be made based on actual hard copy and not on numbers.

A continuing problem encountered by Trilog has been the inability to get a good quality black by mixing the three ribbon colors. Currently, black areas on graphic display terminals translate to a muddy color on the Colorplot. This Fall, Trilog will introduce a four-color ribbon that includes black, which should neatly alleviate the problem. Trilog, Inc., 17391 Murphy Ave., Irvine, CA 92714. Ph (714) 549-4079.



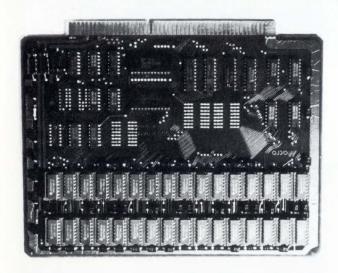
New Products

ROM/RAM BOARDS. The MAC-111 CPU memory board handles up to 16 kB of ROM and 16 kB of RAM. Specs include: 8-bit word size; 450-ns access time; +5V 1.8A. MAC-112, a dynamic RAM CPU memory board, handles up to 64-kB of dynamic RAM. Specs include: 250-ns access time; +5V 2.2A, -5V 0.8A and +12V 1.2A. Prices: 20%-30% below competitive boards. BK and Associates, Ltd., 11891 Martha Ann Dr., Los Alamitos, CA 90720. Circle 173

MONOCHROME CRT DISPLAYS. Two new 12-inch video displays provide the low voltage DC power required for terminal logic circuits; power is scan-derived from horizontal deflection circuit of display. Model DT12-LF has a "flux-nulled" 120/240 volt line transformer which minimizes CRT-flux interaction. Scan-derived terminal supply voltage is essentially constant from 98V to 134V AC input. Model DT12-ZF has input voltage of 120 AC. Its power supply is driven by line operated regulator and horizontal circuits. Also introduced is a new display in the DT12 series for composite video which provides interface with a standard RS-170 signal. Units are available with hybrid integrated circuits (H.I.C.), enabling the displays to be modified to meet special customer needs. Zenith Radio Corp., 1000 Milwaukee Ave., Glenview, IL 60025. Phone (312) 391-8181.

Circle 160

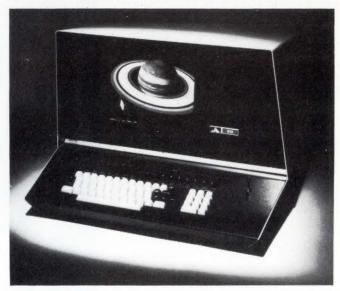
8085 BOARD. A general-purpose μ C, the MAC-011 has 8 kbyte of RAM, 8 kB of ROM, 8155 UART and 8-level interrupts. A dedicated monitor in 4 kB of ROM aids software development and debugging. It provides support I/O rou-



tines for typewriter, CRT, etc. Clock is 3.072 MHz. Prices: 20%-30% under competitive CPU boards from Intel. **BK and Associates**, Ltd., 11891 Martha Ann Dr., Los Alamitos, CA 90720. Circle 172

COLOR DISPLAY. Features include half-second image transfer, continuous joystick panning, full palette of 256 possible hues, and largest refresh memory of any imaging display system on the market. In one frame the AED512 enables up to 256 different hues or 256 shades of gray or 16²⁴ different hue/saturation/intensity combinations to be displayed. Integer zoom from 1:1 to 16:1 can be programmed independently, both vertically and horizontally.

Can be supplied as either a computer peripheral under direct memory access (DMA) control or as a telecommunications terminal that can communicate serially via an RS232C interface or 20 mA loop. Also can be connected



to AED double-density floppies, Winchester technology and mass storage disk pack subsystems via associated minicomputers. Alternately, system can be operated in direct video memory access mode, in either 8- or 16-bit parallel fashion, over bidirectional TTL data lines. Data rate capability of approximately 1 MB per second enables complete data transfer to or from the terminal in 0.5 second. Resolution is 512 horizontal by 480 vertical (512 x 512 optional). Model AED512 (single memory plane; no monitor), \$7100. Monitor, additional memory planes and various interfaces available. Delivery 12 wks after receipt of order. Advanced Electronic Design, Inc., 440 Potrero Ave., Sunnyvale, CA 94086. Phone (408) 733-3555.

WIRE-WRAPPING KIT. Includes a wire wrapping tool, a 50' roll of wire-wrapping wire, two 14-pin and two 16-pin DIP Sockets, and a new high quality PC Board. Model WSU-30 wraps and unwraps 30 AWG wire on .025" square pins, plus strips 30 AWG wire. The new board has 22/22 edge connector contacts on standard .156" spacing. Model WK-3B is \$16.95. O.K. Machine and Tool Corp., 3455 Conner St., Bronx, NY 10475.

8-INCH DISK DRIVES. Two models offer unformatted capacities of 6.9MB and 13.9MB. Both have track capacities of 11.3Kb with corresponding sector capacities of 256B. In addition, both offer recording densities of 7,300 bpi, with MFM recording method. Data transfer rates are 889KB/sec, with NRZ as the data transfer form. Average access time is 70 msec, with a maximum of 150 and a minimum of 30 msec. Average latency is stated at 8.4 msec. The two models offer 230 recordings plus a spare cylinder. Both units utilize a direct drive DC motor, operating at 3.557 rpm. Mountable in either the horizontal or vertical position, the units are completely sealed against dust and adverse environment, and suspended in mounts designed to resist shock. Models DK801-1 and DK802-2. Hitachi America, Ltd, 100 California St., San Francisco, CA 94111. Phone (415) 981-7871. Circle 163

Listen, listen, listen.



You're constantly demanding better and better features from smaller and smaller rigid disk drives. We hear you.

We're responding with our new 8-inch, 20-megabyte D8000. It fits right into the slot now occupied by your 8-inch floppy drive, and it has the easiest and most flexible interface of any drive in its class.

Pertec® gives you Winchestertype technology that keeps contaminants away from environmentally sealed disks and heads. Plus average access time no greater than 50 milliseconds and a transfer rate of 6.914 megabits/second with internal data separation.

The Pertec D8000 does things traditional floppy disks or cartridge drives can't do. Its powerful microprocessor chip handles interface, spindle speed, position control and a variety of self-diagnostic routines.

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Your demands have finally been heard.



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PERIPHERALS

New Products

INTELLIGENT TERMINAL can operate as a synchronous or asynchronous remote batch terminal over the dialup phone network. Local editing, storage, and processing capabilities reduce host dependency, provide faster response, and improve operator productivity, says the manufacturer. Two microfloppy disc drives totalling 320KB (formatted) allow storage of application software, transaction screen formats, operator-entered data for batch communication with remote host, and data for local



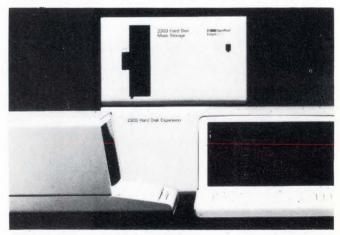
printing. The terminal's Screen Generator software reduces development time for screen formats and also associated data entry and retrieval functions. Software supports all their terminal's video attributes — half intensity, blink, inverse, non-display, and field underline — as well as its extended set of 32 characters for depicting forms. Screen Generator adds field definitions of numeric only, protected and right adjust. Programmer can see each screen as it is built, using the terminal's editing and cursor keys. Model 3500, \$6783. OEM discounts. 60 days delivery. Perkin-Elmer, 360 Rte 206 South, Flanders, NJ 07836. Tel. (201) 229-6800.

MULTIBUS PROTOTYPING CARD AND FORTH. Each Zendex ZX-905 Prototyping Board comes with free layout pads that save a design engineer hours of valuable time. Printed with the top on one side and the bottom on the other, the engineer can lay out his design and pass it on to a technician or assistant for wire-wrapping. Includes 5 edge connectors and enough room for 84 14-pin integrated circuit packs. \$70 ea. in quantities of 5. Also, Zendex's implementation of FORTH is provided, ready to run, in any of a number of Intel's and National's line of SBC-80 CPU cards. It runs completely stand-alone and requires no additional memory, I/O, or disk to operate. Standard features include resident (in ROM) compiler, 8080/8085 assembler, screen editor, and adaptive disk IO. The adaptive disk IO allows a combination of 4 single density drives or 4 double density drives with 2 additional single density units for a total capacity of 2500 screens (which equates to 2.5 MB of source). Complete system price is \$450. Zendex Corp., 6398 Dougherty Rd., Dublin, CA. Circle 148

SMART CRT TERMINAL PLUS A MODEM. The terminal features a 25th status and message line, 22 programmable function keys, expandable definable data, split screen, 13 special characters and printer controls. Controls in TeleVideo allow an operator to move data through the printer via the CRT, talk to host computer via the CRT or move data from host computer to printer. In addition, the controls of the 930 allow an operator to use the CRT while the system is printing information. Model 930, \$1195. Discounts to OEMs. Deliveries beginning 3rd qtr. of this year. The Integral CRT terminal modem, model 9103, is designed for use inside the company's 912/920 model "C" terminals. No other major CRT terminal offers this internal modem capability, says the manufacturer. Designed to fit inside the base of TeleVideo terminals, the 9103 mounts directly on four posts underneath the main logic board. Since there is no acoustic coupler, there is no mechanical vibration or corresponding signal loss, TeleVideo claims. The 9103 is configured to allow the telephone to be used when the terminal is not online, without having to disconnect and reconnect cables. Also, the terminal's numeric keypad becomes the touch tone dialer; the CRT displays the number dialed; the terminal speaker gives audio feedback; the modem's microprocessor remembers the last number dialed and allows re-dialing if carrier signal is lost. The modem board operates at a data rate of 300 baud asynchronously. Model 9103, \$350. (single unit). TeleVideo, Inc, 2149 Paragon Dr., San Jose, CA 95131.

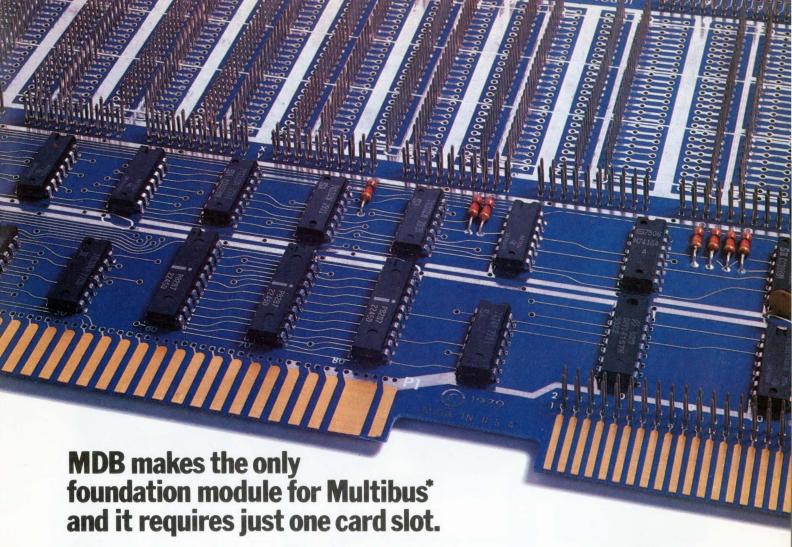
SOFTWARE-TRANSPARENT CONTROLLER meets high density Group Code Replacement (GCR) tape storage requirements of PDP-11/70 computer users. The new TC 70 family from Emulex consists initially of two versions, each of which is designed to functionally emulate the TM03/TU45 magnetic tape controller offered by DEC for handling the 6250 bpi GCR recording format. The controller accommodates all tape speeds and recording densities handled by the applicable formatter — at speeds up to 125 ips and at densities of 800, 1600 or 6250 bpi. Two units of the series were available for deliveries in June and each carried a price tag of \$6,000 in quantities of 50 or more. Emulex Corp., 2001 East Deere Ave., Santa Ana, CA 92705. Circle 141

HARD DISK/FLOPPY DISK. The 2303 Mass Storage system has a 35-MB Winchester-type hard disk and a 1-MB, single-sided, double-density floppy in one compact package. Designed for use with GenRad/Futuredata 2300/2301 uni-



versal development systems and network stations, the new mass storage unit is fully compatible with all existing Gen-Rad/Futuredata systems. A hard disk expansion unit which increases storage capacity to 70 MB is also available. 2303-9000 Hard Disk Mass Storage (includes floppy): \$11,500; 2303-9001 Hard Disk Expansion: \$8,500. GenRad/Futuredata, 5730 Buckingham Pkwy., Culver City, CA 90230.

Circle 139



Imagine what else we can do!

If you've never been excited about a foundation module before, now's the time. MDB offers the industry's first module for use with Intel 16 and 8 bit single board computers. It gives low cost Multibus-to-peripheral interface with complete address and interrupt logic, standard Intel board spacing and room for up to 38 sockets or IC devices of any size on the wire wrap portion of the board. Because all wire wrap pins and components are on the same side of the board, the module requires only one card slot. And it takes any configuration DIP package and provides three 50-pin edge connector positions. In addition, MDB makes a pure wire wrap general purpose module in a single slot configuration which has space for 60 IC positions. This is the kind of flexibility a logic designer dreams about.

If you're not an Intel user, you can still get MDB design flexibility - in single slot bus foundation and wire wrap modules for PDP**-11, LSI**-11, Data General and Perkin-Elmer computers and wire wrap boards for IBM Series/1. Even the dedicated portions of these modules are application adaptable in that they allow a change of functionality by the use of wire wrap pins.

What else can MDB do for you? Look at our line printer controllers. We offer more than 100 computer/printer combinations. If you need communications modules, interprocessor links, multiplexors and PROM boards, we've got them all with the built-in quality MDB is famous for.

MDB interface products are warranteed for a full year; most can be delivered in 30 days or less, and you can buy them under GSA contract #GS-00C-01960. What can we do for you?

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Circle 40 for Intel, 41 for LSI, 42 for PDP, 43 for DG, 44 for PE, 45 for IBM.

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At the Siggraph '79 Show, it was acciaimed as 'The Incredible Graphics Machinel' Since then, the AED512 full-color graphics and imaging terminal has more than lived up to its reputation among sophisticated users. Its ability to display 256 simultaneous colors (from a total palette of 16.8 million) on a 512 x 483 pixel screen; zoom at integer increments to x16; pan continuously via joystick; perform full-screen DMA transfer in 0.5 second; emulate Tektronix 4014 software; allow overlaying TV images with computerized graphics; permit animation by using read/write masks and colorblink make its under \$20,000 price tag seem small. Add to this its unique ability to Superoam an expanded image of 1024 x 1024 pixels and you'll see why the FIVE-TWELVE is features

ahead of the competition. For more information contact Jerry Kennedy, Advanced Electronics Design, 440 Potrero Ave., Sunnyvale, California 94086, phone (408) 733-3555.

TM Trademark of Advanced Electronics Design

Circle 31 on Reader Inquiry Card



New Products

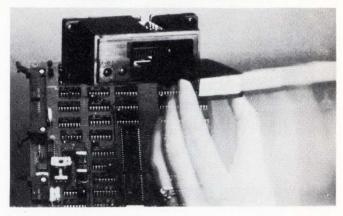
TAPE DRIVE FOR STREAMING BACK UP. Data Electronics' "Streaker" is an OEM digital cartridge tape drive for streaming back-up of Winchester disk drives. The 10 MB and 20 MB low cost tape drives cost \$415 and \$525, respectively. They are described in a new 2-page, 2-color data sheet from the company. The drives use standard 1/4' ANSI/ECMA tape cartridges and transfer data at 5 MB per minute. In addition, "The Streaker" can be mounted in an industry-standard 8-inch flexible disk drive slot. Data Electronics, the world's largest independent manufacturer of digital drives for 1/4" ANSI/ECMA tape cartridges and related systems, has installed more than 19,000 streaming and incremental high-density digital cartridge tape drives, worldwide, for Winchester disk back-up applications. Data Electronics, Inc., 10150 Sorrento Valley Rd., San Diego, CA 92121.

ELECTROSTATIC PRINTER/PLOTTER. For fast, hard copy printing and plotting at low cost, two electrostatic units are now available: Model Z1004 printer/plotter prints at 1000 lpm and plots at 120 ipm. Resolution is 100 dots per inch. Model Z1002 printer has the same 1000 lpm print speed and can be upgraded to the full Z1004 printer/plotter.



Both models support continuous roll and 8-1/2" x 11" fanfold paper. Software and interfaces are available for DEC PDP-11, and Data General's Nova and Eclipse. Printer/plotter is fully compatible with many existing interfaces and software. Printer will accept data in Centronics compatible or RS-232 form. Model Z1002, \$7500; Model Z1004, \$8500 (including software and interface). First deliveries scheduled for September. Nicolet Zeta Corp., 2300 Stanwell Dr, Concord, CA 94520. Phone (415) 671-0600.

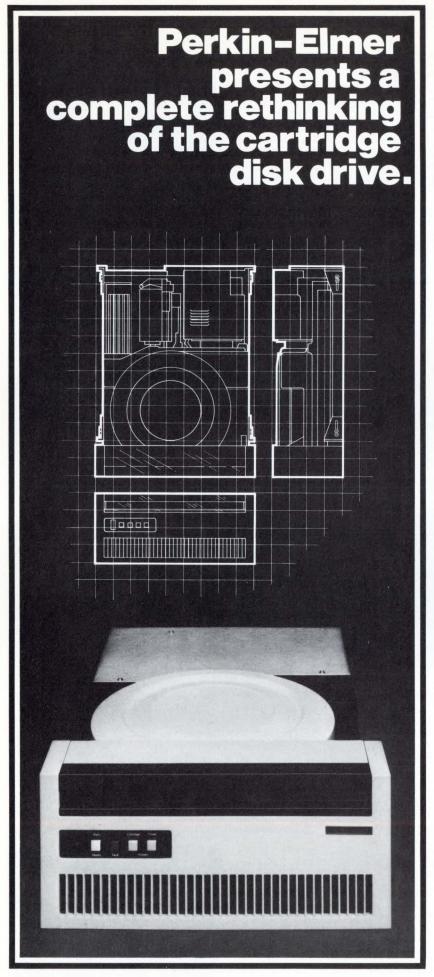
BUBBLE CASSETTE. This portable, detachable bubble memory operates in the same way a tape cassette works with a tape recorder. System consists of: a bubble memory cassette which allows the bubble memory device to be easily loaded and unloaded; a cassette holder unit which combines a linear circuit with a holder into a single unit; and a controller which provides interface with the host system. Up to



8 bubble cassette holder units can be controlled with one interface unit. Each bubble cassette has a capacity of 64k-bit (256-kbit shortly) storage and an access time of up to 0.74 sec. The bubble cassette holder incorporates a linear circuit, coil driver, function driver, sense amplifier, write inhibition device and "busy" check circuit; 8-bit parallel data can be processed (DMA possible) TTL compatible, with the cassette controller interface. Fujitsu America, Inc, Component Sales Div., 910 Sherwood DR-23, Lake Bluff, IL 60044. Phone (312) 295-2610.

OPEN-FRAME SWITCHERS are specifically designed for logic and µP-based equipment with power requirements in the range of 25W to 65W. Designated the OFS65/1 and OFS65/2, the two supplies are adaptable to operation at two AC input ranges - 85/135 Vac and 170/270 Vac over 40 Hz to 440 Hz. Specs are: OFS65/1 (5 V, 6 A; 12V, 1.5 A; -12 V, 1.5A) and OFS65/2 (5 V, 6 A; 15 V, 1.2 A; -15 V, 1.2 A). The 5 V output is adjustable from 4.5 to 5.5 V; all other outputs are fixed, with a tolerance of $\pm 5\%$. Specifically adaptable to microcomputer equipment and smart terminals, the supplies feature a power-loss warning signal combined with a greater than 32 ms full-load, hold-up time to permit protection of information stored in volatile memory. Other functional features include over-voltage protection on the 5 V output and over-current protection with automatic reset. Convection cooling permits operation from 0° to 70° without a fan. \$130 (100-249). Motorola, Semiconductor Products Inc., Box 20912, Phoenix, AZ 85036. Circle 279

PLUG-COMPATIBLE WINCHESTER DRIVES supply 10.4 or 32.2MB formatted, mass-memory for Digital Equipment Corporation's PDP-11 minicomputers and LSI microcomputers at about 40 percent of the cost of similar-capacity DEC drives. Systems are intended for end users with DEC PDP-11 systems, system integrators and small OEMs. The system consists of a microprocessor-based controller/interface, cables and either a Kennedy Model 5300-14 or Model 5300-42 Winchester drive. KSC11 and KSC01 controllers emulate DEC disk controllers and operate with PDP-11/04 to PDP-11/60 minicomputers and LSI-11, 11/2 and LSI/23 microcomputers, respectively. They are software transparent to RT-11, RSTS-E and RSX11M operating systems and are fully plug-compatible with PDP-11 UNIBUS or LSI-11 Q-BUS. Single quantity prices range from \$7325 to \$8725. Delivery 45 to 60 days after receipt of order. Kennedy Company, 1600 S. Shamrock Ave, Monrovia, CA 91016. Circle 167



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To create better back up storage for the office systems of tomorrow, we rethought the role of the cartridge disk drive.

We wanted a totally new cartridge drive that would satisfy systems requirements for backup store and audit trails.

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We built VANGUARD I 24 inches deep for in-desk or rack mounting. We gave it a capacity of up to 20 megabytes and a standard cartridge disk interface for industry-wide compatibility.

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VANGUARD I is everything we think a cartridge disk drive should be. Simple. Reliable. Fast. Universally compatible.

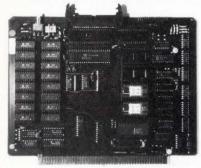
Call or write today for a preview look. And let us know what you think about our rethinking. Perkin-Elmer, Memory Products Division, 7301 Orangewood Avenue, Garden Grove, CA 92641. Call toll free 800-631-2154. In California, call (714) 891-3711.

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MAC-011 CPU Board — (above)
A general purpose microcomputer system

MAC-111 ROM/RAM Memory Board A CPU memory with 16K bytes of ROM and RAM

MAC-112 Dynamic RAM Memory Board A CPU that handles 64K bytes

MAC-211 Digital Input Board
A 32 bit TTL compatible and 4 level interrupt board

MAC-212 Digital Output Board
A 32 bit open collector and 4 pulse

output board

MAC-213 Serial Communication Interface
Board

A synchronous/asynchronous communication control board

MAC-411 Analog Input Board A 16-bit differential voltage A/D

MAC-064 Intel. SBC 80-064 64K × 8 D-ROM (Interchangeable)

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Circle 70 on Reader Inquiry Card

New Products

COMPUTER LOGIC, TESTING AND VERIFICATION. A new title by J. Paul Roth discusses computer logic minimization techniques, testing of logic circuits and verification of both hardware and software, revolving around the cubical algebra. Programs in the book were developed at IBM. Results of sample runs on NASA and IBM problems are presented. Problems in the book serve as a test for an advanced computer design course as well as for self study. Computer Science Press, Inc., 9125 Fall River Ln., Potomac, MD 20254. Circle 154

µC TROUBLE-SHOOTING. Fastprobe. a high-level language software package, runs on a host computer linked to the MicroSystem Analyzer, using industry standard RS-232 serial communication. Interactive software fills the gap between non-programmable testers and costly ATE. Fastprobe controls th MicroSystem Analyzer operation which stimulates the circuit under test and by means of its display guides the operator in placement of data probes to measure response. Programs include software development processes (editing, data entry verification, learn-mode operations and update operations) and execution with routine library files.



The Analyzer/Fastprobe package will support the 8080, 8085, Z-80, 6800, 6802 microprocessors and the 8048 family (including 8021, 8035, 8039, 8041A, 8049, and 8748). The complete Fastprobe package starts at \$5,000 (Delivery, 60 days ARO). MicroSystem Analyzer costs from \$4,600 to \$5,400. Millennium Systems Inc., 19020 Pruneridge Ave., Cupertino, CA 95014. Phone (408) 996-9109.

LOW COST SPEECH RECOGNITION UNIT is being introduced by Heuristics, Inc. Model 7000 will interface with all RS-232-C terminals to provide handsoff operation. Key to the unit is a spectrum analyzer using state-of-the-art digital filtering and pattern matching techniques to analyze audio input. Output is automatically transferred to

the computer in standard ASCII format. Unit can be trained to recognize up to 64 words or phrases, each up to three seconds in length, and is compatible with all common programming



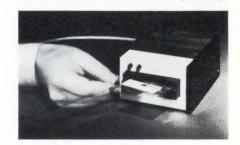
languages, such as FORTRAN, COBOL, PASCAL, and BASIC. It enables computer to take either keyboard or voice input, or both simultaneously. Model 7000, \$3000. Heuristics, Inc., 1285 Hammerwood Ave., Sunnyvale, CA 94086. Phone (408) 734-8532.

Circle 169

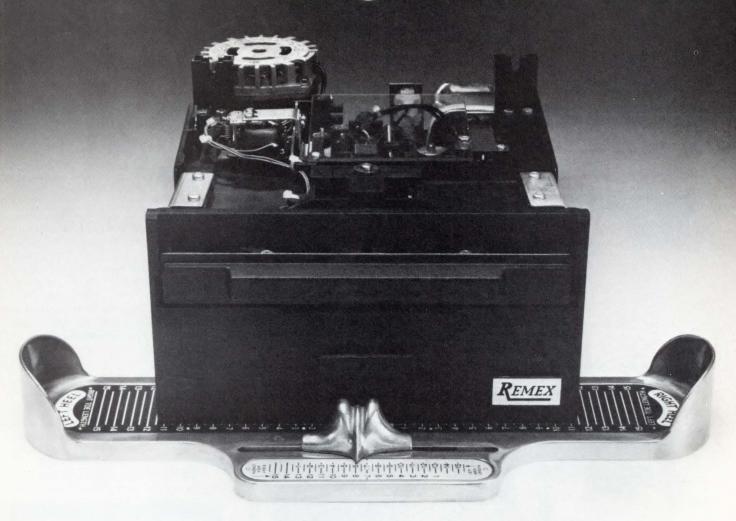
Circle 127

APPLICATIONS CONTROLLER in a 6800 single board computer requires only a power supply and a terminal to operate. The ACS-12 provides two programmable 16-bit timers, software controlled ACIS/MODEM interface on an RS232 serial port, two 8-bit parallel ports with handshake control (or one 16-bit parallel port with handshake control), 4 KB of static RAM and 6 KB of PROM. With 4 KB of static RAM, DOPS-12 and manual, the ACS-12 lists at \$495 in quantity. Datricon Corporation, P.O. Box 19021 Portland, OR 97219. (503) 245-1897.

MASS STORAGE ON A MICRO WAFER. This mass storage device "sops up" programs and data from any computer system that has an RS-232 port. Intended for both endusers and OEMs, the small "box" sells single-piece for \$349.50 to under \$200 in OEM quantities. Called the MICRO-Sponge, the new unit is jumper selectable for 300, 1200, 9600 and 76.8k baud and stores a maximum of 80KB on a 75 Exatron Stringy Floppy wafer. An ESF wafer is a thin, business-cardsized, continuous-loop, digital tape cartridge. Tape lengths from 5' to 75'. Each 5' length stores 5.3KB of RS-232 formatted data. Exatron, 181 Commercial St., Sunnyvale, CA 94086. Circle 150



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Ex-Cell-O Corporation

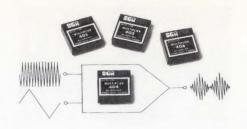
REMEX DIVISION

DATA WAREHOUSE

New Products

MICROHYBRID

MULTIPLIERS interface with μP-based systems. Although small, (0.5 in.³), they include a transconductance multiplying element, a stable reference and an output amplifier with specified accuracy internally trimmed for feed-through output zero and gain trim. Models 403 through 406 multiply in four quadrants with a transfer function of XY/10; multiplying errors (at 25°C) range from 1 to 0.1%. Accuracy

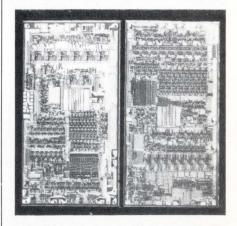


spec (as low as 0.1%) includes the effects of offset voltage, feedthrough, scale factors and nonlinearity. Other features include 0 to 70° C operation, $\pm 10V/5$ mA output, 1-MHz small signal bandwidth, 750-kHz fullpower band-

width and slew rate of $45V/\mu sec.$ Inputs are protected against overvoltage transients, and outputs are fully protected against short circuits to ground or either supply voltage. Price range, \$55 to \$150 (1-9). Deliveries from stock to 30 days. Quantity discounts available. SGR Corporation, Neponset Valley Industrial Park, P.O. Box 391, Canton, MA 02021. Phone (617) 828-7773.

DECWRITER II GRAPHICS TER-MINAL Make any DECwriter II into a full graphics terminal? Use Graphics II. Its single PCB provides: plug compatibility, graphics, improved speed, 1K buffer, programmability, numerous std. DEC options. It gives DECwriter II the versatility of 1,045,440 addressable points to provide for full graphics capability. Specs are: 100 dots/in (hor), 72 dots/inch (ver), 1,320 dots/ line, 792 lines/pg. Graphic data can be fed into the printer from a computer. An operator can create his own graphics by using the printer keyboard and ASCII characters to select and point coordinates. Selanar Corp., 3054 Lawrence Expwy., Santa Clara, CA 95051. Circle 252

TWO-CHIP CODEC WITH FILTERS SET. The S3501 Encoder with Filters and the S3502 Decoder with Filters form a CMOS companding set. It can implement a per channel voice frequency coding conversion for PCM channel banks and PABX systems requiring a μ -255 law transfer character-



istic. The chip set meets or exceeds the AT&T D3 and CCITT G.711 and G.733 specifications. The S3501 and S3502 chips each contain a band-limiting filter and an A/D or D/A converter that conforms to the μ -255 law transfer characteristic. Transmission and reception rates of 8-bit data words containing analog information can be increased to 3.2 million bps with analog sampling at a nominal 8KHz rate. Pricing per set for quantities of 100 is \$37.50. American Microsystems, Inc., 3800 Homestead Rd., Santa Clara, CA 95051.



A unique Rianda MAXI for your Data General MINI: the 6250 Tape System.

For the scientific laboratory, the oil industry, or wherever it's important to have maximum storage in minimal space or 6250 GCR tape media interchange, here's one more Data General subsystem you won't find anyplace else: the Rianda 6250-bits-per-inch tape drive and controller.

ANSII/IBM media compatible, it's also compatible with Ampex, Keronix, Lear Siegler, and SCI computers, and it works flawlessly with your current Data General operating system without software modification.

Rianda 6250 formatter and Tape Drive subsystems are also available interface compatible with *your* CPU adaptor designed for Datum, Pertec, or Wangco NRZI or PE formatters for *other* computers!

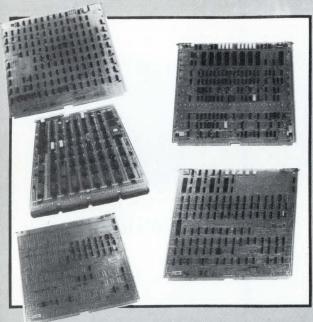
6250 Tape Drive subsystems, configured to your specifications, can

be delivered in 30-60 days from:



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- Disk controllers (10-300 mb) NOVA Compatible
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- Line printer controllers for DEC, NOVA, IBM Series I

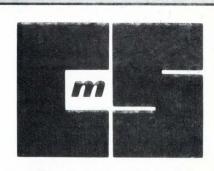
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Representative

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SINGLE OUTPUT IC REGULATED OEM SERIES EAPS U

MEETS UL AND CS A REQUIREMENTS

Not available through distributors contact the engineering sales office near you. Minimum sales order 50 units.

FEATURES

- 3 way barrier block output terminals screw, solder connection or fast on tabs
- Higher efficiency cooler operation 45% efficiency at 5VDC, 60% at 15VDC
- Better noise immunity dual input electrostatically shielded transformer
- High reliability over 100,000 hr MTBF (5V 6A per MIL-HDBK-217B at 40°C ambient, full load, nominal line)
- Metal Cased Hermetically Sealed Pass Transistors used on all units over 25 watts
- 85°C 10 yr life computer Grade capacitors
- · Meets UL and CSA requirements
- Full 5 yr warranty
- Metal Cased Hermetically Sealed IC regulator
- Fully enclosed, dustproof, insulated Potentiometers
- Wider input line voltage range 103-130V/206-260V 47-63Hz
- · Thinner profile 3 plane mounting

\$ 22.25



10-15 Watts

HB Case Series Meets U.L. and C.S.A. Requirements 5 Vdc @ 1.2 Amps to 24 Vdc @ 0.6 Amps Optional OVP available for 5V to 24V units

MODEL	RA	TING	REGUI	ATION	RIPPLE
NUMBER Vdc Amps		Line	Load	(Pk/Pk)	
EAPS 5-12U	5	1.2	±0.05%	±0 10%	3mV
EAPS 12-05U	12	0.5	±0.05%	±0 10%	3mV
EAPS 15-05U	15	0.5	±0.05%	±0.10%	3mV
EAPS 24 0 6U	24	0.6	±0.05%	±0.10%	5mV

\$ 23.25



15-24 Watts

HB Case Series
Meets UL and CSA Requirements
5VDC @ 3 Amps to 24VDC @ 1.0 Amps
Optional OVP available for 5V to 24V
units.

MODEL	RA	TING	REGUI	RIPPLE	
MODEL NUMBER			Line	Load	(Pk/Pk)
EAPS 5-30U	5	3.0	±0.05%	±0.10%	5mV
EAPS 12-1 6U	12	1.6	±0.05%	+0 10%	5mV
EAPS 15-15U	15	1.5	±0.05%	±0.10%	5mV
EAPS 24-1 0U	24	1.0	±0.05%	±0.10%	5mV

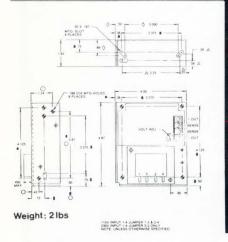
\$44.95

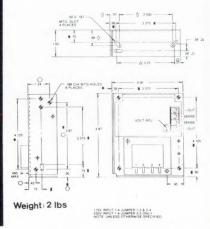


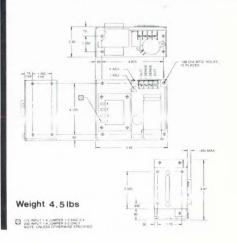
30-50 Watts

HC Case Series Meets UL and CSA requirements 5VDC @ 6 Amps to 24VDC @2.4 Amps Optional OVP Available for 5V to 24V units

MODEL	RA	TING	REGUI	RIPPLE	
NUMBER	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-60U	5	6.0	±0.05%	±010%	5mV
EAPS 12-34U	12	3.4	±0.05%	±0 10%	5mV
EAPS 15-3 0U	15	30	±0.05%	±0 10%	5mV
EAPS 24-2 4U	24	24	±0.05%	±010%	5mV







NOW! Call Toll Free (800) 854-8288)

See Page 67 for List of Local ADTECH Field Offices...

Specifications:

AC Input: 103-130V/206-260V AC 47/63Hz

Derate 10% at 50Hz

DC Output: See tabulation of models

Line Regulation: ±0.05% for ±10% line change Load Regulation: ±0.1% for ±50% load change

Ripple: Less than 5Mv peak to peak

Transient Response: Less than 50 microseconds

Short Circuit and

Overload Protection: Automatic recovery foldback current

limiting

Reverse Polarity Protection: Standard

Remote Sensing: Standard with open sense lead protection

Output Adjustment: ±5% minimum

Operating Temperature Range: 0°C to +50°C at full power rating. Derate linearly to 40% at 70°C or -20°C

Storage Temperature: -30°C to +85°C

Stability: ±0.1% for 24 hours after warm up Temperature Coefficient: ±0.01% typical ±0.03% maximum

Vibration: Per MIL-STD-810B method 514, procedure 1. curve AB (to 50Hz)

Shock: Per MIL-STD-810B method 516 procedure

Overvoltage Protection: Optional

Efficiency: 5V units 45%; 12V units 55%; 15V units 60%;

24V units 62%

Line Noise Suppression: Electrostatically shielded

transformer

ALL MODELS WARRANTED FOR 5 YEARS

\$ 59.45



50-84 Watts

HN Case Series Meets UL and CSA Requirements 5 Vdc @ 9 Amps to 24 Vdc @ 3.6 Amps Optional OVP available for 5V to 24V units

MODEL -	RA	TING	REGUL	RIPPLE				
NUMBER	Vdc	Amps	Line	Load	(Pk/Pk)			
EAPS 5-9.0U	5	9.0	±0.05%	±0.10%	5mV			
EAPS 12-5.0U	12	5.0	±0.05%	±0.10%	5mV			
EAPS 15-4 5U	15	4.5	±0.05%	±0 10%	5mV			
EAPS 24-3.6U	24	36	±0.05%	±0.10%	5mV			

\$71.05

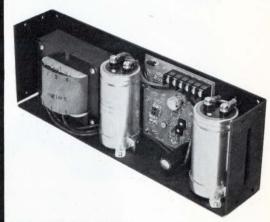


60-100 Watts

HD Case Series Meets UL and CSA Requirements 5 Vdc @ 12 Amps to 24 Vdc @ 4.5 Amps Optional OVP available for 5V to 24V units

MODEL	RA	TING	REGUI	ATION	RIPPLE
NUMBER			Line	Load	(Pk/Pk)
EAPS 5-120U	5	120	±0.05%	±0 10%	5mV
EAPS 12-6.8U	12	68	±0.05%	±0.10%	5mV
EAPS 15-6 0U	15	6.0	±0.05%	±0.10%	5mV
EAPS 24-4.5U	24	4.5	±0.05%	±0.10%	5mV

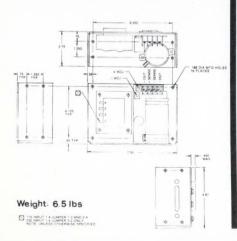
\$ 98.85

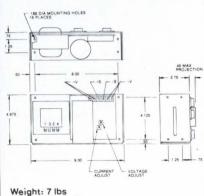


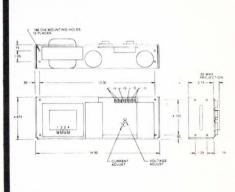
90-168 Watts

HE Case Series Meets UL and CSA Requirements 5 Vdc @ 18 Amps to 24 Vdc @ 7.0 Amps Optional OVP available for 5V to 24V units

MODEL	RA	TING	REGUL	ATION	RIPPLE
NUMBER	Vdc	Amps	Line	Load	(Pk/Pk)
EAPS 5-180U	5	180	±0.05%	±010%	5mV
EAPS 12-10.0U	12	100	±0.05%	±010%	5mV
EAPS 15- 90U	15	9.0	±0.05%	±010%	5mV
EAPS 24- 70U	24	7.0	±0.05%	±010%	5mV







Weight: 9.5 lbs 115 V INPUT 1-4 JUMPER 1-3 & 2-4 230 V INPUT 1-4 JUMPER 3-2 ONLY

ADTECH POWER SUPPL

115 V INPUT 1-4 JUMPER 1-3 & 2-4 230 V INPUT 1-4 JUMPER 3-2 ONLY



New Products

THERMAL PRINTER/PLOTTER. This 44-column fixed head thermal graphic unit will plot and print with μP based systems. Available in two models (desk top and panel mount), Microplot 44 incorporates a fixed head design using thick film linear dot array technology. Both models accept analytical and computational data.



The unit then plots data, prints grid and scale, annotates date with alphanumerics and prints alphanumeric text with both X and Y axis orientation. Features include: individual dot addressing; enhanced vector plotting; double density; 256 dot resolution; manual and programmable mode selection; standard interface; O.E.M. parallel and internal self test. Under \$1000. Gulton Industrial Park, E. Greenwich, RI 02818. (401) 884-6800. Circle 179

PLOTTER INTERFACING LITERA-TURE. Technical literature describes the use of the HI PLOT DMP-2 Digital Plotter with the Apple II, PET and TRS-80. Includes driver programs in BASIC (loaded into RAM via the keyboard) and complete instructions for interfacing each unit and running a series of programs. All three units utilize the same compatible cable, with the Apple II and TRS-80 using their own serial interface cards, while the PET requires a serial interface cable. Houston Instrument, One Houston Sq., Austin, TX 78753. (512) 837-2820. Circle 177

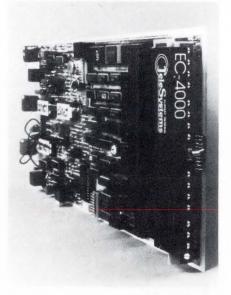
MAIL ORDER CATALOG. Billed by its publishers as "the most complete computer guide available anywhere," a fifth edition is now available. It covers electronics, computers, hardware, software and intelligent computer products and gadgets. This year's edition is 144 pp and costs \$2. Advanced Computer Products, Inc., 1310 E. Edinger, Santa Ana, CA 92705. (714) 558-8813.

Circle 182

stator core yoke offers linearity and min. spot growth for use with fiber optics faceplate line-scan CRTs. The accurate ferrite core design and a tooling breakthrough provide high resolution, fast settling and good L/R ratio. The C 11955 yoke is suited for high resolution applications employing fiber optic faceplate line scan CRTs. Syntronic Instruments, Inc., 100 Industrial Rd., Addison, IL 60101. (312) 543-6444. Circle 178

DEE RESEARCH REPORT. A 181 pp study analyzes and reviews the market for data entry equipment in the 80s. Report includes a lengthy discussion of the changes which are expected to take place in the data-entry market. Also discussed are assessments of the future of the data entry equipment market. Included in the study are Data Entry Trends, Computer Industry Trends, Strategic Analysis of Leading Data Entry Equipment Suppliers, Ten-Year Projections for Data Entry Equipment, Opportunities and Strategies for the 1980s. Report #153, \$985. International Resource Development, Inc., 30 High St., Norwalk, CT 06851. (203) 866-6914. Circle 181

removes echo from long distance satellite, undersea cable, or terrestrial circuits. Model EC-4000 is a special purpose digital processor that cancels echo on analog circuits by dynamically computing and storing an estimate of the upcoming echo and then subtracting



this estimate from the echo contaminated speech signal. May be equipped with an SF Transparency Option which assures that SF signalling tones will bypass the echo cancelling circuits. Unit measures $6.7'' \times 14'' \times 1.4''$ and weighs approximately 2.25 lbs. Convection cooled, it requires no fans. COMSAT General TeleSystems, Inc.,

2721 Prosperity Ave., Fairfax, VA 22031. (703) 698-4300. Circle 180

LSI FACILITIES GUIDELINES. This is a book for companies planning new integrated circuit wafer fabrication programs. "LSI Manufacturing Facilities Guidelines" covers site selection, building space and layout requirements, leasehold improvements, clean room considerations, and utility needs. Equipment selection lists for both laboratory and production modules are provided. Also covered are start-up programs, initial material require-



ments, recommended personnel orgaization, safety aspects to insure conformance with occupational health standards, and accommodation for all major bipolar and MOS processes. An appendix includes names of American architects with semiconductor manufacturing facility experience and a sample request for proposal for architectural engineering services. Price of the "LSI Manufacturing Facilities Guidelines" together with the companion Concepts Handbook (construction blueprints) is \$5,000. A copy of the Table of Contents and selected pages for examination are available to those requesting on company letterhead. Integrated Circuit Engineering Corp., 6710 E. Camelback Rd., Scottsdale, AZ 85251. Circle 153

UPGRADED SUBSYSTEM MOD-ULES. A series of ten new multifunction, modular, microcomputer subsystems is tailored for the harsh industrial environment. The 180 Line of modules provide maximum flexibility and minimum risk and complication for the customer configuring control or data acquisition systems. Among the items in the new 180 line are: an EPROM/RAM; a bankswitched RAM; a high level digital output module; a bidirectional TTL I/O Module; an Analog I/O Module; a Master-Slave Microcomputer which is a self contained microcomputer for high speed, multiprocessor applications. Initial delivery of the units was to begin June 30 with volume deliveries starting the third quarter. Xycom, Inc., 750 N. Maple Rd., Saline, MI 48176.

Circle 145

COMMUNICATIONS **PROTOCOL** CIRCUIT. This device provides both bit and byte oriented protocol capability, including complete Bisync protocol processing on the chip. Four 16-bit addressable registers can be programmed by users to specify the desired protocol as well as options within that protocol. The F6856 device then performs the bulk of the required processing and interfaces with most microprocessors, microcomputers and minicomputers with either 8 or 16-bit data buses. The device has a 1 megabit/s data rate and is fully compatible with TTL logic. Samples available now, with production quantities scheduled for the first quarter of 1980. Pricing in 100 to 999 quantities is \$24.50 for the 40-pin plastic CIP version, and \$29.90 for the ceramic side-brazed package. Fairchild Corp., 101 Bernal Rd., San Jose, CA 95119. Circle 135

ICE SUBSYSTEM. RTE8/8800 supports hardware and software development of the Am9080A/8080A, 8085, 8048 and Z80 when operated in conjunction with the AmSYS 8/8 Development System. It operates in single or multiple ICE (In Circuit Emulator) environment. Or, the emulator can be configured as a subsystem with the AmSYS29 Bit-Slice µP Development

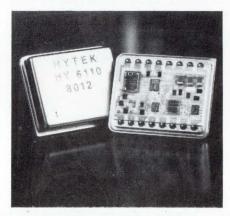


System. Basic hardware configuration includes control processor board, communications board, debug board and real-time trace module. The user tailors the system to a specific µP with a module.,, "personality Advanced Micro Computers, 3340 Scott Blvd., Santa Clara, CA 95051. Circle 131

EXTENDED PROCESSING POWER IMPROVES COMPUTER SPEED. The software development, ARTS (Advanced Real-Time System), is a compatible subset of Data General Corporation's Advanced Operating System (AOS), with emphasis on real-time processing. Designed for the Mil-Spec computer marketplace, this system

now runs faster and requires less memory than its commercial counterpart. It is configurable and modular, providing memory support from 64K to 2048K. It is a memory-only operation and includes high-order language support, memory-resident file structure, efficient interprocess communication, and a flexible process/task scheduler. WCS (Writable Control Store) hardware maximizes the computing power of the processor, while minimizing the critical path execution time for highspeed functions. In time-critical operations, specialized functions can be tailored to the application. ROLM Corp., 4900 Old Ironsides Dr., Santa Clara, CA 95050. Circle 146

PROGRAMMABLE GAIN INSTRU-MENTATION AMPLIFIER is a high speed device for: precision instrumentation; computer controlled data acqui-



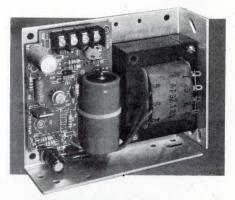
sition and transducer signal amplification. The HY-6110 offers digitally programmable gains of 1, 2, 4 or 8; slew rate $10V/\mu s$; settling time to .01% in 10 μs; gain accuracy .05% adjustable to .005%. Delivery is from stock to 6 weeks. 1,000 piece price, \$110 each. Hytek Microsystems, Inc., 16780 Lark Ave., Los Gatos, CA 95030.

Circle 128

NEW SUB-MODULAR DC POWER SUPPLIES. These new low cost units allow the engineer to custom design a power module to meet exact requirements by adding specialized transformer, heatsink, and other accessories. The 25 Series by Powertek provides output voltages of 5, 12, 15, and 24 VDC at output current ranges of: 2.5 to 6 amps for Model 25C; 5 to 12 amps for Model 25D; and 7.5 to 18 amps for Model 25E. Standard features include: voltage adjustment; current limiting; remote sense; output rectifying, filtering and regulation; output overcurrent and short circuit protections and AC-input fuse. Overvoltage protection is available as an option. Prices in quantities of 100 are 25C - \$31; 25D -\$45.50; and 25E - \$51.25. Powertec, Inc., 20550 Nordhoff St., Chatsworth, CA 91311. Circle 134

Adtech **EAPS"U" Series Power Supplies**

See Ad Pages . . . 64, 65



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Washington, D.C. Phone: (202) 363-9417

Washington, Seattle

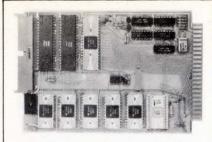
Phone: (206) 455-3460 Wisconsin, Milwaukee Phone: (414) 527-1500

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An Equal Opportunity Employer, Male/Female/Handicapped

Product Index

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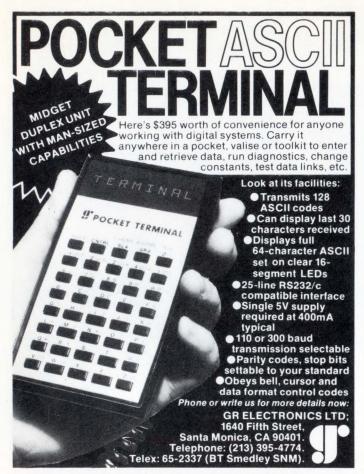
- solid state
- DC operation—12V dc inputs
- choice of signal inputs:
 TTL (standard)
 Composite video (plug-in module)
- standard 15,750 KHz horizontal scan frequency
- 650 lines resolution

Circle 46 on Reader Inquiry Card



AUDIOTRONICS
VIDEO DISPLAY DIVISION

530 FIFTH AVENUE N.W. NEW BRIGHTON, MN. 55112 · (612) 633-3131



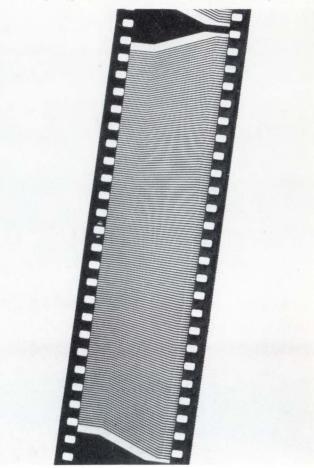
Circle 47 on Reader Inquiry Card



Circle 48 on Reader Inquiry Card

New Products

TRANSITION JUMPER CABLES for PC assembly interconnection are film-base copper conductors typically wave-soldered between adjacent PC boards in electronic assemblies. They're produced on 2- or 3-mil DuPont Kapton film



with 1-oz. ED copper conductors, typically 1.3-mils thick in any customer-designed configuration. Conductor lines may be as narrow as 3 mils on 6-mils centers. The distance to be "jumpered" may range from 11mm to several in. 3M, Box 33600, St. Paul, MN 55133.

UPGRADE PACKAGE FOR COSMAC SYSTEM. This CDP18S837 Package contains the hardware, firmware, and software needed to upgrade a COSMAC Development System, CDP18S005, equipped with a floppy disk system and a minimum of 12 K of RAM to a fuctional level equivalent to the new COSMAC DOS Development System, CDP18S007. The package includes 16K of static CMOS RAM, a UART terminal interface module, a replacement PROM for the utility program, a CDOS system diskette, and appropriate instruction manuals. Program development is enhanced by the CDOS disk file-management and operating system. The modifications required to incorporate the CDOS Disk Operating System software with the CDP18S005 include the installation of memory modules, the extraction of the terminal interface module, the insertion of the UART module, and the addition of the PROM containing utility program UT21. The standard cables supplied with the CDS and the floppy disk system are sufficient for the interconnections between the system components. In single quantities the RCA COSMAC Disk Operating System Upgrade Package, DCP18S837, is priced at \$1600. RCA, Solid State Division, Box 3200, Somerville,

NEW VOICE SYNTHESIZER. This low-cost single circuit board is capable of generating an unlimited vocabulary in 7 different languages and it interfaces with a variety of terminals. Words on this Model VSB are generated by a series of electronic commands that produce the various phonemes which comprise human speech. A built-in clock output allows for natural conversational flow. Along with the manual controls for rate, volume and pitch, a tone control allows the user to adjust the vocal output for esthetic or ambient noise considerations. \$280. Votrax, 500 Stephenson Hwy, Troy, MI 48084. Circle 147

ATTACHED PROCESSOR combines with host computer to provide lowcost, extended-precision, large-memory array processor system with floatingpoint computational performance. Provides up to 12-million floating-point operations per second, plus a concurrent maximum of 6-million integer/ address operations per second. Precision exceeds 15 decimal digits through 64-bit floating-point arithmetic. Based on 16K memory chips, main memory is presently expandable to 1.5-million 64-bit words (12-MB). Large programs and associated data sets may reside in main memory for fast access and high throughput. As 64K chips become available, the memory can be expanded to a maximum of 6-million 64-bit words (48 MB). An address of 24 bits provides for the direct addressing of 16-million words (128 MB). An 8-bit error correcting code provides for single error correction and double error detection (SECDED) on all memory references. FPS-164 with 64K word memory, \$155K; one Mword model, \$428.5K. Floating Point Systems, Inc, 3601 S.W. Murray Blvd., Beaverton, OR. Phone (503) 641-3151.

UPGRADING THE 2200. Two additions have been made to Wang's 2200 small business computer series, (the 2200 SVP and 2200 LVP.) Also announced is the first-time-user PCS-III, a newly designed 2280 Disk Multiplexor and the introduction of a business-application software package, IDEAS. The 2200 SVP is offered with a 32KB processor, a Wang 2236 terminal and a newly designed single-sided, double-density diskette, which increases storage capacity. A single-user system, the 2200 SVP's memory is expandable to 64KB. Complete systems cost \$12,000 to \$20,000. The 2200 LVP small business system is a high performance computer which can support up to four users concurrently. The system, claimed to be similar in architecture to the company's 2200 MVP, offers: disk storage capacity, telecommunications capabilities and an operating system with low overhead. These systems will range in price from about \$15,000 to approximately \$35,000. Wang Labs., Inc., One Industrial Ave., Lowell, MA 01851.

Circle 138

SHORT CUTS IN PROGRAM WRIT-ING. A new software package facilitates the writing of a microcomputer program in a quarter to half the time required under conventional methods. ASPTM, the new package, contains significant extensions to the Pascal programming language standard, including business arithmetic, character string

manipulation, disk random access, and an optional ISAM (Indexed Sequential Access Method). Business support packages, such as a screen data entry module and data base query processor, are available. Included are a system library and full-linkage editor subsystem. A program under development can be broken into separate modules so that each can be worked on individually. The company says this results in a program that's more reliable and easy to understand. \$250 through dealers. InfoSoft Systems, 25 Sylvan Rd. South, Westport, CT 06880.

Circle 144



Want more zest in your PDP-11?

Plug a UMC into your PDP-11 and get a microprocessor system on your UNIBUS.

The UMC is a modular system of boards and support software. It plugs into your UNIBUS, shares work with your PDP-11 and gives you powerful independent processing.

Use the UMC system for terminal control or network attachment. Have it serve as an intelligent controller. Or use it for data acquisition, pre-processing or post-processing.

Since the UMC system is modular, it's flexible. It conforms and grows to meet your demands. Select only the UMC components that serve your specific needs:

UMC Processor Board. With Z80 microprocessor, 4K bytes static RAM, room for 16K bytes user PROM, 2 serial I/O lines and up to 3 DMA channels. UMC Memory Board. Has up to 64K bytes RAM and space for 32K bytes PROM. Use multiple boards for extra memory.

UMC Serial I/O Board. Up to 16 full-duplex channels with independent microprocessors and programmable baud rates. Extra boards serve extra lines.

UMC Terminal I/O Board. Has 8 full-duplex RS-232C channels, a Z80 microprocessor, 32K bytes RAM and space for 16K bytes PROM.

UMC ProtoHex Board. For custom wirewrap work.

UMC Software Development System. Run it in your PDP-11 to support writing UMC programs.

UMC Software Application Packages. For various protocols 2770, 2780, X.25, HASP, 3270, ADCCP and others.

Now then, want to hear more about adding zest to the old PDP-11? Contact ACC right now.

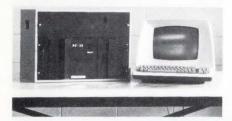
ASSOCIATED COMPUTER CONSULTANTS

228 EAST COTA STREET, DEPT. N, SANTA BARBARA, CA 93101. (805) 963-8801. TWX 910 334-4907.

Wire-Wrap is a registered trademark of Gardner-Denver Co. PDP and UNIBUS are registered trademarks of Digital Equipment Corp. Z80 is a registered trademark of Zilog, Inc.

New Products

MODULAR MICROCOMPUTER. System combines modular Multibus-based hardware with the CP/M2.0 disk operating system software. System is configured around the Z-80A (4MHz)



CPU and includes 48KB of RAM and sockets for 8KB of ROM/PROM. A 2K monitor, dual 8" double density floppy disk drive and disk controller and interfaces for a video terminal and line printer are also included. Hardware is modular; the ZBC 80 single board computer, FFD-1 floppy disk controller/RAM card, CCB-7 seven slot cardcage/backplane with power supply and fan and the DF-28 dual floppy disk drive are all available separately. MAC-10 system, \$5990. Delivery 30-45 days, ARO. Matrox, 5800 Andover Ave., T.M.R. Quebec, H4T 1H4, Canada. (514) 735-1182. Circle 184

NEW BROCHURE ON BENEFITS OF 1/2" STREAMING TAPE. The advantages of half-inch streaming tape as a data storage medium for mini-computer users is explained in "1/2-Inch Streaming Tape, What's It All About." The report compares leading memory technologies such as dynamic NMOS RAM, bipolar RAM, bubble and CCD memories, fixed and flexible magnetic disks and magnetic tape with regard to a number of criteria. It also discusses cost per bit, reliability, cost of hardware, and data access time. The free brochure reviews 1/2" streaming tape as backup for Winchester disks, as an archival storage medium, as a file organization device and as an I/O device. The new literature, "1/2-Inch Streaming Tape, What's It All About," is available free of charge by writing to Cipher Data Products, Marketing Dept., 10225 Willow Creek Rd., San Diego, CA 92131. Circle 185

A NEW BOOK REVIEW. "COM-PUTER DICTIONARY AND HAND-BOOK." Charles J. Sippi and his son Roger have compiled the third edition of this dictionary. The first edition was published in 1966, the second in 1972. Alongside Webster and Roget, Sippi's dictionary belongs on the desk of anyone interested in computers. Charles is author of the article on computers in the Encyclopaedia Britannica.

The excellence of that piece is continued in this 2-1/2 pound, 928-page hardback. If Pulitzer Prizes were to be awarded in lexicography, the Sippis would surely be nominated for one. This excellent book is more than a collection of computer words and phrases. It is a remarkable, readable and excellent treatise (the handbook section) on the whole field of computers. The section on acronyms and abbreviations alone is worth the price of the book. Where else can you quickly find definitions of such little-used acronyms as QDC, PTE, ZFB, ZIC or FXBIN? Where else can you read such stimulating ideas as these closing remarks in the book: "Some of the creative activities by computers which had been described in many experiments are now considered unexplainable by humans. Is this the totally new dimension? A completely new superscience?" If you want to curl up with a nice book some night, try this dictionary. - (Reviewed by H.S.) \$25.95 hardback, \$11.95 papaerback. Published by Howard W. Sams & Co., Inc., 4300 West 62nd St., Indianapolis, IN 46268. Circle 175

QUIET IMPACT PRINTER. Claimed to be the quietest impact printer on the market, the T1705 prints at 160 characters per second using a bidirectional print head. Achieves throughput speeds of up to 200 lines per minute. Unit features dual tractor paper handling, 6 or 8 lines per inch spacing, self test and snap-in ribbon cartridge. Interface has 665 byte buffer; parallel interface unit is also available. Model T1705, \$1895. Delivery 30 days ARO. Tally Corp., 8301 S. 180th, Kent, WA 98031. (206) 251-5524. Circle 189

MODAL ANALYSIS MOVIE. A professionally produced 10-minute 16mm color-sound movie called "Good Vibes" shows what modal analysis can do in solving large vibration problems. It demonstrates a step-by-step real modal test on an automobile and presents the animated mode shapes from the CRT terminal (including a complex



mode). It illustrates simplified data entry, formatting and results. Movie is available for seminars and as a training or teaching aid. Nicolet Scientific Corp., 245 Livingston St, Northvale, NJ 07647. (201) 767-7100. Circle 190

for microprocessor-based data-communications applications — such as modems and multiplexers — have been announced by Ault Inc. Two models are

nounced by Ault, Inc. Two models are available: one supplies +5 VDC at 0.30A, and ±12 VDC at 0.13A; the other furnishes +5 VDC at 0.60A, ±12 VDC at 0.20A. Besides modems, these power supplies are designed to work



with small computer systems, data-communications terminals, medical instrumentation, or wherever a powerful, compact external power supply is required. They plug into any 117V AC outlet, or are available with line cords (models also available for 220V or 50-cycle applications). Line/load regulations is ±5 percent, with less than 10 mv RMS ripple. Ault, Inc., 1600 H Freeway Blvd., Minneapolis, MN 55430.

FREE BROCHURE ON TDC 2000. Honeywell is offering a free new 24-page color brochure on its TDC 2000 Basic system. The brochure details areas such as field instrumentation; process connected systems; process interface units; communications; central operating centers, and computer-assisted process management. Honeywell Process Management Systems Div., P.O. Box 437, 10 Pelham Pkwy., Pelham Manor, NY 10803. Circle 129

WHIZZARD DYNAMICS IN 3D An optional 3D transformation module for WHIZZARD's 7000 vector refresh graphics series permits pictures to be scaled, rotated, or translated in 3 dimensions. Maximum vector utilization and throughput can display both 2D and 3D pictures at the same time! A special set of calls by Megatek Graphics' Software places three dimensional vector information in the WHIZZARD's display list. Addition of

these calls allows vectors to be specified with twelve-bit resolution in all three dimensions. Once the display list for a picture contains three-dimensional vector information, the resultant display can be scaled, rotated, translated and clipped. The new hardware module joins a series of optional addons Megatek offers in support of its WHIZZARD terminals and systems. Modular approach to the equipment design allows end users and OEMers to choose particular needs for specific application. Megatek Corp., 3931 Sorrento Valley Blvd., San Diego, CA Circle 126 92121.

NEW FLEXIBLE DISKS A new 8" flexible disk is capable of sustaining operating and storage temperatures up to 160° F. Problems of disk warp caused by storing disks in automobiles or exposing them to direct sunlight or high temperature environments are all eliminated. An improved personal computer minidisk was also unveiled at the NCC. This minidisk features a newly designed jacket which provides longer life and superior reliability. Comes in several configurations, from single- to double-sided and 35 to 77 tps. The third new product is the 577 Super Minidisk, designed specifically for use with a Micropolis drive but compatible with any drive currently produced. Disk is 100% certified at track densities of 48, 96 and 100 tpi. Verbatim, 323 Soquel Way, Sunnyvale, CA 94087.

NEW PRINTERS AND LCD LINE. At the NCC, Epson America, showed its new 80-column, condensed 132-column Dot Matrix Printers compatible with the full range of small-business /personal computer systems. The company also will show its TX-80 Dot Matrix Printer. A new line of Alphanumeric LCD Modules will be shown as well. Complete with integral CMOS LSI driver, these LCD modules range from 16 characters to 160 characters in display capacity. Epson America, Inc., 23844 Hawthorne Blvd., Torrance, CA.

ENCRYPTION/DECRYPTION HARD-WARE OPTION for the ACI-90 Pascal Computer System (Microenginetm Equipped.) Incorporating Western Digital's WD2001 Data Encryption Device, the hardware enhancement encrypts/decrypts data at a transfer rate of 163KB/s using the algorithm specified in the Federal Information Data Encryption Standard (National Bureau of Standards #46). The user defined password is a 16 hex word. The security hardware option is a factory installed option. Associated Computer Industries, 17751H Sky Park East, Irvine, CA 92714. Circle 151

State-of-the-Art Microprocessor Keyboards

AMKEY's new MPNK-100 Prom Programmable Microprocessor Capacitance Keyboard features two 512 x 4 Proms for encoding. The MPNK-100 is reliable. It has a lower chip count, the silent "no switch" switch, single +5 VDC supply, and the N-Key rollover which eliminates the possibility of missing a character during high speed typing. The MPNK-100 is versatile. It will do word processing, data entry, prototyping, and the same printed circuit board will accommodate both the PROM and masked ROM versions. The MPNK-100 is cost efficient. It has custom designability, lower power requirements, and all components are off the shelf.

AMKEY, The Innovative Leader in Keyboards



Circle 52 on Reader Inquiry Card



Imagine you could design a microprocessor system that would operate almost anywhere in the world with a single switching power supply. Well, you can with Converter Concepts' low-power switchers!

WIDE INPUT VOLTAGES Only Converter Concepts produces 15 to 100 watt switchers that operate on any voltage from 90 to 250VAC or 10 to 40VDC — without switches, jumpers, taps or other modification.

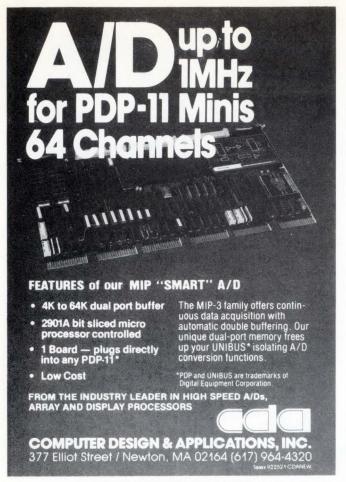
BROWNOUT PROTECTION You get reliable operation during power failure, too, on power as low as 50VAC, with minimum degradation of output voltage.

LATEST SWITCHER CONCEPTS Our advanced switchers use a single transistor, single transformer flyback design with soft turn-on characteristics and short circuit protection. You get less complexity, higher reliability and efficiency, and a cost that's competitive with linears.

Four input power ranges and single, dual or triple output options are available in low-cost printed circuit board, open frame or RFI-resistant enclosed packages.

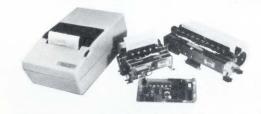
RIGOROUS QUALITY CONTROL We're building a reputation for tough QC, so you're buying confidence with every Converter Concepts' switcher. Call us today for engineering assistance, our latest engineering catalog, prices and your nearest CCI representative.





Circle 54 on Reader Inquiry Card

12 v. DC PRINTERS Impact - Line - Dot Matrix



This family of RUGGED, LOW COST printers is ideal for use in portable, mobile and severe industrial applications. (200,000 char from a 5 amp/hr batt). Three copy. Controller board accepts ASCII parallel or RS-232 inputs. Prints alpha-numerics and limited graphics. Solenoids have Patent Pending.

MODEL	DESCRIPTION	OEM PRICE
DMI-40	40 col Mechanism	\$166.00 EA.
DMI-40E	40 col Controller	150.00
DMI-40T	40 col R.O. Printer	445.00
	(with 115 v input)	
DMI-80	80 col Mechanism	216.00

Made in U.S.A. Order from manufacturer:

DATA MACHINES INTERNATIONAL, INC. Terrace Hill, Ithaca, NY 14850 607-273-1515

New Products

TRIPLE MODEM FOR REMOTE TERMINALS combines a Bell type 212A, a Bell type 103, and a Vadic VA3400 in a compact stand-alone package. The VA3450 series includes six switched network originate/answer models, all of which have been registered for direct connect under Part 68 of the FCC Rules. In addition, there is an originate or answer version for leased line applications. "The VA3450 series represents a major technical breakthrough," says Racal-Vadic "because now a single modem at the remote terminal satisfies every conventional originate/answer application for switched network full duplex data transmission from zero to 1200 bits per second." The VA3450 series incorporates Racal-Vadic's Idle Test, Analog Loopback & Busy Out, Digital Loopback, and Self-Test. In addition, the modems have a unique switch controlled "Standard Option" mode which forces the unit into a standard configuration to simplify and speed up diagnostic testing. Prices for the modem start at \$825. Delivery is 60 days, ARO. Racal-Vadic 222 Caspian Drive, Sunnyvale, CA 94086.

NEW BOOKS. These two new publications chronicle the epochal history of computer development in the U.S. "Project Whirlwind; The History of a Pioneer Computer" describes, in 3rd-person detail, the planning and construction of MIT's Whirlwind. Whirlwind introduced synchronous parallel logic and was the first computer to use random-access magnetic-core memory. Much of today's computer architecture are direct descendants from the Whirlwind. Authors Kent C. Redmond and Thomas M. Smith both have backgrounds as professors of the history of science. 300 pp. \$18. Published by Digital Press, Digital Equipment Corporation, 12-A Esquire Rd., Billerica, MA 10862.

Circle 155

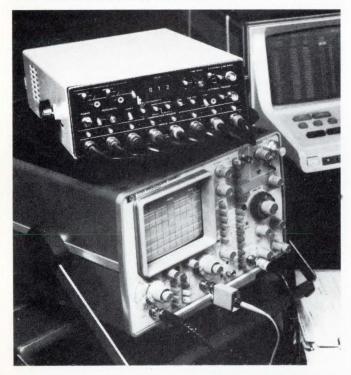
The Whirlwind book belongs on the shelf of anyone with an interest in computer development. On the same shelf, and right beside it, belongs another recent book, "From Dits to Bits." This is a 1st person account of Herman Lukoff's contributions to the ENIAC at University of Pennsylvania. Where "Whirlwind" is a text-book discussion of the high-level problems and decisions of original computer design, "Dits and Bits" is an inside-the-family view. Full of anecdotes and the personal tragedies and triumphs that took place during Eniac's painful birth, the book gives an insight into some of the momentous events marking the beginning of the computer age. (Author Herman Lukoff died in Sept. 1979, four months before this book was printed. Dr. John Mauchly, central figure of the book and co-inventor of the ENIAC, died early this year, one month after the book printing.) 210 pp. \$12.95 Pub. by Robotics Press/ISBS Inc., PO Box 555, Forest Grove, OR 97116. Circle 156

IMPROVED SOFTWARE EXPANDS UTILITY FUNC-TIONS. Designed for shops that use the IBM Time Sharing Option, TSO/Superset-Utilities enhances the performance characteristics of all standard utilities. It also expands functions for the benefit of the TSO user. The LISTJES command allows TSO users to preview SYSOUT data sets prior to printing. By selectively printing only items currently needed TSO/SUPERSET - UTILITIES users are said to realize savings in both critical turn-around time and large volumes of un-needed computer printout. Additional enhancements to both COPY and MERGE Commands make them utilities to be used rather than avoided. The creation of programs, JCL and data files from previously developed and tested elements is claimed to be a time and resource saver. A detailed brochure describing the product is available. Applied Software, Inc., 4440 PGA Blvd., Suite 204, Palm Beach Gardens, FL 33410. Circle 152

HIGH-RESOLUTION TIMING DIAGRAM The troubleshooting capability of most logic state analyzers can be greatly expanded with the addition of Models 20D and 50D Logic Timing Analyzers. Logic State Analyzers, very powerful in tracking down and troubleshooting software problems, are severely limited in capturing the timing and glitch abnormalities found in hardware and bus operations.

In addition, there are many situations in which state and timing problems are interrelated and the ability to trigger on and capture both types of information would be very helpful.

Models 20D and 50D are high-speed timing Logic Analyzers which capture data at 20 MHz and 50 MHz, respectively. With a simple BNC to BNC connection these instruments can be interconnected to most state analyzers. The timing and state analyzers can then work together in a variety of modes which offer wide flexibility and capability in software and hardware troubleshooting.



In a typical application at Tesdata Corp. in Sunnyvale, CA, a Model 20D Timing Analyzer is triggered by an H-P Model 1610A State Analyzer. In this application the diagnostic routine of the Tesdata MS108 System was not responding properly on the 257th occurrence of an illegal OP code. The Model 20D was connected to the expected source of trouble and set to record data at a 20 MHz rate (50 nsec sampling). The H-P 1610A was set to trigger the 20D upon the 257th occurrence of the illegal OP code and to capture state data before and after the trigger event.

After triggering, the Model 20D provided an eight-channel timing diagram which allowed Rick Hobbs of Tesdata to check for glitches and timing errors. Using the 1610A State Analyzer, the program flow around the trigger point was checked for possible software errors.

The addition of timing to a state analyzer is very cost effective when compared to purchasing a new timing/state instrument. A new timing/state analyzer will cost from \$6000 to \$14,000, while the Models 20D and 50D timing analyzers range from \$1,750 to \$4,400. With the Model 20D, 8-timing channels each and 256-deep are added to the state analyzer. The 20D samples at a max. clock rate of 20 MHz (50 nsec) and includes a 10 nsec glitch catcher on all channels. The Model 50D adds from 8 to 16 timing channels, each 510 deep, with a max. sampling rate of 50 MHz (20 nsec) and has a 5 nsec glitch catcher on all channels. Intech, B P Instruments Div., 282 Brokaw Rd., Santa Clara, CA 95050. (408) 727-0500. Circle 171



Circle 56 on Reader Inquiry Card

Another Knock-Out from International Microsystems



IM1010 Universal PROM Programmer

- Programs BIPOLAR PROMs, EP- . 4Kx8 RAM standard ROMs, Single Chip Microcom-
- Full editing capability.
- terminals, development systems and timeshare computers.
- PROM Emulation capability to test and edit programs before committing them to PROM's.
- · Multi-PROM Programs may be loaded into RAM and entire PROM sets programmed
- 16Kx8
- RAM or 32Kx8 RAM optional. puters, FPLA's, PGA's, PMUX's etc. Personality Module to assure fu-
- ture device capability. · Two serial interfaces standard for · Personality Modules may be changed without affecting RAM
 - data Mainframe \$2,095.00 Modules \$375-550.00. CALL US TODAY

IMI 1154 C Avenue Auburn, CA 95603 916 885-7262

Designers' Notebook

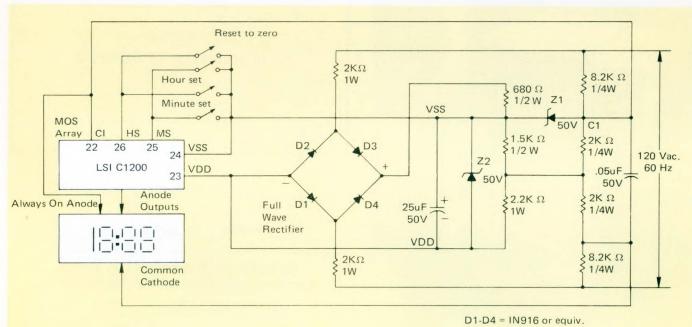
MOS Clock Handles Large LCD Displays

This clock uses a C1200 monolithic MOS/LSI 28-pin IC 40V ac outputs (80V p-p with respect to LCD), offers direct interface to large LCDs, accepts 60 Hz ac input, has a 12-hr. clock format and 3.5-digit hrs. and minutes display. The 1200 offers independent

designate hours. C1 (pin 22) is the 60 Hz count input. Pin 27 (not shown) is the one-second flash output. By additional circuitry (not shown), this output could be used to control other LCD segments or provide pulses for industrial control purposes.

Robert J. Boyle, Boyle Associates, Inc., Dallas, TX.

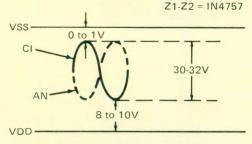
Rate this design: circle 11L, 11M or 11H on Reader Inquiry Card



minute set and hour set at 2-Hz rate with carry inhibit. The LSI Computer Systems IC clock was selected as it met these requirements.

The single supply $(V_{DD} = -25V \text{ to} -50V \text{ at 2 mA, typ.})$ necessitated the full-wave rectification of the 120V ac line, current-limiting via series resistors and then voltage regulation by Z2 to 50V to the supply inputs (V_{DD}) and V_{SS} .

Real timekeeping is not distributed during reset and time-set inputs are protected from contact closure bounce. As for the segment outputs to the LCD segments (anodes), these are designated by a single line, but are as follows. pin 1, LCD segment C4; 2, F3; 3, G3; 4, E3; 5, D3; 6, C3, 7, B3; 8, A3; 9, F2; 10, G2; 11, E2; 12, D2 and A2; 13, C2; 14, B2; 15, F1; 16, G1; 17, E1; 18, D1; 19, C1; 20, B1; and 21, A1. Segments are associated with one of four characters (4, 3, 2, 1), where 2, 1 designate minutes; and 4, 3



8048 Conversion Routine

This compact 16-bit binary to packed BCD conversion routine demonstrates the powerful decimal arithmetic capabilities of the 8048. This routine requires only 30 bytes of ROM storage, and it converts 16-bit binary values (from 0 to 65535) to a packed binary coded decimal (BCD) with two digits per byte. The routine will also convert values of less precision. To use the routine for less precision, modify the following line:

PREC EQU XX ;Precision of Binary where XX equals the number of binary bits to convert

For example, if only 8-bits need be converted, XX = 08.

Mark Perry, Intel Corp., Santa Clara, CA.

Rate this design: circle 12L, 12M or 12H on Reader Inquiry Card

:F1:ASM48 B2D.SRC	LOC OBJ SEQ SOURCE STATEMENT
ISIS-II MCS-48/UPI-41 MACRO ASSEMBLER, X107 BINARY TO BCD CONVERSION ROUTINE	53 54
LOC OBJ SEQ SOURCE STATEMENT	55; BINARY VALUE = BINARY VALUE # 2 56
1 \$ XREF DEBUG 2 \$ TITLE ('BINARY TO BCD CONVERSION ROUTINE 3/29/	0012 97 57 CLR C 0013 F9 58 MOV A,R1 ;LSB BINARY 0014 F7 59 RLC A 0015 A9 60 MOV R1,A ;SAVE RESULT
16 BIT BINARY TO BCD CONVERSION ROUTINE	0016 F8 62 MOV A,RO ;MSB BINARY 0017 F7 63 RLC A
ENT: BINARY VALUE IN RO,R1 R1 HOLDS LSB EXT: BCD VALUE STORED IN R2,3,4 R2 HAS MSD'S	0018 AB 64 MOV RO,A ;SAVE RESULT 65 66
10 11 12 USES: R0-R5 13 14 15 ; REGISTER EQUATES	67; ADD ANY OVERFLOW TO BCD STORE 68 0019 27 69 CLR A 001A 7C 70 ADDC A,BCDO 001B AC 71 MOV BCDO,A
0004 17 BCD0 EQU R4 ;LSD'S OF BCD STORE 0003 18 BCD1 EQU R3	73 74 ; ENDO (WHEN SHIFT COUNT COMPLETE) 75
0002 19 BCD2 EQU R2 ;MSD'S OF BCD STORE 0005 20 COUNT EQU R5	001C EDO6 76 DJNZ COUNT,STRTDO ;DONE YET? 001E 83 77 RET ;YES-EXIT
22 , CONSTANT EQUATES 23	79 , END OF ROUTINE 80 END
0010 24 PREC EQU 16 ;PRECISION OF BINARY 25 26 B2D:	USER SYMBOLS B2D 0000 BCDO 0004 BCD1 0003 BCD2 0002 COUNT 0005 PREC 0010 STRTD
27 ; INITIALIZE BCD STORE 0000 27 28 CLR A 0001 AC 29 MOV BCD0,A 0002 AB 30 MOV BCD1,A 0003 AA 31 MOV BCD2,A	ASSEMBLY COMPLETE, NO ERRORS
32 ; INITIALIZE LOOP COUNT 0004 BD10- 33 MOV COUNT, #PREC ; NUMBER OF BITS OF	F BINARY TO CONVERT ISIS-II ASSEMBLER SYMBOL CROSS REFERENCE, V2.0
35 ; DO OVER ALL BITS OF BINARY DATA 36 ; BCD VALUE = BCD VALUE # 2 37	B2D 26# BCD0 17# 29 39 40 42 70 71 BCD1 18# 30 44 45 47
38 STRTDO: 0006 FC 39 MOV A,BCDO ;LEAST SIG DIGITS 0007 6C 40 ADD A,BCDO ;X2 0008 57 41 DA A 0009 AC 42 MOV BCDO,A ;SAVE	BCD2 19# 31 49 50 52 COUNT 20# 33 76 PREC 24# 33 STRTDO 38# 76
000A FB 44 MOV A,BCD1 000B 7B 45 ADDC A,BCD1 ;X2 000C 57 46 DA A 000D AB 47 MOV BCD1,A ;SAVE	CROSS REFERENCE COMPLETE
000E FA 49 MOV A,BCD2 000F 7A 50 ADDC A,BCD2 ;X2 0010 57 51 DA A 0011 AA 52 MOV BCD2,A ;END OF BCD MULT	8048 Conversion Routine

Designers' Notebook

PLL Handles Small, 0.05-Hz Signals

The classic PLL (as described by Gardner) has a sine wave VCO output which is multiplied by the input signal. If the signal and the VCO output are square waves, the multiplier reduces to an Exclusive OR gate, as in the CD4046 PLL. The signal is converted to a square wave by a self-biased, high gain amplifier (Fig 1a). The typical input sensitivity, with a 10 V power supply, is 400 mV, giving a dynamic range of only 28 dB.

The loop center frequency can be extended to arbitrarily low frequencies by including a ÷N counter between the VCO output and the phase comparator input (Fig 1a). However, the output of the high gain amplifier oscillates at low input frequencies, thus reducing the tracking accuracy of the loop.

The addition of an external zero crossing detector with hysteresis (Fig 1b) will give a clean square input to the PLL at low frequencies and will also

Input amplifier

2
Phase Comparator 1

VCO
CD4046

(a)

To PLL Input
CA3130

To PLL Input
(b)

extend the dynamic range of the loop. With the values shown, the dynamic range is increased to 80 dB. The modified loop has been used to track 0.05 Hz sine waves.

R. H. Smallwood, Weston Park Hosp., Sheffield Univ., and Area Health Authority, Dept. of Medical Physics, Sheffield, England.

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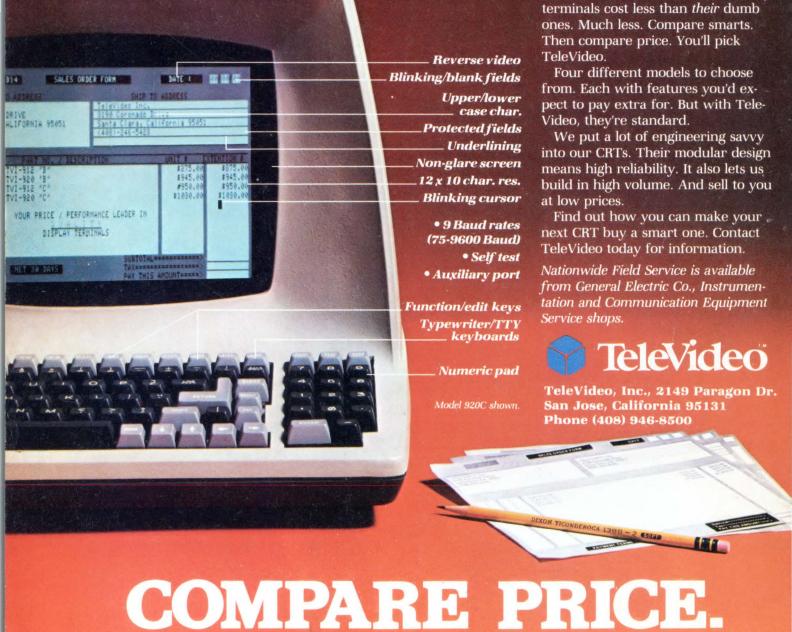
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