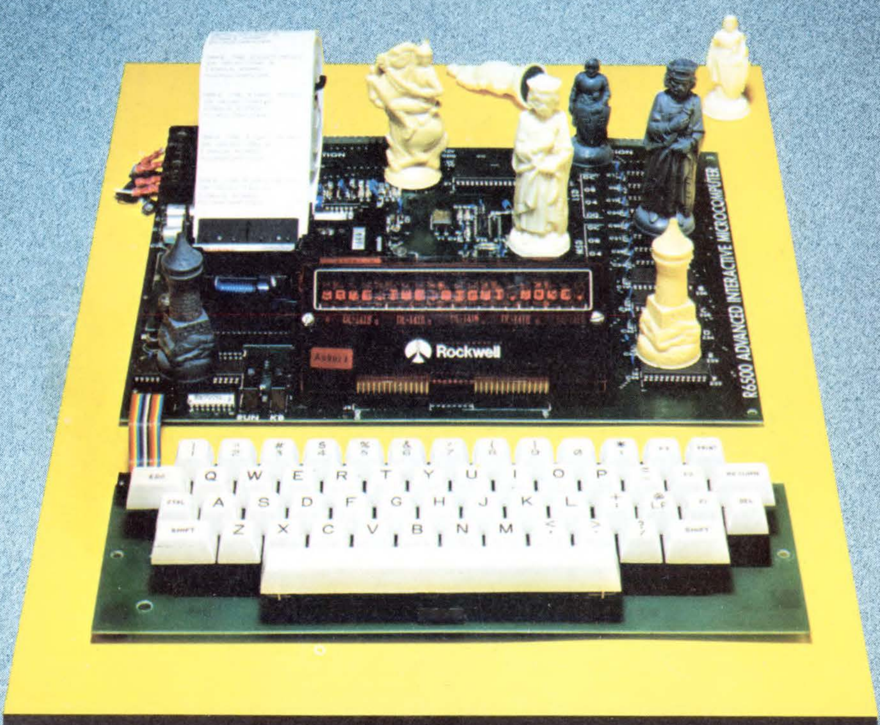
VOLUME 10, NO. 3

MARCH 1980

Digital Design

The Magazine of Systems Electronics

Special Report: Single-Board Computers



Graphic Displays: Spatial Resolution

Computer Printing

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Series 9000...
still the class act in digital tape transports.

Being the best in your business is neither boring, tiresome or repetitive—it's challenging. Now that we have the most dependable and advanced tape transports in the world—what's left?

Delivering them. On time and on-line faster than anyone. That's what! They still have all the features:

- A position arm anticipatory sensing system. An exclusive Kennedy feature, the linear, non-contact (Mag Pot) position sensor requires no lamp source and assures performance for the life of the machine.
- Interchangeable electronics on all Series 9000 transports, reduce stocking costs and down time.
- Front-accessible off-line test panel; marginal skew check; threshold scanning which automatically compensates for drop-ins or drop-outs; Read-After-Write shortened skew gate; simplified tape path and quick release hubs.
- All models are available with either 7 or 9 track, 800NRZ1, 1600 PE or 800/1600 NRZ1/PE.
- 7 and 9 track NRZ1 and PE format/control units to simplify customer electronics. Also, a variety of popular mini-computer mag tape controllers are available. Series 9000's performance is as impressive as its features, with data transfer rates to 72KHz, and tape speeds from 10 to 45 ips.

Being best is nice. So is being fast. Kennedy is both.

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Circle 2 on Reader Inquiry Card

The Chill-able Computer System

Configure Your Severe Environment System With Our SECS 80/10A Microcomputer And Support Modules

Buy a few cards or a complete system

Take our ruggedized SECS 80/10A Microcomputer, a functional counterpart of Intel's standard iSBC* single board computer, surround it with our equally ruggedized support modules, and you have the building blocks you need to design a system which will operate under the most severe environments.

This versatile SECS 80 System likes it cold — or hot. Meets Mil-E-5400, 4158, 16400- and more, making it perfect for space, missile and other military systems and tough industrial applications.

A multitude of modules

With these versatile modules, you'll save valuable time and development costs.

- **SECS 80/10A Microcomputer**
- **RAM, ROM & EPROM Memories**
- **Digital Tape Recorder & Controller**
- **1553 Serial I/O Board**
- **Digital Input/Output Board**
- **Analog To Digital Converter**
- **High Speed Arithmetic Unit**
- **Power Supplies**

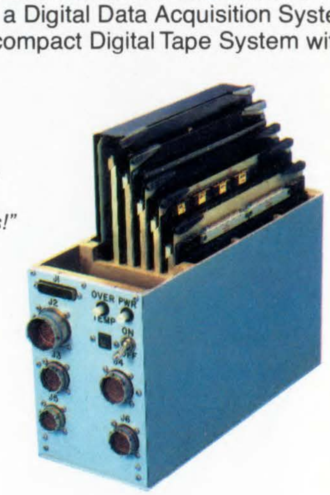
System packaging

All system modules are mounted on 9″ by 6″ shock and vibration resistant boards. A 7.62″ by 4.88″ 12.62″ chassis (½ ATR) holds up to 6 boards.

Other EMM-SESCO products

We've got core and semiconductor memories for military and commercial use, a Digital Data Acquisition System for the 1553 bus, and a compact Digital Tape System with 23 megabit capacity.

When you're faced with a tough environment – "Buy SESCO... it works!"



*Trademark of Intel Corporation

EMM SESCO
A Subsidiary of Electronic Memories & Magnetics Corporation
20630 Plummer Street • P.O. Box 668 • Chatsworth, California 91311
Telephone: (213) 998-9090 • Telex: 69-1404

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Winchester users we did it!

We've put a price tag on your backup dreams.

DEI is happy to announce our new 10 and 20 MByte high density streaming cartridge tape drives.

The basic 10 MByte is $415, the 20 MByte is $525. And here's what you get for the price:

Speed: Transfers data at 5 MByte/ per minute.

Capacity: Just what you want. 10 or 20 MBytes. A perfect match for the 8" or 14" Winchester.

Reliability: We certify our cartridges to provide it for you.

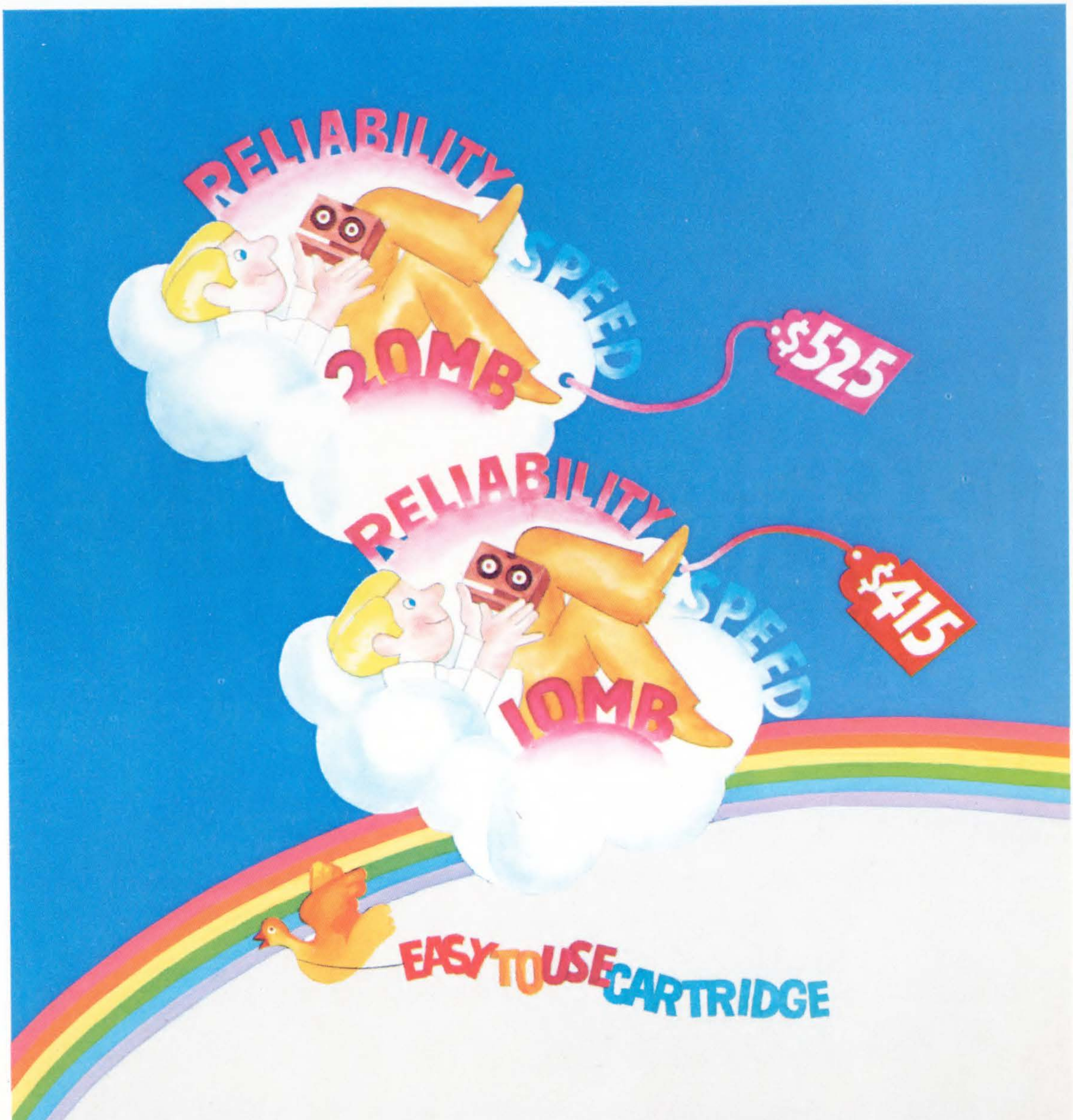
Ease of Use: Cartridge operation is simple enough for a person without any computer training to use.

Size: Compact enough to be interchangeable with flexible disks.

Streaming Electronics: Optional formatter and streaming controller with automatic gain control and interdispersed resynchronization. Error correction is also available as an option.

Delivery: Right now!

Now that we've got them, all we can say is "come and get it." They're your backup dreams come true!



DEI

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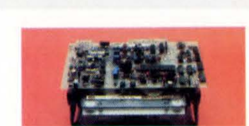
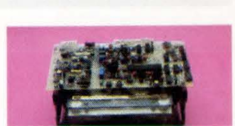
Call (714) 452-7840. Telex 67-5327.



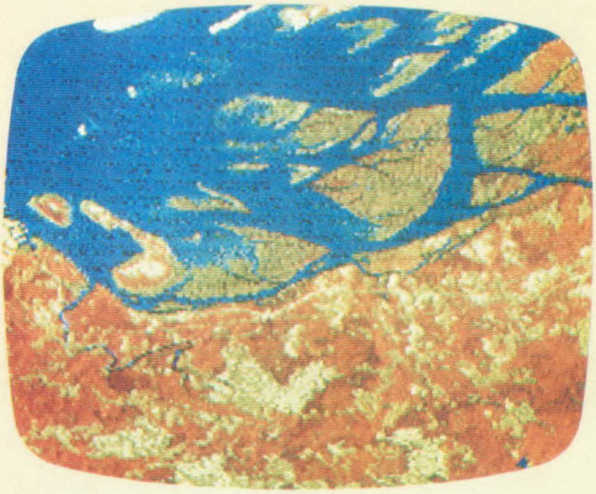
10 MByte Cartridge Tape Drive

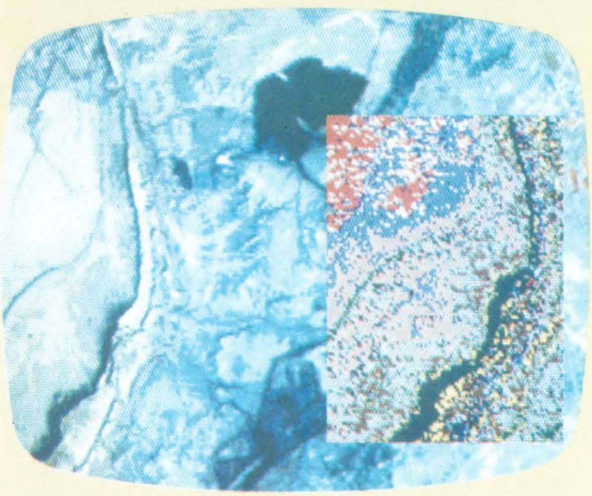


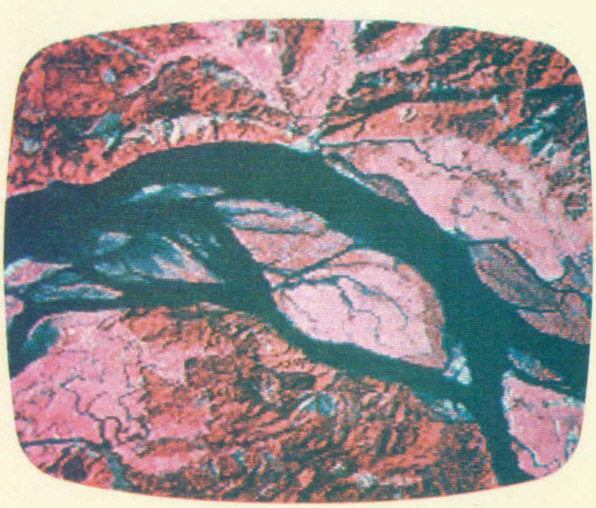
20 MByte Cartridge Tape Drive

Circle 6 on Reader Inquiry Card

Image processing. Your way.







Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
- Image multiplication and ratioing
- Zoom and pan
- 512 x 512 panning window on a 1024 x 1024 image
- Function memories
- Pseudo-color tables
- Video digitizers with frame averaging
- Split screen and image toggling
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- Plug compatible interfaces for most minicomputers

In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 512 to 1024 x 1024.

So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

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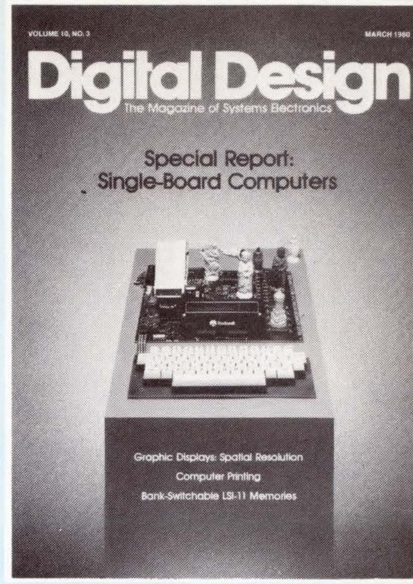
VOLUME 10, NO. 3 MARCH 1980

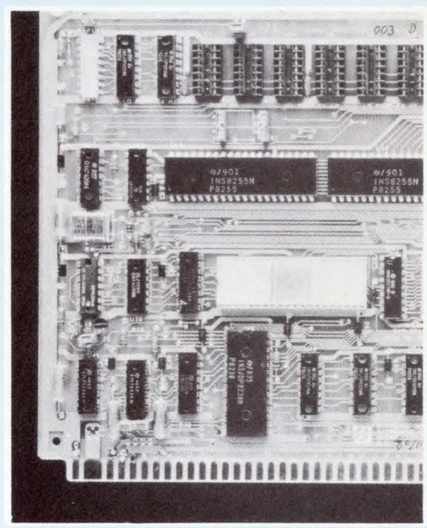
Digital Design
The Magazine of Systems Electronics

Departments



ON OUR COVER

AIM-65, a single-board microcomputer, provides keyboard and display and hooks up to a System 65 or EXORcisor development system, or can operate in a stand-alone mode. Photo courtesy of Rockwell International. Cover design by David Bastille.



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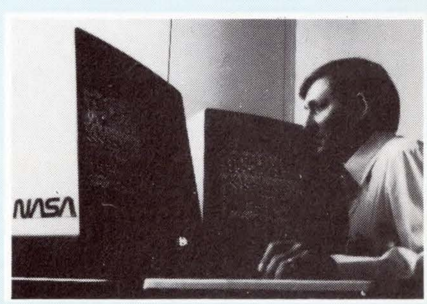

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Letters

Lawyers Flood the Market

Dear Editor:

I enjoyed your Speakout, "The Winds of Change" (Part 1), in the September issue. But, as a lawyer, I disagree with criticism No. 7. You said that, "Readers asked for restrictions on engineering school enrollment – as done by the AMA. Doctors, lawyers and dentists through their AMA, ABA and ADA (and strong political action and lobbying) strictly control their graduates. One reader suggested that to cut medical costs, academics flood the market with MD graduates (but pointed out that unlike IEEE, the AMA has political muscle to stop any such attempt)."

I disagree! The American Bar Association has no control as to how many people go to law school, or how many law school graduates can be admitted to the bar. Yes, law schools are economic bonanzas for universities, because they don't require large labs and frequently, a professor can lecture to 100 or more law students at a time. They're flooding the market with lawyers. This encourages many universities to start law schools, even though no jobs may exist for the law students when they graduate. These lawyers don't earn much.

State supreme courts regulate bar exams and admission to the bar. But most courts make the passing percentage high.

Robert Bigelow
Law Offices of Robert P. Bigelow
Woburn, MA

A Welcome Breeze?

Dear Editor:

Your Speakout, "Winds of Change" (Oct. and Nov.), is a welcome breeze. I realize that news handouts, press releases and announcements provide editors with much material, but there is no reason that a press release from Feerst should be the basis for information. Here's why.

Did Feerst "start something that IBEE could not ignore forever"? No. Young began the Professional Activities Committee in the Santa Clara Section about 7 years ago (before official sanction on a national basis) and worked for the "working EE" for a long time. Incidentally, is an academic, high executive or corporate in the IEEE not "working"? Why not say "engineering practitioner"?

But what bothers me most is the "conspiracy theory." Do conspiracy and tales of intrigue have a place in magazines? Was Young "surreptitiously sponsored by the IEEE hiearchy" "to split the reform vote"? No. I investigated the Board of Director's choice for President, but decided to back Young. Why? I backed him because of his record and platform – not because I "surreptitiously" tried to split the reform vote.

I hope you continue to exert your influence for the Institute's betterment.

Alfred H. Barauck, PE
Palo Alto, CA

The Best. . .

Dear Editor:

One of the best issues (August) you've published.

Lloyd J. Frei
Univ. of Iowa
Iowa City, IA

Small Size

Dear Editor:

Just a quick note to compliment you on the September cover; it is one of the nicest I've seen. The issue was great, but the address you used for Computer Devices, Inc., in the same issue (page 42) changed. The new address is:

Computer Devices, Inc.
25 North Avenue
Burlington, MA 01803

By the way, the next time you do an update on mini-floppies, here's proof to BASF's claim to smallness. After we enclose their drive in our cabinet, total weight is 4 lb. 11 oz. and the dimensions are 9 5/16″ x 6 1/2″ x 3″. I've enclosed a photo.

Richard Herzfeld
Marketing Communications
Computer Devices, Inc.
Burlington, MA

8″ Hard Disks

Dear Editor:

"Guide to 8″ Hard Disks" (August) is excellent. Great information.

Lloyd F. Bazant
Western Instruments
Albany, NY

System Designer's Guide

Dear Editor:

In your informative article, "System Designer's Guide to 8-inch Hard Disk Drives" (August 1979), you stated that: "BASF claims this argument for the 200 mm disks. BASF, which had been providing 210 mm evaluation disks to users, discontinued its 210 mm microdisk, which is not listed on our chart". This inadvertent typo juxtaposed the two values, as we provided 200 mm evaluation units, but discontinued them, and then decided upon the more stable 210 mm diameter (as did IBM). Our 210-mm 6170 Fixed Disk Drives are listed correctly on the chart.

The BASF family of drives offers capacities of 8 and 24 MB, an average access time of 42 ms and a transfer rate of 800 Kb/s. Density is 6542 bpi and 500 tracks/in. We are one of the first companies to develop such a drive and expect to ship units in quantity in November.

John B. Saynor
BASF Systems
Bedford, MA

More Printers

Dear Editor:

The article concerning the selection/purchase of printers was a clear, concise, and useful inclusion. This type of information and article should be included monthly highlighting 12 different segments of the peripheral industry. Along with this, it should be continued on a year to year basis providing insight as to product advances and new manufacturers. The ability to send away for information in an easy, reliable fashion enhances this service greatly. I wish I had more room. Thanks for a fantastic job.

Ted Ross
899 E. Green
Pasadena, CA

Proprietary CAD Systems

Dear Editor:

The article "Design Tools for Multiprocessor Systems" (October 1979) did not mention that Raytheon's CAD system (of which CDL is a small portion) is a propriety product and not available for non-Raytheon use on any basis.

F. S. Hembrough
Raytheon Co.
Bedford, MA

From DeAnza Systems VISACOM Visual Computer System

An extraordinary combination of micro-computer power and DeAnza Systems imaging expertise

VISACOM is a new image graphics concept that provides enormous flexibility for the user. It is powered by a DEC LSI/11 micro-computer with the ability to address 512K bytes of memory. The system operates under RT11 and has all the standard DEC LSI/11 software.

The system can operate off-line with floppy disks or interface to a host computer.

VISACOM as a Computer

- **Addresses 512K Bytes memory**
- **Extended arithmetic operations**
- **DEC LSI-11 compatibility**
- **RT11 Operating System**
- **Fortran IV**
- **Q-Bus compatible peripherals**
- **Dual access MOS RAM memory**
- **User software package**
- **RS 232 and DMA interfaces**

VISACOM as a Display System

- **512 X 480 Image Window**
- **16 bits per pixel**
- **Zoom and Scroll**
- **Intensity Transformation units up to 4096 words**
- **Independent A/N and Cursor Overlays**
- **User software package**

For further information and a list of satisfied users, contact DeAnza Systems, Inc., 118 Charcot Ave., San Jose, CA., 95131, (408) 263-7155.

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A Wilson Exerciser lets you locate problems so much faster, make adjustments, and perform preventive maintenance so efficiently that it guarantees faster, more thorough service calls.

Even intermittent problems don't require waiting for access to a computer or programmer to run diagnostics. Internal programs in the Exerciser can automatically cycle operation of the unit being tested until the fault appears.

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Letters

UNIX, TECO, CANDE

Dear Editor:

How about a short write-up explaining what UNIX, TECO, CANDE, and Programmer's Workbench are. These were mentioned on pg. 27, Nov. 1979 Software Design Series. I bet many readers have never heard of them.

D. Barditch
Baltimore, MD

The author, Dr. Lance Leventhal, responded with this definition of terms:

1) UNIX is a time-sharing operating system with extensive file structures that was developed at Bell Telephone Laboratories. It is now available commercially for PDP-11s and in modified form for LSI-11s, VAX-11/780, and Z-80 or 8080/8085-microcomputers. Relevant references are D.M. Ritchie and K. Thompson, "The UNIX Time-Sharing System," *Communications of the ACM,* July 1974, pp. 365-375, K. Thompson and D.M. Ritchie, "The UNIX Time-Sharing System," *Bell System Technical Journal,* July-August 1978, pp. 1905-1930, and B.W. Kernighan and P.J. Plauger, *Software Tools,* Addison-Wesley, Reading, MA, 1976.
2) TECO is a context-oriented character editor developed by Digital Equipment Corporation for a variety of their computers. It is available from DECUS (the DEC User's Society), although it is not supported by DEC.
3) CANDE is a time-sharing option for the Burroughs B6700 computer. It includes a line-oriented editor and a data entry language. It allows the user to handle files and run programs interactively.
4) Programmer's Workbench is an integrated set of software design and development tools, written in the C language and running under the UNIX operating system, that has been developed at Bell Telephone Laboratories. A relevant reference is T.A. Dolotta and J.R. Mashey, "An Introduction to the Programmer's Workbench," Proceedings of the 2nd International Conference on Software Engineering, pp. 164-168.

Floppy Disk Drives

Dear Editor:

I liked December's comments on double-sided floppy disk drives ("Floppy Disk Drives", p. 62) by G. Goodman of Remex and "Magnetic Bubble Memories" (p. 88) by P. Snigier.

Donald K. Georgi
Teksym Corp.
Wayzata, MN

Likes Bubble Memories

Dear Editor:

December's "Magnetic Bubble Memories" by P. Snigier on pg. 88 is excellent. Could you cover more on magnetic bubble controller design comparison?

Dr. H.J. Chen
Bell Telephone Labs
Whippany, NJ

Speakout

Paul Snigier, *Editor*

The Time Has Come

Executive magazines still warn their readers to shy away from microcomputer-based small business computers (SBCs). Charges were (and are) made that these systems are Mickey Mouse "toys" that suffer from poor reliability, inadequate capacity and inability to grow with the firm's (or department's) needs — not to mention less-than-desirable service. Some of these businessmen relate horror stories and tell of hidden costs that wait, like icebergs, to snare the unwary. Is it true? Unfortunately, much of what these executive publications said (and say) is the truth.

Small business users aren't the only ones to experience woes. Our staff used one of these once-famous, now-vintage systems up until 14 months ago (for engineering use only), and it was a dog. MBTF was poor, and service was poorer. It didn't do what its once-famous manufacturer so grandly claimed it would; and although we used it *only* for engineering and scientific applications, pity those poor small businessmen who fell for the siren song and used it in critical applications.

As EEs, don't we all remember the naive microprocessor hoopla of the past five years? Of how housewives and truckers would become μComputerists (as if they had nothing better to do), about how micros were going to do everything for small businessmen, and all those numerous cottage shops that sprung up like weeds and claimed they were going to take over the world. It was a time of exaggerated claims. But most successful and knowledgeable businessmen didn't buy it. But many of those that did, got bitten and told woeful tales of their bad experiences. One cottage shop (it grew into a middleweight) placed ads in the *Wall Street Journal* and in the financial pages of major newspapers across the nation, but found the time wasn't ripe for the SBC market. This firm lost money; many others just died, and their names are mere memories today.

So, the SBC market, a vast market of immense proportions, never really took off as predicted. It wasn't due to ignorance of the potential customers, but due to the inadequacy of these μC-based systems.

In another closely-related market (one also with explosive growth potential for OEMs), electronic office systems also had their share of bad luck. Poor equipment and a lack of totally integrated or multi-function office systems often brought more curses than blessings. This μC-based equipment all too often duplicated operational costs and added redundant hardware and software costs. It was an infant technology where equipment was outdated so fast that many systems were cost-ineffective within half-a-year of use. System designers not familiar enough with the office environment created systems that merely replaced equipment (not functions), created infighting between DP and WP personnel, upset traditional power structures, and antogonized users (particularly executives). Worse, system designers all too often created poorly-designed equipment that couldn't be integrated into an overall system. Benefits were not what was promised, and once again (just as with the SBC), much of the equipment for the electronic office fell into disuse. Things are about to change.

Key to this change is not education of end users, but improvements made by the electronics, peripheral, semiconductor and microcomputer industries. The μC industry has reached the critical threshold where the original condemnations are no longer valid. Improved semiconductor devices, new mass storage systems (8- and 5-inch Winchesters and high-density, dual floppies), bubbles, lower-cost and higher-MTBF printers and CRT terminals will soon make their full impact. The 16-bit micro-based systems are no longer toys; they will replace today's 16-bit minis (and the mini makers will move up into the 32-bit arena). And hidden costs are coming out into the open, MTBFs are rising and service is improving.

This "coming of age" of the SBC and electronic office system has arrived just in time to meet sudden demand for such systems. Small businessmen and office managers are faced with major problems that are growing worse. This includes increased paperwork, overburdened records-retention systems, greater government-mandated red tape, and inability of many smaller businesses to compete with larger firms. It's also an area ripe for improvement in efficiency. While industrial productivity grew 90% in the last decade, managerial and office productivity grew less than one percent. This sector is coming to represent a more significant portion of a firm's operating expense. Not only that, but corporate executives of all firms are coming to realize that their managers will need better information and management systems to effectively manage their businesses.

Unfortunately, the computer brings trouble. It brings with it an avalanche of hardcopy output—much of it extraneous and onerous. Records retention woes, despite microfilming of original documents, is undesirable for many uses (particularly for SBCs).

Then, there is a far-more fundamental problem than mere records retention and the paper blizzard. It is something analogous to the "combinational explosion" (discussed in November's *Speakout*, "Designing For the 1980s: Heuristic Outlooks Needed"). End users are being inundated with greater quantities of information; and the more it grows, the greater are the interrelationships, and the greater the difficulty of making sense from it all. We've all seen the cartoon of the manager with his thick copy of computer printout conveniently near the edge of his desk, just above the wastebasket, waiting for the next printout so he can nudge this one in over the edge. The "information explosion" is growing worse, and it can choke a business, not to mention careers.

The new developments in electronics that I mentioned above can solve this in three ways. **First**, improvements made by CRT terminal makers and on-line systems is minimizing records retention without sacrificing accessibility in records research. The SBCs and office information systems of the 1980s will reduce record file requirements. **Second**, system designers all-too-often design from an equipment-replacement philosophy — a myopic process of direct substitution. The system designer of the early 1980s must, instead, capture the features of each device or function to maximize the benefits of the total office system. In other words, designers must stop the process of mere equipment substitution and take a functional systems approach. **Third**, and most important, SBC and office systems must do more of the pre-processing of raw data in decision-making tasks. It is not a question of how much information that the manager sees, but how little he sees. With more decision-making functions or algorithms integrated into systems, the less burdened managers will become, thus freeing them to concentrate on the trouble spots. Such intelligent microcomputer-based SBC and electronic office systems will force management-by-exception on workers — whether they realize it or not.

OEMs will provide end users with managerial work stations in each office that have direct access to large amounts of data and data bases, so they can make strategic decisions with up-to-date information that has been pre-processed. CRT terminals will become commonplace in executive offices, as well as voice data-entry terminals. With intelligent voice entry expected to eliminate coding, keypunching and manual data entry *throughout the firm*, information will be processed instantly and be available at all levels. Data entry times will be reduced and productivity increased. The rate of information flow will be increased several orders of magnitude.

The market is enormous, and not only is there room for traditional giants like IBM, Xerox, Wang, AT&T and Exxon, but for small OEMs as well. If the road sounds paved with gold, it isn't without its share of bumps and potholes that can knock out the less-wary firms. It will require a new breed of systems designer. For those engineers who are prepared, career opportunities in these fields never looked so great.

TODAY MAY BE THE BEST TIME TO MAKE YOUR CAREER MOVE

But first make sure your new employer measures up.

With all of those prospective employers trying to attract your engineering skills, now is the best time to look beyond "just a job" and consider your career. Your real objective is to find the perfect combination—challenge, satisfaction, security, and reward. To assist you, we've prepared a checklist of points to consider when you're evaluating a new employment possibility. It's a good way to compare the companies seeking your expertise.

Career Opportunity Checklist for Engineers

INDUSTRY GROWTH AND STABILITY *No one wants to be "phased out," so check for security:*	YES	?	NO
Is the company part of an industry that's vital, growing, dynamic?	☐	☐	☐
Will the growth continue throughout the 1980s and beyond?	☐	☐	☐
COMPANY HISTORY AND REPUTATION *You can tell a lot about a firm by its track record:*			
Is the company recognized and respected in the industry?	☐	☐	☐
Have sales and profits increased at a steady rate?	☐	☐	☐
Is it known for its technological innovations?	☐	☐	☐
Are its employees motivated and well rewarded?	☐	☐	☐
Does the company seek technological employees on a permanent, ongoing basis?	☐	☐	☐
WORKING CONDITIONS AND ENVIRONMENT *Look for good people, team spirit, and top-notch facilities:*			
Is the atmosphere one of loyalty, pride, and achievement?	☐	☐	☐
Do employees welcome the challenge of difficult assignments?	☐	☐	☐
Are creativity and independent thinking encouraged?	☐	☐	☐
Are the company's engineering goals clear-cut and attainable?	☐	☐	☐
THE COMPANY LOCATION *Relocation is a big professional and personal commitment.*			
Is the company located in an existing or emerging electronics center?	☐	☐	☐
Are there major universities and other technological resources nearby?	☐	☐	☐
Will the company assist me in relocating?	☐	☐	☐
Can I provide my family a comfortable lifestyle in this area?	☐	☐	☐
Are there cultural and entertainment opportunities?	☐	☐	☐
Is there a variety of recreational and leisuretime activities?	☐	☐	☐
Are the climate and surroundings pleasant?	☐	☐	☐
PERSONAL AND PROFESSIONAL GROWTH *Job satisfaction means more than just a paycheck:*			
Does the company give full recognition to the engineering role?	☐	☐	☐
Will I be working and interacting with other talented professionals in my field?	☐	☐	☐
Will my accomplishments be acknowledged, appreciated, rewarded?	☐	☐	☐
Will I be encouraged to seek more challenge and responsibility?	☐	☐	☐
Will the company pay for advanced training in technology and management?	☐	☐	☐
Can I pursue my own career goals within the company framework?	☐	☐	☐
THE LONG RANGE PICTURE *Where will you be professionally in 5 years?...in 10 years?*			
Are there plenty of opportunities for rapid advancement within the company?	☐	☐	☐
Does the company encourage engineers to assume positions of authority?	☐	☐	☐
Will I be allowed to move into those engineering areas that interest me most?	☐	☐	☐
Can I choose my own career path—into technological leadership or executive management?	☐	☐	☐

One Company to Evaluate

At Racal-Milgo, we're looking for capable communications hardware and software people to join our engineering team. Our success has created needs at every level, from entry to top management. We have a lot to offer you.

The mainstream of our business is data communications—where today's action is. We're a pioneer, and a recognized leader in the field. Our state-of-the-art product lines include modems, multiplexers, data encryption, and systems for sophisticated network control and performance assessment.

We're proud of our growth—$64 million in sales two years ago, $80 million last year, and over $100 million this year—and we're still growing. Applied research and technology keep us on the leading edge in data communications; our engineers face some of the industry's most challenging (and rewarding) responsibilities.

Racal-Milgo is a great place to work. We encourage our technical people to think creatively, to turn their innovative ideas into successful products—in an atmosphere of friendly, professional teamwork. We provide them with one of the nation's most advanced engineering facilities. Our salaries and benefit programs are among the best in the business.

We're located in suburban South Florida, one of the growing new electronics centers in the sunbelt. It's an international area, gateway to Latin America, blessed with a pleasant climate year-round. There are excellent cultural and entertainment opportunities, plus swimming, diving, boating, sport fishing, golf, tennis, and all the other benefits of a cosmopolitan resort. There's a wide choice of employee clubs to introduce you and your family to new activities. And if you're interested in furthering your professional or business related education, we'll pay for your coursework at any of the major universities nearby.

At Racal-Milgo, we're experiencing dynamic growth, and we need good people at all levels. The working conditions are excellent...advancement and rewards come fast...and our new two-track career program lets you decide whether to rise to the top on the technical side or to move into management. (Our president and board chairman are both EE's.)

We're looking for the best. If you are too, let's get together. I hope to personally welcome you aboard. Send me your resume today; no letter required. You'll receive a prompt reply.

Ed Hilpert

Ed Hilpert
Vice-President, Engineering

Racal-Milgo™

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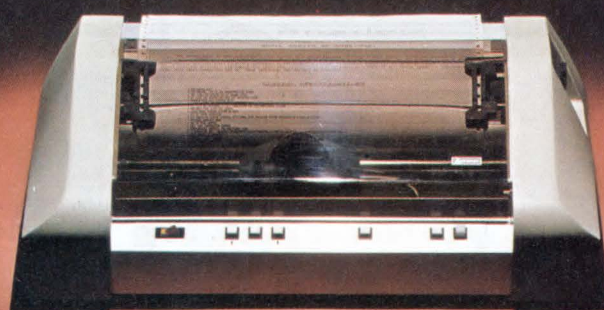
Meet two new Printers from Anadex:

Resolutionary!



Introducing two totally new alphanumeric line printers from Anadex – Models DP-9500 and DP-9501 – featuring 132/175 or 132/220 columns, respectively.

Both models employ a new, Anadex-manufactured 9-wire print head with 150 million character life (optionally, 650 million) that makes them ideal for high-resolution printing requirements including high-density graphics where print quality and reliability must go hand in hand.

The full standard 96 character ASCII character set, including descenders and underlining of all upper and lower case letters, can be printed bi-directionally on up to 5 crisp copies at speeds up to 200 CPS. Adjustable-width tractors, accommodating paper from 1.75 to 15.6 inches wide, allow the printers to adapt to your application.

The three ASCII compatible interfaces (Parallel, RS-232-C, and Current Loop) are standard in every printer; so interfacing is usually a matter of "plug it in and print." With simplified interfacing, the printers also feature sophisticated communications capability including control of Vertical Spacing (6 or 8 lines/inch), Form Length and Width, Skip-Over Perforation, Auto Line Feed, and full point-to-point communications capability.

Other standard features are a 500 character FIFO buffer (optional, an additional 2048 character buffer), shortest distance sensing logic, self test, and replaceable ribbon cartridge with 6 million character life.

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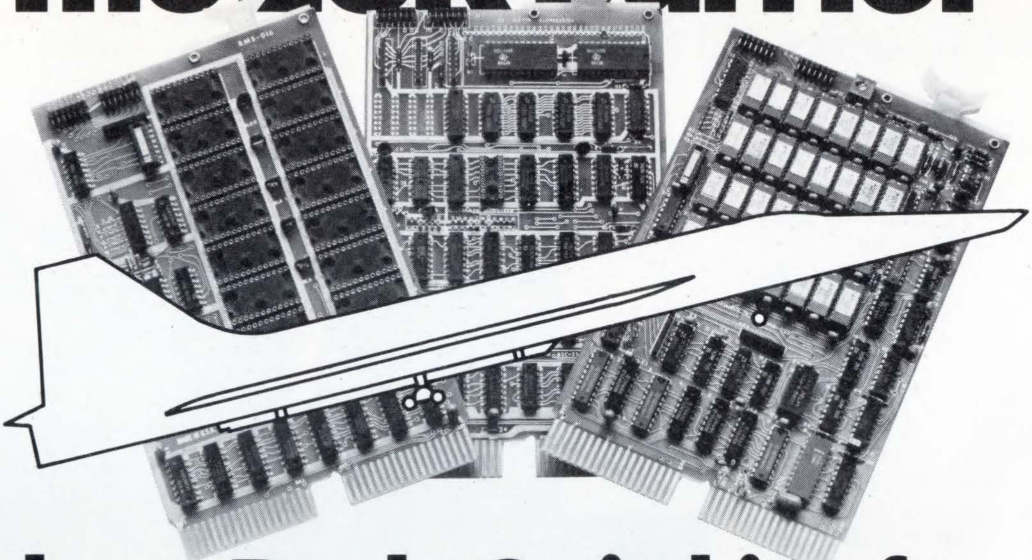
Let your LSI-11* break the 28K barrier



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BSC-256	The Bank-Switch Controller	$300 (Single qty.)

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DIGITAL PATHWAYS

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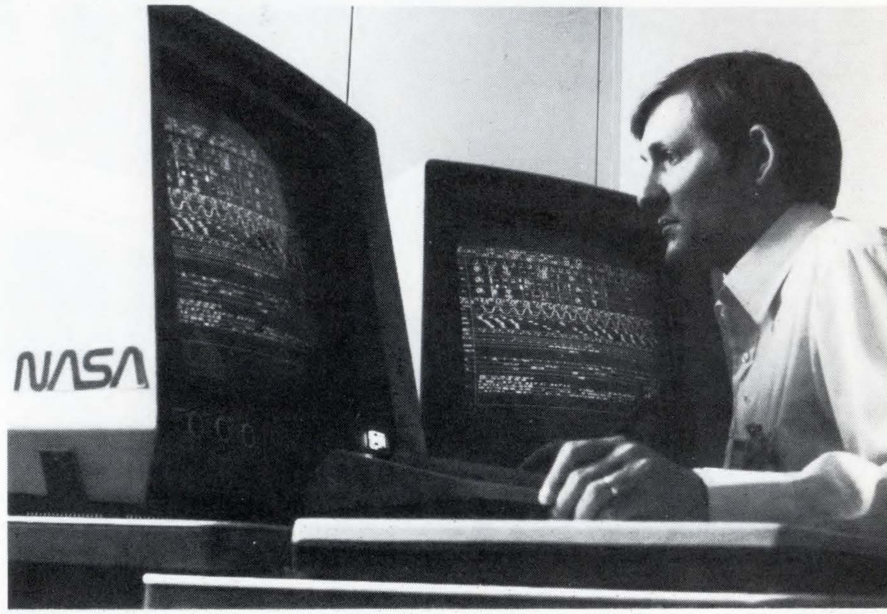
Technology Trends

Computer Graphics Aid Space Shuttle

Computer-driven display systems to help NASA ground crews plan space shuttle crewmember's activities before each flight, undergo checkout at NASA's Lyndon B. Johnson Space Center, Houston, TX. The Sanders Associates, Graphic 7 displays are part of NASA's Crew Activities Planning System, a computerized system for planning crew schedules for eating, sleeping, exercising and performing experiments. The displays also depict spacecraft trajectory information such as ground track, acquisition and loss of ground stations and daylight/darkness cycles. Because the information is visual and in easily-readble form, it makes it easier for NASA scientific personnel to solve complex planning problems in less time than required previously.



LOGIC ELEMENTS

Japanese Develop Josephson Junction Computer

Consider the computer of the future: a cube 6" x 6" x 6" operating at a switching speed of 10 ps or less at 4° above absolute zero – a machine using Josephson technology. It corresponds in performance to today's big mainframes occupying a dozen cabinets or more.

Not long ago Fujitsu, Ltd., brought the practical realization of the Josephson computer a little closer. It developed a 4-bit logic circuit with Josephson junction elements called "double junction quantum interference elements."

Fujitsu has simplified the device by requiring only three Josephson junctions elements per 1-bit circuit, compared with the seven Josephson junction elements used by a competitor.

Fujitsu scientists are now planning 64-bit memories based on the Josephson principle and hope to have them by next year.

Josephson circuitry, named for its inventor, Brian Josephson, requires minimal power so that space-wasting heat sinks are unnecessary. The cryogenic temperatures at which it operates are achieved through the use of liquid helium.

Fiber Optic Production Rising

Worldwide production levels of fiber optic systems will surge dramatically from $39 million in 1978 to $1.77 billion in 1990, according to research by Gnostic Concepts, Inc. of Menlo Park.

By the mid 1980s, optical fiber communication system production levels will grow, with dropping prices justifying them as an alternate transmission media on a strictly cost competitive basis. At this stage, an increase in production levels of fiber optics will further reduce prices and continue penetration of fiber optics into additional installations.

Total fiber optic cable system demand for Canada, US, Japan, and Europe will grow from $39 million in 1978 to $659 million in 1985 and to $1.77 billion by 1990, as shown below.

This growth represents an average annual increase in value of 50% for 1978 through 1985, and 20% annually between 1985 and 1990. These values include cable assemblies plus transmitters, receivers, connectors and splices.

Fiber Optic Cable System Demand

($ M)

	1978	1985	1990
Canada	6	40	85
US	21	350	889
Japan	2	91	333
Europe	10	178	462
Total	$39M	$659M	$1.77B

Use of Data Communication Terminals Will Grow Sixfold By 1990

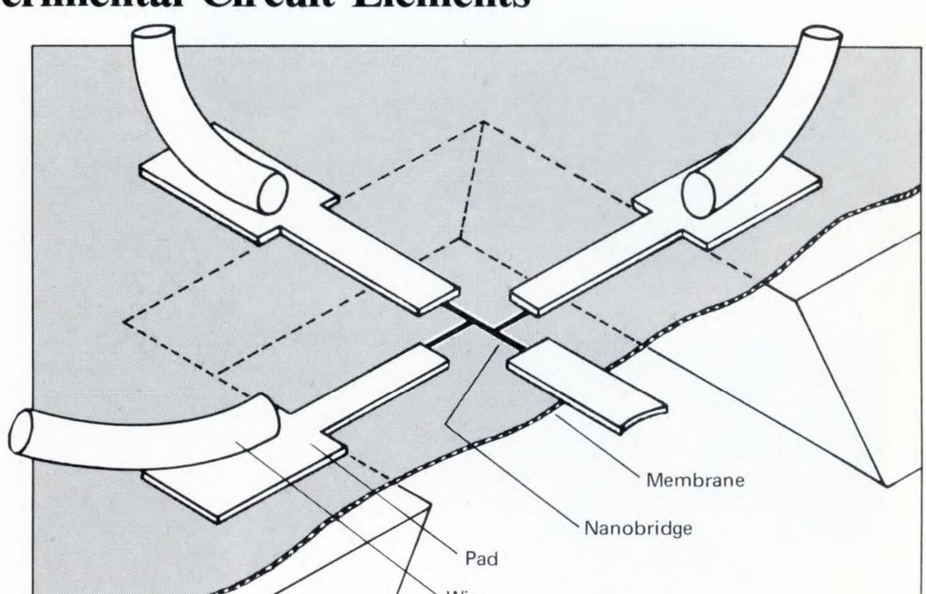
In 1990, over 15 million data communication terminals will be in use – up from 2.5 million in 1978 – representing one terminal for every six white collar workers. According to "Data Communication Systems and Equipment," (Predicasts, Cleveland, OH), terminal usage will skyrocket as computers diffuse rapidly through all segments of the economy, reflecting both the benefits of computer-processed information and the declining investment and operating costs. Shipments of data communication terminals – remote I/O devices linked to a computer over a communication channel – are projected to grow from $1.6B in 1978 to nearly $7B in 1990. "Intelligent" terminals, which are programmable and possess some degree of processing capability, will be the fastest growing segment with sales climbing over 20% annually.

Item	1963	1978	1990	%Annual Growth 1963 -78	1978 -90
Data Terminal Shipments	3	1600	6900	52.0	13.0
Net Exports	–	530	1050	–	5.9
Data Terminal Sales	3	1070	5850	48.0	15.2
Autotransaction Terminal Shipments	–	965	1900	–	5.8
Net Exports	–	10	–250	–	–
Autotransaction Terminal Sales	–	955	2150	–	7.0
CWP* & Facsimile Terminal Shipments	5	336	1340	32.4	12.2
Net Exports	–	–12	–5	–	–7.0
CWP & Facsimile Terminal Sales	5	348	1345	32.7	11.9
TOTAL TERMINAL SHIPMENTS	8	2901	10140	48.1	11.0
Net Exports	–	528	795	–	3.5
TOTAL TERMINAL SALES	8	2373	9345	46.2	12.1
Data Transmission Equipment Shipments	19	560	980	25.3	4.8
TOTAL TERMINAL & EQUIP SHPTS	27	3461	11120	38.2	10.2

*communicating word processor

Sales of autotransaction terminals, which include teller machines, automated tellers, and retail electronic funds transfer and POS terminals, will grow from $995M in 1978 to over $2B in 1990. Automated teller machines (ATMs) will experience the fastest gains at over 7%/year. Twenty-five thousand ATMs will be used by financial institutions in 1990, up from 7,000 in 1978, and will relieve their human counterparts from 625 million transactions. Although anticipated declines in price will render ATMs more affordable, the basis for continued growth is competition among financial institutions. Since ATMs are a marketing tool used to extend service hours and thereby to increase or maintain market share, their ability to attract new business to an institution is primary justification for installation.

World's Smallest Experimental Circuit Elements

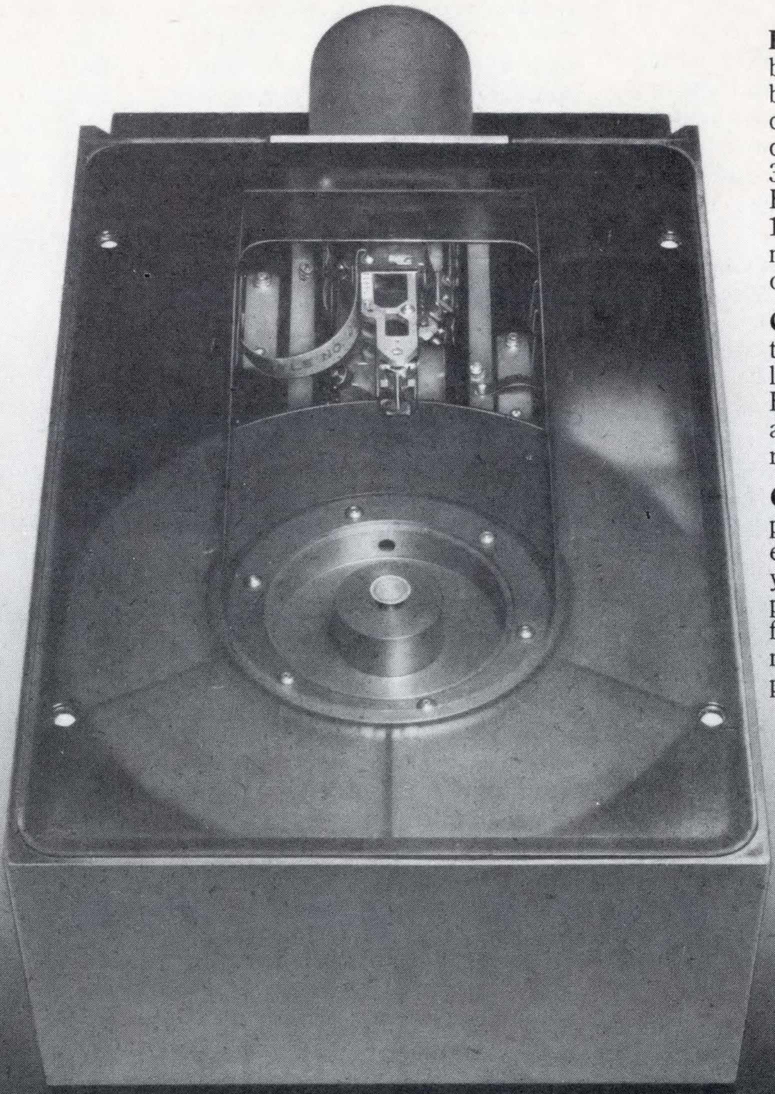


Scientists at the IBM Thomas J. Watson Research Center have controllably fabricated and systematically tested the smallest experimental electronic circuit elements ever reported. The devices have widths and thicknesses of only 100 to 200 atomic diameters – far smaller than human nerve fibers – and the research effort that produced and used them is significant in at least two regards.

First, it represents a successful application of recent advances in electron-beam lithography, a technology originally developed for producing large-scale integrated circuits. Scientific understanding made advances in the technology possible. That technology is now making possible further increases in scientific understanding.

Second, it shows that scientists can explore superconductivity in electronic circuit elements even in a size range al-

Introducing the new BASF 6170 Series 210mm Fixed Disk Drives.



High Performance. Perfect for multi-user multi-tasking applications, the BASF 6170 Series drives give you an average time-to-data of 50 milliseconds...four to seven times faster than standard 8″ floppy drives.

Capacity. The BASF Model 6171 provides 8 megabytes and the Model 6172 provides 24 megabytes of fully usable unformatted capacity. Unique BASF circuitry eliminates user mapping.

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Proven Reliability. BASF, because of its experience in both magnetic media and drives, is highly qualified to develop drives using reliable 3350 Winchester technology. BASF 6170 drives have a 10,000 hour MTBF and require no scheduled maintenance or operator intervention.

Compact Size. Far smaller than 14″ drives, the quiet, lightweight floppy-sized BASF 6170 drives are suitable for desktop office environments.

Competitive Price. Get the performance, capacity, and ease of system integration you need right now...at prices you'd expect to pay for far less sophisticated technology. Write now for competitive OEM prices.

If you need high performance, capacity, easy system integration, proven reliability, in a compact size, at a competitive price, right now...

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most 1/100 of that found in existing microcircuitry (greater than 1 μm, or a millionth of a meter). Superconductivity is a phenomenon in which certain metals and alloys lose all resistance to electricity at temperatures near absolute zero.

Called nanobridges, the devices feature thin-film stripes of superconducting niobium metal as little as 40 nm wide, 30 nm thick, and 120 nm long. The work is an outgrowth of IBM's recently achieved ability to produce fine metal lines only 8 nm wide. The narrowest niobium line made was only 25 nm wide. Previously, dimensions couldn't be controlled to this extent.

The superconducting circuit elements now being reported were found to exhibit what are known as Josephson effects. The narrow stripes function as constrictions or bridges between larger, micrometer-sized areas of superconducting niobium thin films. As such, the bridges are in effect "weak" superconductors, or as they are sometimes called, weak links.

In the Josephson effect, a sufficiently small weak link in a superconducting circuit can function as if it were a good superconductor by allowing a supercurrent of electron pairs to flow between connecting superconductors with no voltage difference across the link (dc Josephson effect). Further, when electromagnetic radiation such as at microwave frequencies is applied to a weak link, dc currents are formed at equally spaced voltage intervals (ac Josephson effect). What is learned from the nanobridge studies of superconductivity and the Josephson effects could be of benefit to Josephson technology research.

Foreign Intrigue And Satellite Spying Invade Silicon Gulch

Lying south of San Francisco and stretching between Stanford and San Jose lies an incredible phenomenon – Silicon Valley. It is the driving force behind our world dominancy in electronic and non-electronic markets. This modern wonder of the world far surpasses any assembly of high-technology companies in any other part of the world, and this region contains the world's largest congregation of semiconductor firms, research laboratories, universities and attendant service organizations in terms of concentration that is related to a single technology and industry.

It's said that New York is the "spy capital" of the nation in numbers; but the amount of Soviet espionage in Southern California's electronics, computer and aerospace industries "is frightening," says the head of the FBI's Los Angeles office.

Herbert Clough Jr. warned that Southern California is an espionage Mecca because "the goodies are here." Half of all classified government contracts are in Southern California – enough to tempt the Soviets, and now the PRC (Red Chinese). Although new FBI programs to alert electronics and computer firms to the dangers of espionage and theft of technology has begun, with the years of strangling of

Technology Trends

US intelligence capability, observers cynically question if the theft of high technology can be curtailed.

Using small hand transmitters, an estimated 50 Russian spies are making daily reports on Silicon Valley's latest breakthroughs – much of it secret or proprietary company information. What makes this massive electronics "theft ring" so incredible – other than the fact that they cannot be punished if caught! – is that their hand transmitters send report up to a Soviet satellite as it passes overhead. Obviously, if U.S. electronics firms or engineers tried to get away with this massive theft of technology, you can bet they wouldn't get off on diplomatic immunity.

Soviet spies, with only moderately sophisticated gear, can listen in on the communications of strategic missile and space firms and other companies. Furthermore, similar telephone spying was used by the Russians to get secret trade information that enabled them to pull off favorable wheat deals.

The Soviets can copy information with small-but-highly-directional microwave dishes, receiving the sidelobe electromagnetic energy of a straightline microwave transmission at a distance of 10 to 20 miles. Russian spies must first listen at random to thousands of conversations. Finally, when they detect a conversation being carried on a line leased by an important electronics firm, they monitor this and all other "dedicated phone lines" leased by the chosen target companies.

Although the Soviet consulate in San Francisco is not on a direct line with phone company microwave relays in the city, its upper floors are loaded with electronic gear.

How many individuals are involved? The FBI estimates that 50 KBG colonels are based in Silicon Valley. As for their San Francisco consulate, estimates pinpoint 35 percent of the Soviet personnel there as involved in industrial espionage.

Will the Peoples Republic of China (PRC or Red China) establish diplomatic spies, i.e., the equivalent of the U.S.-based Soviet KGB espionage staff? Perhaps. However, this may not be so necessary, since the U.S., it appears, is about to make an all-out effort to supply the PRC with massive technological assistance and information. The IEEE will, it seems, play a key role in transferring U.S. computer and electronics technology to the PRC. Former IEEE president, Jerome Suran and General Manager Eric Herz, in a recent trip to the Far EAst, discussed the possibility of opening up an IEEE section on the Chinese mainland admitting PRC EEs to the IEEE. The Chinese Institute of Electronics and its president, Lin Yin, said they also wanted translation right to IEEE publications. As reported in an IEEE newspaper, "The Institute" (Dec. 1979, pg. 4); "Interest was intense throughout Region 10 to get mainland China into the IEEE fold, Mr. Suran reported, adding: 'The Hong Kong Section could assist the formation of a new section in mainland China.' Mr. Suran met in Hong Kong with leaders of that IEEE section to discuss a possible role.

No time was agreed upon for a decision on the mainland Chinese section, but Mr. Liu and several representatives are to meet with IEEE leaders in New York during their current month-long visit to the U.S.

Technology Trends

From our recent discussions of this matter with an IEEE official, the attitude conveyed was that the IEEE is enthusiastic about giving away hard-earned U.S. electronics and computer technology to the PRC. When asked about whether this could antagonize the Soviets, or eventually create an economic (due to low wages) or even military threat, the IEEE spokesman shrugged it off. From his insight into the matter and his apparent enthusiasm for this upcoming U.S. technology transfer, we suspect something is upcoming. But, we seriously doubt if the IEEE would independently take such unilateral action; and, no doubt, some higher organizations gave them the go-ahead.

PRC's armed forces number 4.3 million – by far the largest war machine in the world, with a 115-division army and 4700 combat aircraft. Can anyone doubt that the massive U.S. transfer of electronics and computer technology won't be used to improve this war machine's effectiveness and increase the chances of it being used against neighboring nations like India, Africa, Japan, Pakistan or Afghanistan?

We believe in the transfer of technology to nations that have historically shown a responsible use of it. But, is giving away technology to those who would sooner or later misuse it wise? Is IEEE's explorative intentions to admit mainland Chinese engineers to its membership a responsible action? Or is this planting the seeds of World War III?

Do you agree? Or disagree? Or half-disagree? If so, or if you have other points of view, please write us. We welcome your letters and comments.

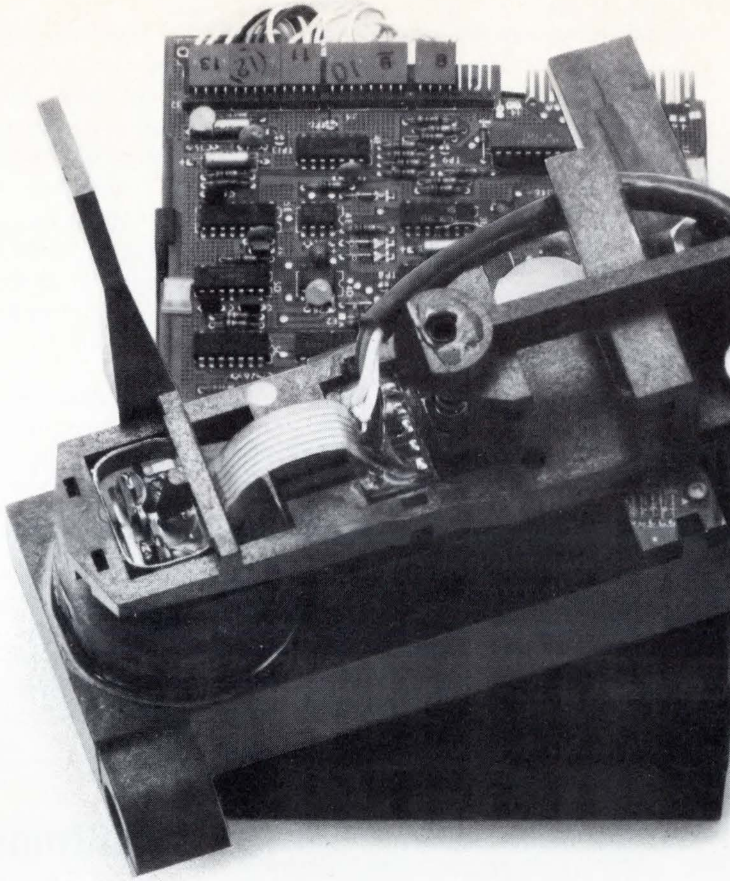
R&D Theft Requires New Countermeasures

"The exploitation and theft of company secrets by employees engaged in R&D is increasing at an alarming rate," declared Norman Jaspan, noted author and president of the New York based international management engineering firm bearing his name, before the Electronic Industries Association. It threatens the industry's investment in new technology and products, which are fundamental for improving productivity and controlling inflation.

More than one-third of the profits of most businesses are poured back into R/D. The stakes are so high that some of the most respected professionals in our society – the engineers, the chemists, the metallurgists, the professors – are too often willing to compromise their ethics for quick financial gain. "The temptation to steal ideas, formulae, designs or blueprints are sometimes overwhelming," Jaspan continued.

Unethical researchers can also obstruct, sabotage, or delay the development of new processes and products until they can exploit this material to their own advantage – in a better job; perhaps an opportunity to go into business for themselves; or for outright sale to others. They are no longer merely content with professional recognition.

The rapid increase of mergers and acquisitions in the electronics field has



Tandon Drives. Heads above the Rest

For years, Tandon Corporation has been designing and manufacturing read/write heads for most major flexible disk drive manufacturers. Their heads are currently in over 1,000,000 field operable units, and deliver a standard of reliability that is positively unmatched.

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compounded the problem of dishonesty in the industry. The decentralization of operations, computerization and the displacement of owner-managers has had a profound effect on employees.

Mergers amd acquisitions, entered into to increase sales and profits, and mass layoffs, may in fact, foster disloyalty and frustrations due to insecurity and unfulfilled expectations. These feelings are reinforced when conglomerates and other companies accelerate the liquidation of marginal operations. Although EEs are generally more loyal than blue-collar workers, or even executives, kickbacks, ventures involving conflicts of interest, and outright theft can become irresistible.

The latest studies by the Joint Committee of Congress and the U.S. Chamber of Commerce revealed that the overall cost of employee dishonesty is in excess of $44 billion/year. The malpractices that receive the least attention are those committed by trusted employees. Their opportunities are great, their methods less subject to scrutiny, and they are the last to be suspected. Data processing personnel and programmers are most likely to engage in computer crime (see Senator Abraham Ribicoff's "Will Computer Crime Slow Computer Growth?" in the August *Digital Design*).

"Policy statements regarding conflicts of interest, kickbacks, price fixing and the integrity of books and records are not enough. They must be supplemented by effective investigative audits that convert insight into convincing fact," Jaspan declared. Opportunists often find it easy to bypass conventional accounting controls. When kickbacks, theft of company secrets, destruction of records, manipulations or embezzlement are suspected, unusual skills are necessary. Business expertise, skills in interviewing and the application of behavioral sciences in a confidential and sensitive manner are essential, the consultant asserted.

Recent court decisions have held directors, chief executives and other professionals responsible not for what they did *but for what they failed to know*. They are also being held responsible for failure to exercise greater iniative and due diligence in pursuing dishonesty.

Many employees know about such abuses but do nothing about them. They emotionally withdraw from a distasteful situation that may involve friends or associates or they are afraid of being found at fault and criticized.

"The need to know what is really going on," said Jaspan, "is highlighted when our management engineers undertake investigative audits, systems surveys and inventory control projects. In more than half of these cases, sizeable losses have been uncovered. Millions of dollars have been recovered annually."

Efforts to protect scientific innovations, trade secrets and confidential information need to be thoroughly reviewed and sensibly strengthened. Will uniformed guards, locked filing cases, alarm systems, and other physical devices help? They are necessary but inadequate. More sophisticated management approaches are necessary.

Non-Impact Printer Growth Accelerates

World wide shipments of non-impact printers and page printers will reach 33,600 units in 1983, achieving a compound annual growth rate of nearly 28%. During the same forecast period, sales of non-impact serial printers will see a somewhat slower unit growth rate of 22%, according to the results of a four-volume multiclient study on the computer printer industry recently released by Creative Strategies International, a San Jose, California-based market research firm.

Within the non-impact line and page printer market, ultra high-speed printers will be the most dynamic segment and will account for the largest dollar value. By 1984, revenues from this segment will attain a growth rate of 32.8%, compounded annually.

High-speed page printer usage is clearly increasing but is not replacing as many impact printers as might be expected. The extensive end-user survey conducted by Creative Strategies shows that the total cost of the printer and related supplies is a very significant concern.

Xerographic technology will dominate high-speed non-impact page printers and line printers in the near future. Further product developments will results in page printers with higher throughput at lower end-user prices.

Software
DESIGN SERIES

Dr. Lance A. Leventhal
Emulative Systems Co.
San Diego, CA

Program Optimization: A Waste of Time?

When microporcessors were first introduced, articles and design on program optimization described in great detail how to save a few bytes of memory or a few microseconds of execution time. In some applications, memory and execution time were at a premium, since the first micros were slow and memories were both small and expensive. Also, this attention came from EEs' fascination with the intricacies of this new toy, plus EEs' failure to understand lessons learned earlier with larger computers.

Have things changed? Definitely, but perhaps not fast enough. Let's look at the costs and benefits of faster and shorter programs, describe some typical applications requiring program optimization, and show how to optimize μC programs in a systematic manner.

Costs vs. benefits. . .

You can always shorten programs and make them faster. Clever programmers always find ingenious (or devious) methods that save time, memory or both. However, do such optimization benefits exceed costs? Although tradeoffs vary with application, let's look more closely at the benefits and costs.

First, what are the benefits of faster program execution? Four major benefits exist. (1) The program may **meet critical real-time requirements**; in such cases, optimization may be essential to make the program work at all. Real-time requirements are most common in process control, industrial control, military/aerospace applications and communications. (2) You may **use more accurate (and more complex) methods.** Such alternatives often exist in signal processing, auto matic control, communications and simulation. You can always extend transforms, optimal control algorithms, detection methods and mathematical models to include more or higher-order terms. (3) The system can **process more data**, often possible in computing applications in which more data can readily be made available. (4) The system may **require less hardware**, because the program may be able to assume tasks that would otherwise require additional parts.

Saving memory

The benefits of saving memory are fivefold.

(1) The system may require **fewer memory chips.** Of course, optimization only produces a real savings if the reduction is sufficiently large or the memory chips are small. Relatively small chips are often all that's available for applications requiring extremely high performance, low power consumption or high environmental tolerance.

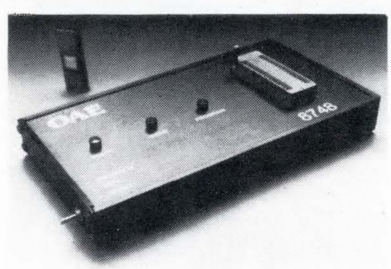

Fig 1 The 8748 single-chip microcomputer includes 1K bytes of EPROM, 64 bytes of RAM, and 27 I/O lines from Intel Corp., Santa Clara, CA.

(2) The program may **fit within a one- or two-chip μC.** Costs may be greatly reduced if a program can fit in the on-board memory available on a one- or two-chip system (such as the Intel 8048 or the Mostek 3870). The system is also easier to package, handle or change. For example, the Oliver Advanced Engineering 8748 EPROM Computer Programmer **(Fig 1)** can quickly and easily revise, customize or correct entire systems based on the 8748.

(3) The system may **fit on a single board or card.** Popular boards or cards (such as Wintek's Wince control module) are immediately available at low cost, if the user can keep a system within the limits of the on-board ROM, RAM and I/O.

(4) You can **add new capabilities at minimal cost.** Even if no chips are saved, the extra program memory can enhance the product at little or no per-unit cost. This enhancement can improve a product's marketability in competitive applications such as calculators or small terminals.

(5) **Room for other programs or data** may exist. Extra room is often important in dp applications, where a few large programs (such as operating systems or compilers) may occupy large amounts of user memory.

But added costs exist. . .

On the other hand, four added costs are involved in making programs run faster or use less memory.

(1) **Additional programming time** required may be the single largest development cost in many applications. Costs will worsen as programming time grows more expensive in the near/long-term do to inflation and a shortage of trained engineers/programmers.

(2) **Additional development time** is needed. Trying to make a program shorter or faster increases development time and associated costs. Early introduction of a product such as Foxboro's Spectrum line of μP-based control systems may be far more important than a minor cost sav-

ings per unit.

(3) The **programs are more difficult to maintain.** The changes required to make a program shorter or faster often make it more complex and more difficult to understand; also, a documentation problem occurs when programs are changed frequently.

(4) **More testing** is necessary to ensure that revised program versions are functionally equivalent to the initial working version.

Are the benefits we mentioned worth the costs? The answer depends upon your application.

Computational applications require optimization

Faster execution is typical of applications that perform a large amount of computation in a limited amount of time. For example, control or signal processing applications fall into this category because their execution time more often depends on program speed than on data availability or peripheral device speeds. If the system can perform extra computations, you can make the algorithms more accurate, use more feedback loops and provide greater precision.

Typical applications that require **reductions in memory usage** include small instruments, calculators and peripherals that often involve one or two-chip μCs. A small overrun may substantially raise costs or even exceed the micro's capacity. The need to save memory is less critical in larger applications, particularly as memory costs drop and increased memory becomes available in larger single-chip micros.

Most applications fall into neither of the above categories. Most instruments, test systems, communications equipment, business equipment, computer peripherals and consumer products do not require real-time operation, do not employ complex algorithms, and do not possess the high-volume and low-processing power of the one- or two-chip micros. In most micro applications, the program spends most of its time waiting for something to happen; that is, it is I/O-bound – not "compute-bound." Since a micro gains nothing by spending a large percentage of its time waiting, you should simply produce a working program as fast as possible. Why improve time and memory usage? It's a useless frill that costs extra.

Seldom can you justify spending additional development time to optimize programs for low-volume applications. Designers with such applications are generally better off using a system such as the Dynabyte Basic Controller; such a system requires extra memory (for the Basic interpreter) and extra time, since it must translate the Basic program. But it greatly reduces programming time, since Dynabyte's industrial Basic version is easy to learn and use and provides I/O, bit manipulation, communications capability, mathematical functions and special constructs for control applications. The controller may also eliminate the need for an expensive development system.

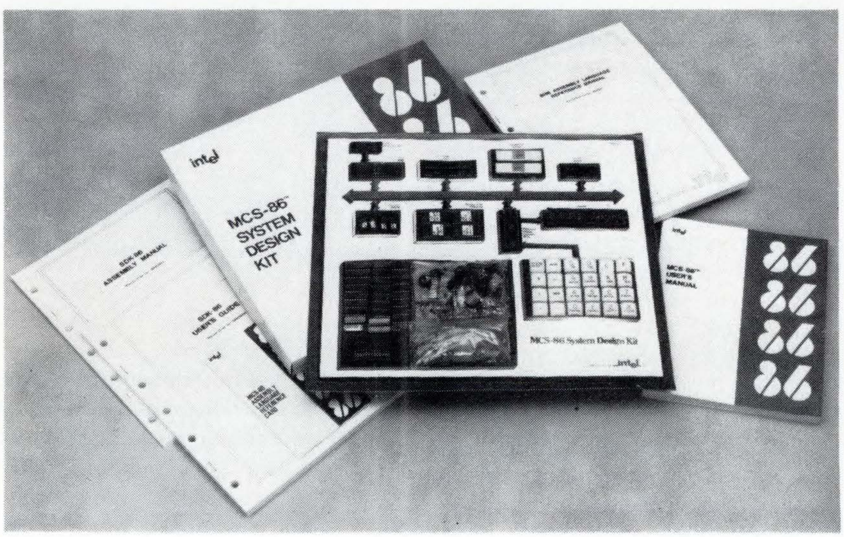

Fig 2 For greater speed/lower memory usage, a new micro may be needed, such as the Z8000, 68000 or 8086. This system design kit is based on the Intel 8086.

Making programs run faster

To make your programs run faster. (1) identify the most frequently executed loops and optimize them, (2) use methods, such as lookup tables, that require fewer instructions and (3) add more hardware to the system.

The first approach requires you to determine which program parts are executed most frequently; savings in these parts can multiply the effect many times over. You can perform this analysis manually or with the aid of monitor programs that are available on some development systems. The key point here is to go where the action is; changing instructions that are only being executed once or a few times is a waste of effort. The programmer must concentrate on sequences that are being executed millions or hundreds of millions of times in each program iteration.

Once you've identified the key program parts, you should: (1) simplify the processing in inner loops by preprocessing data, removing special cases and simplifying operations and (2) use special features of a particular computer, such as special instructions, faster addressing modes, registers and flags (**Ref 1**). This approach may often lead to documentation problems, since the special features are usually non-standard and are difficult to understand. They may also be used in ways that are unusual and not what you (or the original manufacturer) would expect.

Lookup tables are typical of approaches that save time at the cost of extra memory. A lookup table can replace any function; accessing the table runs much faster than calculating all but the simplest functions. Lookup tables also save programming time, since the table lookup procedure is usually quite simple; and the same for any function. Lookup tables can perform all the conversions, linearizations and other procedures required in an application (such as the Electro Scientific Industries automatic digital LRC meter). The problems are that tables may occupy an excessive amount of memory and be difficult to understand because no calculations are performed explicitly. This approach is really a special case of adding hardware, since the operations are really being performed in a ROM rather than by

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a sequence of instructions.

Many different kinds of hardware can also speed program execution; the most common types include: floating point arithmetic units (such as the Advanced Micro Devices 9511); multipliers, such as the TRW MPY series (**Ref 2**), custom or standard ROMs, such as code converters, character generators, sine and cosine lookup tables; programmable I/O devices, such as interrupt, DMA, peripheral and communications controllers; and SSI or MSI logic elements, such as encoders, decoders, multiplexers, selectors, arithmetic-logic units and parity generators. Even relatively slow hardware, (calculator chips, UARTs, and USARTs) may actually increase program speed by removing some CPU burden.

Some techniques we described for saving execution time also save memory. In particular, many micros provide special capabilities, such as interrupts, trap instructions, extra registers and unused flags that can save both time and memory. Additional hardware can often save memory as well as time, though it increases total system cost.

What is perhaps the simplest way to save memory? Eliminate repetitive code. Make such code into subroutines that are called at the appropriate places. The repeated sequences must be long enough so that the extra instructions required to transfer program control back and forth do not consume most of the savings. Your job is to identify the repetitive sequences. In all the techniques that we have mentioned, a large number of subroutines can lead to documentation and maintenance problems. Each subroutine requires separate documentation and frequent transfers of control make programs difficult to understand or maintain.

Will the techniques that we've described create enormous gains? Not likely. But if you need to increase speed or reduce memory usage by 20 or 30%, they can do it; on the other hand, if you need to improve speed or reduce memory usage by a factor of 10 or 10,000, these methods are not too helpful. Instead you need a major change such as using: (1) a different CPU with a longer word or a higher clock rate; and one of the new generation of CPUs (such as the Intel 8086 (**Fig 2**)) may be necessary particularly if the application involves many arithmetic calculations (**Ref 3**), (2) a microprogrammed emulation of the CPU in the existing system; such emulations are most often available for the 8080 or 6800 processors, but are quite expensive and time consuming to use; (3) two or more CPUs working in parallel; and/or (4) a new algorithm, particularly if the task involves sorting, searching or mathematics (**Refs 4-6**). When major surgery is required, cosmetic changes will not do.

Most μP applications do not require optimization of memory usage or execution time. But the ones that do usually involve large amounts of computation, real-time constraints or one- or two-chip μCs. Typical ways to make programs run faster use simplified frequently executed loops, take advantage of special computer capabilities, employ look-up tables and add more hardware. Typical ways to reduce memory usage: replace repetitive code with subroutines, eliminate lookup tables and other memory intensive operations, and optimize programs at the assembly or machine language level. These methods provide some savings, but, they cannot produce enormous gains.

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Determining The Spatial Resolution Required For Real-Time Graphic Displays

Dr. Harry C. Andrews
Vice President and Director of Marketing
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Specifying the spatial resolution of real time displays used for viewing digital imagery can be difficult. Unfortunately, the display industry has also evolved a set of specifications which are often confusing and difficult to relate to when attempting to display digital pictures. In addition, the relatively poor imagery available through commercial television systems (due to low signal-to-noise ratios) has created an underlying prejudice against systems of 525 lines or less resolution.

Video bandwidth specifications, coupled with low-resolution vidicon and shrinking raster tests, are inadequate to describe display systems. Also, graphics monitors, as well as facsimile, battlefield, cockpit, and simulator displays, require particular characteristics that are not necessarily appropriate for the real time display of digital imagery.

How, then, can you decide which characteristics are necessary to define a system of reasonable resolution without sifting through conflicting specifications? Unfortunately, there is no single answer. However, to alleviate the problems when working with digital data, you can adopt computer and digital rather than analog monitor specifications.

The following example should make the importance of digital specifications self-evident. If you wish to display a monochrome image with 1024 x 1024 pixels and 8 bits of brightness (256 grey shades) per pixel, the system must transmit 8×10^6 bits to the monitor 30 times per second to avoid flicker. This requirement implies a $(8 \times 10^6) \times (30) = 240$ megabits per second data transfer rate. In a raster scan system, each pixel should settle to its true value before switching to the next pixel value. Therefore, a 40MHz bandwidth requirement, including horizontal and vertical retrace times as well as pixel settling times, is not too conservative.

More OEMs and end users are looking at color graphic display terminals.

A 2048 x 2048 display system would seem to require 4 times the digital memory and multiplexing costs of a 1024 X 1024 display system. However, a performance degradation of a simple factor of two in horizontal and vertical resolution can quadruple the price of a 2048 X 2048 system with no apparent improvement in display quality. Thus, you must correctly specify resolution when configurating digital image processing facilities.

Let's examine a system from an economic viewpoint. Any system with smaller high-speed refresh memory and display resolution, but designed around a user scenario in which zooming, interpolation, magnification, minification, panning, rolling, are provided by an interactive facility which may be equal to or more powerful than a higher resolution system.

Sensors and dynamic range

As a rule, digitally-processed images are more carefully sensed than a simple stop-framing of a television signal can produce. In addition, the digital refresh of a display at television rates provides a far superior signal-to-noise ratio than traditional commercial analog systems. Consequently, it is useful to reexamine the need for traditional 525-line displays for digital image processing.

Sensor technology can now sense arrays for optical energy at dynamic ranges far exceeding traditional vidicon and film devices. Photomultiplier systems, laser scanners, rectilinear diode scanners and arrays, CCD arrays and microdensitometers – all provide potentially low-noise, large-SNR sources of data for subsequent digital processing purposes. Even low dynamic range imagery on film offers good noise properties, if scanned at high SNRs. In fact, the system should acquire its data signals at the best SNR possible, no matter what the dynamic range of the medium being sensed is, because subsequently applied digital techniques are powerful enough to examine the slightest defects in such pictures. It is possible to sense imagery with signal-to-noise ratios of 64:1 – even 1024.1 – and requiring 6, 8 or 10 bits of brightness (z-axis intensity dynamic range).

With such sources of data for image processing, we can instructively examine the digital refresh rate generated by 6 or more bits of dynamic range. Both shadowmask (for color) and conventional high-resolution industrial-grade CRT monitors operate at digital refresh rates of up to 240 Mbps. Such refresh systems are completely digital up to the DACs at the guns of the CRT. In addition, sweep circuitry is digital for horizontal and vertical signals. The resulting stability in the x, y and brightness axes of such systems provides a remarkably high signal-to-noise ratio output display

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device. No matter how much noise existed in the original image prior to digitization, once it is digitized, the signal and noise become a deterministic process.

This deterministic plane of data is then reproduced on the digital refresh monitor with a spatial stability of 8, 9 or 10 bits, depending on whether you select a 256 x 256, 512 x 512 or 1024 x 1024 array format. The z-axis brightness SNR and stability are reproduced to within one point in 64 or 256, depending on whether the data is displayed at 6 or 8 bits of brightness.

Once even a terribly noisy continuous-tone image is digitized, it is stabilized in the x, y and z axes and the randomness of analog display systems is eliminated. For this reason, you may wish to reevaluate the usefulness of low-resolution (256 x 256) versus intermediate (512 x 512) and high-resolution (1024 x 1024) monitors. The stability of a 256 x 256 x 6-bit digitally refreshed display may appear, in fact, as good in quality as 525-line analog commercial television systems. At the other extreme 1024 x 1024 x 8-bit digitally refreshed system can provide quality that appears far superior to four times the quality of commercial television.

Spatial Resolution

It is as difficult to get a true measure of spatial resolution as it is to get consistent specifications from manufacturers throughout the display industry. Most vendors interpret differently such quantitative definitions as cycles per linear distance (c/mm), line pairs per millimeter, modulation transfer functions and curves, cut-off frequencies. Linearity across the monitor, depth of modulation, 3dB down measurements, horizontal bandwidth, and other quantitative specifications suffer from drawbacks as true specification aids.

Coupled with these inadequacies are psychovisual responses of the human vision system. Here such properties as Mach banding, simultaneous contrast, Weber's law, viewing angle and distance, visual acuity factor, surrounding illumination and minimal detectable resolutions contribute to psychological resolution considerations which may not correlate with quantitative definitions.

Fortunately, we can minimize some of these spatial resolution considerations in the area of digitally refreshed displays. One technique to verify spatial resolution uses computer-generated test patterns. They are noise-free (in digital form) and can generate valid measurements on the display monitors. The technique can modulate adjacent pixels in x and y directions to within from one up to 64 or 256 parts in 64 or 256 different brightnesses. Visually detecting such modulations may be enough for certain applications.

Spot photometers and radiometers can generate other measurements of a more quantitative nature from the monitor. You can quantitatively test z-axis brightness linearity by placing computer-generated grey scales in the image. Finally, spatially-variant measurements can get away from the restrictive space-invariant assumptions implicit in single MTF measurements or on-axis resolution bandwidth specifications.

Interpolation

Proper interpolation of image data can considerably improve displayed pictures over what you might originally expect. Two simple-to-use interpolation techniques consist of two-dimensional replication and bilinear interpolation. Replication simply repeats pixel values to fill up the display plan without regard to continuity. Bilinear interpolation provides interpolated brightness values between pixel data points. The interpolation is linear in both dimensions and guarantees continuity of the displayed data.

Replication and bilinear interpolation are subsets of a family of interpolation functions known as B-splines. The higher-order, two-dimensional B-splines guarantee continuity in higher-order derivatives of the displayed results. Consequently a cubic B-spline provides continuity in the interpolated image in the zeroth, first and second derivatives.

Replication requires storage of only a single pixel, whereas bilinear interpolation requires storage of four neighboring pixels for interpixel definition. Consequently it is conceivable that real-time circuitry could be made available to display lower-resolution data at higher-resolution interpolated results.

Each interpolation technique has its pros and cons. Replication produces sharper images which, for small magnification factors, provide a false sense of high frequency due to artificial block edges. Bilinear interpolation provides continuity in the image display; for large magnification factors, it avoids blockiness of replication techniques. Thus, zooming applications may more meaningfully use bilinear techniques.

Examples

Let's examine the different interpolation techniques for two different illustrated images. The illustrations present different zoomed images at various magnification factors (1x, 2x, 4x) on the new COMTAL Vision One/20. All images were photographed at a fixed distance from the processing station and each represents magnification via replication. These illustrations clearly indicate that replication at 4x becomes a visual limit before blockiness becomes objectional. All images are displayed with 512 x 512 pixels on the monitor.

The Vision One/20 is a dual ported RAM refresh memory system which affords multiple user access to a common expandable data base (4096 X 4096 X 8 bit pixel memory images are available) with dynamic partitioning to afford a multiplicity of different applications. Real-time roaming with a window size of up to 1024 X 1024 pixels through the data base is possible with zooming and 3 X 3 convolution all implementable in 1/30 second. With graphics overlay memories; annotation, labeling, outlining and arbitrarily shaped multiple small area monochrome or color correction are possible. Due to the dynamic allocation of the data base memory, digital loop movies in real-time are possible as is left-right, right-left, up-down or down-up scrolling of new imagery into the refresh memory and viewing window. These and other features are expanded upon herein. Pipeline processors, freeze frame iterative image array feedback, firmware-burned control and instruction commands are descriptive of modern image processing architectures used in the Vision One/20.

Currently, the state of the art of digital refresh black and white as well as color displays seem to be hovering between 512 X 512 X 8 (X3 for color) and 1024 X 1024 X 8 (X3 for color) bits presented to the viewer 30 frames per second. It appears that constraints due to flicker and horizontal amplifier bandwidths will probably not provide significant breakthroughs above such resolution in the near future. Yet high speed RAM memories and clever architectures in the Vision One/20 now allow the user to roam and zoom within far higher resolution digital images at TV refresh rates thereby permitting potential exploitation of a tremendous amount of data in "real time." (Here "real time" refers to the rate at which a human would want to change his scene of observation, it not being expected that he would wish to change it at a rate greater than 30 times/sec.)

Probably the most significant single aspect of the Vision One/20 is that of new architecture designs. The multiplexing of data channels, the pipelining of processors, the availability of high speed RAM refresh memory chips, the perfection of very high resolution color shadow mask and monochrome monitors all have combined to allow the development of this highly interactive image processing exploitation station. With RAM refresh, it now becomes possible to roam around a larger data base memory at will, as well as scrolling, and zooming in a simultaneous interactive environment. Again coupled with table look up monochromes and pseudocolor function memories, as well as the ability to partition a large 8 bit deep monochrome memory into 1/3 the size 24 bit deep true color memory, one obtains a truly interactive "digital light table" exploitation system. In addition to the breakthroughs provided by larger, cheaper, and random access memories, pipeline processing technology has also contributed to modern day image processing stations. Typical 3 X 3 arbitrary convolution filters followed by both linear and nonlinear function memory combinations can process a 512 X 512 X 8 monochrome image in 1/30 of a second (equivalent to a TV time frame).

The refresh memory is comprised of 512 X 512 X 1 bit planes cycling at 800 nanoseconds per bit or spatial position. Four such planes are packaged on a card four deep providing one million bits of 16K RAM or one half of an image plane. A full 512 X 512 X 8 monochrome image requires two cards. Such a configuration defines an image plane, sixty-four of which represent a 4096 X 4096 image in refresh at one time.

Conclusion

An alternative means of evaluating resolution requirements for real-time digital image processing display systems exists. The advantages of digital systems lie in the potential for large dynamic range and SNR (brightness) displays, as well as extreme stability in the spatial positioning and resolution of the output imagery. For such systems, we have presented 256 x 256, 512 x 512, and 1024 x 1024 resolution displays for a common test image. There is increasing visual satisfaction in each of the three different resolution displays (thereby demonstrating that, for this experiment, you are not monitor limited).

While the higher resolution displays are impressive, we still should not ignore the 256 x 256 format, especially when considering cost, modularity, LSI techniques for construction, and those applications (X-ray and biomedical) where data sources are inherently lower-resolution anyway. Indeed, system costs make it difficult to envision applications in which you would need greater than 1024 x 1024 resolution, especially when coupled with an effective interactive scenario for panning, zooming, magnification for handling larger dimensional arrays.

For more on image interpolation algorithms, see "Digital Interpolation of Discrete Images", by H.C. Andrews and C.L. Patterson, IEEE Transactions On Computers, Volume C-25, No. 2, Page 196-202 (February 1976).

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Bank-Switchable Memory for LSI-11s

A Method To Improve System Capability

Mel Schwartz
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When the present mini generation was first on the drawing boards, it appeared no one needed over 32K words of "core" in such small systems. Steep RAM costs made it seem sensible to freeze the internal addressability of memory to 16 or 18 bits. But as the price of RAM fell, this architectural limitation became increasingly disturbing. Although the new generation of 16-bit μCs largely removed the addressability constraint, it still exists within the LSI-11 and PDP-11.

A simple technique for skirting this limitation, "bank-switching," is not a completely new idea; it's similar to "paging." Although it isn't a complete substitute for additional address lines on the internal bus, it goes a long way to solving the problem in numerous applications and is superior to disk simulators and other non-random semiconductor mass storage devices.

Bank-switching systems developed for LSI-11-based computers make use of three module types, each fully compatible with the DEC Q-bus. These modules are the RMA-032 (a 32K word RAM), RMS-016 (a 16K-word ROM) and BSC-256 (the bank-switch controller module).

How does bank-switching work? Imagine we have a total of 1024K words (2MB) in the system composed of an arbitrary mixture of RAM and ROM modules. This memory is logically subdivided into 256 blocks, each block containing 42 words. Now, because only 16 address bits are available, the memory space is normally limited to 28K words. (4KW are usually reserved for peripherals.) Think of this memory space as being divided into 7 sectors, each containing 4KW.

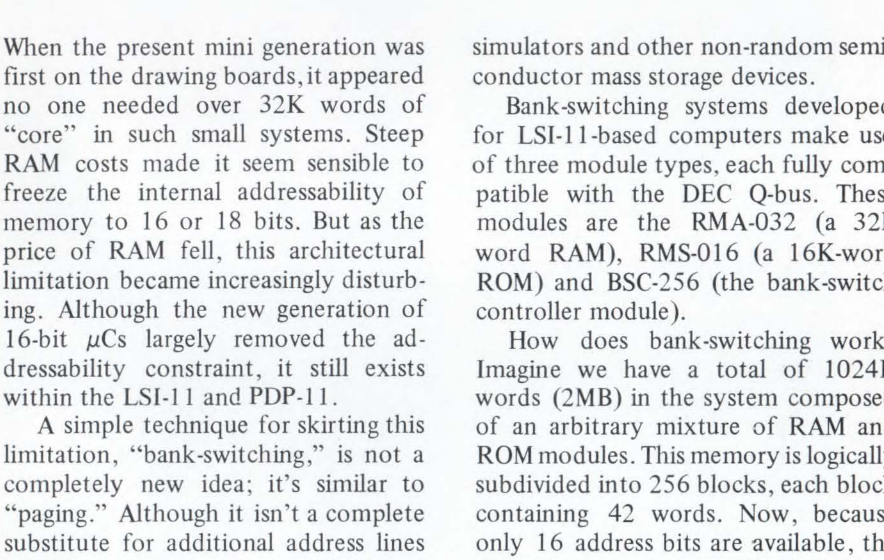

Fig 1 The three current members of the Digital Pathways bank-switchable memory family. From left to right, the RMS-016 ROM board, the BSC-256 Bank-Switch Controller, and the RMS-032 32K RAM board.

In conventional addressing, the assignment of *block* to *sector* is implemented in a permanent way. Indeed, each of the memory boards in the system, if used alone, can be operated in this mode. When bank-switching is implemented through use of the Bank Switch Controller (BSC-256), then the assignment of block to sector is made dynamically variable through a set of assignment registers in peripheral space. That is to say, any 7 of the 256 blocks can be assigned at any given time to any of the 7 sectors of memory space.

The actual mechanism of assignment is simple. The memory boards themselves when operated in this mode derive their addressing from two sources. The 13 least significant bits $A_{12} - A_0$ are taken directly from the back-plane Q-Bus. The 8 most significant bits which do the block selection are derived from an independent MEMBUS which originates at the BSC-256 and is daisy-chained to all the memory modules in the system. The MEMBUS address bits are derived from the three most significant Q-bus address bits A_{15}-A_{13} by means of a look-up table on the BSC-256. This look-up table is either a ROM or RAM depending upon a particular control bit; actual bank-switching is accomplished when the MEMBUS is under RAM control and assignment registers are overwritten.

Now that we understand the nature and procedure of bank-switching, let's explore its usefulness. As we said earlier, bank-switching is not a cure-all: if one has a 200K word program with frequent jumps from one part of memory to another, then one had best go

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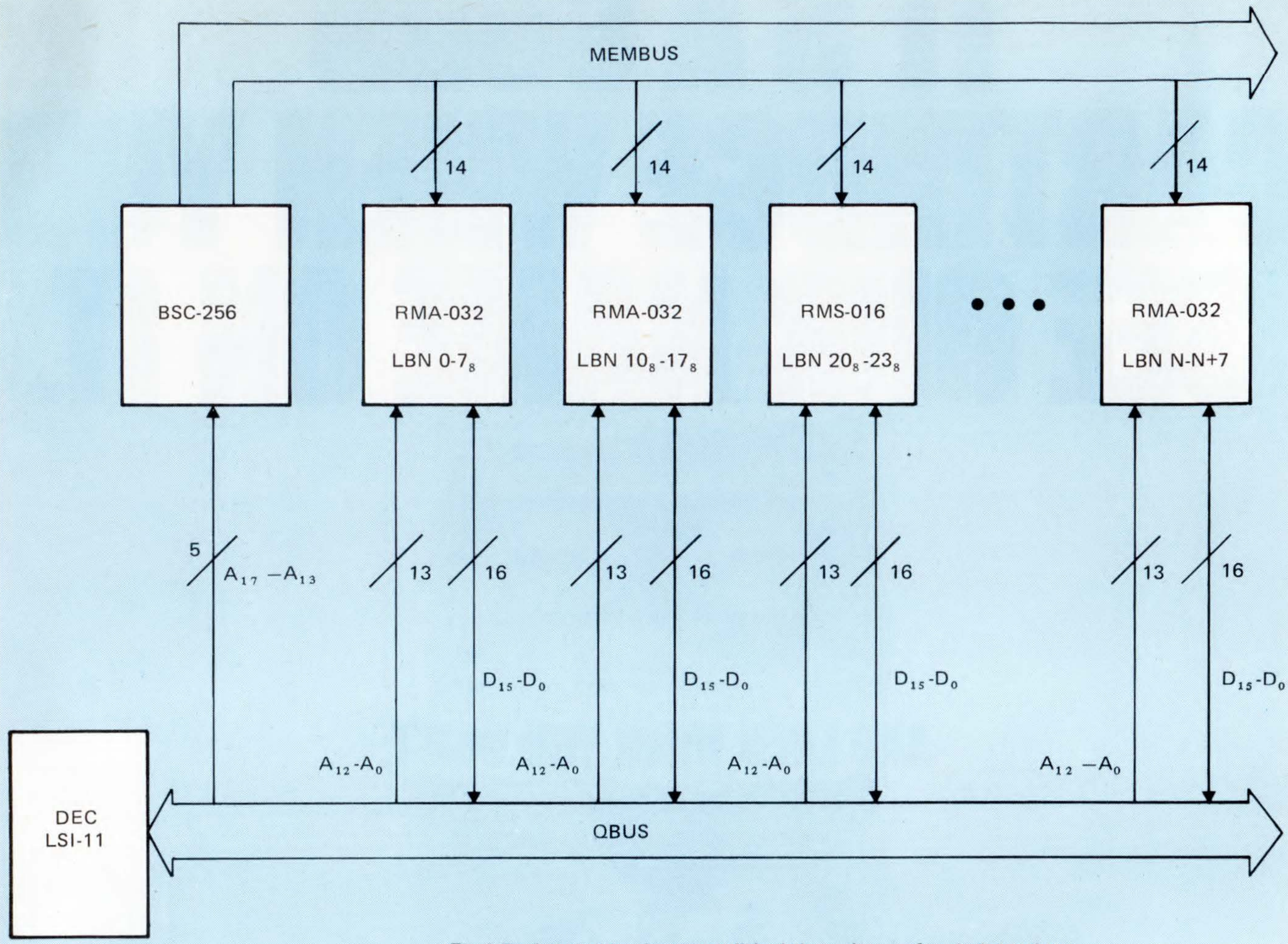

Fig 2 Bank-switching is accomplished through use of an independent 8-bit address code which is transmitted along the MEMBUS by the Bank-Switch Controller.

to another type of computer. But, in at least three broad areas that follow, bank-switching is an effective, if not an elegant, technique . . .

a. *Large numbers of independent programs of conventional size:* In this situation one would normally operate with a small amount of memory space (common block) permanently assigned and containing the linkages between routines in the various blocks. To call up a routine one would begin execution in the common block and then proceed to make the appropriate entries into the block assignment registers (after storing their current contents on the stack). This would switch the appropriate routine into the memory space and a simple jump will begin execution. To exit from the routine one must simply restore the original values to the block assignment registers and then return in the conventional way.

b. *Manipulation of large data bases:* There are numerous situations where it's desirable to manipulate large data bases with extreme rapidity and flexibility. For example, consider the processing of a pictorial image. A reasonable high resolution picture might consist of an array of 512 by 512 pixels each with up to 16 bits of gray scale data. The total amount of storage here is then 256K words. To store this image on a disc and carry out extensive overlaying is terribly time consuming. Using bank-switching, the task becomes essentially trivial. The entire operation is carried out at full memory speed with no need for memory to memory transfers other than those directly involved in the manipulation.

c. *Look-up tables:* Inexpensive memory and bank-switching make it possible to build extensive look-up tables to facilitate high-speed mathematical computation. Values of complicated mathematical functions at large numbers of arguments can be set into ROM and called up virtually instantaneously, when needed. This capability adds orders of magnitude improvement in the ease of computation in small systems.

To summarize, it appears that adding bank-switching capability to conventional memory does allow a very significant improvement in system capability within a number of rather important areas. At the very least, it speeds up operations requiring extensive overlaying from disks; at the very most, it adds a completely new dimension to rapid dp on minis with the limits determined only by the programmer's imagination.

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New Trends In Computer Printers

Engineering Staff Report
Printronix, Inc., Irvine, CA

Improved mechanisms and higher frequencies will mean better and quieter devices

To understand where the printer market is going in the early 1980s, it's first necessary to know where it's been. Under market pressure for lower-cost printers and technological opportunity offered by low-cost intelligence, the computer industry is moving toward matrix printers which put more complexity in the electronics to simplify the mechanism. The first impact of these forces produced low-cost, low-speed matrix printers. "Market pressure and technological advance create Product Change" is a statement applicable to all industries at any time, but particularly appropriate to the computer printer industry.

The advent of the mini and μC made economically-possible small (but complete) data processing systems programmed for many specific applications. This concept, named "distributed processing", is the fastest-growing segment of the computer business. Recent surveys placed the annual growth rate at 30% to 40% for this market segment. Frequently, the printer is the most expensive part of such small computer systems – creating real market pressure for low-cost, heavy-duty line printers in the 100 to 300 lpm range. Since most of these systems serve business applications that operate with multi-part forms such as invoices, purchase orders, and work orders, an essential requirement is the ability to print multi-part forms, for which impact printers are the only current satisfactory technology. Further, 132 columns and tractor feed are important, as well as the ability to operate in a wide variety of environments, not just the controlled environment of the large computer room.

Fifteen years ago it was not commercially feasible to make a semiconductor ROM capable of storing a 64 character set defined in a 9 x 7 matrix (about 4000 bits). Most ROMs at that time were "braided wire" magnetic core memories costing upward of 10¢/bit. Things have changed. But, it was this advance which added a new concept to impact line printers.

Increasing shift to intelligence

The major mechanical difference between matrix printers and conventional line printers is the absence of a drum or belt of type slugs. This is the primary reason for the fundamentally lower cost of matrix printers.

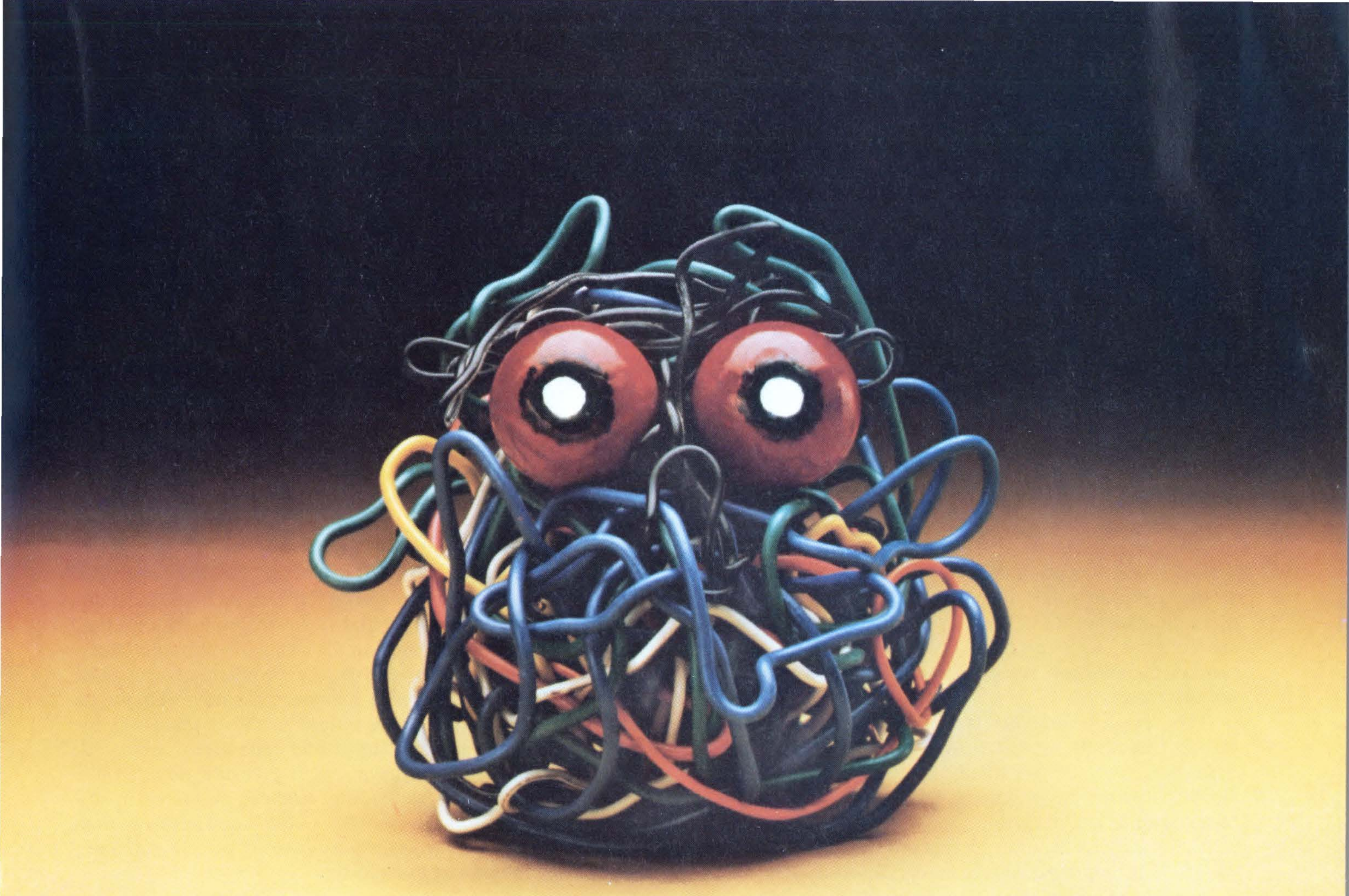
Further, in a conventional printer, to strike an "M" or "W" solid character requires 10 to 20 times the hammer pressure that a single dot requires. For this reason, in the matrix printer, the design of the hammer and hammer driver, to strike only dots, can be considerably simplified, again resulting in a lower cost system.

To print a single character, a drum or belt printer must sequentially present to each print position all 64 characters from which one is selected. With characters spaced at 0.1″, this means a total movement of 6″ or 7″ for each character selected. A matrix printer, however, with a single hammer, has only to move over all 35 separate dot positions to construct a single 5 x 7 (or 9 x 7, with half dot positions) matrix character. The dot separation is typically 0.015″, making a total distance moved of about 0.5″. For this reason the shuttle of a matrix printer moves at about one tenth the speed with which the surface of the drum or belt moves in a conventional printer. Smear and misregistration caused by this movement during hammer dwell time is the principal limitation on print quality of drum and belt printers – it is not a problem in matrix printers. To minimize misregistration, conventional printers have individual flight time controls on each hammer. The cost and complexity of these adjustments are avoided in matrix printers.

Matrix printing advantages

Matrix printing is capable of giving more precise registration, more uniform print density, quieter operation, and a larger character set than conventional printers. A fundamental difference between conventional printers and matrix printers is in the method of character selection. Matrix printers select by electronic random access where conventional printers select by sequential mechanical access. For this reason, a drum or chain printer will have to run slower if a character set larger than the basic 64 characters is required. With electronic random access there is no slowing of the matrix printer as the number of characters in the set is increased.

A matrix printer generates more impacts of much less energy than a conventional printer; these higher frequencies are more easily absorbed, making quieter printers possible.



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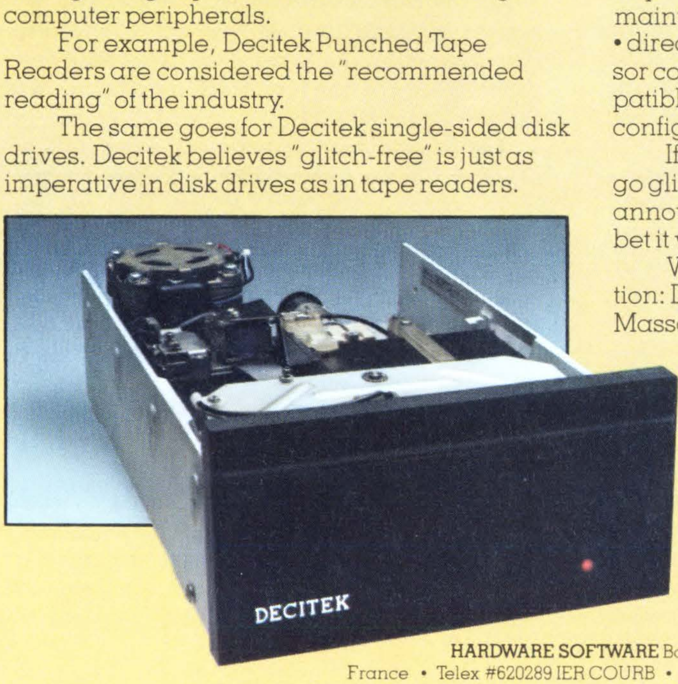

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With matrix printers, the paper is backed up by a solid platen which does not allow the paper to move at impact, in contrast to conventional line printers where the paper is held clear of the drum or chain, and is physically moved by the hammer to come in contact with the ribbon and character slug. This lateral sudden movement of the paper each time a character is printed propagates through the paper in all directions making a difficult noise suppression problem. Because of the solid backing of the platen, the matrix printer does not have this problem.

The full font printer is always faced by the problem of the widely different hammer energy needed to print an "M" relative to a period. The "M" is either printed too lightly, or the period is printed so heavily that the paper is embossed. Since a matrix printer forms each character out of a series of dots, the hammer energy can be optimized for printing only dots, and thereby giving uniform density of printing.

Choice of matrix

The first matrix printers used a 5 x 7 (5 horizontal, 7 vertical, 35 dots total) dot matrix because this was the minimum number of dots which would adequately present a character set. Although for many computer applications the character definition is not acceptable, some printers still use this matrix.

The next logical choice is a 7 x 9 (7 horizontal, 9 vertical, 63 dots total) dot matrix, with more attractive character definition, but has the disadvantage that almost twice as many dots have to be printed, and therefore the character takes twice as long to print.

The ingenious solution to this problem lay in the observation that improved character definition was as much a function of the flexibility of position with which dots could be placed as it is in the number of dots used. The 5 x 7 matrix was improved in flexibility by allowing the placement of dots horizontally in half-dot positions (there is also a rule that no two dots may occupy horizontally adjacent half-dot positions). Thus the 5 dot positions horizontally became 9 half-dot positions and the matrix became known as the 9 x 7 dot matrix, in contrast to the 7 x 9 matrix. The advantage is that more attractive characters can be constructed with the same number of dots as a 5 x 7 matrix, and the printer speed is not slowed. Most computer matrix printers today use the 9 x 7 dot matrix.

Two important additional steps improve the style of the characters to give it the appearance of a solid font. Because of this, it has been possible to overlap the dots in both the vertical and horizontal directions, causing vertical and horizontal lines to have a solid appearance.

Further, with the 9 x 7 matrix it is possible to make a steeper diagonal slope with the dots closer together. Careful design of the character using only the steeper diagonals produced print closely resembling a solid font printer. An example of this technique is the letter "K". The closer spacing of the dots creates steeper diagonals.

Categories

There are basically two types of matrix printers: those with a set of hammers arranged vertically, and those with a set of hammers arranged horizontally.

The Centronics printer is a good example of the first type of printer. It has a vertical row of hammers, mounted in a head which traverses the full width of the paper. The hammers are electromechanically actuated at each horizontal dot position, and when the full line is swept, the paper advances a full line spacing and the process repeats.

The Tally and Printronix printers are a different type of matrix printer, utilizing many more hammers and print at much faster speeds. These printers have the hammers arranged in a horizontal row, and the whole hammer assembly is moved a sufficient distance to create a complete horizontal dot row. The paper is then advanced one dot spacing. After the process has been repeated the requisite number of times, one complete row of characters has been created. Note that the Centronics type of printer generates characters sequentially, and is properly called a serial printer. The Tally and Printronix printers generate a complete line of print simultaneously, and are properly called line printers.

The Tally printer has 132 hammers moving in a single comb structure across 5 dot (9 half-dot) positions and in front of a fixed electromagnet assembly which retracts and then releases each hammer at each dot position.

Our printer differs substantially from the Tally in that it has 44 hammers moving across 18 dot positions, and the hammers are normally retracted by a permanent magnet assembly which is part of the moving hammer bank. The hammers do not have to be retracted at each dot position; they are already retracted and ready to print, making possible a faster printer. Moving the magnetic assembly along with the hammers also solves the problem of crosstalk, which limits the distance a hammer can move relative to a fixed magnetics assembly before it comes under the influence of an adjacent magnetic retraction circuit. A further value of this arrangement is that not only can full width characters be printed, but dots can be placed in any position on the page. In fact, a standard feature is Plot Mode, which allows individual dots to be programmed, thus using the printer as a plotter.

More specifically. . .

Let's look at a typical printer. The hammer is an individual, simple leaf spring. Swagged to it, at its center of percussion, is a hardened steel cylindrical tip. It is retracted about 0.020″ and has high potential energy. This energy is converted to kinetic energy by the time of impact, producing excellent print on six-part and NCR forms. It can be operated at a 1000 cycles/second rate.

The hammer completes a magnetic circuit which includes a ceramic permanent magnet. The pole pin against which the hammer is retracted carries a coil of wire. When current is passed through this coil it cancels the magnetic field and allows the hammer to fly forward and impact the paper. When current is removed the hammer is retracted by the permanent magnet.

The hammer bank is mounted on shafts running in linear bearings, allowing the assembly to sweep over three character positions (0.300″). A cam follower, spring loaded against a two lobe cam, makes two sweeps in each direction for each full revolution of the cam. A counter balance weight, running with its cam follower, moves with equal and opposite motion to cancel reactive forces caused by the hammer bank shuttling motion. The motion has a trapezoidal velocity waveform. While sweeping the print positions the assembly moves with constant velocity. While reversing the motion at the end of travel it moves with constant acceleration.

Driving the cam is a motor, with a flywheel to reduce speed variations caused by the varying motor load. Attached to the flywheel is a timing disk, with notches corresponding to every half-dot position. These notches are sensed magnetically, and the hammer circuits triggered at the appro-


Ontel

priate time. Due to the mechanical advantage through the cam, the physical separation of the notches is about ten times the half-dot separation. This makes magnetic sensing very simple and accurate.

The paper handling mechanism is particularly simple. A straight-through path was selected to ensure that even with heavy or multipart papers there would be no delaminating due to bending. Further, the tractors engage eight holes each, making possible the accurate handling of very light-weight papers, more common today. A digital stepping motor drive, close coupling of tractors to the platen, and a paper "ironing" device that holds the paper pressed against the platen at the print station, provide precise control of paper motion.

The ribbon drive is conventional, with a slanted ribbon path to utilize the maximum ribbon surface. Contacts woven into each end of the ribbon provide electrical contacts for ribbon reversing.

The electronics follow a conventional pattern. A full line of 132 characters of 7 bits each are received at a time, and stored in a recirculating shift register. For each dot positon as indicated by the signal from the timing disc, all 132 characters are presented to the PROM which contains the font matrix and a determination made as to whether a dot is required at each hammer position. This data is stored in 44 latches, and the hammers are fired on receipt of the signal from the timing wheel which indicates the hammers are correctly positioned. The logic is contained on two PC boards measuring 9″ by 11″. The 44 hammer drives and latches are also contained on a 9 x 11 PC board.

The design of the magnetic circuit, using a permanent magnet for retraction, renders the flight time insensitive to changes in firing current. The current simply creates a magnetic field in opposition to the permanent magnet at which time the hammer is released. For this reason, the hammer driver circuit can be very simple. It is a saturated Darlington switch directly driven from the logic.

Current developments in the semiconductor industry show a definite shift from ROM (read only memory) to PROM (programmable read only memory) due to several factors, but primarily due to the semiconductor manufacturers' reluctance to make short runs of custom parts. For this reason the font matrix information is stored in PROM. This has many advantages, allowing maximum flexibility for changes to satisfy customer needs, and even allowing customers to program their own fonts.

New trends

It has been said that there is no new technology for impact printing and that future advances will be made by improvement and cost reduction of existing designs. Not so. The printer industry is undergoing substantial changes due to the pressures of market requirements and technological advances in the semiconductor industry. The emergence of major new companies in the latter half of the 1970s (and which will continue throughout the 1980s) manufacturing low-speed printers using technology which did not exist ten years ago is proof. The matrix printer will continue to penetrate most segments of the printer market on the mid and low end of the applications spectrum.

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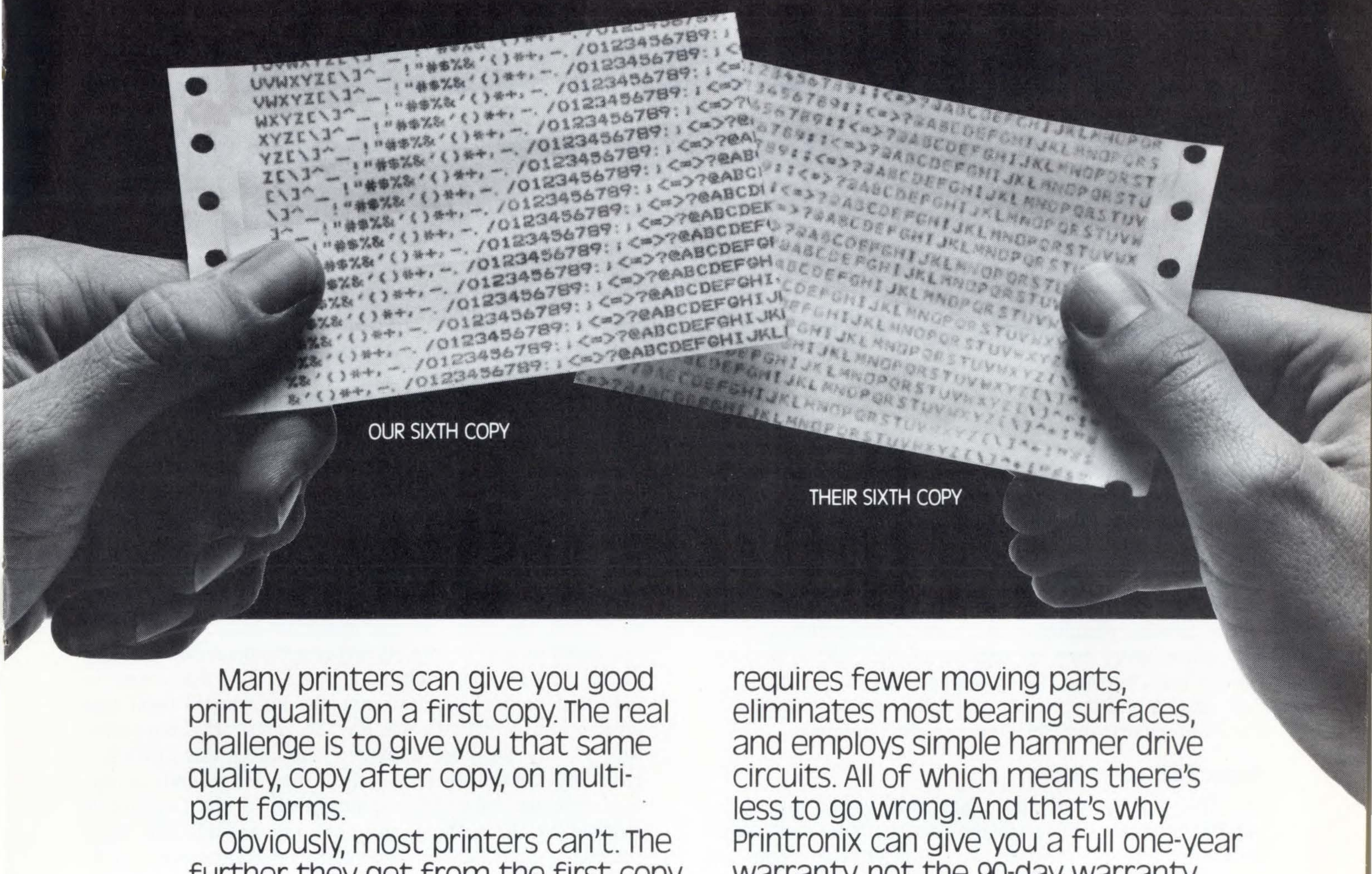

Many printers can give you good print quality on a first copy. The real challenge is to give you that same quality, copy after copy, on multi-part forms.

Obviously, most printers can't. The further they get from the first copy, the more their quality fades. But, as you can see here, the quality of Printronix' sixth copy continues sharp and clear.

This superior quality is achieved through a simple printing mechanism quite unlike any other. It forms characters by printing one dot row at a time, overlapping rows vertically and horizontally, while maintaining uniform hammer impact energy. The result is unequalled print quality and characters that appear solid.

This same design approach also requires fewer moving parts, eliminates most bearing surfaces, and employs simple hammer drive circuits. All of which means there's less to go wrong. And that's why Printronix can give you a full one-year warranty, not the 90-day warranty typical of most other printers.

For more information on the complete line of Printronix printers, call: (714) 549-7700. Or write:

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Circle 34 on Reader Inquiry Card

Special Report:

Single-Board Computers
and Single-Chip Microcomputers

1 Some Do's and Don'ts

Paul Snigier, *Editor*

A single board computer (SBC) circumvents certain subsystem tasks (including those of board design, board stuffing and testing), so the system designer can concentrate on more efficient SBC use and interfacing, and perhaps most important of all, concentrate on the software that will be associated with the board. With the purchase and assembly of the chassis, peripherals and some additional boards for A/D conversion, memory expansion, etc., the system designer's tasks become those of interfacing and software design, coding and testing. It is the the value-added of software that makes your SBC-based product unique.

Some SBC advantages

The SBC is a low-cost and expandable way to microcomputerize products while reducing "designer's trauma". After buying an SBC off-the-shelf, you add wires to a standard bus, to the I/O signal points, add a power supply and software. You've let someone else worry about the hardware headaches associated with design and board-stuffing. Nor does the OEM need to worry about extra memory and test equipment. Spare parts inventory (for field replacement) is minimized. And you've hedged yourself against component and parts shortages. SBCs are a proven design that's tested and burned-in. SBCs are easier to maintain, and they're certainly likely to require less staff training. As for the interfacing and software you'll be involved with, consider this: it may be useful in another, related or similar task coming down the road (or at least it does open up that option if marketing gives the go-ahead later).

With stand-alone SBC boards that are expandable, adding extra memory, A/D-isolated I/O functions to packaging hardware enables the rapid modification or upgrading of an existing product design.

Then, there's the matter of documentation, a matter not to be taken lightly. With existing SBCs, detailed documentation may be superior to what your designers can put together. Some of the SBC documentation we've seen was truly exceptional; a few (from a couple of smaller SBC makers), wretched. Unlike the earlier SBCs, today's SBC documentation was rated as generally adequate. Most provided adequately-detailed functional pin descriptions and bus timing and assignments, troubleshooting guides, installation information and theory of operation.

In the beginning . . .

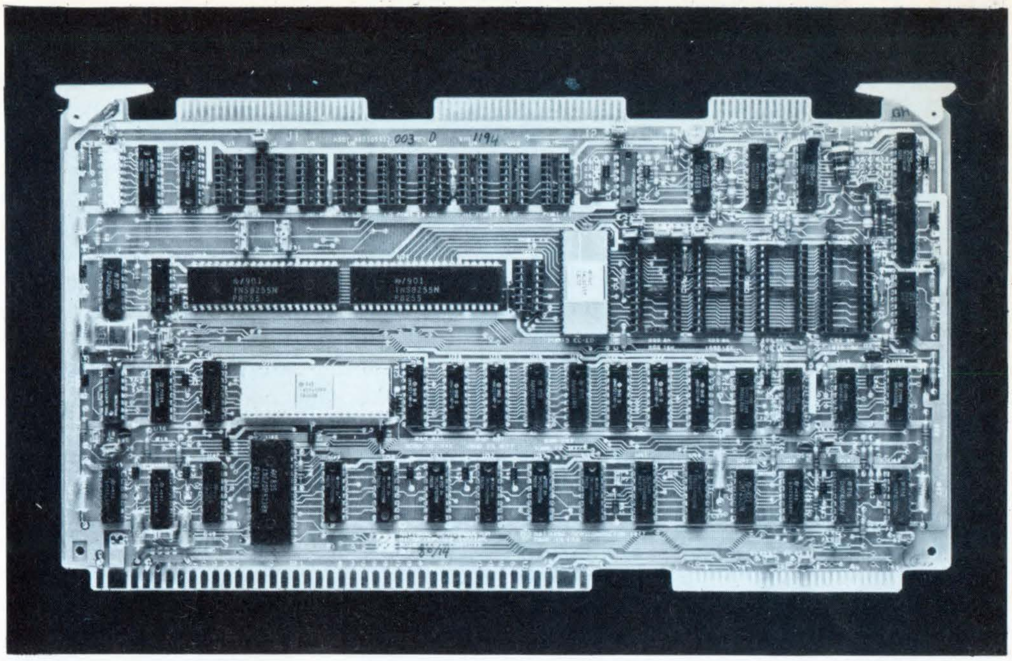
Early μP makers sold chips (CPU, clock, interfaces, ROM, RAM, DMA) separately at first. Next, they sold them as kits, with some (like National Semiconductor's SC/MP) selling in plastic blister packs. The boards, when assembled, didn't work half the time for one reason or other. Instructions contained errors. In one blatant case from a lesser semiconductor firm (it manufactured a popular 8-bit micro used in industrial control applications), the kit's board itself was layed-out incorrectly (it was Rev. 3), and shorted the power supply! Pity the poor designers who chose this firm's kit-built SBC. On the other hand, the firm which second-sourced this particular micro offered an assembled SBC (which was selected by the author); and not only was this SBC more compact (about half the size), but its maker provided superior documentation.

But, in the beginning it was another firm that pioneered SBCs. It started with Intel's vintage MCS-8 development system (which antagonized designers and led to the MDS-80). The MCS-8 could be viewed as an 8080-based SBC with 1k of RAM and 2k of PROM and some I/O ports. Since the MDS series used separate CPU, data memory, I/O and program storage cards, it wasn't an SBC. The SBC 80/10 (1-kB RAM and 4-kB EPROM/ROM) provided 48 programmable I/O lines, followed by a souped-up version – the 6.75 x 12" SBC 80/20, with its 2-kB RAM, increased interrupts, internal timers and, perhaps most significantly, a shared system bus arrangement.

Other manufacturers dogged Intel's steps – among them Motorola, which introduced EXORciser cards. The EXORciser, with its resident software and hardware emulation, was Motorola's system design and development tool. The cards formed the 6800 Micromodule family. Not to be outdone, Zilog's Z80-MCB offered 4-k RAM and double the speed of the SBC 80/20.

With chip prices falling, and with OEMs preferring as-

Board-level computers are offered in increasingly diverse ranges of power and flexibility. Self-contained SBCs, such as this one from National Semiconductor, include CPU, system clock, RAM, ROM, I/O, serial communications interface, and bus logic and drivers on one card.



sembled SBCs for lower-volume production runs, the trend to SBCs accelerated. It was not only a question of OEM demand, but the beginning of an inevitable trend that would make the semiconductor manufacturers into system houses – a trend that will continue into the future (as discussed in January's Special Report on "Add-In/Add-On Computer Memories"). With the cost of chips plummeting, vendors realized that this could not forever be offset by increased sales. By designing, burning in and testing SBCs, they could add value to their chips.

When to avoid an SBC

The buy or make decision boils down to several factors. Of course, the question of cost is foremost. If your firm will manufacture 300K units, then obviously it makes sense to design a board; if only 200, then buying an SBC off-the-shelf is the way to go. In the former case, it may well pay to program on the assembly level and optimize code since the development, production, burn-in and testing costs will be amortized over a long run. In the latter case, however, these costs assume such a significant proportion of system costs that buying complex subsystems off-the-shelf is the optimum route. This includes SBCs and A/D-D/A boards that fit inside a computer and designed for that specific SBC. They are mechanically-compatible to the card guides, bus-compatible to the backplane electrical pinout; and perhaps most important, they are software-compatible to that SBC's assembly- and higher-level language.

The crossover break-even point varies and must be determined on an individual basis. It depends on several factors that vary from OEM-to-OEM and product-to-product. If the product is for a control engineering application, a less sophisticated micro will probably do, and the hardware will be more direct. Less code will be generated, so development tools and costs will be lower – even in the several-hundred volume. But a more sophisticated system is a different story, and unless you can get other departments to share the development tools and aids and their purchase costs, the crossover point will be significantly higher. Such greater complexity could push the crossover to 1,000 units annually or more.

Another factor is the ratio of computer cost to the final end-product selling price. Although it's typically in the 15 to 25% range, it can be less (or more). If less, then it's better not to build. A $180,000 product incorporating a $2000 micro has a 1.1% ratio.

Of course, this all assumes you have manufacturing capability. It involves building prototype boards, debugging software and hardware, PC board (PCB) layout and testing, building production PCBs, testing them and reworking them. Only then can you assemble and test them in the final system before shipping and installing them. If you go the buy-route, debugging software and hardware (and modifying software) will shave months off the development. If getting to market several months earlier can establish more dominance in the marketplace, increased sales may compensate for increased hardware costs from going outside to buy an SBC. Conversely, if your firm is a late starter in this given market, is getting to market later going to make things any worse? In such cases, it's usually better to build, not buy. But as a general rule, if production volumes are great, manufacturing costs will predominate over development costs.

SBCs are less flexible, lack functionality and may have hardware you don't need. SBCs cannot be everything to everyone. This means that if you're lucky, you'll find an SBC that meets your needs with little excess hardware, that is, small mismatch to your application. The smaller the production run, the greater significance will the development costs become; and in such cases, you may be willing to tolerate a greater mismatch between the board and your application. Conversely, as annual production run figures reach greater numbers, you will tolerate less mismatch, since production costs predominate over development costs.

Consider service when evaluating the build-versus-buy decision. Five to ten years from now, those boards will be coming back for service. For example, 4004- and 4040-based boards are still coming back to their makers and must be serviced or replaced – perhaps for another decade!

Lead times are more likely to impact an OEM going the build-route. Lead times affect total material-related costs. Vendor lead times determine your replenished stock levels that are necessary to minimize total cost of stock-outs and inventory holding costs. With a demand that's forecastable and with perfectly predictable supply, precautionary safety stocks may be kept low.

If inventory levels are not high enough, late or unreliable deliveries (a common occurrence in this field) almost guarantee excessive stock-outs. To prevent this, it's necessary to make a tradeoff, that is, to compare the damage (in cost) created by potential late deliveries balanced against cost of increased inventory levels. The latter inventory costs, which may be calculated reasonably well, depends upon known variables; the former, late delivery costs to your system, is often only a rough guestimate. The cost of chips or parts unavailability is difficult to quantify and even more difficult to analyze objectively; it depends upon intangibles like the financial losses incurred by getting to market a month or two late. Or, of using alternate chips or parts (e.g., 1-k or 4-k instead of 16-k RAMs) at the last minute that can make trouble, or even reworking of boards in worst-case situations (although the systems designer would have foreseen this one). Inventory costs include interest charges on money tied up in stored parts, insurance, deterioration, labor (in receiving, storekeepers, material control) and floor space. Taxes on inventory, particularly in California, are a factor. (To circumvent this, a few California firms ship their inventory to out-of-state warehouses in Nevada and elsewhere and later return them, and do this each year.) I mention these factors, since they are among those all too often overlooked when the buy-versus-make decision is being weighed. If boards are made in-house, the shortage of just one part can hold up the entire line. Obviously, with making boards there is more that can go wrong.

If you go the "roll your own" route, then there are other much-overlooked factors, such as the added clerical cost per document. Buying a single SBC can cut this by several orders of magnitude. Whether you build or buy will be determined by the design process.

The system design process

Typcially, the OEM will determine the customer objective(s) and define the solution in terms of its operational specification and requirement. After the performance of the product or system is defined to the customer's satisfaction, the system is defined in terms of size, vibration specs, system support, etc. It is here that the system designer must evaluate the various chip sets and make a preliminary decision on whether to go the component, SBC, modular or box route.

Define the processes to be controlled. It is the system designer's job to understand the processes and determine what must be maintained and controlled. If a complex process, the operational specs may involve considerable effort and meetings. The system designer will be involved in this procedure. Unlike data processing and software types (who all too often live in black boxes) the system designer cannot divorce himself from the physical reality of the total picture, and to do so is to court disaster. For example, if papermaking facilities must be automated, you must gain some understanding of the raw materials and their characteristics, flow, and processess and/or equipment (heating, refining, sizing, loading, forming, calendering and packaging). This involves study, locating and talking to experts, and visiting customers' plants. In this early stage, flow diagrams are drawn and process I/Os are defined. Voltage, temperature, pH and other levels, and switch closures are defined. If front panels are needed, the controls are defined at this stage. Unfortunately, there are no rules because each system application is different. This may include LCD or LED display of pulp temperatures, manual overide control, discoloration, fountain solution pH, moisture content and related variables.

Can the μC-based controller be near the process equipment? Probably not. If there is a particulate or chemical atmosphere, how will this affect packaging constraints? Must the controller(s) interface with a main computer that will modify parameters, depending upon product requirements and other variables?

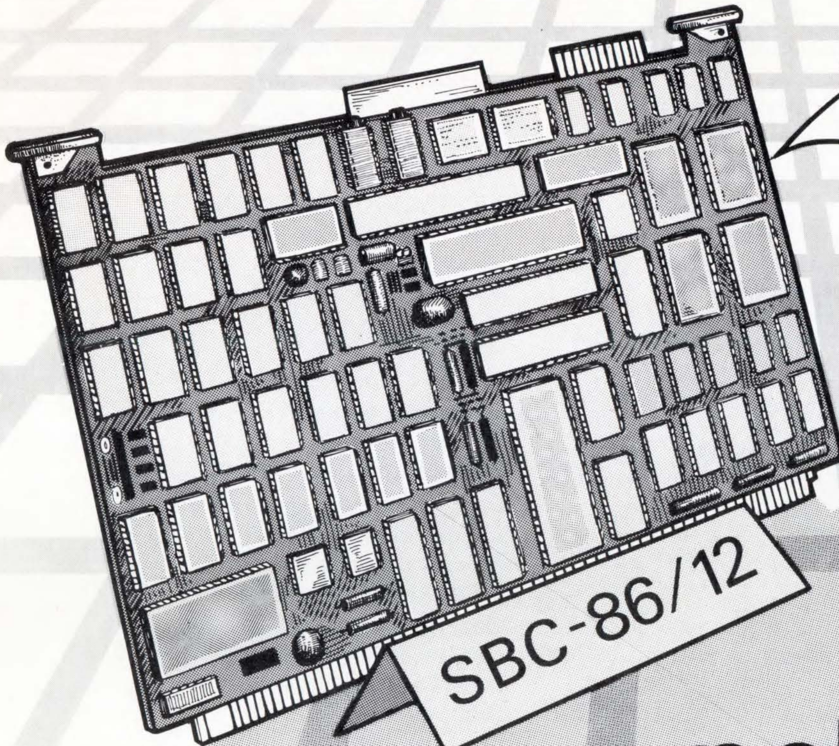
At this point, the operational specification is defined to the satisfaction of both OEM and customer(s), and the system operational requirement has defined the system in terms of its intended use(s).

Next, the actual system design specs are drawn up. How the system functions meet the functional specs and the way the subsystem functions fit in are defined at this point. It is during this process that the initially-chosen chip set may

Board	**Component**
Complex design complete	*Lengthy design cycle*
Intricate PC board layout complete	*Time-consuming layout required*
High-volume PC board fabrication on-going	*Additional fabrication capacity needed*
Parts inventory in place	*Varying parts availability*
Established production capacity	*Additional personnel required*
State of the art test equipment	*High $ capital outlay for testers*
Low incoming-reject rate	*Extensive component incoming-inspection required*
Detailed documentation available	*Functional documentation required*
A limited warranty	*Extensive maintenance/repair procedures needed*
Flexible system design concept	*Specialized application*
Upward expandable/modular compatibility	*Limited compatibility*
Extensive software available	*Major software required*
Responsive board inventory levels	*Long lead-time inventory constraints*
Minimum product development time	*Unscheduled development delays*
Fastest "product to market" cycle	*Long "product-to-market" cycle*
Less flexible; mismatch to application	*Lower cost in high volume applications*
	More flexible; less (if any) mismatch to application

Single board or multiboard computers offer advantages over OEM-designed boards. These advantages, adapted (and modified) from a comparison of the Mostek MD Series, holds true with the caveats mentioned in the text.

I want a real-time, multi-tasking operating system.



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If you are planning to use an SBC-86/12 board in your final system, you have the principal components of a development system already: a CPU, plenty of memory for most applications, and a serial port for a CRT. This simple addition of an SBC-204 disk controller provides the final ingredient for a powerful development system in which you can fully test your application **software and hardware** interactively, without needing cumbersome in-circuit emulation.

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Specific Application	General Application
Control for Remote Security System	Security Systems
Television Station Video Tape Controller	Public Broadcast Control
Test Equipment for Video Disks	Test Equipment
Test Equipment for Tape Drives and Peripherals	Test Equipment
Automobile Testing	Automotive Instrumentation
Control and Monitoring of moisture and humidity during production	Environmental Controls
Smart CRT Terminal	Computer Peripherals
Camera and Model Controller for Special Effect Movie Camera	Electronic Photography
Laser Control for Cloud Monitoring Equipment	Laser Control/Meteorological Instruments
Flight Monitor System	Avionics
Data Logger for Mass Transit System	Information Feedback Systems
Special Card Readers for New York Stock Exchange	Data Sensing Equipment
Office PBX System	Telephony
Automated Pathology Machine (Tissue Tester)	Medical Electronics
Production Control of Utility Power Transformers	Process Controls
Electronic Photographic Processing	Process Controls
Automatic Turnpike Control System	Traffic Control Systems
Automatic Wagering Terminal	Electronic Gambling
Chemical Plant Industrial Control	Process Controls
Portable Terminal for Insurance Salesman	Remote Computer Peripherals
Solar Energy Control System	Energy/Environmental Control
Environmental Monitoring Equipment	Energy/Environmental Control
Plastic Production Machinery	Process Controls
Data Communications Concentrator	Data Communications
Data Communications Line Analyzer	Data Communications Feedback
Data Acquisition from Sonic and Nuclear Sensors	Data Acquisition and Control
Communications Front End Processor	Data Communications
Security System at High Rise Building	Security Systems
Information Processor for Chemical Refinery	Q.C. Control
Oil Field Data Logging Equipment	Instrumentation
Check Verification System for Banks	Credit Security
Pipeline Investigation Equipment	Petroleum Industry
Movie Camera and Animation Control	Electronic Photography
Control System for High Speed Printer	Electronic Typesetting
Instructional Terminal for Shop Operation Control	Process Controls

These specific and general SBC (and multiboard) application categories, though relating to the MD Series, are just a few of the prime application categories for off-the-shelf boards.

prove inadequate or unsatisfactory, or the decision to build versus buy may be altered. The most suitable μP chip is chosen, and the decision to buy or not buy off-the-shelf boards, supply and packaging must be made. Such a decision must be made only in light of the overall picture of the market and your firm. How much sooner will off-the-shelf boards get you to market? And, will this advantage pay off? What is the cost of failure? If time is available to design an SBC, do you have the hardware and software design know-how in-house to transform unproven SBC boards, software and interfaces into a production-ready system within budgetry and time constraints? And can you get experienced individuals assigned to your project? If not, is hiring a consultant or outside firm to assist in the software and/or hardware design worth it? And, if so, will everyone vanish after the system is fabricated? Does your firm have existing in-house board-stuffing and test capability?

This structured approach to creating system design specs proceeds in concurrence with the engineering effort in writing system support and maintenance specs. This involves a consideration of reliability, servicing, product acceptance testing specs, customer training and documentation. Maintenance, if preventive, will require that different diagnostics and test points be speced than if the system will run to failure. If to failure, then the less-sophisticated diagnostics and test will require servicing on the component level more than if preventive. The problem of designing test facilities for micros, and that of testing software, are thorny problems; and, all too often, costs associated with them are overlooked by the system designer.

Examine alternatives

Rare is the day that our editors don't receive at least one SBC product release and accompanying spec sheets. There are hundreds of boards available from both small-to-large independents and the semiconductor manufacturers.

In your comparison of SBCs, be sure to examine as many of the manufacturers' literature as possible. Among other things, compare RAM/ROM size, memory expansion, number of serial and parallel ports, number of interrupt-priority levels, power supply needs and maximum asynchronous baud rate. Do check board size, languages supported in PROM, and bus.

As for languages supported, the availability of high-level languages will continue to affect SBCs. Available in one- or two-chip ROM or PROM sets, these languages first included

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National's NIBL (for its SC/MP) and Lawrence Livermore Lab's BASIC in 1977, but since then have been expanded and now include, among them, the following: BASIC, Mini-BASIC, MicroFORTH, PCROS, PL-65, FANTOM-11, ASM80, PLM80, ZIBL 2.2 (Z80 Industrial BASIC) and MACSBUG. Many SBCs we examined offered just assembler level, or some combination. It was once predicted that PROM-based high-level languages would quickly eliminate the need to code SBCs on the assembly level. No such thing took place. Although the trend is unmistakable, assembly and high-level languages each have their place.

What about a straightforward thing like board size? If SBC makers were to standardize to any meaningful degree, this is an obvious area, or so we would think. No such luck. Calls for standardization among SBC makers are made from time to time, but from what we've seen, little headway is being made. If SBC makers can't agree on this, it's unlikely they voluntarily will agree on anything else. Boards come in the following sizes: 4.5x4.75, 4.5x6.5, 6.75x12, 7.5x11, 7.7x7.5, 8.15x11, 8.4x11.6, 9.4x12, 12x6.75, 12x7 14x9.75, 14.8x12.4, 16x8. If anything, there is an increased proliferation of sizes. Functional differences exist, so before selecting an SBC, choose carefully: once you've selected a firm's SBC, you're locked into that vendor's family; and although it's true that you can interface different boards, it's going to cost in terms of design time and frustration, possibly in system efficiency, and certainly in terms of hidden costs (such as testing).

Is popularity a criterion?

Board makers were never too eager to provide interchangeable boards. After all, what vendor wants to encourage OEM shoppers to buy their CPU boards but someone else's memory boards? From a practical point, there are other difficulties, such as interfacing woes. For better or worse, this can lock you into one vendor's family. As a rule, the semiconductor manufacturers offer more general purpose boards; independents are more likely to offer boards tailored to more specific applications (and therefore, are less popular).

System designers who select a board that's based on a micro that's less popular are gambling, increasing the likelihood that their choice will be provided declining support in the future.

Which will have a greater chance of surviving in the microcomputer jungle? Leaders – 8086, 6800, Z8000, Z80 and their variants – will be there, of course, as will be others. Many less popular micros and SBCs won't die – just age, with less and less support. Lock into one of these and you're in trouble. We won't mention some of these; you know them as well as we do. In case you're not sure about an SBC's or micro's future, there is one clear factor that stands out above all others – its popularity with designers. If users are scrambling to use it, you can bet it will be around for some time and support will be there. Still not sure? Check to see how popular it is with OEMs. And, the micro and its boards should occupy at least 10% of the market. If the alternate sources are numerous and large heavyweights, then their marketing departments have given that micro their vote of confidence. Conversely, if there is only one, smaller firm second-sourcing that micro, watch out. Then, too, don't neglect to see what exists in terms of development aids provided by the big semiconductor makers, whose marketing departments, once again, give their vote of confidence for supporting those micros that will survive the best. Of course the supreme stamp of approval is the Department of Defense, which only accepts those micros (6800, 8080A, 2901A) that they anticipate will remain on the scene for a good while.

Multiboards

SBCs can be inflexible, and the mismatch between board and product sometimes can be great. With multicard expandable board sizes, you select those cards you need and plug them into a card cage or cabinet. Unlike the SBC, the cards are functional, that is, one holds the CPU; a second, the clock and control circuits; a third, RAM/EPROM memory; a fourth, programmable interfaces and I/O; a fifth, diagnotics; a sixth, customizing kluge (blank) cards; and so on. These card families are modular sets.

Multiple boards offer semi-customizing flexibility but cost more than SBCs. Each card is separate, creates a less reliable system, and requires extra parts to intercommunicate with the other cards. Testing is more costly. Unlike SBCs, which can be expanded by adding more memory and I/O with separate cards, multiboard families need a minimum number of cards to be an SBC's functional equivalent.

Pro-Log takes an engineering approach to μP design. Using their techniques, engineers do hardwired logic or electromechanical design without data processing people. If you don't want to be tied up with proprietary software or design aids, and avoid copyrighted mnemonics and other strings-attached situations, it's the way to go.

Pro-Log and Mostek jointly created the STD bus to avoid the overkill of bigger buses. The STD boards are 4.5x6.5″ and interface via inexpensive 56-line edge connectors. For process control applications in particular, and for designers not interested in drowning in the high-priced world of complex development systems run by data processing experts, this approach makes sense. The Pro-Log/Mostek gamble with the STD bus has paid off. Pro-Log makes money selling its PROM programmers, is well-suited to the less sophisticated non-data processing designer and is tailored to aiding the small OEMers.

Development

Don't rely on your board to do the development. Some manufacturers claim their boards come with trace and debug programs and monitors, and some even come with onboard keypads and LED displays. It's better to rely on development systems, with their editors, relocatable assemblers and compilers. True, certain processor systems allegedly are designed to be used as both development system and product boards in the final product to provide complete control of code entry and debugging and other features "not found elsewhere at these low prices". So the product literature says. The boards are toys suited for six-hour courses and seminars – not serious software development. With little or no debugging and editing support, these boards can consume many weeks. Despite warnings from leading μC experts, hardware-turned-software designers still fall pray to the illusion of getting something for nothing.

We do not criticize the approach of a local prototyping board that attaches to the development system when needed. If containing debugging facilities and compatibility with the development system, and used in less-sophisticated applications, it can prove adequate. An example is the AIM-65 featured on this month's cover.

Ingrained attitudes remain. On one hand, a software-oriented firm, particularly if their expertise is in minicomputers, will go the purchase route. Their value-added in terms of software will offset the added costs of buying

boards and/or hiring consultants. This makes sense. But hard-wired designers, used to designing their own circuits, are more likely to take a build-attitude to the boards – an ingrained attitude they often carry over (unfortunately) to the software development.

Hardware vendors generally steer clear of application software. They're in business to sell boards; and if an OEM wants a complete package, he will generally develop the applications routines himself or with a consultant. It is the OEM's development of the software tailored to specific end users that adds value. If he hires consultants, then he should expect to work with them, since it is he (the OEM) who best understands the details of the processes that must be controlled in the customers' applications.

For More Information ...

The following firms supplied us with product literature and information on SBCs. To obtain further information, please contact them.

Advanced Micro Devices Inc.
901 Thompson Pl.
Sunnyvale, CA 94086
(408) 732-2400

Bedford Computer Systems Inc.
3 Preston Ct.
Bedford, MA 01730
(617) 275-0870

Compas Microsystems
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Ames, IA 50010
(515) 232-8187

Creative Micro Systems
11642-8 Knott Ave.
Garden Grove, CA 92641
(714) 898-9669

Cybertek
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Seminole, FL 33542
(813) 392-3467

Data General
Westboro, MA 01581
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Digital Equipment Corp
Components Group
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Dynabyte Inc.
Elwell Court
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(415) 965-1010

Harris Semiconductor Products Div.,
Box 883
Melbourne, FL 32901
(305) 724-7000

Heurlkon Corp.
700 W. Badger Rd.
Madison, WI 53713.
(608) 255-9075

Intel Corp.
3065 Bowers Ave.
Santa Clara, CA 94301
(408) 249-8027

Intersil, Inc.
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Cupertino, CA 95014
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Microproducts
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Redondo Beach, CA 90278
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Monolithic Systems Corp.
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Motorola Semiconductor Products Inc.
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National Semiconductor Corp.
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Santa Clara, CA 95051
(408) 737-5000

Ohio Scientific
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PAIA Electronics Inc.
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Lafayette, IN 47904
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Zilog
10460 Bubb Rd.
Cupertino, CA 95014
(408) 446-4666

2 MC6801 Offers Versatility

James J. Farrell III
Motorola Semiconductor Products, Inc.

How will single-chip microcomputers affect single-board computers? Those that are tailored for industrial and simpler control applications will take one route; those others, the more powerful micros (such as the 6801), will take a higher-ended toute. Accordingly, we will select the 6801 as our example. It will not be our intention to examine the 6801; this was done in September (pg. 62) and October (pg. 42) issues, which discussed the hardware and software concepts of this particular micro. Instead, we will show the 6801 in its evaluation module for system development.

The MEX6801EVM Microcomputer Evaluation Module is a completely self-contained μC on a single card, providing the user with the means of evaluating the 6801. The system allows the user to easily evaluate the MC6801. As configured, the 6801 may be evaluated in the Single-Chip mode by attaching an RS-232-compatible terminal to the serial port of the module. Thus, the minimum functioning system consists of only the 6801, 1488 and 1489.

In the Expanded mode, the customer may add an ACIA, PTM, 4K bytes RAM or 2K EPROM and a programmable gate array for addressing configuration.

The Evaluation Module provides the user with the ability to evaluate the 6801 microcomputer using the DEbug monitor via the serial I/O port and RS-232C interface. Sufficient space remains within the on-chip RAM for the user to write a small I/O program to work in conjunction with the DEbug monitor. The DEbug monitor program (LILbug) uses a patch table established within RAM for all I/O. Thus, the DEbug program's I/O routines can be readily modified by the user for the purpose of evaluation. Since the DEbug monitor uses the timer output and the serial I/O port, these resources are not available to the user in the Single-Chip mode. However, by using the Expanded mode, the user has the choice of adding an ACIA or PTM, thereby freeing more of the on-chip resources. The Evaluation Module has provisions for adding 4K bytes of static RAM and a 2K byte EPROM. This permits the user to develop his programs if desired. In addition, the Expanded mode allocates 8K bytes of off-board program space for further programming flexibility.

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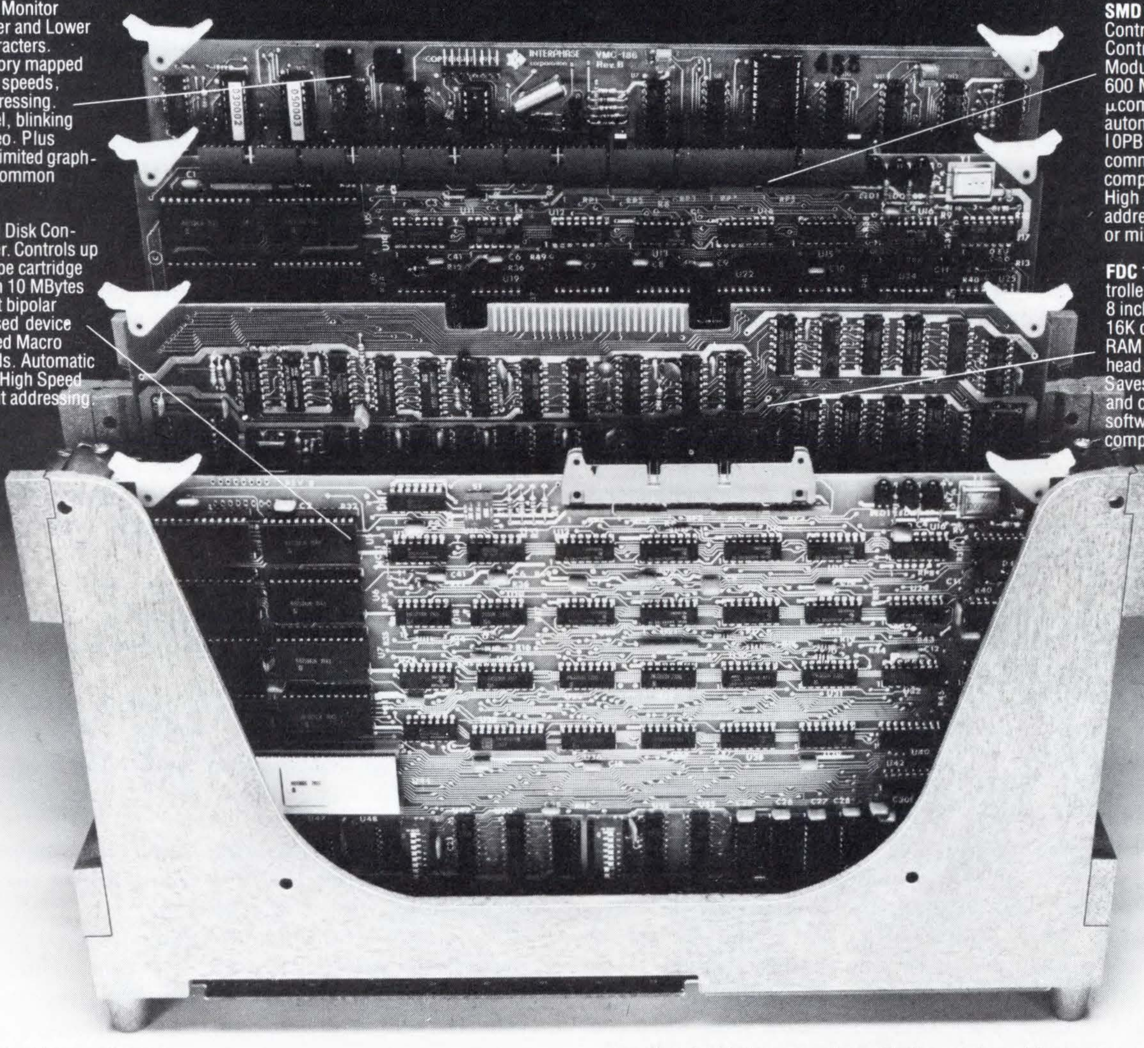

SMD 2180 Storage Module Controller/Formatter. Controls up to four Storage Module drives with up to 600 MBytes each. Bipolar μcomputer based with automatic error recovery. IOPB based Macro Level commands, software compatible with HDC 1880. High speed DMA with 20-bit addressing in 8 bit, 16 bit, or mixed systems.

FDC 1680 Floppy Disk Controller. Controls up to four 8 inch or Mini-Floppy drives. 16K of dual-ported on-board RAM eliminates bus overhead during disk transaction. Saves card slots, power, and cost. Extensive common software drivers. CP/M compatible.

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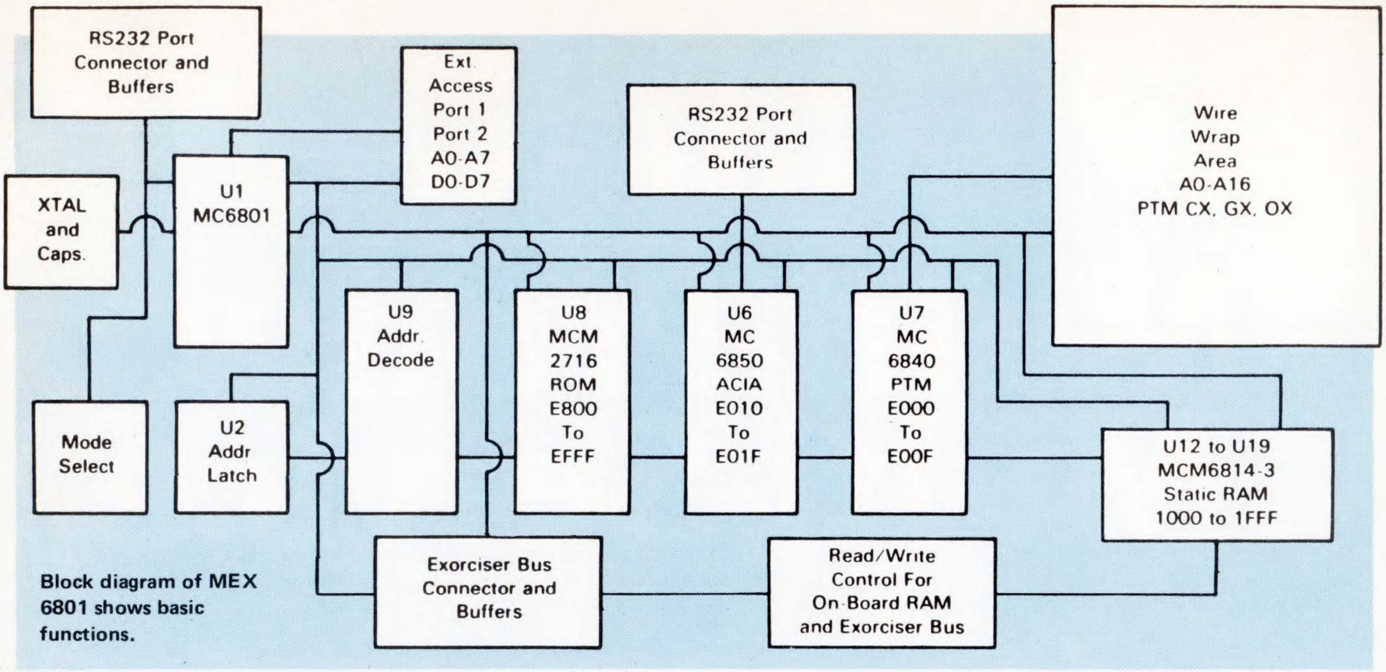

Block diagram of MEX 6801 shows basic functions.

A wirewrap area is provided to permit the user to interface other peripheral devices or special interface circuits to the 6801.

Using the 6801

The MEX6801 Evaluation Module permits the system designer to configure his hardware and develop his software for his system. In order to simplify the explanation of this circuit, the block diagram shows the circuit. Let's examine the MEX6801 functions in greater detail.

Mode Select. The three switches of the mode select circuitry, permit selection of one of the eight modes of the MC6801. The condition of these switches during RESET determine which mode is selected. The modes are explained earlier in this article.

XTAL and capacitor. The crystal used in the clock circuitry determines the internal BAUD rate. If the 4.9152 MHz is to be used, the higher frequency MC6801-1 (1.25 MHz) must also be used. The value of the two compensating capacitors is 39pF.

MC6801. Presently, the 6801 is available in two frequencies– the standard 1.1 MHz MC6801 and the faster, 1.25 MHz MC6801-1.

RS232 port. This RS232 port is directly controlled by the Serial Communications Interface port on the MC6801. The MC1488 and MC1489 perform the ouput and input buffering necessary for this function.

External access. This area of the printed circuit board (PCB) allows user access to Ports 1 and 2, and also to the eight data lines and the eight low-order address lines.

Address latch. This latch separates the multiplexed eight data lines from the lower order 8 address lines when the MC6801 is used in the Expanded Multiplexer Mode. During the MCU Phase 1 (01), this port contains the 8 lower order address lines. During Phase 2 (02), the eight data lines appear. The Address Strobe (AS) line, from the MC6801, informs the latch when the address lines are present.

Address Decode. This chip decodes the 6801's addresses and enables various and enables various chips occupying locations in the 6801 memory map.

MCM2716 ROM. This 2K byte, 5-V only, EPROM occupies memory locations $E800 through $EFFF. This EPROM allows the user to user to developer and correct the 2K byte program he will eventually mask oin the 6801's ROM.

MC6850 ACIA. The Asynchronis Communications Interface (ACIA) occupies memory locations $E010 through $E91F. The ACIA performs its own Serial Communication function through its own RS232 port, separate from the serial port controlled directly by the MC6801.

MC6840 PTM. The Programmable Timer Module occupies memory locations $E000 through $E00F. This timer gives the user three 16-bit timers in addition to the one already available on the MC6801. It should be noted, however, the 16-bit timer on the MC6801 is an up-counter; the three 16 16-bit timers on the PTM are downcounters. Each of the three timers on the PTM has its own external clock pin (CX), external gate control pin (GX) and output pin (OX). The PTM may also use the MC6801 "E" clock. This is selectable in software.

Wire-wrap area. This area on the PCB contains the 16 address lines and all the clock, gate and output lines from the PTM. In addition, an unused area is left for the user to develop his own circuitry.

MCM6814-3 RAMS. 4K bytes of static RAM are decoded from $1000 through $1FFF. The MCM6814-3 chips are organized as 1K by 4 bits. The MEX6801 board decodes them in pairs, to provide the 8-bit (byte) organization.

EXORciser bus. This circuitry buffers the signals interfacing with the Exorciser bus. The connector on the MEX6801 is compatible with the Exorciser bus.

R/W control. This circuitry insures that no "conflict" of memory locations will occur between on-board and off-board memory locations. On-board memory locations priority, and those locations on the Exorciser bus are disabled. The MEX6801 Evaluation Module, with its many functions, permits the designer to develop a powerful Microcomputer system using the 6801.

Software. The 6801 may be purchased with a powerful monitor on the on-board 2K ROM. This monitor, called LILBUG, thoroughly exercises the functions of the 6801. The LILBUG monitor is available as MC6801L1.

Rate this article: circle 1L, 1M or 1H on Reader Inquiry Card.

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Principles of Data Acquisition and Conversion – Part 5

Eugene L. Zuch
Datel-Intersil, Inc.

The previous articles discussed the operation and specification of A/D and D/A converters and associated circuits such as analog multiplexers and sampleholds. These data conversion circuits are used together in a wide variety of applications in industrial, scientific, and military measurement, control, and instrumentation systems.

Although the number of different applications is virtually infinite, a few of the common ones should be mentioned: arbitrary waveform generators, motor speed controls, baseline sweep generators, precision audio delays, X-Y deflection generators, automatic multichannel data recorders, programmable operational power supplies, automatic test and calibration systems, remote digital attenuators, analog data storage systems, digital video processing systems, PCM measurement systems, linear temperature programmers, digital phased locked loops, radar target generators, tape controlled positioning systems,and computerized music systems.

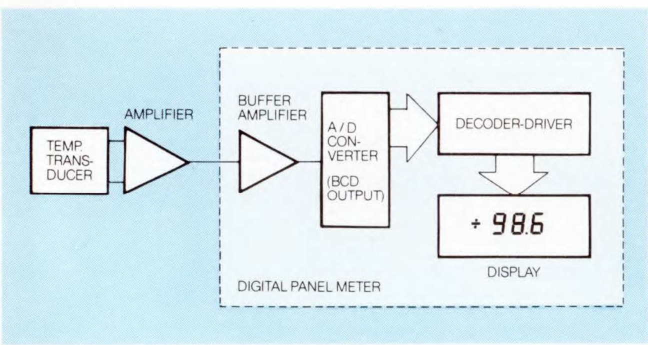

Fig 1 Simple temperature monitoring data acquisition system.

A common thread runs through most of these applications: they are either automatic measurement systems or automatic feedback control systems. Therefore, most applications of data converters are for some type of data acquisition and control system. Some of the most common types of data acquisition systems will be discussed here.

A simple data acquisition system

Perhaps the simplest type of data acquisition system **(Fig 1)** is a basic temperature monitoring system which senses and displays a desired temperature. It has a temperature sensor or transducer, amplifier, ADC, decoder-driver and numerical display.

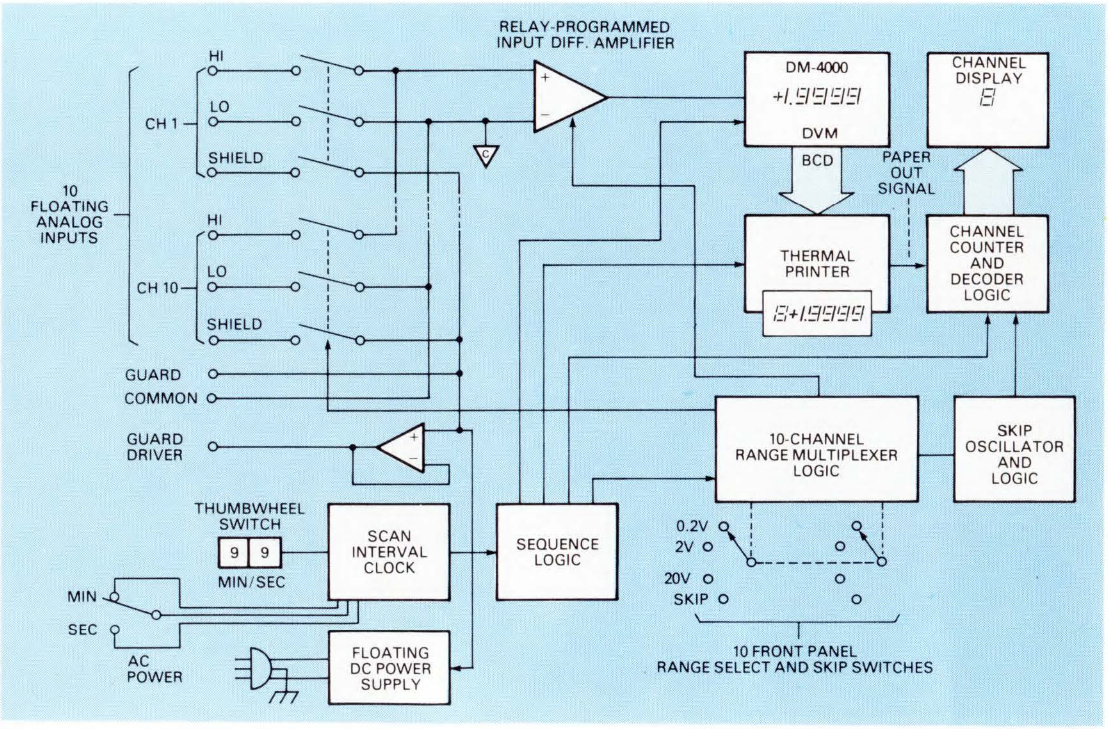

Fig 2 Block diagram of an automatic printing data logger.

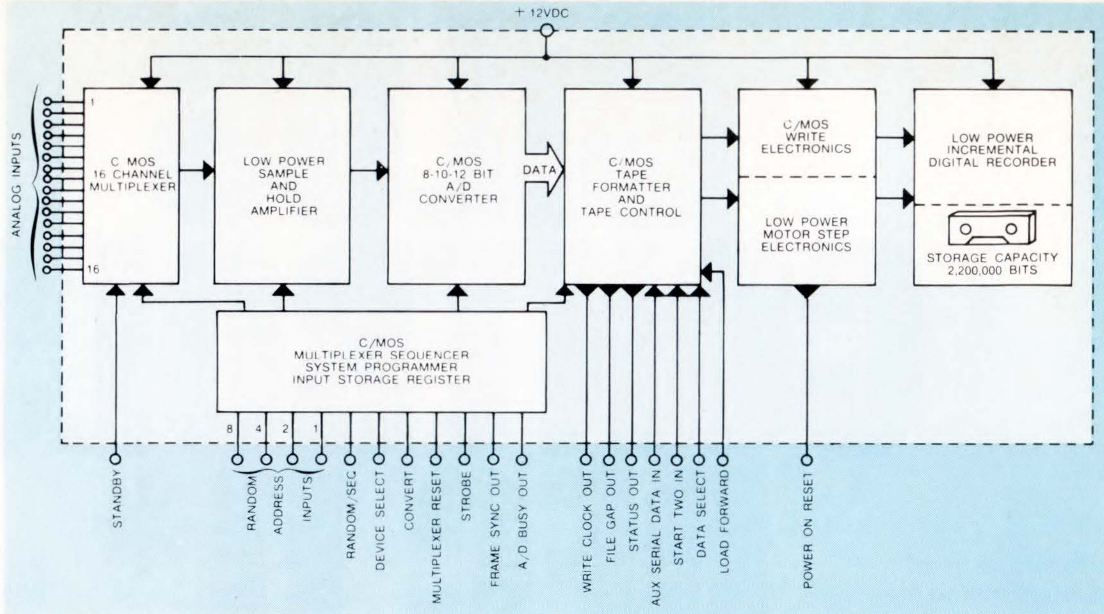

Fig 3 A lower power cassette type automatic data logging system.

Temperature can be sensed by a thermocouple, resistance temperature detector (RTD), thermistor or semiconductor temperature transducer. The output of the temperature transducer must be amplified to the proper level for the ADC input. In this example, the ADC, decoder driver and numeric display are contained in a digital panel meter. By proper scaling and offsetting, the display is calibrated to read temperature directly in °K, °C or °F.

The digital panel meter (DPM), a low cost device with either an LED or LCD-type display, consists of an input amplifier, a dualslope type ADC, a decoder-driver and display. A line-operated power supply may also be included in the DPM. Most DPM's have an internal sampling rate between 3 and 20 samples/sec. to give continuous updating of the measurement.

This simple data acquisition system can be used to monitor a number of different temperatures by using a switched input to the digital panel meter from several different sensors and amplifiers. Also, a number of different parameters can be monitored – such as pressure, flow position, intensity, etc. The system, though inexpensive and simple, has a disadvantage: it's manual and slow.

Automatic data logging systems

A more useful solution to the measurement problem is to use an automatic data logging system to measure and record data **(Fig 2)**. An operator is no longer required except when the system malfunctions or runs out of paper.

This instrument, which is relatively inexpensive, automatically scans up to 10 channels of analog data and prints out the data for each channel. It can be programmed to scan all analog channels in sequence or skip certain channels in the scan; it can also select one-of-three different gain ranges for each channel in the scan. An internal clock permits setting the scan interval from zero to 99 min. As the instrument scans the data, it also indicates the channel number and the measurement value on its own numeric display.

This automatic measuring instrument or data logger **(Fig 2)**, is simply a data acquisition system with a digital printer and numeric display. Analog inputs are scanned by a differential input analog multiplexer connected to an instrumentation amplifier for high-impedance inputs. The amplifier output drives a digital voltmeter which in turn has BCD outputs connected to a thermal printer.

The complete system is controlled by a logic sequencer circuit in conjunction with a scan interval clock and multiplexer logic. Completely automated measurement systems such as this one are commonly used in industrial and scientific applications.

Another useful automatic data logging **(Fig 3)** is a data acquisition system which scans a large number of analog input channels but then records the data digitally on a cassette tape. The cassette can store up to 120,000 16-bit data samples which can then be read out and displayed by a separate instrument.

The advantage is obvious: it can be manufactured as a low-power portable instrument which operates on batteries and is used for remote, unattended data gathering applications. Foremost among such applications are environmental monitoring systems. The user can install the system, program it for the desired data scanning interval and then leave it unattended in the field until the cassette is filled with data. The cassette is then exchanged for a fresh one and the filled cassette is read out and displayed back in the lab.

This type of data acquisition system can be designed for low-power consumption by use of CMOS circuitry and a low-power, electronically-controlled incremental cassette drive mechanism. The cassette is stepped through the digital data while recording and then shuts down until the next data scan is ready.

Data acquisition systems for computer interfacing

By far, the majority of data acquisition systems used today are required to interface with a computer. Many of them must not only acquire the data, but also distribute data from the computer output back to the system being controlled.

Because of widespread minicomputer and microcomputer use in industrial processes today, the data acquisition system has become a widely used and necessary link in the automatic control process. Several different types of data acquisition systems are now commonly used: (1) Miniature data acquisition systems (modular, hybrid, and monolithic devices), (2) High performance rackmounted or cabinet type data acquisition systems and (3) Analog I/O board type data acquisition systems.

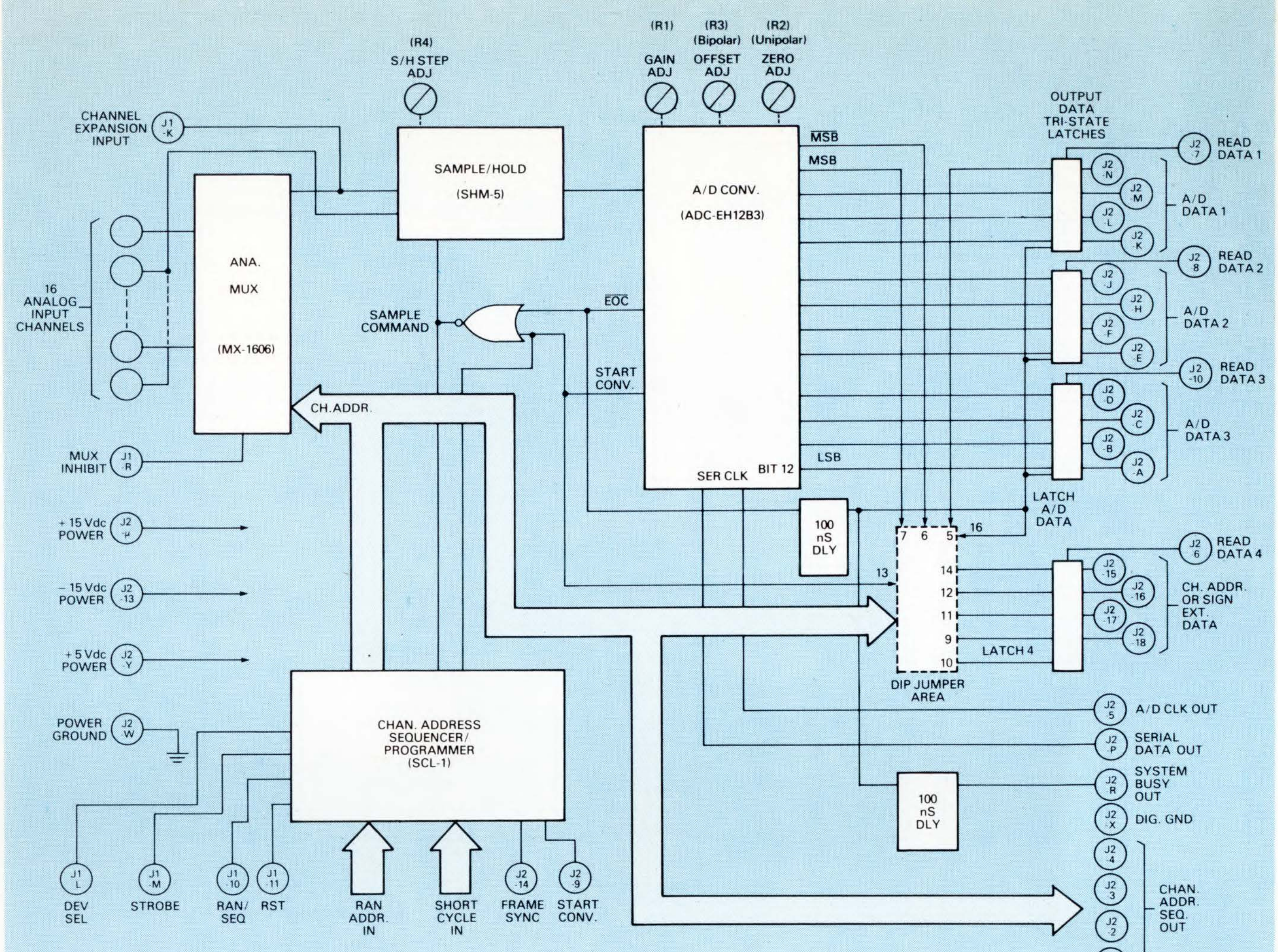

Fig 4 A miniature, high performance data acquisition system for computer interfacing.

Miniature data acquisition system

The computer-interfaceable, miniature data acquisition system **(Fig 4)** is a device small enough to be hand held and scans 16 analog input channels at 250 KHz rate and converts them into digital form. This permits operation as an analog front end to a minicomputer or μC. When operated with a very fast I/O cycle in the computer (<1 μsec), data rates up to 200,000/sec. can be achieved.

This system has a 12-bit binary output and a 4-bit channel address output which are both latched and gated to permit gating the output in 4-bit groups. Thus the system can be used with 4-, 8-, 12- or 16-bit computer data buses. It also has an internal 16 channel address counter and analog multiplexer which increments with each A/D conversion for automatic sequential scanning of channels.

Alternatively, the counter can be used as a fixed register which is loaded with a 4-bit address from the computer bus. This mode provides random channel addressing so that some high activity channels can be sampled more often than others, under program control.

In addition to the control and output circuitry, the data aquisition system has an analog multiplexer, a high-speed sample-hold, and a high-speed 12-bit A/D converter. The high scanning rate is due to both the high-speed circuitry and use of overlapped conversion and storage techniques. This is accomplished by having the analog multiplexer and sample-hold input stage acquire the next channel and settle while the previous channel is being converted into digital form by the A/D. During this time the sample-hold output is holding the previous analog value. When conversion is completed, the data is latched in the output register.

The connection of this data acquisition system to a minicomputer **(Fig 5)** is interfaced to a PDP-11, and the modular data acquisition system is a Datel-Intersil DAS-250. The interface is shown in simplified form.

External circuit modules are used to perform the interface functions, such as bus transfer gates, address decoder, status register and interrupt logic. Some (such as address decoder and interrupt logic) are standard DEC cards which slide into the computer's connector block.

Data acquisition system calibration

Proper calibration of a data acquisition system is critical to system performance. Here is a basic procedure which applies generally to all data acquisition systems: (1) Connect a pulse generator to the start convert input to the system and set pulse rate to desired conversion rate for the system, (2) Set random address inputs for channel 1, (3) connect a precision voltage reference source to channel 1 input, (4) Connect a set of lamp drivers and lamps to system data outputs and (5) Apply power to the system.

Unipolar Operation. Set precision voltage reference to zero +1/2 LSB analog voltage and adjust zero adjustment so that output code just flickers between 000. . .000 and 000. . . 001. Then set precision voltage reference to +FS −1 1/2 LSB analog voltage and adjust gain adjustment so that output code flickers equally between 111. . . .110 and 111. . . .111.

Bipolar Operation. Set precision voltage reference to −FS

Continued on page 66

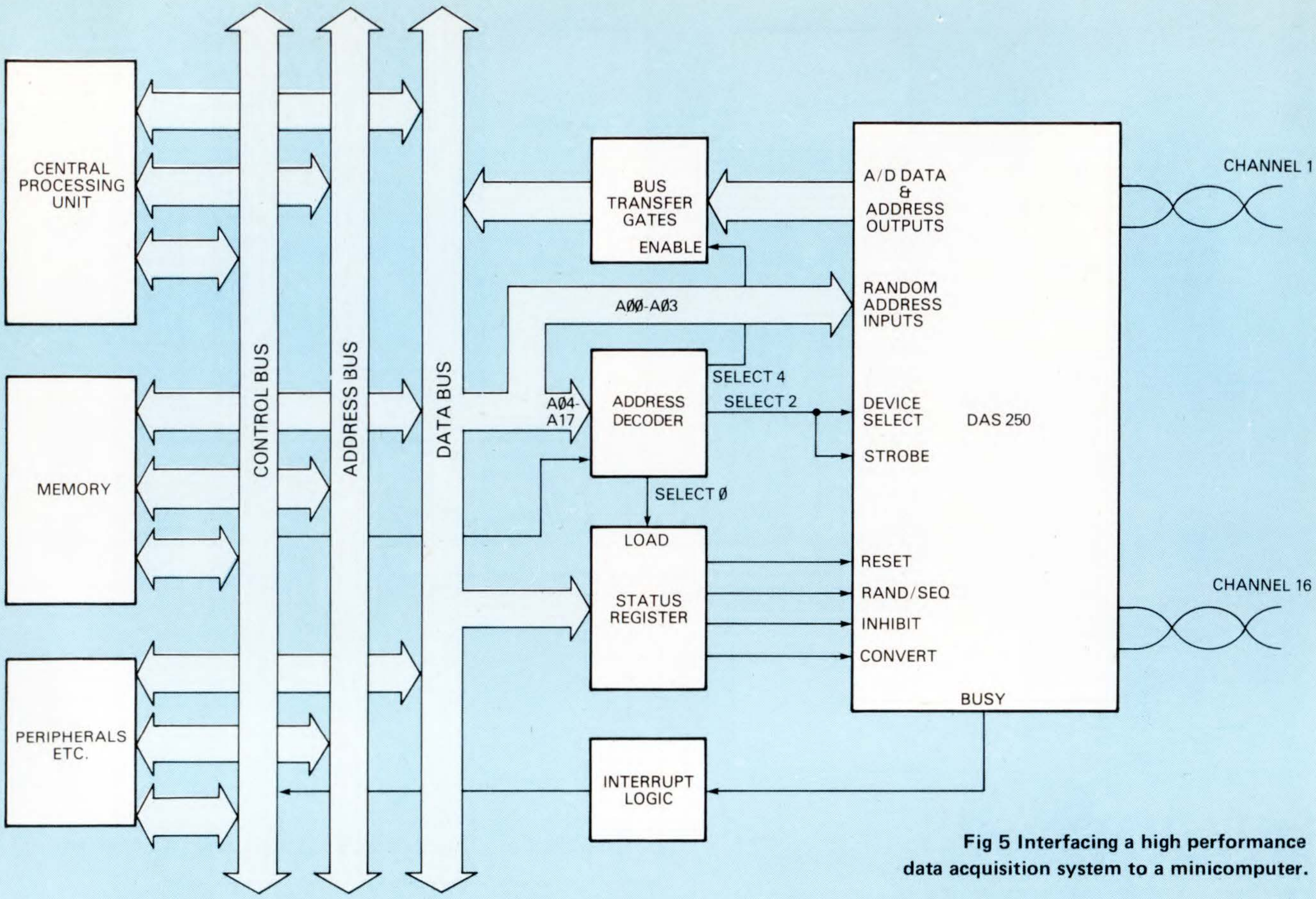

Fig 5 Interfacing a high performance data acquisition system to a minicomputer.

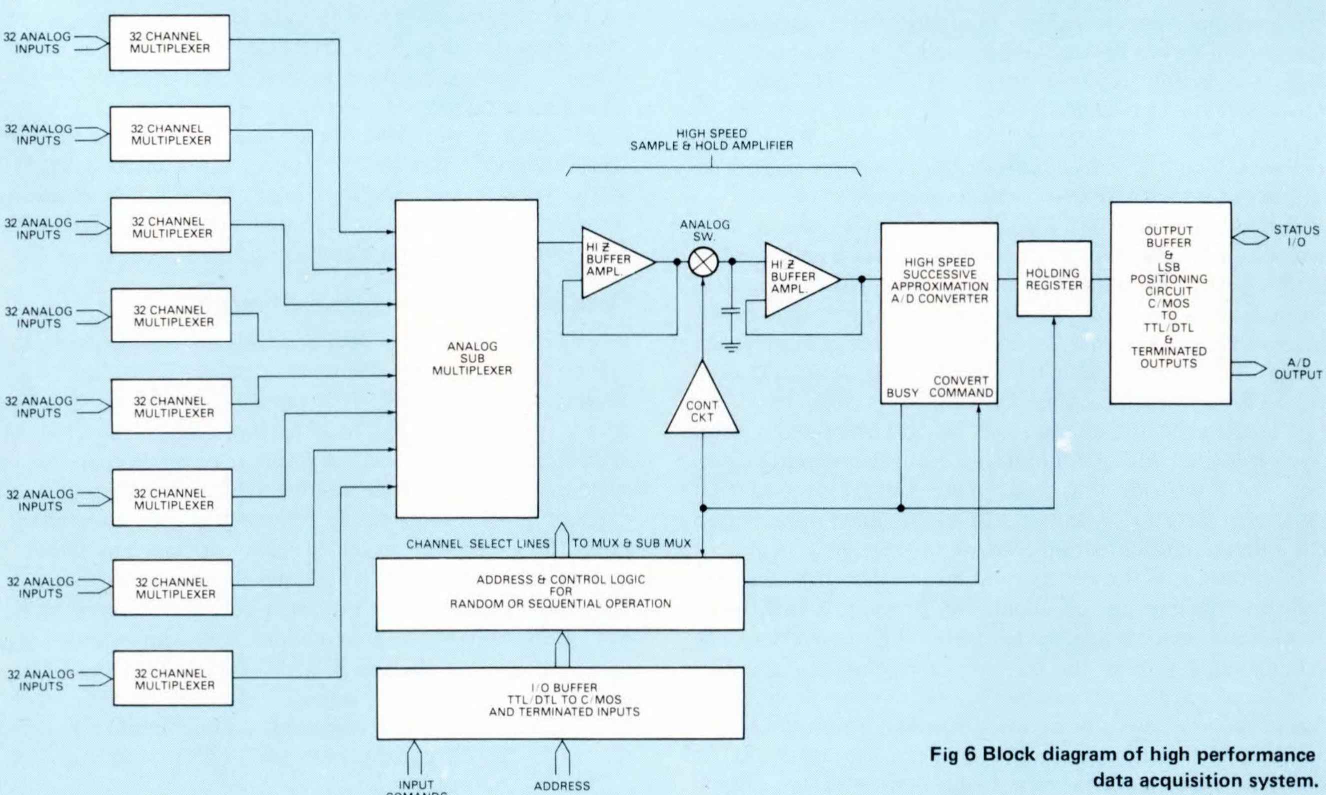

Fig 6 Block diagram of high performance data acquisition system.

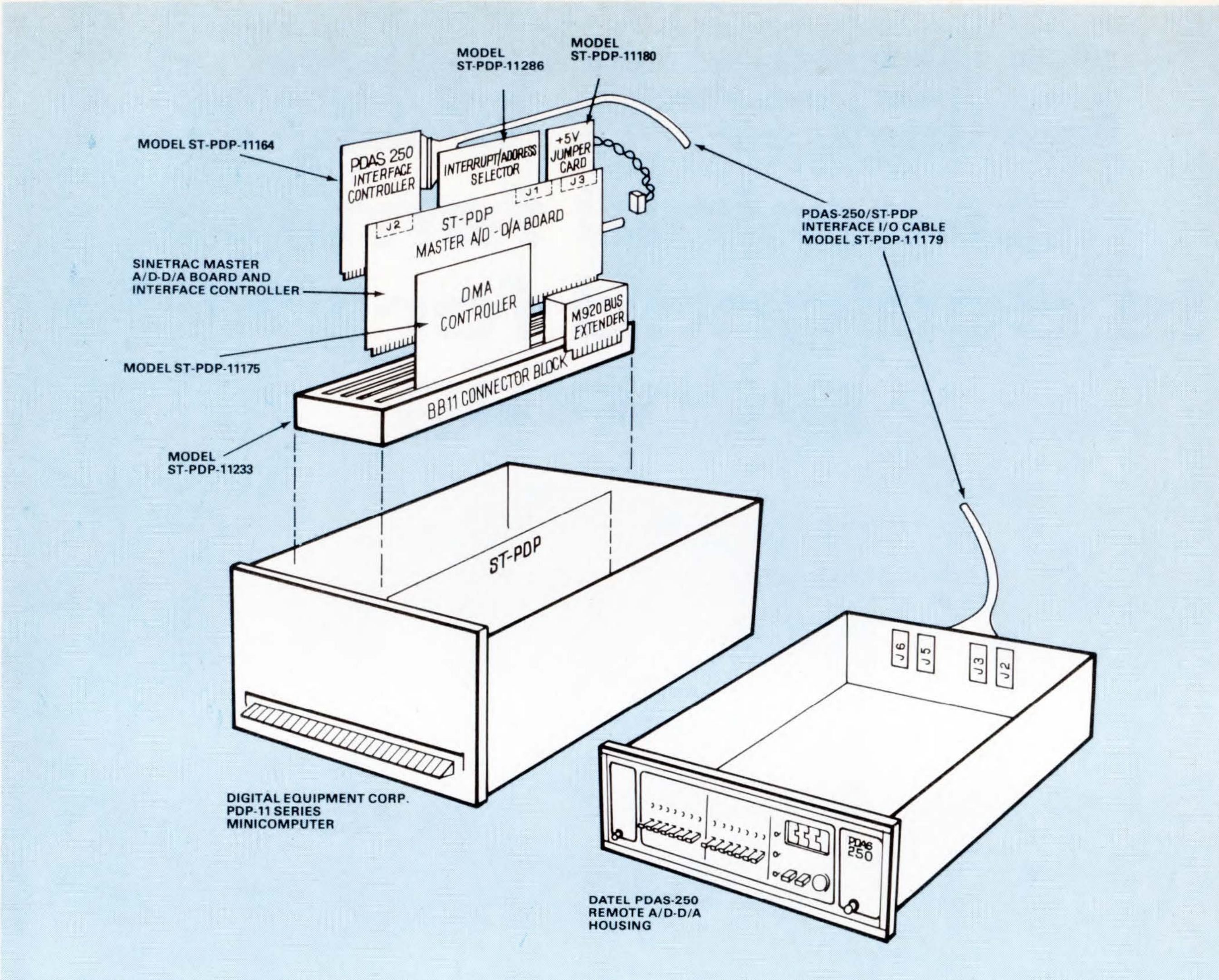

Fig 7 Interfacing a high performance data acquisition system with a minicomputer.

Continued from page 63

+1/2 LSB analog voltage and adjust offset adjustment so that the output digital code flickers equally between 000. . . .000 and 000. . . .001. Then set the precision voltage reference to +FS −1 1/2 LSB analog voltage and adjust the gain adjustment so that the output code flickers equally between 111. . . .110 and 111. . . .111.

In units where a serial data output is available, output code can be observed on an oscilloscope in lieu of display lamp.

High-Performance data acquisition systems

Another popular type of data acquisition system is the more expensive high-performance system which comes in a cabinet or a standard RETMA rack mount. One such system features up to 256 single-ended or 128 differential-input analog channels together with 12-bit resolution and a 250-kHz scanning rate (**Fig 6**).

High-performance systems, such as this one, feature many performance options which can be selected by the user for a particular application. Using plug-in circuit cards achieves various options. For example, the number of analog channels can be chosen in 32 channel increments from 32 to 256 channels and, with an additional rack housing, up to 512 are available.

Simultaneous sample-hold channels permit sampling a number of different channels at the same instant for conversion into digital form. The resultant digitized words then represent the parameters of a process at a specific instant of time – a feature that requires one sample-hold/analog channel and ideal for analyzing realtime dynamic events.

Another useful option in this type of system is up to 32 D/A output analog channels for system control applications. The system can thus close the loop between a computer and a process which is being controlled.

The system, incorporating convenient front panel controls, gives the user capability of operating either on-line or off-line. By means of toggle switches and LED lamp indicators, he has access to all data and addresses. In normal operation, however, the system is controlled by the host computer, which can externally supply random addressing commands or operate from internally-sequenced addresses in the sequential addressing mode.

This data acquisition system employs a high-speed, 12-bit A/D converter (2 μs) together with a fast sample-hold, analog multiplexer, data output register and gatable buffer. To achieve the high scanning rate requires not only fast analog circuits, but also the previously-described overlapped conversion technique.

Frequently used with an interface/controller board which plugs directly into the host computer and interfaces it to the system, the system can be operated in DMA, inter-

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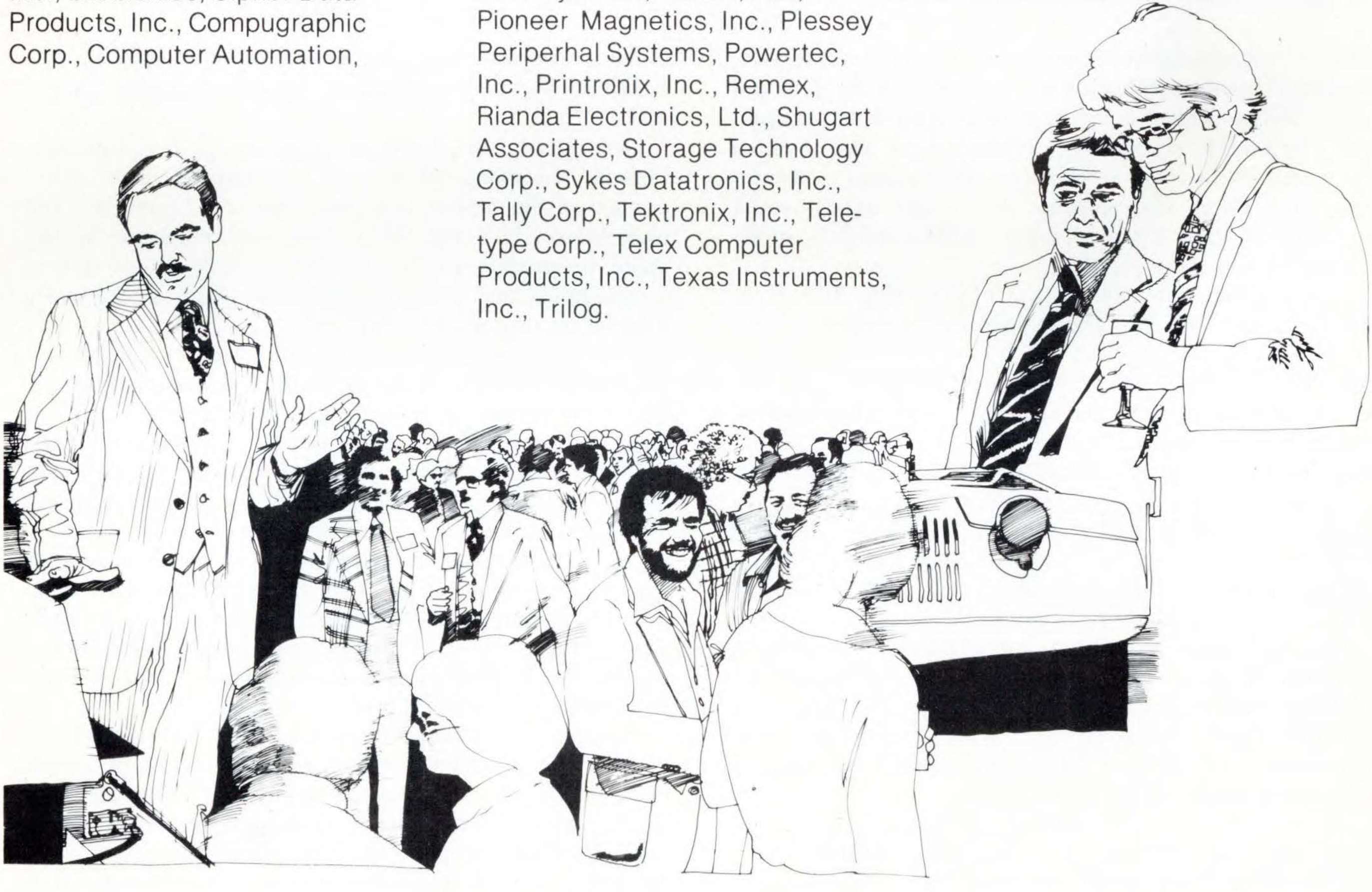

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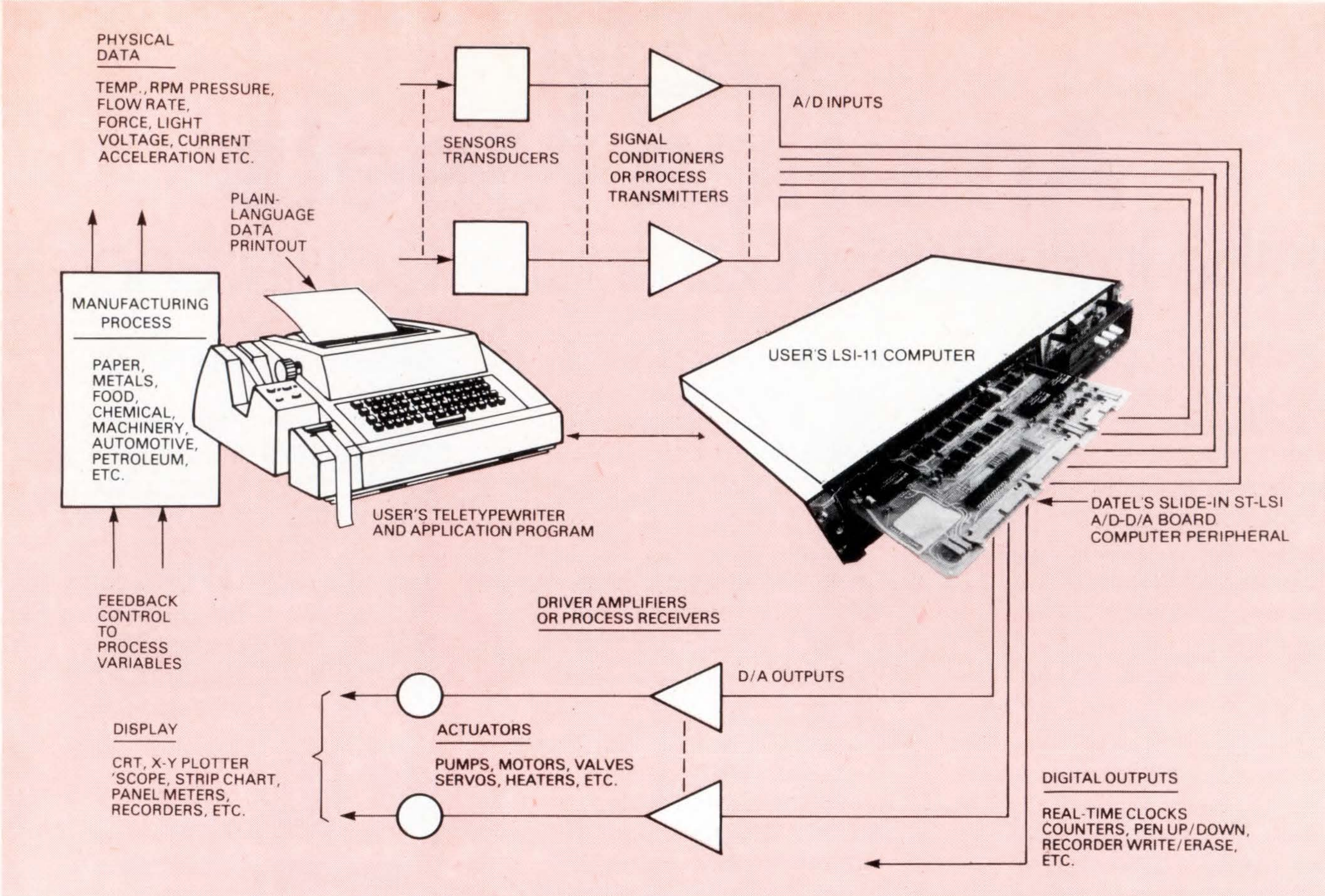

Fig 8 Microcomputer systems application of an analog I/O board.

rupt or program control modes. At the computer interface, the digital mode commands are latched and the data and digital status outputs are gatable onto open-collector computer buses. The device-select inputs can be used to share the system with other devices on a multiplexed computer data bus. Here, two separate 16-bit I/O words would normally be used for data input, address outputs, mode commands and status inputs.

The interface connection to a PDP-11 (**Fig 7**) uses an interface/controller and other plug-in circuit cards.

Analog I/O board data acquisition systems

As a final example of a data acquisition system application, new systems known as computer analog I/O boards have become quite popular in the last couple of years. Since the computer interface to a data acquisition system is always a major problem, a logical solution is to design the data acquisition system onto a board that plugs directly into the minicomputer or μC housing. Thus, such a board contains all necessary computer interfacing logic.

For many data acquisition system requirements, this is obviously the most convenient way to go, particularly for moderate performance systems. Since required interface/controller logic is taken care of, the user simply selects one of a number of different I/O boards which have features most nearly matching his requirement.

These boards are each dedicated to a specific computer family and are mechanically compatible with the computer's circuit board guides, bus compatible with the backplane electrical pinout and software-compatible with the computer's assembly language and higher-level programs. Thus, the analog I/O board appears to the computer as either a register-addressable peripheral I/O device or as a reserved portion of memory (memory-mapped peripheral).

The concept of placing the ADC and DAC components "inside" the computer was not practical before the development of the modern high-performance, 12-bit hybrid and monolithic ADCs and DACs. These new miniature devices make it possible to include ADCs, analog multiplexers, sample-holds, and DACs together with required interfacing logic all on a compact circuit card.

This new concept immediately solves two major application problems which have hampered low-cost data acquisition designs for years. First, it relieves the user of risky, tedious interface circuit design by offering a proven production design. Second, it eliminates the expensive digital cabling required for connecting to external A/D and D/A components. Only analog signal cabling is required.

Further, in many cases the analog I/O board comes with diagnostic software in assembly language on a paper tape, permitting convenient teletypewriter entry into the computer. This permits the analog input signals to be printed out on the TTY as soon as the signals are connected and the diagnostic program is loaded.

An important new application area for such a system is in distributed processing, whereby on-line factory personnel using a local control computer can closely monitor and control the manufacturing process they are responsible for. The existing central computer can still retain the observation of all plant processes by communicating through remote interface-controllers at the process site. A μC-operated process control system is illustrated in **Fig 8**.

A μC analog I/O board (**Fig 9**) data acquisition system,

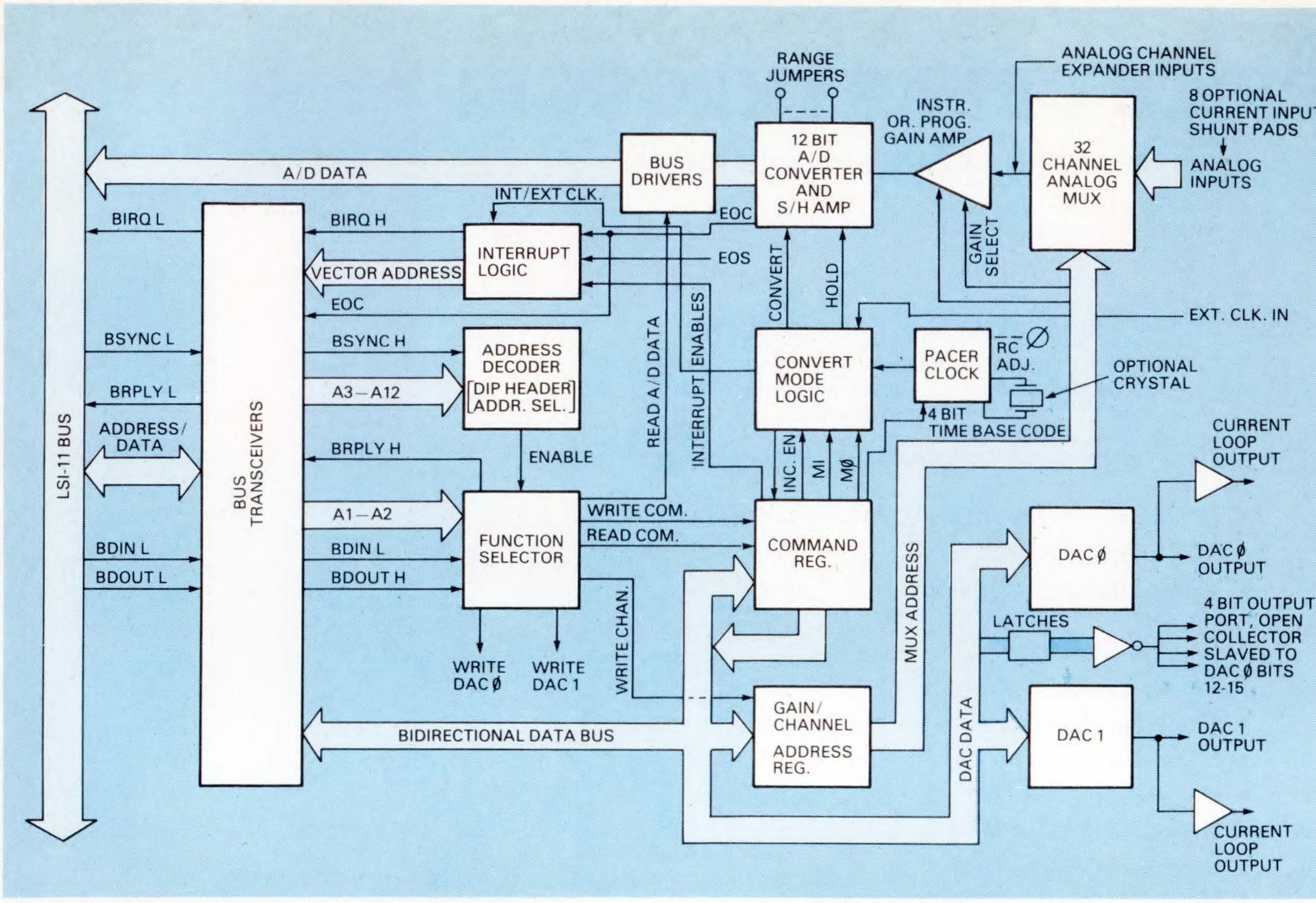

Fig 9 Block diagram of a microcomputer analog I/O board.

designed to directly interface with DEC's LSI-11 series, not only incorporates a 32-channel, 12-bit data acquisition system, but also a 2-channel 12-bit data distribution system. By using two additional boards, A/D channels can be expanded to 64, and additional D/A channels can also be accommodated.

A unique feature of this system is that it incorporates either an instrumentation amplifier or programmable-gain amplifier ahead of the sample-hold and ADC. In the case of the instrumentation amplifier, desired gain is set for all analog channels. However, with the programmable-gain amplifier, gain can be programmed for each individual channel.

High-channel density is achieved on analog I/O boards by using high-performance microelectronic ADCs and DACs together with monolithic analog multiplexers. In one system **(Fig 11)**, the miniature ADC actually has its own sample-hold built in. The ADC uses a fast successive-approximation technique to achieve 12-bit resolution. The microelectronic DACs used on board incorporate their own latching input registers and have an external current loop amplifier for directly driving process control-current loops of 4 to 20 mA or 1 to 5 mA.

The system incorporates a versatile Pacer clock, interrupt circuit and buffered digital outputs. A 4-bit CPU code selects one-of-16 Pacer time bases from 1 sec. down to 30.6 μs. The sequence of operation is commanded by either program instructions, on-board or external Pacer clock, or an interrupt triggered from either the Pacer or an external command.

The 12-bit, binary-output data is routed through on-board interface logic and placed on the LSI-11 data bus under control processor control. The A/D output briefly passes through the CPU and is usually sent to memory according to the stored program. Depending on how the A/D data will be used, the data may be manipulated arithmetically and/or sent to a peripheral device such as a teletypewriter or CRT terminal, magnetic tape, floppy disc mass storage device, or to a communications link for transmission to a remote supervisory processor.

After arithmetic, the modified data may also be returned to the physical process from which it was measured in order to control that process. If a process activator is used, it is controlled by an analog voltage or current signal from the I/O board D/A outputs. In this way the μC acts as a closed-loop controller using a D/A output dedicated to each A/D input channel. Analog indicating output devices such as oscilloscopes, X-Y plotters, chart recorders, and meters can also be accessed through the D/A outputs.

Most analog I/O boards incorporate hardware functions which relieve software requirements for highest speed and easiest programming. The boards incorporate features such as autostart, auto-sequencing of channel addressing, on-board start and DMA clocks, and end of scan/end of conversion interrupt logic to simplify programming.

The above description is about one specific type of analog I/O board. There are currently a large number of these useful data acquisition boards available from several different manufacturers. They are available for most of the popular minicomputers and microcomputers.

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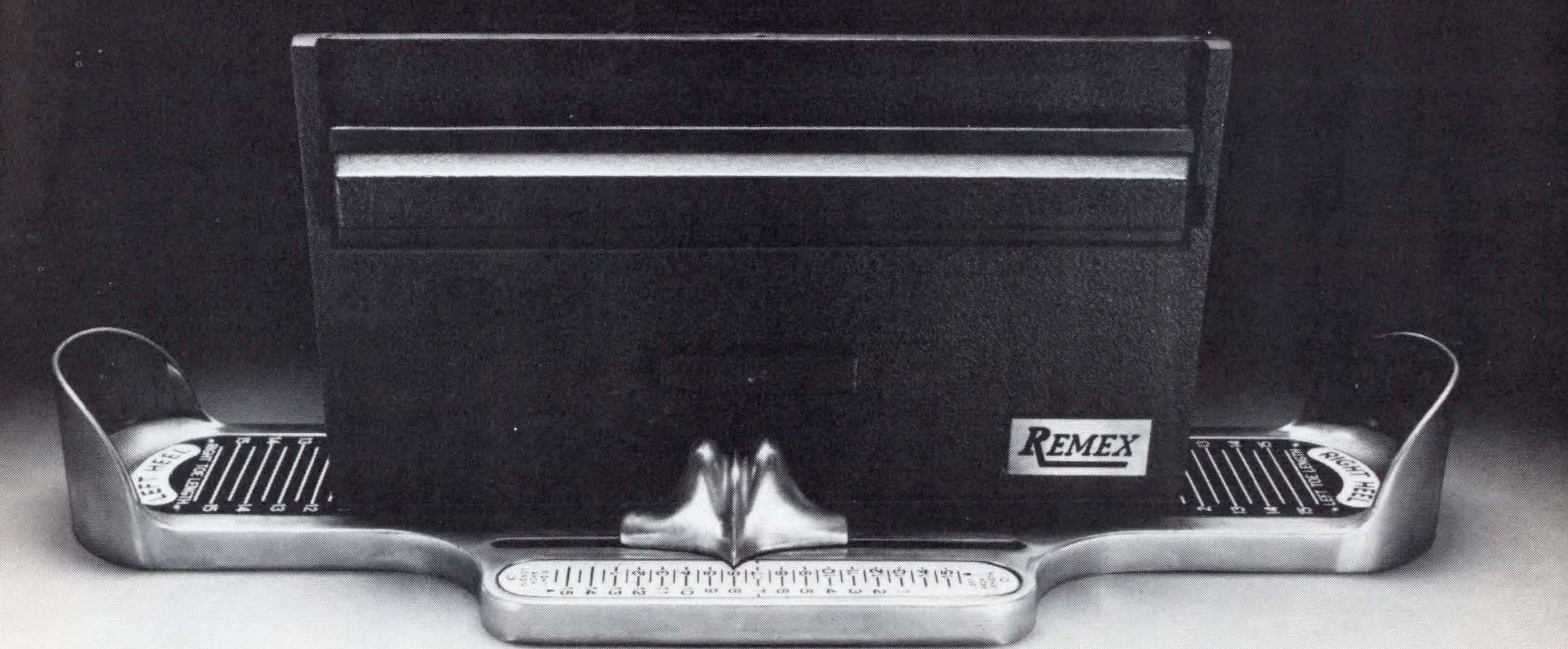

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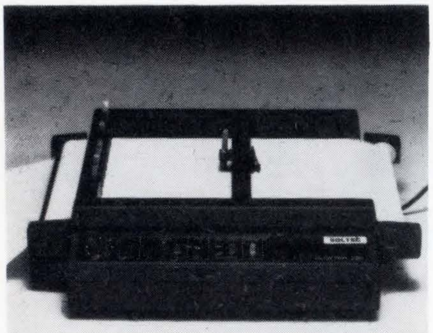
New Products

NEW DIGITAL COLOR PLOTTER This digital plotter provides graphic representation with 8 different-color pens. A Z-80 μP is the center of intelligence for Model 281 and controls the dynamics of the system. Firmware



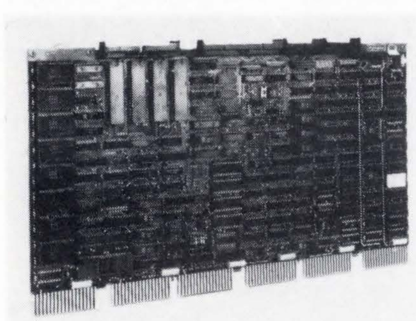
features include circle interpolation, character plotting, generation of axes and grids, various line types, window plotting and off-scale data handling. Other features include internal self testing, character plotting in 5 fonts, automatic or interactive point digitizing, programmable offsets and programmable limits. Access of any point within the plotting area is reached by an extrememly high positioning servo system at speeds up to 1 m/s. Interfaces include a choice of serial RS 232 C/V.24 and 20 mA with automatic generation of offline control signals and the IEEE 488 interface. **Soltec Corp.**, 11684 Pendleton St., Sun Valley, CA 91352. **Circle 289**

MINI-WINI Model D8000 8″ Winchester replaces 5 MB 8″ floppy systems. It is a sealed, screened-environment device with 2 platters, 4 heads data separator, company-guaranteed MTBF of 25 khrs, capacity of 20 MB – which will be increased to 40 MB as thin-film-technology capabilities double. It retains the same physical dimensions, same mounting scheme and voltage requirements as floppies. With a 6801, it creates a bi-directional bus interface and allows the drive to perform many diagnostic routines w/o the help of the CPU. **Pertec Computer Corp.**, 9600 Irondale, Chatsworth, CA 91311. **Circle 219**

DISK UTILITY PROGRAM transmits data between PDP-11 and Intel MDS systems. Operating on PDP-11s and LSI-11s, Ipex reads and writes single density diskettes in standard Intel file and record formats, using DEC RX01 and RX02 diskette drives. The program provides the capabilities to transfer files between standard DEC peripheral and ISIS-format diskette. Additional capabilities include directory listing and file deletions. Ipex facilitates the use of cross assemblers/compilers operating on PDP-11 systems. Medium and large scale applications programs can be assembled or compiled on an-11 system and the resulting binaries coupled to diskette for transfer to an MDS. In addition, source programs written to Intel Fortran-77 or PL/M language specifications can be developed and maintained on an-11 system and downloaded via diskette for compilation. Ipex is coded in Macro-11 assembly language and operates under all DEC operating systems. Perpetual license fees are $2500, including documentation and first year maintenance. **Virtual Systems, Inc.**, 1500 Newell Ave., Suite 406, Walnut Creek, CA 94596. **Circle 238**

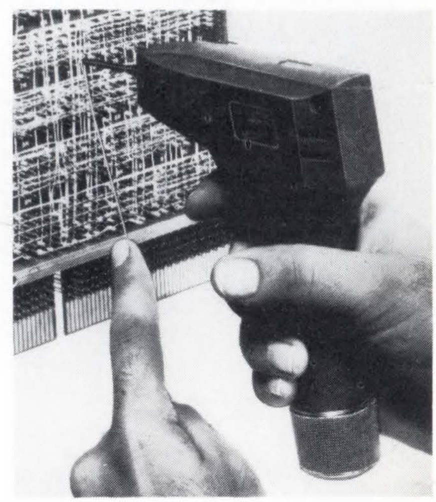
80 CHAR. X 25 L. VDT. These low-cost, μP-controlled CRT visual displays provide: U&L case characters, with 80 char. x 25 lines, 28 switch-selectable features, etc. **TEC, Inc.**, 2727 N. Fairview Ave., Tucson, AZ 85705. **Circle 212**

INTELLIGENT DISK ADAPTER/SUBSYSTEM New intelligent disk controllers provide up to 5.4 billion bytes of storage for users of DEC Unibus and Q-bus families of processors. Model 650 is completely resident on a single 8-1/2″ x 15″ printed circuit board which plugs into any available "Hex" SPC I/O slot in the host computer backplane. Model 550 resides on two 8-1/2″ x 10″ PC boards. Models 650



and 550 both emulate the RM02/3, RP04/5/6, RK06/7, RP02/3, RS03 and RS04 offered by DEC. The new models provide total software and media compatibility when used with disk drives that have the popular "storage module" interface, such as the CDC 9762. Specifications for Models 650 and 550 include: Full emulation and media compatibility; transfer to 64K without additional latency; three sector buffer storage; and ECC error detection and correction. Capability of handling overlapped seeks, and dual port disk drives is the result of bipolar bit slice microprocessor control. DMA, throttle control, built-in two drive control (expandable to eight), power-up self test, single Unibus and Q-bus load are all standard. Models 650 and 550 Storage Module Disk Emulating Adapter are $4,995 each. Delivery is 30-45 days ARO. **Xylogics, Inc.**, 42 Third Ave., Burlington, MA 01803. **Circle 286**

LOW-PRICED WIRE WRAPPER The new BW-2630 is a battery powered wire-wrapping tool priced at $19.75. It operates on 2 standard "C" size NiCad



batteries (not included) and accepts either of two specially designed bits. Bit model BT-30 is for wrapping 30 AWG wire onto .025″ square pins; BT-2628 wraps 26-28 AWG wire. Both bits produce the preferred "modified" wrap and are priced at $3.95 and $7.95 respectively. Designed for the serious amateur, BW-2630 includes positive indexing as well as anti-overwrapping mechanisms. Pistol grip design. **O.K. Machine and Tool Corp.**, 3455 Conner St., Bronx, NY 10475. **Circle 298**

IMAGE PROCESSING. Model 70 performs, in real-time, arithmetic and computations at 10 million arithmetic operations/sec. It processes images at 100 ns/pixel. Intensity manipulation, scroll, zoom, and roam are integral. Extensive library of software. **International Imaging Systems Div., Stanford Technology Corp.**, 650 N. Mary Ave., Sunnyvale, CA 94086. **Circle 214**

New Products

MULTIPLE PRECISION ARITHMETIC. Plugging in the MATH-I ROM provides routines for both 32-bit long integer and 64-bit floating point add, subtract, multiply, divide, modulo and normalize. The code is reentrant and relocatable so that it can appear anywhere in memory space. MATH-I is supplied in a 2708 EROM and is intended for use in any of the 16 sockets on the Wintek 16-byte ROM Module. **Wintek Corp.**, 902 N. 9th St., Lafayette, IN 47904. **Circle 203**

DISK CONTROLLERS. This family of intelligent disk controllers includes: Model 410 SBC/Multibus Cartridge Disk Controller, 510 LSI-11 Cartridge Disk Controller, 610 PDP-11, Cartridge Disk Controller, 810 Nova/Eclipse Cartridge Disk Controller, 211 PDP-11 Storage Module Disk Controller, 850 Nova/Eclipse Storage Module Disk Controller. **Xylogics, Inc.**, 42 Third Ave., Burlington, MA. **Circle 207**

GRAPHICS SYSTEM CAT-100 will digitize inputs in 16.7 ms with 256-1280 pt/line resolutions. It buffers the data in its own 32K-byte memory (expandable to 256K) and displays the digital image on a standard B&W or color TV monitor. $1450. **Digital Graphic Systems**, 595 Matadero Ave., Palo Alto, CA 94306. **Circle 208**

DIRECT CONNECT MODEM PLUGS INTO STANDARD TELEPHONE JACK A direct connect modem (2400 bps) which is both Bell 201B/C and CCITT compatible is available from Racal-Vadic. The VA2440 can be connected to a switched network by merely plugging into a standard RJ-11C voice jack, or through programmable

data jacks (RJ-41S and RJ-455). The VA2440 features a switch-selectable 75 bps and 150 bps reverse channel which can also operate as an auxiliary and forward channel. An extensive interface display coupled with local (analog) loopback and forced "Request to Send" (RTS) can isolate a problem on the network. In addition, Racal-Vadic operates five regional diagnostic centers, staffed by engineers and technicians trained in modems, terminals, telephone systems, front ends and computers. Mounting can be done from a single channel to 80 channels in a single cabinet. The VA2440 is $575 in single quantity. OEM discounts are available. Delivery is 60 to 90 days ARO. **Racal-Vadic** 222 Caspian Dr., Sunnyvale, CA 94086. **Circle 288**

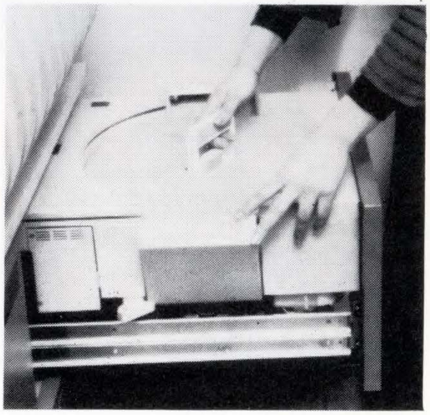
IC INSERTION/EXTRACTION KIT makes it easy and *safe* to insert/extract CMOS. The complete kit (WK-7) is $29.95, but may be purchased individually. MOS/CMOS inserters include: MOS-1416, 14-16 pins; MOS-2428, 24-28 pins; MOS-40, 36-40 pins (ea. at $7.95). MOS/CMOS extractors include: EX-1, 14-16 pins ($1.49) and EX-2, 24-40 pins ($7.95). **OK Machine & Tool Corp**, 3455 Conner St, Bronx, NY 10475. **Circle 161**

DIGITAL LOGIC PROBE. PRB-1 is compatible with DTL, TTL, CMOS, MOS and μPs using a 4 to 15V power supply. Thresholds automatically programmed. Automatic resetting memory. No adjustment required. Visual indication of logic levels, using LED's to show high, low, bad level or open circuit logic and pulses. Sophisticated, shirt pocket portable (protective tip cap and removable coil cord). $36.95. **OK Machine & Tool Corp.**, 3455 Conner St., Bronx, NY 10475. **Circle 213**

RASTER SCAN GRAPHICS. This system offers: full refresh, flicker-free, raster scan display with (1) up to 1280 x 1024 pixels in 16-levels of gray-scale, (2) display 1024 simultaneous colors from color look-up table and (3) up to 16 bits of intensity or overlay data/pixel. It has interfaces for most minis. As for its Gamma-corrected and composite video output high-speed, variable image processing, it offers: (1) pixel update as fast as 45 ns/pixel, (2) random and sequential update, (3) dynamic memory allocation, (4) writeable control store. **Lexidata Corp.**, 215 Middlesex Tpke., Burlington, MA 01803. **Circle 215**

APL MANUAL. "SHARP APL Reference Manual", by Paul Berry, is the first complete manual to cover all aspects of SHARP APL implementation – a source of information for casual APL users and professional programmers. Features such as direct file access, report formatting, batch APL and even trapping are reviewed in depth. Topics include: syntax APL, APL primitive functions & operations, workspace environment, structure data, shared variables, event trapping, system functions for function definition and line editing. 349 pgg. $18. **I. P. Sharp Associates Ltd.**, 145 King St. West, Toronto, Ontario M5H 1J8, Canada. **Circle 234**

TWO NEW TOP-LOADING DISK CARTRIDGES For specific drive applications. The 933/1-48 disk cartridge is designed for Data Point 9374 drives and Wangco T2422 drives with 48 sectors. The 933/1-24 cartridge has 24 sectors and is designed for Data General 6070 drives. Capacity



per cartridge is 10 mb. Both single-disk cartridges have 3M's "Crashguard" protective disk coating, which reduces the possiblity of damage to disk surface or to read/write heads because of headcrash. Department DR9-4, **3M**, Box 33600, St. Paul, MN 55133. **Circle 290**

THREE NEW POWER SUPPLIES Three new higher output models of convection-cooled power supplies are offered to users with high power requirements. Catalog designations for the new power supplies mirror the power ratings of each model. The MG12-43 is rated at 12 volts, 43 amps; the MG15-34 is rated at 15 volts, 34 amps; and MG24-21 is rated at 24 volts, 21 amps. Each unit is priced at $630 in quantities of 1-9 units; volume discounts available. Output voltage regulation of all three models is 0.1% maximum for a worst case combination of 0-100% load change and ±10% line change. Ripple is rated at 10mV RMS and 50mV peak-to-peak (30MHz bandwidth). Overload protection is constant current, set at 110% ±5% full load. Over-voltage protection is set between 115% and 125% for the 12 volt MG12-43 and between 110% and 120% for the 15 volt MG15-34 and the 24 volt MG24-21. All three models operate within an ambient temperature range of –10°C to +70°C (derating from 50°C at 2-1/2%/°C). All three units meet requirements of UL478, VDE 0804 and VDE 0875 "N" and can provide 28ms hold-up (whole cycle) with up to 8% margin on the input voltage. **Gould Inc.**, Electronic Power Supply Division, PO Box 6050, El Monte, CA 91731. **Circle 125**

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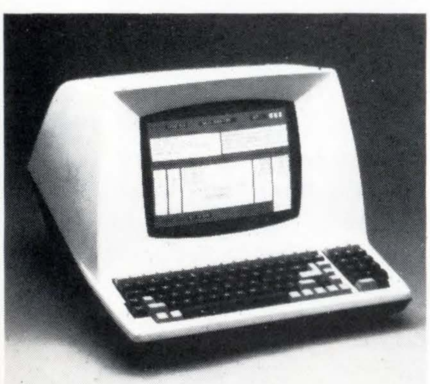
New Products

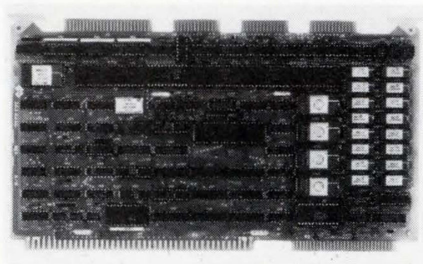
LOW-COST, MULTI-FEATURED CRT TERMINALS Four smart, µP-controlled CRT terminals, all in the $1M range and with added standard features are being marketed by Tele-Video. Included as standard in all models are: u/l case, printer/extension port, imbedded numeric pad, remote computer control, selectable transmission rates from 75-9,600 baud, and other editing and special functions. A serial RS232C communications interface and 20 mA current loop are also standard. The four terminal models are 912B, 912C, 920B and 920C. The 920 models offer 11 special function keys, 6 editing keys, and 2 transmission keys, all in an additional row on the keyboard. The keyboards are teletype-style in the "B" models, and typewriter-style in the "C" models. A second page of memory is optional with all models. The terminals' non-glare, 12-inch diagonal CRT screens provide 12x10 dot matrix resolution and dual intensity for 1920 characters A full 96-character ASCII set is displayed, in a 24-line by 80-characters/line format. Other features include switch-selectable parity (odd, even, mark, or space) and a 240-character input buffer. The overall design of the terminals is modular, with separate modules for the CRT, the video board, the logic and control board, the keyboard, and the power supply. The



logic and control module is µP-controlled. Single-quantity prices are 912B, $875; 912C, $950; 920B, $945; and the 920C, $1030. Optional second page memory is $80. **TeleVideo, Inc.,** 3190 Corondo Dr., Santa Clara, CA 95051. **Circle 282**

DESIGNERS' PR. "Public Relations for the Design Professional" by Gerre Jones examines the process from conception and research to planning and implementation in the electronics and computer field. 278 pp. $18.50. **McGraw-Hill Book Co.,** 1221 Ave. of the Americas, New York, NY 10020. **Circle 294**

NEW SINGLE-BOARD µC The new MSC 8007 features three serial ports and one parallel port to meet the majority of today's I/O requirements. The MSC 8007 is a Z80 based microcomputer designed for applications requiring two or more independent serial ports. The fully MULTIBUS compatible µC offers OEM designers a flexible single board computer with extensive on-board memory capabilities and I/O



resources. The new unit can reduce the number of boards from three or more to a single board, which has the computing power of the 4 MHz Z80A, enhanced by an optional Am9511 or Am9512 Arithmetic Processing Unit. Single piece price for an MSC 8007 with 16K bytes dynamic RAM, three serial I/O ports, and 24 lines programmable parallel I/O is $1250.00. **Monolithic Systems Corp.** 14 Inverness Dr. East, Englewood, CO 80112. **Circle 299**

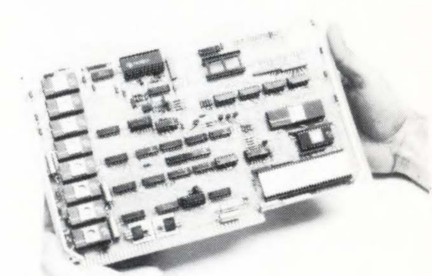
"COMPUTERIST'S DATABOOK/ Dictionary" (No. 1069) by Clayton Hallmark includes conversion formulas, octal-decimal tables, no. systems and codes, logic symbols and engineering units, number related codes, flow chart symbols, and a dictionary of the most frequently used terms, plus explanations of abbreviations and acronyms. Specific data on MC6800 and 8080A. 96 pgg. $3.95 (paperback). **Tab Books,** Blue Ridge Summit, PA 17214. **Circle 220**

NEW GRAPHICS PACKAGE FOR VAX 11/780. A new software system, the MGS-7F, supports the use of Megatek's Whizzard 7000 graphics display unit with VAX computers operating under the VMS operating system. The package has fully buffered DMA transfer capabilities which permit transfer of graphic data using either programmed I/O or DMA modes. Both methods operate transparently. Greatly increased speed, is claimed, at which data can be added to the display memory of the 7000 unit. The software package consists of a series of FORTRAN callable routines as well as a set of driver routines programmed in Assembly language for each computer and operating system with which the displays are used. **Megatek Corporation,** 3931 Sorrento Valley Blvd., San Diego, CA 92121. **Circle 296**

"NET/ALERT" SYSTEM provides operations managers real-time, on-line information about the performance of every terminal on every line in their telecommunications network – and displays it on a large-screen color graphics CRT. NET/ALERT allows operations personnel to track current status of the entire telecommunications system, a group of applications, a single application, pinpoint the status of an individual line within a specific line group, and the status of each terminal on a single line. **Avant-Garde Computing, Inc.,** 21 Olney Ave., Cherry Hill, NJ 08003. **Circle 229**

COS/MOS SEMIS. A 440-pg. databook on "COS/MOS Memories, µPs and Support Systems," SSD-260, includes technical data on the CDP1800, MWS-5000, CD4000, CDP18S600 and CDP-18S000 series. $7. **RCA Solid State Division,** Box 3200, Somerville, NJ 08876. **Circle 295**

SPEECH SYNTHESIZER MODULE The TM990/306 module offers a basic industrial vocabulary of over 160 words which can be combined to construct sentences that have a human but relatively flat inflection. This speech synthesizer module is fully compatible with other TM990 microcomputer modules and can be used in industrial control applications, for example, as a learning aid to prompt trainees in correct procedures or to alert operators of conditions requiring maintenance or attention. An on-board amplifier is capable of driving an 8-ohm speaker with a 2.5-watt output. For more output power, users can connect an external amplifier to the pre-amplifier output of the speech synthesizer module. Two modes of operation are possible. In the polled-status mode, the host CPU issues addresses of a word, sets the talk command, and polls the status bit to determine when the word has been spoken. Delays between words and sentences are inserted by addressing the particular delay word which is processed as if the delay was, itself, just another word.



$1,280 in quantities of one. Production availability begins in first quarter 1980. **Texas Instruments Inc.,** Inquiry Answering Service, PO Box 1443, MS-6404, Houston, TX 77001. **Circle 287**

NEW VECTOR GENERATOR A fast, powerful 2-Dimensional Vector Generator is now available for Aydin's Model 5216 Display Computer. This device permits vector generation at 800 ns per pixel, plus 8 μs average set-up time. In addition to high speed vector generation, the option permits hardware window clipping, conversion from a World Coordinate System with 64K x 64K to a 512 x 512 or 1024 x 1024 pixel screen format, with translation, rotation and scaling of 2-Dimensional data. $5K. Available: February 1980. **Aydin Controls,** 414 Commerce Dr., Fort Washington, PA 19034. **Circle 283**

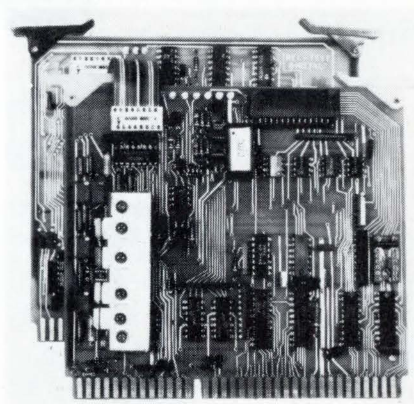
SMALL ALPHANUMERIC PRINTER PRINTS 21 COLUMNS This new printer, Model 0533, will print 21 columns of alphanumeric information on standard 3-7/16″ wide plain paper tape. The bar matrix printer can produce multiple copies, in two colors. A

snap-in ribbon cartridge permits fast, easy replacement. The unit measures 13-1/2″ x 6-1/2″ x 6-7/8″. It contains its own power supply and an ASCII compatible interface controller to perform all printer functions. Continuous print speed is 90 lpm with rapid line feed control that slews paper up to 10 lps. A take-up mechanism for rewinding label stock or audit copy is optional. Typical applications include electronic scales and weighing systems, POS terminals, receipt printing for fuel dispensing, label printing, and as a printer option for general instrumentation. $495. OEM discounts are available. Delivery, 8-10 weeks ARO. Sodeco Div., **Landis & Gyr, Inc.,** 4 Westchester Plaza, Elmsford, NY 10523. **Circle 281**

A TRIPLE MODEM This new series of triple modems is specifically designed for remote terminal use. The VA3450 series includes six switched network originate/answer models, all of which have been registered for direct connect under Part 68 of the FCC Rules. In addition, there is an originate or answer for leased line applications. A VA3450 at the remote terminal can call three different types of modems, a

212A, a 103, or a VA3400, with automatic identification of the called modem. The VA3450 series incorporates special diagnostics; such as Idle Test, Analog Loopback & Busy Out, Digital Loopback, and Self-Test. In addition, the modems have a switch-controlled "Standard Option" mode which forces the unit into a standard configuration to simplify and speed up diagnostic testing. Prices for the VA3451 (212A, 103 and VA3400) start at $900. The VA3452 (212A and VA3400) is priced at $850. The VA3453 (103 and VA3400) is $825. Delivery is 60 days ARO. **Racal-Vadic** 222 Caspian Dr., Sunnyvale, CA 94086. **Circle 297**

NEW PROM PROGRAMMING CARD A program card which fits all Data I/O PROM programmer Models 1, 2, 3, 5, 7, 9, 17 and 19 is now available. Now only one programming card set is required for NMOS PROMS – SuperMOS. The new program card features on-board CPU including built-in diagnostics. The card set easily fits into existing Data I/O PROM programmers and provides the latest programming techniques. Present socket adapters can be used. Only one Super MOS card



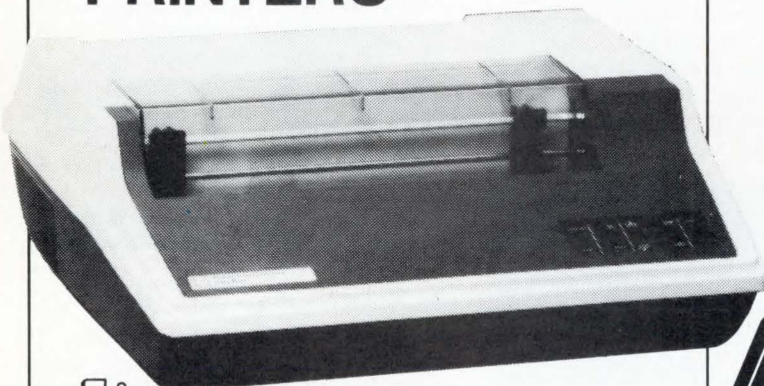
set is required for all N-channel EPROMS including the newer 32K types. Basic operation of the PROM programmer remains unchanged and can be used by present operators with no additional training needed. $895. **E-H International, Inc.,** 7303 Edgewater Dr., Oakland, CA 94621. **Circle 285**

DISK SYSTEMS

Shugart

apple

PRINTERS



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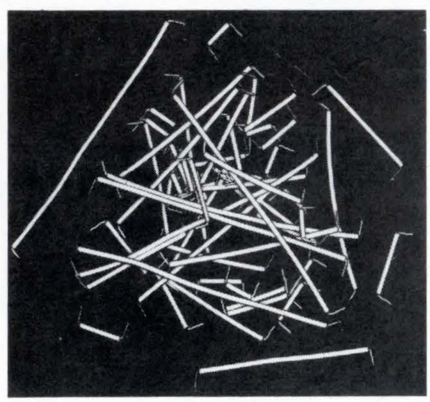
New Products

EPROM WITH 64K AND 24-PINS The MCM68764, Motorola's new EPROM, has 64K, uses single 5V supply and is in standard 24-pin ROM package. The use of a 24-pin package (rather than 28) was made possible by placing a dual function on pin 20. During programming it handles the 25V programming pulses and in read operation it is the chip enable. The MCM68764 has a 450 ns access time, will dissipate less than 880 mW in the active mode and less than 140 mW in the standby mode. Price of each in 100s is $164. Another EPROM, the MCM68A764, has 350 ns access time and is priced at $196 each in 100s. Both are available in sample quantities. **Motorola Inc.**, MOS IC Division, 3501 Ed Bluestein Blvd., Austin, TX 78721. **Circle 280**

BOOST IN 8086 μP PERFORMANCE Two developments by Intel are claimed to extend the performance range of μPs by 50 percent or more. The first is a fast CPU, the 8086-2, for the MCS-86 family. The second is an EPROM, the 2732A, that is twice as fast as previous EPROMs. The 8 MHz 8086-2 16-bit μP, utilizes HMOS II technology to upgrade the performance of the CPU by 60 percent while maintaining total software compatibility with existing applications. Intel expects new applications to be opened in telecommunications equipment (such as digital telephone switching), data processing (such as intelligent terminals), business equipment (such as word processing), and real-time process control. The new 2732A 32kb EPROM is a fourth-generation design based on Intel's HMOS-E technology. The EPROM operates at maximum access times down to 200 ns. In contrast, 450 nanoseconds is the industry standard speed for high-density EPROMs, which are generally used to store microprocessor programs. Total system support is also available for the 8086-2 since all bipolar bus support, LSI peripheral, and dynamic and static memory devices usable with the standard 5 MHz 8086 can also be used with the 8 MHz version. Additionally, the recently introduced 8089 I/O processor can be used in 8086-2 systems to increase the input-output capabilities significantly. The 8089 acts as a coprocessor in the system, executing input-output programs concurrently with the 8086 execution of the main program. For program storage, the 8086-2 can use the new 2732A EPROM, the third-generation 2716 16kb, and 2732 32 kb EPROMs, and interchangeable mask-programmed ROMs. At 200 nanoseconds access time, the 2732A is faster than typical 8086-2 applications require. (Memory devices with 250 ns access times were used without wait states in benchmark studies.) However, the extra speed may be needed in some large system applications. The new EPROM can be programmed with the Intellec system's universal PROM programmer and UPP 833 personality card or with standard PROM programmers. The 8086-2 is available now and can be ordered in volume immediately. $200 ea. in quantities of 100. The 200 ns 2732A EPROM is $570. A 250 ns version is offered at $475. These devices are available in limited quantities for customer sampling. **Intel Corp.**, 3065 Bowers Ave., Santa Clara, CA 95051. **Circle 279**

JUMPER WIRES. New kit contains 20 AWG (0,8mm) RW-50 jumper wires that are precut and turned 90° at both ends allowing easy insertion in breadboarding modules. Jumpers are Kynar insulated and prestripped .250″ on each end. These jumper wires replace cutting, stripping and bending wires for interconnecting components in both solderless and soldered proto-



types or laboratory applications. Offered 50 per package in assorted lengths from 1/2″ to 4″. RW-50 is priced at $2.95. In stock at local electronics dealers or directly from **O.K. Machine and Tool Corp.**, 3455 Conner St., Bronx, NY 10475. **Circle 64**

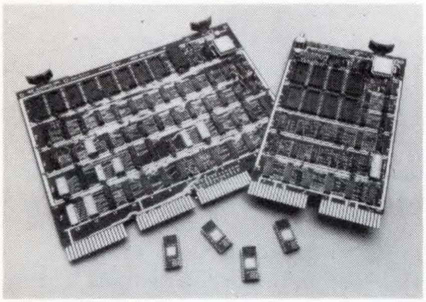
PDP-11 MAGTAPE CONTROLLER. The TC-130 provides mixed density (1600 bpi PE and 800, 556, 200 bpi NRZ) and a software-compatible, embedded design. It permits an intermix of 9- and 7-track, up to 8 drives. The dual-speed switch-selectable (12.5 to 125 ips) TC-130 fits all PDP-11s. **Wespercorp,** 1100 Claudina Pl., Anaheim, CA 92805. **Circle 274**

NEW μP CONTROLLED TAPE BACK-UP A new microprocessor-controlled one-half-inch reel-to-reel tape transport provides price-compatible back-up and archival storage for multi-platter 8-inch and 14-inch Winchester disk drives. The 6809 Data Streamer™ Transport by Kennedy operates at 100 ips using IBM and ANSI compatible 1600 cpi phase-encoding techniques. In streaming mode, the transport stores or restores 12M bytes of data in 75 seconds and 40M bytes in 250 seconds. Total unformatted capacity is 46M bytes on a 10.5 inch reel. The unit also operates at 12.5 ips in a start/stop mode to accommodate conventionally-recorded tapes. The integral formatter has all logic necessary for reading, writing and control of 1600 cpi ANSI and IBM compatible nine-track tape. It generates preamble, post-amble, file marks, and identification bursts. All timing is referenced to a quartz-crystal-controlled oscillator. In the 100 ips streaming mode, access time is 295 msec for both read and write; in the 12.5 ips start/stop mode, read access time is 44 msec and write access is 40 msec. Rewind is accomplished at 200 ips. The Data Streamer Transport has a MTBF of more than 10,000 hours; mean time to repair is 0.5 hours. The recoverable read/write errors do not exceed one-bit in 10^{10}. Voltage required is 115V at 60Hz with 100V, 50Hz or 60Hz; 220V, 50Hz; 230V, 60Hz; and, 240V, 50Hz options available. $2,500 each in OEM quantities. Delivery 60 to 90 days, ARO. **Kennedy Company** 1600 South Shamrock Ave., Monrovia, CA 91016. **Circle 277**

DATA-MONITOR DATA SHEET Halcyon's new data sheet features their 802A Data Monitor that automatically monitors and stores data for all lines up to 56K bps (full duplex), on display screen or scrolls. The data sheet illustrates the unit and describes operation, special features and preliminary specifications. Copies of this data sheet and additional information available from **Halcyon,** 2121 Zanker Road, San Jose, California 95131. **Circle 201**

BUSINESS GRAPHICS PACKAGE ZCHART III by Nicolet Zeta Corp. produces multicolor line, bar and pie charts created in an interactive session by the user's responses to simple, English-language questions. Plot description and data files are stored separately, allowing the user to run new data with an existing chart design or the same data with a different chart design. Software takes full advantage of the unique features of Zeta's microprocessor based controller. Combined with any Zeta plotter, the controller provides higher throughput and reduced operating costs. This is due to the distributed processing performed by the controller. Typically host CPU time is reduced by 50%. Available on a 30-day delivery schedule. **Nicolet Zeta Corporation,** 2300 Stanwell Dr., Concord, CA 94520. **Circle 187**

ON BOARD PROGRAMMER FOR DEC PDP-11 and LSI-11. PROM Programmer Modules with On-Board Programmer capability are designed for use with the DEC PDP-11 and LSI-11 computers. On-Board Programming permits system design engineer to blow PROM's on-line utilizing the computer in lieu of an off-line device. Results can be tested, compared and executed immediately. The MDB-MR-004 module accommodates commercially available



2716 and 2732 UV eraseable PROMs. The On-Board Programmer is switch or program selectable. It has a status register for programming write, interrupt enable, and done. The PROM, status register and vector addresses are switch selectable. Bus Request levels are selectable. The module requires one quad slot in the PDP-11 chassis. The MLSI-MRV-004 PROM Programmer Module for use with LSI-11 computers accommodates commercially available 2716 and 2758 UV eraseable PROMs. The On-Board Programmer is switch selectable, as are memory area allocations. It is a dual module requiring one-half quad slot in the chassis. MDB also offers the MR-005 PROM/RAM Module for use with PDP-11 computers. It accommodates commercially available 2704, 2708, 2716 and 2732 UV eraseable PROMs and 4118 and 4016 RAMs. Other features are the same as the LSI module; it requires one quad slot. The MLSI-MRV-005 PROM/RAM Module is available for use with LSI-11 computers to accommodate 2716 and 2732 UV eraseable PROMs and 4016 RAMs. PROM and RAM are mixable but chip addressing must match; memory allocation is strappable. It is a dual module. There are no DEC or other vendor modules of these types commercially available. PROM Programmer Module (-004) is $495 for the LSI-11 and $995 for the PDP-11. PROM/RAM modules (-005) are $225 for the LSI-11 and $575 for the PDP-11. Delivery, 30 days ARO. **MDB SYSTEMS, Inc.**, 1995 North Batavia St., Orange, CA 92665.
Circle 66

BUS CONVERTER BOARD A dual-purpose bus converter "Qniverter" by Able can be used two different ways. It can permit a PDP-11 Unibus system to access LSI-11 compatible controllers and memories. It can also permit an LSI-11, LSI-11/2, LSI-11/23, PDP-11/03 or PDP-11/23 system to access Unibus compatible controllers and memories. Qniverter supports many features of the LSI-11/23 including four-level interrupt structure, memory parity and full 256K byte addressing. It also provides for extended bus loading by making possible the addition of 19 Unibus loads to an LSI-11 system or a Q-bus drive capability to a Unibus system. The dual-purpose quad-width converter installs into a quad slot of the LSI-11 backplane and is software transparent to the host computer. Memories and controllers may reside on both the Unibus and Q-bus. $750. Delivery, 30 days ARO. **Able Computer**, 1751 Langley Ave., Irvine, CA 92714. **Circle 275**

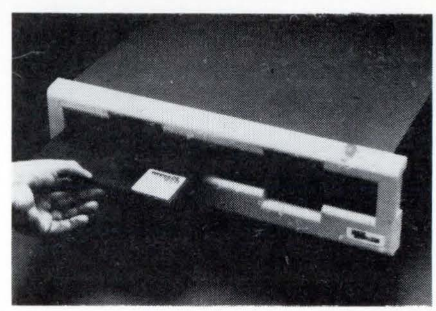
BOOKLET ON VOICE READOUT SYSTEMS A 12-page colorful brochure describing the capabilities and applications for Master Specialties seven products is now available. Design and operational specifications for the entire line of Master's telecommunications and voice readout systems are included. Each of the voice reproduction systems utilizes IC's instead of mechanical tape, eliminating wear and maintenance by eliminating moving parts. Detailed specifications are written in diagramatic form. **Master Specialties Company**, 1640 Monrovia, Costa Mesa, CA 92627. **Circle 276**

6502 ASSEMBLY LANGUAGE PROGRAMMING is the newest addition in OSBORNE/McGraw-Hill's continuing series of books on microcomputer assembly languages. This 550-pg. paperback ($9.50) includes: over 80 programming examples with standard format, including flowcharts, source programs, object code and text; • each 6502 instruction fully explained • 6502 Assembler conventions; • programming the 6502 interrupt system; and • 6502 I/O devices and interfacing methods. Other well-known μC books by Dr. Leventhal – Z80 Assembly Language Programming, 6800 Assy. Lang. Prog., 8080 Assy. Lang. Prog. (Osborne), etc. – are standard μC texts, well-known classics and are widely used throught the electronics industry. **OSBORNE/McGraw-Hill**, 630 Bancroft Way, Berkeley, CA 94710. **Circle 127**

EPROM WITH 24-PINS AND 5-VOLTS, A 64K EPROM that uses a single five-volt supply and a standard 24-pin ROM package has been introduced by Motorola. Designated MCM68764, the new EPROM preserves the ROM/EPROM package and function interchangeability of Motorola's 8K to 64K Memory series. The use of a 24-pin package (rather than 28) was accomplished by placing a dual function on pin 20. During programming it handles the 25V programming pulses and in read operation it is the chip enable. With a 450 ns access time it will dissipate less than 880 mW in the active mode and less than 140 mW in the standby mode. Unit price in quantities of 100 is $164. Another selection, the MCM-68A764, with a 350 ns access time, is priced at $196 each in lots of 100. Both numbers are available in sample quantities. **Motorola Inc., MOS IC Div.**, 3501 Ed Bluestein Blvd., Austin, TX 78721. **Circle 197**

MULTIBUS RAM BOARD Electronic Solutions offers a new 48K RAM Board product line that is fully compatible with Intel's "iSBC-80 Multibus." The RAM-048 contains 48K of Dynamic RAM and has memory access time of 450 ns. Additionally, the RAM-048 is burned in at 55°C for 168 hours prior to 16 hours of reliability testing, and has a 3-year warranty. Price is $1565 for quantity of 1-9 and $1410 for 10-24. Delivery is from stock. **Electronic Solutions, Inc.**, 5780 Chesapeake Ct., San Diego, CA 92123.
Circle 192

FLEXIBLE DISK MEMORY SYSTEM. Double sided, DEC-compatible. First system compatible with all DEC and IBM diskette formats, (including IBM double density, double sided.) The DSD 480 system R/W on both sides of industry-standard 8″ diskettes for a formatted capacity of one megabyte per diskette, or two megabytes of on-line storage. Doubles capacity of other



DEC compatible flexible disk systems, and allows DSD 480 users to conveniently transfer data and programs between DEC and IBM computers. It is possible to transfer utilities and applications programs written for IBM machines directly to DEC computers, or vice versa. Packaged in a low-profile 5¼-inch chassis for easy rack mounting or tabletop operation. Simple operation and complete documentation facilitate system integration. Delivery 30 to 45 days ARO. OEM discounts available. **Data Systems Design, Inc.**, 3130 Coronado Drive, Santa Clara, CA 95051. **Circle 69**

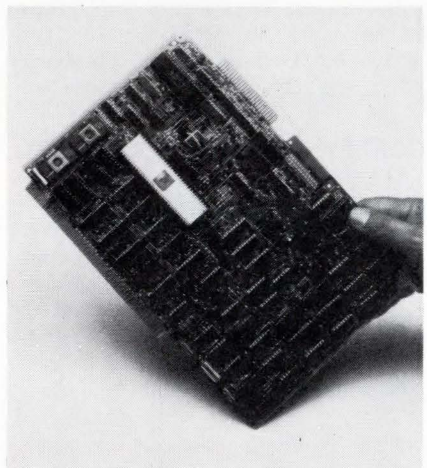
New Products

NEW COMPUTER SYSTEM This Model 8200 system is designed especially for small business and professional office environments. The system hardware includes: Z-80 microprocessor at 4 megahertz, 3 usarts, 56K RAM memory, 24 x 80 no glare video screen with inverse video, detached matching keyboard, dual floppy disk drives with 630K bytes of storage, and typewriter-quality or high-speed printer with forms tractor. Hardware options include: acoustic modem for communications over phone lines, sheet feeder for automatic feed of stationery, and a variety of other standard peripherals. The system sells for $11,995 with typewriter quality printer or $10,995 with high-speed matrix printer. Included in the price are: one software package, BASIC and ASSEMBLY languages, a designer desk, reference manuals, training, starter supplies and delivery. Delivery 2-3 wks ARO. **Compal, Inc.**, 6300 Variel Ave., Woodland Hills, CA 91604. **Circle 300**

FREE ELECTROSTATIC PLOTTING SOFTWARE A free utility plotting package is available from Houston Instrument. It will support its 8400 series of electrostatic plotters and plotter/printers when used in conjunction with EPIC I or II vector to raster converters. This software package, written in Fortran, has been specifically tailored to PDP-11 computers utilizing the RT-11 operating system. Subroutines supplied are the same as those for Houston's COMPLOT® pen plotters. Compatibility allows existing application programs currently running on the company's supplied software to run on an electrostatic plotter with a minimum of problems. It is easily adaptable to other computer systems using Fortran. For details of the software package contact Jim Raska, **Houston Instruments**, One Houston Sq., Austin, TX 78753. **Circle 278**

M6800. The 2nd vol. of the "Practical Microcomputer Programming" series addresses the problems of applications programming at assembly level. In 16 ch. and more than 100 formal examples, the fundamental techniques of assembly level programming are applied to specific problems. It covers number base conversion; table lookups; trig; subroutines and SP usage; multiplication; div; multiple precision arithmetic; generation and use of pseudo random numbers. I/O under both program and interrupt control are covered, with complete operating examples, and use of real time clock interrupt. Program debugging methods and full source text debug program are included. $21.95. **Northern Technology Books**, Box 62, Evanston, IL 60204. **Circle 292**

NEW FLOPPY-DISK CONTROLLER This new floppy-disk controller (FDC) is compatible with the TM990 series of microcomputer board products. The board, designated TM990/303, supports up to 4 double-sided drives and provides complete floppy disk mass storage capability. It is programmable by the CPU for data encoding formats and number and types of diskette



drives. It can interface to single density drives or either of the two most popular dual-density drives (FM or MFM). The controller is compatible with IBM 3740 and TI disk formats. Data transfer format and steppermotor rates are both programmable. Other features: write precompensation, 5″ or 8″ diskette compatiblity, soft sector compatibility, internal phase acquisition and address mark detection. $845. Delivery, 4 wks ARO. **Texas Instruments Inc.**, Inquiry Answering Service, P.O. Box 1433, MS 6406, Houston, TX 77001. **Circle 291**

8080/8085 ASSEMBLER. The assembler in this book, "An Editor/Assembler System For 8080/8085-Based Computers," follows the rules in "Practical Microcomputer Programming: The Intel 8080," by Weller, Schatzel and Nice. The NTA80 is assembled to use the first $1B90_{16}$ or 7056_{10} locations of memory, with the source program that is to be assembled residing in any other region of memory you like. Your own I/O routines may reside anywhere else in memory. The assembler can be used immediately with an ASR-33 or equivalent that is connected to port 0 (status) and port 1 (data). Both books are from **Northern Technology Books**, Box 62, Evanston, IL 60204. **Circle 293**

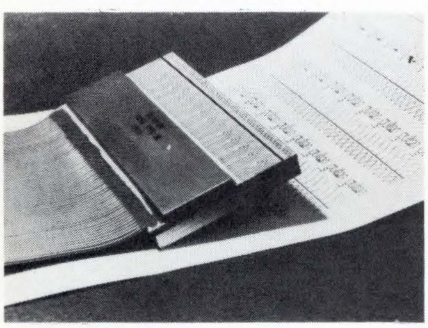
SMALLER-SIZED IC'S? A new electro-plating development gives promise that circuit boards of the near future may be smaller in size and have more, closely-packed microcircuits. Scientists at IBM's Thomas J. Watson Research Center have developed an electroplating method that uses the heat from a laser in depositing metal over microscopic areas. This offers a potentially simpler means of producing the small metal patterns that form the basis of modern electronic circuitry. Where this new approach can be applied, there would be no need for the overlaid "masks" that are used in conventional photolithographic methods of fabricating circuits. With conventional electroplating, electrons at the cathode combine with positively charged metal ions in solution to form a metal layer. Meanwhile, metal from the oppositely charged anode dissolves and supplies the solution with fresh metallic ions. This old process of metallization can now be combined with photographic and lithographic methods to define metallic and nonmetallic structures in microcircuits. With the new experimental method, a finely focused laser beam heats a small surface area on which metallic material is to be deposited, and thus enhances deposition of the metal. The researchers have succeeded in electroplating regions as small as four micrometers in diameter (one micrometer equals about 1/25,000 inch). The initial IBM work on the system was done by Robert J. von Gutfeld and Robert L. Melcher; additional contributions were made by Lubomyr Romankiw, Samuel E. Blum, and Eugene E. Tynan. **IBM's Thomas J. Watson Research Center**, P.O. Box 218, Yorktown Heights, N.Y. 10598.

VIDEO-SPEED 8-BIT MONOLITHIC CONVERTER. A mil-temp version of its 8-bit monolithic video-speed analog-to-digital converter, has been introduced by TRW LSI Products. The new product (TDC-1007J-M) is a military version of the commercial TDC-1007J, introduced in 1978. The new unit is guaranteed to operate over a case temperature range of −30 to +125°C. The TDC-1007J-M is also available tested to any of the MIL-STD-883B environmental test conditions. Designed to replace bulky discrete and hybrid circuits in high-performance military radar and image acquisition system, the TDC-1007J-M performs 30 million conversions per second while drawing only 2.5W. It utilizes a fully parallel, single chip of 20,000 closely matched bipolar components. The device is housed in a standard 64-pin DIP and weighs one-half ounce. R781. Testing to 883B specs is additional. **TRW LSI Products**, PO Box 1125, Redondo Beach, CA, 90278. **Circle 126**

GENERAL PURPOSE LOGIC MODULES include five different modules tailored for different applications users are likely to encounter. The MLSI-1710 is a General Purpose Interface Module; the MLSI-DRV11P, a Bus Foundation Module; the MLSI-11B, a General Purpose Direct Memory Interface; the MLSI-WWB1, a Universal Quad Wirewrap Module; sockets optional; and the MDB-W9501, a Universal Quad Wirewrap Module. **MDB Systems, Inc,** 1995 N. Batavia St., Orange, CA 92665. **Circle 142**

WIRE-WRAPPABLE SOCKETS. What you always wanted to know about wire-wrappable sockets – selection criteria, pros and cons of various constructions and other facts – are all included in this literature. When is dual-leaf spring action's contact redundancy needed? When should you go with gold or tin plating? When must new techniques replace traditional ones? These and more design tips are covered in this free socket brochure and IC packaging manual. **Thermionic Corp,** 445 Concord Ave, Cambridge, MA 02238. **Circle 164**

THERMAL PRINTHEADS. For high-density graphic printing, Series DM 48256/48288/69414 have corresponding dot densities of 88, 91, and 100 dots/in. across 3", 3.3" and 4.3", respectively.



High dot density is by an "interleaved" interconnect arrangement of the dot address lines. Printing speed: 5 lps of alphanumeric text, up to 0.5 ips of graphics. **Gulton Industries, Inc.,** 212 Durham Ave., Metuchen, NJ 08840. **Circle 228**

PDP-11 MODULE. Plug a UMC-Z80 into a UNIBUS SPC slot and get a total μC system to increase throughput and processing capabilities, handle protocols, terminals, network interfaces, controller emulation, data acquisition, processing and highspeed DMA transfer. Total software development system speeds programming. Memory can expand to 1M byte and it supports over 32 serial I/O lines. **Associated Computer Consultants,** 228 East Cota St, Santa Barbara, CA 93101. **Circle 172**

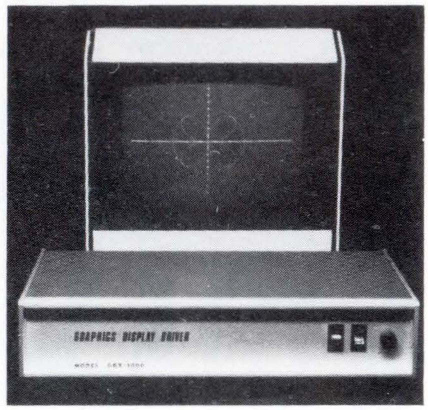
New Products

PLUG-IN DATA MONITOR 802A accomodates any data rate from 50 bps to 19.2K bps (option to 56K bps) and has a 7" CRT to display 1024 char. It has statistical error analysis, storage capacity of 64K bytes, displaying of continuous key configuration parameters, automatic turnaround-time measurement and transmitting capability for terminal polling. **Halcyon,** 2121 Zanker Rd., San Jose, CA 95131. **Circle 221**

CRT DISPLAY. With this electron-gun CRT computer terminal displays won't "bloom" at high-brightness levels. The high-density electron beam provides increased brightness up to double present peakline brightness (w/o a corresponding reduction in resolution). Operated in high-resolution CRT terminals at 60 Ft.-Lamberts w/o blooming. Screen can be viewed in direct sunlight. **Watkins-Johnson,** 3333 Hillview Ave., Palo Alto, CA 94304. **Circle 216**

PDP-11/LSI-11 CALENDAR CLOCK, TCU-100 ($495), provides month, day, hrs, min, and sec and can interrupt on date/time (or periodic intervals) for PDP-11. TCU-150 ($430) provides year, mon, day, hr, min and sec (for PDP-11), and automatic leap year. Patches for RSX-11M, RT-11 FB/SJ VO2, VO3 and UNIX. For the LSI-11/2, there's the TCU-50D ($295) to provide mon, day, min, and sec. Dual-size board. Patches for RT-11 SJ/FB VO2, VO3B. **Digital Pathways Inc.,** 4151 Middlefield Rd., Palo Alto, CA 94306. **Circle 217**

UNIVERSAL GRAPHICS DISPLAY G-Box peripheral device used with any computer adds high density graphics.



Video image output is a matrix of 512x240 dot positions with capability of expansion using larger memories. Each of the dots can be selectively set or reset. In addition, many high level commands for drawing lines and other graphic actions are automatically performed by the G-Box. $350-$2k. **Objective Design, Inc.,** Box 20325, Tallahassee, FL 32304. **Circle 232**

"MICROPROCESSOR INTERFACING TECHNIQUES" (2nd ed), by Rodney Zaks and Austin Lesea, contains useful information hard to find elsewhere. Experienced μP users won't learn much from it, but newcomers who do not want to spend a long time reinventing the pyramid will find it a useful reference book. Ch. 4 and ch. 5, devoted entirely to D/A-A/D conversion, are the heart of this book; it is on these chapters that the book should be judged. There are some surprising omissions – the 6500 and 9900, two of the most important devices, are not mentioned! (6500 users are partly catered for by references to the 6800). The section on D/Ac's ignores the existence of Analog Devices' AD6522 – one of the best μP-compatible DACs around. But, these are relatively minor faults, in what is, on the whole, a useful collection of circuits, illustrations and descriptions covering all of the important interface problems. Ch. 6 covers bus standards such as S-100, IEEE-488 and Camac, and topics such as supplies. **Sybex,** 2020 Milvia St., Berkeley, CA 94704. **Circle 193**

SYSTEM INTEGRATION. NOVA-COMPATIBLE tape controllers, more CRT ports, etc, can be added to your system. Bytronix puts together a CPU with 64K bytes of memory, disk controller, 4-port multiplexer, printer controller – a 3-board configuration in a 6-slot chassis. Or just about any other configuration. All hardware is integrated, thoroughly checked as a system and guaranteed by the same single source. Performance has been proven: 100s of systems are running successfully under various OSs (IRIS, BLIS/COBOL, MICOS, VMOS, FORTH). Simple systems delivered from stock (others within 30 days). **Bytronix**, 2751 E. Chapman Ave., Fullerton, CA 92631. **Circle 233**

PDP-11V23/PDP-11T23 use floppy-disk storage and higher-capacity hard-disk storage, respectively. Each of these high-end members for DEC's line of packaged μC systems has 2.5X the execution speed of the entry-level PDP-11/03-based packaged systems. Both are general-purpose systems. PDP-11V23 consists of two RX02 floppy-disk drives, PDP-11/23 processor with 128 K bytes expandable to 256 K bytes of memory and either a hardcopy or VDT. PDP-11T23 employs a 40" H cabinet for processor and two RL01 hard disks. It employs 128 K bytes of memory and has hardcopy or video terminals. Available software: RT-11 OS, programming language compilers, editors and utilities. Compilers include ANSI-standard FORTRAN IV, and BASIC. PDP-

11V23, $15,150; PDP-11T23, $20,750. **Digital Equipment Corp.**, Maynard, MA 01754. **Circle 223**

REMOTE PRINTERS. Serially interfaced, high-speed printer systems, are capable of receiving data from minicomputers positioned up to 2000 ft away. Designed and manufactured by SSI, the SI-22 interface may be used with the firm's complete line of high-speed impact printers, including the 200 lpm impact matrix, 300 and 600 lpm band printers, the SSI 2200 printer series (300 and 600 lpm drum) and 600 lpm ChainTrain. EIA/RS-232C, current loop, X-ON/X-OFF, ACK/NACK, modem control signals, baud rates to 19.2K baud and 45 other variables are available. **Southern Systems Inc.**, 3000 NE 30th Place, Fort Lauderdale, FL 33306. **Circle 199**

SYSTEM/38 purchasers in a bind can update their System/3 Model 15Ds and hook up more terminals in the interim. Are you now operating with 160K – and is your system's response to on-line applications creating data traffic jams? Then, these special packages can add 32K additional memory, 2 Memorex disk drives (20% faster than 3340A 2 or B2) and 72 KB tape drive for more capacity and speed. **Memorex** 3015 Daimler St., Santa Ana, CA 92705. **Circle 141**

REAL-TIME EXECUTIVE. This 60-pg. paper covers organization, design concepts, data structures, and major facilities of the REX-80 Real-Time Executive for 8080, 8085, Z-80. Advantages of the real-time executive approach are discussed, plus several application examples. $5. **Systems and Software, Inc.**, 2801 Finley Rd., Downers Grove, IL 60515. **Circle 224**

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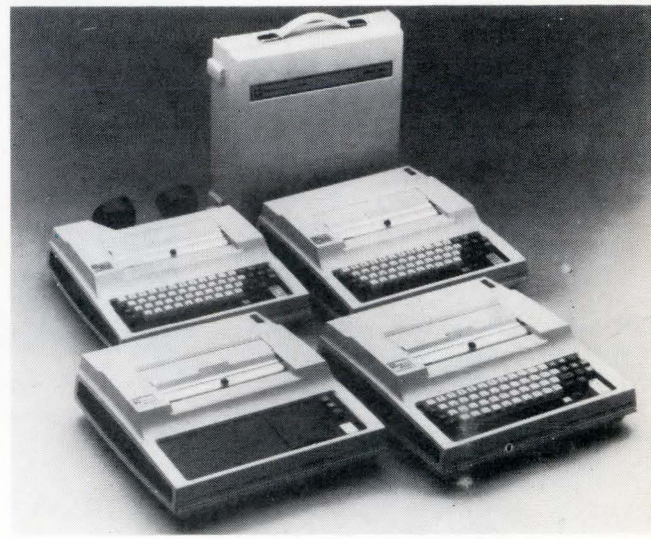
New Products

FOUR 120-CPS DATA TERMINALS offer a dual-matrix thermal printhead that prints two 5x7 dot-matrix characters with each movement across the page. The Model 781 Receive-Only (RO) Printer, the Model 783 Keyboard Send-Receive (KSR) Data Terminal, the Model 785 Portable Data



Terminal and the Model 787 Portable Communications Data Terminal comprise the 780 Series of terminals. Standard features include bidirectional printing, full duplex operation, a receive buffer for data overflow protection, answerback memory that can store up to 21 characters in nonvolatile memory for terminal identification to the host; 128-character ASCII set and self-test diagnostics capability. Prices: 781 RO, $1595; the 783 KSR, $1795; 785 Portable Data Terminal, $2445; and 787 Portable Communications Data Terminal, $2895. **Texas Instruments,** P.O. Box 1444, M/S 7784, Houston, TX 77001. **Circle 242**

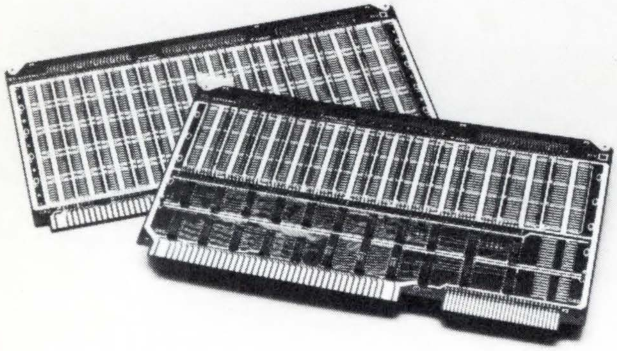
NEW HORIZONTAL CARD CAGE lets users combine analog and digital circuits within one enclosure. Users can also mix wire-wrap with stitch-weld and stitch-wire boards or PC cards. Guide separator locations are optional to permit mixing single, double and triple width boards. The card cage comes with either a continuous backplane or three separate backplanes to provide the different voltages and grounds needed to mix analog and digital boards. All use 96 pin I/O connectors. Flexible spacing permits users to install up to four wire-wrap boards or seven stitch-weld boards or a combination of the two. The card cage mounts into standard 19-in. cabinets. Fan is optional. **Augat Inc.,** 33 Perry Ave., P.O. Box 779, Attleboro, MA 02703. **Circle 241.**

MICROLINE 80 PRINTER makes it unnecessary for customers to purchase different printers for different forms; the unit accommodates friction, pin and tractor feed forms with one model. Its platen handles friction and pin feed and optional tractors snap in place for tractor feed. Standard 1-, 2- and 3-part paper can be used. The Microline 80 fits in an attache case and features program-controlled font selection, MPU-controlled interfaces and a 200M character head warranty. The printer operates continuously at 80 cps with no duty cycle limitations, producing 9 x 7 uc/lc characters across an 80-column page. It also prints condensed characters at 16.5 cpi, accommodating 132-column formats. Line spacing, at six or eight lpi, character spacing and font selection are all under program control. Prices start at $760. **Okidata Corp.,** 111 Gaither Dr., Mount Laurel, NJ 08054. **Circle 237**

DUAL HEADED FLOPPIES. Remex RFD 4000 improved dual head and carriage assembly treat diskettes gently. The ceramic bottom head is fixed in a special lightweight carriage; the top head is mounted via a movable load arm. It has 4 times the storage capacity over std. drives. Its band drive positioning improves data track and reliability. Improved access time of 3 ms track-to-track means an avg. seek of 91 ms (including settle). It's physically and electrically compatible with systems designed to use other (Shugart/IBM) popular dual-head drives. **Ex-Cell-O Corp., Remex Div.,** 1733 E. Alton St., Box C19533, Irvine, CA.
Circle 227

TWO MAGNETIC TAPE SYSTEMS for VAX-11/780s Model TFS-812 800/1600-bpi and Model 804 GCR 1600/6250-bpi systems – operate on the Unibus adapter and comes with software drives compatible with VMS operating systems. Model TFS-812 consists of a controller, industry-standard transport and cables. The system throughput requirement can be matched by providing tape transports at 45, 75 or 125 ips. Up to eight tapes can be daisy-chained off the same controller. Prices start at $8250. Model 804 reads and writes in IBM and DEC packing formats and also reads and writes on the fly. The dual-density, 9-track 75-ips system provides storage in excess of 150 MB on a 2400-ft reel. Data transfer rate is 470 Kbps. A simultaneous on-the-fly two-track-error-correction capability enhances data integrity. Price: $28,200. Optional cabinet with cooling fans for housing a single tape drive and formatter: $1200. Suitcase tester: $6500. **Aviv Corp.,** 6 Cummings Park, Woburn, MA 01801. **Circle 246**

INTERFACE PRODUCTS FOR MULTIBUS single board computers include two general purpose Bus Foundation Modules, one for 16- and one for 8-bit Intel computers, $295 and $245, respectively. A Universal Wire Wrap Module ($145) and Extender Board ($100) require only a single slot in an Intel chassis. The foundation modules consist of basic multibus logic elements plus wire wrap positions for



up to 38 IC devices using low-profile sockets or direct mounting of 14 to 40-pin ICs. The wire wrap module provides for up to 60 low-profile sockets or ICs in combination from 14 to 40-pin packages. **MDB Systems, Inc.,** 1995 N. Batavia St., Orange, CA 92665. **Circle 248**

REVAMPED SYSTEM ACCOUNTING AND CHARGE BACK SYSTEM. Arsap now supports RSX-11M V3.1 and V3.2, multiple disk device storage accounting, multiple UFD storage accounting, reformatted and improved reports, and expanded documentation. In addition, installation has been shortened to 20 minutes. Arsap's method of statistics collection requires no system generation and does not jeopardize DEC software support. Arsap is a proprietary software product that enables PDP-11 system managers to monitor computer usage, measure system performance and bill for resource utilization. Licensing fee $2995. **Gejac, Inc.,** PO Box 188, Riverdale, MD 20840. **Circle 236**

Designers' Notebook

A True Random Number Generator

Briefly, the 8080 subroutine described here generates, in software, a true random number, based on the length of time an operator takes to type a response to a prompt on an output device such as a TTY. The subroutine increments a register pair and checks the keyboard status flag. If a character is not waiting, the register pair is incremented and the subroutine continues to loop.

The subroutine as described can be used in a system using an Intel 8251 USART, or with minimal modification, in a system using a UART or parallel I/O port.

Random number generators are frequently needed in computer programs for simulations, educational programs, games, etc. Implementation of a random number generator is usually achieved in one of two ways. The software pseudo-random generator is most often used, because pseudo-random routines are widely available and are easy to add to a program. The drawback is that, since pseudo-random sequences are not truly random, they will eventually repeat. Hardware generators are also used, but require hardware system modification – not always possible.

The subroutine works as follows: A Listing is truly random because it relys on operator response time. The only hardware required for the subroutine as described is a serial I/O port (an Intel 8251 is described but not mandatory). A parallel I/O port can be used if a Data Ready flag from the keyboard is available.

The subroutine works as follows. A prompt requiring an operator response is sent to the output device (TTY, CRT, etc). After the last character has been sent, the keyboard status flag is cleared. If it were not cleared, the operator could begin typing the response prior to the end of the prompt, thereby resulting in a zero response time. Register pair B&C is used as a counter in a loop, so the contents are saved on the stack prior to entering the count loop. There is no need to initialize the register pair to a known value for the random number count loop. On each pass through the loop, the keyboard status flag (RxRDY for the 8251) is scanned. If it is a logic one, a character has been transmitted from the keyboard, so the loop is terminated. Before inputting the keyboard character, the contents of register pair B&C are saved in memory at locations RN1 for register B and RN2 for register C. The results can be handled as two 8-bit numbers or one 16-bit number. After the original contents of B&C are retrieved from the stack, the character transmitted from the keyboard is input and the subroutine is exited with the character in the Accumulator. The value of the random number generated is a function only of how quickly the operator responds to the prompt. Generally, RN2 will be larger than RN1.

The subroutine RNDNO listing, written in Intel 8080 mnemonics, for a true software random number generator, is . . .

LABEL	MNEMONIC		COMMENTS
*	USARTS	EQU 021	/ status port of 8251 USART
*	USARTD	EQU 020	/ data port
*	RXRDY	EQU 002	/ receiver ready flag
*			/ enter subroutine here
RNDNO	IN	USARTS	/ clear status flag
	PUSH	B	/ save B&C registers
LOOP	IN	USARTS	/ get USART status
	ANI	RXRDY	/ character waiting?
	JNZ	SAVENO	/ yes, exit count loop
	INX	B	/ no, increment count registers
	JMP	LOOP	/ and continue to loop
SAVENO	MOV	A, B	/ save MSByte of random
	STA	RN1	/ number in location RN1
	MOV	A, C	/ save LSByte of random
	STA	RN2	/ number in location RN2
	POP	B	/ retrieve original contents of B&C
	IN	USARTD	/ input character waiting
	RET		/ return with char. in Accum.

J.C. Hassal, H&H Enterprises, 1201 Highland Circle, Blacksburg, VA.

Rate this design: circle 13L, 13M or 13H on Reader Inquiry Card

Console Message Display

To add to your string of "Console Message Display" subroutines (October 1979, pg. 94 and January 1980, pg. 79), here is my version:

```
MSGXP   XTHL
        MOV    A,M
        INX    H
        XTHL
        CPI    0
        RZ
        CALL   CO
        JMP    MSGXP
```

CO is the single-character output subroutine; no special assumptions about it are needed (e.g., subroutine CO may change the contents of the accumulator). Any desired message terminator byte other than 00 can be readily accommodated by changing the second byte of the CPI 0 instruction.

The key to this version of the MSGXP subroutine is the often-neglected XTHL instruction, which exchanges the HL register pair with the two bytes at the top of the stack. This instruction allows the "would-be" return address at the top of the stack to be incremented by 1 each time the subroutine encounters a message character. When it finds the terminator character, the return address is then correctly set to the main program address which follows the terminator byte.

A nice feature of this MSGXP is that the HL register pair comes out of the subroutine unchanged. As a result, PUSH H and POP H instructions are not needed before and after each main program call to MSGXP. This 2-bytes-per-call saving over the previous versions of MSGXP is only slightly reduced by the one-time 1-byte increased length of MSGXP (compared with Mr. Quilici's 12-byte next-to-final-version – January 1980, pg. 79). As with the other versions, another byte can be saved in MSGXP if you use 00 as the terminator byte; simply replace CPI 0 with ANA A.

An analogous subroutine for the 6800/6801 microprocessor is:

```
MS2     JSR     CO
MSGXP   TSX
        LDX     0,X
        LDA A   0,X
        TSX
        INC     1,X
        BNE     MS4
        INC     0,X
MS4     CMP A   #0
        BNE     MS2
        RTS
```

This subroutine, which is entered at MSGXP, is 20 bytes long. It can also be modified to work with any desired terminator byte by changing the 2nd byte of the CMPA A #0 instruction. Unfortunately, this subroutine destroys the contents of the index register, and so a PSHX . . . . PULX instruction pair (6801 processor) may be required around each main program call to MSGXP. 6800 users will have to save and restore the index register (when necessary) in read-write memory.

Robert J. Borrmann, EE Dept., Manhattan College, Bronx, NY.

Rate this design: circle 14L, 14M or 14H on Reader Inquiry Card

A Glitch Detector and Expander

Sometimes it is very difficult to detect troublesome "glitches" or spikes, caused by race conditions, in complex timing signals or signals with low repetition rates. The circuit shown in **Fig 1** overcomes this by detecting glitches (positive- or negative-going), and expanding them, while remaining insensitive to normal timing pulses. The glitches can be expanded to any desired length so that they can be readily displayed on a second oscilloscope channel and compared to the original data trace to obtain their temporal displacement. **Fig 2(a)** shows a typical

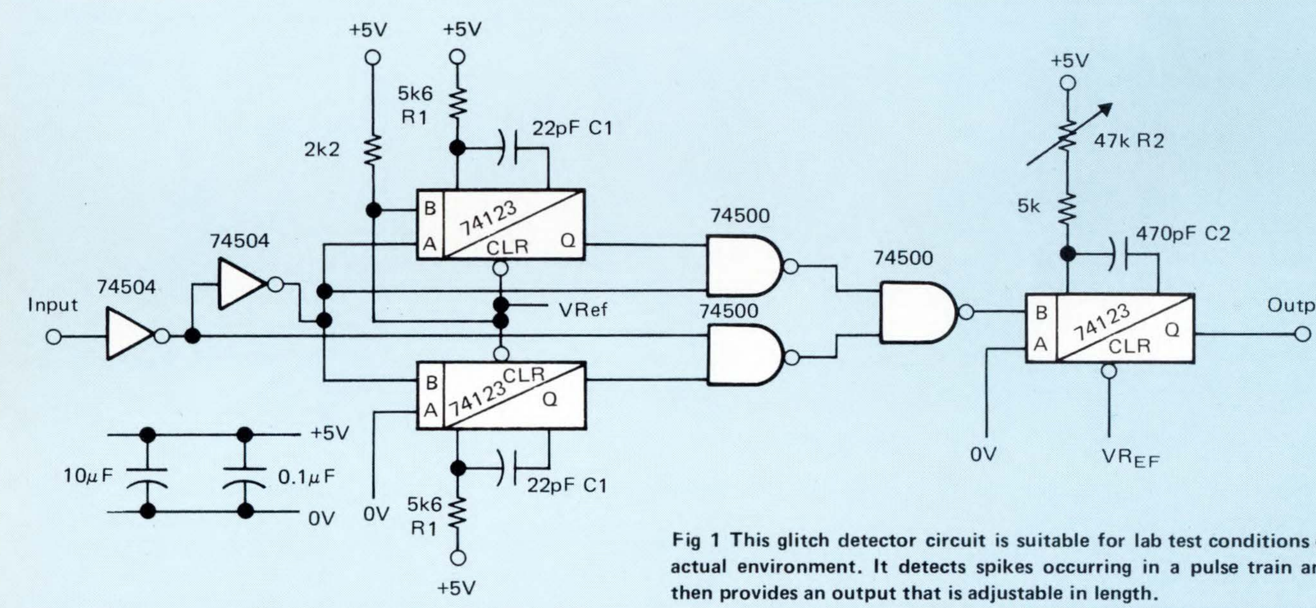


Fig 1 This glitch detector circuit is suitable for lab test conditions or actual environment. It detects spikes occurring in a pulse train and then provides an output that is adjustable in length.

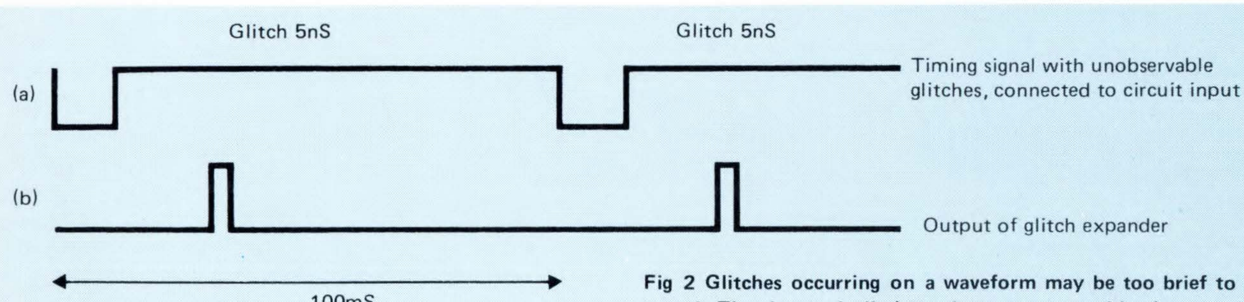


Fig 2 Glitches occurring on a waveform may be too brief to be observed. The detected glitches trigger a monostable that provides an expanded output easier to detect.

timing signal with glitches which would normally be unobservable on a scope. The output of the circuit is shown in **(b)**, glitches being at leading edges.

The circuit operates by triggering one monostable from each positive-going edge, and one from each negative-going edge. The outputs of the monostables are inhibited by normal timing pulses of greater than about 70nsec duration (the monostable period). Short pulses of less than 70nsec duration allow the monostable outputs through the gating network to trigger the expander monostable, which can be set and adjusted to give any desired expansion to suit the oscilloscope time base range being used. The pulse width discrimination is adjusted by the two monostable time constants controlled by R_1 and C_1 and the displayed pulse width is controlled by R_2 and C_2 .

P. Shouler, Stalbridge, Dorset, England.

Rate this design: circle 10L, 10M or 10H on Reader Inquiry Card

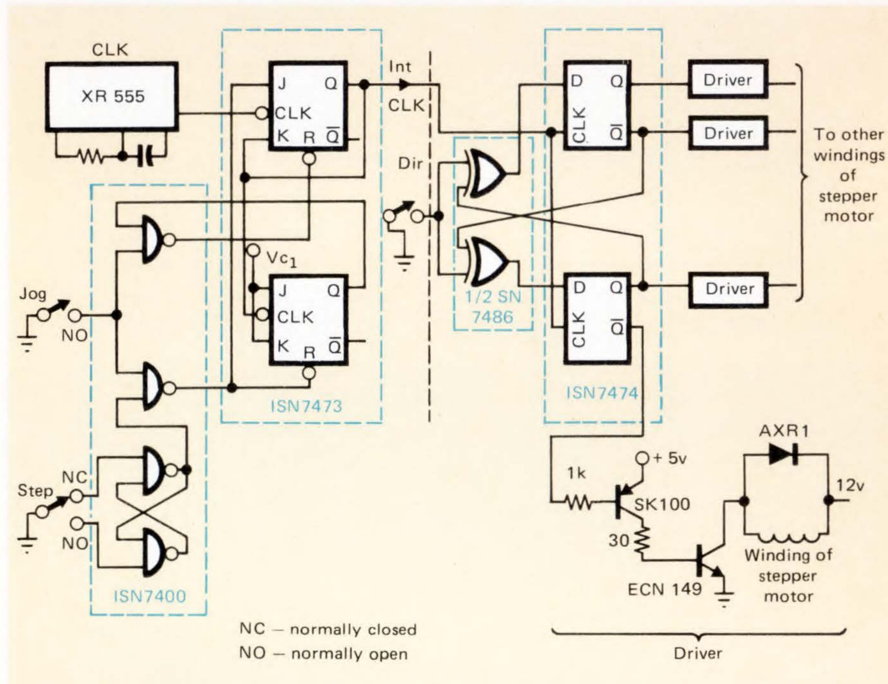
Digital Circuitry Controls 4-Phase Stepper Motor

Here's a four-phase stepper that overcomes the need of a separate start/stop switch and inhibit controls. Two independent step and jog controls provide less complexity and save two ICs. Note that the clock generated by the timer chip is twice the frequency of the internal clock (INT CLK) required.

This stepper motor was used in process control systems as a control drive. The input signals are direction control and digital pulses only, thereby overcoming the need of a DAC and other analog circuits. A simple 2-line-to-1-line multiplexer can be inserted at the dotted line to enable the user to select either internal or external clock and direction control merely by means of the MUX select bit. In such applications, step and jog controls are used for initial setting only.

Vikram Manuja, *I.I.T.*, India.

Rate this design: circle 11L, 11M or 11H on Reader Inquiry Card



This four-phase stepper motor controller circuit eliminates D/A converters, since input signals are direction control and digital pulses.

Have you designed and breadboarded a novel and useful circuit that would interest other engineers? Or have you written a unique microcomputer (or even programmable calculator) subroutine or program? If so, then we invite you to share your experiences with our readers.

What if your circuit is simple? Don't despair; big is not better, and circuit complexity doesn't guarantee a winning entry. What do we look for in a design entry? Both simple and complex winning entries should pass one test – fulfilling a need. So, if that circuit idea tucked away in your notebook or file is an ideal "cookbook" circuit, it will be clipped, saved, referenced to and used by engineers for years to come.

When you send in your program or circuit idea, do include enough detailed program or circuit description. "Should I worry about grammar?" is a question we're often asked. The answer is "No," since we will edit it. Include flow diagrams, printout, schematics, block diagrams and a detailed description. We prefer a typed entry; but, if typing is not your forte, don't let it stop you: hand write it. And whether hand-written or typed, leave a space between each line.

When you do submit your entry, keep a photocopy for yourself. If the U.S. Mail loses the original, or if we call for info, that second copy will be a life saver.

Finally, we ask that all circuits and software not be previously published (house organs and related publications excepted) and that your program be debugged and your circuit bench-tested. Send your ideas to: Circuits Editor, **Digital Design**, Benwill Publishing Corp., 1050 Commonwealth Ave., Boston, MA 02215.

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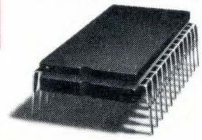

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MOH	374	MUC—ULA	225
MOJ	168		
MOL	403		

Interdesign is a Ferranti Company.

Circle 50 on Reader Inquiry Card

8080 Data Transfer By Cycle Stealing

The normal mode of data transfer between memory and an external device in an 8080 based system is either by DMA or I/O transfer under program or interrupt control. DMA is inefficient when the transfer is sporadic and at a relatively low rate; and so is I/O under program control. The best way is to generate interrupts when data transfer is to be effected. However, interrupt service routines involve a certain amount of overhead for saving and restoring the accumulator and program counter contents. Normal program execution is also suspended under interrupt-initiated I/O.

One way of improving system performance is to go in for "cycle stealing" whereby the 8080 continues its normal operations without interruptions. The device gains control of the system address and data busses during moments when they are not required by the 8080 itself. Thus, data transfer between the memory and the device takes place while the 8080 is busy with internal operations. Normal program execution is therefore, not suspended or affected in any way. A cycle steal is not an interrupt and does not change instruction register contents.

Every instruction cycle in the 8080 consists of up to five machine cycles, each consisting of three, four or five states. The *first* machine cycle of each instruction cycle has at least four states. The first three states are used for fetching an instruction. The data and address busses are required to be under 8080 control to achieve this. The fourth state T4 is the instruction execution state. Operations during this state are internal to the 8080 processor. Data and address bus levels are unimportant to the functioning of the 8080. To achieve cycle stealing, T4 is detected and the address and data buffers consisting of 8212's are set to the high impedance state. The busses are now available for external control. Data transfer between the device and memory may be done now, while the 8080 continues with its internal operations. Note that the transfer is to be achieved within the T4 duration. Even with a 2 MHz clock, 500 nsec is available for this and is therefore, easily achieved. At the end of T4, control of the busses reverts back to the 8080.

In **Fig 1**, SYNC denotes the beginning of every machine cycle and is used to reset counter C. ϕ_2 (TTL), which is generated by 8224 is fed to C. C is prevented from counting during the first two stages by SYNC applied to CLR of C. After SYNC goes low, C starts counting. When the count is 2, T4 is indicated. This count is detected and is used to set the 8212s to the high impedance state and to initiate cycle stealing **(Fig 2)**.

Using this method of cycle stealing, one data transfer can be effected for every instruction executed. The 8080 needs anywhere from 4 to 17 clock cycles to execute an instruction. Assuming a 2 MHz clock data transfer ratio of well over 100 Kbytes/sec are possible.

S. Shankar, Tata Electric India.

Ed. Note: for additional information, see "This 6800 System Handles Clock Stealing" (by B. Ferguson) and "6800 Clock Primer" (by P. Snigier), *Digital Design*, Oct. 1978.

Rate this design: circle 12L, 12M or 12H on Reader Inquiry Card.

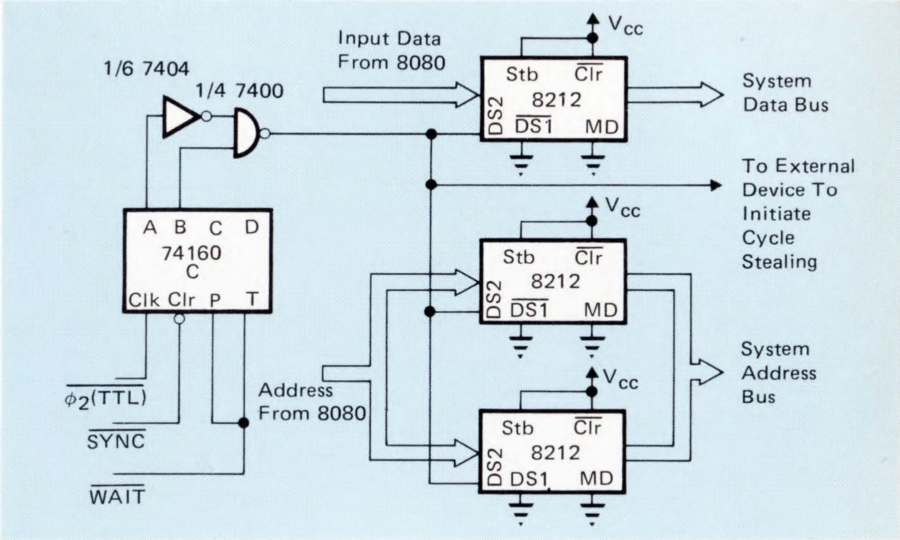


Fig 1 In cycle-stealing, the μC operates without interrruptions, using the address and data buses when unneeded by the CPU.

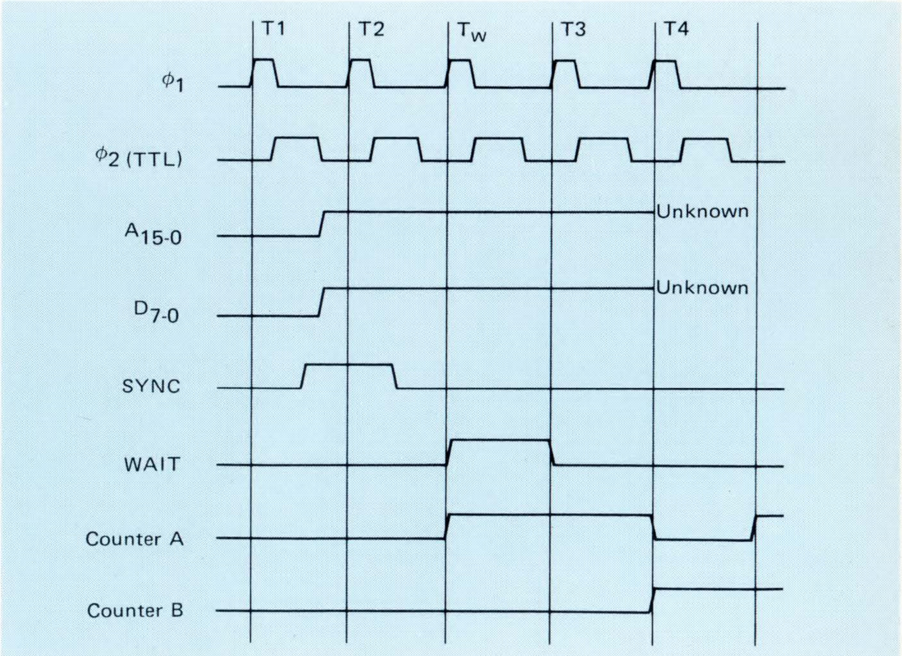
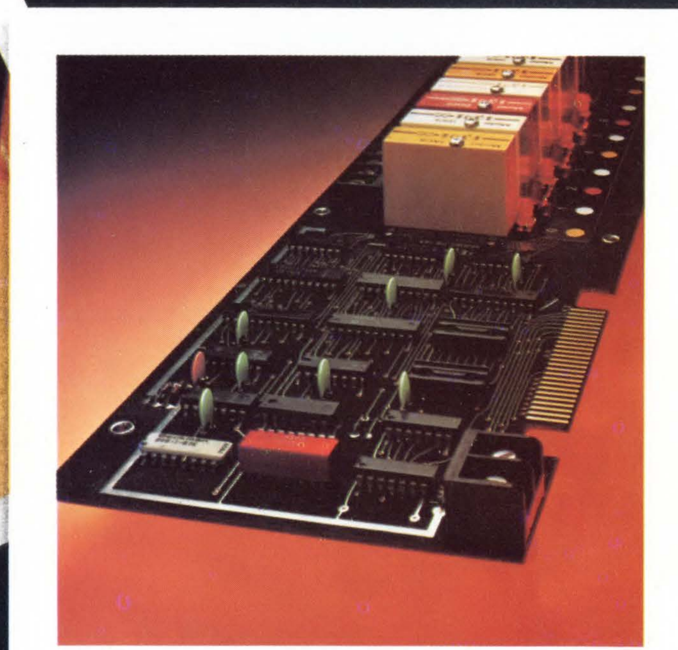


Fig 2 8080 timing waveforms.

ADDRESSABLE I/O SYSTEMS FROM OPTO 22

(PB 16S1)



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