VOLUME 10, NO. 1 JANUARY 1980

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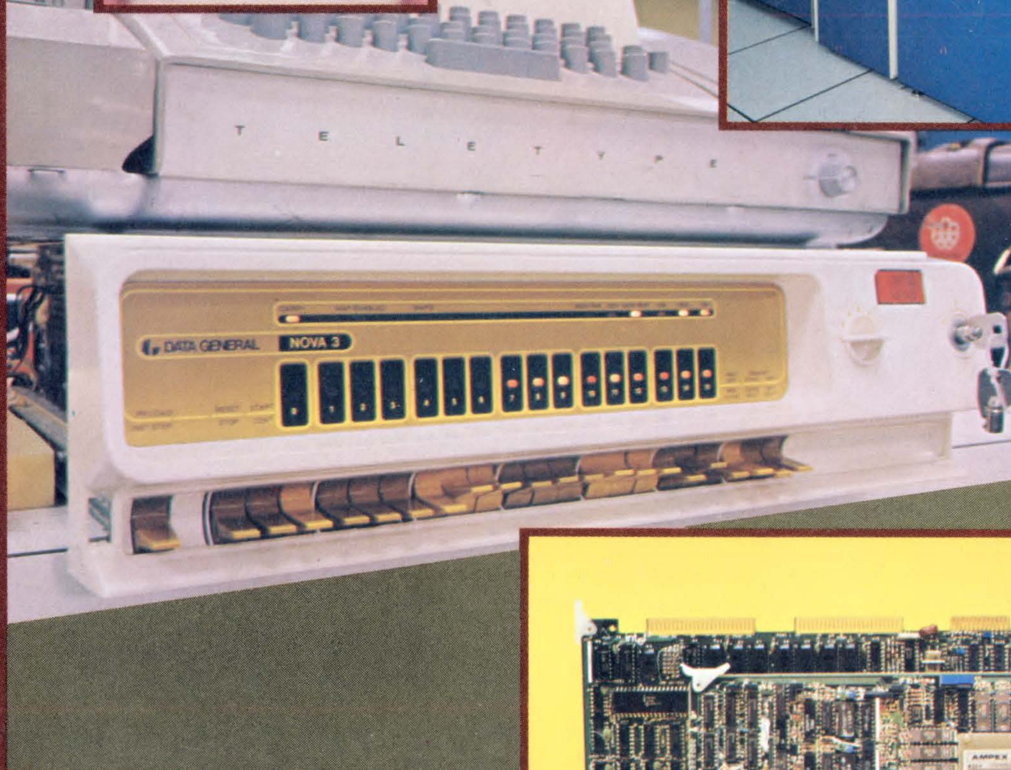
Digital Design

The Magazine of Systems Electronics

Add-In/Add-On Memories

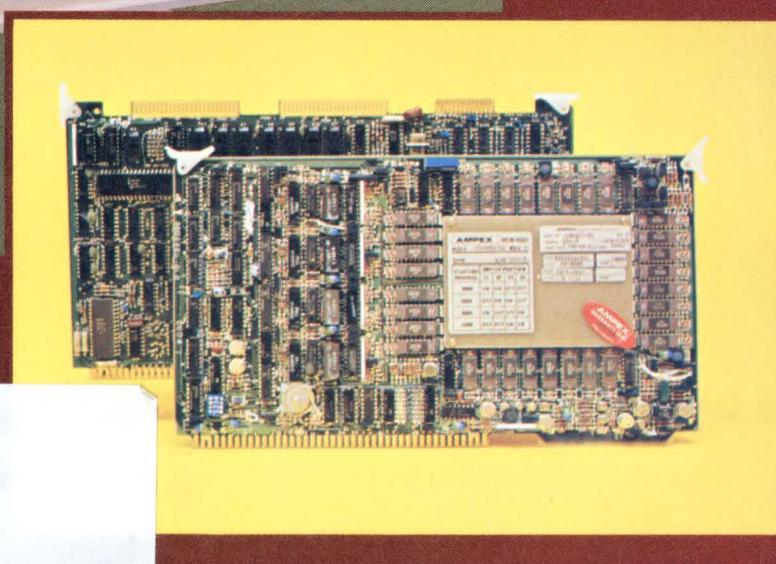


Logic Analyzers

Alphanumeric Data Terminals

Microcomputers

Semiconductor Memories



Models 9100/9300 Vacuum Column Tape Transports . . .

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Model 9100 (75 ips) and 9300 (125 ips) offer crystal controlled timing, read-after-write shortened skew gate, front-accessible test panel, quick release hubs and simplified tape loading.

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Models 9100/9300 offer more features, more performance, and most important, more time-in-the-field than any competitive units.

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Magnetics & Electronics, Inc.

Circle 2 on Reader Inquiry Card

The Chill-able Computer System

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This versatile SECS 80 System likes it cold — or hot. Meets Mil-E-5400, 4158, 16400- and more, making it perfect for space, missile and other military systems and tough industrial applications.

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With these versatile modules, you'll save valuable time and development costs.

- **SECS 80/10A Microcomputer**
- **RAM, ROM & EPROM Memories**
- **Digital Tape Recorder & Controller**
- **1553 Serial I/O Board**
- **Digital Input/Output Board**
- **Analog To Digital Converter**
- **High Speed Arithmetic Unit**
- **Power Supplies**

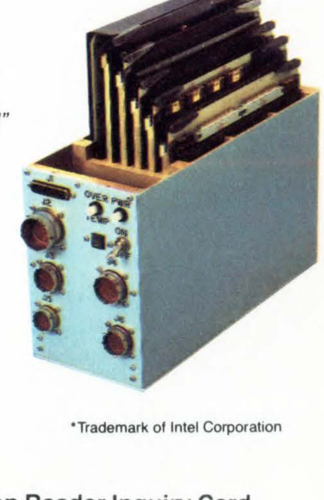
System packaging

All system modules are mounted on 9″ by 6″ shock and vibration resistant boards. A 7.62″ by 4.88″ 12.62″ chassis (½ ATR) holds up to 6 boards.

Other EMM-SESCO products

We've got core and semiconductor memories for military and commercial use, a Digital Data Acquisition System for the 1553 bus, and a compact Digital Tape System with 23 megabit capacity.

When you're faced with a tough environment – "Buy SESCO... it works!"



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The Anadex 80 Column Printer.

First check the specs. Then check the price.

Our new 80-column dot matrix line printer – the DP-8000 – combines high performance and operating convenience with a low price that's worth checking into.

Check Performance

The DP-8000 features a precision engineered, heavy duty printing mechanism that can print the complete 96 ASCII character set, bi-directionally, at 84 LPM.

Check the Interface

Included at no extra cost, are two input connectors (see photo) that provide three basic ASCII compatible interfaces: EIA Std. RS232C, for interfacing at up to 9600 Baud with most mini-computers and modems; the 20/60 ma current drive mode required by Teletype® ASR33-35 printers; and the parallel-bit, serial character synchronous Centronics compatible interface.

The DP-8000 includes 12 lines of internal FIFO buffer storage and can accept data continuously or in bursts. Optionally, increased buffer storage of 2048 characters can be supplied for CRT dump and similar applications.

Check Printer Quality

A 9 × 7 character font provides virtually half-dot resolution for clean crisp print quality on the original plus three copies.

Precise paper positioning is ensured by a sprocket-feed paper advance, user-programmable Top of Form control, and up to 8 vertical tab positions.

Check Convenience

For operating ease, the DP-8000 accepts paper through the rear or bottom of the unit, provides programmable Skip Over Perforation control, and Out of Paper indication and logic signal. And movable sprockets allow the use of forms or paper from under 3 inches to 9½ inches wide.

Check the low Price

The best news is the price. A complete DP-8000 is unit-priced at under $1000, with substantial discounts in larger quantities.

Once you've checked out the performance and price, we think you'll agree that the DP-8000 is definitely worth checking into. Contact us today for complete details and a demonstration.

Anadex®

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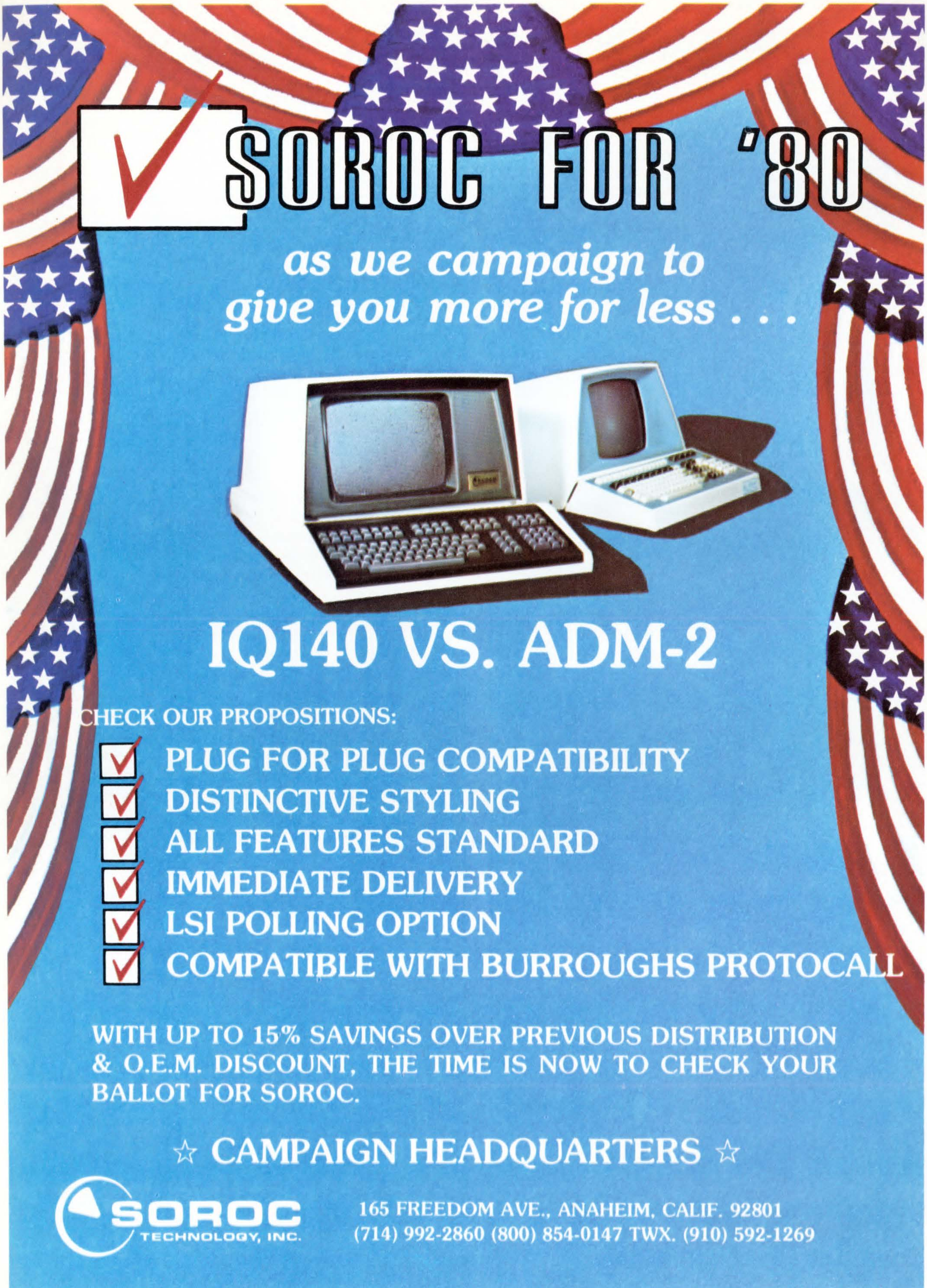
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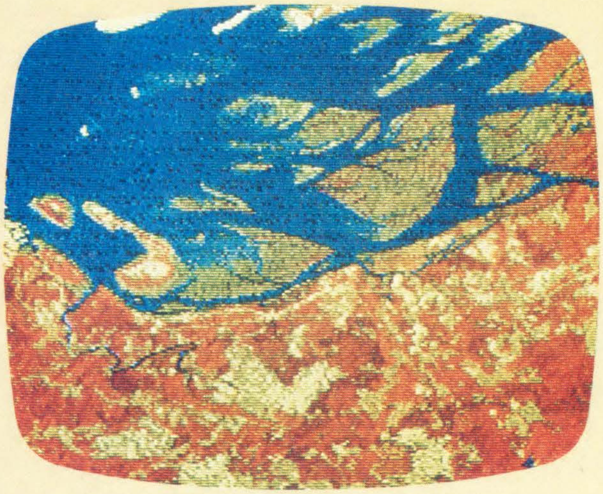
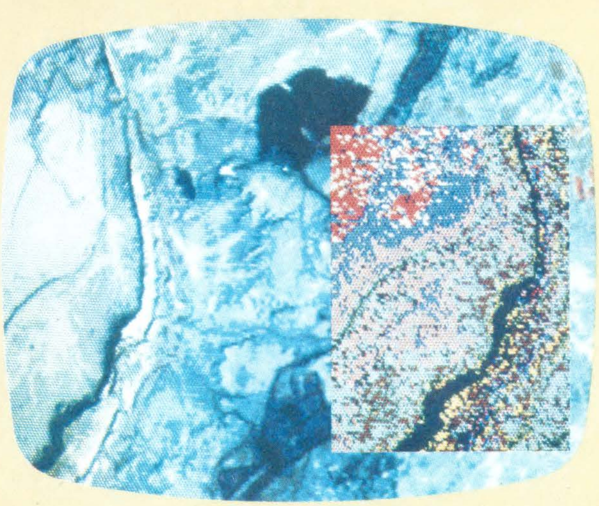
Image processing. Your way.





Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
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- Zoom and pan
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In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 512 to 1024 x 1024.

So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

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VOLUME 10, NO. 1 JANUARY 1980

Digital Design
The Magazine of Systems Electronics

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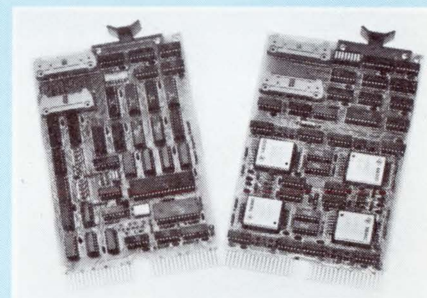
Features

Departments

ON OUR COVER

Add-in and add-on memory can upgrade microcomputer, minicomputer and mainframe storage capacity, and increase computer performance. Photos courtesy Ampex Corp., El Segundo, CA.



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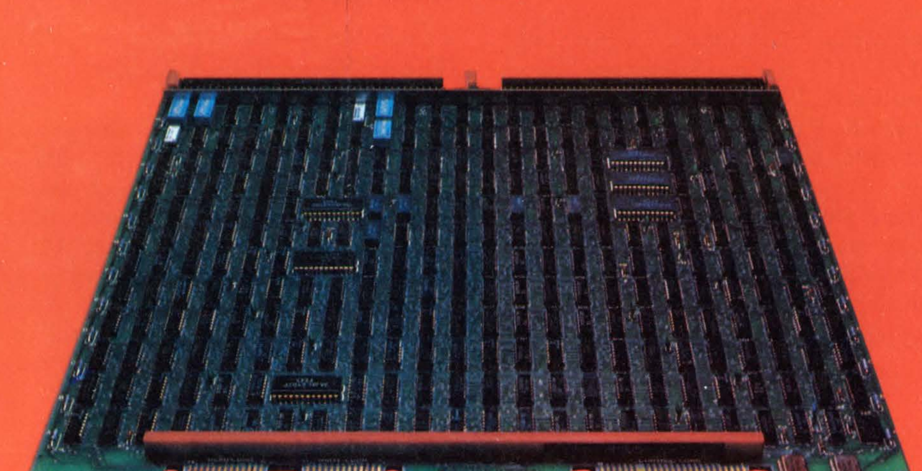

Universal Tape Controllers

- Software compatible for PDP-11*, NOVA**& Interdata.
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Letters

Software Maintenance

Dear Editor:

Software maintenance (June 1979) was an interesting article; it makes a welcome change from other magazines to be able to read about the strategy of design.

N.R. Bailey
GEC Computers Ltd.
Boreham Wood, GB, WD 6 IRX

Can Supply Documents

Dear Editor:

I doubt that you will want to publish my letter. In your Speakout, "The Winds of Change," you briefly pointed to "certain firms" that practice age control or discrimination by controlling salaries; in particular, one whose president was also an IEEE president! You failed to elaborate on this. Many (perhaps most) other companies practice age control under other pretexts. One was based on declining creativity of mature engineers as evidenced by the age distribution of awarded patents. A high-level manager of the same large corporation later proved the falsity and absurdity of this contention (but the controls are still in effect).

At least they were three years ago when the company's famous research lab refused to even look at many older EEs out-of-hand, despite their impeccable qualifications. It's illegal, so how do they do it? Here is the "Legal" way out: the company closes down a mature activity (preferably during a recession). Then, when it hires again, at nearby locations, the laid-off, older engineers get the runaround until all positions have been filled with younger people (even though senior personnel on layoff are *supposed to* get "first crack" at new jobs).

In my case, *the violation was so blatant that I filed a complaint.* The New Jersey Division dragged its feet, to finally come up with a verdict of "no probable cause" in spite of *company documents that proved my contention.* An appeal to the Division VP (company rules had been violated as well) remained unanswered.

If you decide to publish this letter, I can supply all legal documents, including names, dates, etc. However, at this time my job could be in jeopardy if my name gets known prematurely. What measures can working EEs take to protect me and other misused EEs? How can I reveal the gory details? Certainly the IEEE won't help us, will it? With another recession coming up, the topic of age discrimination is very timely. You can contact me by writing to the following address.

Name withheld
Box 4
Boonton, NJ 07005

Against Conflict of Interest

Dear Editor:

Congratulations on your Speakout "The Winds of Change" (Sept. and Oct. 1979). You pinpointed the conflict of interest between the present IEEE establishment and the practicing EE. There was only one statement that I could not understand: that Leo Young has *suddenly* changed his views in favor of the working EE. Leo has a long record of working to improve our professional environment. For example: he was U.S. Activities Committee chairman before it became an IEEE board, organized the Professional Activities Committee within the IEEE MTT society, started an ad hoc professional activities committee in the S.F. Bay area before professional activities became part of IEEE and is the Pension Committee Chairman. These are only a few samples from a long record of service. Yes, I'm sure that we'll see a lot more from our new IEEE president.

Al Hemel, SM
Cupertino, CA

A Better Future . . .

Dear Editor:

With regard to Mr. Barauck's letter defending Leo Young, there are several points he ignored.

First, where were Leo's outcries about that outrageous lunch (cost = $45 per attendee) sponsored by IEEE at the "21" Club? Leo had no criticism of IEEE about this, especially since he was unable to speak with his mouth full. Second, where were Young's outcries when IEEE authorized fully ten members of IEEE's Board of Directors to go to Great Britain this Spring? Or is it possible that Young's criticisms could not be heard because little sound that emanates from London is received here in the U.S.? Third, Young (and his wife) did not hesitate to publish (under the aegis of Bethesda Books, Inc.) the information about pensions gathered for IEEE. I have received no reply to my questions about the sales of the book, or if either one ever received fees, salaries, or expenses from IEEE in connection with the gathering of material for this book. Fourth, where is Young's proof (even in the flimsiest sense) for his untruthful statement that I have repeatedly received offers to serve IEEE but that I have always turned them down? Fifth, at our dinner meeting on 3/12/79 in Washington and Arlington (VA), Young refused to endorse the principle that no foreign engineers should be admitted to the U.S. He also declined to support the position that IEEE should help with the fight to stiffen the backbone of the Labor Dept. in the matter. By contrast, Burk Schneider supported this position and IEEE is now actively involved in this matter.

In any case, this is now history. I hope that the future is better.

Irwin Feerst
CCEE
Box 19
Massapequa Park, NY

Editors Never Make Misteaks

In Part 1 of "The Winds of Change" (September), we inadvertently misworded a sentence. "Although an IEEE VP for 5 years and a member of the Board. . ." was intended to be "Although an IEEE VP and a member of the Board for 5 years. . ."

As for the speakout, reader mail and Reader Service Card comments have been favorable with approximately a 9-to-1 ratio, IEEE's members have given Dr. Leo Young their mandate. We wish Dr. Young the best in his reform efforts; and, if he accomplishes his campaign promises for reform, IEEE will change for the better.

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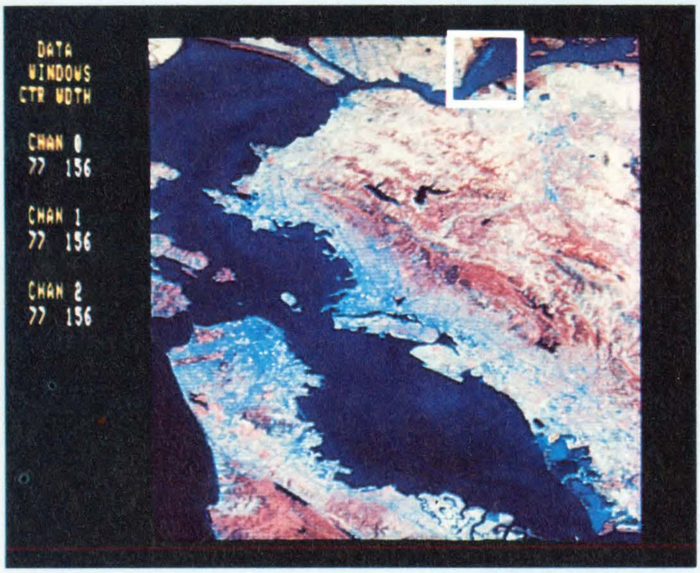
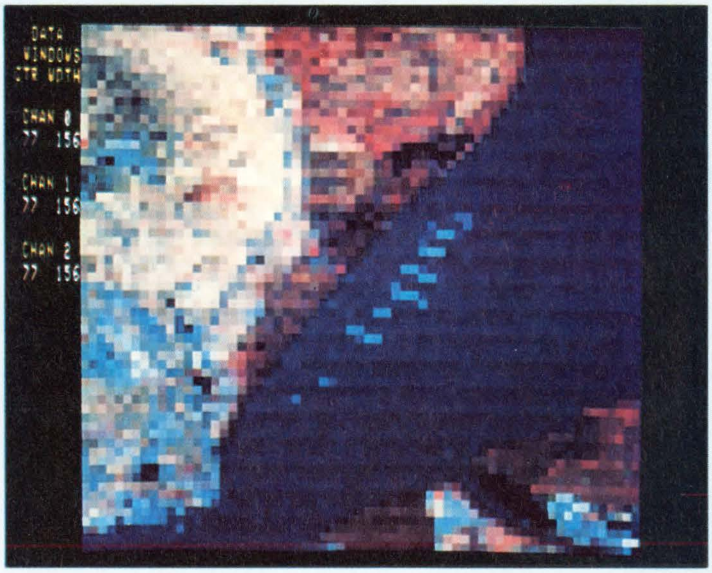
THE IMAGE ARRAY PROCESSING SYSTEM



Three band LANDSAT image of San Francisco Bay


Eight-to-one zoom of Suisun Bay

If image analysis and aquisition is your problem, you need the IP 5000 Image Array Processor.

The display system that:

- Stores up to one megabyte of data for single or multiple image arrays.
- Has complete independence between refresh memory (raster scan output) and host computer addressability of memory.
- Includes memory management and data control for direct high speed access to refresh memory.
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- Digitizes video signals up to 8-megahertz bandwidth with true 8-bit precision.
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For further information and a list of satisfied users, contact DeAnza Systems, Inc., 118 Charcot Ave., San Jose, CA., 95131, (408) 263-7155.

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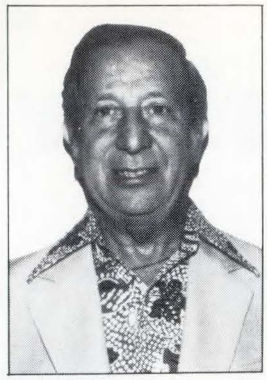


Speakout

Harry Shershow
Associate Editor

There May Be Smoke, But There's No Fire!

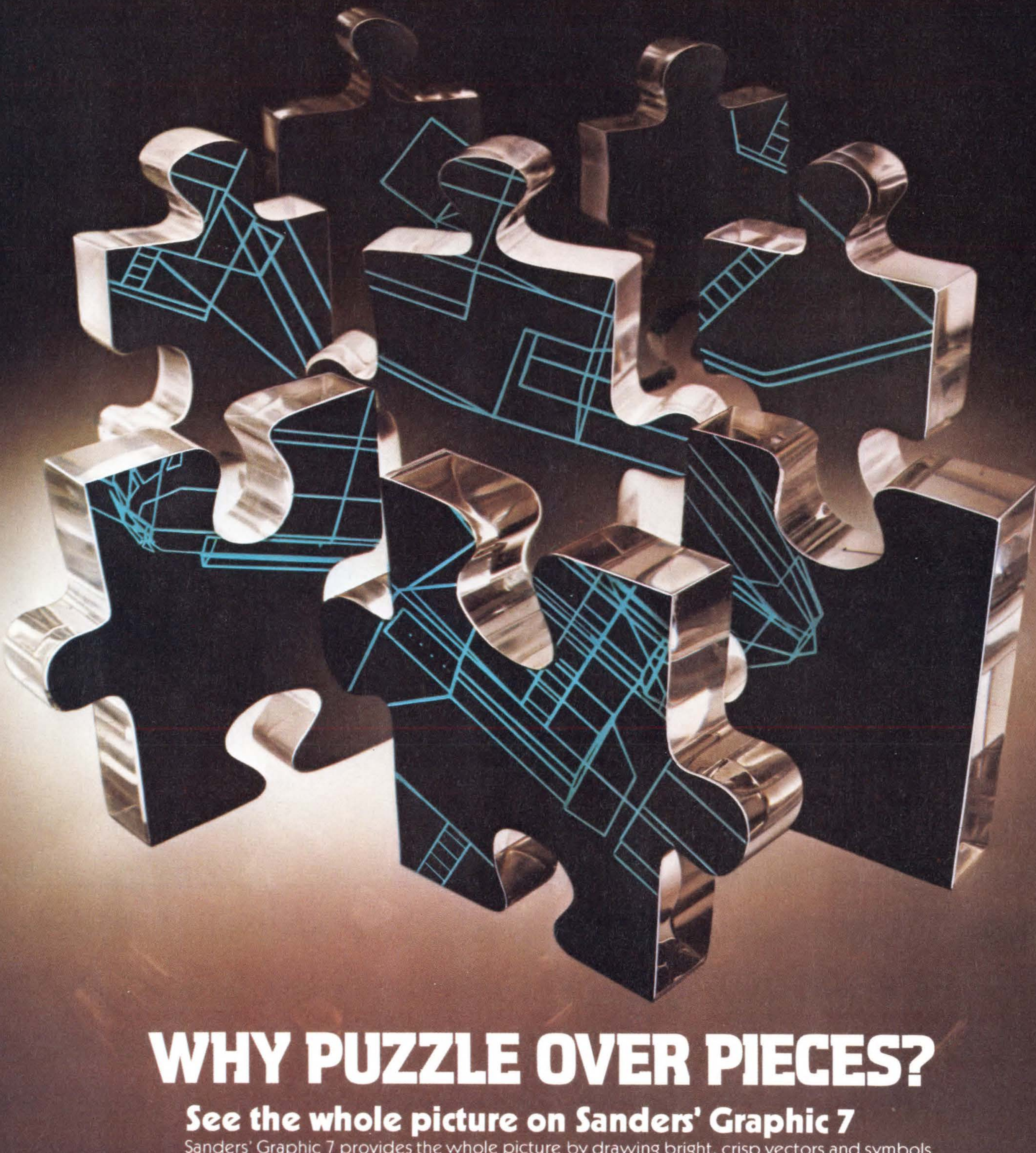
Glancing through some of the other computer magazines in this specialized world of publications, I recently noticed an editorial headline: "The 8-inch Shortfall!" I forget the name of the magazine or the name of the feller who wrote the words under the head. But I do remember some of the things he said:

> "With all the hoopla surrounding the 8″ Winchester disk drive sweepstakes, systems designers would be wise to question when they will be available in volume! There's considerable concern that media suppliers won't be able to meet the demand! Shortfall of the devices will develop until media makers can ramp up production and that probably won't happen until next spring!"

Well, I for one, can assure systems designers around the country not to fret about production. While magnetic media manufacturers are not able to switch from 14″ to 8″ disks as easily as shoe factories switch from size 12 to size 5 shoes, the need for retooling is hardly the formidable task faced by Detroit when they're ready to market a new automobile model. The major difference between the 14″ and 8″ is the outside and inside diameters of the disk.

I learned all this after a recent visit to 3M's Data Recording Products Division. Last September I spent a few days at that company's bustling plant at Weatherford, Oklahoma. They are working three shifts around the clock and turning out a steady stream of orders for 14″ disks and 5″ and 8″ diskettes and will be ready to handle orders for the 8″ disk by the time you read this. In fact, 3M's general manager for the Data Recording Products Division, Al Smith, says: "Any systems designer that can't fill his needs, please contact us. We'll have your 8″ qualification disks on our shipping platform the day after we get your order." And if 3M is ready, can the other companies be far behind?

As our local chief, Barney Gooser, tells his newly-hired firemen: "Before you fellers pull an alarm – make gol' darn sure there's a fire out there!"



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At Sanders we build graphic displays to tough standards and we support them. The reliability of a solid product backed by a solid organization helps keep your job on track.

To make sure you get the whole picture of performance, convenience, and reliability, call us at (603) 885-5280 and let us arrange a demonstration of the Graphic 7.

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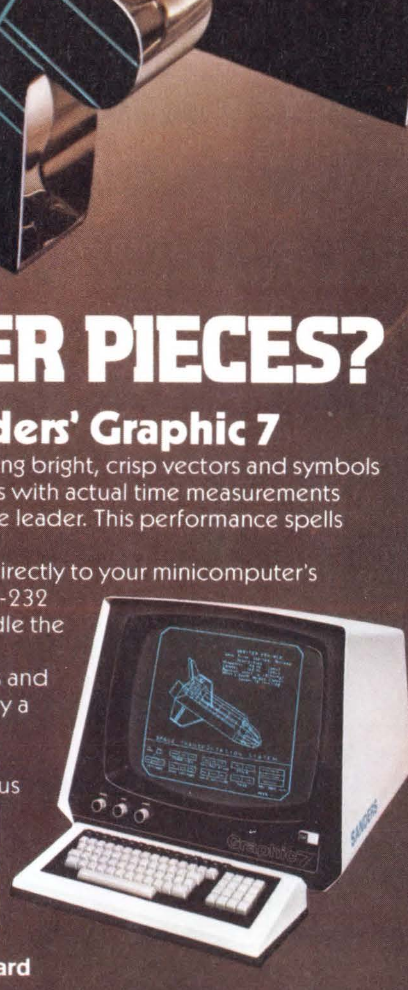

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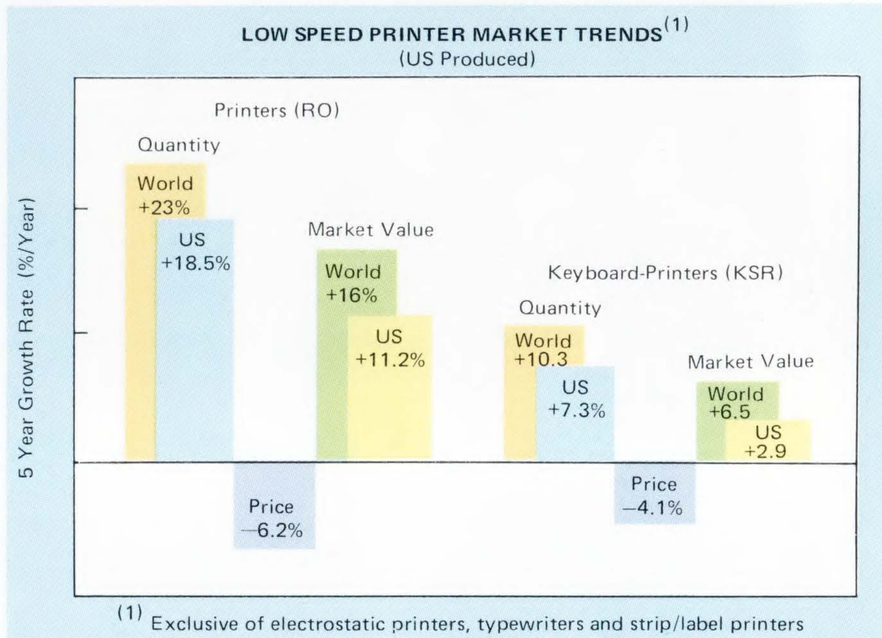
Technology Trends

Competitive Pricing Restrains Low-Speed Printer



Competition will reduce the average unit price for low speed printers 6%/year in 1982, as market values rise 11.2% annually in the receive-only (RO) segment and 2.9% in the key-send-receive (KSR) segment.

Shipment values will reach $1 billion for ROs and $450 million for KSRs in 1982, the study estimates. Unit shipments will increase 18% annually on the RO side and 11% on the KSR side through the forecast period.

Competition among technologies will characterize the low-speed printer market through the early 1980s as the ongoing shift to matrix printing continues. Impact printers will continue to dominate at first, but will yield market share to ink jet designs over the long term.

Ink jet printers will find applications in the fast-growing office automation and business graphics markets on the strength of their speed and paper handling capabilities. Nonimpact page printers, however, will begin to edge solid-character printers out of WP.

The above technology forecast was condensed from the report, "Low Speed Printers," which analyzes the market to 1982 for serial and line printers at 200 lpm and below. Gnostic Concepts, Inc, 2710 Sand Hill Rd, Menlo Park, CA 94025.

Independent Software Shows Fast Growth

The computer services/software industry has become a $7 billion-plus market. With demand for computing growing faster than the number of programmers available for implementation, more users are seeking outside help for solutions to their dp problems. By 1983, revenues for the services/software market should reach $15 billion – more than doubling in five years. This accounts for IBM and minicomputer makers' shift in emphasizing software costs and slashing memory prices.

Processing services accounted for $5 billion in 1978 – a 17% increase over 1977 – and 1979 is up even more. This segment of the services/software market will broaden steadily – reaching $10.7 billion by 1983. Examining the growth of this market in terms of access methods clearly indicates that *today's processing services company is communications oriented.* Carry-in batch services – 74% of the market in 1979 – will comprise only 28% of the market by 1983. Batch service vendors, even the smaller $1 million firms, are now providing remote capabilities and adding minicomputers to their lists of service offerings. Remote-batch processing will grow rapidly in the coming years – 25% annually compounded through 1983.

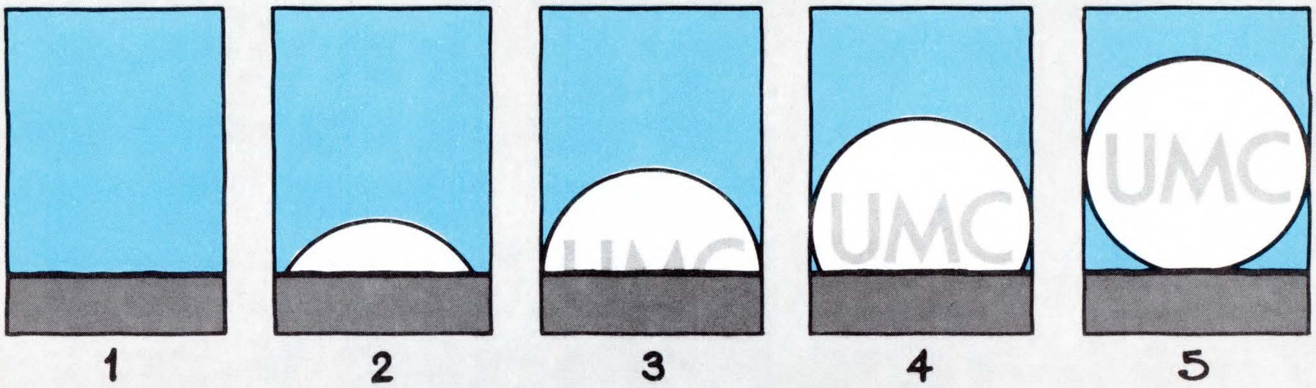
Independent software, the fastest growing market segment, will jump from an 18% share of the overall market to 22% of the total by 1983. During the same time frame, processing services will decrease slightly, dropping from 72% to 70%. Independent software generated revenues of $1.3 billion in 1978 – up 21% from 1977 – and will exceed $3 billion by 1983. Packaged software will show the greatest gains. Growing a whopping 34%, packaged software accounted for half ($670 million) of the entire software market. Looking ahead, 1983 will see packaged software accounting for 70% ($2.3 billion) of all software revenues.

Independent Packaged Software Revenues

Type	1978	% Per Year	1983
Systems	$102M	16%	$ 218M
Utility	$243	27	$ 806
Application	$325	31	$1,276
Total	**$670M**	**28%**	**$2,300M**

The above research was condensed from a report from IDC's Services and Software Information Program: "Statistical Reference Book 1979" ($2,500). For more information, contact IDC, 214 Third Av, Waltham, MA 02254.

PDP-11 ready for the 80s?



The future is here. The decade is dawning. Upgrade your PDP-11 for work of a new age.

Upgrade your PDP-11 by front-ending it with our UMC processor system. It plugs into your UNIBUS, shares work with your PDP-11, and gives you powerful yet independent processing.

Use it to support network expansion. Have it control data acquisition, translation, formatting and processing. Or maybe emulate peripheral controllers. Or serve as terminal concentrator.

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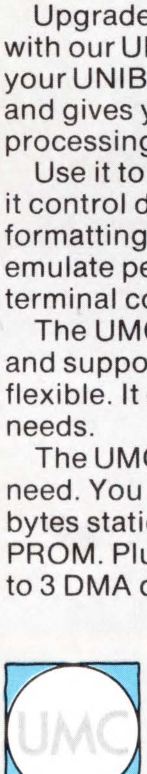

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Self-Contained Professional/Personal Computer Offers BASIC/CAD

Paul Snigier, *Editor*

Looking for a one-unit, low-cost, standalone personal computer with built-in, interactive graphics? The HP-85 is a bit different from the TRS-80, Apple, Sorcerer and the rest: its typewriter-like keyboard, CRT display, printer, tape cartridge and graphics come complete in a fully self-contained system the size of a portable electric typewriter. If you're not a whiz at BASIC, fret not; the HP-85's English-like BASIC language programming makes it easy to use. Its 16"W by 18"L by 6"H size and 20-lb. weight suit it to desktop use in the engineering environment or lab.

Its one-unit, self-contained structure sets it apart from personal computers and may even signal a new generation of personal computers that are easier to use and carry, and distinctly tailored to the engineering professional.

Interfacing peripherals made easy

Want to expand the system to include plotters, printers, disk drives and other peripherals? Easy. Four I/O parts make this a snap, giving your unit data acquisition and control capabilities.

The 16-Kbyte R/W memory (14.5 Kbyte, user accessible) can be expanded to 32 Kbytes by plugging a memory module into one of the ports. The BASIC offers 12-digit accuracy, string operations, editing, 42 predefined functions, four levels of program security and output formatting for designing program output with headings, columns and spaces.

Built-in graphics

With the built-in, interactive graphics, you can plot data on the display to check and test both results and calculations by doing curve-fitting and distribution analysis on the screen (or see trends graphically). The CRT graphics display can be printed with the built-in printer.

Our engineering editors found the 5" high screen a bit small, but with one programmer working at his desk in front of it, this would be acceptable. The high-contrast, B&W CRT display holds up to 16 lines of data at 32 characters/line. It "remembers" up to 64 lines, which are viewed by scrolling the data up or down.

What about the graphics mode? The display is a 256W-by-192H-dot field. HP-85 stores both the last alphanumeric display and last graphics display, which is convenient when you want to switch from one mode to the other – without losing data.

The thermal printer was quiet, and would not upset anyone else. It prints two 32-character lines/sec. In the alphanumeric mode, it prints the full 128 ASCII set – U&L case with underlining.

In graphics mode, it reproduces any plot on the CRT under program control (or by a button). When plotting, the printer "rotates" the display 90° – a nifty feature that lets it print endless strip charts. With the ports available for interfacing with the outside world, perhaps with suitable I/O modules, it seems that the HP-85 could replace other test equipment.

The HP-85 personal computer features powerful central processor, typewriter-like keyboard with 20-key numeric pad, high-resolution CRT display, thermal printer, cartridge tape drive, enhanced BASIC language and interactive graphics in a fully integrated system the size of a portable electric typewriter.

As for storage, HP-85 uses 217-Kbyte HP Data Cartridges and operates at a 10-ips R/W speed and 60-ips search speed. It sets up a tape directory at the beginning of each tape, and using this "table of contents", it locates programs and data.

Nine application software packages come on prerecorded cartridges. Others are to come. Although our engineering and programming editors programmed the HP-85, there was a difference of opinion on how readily other BASIC programs could be adapted to the HP-85. However, H-P spokesmen claimed that since HP-85's language meets the ANSI standard, most existing software complying with this standard can be readily adapted to HP-85 use.

Circuit Analysis Program (CAP)

For analog designers modeling networks, the HP-85 and its CAP cartridge prove a nice aid that permits modeling passive filters, making phase-magnitude Bode plots of active high-pass filters, etc.

CAP is limited to steady-state (AC) analysis and 9 nodes and 12 branches (expandable in CAP 32 with 32-Kbyte memory to 20 nodes and 44 branches). Circuits modeled may contain the usual passive (R,L,C) and active sources (voltage-controlled and independent current sources). Output can be any node-to-node or branch voltage, or branch current and power. Linear or logorithmic outputs are provided in tabulated or plotted form, and families of curves can be superimposed.

As in larger CAD languages, circuit elements are defined by nodes, value and branch number. The CAP program lists independent current sources first. CAP allows modifications of elements in any of its three program sections (inputs, outputs, plotting) without altering the rest.

If you're modeling networks with other, high-priced CAD languages, you will not find a transient-state analysis mode, or worst-case capability that considers tolerances, or more than three current-controlled sources, etc. Aside from this, and considering the $3250 price tag, the HP-85 makes a nifty design aid that could trigger a new breed of professional and personal computers.

OEM/Systems House Market — A Hotbed of Activity

Hardware expenditures for the top 20 SMSAs has increased 20% over the last 12 months – representing almost $1.3 billion worth of mini/microcomputers and peripherals. California still has the largest number of these firms (21%), followed by Mass. (11%), New York (10%), New Jersey (7%), Texas (7%), and Illinois (6%).

Digital Equipment Corp. shows the deepest penetration in the OEM/systems house market of any mini-manufacturer. Some 38% in this market purchase equipment from DEC. Data General is in second place capturing 20%. Hewlett-Packard and Interdata are third and fourth with 8% and 6%, respectively. IBM has moved up to fifth place in the number of OEM minicomputer customers. This is due to a 55% increase in Series/1 purchases over the last six months. IBM now has a 5% share of the market.

Of the companies, 50% price their turnkey system offerings under $50K, while 48% price them between $50-$250K. Only 12% of the companies carry systems with price tags over $250K. Analysis of these companies by number of systems installed in 1978 shows that 45% had installed 1-9 systems, 33% had installed 10-49 systems, and 22% had installed over 50 systems.

OEM/systems houses are directing their marketing efforts primarily to the following end user industries: manufacturing, general business, medical/health services, government, and distribution. General business, accounting, control functions, communications, inventory control, and process control still dominate the application functions of the turnkey systems offerings.

Digital Design based the above information on data taken from "U.S. OEM/Systems House Prospect Data File" (IDC, 214 Third Av, Waltham, MA 02254). It provides detailed company profiles and information on hardware expenditures for organizations buying mini micro computers and peripherals for resale.

Computers and Communications to Merge in 1980s

The recent AT&T delay in implementing its Advanced Communications Service (ACS) has given the industry breathing time. It is important for the marketplace to get some direction on how the commission will allow dp and data communications to be offered. In an interview, Richard Wiley, former FCC chairman and now a regulatory attorney, stated that regardless of the outcome, it will be important for the FCC to retain oversight of AT&T as the dominant carrier. The commission will need to regulate the interference between the parent company and the regulated subsidiary in the case of an underlying carrier such as AT&T. If this is not done, there will be cross-subsidy problems where financial support is shifted from an entity to the other. "We want regulation to be sure that the rules of the game permit true competition," Wiley explained.

Collision course ahead

Inevitably Bell will get into nonregulated areas closer to data processing, either through changes in the Consent Decree, legislative action or more decisions before the FCC like the Dataspeed 40 case where individual devices are judged on their features.

But Bell's dominance must be recognized and the safeguards to the industry must be made clear. "Bell seems to be looking for insulation from the antitrust laws in this matter," Wiley said, "and I don't think that will happen."

Commenting on the emerging Viewdata type of services, Wiley said the US is behind other countries who are already offering these data base features. Current FCC rules don't permit portions of the TV broadcast image to be used for data and the Commission will have to deal with this issue. These services are consistent with broadcasting and they should ultimately be permitted. If the TV screen is used for transmission, then regulation is probably required to avoid interference with regular TV. But these services could grow via cable distribution or other systems.

The FCC or the marketplace will determine which methods will become standards. There are still many unanswered questions and they need to be addressed. Meanwhile, there is no doubt that a Teletext type service is in the public interest, although the economic questions must be studied.

Depending on the vagaries of the regulatory system, will the Xerox network begin operating before late 1981? Perhaps. Thus far, both the regulatory process and technical development of the network service seem to be progressing well.

Will Bubble Memories Replace Micro-Winchesters/Floppies in 1985?

Mini-Winchesters and low-cost floppy disks will dramatically impact μC systems during the next five years. During the next two years, several new storage technologies are expected to enter the microsystems memory market, including: (1) very low-cost consumer/commercial grade 5″ floppies, (2) 8″ diameter mini-Winchester hard disks, (3) 4-6″ flying head micro-winchesters, (4) "back-end" processors combining disk controller and database management functions in specialized hardware and (5) on-line archive devices in both videodisk and automatic cartridge tape library configurations. Will these innovations, along with magnetic bubble memories, pose a serious threat to the market for an expanded capacity, double-sided floppy disk? Definitely.

Low-cost mini-floppy drives, made in Japan on automated assembly lines currently used for cassette and eight-track tape decks, are offered in both commercial and consumer grades. These very low-priced mini-floppies will be targeted at intelligent typewriters, home computers and other light duty applications. By 1981, low-cost mini-floppies will be functionally

equivalent to currently-available mini-floppies, accounting for over 40% of total floppy production, but at under one-third the price of conventional mini-floppy drives.

R&D efforts made by manufacturers of hard disks have resulted in 8″ diameter mini-Winchester disks. Over the next five years, prices of these "mini-Winnies" will approach the current price of a 1.2-Mbyte double-sided floppy. The high-end unit capabilities will exceed 60 Mbytes through the use of thin film heads and track following.

Mini-floppies will also come under attack from flying-head disks when micro-Winchesters are available in quantity. "Micro-Winnies" will be 1 Mbyte and up, 4-6″ diameter disks (both hard and floppy), sometimes packaged with thin film heads in a removable module about the size of an eight-track tape cartridge. Pricing will eventually approximate the level of today's double-sided minifloppies, with extra disk/head modules going at around $25 retail. The micro-Winnies' ten-times-access-speed advantage will be increasingly attractive as multi-tasking, virtual memory, and database management software become more common on μPs, alleviating system bottlenecks created by the number of disk accesses.

Back-end processors will enter the marketplace in the early-to-mid 1980s. Specialized LSI systems which combine disk controller and database management functions, back-end processors will use highly parallel architecture, content-addressed memory, and CCDs or magnetic bubble buffers, in conjunction with Winchester disks, to substantially improve file handling performance. Back-end processors will serve as a shared database resource which can support an office network of word processors, intelligent copiers, data entry terminals, personal computers, and other workstations.

A related development will be on-line archives (OLA) at microsystem price points, ie, 1000 Mbytes or more for an end-user price of a few thousand dollars. Major advantages of maintaining all data on-line include improved security, constant accessability from remote locations and unattended operation of systems. Data is staged to disk before actual processing, making access speed relatively unimportant.

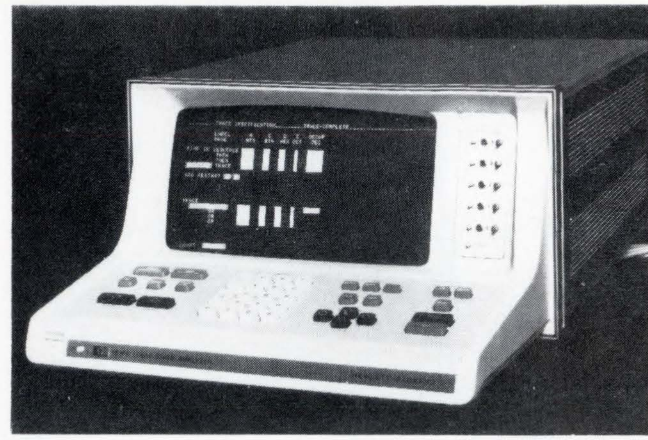
The leading OLA technologies are optical video disks and automatic cartridge tape libraries. Video disks offer fast access (under 1 sec) and low costs reaped from utilizing consumer production scale economies. Automatic tape libraries could be an adaptation of video cassette recorders (particularly longitudinal format), 3M-tape cartridges or a new wide tape format.

In the future, Arnett states that 8″ floppy technology can be advanced to at least 5 Mbytes, but the payoff from going beyond that is in doubt. The on-line storage applications are vulnerable to the ten-times and 100-times-speed advantage of hard disks and magnetic bubbles; and the off-line storage uses are susceptible to low-end floppies, micro-floppies, micro-Winnies, data communications, OLAs and high transfer rate sequential media more suitable for "save/restore" hard disk back-up.

Want more information? It's all in a new report, "Rotating Peripheral Memories I: Floppy Disks And Low-Cost Winchesters" ($895). Contact Creative Strategies Intl., 4340 Stevens Creek Blvd., Suite 275, San Jose, CA 95129.

TOREN/GAYNOR

Logic Analyzers



Bruce Farley
Hewlett-Packard, Colorado Springs, CO

During the last few years, industry, recognizing a need, has dramatically increased the number of logic analyzers on the market. Estimates for total logic analyzer sales in 1979 run as high as 60 million dollars. But despite the proliferation of analyzers, few of the many models share a common, standardized feature set.

Lack of definition for logic analyzer features does not surprise those who feel the industry has not yet reached maturity. People who select and use logic analyzers must choose the best instrument for their needs. But since the variously defined feature sets defy comparison, potential buyers must approach the selection decision from a different vantage point.

In any selection process, the first factor must be a common baseline from which to make a comparison. In choosing measurement tools, this reference point is the measurement application. Understanding the factors to be measured and measurement environment is the keystone in choosing measurement tools.

Once the needs are defined, study the available features — not a simple task in purchasing a logic analyzer.

- Few feature sets are common to all logic analyzers, or even large subsets of analyzers.
- Features often seem the same, but, when implemented under operating conditions, are not.
- Features should not be judged singly, but rather in combination with other features, for example, selective tracing and memory depth in state analyzers.

To understand the measurement application, first break the overall measurement into its component factors. Does the measurement require analysis of state flow, timing sequence, or both? State analysis is based on sequences of "words," moved through a digital system, in parallel, usually with a synchronous strobe signal. Timing analysis is appropriate for investigating asynchronous events, either logic states or control signals. Some measurements require both state and timing analysis, such as studying state flow in relation to handshake signals.

Timing analysis

Reviewing control bus signals and I/O signals are the most common applications of timing analysis; both are generally asynchronous to a system's primary data strobe. Of asynchronous measurements, function analysis concerns the sequence of events; parametric timing analysis measures particular times and is used in fine tuning. If you perform a timing analysis to check whether line 2 went high during the period line 3 was active, you are performing a functional analysis. If you measure the elapsed time between a signal on line 3 and a responsive signal on line 6, you are performing parametric timing analysis.

Rules of thumb have evolved for the proper speed (resolution) required of a timing analyzer. The number varies with the reference thumb, but, for functional timing analysis, resolution 5 to 10 times the normal data rate is recommended. For example, in an MPU-based system with memory cycles around 500 ns and a 2 MHz maximum data rate in the system under test, a timing analyzer should have a resolution as good as 20 to 200 ns. This rule for resolution presumes that the analyzer has a separate mechanism for glitch capture and that functional analysis only is applied.

By contrast, parametric timing analysis requires finer timing, as for setup and hold times. TTL circuits require a resolution of a few nanoseconds for adequate parametric measurements, even in a microprocessor system slogging along at a sedate memory speed of 500 ns. Resolution at the nanosecond level is expensive, both in acquisition circuitry and memory depth requirements, and it's questionable whether you can achieve a reasonable economic payback. Currently, the highest timing resolution available is ±5 ns (plus skew on multichannel measurements) on a $20,000 instrument with a 200-MHz sample rate. The more common solution is to use a synchronized output signal, available on most logic analyzers, to trigger an oscilloscope for these fine tuning instruments.

Analysis landmarks

In timing measurements, determine which "landmarks" can serve as reference points for analysis. What kinds of events will you use to trigger an analyzer to collect information? Two triggering methods for logic timing analyzers are synchronous and asynchronous. The synchronous method samples the lines of interest using the internal clock. The trigger state selected must exist on the lines when the sample is taken. A longer time interval between samples causes a longer time window while sacrificing the ability to detect a "narrow" trigger event. In contrast, asynchronous triggering is independent of the sample rate, and allows you to specify an event and a time filter. The time filter defines a minimum valid state to avoid triggering transitional states

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Circle 50 for DG; 51 for PDP; 52 for LSI; 53 for P-E; 54 for IBM; 55 for INTEL.

that momentarily satisfy trigger conditions only by chance.

You can accomplish glitch detection, an integral part of timing analysis, in two ways. You can "stretch" short duration events so they can be clocked into the analyzer like any other data bit (the drawback is the lack of differentiation between legitimate data and the glitches) or you can use a separate memory for recording glitches, apart from the data memory. When more than one transition occurs on a line during a single sample period, it is recorded in glitch memory, and can be displayed simultaneously yet differentially with the other, normal activity. This method guarantees the capture of all detectable glitches. Also, the occurrence of glitches can be added to trigger conditions, a handy feature when you must distinguish illegitimate from legitimate signals.

The logic analyzer market has grown over the past seven years to a predicted total sales of $60M in 1979.

For a given memory depth, increasing the sample rate reduces the size of the time window that can be viewed with a logic timing analyzer. Therefore, you must be able to focus on the information you need for analysis. With more sophisticated triggering, the presence or absence of a carefully defined trigger condition can solve many problems directly.

All timing analyzers have mechanisms to trigger data collection. With more sophisticated trigger features, you can more narrowly specify the system activity to be viewed. As an example, OR triggering allows you to view activity when either of two trigger states occurs. Some analyzers offer NOT triggering for situations when, knowing a proper state or word, you want to collect information when the next (unknown) state sequence occurs.

Delay features let you collect information beginning a long time after a trigger point is recognized. Delay can be based on elapsed times or number of events; some timing analyzers offer both forms of delay. Delay features bolster situations in which the only convenient, unique event to define as a trigger occurs long before the trouble spot, which is buried in a long string of recurring, nonunique events. Collecting information only at the point of interest results in a more narrow window, with a correspondingly higher degree of resolution.

In review, when comparing logic timing analyzers,

- Describe the major characteristics of your measurement needs and determine whether they call for functional or parametric measures.
- Specify the resolution required for your measurements. Be realistic; faster is not always better.
- List the landmarks, the distinguishing characteristics of your system's operation most convenient to use in specifying trigger points.
- With your measurement needs well defined, investigate the feature sets of logic timing analyzers available. Evaluate these features in actual operation.

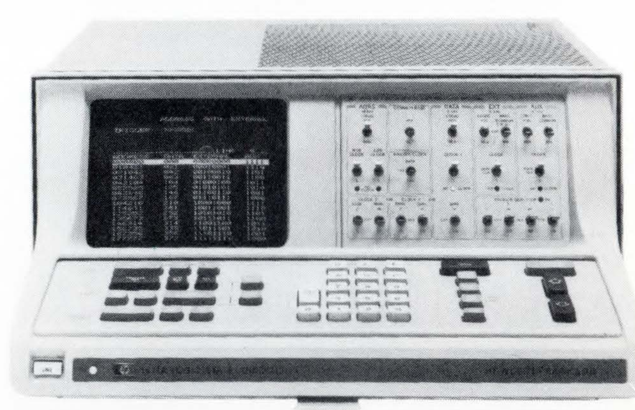
State analysis

"State analysis" is the recording of logic states versus a synchronous strobe signal of the target system. Although some refer to state analysis as "software analysis", state analysis provides a hardware *and* software window into the system by portraying a real-time view of the interactive operation of both. The strobe signal is chosen from the edges active when the information you need for analysis is valid.

Sometimes this window is the system's master clock; more often, a memory enable signal is used. Note that these are functional rather than parametric measurements; the basis for analysis is word or data flow rather than electrical or timing variables. Again, you must describe the measurements you need before comparing feature sets of logic analyzers.

Consider word width first. You will probably want to see the address (16 bits) with the associated data (8 to 16 bits) simultaneously. For timing analysis, memory depth is a critical factor; for state analysis, word width is more important.

When applied to memory depths for logic state analyzers, the old adage "more is better" is only half-true. You can always add a printer to a system (or take advantage of an existing print-out capability) and examine program code line by line. . . If this is your usual analysis mode, and real-time measurement isn't mandatory, you don't need an analyzer; but, for most situations, this only wastes your time and skills. Analysts are interested only in particular state sequences, or in specific system transactions. Then, a given logic state analyzer's memory depth must be evaluated in conjunction with capacity for selective capture of information. Analyzers that allow you to collect only the states of interest measure more efficiently and eliminate your need for a deep memory.



Logic state analyzers display the sequence of logic status occurring at the time of strobe signals in the system under test. State analysis is based on functional rather than parametric measurements.

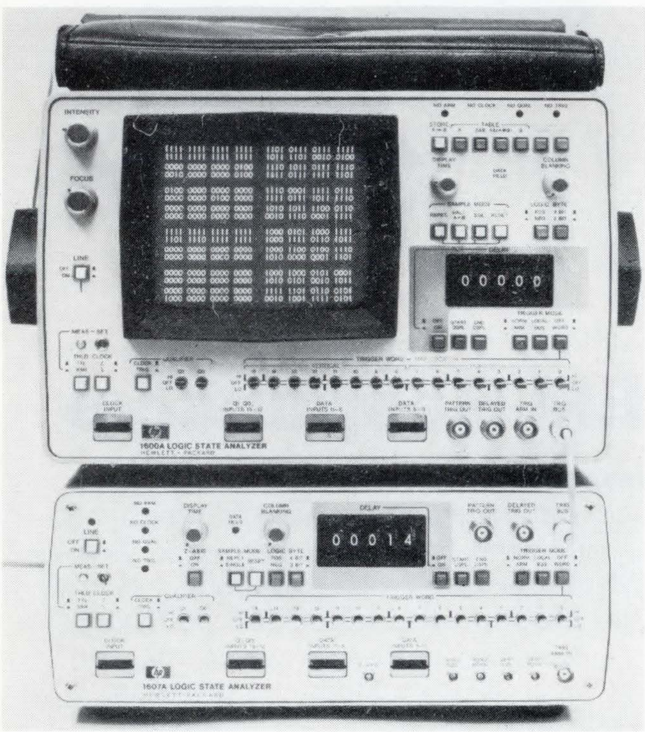
In a simple tracing function, where you may only want to know if a program branched correctly or incorrectly, you need no more than the three or four incoming and existing states at the branch node. If you check data written to a set of memory locations, memory depth requirements vary with the number of locations or entries you want to consider. But if you can specify only those locations and omit all the program flow associated with each memory write, you can vastly reduce extraneous material you must scan. The same situation exists in analyzing I/0 interactions. An

effective logic state analyzer lets users track only data of interest and ignore date irrelevant to the measurement application.

Logic state analyzers offer various features for selective tracing. Their names and functions vary with each instrument. In evaluating these features, you must not only know *if* a feature exists, you must know *how* it is implemented.

Besides considering how features work you should also check their work in combinations. For example, you might set a "trace only" specification to collect states meeting certain criteria, such as only states from addresses in the range from 2000_{16} to $2FFF_{16}$. Then you could add a "clock qualifier"; in this case you might monitor a set of control lines, and collect data whenever the state of control lines indicates a read from memory. The resulting trace would be reads only from memory locations $2XXX_{16}$.

Many logic systems use multiple clocks. A microprocessor system could have individual strobes for READ signals, WRITE signals and I/0 transactions. No signal can strobe a combination of these three activities into a logic analyzer; yet, most logic analyzers have a single input clock. Two routes cut through this apparent dilemma. You can try an analyzer that uses two or three input clocks, or buy or build a preprocessor for use with single-clock logic analyzers. Preprocessors demultiplex complex bus structures so address, data, and I/0 information are aligned for display on one line of a single-clock logic analyzer. Since each preprocessor is specific for the system under test, all compatibility and bus loading factors are automatically accommodated.



Hewlett-Packard 1600A and 1607A logic state analyzers working together produce 32-channel data domain display, *e.g.,* to show 16-bit address with 16-bit data located there.

Logic state analyzers that offer true demultiplexing best monitor multiplexed systems for which no preprocessors are available. Analyzers with multiple clocks do not necessarily offer this feature. If address and data are multiplexed on a system bus, true demultiplexing permits defining a trigger using both address and data, and displays the associated pairs of address and data on single lines.

Synchronous digital systems often permit transitions to occur immediately following the master strobe signal. (Just prior to the master strobe signal, all data must be stable and latched by the circuits, but once the strobe signal occurs, transitions to the next state may begin at once.) There is a setup time, but no hold time requirement. Many logic state analyzers have zero hold time. *Always make sure that setup and hold times meet the constraints of the system under test.*

Triggering features are an even more critical factor in logic state analyzers than in logic timing analyzers. Logic state analyzers usually trace program flow in real time. Triggering requirements vary with the complexity of the programming. For simple, in line code, simple triggering modes suffice; complex programs with many branching operations, nested loops, recursive and reentrant routines require correspondingly more complex trigger modes. If most of the analysis merely requires checking program flow from a defined point, any logic state analyzer providing a single-term trigger will suffice. If the analysis is more complex, you should consider other trigger modes.

Various instruments offer a large assortment of trigger modes. Sequential triggering comes in many guises. You can use a first trigger world to "enable" or "arm" the search for a second trigger condition, or you can select up to seven terms, each appearing a specified number of times, before initiating data collection. Some instruments provide a restart term; if proper trigger conditions aren't met before the restart term appears in the data flow, the search for the trigger sequence begins from the first step again.

With triggering features, *look at how they're implemented.* Logic analyzers are still relatively new, and few standardized concepts are in general use; in triggering modes particularly, similar terms do not necessarily describe similar functions.

Excursions into forbidden areas

A convenient tool for quick, global analysis is an overview of system activity. Many logic analyzers offer a (static or dynamic) map or graph mode to present a macro view. Static maps show data is stored in memory; dynamic maps show system operation and responses, and can display the entire address space. Excursions into "forbidden" areas, system crashes, frequent interruptions and stimulus/response relationships stand out boldly on a dynamic map. The state space graph shows state magnitude plotted as a function of state sequence. For example, if the system slips into a looping sequence, the graph shows the characteristic sawtooth pattern as the original state value is continually reset. When maximum and minimum limits can be set for the axis, the graph provides immediate feedback on operations that cross the boundaries.

Many logic state analyzers offer some form of count for events or time. Count capability permits measuring execution times or path lengths in subroutines or code segments. These parameters serve as crude measures of system performance as well as troubleshooting criteria, and significantly add to the analyzer's utility.

Why not the best?

To summarize, if you want the best logic state analyzer for your needs, include the following considerations:

- Determine the number of channels you want to view simultaneously.
- Outline briefly the likely analysis modes you'll use, so you can specify the most convenient trigger modes.
- Describe the particular information types you'll need, so

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you can decide on the most useful forms of selective tracing.

- Check your systems for setup and hold time specs.
- Do any buses of the system to be analyzed use multiplexed transmission?
- Consider the potential worth of preprocessors for your measurement and analysis needs.
- Rank the values for an overview feature, count time or state feature.
- Compare the probing schemes and available accessories of the analyzers you're considering.

Combined state/timing analyzers

To prepare yourself for any contingency, you might be tempted to buy a logic analyzer offering both state and timing analysis. Taken individually, logic state and logic timing analyzers are complex measurement instruments. Combining the two functions in one box requires a new technology, a degree of compromise, or both. Some of the more sophisticated features of a dedicated instrument may be missing.

Most combined analyzers offer state and timing analysis as mutually exclusive operations; only a few offer simultaneous and interactive state and timing analysis. Combined analyzers best serve measures such as debugging a DMA operation or an asynchronous I/0 operation – cases where you want to monitor the program flow and keep track of asynchronous signals on the control lines.

Some factors apply to buying any instrument. Consider the Operator interface. Operating modes should be convenient and easy-to-learn; the instrument should assist, rather than hinder. Most analyzers offer several numerical bases so the operator can view parameters in the system's numerical base. Not all analyzers permit keyboard entry in all displayable bases; operators must make conversions.

A key-per-function is an obvious user aid for simpler analyzers, but as more functions are added, some variation of the "menu" approach is easier to use. Probing (connecting to the system-under-test) should be easy, reliable and nonintrusive. Sufficient impedance should be provided and capacitance loading specifications observed. In comparing capacitance specifications, *note where the measure is made;* some manufacturers list the capacitance at the point of connection to the system, the probe tip, while other manufacturers only specify capacitance back to the probe body. Since the greater part of the probe capacitance load exists in the probe wires, these specifications can be confusing.

Currently, few accessories are interchangeable between manufacturers. Be sure that any accessories important to your applications are available for the instrument you select.

Don't forget programmability for automated control or enhanced measurements in the lab. If you are selecting a logic analyzer for the first time and are unsure you need automated measurements, you should consider this feature's future potential. Many analyzers can be converted after purchase with field installed kits; you can always add automated modes later.

Price may be the last factor you consider in selecting a logic analyzer. After determining your measurement needs and matching them to the analyzer that offers the optimal solutions, fit your purchase into your budget restraints. Remember, buying a logic analyzer that falls short of your needs is false economy. You are not obliged to buy the top-of-the-line – just the best logic analyzer for your job.

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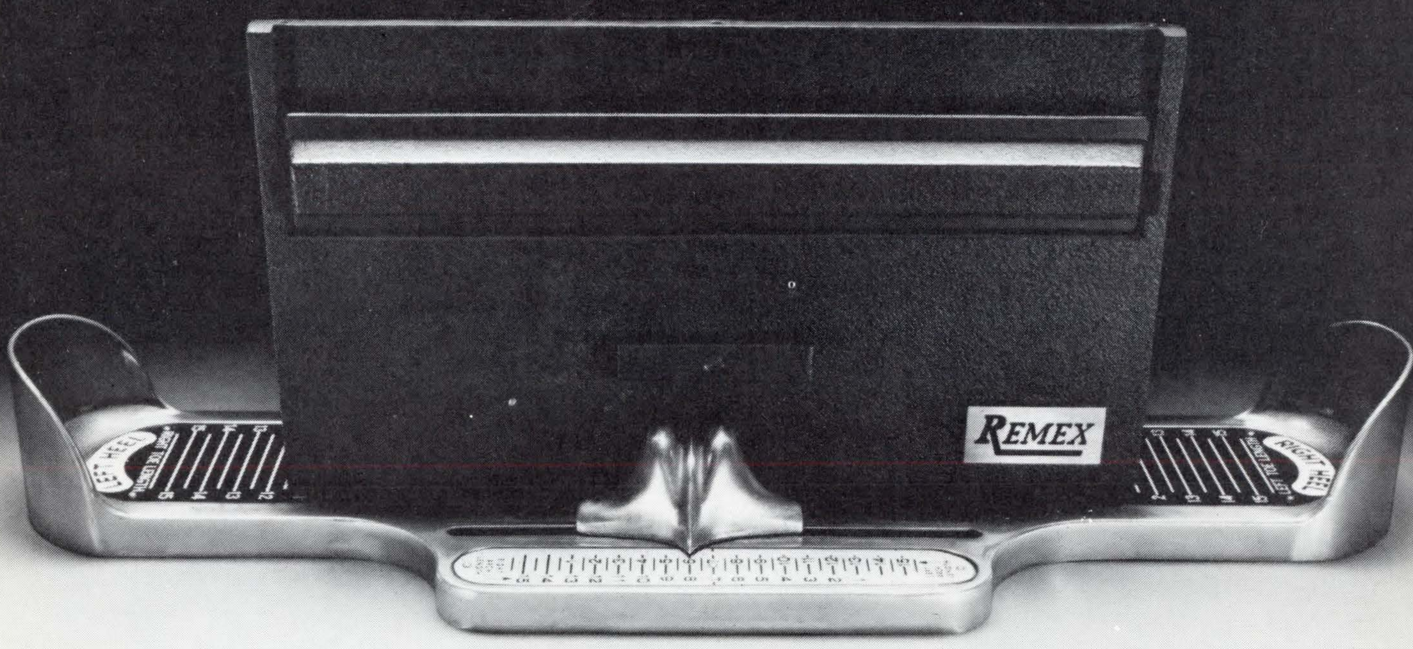

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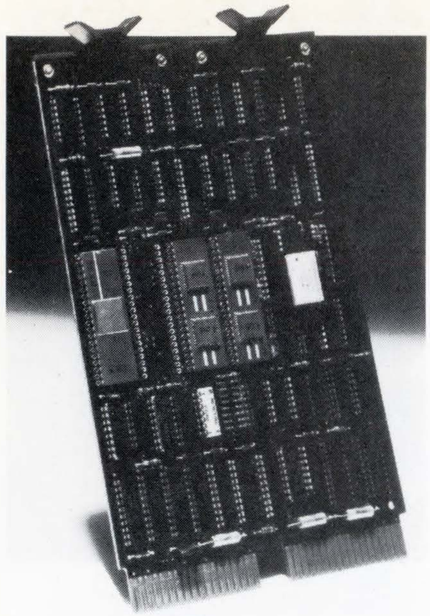

Microcomputers

Al Moore
System Products
Motorola Semiconductor Group

Some industry standardization of microcomputers is slowly beginning to emerge. But there are three different classes of this product, and each of them is sometimes called a microcomputer. In this article, the term "microprocessor" (μP) will refer to semiconductor large scale integrated (LSI) circuits that are essentially only central processing units; that is, they do not have significant amounts of on-chip memory and I/O. Devices that include these (and other) functions on-chip will be referred to as microcomputing **units** (μC). Using these definitions, the 6800 and 8080 are typical μPs; the 6801, 8048, and 3870 are representative μCs. The term "microcomputer" will be reserved for products of printed circuit board of greater complexity. The microcomputer usually, but not always, uses either a μP or a μC as its central element.

The years prior to 1978 were a time of new-product introduction and design. Manufacturers began delivering in volume during 1978 and 1979. And now, the mid-range and a large part of the low end are entering the mature portion of the product life cycle.

The low, mid, and high ranges correspond loosely to bit lengths of 4, 8, and 16, respectively. However, bit length is becoming a misleading measure of performance. For example, many of the 8-bit μCs are now cost effective enough to use in applications areas previously served only by 4-bit devices. A more meaningful distinction to make is between μPs and μCs. The μCs, with just the right amount of ROM and RAM (and with I/O on the same chip as the central processor) have been optimized to provide the most cost effective solution in many low end applications. More than 75% of all units being shipped today are single-chip μCs and the percentage would probably go higher if manufacturers could supply the demand.

Relative cost is a function of performance and representative device performance is normalized to 8-bit general purpose (6800, 8080) performance. Low-end performance is associated with high volume, low cost, consumer oriented applications. However, many low end μCs have enough performance and features to be used as components in instrumentation, process control, automotive, etc. μCs are an extension of the original microprocessor thrust toward replacement of random logic.

The original processors have also evolved upward toward more computer-like devices in both their internal architecture and in the peripheral devices that support them. As expected, the high end devices have the most computer-like characteristics. In this region software becomes as important

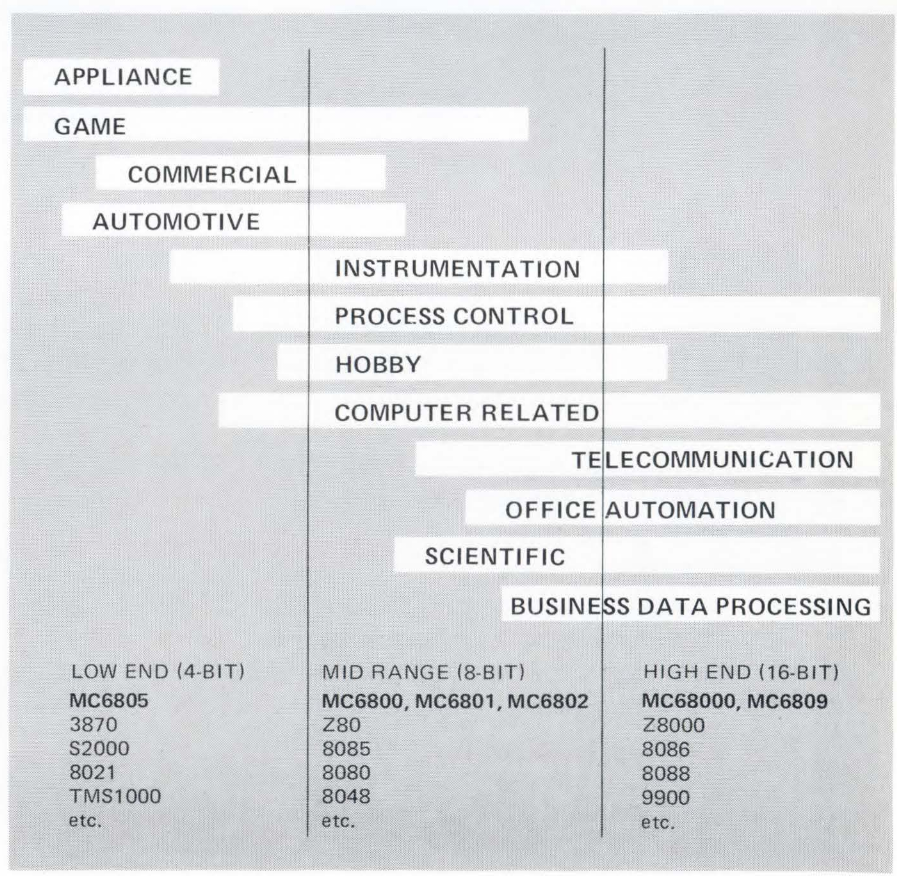

Fig 1 Chart shows range of usage of μP and μC in applications categories and lists some representative devices.

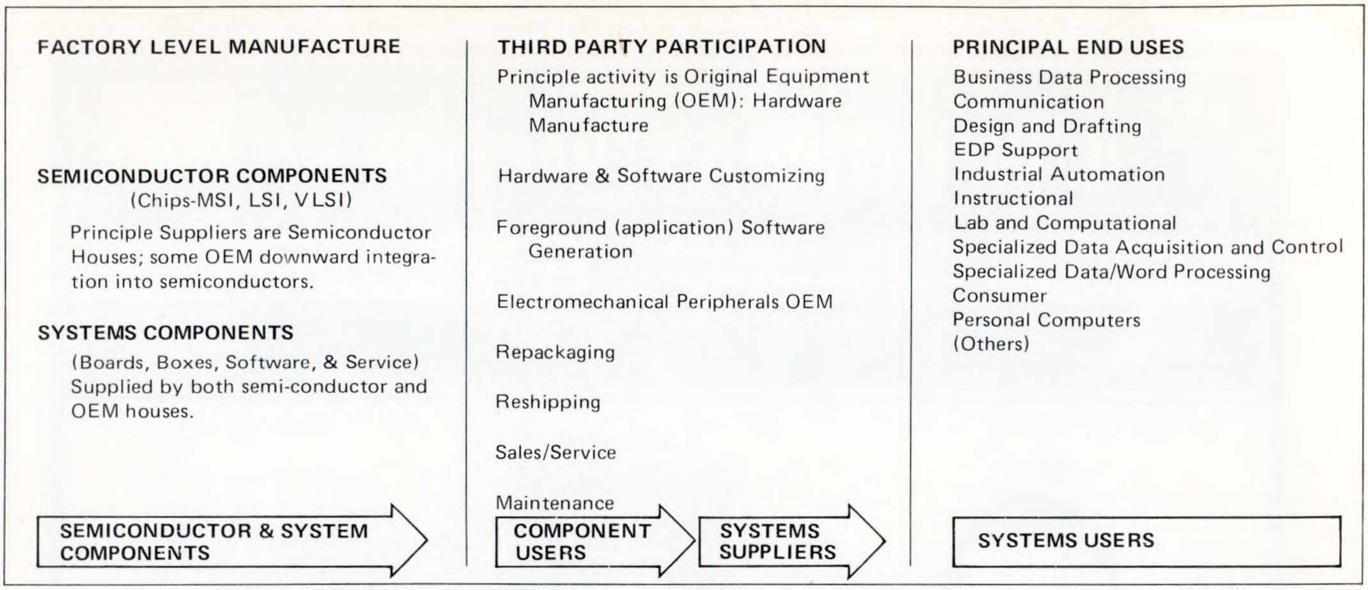

Fig 2 Typical flow of product-to-market for board and box level microcomputers involves a middle man.

as hardware. Programs in the lower performance ranges tend to be small and their development costs can be amortized over many thousands of systems. In the high end, the programs are much larger and unit volumes are lower. This point is illustrated by the current situation in computers in general. For mainframes, minicomputers, and microcomputers, hardware costs are 15%, 40%, and 75% respectively. Thus, the higher the performance, the greater the software cost. For all three categories, that portion of sales revenue directly attributable to software is on the increase.

The performance of the newest high performance μPs is in the gray region between micros and minis. Suppliers of high performance μPs are taking advantage of the inertia imposed on minicomputer suppliers by their large installed base of hardware and software. They do this by offering lower cost, modern software capability, and innovative architectures.

Microcomputers

LSI and the soon to be available VLSI (Very Large Scale Integration) are eliminating the number of chips used in a system dramatically as additional system functions are reduced to silicon. The building of low and medium performance systems has been greatly simplified to not much more than selecting a few semiconductor components and putting them together. The μP and other VLSI products are, at the same time becoming more complex, yet they are being used for a wider range of applications in different industries that are becoming less familiar with the increasing complexities of computers. These types of users are no longer simply looking for semiconductor components. They now are concerned with buying a **function** and they don't care whether it is on a chip, on a board, or in a box. They are prepared to buy the hardware and then add their own area of special expertise to arrive at a marketable end use product.

The market is beginning to search for products in which the processor will be more transparent to the user through the use of high level languages, thus allowing software transportation between competing products. Emerging component markets and traditional systems markets are becoming less and less distinguishable from each other. This is now leading to some changes in the traditional Factory-to-OEM-to-End-User flow of products. "Third party participants", who have no desire to perform the classical OEM hardware manufacturing function are beginning to emerge. This has led to the development of a generation of microcomputer board and box level products supplied by both traditional OEMs and semiconductor companies. Microcomputers are an outgrowth of semiconductor component evolution and depend for their existence on applications having high volume relative to minicomputers. Microcomputers are by design aimed at high volume, low cost, "just enough performance" applications and depend on generating volume by providing cost effective solutions.

This second tier industry is well established and suppliers are beginning to concern themselves with bus standards, second sources, etc. That is, they are regarding the microcomputer as a *component* rather than a *system* and the goal is to achieve similar kinds of standardization. It remains to be seen whether or not the market needs this new concept, except perhaps in the area of software transportability. This is, at any rate, an area in which 1980 may well be the shake-out period.

Personal computers

Personal computers (broadly defined as systems affordable by individuals and intended for personal rather than commercial use) were expected to develop a major impact in the market in 1979. While over 500 thousand units will be purchased in 1979, personal computing still has not gained the wide acceptance that was predicted. This has caused a number of smaller suppliers to re-direct their attention toward commercial small business applications. Several of the slower entering large firms, particularly the semiconductor houses, also appear to be foregoing the personal computer market in favor of the more profitable small business arena.

The unexpectedly slow acceptance of personal computers can be attributed to two factors. The first is the lack of a suitable network of retail outlets that would provide effective after-sale service. Only Tandy, with its TRS-80 series and ubiquitous Radio Shack outlets, has successfully marketed personal computers in significant volume. The second limitation is related to ease of use. Personal computers still are difficult to use for the non-technical operator. The best available products require owners to be computer programmers. In order to gain wide acceptance, personal computers are going to have to acquire rudimentary speech recognition and some synthesis capa-

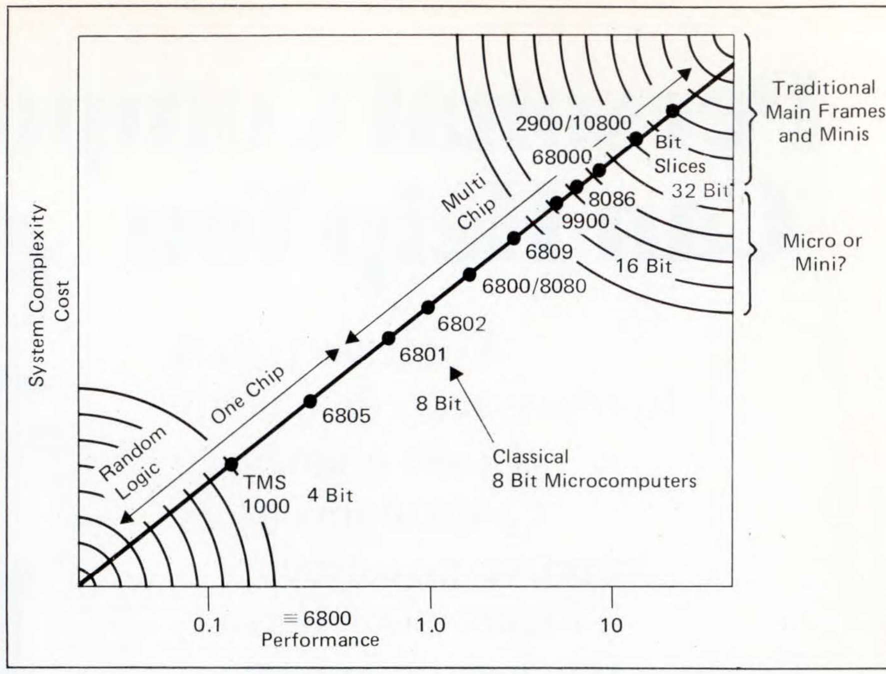

Fig 3 Relative system cost as a function of device performance. Performance normalized with respect to 6800, 8080 classes.

bility. These capabilities are available through present day semiconductor technology; however, their development has been slower than expected. Experts are still predicting that personal computing will grow at a rate greater than 60% per year, but 1980 may be disappointing because volume production of cost-effective speech circuits is still some time away.

Capacity crunch

Semiconductor manufacturers have, in a sense, done their work too well. They have continuously improved and refined their technology and manufacturing processes so that they are now able to provide a wide variety of products. The presently available cost-performance range spans the spectrum from the under \$5.00 μP aimed at dedicated applications (National COPS, Texas Instruments TMS 1000, Intel 8021, Motorola 6805, etc.) to μPs that can perform with the CPUs of present generation minicomputers (Zilog Z8000, Motorola MC68000, etc.)

Integrated circuit densities have also increased by at least two orders of magnitude during the past ten years; and an additional order of magnitude increase is expected within the next four years. The lower-cost products resulting from these advances have stimulated a demand that is being translated into expanding markets for electronic products. They are eliminating restraints in established market segments and opening up whole new areas. In many instances, newly created demand has quickly exceeded the capacity to supply. Even the threat of a major national recession has failed to quench the industry's appetite for silicon. Capacity limitation is easily the biggest problem facing both suppliers and users in 1980.

The semiconductor industry is being accused, with some justification, of failing "to put its money where its mouth was" by not developing adequate capacity in a timely fashion. Because of the characteristic long-range planning of the automotive industry, their massive μP and μC needs have been known for some time. A rapidly-growing high volume consumer segment was also predicted. Early acceptance of new high performance 16-bit processors was expected and timely capacity was added to handle this. But manufacturers were caught unprepared by the higher than expected demand for some of the older, mature standards. And the capacity crunch was increased by an unexpected demand from all quarters. The industry it seems, is not quite ready for the greater than 60% growth rate that occurred in 1979 and which is expected to continue during the next few years. For 1980, at least, users should be prepared to scramble for products. They may also see rising prices, a rarity for the semiconductor business!

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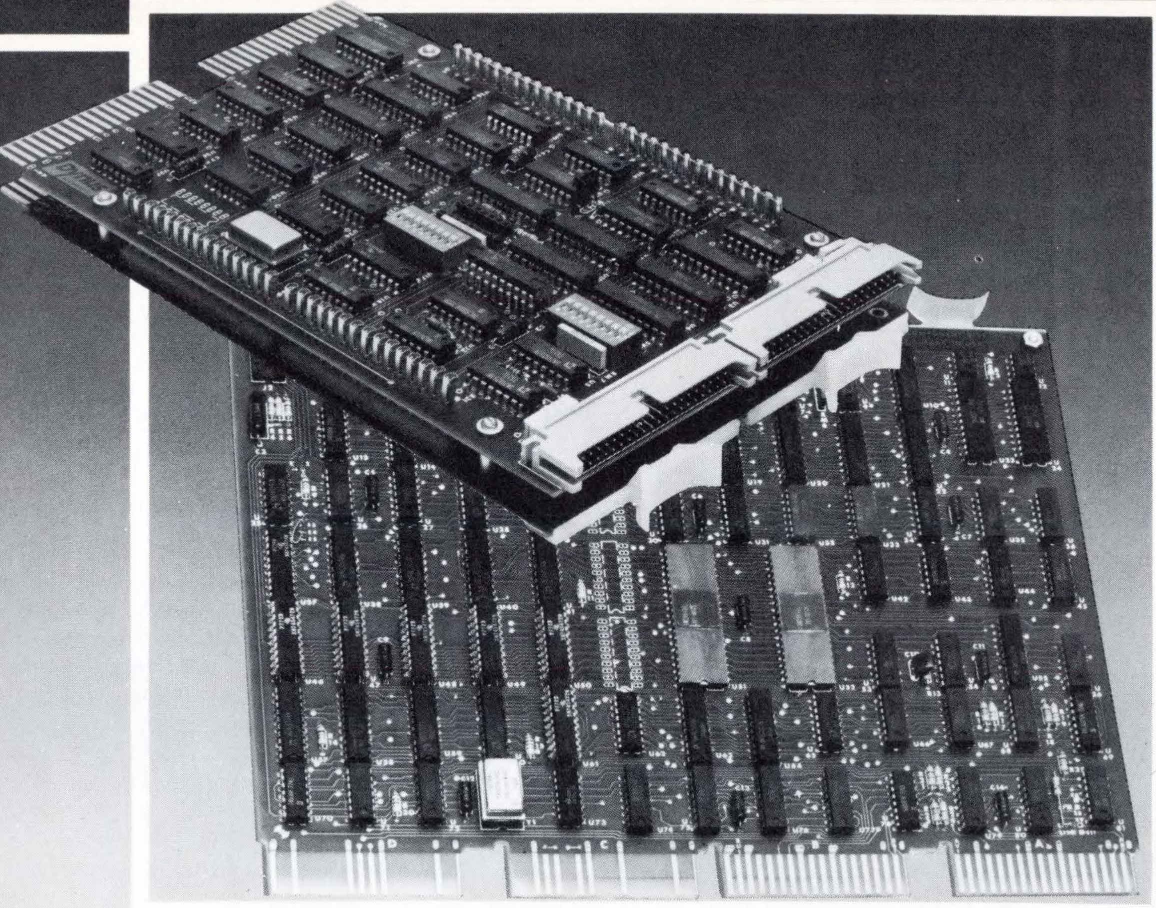

Alphanumeric Data Terminals

Low-cost "smart" terminals to proliferate

K. Phillip Hwang
TeleVideo Inc., Santa Clara, CA

By far the most significant event in 1979 in the Data Terminal Market was the introduction and shipment into the marketplace of the low cost "Smart" data terminal. The design of the data terminals to include the latest "State of the Art" in μP technology now places this formerly high cost feature to data terminals in the reach of everyone, expanding the market and supporting the growth trends projected for this equipment market.

The past. . .

Designed for high volume mass production and low labor content, as well as taking advantage of semiconductor techniques to provide all the "Smart" features offered in any data terminal, the series of data terminals that came into the market in the early 2nd quarter of '79 proved that well designed and economically produced terminals were an attractive product for the market.

The real "secret", if there is one in this type of "smart" terminal, which can offer all the editing and visual attributes of terminals listing hundreds of dollars more, is the proper implementation of an engineering design plan that has been targeted for high volume mass production and ease of assembly. With this modular approach, maintenance cost is low because of a low MTTR and high module reliability. Looking at the current market acceptance of these products only reinforces the conclusions that smart terminal featuring is applicable to *all* kinds of uses and not just the sophisticated high technology application. Most office environment users feel that a μC coupled to a smart CRT and small printer offers the low cost "do it yourself" WP system. That is why features offered – such as character and line insert and delete, line and page erase, send line and page, tabbing, conversational and block mode transmission, line, local keyboard selectable, protected and unprotected fields, reverse video, underline and blink and blank (formerly available only in higher cost terminals) – now make the smart terminal available for every application (including computer hobbyists).

Another major factor in the terminal business in 1979 was the increasing demand coupled with increasing lack of availability that has extended lead times on some products up to 120 days. This means that high volume mass production designs are eventually the real solution to the expected rapid growth of this dynamic market.

. . . and the future

What can we look to for the future? In 1980 and 1981, applications and demand for CRT data terminals will grow. The trend in the CRT market is toward low cost with high performance; in today's inflationary spiral, products that will become accepted are those offering this high value and performance ratio to data terminal users.

This same rationale applies to OEM system companies who will prefer purchasing low-cost, high-performance terminals rather than invest in costly capital equipment and engineering skills to develop their own product to compete in this upcoming low-cost, high-performance marketplace. The future is bright and growing. The opportunity for successful growth of the market share for those who have made the investment in engineering design and volume production is good.

Will CRTs challenge graphic terminals?

Paul Snigier, *Editor*

With 16-bit micros growing in power, with upcoming 32-bit micros and with widely-available 64K RAMs available by 1982, a new trend to more intelligent terminals with limited 3-D images will accelerate. With so much number-crunching capability and inadequate software to date, true graphic capability has been confined to higher-priced graphic terminals. This will change, and the next 24 months will see this trend emerge; and by 1984, the trend to intelligent terminals with limited 3-D graphics will become a factor.

The future of graphic modeling? I predict lower-cost units available in new industrial and commercial applications. Graphic modeling will occur in low-, medium- and high-end applications. With greater processing power, better algorithms and software, better texturing, improved blending (to avoid double imaging, size changes, edge wobbling, etc), costs will continue to fall, until these displays are affordable by markets now untapped. Costs will plumet.

Increased intelligence and greater processing power at lower costs is having an effect upon computer graphics; and computer displays now produce color pictures in full 3-D, with dimensional capability approaching that of photographs in their realism. Will stick drawings remain the mainstay among CAD/CAM users? Yes, although improved software and newer computers are making realistic displays at lower cost more attractive to users. Low-cost CAD has already come down to personal computers; and our editors recently evaluated such a unit (see "Self-Contained Profes-

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The Orion-60/S4.

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sional/Personal Computer Offers BASIC/CAD" in this month's Technology Trends).

Basic research can be borrowed by the CRT makers from pioneering work done by graphic terminal makers. Shadow placement, extensive calculations and perspective alteration – these and other techniques requiring extensive software have been overcome; and realistic displays are now being used to generate product promotions, instructional films, flight simulations, advertising materials and fill the needs of a sundry host of other applications that grow as costs plummet. CRT terminals will first use stick figure modeling with matrix multiplication for perspectives.

As for the high-end graphic terminals, programmers will define surfaces of objects; and clusters of these polygons will form the surface, with prioritization determining which polygon can mask which other one when maneuvered about in three dimensions. With surface definition via polygons now possible, the next step is to s imulate lighting effects, whether from a single source, or multiple sources, whether sunshine or indoor lighting. A vector of a given magnitude, which corresponds to polygon surface reflectivity, is defined such that it is normal to each polygon surface. Thus, vector magnitude defines the amount of reflected light. With a program knowing the position of the light source and the reflectivity vector for that polygon, it performs a scalar multiplication to obtain a scalar value to be associated with that polygon. This is the shading of that polygon.

The object, now comprised of a multi-faceted array of different-shaded polygons, begins to resemble the object. To smooth out these polygons, software-smoothing routines alter the reflectivity vectors and break the polygons into pixels (small squares). Interpolation smooths the intensity over each polygon, creating a gradual transition of intensity.

By the later half of the decade, other low-end CRT terminals will use other techniques, such as solid-description geometry, where fundamental geometric shapes (cones, cubes, pyramids and spheres) with software adding or removing elements. This creates the final shape. Instead of a matrix of vectors, this solid description geometry (used a good deal in CAD/CAM) stores in memory an array of separate solid characteristics.

As for 3-D motion, don't expect much outside of graphic terminals; and even with some of the larger machines, using software to perform the numerous calculations needed for realistic and continuous motion, with an updating of frames at a sufficient rate to avoid jerkiness, is certainly asking the software to do too much. Instead, dedicated software is used, and utilizes pipelining and can handle large vectors or arrays of data. A single instruction can perform an operation (such as multiply, subtract or add) concurrently on a large array of data. A data block passing through the pipeline processor is first operated upon by one operation, followed by a second, and so on, with subsequent data blocks following behind it. When the pipeline is full, the first data block will be outputted. Lower-cost array processors should provide increased number crunching capability needed and will lower overall graphic processing costs.

When will low- or medium-end intelligent CRT terminals develop 3-D motion? Certainly not in the foreseeable future.

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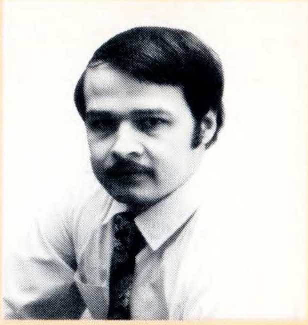
Paul Snigier, *Editor*



Add-In/Add-On Computer Memories

Traditional add-in/on computer memories, so critical to system integrators, are going through sudden change.

"It was the best of times, it was the worst of times. . ."
A Tale of Two Cities
Charles Dickens

The add-in memory and add-on memory market never looked so good for OEMs and end-users – and so bad for independent add-in/on memory makers. A price war, chaotic parts shortages and stretched lead times – all these and other factors (such as mini makers following IBM's aggressive memory price cuts) have sent independent add-in/on makers reeling. Some have (or will) quit the business; others are diversifying.

Independents in a vise

Pressured by mainframe and mini makers' price cuts and their new marketing strategy on one side and on the other by a growing number of IC houses going into systems, and with so many independents competing in what once was a good market, the minicomputer add-in/on market will be hit by lean times.

Other factors also spell gloom for independents. Historically, independents sold memory at two-thirds to a half of mini makers. This is changing. Mainframe and mini makers, traditionally making little on CPUs but more on memory, are changing strategy and cutting memory while raising software costs. Although the market is growing (20%/year), the semiconductor houses have an edge over the independents and could emerge as the dominant force in the add-in/on market by 1985.

Will the above gloomy scenario come to pass? Probably not, since several areas are opening to independents. And, for you, the OEM (and end user), bargains in add-in/on memories have never been better. However, pitfalls exist. To help you avoid these pitfalls we have prepared this comprehensive report (the most exhaustive published to date) to help you select an add-in/on memory maker and to properly evaluate manufacturers' models.

Memory	1979 ($115M)	1985 ($353M)	Increase/Decrease
NMOS	63.9	63.0	–1.4
Core	21.7	8.6	–60.4
Bipolar	9.1	10.1	+11.0
CCD	2.2	4.0	+81.8
Bubble	1.6	12.7	+693.8
Other	1.5	1.6	+6.7

By asking add-in/on marketing managers and authorities for their estimates and averaging them, these results emerged. There are no surprises. All values are percentages.

Watch out

Some of the smaller independents offer as good or better memories; others are cottage outfits bombing the market with bargain basement prices. Lock into one of these and your troubles have just begun. Such add-ins may lack compatibility, provide different interfacing and not comply with specs. If speed is below specs, the vendor usually will replace it, but it's a hassle. A PDP-11 memory-expansion-only that's supposed to serve as well for SBC-slot expansion, but that you suddenly discover doesn't, can hold things up.

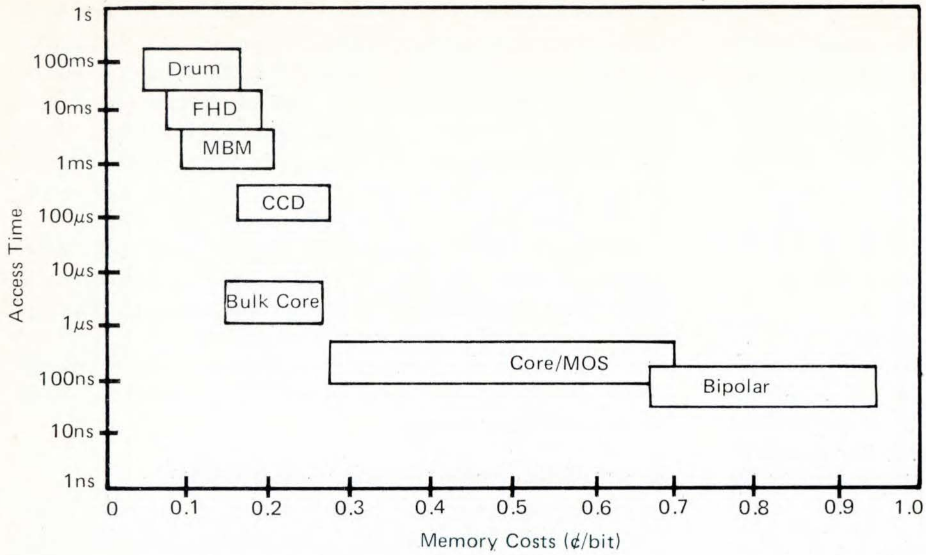
Then there's customer support. For many small garage-type outfits, it's minimal or doesn't exist. Intel has its own service force; IBM does; and since using an independent add-in/on memory maker adds a second vendor, then third-party maintenance can make for some interesting finger-pointing games when something goes wrong. Of course, the way things are going, there's the possibility this won't matter; many independents won't be around in a few years to service anything. And even if they survive the near-term shakeout, what happens in several years when IBM, DEC, Data General and others catch up with their backlogs? A bargain board or box whose maker won't be around in two years is no bargain.

Company reputation and the determination and ability to survive in a tough market are good signs. If overall systems cost savings of an independent is, say, under 3%, can you as a user risk this against the security of one-vendor service? But there is another side. . .

Independents offer advantages

Users want memory now; what DEC or IBM announces that's two years off due to staggering backlogs is no help today. While playing catch-up, they cannot supply enough additional memory.

But independents tout more than faster delivery and lower prices. They offer easier financing terms, will lease for shorter periods (6 mo. vs. IBM's two-year minimum), will sell in smaller increments, will add more memory per system, may supply unique technology and offer additional features. Now, with all this going for the independents, you would expect computer makers to oppose them.



With decreasing access times and falling cost/bit, all AIM/AOM memory categories will migrate toward the lower left origin. Certain categories — such as magnetic bubble memories (MBM) and fixed-head disks (FHD) — will decrease in cost more rapidly than others, (such as CCDs, which appear to be long-term losers). MOS and bipolar will overlap more, but MOS add-in/on memories will remain more popular.

Do computer makers hate independents?

The computer-independent memory maker relationship is one of love-hate. To ship more units, computer makers will put less memory into a system so they can ship faster. They let independents take up the slack, which has helped the computer makers, who the independents feel should be thankful for bailing out customers in need of memory and keeping them from buying, say, DEC minis, getting mad at DEC and switching to Data General. But times change, and at this stage, many mini makers see independents as taking business away.

Add-on versus add-in

Add-on memory, as its name implies, hooks onto the computer as an external expansion chassis that is often core. Add-in memory replaces memory within the computer and is inserted directly into the connector backpanels. These add-in boards are specifically designed to slide in with minimal effort and may have a mechanical cut-out to allow clearance for an internal fan assembly. Add-on memory, now fading from the market, is independent memory. A separate power supply in a separate chassis usually provides power, and the user's memory and interface board are in a separate enclosure, with a cable connecting it onto the processor bus.

How big are they? Add-ons may range from shoebox-size to large cabinets in the case of mainframes. Typically, memory modules and controllers are inserted in the rear of the expansion chassis or enclosure, which may include a backplane, power supply, cooling fan, programming plugs and I/O cables.

Add-on memory was once more popular for several reasons, and it is for these very reasons (which have grown less significant with each passing year) that add-ons are now fading from the scene. When semiconductor manufacturers made smaller chips, adding extra memory to a system added complexity, took more board space and value, and increased power consumption. With backplanes filled and without sufficient power for such added memory, the only alternative in many cases was an add-on memory.

With higher-capacity memory devices, the picture changed, and the larger-capacity boards proved cheaper for several reasons. For example, although two 64k add-on boards need two busloads (taking up another backplane slot), one single-hex 128k board for the PDP-11/34 takes one busload, thereby saving more than just cost. Additional power supply, extra chassis, interface controller card and greater size — these drawbacks of add-on boxes account for their waning popularity, not to mention their lack of flexibility.

However, actually selecting add-on memory is straightforward; add-in memory, more complicated. The reason for this is that add-on systems are treated mechanically as peripherals and have bus-compatible cable assemblies. Therefore, the add-on box generally can be added to any computer (of that manufacturer's family) simply by breaking the bus chain and inserting the add-on system. On the other hand, add-in systems require more careful selection to ensure complete compatibility — that is, interfacing, electrical, electronic and mechanical. The greater variety offered by add-in memory makers means your choices are better, but it is also more reason for taking greater care in selecting.

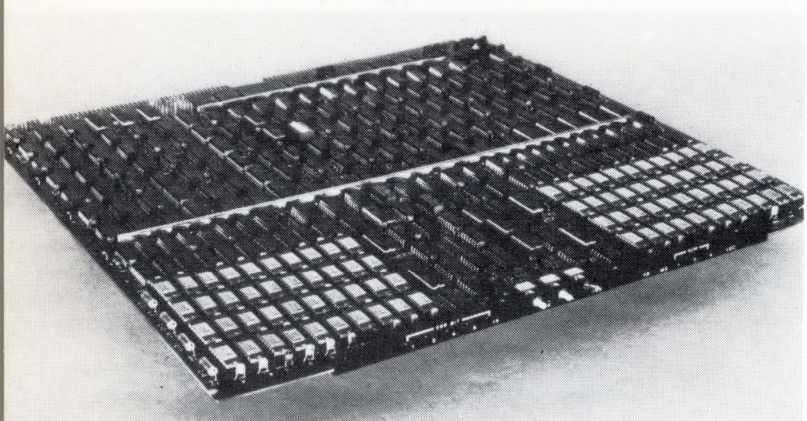
Will add-on memory die?

Despite the trend away from add-on boxes, there is a niche for such add-on memories: in higher storage-capacity systems. In such systems, such as the VAX-11/780 or PDP-11/70, since users address a lot of memory, and since it's often impossible to add in an extra megabyte or so of memory, then the most economical way to enhance computer performance is with an add-on system. If a user starts out with a minimum amount of memory, but anticipates large memory expansions immediately (or in the future), then selecting an add-on system makes sense. If future memory expansion up to the maximum addressable is contemplated, then a single model (or combination) will permit incremental expansion as needed. Such units will typically fall into one of three categories: (1) for the PDP-11/70-type, *large* would be 512k on up, (2) *medium*, 192k or 256k or so and (3) *small*, at 64k or 128k or so.

Through use of memory interleaving, system throughput is raised. Interleaving, the splitting of memory into two (or more) sections with two paths to the CPU, speeds processing; it lets a second word be read while the previously-read word is being written back in memory. Interleaving takes full advantage of the asynchronous nature of processors; this allows, as we said, for simultaneous R/W from different memory sectors at the higher speed of the expandable memory. By providing two-, four- or eight-way internal interleaving, or external interleaving with DEC or other plug-compatible add-on memories, the faster effective cycle time increases throughput (by 15% or so for four-way internal interleaving). Other add-on memory makers claim a 30% faster-than-rated-maximum for the PDP-11 with fully-interleaved systems.

The success of the PDP-11/70 is partially due to its easy upgrade path, not to mention its versatility, since it is just as suitable in an office environment or front-ending for a mainframe. But no mini lives forever. The 32-bit, (4 Gbyte virtual address space), top-line VAX-11 machine will eventually replace the PDP-11/70, whose 16-bit addressing limitation prevents addressing a lot of real store.

By assuming a long-term 50% drop in memory cost/bit/year, this means an increase of one extra bit of physical address/year is needed; hence, 32-bit (not 24-bit) virtual address was chosen by the VAX designers, who also made this address space linearly addressable. With memory capacity/chip rising and long-term costs falling, the VAX-11/780 should continue its growth throughout the 1980s until the size of typical physical memories approaches the virtual address space. I use this example to illustrate the move of mini makers into the 32-bit arena as a possible niche for add-ons' survival.



Intel's 5150 multifunction add-in memory board features on-board cache memory, cuts cost and improves memory system performance for the Data General Eclipse.

A brief aside. Virtual storage, a storage management technique first used in 1974 on the IBM 370, allows the CPU to have storage capacity many times that physically in the CPU. By breaking the program into segments external to the CPU, and calling the segments (or pages) up as needed, memory costs are cut, the computer can process longer programs than could originally be physically stored in the CPU memory, thus extending computer processing power and cutting memory costs. Virtual storage is like reading a magazine page-by-page, with the only trouble coming from the number of times to turn pages; the more movement in and out of the CPU (swapping) of these sections of coding, the more time-consuming it gets. Many mainframes provide large virtual address spaces but break them into many segments. Since the VAX-11's address space is linearly addressable, there is no further segmentation. Unlike the mainframes, the PDP-11 operating system needs little virtual memory management; the small programs are often swapped en toto. The VAX-11, on the other hand, has large virtual address space, and programs often will be larger than the system's physical memory. What will the 32-bit minis of the 1980s be like? Much like today's medium mainframes — a megabyte of central memory, 100s of megabytes of disk storage, etc.

What does this mean for the add-on/in memory makers, OEMs and end users? Perhaps a different perspective. Certainly, the 16-bit micros — more and more resembling minis — offered by semi makers like Intel, National, Zilog, Motorola and Texas will need add-in memory, and is one reason why these firms are vying for a share of this market. When will the micro makers alter their memory and software marketing strategy to follow the DECs and Data Generals (who, in turn, have begun to follow IBM's footsteps)? Soon.

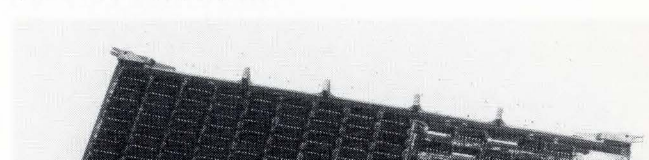
Although IBM's strategy will impact semi and micro makers indirectly at first, in the long term it will strongly affect them, despite their present protestations to the contrary. Also, since semi-makers-turned-system-makers are moving into a direct head-on clash with mini makers in the 16-bit arena, the semi makers will be forced to adopt a similar marketing strategy.

Buses make memory expansion possible

One thing that will not be affected that much by such change is buses. When adding in/on additional memory, the key to this is the bus used by that particular computer (that is, the added memory must be bus-compatible). Since most add-in/on memory is designed for the PDP-11, I will use the PDP-11 "Unibus" for my example. The PDP-11's Unibus structure, one of the PDP-11's original strengths, enabled everyone and his uncle to attach peripherals to it.

In all PDP-11s, Unibus, chained from element to element interconnects everything. Since it is a transmission line, with all the problems of reflection and unwanted multiple switching from impedance mismatches, it must be terminated at the end of the chain by a resistor network. Signal connectors (A and B) at each connector assembly input are wired compatible with Unibus, as well as the A and B output connectors. This accounts for the 11's building-block modularity. Peripherals are wired just like connectors, and have two or more input connectors for a bus cable. The peripherals each have two A and B output connectors to continue the bus, unless, as we said, it's the end of the chain.

If we want to add peripherals or memory or Unibus-compatible connector assembly, we can break into the bus anywhere. Although the I/O A and B connectors are Unibus, the internal A and B connectors need not be. In the PDP-11/34, A and B connectors on the single-board core and semiconductor memory systems have a Mudbus (modified-Unibus) interface. Internal connector assemblies for 11/34 memories have this Mudbus interface. Is system compatibility a problem? Not if Mudbus is connected to Unibus at the I/O A and B connectors.



This Mostek MK8012 add-in memory system for DEC's PDP-11 features density up to 128K words X 18 bits on a single board with a parity option.

What do two such interfaces mean for add-in/on makers? They should offer both, since boards inserted into internal connectors must conform to that connector assembly's Unibus or Mudbus interface.

Add-on memory multiprocessing systems

Add-on memory systems with a dual-port option enable two CPUs (or one CPU and a direct access peripheral) to access one plug-compatible expansion memory through its Unibus. Since each system Unibus has its own CPU and probably its own resident memory and peripherals, one system accessing the add-on expansion memory won't stop the independent operation of the other. By using two or more add-ons to three or more slave CPUs, system designers may configure multiprocessing systems to a specific application.

The add-on memory future. . .

Although add-on memory is quickly disappearing from the memory scene, it will survive. In the situation of an inadequate power source for add-on, or filled-up backplanes, then add-on makes sense, since it takes only one slot. Disk emulation will remain an add-in stronghold. Basically, a full system, with controllers, doesn't lend itself that well to an add-in approach.

Although the add-in approach is cheaper (no extra support, cables, supply, enclosures, etc.), with large capacity memory modules, the emphasis shifts to the add-on approach. But a warning for independents: they will find increasing competition from semi makers like Mostek when they design add-on systems.

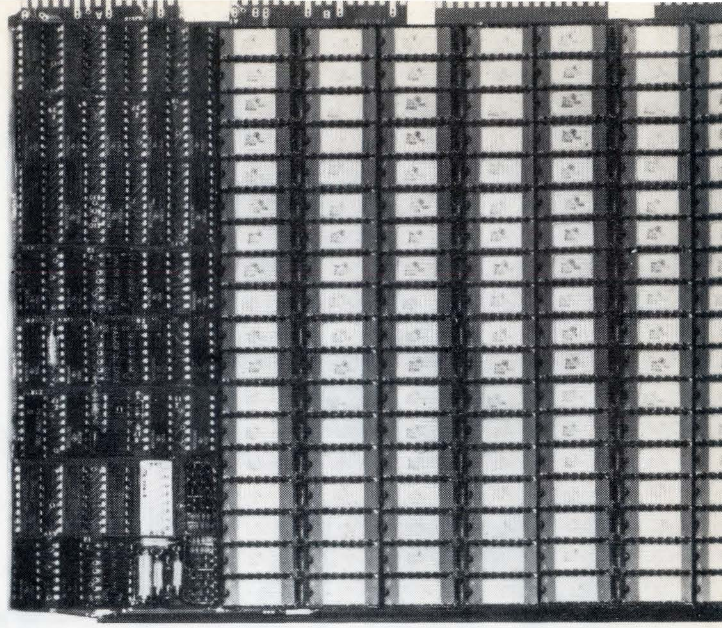
Solid state disks

Solid state disks are a form of add-on memory and are core-, CCD- or RAM-based (with bubbles expected to come on strong). CCDs are being replaced by 16-k RAMS, aggravating a shortage already made worse by unexpected demand, multiple ordering, IBM going outside for 16k RAMs and Intel's switch to more lucrative UV-EPROMs and static RAMs.

If your system will be accessing data stored in peripheral swapping devices a lot, the cumulative delays from accessing and transferring data into the computer will seriously lower throughput. The rotational (and positional) latency of fixed- and moving-head disks slows accessing information. Must the sub-μs processor wait around for a pure rotational latency (8.5 ms or so) of a fixed-head disk? No. The way to increase system performance is through solid state disks, with megaword capacities and speeds typically 4,000 to 8,000 times faster.

Such add-on systems typically consist of controller, card rack, power supply, blowers and logic modules permitting future expansion. If possessing dual-port capability (two controllers), two computers can access the solid state disk, with simultaneous access through both ports. Such systems are transparent to the host computer. Control signals are transmitted from the CPU; status signals, to the CPU; and few (if any) programming or electrical changes should be made.

You should consider using solid state disks for several advantages: (1) increased system throughput (higher process sytem control loop bandwidths, greater data acquisition system sampling frequencies, etc.), (2) environmental – atmospheric and ruggedness – reasons, (3) negligible maintenance costs – motor bearing failures, head crashes, etc., (4) ease of expansion, (5) increased system availability – more communication lines/processor in data communication systems), (6) increased uptime, (7) elimination of redundant devices and (8) applications (eg, seismic processing) that require buffering high volumes of real-time data. The disadvantage? Extra cost.



Dataram's 128K X 18 DR-113S semiconductor add-in for the LSI-11/23 typifies the new μC boards.

Add-on/in cache

Cache (buffer) memory lets a computer incorporate both high speeds and large memory capacity. To maximize memory performance and minimize cost/bit, a performance-cost hierarchy of memory is used: (1) at the bottom is slow, low-cost bulk storage (disks, tapes, bubbles) to minimize cost, next (2) processor NMOS RAM main memory and finally (3) high-speed, high-cost cache memory (typically bipolar). A fourth category, buffer storage (CCD or bubbles) could operate between main memory and cache to minimize main memory.

Since certain memory locations are accessed often, to speed system throughput, a small-but-very-high-speed memory buffer between processor and main memory stores (buffers) contents of the most-recently accessed addresses in a scratchpad within the cache. Now, the trick is to transfer large batches of data into the small memory in one cycle. When the processor presents an address, the memory checks its cache for data; if resident, it's accessed quickly; if not, it initiates a normal memory cycle and reads data into CPU and cache.

Now, if the cache always contained data required by the processor, performance would be 100% (all "cache hits" and no "misses") with minimum system overhead due to storage access. In reality, no such thing occurs and performance ("hit ratio") may be half the theoretical maximum (more with a larger cache). For example, with a 2-kbyte cache (290-ns access time) and 2-Mbyte main memory (500 ns), 95% of all memory accesses find the data in cache; and the memory system behaves like it's 2 Mbytes of 310-ns memory. This provides a memory system performance improvement of 38%. By way of comparison with minis, all 4300s have an 8-kbyte cache.

Generally, program instructions are in sequential locations and blocks of data are in successive locations. Although mainframe cache can improve processor speed three- or four-fold, minicomputer cache (which is smaller) may only double it.

Cache buffers are offered for minis, such as the PDP-11/45 and save the user from having to shift to an 11/70 for an equivalent processing speed increase. By using an on/off-line switch, users can run benchmarks to determine the difference (or for maintenance checks). A cache register also should permit (dis)enabling cache software control. Incidentally, independents offer cache as both add-in and add-on. For comparison, one independent's 2-kbyte cache is a PDP-11/45 add-in; another, an 8-byte cache, an add-on.

With a view to keeping the ratio of bipolar cache to main MOS memory constant, some memory expansion boards contain both, so that adding memory modules won't alter this ratio.

One advantage of an asynchronous memory cycle (more common on minis) is that the system can operate as fast or slow as necessary, so that system throughput can easily be increased by upgrading the memory by adding cache memory (or using faster main memory). In any event, cache memory was first developed for mainframes and now minis. High-end micros by the mid-1980s should commonly use add-in/on cache, and will exhibit more minicomputer and even mainframe features. Distinctions will blur.

When should an OEM or end-user look at add-in/on cache? Whenever his system needs the extra reserve to prevent bogging down during peak CPU loads. Or, when all the number-crunching power he can get is needed. In selecting cache add-in/on memory, choices involve balancing several factors — add-on vs. add-in cache and increased performance and *overall* saving vs. added cost. Other factors to consider include increased demands, added main memory, decision to replace the present computer system and extended delivery dates due to backlogs.

The future of cache? Expect to see new, higher-speed, thrifty MOS emerge to challenge TTL and commonly-available, off-the-shelf, lower-power and affordable ECL showing up (as well as ECL-compatible MOS RAMs). The battle for cache may see fast MOS lose some of its power advantage, although its low-power standby feature will lower dissipation. As cache memory size grows, and with more statics in main memory, dissipation will become a factor to be reckoned with. High-speed, power-down MOS with a ten-to-one switching ratio (0.1-to-1 for bipolar) make cache layout design a nightmare. For now, the next generation for high-speed cache will be the 16k X 1 static RAM.

General purpose memories: flexible gap-fillers

General purpose add-in/on memory provides various configurations for general use. Since they must be flexible for the many possible OEM/user applications, standard features generally include the following. **Switch-selectable address range** is a must, since for maximum flexibility in system configuration, starting address and memory size must be selectable in increments. For **TTL-compatible interface lines**, data output lines are open-collector and respective data I/Os can be interconnected, forming a bi-directional data bus. **Byte-control capability** allows independent R/W on each byte. Each byte may be up to a given maximum. If dynamic, an **internal-external refresh switch** enables the memory to refresh its RAM automatically from an on-board clock that automatically inserts a refresh — or to avoid conflicts between refresh and cycle requests, can be switched to external refresh to synchronize refresh with the processor.

Battery backup protects data during power-off or failure. It may be from separate battery backup inputs or internal. One mode may employ a constant output at lower voltage; a second, the burst-refresh mode would supply far less current.

General-purpose add-in/on memories aren't as common as the rest, but do provide flexibility for applications requiring access to large banks of data that can't be met by other auxiliary modules or boxes. However, expect to pay: such flexibility comes at added cost.

Terminals need auxiliary storage

Upgrading high-end terminals and graphic systems will become increasingly-important for OEMs and end-users in the early 1980s. Such add-ins tend to be more dedicated than other add-in/on systems, but will respond to future price cuts.

With makers shoehorning more capabilities into their terminals, and with graphic systems increasing, and with the need for enhancing terminals, add-in/on memory for terminals represent a growing market. Graphic systems, with their need to run large programs, need additional workspace area to generate more effective graphics and manipulate large amounts of data. With add-in memory, programming time is cut and program revision made easier. Shoehorning a program into 8k and wasting programming time — when add-ins could easily expand the memory — is unwise.

New game, new rules

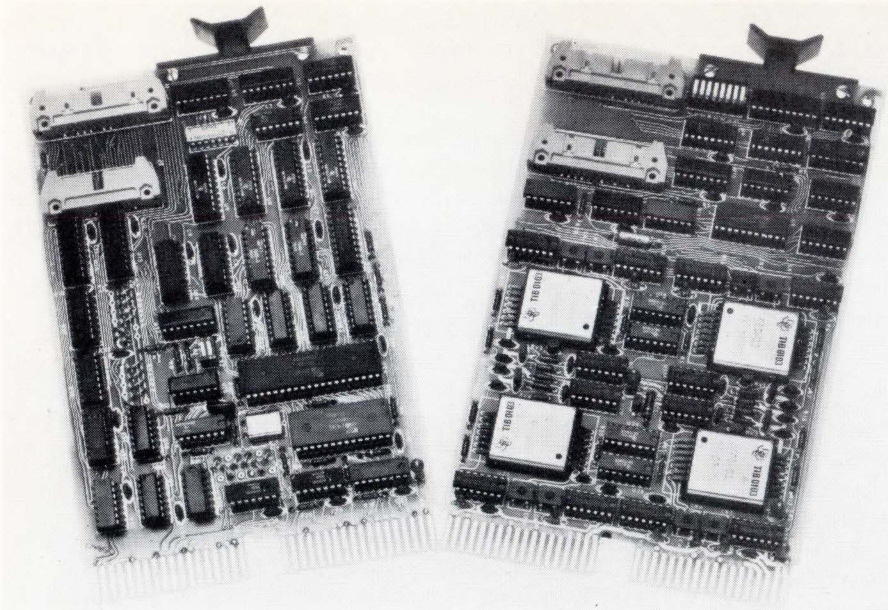
Since rising software development, plumenting semiconductor prices and blurring computer-communication distinctions are occuring, the semi (micro), mini, mainframe and communication fields will merge as these firms integrate vertically to survive. They will awaken in the mid-1980s to discover themselves in competition.

IBM's unbundling portions of its operating systems and all its software maintenance services, charging a monthly fee for software capabilities (previously free), and its slashing memory costs represents one stage in this inevitable scenario. With semiconductor prices falling and software costs growing, the shift was inevitable. With further memory price cuts expected, a series of memory price reductions among the mini, micro and eventually semi house will continue, prodding them all to integrate upwards even faster.

Although users can anticipate higher software and support costs from all computer makers, falling hardware costs will more than compensate.

Some independents forecast increased sales for themselves as users anticipate 4300 deliveries and the mysterious H-Series. The 4300 has forced users to make decisions; and, as they await 4300 delivery dates, many will opt to upgrade their current installations. Despite the downturn in earnings for independent add-in/on memory makers, caused by the 4300 announcements, perhaps the longer-term outlook is bright. The large independents will do well.

But what about the H-Series? Rumors say it will have so much memory it will make today's mainframes look positively pedestrian. This means that 158, 168 and 303X users will want to retread with several megabytes of add-on memory. It's possible that the H-Series will create a need for add-on boxes. Then again, if IBM uses a 256-k RAM in its H-Series, the memory prices will plummet once more and a $2,000/megabyte price is distinctly possible. Whatever the outcome, *these changes will affect everyone* from semiconductor and microcomputer makers to minicomputer and system manufacturers.



The MBB-80 magnetic bubble memory system provides 92,304 bytes of non-volatile mass data storage, and is memory-mapped for CPU control. Each MBB-80 requires 16 memory locations in the μC address space. As few as one or as many MBB-80 modules as desired may be incorporated into the μC system to provide the required non-volatile storage capacity.

Not "apples and oranges"...

IBM, by far the world's largest maker of semiconductors, is said to have developed the μP two years before Intel's 4004; and while other semi makers grappled with 4k memories, IBM was mass-producing 8k RAMs for in-house use. No one cared that much, as long as these developments were used in-house and didn't upset the ballgame for everyone else. With IBM producing almost as much memory chips as everyone else put together, and mass-producing 64k RAMs while everyone else cannot get 16k RAMs, let alone the 64k RAMs, the news that IBM is going outside for 16k RAMs is not reassuring.

IBM, traditionally good on service, has extended its advantage over independents with lower-priced memory. The \$15k/megabyte barrier reached by IBM, as shocking as it was to the independents, was discredited by edgy independent spokesmen. But if it is an "apples and oranges comparison" for mini add-in/on makers, as some claimed, they still have every reason to worry: IBM's price cuts are about to enter the minicomputer add-in/on market. IBM's General Systems Division hasn't been idle, and its price cuts in purchase (32%), lease and rental (19% or so) for memory increments include the System 13 and 34, 5100, 5110, two Series 1, 3741 Data Station and 3747 Data Converter. DEC, Data General and other mini makers, owning more of the mini market, are under less pressure than independents, but are forced to follow IBM's pricing and marketing strategy (i.e., cut memory prices and raise software prices).

Although mini makers *claim* that IBM's price cutting had little effect on them, they've also begun cutting their prices. DEC cut 20% off its DECsystem; H-P, 40% off its HP-1000 (dropping its memory from \$32k/MB to \$18k/MB); and Data General is cutting its Eclipse series. H-P's 3000 and 300 were cut by 12-14% (with add-on memory prices dropped), and H-P has altered its software support program. By the time this appears in print, expect to see more price reductions. And, by late 1982, expect to see a memory price per megabyte in the \$2k to \$3k ballpark.

With mini and mainframe makers forced to overlap each others' markets, and with mini makers prodded from below by semi (micro) makers invading the 16-bit arena, it's certain that mainframe, mini and micro makers will more closely resemble one another by the end of the next decade. Furthermore, IBM and AT&T will be forced into inevitable confrontation as the dividing line between communications and computer systems blurs even more – despite their denials. Computers or communications? Ultimately the users will decide, not IBM or AT&T.

It is my feeling that those mainframe, mini or micro makers who choose not to actively enter the computer-communications arena will grow weaker and be relegated to the sidelines by the end of this decade. Those semi houses that refuse to continue their vertical integration further will be relegated to component makers and will survive doing custom work or as the acquisition of a rich parent firm. Another factor, the Space Shuttle, will cut satellite communication costs drastically and open the door for these computer systems makers. To survive, IBM and later the rest, will be forced into satellite communications, with IBM dividing itself up by function (not product) categories. But that is a different story. Other more immediated problems confront the industry, such as partials.

Partials: yes or no?

With semi makers cranking out 64-k memory chips, a question emerges: what to do with scads of "almost good" RAMS? With a couple of bad bits on a 1-k RAM, junking it made sense; but junking partially good 64-k RAMS ("partials") when they can be saved for internal use as 32-k chips makes no economic sense. This is especially true, considering that yields are inherently lower for a greater-capacity chip, which also costs more to fabricate.

Now, since partials aren't a first-line product, semi makers have a sudden need for a product that they can manufacture that will use these chips, thus improving chip yields. Add-in/on memories are well-suited to this. This advantage in partials is just another edge semi makers have over independents. As of this writing, certain semi firms (Mostek, Motorola) condemn use of partials; others (Intel, Texas) say that there is no difference that they've detected.

Despite the stigma attached to partials by some semi makers, I feel that they will see increasing acceptance.

64K, 16K, 4K RAM shortages persist

Semiconductor memories remain the bread-and-butter mainstay of semi houses. Over half the U.S. market (\$1B last summer) for semis was in RAM sales, with dynamic

RAMs the largest, at \$300M. By contrast, UV-EPROMs were at \$100M; mask programmed, fusible link and EAPROMs, \$350M. CPUs and other family chips are still seen as a way to sell more memory. How will IBM and mini makers' new strategy to raise software prices and bomb memory prices affect the semiconductor makers? OEMs will benefit, users definitely will, and semi makers *claim* they are insulated from the mini/mainframe memory price slashing – at least in the short term. In the long term, the new strategy *will* affect semi makers. With less real profits in memory chips themselves, semi firms that expect to be more than mere component makers in the 1980s will be forced to accelerate their already-upward move into making higher-level computer systems.

The 16k RAM sales will peak in a couple years as the 64k RAMs become available in quantity. The industry-standard, 16-k, three-supply 4116-type memory is supplied by Mostek, Texas, Intel, Motorola (together producing 70%), and the Japanese (Nippon Electric, mostly) supplying the rest.

What are these semi makers doing about the shortages? Fearing overexpansion in the face of a long-predicted recession and growing 64k RAM production, most haven't increased 16k RAM production as quickly as they could have. Unfortunately, the 64k RAM didn't materialize as quickly as the rule of doubling chip capacity per year had predicted.

Delays in 64k RAMs occurred due to the quest for a 5V, single supply device; and some firms first worked on a 5V 16k RAM as a learning experience for their 64k RAMs, costing them development time and pushing 64k RAM availability into the future an extra year. But the problem is more fundamental.

The approximate doubling of memory size every year and the "learning curve" (n% price reductions for each doubling of total units manufactured) will no longer hold true. The game has changed, and it's not merely supply and demand that will alter the learning curve philosophy. Ballooning product development costs and design limitations will hamper VLSI. New lithographic technologies (direct-writing E-beam, X-ray, etc.) will be needed. Wafer-fabrication production module costs at \$10M and mask aligners at \$1M by 1985 may be the norm. Due to the amount of R&D and equipment costs needed to remain at the leading edge of technology, those marginal firms that aren't acquired or become specialized custom houses will fold. The result? Technology life cycles will lengthen due to these skyrocketing costs, larger application base and greater number of committed customers. Then, too, as we approach the limits of silicon more closely, progress will asymptotically approach the limit and the emphasis must be shifted to new architectures for memory (more about that later).

As if these changes aren't enough to make predicting the future of add-in/on memories a bit like reading tea leaves, other memory trends are being set by semiconductor makers. Here are the latest developments. . .

Bipolar memory: a trend to ECL

High-speed cache (and not main memory) uses most of the bipolar add-in/on memory, although higher-speed MOS is moving in, with fast 4k-static RAMs the first proving ground. MOS developments have prodded bipolar makers into action, and new technologies such as isoplanar-scaling, I^2L and integrated Schottky logic will extend bipolar speed, increase density and cut power consumption. Bipolar speed is diffusion-dependent in fabrication and consequently is easier to control than MOS, which depends on lithographic registration – inherently prone to greater variations. So, to get high-speed MOS requires skimming off the top MOS devices.

As a rule, memory devices trade speed for power; and MOS is no exception: high-speed MOS chips generally consume more power. Although firms – like Fairchild which is developing a 64-k static bipolar RAM for 1981 – are pushing bipolar, the consensus is that lower-cost, high-speed MOS will win out. Bipolar makers feel that device scaling (not circuit shrinking) will cut gate delays to 300ps.

A trend to ECL with its higher speed (due to its smaller voltage swings) is emerging, and more complex chips are on the way. If integrated Schottky logic memory chips can be fabricated economically with Signetic's ternary logic, could this lead to denser chips?

Prognosticating the future of semiconductors beyond two years is risky. Bipolar makers, like Fairchild, claim one thing; MOS manufacturers, like Intel, claim another.

MOS challenges bipolar's speed

Main computer add-in/on memories, which are mostly NMOS, fall into three categories – dynamic, static and pseudostatic. Although traditionally slow, new fast MOS RAMs will continue eroding bipolar markets.

Despite their increased complexity and refresh circuitry, **dynamic RAMs** cost less and dissipate less than statics. Access times for some 16k dynamic NMOS RAMs are at 80ns. Intel, the leader in the MOS speed race, is repositioning its emphasis from dynamic 16k RAMs to statics (further aggravating shortages). Any OEM who still sees the future of MOS in traditional terms (low dissipation, but slow) would be advised to look at the trends, of which the 4k X 1 2147-type RAM (55-ns access time) 4k 93F470 (30ns), 4k 2147H (35ns), 1k 93F415 (20ns) and 1k 2125H (20ns) will typify.

Bipolar will be hard pushed to keep up with new MOS speed breakthroughs and this will create a trend to ECL (sub-10ns) for high-speed buffers and cache memory.

Static RAMs are faster than dynamics, require no refreshing and are easier to design with, but are less popular due to extra cost. **Pseudostatic RAMs** combine dynamic (internal refresh) and static NMOS advantages, and permit accessing cells during refresh. If pseudostatics can move up into the 64k market soon, they will find a niche.

Finally, the advantage of single-supply, 5V-only, 16k and 64k NMOS dynamic RAMs cannot be overemphasized. They cut add-in/on memory costs by freeing up space now used for the extra 12V, so that the additional memory added will lower the cost/bit ratio. Competition for these devices could create shortages as memory makers compete for the devices at steeper-than-predicted prices.

CMOS backs up NMOS

CMOS, with its extremely low dissipation, will show up more as nonvolatile backup in case of power failure (18% growth per year). Backup batteries for NMOS are no panacea (a fact overlooked by too many end users). For the megabyte region, backup can be five to fifteen minutes, and periodic maintenance is needed to check batteries. OEMs too often forget to consider how much space the battery will take or even to include it in their cost calculations.

CMOS' lower junction temperatures and noise immunity suit it for severe environments. Unfortunately, CMOS never took off – except for watches and calculators – due to cost (25% over NMOS) and yield (it uses 10 masking steps instead of NMOS' 7). CMOS needs two transistors at each switching stage, making chips 35-40% larger.

Since CMOS reduces heat dissipation by 15¢/W – and since it cost $1/W of power supply and another half dollar per watt to dissipate the heat – CMOS looks attractive.

As for backup in case of power interruption – a concern add-in/on users will face soon due to oil shortages and nuclear plant construction slowdowns – these power interruptions will be taken into account more by the system designer of the 1980s when he is specifying add-in/on memories. NMOS, as we said, needs an expensive, bulky battery-backup system to preserve memory; CMOS, on the other hand, can hold data for seven days with only a few, tiny NiCad batteries.

CMOS is resistant to soft errors from alpha-particles of specific wavelengths. (See "New Static RAMs Combat Alpha Threat," by P. Snigier, *Digital Design,* September 1979, p. 24.) For development and small jobs (where a system crash only means hitting the reset button), it's not worth using conventional statics (2114, 2141) to combat the alpha threat; dynamic 16k RAMs will do. Then again, with ECC, most soft errors are caught. Single-bit error-correction produces an 85-fold improvement in memory reliability. When examining add-in/on memory modules, look for ECC detection/correction, error status storage for CPU access, LEDs to indicate chip row/column, error interrupt for multiple-bit errors, and various other options.

Core headed for extinction?

Core will always survive in military, aerospace, process control and in adverse environmental uses where nonvolatility and ruggedness count. Otherwise, core, a mature technology, will fall off fast in the face of semiconductor's plummetting prices. Ampex and Dataram stand to profit, taking up the slack orders dropped by those getting out. Core won't die, since custom and special memories will come to overshadow general add-ins.

Also, since old computers never die – they merely migrate to third-world nations – core may keep a toehold there throughout the 1980s. With embassy takeovers, riots and frequent blackouts a way of life in these backward nations, core's nonvolatility can't be beat. With battery backup times of ten minutes for 1 megabyte of NMOS, core looks attractive for these add-ins/ons.

For core memory makers, there's also another advantage over semiconductor: less cutthroat pricing. Still, dynamic RAM is selling for one-fourth core's price. For example, a 64-Kbyte memory is $695 (unit qty.); 64-Kbyte core, $2900. But core is still the only nonvolatile memory viable in large quantities, despite the large power needed to flip the cores and the odd voltages that will soon be non-compatible.

Core will survive in two areas – core for main memory and bulk (0.5 to 1 MB) core for emulating fixed-head disks (peripheral) systems with their slow, 8.4ms access times. Bulk core is sold in swapping disks, multi-processor shared memory, video storage, high-capacity buffers (for seismic processing, etc.) and also main memory expansion.

Unlike earlier forecasts of core's impending doom, this time the handwriting is on the wall; its effective demise could come by 1984.

CCD revival? Not likely.

Will CCDs ever compete against bubbles and NMOS dynamic RAMs? If they can improve yields and make a quantum density jump, yes; if not, no. Although volatile, CCDs can move data in blocks, which is fast for moving entire pages around. The unexpected 16k and 64k CCD yield problems slowed manufacturers down, so the needed fourfold edge over NMOS never materialized. CCDs were also introduced to act as low-cost, high-speed buffers between cache and main memory.

Only TI and Fairchild remain in CCDs (with TI a bit erratic on deliveries awhile back); and STC has replaced its CCDs with 16k RAMs on its solid state disk, further aggravating 16k RAM shortages. CCDs will survive in line imaging, filtering and delay line applications. As for CCD's analog nature, could it prove cost effective as a base-3 memory for tenary logic applications? Probably not. Only if CCD can steal a two-generation lead on NMOS can it make it in the add-in/on market. Prospects look bleak.

Bubbles will explode

Bubble memories will be utilized by designers first in those replacement applications where nonvolatility, ruggedness and size constraints are paramount. Other applications will come later. (See "Magnetic Bubble Memories" by P. Snigier, *Digital Design,* December 1979, pgg. 88-91.)

Bubbles won't compete with core, since access times of 200-300μs don't come near core's sub-μs speeds. Throughput is comparable, i.e., not separated by more than an order of magnitude. Bubble won't compete with NMOS yet.

Bubbles will compete against mechanical mass-storage drives and add-in/on boards for environmental and cost reasons. Expect to see them first in process control and data acquisition. They will compete first in μC systems in intelligent terminals, POS systems and text editing. Bubble Tec's $650 MBC-11 ("Bubbl-Board") for the LSI-11 is an example. LSI-11 system designers can add up to 655 KB in 40,960-byte increments. Six modules provide the capacity of a single-sided floppy. The MBB-80 add-in for SBC-80-type boards provides 92,304 bytes in 8-bit bytes. The $1695 (23 m¢/bit) memory, using 8 TI 92-Kbit bubble modules, transfers 22 Kv/s with 7.3ms access time.

Bubbles won't replace mainframe fixed-head disks for awhile (probably late 1980s). When they reach 5-Mbit-plus capacity, they could serve as buffers for moving-head disk systems.

An infant technology, bubbles guarantee a fast cost/bit drop. By 1983, prices will drop tenfold or lower. By 1982, expect a 4-Mbit device on the market; by 1984, 16Mb; and by 1986, 32Mb. But bubbles over 4Mb will require a switch from chevron to contiguous-disk propagating structure to handle smaller bubbles. The big quantum cost/bit decline will come when field coils are replaced, cutting costs and bubble size by a third. Bell's current-access bubbles promise a 20-MHz speed limit (up from today's 1 MHz).

Independents will offer add-in/on bubble memory boards in 1980 for minis and micros. Eventually, Texas, Intel, National, Rockwell, Nippon and Fujitsu will drive the costs down and may repeat the present hard-times scenario for today's independents. But for now, since bubble memory is relatively easy to design with (no messy support circuitry as in MOS), this will prove a lucrative market.

Dumb, smart, intelligent memories?

Everyone knows increased density will beget higher-capacity devices. Other novel possibilities open up by fabricating other functions on the RAM. Chips (such as the 6801) combine a CPU with a relatively small amount of memory. A microcomputer? Definitely. But look at what happens

in the future as RAM capacity keeps growing: is it then a μC with on-chip RAM – or a RAM with on-chip intelligence? This trend to intelligent memories will come from distributed processing's growth. It's popularly claimed in other electronic magazines that distributed processing will be adopted on a large scale. But, are μPs suitable for this? No, and even considering certain μPs with features that lend themselves to interprocessor communications, there's still a long ways to go.

Will these intelligent memories' I/O structures be the same as today's memory devices? No. Since data is stored or fetched every few μs, memories require parallel address and data buses. With growing capacity/chip, packaging constraints must be reckoned with. Intelligent memories could alleviate this. Surely, such smart/intelligent memories would transfer data among themselves, yet also would spend time processing their own stored data.

Unlike today's ROMs, RAMs and PROMs used in inter-device communication, speed may not be so critical in such intelligent memories and parallel buses could be replaced by fast serial paths. Each smart memory I/O would possess high-speed SPCs (serial-to-parallel converters).

The first such memories could be used in military systems and be fabricated with wafer-scale integration (i.e., over the face of an unbroken wafer). If WSI succeeds, the rules of memory and system design will radically alter. On-wafer intelligence, ECC, self-test and memory self-repair (through reconfiguring memory) could create bulk-wafer memories rivaling bubbles for mass storage (an order or more faster) and be used for solid-state disks.

By fabricating many μPs on one wafer with, say, a megabyte or two of memory, an adaptive multiprocessor system with these CPUs working in parallel would promise increased system throughput. And, with short, on-wafer propagation paths, delays will be reduced further. With the multiprocessor able to adapt and alter interconnections, and with spare memory arrays on-wafer, memory arrays damaged in fabrication could be replaced by spares automatically by the multiprocessor. This keeps yields high.

Such a "system-on-a-wafer" would consume 25W for a 5″ wafer if made with MOS. Present experimental wafer systems use metal-nitride-oxide (MNOS), an inherently-nonvolatile FET approach that consumes power only during R/W. Such a 5″ wafer would consume only 2.5W. At present, the military's very high-speed IC (VHSIC) program is looking into one-wafer multiprocessors.

If WSI becomes available, expect system design to alter radically. However, one-wafer, adaptive multiprocessors won't be a factor until well into the 1980s.

Another development that would affect memory users and OEMs will be the blurring of distinctions between different memory types – perhaps between RAM and ROM. Assume that a high-speed, low-cost, single-control 5V-only RAM is developed that offers fast program and erasure and is switchable between read-only and read-write. If so, and if endurance is at 10^7 cycles or more, engineers designing a prototype μC system could load a program in one half (RAM), debug it, then switch to nonvolatility. But greater possibilities open up to the designer: software-modified ROM opens the door to self-modifying code, the elimination of a good deal of indirect addressing and resultant increase in speed.

Now that we've seen the trends taking place among add-in/on makers and in the memory technologies, a logical question emerges – "Should I make or buy?" – and leads in turn to the question of customer support.

Memories: make or buy?

For OEMs with large-volume systems and comprehensive in-house engineering capability, manufacturing proprietary memory systems will save substantial added-value to their end product. Lacking either of these, system integrators must purchase memory systems ready-made or have a custom memory maker design one.

A memory maker who has designed and inventoried an array of memory systems for a large number of applications has a staff of memory system design specialists. Since they specialize in developing "standard" and proprietary "custom" memory systems, they have an edge. This edge extends to other areas. For LSI testing, a large investment in equipment, facilities and qualified techs is needed. Only constant use of such a capability through large-volume memory manufacture makes this cost-effective.

This brings up the matter of warranty and service.

Customer support: how critical?

Semiconductor-manufacturers-turned-memory-makers will be more likely to offer the total product from manufacturing and marketing to servicing. Certain independents with third-party service have been criticized by some users, some who related unpleasant experiences. Is saving $10k/megabyte worth risking two-day downtimes?

Mini and mainframe makers stress service. For example, IBM is known for dispatching a tech within hours, or for a worse difficulty, a central-field rep. If the application is a process control type, it's one thing; but for a complex, user-oriented installation, it makes no sense having to call several vendors and risk poor coordination, vendor finger-pointing games and delays.

Add-in/on makers provide several levels of service support for purchasers. These range from return-to-factory warranty service through full routine maintenance agreements to providing support for individual purchasers. **Return-to-factory warranty** support provides for factory repair of defective modules or subsystems. It's best suited to OEMs providing their own system integration and maintenance, including stocking spares.

On the other hand, **on-demand service support** under an annual agreement, provides assistance as needed, including original installation. However, be sure to purchase spares. Want full maintenance support? Such an agreement provides installation, plus routine and emergency service, and a full-support, user-package that includes all required parts. The catch? It costs more. The advantage? Less hassles later.

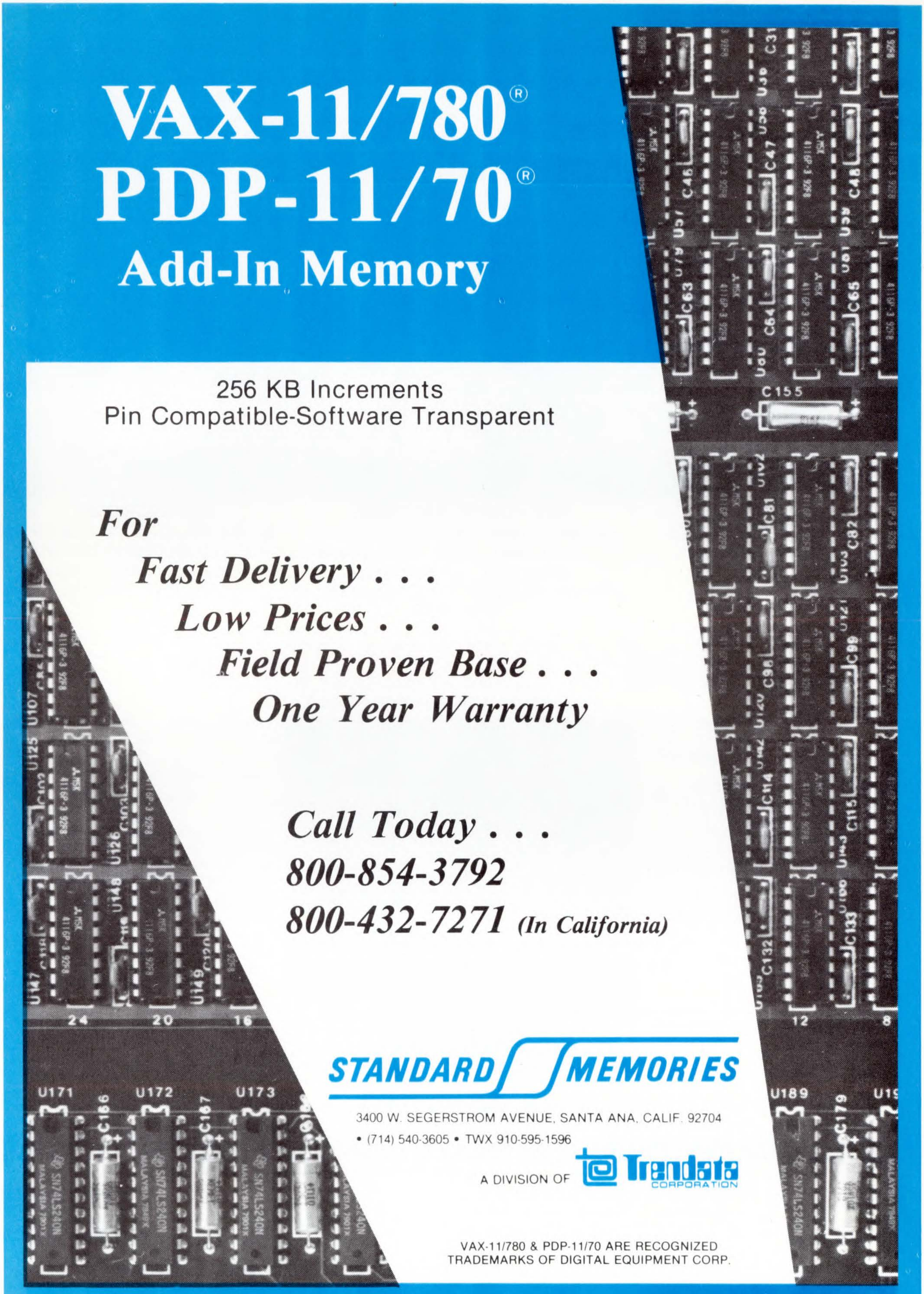
But services under on-demand and full service agreements are often provided not by the memory makers, but by a computer service organization with the memory maker retaining basic responsibility. Be sure to ask about customer support. Can the memory maker's staff provide adequate training, technical assistance and on-site assistance? If so, can they deliver it when required at any support level?

Remember, add-in/on memory makers are not in business for hand-holding or servicing boards; they earn their living selling memories. And the business does contain its share of memory makers no better than cottage shops, not to mention others that are or soon will leave the business. OEMs and users will be left high and dry soon in increasing numbers – a potential bonanza for service organizations.

Independent service organizations

When an out-of-warranty board fails, what do users do? Either they send it back to the manufacturer or to an inde-

Continued on page 58



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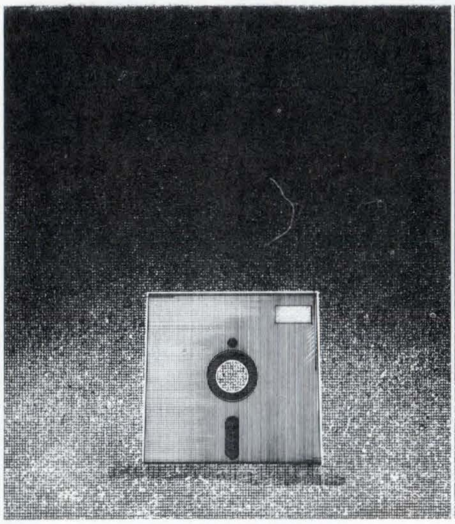
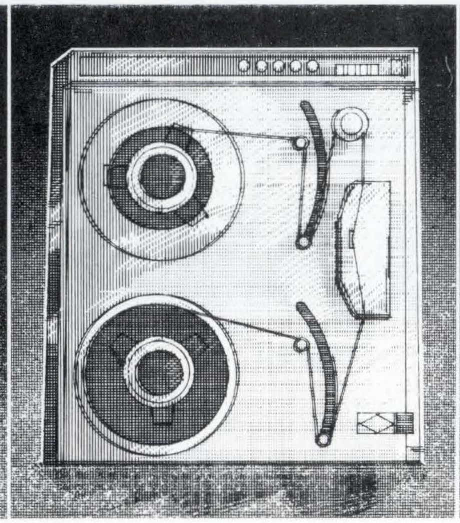
THERE ARE A LOT OF ALTERNATIVES TO THE DISK BACK-UP PROBLEM.



FLOPPY DISKS
Storage capacity: limited.
Handling problems.
Low cost.



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Low performance: 36 megabyte capacity.
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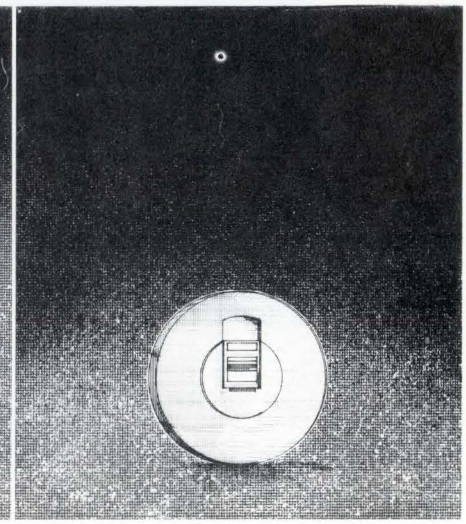

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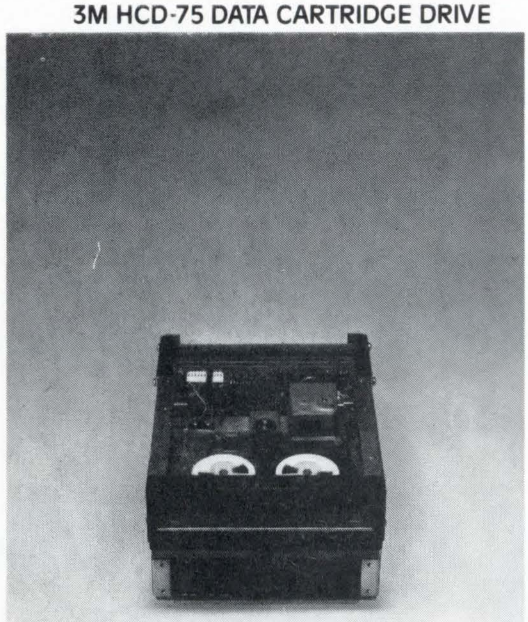

Fully-buffered I/O channel, permits asynchronous data transfers.

Serpentine recording, eliminates wasted rewind times.

List price, including Controller, $2,150.00.

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Hefte Industries, Inc.
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CTI Data Systems, Inc.
Long Beach, CA
213/426-7375

P.A.R. Associates
Denver, CO
303/355-2363

P.A.R. Associates South
Albuquerque, NM
505/881-5000

MIDWEST

OASIS Sales Corporation
Elk Grove Village, IL
312/640-1850

Carter, McCormic & Peirce, Inc.
Farmington Hills, MI
313/477-7700

EAST

J.J. Wild of New England, Inc.
Needham, MA
617/444-2366

Wild & Rutkowski, Inc.
Jericho, Long Island, NY
516/935-6600

COL-INS-CO., Inc.
Orlando, FL
305/423-7615

3M

Add-In/Add-On Memory Manufacturers

Able Computer Technology, Inc.
1751 Langley Ave.
P.O. Box 18162
Irvine, CA 92714
(714) 979-7030
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Ampex Corp.
Memory Products Div.
200 N. Nash St.
El Segundo, CA 90245
(213) 640-0150
Circle 261

Bubbl-Tec Div.
PC/M Inc.
3120 Crow Canyon Rd.
San Ramon, CA 94583
(415) 837-7150
Circle 262

California Computer Products, Inc. (Braegen Corp.)
3320 E. La Palma Ave.
Anaheim, CA 92803
(714) 632-0400
Circle 263

Cambridge Memories, Inc.
360 Second Ave.
Waltham, MA 02154
(617) 890-6000
Circle 264

Central Data Corp.
1207 N. Hagan St.
Champaign, IL 61820
(217) 359-8010
Circle 265

Chrislin Industries, Inc.
Computer Products Div.
31352 Via Colinas #102
Westlake Village, CA 91361
(213) 991-2254
Circle 266

Computer Extension Systems
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Houston, TX 77058
(713) 488-8830
Circle 267

Computer Interface Technology
201 W. Dyer Rd.
Santa Ana, CA 92707
(714) 979-9920
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Computer Memory Div.
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Bloomington, MN 55420
(612) 830-6018
Circle 269

Datacube Inc.
670 Main St.
Reading, MA 01867
(617) 944-4600
Circle 270

Dataproducts
3301 Olcott St.
Santa Clara, CA 95051
(408) 249-9900
Circle 271

Dataram Corp.
Princeton-Hightstown Rd.
Cranbury, NJ 08512
(609) 799-0071
Circle 272

Decision Data Computer Corp.
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Horsham, PA 19044
(215) 674-3300
Circle 273

Digital Data Systems, Inc.
1396 N.W. 65th Terrace
Plantation, FL 33313
(305) 792-3290
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Digital Pathways
4151 Middlefield Rd.
Palo Alto, CA 94306
(415) 493-5544
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Electronic Memories & Magnetics Corp.
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20630 Plummer St.
Chatsworth, CA 91311
(213) 998-9090
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Electronic Solutions Inc.
5780 Chesapeake Ct.
San Diego, CA 92123
(714) 292-0242
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Fabri-Tek Inc.
5901 S. County Rd. 18
Minneapolis, MN 55436
(612) 935-8811
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I Corp.
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Berkeley, CA 94710
(415) 848-6600
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Infotek
2030 Fourth St.
Santa Ana, CA 92711
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Intel Corp.
Commercial Systems Group
2402 W. Beardsley Rd.
Phoenix, AZ 85027
(602) 869-4000
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Keronix, Inc.
250 E. Emerson
Orange, CA 92665
(714) 974-0800
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Micro Memory, Inc.
9438 Irondale Ave.
Chatsworth, CA 91311
(213) 998-0070
Circle 283

Minntronics Co.
2599 White Bear Ave.
St. Paul, MN 55109
(612) 770-5247
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Monolithic Systems Corp.
14 Inverness Dr. E.
Englewood, CO 80110
(313) 770-7400
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Mostek Memory Systems
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Carrollton, TX 75006
(214) 323-6000
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Motorola Semiconductor Products Inc.
3501 Ed Bluestein Blvd.
Austin, TX 78721
(512) 928-6776
Circle 287

Mupro Inc.
424 Oakmead Pkwy.
Sunnyvale, CA 94086
(408) 737-0500
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National Semiconductor Corp.
Computer Products Group
2900 Semiconductor Dr.
Santa Clara, CA 95051
(408) 737-5000
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Periphonics
75 Orville Dr.
Bohemia, NY 11716
(516) 567-1000
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Plessey Peripheral Systems
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Irvine, CA 92714
(714) 540-9945
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Recognition Systems, Inc.
15531 Cabrito Rd.
Van Nuys, CA 91406
(213) 785-2179
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Southwest Data Systems
2509 W. Empire Ave.
Burbank, CA 91504
(213) 841-1610
Circle 293

Standard Engineering Corp.
44800 Industrial Dr.
Fremont, CA 94538
(415) 657-7555
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Synertek Systems Corp.
3001 Stender Way
Santa Clara, CA 95052
(408) 988-0135
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Texas Instruments Inc.
Digital Systems Group
P.O. Box 1444
M/S 784
Houston, TX 77001
(512) 258-7305
Circle 296

Trendata/Standard Memories
3400 W. Segerstrom Ave.
Santa Ana, CA 92704
(714) 540-3605
Circle 297

Zitel Corp.
2900 Coronado
Santa Clara, CA 95051
(408) 727-2595
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Continued from page 54
pendent memory module repair facility. Unfortunately, an add-in/on memory maker is often not motivated to offer fast and efficient repair. Since servicing is not his main source of income, extended turnaround and excessive charges are too often the norm. But there are pitfalls with independent memory repair facilities; and to avoid the problems, compare typical (and emergency) turnarounds, prices (cost-plus), guarantees, QC, "not-to-exceed" estimates, and test report availability.

The future

Japanese firms should increase their memory output by 40% in 1980. They are expanding or setting up plants in Europe and America. Although the Japanese memory device makers' chips are welcomed by U.S. add-in/on memory makers, it will be only a short time before the Japanese, too, like American semi makers, begin offering add-in/on memories in large quantities to OEMs and end users.

Do big add-in/on memory markets exist in Eastern Europe? If so, no one knows how big. CDC feels it can make \$400M on computer sales there in five years; IBM and Sperry Univac, over \$2B. According to a recent Control Data study, Russia is now only two to three years behind U.S. computer makers – not four to five years. If so, this will mean a lifting of government restrictions on computer and memory shipments to communist nations.

Since USSR computer products are rarely available for inspection (except when an occasional MiG pilot lands his jet in Japan), little was known. Now, CDC has examined several Soviet memories, including a 16k dynamic RAM. Although resembling an improved Mostek 4416 (rev. E), access time was slightly better. CDC concluded that the Soviets could produce LSI/VLSI devices in great quantity. If so, this will open a new market for ailing independent U.S. memory makers.

But, one of the biggest new add-in/on memory markets will come from 16-bit micros; they will create gluttonous appetites among OEMs and end users for add-in/on memories. This will mean a change in selecting μC add-in/on memory. The 8-bit μCs used 32kB, with some at 2kB to 4kB. Since static RAMS are easier for designers, that's what 8-bit μC systems designers preferred. But, with the increased memory addressing ranges of the 16-bit μCs, lower cost and power consumption grow significant, and the trend to dynamics makes sense. Also, until now, most add-in/on makers concentrated on the minicomputer (or mainframe markets); they were more lucrative than μC-compatible auxiliary memories.

These coming changes that I have covered here will aid independents; and after a shakeout of weaker ones, the survivors will do well. OEMs and end users will benefit in either case.

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Product Higl

10-MByte Winchester Disk Memory System For 6800 EXORcisor

The "Storage Demon" Memory System, provides Motorola 6800 EXORcisor system users with hard disk memory expansion capabilities. The Storage Demon comes complete with disk controller, 10-megabyte Winchester disk drive and SDOS disk operating system. It relieves problems of limited disk capacity inherent in Motorola-supplied EXORdisk configurations and is upward- and downward-compatible with both the EXORcisor I and II.

Storage Demon aids EXORciser

To develop a computer, it takes a computer with even greater capacity than the system under development. The EXORciser is such a computer, developed expressly as a design, evaluation and diagnostic instrument for M6800-based microcomputer systems.

The EXORciser is an expandable "breadboarding" system that allows almost instantaneous emulation of any M6800 microcomputer configuration, from the simplest to the most elaborate. Built-in programming and diagnostic routines then facilitate the development and debugging of the dedicated programs for the system under design.

There are important differences in system-design with hardwired circuitry and designing with microprocessors. With hardwired, dedicated circuitry, once the necessary components have been functionally interconnected, the job is done; with microprocessors, when the hardware of the system has been emulated, that's when the real design starts – the job of designing the program that turns a basic uneducated computer inot a functional system dedicated to a specific task.

The key to developing a dedicated MPU system and, ultimately, to manufacture and service the system, requires an umbrella of support equipment ranging from development aids to manufacturing and service instruments. The M6800 product family is already complemented with an array of such user-oriented developments and test equipment, and additional items are implemented as quickly as a need for them is demonstrated. It's part of a systematic plan to keep The Family foremost on the "preferred product" list of the system designer; and with the Storage Demon, the disk capacity is extended.

The basic EXORciser contains a power supply and three functional modules – an MPU Module, a Debug Module and a Baud-Rate Module. Together, these form a development microcomputer, requiring only additional memory capacity – such as the Storage Demon provides – and appropriate interface circuitry for the peripherals. Some of these additional requirements are available as add-on modules, permitting the designer to purchase as

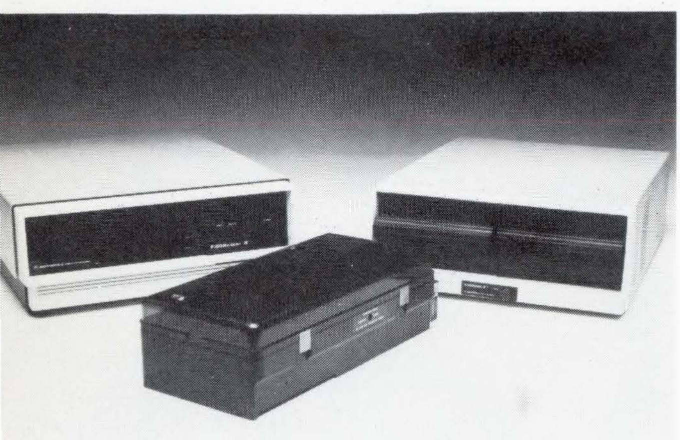
ight

few or as many as required for the anticipated end-functions of the system(s) to be developed.

The chassis is capable of accommodating up to 12 additional plug-in modules to give the EXORciser increased versatility, with memory capacity of up to 65536 bytes.

SDOS provides software support

What about software support? It's provided by SDOS, an interrupt-driven disk operating system with keyboard permitting the designer to purchase a few or as many as required for the anticipated end-functions of the system(s)



of the anticipated end-functions of the system(s) to be developed.

The chassis is capable of accommodating up to 12 additional plug-in modules to give the EXORciser increased versatility, with memory capacity of up to 65,536 bytes.

SDOS provides software support

What about software support? It's provided by SDOS, an interrupt-driven disk operating system with keyboard type-ahead, automatic disk read-ahead and disk sector pooling, dynamic files with random access to the byte and complete device independence. SDOS also supports EXORdisk I, II or III, allowing use of existing floppy disk droves for additional data storage and/or back-up for the Winchester hard disk drive. SDOS will accommodate the powerful Software Dynamics Business Basic Compiler, with 10-digit BCD arithmetic, long names, IF-THEN-ELSE, file I/O, error trapping and other features. The unit quantity price is $6995. Delivery: 30 days ARO.

Software Dynamics, 2111 West Crescent Ave., Suite G, Anaheim, CA 92801. **Circle 257**

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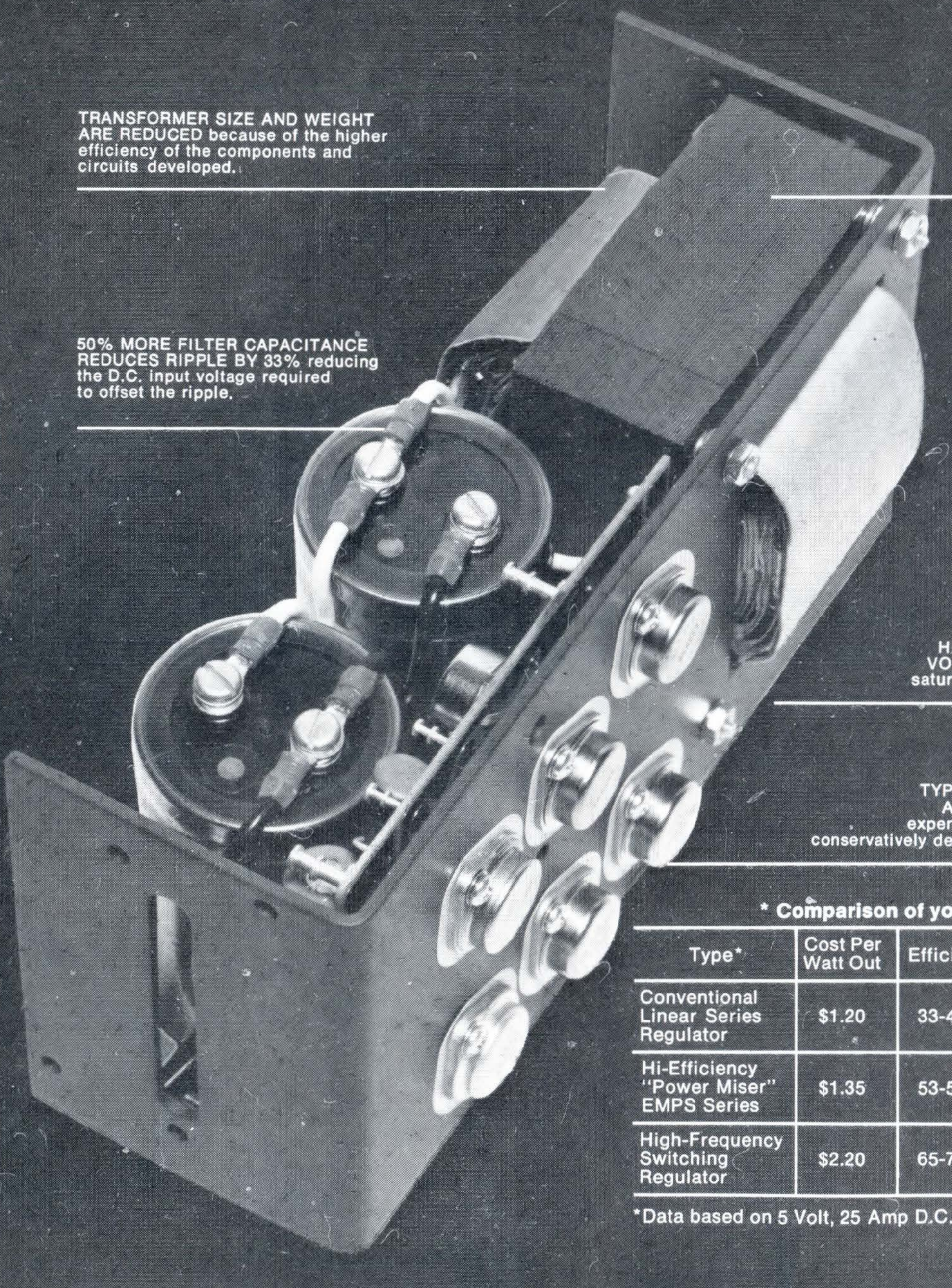
30-40% more efficient and 30-45% smaller than series regulators.. half the cost of less reliable switchers!



*** Comparison of your three alternatives.**

Type*	Cost Per Watt Out	Efficiency	Volume Per Watt Out	Power Density Per Watt Out
Conventional Linear Series Regulator	$1.20	33-43%	3.74 Cu. In./W.	0.27 W/Cu. In.
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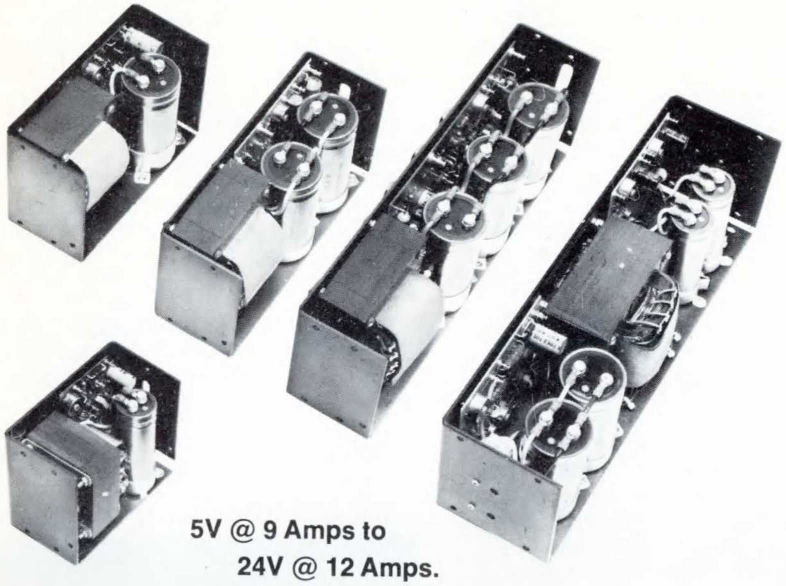
A complete series of 18 Single Output, Dual Output and Triple Output Microprocessor Models with no EMI problems...an MTBF of 60,000 to 80,000 hours...backed by a 6-year guarantee!



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18 Models/ 7 Configurations

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5V @ 18A	54% ±2%	EMPS 5-18	135.00	127.95	122.80	119.15	116.75
5V @ 25A	54% ±2%	EMPS 5-25	180.00	171.00	164.00	159.25	156.00
5V @ 40A	54% ±2%	EMPS 5-40	220.00	209.00	200.60	194.60	190.00
12V @ 12A	59% ±1%	EMPS 12-12	170.00	161.00	154.00	149.25	146.00
12V @ 18A	59% ±1%	EMPS 12-18	210.00	199.00	190.00	184.60	180.00
15V @ 11A	65% ±1%	EMPS 15-11	170.00	161.00	154.00	149.25	146.00
15V @ 16A	65% ±1%	EMPS 15-16	210.00	199.00	190.60	184.60	180.00
24V @ 8A	68% ±1%	EMPS 24-8	170.00	161.00	154.00	149.25	146.00
24V @ 12A	68% ±1%	EMPS 24-12	210.00	199.00	190.60	184.60	180.00
Dual Output Models							
±12V @ 6A	OVER 50%	DEMPS 12-6	190.00	188.10	180.60	175.15	171.65
±15V @ 5.5A	OVER 50%	DEMPS 15-5.5	190.00	188.10	180.60	175.15	171.65
Triple Output Microprocessor Models							
5V @ 12A ±12V @ 2A	OVER 50%	TEMPS-3	185.00	175.75	168.70	163.65	160.40
5V @ 18A ±12V @ 3A	OVER 50%	TEMPS-4	230.00	218.50	209.75	203.50	199.40

*For ±15V add "-2" suffix to model no.
Overvoltage protection standard on TEMPS-3 & 4, 5V. output

Specifications: All Models

A.C. Input:
5 V.D.C. OUTPUT UNITS: 105-125 Vac. 47-440Hz (derate 10% for 50Hz operation)
ALL OTHERS: 105-125/210-250 Vac, 47/440Hz

Extended A.C. Input: 100-130 Vac (derate 20%)

D.C. Outputs: See Tabulation of Models

Control: ± 5% Voltage Adjustment (Screwdriver adjust pot.)

Regulation: ± 0.05% Line or Load

Remote Sensing:
Standard on all models, (includes open sense lead protection.)

Ripple: 5mV Peak to Peak

Reserve Power:
+5% of output available for external load line drop on 5V. and 12V. units; +0.6V. on all others.

Temperature Coefficient: 0.02%/°C.

Stability:
± 0.1% for 24 hour period after 30 minute warmup

Overshoot:
No turn-on, turn-off or power failure overshoots.

Transient Response:
Output recovers to regulation band within 50 microseconds after an instantaneous load change of 50 to 100%.

Operating Temperature:
-25° to +70°C. (derate linearly above +50°C. to 40% at +70°C.; derate linearly below -5°C. to 70% at -25°C.)

Cooling:
Convection cooled for full power rating at 50°C. ambient. Forced air cooling extends full power rating to 60°C.

Protection:
Overload and short circuits: Automatic recovery foldback current limiting fully protects against overloads and short circuits.
Reverse Polarity Protection: Prevents damage from reverse voltage swings.
Inductive Load Protection: Prevents damage due to inductive voltage swings.

Overvoltage:
Optional crowbar overvoltage protection. (Standard on 5V. output TEMPS)

Transformer:
Electrostatically shielded for better line noise immunity.

All Models Meet U.L. Recognition Requirements.

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California, Anaheim
Phone: (714) 634-9211

California: Long Beach
Phone: (213) 426-7375

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Phone: (408) 354-6496

California, San Diego
Phone: (714) 560-1009

Colorado, Denver
Phone: (303) 688-4154

Connecticut, Meriden
Phone: (203) 237-9232

Florida, Coral Springs
Phone: (305) 752-7520

Florida, Largo
Phone: (813) 536-8536

Georgia, Atlanta
Phone: (404) 233-6679
(404) 981-9753

Illinois, Chicago
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Indiana, Indianapolis
Phone: (317) 844-2800

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Kansas, Kansas City
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Kansas, Wichita
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Washington, Seattle
Phone: (206) 641-3535

Washington, D.C.
Phone: (202) 363-9417

Wisconsin, Milwaukee
Phone: (414) 527-1500

ADTECH POWER

Europe: ADTECH INTERNATIONAL, Subsidiary of Adtech Power, 46 BD, Roger Salengro, 78200 Mantes La Ville, France. Tel. 4775301+
DISTRIBUTORS: Call Kathy Nelson, Distributor Products Group, (714) 634-9211, for the name of a distributor near you.

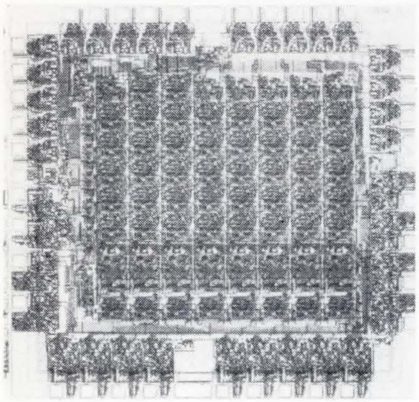
Power Misers are also manufactured in Europe.

ADTECH POWER, INC., 1621 S. SINCLAIR ST., ANAHEIM, CA 92806. (714) 634-9211 ● TELEX 68-1498

Circle 64 on Reader Inquiry Card

New Products

FAST COMBINATORIAL MULTIPLIERS. Am25S558 performs a full 8-bit by 8-bit multiplication in 45 ns. It is a pin-for-pin replacement of the similarly numbered Monolithic Memories' part (67/57558). Am25S557 adds a 16-bit transparent latch between



the multiplier array and the three-state output buffers. Am25S557 and 25S558 come in 40-pin DIPs, require a single +5V supply and consume 280mA max. From $700 (100). **Advanced Micro Devices Inc.**, 901 Thompson Pl., Sunnyvale CA 94086. **Circle 129**

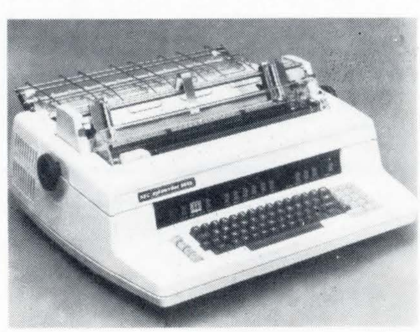
WP SYSTEM. SDS 420, now available as a word processor, is a small business computer w/o WP or with a combination of capabilities. As a WP, it has a CRT display, detachable KB, floppy disk storage, computer and printer. Unlike many WPs which require extensive space, the 420 (less printer) is completely integrated into a small, desktop cabinet. It's 13″ H x 20.5″ W x 25″ D . The 12″ screen displays 25 lines of 80 cpl. For text over 25 lines, the page is scrolled at variable speeds. The printer prints up to 96 std. char./line or up to 88 proportionally-spaced char./line at 45 char/sec. $12K. **Scientific Data Systems**, 12640 Beatrice St., Los Angeles, CA 90066. **Circle 126**

SERIAL ADDRESSABLE BOARD. SAMUX (Serial Addressable MUX) board combines multiplexing with serial data transmission, providing an asynchronous full-duplex serial link between a host processor and the Opto 22 power I/O modules. Both monitoring and control functions can be accommodated by this system. It interfaces with the serial I/O port of the host computer; successive SAMUX boards contain 16 I/O modules that can be connected to provide up to 512 total modules. Data is transmitted over two twisted-pair leads up to a distance of 5,000′. Expansion up to 32 stations can be accomplished any time after the initial installation, providing a distributed I/O system utilizing std. I/O modules. **Opto 22**, 15272 Relay Circle, Huntington Beach, CA 92649. **Circle 127**

GRAPHICS PACKAGE. Interfacing with DEC's VAX 11/780, the MGS-7F supports the Whizzard 7000 graphics display unit with VAX computers operating under the VMS operating system. The package incorporates new fully-buffered DMA transfer capabilities which permit transfer of graphic data to the Whizzard 7000 using either programmed I/O or DMA modes, whichever is faster or more efficient given the nature of the graphics data being transferred. **Megatek Corp.**, 3931 Sorrento Valley Blvd., San Diego, CA 92121. **Circle 128**

DEC/DG BULK CORE. A peripheral storage or main memory, in either 7″ or 15-3/4″ chassis, with storage capacities up to 2 MB/chassis, and with dual-port capability available for DEC and DG disk emulators, "Bulk Core" also offers non-volatility/high reliability. **Dataram Corp.**, Princeton-Hightstown Rd., Cranbury, NJ 08512. **Circle 218**

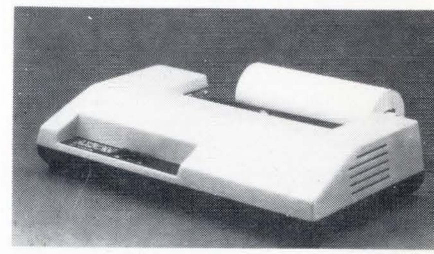
SPINWRITER PRINTERS. Models 5510, 5515 and 5530 are receive-only printers (used where keyboard input is not required). Model 5530's "compatability-plus," parallel interface enables smooth migration from a standard Centronics printer to the Spinwriter. Models 5520, 5525 and 5540



offer built-in keyboard with numeric pad for keyboard send-receive functions. Providing full APL/ASCII compatibility, Model 5540 features APL/ASCII dual-coded keys with program or operator-selectable APL or ASCII mode selection. **NEC Information Systems, Inc.**, 5 Militia Drive, Lexington, MA 02173. **Circle 136**

SERIAL MATRIX PRINTER. Using 9 stored force flexible hammers to print a 9 x 9 dot matrix pattern bidirectionally at 250 cps, the 4540 printhead movements are reduced to a minimum for long printhead life. No adjustment, lubrication or much wear. Sharp and consistent printing results guaranteed for 500 million characters. **Facit, Inc.**, 66 Field Point Road, Greenwich, CT 06830. **Circle 133**

LOW-PROFILE IMPACT PRINTERS. The IMP series stand 3.5″ and print 80, 96 or 132 col. at 1 lps. Friction fed IMP-1 makes 3 copies on plain 8.5″ W paper for WP and handles TTY rolls. It has friction and tractor feed, with 2.5-9.5″ tractor adjustability. The 7 x 7 dot matrix has a std. 96 ASCII char.



set, with special char. sets available. Double-width characters for headlining or accenting. Handles graphics under software control. 17.5″ W x 8.75″ D x 3.5″ H. 15 lb. Friction feed, $695; both friction and tractor feed, $795. **Axiom Corp.**, 5932 San Fernando Rd., Glendale, CA 91202. **Circle 137**

INTELLIGENT TERMINALS. The OP-1 user programmable intelligent terminal series is a complete systems family. All terminals permit on-site feature enhancements. A full range of peripheral controllers provides communications, mass storage and printer interfaces. Master processors, coupled with secondary processors, provide unique distributed computing capabilities. **Ontel Corp.**, 250 Crossways Park Dr., Woodbury, NY 11797. **Circle 138**

V52 EMULATION. "Micro B" Model DM1S emulates VT52, Prism, Beehive B150; Model DM2S offers editing capability, expanded keyboard with 16-function keys, block send; while DM3S offers 8K RAM multi-page capability, parallel printer interface, Beehive B300 Emulator. These 3 "family planned" μP-based terminals can be Beehive or customer software designed as users require. **Beehive International**, Box 25668, 2910 Amelia Earhart Dr., Salt Lake City, UT 84125. **Circle 130**

ENCODERS. Incremental position encoders: std. 1-48,000CPT and higher resolutions; quadrature square wave or direction-sensed pulsed outputs at TTL levels (2-1/2", 2-5/8", 3-1/2" and 6" OD packages). Absolute position encoders: std. resolutions to 2^{20} bits/turn, special resolutions to 2^{24} bits/turn, non-ambiguous code formats. **BEI Electronics, Inc.,** 1101 McAlmont St., Little Rock, AR 72203. **Circle 139**

Z80 ASSEMBLY LANGUAGE PROGRAMMING by Dr. Lance Leventhal includes: over 80 programming examples with std. format including flowcharts, source program, object code and test; Z80 – 8080A/8085 comparisons of instruction sets, interrupts and other pertinent areas; each Z80 instruction fully explained; Z80 Assembler conventions; programming Z80 interrupt system; and Z80 I/O devices and interfacing methods. 650 pgg. $9.50. **Osborne/McGraw-Hill,** 630 Bancroft Way, Berkeley, CA 94710. **Circle 144**

NOVA/ECLIPSE controllers, disk drives and data storage subsystems are all in "Ball Data Storage for Nova/Eclipse." This booklet covers single board disk, tape, and cartridge drive controllers, disk drives in 3 capacities and integrated data storage subsystems. **Ball Computer Products,** 860 E. Arques Ave., Sunnyvale, CA 94086. **Circle 141**

DIGITAL READOUT METERS 400A series are for use with thermocouples, thermistors or RTDs. Each readout's simple, interchangeable, plug-in modules convert to any of 13 different

ranges and calibrations. A "dip switch" which is easily accessible behind the front panel plexi makes conversion between C° and F° easy. **Omega Engineering, Inc.,** Box 4047, Stamford, CT 06907. **Circle 131**

8" WINCHESTER. With a choice of 4.2 and 8.4 formatted megabytes, this line of 8" fixed media drives costs under $1000 (OEM qty). It is said that the SA1000 provides the lowest cost/MB in its capacity and has detailed mechanical and electrical similarities with existing Shugart 8" floppy drives. On the drive are point-by-point physical dimensions and matching holes of a Shugart floppy. Recording density is 6270 bpi with a track density of 172 tpi. **Shugart Assocs.,** 435 Oakmead Pkwy., Sunnyvale, CA 94086. **Circle 135**

TRIPLE MODEM. This series of triple modems, designed for remote terminal use, combines a Bell-type 212A/103 and Vadic VA3400 in a compact standalone package. The VA3450 series includes 6 switched network originate/answer models, all of which have been registered for direct connect under

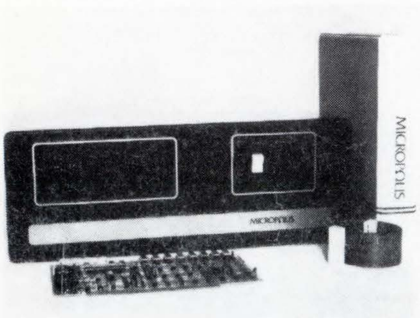
Part 68 of the FCC Rules. In addition, there is an originate or answer version for leased line applications. VA3451 (212A, 103 and VA3400), from $900; VA3452 (212A and VA3400), $850; VA3453 (103 and VA3400), $825. Delivery, 60 days ARO. **Racal-Vadic,** 222 Caspian Dr., Sunnyvale, CA 94086. **Circle 140**

WIRE WRAPPING. Version 62H-1979 catalog of wire wrapping tools and other electronic assembly tools and parts features the PRB-1 10ns Logic Probe and contains a broad range of products and specs. 20 pgs. **OK Machine And Tool Corp.,** 3455 Conner St., Bronx, NY 10475. **Circle 147**

DEVELOPMENT SYSTEM. The DCS/80 Multibus-compatible development/control system includes a 16K RAM system and dual 8" floppy disks ($3595). The DCS/80 provides an industrial-quality, rack-mountable, integrated Multibus system. Also offered is a complete range of high-level languages (including Pascal), an expanding selection of cross-assemblers for μPs other than the 8080/Z80, and IBM bisynchronous telecommunication software. DCS designs and manufactures its own CPU boards, disk controllers, backplanes, etc. **Distributed Computer Systems,** 223 Crescent St., Waltham, MA 02154. **Circle 134**

New Products

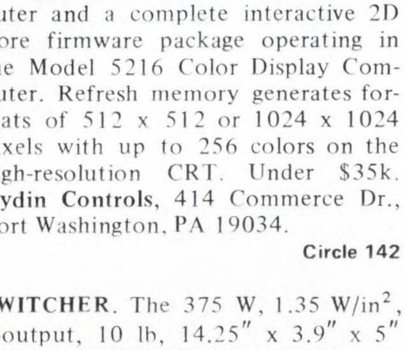
MULTI-USER OS, for the "Micro-Disk" – an 8" rigid disk drive with up to 31.2 Mbytes of formatted data storage capacity – is a fully integrated rigid disk subsystem. With the OSM, users can plug in a primary storage device with performance characteristics



equal to or surpassing that available on many mini systems costing two to four times more. The subsystems come in formatted capacities of 6.2, 18.7 and 31.2 Mbytes and are expandable by daisy chaining. Up to three add-on modules may be connected to a master unit. From $5k. **Micropolis Corp.,** 7959 Deering Ave., Canoga Park, CA 91304. **Circle 143**

COLOR RASTER SIGGRAPH compatible 2D core system, Model 5216 Display Computer, has 2D Core-compatible software. The 5216 Aygraf/Core System includes a Fortran package installed in a host computer and a complete interactive 2D Core firmware package operating in the Model 5216 Color Display Computer. Refresh memory generates formats of 512 x 512 or 1024 x 1024 pixels with up to 256 colors on the high-resolution CRT. Under $35k. **Aydin Controls,** 414 Commerce Dr., Fort Washington, PA 19034. **Circle 142**

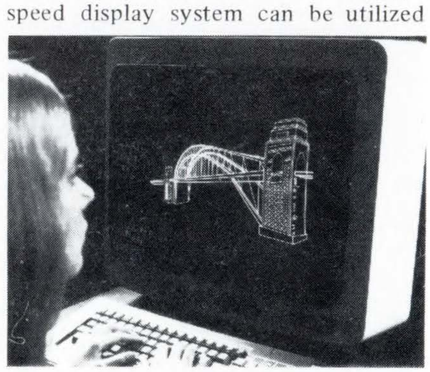
SWITCHER. The 375 W, 1.35 W/in^2, 3-output, 10 lb, 14.25" x 3.9" x 5" "Mighty-MITE" MM-23 switching-regulated supply provides 5 V dc at 75 A,



with additional main current rating available through masterless straight paralleling. **LH Research,** 1821 Langley Ave., Irvine, CA 92714. **Circle 145**

DEC-COMPATIBLE SINGLE-BOARD PROCESSOR, "Uniface," lets you get the most from DEC's Unibus and develop your controllers, preprocessors and intelligent channels – or add Unibus channels to existing systems. It uses bit-slice 2901, implementing a 32-bit-microword instruction set. Its 200-ns instruction rate provides computational muscle comparing favorably with host computers it offloads. The Unibus-compatible microconsole and microassembler lets you write specialized software to drive Uniface and perform the interface task. Processor board stores these programs in ROM. Can you install more than one Uniface/Unibus CPU? Yes, one board can drive 32 communications channels at 19.2k baud/channel with full modem control. Board measures 8.5" x 16.5". 5V, 4A. $45 (100). **Able Computer,** 1751 Langley Ave., Irvine, CA 92714. **Circle 146**

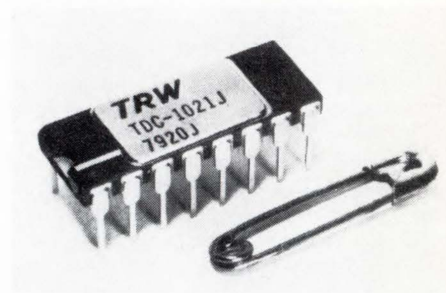
FOUR-COLOR GRAPHIC DISPLAY uses dual-anode technique, using less power than single-anode color units. It reduces system stress and increases indicator reliability and provides greater color stability and fewer maintenance adjustments. Layered phosphor, beam penetration technique enables simultaneous display of 4 colors, and full deflection rates of a high-speed display system can be utilized



for all 4 colors. Typ. char. can be traced in 2.1 μs in any color. Built-in test feature displays test pattern, showing failed modules. Model 740 Series, 21" (vert. or horiz.) rectangular face; Model 760 Series, 23" round configuration – each available in desktop or rack-mounted version. Additional information on the Sanders Color Indicators, priced at 740, $17,500; 760, $20,000. **Sanders Associates, Inc.,** Daniel Webster Hwy. South, Nashua, NH 03061. **Circle 148**

MERGERS and acquisition continue in the electronics industry as larger firms diversify, affecting engineering environments, and, although opportunities exist, pitfalls await the unwary, as examined in D. Gussow's 262-pg. hardcover, "The New Merger Game." $12.50. **AMACOM,** 135 West 50th St., New York, NY 10020. **Circle 178**

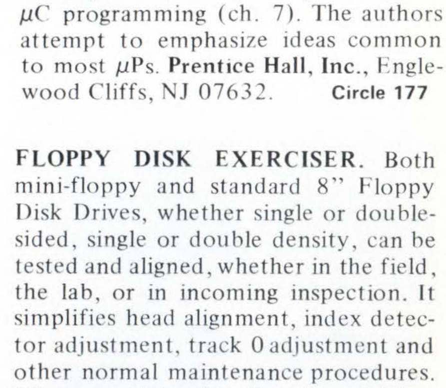
LOW-COST, MONOLITHIC 4-BIT A/D CONVERTER A low-cost, video-speed, monolithic, 4-bit ADC, the TDC-1021J, provides digitizing rates from dc to 30 Msamples/sec w/o an external S&H. The 16-pin ceramic DIP is fully parallel, TTL-compatible and suited for applications where high speed, small size, and low cost are important – but high resolution is not – such as video data conversion, radar



data conversion, high-speed mux'd data acquisition, X-ray and ultrasound imaging, image processing, and facsimile systems. A single convert signal controlling the operation, has 15 sampling comparators, combining logic, and an output buffer register. The 250 mW device requires only two power sources: +5.0V and –6.0V. **TRW LSI Products,** Box 1125, Redondo Beach, CA 90278. **Circle 181**

μPs/μCs. Approaching the μC/μP from the 6800/6502 viewpoint, Tocci and Laskowski's 324-pg. hardcover, "Microprocessors and Microcomputers: Hardware and Software," introduces micros in the traditional way (ch. 1-5), before moving into I/O-interfacing (ch. 6) and μC programming (ch. 7). The authors attempt to emphasize ideas common to most μPs. **Prentice Hall, Inc.,** Englewood Cliffs, NJ 07632. **Circle 177**

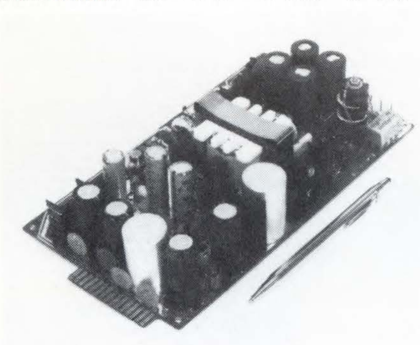
FLOPPY DISK EXERCISER. Both mini-floppy and standard 8" Floppy Disk Drives, whether single or double-sided, single or double density, can be tested and aligned, whether in the field, the lab, or in incoming inspection. It simplifies head alignment, index detector adjustment, track 0 adjustment and other normal maintenance procedures. It's compatible with all makes of drives



using the standard Shugart interface; two connectors are provided, one 34 pin for mini-floppy drives and one 50 pin for standard 8" floppy drives. It needs no power supplies and uses power from the drive under test. Under $500. **Ava Instrumentation, Inc.**, 9672 Manzanita Ave., Ben Lomond, CA 95005. **Circle 188**

6502 OPERATING SYSTEM software, CRS-DOS, includes a general-purpose monitor package, routines for handling serial/parallel I/O, cassette file handling and floppy disk processing routines. It provides general operations control and a series of unique software development aids. The user has access to all portions of the μC system, including pages zero and one (stack) and all interrupt processing. User programs can be interrupted with the BRK command, use CRS-DOS commands, and return to the users program with system reset to the exact state it was in when interrupted. With the 6502 Professional Development Computer, $2500; stand alone item on ROM and diskette, $125. **CGRS Microtech**, Box 368, Southampton, PA 18966. **Circle 185**

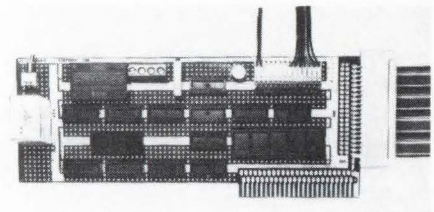
SWITCH-MODE POWER SUPPLY has maximum continuous power rating of 65 W up to the following limits: +5V 6A, +12V 2.5A, −12V 1.0A, −5V 0.5A and +24V 1.5A. All outputs are protected from short circuits. The other dimensions are 9.45" x 5.0" x 2.0"



with a weight of 1.7 lbs. The unit is designed to the EMI and safety requirements of UL 478, CSA 22.2 #155, VDE 0804 and 0730 and features an unusually wide tolerance of input voltages; 80 to 140VAC and 160 to 264 VAC. **Conver Corp.**, 10631 Bandley Dr., Cupertino, CA 95014. **Circle 184**

"**MICROPROGRAMMING** Techniques With Sample Programs," a 230-pg. hardcover by Dr. Stanley Evans, covers Advanced Basic, PL/M, APL and lists reference tables (ASCII codes, HEX conversion, etc). Emphasizes (33.5%) PL/M, with 14.3% on Basic and only 4.4% on APL. **Reston Publishing Co., Inc.** (Prentice Hall), Reston, VA **Circle 179**

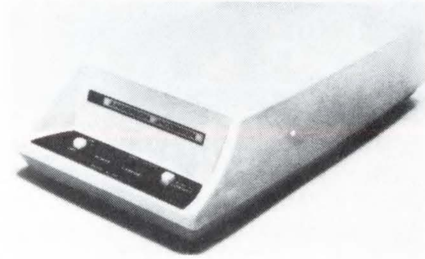
INTERFACE BOARDS. Compatible with Apple II and Superkim micros w/o any special adapter unit, and compatible with the PET Commodore provided an adapter unit called "Expandamem**" (formerly "Expandapet") has been installed in it, the 4609 boards have provisions for three additional types of I/O connectors, extended board area and dual heavy-duty power buses between the DIP IC leads for easy, short bus connections.



The Model 4609 is designed for construction of special control, communications, peripheral or memory interface circuits using the growing number of support devices from major semiconductor manufacturers. It also serves for breadboarding experimental circuits. $21.50 (4). **Vector Electronic Co.**, 12460 Gladstone Ave., Sylmar, CA 91342. **Circle 186**

SDRC SYSTEM SIMULATION and Modal Analysis Software (SDRC MODALPLUS and SDRC SABBA) are now available for use on the GenRad 2508 Structural Analysis System. MODALPLUS is an interactive software package that collects, analyzes, and displays data from artificial excitation tests of mechanical structures. SABBA is an interactive system analysis software package that determines the dynamic response of complex machinery. **SDRC**, 2000 Eastman Dr., Milford, OH 45150. **Circle 189**

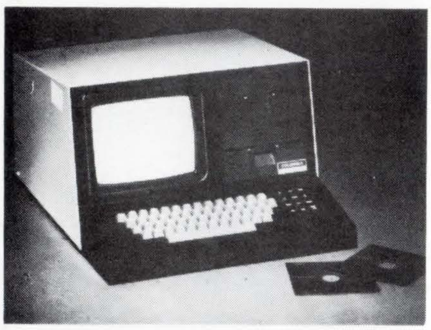
DIRECT CONNECT MODEM, the AJ 245, is easily connected to a modular jack or DAA. Line connections are switch selectable and do not require internal modifications. Compatible with Bell 103/113 type modems, the AJ 245 transmits and receives full du-



plex asynchronous data at speeds up to 450 bps. The AJ 245 provides a dual terminal interface for either EIA RS 232 or 20 mA current loop terminals. $192, (50). **Anderson Jacobson, Inc.**, 521 Charcot Ave., San Jose, CA 95131. **Circle 195**

MULTIBUS-compatible positioning servo interface for use in single axis servo loops equipped with encoder feedback, PS-10, incorporates an analog voltage output compatible with most velocity servo loops. An on-board 12-bit incremental up/down position counter minimizes real-time service requirements. $700. **Controlsmith, Inc.,** 17 Airport Rd., Nashua, NH 03063.
Circle 176

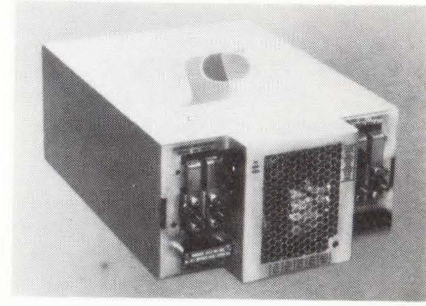
COMPUTER WITH CUSTOM I/O contains dual Z80 CPUs with up to 80K RAM and 320K disk storage, CRT display and a full keyboard with separate editor/user defined function keys. Some versions include an optional built-in printer. Commander computers



execute programs in CBasic, Cobol, Fortran and Macro-80 Assembler under CP/M. Four RS-232 ports handle low speed I/O while the parallel bus supports high speed peripherals. Optional IEEE and DMA controllers support peripherals ranging from instruments to Winchester disks. A real time interface handles bit-oriented I/O such as a bar code reader. **Columbia Data Products,** Computer Systems Division, 9050 Red Branch Rd., Columbia, MD 21045.
Circle 197

PAPER TAPE READER. Unique design of the 2001-3 incorporates wide opening cover making tape loading easy, and new read head reduces errors due to out of tolerance and skewed tapes. Power supply is self-contained. Operational characteristics include 200 CPS bi-directional read in either step or slew mode; bi-directional rewind at 400 CPS while under front panel control; the unit can handle strip or loop tapes of paper, mylar or other combinations not exceeding 0.0045″ in thickness and punched per EIA standard RS227 tolerances. Power requirements are 115/230 VAC, 50-60 Hz. TTL, DTL interface is switch selectable for either postive or negative logic levels. $595 each. **EECO Inc.,** 1601 E. Chestnut Ave., Santa Ana, CA 92701.
Circle 196

SWITCHING REGULATOR POWER SUPPLY, PM2809, features two high power output channels providing output voltage selections of 2, 3, 5, 12, 15, 18, 21, 24, 28 and 48 VDC and a third channel with voltages including 2, 3, 5, 12 and 15 VDC. Maximum total output power is 800 W including 400 W



max. on the main channel and 400 W max. on the second channel less third channel power which may be up to 10 A at 15 V. $1075. **Pioneer Magnetics,** 1745 Berkeley St., Santa Monica, CA 90404.
Circle 200

"Z80 SOFTWARE Gourmet Guide & Cookbook," a 324-pg. paperback by N. Wadsworth, provides already programmed and ready-to-use routines, subroutines and short programs. Also a good deal of plain-talk explanation of the Z80. **Scelbi Publications,** Elmwoods, CT 06110.
Circle 235

32-BIT MICROCOMPUTER includes 512KB of memory, a floating point processor, writable control store, the model 550 CRT, a 75 ips magnetic tape drive, and an 80 Mbyte disk. The Model 3240 directly addresses up to 16MB of physical memory, configurable in up to four interleaved banks. The processor uses 16K RAM chips. The model 3240 provides eight sets of 16 registers, for a toal of 128. The processor has 2K words of fixed control store (ROM) available to implement the standard instruction set. Error Checking and Correcting, performed on a full 32-bit word, is standard. A 8KB four-way set-associative cache memory improves memory access times. The unit uses a multiplexor bus and from one to four DMA buses. Software is compatible with Model 7/32, Model 8/32, and Model 3220 computers. **Perkin-Elmer**, 2 Crescent Pl., Oceanport, NJ 07757. Circle 180

Q BUS ANALOG OUTPUT. The MP1104 analog output interfaces directly to the DEC "Q" bus. MP1104 consists of four 12-bit D/A converters plus address decoding and control logic. It also includes an on-board DC/DC converter for operation from the computer's 5VDC supply. The MP-1104's 4-channel output system accepts 12-bit inputs from the data bus and converts them to analog outputs with an accuracy of ±0.025% FSR. $550. **Burr-Brown**, PO Box 11400, Tucson, AZ 85734. Circle 194

X.25 SIMULATOR/TESTER interfaces directly with terminals and front-end processors for testing, or it can be operated remotely over full-duplex synchronous lines using modems. The console can also be used remotely from the Simulator/Tester via asynchronous lines. Principal applications of the Simulator/Tester are to simulate the X.25 network for terminal inter-

face development and to simulate terminal inputs via the X.25 network for testing and debugging of front-end processors. After installation, the Simulator/Tester is then used as a line monitor and as an X.25 protocol validator in all these applications. $11,900; **Applied Data Communications**, 14272 Chambers Rd., Tustin, CA 92680. Circle 198

SWITCHING SUPPLY. The LH Research Mighty-MITE MM-22 switching regulated power supply is typically used in main frame and minicomputers, process controllers, add-on memories, medical instrumentation, satellite communication systems, test and transmission equipment, word processors and video display systems. Main output is rated at 5 V dc @ 75A. Seven choices are available for the 2nd output: V dc 2 (12A), 5 (12), 12 (10), 15 (10), 18 (8), 24 (5), 28 (5). Additional current rating can be obtained through masterless straight paralleling. **LH Research Inc.**, 1821 Langley Ave., Irvine, CA 92714. Circle 187

FORMS FLEXIBLE PRINTER. This line buffered serial impact printer features an integrated cutting device for handling special forms such as airline tickets, statements, ledgers, checks and labels. The M78 uses a continuous fanfold paper supply and automatically cuts off the completed form. The 80 column unit prints at 200 cps. The

standard M78 has a 7 x 7 matrix font, but optional 9 x 9, 9 x 7 and 9 x 12 fonts can be used. For forms compatibility or best readability, the operator can switch from 6 to 8 line per inch spacing or switch character spacing from 10 cpi to 12, 14 or 16.5 cpi. **Tally Corp.**, 8301 S. 180th St., Kent, WA 98031. Circle 202

ON-LINE PLOTTER CONTROLLER, the Model 907 permits specified CalComp plotters to be driven locally or remotely by a wide range of computers and calculators. The 907 accepts data in serial RS-232C, 20 mA current loop, IEEE parallel formats, or selected special parallel inputs. The Model 907 offers integral firmware to generate plotter commands for drawing lines, dashes, arcs, circles and characters/symbols, which can be scaled and rotated. Up to 288 characters/symbols, including a 95 character ASCII set, foreign characters and special symbols, are stored in its Read Only Memory (ROM). Up to 192 user-defined characters can be downloaded from the host to the RAM. $5,060. **California Computer Products, Inc.**, 2411 West La Palma Ave., Anaheim, CA 92801. Circle 201

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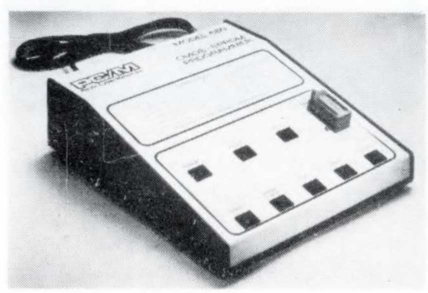
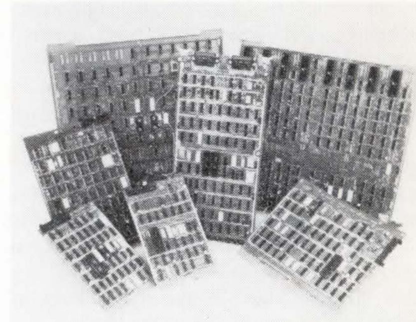
PROGRAMMER for programming Intersil 6653 and 6654 devices contains its own μP and 4096-bit RAM buffer. It can be operated stand-alone from its own front panel or interactively with an ordinary TTY or CRT terminal through the programmer's built-in RS-232 and 20-ma current-loop interfaces. Built-in features of the Model 660-A programmer include a full complement of editing capabilities for loading and checking the programmer's



RAM buffer and/or 6653/6654 EPROM, ability to accept all popular paper-tape formats, firmware for EPROM copying and verifying, ability to punch a paper-tape image of the buffer or EPROM contents, and a front-panel erase-check capability. Programming time for a 4K CMOS-EPROM is typically 40 seconds. $795. **PC/M, Inc.**, 3120 Crow Canyon Rd., San Ramon, CA 94583. **Circle 204**

SB DISK CONTROLLER. The Ball 3255 single-board disk controller relieves the Data General computer of many disk system control operations. The 3255 controller supports up to four Storage Module, Winchester or 3300-type disk drives in any mix of capacities and accommodates multiple disk organization and transfer rates from 806K bytes to 1.2 Mbytes/sec. **Ball Computer Products**, 860 East Arques Ave., Sunnyvale, CA 94086. **Circle 182**

COMMUNICATIONS / TERMINAL MODULES. For use with the PDP-11 computer, this Ansync. Serial Line Adapter (DL-11 type, includes operational features A through E) or with Line Frequency Clock (DL-11W), and Synchronous Serial Line Adapters (DU-11 types). New products include a DUP11 Synchronous Serial Line



Adapter for bit or byte oriented protocols, an Eight-Line Asynchronous Multiplexor (DZ11AC), and a Byte Parallel DMA Terminal Interface (PDI-11). An Asynchronous Serial Line Interface (DLV11, or DLV11E with modem control) is available from MDB for use with the DEC LSI-11 computer, as well as a Synchronous Serial Line interface (DUV11 type). **MDB Systems, Inc.**, 1995 N. Batavia St., Orange, CA 92665. **Circle 205**

TI 9900 SINGLE-CHIP MICRO. "How To Build Your Own Working 16-Bit Microcomputer" (No. 1099), by Ken Tracton shows how to use interfaces (or even circumvent them if necessary), TMS 9900 family support chips, including TMS 9901 Programmable System Interface, a look at TMS 9902 system architecture, the TMS 9903 synch. communication controller, TIM 9904 clock generator, ect. 96 pgg. $3.95. **Tab Books,** Blue Ridge Summit, Pa. 17214. **Circle 209**

PDP-11-COMPATIBLE MEMORY offers 256K on single card and provides 22-bit addressing. The NS11L, a direct replacement for DEC's MS11 series memories, uses only a single voltage (5V), greatly simplifying its use in systems requiring battery backup. Its partitioned power plane minimizes battery drain by powering only the memory elements and refresh circuitry. High throughput rates due to address and data latches that isolate memory from spurious bus noises permit the bus to be released within 100ns on write operations. Read operations are completed in 300ns, over 50% faster than comparable DEC memory. Memory cycle time is 450ns. $5,750. **National Semiconductor Corp.**, MS 7C-265, 2900 Semiconductor Dr., Santa Clara, CA 95051. **Circle 192**

New Products

U.C. TIMESHARED 8080/Z80 OS. Utilizing Bell Lab's UNIX system as its model, CHAOS II offers multiprogramming (multi-user) capability with facilities for interprocess communication and synchronization and availability of: MITS BASIC, version 4.1, 8080 assembly language and Shell (command line interpreter). CHAOS II includes: Utility programs for text editing and formatting, file/directory management, disk system maintenance and debugging assembly language code. CHAOS II Object Code Disk, $300; Source Listings, $500; manual, $25. **Computer Systems Design Group**, 3632 Governor Dr., San Diego, CA 92122. **Circle 190**

"THE ACTIVE FILTER HANDBOOK" (No. 1133) by Frank P. Tedeschi strips away the mystery normally associated with active filters and thoroughly discusses filters and their purpose, compares different filters, and covers LC passive filter operation, op amps, Butterworth filters, Chebyshev filters, low-pass filters, high-pass filters, etc. 280 pgg. $6.95. **Tab Books**, Blue Ridge Summit, PA 17214. **Circle 225**

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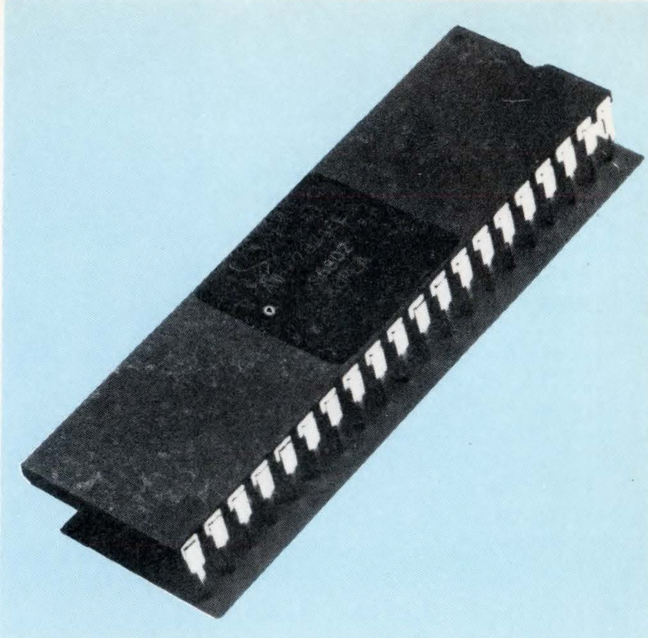
Semiconductor Memories



S. Cash Olsen
Signetics Corp.,
Sunnyvale, California

Sales of semiconductor memory chips totaled $1.3 billion in 1979 – a 50% increase over 1978. Fueling that growth is the ever-declining price/bit, which has plummeted some fiftyfold in the past five years, generating a demand for memory capacity that should again double this year, as it has in each of the last three years. Speeds have increased and instruction cycle times are shorter. Various IC manufacturers have developed new technologies; and circuits over the next few years should be twice as fast as today's circuits.

Chips proliferate

Like the supermarket shopper who has dozens of soups to choose from, the system designer also has a seemingly infinite variety of memory types open to him. Memory types include RAMs, ROMs, PROMs, EPROMs, EAROMs, EEPROMs and the new ones continually being developed.

RAM, by far the largest market segment for semiconductor memories, includes three basic types of access:
- sequential, in which data is entered at an input and a fixed number of clock cycles will produce the data at the output;
- random access, where any part of a data word can be reached in one clock cycle by applying the address of the data; and
- content-addressable (associative) access where data is retrieved whenever a portion of the data matches an input.

RAMS can be R/W, read-only or variations of each. Most R/W semiconductor RAMs are volatile; that is, when power is removed, data stored in memory is lost. The major distinguishing feature of R/W RAM applications is that data must be frequently accessed and changed.

ROMS, on the other hand, are used in applications where the programs or data stored in ROM are not to be changed. A masking step fixes data patterns during the manufacturing operation. As such, the pattern is nonvolatile; that is, removal of power doesn't destroy the data.

In PROMs (programmed by severing fusible links) a data pattern is burned in at low speed, and a bit of data can be written into a cell one time. PROMs are used in low-volume applications.

While PROMs can only be written into once, EAROMs can be erased and rewritten many times. The largest segment in the programmable market is the ultraviolet Erase-able PROM (EPROM). Content-addressable memories (CAMs) are memory devices which yield the remaining contents of an address when a portion (field) of the address contents matches a presented value.

Never before have design engineers faced such a bewildering choice of semiconductor memories. The pace of activity in the marketplace has grown more frenetic in the past 18 months, as new products and new processing techniques debut. Static or dynamic; NMOS, HMOS, CMOS, CCDs or bipolar; – the choices grow more numerous, the opportunities for creative system design more exciting.

To make your design choice easier, let's look at the most promising areas of today's memory market.

Which technology to use?

MOS and bipolar are the two major technologies used in semiconductor memories. MOS technology is based on the MOSFET; bipolar technology, on the epitaxial transistor. Bipolar transistors have a 100:1 transconductance advantage over MOSFETs. Bipolar produces significantly faster memories that require higher power due to low input impedances and produce high peak currents due to fast capacitor-charging rates.

New MOS photolithographic and process advances are pushing MOS memories into regions until now exclusively occupied by bipolar memories – and pushing bipolars into only the speediest digital system designs. Static MOS RAMs have moved from a 500ns 1K to 250ns 1K, a 200ns 4K down to a 55ns 4K in seven years. Generally, MOS has a cost advantage over bipolar down to 50ns access time; below 50ns, bipolars are superior.

Although other technologies are closing in on bipolar, they still can't achieve the speeds possible with this approach. Manufacturers working with bipolar technology, such as Fujitsu, Motorola, National, Signetics and Fairchild, are aiming for 10- to 20-ns access times. In addition, all of them are working on or sampling 4K devices in this speed range.

In the past, the fastest bipolar devices used TTL and ECL. But as memories reach the 4K level, they generate more heat than the IC or its package can handle without extraordinary cooling methods. Therefore, is 4K the limit for TTL/ECL? It seems so.

Bipolar memories with capacities greater than 4K will probably use some form of I^2L because of that logic family's lower power and higher packing density. Although static I^2L devices exhibit 20ns access times and 300 mW dissipation in 1K versions, the breakthrough will be the tighter geometries that I^2L promises.

HMOS and its sequel

Different technological improvements have contributed to the MOS cause over the years. MOS advances, such as HMOS (the H means "high performance"), introduced two years ago, are higher-performing processes that guarantee a host of faster and denser memories. A comprehensive approach to scaling was applied in developing the HMOS process. Selective scaling of many critical physical and electrical parameters of the MOS devices maintained the trend toward higher speeds. At the same time, reduced power requirements significantly improved the power-delay product of MOS technology.

HMOS II, a newer technology, goes a step farther, employing device-scaling principles to extend performance beyond any current MOS technology. HMOS II memory chips have 15ns typical address access times, twice the speed of HMOS memories. The fast HMOS 1K and 4K parts appeal especially to cache-memory designers. MOS statics would be in the same speed range as equivalent bipolars, but won't dissipate nearly as much power. HMOS II designs could become a bargain once in production, since MOS processes are cheaper to implement than bipolar.

A variation of the HMOS technique using a two-layer polysilicon HMOS structure results in a fully-static 16K RAM with access times typically 45ns. The 16K x 1 bit double-poly HMOS design does not use increased scaling. Its four fold density improvement over the standard HMOS process stems from tighter cell dimensions resulting from double-poly structures.

Double-poly HMOS 16K static RAMs break new ground in system designs, offering mainframe memory designers a high performance choice over previous 16K dynamic parts. These fully static 16Ks operate at typically 45ns access and require less overhead circuitry than dynamics. In the future, many designers may turn to the fast statics for medium-size, high-performance main memory design, while moving up to 64K dynamics for next-generation large-capacity mainframe applications.

HMOS II is not the end of the road. With the introduction of improved lithographic equipment such as direct-wafer-stepping exposure systems, resolution well below one micrometer will soon be possible. But though the technology to produce submicrometer devices is within reach, industry adherence to today's standard 5V power supply could delay introduction of such services in a commercial process. Although HMOS II and possibly the next generation of scaled devices are achievable without reducing supply voltage, industry acceptance of a new voltage standard – for example, a 2- or 3-volt level – is inevitable.

HMOS II has been in production for a while and the 4K by 1-bit static RAM designed to be fully optimized for this process is available to systems designers. Not only is a large family of static RAMs planned for the future, but HMOS II exhibits the same flexiblity for a broad design base enjoyed by HMOS – it will be applied to high-performance μPs and a variety of peripheral chips. Because MOS is more suited to device scaling than bipolar technology, recent advances in photolithography and scaled wafer processing indicates a bright future for MOS performance.

More alphabet soup: CMOS and CCDs

CMOS has a high-noise immunity, wide tolerance to power supply variation, low-temperature sensitivity and low-power dissipation. Its complementary nature holds the promise of its becoming the fastest technology. These static RAMs are strengthening their foothold in the military and high-reliability areas with their extremely low supply-current drain and wide performance range. Several new high-density CMOS techniques will appear in 1980 in addition to the use of tighter lines and scaled geometries. Also, the use of silicon-on-sapphire (SOS) CMOS technology is increasing as the cost of producing the sapphire and processing the silicon drops.

As pinouts become further standardized, CMOS equivalents will appear for available NMOS devices. However, unlike the NMOS market, where prices for the next larger size started out as just above four times the cost, 4K CMOS devices cost less than four times the cost of 1K RAMs. Although the order of the day for CMOS is 4Kx1 and 1Kx4, few companies introduced 16K CMOS RAM samples this year. In fact, there may even be a family of 16K devices – 16Kx1, 4Kx4 and 2Kx8 organizations – to satisfy a wide range of memory requirements. CMOS RAM speeds now start at 70ns for 1K parts and only 80ns for 4K units. This coming year, look for the emergence of another CMOS development – CMOS ultraviolet-EPROMs.

A few manufacturers think CCD memories have a definite market niche, and they feel the 64K devices will give them an edge in both design experience and product recognition if the 256K CCD makes its debut next year. CCDs are slower than semiconductor RAM, are volatile, and do not offer true random access operation. However, they can replace disk products, and act as staging areas for storage peripherals, thereby increasing CPU throughput. With them, a CPU does not have to wait for the storage device to deliver or accept data.

Despite its potential for a place in the memory hierarchy as a block-oriented storage of high speed and density, the CCD has not outdistanced the dynamic RAM far enough in cost or availability to succeed. Further dampening enthusiasm for CCD believers is CCD susceptibility to alphaparticle radiation, which exceeds even that of dynamic RAMs. Nevertheless, CCD technology should survive because of imaging and filtering applications.

Static or dynamic

To use static RAM or dynamic RAM – that is the question in the NMOS area. Static RAMs retain data even with power turned off; this memory is used for data base storage. Dynamic RAMS need a constant source of current to keep data. Choosing one over the other is usually decided by cost.

Static is less expensive for small systems in which the cost of the extra refresh circuitry cannot be amortized over the small number of RAMs. At the 4K level, a crossover in cost occurs somewhere between 12-16K words in the system. Some memory users include the larger engineering costs of dynamic RAM in their decisions, since statics are considerably simpler to design. Other users opt for static alone to save their engineering talent for designing features into their equipment that will enhance its position.

Two distinct paths emerging in static RAMs should give system designers pause: very high-speed static RAMs for cache and mainframe applications and word-oriented, slower static memories for microcomputer applications.

In the N channel static RAM area the trend is toward high speed and low power. There are two segments to the static 4K RAM market: μP-based systems in which low power is desirable and 150 to 200 ns or slower speeds are acceptable, and add-on/in memories requiring high speed (50ns). The current art in N channel static RAMs is at the 4K level with both 1Kx4 and 4Kx1 versions available. This year, sub-100ns versions and 150ns or up versions of both the 1Kx4 and 4Kx1 organizations appeared – all with the chip select power down feature. In addition, some vendors have already developed 16K static RAMs – the next generation for high-speed cache and control-store memory. With an inherent speed edge over dynamic devices, static units are now also pressing dynamic chips in the area of power dissipation.

Static devices inherently dissipate relatively large amounts of power through each cell's latched gate resistors, and buffers are also power hungry. Polysilicon resistors, however, lower the former loss, while several newly developed circuit techniques minimize the latter loss mechanism. Power gating is one such method. With this technique, power goes to high dissipation elements only when the memory device is selected. Another technique, edge activation, reduces power consumption by eliminating DC paths; power is only dissipated when charging and discharging capacitors. Address activation primarily serves high-speed systems.

Whether power-down modes are used or not, a static RAM still uses a lot of power in read or write modes. However, investigators have modified the standard six-transistor cell configuration so that some RAM designs require only four cells and therefore dissipate less power. Phasing this and other power-reducing techniques will eliminate the major drawback to using static devices in large memory systems.

When dynamic RAMs first reached the market, they were viable choices only for minicomputer and mainframe applications; thus, IC makers concentrated on nx1 organizations to let large computers capitalize on the word depth possible with these arrangements. But x4 and x8 organizations, always possible with dynamic RAMs, are now appearing. Part of the stimulus for these new organizations comes from a desire to take advantage of current advances and provide interim design alternatives until each new generation of denser memories appears. Also, dynamic NMOS RAMs are now faster; they can compete with static devices in many applications. However, the big development in 1979, and the thing to watch for in 1980, is the 64K dynamic RAM.

Will 64K RAMs kayo 16K RAMs?

Highlighting the memory developments over the past year is the single-supply 65,563-by-1-bit dynamic RAM – the heir apparent to the industry-standard 16K device and an advance resulting from pressure put on semimakers for higher-density memories. With it, board capacities can be quadrupled with almost no power and performance penalties. Although dozens of chip makers produce similar 16K RAMs, design approaches to the 64K successor took many forms.

Fujitsu's MB8164 and Texas Instruments' TMS 4164 were the first 64K dynamic RAMs to reach the market. Many other manufacturers – including Signetics, AMD, Fairchild, Intel, Mostek, Motorola, National Semiconductor, OKI, Panasonic, Siemens, Toshiba, and Zilog – also developed 64K parts, so at least half a dozen viable sources will appear this year.

With the technology used, on-chip transistors will be closer and smaller, shortening propagation delays as well as overall access times. That means 64K access should range from 80 to 150ns instead of the typical 120 to 250ns.

16K RAMs win popularity contest

Perhaps partly because of this uncertainty in the 64K market, customer demand for 16K dynamic RAMs has exceeded many manufacturer forecasts, putting these parts in short supply. As a result, the product lifetimes of 16K devices have been extended, and some manufacturers have applied their latest processing and design advances to produce "new" 16K chips with impressive specs. Most of these improved 16K devices need only +5V, and some will boast access times shorter than 100 nsec; used in memory systems, they will permit simpler upgrades to 64K parts than would three-supply devices.

Most of the coming crop of 5V, 16K x 1 RAMs will permit simple system upgrades to 64K units. However, they will require minor redesigns of current 16K systems – changing the bypass capacitors, strapping the supply pins, modifying the address connections . . . perhaps even altering the refresh timing.

Chip makers agree: the single-supply 64K RAM is a double advance. Quadrupling density of today's RAMs is tough enough; redesigning for single 5V-operation doubles the effort. That's why several firms struggling with the power supply problem chose to develop a 5V-only 16K RAM as a stepping stone to the 64K part.

Ironically, that interim measure could push back industry acceptance of the 64K RAM by a year or two. Chip makers (National Semiconductor, Intel Corp, Mostek Corp, and Motorola Inc.) build single-supply 16K RAMs with almost exactly one quarter of their 64K designs. Not only do these parts have better yields than next-generation devices, also they have so much more to offer than the three-supply 16K RAM – superior access time that might fall as low as 80ns, lower power and a scaled-down die size – that customers might be willing to pay a premium for them.

ROMs, PROMs and relatives

Developments over the next few years will focus on erasable-type ROMs. 1979 saw the first 64K UV-erasable PROM. The largest segment in the programmable market is the MOS UV EPROM. Current EPROMs are at the 16K and 32K levels, and 64K devices are imminent. All EPROM makers are trying for quicker access. EPROMs have the slowest access of all NMOS memory technologies (350 - 450ns). But problems occur with newer μPs which lose their speed advantage if EPROM program storage cannot meet the 100- to 200-ns cycle times. Will chip makers get access times down? They're trying.

Offering the fastest EPROMs available, the long-controversial technology of amorphous semiconductors just headed for market. Besides storing 1000 bits and accessing any bit in 10ns, amorphous semiconductors allow each bit of data to be individually erased and reprogrammed. ECD Inc., developer of this technology, distinguishes this capability with the acronym EAROM (electrically alterable PROM).

The parts that will eventually dethrone UV EPROMs have surfaced – electrically erasable PROMs (EE-PROMs). Slow to develop because no forced electrical leakage has proven as reliable as the photon-generated leakage of the UV devices, EE-PROMs are researched in many chip manufacturer labs, though last year there were few commercial announcements of EE-PROMs as EPROM replacements.

EAROMs and EEPROMs differ in application. EEPROMs replace UV EPROMs (EAROMs are aimed at applications requiring more program/erase cycles); and, as such, perform differently. For instance, EEPROMs must have much shorter access times, compatible with EPROMs. EEPROMs can only be block erased and lack flexibility of being word erasable like EPROMs. But since UV EPROMs aren't word erasable, this isn't bad. In addition, erase time is much longer than that for the EAROM, but still exceeds UV EPROM speed.

A look in the crystal ball

In the next few years, a hierarchy of these nonvoltatile memory products will fall out: ROM types that are rarely reprogrammed but offer high density and relatively quick access times to replace EPROMs; read-mostly memories that provide a fair amount of endurance for the daily power-down situations to which cash registers and TV tuners are exposed; and nonvolatile RAMs that provide fast program and erasure and superlative endurance of 10 cycles or more.

In addition, the trend toward pin-compatible ROM, PROM and RAM families will continue, allowing designers to substitute one device type for another at will. Also, expect increased activity in byte-wide memories as the semiconductor industry attempts to achieve the next capacity improvement above 64K. This increase will probably require a combination of process advances, new circuit design and larger dies.

Finally, as new high-volume markets open up, expect semi makers to add special features – such as counters and timers – to their 4K and 16K designs rather than squeeze more bits into the smallest possible space.

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2. Mini-computers
3. Computer Peripheral Equip.
4. Data Processing Systems (systems integration)
5. Office and Business Machines
6. Test, Measurement and Instrumentation Equip.
7. Communications Systems and Equip.
8. Navigation and Guidance Systems and Equip.
9. Consumer Electronic Appliances
10. Industrial Controls, Systems and Equip.
11. Components and Subassemblies
12. Materials and Hardware
13. Aircraft, Missile, Space and Ground Support Equip.
14. Oceanography and Support Equip.
15. Medical Electronics
16. Industrial Co. within the OEM Incorporating Electronic Equip. in Their End Product, Not Elsewhere Classified
17. Independent Research, Test and Design Laboratories and Consultants (only if you are not connected with a manufacturing company)
18. Govt. Agencies and Military
19. School, University or Library
20. Industrial companies using any electronic products in their manufacturing, research or development activities
21. Commerical user of electronic equipment

PART V Within the next 12 months I expect to select, specify or buy (please circle no more than 20 items; read carefully before selecting):

TEST & MEASUREMENT INSTRUMENTS
1. Analyzers, Waveform
2. Analyzers, Logic
3. Bridges
4. Comparators
5. Calibrators
6. Calibration Standards
7. Counters
8. Current Sources
9. Data Acquisition Systems
10. Meters, Phase
11. Meters, Benchtop
12. Meters, Hand-Held
13. Meters, Panel
14. Spectrum Analyzers
15. Oscilloscopes
16. Probes, Hand-Held
17. Function Generators
18. Recording Instruments
19. Data Communications Testers
20. Signal Generators

MICROPROCESSOR TROUBLE SHOOTING TOOLS
25. Logic Probes/Analyzers
26. Microprocessor Analyzers
27. Microprocessor Development Aids
28. Portable Digital Testers
29. Portable Microprocessor System Testers
30. Signature Analyzers

FIELD & SERVICE TESTERS
35. Service Test Consoles
36. Portable Testers

TEST HARDWARE/SERVICES
40. Buses/Interface Adaptors
41. Clips, Test
42. Connectors, Test
43. Electrical/Electronic Test Services
44. Fixturing, Test
45. Probe Cards
46. Probes/Contacts, Test
47. Rental Services
48. Sockets, Test
49. Switching Matrices

SOFTWARE
55. Test Software Development Aids
56. Test Software
57. Test Software Services
58. Software Test

PRODUCTION QA TEST
64. Bare PC Board Testers
65. Burn-in, Aging Equipment
66. Cable/Harness/Wiring Testers
67. Discrete Component Function Testers
68. Environmental Test Equipment
69. Handlers/Sorters
70. IC Component (including Memory & Microprocessor) Function Testers
71. Inspection Equipment/Tools
72. PCB Assembly Testers, Edge-Card
73. PCB Assembly Testers, In-Circuit
74. Surface Analysis, Measurement
75. Systems Testers
76. Temperature Cycling/Measurement Equipment
77. Wafer Probe & Measurement

PART VI Specifying/Purchasing/Responsibility/Authority
(Fill out completely)

I *recommend* purchase of equipment/instruments/services that cost:
1. < $1K
2. $1-5K
3. $6-10K
4. $11-50K
5. > $50K

I *authorize* purchase of equipment/instruments/services that cost:
6. < $1K
7. $1-5K
8. $6-10K
9. $11-50K
10. > $50K

I recommend *or* authorize purchase of:
11. Test instruments only
12. ATE only
13. Both
14. Other ________

PART VII Circle all that describe your work:

1. Incoming inspection
2. Production testing
3. QA/QC Reliability
4. Prototype evaluation
5. μ Processor devel.
6. Design test
7. Field service
8. STDS/Calibrat.

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Designers' Notebook

8086 Single-Step Eases Software Debugging

Currently two execution vehicles, the SDK-86 System Design Kit and the iSBC 86/12 Single Board Computer are avilable to test and debug 8086 software. Both of these are easily interfaced to Intellec Development Systems which allow the downloading of user software into the execution vehicle's RAM for subsequent execution. The SDK-86 and iSBC 86/12 board utilize on-chip debugging features of the 8086 to provide user debugging aids. One of these powerful features is the single-step interrupt.

```
PUSH   AX    ; SAVE AX
PUSH   BX    ; SAVE BX
PUSH   CX    ; SAVE CX
PUSH   DX    ; SAVE DX
PUSH   BP    ; SAVE BP
MOV    BP,SP ; INITIALIZE BP
```

Fig 1 Save registers and initialize BP.

The single-step interrupt provides a way of examining processor operations while single-stepping through the user program. When the trap flag (TF) in the flag register is set, a type 1 interrupt is generated after each instruction is executed. The interrupt service routine can then provide a user interface which performs a variety of diagnostic functions. It can simply display the contents of flags and registers, or, if desired, it can display selected memory locations and input ports.

After receiving the single-step interrupt, the 8086 pushes the flag register (FLAGS), code segment register (CS), and instruction pointer (IP) onto the stack and resets the interrupt and trap flags. Resetting the trap flag allows the single-step interrupt routine to run normally without single-stepping. When the diagnostic functions are complete, an interrupt return instruction is executed which pops data from the stack into IP, CS and FLAGS. This restores FLAGS with TF set and allows the next users instruction to be e executed followed by a type 1 interrupt.

Upon entering the single-step interrupt routine, the state of the user program must be preserved by saving the contents of registers on the stack. Only those registers that are used to provide the diagnostic functions are saved. For example, assume that the AX, BX, CX and DX registers are used. Next the contents of the base pointer

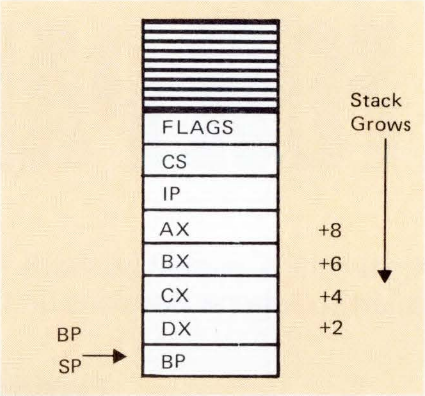


Fig 2 Contents of stack.

(BP) are saved on the stack and the stack pointer (SP) contents are transferred to BP. Figure 1 shows the 8086 instructions to accomplish this and **Fig 2** displays the contents of the stack. Assume that the single-step routine now displays the register contents. Copying SP into BP allows the 8086's based addressing mode to access all saved data without popping data from the stack. Access to this data is accomplished by adding the contents of BP with an offset. For this example, BP plus 4 allows access to the saved CX data. **Fig 3** shows code that accesses and prints the saved values of AX, BX, CX and DX. Separate print procedures are called with the desired register value passed in the DX register. Note that the use of BP also allows procedures called by the single-step routine to access the saved data.

This technique displays diagnostic data after each instruction is executed. As the user software development progresses it is unnecessary and even undesirable to examine processor operations after every instruction. When using top-down structured programming techniques, it is desirable to examine operations only for the newly added software module. This can be accomplished by programming the single-step routine to provide diagnostics when instruction pointer values are those of the new modules. The single-step routine can be programmed to print diagnostics and continue execution of the user software or suspend execution until some external stimulus is received, such as a prompt from the system console. More powerful capabilities can be programmed into the debug routine such as providing notice when a memory location or input port has changed to a predetermined value or when the processor attempts to execute code outside of the user program. The single-step routine can also be programmed to execute a section of code for a specified number of times before providing diagnostics. It should be noted that use of the single-step interrupt does not allow real-time user program execution since this interrupt occurs after each instruction.

```
MOV    DX, [BP + 8]   ;   ACCESS   AND
CALL   PRINT AX       ;            PRINT AX
MOV    DX, [BP + 6]   ;   ACCESS   AND
CALL   PRINT BX       ;            PRINT BX
MOV    DX, [BP + 4]   ;   ACCESS   AND
CALL   PRINT CX       ;            PRINT CX
MOV    DX, [BP + 2]   ;   ACCESS   AND
CALL   PRINT DX       ;            PRINT DX
```

Fig 3 Access and print saved registers AX, BX, CX and DX.

Hal Kop, Intel Corp., Santa, Clara, CA 95051.

Rate this design: circle 9L, 9M or 9H on Reader Inquiry Card.

Designers' Notebook

8080 Routine Displays Console Messages

I just saw the Little Program "8080 Routine Displays Console Message" (pg. 94) in the October 1979 issue. The routine is shown below.

```
PUSH    H
CALL    MSGXP
DB      'READ ERROR'
DB      0
POP     H
.
.
.
MSGXP   POP     H
MSGX1   MOU     A,M
        CPI     0
        JZ      MSGEX
        CALL    CO
        INX     H
        JMP     MSGX1
MSGEX   INX     H
        PCHL
```

I noticed some things which could shorten your MSGXP routine. First, since you have to increment HL after getting each character and also before exiting the MSGXP routine, you can get by with only one increment statement. Second, if you simply need to test the A register for the zero condition, it is shorter and faster to use "ANA A" instruction. Implementing these changes yields the following:

```
MSGXP   POP     H
MSGX1   MOU     A,M
        INX     H
        ANA     A
        JZ      MSGEX
        CALL    CO
        JMP     MSGX1
MSGEX   PCHL
```

If CO returns the register intact, more reductions are possible. A typical form for CO is as follows:

```
CO      MOV     C,A
CO1     IN      UARTS
        ANI     2
        JZ      CO1
        MOV     A,C
        OUT     UARTD
        RET
```

By using the fact that CO returns A intact, we get the following:

```
MSGXP   POP     H
MSGX1   MOU     A,M
        INX     H
        ANA     A
        CNZ     CO
        ANA     A
        JNZ     MSGX1
        PCHL
```

Since most terminals ignore null characters, one last byte can be removed from the routine.

```
MSGXP   POP     H
MSGX1   MOV     A,M
        INX     H
        CALL    CO
```

Thus, the 16-byte routine shown in the October Designers' Notebook can be reduced to only 11-bytes. While saving 5 bytes may not be important in a "quick and dirty" application, these techniques may also be applied in time-critical programs.

Tim Quilici, Rockwell International, M.S. 401-137, Dallas, TX 75207.

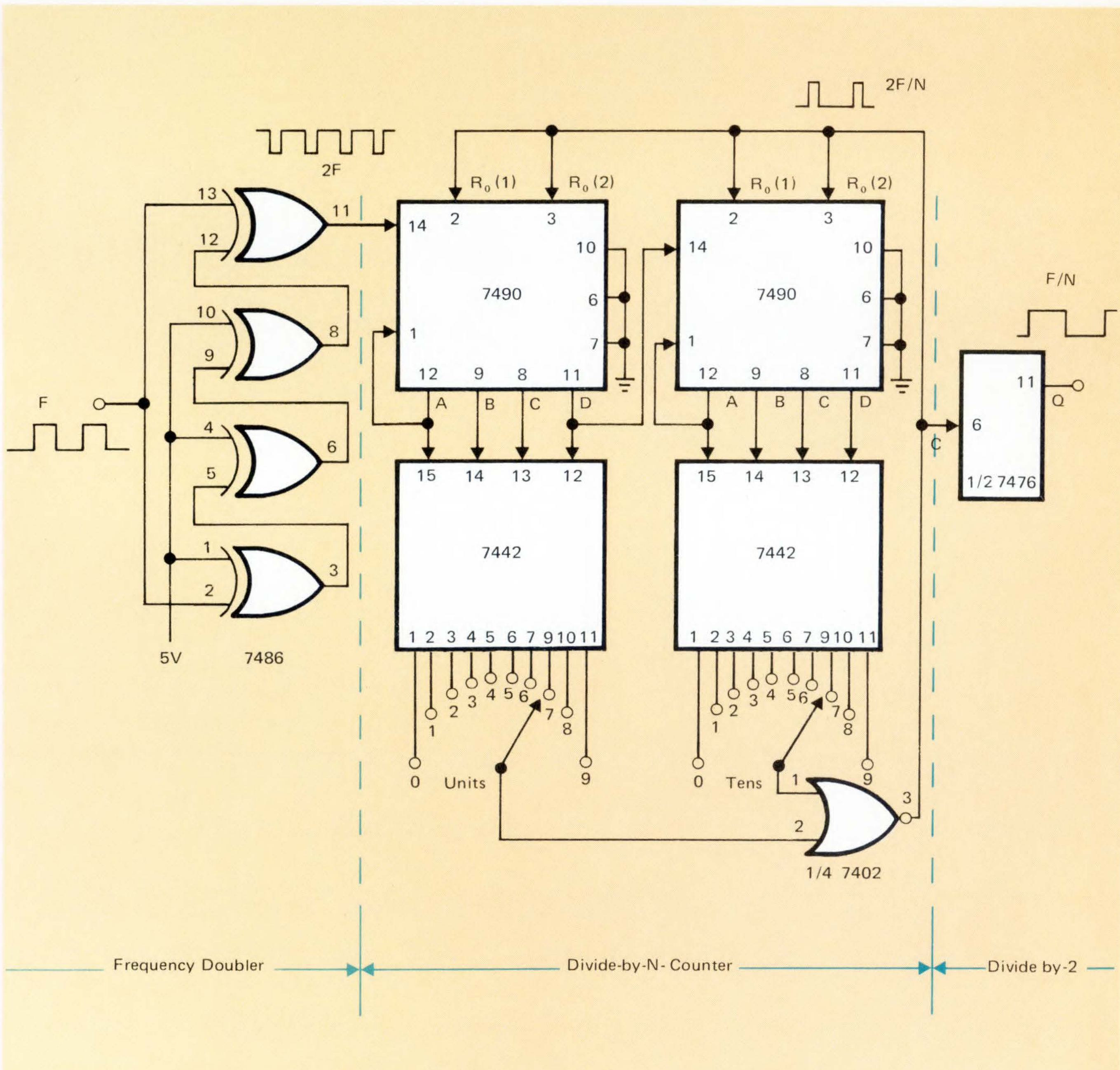
Rate this design: circle 11L, 11M or 11H on Reader Inquiry Card.

Decimally-Programmable Divide-By-N-Counter Maintains Pulse Symmetry

The divide-by-N-counter with symmetrical output can be programmed decimally via thumb-wheel switches. The circuit consists of frequency doubles, divide-by-N-counter and a flip-flop for divide-by-two operation to get a symmetrical waveform at its output. The frequency doubler is used to obtain narrow pulses, at both the leading and trailing edges of the input waveform. These narrow pulses of frequency 2F are then applied to the divide-by-N-counter. When the counter (7490s) reaches a number equal to the set value N, the NOR gate output goes to "1" level, thereby resetting the counter to zero. As soon as the counter is reset to zero the NOR gate output assumes "0" level. Thus a narrow pulse is generated at the NOR gate output for every N count, resulting in a pulse train of frequency 2F/N. This is further divided by 2 in a flip-flop to obtain a squarewave output of frequency F/N.

V.L. Patil and Dilsukh Jain, NRSA, Hyderabad, 500 037, India.

Rate this design: circle 10L, 10M or 10H on Reader Inquiry Card.



Decimally-programmable Divide by -N- counter with symmetrical output.