VOLUME 9, NO. 11 NOVEMBER 1979

# Digital Design

The Magazine of Systems Electronics

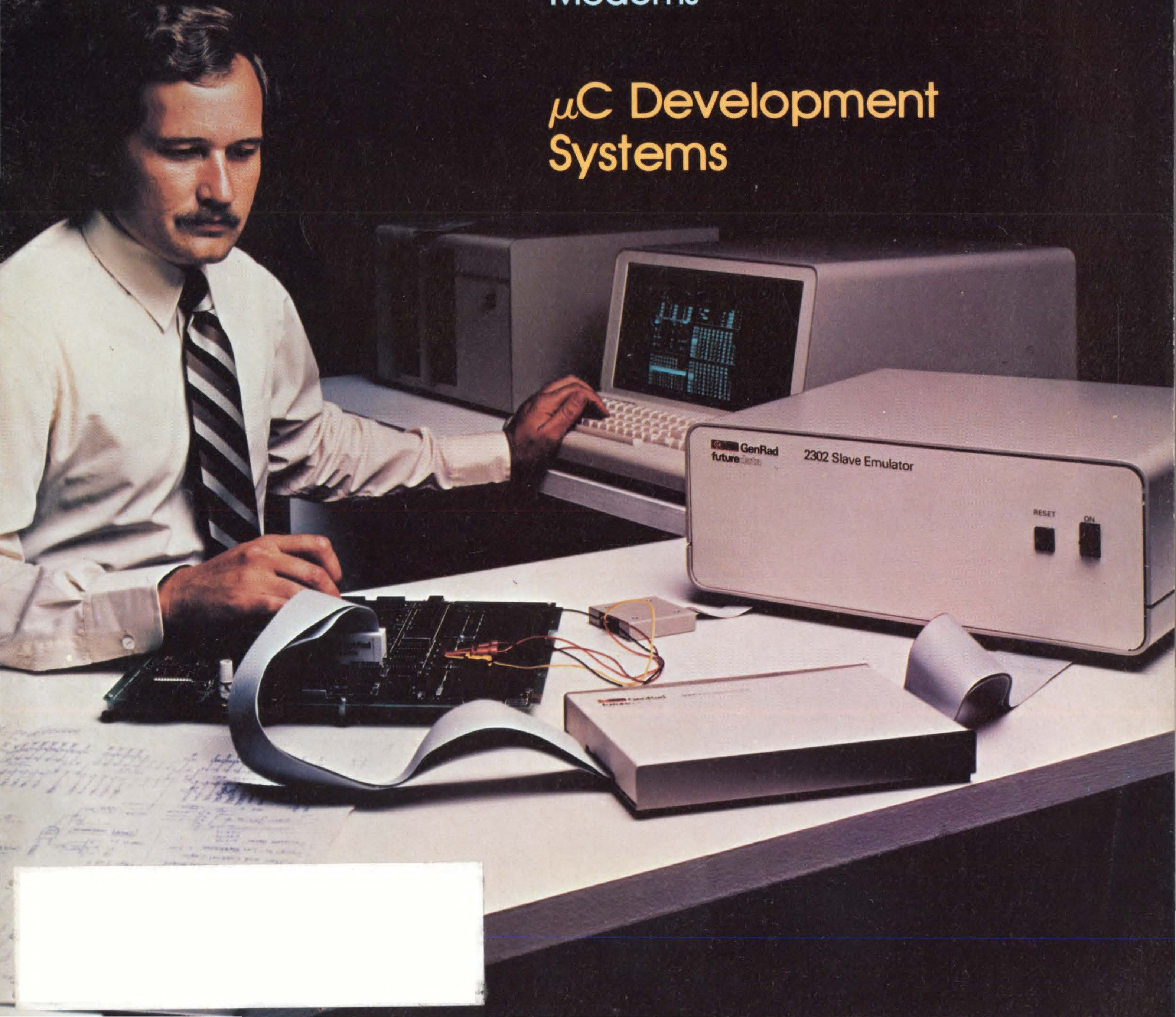
Video Terminals

Bubble Memories

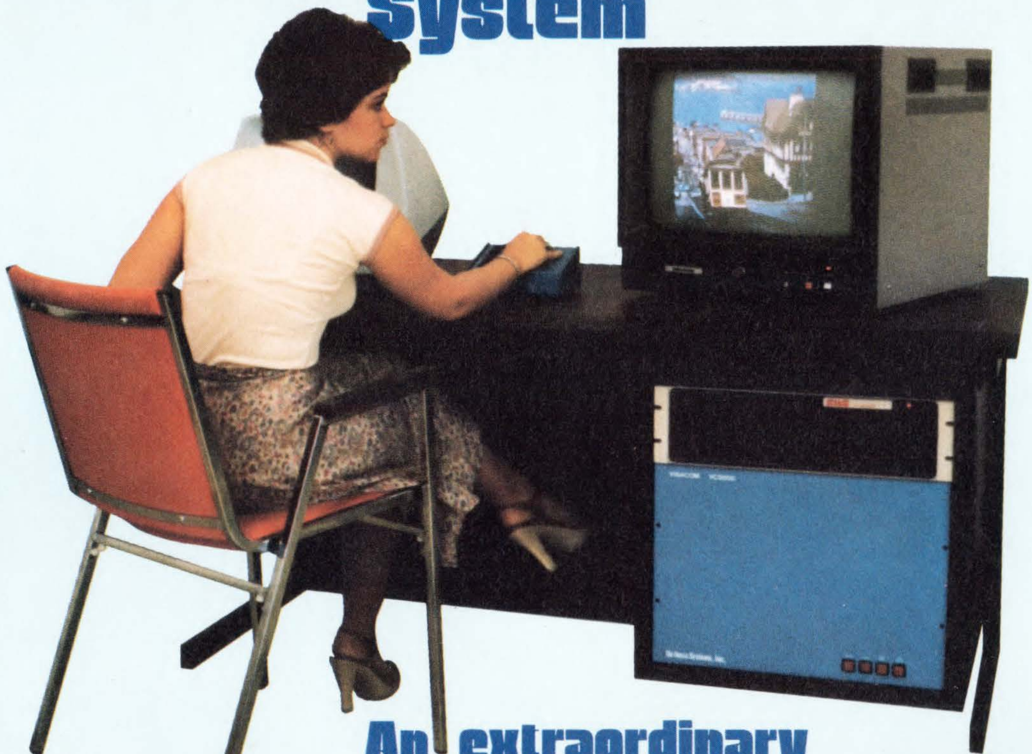
Intelligent Terminals

Modems

## μC Development Systems



# From DeAnza Systems VISACOM Visual Computer System



## An extraordinary combination of micro-computer power and DeAnza Systems imaging expertise

VISACOM is a new image graphics concept that provides enormous flexibility for the user. It is powered by a DEC LSI/11 micro-computer with the ability to address 512K bytes of memory. The system operates under RT11 and has all the standard DEC LSI/11 software.

The system can operate off-line with floppy disks or interface to a host computer.

**VISACOM as a Computer**

- Addresses 512K Bytes memory
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- DEC LSI-11 compatibility
- RT11 Operating System
- Fortran IV
- Q-Bus compatible peripherals
- Dual access MOS RAM memory
- User software package
- RS 232 and DMA interfaces

**VISACOM as a Display System**

- 512 X 480 Image Window
- 16 bits per pixel
- Zoom and Scroll
- Intensity Transformation units up to 4096 words
- Independent A/N and Cursor Overlays
- User software package

**For further information and a list of satisfied users, contact DeAnza Systems, Inc., 118 Charcot Ave., San Jose, CA., 95131, (408) 263-7155.**

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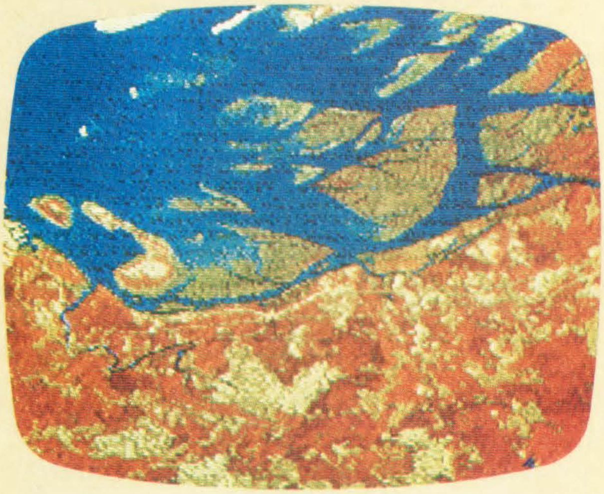

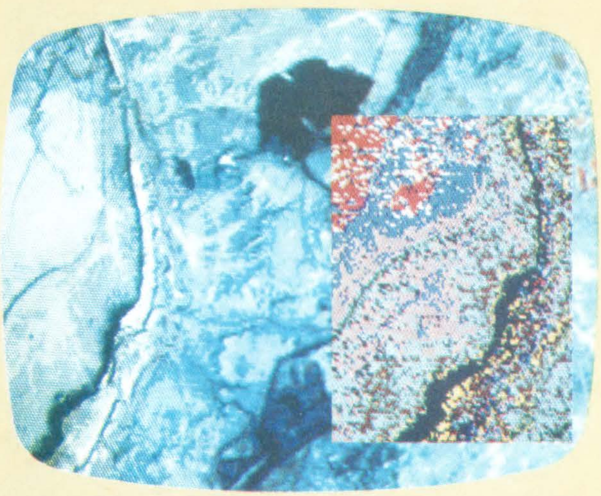

Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
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So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

## GRINNELL SYSTEMS

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VOLUME 9, NO. 11 NOVEMBER 1979

# Digital Design

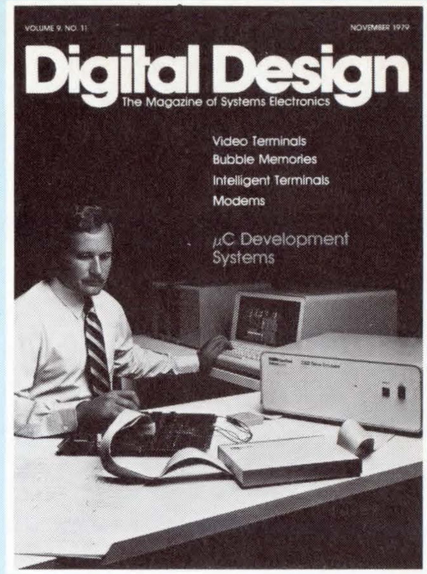
The Magazine of Systems Electronics

## Features



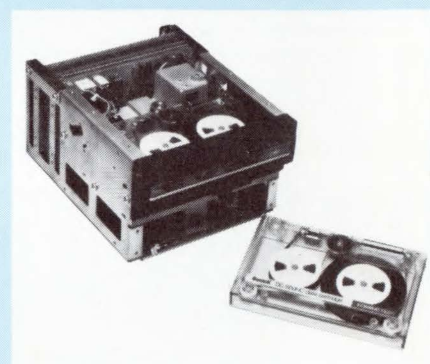
## Departments






**ON OUR COVER**

With new architecture, a new generation of microcomputer development systems provide users with vastly improved development capability that eliminates previous compromises in development systems. (*Photo Courtesy of Gen Rad/Futuredata.*)



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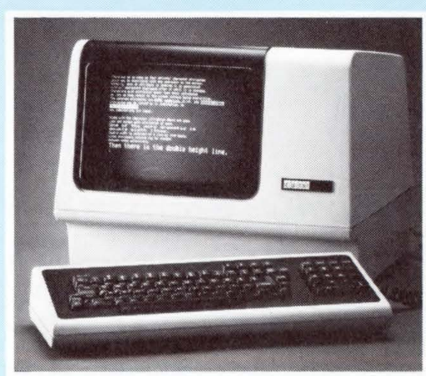

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**DIGITAL DESIGN**
**Publication number: USPS 407-010**

Published monthly by Benwill Publishing Corp., a Morgan-Grampian Company, 1050 Commonwealth Ave., Boston, MA 02215. Controlled circulation paid at Long Prairie, MN 56347.

# Digital Design
The Magazine of Systems Electronics





**Editorial Offices**
Publishers Office: (213) 478-3017
Western Office: (714) 675-7123
Eastern Office: (617) 232-5470

**Director of Publications** Harold G. Buchbinder


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BPA CIRCULATION: 57,654 (OCTOBER 1979)

Published monthly by Benwill Publishing Corporation, a Morgan-Grampian Company, Harold G. Buchbinder, Chief Executive Officer; George Palken, President; Domenic A. Mucchetti, Treasurer; Executive, Editorial and Subscription Offices, 1050 Commonwealth Ave., Boston, MA 02215. Telephone: (617) 232-5470.

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Circle 9 on Reader Inquiry Card

# Letters

## Misleading

Dear Editor:

I was happy to read your July speakout discussing open universities as a useful way for overcoming high tuition. I am confident that the considerable opinion against open universities from your readers is based largely on misinformation or lack of information regarding what open universitiies are and can do for the student.

In the United States the term "open university" has fallen into considerable disfavor. Contrary to the wide acceptance which "open universities" have received in many European countries, such universities have been greatly misunderstood in America. A more recent term which more adequately describes the "open universities" is external universities.

Accrediting associations are now recognizing the practice by many universities of evaluating prior learning from a variety of sources as well as evaluating and crediting experience as a viable and needed educational function. It is interesting to note that the National Institute of Education has said that of all adult education going on in America today only 23% of it is conducted within the auspices of a recognized university; 77% of it goes on outside of university domain. This adult education is specific and practical and frequently directed towards the solving of particular needs of the student. This learning, we believe, deserves evaluation and academic credit for it is equal if not superior in value to much of the education conducted on university campuses.

Finally, your readers need to understand that the quality of engineering education need not suffer merely because the course is not conducted on the campus. Speaking for our institution, I can assure you that our faculty are of a caliber equal to that of any university you can mention.

Sincerely,
Eugene G. Stone
President
Clayton University
Box 16150
St. Louis, MO 63105

## Likes TRS-80

Dear Editor:

In response to your article on microcomputer software, "Software Bedevils Small Business μCs" by P. Snigier (July 1979), I am shipping you, direct from our warehouse, three TRS-80 business packages. These programs are among 50 packages currently complete in fields ranging from Real Estate to Receivables and Construction Estimating to Manufacturing Inventory.

As you will see, the manuals are easy to understand, professionally packaged and reasonably priced ($100-$200 each). What you won't see is the substantial investment we have made in thc development and testing of these programs. We have standardized menus and input formatting, trapped all system errors for auto-recovery, maximized storage through data compression, and generally pushed the TRS-80 as far as it can go.

Off-the-shelf software is a new market. We don't have the luxury of installing the package, the benefit of onsite training or the sophisticated user base enjoyed by the minicomputer companies. These problems required novel solutions: (1) there is a customer service department with 7 WATTS lines and 4 direct lines, (2) programmers in this department train customer service reps on each new package, (3) each program endures a 60-day pounding by a Software Evaluation department, (4) manuals are written at a 7th-grade reading level, (5) total keyboard control is maintained at all times (for example, only numeric keys are active on numeric inputs), (6) test sites in local small businesses validate every package and (7) if bugs are found in the field, programs are replaced free. These are just a few of the steps we have taken to insure customer satisfaction.

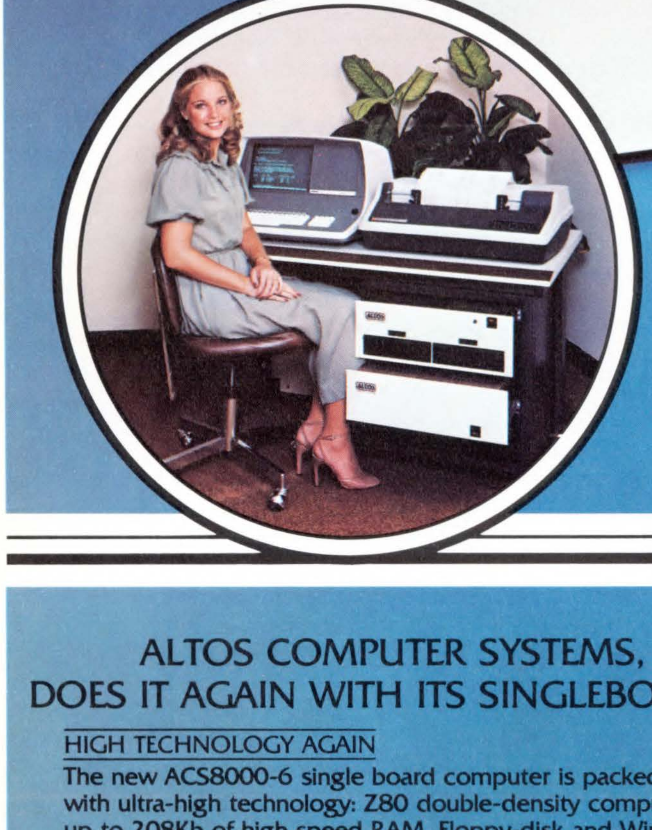
There are many good software packages now available for microcomputers. The Structured Systems Group (Oakland, California) has several fine products and Peachtree Software (Atlanta, Georgia) has well organized and reliable packages. Other firms are following suit with accounting packages tailored for specific industries.

I hope we respond to the further needs of the SBC user quickly enough to avoid any more pot shots.

Van S. Chandler,
Director
Computer Applications
Radio Shack
Fort Worth, TX

# ALTOS COMPUTER SYSTEMS PROUDLY ANNOUNCES

## SUN-SERIES ACS8000-6

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Double Density Z80 Micro-Computer
plus Twin 8" Floppies
plus 14.5Mb Winchester Disk
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And more! 4 user CP/M® for under $12,000!

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### HIGH TECHNOLOGY AGAIN

The new ACS8000-6 single board computer is packed with ultra-high technology: Z80 double-density computer, up to 208Kb of high speed RAM, Floppy-disk and Winchester Hard Disk controllers, DMA, up to 6 serial/2 Parallel I/O, optional 32 bit floating point processor . . . All on One Board, fully socketed, fully documented reliable and maintainable.

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We're staying with Shugart for both floppies and Winchester hard disk. Why? Simple, low price, solid reliability and they're our next door neighbor. Our single board computer supports up to 4 Mbytes of floppies and 58 Mbytes of Winchester running under AMEX.

### MINI PERFORMANCE FOR 1/2 COST

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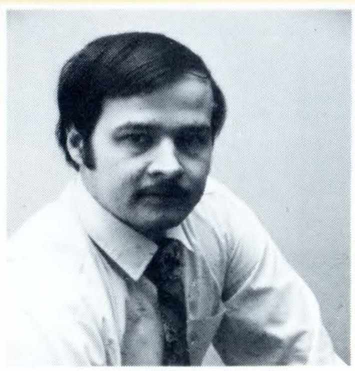
# Speakout

Paul Snigier, *Editor*

# Designing In The 1980s: Heuristic Outlooks Needed



Even though I find a recent projection estimating logic gates/single CPU chip in 1990 will exceed the *combined* gates in *all* of today's CPUs a bit hard to swallow, the future will see far larger devices, with improved CAD techniques needed to handle them. Yet, despite these increases in computational power, are there as many uses for, say, an 8-Mbit CPU chip as we might think? Probably not. The limitations of the 1980s won't be in the semiconductor processing industry, but in terms of user needs. Aside from memory, which apparently can grow without limitation, not even the computer industry will have much need for some of these larger devices. But a worse obstacle exists – development – and is aggravated by the growing chip complexity.

With LSI/VLSI, the complexity of $\mu$Ps, $\mu$Cs, ROMs and other devices has reached a level where traditional design methods prove tedious or impractical. To handle this complexity, software/hardware designers must turn to CAD, which has achieved its most notable success at the manufacturing and logistics stages (and even then, is underutilized), and less success elsewhere.

But designers' reluctance to use CAD in design is justified: unfortunately, CAD has a long way to go in aiding in the conceptual design stages. Attempts have been marginal in creating realistic synthesis techniques, specification and evaluation languages, design methods, algorithms for test sequence generation and so on. The problem is an inherent one involving a serious limiting factor – computation time, which expands very rapidly with increasing variables (combinational explosion) and requires vast storage and computation. Since they examine variables in every possible combination, blind search algorithms use time exponentially. Increasing device sophistication and speed, which ironically creates these computational obstacles, also aids in increasing both storage and computation capability of CAD systems. This is a losing race, as increasing CAD storage and computational muscle cannot keep up with ever-larger system designs and will ultimately approach an asymptotic computational limit set by nature – the speed of light. With the essentially unbounded input sets of today's systems, designers' attempts to tightly constrain such input sets (analogous to closed systems) will usually defeat system design objectives.

Better heuristic techniques are needed. CAD systems using formal algorithms, though they may generate an exact optimum solution, simply can't handle today's many-variabled, real-world problems – let alone what's coming in the 1980s. Heuristic techniques are probabilistic methods that search for certain patterns and satisfactory solutions, not exact ones. For example, consider this open system: the case of user interaction in modifying the basic input set, even going so far as reconfiguring a complex OS's original structure, or algorithm, if you will, to perform many different functions.

Despite use of heuristics by CAD researchers, not enough has been done. Since many of the problems (particularly pattern recognition) that AI researchers encounter are similar to CAD problems, we feel that closer cooperation could benefit CAD system development.

But, perhaps part of the problem is ours. Unfortunately, EEs suffer from a "black box mentality" that colors our outlook. We are conditioned from our first college courses to think in terms of deterministic, closed systems – black boxes which do not interact with the real world, each with a neat transfer function that provides a corresponding output for each set of given input conditions.

Such a design philosophy will hamper our outlook in the 1980s. With the growth of LSI and VLSI, no longer can we afford to design and test to see that a known, correct output occurs for each and every input condition, since the input set is unbounded from all practical considerations. Treating a system as open – that is, responding to external inputs (from the total environment, or real world) – is the only alternative for complex systems.

# Tālos introduces the Class III Graphic Digitizer.

Class III adds a new dimension to the extensive line of Talos digitizers. Developed specially for graphics input, this new digitizer provides super durability and real convenience.

The digitizing surface is super thin, only ½ inch thick, making operation very natural. This low profile surface is constructed of hard formica encased in a sturdy metal frame so Class III is ready to stand up to heavy-duty use.

As an added feature, Class III comes equipped with a new Talos exclusive, a completely electronic pen with no mechanical parts to wear out. And the tip of the pen is tapered to improve work visibility.

Class III offers 400 lines per inch resolution, switch selectable point and run modes, and a choice of three interfaces, 16 Bit Parallel Binary and BCD, RS232C, or GPIB.

Class III is reliable, durable, and very affordable. Ask about our OEM discount schedule.

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- **System $5350, add-on disk $2990.**

**Corvus offers a complete systems solution to the mass storage problem of micro computers. In a package smaller than a briefcase, we provide an intelligent controller, disk, and personality module. Call or write today for additional information. Get up to speed with Corvus.**

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408/246-0461

*Distributor information and dealer package available on request.*

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# Technology Trends

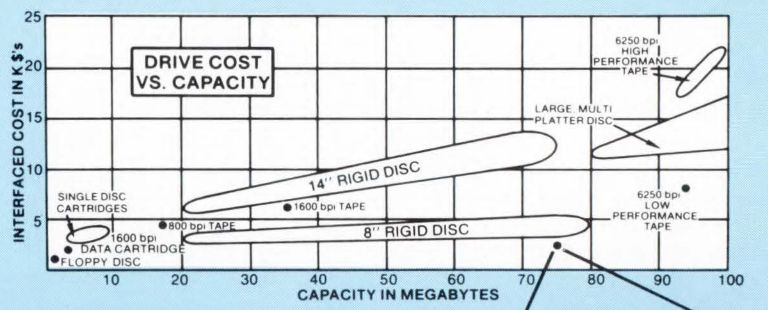
## 75-Megabyte Data Cartridge System Improves Disk Backup

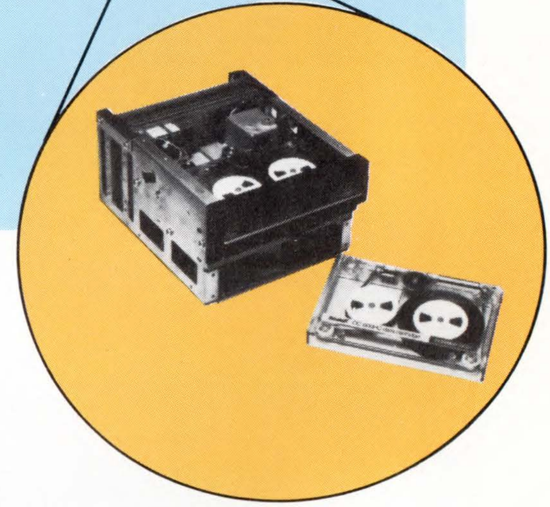
A new generation data cartridge system that gives a 4 X 6" data cartridge more than twice the capacity of a 2,400' reel of 1/2" 1,600bpi computer tape or dozens of floppy disks–the 3M HCD-75 High Capacity Cartridge Drive and its new cartridge – provide 75 Megabytes of user data storage capacity (total tape capacity of 144 Megabytes includes 3M formatting). This capacity, coupled with an information transfer rate of up to 4 Megabytes/sec,– higher than any current system, makes the system a good backup for fixed disk drives, such as the 8" and 14" Winchester type disk drives.

Said to be the "first truly inteligent data cartridge drive system," the high-capacity system is well suited for disk backup, program distribution, data interchange, journal and archival applications.

The higher capacity, 48 times that of the present data cartridge developed by 3M, is achieved through the combination of a new 16-track drive, special magnetic tape and new recording methods.

The drive utilizes a single specially designed ceramic R/W head. A μP-controlled servo mechanism positions the head to address one of 16 tracks across the 1/4" tape width. Data is written or read in a "serpentine" mode (alternate forward and reverse directions as track assignments change) to eliminate time-wasting rewinds.



HCD-75 high capacity cartridge drive.

Micros are used for tape drive control, diagnostic self-test (cycled continuously while the system is idle), and sophisticated error-detection during data read functions. μP control of tape transport operations eliminates all manual adjustments.

Although the DC600 HC tape cartridge is similar to 3M's original

**Capacity & Cost Comparisons Of Selected Magnetic Media Potentially Used For High-Capacity Backup**

| | Capacity of User Data in 1000-Byte Blocks | Est. Cost/MB | Media Unit Price(approx.) | Rough Ballpark of Drive Cost (single unit with formatter/controller |
|---|---|---|---|---|
| 8" floppy diskette dbl. sided/dbl. density | 1.2MB | $8.00 | $ 9.75 | $1,000-1,500± |
| 2400' 1/2" tape on 10-1/2" reel–1600bpi | 24 | $ .80 | $19.50 | $6,500± |
| 2400, 1/2" tape on 10 1/2" reel– 6250bpi | 60 | $.33 | $19.50 | $8,500± (low performance)<br>$17,000-23,000± (high performance) |
| 3M DC300A data cartridge – 1600bpi | 2.3 | $8.50 | $20.00 | $2,000± |
| 3M DC600HC data cartridge – 10,000bpi | 75 (144 unformatted) | $ .40 | $30.00 | $2,150 |

**Cost of the cartridge medium for the new 3M HCD-75 system – based upon user storage capacity – represents a reduction of over 20 times. In ANSI-compatible systems using the standard DC300 cartridge, medium cost is $8.50/MB compared to $.40/MB in the new system using the DC600HC High Capacity Data Cartridge.**

Our raster-scan systems are fast becoming leading contenders for top honors in the digital computer graphics and image display field. The clarity and conciseness afforded by monochrome resolutions as high as 1280 X 1024 and full-color versions to 1024 X 1024 pixels, are good reasons why. There's many more . . . let's peruse just a few.

**16-Bit High-Speed Programmable Processor.**
Consisting of 16 general purpose and 9 operational registers, plus a set of 55 mnemonic instructions, along with 16-bit writeable control storage, the processor can manipulate data at internal cycle rates of 150 ns.

And it provides automatic DMA access, selective erase, user selection from a range of over 16-million different color intensities, plus flicker-free operation.

**Modular, Versatile Hardware.**
Since Genisco's systems are capable of being expanded from a single monochrome memory plane to a number of planes that support the full range of gray scales or colors required, you can inexpensively start-out and add-on as needed. Our monitor control module lets you operate up to 12 monitors, mix TV/Video and remotely monitor — as well as fill areas outlined in the bit-map memory — and allowing RS232 interfacing with a keyboard, trackball, joystick or graphics tablet.

Genisco also provides a full complement of standard minicomputer interfaces or can economically build one to suit. Scroll/Zoom and high-speed Character-Vector Generator hardware are also available.

**Cost-Effective Graphics for the OEM.**
For applications where minimal cost without sacrifice in performance is a major consideration, Genisco offers the GCT-3400 OEM models.

**FORTRAN Software.**
In addition to the Basic Graphics instructions and diagnostics provided with the system, Genisco offers GRAFPAC II, the most comprehensive FORTRAN Callable Subroutine Package available for raster graphics.

Since space does not allow for greater enumeration of the many ways your computerized displays can be truly picture-perfect, contact Genisco — a name that has stood for technological expertise for over 30 years — 17805 Sky Park Circle Dr., Irvine, CA 92714, (714) 556-4916.

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## It's just one way Genisco makes your pictures perfect.

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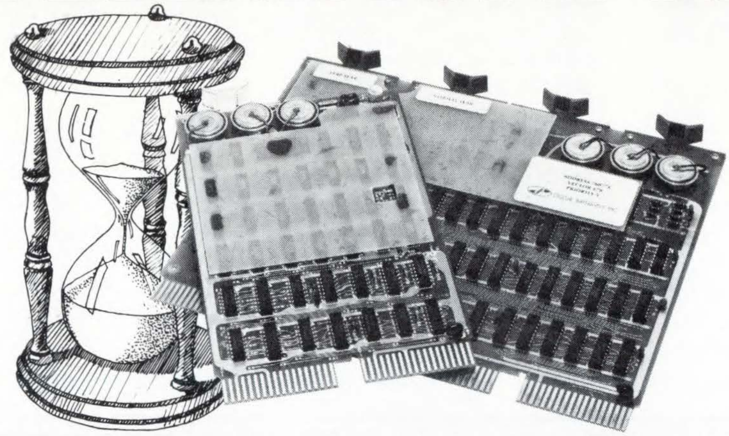
# TIME after TIME



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TCU-100 • $495
- Provides month, day, hour, minute and second.
- Can interrupt on date/time, or periodic intervals.

TCU-150 • $430
- Provides year, month, day, hour, minute and second.
- Automatic leap year.
- Patches for RSX-11M, RT-11 FB/SJ VO2, VO3 and UNIX.

## LSI-11/2*
TCU-50D • $295
- Provides month, day, hour, minute and second.
- Dual size board.
- Patches for RT-11 SJ/FB VO2, VO3B.

## Lockheed SUE
TCU-200 • $550
- Provides year, month, day, hour, minute, second and milli-second.
- Interval interrupts between 1/1024 seconds and 64 seconds.

## Computer Automation (Naked Mini)***
TCU-310 • $385
- Provides year, month, day, hour, minute and second.

## Multi-Bus**
TCU-410 • $325
- Provides year, month, day, hour, minute and second.
- SBC/BLC compatible.

## HP 2100
TCU-2100 • $395
- Correct time restored after power failure.
- Compatible with the HP TBG card.

## Serial Clock (RS 232 or 20 mA)
SLC-1 • $575
- Connects between any terminal and host computer.
- Provides date, time and more!

All Digital Pathways TCUs have on board NICAD batteries to maintain time and date during power down. Timing is provided by a crystal controlled oscillator. Prices are U.S. domestic single piece. Quantity discounts available.

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# DIGITAL PATHWAYS

**Circle 11 on the Reader Inquiry Card**

DC-300A data cartridge, it contains 600' of specially formulate high-density tape. The drive is the same size as a standard floppy disk drive (4.62" X 7" X 19" including formatter controller module; drive only is 9.5" deep).

Higher capacity is also a result of recording information in contiguous pre-recorded data blocks defined by forward/reverse reading block keys, thus eliminating need for "inter-record gaps." Asynchronous 16-bit words are recorded and read in 1,024-byte blocks. The use of pre-recorded block keys permits unlimited, precise recordings. The system's error-detecion and recovery capabilities can accommodate substantial signal loss or tape dropouts.

The 4 Megabyte/sec transfer rate is the maximum achieved in the "burst" mode, unloading into an integrated buffer storage system. In the "streaming" mode, with continuously running tape, an average rate of 20 kp/s.

In addition to the standard high-speed I/O channel interface, the HCD-75 system allows DMA, routing data directly to computer memory without tying up computer control circuitry.

One μP-controlled module can direct one to four cartridge transports, if such a system configuration is desired. The system's mechanical and electronic design promotes complete interchangeability and transportability of data cartridges.

The HCD-75 High Capacity Cartridges will be available the 2nd quarter. Unit prices, $2,150; unit prices for additional drives, $1,050. Cartridge, $30.

**3M**, Dept. MN9-31, Box 33600, St. Paul, MN 55133.

# Tape Streaming: Backup For 8-Inch Winchesters

**Paul Snigier,** *Editor*

The 8″ Winchester "Microdisks" (first reported in *Digital Design*), are already promising to become the most significant peripheral product development to come on the design scene since the flexible disk drive first made its debut.

Unfortunately, the 8" Winchester disk isn't exactly a low-cost removable media in the sense that floppies are. Unlike flexible disks, the 8" Winchester suffers from mass storage backup – a potentially serious threat to its rapid acceptance. Unlike removable disks, where system users employ dual drives to duplicate programs/data for storage (or editing) purposes, 8" hard disk drives will need a different approach to removable media.

Tape streaming drive is a promising new peripheral product that already promises to boost the already-rapid initial acceptance of 8" hard disk drives. Manufacturers in increasing numbers are introducing backup units. Examples include IBM's 8809 streaming tape drive that copies/dumps data from IBM's fixed 62PC "piccolo" disk drive. Cipher Data Products' under-$1800, low-profile streaming tape drive (STD), whose 1/2" tape rate is 100 ips (12.5 ips in stop/start mode), can take data on the fly (up to a full 8" Winchester disk). CDP's STD writes in industry-standard inter-record gaps. It holds 30 MB/10.5" reel. Another more recent entry is Data Electronic's 30.2-MB, 576-kb/s "Streamer" and 34-MB, 648-kb/s "Streaker". Both use standard ANSI/ECMA 1/4" cartridges.

Tape streaming advantages include: (1) high capacity (30 MB or more/reel), (2) high copying/dumping speed (100 ips or so); 12 ips stop/start mode, (3) dumping many disk files is done in continuous motion, (4) no vaccum columns, (5) no tape-buffering tension arms, (6) access times 4X that of floppies, (7) low $1.3K-$2.1k prices, (8) compact, smaller size, (less than skin and framing), (9) lower power consumption, (10) accurate speed and consistent data-transfer rate (compact 1" brushless dc motors are often used).

With new manufacturers rapidly entering, or about to enter the streaming tape drive market, and with increased tape speed/densities, system designers should begin evaluating the new 8" Winchester drives and tape streaming backup units. It is not a question of the 8" hard disk drive winning slow acceptance as the flexible disk drive did: the strong need and demand for 8" hard disk drives already exists; and, unlike the floppy, the drives and their backup systems will gain rapid acceptance.

# First Single-Chip Real-Time Signal Processor

The first single-chip, real-time analog I/O μC, the 2920 Signal Processor and SP20 hardware and software support package, converts analog input signals to digital information, processes this information in its high-speed computer, and produces analog outputs in a real-time mode.

The SP20 support package includes a 2920 software simulator assembler and 2920 EPROM programming personality board. Both 2920 assembler and software simulator run on the Intellec μC development system; the programming personality card provides the capability to program the 2920 EPROM on the Intellec Universal PROM Programmer.

Bringing μC benefits and programming to analog designers, the device and software provide a total system solution to real-time signal processing problems and enable literally thousands of different complex analog systems to be formulated from one standard IC.

### EPROM stores programs

As in μCs, product operation is controlled by programs stored in on-chip memory – in this case, an EPROM. The 2920 interfaces directly with analog signals using the on-chip circuitry and can handle multiple sig-

nals using I/O multiplexers. The device can implement functions such as filters, limiters, oscillators, demodulators, nonlinear conversions, and perform logical operations all under program control.

The powerful instruction set and chip architecture plus EPROM program storage can implement complex circuits such as MODEMS and scanning spectrum analyzers on a single chip. Building block functions can be combined to realize DTMF receivers, PLLs, complex filters, linearizers, waveform generators, guidance and control modules, test and instrumentation circuits, speech processing, seismic processing, medical electronics and applications which process DC-10 KHz signals.

### Offers precise operation

The 2920 avoids several common analog system problems: component matching is eliminated because performance from device to device is identical (digital processing is stable, predictable and repeatable), costly components, like precision resistors and capacitors, are not needed; circuit performance does not vary from one production lot to another; performance degradation over time due to circuit interaction or noise is virtually eliminated.

The 2920 enables designers to look at practical functions in a new way; for example, they can design a filter with three poles at the same frequency and expect the poles to exactly coincide in a production version. Discrete component tolerances normally prohibit this operation in conventional analog circuits.

The system designer can employ the 2920 as an economical alternative to developing a custom analog IC without risks and commitments associated with special-purpose components. The 2920 gives the user flexibility for making modifications, design improvements and adding extra features by simply changing the 2920 program.

Maximum program capacity is 192 instructions. Each instruction controls the processor and I/O sections separately so that digital and analog operations can usually proceed concurrently. The computer sequences through each step at a constant rate without any jumps except at program end. This sequence establishes a constant time between samples, and by program shortening, it increases sample rate and maximum bandwidth.

The 2920 costs $250 (100 qty); the SP20 support package, $3400.

Intel Corp, 3065 Bowers Ave., Santa Clara, CA 95051.

The designer can quickly transfer 2920 programs to the 2920 device via the Intellec μC development system and its Universal PROM Programmer by using the SP20 EPROM programming personality board and adapter socket.

# Chip Pair Transforms TVs Into Universal Terminals

A unique chip set from National Semiconductor Corp. transforms standard TV receivers into "universal" terminals for receiving signals other than those from commercial TV broadcast transmitters. The 20-pin LM1886 ($3.50) and 18-pin LM1889 ($.70), which permit a standard TV set to perform functions of sophisticated terminals, promise to fill a pivotal role in transforming TV into multipurpose home entertainment and information systems.

More firms are looking at the commercial TV set as a potential low-cost data display terminal that is already in the home for home computers, VTRs, video disc playback systems, etc. To date, however, providing this interface was difficult and time consuming, requiring construction of discrete multicomponent circuits. Now, designers using the LM1886/1889 need only two chips.

The LM1889 contains a sound-terminal oscillator, chroma subcarrier oscillator, quadrature chroma modulators and RF oscillators for two low VHF channels. LM1889 allows video information from VTRs, games, test equipment or similar sources to be displayed on B/W (and with the LM1886), on color receivers.

LM1886 is a TV video matrix DAC which encodes luminance and color difference signals from 3-bit red, green and blue inputs.

National Semiconductor, 2900 Semiconductor Ave., Santa Clara, CA 95051.

# AED ANNOUNCES ITS NEW DEC TEAM.

## Single card RM-02® emulation

The fullback for the PDP-11 team is AED's new STORM-02, a hex-card controller/formatter for storage module drives.

We tried out a lot of fullbacks for the team but STORM-02 was the only player that could offer everything! Single hex-card electronics; RH-11, RM-02 and RM-03 emulation; the ability to plug right into the SPC slot on your PDP-11; plus the ability to get along with the media. That's the kind of compatibility we like!

A standard single board STORM-02 handles 4 SMDs. With an optional second hex-card, the STORM-02 can accommodate four more drives for a total capacity of over 500 megabytes.

Our big surprise was the bottom line on the contract. The OEM price for the STORM-02 is just $2370 for the hex-card electronics — far less than any fullback in the league. The complete system with one 80-megabyte storage module drive, in quantities of one, is $13,500 . . . about half the price of a comparable DEC fullback.

For the complete statistics and quick delivery, call or write Bob Deisher, Rigid Disk Products Manager.

ADVANCED ELECTRONICS DESIGN, INC.

COMPUTER PERIPHERALS DIVISION
440 Potrero Ave., Sunnyvale, CA 94086
Phone 408-733-3555, Boston 617-275-6400

## RL-01® compatible Winchester

The linebacker for our LSI-11 team, the WINC-01, is surprisingly small for a pro. He consists of just two PCBs — one a microprocessor-based formatter/controller mounted with a SA-4008 drive, and the second, a dual-width Q-BUS interface card that inserts directly into the CPU backplane.

However, when WINC-01 proved he could deliver Winchester technology to DEC LSI-11, -11/2, -11/23 users, we signed him up immediately. He amazed us by playing with up to three SA-4008 Winchester drives and tackling up to a total of 60 megabytes of data. Additionally, he has the capacity to include a plug-in floppy disk drive.

Best of all, he bunked with the DEC RL-01 driver software and we can report they are very compatible up to 20 megabytes.

In contract talks, the WINC-01 demanded considerably less than the DEC hardware: his two boards sell together for under $1150 in OEM quantities. The complete system, including the two PCBs, an AED power supply, one SA-4008 drive and a DEC look-alike cabinet sell for $6700 in quantities of one.

For WINC-01 technical information and quick delivery, contact Bob Deisher, Rigid Disk Products Manager.

## Full color graphics system

The coach of PDP-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in high-resolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

Other features that make the new PDP-11 'coach' a cost/performance leader include:

- DMA interfaces (Q-BUS® or UNIBUS®) available.
- 2:1, 3:1 . . . 16:1 zooming. Panning via integral joystick.
- Vector and circle generation. Curve fill. Single-point addressability.
- Crosshair cursor with programmable color.
- SUPEROAM panning over 1024 x 2048 contiguous pixels.
- Programmable character fonts and 8 programmable special function keys.
- $6,875 with two colors only, excluding monitor and DMA.

For delivery information, write or talk to Jerry Kennedy, VP Marketing.

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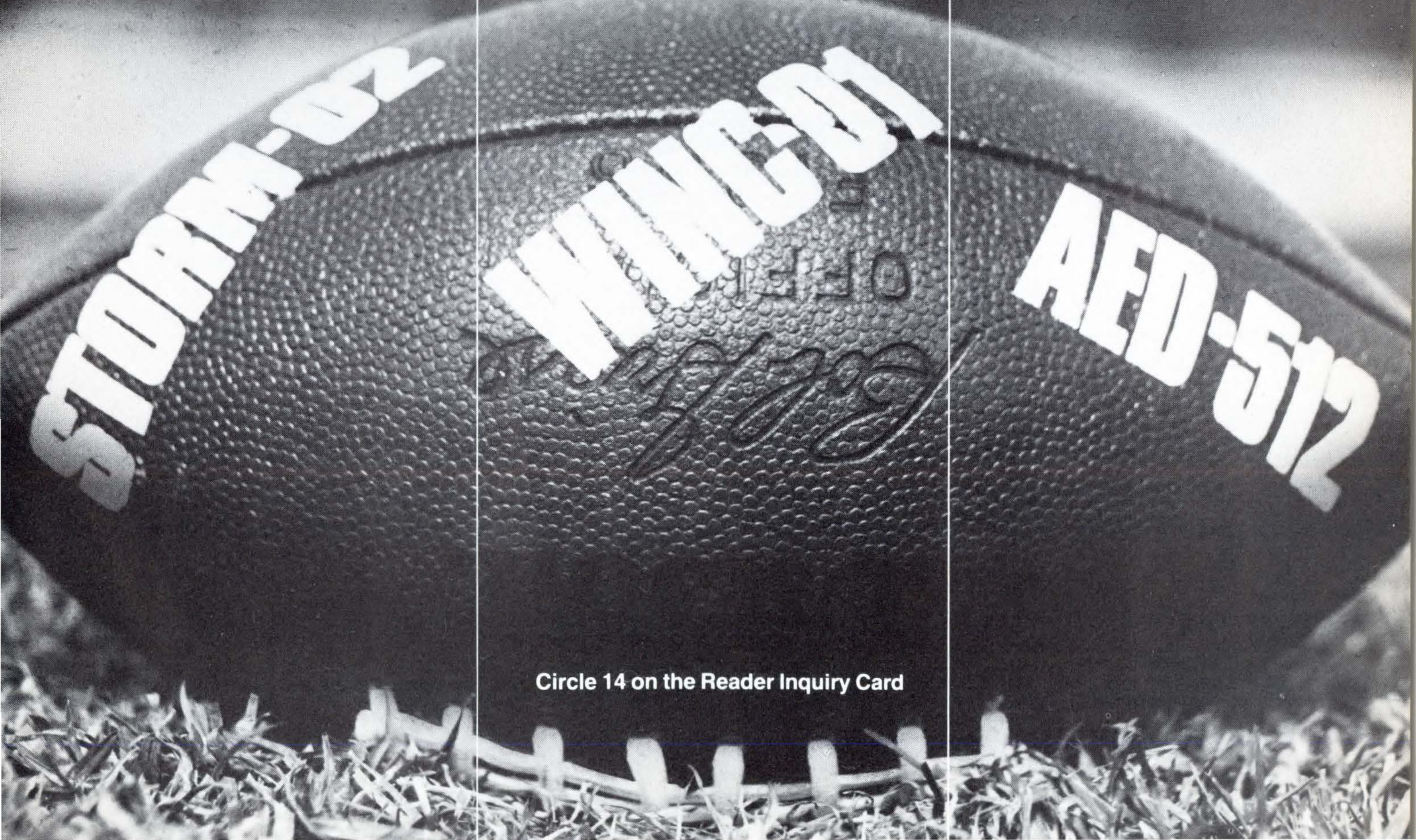


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# Software
## DESIGN SERIES

Dr. Lance Leventhal
*Emulative Systems Co.*

# Design and Development of μC Software

More and more engineering time is going into the development of μC software. Engineers are learning that software can lower count, increase reliability and decrease system cost. As memory costs have decreased and chip sizes have grown larger, the incremental hardware cost (extra memory) of additional software has steadily decreased. But, as might be expected, numerous problems remain to be solved, especially software management, software reliability and training of personnel.

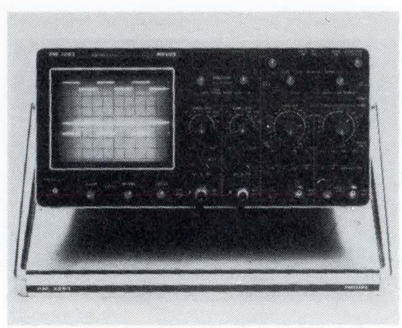
**Software Management**. Engineering departments are now experiencing the same trials and tribulations in software project management that data processing departments have been complaining about for years. They include large cost and time overruns, inadequate estimating, planning and quality control, plus the lack of standards – the common features of software projects.

**Software Reliability**. Of course, software should be more reliable than hardware, since it doesn't wear or suffer from the numerous physical ailments that bedevil hardware. But is this really the case? We know surprisingly little about the reliability of computer software.

**Training of Personnel.** Obviously, the need for μC programmers far exceeds the current supply. Should you train hardware designers to write software or programmers to do this job? If you plan to develop μP-based products or intelligent terminals, what kind of people do you need? What do they have to know? Can hardware designers write software effectively? What skills are really necessary? What problems should you expect to overcome?

### A dichotomy – design and development

Software writing consists of two different stages: designing or defining and outlining the program, and developing or the coding, debugging and testing the program. Design requires an intimate understanding of the application. The designer must know what tasks the product will perform, how it is to be tested, used and maintained, how it is related to other products, and how it should receive its inputs and produce its outputs. These same issues occur in hardware design when microprocessors are not involved. The only change is in the method of implementation.



Design of μP-based instrumentation, such as this Philips PM3263 scope, requires that hardware/software job functions be carefully defined to prevent designers from re-inventing the pyramid – a costly and too-common occurence.

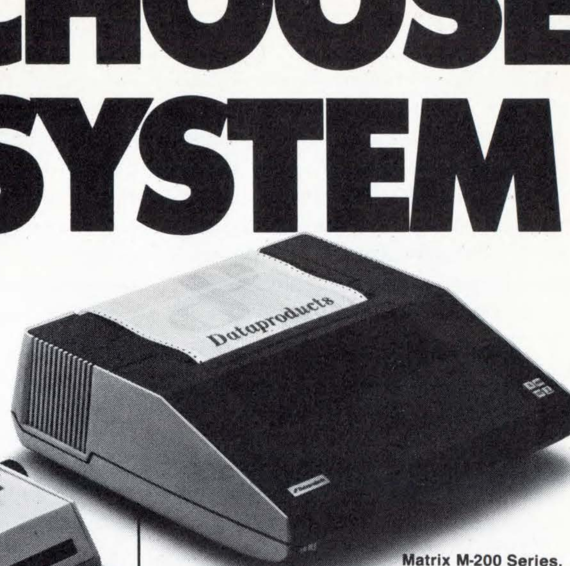
The designer must now learn how to implement functions in software and make tradeoffs dependent on the new economics of μPs. Obviously, it is very difficult to train a programmer to perform this kind of design, since the job really belongs to an engineer. Also, an EE can learn μC programming far faster than a programmer can try to learn μC hardware design. The new implementation technique does not change basic design principles and methods; it merely involves the introduction of new technologies and levels of integration. Obviously, changes have occurred. μCs have affected hardware design, just as ICs and transistors did years ago. But the changes are evolutionary and hardly call for giving the design task to programmers or others.

Development, on the other hand, is quite a different business. The development of μC software is similar to the development of software for large computers. Are many of the differences minor or temporary in nature? Comparing minis and the newer micros is like comparing subcompact and compact cars. Designers must use programming tools, such as: keyboard/display systems (like the Motorola EXORterm 220), disk or other mass storage systems and software-like operating systems, editors, assemblers, compilers, debuggers, loaders, linkers and utilities.

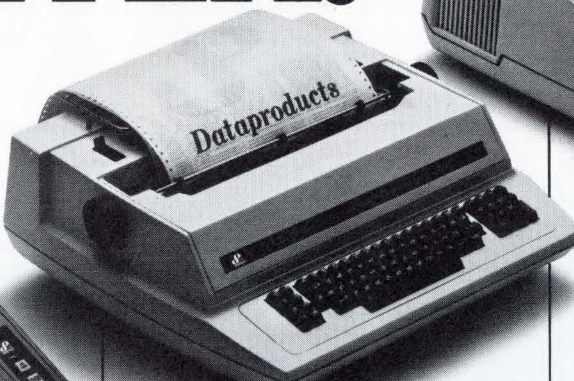
Hardware designers suffer from a disadvantage when developing software. Development work, particularly for number-crunching or dp applications, often has little connection with underlying hardware. Old-school hardware designers – who are more familiar with soldering than programming and more at home with a scope than with an interactive debugger – often find software development slow, awkward and cumbersome.

Furthermore, a good set of development tools is difficult to evaluate and select. Would you trust a programmer to purchase an oscilloscope, signal generator or spectrum analyzer? Then why should you choose (and even write) operating systems, editors, assemblers,

# HOW TO CHOOSE A SMALL SYSTEM PRINTER.




Matrix M-200 Series.

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compilers, debuggers and other software without a programmer's recommendations? A development system is a computer, even if an instrument maker or semiconductor company manufactures it; the quality of its software and peripherals is the key to making it really useful. Designers or manufacturers of development systems don't understand this key fact.

### The hardware designer's role

What role does the hardware designer play? Certainly, he solves enough problems in hardware and software, but is unfortunately also expected to become fully aware of modern software tools and methods – an undesirable and added burden.

New problems in designing μCs involve implementing system functions in software or in a mixture of hardware and software. Some of the required functions include: arithmetic and logical functions, simple input and output, decoding and encoding, timing, counting, data collection, array processing, status and control, and serial communications. All of these functions are common to systems with or without μPs.

An obvious temptation for the hardware designer is to try function-by-function replacement. That is, the designer may try to formulate the problem in the way required for hardware implementation and then replace components with programs. This technique makes the formulation simpler for the designer, but ignores the fact that the basic components in programs may differ very markedly from hardware devices. Other formulations, derived from software methodology, are frequently far more efficient and sensible.

This temptation exposes typical weaknesses in most hardware designers' experience when confronted with a transition to the software. The designer tries to stay as close as possible to previous experience. He must overcome a tremendous desire to work at a very low level, at which the exact effects of instructions can be seen and understood, even if the development of software becomes very inefficient. μC system designers too often act like the original computer programmers by choosing (or even designing) tools that are as familiar as possible. Many rediscover known principles and relearn the lessons that those who have worked with larger computers have learned over the last 25 years. In particular, many hardware designers tend to forget the need for adequate documentation and maintenance. Software is such a fascinating new toy that time spent writing it almost seems not to count in project budgets! So, lack of software expertise frequently results in large amounts of time spent debugging low-level programs and final products that are virtually impossible to maintain or extend.


**Many programmers can evaluate software development tools, such as this Motorola M68SX220 EXORterm 220, with better insights than many hardware specialists. Let each specialist do his own job – not others'.**

But the hardware designer's education and experience provide great strengths. First, he understands system operation in a way that cannot easily be taught to programmers. The designer comprehends electrical and mechanical realities in terms of timing, directionality, response times and physical limitations of which programmers are totally unaware. Certain hardware functions are readily available, while others of equivalent complexity are far more expensive. The hardware designer also understands previous hard-wired designs, so that new products can maintain compatibility with previous products and with user expectations.

However, one area in which neither hardware nor software designers are often entirely comfortable is use of programmable interfaces and controllers. Hardware designers are usually familiar with the tasks that these devices perform and with their electrical idiosyncrasies. On the other hand, some hardware designers find the programming of these devices a bit mysterious. Software designers are used to dealing with "black box" interfaces (common in the minicomputer world), but are seldom accustomed to gate-level tasks that chips perform or with timing and interfacing problems that they present.

### The software designer's role

Once you have formulated the problem and specified program requirements, development is a completely different business. Here, the key is the effective specification and use of software development tools. The key software consists of tools familiar to the large computer world – compilers, debuggers and other packages. Developing software

A lot of complex thinking goes into the Teletype* model 40 printer. And, incredibly, it all fits on this 9″ by 19″ circuit card.

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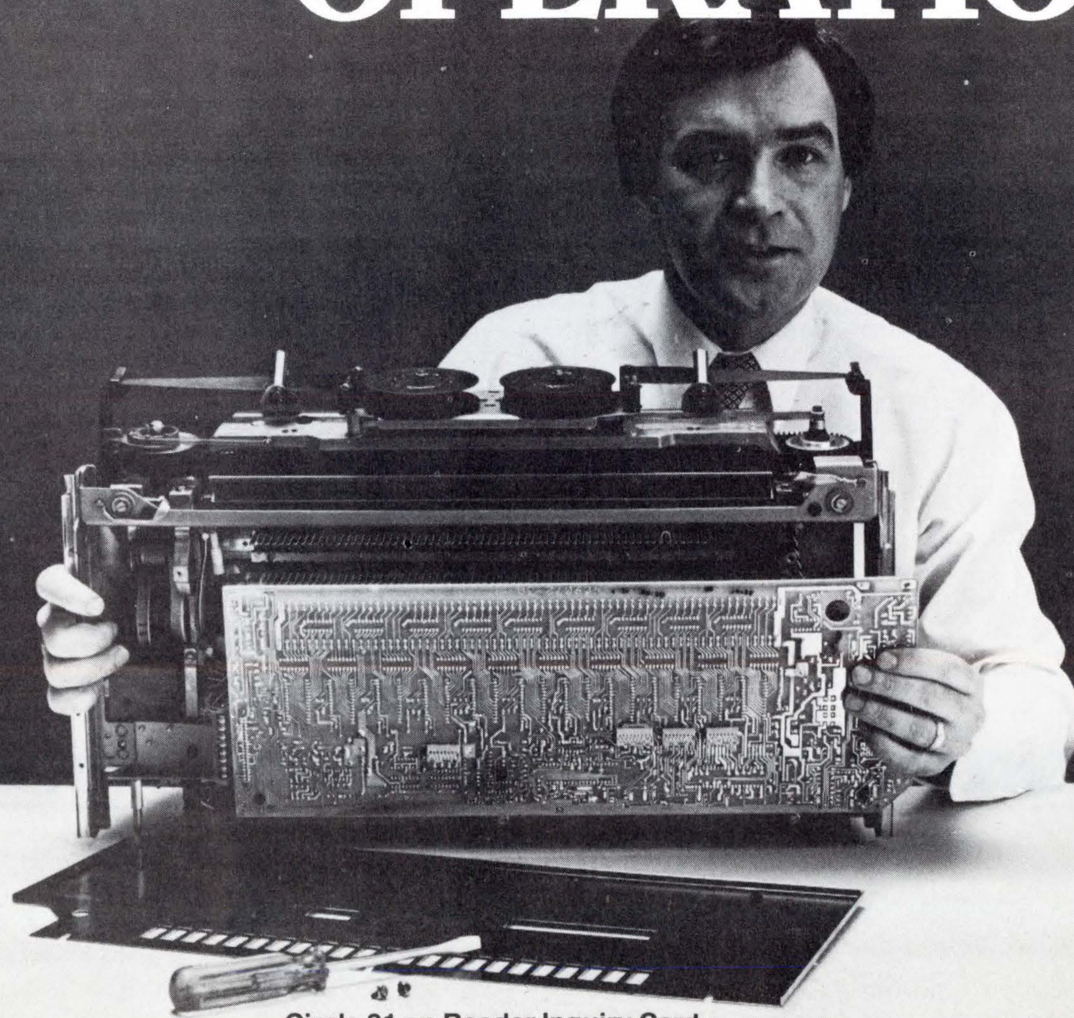
# MEET THE BRAINS BEHIND THE OPERATION.



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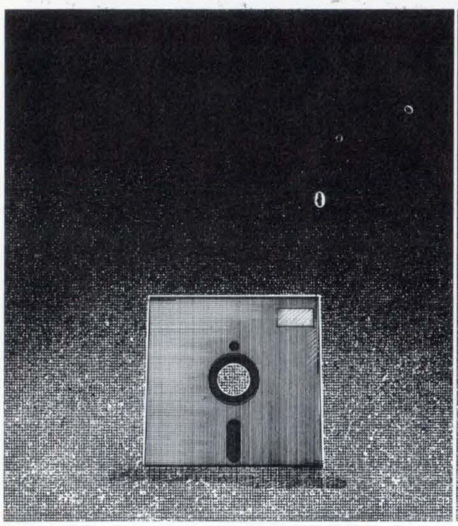
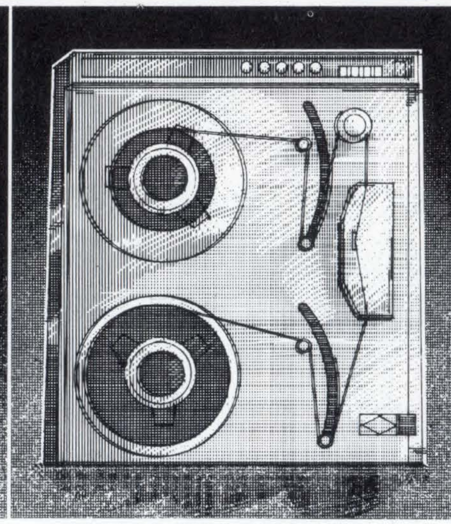
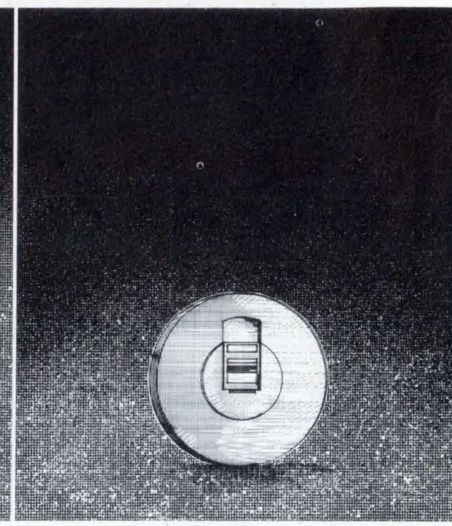
# THERE ARE A LOT OF ALTERNATIVES TO THE DISK BACK-UP PROBLEM.



**FLOPPY DISKS**
Storage capacity: limited.
Handling problems.
Low cost.



**REEL-TO-REEL TAPE DRIVES**
Low performance: 36 megabyte capacity.
High performance: 90-100 megabyte capacity.
Large, bulky, high cost drives.
Cost: very expensive, up to 20 times that of floppy disks.



**DISK CARTRIDGES**
Storage capacity: 5-10 megabytes.
Back-up data remains on a disk.
Large drive mechanisms.
Cost: up to $5000.00.

# HERE'S THE SOLUTION.

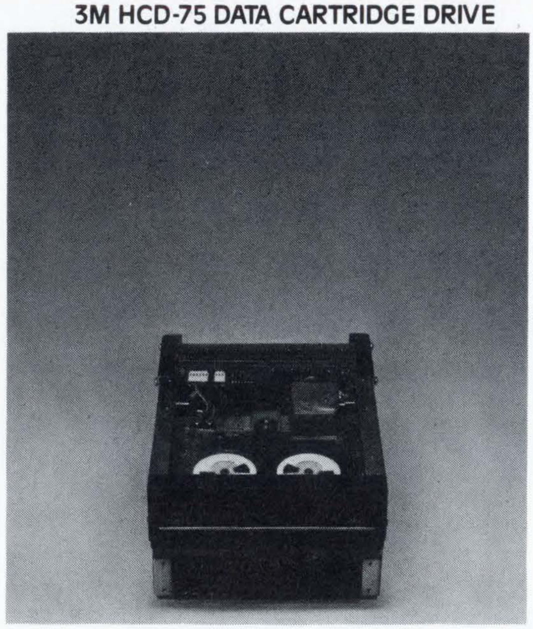
**3M HCD-75 DATA CARTRIDGE DRIVE**

Storage capacity: 75 megabytes formatted (144 Mbytes unformatted).

Drive dimensions: 4.62" x 7" x 8.625".

Preformatted tape, allows unlimited record replacement.

Built-in error detection/correction capabilities.



Fully-buffered I/O channel, permits asynchronous data transfers.

Serpentine recording, eliminates wasted rewind times.

List price, including Controller, $2,150.00.

To learn more, check the listing at the right and contact the Data Products Representative nearest you. Or write: Data Products/3M, Building 223-5E/3M Center, Dept. 125, St. Paul, MN 55101.

## THE DISK BACK-UP SYSTEM THAT'S SUDDENLY WAY OUT FRONT.

3M

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without these tools is like developing hardware without an oscilloscope, logic probe, multimeter and signal generator. Yes, you can do it – but inefficiently. You're unwise not to use tools which are commonly available at reasonable cost.

The strength of software designers is familiarity with software tools. They know by experience what capabilities an operating system should have and what an assembler, editor, compiler and debugger should do. Too few hardware designers are aware of such names as UNIX, TECO, CANDE or Programmer's Workbench, much less know why they are important milestones in software development. These strange new gadgets for the hardware designer are familiar items to those who have worked with minis or large computers. The software designer thinks nothing of moving from editor to compiler to linker to debugger and back again, while the hardware designer may find the mere typing of a program slow and onerous.

## Some disadvantages

There are disadvantages: the software designer doesn't usually know if the program makes any physical sense. Has the data at a particular input port actually settled and is it available for reading? Has enough time elapsed for a new command to be sent to a piece of mechanical gear? Does the order in which signals have been transmitted meet the requirements of the receiving piece of equipment? Will transients or electromagnetic interference result from a particular sequence of operations? Seldom does the software designer, who is usually woefully ignorant of the underlying hardware, possess any insight. Too often, the software designer is trying to learn the lessons of a basic circuits course.

## Some solutions

Obviously, there is no way to make μC software designers into μC hardware experts or vice versa. Each expert has enough work to do in his own area. Therefore, software people must select the software tools found useful in software development; they must specify operating systems, compilers and advanced software development methods.

Several years ago some firms tried to re-tread programmers (accustomed to big machines) for micros, and this led to some disastrous results. Was it easier to retrain an EE to be a μC programmer than vice versa? Perhaps this was true several years ago, but times have changed, the applications have changed, and many micros are more closely resembling minis. Programs are now longer, and software development more sophisticated.

Today, hardware designers must approach the advanced software development tools (not available just a few years ago) as users. They might as well start with a good foundation. We suggest that they use PASCAL as the fundamental language (not BASIC or assembly) and stick to standard systems as much as possible.

One important trend, the use of software tools to check system descriptions, was discussed in the August issue. Programs can check for hardware errors, much as design automation programs now check for incomplete circuits or physically unrealizable mechanisms. Integrated design and development packages can do much of the rote work now performed by both hardware and software designers. Such automation will remain essential due to a lack of qualified personnel.

## Conclusion

Hardware and software designers should follow more separate roles in μC software design and development. In the design stage, hardware specialists can provide physical insight and experience gained from similar hard-wired systems; in the development stage, software specialists can provide experience with software tools that are widely used with larger computers. Why misapply the experience of both in repeating old mistakes and costly lessons? It makes no sense.

**Rate this article: circle 1L, 1M or 1H on Reader Inquiry Card.**

# Evolution of Video Terminals

**Mary Cole**
*Digital Equipment Corp.*
*Maynard, MA*

Modular design of CRT terminals permits the addition of functionality and use in situations requiring greater computer power. Pursuing a modular video terminal plan goes against the industry tradition of designing monolithic terminals where the whole terminal is optimized for low cost at the expense of easy evolution.

In modular computer systems, the CPU evolves at a different rate than mass storage devices and other distinct subsystems. With a modular system architecture, the development of a new, faster and compatible central processor would permit a system upgrade requiring a minimum of reconfiguration — frequently a reconfiguration at the plug and cable level. Within a central processor "box," modular design approaches can permit upgrading via plug-in board, either as an addition or an exchange. For example, the exchange of CPU boards can convert a PDP-11/04 system to a PDP-11/34 system, while the addition of floating point or memory management functionality can be done by inserting a board into an existing PDP-11 system. The VT100 terminal was designed in the tradition of modular computer systems.

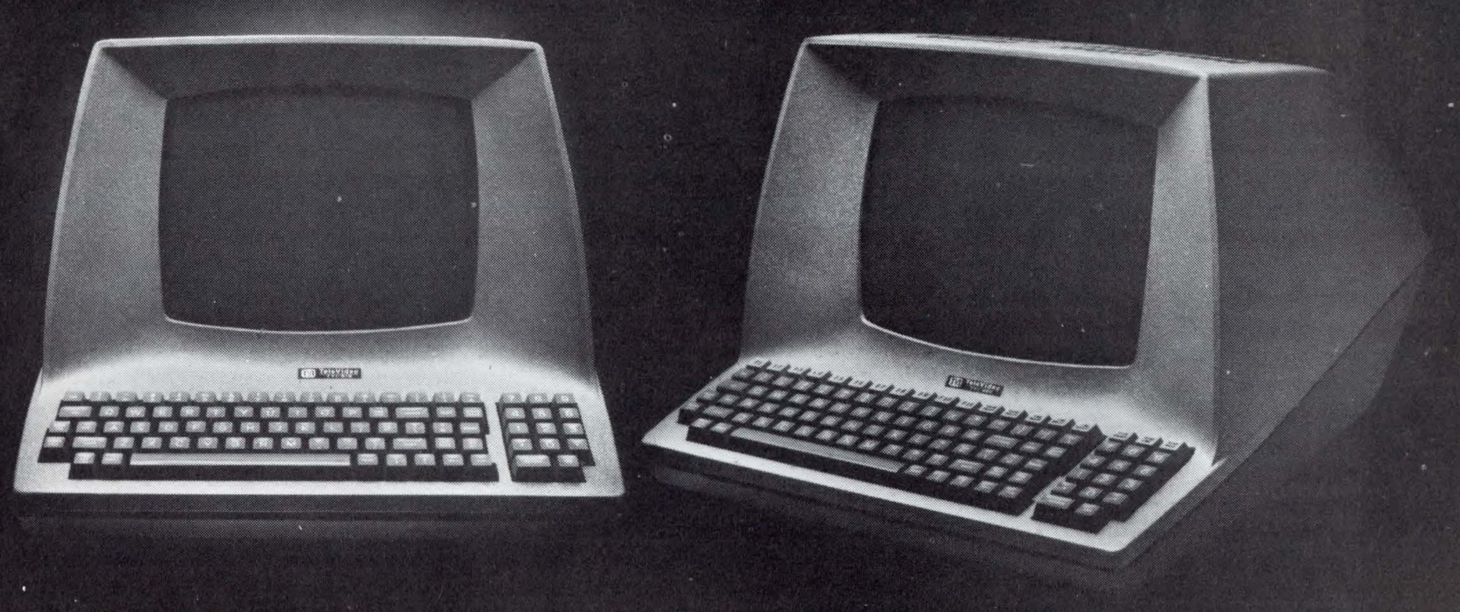
Earlier video terminals were, for the most part, "dumb" terminals with a tendency to become more sophisticated in slow, evolutionary ways. Earliest terminals had upper case letters, conventional packaging and cooling and were physically large for the screen size. Terminals which followed had further features: convection rather than forced air cooling, upper and lower case characters, sufficient local storage within the terminal to permit an additional screenful of data to be stored and recalled without processor intervention, and conveniences such as an optional key click for audible verification of keystrokes. One especially important design feature was that sufficient room was provided in the packaging so that other components could be added, either electronic or electromechanical. The extra room allowed the VT5x series to later incorporate an optional hard copy device and to be used as the basis for the VT78 Video Data Processor with the addition of a $\mu$C board. Both the VT05 and the VT5x series, however, had all elements contained in a single housing. While this did not restrict the electronic aspects of the architecture greatly, it did imply that a major change or upgrade would likely require both electronic and mechanical redesign of the whole package.

Developments of the past couple of years have permitted greater functionality to be packaged electronically into terminals without substantially increasing cost. As an example, the price of semiconductor memory has decreased significantly — and memory density has increased — permitting a larger buffer space to be incorporated into terminal design.

The VT100 package is divided into


A detachable keyboard increases flexibility of positioning.

# TeleVideo delivers...



# Smart Terminals for the price of dumb.

The TVI-912 and TVI-920 are the results of one and a half years of development by TeleVideo, Inc., a four year old company whose main business has been the production of CRT video displays. The SMARTS, RELIABILITY, and FLEXIBILITY offered in both our products are available only on terminals costing hundreds of dollars more.

We make the choice easy. There are only two extra cost options. Thousands of units have been installed and a nationwide Distributor Network has been set up to serve you. Therefore, why pay more for equal or less capability? Call us now for the Distributor nearest you.

**TeleVideo®, Inc.**
3190 Coronado Drive, Santa Clara, CA 95051
(408) 246-5428 TWX 910 338-7633 "TVI VIDEO"

**Standard Smart Features:**

- Upper/lower case
- 14 Key Numeric Pad
- Cursor Addressing/Controls
- Editing
- Reverse Video
- Underline
- Reduced Intensity
- Blinking/Blanking
- Protected Fields
- Tabbing
- Self-Test Mode
- Much More

**Options:**

- Serial Buffered Printer Port
- 2nd Page Display Memory

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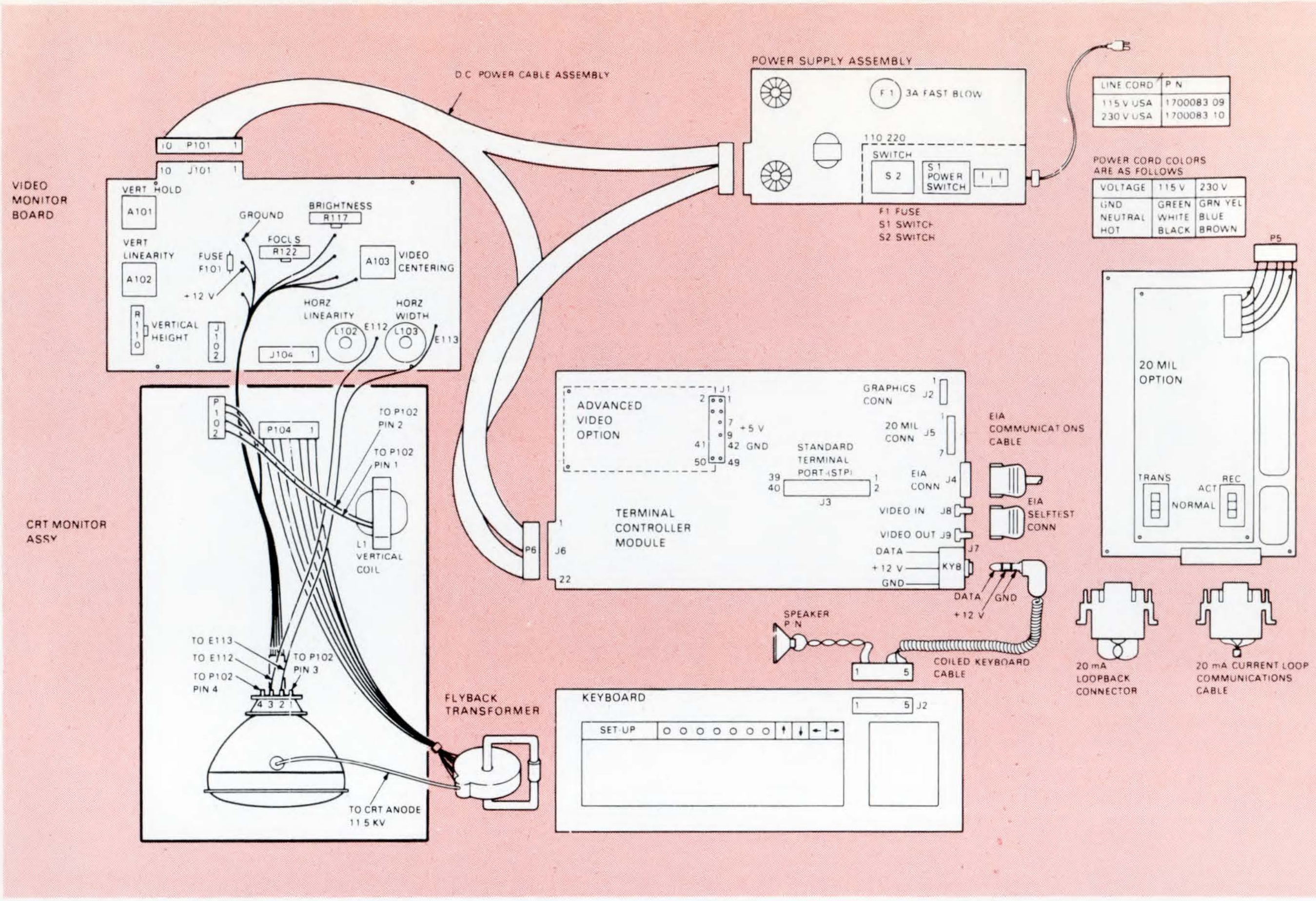


**A modular VDT layout, as shown here, makes repair easier.**

two distinct parts: the main chassis, where the logic and CRT screen are located, and the keyboard assembly, which is connected to the chassis by a coiled cable. This permits flexibility in terminal placement and usage. The keyboard no longer has to have a fixed relationship to the screen (in fact it need not be there at all). The two-part design approach permits alterations to the keyboard assembly without affecting the design and manufacturing process of the chassis. Alterations which could be easily considered include a different keycap set for other languages or special functions, a new keyboard layout to accommodate special function keys, additional intelligence and capability could be built into the keyboard itself to make it usable with a TV monitor or permit some sort of special processing of typed input, different audible devices could be installed in the keyboard assembly to supplement the one device currently there, LED lights on the keyboard can be programmed to provide feedback to the operator, additional LEDs could be installed on the keyboard assembly, in fact the keycaps themselves could conceivably be lighted or unlighted to provide some type of feedback, and cheaper types of keyboard assemblies could be used as the technology evolves. These are only some of the possibilities.

The keyboard is connected to the main chassis through a plug-in cable. This permits easy transportation and easy replacement for maintenance and repair. Such an arrangement can minimize total terminal downtime for an installation. From a standpoint of electromechanical design, it is worth noting that the keyboard keys represent the only moving parts of the terminal. Typical functions, such as brightness, which are handled by electromechanical knobs in conventional terminals are controlled electronically from the VT100 keyboard.

Within the main chassis, the controller logic is located on a module alongside the CRT such that each can be considered a separate subassembly. Improvements in either area could be made with minimal impact on the other. Thus, for example, it would be possible to introduce a color CRT capability or a different screen aspect ratio with little effect on the control logic. Such a design segmentation also makes service and maintenance easier and more systematic for support personnel.

The basic VT100 operations are controlled by a $\mu$P and associated circuitry. A number of functions are keyboard-selectable (such as column width, character height, cursor attribute) with default values if none are specified. In total there are 22 features that are keyboard-selectable in the set up mode. These include choice of transmit and receive speeds, standard or reverse video screen. A series of less commonly used features can also be altered by the user, but requires enough interaction at the keyboard to insure that the casual "button pusher" will not inadvertently change the terminal characteristics.

The VT100 represents a design approach that has not been exploited before by CRT engineers. The basic terminal design is structured so that improvements can be made on a modular basis, permitting improvements in one area without being bound by the technology of another area. The packaging, CRT, power supply, control logic, and keyboard are designed for independent evolution and the first wave of that evolution can be seen in the VT105, VT110 and PDT's.

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# Intelligent Terminals: What The Systems Designer Should Look For

**Darrell Crow**
*Zentec Corp.,*
*Santa Clara, CA*

When should you implement an intelligent terminal system? The answer to this question is readily apparent to any potential buyer who currently has a sufficient number of smart or dumb terminals tying up his CPU. But essentially an intelligent terminal is of benefit in two situations. First, where an operation is desired in a stand-alone environment for output to the floppy disk, larger data base or other peripheral or printer. Second, an intelligent terminal is of tremendous advantage in situations where the user desires to bring more pre-processing down to each individual terminal. This allows each operator to perform a number of functions and transmit to the CPU only when absolutely necessary, reducing both lease-line costs and host computer time.

The selection of an intelligent terminal requires smart buying. You should thoroughly investigate requirements, survey vendor capabilities, discuss alternative problem solving and review the manufacturer's operations facilities. Above all, be sure that the vendor will respond to your needs, problems and small emergencies that occasionally arise. And, be sure of the intelligent terminal's technology – and of the vendor's response technology.

## Opening new applications

Dumb terminals offer few if any operational functions and even fewer options for interfacing with peripheral devices. Unlike its dumb counterpart, a smart terminal does offer significant operational functions, but the user has limited control over the hardware. Smart terminals have the capability to edit and store data as well as the ability to perform unattended operations. These can include management of peripherals such as tape cartridges, floppy disks or printers. A major disadvantage with the smart terminal is simply that its intelligence is limited and it must eventually rely on the "brain power" of the host CPU for sophisticated operations. As a consequence, only a limited number of smart terminals may access the CPU at one time, severely restricting simultaneous terminal activity within a production environment.

The intelligent terminal, however, has the advantage of superior intelligence, allowing extended editing and forms handling capabilities at various workstations, further freeing the CPU for additional duties. Intelligent terminals not only boast extended editing capabilities and possibilities for interfacing, but can also be programmed by the user. Consequently, the user, at will, can determine the terminal's functions based on his particular requirements and whenever the need arises, change the programs (terminal functions) to meet the new requirements.

The intelligent terminal, by virtue of its superior versatility and extended capabilities is one of the driving forces in the growth of distributed data processing. The past six years have seen tremendous inroads into distributed dp systems by intelligent terminals. They support high systems performance, fast response and high throughput in a variety of operations. With their implementation, data is highly available, highly reliable and (due to high interfacing and communications capabilities) entire network costs are greatly reduced. Because intelligent terminal system architectures can be quite modular, they provide for sufficient growth and unlimited terminal configuration. As well, their high degree of adaptability for nearly any type of change or workload results in an expansion of both capacity and function.

## ITs aid host computers

The heart of any intelligent terminal, (IT), its μP, allows the terminal two basic operations previously impossible at the terminal level: the ability to make decisions based upon specific guidelines and perform calculations.

The μP allows the intelligent terminal to achieve a combination of rapid response and simplicity in design that was heretofore impossible. The unit's modularity allows it to meet a variety of user requirements, including control of other terminals and buffering capability for communications interface with the host computer. In other words, more and more of the communications functions can be performed inside the terminal rather than by the CPU. μPs are now being used in all functional areas of intelligent terminal design, including print mechanisms, carriage control, interface control and maintenance testing. The more intelligence placed in the terminal, the less required of the host computer.

Aside from the μC, the intelligent terminal architecture consists of a number of subsystems. These would typically include a CRT video display, a keyboard, power supply, memory, a telecommunications interface and mechanisms for future expansion. In each of our terminals, the architecture is organized around a general purpose μC bus onto which the major subsystems consist of a 15″ diagonal video display, keyboard, power supply, memory, an RS-232C asynchronous/synchronous interface and, of course, the μP itself. All our intelligent terminals typically contain two PC boards. The μC PCB itself consists of an Intel 8080A-1, a programmable interval timer, capacity for up to 12,000 bytes of Read Only Memory (ROM or PROM), as well as all necessary μP support electronics. The video interface PCB provides 32,000 bytes of RAM (R/W) memory as well as a great deal of flexibility between how data is stored in RAM and how data is displayed on the screen.

Intelligent terminal housings typically are structured similar to a standard typewriter, with the keyboard below

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and the CRT display unit mounted above. Most display screens are composed of a white phosphor on a dark black background. Many manufacturers, however, utilize or offer an option of green phosphor on a dark black background. Green is typically used by IBM Systems and has been prevalent in word processing environments although, as a rule, white is very easy on the eyes. It should be noted that if your application requires some very fine character definitions, the hardware circuitry may be forced to utilize a technique of displaying characters that would require a CRT phosphor with long retentivity.

### Video display methods

As we said earlier, a number of video display methods exist defining how data is stored in RAM and displayed on the screen. Two of the most popular techniques are the Fixed Memory and the Video List methods. Simply speaking, in the Fixed Memory Video technique every location on the CRT screen has a corresponding RAM memory location. Thus, in order to display any characters on the screen, that data must be moved to a specific RAM location.

The Video List technique is quite different; it allows data to reside anywhere in RAM regardless of the screen display position. Simply speaking, the list driven technique allows the user to have the lines of display data defined by a 4-byte entry in the Video List. This 4-byte entry provides useful information concerning the number of characters in a line, double width/single width characters, address of characters to be displayed and so on. Advantages of the Video List technique include smaller memory requirements, faster movement of display data, split screen displays and horizontal scrolling, to name just a few.

Another feature to consider is the available video attributes the user has access to. Typically, characters can be enhanced on the screen, in a variety of ways to suit the video requirements of various applications. These enhancements, or attributes as they are commonly called, can include half-intensity, blink, blank, reverse video, half brightness, underscore, double-width characters and meaningful combinations thereof. All vendors are not alike, meaning user accessibility can be limited or the video attribute codes may take up valuable space on the screen. Again, review the vendor's capability against your requirement.

### Programmability measures intelligence

Programmability is the key to the depth of a terminal's intelligence. Thus in an intelligent terminal, the microcomputer controls a variety of functions to assist in text editing and word processing applications. For example the keyboard is constructed such that whenever a key is depressed a ROM will output an 8-bit key code to the microcomputer as well as an interrupt signal and possibly a character repeat signal. To change the key code or repeatability of a key one simply reprograms the keyboard ROM. Once the key code has been received into the terminal either a function will be performed or a symbol will be displayed. Any key can be programmed for any function and any key can display any symbol. This is all under user program control.

By changing the keyboard handling routines the user can change the functions of any key or symbol that will be displayed on the screen. This conveniently allows for any arrangement of functions for operator ease. For specific text editing applications such a feature is invaluable. Keys may be coded to perform such functions as block definition, block movement, margin definitions, tabbing, column formatting, character deletes, word deletes, search and replace, temporary data storage, file appendix, document merging, pagination, printing and various methods of hyphenation and justification.

### Character definition

There is a great deal of flexibility offered by the manufacturers of intelligent terminals with regard to character definition. Characters are formed within a dot matrix, typically within a 10-by-10 dot matrix on the screen. The data that forms each of the character dots are stored in some type of memory device, either a ROM or RAM. A ROM memory pattern cannot be changed. Data can be rewritten in a RAM any number of times whenever the user wishes to change the character font pattern. Thus, the RAM character set requires the RAM be loaded upon power-up with data from another source, either from a floppy disk or from a CPU. Effectively, the data has to be stored in the terminal every time the system is powered-up. The beauty of this is that whenever you want to change your character set – say from an English character definition to Hebrew, French, Finnish or even mathematical symbols – then simply by loading this one individual RAM area, the user can instantly redefine the character set. Some manufacturers can build in a right-to-left character progression capability that will handle Middle Eastern languages (such as Farsi). One-half dot shift is a terminology which refers to movement on a 10-by-10 character cell grid. This capability allows for finer character definition for highly curved symbol, such as a G or the hump on an M. So when your terminal requires the use of italics or a set of specialized symbols, it might be beneficial to consider a terminal that has the half-dot shift capability. Additionally, if a specific terminal will always use a specific set of characters, then a ROM character generator should be specified. For a terminal that is going to constantly have several character sets, it is best to use a RAM character generator. In either case, most intelligent terminals should be able to address up to two different character generators.

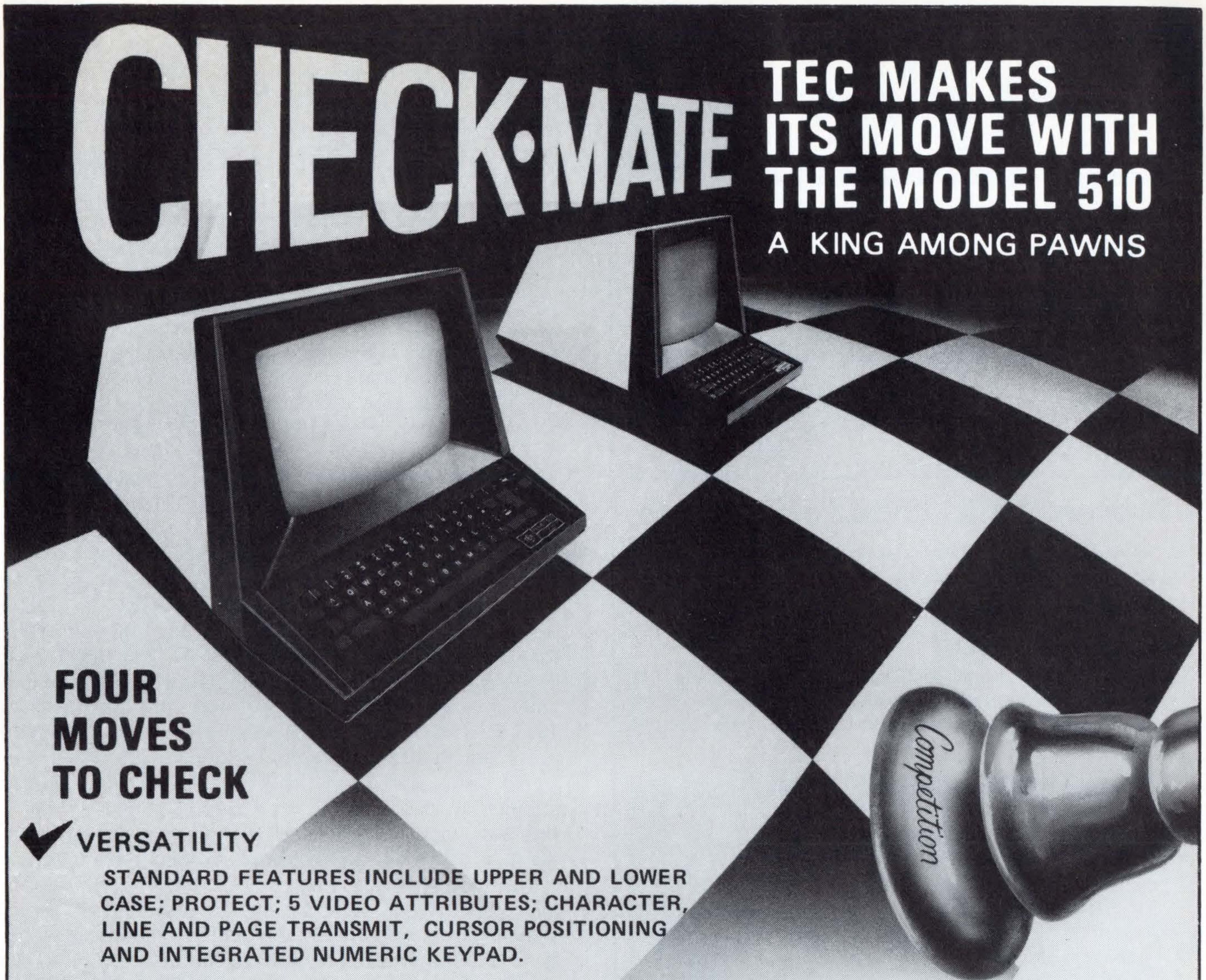
### Communications

Probably one of the most dynamic aspects of intelligent terminals occurs in the area of communications. Intelligent terminals can be adapted to communicate with one host computer after another, simply by changing the protocol of the terminal rather than adapting the host for a terminal. Protocol refers to the vast sequence of messages and responses required between a terminal and a host computer, or between a terminal or a peripheral, such as an on-line printer. Most typical intelligent terminal configurations make use of either an RS-232C type of interface or a current loop interface. RS-422/423 is a long distance differential driver-type of communication interface that is rapidly becoming popular. Most recognized vendors are now offering this option, which allows the user to have CRT terminals some 4000' away from the host computer without using a modem.

LSI, or large-scale integration, has been advancing quite rapidly within the past few years. As a consequence, an intelligent terminal's communications interface can now be programmable for three types of operations: asynchronous, synchronous or isochronous. Similarly, word length, parity and baud rate are all under program control.

### Selecting a supplier

Once the customer's application has been defined, the vendor's capabilities studied, then the buyer must narrow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the choice to a single supplier. Every job application is very specific and very special, and each intelligent terminal vendor makes a significant effort to match his own equipment, resources, programs and engineering capabilities with the customer's requirements and a realistic but competitive price. Visit all potential vendor suppliers. One visit to a plant can reveal a lot of surprises. You can tell whether a particular company can supply a quality terminal. Write down the vendor's requirements and ask for suggestions for your specific applications during your plant visit.

Quality does not happen by accident: it is an integral part of the manufacturing process. It is designed into the system from day one. When visiting the vendor's facilities, examine the testing procedures. Are incoming parts tested? Are subsystems tested at each level of assembly? How precise and complete is the assembly documentation? Is environmental testing done? Is stress testing done? What types of incentives are offered employees for quality work?

Because of its commitment to quality, many firms make it a policy to maintain a particular high standard of quality control. All component parts for any given PC board are checked, tested, examined and re-examined. ICs and memory devices, for instance, are submitted to an initial 168 hours of burn-in at 125° F. Following assembly, a function test is performed that subjects the PC board to temperature extremes from ambient to over 135° F. Once the PC board is configured into the system, the unit will undergo a minimum of four continuous days of host controlled testing at 125° F. Throughout the assembly process an examination procedure should include power supply load testing, automated testing and a functional systems test that runs each terminal at load capacity for a specific period of time. In this way, they insure that all components throughout the machine will work and continue working for a long time.

Such stress testing is one way the buyer can be sure that his equipment will have a long and maintenance-free life. Many vendors will offer for a small fee some special warranty or extended warranty covering anywhere from 30 days to two years from purchase. However, if you have purchased equipment with a high MTBF rating in the 3000 plus hours category, an extended warranty may not be a requirement. In such cases the cost of repairing faulty terminals will be quite low in comparison to the cost you are paying for the extended warranty.

In specifying an intelligent terminal, consider interface requirements, environmental factors and architectural design. For printers and other peripherals, you may well need special hardware or firmware built into the system. You may also need to define the exact protocol required whenever intelligent terminals communicate with one another or with the CPU. Special temperature and humidity requirements could be necessary for terminals to be used in extreme climates like Fairbanks, AK or Needles, CA. If, however, terminal operation will occur in air-conditioned environments, stringent environmental specifications should be by-passed. The important thing to remember is that if you have a requirement, *state it.* If you have a problem and want it solved, state it and leave the solution to the vendor. Unnecessary requirements are costly for both user and developer.

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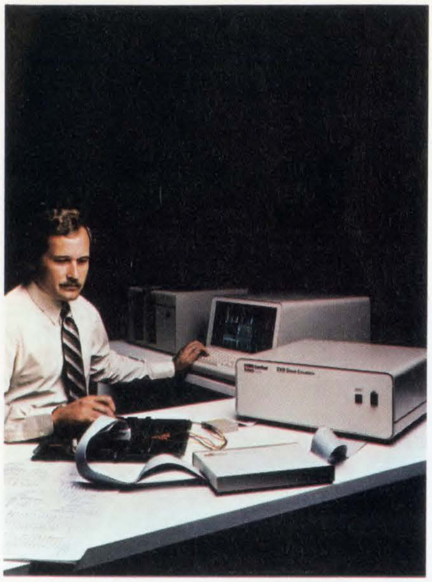


# New-Generation μC Development System

## Supports Development of Real-Time and Multi-Processor Systems

**Lester G. Matheson and**
**David J. Ulmer**
*GenRad/Futuredata, Los Angeles*

Today's μC development systems essentially are bundles systems. Since system hardware and software features are in one box, compromises were made.

The compromises exist due to economic considerations. At that time, μP components and memory were still quite expensive, and this had a strong effect on system design. This caused systems to appear as bundled, resource sharing, time sharing, bus sharing, memory sharing, processor sharing systems. With all this sharing going on, it was inevitable that the user and user's system had to share resources with the development system. In doing this, the compromises of the development system design were propogated into the user's system. The user's ability to develop modern multi-processor and real-time systems was therefore limited by the outdated architecture of the development system tools.

The development of the GenRad/Futuredata 2302 Slave Emulator is the first serious attempt to revolutionize the architecture of development systems and provide the user with vastly improved development capability. With these new tools a μC systems designer will be able to do a much better job of designing the systems of the future.

### The slave emulator

The Slave Emulator, therefore, was designed to unbundle this outdated architecture. The goals were to develop an emulation system that would allow the user complete freedom to develop new systems' architecture as he saw fit to provide new development system capability that currently did not exist in the market.

The Slave Emulator is unbundled in the respect that the emulation processor, emulation memory, and emulator bus are completely separated from the development systems' master control computer. **(Fig. 1)** Emulation is truly transparent and no processor resource restrictions are placed on the user's system. Full real-time emulation is started just as soon as the Slave Emulator power switch is turned on, and from that time on the emulator acts as if it were the processor chip itself. Operation of the user's system is not halted or otherwise interfaced with by the emulator unless specifically told to do so by the user at the console of the master control computer. For normal debugging requests only the absolute minimum of emulation processor time is used to answer the user's requests.

The master control computer for the Slave Emulator is the GenRad/Futuredata 2300 Advanced Development System (ADS) computer. This unit is the same console used to support the existing line of bundled emulators and can easily be upgraded to support the new Slave Emulator concept.

The 2300 ADS provides all the software development resources and Slave Emulator control programs needed to complete the user's development system. It can have its own stand-alone disk and printer resources or be attached to the GenRad/Futuredata 2301 Network Control Processor (NCP) in order to share disk and printer resources with a network configuration.

The new Multi-emulator Debugger software running on the 2300 ADS with Slave Emulators allows a single user to control and debug a system consisting of up to eight μPs running simultaneously. The debugger uses a concise command language designed to

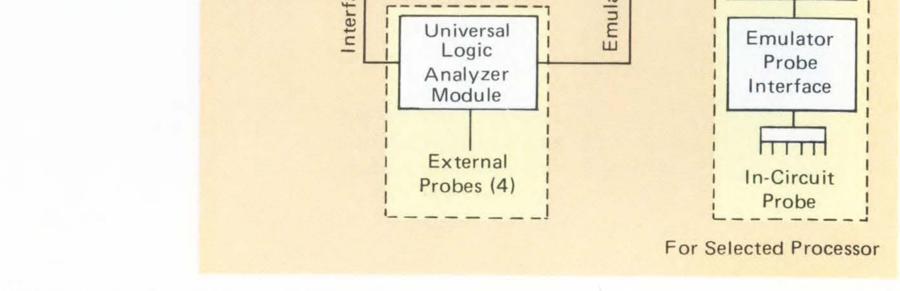
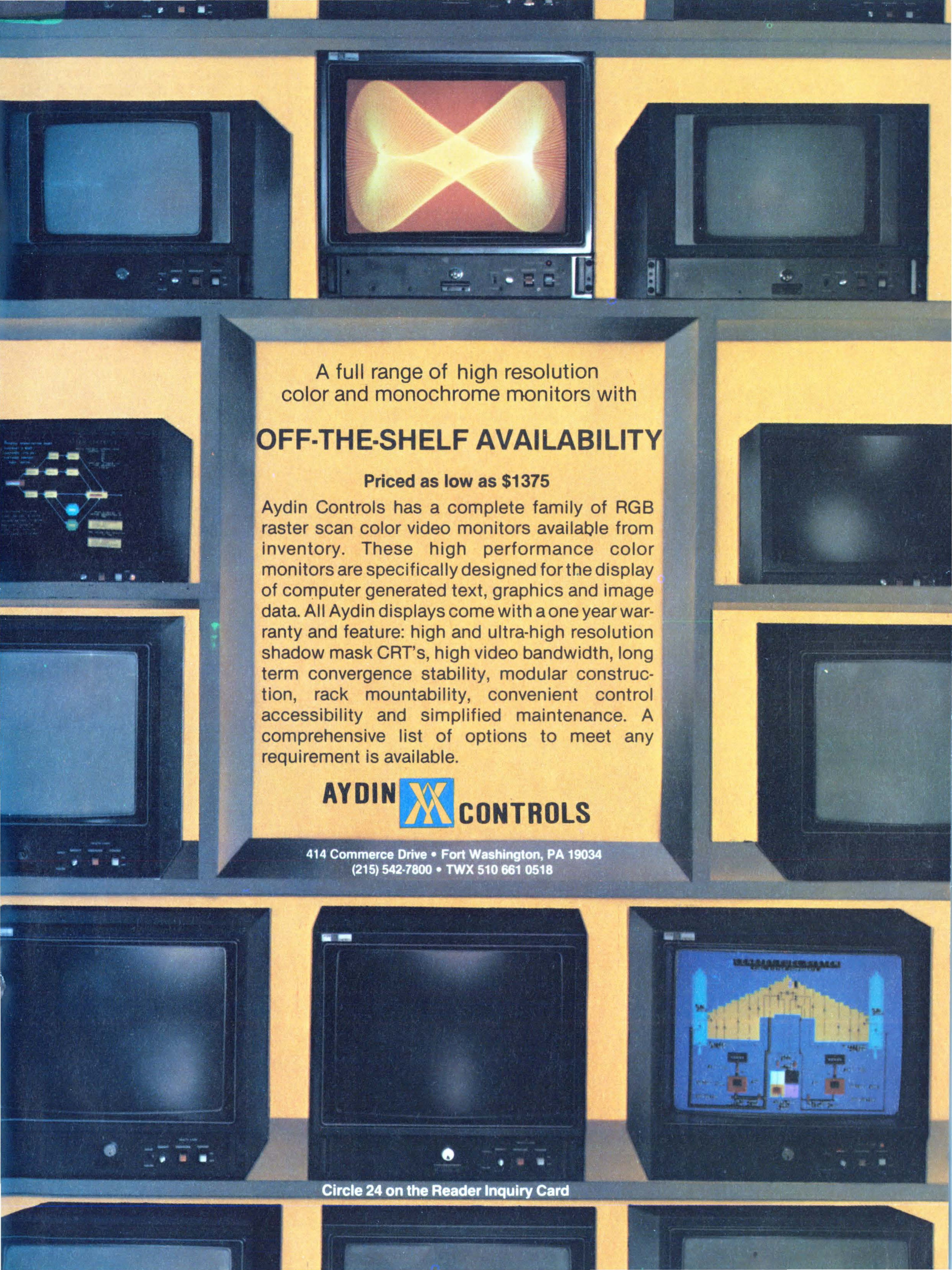



**Fig 1 Slave emulator block diagram.**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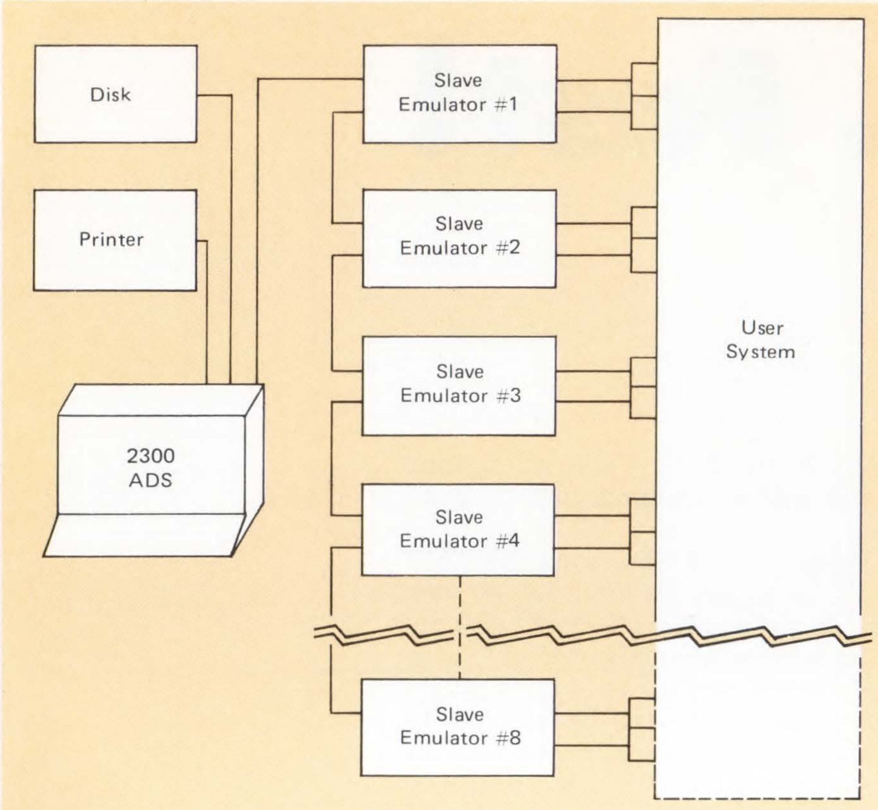



**Fig 2 System diagram multiple slave emulators**

maximize usability by minimizing keystrokes and utilizing confirmation of critical commands.

The 2300 ADS software set also provides a file manager, text editor, compilers, assemblers, linker and utilities. The 2302 Slave Emulator includes a logic analyzer and is equipped with the desired processor personality modules. If multiple Slave Emulators are utilized, the units are linked together via a high-speed RS232 daisy chain **(Fig. 2)**. Together, master computer, the Multi-emulator Debugger, and the Slave Emulator provide a new level of capability for the development and test of multi-processor systems.

It should be emphasized here that $\mu$P-based products are no longer limited to the use of just one processor. Selecting the right processor for a particlar function remains a challenge, particularly since so many options exist. The process of checking and optimizing each selection is greatly aided by the slave emulation concept; however, in many cases, the concept of simultaneous emulation of multiple chips is an absolute necessity.

With this new system, the user is allowed to interact with any of the slave emulators at any time via the keyboard, the CRT and the emulator debugger. The user can switch debugging operations to any slave emulator by use of the debugger context switch command. With the CRT the user can display up to four memory areas and CPU of any one processor system **(Fig. 3)**. The CRT is also used to display error messages and user prompts. The user interface is further enhanced by the use of reverse and double intensity video effects on the CRT display.

The Slave Emulator thus provides real-time, full-speed, transparent emulation. This remains true even when all memory resources are mapped into the slave emulator memory, and for processors with memory cycle times down to 100ns. The Slave Emulator requires no CPU resources in the target system such as memory space, I/O space or interrupt vectors. Up to 128K bytes static RAM or 512K bytes dynamic RAM can be mapped in 4K or 16K blocks to any locations within a total 1M byte memory space. Mapping of memory references to internal or external memory is done in 256 byte sections. Write protection throughout the 1M byte space is also done on a 256 byte basis. All I/O is mapped externally.

As noted previously, the Slave Emulator also provides a 64 channel logic analyzer. Sixty bits of information are acquired from the internal bus and four bits from external probes. Examination of the logic analyzer trace and logic analyzer setup are integral functions of the debugger. Four hardware breakpoints, settable for trigger combinations and sequences are provided to control trace and debug operations. An example of a slave emulator logic analyzer display for the 8085 is shown in **Fig 4**.

## Non-stop visibility

Perhaps the most significant feature of the slave emulator is that it allows debugging operations to be performed concurrently with the normal operation of the system under test. This is

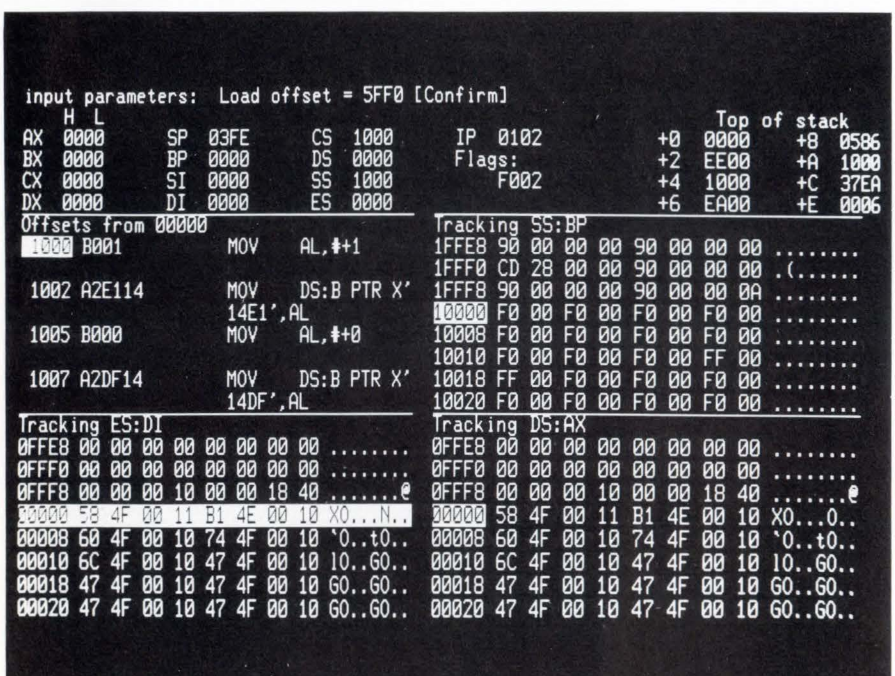
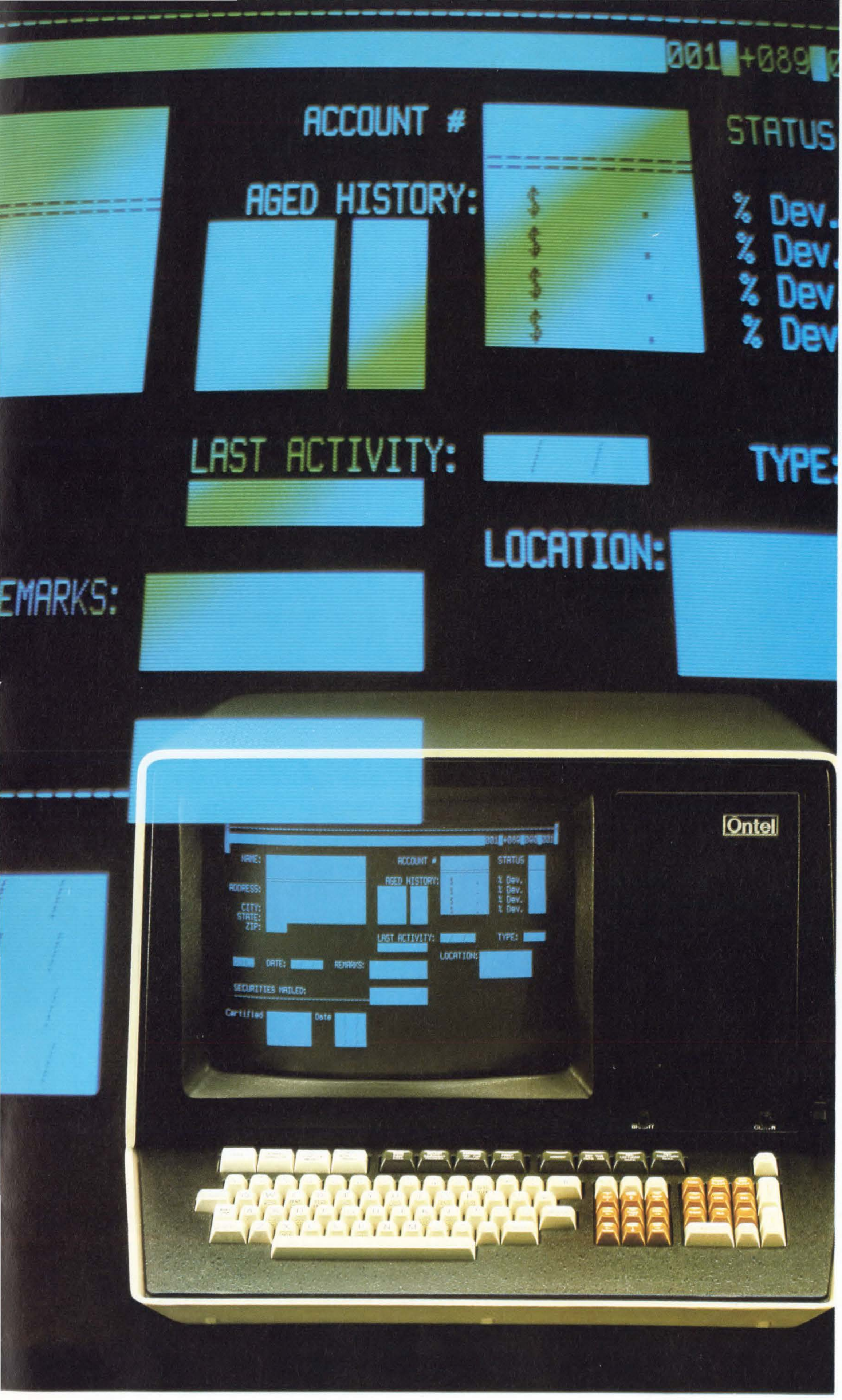



**Fig 3 8086 Multi-Emulator Debugger Display showing the 8086 register display along with an image of the top of the user's stack.**

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accomplished by allowing the emulation processor to return immediately to the target system program after completing a short debug sequence. No longer must the system under test be halted for relatively long periods of time, making debugging of time-critical processes and real-time systems impossible.

The internal architecture of the slave emulator affords, to the sophisticated user, the ability to specify special debug sequences to be executed by the emulation processor. This allows the user to develop a command set tailored specifically to the problems being attacked.

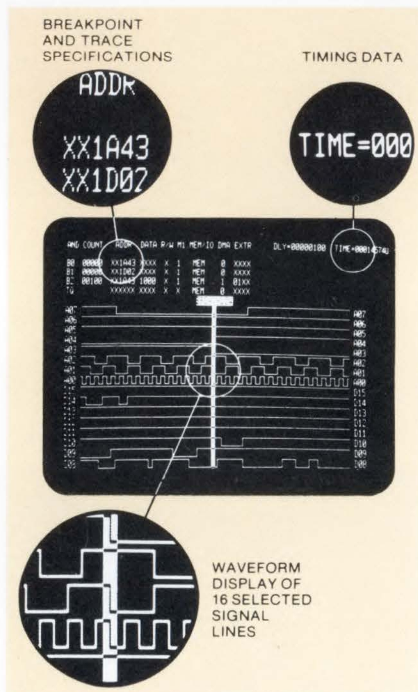


**Fig 4 Slave emulator logic analyzer display.**

Another unique capability of the slave emulator is its ability to allow the user to stimulate the system under test. Without halting normal system operation, variables can be forced out of range, or I/O ports can be manipulated. This is possible because of the truly transparent nature of the emulation provided by the slave emulator system.

The slave emulator along with the command file processing function of the Multi-emulator Debugger provide the ability to do automated testing or production testing of single or multiple processor systems. Tests can be run on read/write memory, read only memory, input/output, interrupts, and even multiprocessor interaction. Tests can be fully automated or set up to allow operator intervention using the CRT and keyboard of the ADS.

## Real-time environment

An example of using the Slave Emulator in testing in a real-time system would be in the development of a control system for automotive engine. Here the engine control processor is required to constantly maintain data on temperatures, pressures, throttle position, RPM and rotational position. At the same time, the processor must make calculations and provide precise ignition timing, control of fuel injection and emission control. Since the processor must be running in order for the engine to be running, this is a class of real-time system. The 2302 Slave Emulator has been designed to provide the developers of these types of systems with a real-time debugging tool that will allow them a window into the actual operating real-time system.

In the case of the engine control processor, utilizing the Slave Emulator's ability to perform tests very rapidly and transparently allows tests to be performed while the automotive engine is actually running. This prevents the constant restarting or resetting up of the conditions which are being examined, as would be necessary if the control processor and engine were halted each time the user examined some particular element.

## Multi-processor environment

Next, consider a network of point-of-sale terminals connected to a central computer. This network can be examined and debugged by emulating with a Slave Emulator each of the processors on the network which is involved in any particular problem. Up to eight processors of any supported type can be debugged simultaneously using the Multi-Emulator Debugger. While interacting with any particular Slave Emulator, the user has the full capability of the debugger and Slave Emulator at hand. To debug or test the network of point-of-sale terminals, a breakpoint can be set in any processor under test to detect the particular condition desired. This breakpoint can be used to trigger the debugging and tracing functions on all processors which are being emulated and allow analysis of complex interactions between various processors of the multi-processor system.

Want additional information? Contact **GenRad/Futuredata**, 6151 West Century Blvd., Suite 1124, Los Angeles, CA 90045, (213) 641-7200.

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# A Beautiful Way To Interface

## IQ 140

SOROC's first and foremost concern, to design outstanding remote video displays, has resulted in the development of the IQ 140. This unit reflects exquisite appearance and performance capabilities unequaled by others on the market.

With the IQ 140, the operator is given full command over data being processed by means of a wide variety of edit, video, and mode control keys, etc.

The detachable keyboard, with its complement of 117 keys, is logically arranged into 6 sections plus main keyboard to aid in the overall convenience of operation. For example, a group of 8 keys for cursor control / 14 keys accommodate numeric entry / 16 special function keys allow access to 32 pre-programmed commands / 8 keys make up the extensive edit and clear section / 8 keys for video set up and mode control / and 8 keys control message and print.

Two Polling options available: 1) Polling compatible with Lear Siegler's ADM-2. 2) Polling discipline compatible with Burroughs.

## IQ 120

The SOROC IQ 120 is the result of an industry-wide demand for a capable remote video display terminal which provides a multiple of features at a low affordable price. The IQ 120 terminal is a simple self-contained, operator / computer unit.

The IQ 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IQ 120 terminal incorporates a 12-inch, CRT formatted to display 24 lines with 80 characters per line.

**SOROC TECHNOLOGY, INC.**

**165 FREEDOM AVE., ANAHEIM, CALIF. 92801**
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**Phil Spiegel,**
*Intel Magnetics, Inc,*
*Santa Clara, CA*

# Getting Started In Bubble Memories

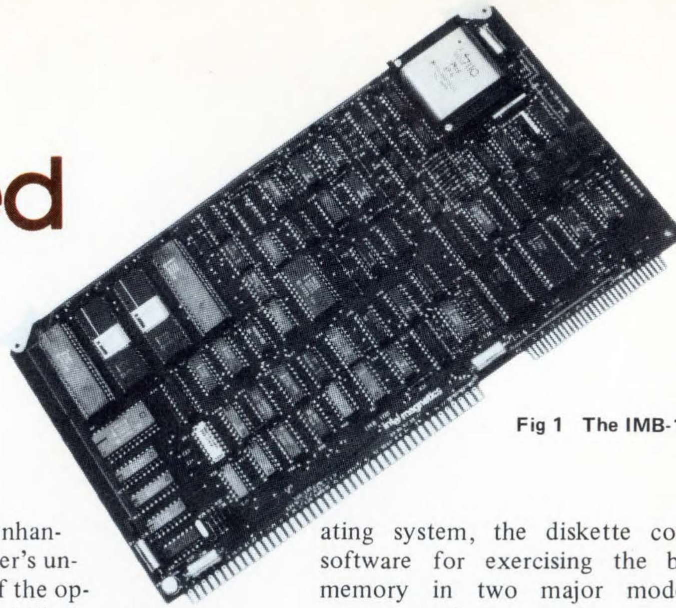

Fig 1 The IMB-100.

Magnetic bubble memory is becoming extremely attractive to system designers because of its high density, non-volatility and solid-state reliability. However, interfacing the MBM device with the rest of a system has been a challenge. Recently, Intel Magnetics, Inc. introduced a complete megabit bubble-memory system, the 7100. The new system enables an entire megabit of storage and interface circuits to be implemented within 15 in² and requires only 7 active component packages. Along with its system, Intel Magnetics offers the IMB-100, One Megabit Bubble Memory Development Board. This board aids in the utilization of the megabit bubble memory and its associated support circuits. It also enhances the designer's understanding of the operation of the bubble memory.

The IMB-100 is a completely assembled and tested 128 KB nonvolatile memory. All necessary circuits drive, control, and sensing are provided in the package. It is designed to interface with MULTIBUS development systems. Supplied with both single- and double-density diskettes, the IMB-100 is ready to operate upon insertion into any Intellec microcomputer development system.

**Fig 1** is a photograph of the 12" x 6-3/4" IMB-100 board and **Fig 2** is its block diagram.

Besides providing the ISIS II operating system, the diskette contains software for exercising the bubble memory in two major modes of operation. One set of programs allows the user to write data into memory creating files which simulate his intended system application. The same program allows data to be retrieved as desired. Another program, "TESTS", is useful for longevity testing and performance characterization of the device. The IMB-100 will be found useful as an incoming inspection tool following initial system design and familiarization with the megabit bubble memory.

One unique feature of the bubble memory is its ability to function in distress situations. Some storage loca-

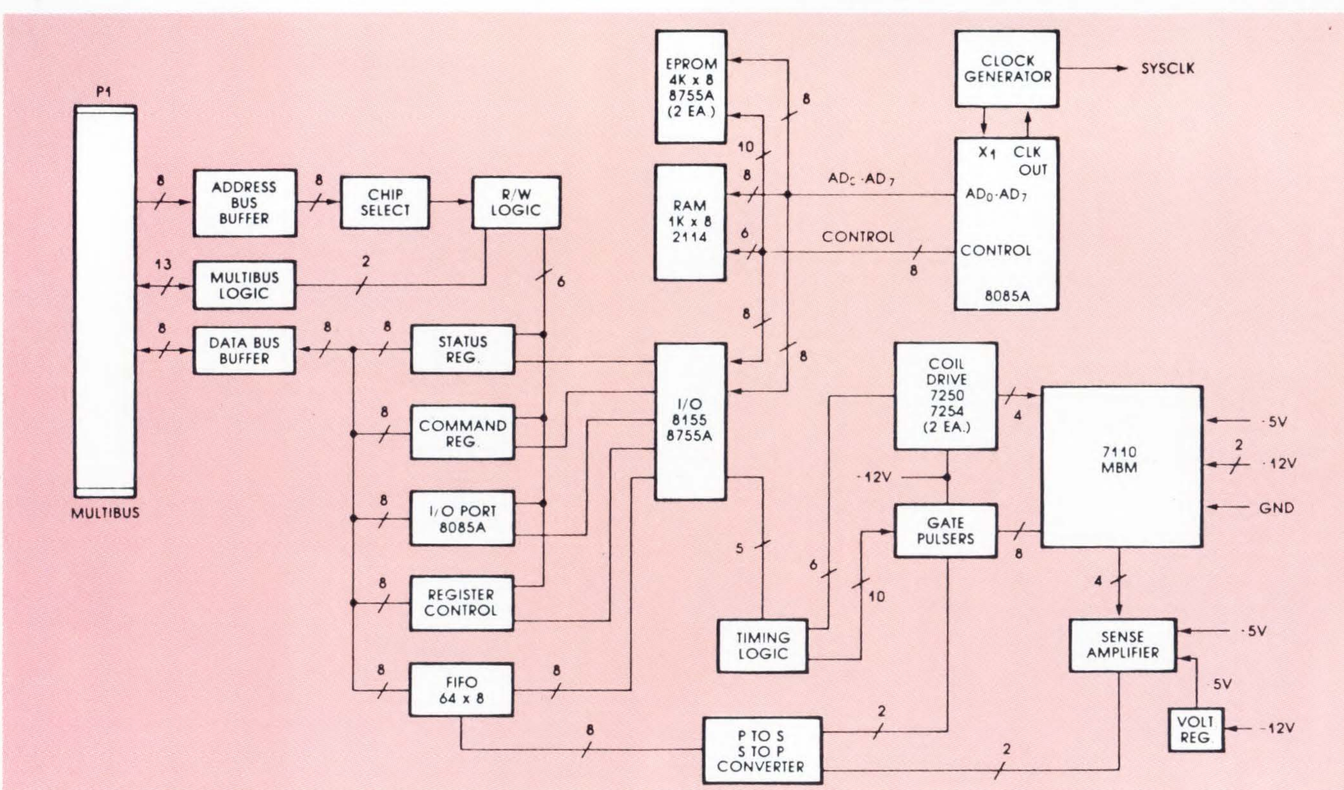


Fig 2 Block Diagram of the IMB-100.

```
-TESTS
MASK FILE 98G7
COMMENT
REPORT FILE

BAD-LOOP MAP AS EXPECTED
A1 01 37 38 40 45 63 66
A2 01 08 19 22 38 58 67 68
B1 02 10 17 28 48 62 65
B2 01 08 21 23

BAD-LOOP MAP AS READ
A1 01 37 38 40 45 63 66
A2 01 08 19 22 38 58 67 68
B1 02 10 17 28 48 62 65
B2 01 08 21 23

BAD-LOOP MAP AS READ
A1 01 37 38 40 45 63 66
A2 01 08 19 22 38 58 67 68
B1 02 10 17 28 48 62 65
B2 01 08 21 23

STATUS BITS (7 - 0) 00000 00003 00000 00000 00000 00000 00000 00003

STATUS BITS (7 - 0) 00000 00512 00000 00000 00000 00000 00000 00512

98G7

BITS IN ERROR (0/1 READ)

00000 BITS IN ERROR ON A SIDE,  00000 BITS IN ERROR ON B SIDE.
```

**Fig 3** TESTS Printout for a typical 7110. After initializing (reading the bootloop and bootloop register), a random pattern is written and read. The status bits reported indicated that the test was successfully completed. There were no errors.

```
ISIS-II, V3.4
-BUBBLE

SELECT FUNCTION DESIRED  (SINGLE DIGIT 1 - 7)
 1  INITIALIZE BUBBLE MEMORY DEVICE
 2  ISIS FILE       TO    RAM BUFFER
 3  RAM BUFFER      TO    BUBBLE FILE
 4  BUBBLE FILE     TO    RAM BUFFER
 5  ISIS FILE       TO    RAM BUFFER
 6  RAM BUFFER      TO    ISIS FILE
 7  EXIT TO ISIS COMMAND LEVEL
- 1
FIFO AVAILABLE
OPERATION COMPLETE

 - 5:C1:
HELLO DOLLY
■
■

 - 3D
FIFO AVAILABLE
OPERATION COMPLETE
```

*(Continued on p. 50)*

**Fig 4** Sequence of creating a file and retrieving it.

tions may be defective but the device will still meet all specifications. The 7110 contains 256 loops of 4096 bits each and provides a binary megabit of guaranteed useful data storage. There are 48 additional loops in the device which may be defective. They are considered "redundant". In system operation the controller notes the locations of the extra loops and "ignores" them when writing or reading. The defective loops are permanently stored in two "bootloops". A factory code word for "good" or "bad" is written into the bootloops, based on results of testing each storage loop. As a convenience, locations of bad loops are written into the diskettes supplied with each IMB-100. A user can ascertain if the bootloops are still storing the original bad loop maps by using the TESTS program. The bad loop map (as stored on the diskette) will be compared with the maps read from the bubble memory. See **Fig 3**.

Other features of the IMB-100 enable users to check out bubble memory system hardware. The 7110 is supplied in a socket construction which allows for easy removal and replacement by another 7110 device or by a dummy module. (The dummy module facilitates measurements of voltages and timing from the current pulse generator and coil drivers.)

The method of writing data into the 7110 is called generation. Binary ones are represented by bubbles which are replicated from a "seed" bubble at the generator site. This approach provides superior operation over a wider temperature range than conventional nucleating generators used in earlier bubble memory devices. Four seed bubbles reside in the 7110. Under normal operating conditions these bubbles will remain at their generator sites indefinitely. However, in the event of loss of coil current while current pulses are being applied, one or more of the seed bubbles may collapse. This may occur if power should fail while the bubble memory is operating or if operating limits are exceeded. However, this is not catastrophic because each IMB-100 is supplied with a seed replacement kit consisting of a PROM and a dual-in-line plug-in module. By following the seed replacement procedure and calling for the SEED program (contained within the diskette) the lost seed bubbles are replaced in a few minutes.

A 7220 bubble memory controller will be available in early 1980. It will have power-fail reset features which

(Continued from p. 48)

```
– 4D
FIFO AVAILABLE
OPERATION COMPLETE

– 6:C0:
5:C1:
HELLO DOLLY

– 7
–BUBBLE

SELECT FUNCTION DESIRED (SINGLE DIGIT 1 – 7)
1   INITIALIZE BUBBLE MEMORY DEVICE
2   ISIS FILE       TO    RAM BUFFER
3   RAM BUFFER      TO    BUBBLE FILE
4   BUBBLE FILE     TO    RAM BUFFER
5   ISIS FILE       TO    RAM BUFFER
6   RAM BUFFER      TO    ISIS FILE
7   EXIT TO ISIS COMMAND LEVEL
– 1
FIFO AVAILABLE
OPERATION COMPLETE

– 4D
FIFO AVAILABLE
OPERATION COMPLETE

– 6:C0:
5:C1:
HELLO DOLLY
```

will permit orderly shut down of power to coils and current pulses in the event of power failures, thus protecting both the seed bubbles and the stored data. The 7220 is being designed with several other features which will be extremely useful in equipment utilizing bubble memories but are not necessary on a development board. These features will include direct memory access, expansion to control up to 8 megabits of bubble memory, and automatic error correction. The IMB-100 does not have these features. However, it is compatible with the 7220 in terms of: addressing and commands for the basic control functions of a one megabit bubble memory device; and interfacing with an 8-bit microprocessor.

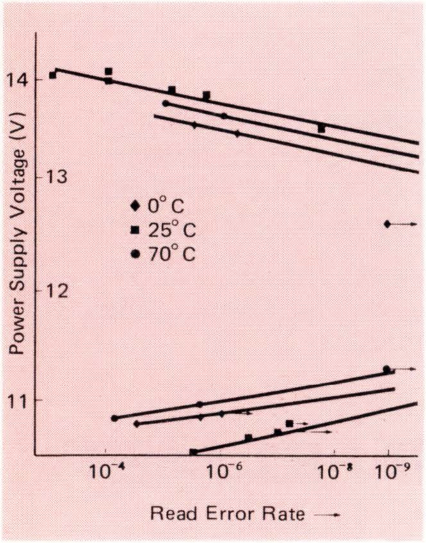


**Fig 5 Read error rate as a function of power supply to coil drivers and detector bridge. Data points with arrows (→) indicate that no errors were observed for that particular power supply voltage.**

To interact with bubble memory a user types "BUBBLE" on the keyboard. A list of seven possible functions is then displayed on the CRT:

- "INITIALIZE". This function is required upon power up. The bootloop data is read and the system is set to page zero.
- "LOAD EXECUTABLE CODE". Allows the ISIS file to be loaded into the RAM buffer. (It is not necessary to use this function if the diskette is to be used.)
- "RAM TO BUBBLE". Writes the contents of the RAM buffer into the bubble memory, overwriting existing contents. A file is created by specifying any letter from A to P.
- "BUBBLE TO RAM". Reads the contents of a specified bubble memory file.
- "DEVICE TO RAM". Allows a specified ISIS file to be read into the RAM buffer.
- "RAM TO DEVICE". Displays the contents of the RAM buffer.

(Fig 4 is an illustration of a sequence of creating a file in the bubble memory and reading it out at a later time after turning power off and on, thus demonstrating non-volatility.)

- "TESTS". This program is useful for long term bubble memory device life testing. A random data pattern fills the megabit memory and is read 100 times ($10^8$ bits read). The bootloop is re-read and the complement of the random data pattern is written. The complementing data are now read 100 times and the sequence is repeated. Extensive testing of (more than 50 samples of the 7110) has shown that under normal operating conditions (0-70°C ambient temperature with ±5% tolerance on power supply) the read error is $10^{-9}$, **or 1 reading error in one billion bits. Fig 5** shows a plotting of the read-error rate, taken on a component tester, as a function of power supply voltage temperature. (Similar data can be taken on an IMB-100.)

The error rate can be improved by seven orders of magnitude by use of an automatic error correction being designed into the 7220 controller and 7242 formatter. These two devices will be part of a family of support circuits produced by Intel Magnetics which will enable the design of a megabit (128K byte) bubble memory system in an area only 16 square inches, and requiring only seven active device packages.

The IMB-100 development board is an excellent tool for introducing a user to bubble memory and Intel Magnetics' support circuits. The availability of the support circuits and the IMB-100 will greatly simplify the task of interfacing a bubble memory to a microprocessor.

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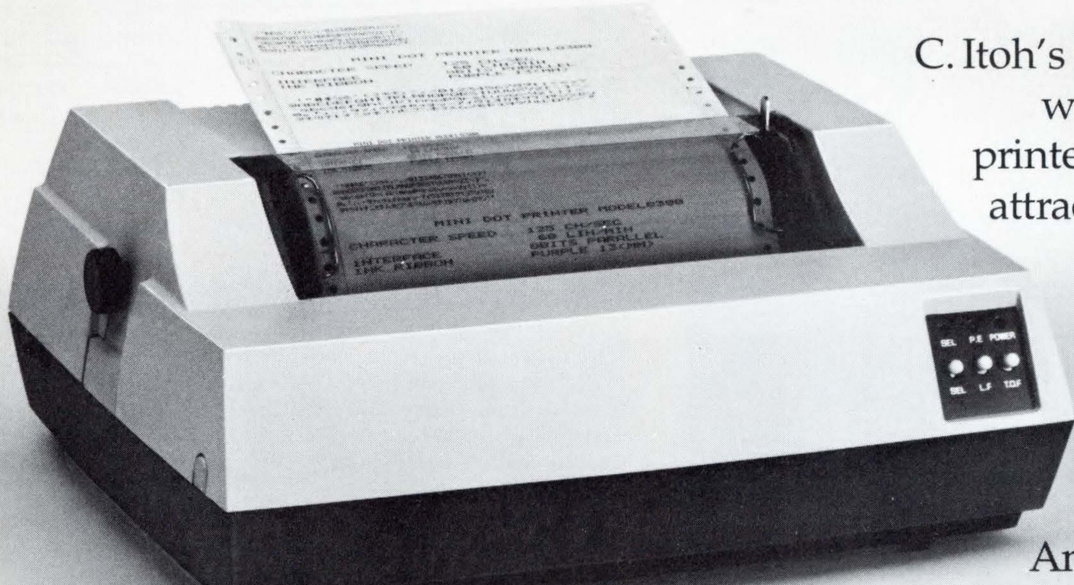
# Only one printer is equal to our Model 8300P.




C. Itoh's model 8300 was one, fine printer. It was an attractive, quiet, low-cost unit with a straight-forward, reliable design.

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So when we created our new 8300 Series Printers, we not only made them better, we gave you a choice: the 8300R has an RS-232C designed to interface at rates up to 9600 Baud with a 20/40/60 mA current loop; and the 8300P designed with a 7-bit parallel interface. Both feature a continuous-duty 7-wire head with a life expectancy of 100 million characters, and both print bi-directionally in 80 columns of crisp, 9x7 dot matrix at 125 CPS. An 132 column format with condensed print capability is also available. Both accept multi-ply pin-feed paper in any width from 4.5″ to 10″; paper can be loaded from the bottom or rear; and the print position line is easily adjustable. Both our 8300P and our 8300R are still attractive, quiet, low-cost units with straightforward, reliable designs. Because both are still from C. Itoh. Of course.

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# New Products

**GRAPHICS IMAGING.** The Visacom visual computer system is powered by a DEC LSI/11 with the ability to address 512K bytes of memory. The system operates under RT11 and has all the standard DEC LSI/11 software provided. It operates off-line with floppy disks or can be interfaced to a host computer. The display system allocates a portion of the computer memory to visual display with a choice of 512 horizontal by 480 vertical pixels with 16 bits for each pixel or 156 horizontal by 156 vertical. The image system has hardware zoom and pan (scroll) as well as color and monochrome intensity transformation unit. $15,000. **DeAnza Systems**, 118 Charcot Ave., San Jose, CA 95131.

**Circle 283**

**UNIVERSAL BINARY-SYNCHRONOUS EMULATOR** known as the Remote Batch Terminal Emulator (RBTE) emulates most binary synchronous terminals including the IBM 2780, 2770, 3741, and 3780. Each supported terminal has a configuration file containing 13 configuration parameters set to define a specific terminal. The RBTE reads disk records from a CP/M file, reformats them into a Bisync block, and transmits them to a remote terminal. Alternatively, a Bisync Block will be received from the remote terminal, unpacked into disk records and written to the specified CP/M file. Another product, the Bisync Communication Driver, allows an application program to directly communicate to the Bisync communication ports with simple open, close, read, write, connect and disconnect commands. **Winterhalter & Associates, Inc.**, 3825 N. Zeeb Road, Dexter, MI 48130. **Circle 281**

**PROTOCOL CONVERTER**, the PCU 200, has two serial I/O ports and allows most RS-232 compatible devices to be put on line under various communications protocols. A single board 8085 μP-based controller with up to 8K of buffer storage and up to 8K of program storage, it is designed to function at program selectable baud rates in asynchronous or synchronous modes independently at each port under program control. **Air Land Systems**, 2820 Dorr Ave., Fairfax, VA 22031. **Circle 289**

**TRS-80 SOFTWARE (PROGRAMS)** include: General Ledger I, (diskette only) for a small business; Disk Mailing List System for TRS-80 mini-disk owners, Cassette Mailing List System, RAM-based Level-II program for non-disk users, and an Inventory Control System (ICS), (diskette only). Statistical programs include Statistical Analysis, Double-Precision Subroutine (15-digit accuracy with sine, cosine, arctangent, natural logarithm, exponential and square root functions), and Advanced Statistical Analysis (ASA). RS232C Communication Software (Level-II), used with a telephone interface, permits TRS-80 to TRS-80 communications by telephone. **Radio Shack Computer Customer Service**, 205 NW 7th St., Fort Worth, TX 76106.

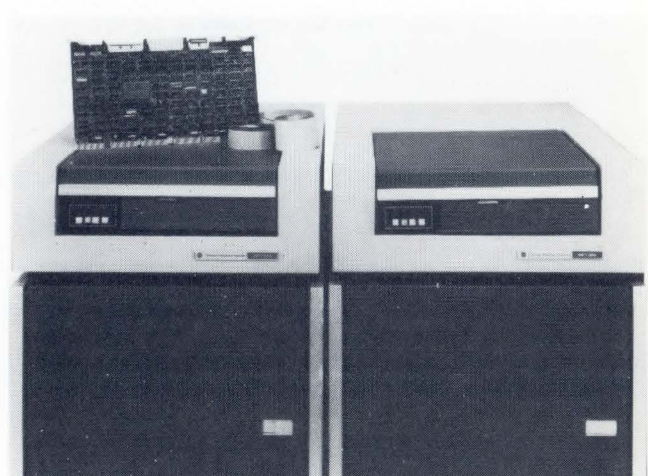
**Circle 293**

**MONITORS.** Medium and high resolution color and monochrome monitors are designed to serve users of digital raster scan display systems. RBG color monitors are offered in resolutions up to 1000 lines in 13 and 19-in. CRT (diagonal). Prices start at $3,450. Monochrome monitors are offered with the same resolution in 9, 14, and 17-inch CRT (diagonal). Prices start at $750. **DeAnza Systems, Inc.**, 118 Charcot Ave., San Jose, CA 95131. **Circle 292**

**POCKET TERMINAL** can be carried in a toolkit or pocket and plugged into a digital system to input and read data. The terminal has 40 positive response keys, allowing 128 ASCII codes to be selected and transmitted as eight bit words with parities and start/stop bits. Data received is held in the 30 character memory for access in 8-character blocks on the LEDs which will display a clear correctly formed 64-character upper case alphanumeric and symbol set. The terminal is interfaced for RS232/C compatibility. A single 5V power supply is needed at 450mA max. **G.R. Electronics Ltd.**, 1640 Fifth St., Santa Monica, CA 90401.

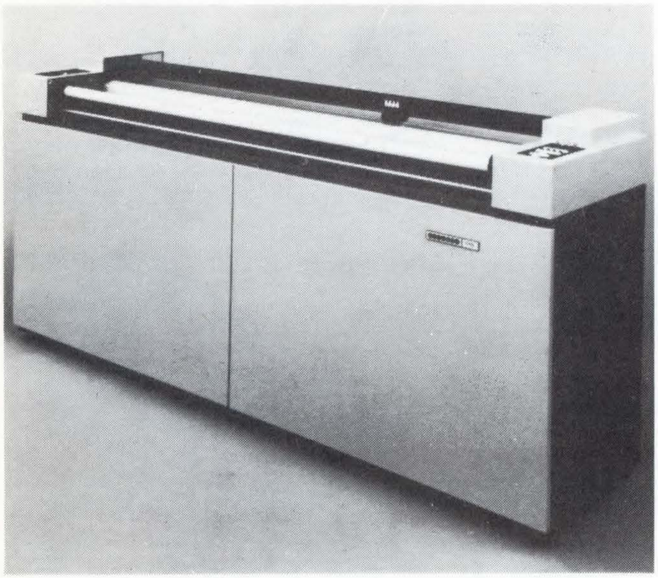
**Circle 282**

**DISK CONTROLLER** emulates the DEC RP11 and provides compatibility with system software for the RP11, RP02/RP03 subsystems. The PM-DC1100 is a μP-based single board controller capable of directly handling two storage modules (80 or 300 Mbyte), or up to eight storage modules with multidrive interface chassis. The compatible mode emulates the RP11 and three RP02 logic drives on the PM-DD11/80 80 Mbyte drive, without requiring any software changes. $3,230. **Plessey Peripheral Systems**, 17466 Daimler, Irvine, CA 92714. **Circle 280**



**PLANAR GAS DISCHARGE DISPLAY**, the SP-452, displays up to 16 characters. Total display package measures 1.55 by 8.90 in. Each character is 0.5-in high and is readable thru a 150° viewing angle. The SP-452 technical bulletin provides complete specifications, dimension, mounting instructions and applications information. **Beckman Instruments, Inc.**, Display Systems Division, 350 N. Hayden Rd., P.O. Box 3579, Scottsdale, AZ 85257. **Circle 287**

**6-FOOT-WIDE PLOTTER** – the 1065 has a maximum axial drawing speed of 30 ips, uses linear pen actuation for fastest pen up/down times available, and has an acceleration rate of 2G. The 1065 drum plotter features resolution of .0005 in., uses four program selectable pens and can operate in online, offline and remote/timesharing environments. Other features include y-axis limit switches, paper supply monitor, paper cutter bar, plot time meter and plot speed



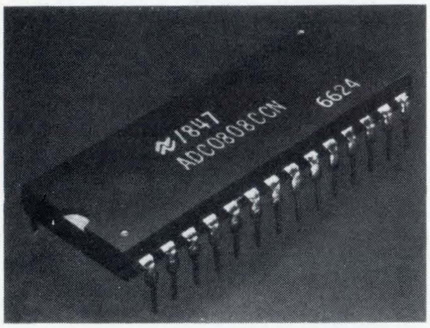
control. A return to last plotted position feature and self-test diagnostics are also included. **California Computer Products, Inc.**, 2411 W. LaPalma Ave., Anaheim, CA 92801. **Circle 288**

**MULTI-USER DATA ENTRY** system offers, in its basic configuration, 10 Mbyte of hard disk storage, a 10-Mbyte capacity tape cartridge drive for software backup and recovery, and four user ports. The 5000/ES includes the Multus multi-user timesharing executive. Disk storage may be expanded in increments of 10, 29 or 58 Mbytes to 184 Mbytes. Up to four tape cartridge drives may be installed in the basic tape module. The number of user ports, which are used with asynchronous, ASCII RS-232C compatible terminals, may be expanded from four to 32. **BTI Computer Systems**, 870 W. Maude Ave., Sunnyvale, CA 94086. **Circle 277**

**HIGH SPEED DATA MODEM** conforms to CCITT recommendations V.27 bis and V.27 ter. The LSI 48/V.27 unit operates at 4800 bps over 2- and 4-wire leased lines or 2-wire dial networks. It can be used in either point-to-point or multipoint networks, and includes a fully automatic adaptive equalizer. System monitoring and fault isolation features, including V.54 remote loopback and a low speed V.23 secondary channel, are provided. The LSI 48/V.27 processes synchronous serial data at 4800 bps with fall-back to 2400 bps and uses 8-phase DPSK or QAM for primary signaling in the transmitter and receiver with narrow band modulation. $4,585. **Codex Corp.**, 20 Cabot Blvd., Mansfield, MA 02048. **Circle 286**

## New Products

**DATA ACQUISITION SYSTEM.** The ADC0808 and ADC0809 incorporate all essential elements of a μC compatible data acquisition system onto a single chip, including an 8-bit ADC, 8-channel multiplexer and μP compatible control logic. ADC0808/09 is designed for users who may not require




the ADC0816's 16-bit multiplexing capability. Able to perform a conversion in 100 μs, ADC0808/09's resolution is 8 bits, zero error is ±1/4 LSB, FS error ±1/4 LSB and quantization error is ±1/2 LSB. It's supplied in a 28-pin cavity DIP, features a linearity error of ±1/4 LSB typ. and ±1/2 LSB max, a total unadj. error of ±1/4 and an abs. accuracy of ±3/4 LSB typ. and ±1 1/4 LSB max. The 8-channel MUXr can directly access any of 8 single-ended analog signals. ADC0808CD, $29; ADC0809CCN, $19.95 (100-999). **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 180**

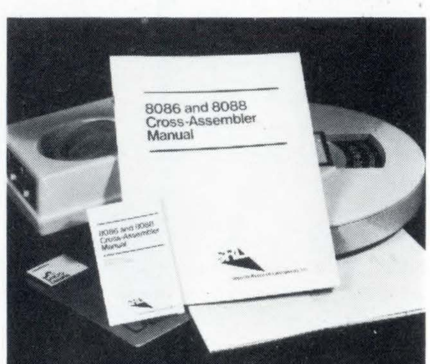
**RASTER SCAN GRAPHICS SYSTEM** emphasizes display clarity and memory plane versatility. The GMDS-4000 monitor with non-interlaced refreshing of the full 1024 scan lines 60 times per second, provides a clear and stable display. The monitor offers 1024, 864 or 768 pixels on each of the 1024 lines, with any two of these formats selectable under program control. This graphics system optionally allows up to 4 separate memory planes, each containing 1 Mbit. Multiple memory planes can be selected to provide a combination of capabilities. Interfaces are available for Intel multibus, Zilog Z-80 or LSI-11 Q bus. **Image Automation, Inc.,** Santa Clara, CA 95051. **Circle 296**

**32-BIT SUPERMINI** Model 3240 handles large and complex problems, such as those found in real-time simulation, scientific computation and high-speed data acquisition applications. The Multi-Terminal Monitor allows up to 32 concurrent users to program interactively with the system in any mix of languages (FORTRAN VII, COBOL, RPG II, BASIC, CORAL 66, CAL and CAL MACRO). Model 3240 can be configured with up to 16 Mbytes of directly addressable MOS memory which allows for the easy implementation of large, complex systems. It allows memory size and system throughput rates to be tailored to the application at hand. Memory systems can be built from a min. of 256KB up to 16MB. I/O rates of 10MB/sec through 40 MB/sec are available. From 8 to 32 DMA access ports can be configured on a Model 3240 system with each port capable of controlling up to 16 devices. **Perkin-Elmer, Computer Systems Div.,** 2 Crescent Pl., Oceanport, NJ 07757. **Circle 183**

**200 CPS 7 x 9 MATRIX PRINTER.** Model 2056 for attachment to System/34 and System/38 computers has a print speed of 200 cps, a printhead advance of 60 ips and a paper slew rate of 20 ips. The graphics set for the Model 2056 is 96 printable characters. A choice of either 10 or 16.5 cpi permits selection of horiz. spacing most appropriate for a particular run. $5,975. **Memorex Corp.** San Tomas at Central Expwy., Santa Clara, CA 95052. **Circle 176**

**8-BIT A TO D CONVERTER** performs a full-accuracy conversion in 15μs, can be connected directly to a μP bus and addressed as RAM. The AD7574 acts as a memory mapped peripheral and at the user's option may be interfaced like static RAM, ROM, or slow-memory. A data read is performed by executing a memory READ to the AD7574. The AD7574 uses control input signals CS, RD and BUSY. **Analog Devices Semiconductor,** 829 Woburn St., Wilmington, MA 01887. **Circle 143**

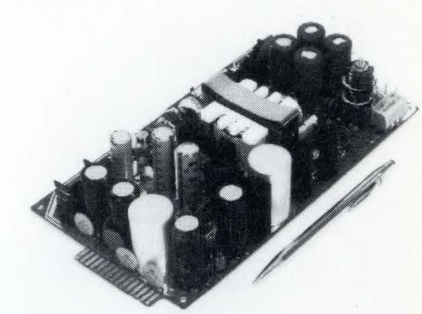
**8086/8088 CROSS ASSEMBLER.** The SRL86 produces object code in 8086 or 8088 machine language format, is written in simplest DEC BASIC, and runs directly on systems with OS-8 or RSX-11M operating systems. It can be easily adapted to other forms of BASIC for other CPU's by modifying a few statements or symbols. Approximately 1000 lines in length, the SRL86 can be run on any system




that supports BASIC and FILE structure and which has at least 16kb of memory. $80.86. **Security and Reearch Laboratories, Inc.,** 3 Ledgetree Rd., Medfield, MA 02052. **Circle 192**

**DUAL REDUNDANT QPSK MODEM** offers a high availability communications link for critical data paths. The unit features dual modulator/encoders and dual demodulators/decoders interconnected to switching networks. Each unit features internal fault sensing which causes an automatic switchover to the standby unit. The demodulator data output is further processed by a convolutional decoder and bit synchronizer. Data rates are available from 32 KBPS to 20 MBPS. **Aydin Monitor Systems,** 401 Commerce Dr., Fort Washington, PA 19034. **Circle 141**

**65W SWITCHER.** This multiple-output switchmode supply for μP and floppy-disk applications offers max. continu-



ous power rating of 65W that can be drawn from any output(s) up to: +5V -6A, +12V-2.5A, -12V 1.0A, -5V-0.5A and +24V-1.5A. All outputs are protectected from shorts. 9.45″ x 5.0″ x 2.0″; 1.7 lbs. $83-$165 (25-49). **Conver Corp.,** 10631 Bandley Dr., Cupertino, CA 95014. **Circle 188**

**6802 SUPPORT CAPABILITY MODULE** called the EM 6802 – supports the 6802 μP for use with Millenium's MicroSystem Analyzer-Series 4000. The Analyzer is a universal tester for μP-based systems – a test instrument that combines time-domain analysis, in-circuit emulation, and signature analysis capabilities within a single package. The analyzer performs functional board and systems testing and node level fault isolation. **Millenium,** 19020 Pruneridge Ave., Cupertino, CA 95014. **Circle 132**

**PDP-11 μP DISC CONTROLLER,** Model DU100 is a RK11 replacement for RD05 drives. The DU100 uses any industry standard drive, expanding your storage to 20MB with improved transfer rates and savings up to 50%. **Distributed Logic Corp,** 12800 Garden Grove Blvd, Garden Grove, CA 92643. **Circle 201**

ITEM NO.
WK-7

CMOS SAFE

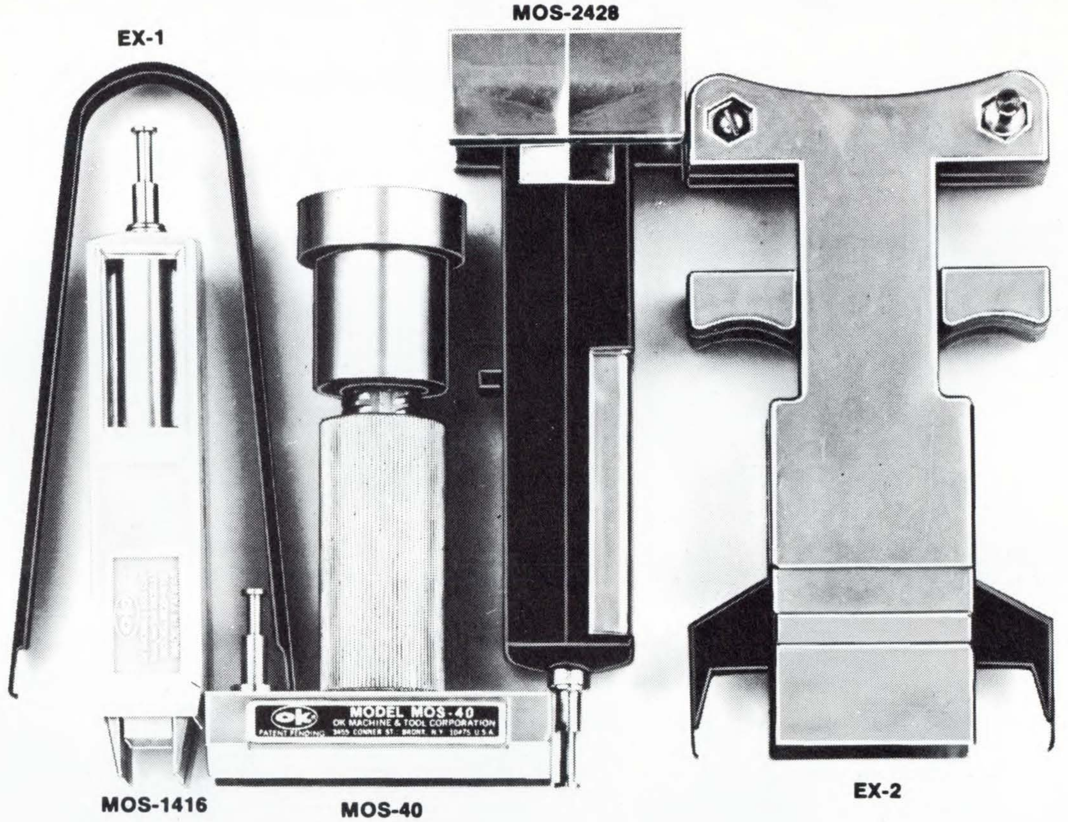
# IC INSERTION/EXTRACTION KIT

**KIT INCLUDES**

- MOS-1416 14-16 CMOS SAFE INSERTER
- MOS-2428 24-28 CMOS SAFE INSERTER
- MOS-40 36-40 CMOS SAFE INSERTER
- EX-1 14-16 EXTRACTOR
- EX-2 24-40 CMOS SAFE EXTRACTOR

**OK MACHINE & TOOL CORPORATION**
3455 CONNER ST., BRONX, N.Y. 10475 U.S.A.
PHONE (212) 994-6600 TELEX NO 125091

PRINTED IN U.S.A. PATENT PENDING




| | | |
|---|---|---|
| WK-7 | COMPLETE IC INSERTER/EXTRACTOR KIT | $29.95 |

INDIVIDUAL COMPONENTS

| | | |
|---|---|---|
| MOS-1416 | 14-16 PIN MOS CMOS SAFE INSERTER | $ 7.95 |
| MOS-2428 | 24-28 PIN MOS CMOS SAFE INSERTER | $ 7.95 |
| MOS-40 | 36-40 PIN MOS CMOS SAFE INSERTER | $ 7.95 |
| EX-1 | 14-16 PIN EXTRACTOR TOOL | $ 1.49 |
| EX-2 | 24-40 PIN CMOS SAFE EXTRACTOR TOOL | $ 7.95 |

*MINIMUM BILLING $25.00. ADD SHIPPING CHARGE $2.00. NEW YORK RESIDENTS ADD APPLICABLE TAX.*

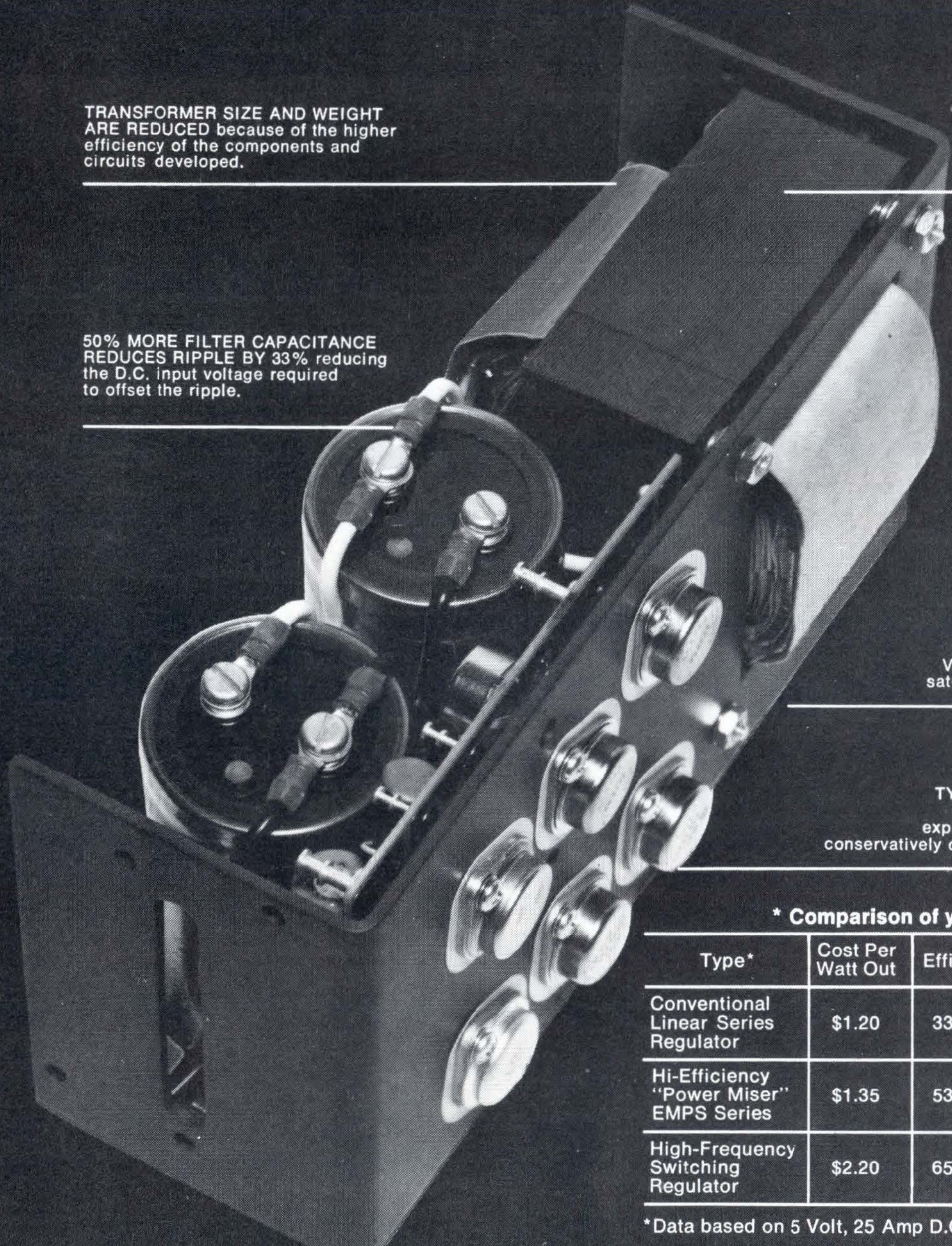
**OK MACHINE & TOOL CORPORATION 3455 CONNER ST., BRONX, N.Y. 10475 (212) 994-6600/TELEX 125091**

**Circle 41 on the Reader Inquiry Card**

# 'Power Misers':

# Adtech Power's new high efficiency linear DC Power Supplies.

## 30-40% more efficient and 30-45% smaller than series regulators.. half the cost of less reliable switchers!



TRANSFORMER SIZE AND WEIGHT ARE REDUCED because of the higher efficiency of the components and circuits developed.

TRANSFORMER LOSSES HAVE BEEN REDUCED 13% through the use of higher grade steel and square copper magnet wire.

50% MORE FILTER CAPACITANCE REDUCES RIPPLE BY 33% reducing the D.C. input voltage required to offset the ripple.

THE EMPS 5-18 (5V/18A) PICTURED IS THE SAME SIZE AS A CONVENTIONAL 5V/12A SERIES REGULATED UNIT.

HIGHER POWER, LOWER SATURATION VOLTAGE SERIES TRANSISTORS reduce saturation voltage drop dissipation by 40%.

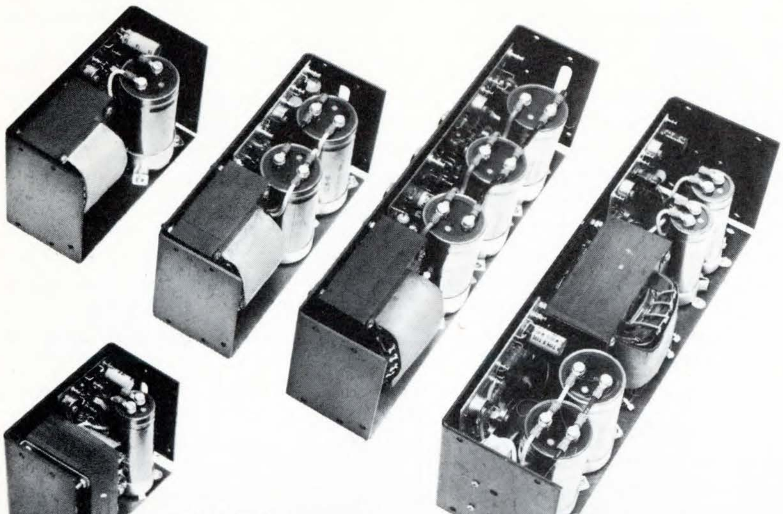
TYPICAL RECTIFIER LOSSES OF 20-25% ARE REDUCED 50% by the use of more expensive, high powered Schottky rectifiers conservatively derated 50% in both current and voltage.

*** Comparison of your three alternatives.**

| Type* | Cost Per Watt Out | Efficiency | Volume Per Watt Out | Power Density Per Watt Out |
|---|---|---|---|---|
| Conventional Linear Series Regulator | $1.20 | 33-43% | 3.74 Cu. In./W. | 0.27 W/Cu. In. |
| Hi-Efficiency "Power Miser" EMPS Series | $1.35 | 53-56% | 1.91 Cu. In./W. | 0.52 W/Cu. In. |
| High-Frequency Switching Regulator | $2.20 | 65-71% | 1.34-1.62 Cu. In./W. | 0.61-0.74 W/Cu. In. |

*Data based on 5 Volt, 25 Amp D.C. Output Rating.

# A complete series of 18 Single Output, Dual Output and Triple Output Microprocessor Models with no EMI problems...an MTBF of 60,000 to 80,000 hours...backed by a 6-year guarantee!



**5V @ 9 Amps to 24V @ 12 Amps.**

### 18 Models/ 7 Configurations

| D.C. RATING | EFFICIENCY | MODEL NO. | POWER SUPPLY PRICES | | | | |
|---|---|---|---|---|---|---|---|
| | | | 1-9 | 10-24 | 25-49 | 50-99 | 100-249 |
| **Single Output Models** | | | | | | | |
| 5V @ 9A | 54% ±2% | EMPS 5-9 | 99.00 | 94.00 | 90.30 | 87.60 | 85.80 |
| 5V @ 12A | 54% ±2% | EMPS 5-12 | 109.00 | 103.55 | 99.40 | 96.40 | 94.50 |
| 5V @ 18A | 54% ±2% | EMPS 5-18 | 135.00 | 127.95 | 122.80 | 119.15 | 116.75 |
| 5V @ 25A | 54% ±2% | EMPS 5-25 | 180.00 | 171.00 | 164.00 | 159.25 | 156.00 |
| 5V @ 40A | 54% ±2% | EMPS 5-40 | 220.00 | 209.00 | 200.60 | 194.60 | 190.00 |
| 12V @ 12A | 59% ±1% | EMPS 12-12 | 170.00 | 161.00 | 154.00 | 149.25 | 146.00 |
| 12V @ 18A | 59% ±1% | EMPS 12-18 | 210.00 | 199.00 | 190.00 | 184.60 | 180.00 |
| 15V @ 11A | 65% ±1% | EMPS 15-11 | 170.00 | 161.00 | 154.00 | 149.25 | 146.00 |
| 15V @ 16A | 65% ±1% | EMPS 15-16 | 210.00 | 199.00 | 190.60 | 184.60 | 180.00 |
| 24V @ 8A | 68% ±1% | EMPS 24-8 | 170.00 | 161.00 | 154.00 | 149.25 | 146.00 |
| 24V @ 12A | 68% ±1% | EMPS 24-12 | 210.00 | 199.00 | 190.60 | 184.60 | 180.00 |
| **Dual Output Models** | | | | | | | |
| ±12V @ 6A | OVER 50% | DEMPS 12-6 | 190.00 | 188.10 | 180.60 | 175.15 | 171.65 |
| ±15V @ 5.5A | OVER 50% | DEMPS 15-5.5 | 190.00 | 188.10 | 180.60 | 175.15 | 171.65 |
| **Triple Output Microprocessor Models** | | | | | | | |
| 5V @ 12A ±12V @ 2A | OVER 50% | TEMPS-3 | 185.00 | 175.75 | 168.70 | 163.65 | 160.40 |
| 5V @ 18A ±12V @ 3A | OVER 50% | TEMPS-4 | 230.00 | 218.50 | 209.75 | 203.50 | 199.40 |

*For ±15V add "-2" suffix to model no.
Overvoltage protection standard on TEMPS-3 & 4, 5V. output

## Specifications: All Models

**A.C. Input:**
5 V.D.C. OUTPUT UNITS: 105-125 Vac. 47-440Hz (derate 10% for 50Hz operation)
ALL OTHERS: 105-125/210-250 Vac, 47/440Hz

**Extended A.C. Input:** 100-130 Vac (derate 20%)

**D.C. Outputs:** See Tabulation of Models

**Control:** ± 5% Voltage Adjustment (Screwdriver adjust pot.)

**Regulation:** ± 0.05% Line or Load

**Remote Sensing:**
Standard on all models, (includes open sense lead protection.)

**Ripple:** 5mV Peak to Peak

**Reserve Power:**
+5% of output available for external load line drop on 5V. and 12V. units; +0.6V. on all others.

**Temperature Coefficient:** 0.02%/°C.

**Stability:**
±0.1% for 24 hour period after 30 minute warmup

**Overshoot:**
No turn-on, turn-off or power failure overshoots.

**Transient Response:**
Output recovers to regulation band within 50 microseconds after an instantaneous load change of 50 to 100%.

**Operating Temperature:**
-25° to +70°C. (derate linearly above +50°C. to 40% at +70°C.; derate linearly below -5°C. to 70% at -25°C.)

**Cooling:**
Convection cooled for full power rating at 50°C. ambient. Forced air cooling extends full power rating to 60°C.

**Protection:**
Overload and short circuits: Automatic recovery foldback current limiting fully protects against overloads and short circuits.
Reverse Polarity Protection: Prevents damage from reverse voltage swings.
Inductive Load Protection: Prevents damage due to inductive voltage swings.

**Overvoltage:**
Optional crowbar overvoltage protection. (Standard on 5V. output TEMPS)

**Transformer:**
Electrostatically shielded for better line noise immunity.

**All Models Meet U.L. Recognition Requirements.**

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**California,** Anaheim
Phone: (714) 634-9211

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**California,** Los Gatos
Phone: (408) 354-6496

**California,** San Diego
Phone: (714) 560-1009

**Colorado,** Denver
Phone: (303) 688-4154

**Connecticut,** Meriden
Phone: (203) 237-9232

**Florida,** Coral Springs
Phone: (305) 752-7520

**Florida,** Largo
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**Georgia,** Atlanta
Phone: (404) 233-6679
(404) 981-9753

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**Washington, D.C.**
Phone: (202) 363-9417

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Phone: (414) 527-1500

ADTECH POWER

**Europe:** ADTECH INTERNATIONAL, Subsidiary of Adtech Power, 46 BD, Roger Salengro, 78200 Mantes La Ville, France. Tel. 4775301+
DISTRIBUTORS: Call Kathy Nelson, Distributor Products Group, (714) 634-9211, for the name of a distributor near you.

**Power Misers are also manufactured in Europe.**

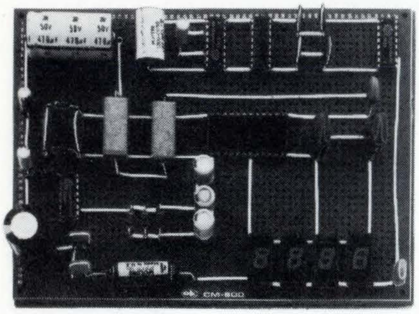
ADTECH POWER, INC., 1621 S. SINCLAIR ST., ANAHEIM, CA 92806. (714) 634-9211 ● TELEX 68-1498

**Circle 64 on Reader Inquiry Card**

## New Products

**CMOS MONOCHIPS.** Convert your discrete designs to space- and weight-saving custom ICs. Designing a digital CMOS Monochip is easy; you don't need previous IC design experience. You need your circuit logic diagram and CMOS Design Manual. You get 200X layout sheets, transparent overlays allowing you to connect most common digital functions and personalized applications engineering. **Interdesign Inc.**, 1255 Reamwood Ave., Sunnyvale, CA 94086. **Circle 267**

**SOLDERLESS PROTOTYPE BOARD** CM-600, a system for solderless construction of circuit prototypes, is a neoprene board 4 1/2" x 6" with 2280 holes on 0.100" centers. Std. components including DIPs are mounted by simply inserting leads into the holes in the long life neoprene material. **O.K. Machine and Tool Corp.**, 3455 Conner St., Bronx, NY 10475. **Circle 189**



**FLAT-CABLE CONNECTOR** doubles signal density, maximizes board real estate. This selective grounding (SG Series) flat-cable IDC connector assembly and header system doubles the number of I/O signal connections with the same PC board real estate as conventional signal header-connector pair. It allows any combination of signal-ground assignments. It eliminates paddle boards, lowers PCB costs and reduces space requirements of both cable runs and board mounted mating headers. **Augat Inc**, 33 Perry Ave., P.O. Box 779, Attleboro, MA 02703. **Circle 155**

**8089 ASSEMBLER SUPPORT PACKAGE**, contains an assembler (ASM 89) that eases the programming task, as well as a set of software development utilities which aid in integrating an 8089 into an 8086 or 8088 multiprocessor system program. The 8089 assembler produces relocatable object (machine code) modules in the same format as the 8086/8088 translators: ASM 86 and PL/M 86. The LINK86 utility program combines relocatable object modules produced by any of the 8086 family language translators (ASM 86, PL/M 86 or ASM 89) and resolves references between the modules. The LOC86 utility assigns absolute memory addresses to these relocatable object modules. $1500. **Intel Corp.**, 3065 Bowers Ave., Santa Clara, CA 95051. **Circle 186**

**DISTRIBUTED DATABASES.** This two-volume state of the art report pursues the technological and operational problems of designing and managing distributed databases. It presents the rationale for these systems, identifying key technological problems in design, and assessing current advances as they are likely to impact the user. $295. **Auerbach Publishers Inc.**, 6560 N. Park Dr., Pennsauken, NJ 08109. **Circle 145**

**PROGRAMMABLE PERIPHERAL INTERFACE** (PPI), general purpose I/O chip features three 8-bit ports (24 I/O pins) that can be individually programmed to function as input, output or bidirectional ports. Interface with a $\mu$P is accomplished through an 8-bit bidirectional data bus. Although designed for use in 2650-based systems, the 2655 is said to be easily interfaced to all other $\mu$P. **Signetics**, 811 E. Arques Ave., Sunnyvale, CA 94086. **Circle 135**

**INTELLIGENT PLOTTER CONTROLLER**, Model IF-751, is designed to drive an incremental plotter, and remove the computational burden from a host computer. Microprocessor based, it can generate, scale and rotate 96 ASCII characters from memory and can product slant and mirror lettering. Built-in capabilities include vector and arc generation, curve smoothing, self test, speed control, and operator selected windowing and zero references. $4400. **Data Technology, Inc.**, 4 Gill St., Woburn, MA 01801. **Circle 142**

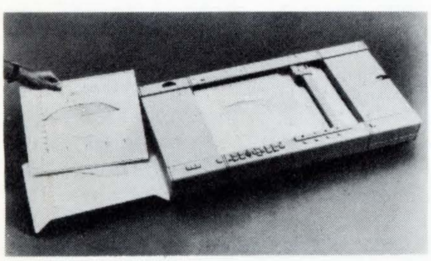
**FLOPPY DISK CONTROLLERS** interface directly with a variety of standard and mini-sized floppy disk drives, and can control up to four single- or two double-sided floppy drives. BLC-8201 is a single board replacement for Intel's two board SBC 201 and requires 71% less power. The BLC-8221 has buffered data transfer for system efficiency. Both boards are Multibus compatible. Their design allows multiple controller boards to be used, and for the boards to have multiple master CPUs. $995. **National Semiconductor**, 2900 Semiconductor Dr., Santa Clara, CA 95051. **Circle 134**

**LINE PRINTER INTERFACES.** Transparent to the host computer, the MDB controller is completely compatible with diagnostics, drivers and operating systems. Operation and programming are exactly as described by the host computer manufacturer. More than three dozen computer-to-printer controller combinations are now available from MDB. In addition, printers which emulate the Centronics, Dataproducts, or Data Printer interface specifications are fully compatible with MDB line printer controllers. **MDB Systems, Inc.**, 1995 N. Batavia St., Orange, CA 92665.

**Circle 130**

**MULTIBUS MEMORY.** The iSBC-compatible memory is compatible with iSBC Multibus, Extended Multibus, Multiprocessor Operation and Series II Development Systems. It's available in ten memory sizes – 16K, 32K, 48K, 64K, 96K, 128K, 192K, 256K, 384K, 512K bytes. It accommodates both 8-bit byte and 16-bit word transfers. Available models include: memory only, memory with parity and memory with error correction and error indicators (LEDs). **Mupro Inc**, 424 Oakmead Pkwy, Sunnyvale, CA 94086. **Circle 196**

**4/C FLATBED PLOTTERS.** Three 4-color graphics plotters (Models 7220S, 7221S, 9872S, 9872B) now have automatic paper advance for unattended plotting applications which include: (1) repetitive/sequential graphics output, (2) unattended graphics at a central computer site and (3) multiple copies of presentation quality graphs.



7221S, $6,750; 7220S, $6,750; 9872S, $6,500; paper advance upgrade on 7221A/9872A, $2,750. **Hewlett-Packard Co**, 1507 Page Mill Road, Palo Alto, CA 94304. **Circle 179**

**INTELLIGENT VDTs.** Model 2404 Intelligent Terminals contain a 9″ CRT display, a 4″ rotary printer, a mag card reader and a detached, user-definable keyboard. Rotary printers include a new highlighting feature giving the printer a dual intensity capability. An IBM 3275 emulation is complete; a modified version of the BSC Contention Mode protocol has been developed and initial production has begun. It offers ease of customization and expansion. **SCI Systems, Inc.**, 8600 S. Memorial Pkwy., Box 4000, Huntsville, AL 35802. **Circle 185**

**RASTER-SCAN DISPLAY.** Employing a monitor control module that can handle up to 8 memory planes and display 256 different colors from a selection of 4096 tones, the GCT-3500 1,048,576 pixel resolution computer-based color graphics system offers clarity and concise color delineation. It is available with 19″ or 25″ high-resolution color CRT monitors. The PGP provides 150 ns internal cycle time high-speed data manipulation, has a 55 mnemonic instruction set, offers selective erase, DMA data transfer from a host computer and flicker-free operation. $25K. **Genisco Computers**, 17805 Sky Park Circle Dr., Irvine, CA 92714. **Circle 187**

**RELAY MUX A/D PERIPHERALS** for SBC-80 μCs, features 8 or 16 differential A/D channels using a "Flying Capacitor" relay multiplexer for high common mode noise rejection (126 dB) and high isolation (±250 RMS). It has complete hard and software compatibility to Multibus and SBC-Series micros. Uses identical programming and register assignments to SBC-711/732, and ST-711/732 A/D-D/A boards. ST-71 RLY16D (16 channels), $995. **Datel Systems, Inc**, 11 Cabot Blvd, Mansfield, MA 02048. **Circle 252**

**SEMIDISK FOR PDP-11.** Semiconductor disk subsystem to its DEC OEM/End-User compatible product line, the CMI-05 SemiDisk is a direct replacement for RK-05 Disk and is compatible with DEC software supporting RK-11 Disk systems. The CMI-05 SemiDisk provides users with significantly increased PDP-11 system performance. **Cambridge Memories, Inc**, 360 Second Ave, Waltham, MA 02154. **Circle 253**

**RT-11 EMULATION UNDER UNIX.** With RT/EMT, any UNIX system can execute RT-11 binary programs. It is able to handle most RT-11 programs: for instance, MACRO, LINK, FORTRAN, TECO. RT/EMT runs in user mode, and allows RT-11 software to be developed and tested in a sophisticated timesharing environment. RT/-EMT is available for a one-time license fee of $1350. (Includes complete source code and extensive documentation.) RT/EMT purchasers must already be licensed to use both UNIX and RT-11. **Human Computing Resources**, 10 St. Mary St, Suite 401, Toronto, Ontario M4Y 1P9, Canada.

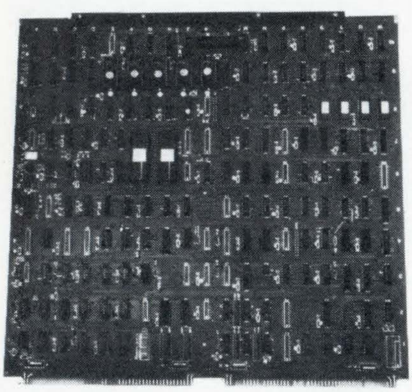
**Circle 269**

**VIDEO DISPLAY DRIVERS.** The VRQ-11, a compatible family of direct–access video display drivers, spans the entire DEC LSI-11/PDP-11 line. They are the VRU-11/XX and VRQ-11/XX. Their programmability, alphagraphic operation, and high speed are key features for a growing market segment. **Computer Technology**, 3014 Lakeshore Ave, Oakland, CA 94610. **Circle 254**

# New Products

**CARTRIDGE DISK/NEW SOFTWARE.** To give μC development engineers greater performance and program capacity, this software and cartridge disk drive combined into its latest development system, the Intellec Series-II Model 240. Hardware speed has doubled, but overall system performance has increased many times, as the cartridge disk subsystem on Intel's new Intellec Series-II Model 240 Microcomputer Development System markedly reduces operator disk-swapping during development of large programs. The two-disk system – one nonremovable, and one removable IBM 5440-type – stores 7.3 megabytes of data. Its faster speed reduces average latency time from 340 ms in previous systems to only 50.2 ms. $22k. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051. **Circle 260**

**NOVA DISK CONTROLLER.** Used in a std. emulation format, the single-board Garnet will support up to four 10-Mbyte disk drives in a daisy-chain configuration and features a full 1K-



word buffer. Garnet is a fully featured emulation of the Data General 10-Mbyte 6045 Disk system controller. It uses a 2901-bit slice processor for its expanded control capabilities and plugs into a Nova or Eclipse std. I/O slot with existing wiring and cable and is fully software compatible, including diagnostics. $9250. **System Industries,** 525 Oakmead Pkwy., Box 9025, Sunnyvale, CA 94086. **Circle 182**

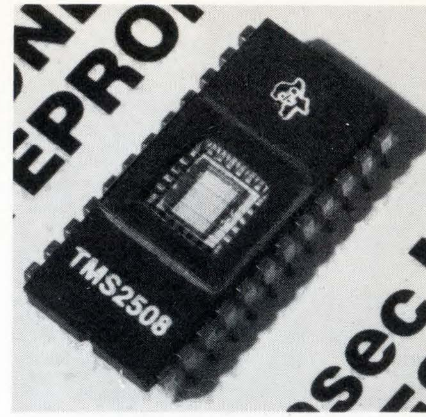
**FFT PIPELINE PROCESSOR.** SPS-1000 FFT Pipeline Processor offers 1000 times higher thruput than conventional computers and 5 to 10 times price/performance improvement over conventional Array Processors. Its effective computation time for a 1024 complex FFT can be as low as 310 μs for a single pipeline configuration or 77μs for a quadruple pipeline. This compares with 3 ms for today's highest performance commercial Array Processor. Arithmetic word lengths are 8, 16, 24 and 32 bits, and single pipeline speeds reach 3.3 million complex words/sec. Speeds can be further doubled, quadrupled and so on by adding parallel combinations of the same modules. $50K. **Signal Processing Systems, Inc**, 223 Crescent St, Waltham, MA 02154. **Circle 156**

**MODEM.** The FCC-Registered 1200 bps, switches network modem GDC 202S offers built in diagnostics for simplified fault isolation and minimal downtime. It's compatible with less expensive 500 or 502 series phones. It can be configured for use with phone or for answer-only operation. $475. **General DataComm Industries, Inc**, One Kennedy Ave., Danbury, CT 06810. **Circle 154**

**C COMPILER 8080/Z80.** Whitesmiths' C produces faster code than PASCAL with more extensive facilities, and has over 75 functions for performing I/O, string manipulation and storage allocation. It conforms to the full UNIX version 7 implementation. The compiler output is in A-Natural source, translatable to Microsoft MACRO-80 assembler source. A-Natural, supplied with Whitesmiths' C, is also available as a standalone package for $330 ($15 for the manual alone). **Lifeboat Associates,** 2248 Broadway, New York, NY 10024. **Circle 251**

**10W SWITCHERS.** These MP (single output) and CMP (dual output), cigarette-sized packaged (1-1/8" x 2-3/4" x 3-3/4") switchers are physically similar to encapsulated non-repairable suppy modules. The MP and CMP are fully accessible, repairable units with two-piece aluminum housing for protection and EMI shielding. Voltage is adj. over a ±10% range with an externally-accessible trimmer pot. MP ratings: 5V, 2.0A; 9V, 1.1A; 12V, 1.0A; 15V, 0.8A. These mini supplies operate with 73% (MP) or 75% (CMP) efficiency. **Kepco, Inc**, 131-38 Sanford Ave, Flushing, NY 11352. **Circle 230**

**LSI-11 SMD DISK CONTROLLER** interfaces any two removable media or Winchester drives and cuts cost/-space/power requirements 40-50%. Quad-size Model DQ-200 controller has soft sector format which provides up to 20% more disk storage through variable sector size and number of sectors/track for highest utilization of disc storage and more convenient data base structure. Soft sectoring also offers up to 992 bytes/sector, different sector sizes on different tracks, write protect, and "bad media" flagging on a sector-by-sector basis. **Distributed Logic Corp,** 12800-G Garden Grove Blvd, Garden Grove, CA 92643. **Circle 238**




**8K EPROM.** With a max. access time of 250 ns, TMS2508-25 is believed to be the fastest EPROM available. The 24-pin ceramic DIP requires only a single 5V supply and is also pin compatible with the other family members. It features automatic chip-select/power down, low power-dissipation and fully static operation. Data stored is UV-erasable and can be programmed singly or in blocks, sequentially or at random. TMS2508-25, $36.90; TMS2508-30, $30.80 (100). **Texas Instruments Inc.,** MOS Memory Div., Box 1443, M/S 6955, Houston, TX 77001. **Circle 190**

**PATCH MODULE.** Model 8502-P Quick Connect/Disconnect Patch Module to the expanding line of Series 8500 MiniTech Modules is connected in series between the Data Terminal Equipment and the Data Communication Equipment for switching, patching, and monitoring all 25 lines of the modem-terminal interface. $70. **International Data Sciences, Inc,** 7 Wellington Rd., Lincoln, RI 02865. **Circle 159**

**DATA COMMUNICATIONS MODULE.** Visual display of key signals on any RS-232C communications line provides simplified techniques to allow unskilled operators to locate and isolate modem or terminal problems. Model 40 derives its power from the signal line and features constant current drivers for the displays so that each display only requires 3 mA over the EIA range of +3V to +25V. In addition to the eight visual displays the Model 40 features 25 test points that breakout the data communications cable. $85. **Remark International,** 4 Sycamore Dr, Woodbury, NY 11797. **Circle 258**

**SMALL TERMINAL.** The Sprint 100 Order Entry Terminal, a 4K terminal, is small, light and easy to operate. Barely 6.5" long and weighing 13 oz, this pocket-size terminal features a large color-coded keypad and a big 12-char. alphanumeric display. $495. **Norand Computer Systems,** 550 Second Street SE, Cedar Rapids, IA 52401. **Circle 294**

**INTERFACE PANEL** Model 56-11446-1 simplifies data acquisition wiring. Why hand solder and wire those connectors located on the back of rack mounted devices? Instead, the Interface Panel (IP) brings these pins out to a front panel located on a rack mount in the form of 2 rows of 25 screw-on terminals. This is done by joining the connector and IP with ribbon cable and connector. 19"L x 3.47"H x 0.5"D. $195. **Datel Systems, Inc,** 11 Cabot Blvd., Mansfield, MA 02048. **Circle 147**

**12-BIT DAC.** DAC863, a complete 12-bit current-output DAC (with internal reference), is pin-compatible with "563"-type converters. Its nonlinearity is as low as ±1/4LSB; gain drift is ±5ppm/°C max and bipolar offset drift is just ±4ppm/°C. $29 (100). **Burr-Brown,** Box 11400, Tucson, AZ 85734. **Circle 148**

**PROGRAMMABLE DIGITAL PRINTER.** Model 2000 operates with any IDS modem test set to provide a permanent record of bit error rate tests (BERT). Features of the IDS printer include a presettable real time clock, seven selectable trigger channels, and three print routines. Trigger channels A through G are labeled Clock Lost, Data Error, Sync Recovered, Sync Lost, Counter Overflow, External, and Time, respectively. 16"W x 5 1/4"H x 12"D; 19 lbs. $3,325. **International Data Sciences, Inc.,** 7 Wellington Rd., Lincoln, RI 02865. **Circle 149**

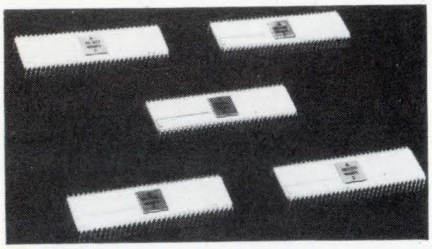
**QUAD LINE DRIVER** with NAND-enabled 3-state outputs is intended for digital data transmission over balanced lines. It 2nd-sources the AM26LS31, meeting all requirements of EIA Stnd. RS-422 and Fed. Stnd. 1020. It meets full $V_O$=6.0V, $V_{CC}$= OV, $I_O < 100\mu A$ RS-422 driver requirements. Plastic, $2.25; ceramic, $2.50. **Motorola Semiconductor Products, Inc,** Box 20912, Phoenix, AZ 85036. **Circle 151**

**COLOR DISPLAY.** Applicable as graphics terminals, peripherals or frame buffers, the Light 50 Color Display combines generic graphics and image strengths with dynamic color capacity. The family offers a multi-processor, multi-bus architecture for unparalleled flexibility, combined with specific function hardware for rational task allocation. Multiple video outputs are provided for red/-grn/blu or composite video as well as sync and subcarrier in and out for external synchronization. An inherent color look-up table facilitates color changes. Scrolling and scaling are contained in the basic hardware. Overlay is provided for separate text or dynamic annotation. Up to 4 independent image outputs may be accommodated with up to 2K by 2K image space with 512 by 512 windowing. **Applied Dynamics International,** 3800 Stone School Rd., Ann Arbor, MI 48104. **Circle 150**

**VIDEO DIGITIZER** allows display/-storage of computer-generated images. For S-100 bus computers, it converts output from the camera or other source of composite video into 8-bit gray scale digital information. Data can be transferred via software to either a memory-mapped high resolution video board or to main memory for subsequent retrieval. A complete driver program, implementing 16 shades of gray, is included for controlling the board, displaying images on a high-resolution video board, storing images on disk and printing images on a matrix printer. Max. horiz. resolution, 700 points/line; vert. resolution, 480 lines/image. $175. **Vector Graphic Inc.,** 31364 Via Colinas, Westlake Village, CA 91361. **Circle 152**

# New Products

**SUPER 4-BIT $\mu$C.** The MN1500 Series family includes 4 single-chip micros, an Evaluator chip (MN1599) and an I/O Expander chip (MN1599). Two micros (MN1542 and MN1544) come in 40-pin plastic DIPs; MN1562, in a 64-pin plastic DIP; MN1564, in a 64-pin ceramic DIP. The family is fully



backed up in depth by an array of software/hardware development tools. The instruction speed is 2 $\mu$s. Most processing is performed in bytes. On-chip ROM is 2 or 4k bytes, with 6 or 12 bidirectional I/O ports for greater flexibility in assigning I/O. **Panosonic,** One Panosonic Way, Secaucus, NJ 07094. **Circle 191**

**6502 DEVELOPMENT SYSTEM** 6502 PDS features the CGRS 6502/S100 MPU Board. Additional boards in this multi-card computer consist of: the CGRS multiple-I/O board, S100 disk controller board and 16K RAM board. All boards are mounted in a 10-slot S-100 mainframe. It comes with dual minifloppy (5") or dual full size (8") floppy disks. Minifloppy systems, $2500? full-size floppy system, $3300. **CGRS Microtech,** Box 368, Southhampton, PA 18966. **Circle 160**

**EDP SUPPLIERS.** This year's 204-pg. "Datapro Directory of EDP Suppliers" helps choose vendors by publishing standardized entries describing each company's location, size, management, financial status, product line and sales and service organization. These facts are arranged in a comparison chart format that permits quick references and direct comparisons. $24. **Datapro Research Corp.,** 1805 Underwood Blvd., Delran, NJ 08075. **Circle 146**

**PRINT WHEELS** for use with Qume and Diablo WP/dp printers are made from high-tensile-strength plastic and are used with printers achieving speeds up to 55 cps. All have a metal cap on the period to maintain print quality throughout wheel life. **National,** One Water St., Holyoke, MA 01040. **Circle 226**

**IBM-COMPATIBLE DISKETTES.** Off-the-shelf delivery of a complete line of IBM-compatible diskettes for users of IBM System/32, S/34, Series 1, 5110, and OS-6 WP systems and OEM equivalent drives includes one-sided/single density (equivalent to IBM Diskette 1), two-sided/single density (IBM Diskette 2), and two-sided/double density (IBM Diskette 2D). Diskettes are totally interchangeable. 3740/1, $4.25; 3740/2, $5.25; 3740/2D, $6.25 (10). **Dysan Corp.,** 5440 Patrick Henry Dr., Santa Clara, CA 95050. **Circle 228**

**IMPACT PRINTERS.** Two models, plug-compatible with IBM 3287 printers, can be attached to the Telex TC 276, the recently-introduced plug-compatible replacement for the IBM 3276; IBM 3276, which controls up to 8 operator stations; or IBM 3274, which controls up to 32 devices. TC 286B Model 1 and 2 are fully-formed char. printers containing "daisy wheel" print elements. Model 1 operates at 45 cps. Model 2, designated for ATMS applications, operates at 40 cps. Both operate up to 70 cps by using a look ahead feature. **Telex Corp,** 6422 East 41st St., Tulsa, OK 74135. **Circle 157**

**COMPUTER SYSTEMS.** Three product families are the entry-level 100 with 192KB memory, expandable to 768KB; the 500 with 192KB memory, expandable to 3MB; and the top-of-the-line Harris 800 with 384KB memory, expandable to 3MB. The Harris 100 supports 6MB of virtual memory, while the 500 and 800 both support 12MB of virtual memory. 1920KB, $28,800. **Harris Corp,** 2101 W. Cypress Creek Rd, Fort Lauderdale, FL 33309. **Circle 261**

**COLOR GRAPHICS TERMINAL** MCD 4001 can communicate like a TTY compatible WP, interactive semi-graphics process control or full-graphics analytical terminal. Applications range from simple-output-only terminals through clustered terminals for network and process control. Features include 8-color foreground and background, 80 large or small char/line, 24 or 48 lines/page, modular hardware/firmware architecture, 3 display generators/chassis option, RS-232C, 20mA current loop (TTY) and parallel DMA interfaces, RS-170 RGB and monochrome video output, full graphics overlay and underlay option, and floppy disk and printer interface option. **The Telecrafters Corp,** 999 Pieffers Lane, Harrisburg, PA 17109. **Circle 262**

**BAR CODE READER** option for Model 1206 Miniterm the 1206/BCR, includes bar code reader option and allows personnel with no special training to enter Code 39 alphanumeric information via a hand-held wand in a variety of point-of-transaction and data collection applications. **Computer Devices, Inc.,** 25 North Ave., Burlington, MA 01803. **Circle 158**

**SOFTWARE CLEARINGHOUSE.** Who can you sell your software to? Where can you buy the software you need? This service helps you "market" your software, helps you "locate" needed software, advertises nationally through magazines, newspapers and direct mail to software and system houses, and management consultants. Potential buyers of your software get your name, address and phone number. **Software Clearinghouse,** 2030 E. Fourth St., Suite 153, Santa Ana, CA 92705. **Circle 227**

**$\mu$P COMPONENT LINE.** The GL868 line permits purchase of modules for do-it-yourself design and assembly of $\mu$C systems. The 6800-based line includes: $\mu$C, analog I/Os, servo-positioning modules, CRT modules for video display, RAM, EPROM, CMOS with battery backup, software packages and development centers, nest and supply assemblies. **Giddings & Lewis Electronics,** 1 E. Wacker Dr, Chicago, IL 60601. **Circle 233**

**Z80/8085 SYSTEM ANALYZERS.** M824 (Z80) and M825 (8085) system analyzers, self-contained units, connect to a system micro via a single-DIP clip or low-profile plug-in connector. Includes address interrupt, trigger enable, Nth pass, address plus N instruction, hold or refresh, and binary data displays, address display and 8 LED status displays. $1590 ea. **PRO-LOG,** 2411 Garden Rd, Monterey, CA 93940. **Circle 234**

**FIBER OPTIC KIT** includes: fiber optic infrared source (LED), MFOE103 FB; integrated detector/preamplifier, MFOD402FB; lm length of fiber optic glass cable, terminated with appropriate matching AMP connectors. In addition to the emitter (MFOE103FB) and


detector (MFOD402FB) included, Motorola offers 5 additional ferrule semiconductors. Price for the "The Link" kit is $99 (unit qty). **Motorola Semiconductor Products, Inc,** Box 20912, Phoenix, AZ 85036. **Circle 177**

**LED MOUNT.** By combining P-C-LITE with CLIPLITE, this assembly allows either vert. or horiz. mounting of stnd. T1 3/4 LED to a PCB. This results in a securely mounted device with a lens at a standard height compatible with other PC-mounted switches and components. It eliminates hard wiring to the panel, yet allows lens to be flush-mounted, recessed or extended through panel for visibility. $0.24 (1k). **Visual Communications Co**, Box 986, El Segundo, CA 90245. **Circle 236**

**I/O SYSTEM.** Teledyne 674, compatible with most μP systems, has ac and dc I/O modules and a mounting track containing integral interconnect wiring. Output rating for ac output modules is 4A, 250 Vrms; for dc modules, 3A, to 250 Vdc. $8.05 (1k). **Teledyne Relays,** 12525 Daphne Ave., Hawthorne, CA 90250.
**Circle 237**

**6089 OPERATING SYSTEM** uses structured programming for easy hardware adaptability and command expansion. This 6809 OS is for Percom's SS-50 bus-compatible 6809 control computer and other 6809 MPU systems. The 1K PSYMON (Percom SYStem MONitor), includes 8 monitor-type commands and 15 callable utilities. Its power lies in its command extensibility and adaptibility to any hardware environment. EPROM version for SBC/9, $39.95; versions for other systems, $69.95. PSYMON program listing, $9.95. **Percom Data Co,** 211 N. Kirby St., Garland, TX 75042.
**Circle 224**

**64K RAM BOARD,** RAM-064, is fully compatible with Intel's iSBC-80 Multibus. It contains 64k of Dynamic RAM and a 450 ns memory access time. RAM-064 is warranted for 3 yrs. $1850 (1-9); $1665 (10-24). **Electronic Solutions, Inc,** 5780 Chesapeake Ct, San Diego, CA 92123.
**Circle 229**

**MC68000 DESIGN MODULE** (MEX 68KDM), when used in a Motorola EXORciser, offers a development for the design of MC68000-based systems; or, when used "standalone" with a power supply and suitable peripherals, represents an elaborate μC with on-board software development and debug capability. $1795. **Motorola Semiconductor Products, Inc.,** Box 20912, Phoenix, AZ 85036. **Circle 222**

**LINE PRINTER CONTROLLER** handles any printer up to 500,000 bytes/sec (3700 lpm). The controller board can be plugged directly into any available I/O slot in either 16- or 32-bit Perkin-Elmer/Interdata computers. The module is fully software compatible with both OS/16 and OS/32, and host-supplied diagnostics. Pin-compatible Interdata cables are provided which allow the host-supplied Centronics or Data Printer Interface to be directly replaced by the MACROLINK controller module. Using one-half the power – 0.5 A at 5 V – of host-supplied interfaces, the MACROLINK printer controller also employs connectors with locking hardware to eliminate intermittent connections. $650 complete. **Macrolink,** 1740-E S. Anaheim Blvd., Anaheim, CA 92805.
**Circle 249**

**PDP-11 COMPATIBLE MEMORY** packs 256 kbytes of dynamic NMOS RAM on a single card. The NS11L memory board is compatible with the PDP-11 family operating on stnd., modified or special buses. It's a direct replacement for DEC's MS11 series memories, yet it offers significant price and performance advantages by providing the entire 256K bytes on a single, one-slot hex-wide card. $5750 for the 1/4-megaword configuration. **National Semiconductor Corp.,** M/S 7C-265, 2900 Semiconductor Dr., Santa Clara, CA 95051. **Circle 223**



**Circle 35 on the Reader Inquiry Card**

# Product Index

Here's how to get product information from ads in this issue. Simply (1) tear out the Reader Inquiry Card, (2) **circle** the numbers listed for those subjects you're interested in and (3) mail it to *Digital Design*.

**PERQ COMPUTER** System provides the computing facilities a single user needs, including a microprogrammed CPU which executes 1 million Pascal P-Codes/sec, a quarter megabyte of memory with a 32-bit virtual address, a 12-megabyte disk, high resolution interactive graphics display, keyboard, touch tablet and speech output. PERQ systems can be interconnected on Three Rivers "Packet Stream" local network which uses packet broadcast protocols at 10 million bits/sec on a multi drop coaxial cable. The video display, which is vertically oriented like a piece of paper (8 1/2 x 11") provides resolution of 768 x 1024 with 60 Hz non-interlaced, blk-on-wht refresh which displays multiple font, proportionally spaced text as well as complex, flicker free graphics. PERQ systems replace time-shared computers by giving each user his own processor, memory, disk and display. The high band-width packet stream network allows a PERQ system to access data on another PERQ as easily as if it were local. The network also allows access to printers, mag tape drives and other peripherals shared by several users. (CPU, 256K memory, 12M disk, display KB, pointer, speech output, RS-232 and IEEE-488 interfaces), $19.5k; packet stream option, $2k. **Three Rivers Computer Corp,** 160 North Craig St, Pittsburgh, PA 15213. **Circle 240**

**IBM 2780/3780 Emulator,** Model C8000, features a built-in Winchester disk drive. COBOL and the IBM 2780/3780 Emulator have been added, so that the C8000 can compete against minis for small business applications. The 2780/3780 supports C8000 with a simple, fast and reliable exchange of data files with most minicomputers, mainframes or other Onyx systems. Using the industry standard BSC protocol and leased/switched telephone lines, the 3780 permits C8000 to operate in a distributed processing network with a wide variety of computer systems. Emulators, $500 ea. (on st 1/4-inch cartridge tape). **Onyx Systems, Inc,** 10375 Bandley Dr, Cupertino, CA 95014. **Circle 241**

**EXTENDER CARDS** are DEC-compatible, high frequency wire wrappable boards, which includes the dual, quad, quad and hex-size boards (DE2ET, DE4ET, DE6ET). Remaining extender cards fit board series to include the Intel SBC 8010, Zilog Z80 and Motorola 6800MMA-compatible boards. Gold-plated, double-looped test points are on every connection between the card under test and back-plane. $65-$130 (1-4). **Hybricon Corp,** 410 Great Rd, Littleton, MA 01460. **Circle 242**

**IBM-COMPATIBLE DISKETTES** for users of IBM System/32, S/34, Series 1, 5110, and OS-6 wp systems and OEM equivalent drives are formatted and available in one-sided/single density (equivalent to IBM Diskette 1), two-sided/single density (IBM Diskette 2) and two-sided /double density (IBM Diskette 2D) versions. 3470/1 (IBM Diskette 1), $4.25; 3740/2 (IBM Diskette 2), $5.25; 3740/2D (IBM Diskette 2D), $6.25. **Dysan Corp,** 5440 Patrick Henry Dr, Santa Clara, CA 95050. **Circle 243**

**IBM PROTOCOLS** can now be handled by a TRS-80. IBM users can transfer data to a TRS-80, with data then available for special analysis or managerial review. Because the TRS-80 is easily programmed using a resident Basic interpreter, many specialized applications are possible. **Omni Computer Systems, Inc,** 4 W. Lafayette St, Trenton, NJ 08608. **Circle 244**

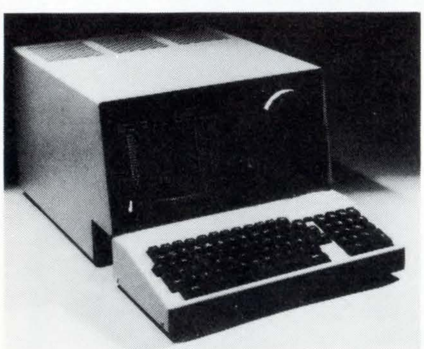
**COMPUTERIZED SERIAL LINE MONITOR,** P1-5 LM, lets the user quickly select the features desired using the monitor keyboard. The unit has a 48K byte buffer which allows the user to page through the last 48,000 characters transmitted. $6,000. **Phone 1, Inc.,** POB 1522, Rockford, IL 61110. **Circle 279**

# New Products

**CRT TERMINAL** ZMS-70 is suited for the "systems house" that wants to serve both the small business and WP markets and is totally software-oriented. It utilizes a list-driven architecture that provides the degree of video flexibility needed in heavy text editing and data base manipulation applications. In its desk-top enclosure, the ZMS-70 houses a $\mu$C system with up to 65K bytes of memory, a 15" diagonal video screen, an extensive "Selectric-styled" keyboard, a telecommunications interface, and a pair of built-in diskettes that supply 143K bytes of on-line storage. **Zentec Corp.**, 2400 Walsh Ave., Santa Clara, CA 95050. **Circle 178**

**ELECTROSTATIC PLOTTING.** Model 130 Interface permits Sperry-Univac (Varian) 620 and V70/V77 computers to use any of 40 Versatec ES printer/plotters. The interface, carried on a single PCB, allows line printing under Sperry-Univac's Vortex I/Vortex II operating system. It supports all standard Versatec printer/plotter options and provides for Program Controlled I/O, Interrupt Initiated I/O (PIM), and DMA (BIC). **Versatec,** 2805 Bowers Ave., Santa Clara, CA 95051. **Circle 181**

**CAPG (COMPUTER-AIDED PROGRAM GENERATOR)** reduces test program generation time down to 30



min. through use of a special software module. It allows interactive compilation of semi device test programs for all Tektronix S-3200 Test Systems. It's possible for a CRT terminal operator to quickly assemble a complete device test program including DC and AC parametric tests starting from an existing functional test pattern. CAPG can generate test programs for digitla SSI, MSI, LSI and VLSI parts. Program listing will appear similar regardless of the device size. Only the pin labels, parameters, and functional pattern will vary. A disc cartridge containing the CAPG program, all documentation on the use of CAPG, and user training cost $5000. **Tektronix, Inc.**, Box 500, Beaverton, OR 97077. **Circle 184**

**PDP-11/34 MEMORY.** The 94134 MOS RAM module is fully compatible with PDP-11/34s and uses either the standard or modified unibus connector. Maximum configuration is 128K x 18, but smaller densities are also available. Refresh is automatic. **Control Data Corp,** Computer Memory Div, 8001 E. Bloomington Freeway, Bloomington, MN 55420. **Circle 200**

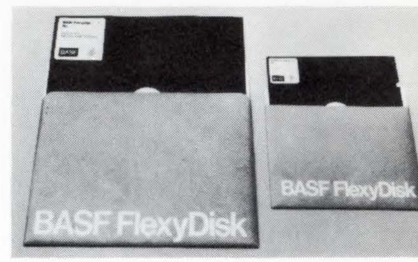
**MC68000 DESIGN MODULE** MEX-68KDM is a means for evaluating and designing with the MC68000. The module permits chip evaluation, using either an EXORciser development system or with an IBM370 or PDP-11, in conjunction with cross computer software. For system emulation, the module includes 32K bytes of RAM, two 16-bit parallel I/O ports, three 16-bit programmable timers, two serial RS-232 ports and 8K bytes of debug ROM. MEX68KDM includes the 16-bit debug tool MACSbug. MEX68-KDM (68000 Design Module with ACIA serial RS-232 cables), $1,795; MEX68KDAP (MC6800 Bus Adapter Board), $100 (1-5). **Motorola Semiconductor Products Inc.**, Box 20912, Phoenix, AZ 85036. **Circle 194**

**8MB MEMORY.** With up to 8Mbytes of memory in a single 15 3/4" chassis to meet disk emulation and main memory requirements, BULK SEMI is compatible with its BULK CORE modules; you can take advantage of the wide range of existing BULK CORE controllers to use BULK SEMI as main memory or in disk emulation systems for DEC, Data General or Interdata minis. The system consists of a controller board and up to 16 Array boards. Error correcting is standard. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512. **Circle 198**

**DISTRIBUTED PROCESSING.** For high-power processing, top-of-the-line XL40 handles up to 16 local and remote terminals. With up to 512K bytes of memory and disk storage expandable to 70 megabytes for local data bases, it can also interactively access your headquarters mainframe via 3270 inquiry mode for non-XL40 resident files. **Pertec Computer Corp,** 12910 Culver Blvd, Box 92300, Los Angeles, CA 92300. **Circle 199**

**IMAGE PROCESSING SYSTEM** performs pipeline arithmetic and image processing functions at video rates in real time. The GMR 270 features 512 x 512 pixel resolution and has up to four banks of 8-bit image memory. It can have up to four overlay memory planes. Complete line drawing vector graphics are provided by a high-speed graphic/alphanumeric generator. The 270 includes a 16 bit parallel, TTL-compatible, bidirectional interface. Plug-compatible DMA parallel interfaces are available for most minis. GMR 270 video output is RS-270-compatible and drives std. TV monitors. **Grinnell Systems,** 2159 Bering Dr., San Jose, CA 95131. **Circle 195**

**DOUBLE-SIDED 5.25" FLOPPY.** This line of double-sided, single and double density 5.25" FlexyDisks are in either soft or hard (10 and 16)-sectored formats. Single-density capacity is 250,000 bytes (unformatted), while double-density capacity is 500,000 bytes at 48 tpi. They are available in soft 5 or 10 packs, Kas-Ette/10 Library Boxes, or bulk packaging of 100




units. Each box contains a supply of write-protect tabs and special labels for coding and filing. $6/diskette. **BASF Systems**, Crosby Dr., Bedford, MA 01730. **Circle 193**

**16-LINE MULTIPLEXER.** DMAX/16, programmable multiplexer for connecting PDP-11 to 16 asynchronous serial communications lines makes the most of the 11's DMA capabilities to establish computer-overhead and level far below that of competitive units. It offers software compatibility with the DH11. You don't need an expansion box or special back planes. DMAX/16 has two hex boards which install easily into standard SPC slots units and connect to the current loop or EIA/RS-232 panel by separate flatribbon cable. As many as 16 can be placed on a single PDP-11 for a total of up to 256. **Able Computer Technology, Inc,** 1751 Langley Ave, Irvine, CA 92714. **Circle 202**

**SB TAPE CONTROLLER.** The 3120 single-board magnetic tape controller controls up to four mag tape drives without additional formatters or adapters. One controller can simultaneously interface IBM-compatible 7-track and ANSI standard 9-track NRZI formats. The 3180 SB mag tape controller interfaces any NOVA mini with up to four unformatted phase encoded (PE) mag tape drives, including Wangco and Pertec. "Edge connector" technique eliminates NOVA back plane wiring. No external formatters or adapters are required. **Ball Computer Products,** 860 E. Arques Ave, Sunnyvale, CA 94086. **Circle 197**

# New Products

**IMS/VS HDAM OPTIMIZER.** Internally Developed Software (AIDS) are a series of software products designed to improve system performance and productivity. The first AIDS product, IMS/VS HDAM Optimizer (for 470 users), improves IMS/VS HDAM data bases' performance. Operating during normal data base reorganization, HDAM Optimizer determines the optimal placement of data for a data base and insures that this placement is used. Because data is optimally placed, fewer I/O operations are required to process it. It reduces I/O requests required to retrieve data by 10-15%. HDAM Optimizer monthly license fee, $225. **Amdahl Corp,** 1250 E. Arques Ave, Box 5070, Sunnyvale, CA 94086. **Circle 255**

**68000 CROSS MACRO ASSEMBLERS** for use with the EXORciser, IBM370 and PDP-11 include M68KOXASMBL2 (370 Version), $1500; M68KOXASMBL3 (PDP-11 Version), $1500; M68KOXASMBL0 (EXORciser, 6800 Version), $990; M68KOXASMBL1 (EXORciser, 6809 Verssion), $990. **Motorola Semiconductor Products Inc,** Box 20912, Phoenix, AZ 85036. **Circle 256**

**NON-VOLATILE MEMORY.** Model 701, for use with Moxon Model 740 Logic Analyzers and Model 720 Data Generators, has a removable, Model 2716 ultraviolet, erasable PROM; UV lamp; and logic to interface the unit to the Moxon line. Data is entered from the KB of either the 740 Logic Analyzer or the 720 Data Generator, in either hexi-decimal, octal or binary format, or even as a serial or parallel timing-diagram. The data is displayed on the built-in CRT, can be edited if required, and then, at the touch of a button, can be stored in the 2716 PROM. $850. **Moxon, Inc,** 2222 Michelson Dr, Irvine, CA 92715. **Circle 257**

**FLOPPY POWER SUPPLY.** The open frame CP340 powers one "Mini-Floppy"-type Floppy Disk drive. DC outputs provided are: +5 @ 0.5/0.7A PK. 2.10"D x 5.5"L x 4"W. Mounts within metal enclosures used for housing one Mini-Floppy plus one supply. $44.95 (1-9). **Power-One, Inc,** Power One Dr, Camarillo, CA 93010. **Circle 239**

**CLOCK/M POWER RESTART.** A plug-in half-board module for Perkin-Elmer/Interdata computers incorporates: (1) precision interval clock and line freq. clock, (2) power fail/auto restart hardware. This U Clock Module combines on a single half-board three functions: precision interval clock, low frequency clock and power fail detect hardware. It's fully compatible with both OS-16 and OS-32 software and host-supplied diagnostics. As a replacement for the P-E M48-000, the Clock Module on a 7" x 15" half-board can be plugged into any available I/O slot of either 16- or 32-bit CPU's. $550. **Macrolink,** 1740-E South Anaheim Blvd., Anaheim, CA 92805. **Circle 270**

**DOUBLE DENSITY FLOPPY** interface board, supplied with Basic I/O System software for CP/M on single-density diskette, permits users to intermix single and double density diskettes. The system automatically determines whether single or double density is in use. As many as four drives can be selected, using either single or double density. $425. **Tarbell Electronics,** 950 Dovlen Pl, Suite B., Carson, CA 90746. **Circle 246**

**PLM/S86,** a superset of Intel's PL/-M86, is the first of a family of high-performance crosscompilers designed to meet the needs of installations where a large number of programmers must generate both quickly and accurately relocateable programs that take advantage of the megabyte address space provided by the new 16-bit μPs. Since PLM/S86 is written in IBM's optimizing PL/I, a user must run on a large IBM compatible system that has facilities for conviently editing, quickly compiling, and syntactically debugging a source program. **SLR Compilers Inc,** 1109-20th St, Suite 6, Santa Monica, CA 90403. **Circle 247**

**NOVA 1200** will execute NOVA 4 instructions with the Model 2010 CPU Option Board. Using the Option Board with existing NOVA 1200 memories also increases NOVA 1200 speed by 25%. If existing memories are replaced by a 32KW Memory Board (also available from Quentin), speed of a NOVA 1200 system can be increased to 800 ns (40%). Lifetime guarantee. $1,800. **Quentin Research, Inc.,** 610 Hawaii St., El Segundo, CA 90245. **Circle 248**

**1802 MEMORY.** CDP18S621V1 16-kbyte RAM, CDP18S623 8-kbyte RAM and CDP18S624 4-kbyte battery-backup RAM modules feature static CMOS and operates from 5V. Current, 11 mA for 18S621V1; 8 mA for 18S623; 13 mA for 18S624. 96-hr memory-retention capability w/o external power. 16-kbyte RAM, $1195; 8-kbyte RAM, $650; 4-kbyte battery-backup RAM, $515. **RCA Solid State Div,** Box 3200, Somerville, NJ 08876. **Circle 235**

**TAPE FORMATTER** Model 9X00F employs a bipolar bit-slice μP to allow signature analysis while improving control and reducing the number of integrated circuits required. It has logic patterns and diagnostic routines programmed into on-board ROMs. Using a signature analyzer, a tech can compare patterns generated by the micro with ROM-based patterns to quickly ascertain malfunctions. MTTR is under one hour. The single-board embedded formatter provides all logic necessary for R/W both 1600 cpi P-E and 800 cpi NRZ-inverted formats for ANSI and IBM compatible tape. $1950. **Kennedy Co,** 1600 So. Shamrock Ave, Monrovia, CA 91016. **Circle 250**

**PDP-11/34A CACHE MEMORY.** This high-speed, 1K word cache memory, PM-KK11A, is a direct replacement for DEC's KK11A and is housed on a single, space-saving hex card which resides next to the CPU. The cache memory provides the necessary interconnect jumper boards for use with or without the floating point option. It captures data from the Unibus during main memory to CPU transfers; this allows the cache to hold data most often required by the program. Typical program behavior is such that the cache will have the required data 85% of the time. Thus, each time the cache hit occurs, a substantial savings of time, 500 ns with MOS memory and 700 ns with core, are realized. $2,984. **Plessey Peripheral Systems,** 17466 Daimler, Irvine, CA 92714. **Circle 263**

**MEMORY INTERFACE IC.** Memory address multiplexer and refresh counter circuit MC3232A is for use with 16-pin, 4K dynamic RAMs (such as MCM4027). In conjunction with the MC3480 memory controller, it accomplishes the entire memory control function in a 2-chip set (plus an external refresh oscillator.) Plastic, $4.70; ceramic, $5.10. **Motorola Semiconductor Products, Inc,** Box 20912, Phoenix, AZ 85036. **Circle 264**

**X.25 SIMULATOR/TESTER** interfaces directly with terminals and front-end processors for testing or operates remotely over full-duplex synch. lines using modems. The console can also be used remotely from the Simulator/Tester via asynch. lines. Packed in its convenient case with both handle and rollers, it can be hand-carried or shipped from installation to installation as required. Principal applications of the Simulator/Tester are to simulate the X.25 network for terminal interface development and to simulate terminal inputs via the X.25 network for testing and debugging of front-end processors. $11,900. **Applied Data Communications,** 14272 Chambers Rd, Tustin, CA 92680. **Circle 266**

**INSTRUMENTATION BUS MODULES.** Designated Micromodules 12 and 12A, these monoboard subsystems are designed to provide a user with all necessary hardware to implement an interface between a $\mu$P (6800) and one or more test instruments in accordance with the IEEE STD 488-1978 bus specification. Micromodule 12A allows the user's system to send/receive data bytes, request service and respond to parallel and serial polls. This module provides the user's system with all of the above capabilities, plus the ability to send commands and conduct parallel/serial polls. Supporting software for M6800-based systems is available on MDOS diskette. Module 12, $795; 12A, $305. **Motorola,** P.O. Box 20912, Phoenix, AZ 85036. **Circle 144**

**LOGIC DEVELOPMENT SYSTEM,** Model 64000, is hard-disk based with multistation architecture for a flexible, high-performance operating system. It helps software and hardware designers in design, debugging, and troubleshooting of $\mu$P-based products. The 64000 handles conventional software development functions (editing, file management, assembling, compiling), real-time, transparent logic analysis. Currently, four microprocessors (Intel 8080, 8085, Motorola 6800, and Zilog Z80) are fully supported with relocating macro assemblers and emulators for real-time emulation at processor speed. **Hewlett-Packard Co.,** 1507 Page Mill Road, Palo Alto, CA 94304. **Circle 133**

**24- and 32-CHANNEL DATA CONCENTRATORS.** The Model 8032 provides 32 channels without interface control signals and is suitable for dedicated terminal applications; the Model 8132 provides 32 channels with interface control signals and permits support of dial-up access to each channel. Models 8024 and 8124 provide the same capabilities for 24 channels. The 8024, $7150; 8124, $7350; 8032,

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**INTELLIGENT CRT TERMINAL** ZMS-50 offers substantial amounts of intelligence in a terminal with limited peripheral capability. Used with a host computer, the unit executes user-written codes and programs within the terminal, relieving the host from constant decision-making. ZMS-50 comes with 4K bytes of RAM; a 16K factory-installed version is available for executing downloaded programs. Also available are a comprehensive text editor, and a form generation package. **Zentec Corp.,** 2400 Walsh Ave., Santa Clara, CA 95050. **Circle 131**

**$\mu$P DEVELOPMENT.** Model 64000 is 20-120MB hard-disk-based with multistation architecture for a flexible, high performance OS. It helps software/hardware designers in design, debugging and troubleshooting. The 64000 handles conventional software development functions (editing, file management, assembling, compiling), real-time emulation of popular microprocessors and real-time, transparent logic analysis. Currently, 4$\mu$Ps (8080, 8085, 6800, Z80) are fully supported with relocating macro assemblers and emulators for real-time emulation at processor speed. From $25k. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304. **Circle 265**



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**GRAPHICS IMAGING.** The RGB-256 card contains a 256 x 4 bit display refresh memory and includes NTSC (American) or PAL (European) color and grey scale encoders which can provide up to 16 shades of colors. The encoders permit the RGB-256 to directly drive standard low cost color or monochrome TV monitors on a single 75 Ohm cable. In addition, the card has an on-board phase-locked loop which permits the output video to be synchronized to an external sync source such as a TV camera. The RGB-256 video output can then be mixed with other video signals. The FG-01 accepts up to four video inputs, one of which is digitized "on the fly" into a 256 x 256 pixel image, 4, 6 or 8 bits per pixel. This output is fed to one or two RGB-256's continuously, allowing the user to watch the live digitized picture on a standard TV monitor. A single command freezes the desired frame. The computer now has complete access to the picture. RGB-256, $1595; FG-01/4, $795; FG-01/6, $1195; FG-01/8, $1995. **Matrox Electronic Systems Ltd.,** 5800 Andover Ave., Montreal, Que. H4T 1H4, Canada. **Circle 138**

**CRT TERMINAL** features four pages of display memory, additional memory for function key programming, large buffer for enhanced operation at high speed, "windowing" (multiple subscreen) capability for simultaneous multi-function performance, multiple user-selectable character sets, generalized I/O communications capability for sophisticated networking between up to three communications lines, and a range of software enhancements to facilitate text editing, data entry and retrieval, business graphics, and other applications. The μP-based terminal has a 24 line/80 character screen, and provides forms control, text editing, upper/lower case, accents, up to 19 user programmable function keys, line drawing graphics, and shared printing capabilities. **Human Designed Systems, Inc.,** 3700 Market St., Philadelphia, PA 19104. **Circle 139**

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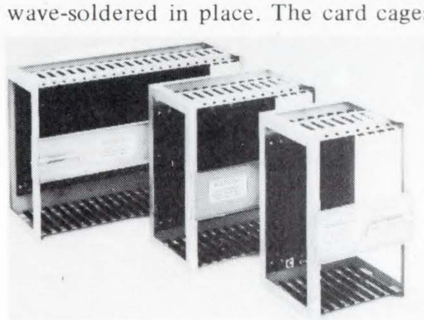

themselves are sturdy steel construction and include a rugged retaining bar to ensure that cards cannot be shaken from their sockets. **Cromemco, Inc.,** 280 Bernardo Ave., Mountain View, CA 94043. **Circle 295.**

**"6502 APPLICATIONS BOOK"** presents I/O program design, handling control signals and other I/O chip resources and also covers and studies real application board building – including a DC motor control, dot matrix character display, A/D conversion, etc. 284 pp. $12.95. **Sybex Inc.,** 2020 Milvia St., Berkeley, CA 94704. **Circle 140**



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# Waveshaping in MODEM Transmitters

**Howard Hwang**
*Rockwell International*

Certain constraints on the spectrum of MODEM transmitters – imposed by the telephone company or MODEM designer to improve overall quality – are easily met for low speed modems. Unfortunately, as MODEM speeds increase, available extra bandwidth drops and gets more difficult for the transmitter output spectrum to simultaneously conform with telephone company requirements and maintain minimum bit error rate. Let's examine some solutions.

## TRANSMITTER STRUCTURE

For MODEMs operating at 2400, 4800 or 9600 bps, the International Telephone and Telegraph Consultative Committee (CCITT) has standardized modulation schemes – "CCIT Recommendations," V 26, 27 and 29 – which is, in general, quadrature amplitude-modulation or more often called QAM, where two orthogonal carrier waves are multiplied by the baseband signal structure to give the modulated output. Filtering then performed **(Fig 1)** can "fit" the spectrum to the requirement.

The signal point structures for 4800, 9600 bps configurations are shown in **Fig 2a** and **2b** as a set of complex points in the plane. For the case of Fig 2a, it results in pure phase modulation.

The filter shown in Fig 1 is a bandpass type which usually has the passband from 400 to 3000 Hz. Or, in another preferred method, this band-pass filter can be replaced by two low-pass filters before the modulator (multiplication by $\sin(\omega_c t)$ and $\cos(\omega_c t)$ ) because it is always easier to implement the low pass filter as opposed to band pass ones. This is called the "baseband shaping" and the resulting structure is shown in Fig 3.

This scheme has another advantage: implementing it is easy via digital hardware – by memory ROMs, transversal filters, digital multipliers and accumulator – and they can either take the form of custom LSI or µPs. For the digital approach, we need another analog low pass filter after the accumulator to filter out the aliasing frequency components. However, this is a comparatively easy task and the hardware requirement is usually minimum.

## TRANSVERSAL FILTERING

An m-tap transversal filter, which takes the form shown in Fig 4, is also known as Finite Impulse Response (FIR) or moving average filter because we can picture it as a trun-

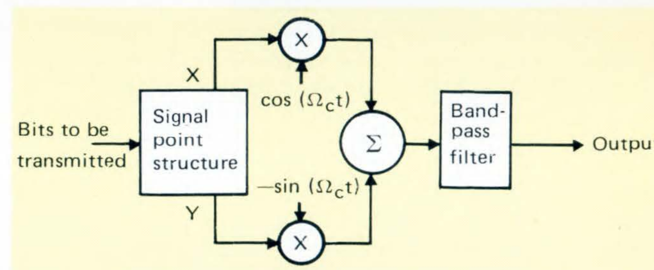


**Fig 1 Quadrature amplitude modulation transmitter structure. See Fig 2 for signal point structure.**

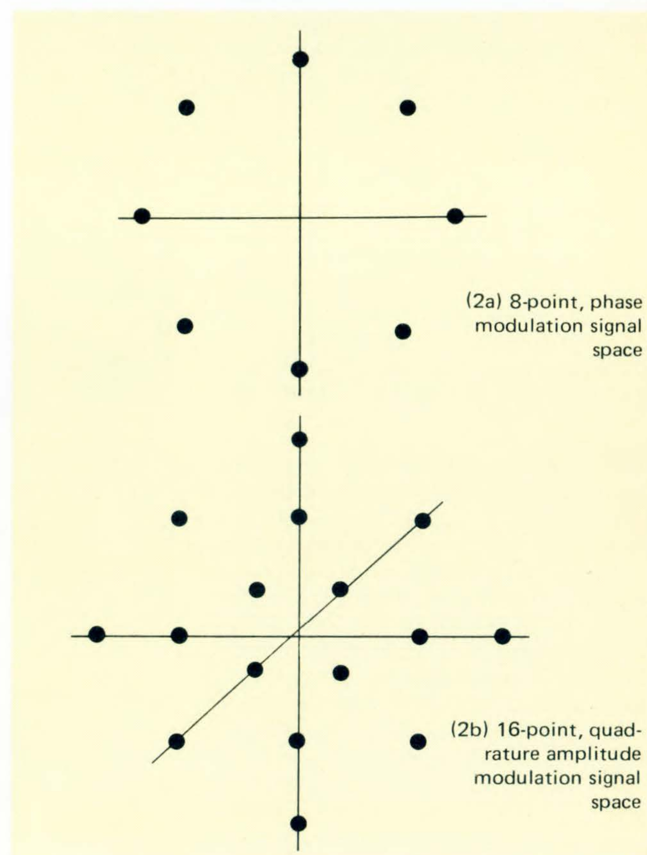


**Fig 2 Signal point structures for 4800, 9600 bps configurations appear as a set of complet points.**

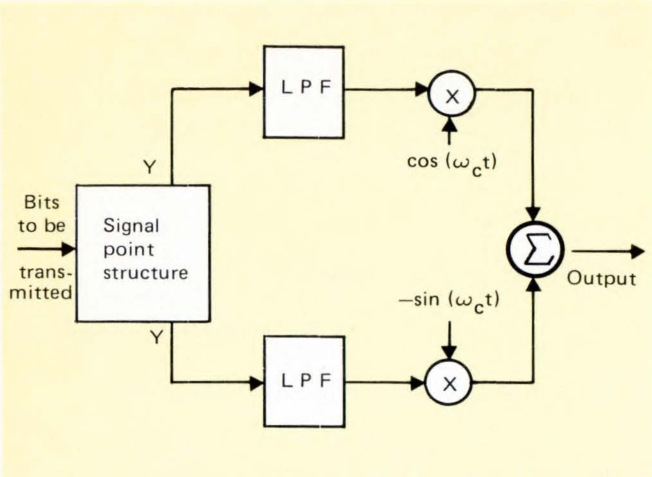


**Fig 3 "Baseband shaping" transmitter is implemented by replacing the band-pass filter of Fig 1 by two low-pass filters, but before the mulator.**

cated (and hence, finite) convolution process.

Assuming that the transmitted data is arbitrary, then input to this filter **(Fig 3)** is approximately "white." The frequency content of the transmitter output is then completely determined by this low pass filter and carrier frequency. Therefore, if we specify amplitude and delay characteristics for transmitter output (which must conform to telephone company specs) we can have the frequency response of this low pass filter simply by a translation. Then, by taking an inverse Fourier transform, we'll have the filter's impulse response, which is usually significant only when close to the center. Giving the sample rate (which should be at least twice the highest frequency at the passband), tap coefficients for this transversal filter can then be determined directly.

One other factor that determines output is the final stage analog filter. Generally, it's used only to filter out higher aliasing frequencies and should be reasonably flat within the band of interest.

Aliasing or overlapping results from ambiguity introduced in uniform sampling. Although an ideal filter with a cutoff frequency is physically unrealizable, it can be approximated as closely as desired with sufficient delay. If the sampling frequency $\omega_s$ is less than twice cutoff frequency, $2\omega_c$, or the signal is not band-limited, then translations overlap and the original signal cannot be recovered by low-pass filtering the sampled signal. This overlapping (aliasing) results from sampling-caused ambiguity.

If the sampling pulse train of uniform periodicity is identically zero over finite intervals, then it is not possible in general to uniquely determine the signal from the sampled signal. For example, consider the sampling of a sinusoid, $f(t) = \exp(j\omega_0 t)$, whose samples, $f(nT)$, equal $\exp(j\omega_0 nT)$. Since $\exp(j\omega_0 nT)$ equals $\exp[jnT(\omega_0 + k\omega_s)]$, then $\exp[j(\omega_0 + k\omega_s)t]$ is going to have the same samples as f(t). To keep aliasing negligible, the original continuous-time signal must be sufficiently band-limited.

However, getting back to the analog filter, should it cause distortions, we can always correct this by pre-compensating in the transversal filter. We'll look at the method of compensation in the next section. It turns out that the compensation doesn't cost us any extra hardware; therefore, if the output spectrum allows, we can even have some compensation for delay distortions caused by the receiver filters. This generally improves overall MODEM quality substantially with minimum extra effort.

Note that input to this transversal filter changes only once a baud. This would then have the effect of sin(x)/x shaping instead of "white" spectrum; and, therefore, the transmitter output spectrum would be different from that for the transversal filter. This problem is solved by compensating this sin(x)/x shaping in the transversal filter. But a more straightforward way is to set the input at transversal filter to zero except for only once a baud. This will "whiten" the spectrum.

For this scheme, if we have n samples in a baud, then input to transversal filter would be: X 0 0 . . . 0 0 X 0 0 . . . 0 0 X 0 0 . . . 0 0 X 0 0 . . . X can take any complex value in the signal point structure.

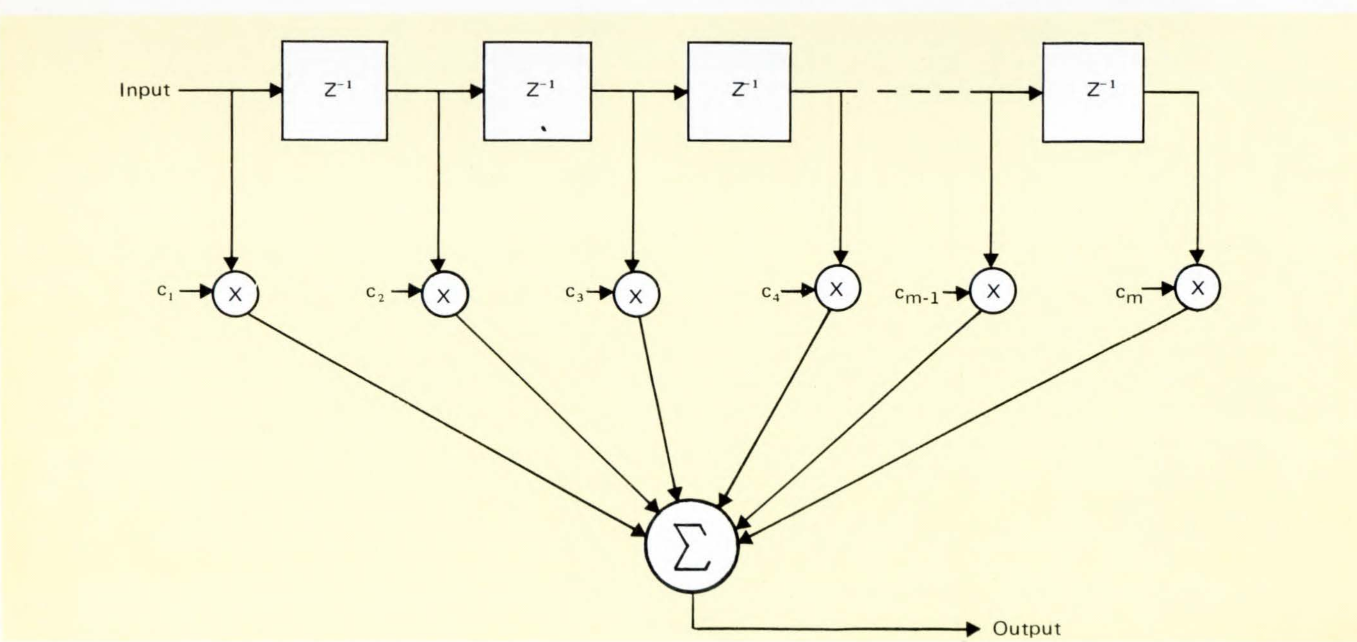


**Fig 4 Output, y (nt), of a nonrecursive or recursive, casual, linear, time-invariant system equals a difference equation:**

$$\sum_{k=0}^{M} a_k f(nt-kt) - \sum_{k=1}^{M} b_k y(nt-kt).$$

**An M+1 tap transversal filter (above) results if it's nonrecursive, i.e., if $b_k = 0$ for k = 1...N.**

Looking at the transversal filter's structure (Fig 4), we see that the number of multiplications for this scheme is reduced to m/n instead of m. The number of additions is also reduced by the same proportion. For example, if we have 8 samples/baud, and 24 taps for the transversal filter, then instead of 24 multiplications and 23 additions, we need only 24/8 = 3 multiplications and 2 additions. Since this is quite a substantial saving on both hardware and execution time, transversal filtering is popular in baseband shaping.

## Root-Mean-Square fitting

How are tap coefficients determined? It's basically an equalizer problem; or, in other words, the problem can be phrased as follows. Given transfer functions $G(\omega)$ and $H(\omega)$, find a function $C(\omega)$ such that

$$\text{Error} = \int_{-\infty}^{\infty} | C(\omega) \cdot G(\omega) - H(\omega) |^2 \, d\omega$$

is minimized. Here, $H(\omega)$ is the desired spectrum for transmitter output, $G(\omega)$ is the spectrum for analog filter and all the compensations, and $C(\omega)$ is the spectrum of the m-tap transversal filter.

Let's denote impulse responses for $G(\omega)$ and $H(\omega)$ as $g(t)$ and $h(t)$. Then from Parseval's theorem, we get

$$E = \text{Error} = \int_{-\infty}^{\infty} \left[ \sum_{j=1}^{m} C_j \, g(t - j\tau) - h(t) \right]^2 dt.$$

For this error to be a minimum, we have

$\partial E / \partial C_k = 0$ for $k = 1, 2, \ldots m$. Substituting, we get:

$$2 \int_{-\infty}^{\infty} \left[ \sum_{j=1}^{m} C_j \, g(t - j\tau) - h(t) \right] g(t - k\tau) \, dt = 0.$$

We can reduce it to a set of simultaneous equations:

$$\sum_{j=1}^{m} C_j \left[ \int_{-\infty}^{\infty} g(t - j\tau) \, g(t - k\tau) \, dt \right] =$$

$$\int_{-\infty}^{\infty} h(t) \, g(t - k\tau) \, dt, \quad \text{for } k = 1, 2, \ldots m.$$

### EXAMPLE:

As an example of the above algorithm implemented on a single LSI chip, the R24 MODEM (2400 bps) transmitter provides the desired waveshape as a square root of 90% raised cosine wave plus some delay compensation. The number of taps used is chosen to be 24. Following methods described in the article, we found the tap coefficients. The DB and delay curves can then be computed from it; these responses are shown in Figs. 5, 6 and 7.

Observe that the db response is very close to the squareroot of 90% raised cosine wave, with the response beyond the baud rate (1200 Hz) less than -40 db. This is particularly desirable if reverse channel of up to 600 Hz is to be used because the transmitter spectrum is within the 1800 + 1200 or 600 to 3000 Hz range and the reverse supervisory signal can then be added directly to this output.

Note also in Fig. 7 that delay is added to this transversal filter to offset that in the analog filters. They are evidenced by a nonsymmetricity in the impulse response (tap coefficients).

Our actual implementation for R24 modem transmitter is a slight variation to the one described; it uses the "signal element" concept (see article for details). This is essentially a trading of ROM for arithmetic logic circuits and can be advantageous in many cases.

In the R24 MODEM transmitter, the signal ROM mentioned at the end of the article is only 96 X 8 bits; yet it accomplishes all shaping requirements, and should shaping requirements be changed in the future, this will only require a simple reprogramming of the ROM.

Looking at the transversal filter's structure (Fig. 4), we see that the number of multiplications for this scheme is reduced to m/n instead of m. The number of additions is also reduced by the same proportion. For example, if we have 8 samples/baud, and 24 taps for the transversal filter, then instead of 24 multiplications and 23 additions, we need only 24/8 = 3 multiplications and 2 additions. Since this is quite a substantial saving on both hardware and execution time, transversal filtering is popular in baseband shaping.

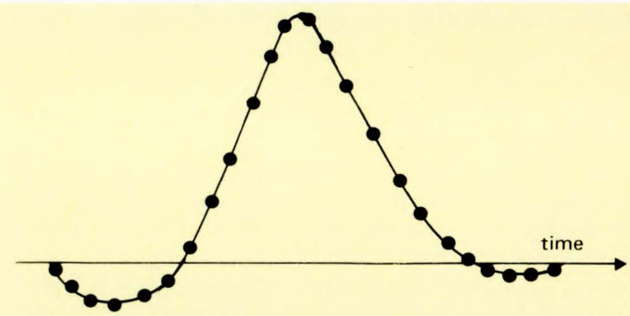


**Fig 5 Tap coefficients for transversal filter.**

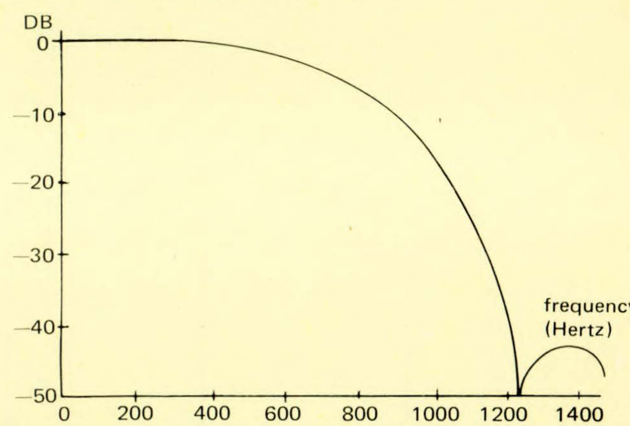


**Fig 6 Frequency response.**

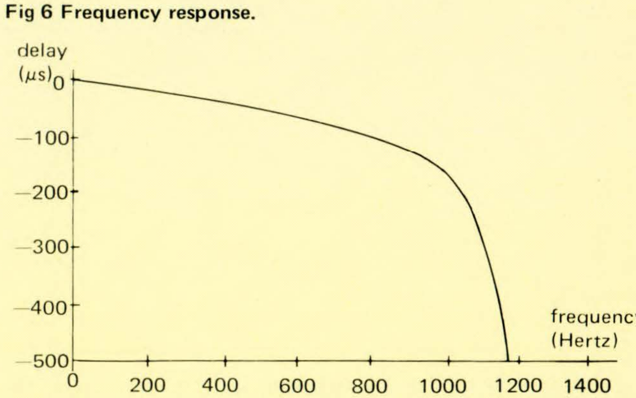


**Fig 7 Delay response.**

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Using matrix methods and a computer, we can then solve it easily. Note that we also can introduce some weighting function into the error criterion in the first equation of this section (although we left it out only to make things clearer).

## Appendix

The transmitter output can be represented as:

$$s(t) = \text{REAL} \sum_{j=1}^{m} a_i f(t - iT^1) e^{j\omega_c t}$$

In this expression, "m" is impulse response duration in terms of sample interval; "$T^1$" is sample interval; f, baseband shaping (impulse response) function; $a_i$, transmitter signal structure points (complex); and $\omega_c$, carrier frequency in radians.

Now, since we said that $a_i$ will be reset to zero except only once in a baud, we can rewrite the above equation as:

$$s(t) = \text{REAL} \sum_{i=1}^{p} a_i f(t - iT) e^{j\omega_c t}$$

Here, "p" is impulse response duration in baud intervals and "T" is baud interval.

Take the case of phase modulation, as is commonly used for 4800 and 2400 cases (Ref. 1). We know from Fig. 2a that:

$$a_i = e^{j\phi_i}, \text{ where } \phi_i = 0, \pi/4, \pi/2, 3\pi/4, \pi, 5\pi/4, 3\pi/2, 7\pi/4$$

Therefore, we get:

$$s(t) = \text{REAL} \sum_{i=1}^{p} f(t - iT) e^{j(\omega_c t + \phi_i)} =$$

$$\sum_{i=1}^{p} \text{REAL} \left[ f(t - iT) e^{j(\omega_c t + \phi_i)} \right]$$

We can treat each term in this summation as a "signal" element". If we store these signal elements in memory, then by properly selecting and adding them, we'll have the transmitter output. This scheme gets rid of the multiplication which takes a lot of hardware and execution time, and reduces the entire process to a simple address selection. Also, roundoff errors due to multiplication are eliminated for the obvious reason.

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# Designers' Notebook

## A Watchdog Circuit for $\mu$C-Based System

This circuit will significantly improve operation of an 8022-based design in a noisy environment. Minor modifications make it useful with almost any $\mu$C-based system.

When a $\mu$C is placed in an electrically hostile environment it is necessary to ensure that the unit remains operational even when subjected to large noise transients on incoming power leads or interface circuitry. Proper supply design and I/O circuitry provides this immunity. No matter how noise immune the circuitry is, however, it's always possible for a noise transient to occur which exceeds protection circuitry design limits. You must weigh relative costs of additional protection circuitry vs. failure costs to optimize the final product performance. Remember, internal $\mu$C circuitry is often driven into undefined states by noise transients which exceed the design limits of the part but which do not contain sufficient energy to physically damage it. Under these conditions a watchdog timer can be used to ensure that the $\mu$C-based system returns to a normal operating mode after the noise conditions end.

A watchdog timer adds circuitry external to the $\mu$C which resets the system if it does not receive periodic signals from the $\mu$C – signals generated by the software if, and only if, the software is executing instructions in a reasonably sane manner. If the processor is halted, or executing a tight loop (or even waiting for an I/O event that never occurs), the periodic signal to the watchdog circuit will not be generated and a reset will occur. This circuit **(Fig 1)** can add a watchdog timer function to almost any $\mu$P based system. A simple comparator is used both to generate power-on reset and to perform the watchdog function. The 8022 incorporates an onboard power-on reset circuit, which only requires an external capacitor. The additional circuitry shown is only required if the watchdog function is to be used.

Before power is applied, Capacitor C1 is discharged through Resistor R1. The time constant for this discharge is only 47 $\mu$s so that the circuit will properly recover from relatively short power outages. (Poor recovery from short power "glitches" is a common cause of reset problems.) When the unregulated dc input reaches a voltage which guarantees that the regulator has sufficient input voltage to maintain regulation on the $V_{CC}$ supply, Zener Z1 starts conducting and back biases Diode D1 so that C1 is no longer discharged through R1. Since the resistor divider established by R3 and R4 biases the comparator so that its output is high at this point, C1 starts to charge through R7. The time constant of this charging determines the power-on reset duration for the $\mu$C. (A high level resets the 8022.) When C1's voltage exceeds threshhold established by R3 and R4, comparator output will drop to a low level and the $\mu$C will come out of the reset state. Resistor R5 supplies hysteresis to ensure a clean transition. Circuit action so far has produced a clean reset signal, which is asserted for a fixed delay following the availability of sufficient input voltage to guarantee the availability of power to the system. Let's look at the watchdog function.

When the reset signal goes LOW, releasing the processor from the reset state, Resistor R7 begins to discharge C1. If the voltage on C1 drops enough

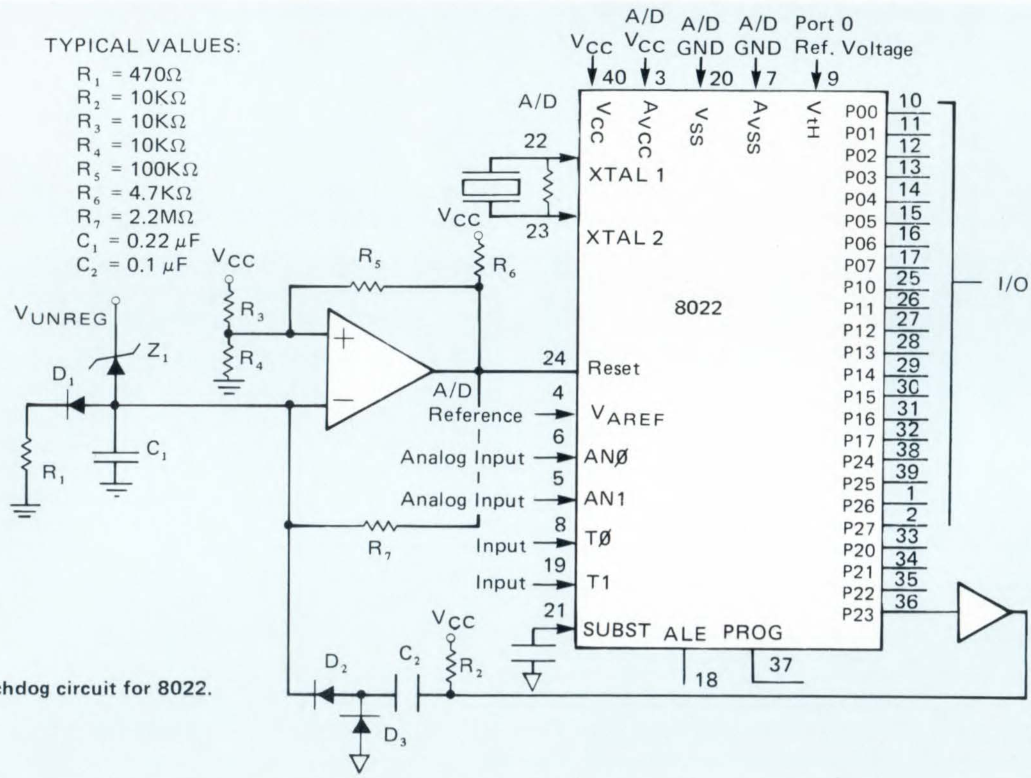



Fig 1 Watchdog circuit for 8022.

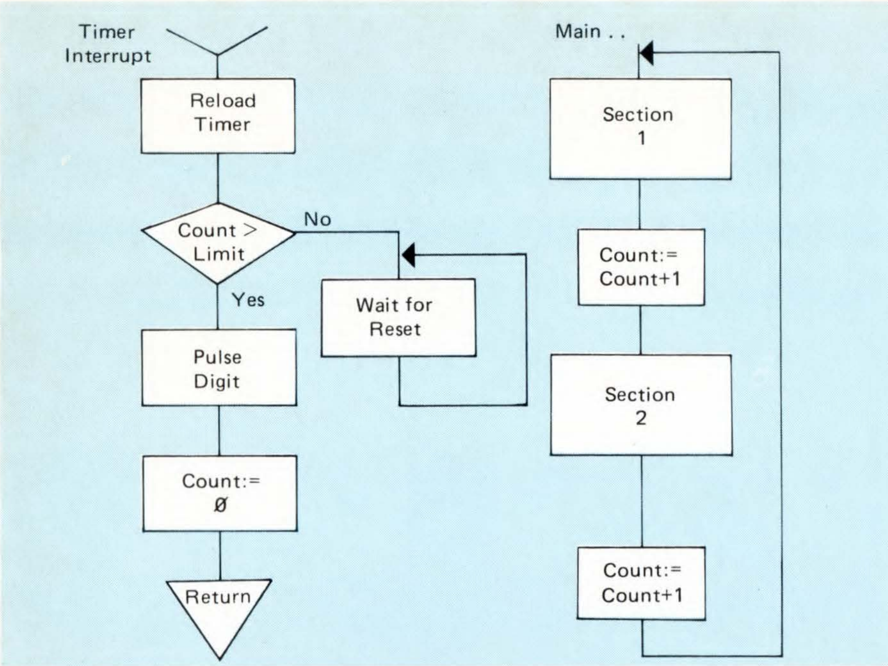



**Fig 2 Avoiding watchdog reset condition.**

to overcome the hysteresis built into the circuit, then reset will occur again. The only way to prevent this is to supply current pulses through D2 at a high enough rate to ensure that C1 does not discharge. These pulses are ac-coupled to ensure that the program cannot prevent the watchdog from timing out by going into left field with the watchdog output stuck either at a logical "1" or a logical "0". It is necessary for transitions to occur to keep the watchdog timer reset. If these transitions don't occur, circuitry surrounding the comparator oscillates at a period determined by R7 and C1 so that the $\mu$C receives periodic reset signals. If transitions begin after the occurrence of a reset, then reset circuit oscillations will end and the program in the $\mu$C will continue to run.

In practice it is often possible to drive the watchdog timer with a signal which is generated already by the system. A good example of such a signal would be one of the digit drive signals going to a multiplexed display. Since software has to pulse these lines anyway, no additional software burden is necessary; the system will reset whenever the processor stops scanning the display. A problem which can occur if this is done, however, is that it is sometimes possible for the background routines to hang up in an undefined state while the interrupt routine continues to operate. Since the display scanning is often handled in response to a timer interrupt, this means that the watchdog will continue to be reset even though the main routines of the system are not functioning. This situation can be avoided **(Fig 2)**. A variable (COUNT) has been implemented which is incremented at various points in the main routines. These points have to be selected by the system designer so that it can be guaranteed that the variable will be incremented by a minimum count between occurrences of the timer interrupt. When the timer interrupt routine occurs, the timer service routine will test the variable to see that it exceeds a preset limit (LIMIT) before it pulses the digit line. Having reset the watchdog by generating this pulse, the service routine sets the variable to zero. If the timer interrupt service routine is ever invoked with the variable less than the preset limit, it can assume that the main routines are not operating correctly and go into a tight loop to wait for the watchdog timer to reset the system.

Lionel Smith, Intel Corp., Micro-Controller Div., Phoenix, AZ.

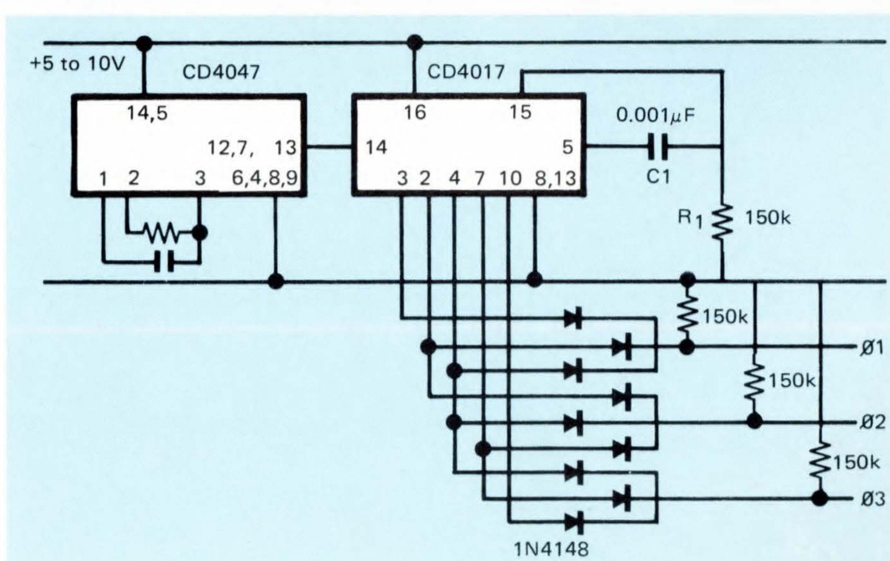
**Rate this design: circle 7L, 7M or 7H on Reader Inquiry Card.**

# CD 4047/17 Make Three-Phase Generator

This circuit was originally designed to provide three outputs, phase shifted by 120° to provide (after buffering and filtering), drive to a low-voltage three phase supply for a linear motor. Used as a clock at six times the required frequency, the CD 4047 drives a one-of-ten decoded counter, which is reset after a count of six by $R_1$ and $C_1$. The appropriate outputs of the CD 4017 are picked off with diodes to give three-phase shifted square waves. The circuit can easily be adapted to give a wide range of phase related outputs.

A.J. Richardson, 32 Cook Ave., Newport, Isle of Wight, England.

**Rate this design: circle 8L, 8M or 8H on Reader Inquiry Card.**




**Two IC, three-phase generator outputs square waves.**

# Special PROM Simplifies Board Testing

By including a $\mu$P and its support chips on the same board as a number of analog circuits, you can use a $\mu$P to generate test stimuli for these analog circuits instead of dedicated test equipment. Inserted in place of one of the normal memory chips, a special test PROM simplifies production testing. For example, this approach can test a number of analog functions on the servo/transport control board fitted to the EMI 8800 digital tape transport.

This $\mu$P and its associated logic circuits are tested first and then used to stimulate the signals for the analog circuits. To provide independent control of the $\mu$P outputs for the required test signals, the connections to the processor's ports are fed to the appropriate test equipment. The system can activate inputs to the analog circuits without recourse to special links for testing. It can test the board much faster. In addition, no board space is wasted solely to assist testing and normal board interconnections between analog and digital circuits are maintained.

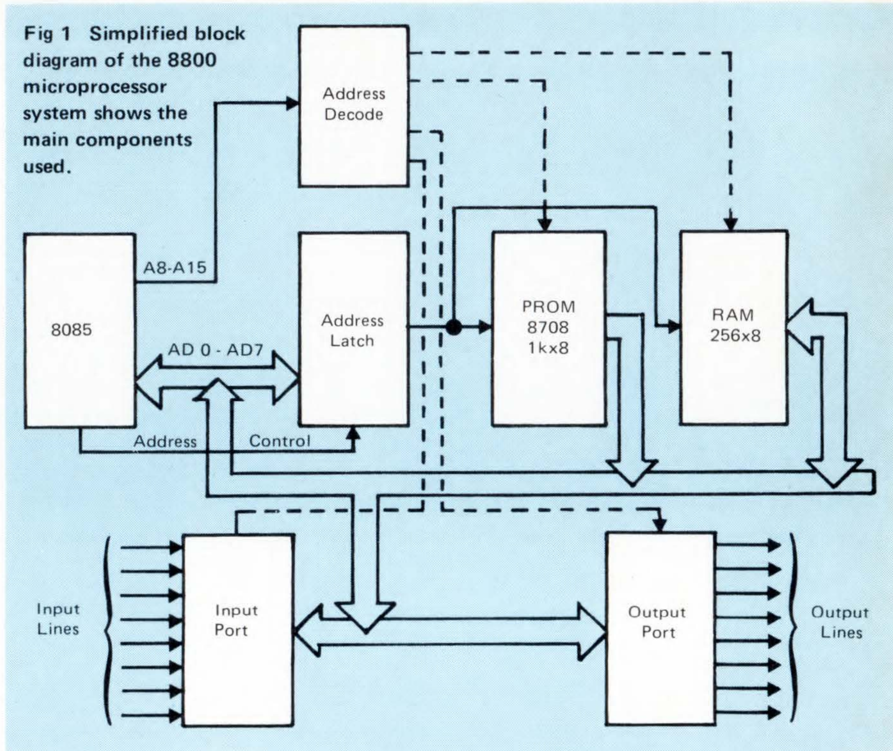



Fig 1 Simplified block diagram of the 8800 microprocessor system shows the main components used.

**Fig 1** shows the basic structure of the $\mu$P system and the 1K x 8 test PROM inserted in place of the normal test program. **Fig 2** illustrates how the $\mu$P interconnects with the various analog circuits. It also shows the variety of circuits controlled by the $\mu$P and stimulated by the test PROM.

D.S. Cutler, S E Labs (EMI) Ltd., Eng. Div., The Mill, Wookey Hole, Nr. Wells, Somerset BA51BB, England.

**Rate this design: circle 9L, 9M or 9H on Reader Inquiry Card.**

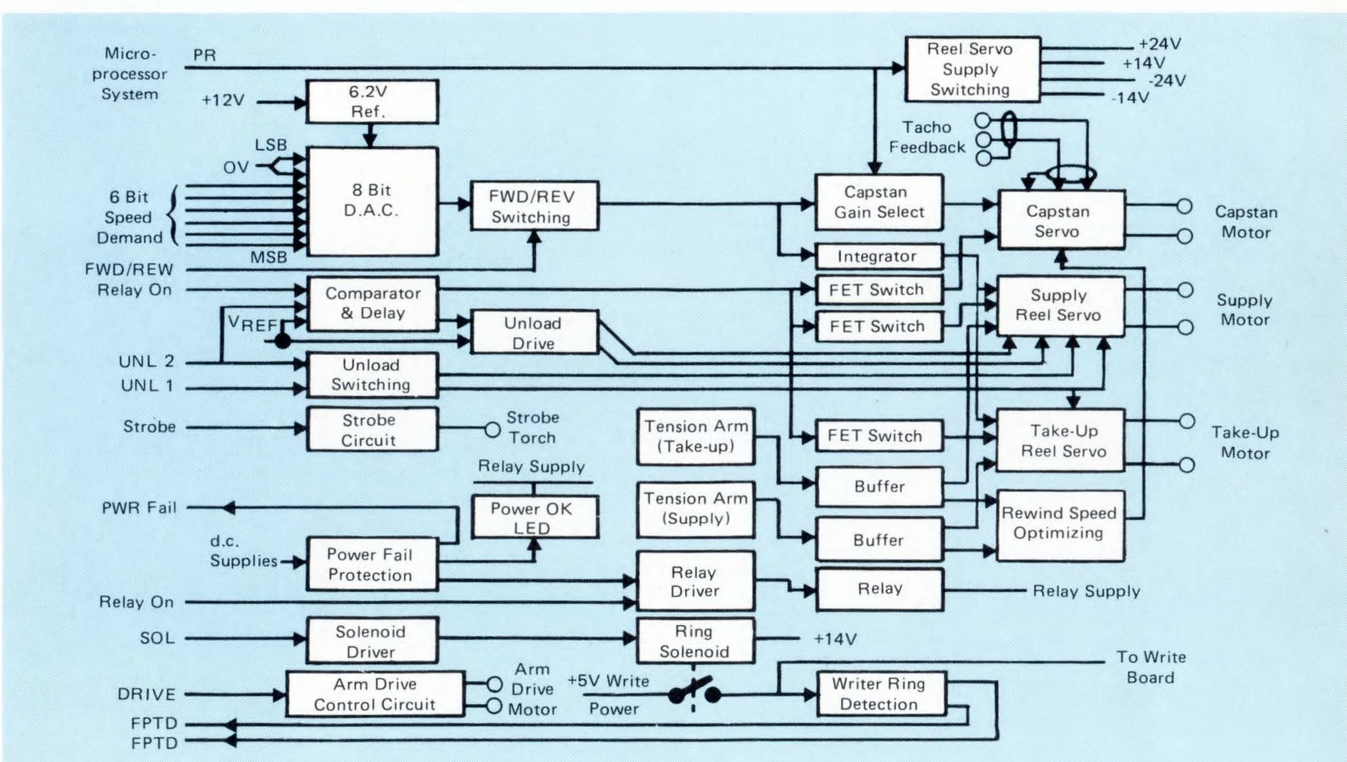
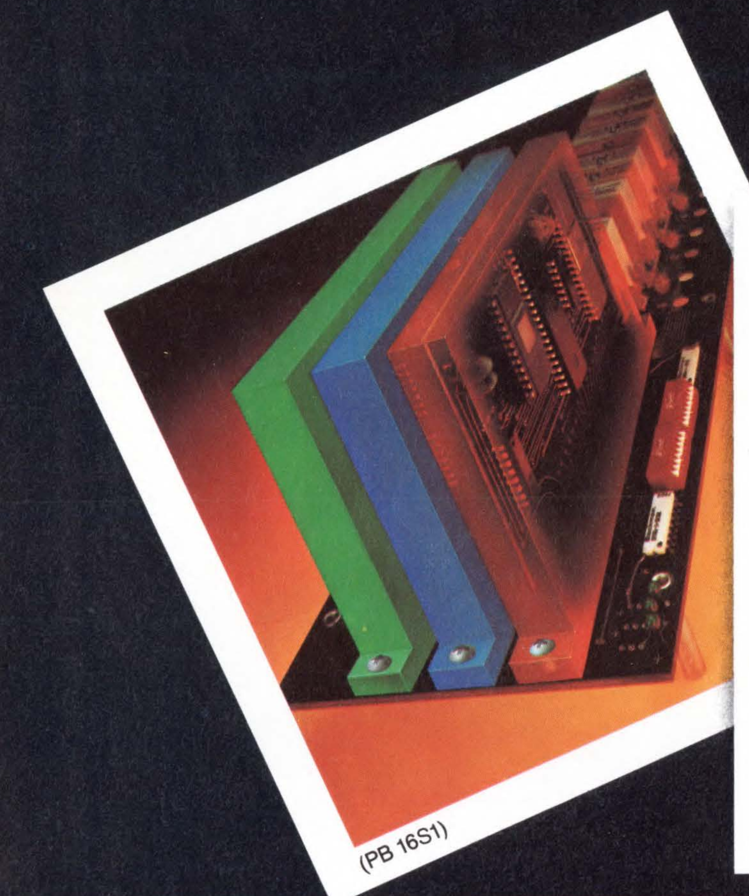
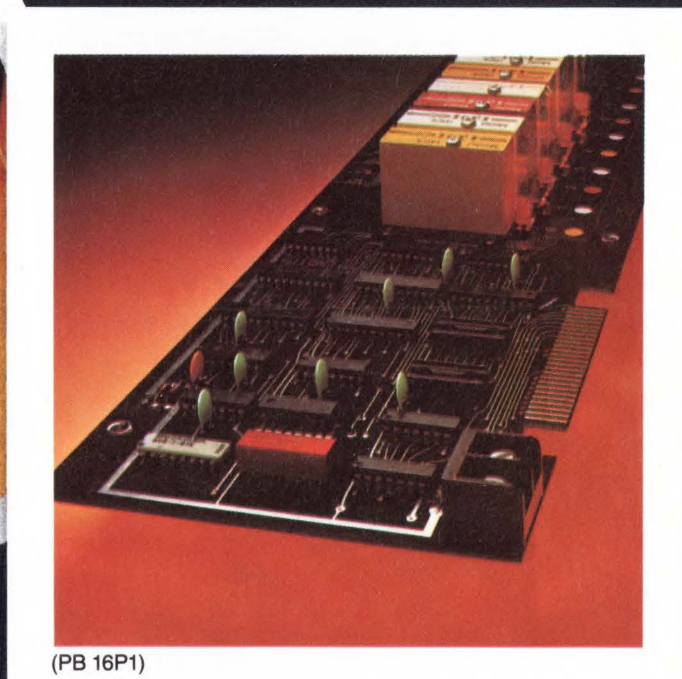



Fig 2 Various analog functions receive their control signals and, where appropriate, send back status information.

# ADDRESSABLE I/O SYSTEMS FROM OPTO 22



(PB 16S1)



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