VOLUME 9, NO. 10 OCTOBER 1979

Digital Design

The Magazine of Systems Electronics

We've Earned Our Stripes

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Opto 22 combines the latest and best in I/O modules with plug compatibility to single board computers. Opto 22 I/O Systems are available in plug compatible racks holding eight, sixteen or twenty-four modules. These highest quality Input/output modules are available for 5, 15, or 24-volt logic—all employing 2500 volts RMS photo-isolation.

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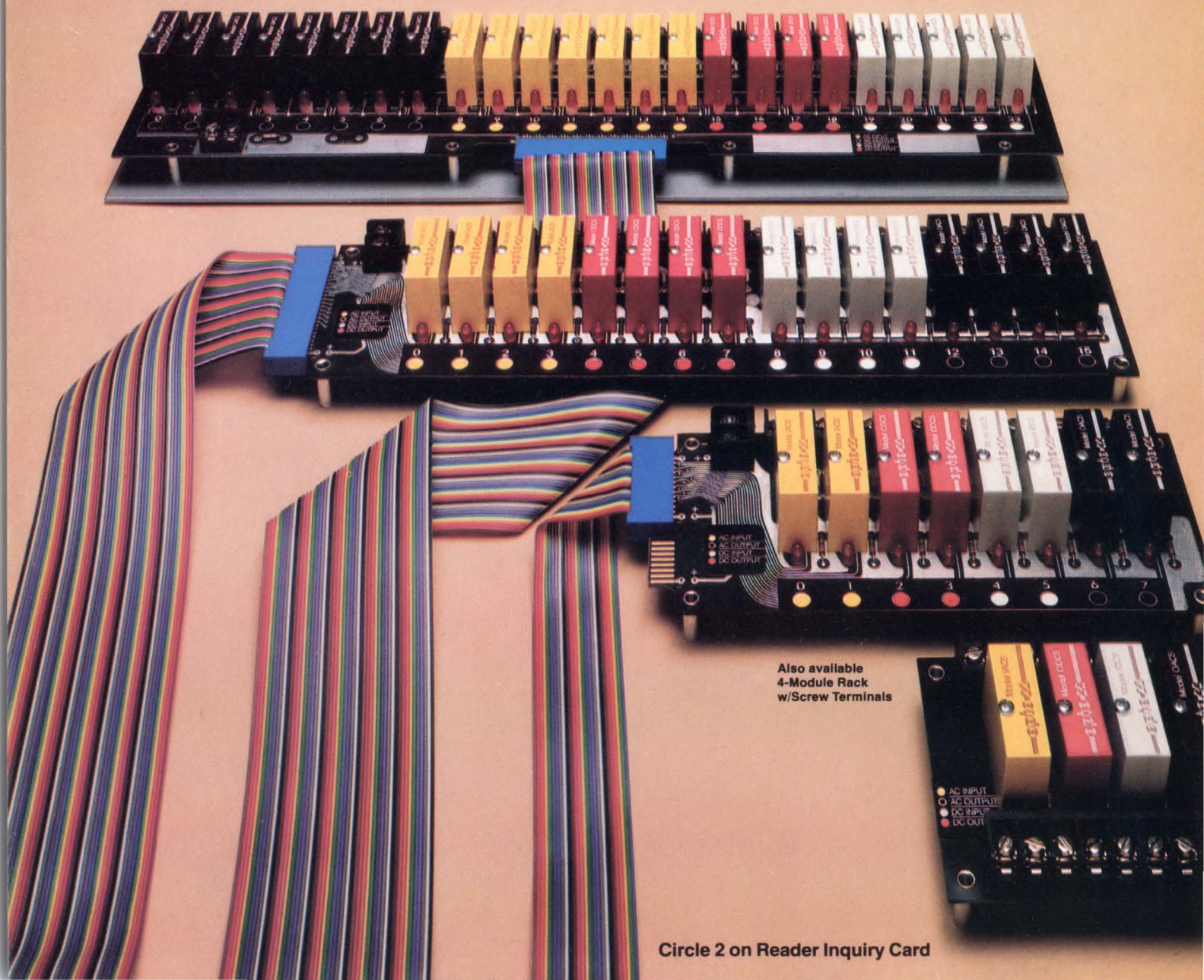

Also available 4-Module Rack w/Screw Terminals

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Our raster-scan systems are fast becoming leading contenders for top honors in the digital computer graphics and image display field. The clarity and conciseness afforded by monochrome resolutions as high as 1280 X 1024 and full-color versions to 1024 X 1024 pixels, are good reasons why. There's many more . . . let's peruse just a few.

16-Bit High-Speed Programmable Processor.
Consisting of 16 general purpose and 9 operational registers, plus a set of 55 mnemonic instructions, along with 16-bit writeable control storage, the processor can manipulate data at internal cycle rates of 150 ns.

And it provides automatic DMA access, selective erase, user selection from a range of over 16-million different color intensities, plus flicker-free operation.

Modular, Versatile Hardware.
Since Genisco's systems are capable of being expanded from a single monochrome memory plane to a number of planes that support the full range of gray scales or colors required, you can inexpensively start-out and add-on as needed. Our monitor control module lets you operate up to 12 monitors, mix TV/Video and remotely monitor — as well as fill areas outlined in the bit-map memory — and allowing RS232 interfacing with a keyboard, trackball, joystick or graphics tablet.

Genisco also provides a full complement of standard minicomputer interfaces or can economically build one to suit. Scroll/Zoom and high-speed Character-Vector Generator hardware are also available.

Cost-Effective Graphics for the OEM.
For applications where minimal cost without sacrifice in performance is a major consideration, Genisco offers the GCT-3400 OEM models.

FORTRAN Software.
In addition to the Basic Graphics instructions and diagnostics provided with the system, Genisco offers GRAFPAC II, the most comprehensive FORTRAN Callable Subroutine Package available for raster graphics.

Since space does not allow for greater enumeration of the many ways your computerized displays can be truly picture-perfect, contact Genisco — a name that has stood for technological expertise for over 30 years — 17805 Sky Park Circle Dr., Irvine, CA 92714, (714) 556-4916.

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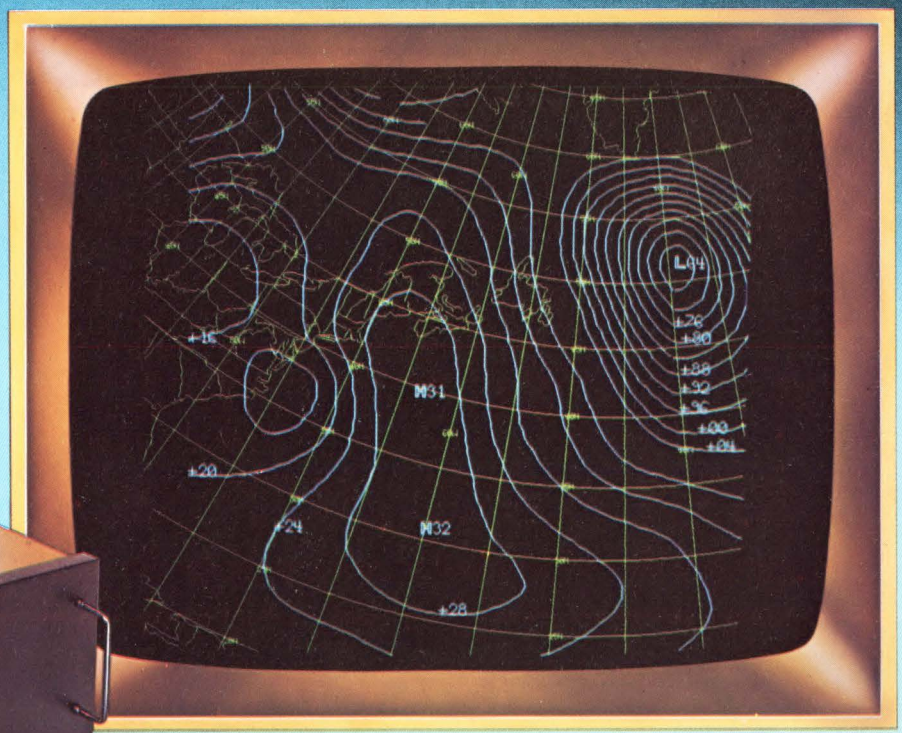
It's just one way Genisco makes your pictures perfect.



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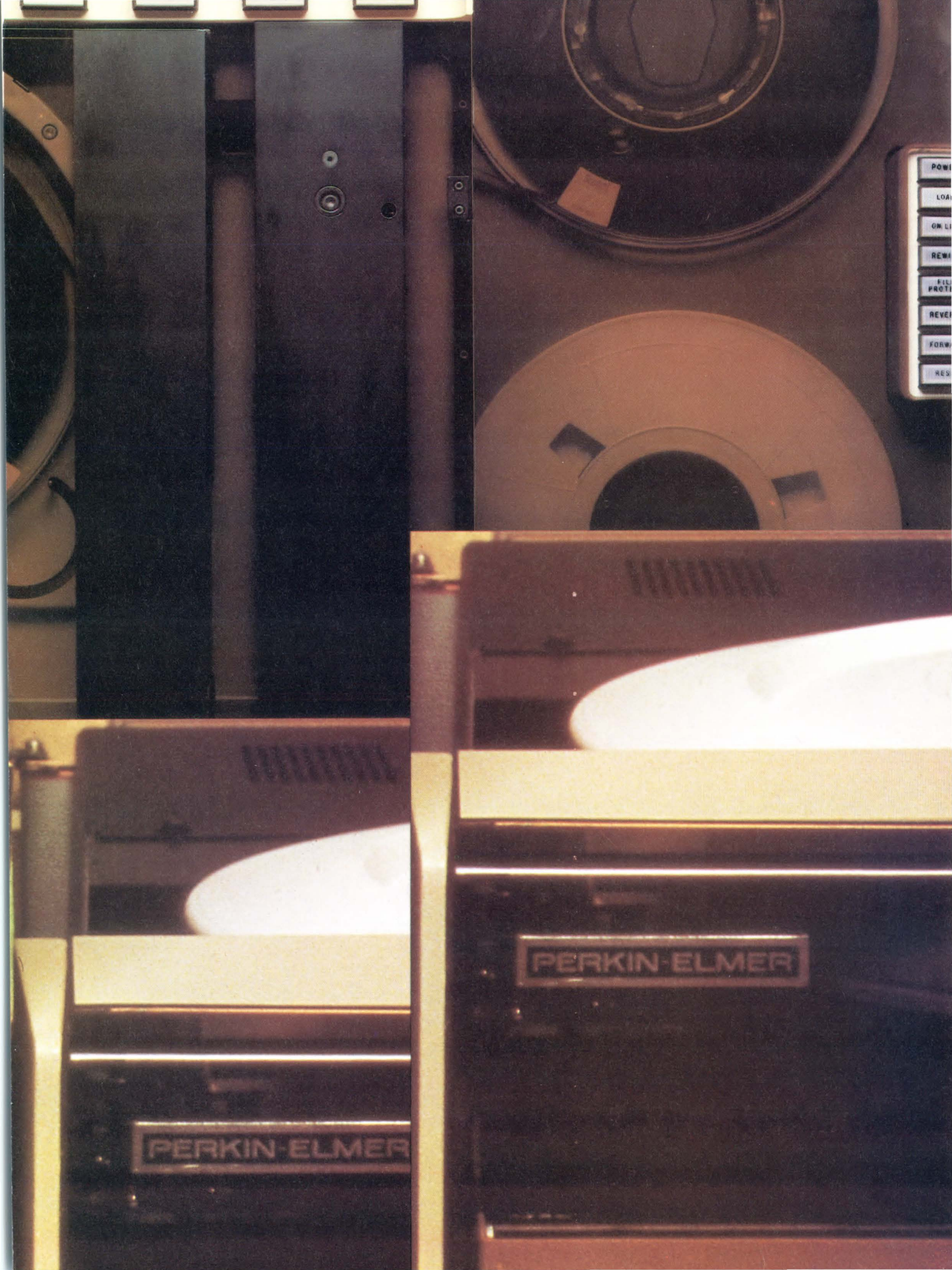
PERKIN-ELMER
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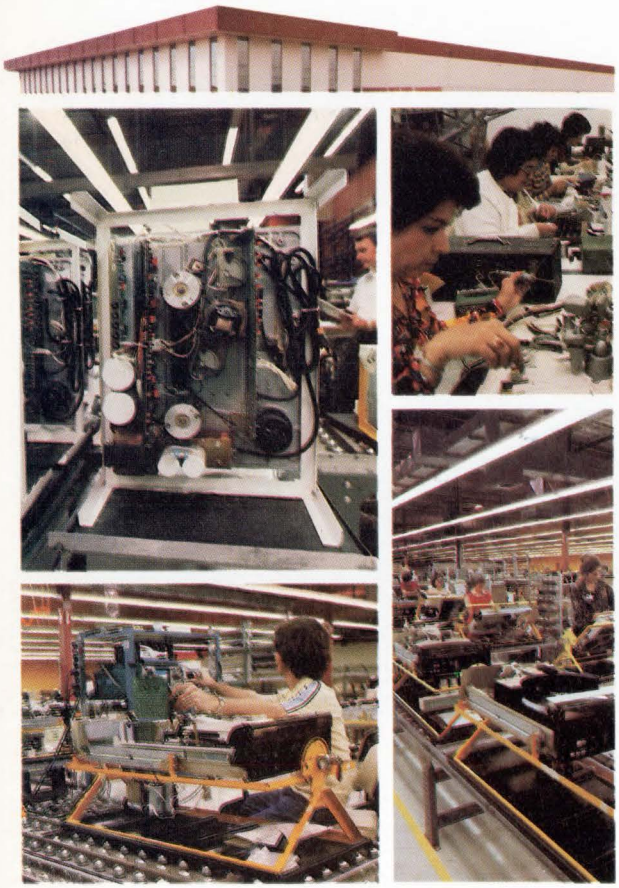
Delivery That's OEM Responsive

Perkin-Elmer tape and disk drives are available now. When we saw the demand for our drives grow, we responded by making the investments necessary to be responsive to OEM delivery requirements. Our commitment to OEMs includes a new 250,000 square foot manufacturing complex with the production capacity that can meet today's requirements.



Our OEM Commitment Our commitment to the OEM goes beyond new facilities. It's a multi-faceted corporate commitment that involves a powerful combination of investments in advanced production and testing equipment, responsive management, financial strength and competitive products. A commitment that assures product reliability, on-time delivery, and responsiveness for our OEM customers.

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Responsive Answers For a responsive answer to your tape or disk requirements, write or call today. Then, you'll see what it means when we say we're OEM responsive.

Perkin-Elmer, Memory Products Division, 7301 Orangewood Avenue, Garden Grove, CA 92641 (714) 891-3711

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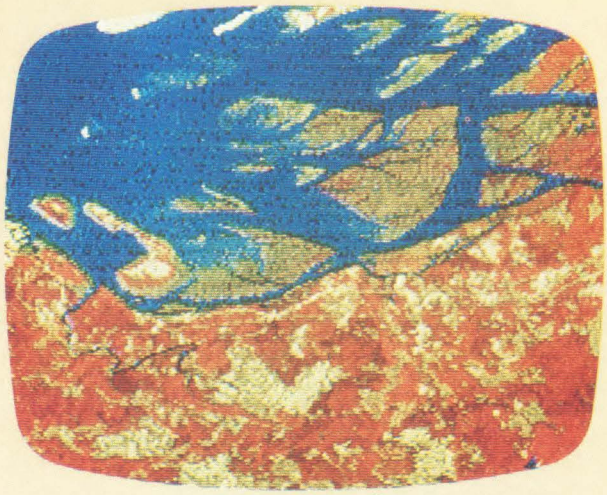
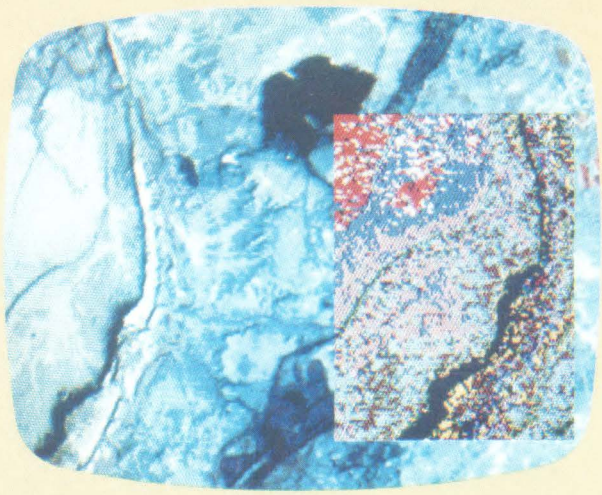
Image processing. Your way.





Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

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- Zoom and pan
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In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 512 to 1024 x 1024.

So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

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VOLUME 9, NO. 10 OCTOBER 1979

Digital Design

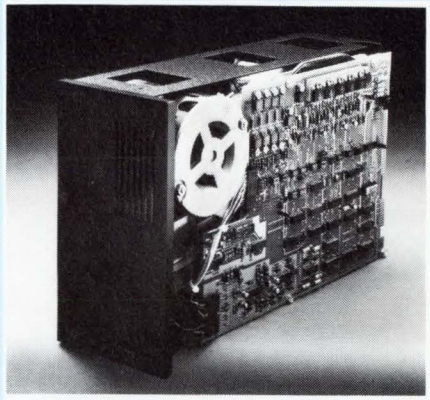
The Magazine of Systems Electronics

Features

Departments

ON OUR COVER

Symbolizing the growing trend toward outside sources offering μP support equipment is the new MicroSystem Emulator. It provides universal hardware support for six μPs (soon to be 12) on any computer. *(Photo courtesy of Millenium Systems Inc.)* Cover design by David Bastille.



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Class III offers 400 lines per inch resolution, switch selectable point and run modes, and a choice of three interfaces, 16 Bit Parallel Binary and BCD, RS232C, or GPIB.

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Letters

Poor Software Support

Dear Editor:

Your article, "Software Bedevils Small Business μCs", in the June issue on small business software was very perceptive – not at all what I am used to seeing in magazines devoted more to the larger systems. Most of the large computer people have a chauvinism toward microcomputers which interferes with them absorbing what has happened, what is happening, and what this portends.

Wayne Green
Publisher
Peterborough, NH

Canada's Open Universities

Dear Editor:

Please forward these copies received from the Canadian School of Management, Northland Open University to P.T. Rowe (Letters, "Shocked Canadian", July 1979). Yes, Canada does allow open universities!

I am enclosing literature from Northland Open University of Toronto. Here are some excerpts.

"By virtue of its Charter, Northland Open University is authorized to award certificates, diplomas, fellowships and to confer academic degrees. Northland Open University is a member of the University Without Walls (UWW) consortium of academic institutions called the Union for Experimenting Colleges and Universities which offer non-traditional educational programs.

"Prior college work can be demonstrated with transcripts of records from other schools and/or copies of Degrees, Diplomas and Certificates. Informal and experiential learning (including learning from independent study, or learning acquired from a job) can be demonstrated by any suitable means of documentation, including essays, examinations, published articles or other student projects which intrinsically demonstrate learning acquired. Prior learning must be judged by the Committee to be suitably demonstrated and documented before credit towards the degree is granted. Professional experience should be documented by letter(s) from employer(s) outlining duties and responsibilities. These would be in addition to the required three reference letters.

"This program because of its independent study approach is of special interest to highly motivated experienced professionals, who have a clear awareness of their own educational needs and professional goals."

Phil Bender, P.E.
Johnson Controls Ltd.
Toronto, Ontario

Achieving Results

Dear Editor:

The IEEE is essentially a volunteer organization. The interests of EEs vary widely – from the academician to the corporation executive to the job shopper in Seattle. It is always impossible to please everyone.

The fact remains that IEEE is the only significant EE organization we have. It is by far the largest technical society in the world. It is easy for engineers to stand on the sidelines and criticize; it is much harder to put in long volunteer manhours to achieve results.

Sincerely,
Robert S. Duggan
Lockheed-Georgia Co.
Marietta, GA

Data Acquisition Book

Dear Editor.

As I mentioned to you a couple of months ago, the series of articles "Principles of Data Acquisition and Conversion" is part of a book just published. The title of the book is "Data Acquisition and Conversion Handbook". edited by myself, and available from Datel-Intersil, Inc. for $3.95.

Eugene L. Zuch
Datel-Intersil, Inc.
11 Cabot Blvd.
Mansfield, MA 02048

Soft Copy Displays

Dear Editor:

I would like to take this opportunity of thanking you for your very nice write-up on the subject of quantitative evaluation of soft copy displays which appeared in *Digital Design* June 1979. I think the article came out very nicely.

Dr. Harry C. Andrews
Comtal Corp.
Pasadena, CA

From DeAnza Systems VISACOM Visual Computer System

An extraordinary combination of micro-computer power and DeAnza Systems imaging expertise

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For further information and a list of satisfied users, contact DeAnza Systems, Inc., 118 Charcot Ave., San Jose, CA., 95131, (408) 263-7155.

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Speakout

Paul Snigier, *Editor*

The Winds of Change

Part Two

Free enterprise is best. Competition keeps every manufacturer on his toes to satisfy customer needs; if not, competition offers a new product that does provide what customers want.

The same goes for organizations. Whenever there is a lack of competition, or whenever competing organizations merge (such as IRE and AIEE), the loss of competition too often creates an organization that is not responsive to its members' needs; or, worse, as in the case of IEEE, a leadership riddled with academics and corporate executives – men whose interests all too often conflict with that of working EEs. As we saw in Part One, IEEE memebers voted overwhelmingly (96%) for major reform. But, can IEEE override the vested interests of its leaders, who can quickly marshal enormous resources to protect their interests? Or is it too late for IEEE? Is it time to start a new organization that better serves the needs of working EEs?

It's hard to imagine a corporate executive-IEEE officer supporting a program that raises EEs' salaries, or academics supporting programs that limit the number of students entering their programs; and, history shows us whose interests usually get served first. For example, when a certain firm's now-infamous hiring/firing policy came to light – "to control the aging rate of the company's population, particularly for scientists and engineers," and "to increase incentives to hire qualified personnel at the lowest salary" – why did IEEE remain silent? Was it because the president of this firm was also an IEEE president? Or was it mere coincidence? And, is being on the IEEE board of directors and of his firm a conflict of interest? Then there's the case of seven top IEEE officials (including another former IEEE president) serving on an open university board – not to mention several of them receiving "doctorates" from the same open university. Many other examples exist.

Perhaps it's time for IEEE to take a lesson from any trade or professional union: prohibit members of management from being IEEE officers or members. Until IEEE can eliminate this conflict of interest in its leadership, there is simply no way it can ever transform itself into a strong professional society to represent your best interests.

Fortunately, change is coming to IEEE. One positive sign is the latest moves by IEEE to adopt the Feerst-Schneider Proposal establishing a Skills and Availability (S & A) data bank for IEEE members that would list skills and specialties for each participating EE (both direct and consulting). This would ease the shock of any future mass layoffs due to recession. As pointed out by the sponsor, Burk Schneider, "IEEE would not again be caught unprepared." Also, this S&A data bank could be used by the U.S. Department of Labor to determine availability of EEs to fill openings *before* passing on visa applications from foreign EEs. The DOL is currently hampered by a lack of authoritative data. Also, such data could be used by high school guidance councellors to give students a fairer picture. Much more is needed, and this is a start.

But IEEE better reform its ways. Spending an undisclosed sum of its members' dues to hire a large PR firm (unforunately, the Shah of Iran's) to improve its image is not the right way to do things. Major reform, not sugar-coated PR, is needed.

We wonder how much longer the working EE will tolerate conflict-of-interest leadership, and whether starting a new organization wouldn't be a better idea. If the mass dissatisfaction we've seen in letters from our readers is any indication (not to mention the surprising number who say they have or are resigning in disgust), then the potential for mass resignations must be significant. If anything more than mere superficial PR surface changes aren't forthcoming *soon*, then there is only one answer: a new organization.

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Technology Trends

COVER STORY

μP Emulator Supports Six Types, Speeds Development Times

Millennium Systems' MicroSystem Emulator-Series 2000, when connected to a host computer, lets that computer serve as a μP development system to solve hardware and software needs (in the user's application) of μPs (6800, 6802, 8048, 8080, 8085A, Z80A) emulated by the Millennium instrument.

The Emulator can also be used with dedicated μP development systems, allowing any such system to support a variety of μP types. The high-performance instrument operates at speeds to 5MHz, which allows real-time emulation of fast μPs. Real-time operation extends to an optional real-time trace capability—a valuable debugging tool that lets users step test their design performance at full-rated speed. Real-time trace capability also provides a record of 128 past operations so that program faults are quickly uncovered.

Emulator provides complete debug facilities, with 8K of RAM available. This on-board memory space lets users down-load programs for execution in the Emulator. They can start to debug a system even before it's built. Users working on designs that incorporate DMA will find this unit to be the only 8-bit emulator capable of operation under DMA conditions in all of the supported μPs. There's also a high-speed serial data link; it further accelerates development time by immediately transferring programs and data out of the host computer. Emulator's keyboard allows it to be used as a stand-alone instrument, permitting the host system's resources to be shared among several users. The MicroSystem Emulator Series 2000 costs $4500. Want more information? Contact: **Millennium Systems, Inc.** at 19020 Pruneridge Ave., Cupertino, CA 95014.

Circle 275

Emulator – Series 2000 will soon support 8049/41/35/39/21 and 8748.

Computer Data Predicts Downturn

Today's EE shortage could transform itself into a glut by mid-1981, with mass layoffs equalling or exceeding those of the early 1970's, when the Defense Dept. was cutting its budget and NASA was winding down its Apollo program.

In an early-warning forecast from the Science Registry Group (SRG) of Anaheim, CA, comes a grim forecast that layoffs are now on the way. SRG forecasts that the demand for EEs should continue throughout the next year, but that layoffs will begin in certain key industrial and consumer industries and then spread. Although overall demand will taper off next year, the downturned sectors will be slightly offset by increases in certain segments, notably the military and energy. These contrasting trends will become evident sometime in the first half of 1980, but won't last long. By mid-1981, the full scale downtrend in hiring will emerge, rapidly followed by mass layoffs. Before release of the startling findings, SRG checked and rechecked the data and results. Although these computer predictions are generally never released for outside use, this time SRG felt that the seriousness of the situation demanded its release.

SRG's data was based on a computer analysis updated every 30 days – one which accurately predicted the timing and severity of the last downturns. Data is inputted to SRG every 30 days from over 500 subscriber firms (as to their staffing needs), 150 engineering schools (on demand and number of graduates), all government contract sources and related economic data sources. This data is evaluated, tabulated and then fed into a computer that models the EE job market. Data already indicates a drastic drop over last year's demand for EEs.

Several factors are causing this drastic downturn: (1) less EEs leaving engineering, as occured in 1970-72 and 1974-75, (2) the economic downturn and (3) engineering schools flooding the market with more EE graduates than the market can absorb.

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Sanders' Graphic 7 provides the whole picture by drawing bright, crisp vectors and symbols so rapidly that you see all the data you want. Benchmark tests with actual time measurements have proven Graphic 7 to be the refreshed cost/performance leader. This performance spells results for your application.

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At Sanders we build graphic displays to tough standards and we support them. The reliability of a solid product backed by a solid organization helps keep your job on track.

To make sure you get the whole picture of performance, convenience, and reliability, call us at (603) 885-5280 and let us arrange a demonstration of the Graphic 7.

Sanders Associates, Inc., Information Products Division, Daniel Webster Highway South, Nashua, NH 03061. (603) 885-5280; TWX: 710-228-1894.

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Model 1453 gives you 4-pen, programable multiple-color plotting. The 1553 is a one-pen plotter with low price but high-speed and high resolution. This inexpensive new plotter generates charts of unsurpassed plot quality. Both models plot with speeds of 10 inches per second. Both can give you multicolored graphics over a plotting area of 11 inches by 144 feet.

Color communicates better.

Our ZCHART II Interactive Business Graphics Program generates line charts, bar charts or pie charts with such relative ease that a secretary who's a novice to plotting can produce colored business graphics that communicate as only charts can.

Prices start at less than $6,000. We'd welcome an opportunity to tell you more. Write us. Or better yet, call. **(415) 671-0600.**

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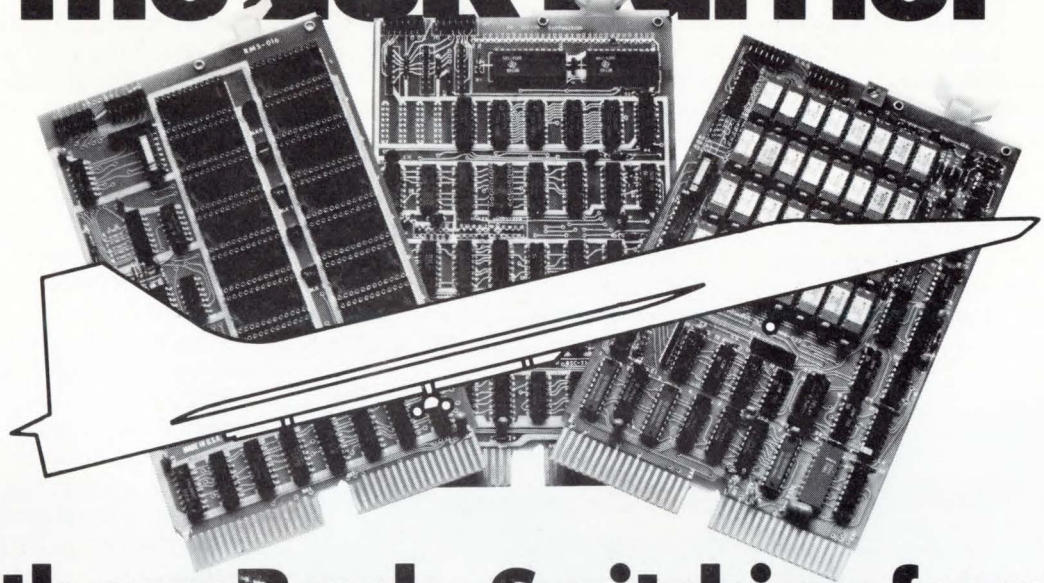
Let your LSI-11* break the 28K barrier



With our Bank-Switching family

In LOCAL mode our memory is functionally just like DEC memory. But when you run out of memory space you're not lost. Add an inexpensive Bank-Switch Controller (BSC-256) and you can go to **two megabytes.** Add another and go to **four megabytes.**

So don't get boxed in with other brands of LSI-11* memory. Break free. Join the family:

RMA-032	32K by 16 bit RAM. On-board refresh	$1200 (Single qty.)
RMS-016	16K by 16 bit ROM. (Intel 2716)	$300 (Single qty.)
BSC-256	The Bank-Switch Controller	$300 (Single qty.)

Substantial quantity discounts are available. For a free copy of our Bank-Switching manual, call or write on your company letterhead.

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DIGITAL PATHWAYS

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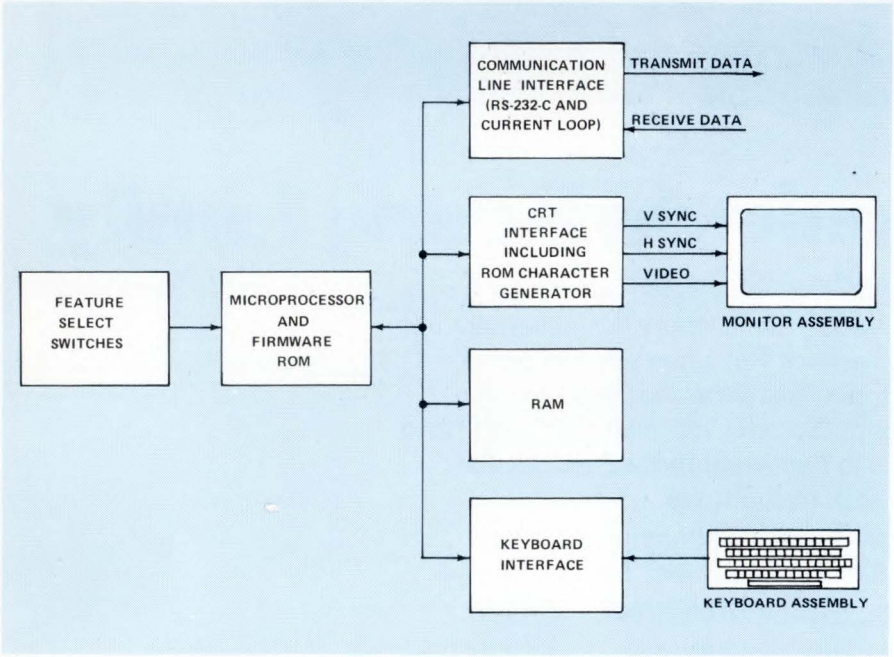
Low Cost No Longer Means Minimal Features in CRT Terminals

Model 510 Data-Screen Terminal features an 80 x 25 display, u & l case, protected data fields, conversational and block data transmission, five video attributes and self test coupled with a price tag before found only on "glass teletypewriter" terminals.

Product conception

Recognizing that a terminal with highly desirable operating features at a truly low price was nonexistent, TEC committed itself to producing this product by defining the required features. Numerous discussions with CRT terminal users familiar with other TEC products, as well as those produced by other manufacturers and a detailed analysis of currently available CRT terminals results in this list of mandatory standard features that became part of the Model 510 design specification:

1. Display: 25 lines of 80 characters (2000 character screen); u & l case; optional international character sets; 12″ diagonal P-4 phosphor CRT and blinking block cursor.
2. Keyboard: typewriter layout with 60 kays; integrated (or shaded) numeric pad; optional separate numeric pad and control keys for cursor movement, TTY lock, etc.
3. Interface: RS-232-C; 110 baud through 9600 baud; serial, asynchronous ASCII, full or half duplex; odd, even or mark parity; optional 20/60 mA current loop and optional auxiliary I/O.
4. Operational features: load/read cursor position; video attributes to include blinking, reduced, inversed, underlined, and blanked data; protected data fields; forward/back tab; page transmit; partial page transmit; line transmit; and optional "line lock" for stable display in 50 Hz power environment.



Model 510 Data-Screen Terminal functional block diagram.

Off-the-shelf parts

One major design question concerned the LSI circuits needed to complement the microprocessor. Should they be custom devices or "off-the-shelf" parts? Although custom circuits held the potential of fewer required parts, three major drawbacks were identified: tooling costs, long lead time and initial parts may contain design faults, causing delays in product shipments. In view of these items, a decision was made to design the Model 510 using off-the-shelf parts.

TEC, Inc., 2727 North Fairview Ave., Tucson, AZ 85705. **Circle 299.**

Largest Bubble Memory Exceeds Eight Megabits

Paul Snigier, *Editor*

With 1792 minor loops, each storing up to 6441 bits with separate accessing R/W lines, the largest experimental magnetic bubble memory (MBM) ever designed crams over 8 megabits onto a 1.3 in^2 chip! Bubble diameter measures 1.7 μm in diameter; per-bit storage area, 64 μm^2; and maximum chip capacity, 11.5 megabits (providing fail-safe redundancy to offset processing defects).

Ion-implantation the key?

What is so unusual about this giant memory chip from Bell Labs is the technology used—ion-implantation—since it could be the key sought by chip designers to raise MBM densities beyond those size constraints set by permalloy guide lines.

Ion implantation, which controls the dopant level, can be applied to P- or N-channel devices, to self-aligned gate devices, to CMOS and in other ways. By implanting dopant ions in the gate region after source and drain formation, it's been used to adjust threshold voltages. The ion accelerator beam current and implant time controls the implanted doping level. Ion implantation fabrication technologies, using self-aligning processes, reduce overlap capacitance, thus increasing speed over *equivalent* diffused devices.

To control bubble trajectory, ion implantation alters the axis of magnetization from perpendicular to parallelling the thin, synthetic magnetic-garnet crystal film, which contains the small magnetic domains. The magnetic gradient moves these domains across the film. A bubble at a specific location indicates a ONE; its absence, a ZERO. Unlike the large semiconductor cells of RAMs, bubbles provide non-

LSI-11*

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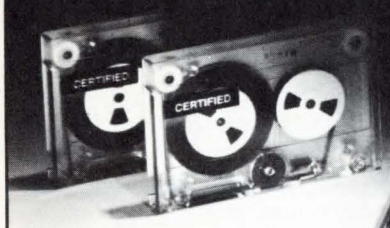

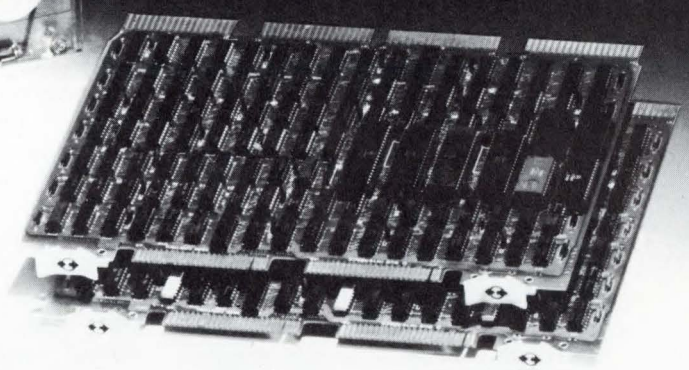

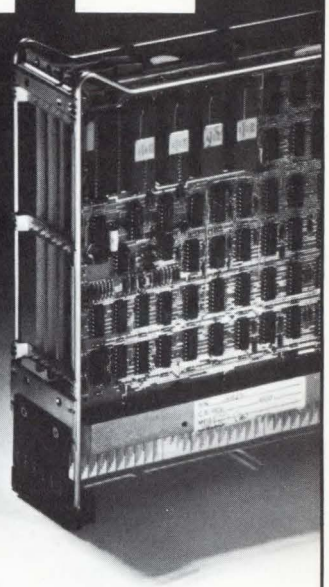

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volatility, pack more bits/device and require less board space. MBM penalties exist: slower access and transfer rates.

Unlike IBM's MBM (which uses one bubble-containing magnetic-garnet layer and a second containing the ion-implanted guiding pattern), Bell's chip has both functions in the same garnet layer. The IBM (vs. Bell) MBM creates higher densities—with 1 (vs. 1.7 – 1.3) μm diameter and 5 (vs. 8 – 6) μm period.

Bell fabricated its MBM chip by: (1) ion implanting through a photoresist mask on the garnet crystal, (2) adding a thick metal (AlCu) overlay for control—i.e., for generating magnetic bubbles and transfer between minor/major loops—and (3) adding a permalloy layer for sensing bubbles.

Bubble trouble ahead?

Although Bell's approach to bubble memory technology yields higher lithographic resolution, other difficulties exist: a critical mask alignment step, a requirement for more masking steps than certain other approaches and failure to incorporate some recent MBM developments (for example, it doesn't eliminate external coils which provide the rotating magnetic fields).

Testing the new MBM chips will pose problems and could be the economic Waterloo of these "monster chips". With quarter-megabit MBM test times ranging all the way up to several minutes/device, and because bubble memories are serial devices, test time increases/device will be more linear than exponential (as in RAMs, ROMs, etc.). This means test time/device could exceed half an hour!

Its not-too-fast clock rates, its high-density shift-register-type architecture and its need for carefully-balanced and timed fields all combine to make testing a difficult matter.

As chip capacity continues upward, both voltage and average access requirements will increase. The only alternative, changing MBM organization, includes placing two major-minor loop chips/die (Bell's Bonyhard organization) or positioning pages with most-recently accessed information near the read port (on-chip cache).

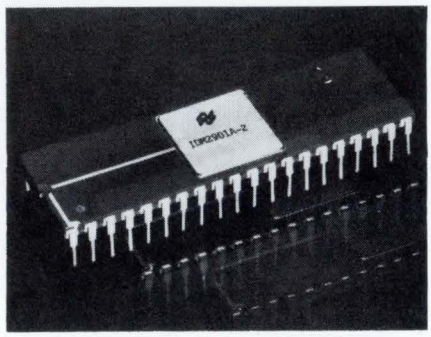
In its design, Bell allocated many extra loops to compensate for defective loops. Since a certain number of loops must inevitably be defective during fabrication of any dense memory device, a test system must locate these defective loops and store their location. Remembering these bad loop locations and their total, errors/loop and total error rates and other variables enable the test system to create a mask register to selectively mask bad loops, so the computer later can't attempt to write in these defective loops. Although some MBM chips use an extra loop with independent transfer gates to store a map of bad loops, it's not known whether Bell's chip uses this approach.

In either case, the new 8-megabit MBM chip demonstrates that increased density breakthroughs are possible via ion implantation. Whether or not commercial bubble makers will incorporate much of the technology into their designs is another story.

Third-Generation 4-Bit μC Reaches 60 nsec

National Semiconductor Corp. is developing an even faster version of its Schottky-Coupled-Logic IDM2901A 4-bit slice μP which is capable of microcycle times as low as 60 nsec.

Like the earlier IDM2901A and IDM2901A-1, the new third generation device — designated the IDM2901A-2 — is 100% functionally-



compatible with currently available and slower low power Schottky devices, and features DC performance levels which meet or exceed those of competing LS designs. The new device allows the design of systems which can perform a simple "add" as quickly as 67 nsec and a more complex add and shift (multiply) in only 78 nsec. By comparison, the original IDM2901A performs such operations in 100 and 125 nsec respectively and the second generation IDM2901A-1 in 87 and 105 nsec, respectively.

Double pipeline architecture

Depending on the architectural approach used, significant improvements in system throughput are possible, says Uimari. In the traditional non-pipeline architecture — where microprogram control and ALU execution are serial to each other and the sum of their delays determines the microcycle length — microcycle time ranges from 196 to 270 nsec. In the newer single pipeline architectures — where the arithmetic operations are performed in parallel with the microprogram sequencer operation — system microcycle times in the 130 to 160 nsec range are possible.

To take full advantage of the IDM2901A-2's speed designers of bit-slice-based systems should take advantage of the double pipeline architectural approach used in many large mainframe computers. In this approach, microprogram sequencing, micromemory access and Register/ALU operations are all performed in parallel; that is, while the Register/ALU is operating on one microword, two, rather than one, are "in the pipeline." Using this approach with the IDM2901A-2 results in the delivery of microcode to the Register/ALU in 60 to 80 nsec.

National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051.

128-Kbyte Magnetic Bubble Board Utilities

Intel's IMB-100 ($3900), a 128K byte nonvolatile 1 Mbit bubble memory development board, uses one 7110 MBM module, an 8085A-based controller and standard components. Organized on a 6.75 x 12" SBC PCB, IMB-100 interfaces with Multibus systems. It plugs into only Intellec Series II μC development systems and is used with the ISIS-II operating system. Performance is at a nominal data rate of 68 Kbps. All address, data and control signals are TTL- and Multibus-compatible.

The CPU communicates with an 8085A through a set of registers on the board via I/O commands. The 8085A interprets these registers then controls timing and analog circuits to perform bubble memory accesses. The data is passed via a FIFO on the board also through I/O commands.

A set of software programs for exercising the IMB-100 is included on a double-density diskette (single-density diskette optional). Six programs provide transfers of data between an internal RAM buffer and either a standard ISIS-II device and file, or the bubble memory.

The IMB-100 utilizes the transparent redundancy inherent in the 7110 bubble memory module. The 7110 device is mounted in a socket to facilitate system checkout before applying power. Operation is from 0°C to 50°C over ±12V and +5V DC power supplies.

Intel Magnetics, 3000 Oakmead Village, Santa Clara, CA 95051.

Continued on p. 92

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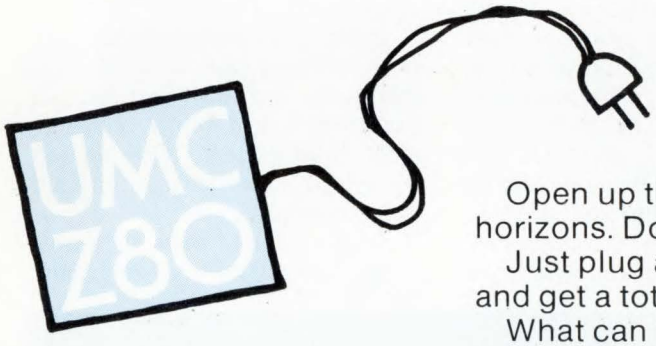

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Many problems encountered during the design of microcomputer-based systems have already led to the introduction of many new design tools. Recent developments, such as faster and more powerful processors, multiprocessor systems and microprogrammed systems, have greatly increased the complexity of design problems.

The problems

Microprocessors have introduced many new problems into digital design. These problems include mixed hardware and software functions, complex signal structures with poorly defined timing, uncertain device characterizations, software debugging and testing, and a general inability to observe overall behavior in a systematic way. The number of new tools to solve these problems is considerable. In-circuit emulators, microcomputer development systems, interactive editors, disk operating systems and ROM simulators are only a few of the hardware and software tools that are available. A reasonably-equipped μC design facility can cost $50,000 or more just to support a $10 or $20 CPU.

Nor are design problems becoming simpler: in fact, they are becoming more complex because of recent developments.

A new generation of μPs with more complex instruction sets, larger memory capacities, and faster cycle times has appeared **(Ref 2)**. The use of processors like Intel's 8086 can make systems like the Aydin Controls 5216 color graphics display computer as complex and as powerful as minicomputer-based systems.

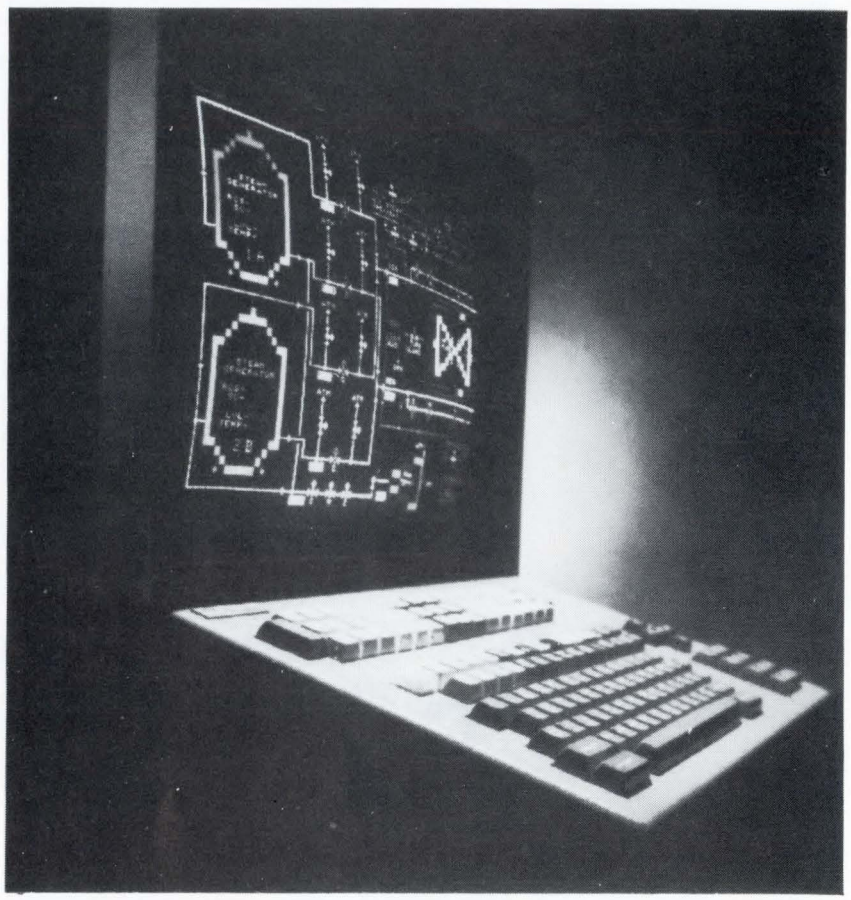
Larger memories at lower cost are available. Intel's 8086 can support up to 1 Mbyte of memory, while Zilog's Z8000 and Motorola's 68000 handle even more. Large memory cards like Vector Graphic's 48K RAM board are now commonly available at prices well under $1000.

Industry is making wider use of multiple processors. The low cost of CPUs means that there is no reason not to use several in a single system. Even large computers such as the Sperry Univac 1100/60 are based on multiple microprocessors **(Ref 3)**. Although the added hardware cost is small, the extra μPs complicate the design, debugging and testing procedure considerably.

Industry is making wider use of bit slices and microprogrammed systems **(Ref 4)**. Applications like Lear Siegler's 415 data processor and the Tektronix 4054 graphic computing system are typical. Such systems are intermediate between μP-based systems and logic-based systems, and have many of the complexities of both.

Industry is emphasizing testability due to high costs of test systems (hardware and software) and of maintenance and repair. Development of adequate software for test equipment, in particular, is difficult and expensive.

What's worse than increasing design complexity? An even more



Model 5216 color graphics display computer, based on the Intel 8086 microprocessor. *Aydin Controls, Inc., Fort Washington, PA.*

annoying problem – lack of qualified personnel. If you read classified ads or trade magazines, you know that there's a shortage of engineers, techs and programmers.

Automating the design process

The solution? Automate the design process. Let computers perform many mundane design tasks and let people add refinements and intuition that machines lack.

One way to automate uses simulation: a computer provides a model that you can check, monitor and test. You introduce changes *without* complex rewiring or development of new PC boards. And, you can interact with the system through the facilities of a powerful computer system.

Simulation cannot replace breadboarding or eliminate the need for a full μP lab. But, you can use it to run feasibility studies, handle functional testing, define and verify system designs, and evaluate performance. You can easily rearrange circuits, add or delete parts, change timing and explore alternative implementations. The system that emerges from the simulation should be reasonably close to a final product; although you still must check precise timing and detailed circuit behavior, and "fine tune" it.

MICROPROCESSORS			
SEM	Description	VLSI Circuit Technology	Application
1. μCPU-1	Microprocessor central processing unit, 8-bit-byte general register; 2 μs R-R, Add	N-MOS, CPU-on-a-chip, (MIL-8080)	• Telemetry • Fuzing • Head control • Autopilot
2. μCPU-2	Microprocessor CPU, 8-bit byte, general register, 600 ms (8080 Emulator)	CMOS-SOS, bit-slice RALU and μCPU hybrids (2900/3000 series or equivalent)	• Autopilot • Head control • Fuzing
3. μCPU-3	Microprocessor CPU, 16-bit word, fixed point, general register; 600 ns R-R, Add	CMOS-SOS, bit-slice RALU and μCPU hybrids (2900/3000 series or equivalent)	• Autopilot (Adaptive)
4. μCPU-4	Microprocessor CPU, 16-bit word, fixed and floating point, general register; 600 ns R-R, Add (1.0 to 3.25 μs flt. pt.)	CMOS-SOS, bit-slice RALU and μCPU hybrids (2900/3000 series or equivalent)	• Signal processing • Estimation • Guidance
HIGH-SPEED ARITHMETIC AND MEMORIES			
SEM	Description	VLSI Circuit Technology	Application
5. HMPY-1	Hardware multiplier, 200 ns, 16 x 16-bit multiply	CMOS-SOS single hybrid	• Throughput enhancement for μCPU, e.g., Class I signal processing
6. μFFT-1	Micro Fast-Fourier Transform processor, 40-400 μs for 64 points, 8 + J8	CMOS-SOS or CCD RALU and μPCU hybrids (2900 series or equivalent)	• Throughput enhancement for μCPUs, e.g., Class II and III signal processing
7. RAM-1	Random-access, read/write memory, medium speed, 128-2 K bytes, 500 ns max. access time	N-MOS DIP hybrid	Data • Telemetry • Fuzing • Head Control • Autopilot
8. P/PROM-1	Programmable (mask/electrically) read-only memory, medium speed, 1K-16K bytes, 500 ns max. access time	N-MOS DIP hybrid	Programs
9. RAM-2	Random-access, read/write memory, high speed, 256-1K x 16 bits or 256-2K bytes, 100 ns max. access time	CMOS-SOS DIP hybrid	Data • Signal Processing • Estimation • Head Control • Autopilot • Fuzing
10. P/ROM-2	Programmable (mask/electrically) read-only memory, high speed, 1K - 4K x 16 bits or 1K-8K bytes, 100 ns max. access time	CMOS-SOS DIP hybrid	Programs
INPUT - OUTPUT			
SEM	Description	VLSI Circuit Technology	Application
11. DMAIO	Direct-memory-access input-output channel, parallel word/byte transfers to/from micro-computer RAM	CMOS-SOS bipolar single hybrid	All microporcessor applications
12. PDIO	Parallel digital input-output channel, parallel discrete transfers to/from μCPU	CMOS-SOS bipolar single hybrid	• Telemetry
13. ADAC	Analog-to-digital/digital-to-analog input-output channel A-D: 8/16/24 chs. sim. S/H mux 8/10/12-bit. A/D 3/6/8 μs max/ch D-A: 8 chs. demux., S/H, 12-bit D-A, 5μs max/ch.	CMOS-SOS single hybrid	• Head control • Autopilot • Telemetry • Radar receiver
14. SDIO	Serial digital-input-output channel, word and bit serial-data/command transfers. 1Mbit/s max., MIL-STD-1553A	CMOS-SOS single hybrid	• Avionics • Inter microcomputer

S/H - sample-and-hold
Mux - multiplexer
Demux - demultiplexer

Modules Simulated By Raytheon's CAD System.

Simulation system requirements

To be useful, a simulation system must contain the following:

- A method for describing complex devices, such as μPs, memories, interface chips, peripheral controllers and such functional subsystems as arithmetic processors, multipliers and signal processors
- A library of models for common processors and other devices
- An ability to model clock control, memory timing, interrupts, DMA and other common signal structures
- Adequate facilities for the development and loading of programs
- Interactive debugging facilities, sc that the user can easily observe the system behavior.

Obviously, the system should be relatively small, capable of running on different computers, fast-executing and compatible with standard operating systems and code generation procedures. Is the simultaneous achievement of these characteristics simple? No.

It's good to integrate everything into one CAD system to handle simulation, generation of hardware and software, debugging, testing and documentation. Models developed in design stages should be directly usable in test and evaluation.

Examples of Simulation Systems

Here are simulation systems: one which runs as part of Raytheon's CAD system **(Ref 5)** and the N.mPc (pronounced as if the "." were the word "dot") system from Case Western Reserve Univ. **(Ref 6-9)**. Both offer these features:

- A register transfer language **(Ref 10-14)** provides functional descriptions of μPs and other devices.
- Some device models are available, most notably the Intel 8080 family; others are either in development or can be produced in a reasonable amount of time by an experienced programmer.
- Gross timing can be modeled, usually in terms of single clock cycles, so that the user can check synchronization at that level.
- Interrupts, DMA and other control signals can be modeled, though their use slows the simulation, and the structures are often somewhat cumbersome.
- The package is integrated into an overall computer system, which makes a range of tools available to the user.

In particular, Raytheon's system is based on the hardware description language CDL, **(Ref 12)** which is widely used, but has limited ability to model multi-phase clocks, data bus arbitration or interrupts. It contains a full board design automation system that includes packages for circuit analysis, board design, test generation and reliability analysis, plus a large CDC-6700 computer facility.

The **Table** describes the modules that have been simulated in this system. Note that the simulation in the package we are describing is at the register or functional level only – not at the gate level. Clearly the package can support the modeling of a wide range of μPs and other devices, though the signal structure is somewhat limited and models are somewhat difficult to implement.

The N.mPc system is based on the hardware description language ISP **(Ref 13)** which was designed specifically to allow description of multiple processor/module architectures. ISP can synchronize module activities and separation of events in time. It contains the UNIX OS, a time-sharing system with a wide range of interactive utilities and other systems programs **(Ref 14)**, plus any of a range of PDP-11 computers from the small PDP-11/34 to the large PDP-11/70.

The modules that have been simulated in M.mPc include most of the 8- and 16-bit μPs and their associated families of chips. The 8080 family has been modeled completely; and several microprogrammable devices, including the AMD 2900 family, have been modeled. The system's developers estimate that an experienced user can model a new family with just a few days of work.

The N.mPc system provides the obvious advantage of running on a reasonable-sized mini under a powerful time-sharing operating system. Typical execution speeds for simple models are 100 to 200 instructions/second on a PDP-11/34 and 500 to 1000 instructions/second on a PDP-11/70. Certainly, the introduction of the DEC 32-bit machine, the VAX-11/780, could provide even higher speeds. Extensive facilities are available for users to interact with the simulation, save its current state, control its execution and collect statistics.

Neither of these systems can run in anything like real time. Remember that a standard 8080 CPU works at 2 MHz and executes an average instruction in 2 to 3 μsec. Thus, you don't want to debug long programs in this way (nor would you care to afford such debugging sessions). As with most simulations, be careful not to overspecify the system and degrade execution time. While simulation can be a very useful approach, very carefully define information you want or you risk running up a lot of costly computer time.

Current State and Availability

Raytheon's system is presently running on an in-house Control Data 6700 at its Missile Systems Division, Bedford, MA. Those interested in the system should contact the program manager. Frank Langley at the Missile Systems Div. of the Raytheon Corp. in Bedford, MA 01730.

The company plans to improve the interrupt structure, allow use of subprograms to describe functions like arithmetic processors or signal processing chips, and extend or replace the hardware description language.

The N.mPc system is also currently operational. It includes its own microassembler which can produce the required object code for a variety of CPUs. The maker plans to provide a generalized compiler, allow the linking of C **(Ref 15)** programs to describe functions like arithmetic processors or signal processing chips and offer more user facilities. This system can be licensed. Interested? Contact: Dr. Fredric Parke or Dr. Charles Rose at the Computing and Information Sciences Dept. of Case Western Reserve Univ. in Cleveland, OH 44106, or call (216) 368-2800.

Note that this system can run on any PDP-11 that supports the UNIX operating system; however, UNIX itself must be licensed separately (at no small expense). The system is written in C and could possibly be transferred to other computers that can run that language, though it is greatly dependent on the facilities of UNIX.

Acknowledgments

Much of the information on Raytheon's system was obtained from articles in Simulation *magazine and in various conference proceedings. Dr. Ralph Martinez of General Dynamics/Convair brought this work to our attention. Much information about N.mPc was presented at the Design Automation Conference by Dr. Fredric I. Parke, Dr. Charles Rose and Mr. Gregory Ordy of Case Western Reserve Univ. and Mr. Larry Rogers of Western Electric. We thank them for sharing this information with us.*

References

1. Schweber, Bill, "Setting up a Microcomputer Development Lab", *Digital Design*, May 1979, pp. 42-49.
2. Snigier, P., "μP Selection: Some Do's and Don'ts – Part One", *Digital Design*, April 1979, pp. 28-32.
3. Borgerson, B.R., "The Viability of Multimicroprocessor Systems", *Computer*, January 1976, pp. 26-30.
4. Alexandridis, N.A., "Bit-Sliced Microprocessor Architecture", *Computer*, June 1978, pp. 56-80.
5. Langley, F.J. et al., "Simulating Modular Microcomputers", *Simulation*, May 1979, pp. 141-154.
6. Parke, F.I., "An Introduction to the N.mPc Design Environment," *Proceedings* of the 1979 Design Automation Conference, San Diego, CA, pp. 513-519.
7. Rose, C.W. et al., "The N.mPc System Description Facility," *Proceedings* of the 1979 Design Automation Conference, San Diego, CA, pp. 520-528.
8. Parke, F.I. et al., "The N.mPc Runtime Environment", *Proceedings* of the 1979 Design Automation Conference, San Diego, CA, pp. 529-536.
9. Ordy, G.M. and F.I. Parke, "An Evaluation of the N.mPc Design Environment", *Proceedings* of the 1979 Design Automation Conference, San Diego, CA, pp. 537-542.
10. Su, S.Y.H., "A Survey of Computer Hardware Description Languages", *Computer*, December 1974, pp. 45-51.
11. Lipovski, G.J., "Hardware Description Languages", *Computer*, June 1977, pp. 14-17.
12. Chu, Y., "Introducing CDL", *Computer*, December 1974, pp. 42-44.
13. Barbacci, M.R., "Instruction Set Processor Specifications for Simulation, Evaluation, and Synthesis", *Proceedings* of the 1979 Design Automation Conference, San Diego, CA pp. 64-72.
14. Ritchie, D.M. and K. Thompson, "The UNIX Time-Sharing System", *Communications of the ACM*, July 1974, pp. 365-375.
15. Kernighan, B. and Ritchie, D.M., *The "C" Programming Language*, Prentice-Hall, Engelwood Cliffs, NJ, 1978.

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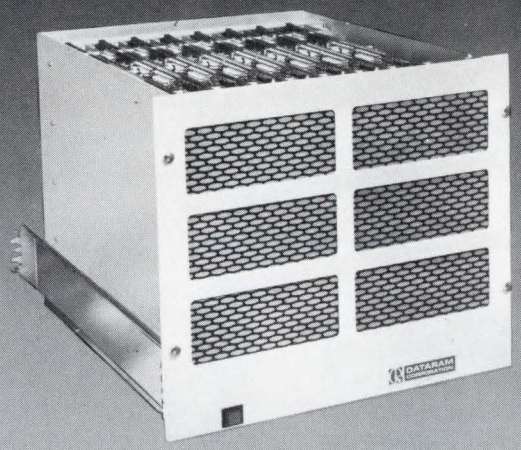

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New CRT Graphics Display Technology Broadens Uses

Loren Werner
Vector General, Inc.
Woodland Hills, CA

Although interactive CRT graphics systems are becoming increasingly familiar in a wide range of engineering, scientific and industrial applications, many people in these fields, and in computer operations as well, are not familiar with how these systems work and how they can be put to work.

The capabilities of 2-D and 3-D graphics displays can help impart a great deal of information exchange between the computer and the operator. Not all data lends itself to the graphics format, of course, but graphics, and the appropriate software, can contribute in an unparalleled way with any data that can be transformed into display format.

To make full use of this technology, some insight into its design and function will make the overall system more readily understood and, thus, more useful.

One of the more advanced CRT graphics display systems available today is our recently announced 3300-Series.

The 3300 may be interfaced with a computer system using standard I/O techniques. The system interacts with a program by accepting inputs from the host computer and/or external devices, and displays the pictorial data on the face of the CRT. The information may be displayed 2-dimensionally, or 3-dimensionally with intensity modulation.

The CPU composes the desired display information into a display list. This is very similar to a computer program, containing instructions and data for drawing lines and characters on the screen, specifying display control parameters, and controlling the sequencing through the display list.

The 3300-Series is of modular design, with modules providing the basic functions of the system, as well as making for convenient incorporation of options into the system (block diagram).

Four modules comprise the interface to the host computer: The I/O interface, micro-programmed controller (MPC), the programmed input/output-direct memory access (PIO/DMA) adapter and the refresh memory. This segment of the system architecture is concerned with control of the display system, the placement of display lists in the refresh buffer for maintaining a picture on the face of the CRT.

Micro-programming (through the MPC) is used to adapt the system to various host computers. By changing the I/O interface board, which provides circuit interfacing to the I/O bus of the host computer, the MPC handles variations in timing and instruction format.

The refresh memory can be on one or two boards, each holding up to 64K 16-bit words of memory. It is a dual-ported memory which can be accessed by both the MPC (for loading of display lists from the host computer), and by the display refresh controller. Originally, computer memory was used to store the display list. This meant that each word of the display list had to be pulled through the computer I/O bus. This could interfere with computer operations and meant that it took longer to access each word in the display list. With the 3300's off-line refresh buffer, it is not necessary to go to the computer; and access to the display list by the display refresh controller is significantly faster. The MPC is micro-programmed to block-transfer information into the buffer, using the DMA facilities of the host computer.

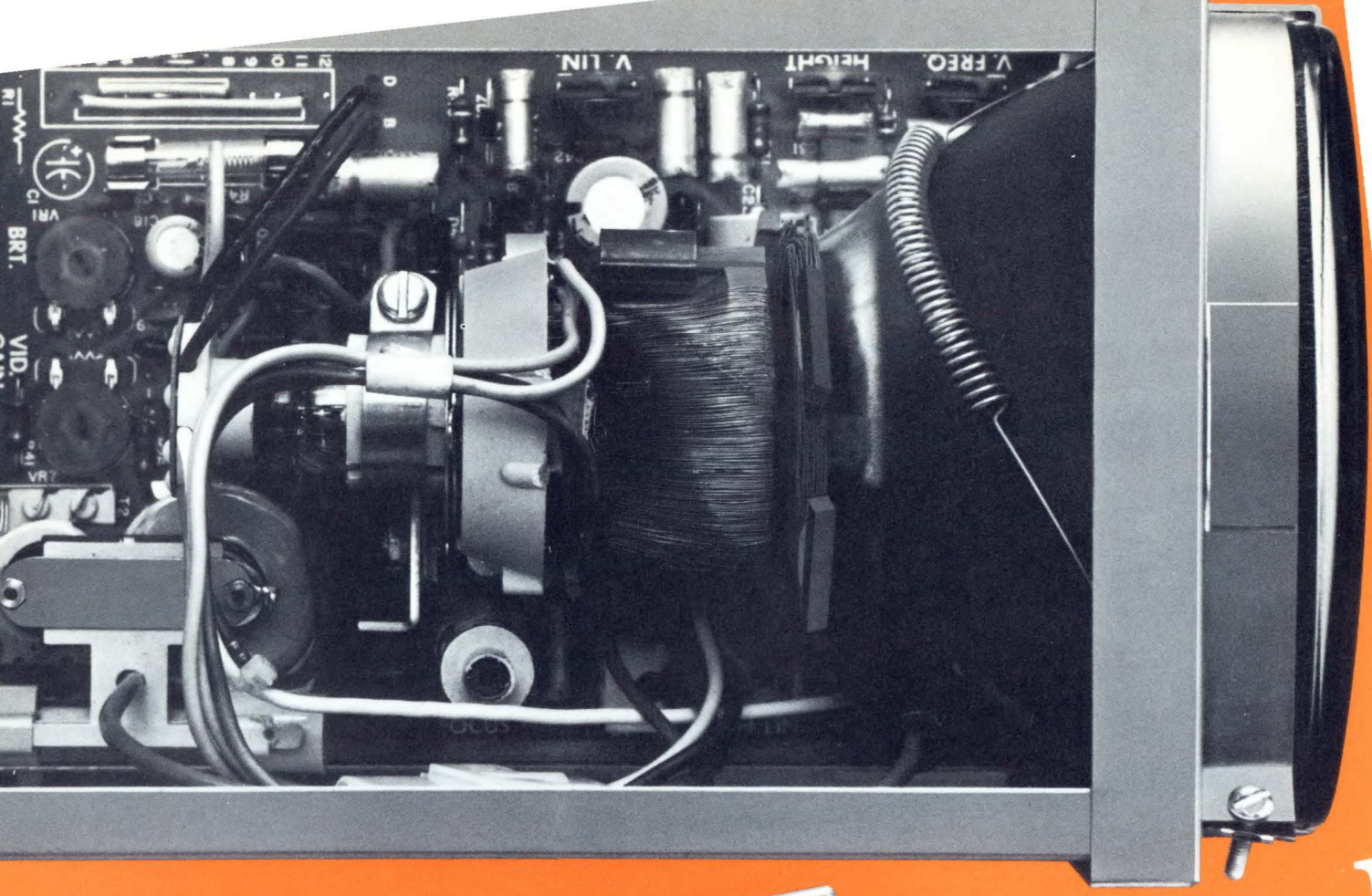
Through the use of a dual-ported memory, rather than one memory going to one common bus, loading the memory from the computer creates virtually no interference in the running of a display list. It is possible to run display lists from one part of the buffer, while simultaneously loading another display list, without that loading affecting information on the face of the CRT.

The PIO/DMA adapter basically controls display controller access to the refresh buffer and passes through the programmed I/O to the computer.

The input/output controller extender (IOCX) and the I/O controller (IOC) are the heart of the display refresh controller, which is based on bipolar bit-slice micro processors with a 16-bit wide data path and 1K words of 48-bit control firmware stored in PROMs. The B bus is the internal processing bus of the IOC, and is used for all of the internal transfers between registers, etc. It is a synchronous bus that is totally controlled by the IOC.

The 3300 utilizes a "pipeline" approach, rather than a common bus. The common bus approach employs one data bus, extending from the I/O interface to the vector generators. Each unit transferring data from or to another unit, must become master of the bus, and enter its data on the bus. Each data transfer uses bus time that might otherwise be used by the display controller to transfer data to the vector generator. With the pipeline approach, where each transfer has a dedicated bus, the MPC can transfer data from the computer to the refresh buffer, while a display list word is being accessed from the refresh memory into the front-end of the IOC circuitry.

Simultaneously, with the previous word being processed in the IOC, prior words are being processed in the 3-dimensional transfer unit, and the vector generator is drawing the line processed previously. None of these transfers interfere



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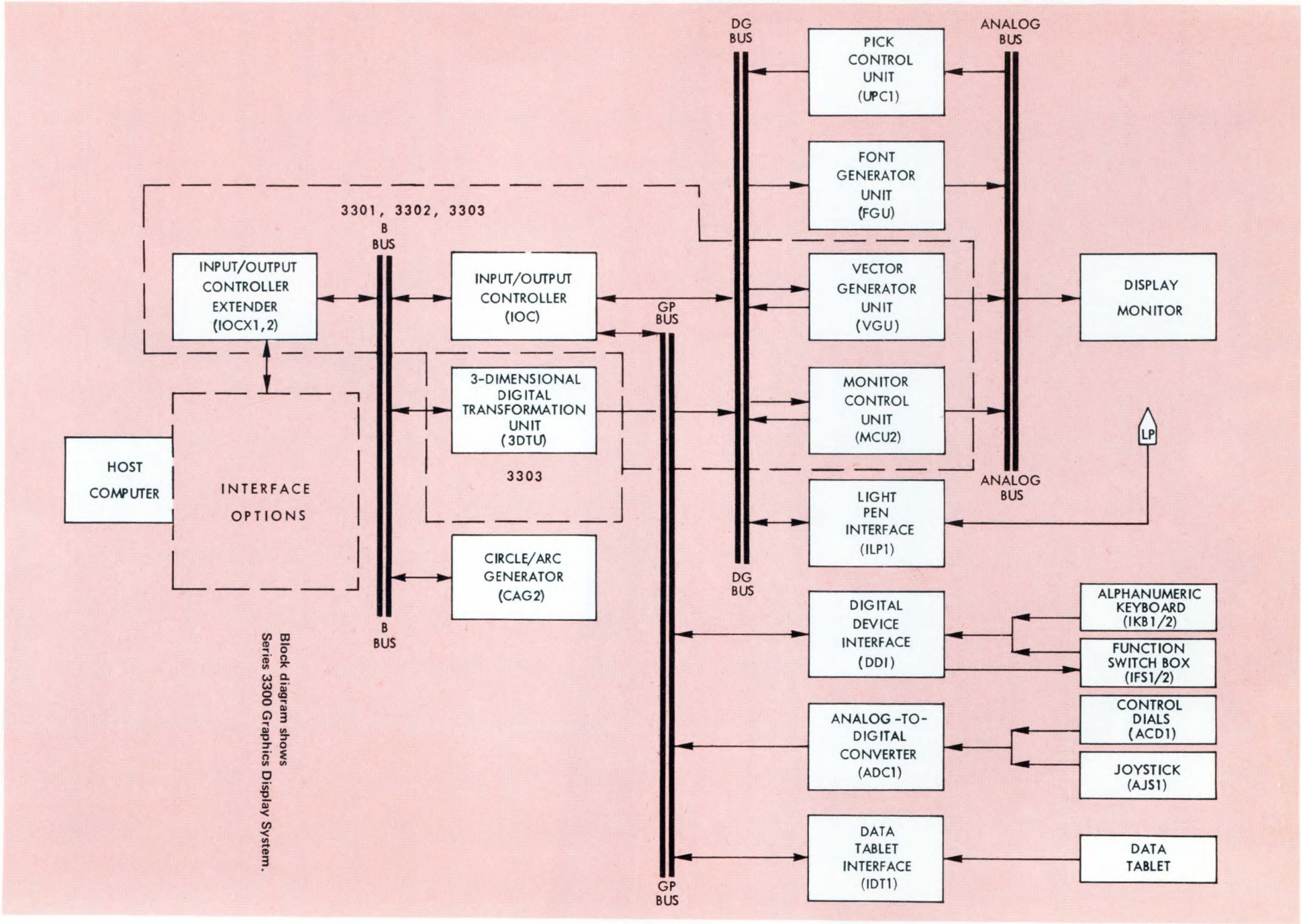

Block diagram shows Series 3300 Graphics Display System.

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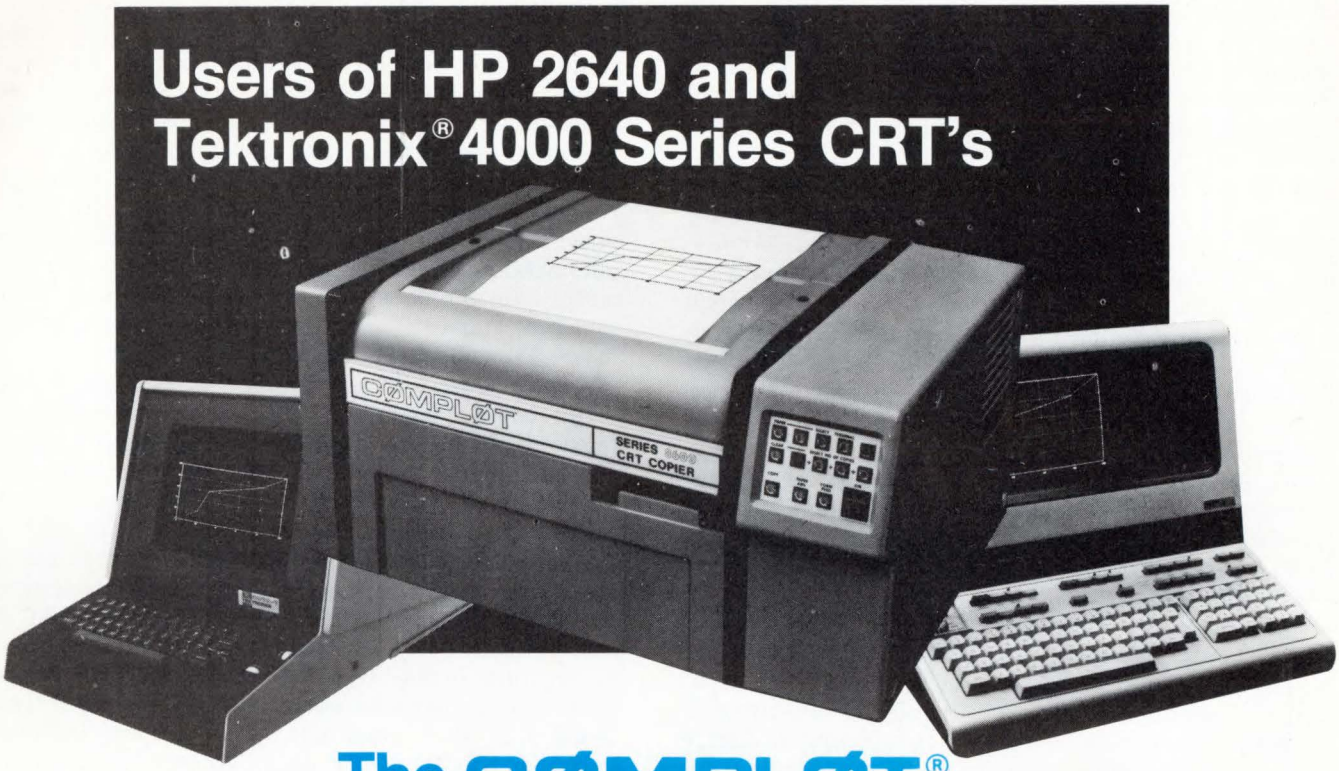

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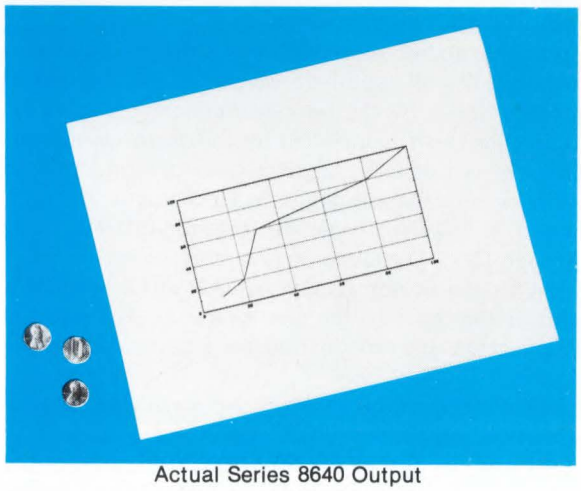

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with each other.

If, for example, the vector generator is drawing an extremely long line, which takes a relatively long period of time, the other units can be stacking up the next vectors, ready to proceed when the line is completed. This also prevents interference between front-end loading and the drawing of vectors.

The IOC has several basic responses: first, there are programmed I/O requests from the computer. In response to these requests, outputs will, typically, start display lists, acknowledge interrupts and initialize the address pointer into the refresh buffer.

A second function of the IOC is to handle peripherals. For example, when a switch on a function switch box is activated, or a key on the keyboard is depressed, an interrupt is sent back to the IOC. The IOC then reads in the appropriate information and stores it. If that key or switch is supposed to interrupt the computer, then the IOC sends the interrupt to the computer. In addition, requests for analog values are handled by the IOC. This function is performed on the GP bus, which is a 16-bit bus with full interrupt protocol.

The primary function of the IOC is to process the display list. Given an initial address into the refresh buffer, it can then read out successive words, some of which will modify parameters such as intensity, scale, displacement, 3-D rotation, etc.

The IOC goes through the display lists, picking up successive words. The micro-programming makes instruction and register definitions possible at any time, move registers, etc. Control information is transferred directly from the IOC to the DG bus, and then to the appropriate display generator. Vector information is sent by the IOC, on the B bus, to the 3-D transformation unit. This unit works independently of the IOC to take the X-Y-Z coordinates of each vector endpoint, apply a 3 x 3 transformation matrix and end up with a 3-D transformed end-point. This is then sent directly out on the DG bus to the vector generator. This transformation involves a total of 9 multiplies and 3 summations of 5 terms each. This entire operation is done in approximately 1.4 μs. It is accomplished by using 3 16-bit x 16-bit bipolar multiplier chips.

The primary module on the DG bus is the vector generator, which handles all vector draws and moves. Individual characters are drawn by the font generator, but spacing between the characters is controlled by the vector generator. The IOC, in processing character information, utilizes PROMs that specify the spacing for each character and each possible size. It takes the constants from the PROMs, sends them through the 3-D transformation unit, as vector information, on to the vector generator. The vector generator then controls the move to the next character. The user can specify special spacing information for a particular character set.

The 3-D transformation of the move means that character information can be moved with a 3-D object on the face of the CRT and, in fact, if the font generator includes the character rotation option, the individual characters can also appear to turn as the object is being rotated.

The font generator is a special vector generator. The difference is that it draws over a relatively small area. Instead of a 4096 x 4096 matrix, it draws over a 32 x 32 matrix. What it draws is based on PROMs on the font generator that are basically a display list. Fonts and/or characters can be changed by changing the PROMs. In addition, there is a programmable font board that can be attached to the font generator that supplies RAM memory. It can be loaded from the display list, through the IOC, and can be substituted for the PROM to draw characters as defined by the user.

The monitor control unit (MCU) performs three basic functions: It selects which display monitor(s) on which portions of the display list are to be displayed, controlling up to six monitors. Another function of the monitor control unit is involved with color monitors. Data in the display list selects colors on the monitors, and the MCU has a special cable that connects to color monitors so that various portions of the display list can be in color.

For some color monitors, the speed at which the vector is drawn is based on the color being drawn. Red must be drawn slower than green, for instance. The MCU has the information and control logic so that, based on the color, information can be sent to the vector generator and the font generator to control the velocity at which the beam moves across the face of the CRT.

The circle-arc generator option is an example of the use of the micro-programmed IOC to generate special display functions. Its logic board comprises PROM look-up tables, and computational circuitry. When circle arc instructions are recognized in the display list, the IOC controls the computation that leads to the desired display. The circle arc option can draw circles based on a point on the circle and the center of the circle. Clockwise and counterclockwise circular arcs can be produced, between a start point and an end point, based on a center point. On-axis elipses can be vertically or horizontally oriented. The CAG can also draw n-sided polygons where n is any number between 2 and 512. Other commands include 2-D and 3-D quadrilateral draws. These commands generate a fan of lines within a quadrilateral area to provide filling or shading.

There are several areas of engineering to which computer graphics has become an almost indispensable tool. Chief among these are computer aided design and structural analysis. CAD used graphics systems in conjunction with automated drafting tables to help develop designs faster and with greater accuracy than the older hand-drawn methods. The speed of the CRT and the computer allow for rapid updates. In addition, the amount of materials used is greatly reduced. CAD is widely used in many major industries, including automobile and aircraft design.

Computer graphics has been valuable in structural analysis work from two angles. On the front end it has allowed engineers to develop complex finite element models for stress and thermal analysis, with a savings of several man-months/model.

Several software packages exist which make use of the power of computer graphics systems to generate these models very rapidly. After processing, graphics systems allow for very effective data reduction and presentation, especially in the animation of structures in dynamic analyses.

Other applications of computer graphics include command control, signal analysis, data reduction, simulation, war gaming, printed circuit layout, architectural design, molecular modeling, medical support and cartography. The uses for computer graphics are being expanded every day.

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AED ANNOUNCES ITS NEW LSI-11 LINE-UP.

Low priced RX-02® emulator

The quarterback for the LSI-11 team is the new FLEX-02, a dual-width floppy disk controller/interface card. The FLEX-02 earned its starting role by proving its ability to completely emulate DEC's RX-02 while offering RX-02 users double-headed drive capabilities — a feature no other league quarterback has right now.

Best of all, in OEM quantities the single bluechip FLEX-02 dual-width PC board costs just $700, including the bootstrap loader. (Try getting a 'quarterback' with this kind of talent elsewhere at the same price).

In full gear, a two-drive double-headed disk system with an AED power supply in a 5¼" DEC look-alike cabinet is only $3940 for quantity one. The complete double-drive, single-headed system is just $3440 in a quantity of one.

Whether you have RSX-11/M, RT-11V3A/B, I.A.S., RSTS-3, CTS-500 or CTS-310 operating systems centering the ball, the versatile FLEX-02 can now complete the line-up and lead your DEC data to the end zone.

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RL-01® compatible Winchester

The linebacker for our LSI-11 team, the WINC-01, is surprisingly small for a pro. He consists of just two PCBs — one a microprocessor-based formatter/controller mounted with a SA-4008 drive, and the second, a dual-width Q-BUS interface card that inserts directly into the CPU backplane.

However, when WINC-01 proved he could deliver Winchester technology to DEC LSI-11, -11/2, -11/23 users, we signed him up immediately. He amazed us by playing with up to three SA-4008 Winchester drives and tackling up to a total of 60 megabytes of data. Additionally, he has the capacity to include a plug-in floppy disk drive.

Best of all, he bunked with the DEC RL-01 driver software and we can report they are very compatible up to 20 megabytes.

In contract talks, the WINC-01 demanded considerably less than the DEC hardware: his two boards sell together for under $1150 in OEM quantities. The complete system, including the two PCBs, an AED power supply, one SA-4008 drive and a DEC look-alike cabinet sell for $6700 in quantities of one.

For WINC-01 technical information and quick delivery, contact Bob Deisher, Rigid Disk Products Manager.

Full-color graphics system

The coach of LSI-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in high-resolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

Other features that make the new LSI-11 coach' a cost/performance leader include:

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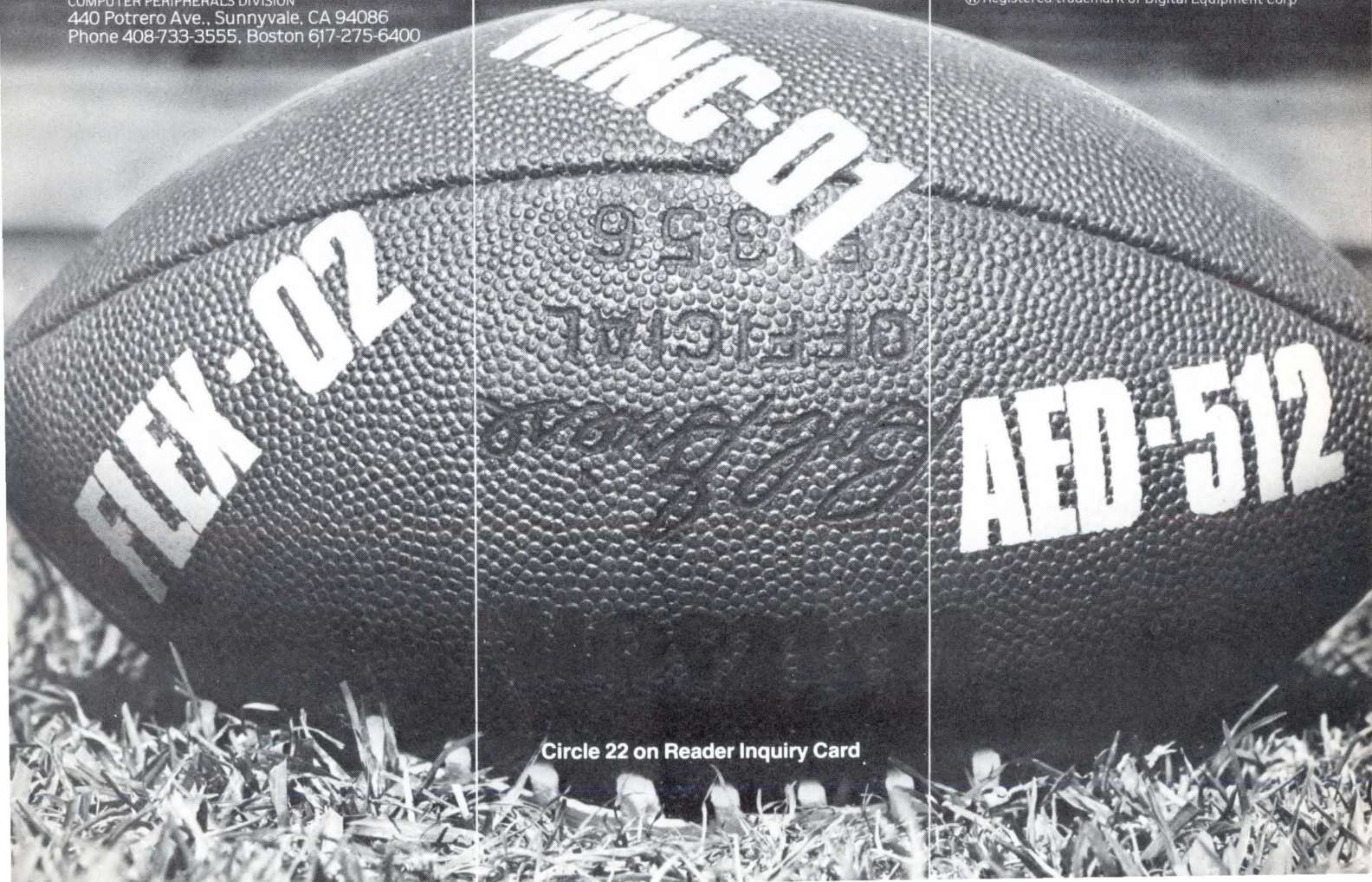

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FIGHTING FLICKER in Raster Graphics

J.V. Howell
Genisco Computers
Irvine, CA

Because of low-cost television CRT technology and low-cost dynamic MOS RAM memory technology, raster graphics displays are providing cost-effective graphics displays. Early raster graphics displays had resolutions of 320 elements by 240 lines – roughly comparable to display resolutions of commercial TV. Flicker, (caused by longer display persistence over the eye's natural persistence) was an insignificant problem because a display resolution of 320 elements by 240 lines easily fits within a single field of standard (commercial) TV. Television in the U.S. provides 525 lines each frame, 480 to 486 lines viewable, with two interlaced fields per frame, and with a 59.97 Hz field rate. The refresh rate of the 320 element by 240 lines display was then effectively almost 60 Hz because the display was repeated in each field. Adjacent lines were identical in the interlaced frame, causing them to merge into one at observing distances. Non-interlaced operation merged adjacent lines into one on the face of the CRT. The 60-Hz refresh rate applied to CRT phosphors used in commercial TV yields a persistence factor exceeding the normal photopic (cone) vision of most observers, thus eliminating flicker.

Graphics display users began to demand increased resolutions. As display controller memory costs decreased, designers responded by providing graphics displays with medium resolution of 512 to 640 elements/line, and 480 to 512 lines. High-resolution graphic displays were obtained with 1024 to 1280 elements/line and 960 to 1024 lines. The result, however, produced an annoying flicker, particularly in displays of individual horizontal lines which had been refreshed at only 30 frames/second.

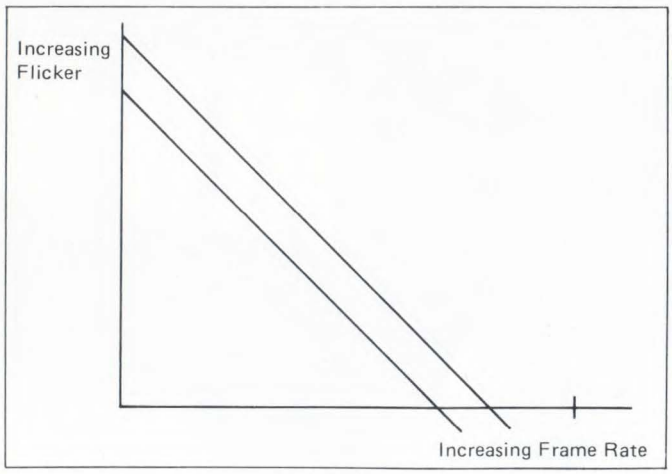

Fig 1 With increasing frame rate, observer sensitivity to flicker drops.

Observer sensitivity to flicker is inversely proportional to the refresh or frame rate **(Fig. 1)**. Such displays gained acceptance for presentation of complex graphics or images (pictures) because information content varies gradually from one line to the next. Such displays provided pairing which reduced flicker to an acceptable amount. An anomaly was created. Complex graphics and image display systems required expensive display controllers because large image memory was required to provide smoothly varying shading in monochrome or color. Lower performance CRT display was refreshed at 30 frames/second. On the other hand, simpler, less expensive displays using less memory to provide line drawings and alphanumerics, required higher performing CRTs refreshing at 60 frames/second to eliminate annoying single horizontal line flicker.

CRT displays containing longer (more slowly decaying) phosphors, (the TV industry standard P4) may be used to eliminate flicker at some sacrifice of cost effectivity, availability, sharpness, and contrast for **static** displays. **Dynamic** (changing) displays, on the other hand, leave undesirable trails on long phosphor CRTs. Overall, however, the industry standard or equivalent is more desirable.

Monochrome CRT displays have recently been developed for use in word processing systems. These CRTs display 8-1/2″ X 11″ printed-page information with high quality characters and achieve a 60-frame-per-second refresh rate. The new CRTs gained quick user acceptance because flicker was eliminated and because with newly developed high performance semiconductors horizontal frequencies could be increased. CRT display costs have been reduced below those of high-resolution TV monitors (not offering equivalent horizontal frequencies). This reduction of costs was achieved by eliminating many classic TV monitor features. Circuit simplification was obtained by using available semiconductor components. Such a CRT display offers the

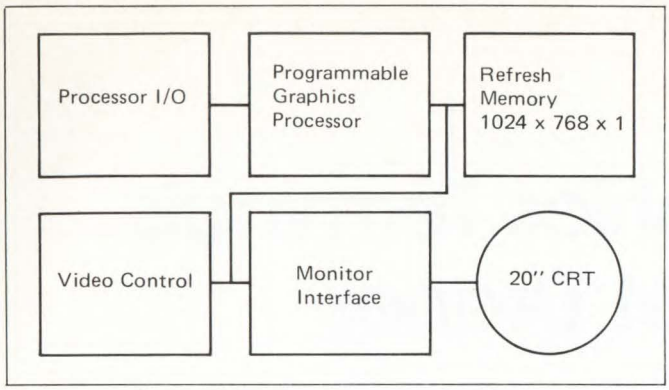

Fig 2 Monochrome display controller Model CT-3400 is optimized to drive a CRT display.

following performance specs: horiz. freq., to 50 KHz; horiz. retrace, no more than 5 μs; vert. retrace, no more than 666 μs; video BW, greater than 75 MHz; display size, 20″ diagonal, 13.3″ X 10″ usable.

A display controller optimized to drive such a CRT display **(Fig. 2)** consists of five 15″ boards housed in a low-cost, 5-card, rack-mountable chassis.

The processor I/O card allows the display controller to be connected to most popular midi, mini and μPs serving as the user's host computer. The Programmable Graphics Processor is a high-speed Schottky TTL processor which provides operational modes such as X/Y raster, alphanumeric, memory clear/set, cartesian, graphic memory readback, point-to-point vector and incremental vector. Program download capability is also included which allows the user to write his own application programs. The video control board provides all CRT synchronizing signals, memory timing, refresh readout address generation, and a buffer of overlay programs by the graphics processor. The 1024 elements by 768 lines refresh memory (1024 X 1024 addressable, 1024 X 768 displayable) provides a full bit map of the display. Interlaced memory cycles provide a 64.7 Megabit/second rate to refresh the CRT display and a 1 Megabit/second write-rate for the graphics processor. Refresh data from the refresh memory is received by the monitor interface board on four separate lines (16.2 MHz rate) and serialized to 64.7 MHz for transmission to the CRT display.

ABOUT THE AUTHOR

J. V. Howell is Vice President of Engineering at Genisco Computers, a Div. of Genisco Technology Corp., where his responsibilities include New England Development in graphics display systems. Mr. Howell holds a BS in Physics from Davidson College and an MS in Applied Mathematics from North Carolina Univ.

Rate this article: circle 3L, 3M or 3H on Reader Inquiry Card.

Computer Graphics Terminals Track Target Drones

Engineering Staff Report
Megatek Corp.
San Diego, CA

Computer-generated graphic displays provide flexibility and capacity for change and growth. Possibilities for manipulating displays and data now go far beyond the old electromechanical plot-board. Possibilities of changing basic types of display presentations through software offer a new degree of freedom to display operators using such systems and to those who have to plan how to use it in the future. Let's examine one successful application.

Graphic terminals replace plotters

The U.S. Navy's Pacific Missile Test Center, Point Mugu, CA, goes about its task of testing the missiles under development to upgrade the shipboard and aircraft firepower.

The new computer-graphics system, Graphic Target Data Display (GTDD), utilizes a Megatek 5000 vector refresh graphics system driving four 21" CRT display monitors. The graphics system software resides in a general-purpose 16-bit computer with 32K of core memory; two additional computers, each with 96K of memory, perform tracking and control functions for remotely-controlled target drones.

Toward an integrated system

The Motorola-developed system, Integrated Target Control System (ITCS), was implemented in various phases and at a number of Naval installations since 1970. The most recent implementation is the four-to-eight-target system at Point Mugu's Pacific Test Center – the first to utilize Megatek's GTDD.

Command and signal frequencies for previous target control systems were in the UHF band, 405-550 MHz. Crowding of this band – primarily by UHF TV – mandated target control activities be conducted on another band. A microwave band of 4400-5000 MHz was chosen for the ITCS system.

In a typical operation, the station operator establishes the command and telemetry link with the target via acquisition of the target responder signal. Once positive track is established, control is turned over to a target controller at one of the graphics terminals in the GTDD system. This controller "flies" the drone during the remainder of its flight – viewing its movement on the map-like Plan Position presentation on his CRT, monitoring readouts of the drone's telemetry data showing such things as speed, altitude and flight altitude, and literally piloting the drone via a control stick at the target controller's position. Before the drone's fuel is exhausted, its remote operator must fly it to a designated recovery area, where it is parachuted to the water and recovered.

Selection Criteria

Before selecting a graphics terminal, first define your application needs in terms of the following factors:

- cost and cost/performance
- current needs
- growth expectation
- operating environment
- flexibility
- support
- human engineering factors
- manufacturer's reputation
- maintainability
- product service capability
- system criteria

In addition to superior graphics, other considerations exist. Not unlike other information processing market segments, graphics processing has evolved. At the beginning of the cycle manufacturers presented the concepts and let the market do with it what it could. Soon, users discovered graphics to be a very useful tool and defined improvements and refinements (which the industry adapted). But the industry has matured, and now both users and manufacturers are facing other factors.

Although trends are emphasizing superior quality and enhanced capabilities, ease of implementation, software and modularity are some non-technology-related aspects that users are now looking for.

Modularity is important to the OEM; it gives him the opportunity to satisfy his customers' sophisticated applications requirements at lowest cost. Using the building block approach, OEMs can design around a standard shopping list of hardware; they're not locked into one configuration.

Modularity means OEMs can buy little or as much as they need. They get as little as a vector generator and vector processor, the hardware, or can buy a graphics terminal or a complete graphics processing system. With graphic equipment more computer independent — not tied to one mainframe — it's more important that universal computer interfaces, communications capabilities, remote graphic processing configurations and ability and more hardware features be available for users.

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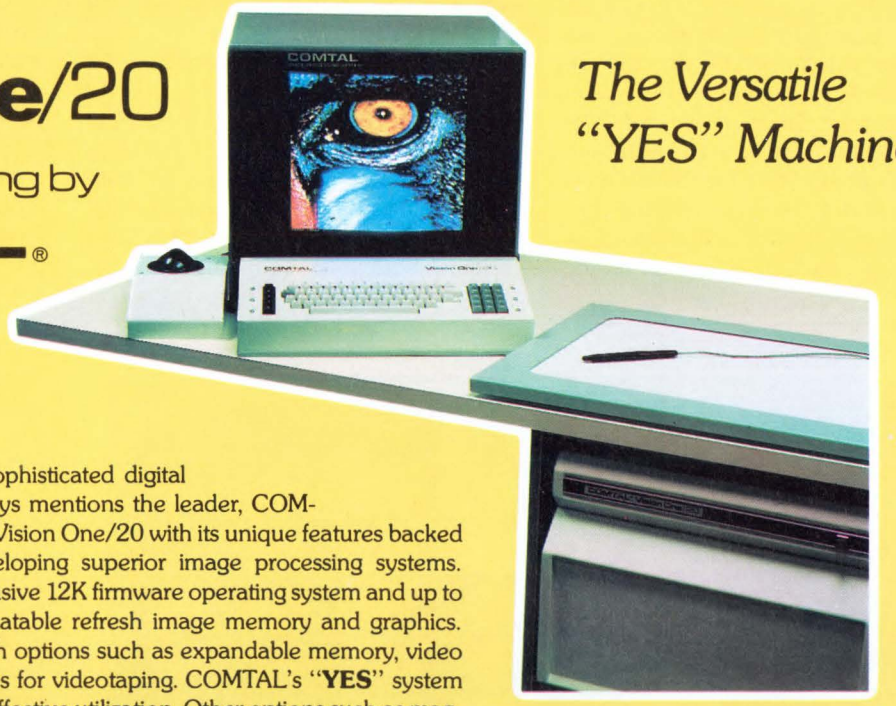

Professional talk about the most sophisticated digital image exploitation equipment always mentions the leader, COMTAL. ☐ **YES**, and that includes the Vision One/20 with its unique features backed by the experience gained in developing superior image processing systems. ☐ **YES**, Vision One/20 has an exclusive 12K firmware operating system and up to 48 megabytes of dynamically allocatable refresh image memory and graphics. ☐ **YES**, field upgradeability through options such as expandable memory, video input and output, as well as TV rates for videotaping. COMTAL's "**YES**" system requires a minimum of training for effective utilization. Other options such as magnetic tape and disc storage are available. Specialized image processing hardware is available for image arithmetic combination, convolution, Landsat classification, plus small area color correction, and all function in real-time, in 1/30 second. ☐ **YES**, all this—in a system that can accommodate future growth as application requirements expand. Multiple user capability, up to 4 work stations, offers resource sharing. ☐ **YES**, with COMTAL's leadership pacing the state-of-the-art, it adds up to flexibility now—and flexibility later. ☐ **YES**, Vision One/20 image processing systems have dual-ported random access memories starting at 512x512 pixels at multiples of 4 bits of brightness depth, with growth up to 4096x4096-24 bit pixels. ☐ **YES**, random access refresh memories are constantly growing in size and shrinking in cost. Digital image rotation is a reality now. ☐ **YES**, a 24 bit x 24 bit color computer is available for image composition, as is independent arbitrarily shaped small area processing capability in monochrome and color. There's high resolution digital stereo and instantaneous—1/30th second—convolution for filtering. Or, bigger filters exist by recursively iterating and updating kernels 30 times/sec. ☐ **YES**, Vision One/20 provides stand-alone full feature image processing as well as the ability to interface to numerous host computers. ☐ **YES**, dynamic refresh memory partitioning allows for different applications. ☐ **YES**, real-time roaming, with window sizes 512x512 pixels or larger, through the data base, as well as 2X and 4X zooming and 3x3 convolution at 70 MIPS—all implementable in real-time. Ask about the future of image processing from the company with renowned research experts, hardware experts, firmware experts and software experts. COMTAL's field service offices on the East and West coasts are there to help users. ☐ **YES**, successful sales representation worldwide as COMTAL triples its present production capacity in new facilities.

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More man-machine interaction

The primary use of the graphics in this system is to close the loop in the tracking and control situation. At the same time as the operator flies the target, he needs to see where it is within the range area. Since this graphic system changes scale rapidly and keeps the target centered within the display area, it's a great help in accomplishing this.

To some extent, it could also close this loop by tracking the target on the X-Y plot-boards previously used, but our ability to interact with the system computers is much greater with the graphic system.

In addition to the basic use of the graphics to close the tracking/control loop, these displays are also used as an aid in initializing telemetry LED readouts, which are displayed on the control consoles' telemetry panels. In this initialization mode, the operator can interact with system computers to sort telemetry words, manipulate and scale them, etc.

Display hardware includes two Megatek MG552 Graphics Processors, which are contained within the graphics computer mainframe to drive four 21" CRT display monitors. Each processor drives two CRT displays and uses a portion of the computer memory to derive beam position information that creates various points, vectors and alphanumeric characters in a specific CRT presentation. This stored beam-position information, collectively known as the Graphic Display List, is continuously updated and maintained by the GTDD software. The CRT display format is operator controlled and includes such features as variably scaled range maps and target flight profiles, profile time mark generation, and up to 16 selectable target tracks (including track histories) by target ID designation.

A data terminal interface card in the graphics computer facilitates the loading of the graphics display system software via one of the data terminals assigned to the main computers. Once loading is complete, the system software is resident in the graphics computer and need not be reloaded.

The ITCS system computers are also interfaced to a Univac 1230 computer system at the Range Real-Time Data Center located in the same building. The Real-Time Center computers provide radar tracking information on all operation participants within the range area, and this radar data is used by the ITCS/Graphic Target Display System in two ways: (1) for presentation of external target data on the graphic displays, and (2) to provide data to aid in target reacquisition if an ITCS tracker should lose contact with a target in the midst of a tracking operation. Turnkey system development for the ITCS graphic display system, as well as all initial applications programming, was performed by Motorola Inc., Government Electronics Div., Scottsdale, AZ, using graphics display equipment supplied by Megatek Corp., San Diego, CA. A full complement of computer peripherals have been included with the graphics system so that Test Center personnel can perform ongoing applications programming themselves as new types of target drones are put into service or system modification are desired.

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Single-Chip 6801 Offers Versatility – Part 2

James J. Farrell III
Motorola Semiconductor Product Inc.
Austin, TX

In Part 1, we introduced the MC6801 single-chip, 8-bit microcomputer. We continue the discussion where we left off – mode selection.

Mode selection

The MC6801's mode of operation is determined by the logic levels on pins 8, 9 and 10 on the rising edge of Reset. These pins are the three least significant bits (I/O 0, I/O 1 and I/O 2) of Port 2. These inputs are latched into program control bits PC0, PC1 and PC2 by the rising of Reset. (See the example in **Fig 8.**) The current operating mode is available by reading the Data Register for Port 2 where PC2, PC1 and PC0 are latched as bits 7, 6 and 5 respectively.

Table 3 shows a mode selection summary for the MC6801. The mode should be selected based upon the particular bus configuration and memory map the user needs. **Table 4** gives an overview of the operating modes with respect to the internal/external, RAM/ROM addressing area. The mode selection also controls whether a port is I/O, external data lines, external address lines or multiplexed external address/data lines.

Single chip mode

The Single Chip Mode, shown in **Fig 6** and 7, configures all 4 ports as parallel input/output ports. The device is self-contained in this mode, without external address or data buses, therefore maximizing the number of available user I/O lines.

Expanded non-multiplexed-mode (5)

In this mode, the MC6801 will directly address MC6800 peripherals with no external logic. Port 3 becomes the data bus, Port 4 becomes the A7-A0 address bus or partial address and I/O (inputs only), Port 2 can be parallel I/O, serial I/O, Timer, or any combination thereof. Port 1 is parallel I/O only. The 8 address lines associated with Port 4 may be substituted for I/O (inputs only) if a fewer number of address lines will satisfy the application. Note that Reset configures Port 4 Data Direction Register to be all inputs and the user software must configure Port 4 Data Direction Register to output the address lines desired. **Fig 6** and **8** show the MC6801 in the Expanded Non-Multiplexed Mode.

Expanded multiplexed modes (1, 2, 3, 6)

In these modes Port 3 is a multiplexed address/bus (A0/D0-A7/D7) with the address being valid with the trailing edge of Address Strobe (AS) and the data valid during Enable (E). Ports 1 and 2 remain the same as in the single chip mode. Port 4 becomes the higher-order address lines in Modes 1, 2, 3. In Mode 6 the Data Direction Register for Port 4 is cleared on Reset to be all inputs, and the data direction register bits must be programmed for outputs after Reset to provide any or all of the higher order 8 bits of the address bus (A8-A15). Using Mode 6 only, the designer may select a subset of upper 8 bits of the address bus while retaining the remainder as input data lines. In these modes, MC6801 is expandable to a 64K byte address space. **Fig. 9** shows the MC6801 in the Expanded Multiplexed Modes.

The system configuration shown in **Fig 9** shows the MC6801 operating in the Expanded Multiplexed Mode. This configuration uses an 8-bit latch for the 8 low-order address lines to interface with standard MC6800-family parts. The address strobe (AS) is used to latch the address lines so these lines can become data bus lines during the E pulse. The transparent octal D-type latch (MC34828) can be used with the MC6801 to latch the address' LSB.

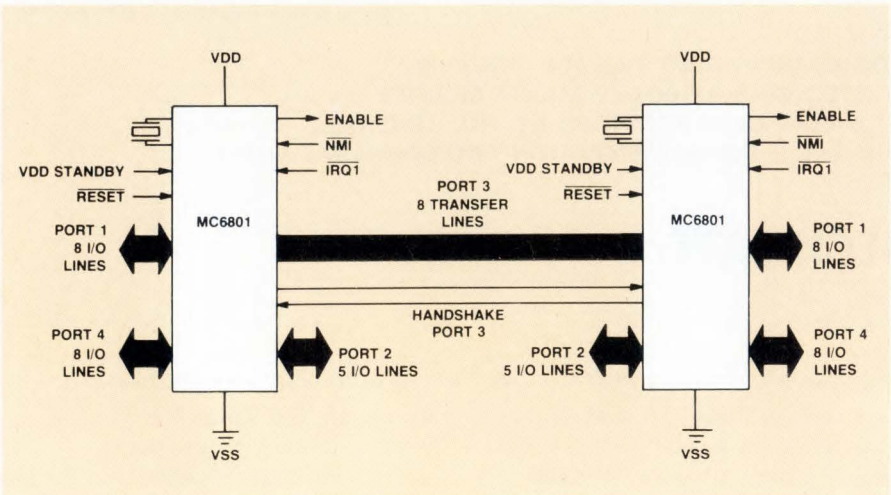
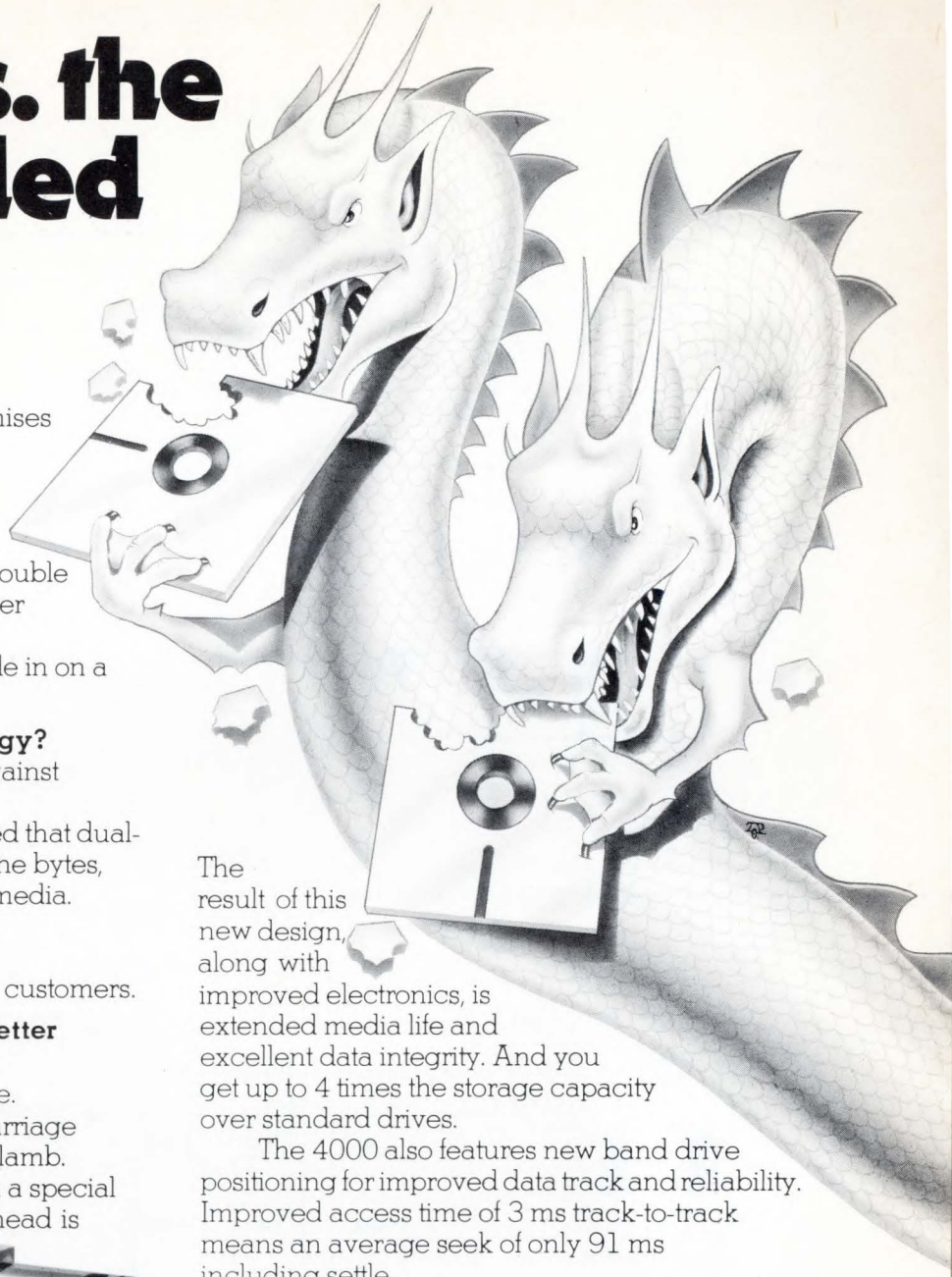


Fig 7 Dual processor configuration – parallel I/O interface.

Remex vs. the two-headed monster.



Were all those dual-head promises just fairy tales?

A lot of people are starting to think so.

They waited. And they waited. And what they finally got for their trouble was trouble — a two-headed monster that ate diskettes.

Until the Remex RFD 4000 rode in on a white horse, that is.

Is it taps for dual-head technology?

Tap, tap, tap went the heads against the diskettes.

In no time at all tap tests showed that dual-head drives not only offered twice the bytes, they took twice the bites out of the media.

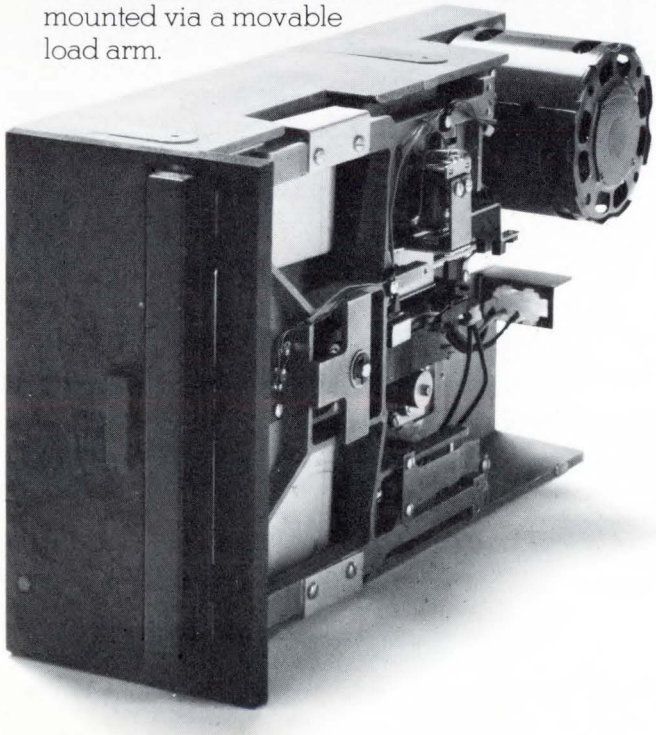
Diskettes just wore out too fast, causing errors.

"Off with their heads," shouted customers.

Rejoice. Two heads really are better than one.

Remex RFD 4000 to the rescue.

Its improved dual head and carriage assembly treat diskettes gentle as a lamb. The ceramic bottom head is fixed in a special lightweight carriage while the top head is mounted via a movable load arm.



The result of this new design, along with improved electronics, is extended media life and excellent data integrity. And you get up to 4 times the storage capacity over standard drives.

The 4000 also features new band drive positioning for improved data track and reliability. Improved access time of 3 ms track-to-track means an average seek of only 91 ms including settle.

Shugart/IBM-compatible

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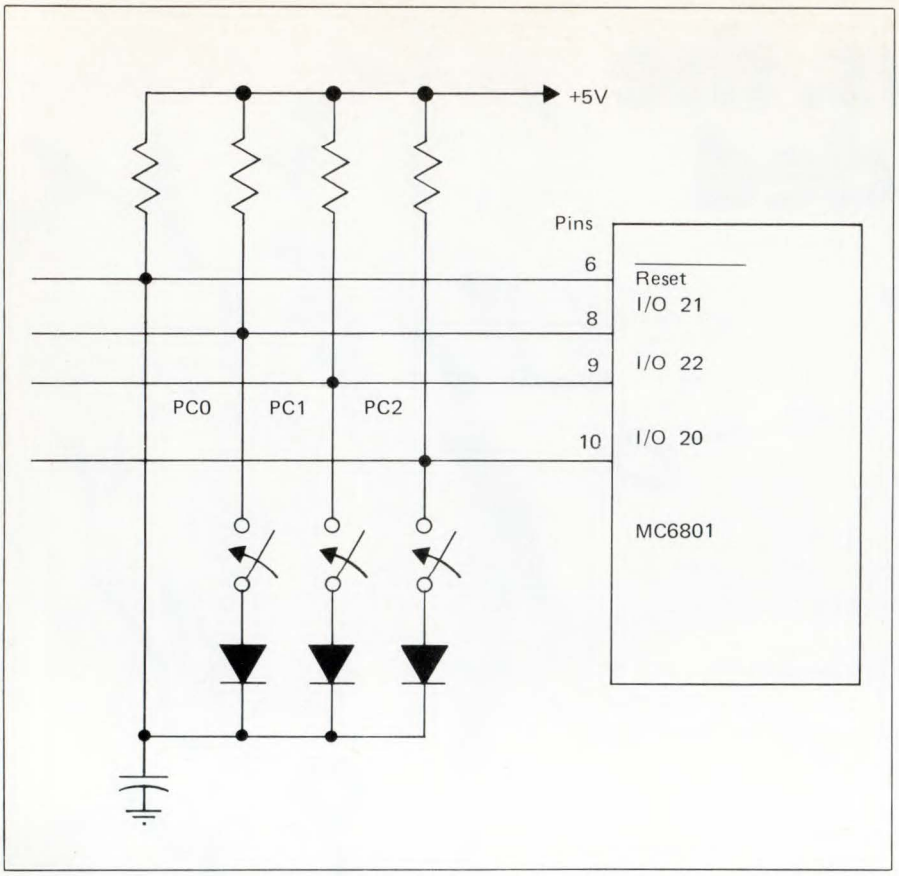


Fig 8 Three program control bits latched by Reset.

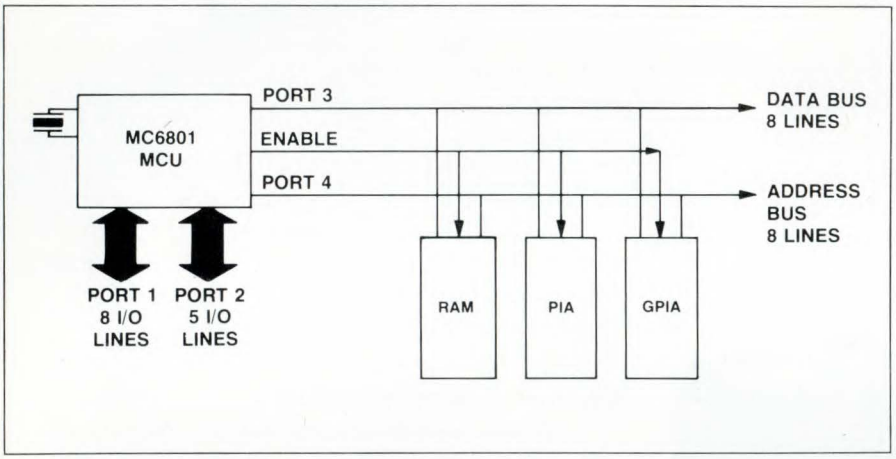


Fig 9 Expanded non-MUX'ed configuration.

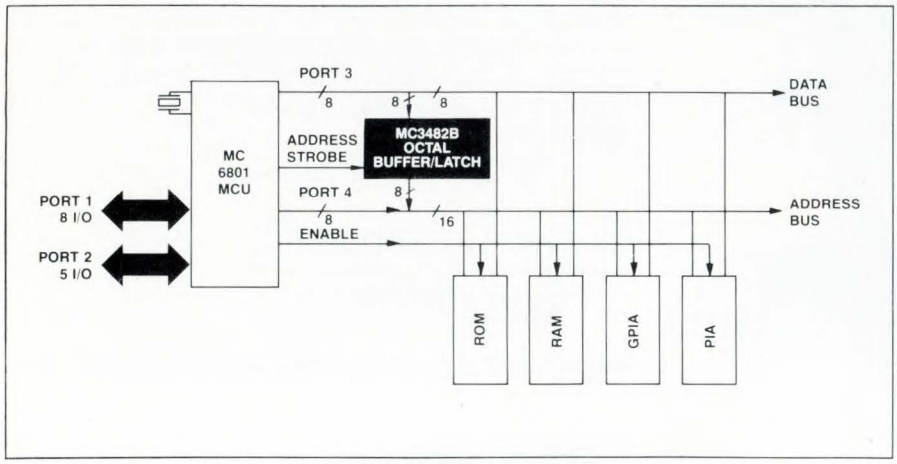


Fig 10 MC3482B octal buffer latch in expanded multiplexed application.

Serial communications interface (SCI)

The MC6801 contains a full-duplex asynchronous serial communications interface (SCI). Two serial data formats (standard mark/space – NRZ – or Bi-phase) are provided at several different data rates. The SCI consists of a transmitter and a receiver which function independently but use the same data format and bit rate. The transmitter and receiver interface with the MCU using the internal data bus and with the outside world using bits 2, 3 and 4 of Port 2.

Wake-up feature

In a typical multi-processor application, the software protocol will usually contain a destination address in the initial byte(s) of the message. In order to permit non-selected MPU's to ignore the remainder of the message, a wake-up feature is included whereby all further SCI Receive interrupts may be optionally inhibited until the data line goes idle. The "wake-up" bit is automatically reset by a string of ten consecutive 1's which indicates an idle data line. The software protocol must provide for the short idle period between consecutive messages and for no idle period within messages.

Programmable options

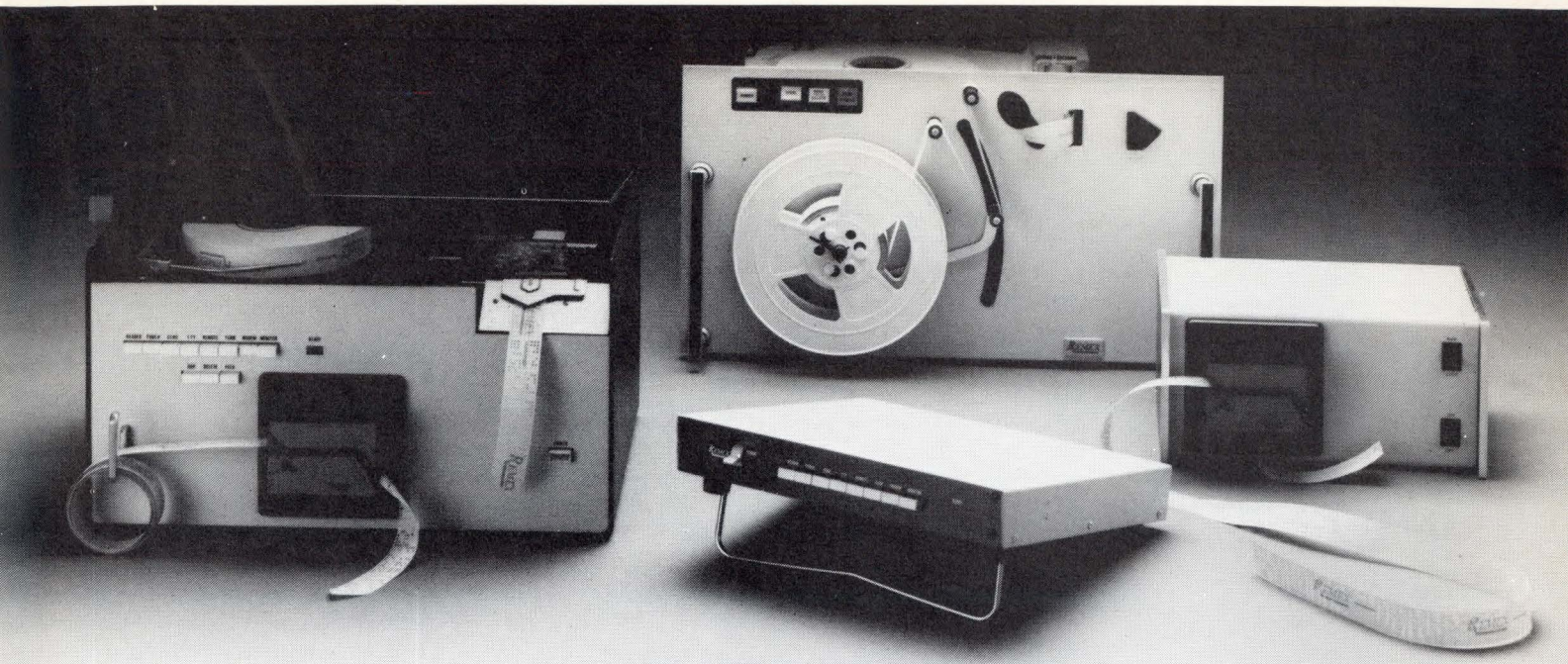
The following features of the MC6801 SCI are programmable:

- Format: standard mark/space (NRZ) or Bi-phase
- Clock: external or internal
- Baud rate: one of 4 per given MCU E-clock frequency, or external bit rate (external clock ÷ 8)
- Wake-Up Feature: enabled or disabled
- Interrupt Requests: enabled individually for transmitter and receiver data registers
- Clock Output: internal bit rate clock enabled or disabled to Port 2 bit 2). Port 2 (bits 3 and 4) – used for I/O or individually programmable for SCI transmit and receive.

Serial communications hardware

The serial communications hardware is controlled by 4 registers as shown in **Fig 11**. The registers include: an 8-bit control and status register, a 4-bit write only rate and mode control register, an 8-bit read only receive data register, and an 8-bit write only transmit data register.

In addition to the four registers, the serial I/O section utilizies bit 3 (serial



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(Punched tape products that communicate)

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The talkies (they listen, too).

Each device is based on RS232C and current-loop interfaces to work with modems, terminals, printers and other peripherals.

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For byte-parallel applications, choose the model RAR 8050 combination reader/perforator. Or choose the RAR 8051 combo with built-in RS232C series interface. Or you can get either type in perforator-only models.

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This reader with built-in RS232C or current-loop interface is ideal for mini/micro-computer program loading. LED's and photo transistors assure rugged reliability. Baud rates range from 110 to 9600, reading continuously to 300 cps at 2400 baud.

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Table 3. Mode Selects

Mode		Program Control Pin 10 P22	Pin 9 P21	Pin 8 P20	ROM	RAM	Interrupt Vectors	Bus
7	Single Chip	HI	HI	HI	I	I	I	I
6	Expanded Multiplexed	HI	HI	LO	I	I	I	Ep/M
5	Expanded Non-Multiplexed	HI	LO	HI	I	I	I	Ep
4	Single Chip Test	HI	LO	LO	I(2)	I(1)	I	I
3	64K Address I/O	LO	HI	HI	E	E	E	Ep/M
2	Ports 3 & 4 External	LO	HI	LO	E	I	E	Ep/M
1		LO	LO	HI	I	I	E	Ep/M
0	Test-Data Output from ROM & RAM to I/O Port 3	LO	LO	LO	I	I	I*	Ep/M

E – External all vectors are external
I – Internal
Ep – Expanded
M – Multiplexed

*First two addresses read from external after reset
(1) Address for RAM XX80-XXFF
(2) ROM disabled

Table 4. Overview of MC6801 Operating Modes

Common to all Modes:
- Reserved Reigster Area
- I/O Port 1 Operation
- I/O Port 2 Operation
- Timer Operation
- Serial I/O O] eration

Single Chip-Mode 7:
- 128 bytes of on-chip RAM; 2048 bytes of on-chip ROM
- Port 3 is parallel I/O handshaking port
- Port 4 is parallel I/O port

Expanded memory Space/Non-Multiplexed Bus-Mode 5:
- 128 bytes of on-chip RAM; 2048 bytes of on-chip ROM
- Port 3 is 8-bit data bus
- Port 4 is optional 8-bit address bus
- 256 bytes of external memory space
- External memory space select output (IOS)

Expanded Memory Space/Multiplexed Bus-Modes 1, 2, 3, 6:
- Port 3 is multiplexed address/data bus
- Port 4 is address bus
- 4 memory space options, (total 64K address space)
  - (1) No internal RAM or ROM (Mode 3)
  - (2) Internal RAM (Mode 2)
  - (3) Internal RAM and ROM (Mode 1)
  - (4) Internal RAM, ROM with partial address bus (Mode 6)

Test-Modes 0 and 4:
- Expanded Test-Mode 0
- May be used to test internal RAM and ROM
- Single Chip and Non-Multiplexed Test-Mode 4
  - (1) May be changed to Mode 5 without $\overline{\text{RESET}}$
  - (2) May be used to test Ports 3 and 4 as I/O ports

input) and bit 4 (serial output) of Port 2. Bit 2 of Port 2 is utilized if either the internal clock-out or external clock-in options are selected.

A description of the SCI control register bits in **Fig 11** is shown below:

Bit 0 WU "Wake-Up" on Idle Line – when set enables wake-up function, cleared by hardware on receipt of ten consecutive 1's. WU will not set if the line is idle.

Bit 1 TE Transmit Enable – when set, changes DDR value for Port 2 bit 4 to a "1"; the DDR value cannot be cleared while TE is set, and will be left at "1" when TE is subsequently cleared. A preamble of nine consecutive 1's is produced when TE is changed from clear to set. While TE is set, the transmitter output is gated to Port 2 bit 4.

Bit 2 TIE Transmit Interrrupt Enable – when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur if TDRE is set; when clear, the interrupt is inhibited.

Bit 3 RE Receive Enable – when set, changes the DDR value for PORT 2 bit 3 to a "0", the DDR value cannot be set while RE is set, and will be left at "0" if RE is subsequently cleared. While RE is set, Port 2 bit 3 is gated to the receiver.

Bit 4 RIE Receiver Interrupt Enable – when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when either RDRF or ORFE is set; when clear, the interrupt is inhibited.

Bit 5 TDRE Transmit Data Register Empty – set by hardware when a transfer is made from the transmit data register to the output shift register. This transfer is synchronized with the bit rate clock. The TDRE bit is cleared by reading the status register. Then writing a new byte into the transmit data register. Data will be transmitted only when this sequence is followed (read TRCS, write TDR). $\overline{\text{TDRE}}$ is initialized to 1 by $\overline{\text{Reset}}$.

Bit 6 ORFE Over-Run-Framing Error – set by hardware when an overrun of framing error occurs (receiver only). An overrun is defined as a new byte ready for the Receiver Data Register with the RDRF flag set. A framing error has occurred when the byte boundaries in the bit stream are not synchronized to bit counter. An overrun may

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Circle 87 for LSI; 88 for PDP; 89 for DG; 90 for P-E; 91 for IBM.

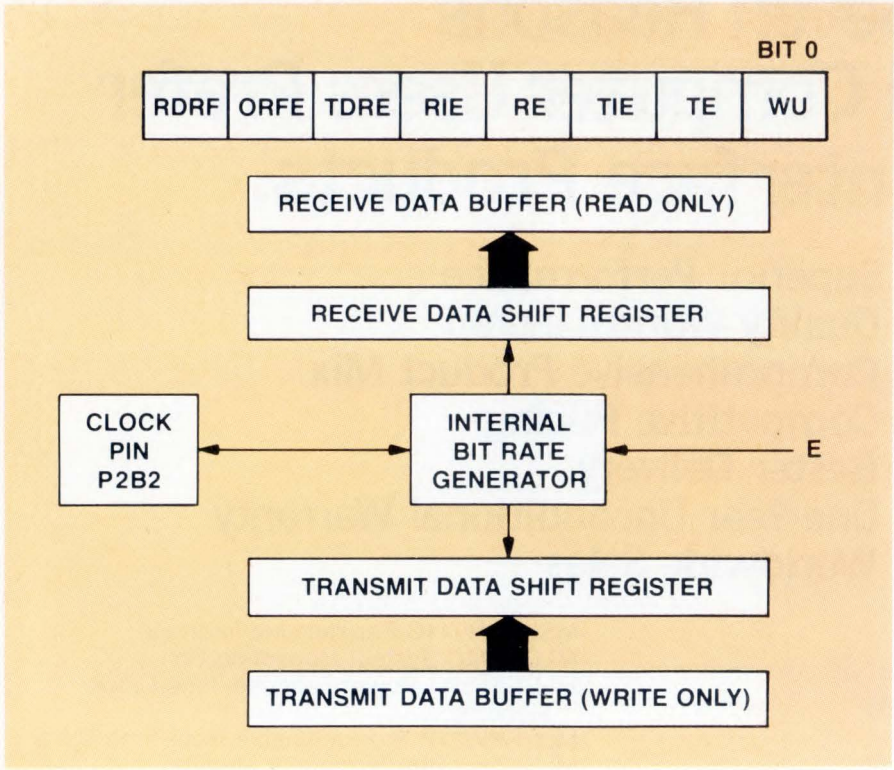


Fig 11 Serial communications interface registers.

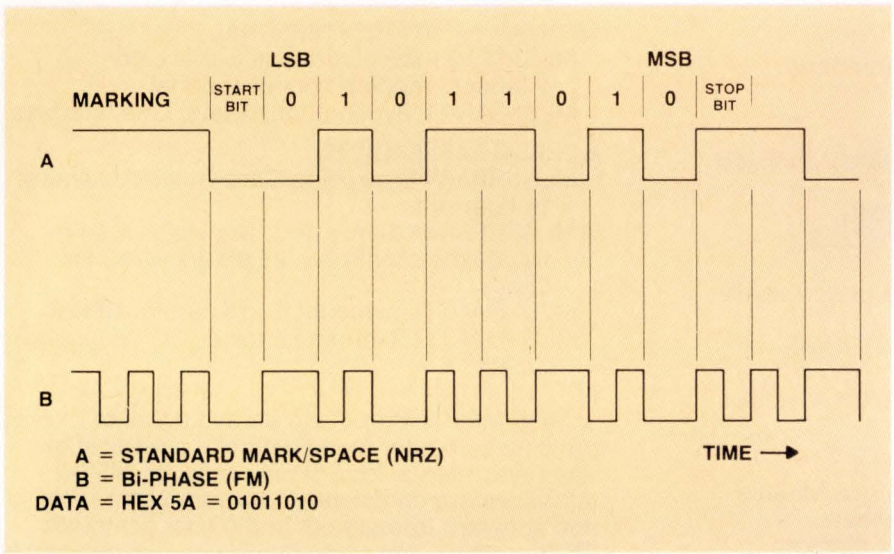


Fig 12 Serial communications interface data formats.

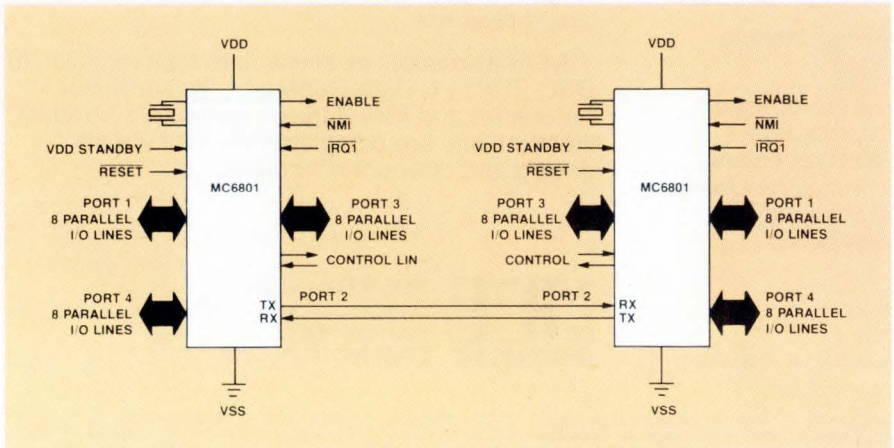


Fig 13 Single chip dual processor configuration – full duplex interface.

be distinguished from a framing error by the corresponding value of RDRF. If RDRF = ORFE = 1, then an overrun has occurred. If RDRF = 0 and ORFE = 1, a framing error has been detected. The ORFE bit is cleared by reading the status register, then Receive Data Register, or by Reset.

Bit 7 RDRF – Receive Data Register Full – set by hardware when a transfer from the input shift register to the receive data register is made. The RDRF bit is cleared by reading the status register, then reading the Receive Data Register, or by Reset. Data is not transferred to the Receive Data Register, nor is the RDRF bit set, on an overrun or framing error condition, i.e., the last good byte is retained.

Rate and mode control register

The Rate and Mode Control register controls the following serial I/O variables: baud rate, format, clocking source, and Port 2 bit 2 configuration.

The register consists of 4 bits all of which are write-only and cleared on Reset. The 4 bits in the register may be considered a pair of 2-bit fields. The two order bits control the bit rate for internal clocking and the remaining two low-order bits control the bit rate for internal clocking and remaining two bits control the format and clock select logic. The register definition is as follows:

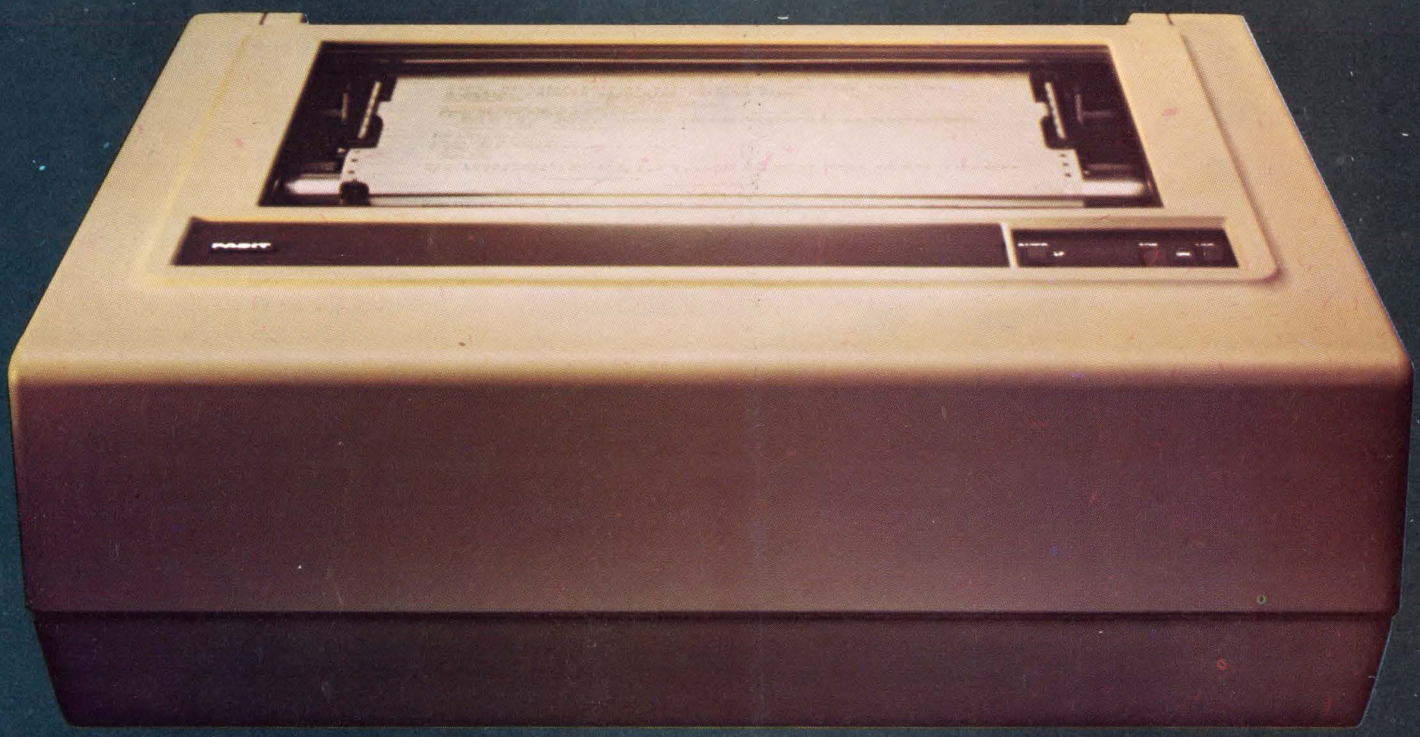
7	6	5	4	3	2	1	0	
X	X	X	X	CC1	CC0	S1	S0	ADDR $0010

Bit 0 S0 Speed Select – These bits select the speed.

Bit 1 S1 Baud rate for the internal clock. Four rates may be selected which are a function of the MCU E-clock frequency. **Table 5** lists the bit times and Baud rates for three selected crystal frequencies.

Bit 2 CC0 Clock Control and Format Select – this 2-bit field controls the format and clock.

Bit 3 CC1 select logic. **Table 6** defines the bit field. If external clocking is selected (CC1 = CC0 = 1), the speed select bits are ignored. If CC1 is set, the DDR value for Port 2 Bit 2 is changed to the complement of CC0 and cannot be altered until CC1 is cleared. If CC1 is subsequently cleared after having been set, the DDR value for Port 2 Bit 2 is left unchanged.



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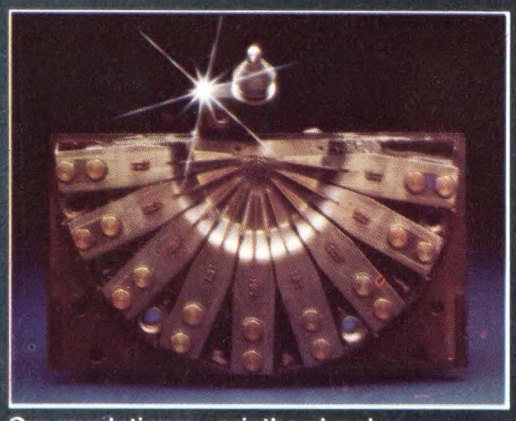

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FACIT DATA PRODUCTS

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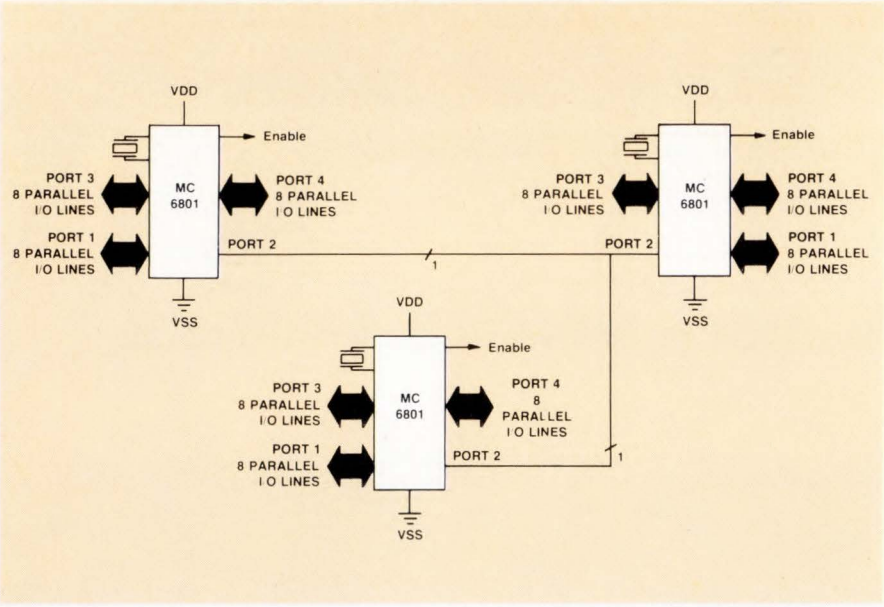

Fig 14 Multiple processor configuration – half duplex interface.

SERIAL OPERATIONS

The serial I/O hardware must be initialized prior to operation. This sequence will normally consist of: (a) Writing the desired control bits to the Rate and Mode Register and then, (b) writing the desired control bits to the Transmit/Receive Control Register.

Transmit operations

The transmit operation is enabled by the TE bit in the Transmit/Receive Control and Status Register. This bit, when set, gates the output of the serial transmit shift register to Port 2 Bit 4 and sets the Port 2 Bit 4 Data Direction Register value for output.

Setting the TE bit initiates the serial output by first transmitting a 9-Bit preamble of 1's. Following the preamble, internal synchronization is established and the transmitter section is ready for operation. At this point one of two situations exits: (a) If the Transmit Data Register is empty (TDRE = 1), a continuous string of 1's will be sent indicating an idle line, or (b) if data has been loaded into the Transmit Data Register (TDRE = 0), the word is transferred to the output shift register and transmission of the data word will begin.

During the serial transfer, the 0 start bit is transmitted. Then the 8 data bits (beginning with bit 0) followed by the stop bit, are transmitted. The TDRE flag bit is set by SCI hardware when the data transfer from the Transmit Data Register to the Transmit Output Shift Registers occurs synchronized to the bit clock.

If software fails to respond to the flag within the proper time, (TDRE is still set when the next normal transfer from the parallel data register to the serial output register should occur), 1's will be sent until more data is written to the data register.

In the Bi-phase mode, the serial output toggles at the start of each bit time, and at 1/2 bit time when a 1 is sent; while in the NRZ mode, the serial output toggles only when the data changes from a "1" to a "0" or from a "0" to a "1". These data formats are shown in **Fig 12**.

Internally generated clock

If the user desires an output bit rate clock, the following requirements are applicable:

- the value of RE and TE are immaterial,
- CC1, CC0 must be set to 1, 0 (**Table 7**),
- the rate is selected by S1, S0 (**Table 6**), and
- the clock will be at the selected bit rate with a positive edge at the mid-bit time (**Fig 14**).

Externally generated clock

If the user desires to provide an external clock to drive the SCI, the following requirements are applicable:

- the (CC1:CC0), field in the Rate and Mode Control Register must be set to 1, 1 (**Table 6**)
- the external clock must be 8 times (X8) the desired bit rate
- the maximum external clock frequency is $< E$

Receive operation

The receive operation is enabled by the RE bit which gates in the serial input from Port 2 Bit 3. The receiver section operation is controlled by the contents of the Transmit/Receive Control and Status Register and the Rate and Mode Control Register.

The data bit interval is divided into 8 sub-intervals for internal synchronization. The received bit stream is synchronized by the first 0 (assumed to be a start bit) encountered following and idle line condition (continuous 1's on the data line). The approximate center of each bit time is strobed during the next 10 bits. If the 10th bit is not a 1 (stop bit) a framing error is assumed, and bit ORFE is set. If the 10th bit is a 1, the data is transferred to the Receive Data Register, and receiver flag RDRF is set. If RDRF is still set at the next 10th bit time, ORFE will be set, indicating an overrun has occurred. Both RDRF and ORFE are cleared by reading the TRCS register followed by reading the Receiver Data Register.

Operation

The operation of SCI is shown in Figures 12 and 13. Figure 12 shows port 2 in operation in full duplex interface between two MC6801s'. Two lines, transmit (TX) and receive (RX) handle the serial data transfer. (**Fig 6** showed parallel or byte by byte data transfer.) Figure 13 shows three MC6801 using the single line, half duplex interface. While only three 6801s are shown here, the only limitations are the electrical drive capability of the sender (which may be buffered) and addresses available.

Programming considerations

Most programmers object to programming considerations being "considered" last. They consider it a personal affront that it wasn't covered first. In any case, it is being covered now. As stated earlier, the MC6801 is a compatible superset of the MC6800.

In order to refresh MC6800 users' memories, a short definition of each of the six addressing modes follows:

MCU addressing modes

The MC6801 8-bit microcomputer unit has 6 address modes which are a function of both the type of instruction and memory reference within the instruction. A summary of the addressing modes for a particular instruction can be found in the tables here, along with the associated instruction execution time provided in MPU E-cycles. With a crystal frequency of 4MHz, these times would be 1 microsecond each.

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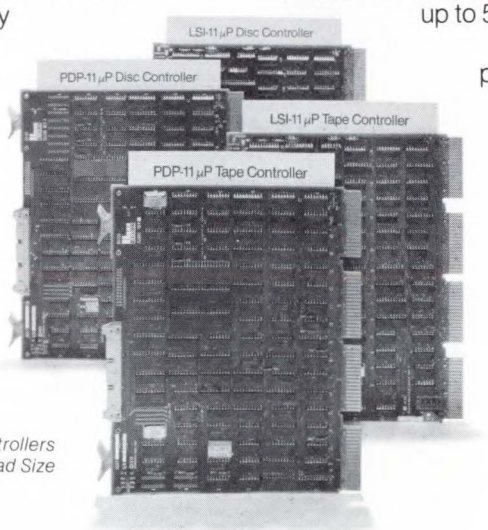

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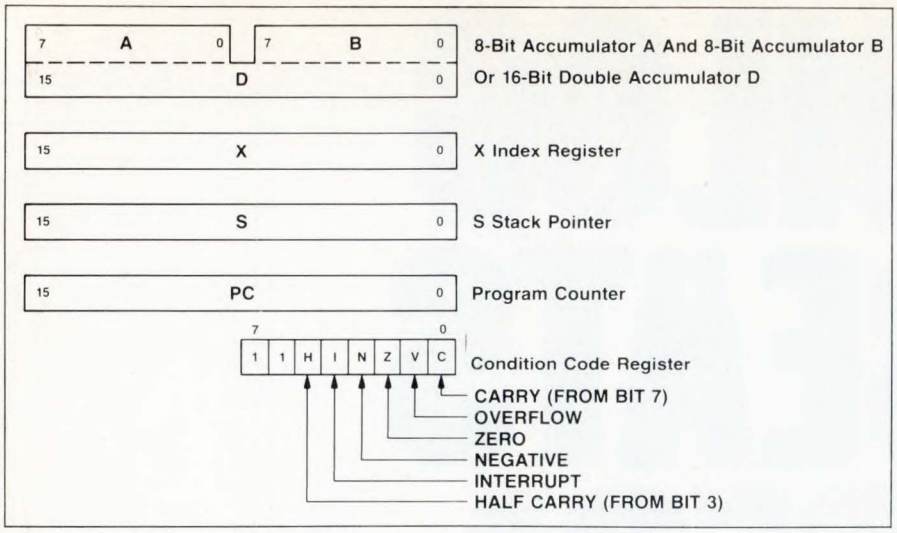

Fig 15 MC6801 programming model.

Immediate addressing: The operand is contained in the following byte(s) of the instruction. The number of trailing bytes matches the size of the register involved. The MCU addresses this location when it fetches the immediate operand for execution. These are two or three-byte instructions.

Direct addressing: The least significant byte of address of the operand is contained in the second byte of the instruction. The most significant byte of the address is assumed to be $00. Direct addressing allows the user to access locations $00 through $FF using only two byte instructions. Enhanced execution times are achieved by eliminating the additional memory access. In most applications this area is used for frequently referenced data.

Extended addressing: The address contained in the second byte of the instruction is used as the higher 8 bits of the address of the operand. The third byte of the instruction is used as the lower 8 bits of the address for the operand. This is an absolute address in memory. These are 3 byte instructions.

Indexed addressing: The offset contained in the second byte of the instruction is added to the 16-bit content of the Index Register. This result is then used to address memory and is held in a temporary address register so there is no change to the index register. These are 2 byte instructions.

Inherent addressing: The address is implied by the instruction, i.e., stack pointer, index register, etc., and requires no memory reference. These are 1 byte instructions.

Relative addressing: If the branch condition is true, the Program Counter is overwritten with the sum of a signed single byte displacement and the current Program Counter. This allows the user to branch to a range of -126 to 129 bytes from the first byte of the instruction. These are 2-byte instructions.

The instruction set from the MC6800 operates identically in the MC6801. That is LDAA (op code 86) works exactly the same in both the MC6800 and MC6801. All the operation codes from the MC6800 are included in the MC6801 at the same location in the operation code map. That means a MC6800 program will run, without change, in the MC6801, if it contains no critical timing loops. Several instructions have been "speeded up" and one "slowed down" by changing the number of cycles (E-clock) required to complete the instruction:

- Instructions Reduced 3 Cycles
  - JSR Exten
- Instructions Reduced 2 Cycles
  - JSR Index
  - BSR
- Instructions Reduced 1 Cycle
  - All Indexed Addressing
  - All Branches
  - STAA, STAB, STX, STS
  - INX, INS, DEX, DES
  - PSHA, PSHB
  - TSX
- Instructions Increased 1 Cycle
  - CPX (Now Sets All Flags Properly)

Programming model

Fig 15 shows the MC6801 programming model. The registers are identical to the well-known MC6800, with exception of the 16-bit double accumulator "D". The "D" accumulator is not an additional register. It is the concatenated "A" and "B" accumulator being handled as one 16-bit word.

The MC6801 has now additional instructions to manipulate the "D" accumulator. These instructions occupy unused op codes in the MC6800 op code map, so that no conflict will occur when running a MC6800 program.

New instructions

The MC6801 has implemented a total of ten new instructions in order to greatly reduce programming time, software errors, and programming costs:

ABX – Accumulator B is added to the index register and the result is placed in the index register.

ADDD – Two consecutive memory locations are added to the D accumulator, and the result is placed in the D accumulator.

ASLD – An Arithmetic shift left is performed on the D accumulator. A zero is shifted into the least significant bit (LSB) and all others shifted "up" one position to the next higher order bit. The most significant bit is shifted into the carry bit (C) of the condition code register.

LDD – Two consecutive memory locations are loaded into the D accumulator.

LSRD – An arithmetic shift right is performed on the D accumulator. A zero is shifted into the MSB. All other bits are shifted "down" one position to the next lower order bit. The LSB is shifted into the carry bit (C) of the condition code register.

MUL – A hardware multiply! Accumulator A is multiplied by accumulator B, and the result appears in the 16-bit D accumulator. This is an unsigned multiply.

PSHX – The contents of the index register are "pushed" onto the stack.

PULX – The location pointed to by the stack pointer, and that location +1, are "pulled" off the stack and loaded into the index register.

STD – The contents of the D accumulator is stored in two consecutive memory locations.

SUBD – Two consecutive memory locations are subtracted from the D accumulator and the result placed in the D accumulator.

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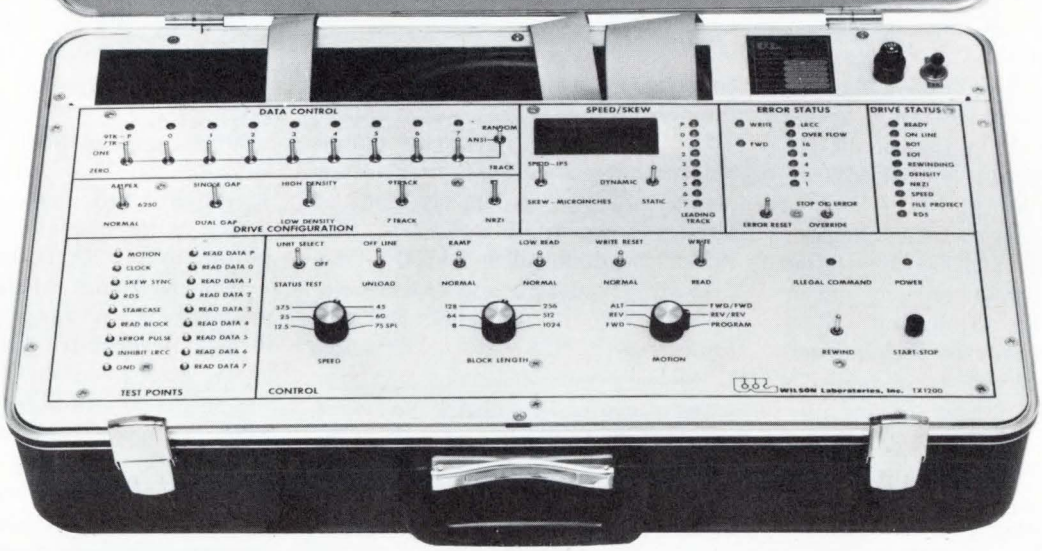

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Product Highlight

Shugart Offers 8" Hard Disk Drive

Harry Shershow, *Associate Editor*

Having already been acclaimed the country's leading producer of floppy disk drives, Shugart Associates, on Sept. 13, 1979, placed on the market a new 8" rigid disk drive which hopefully will push the company into the topmost ranks of producers of such devices. It places this hope on the fact that this is the first 8" disk drive to be offered below a $1,000 price tag. The costs, as a matter of fact, range from a high of $1980 to a low of around $900 depending both on quantity and on megabyte capacity.

Besides the lower cost, Shugart claims that its SA1000 has faster access times, increased capacity and an overall jump in throughput, when compared to its industry-popular floppy disk drive. Simplicity of design is emphasized and Shugart points out that the new drive has 40 percent fewer parts than its SA800 floppy system. This, says Shugart, means a higher MTBF, more trouble-free operation and greatly improved performance.

The SA1000 features the same Winchester head and media technology proven in Shugart's SA4000 14-inch drives. More than 2,000 SA4000 drives have been sold by the company to date, and this, says a company spokesman, provided an unmatched basis of experience and field usage upon which the new eight-inch drive was founded. The "1000" takes a middle position in Shugart's disk-drive family which now ranges in choice of capacity from 29 Mbytes down to 110 Kbytes. The single-head double-disk SA1002 has a 5.33 Mbytes capacity and its sister, the SA1004 with its four disks and two heads, has a 10.67 Mbyte capacity.

Shugart says that the SA1000 series offers to the industry the lowest cost per Mbyte Winchester drive in its capacity range. The newcomer has the same physical dimensions and mounting holes as an 8" Shugart floppy. It features a simple interface using a command structure similar to floppies; and the DC voltage requiremetns are the same as those for floppy disk drives permitting single power supply with both drives.

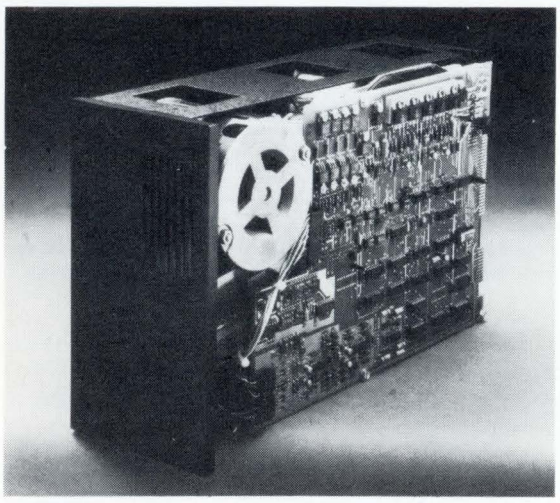
The actuator head is Shugart's reliable Fasflex III™, which is used on other Shugart drives. The Fasflex III operates on less power, is weatherproof, and requires neither field adjustment nor preventive maintenance. An optional PCB offers VFO data separation, write-precompensation, a crystal write oscillator and will support up to four SA1000 drives.

The electronics for the SA1000 are mounted on one removable PCB and include Read/Write, Actuator Driver, and Control functions. The spindle of the disk is rotated at a speed of 3125 RPM through a belt drive system at 50 or 60 Hz. A notable feature of the new series is the special emphasis placed by Shuggart on air control. The air is circulated through a series of filters and maintains a clean inner dust-free environment. Pressure is equalized in the closed system by separate, absolute breather valves. The unit is relatively safe in temperatures ranging from 50° to 150° F and in relative humidity of 8-80%. The recording disks used on the "1000" models have lubricated thin coatings of magnetic oxide placed on aluminum substrates. Data on the disk surfaces are read by a head which accesses 256 tracks on its own side. The two-disk drives have four heads for the R/W functions. Access time (track to track) is claimed to be 19 msec. with an average of 70 msec. and a maximum clocked at 150.

Heat from the unit is dissipated at about 150 W/hr and Shugart claims that component life is about 5 years. The compact unit measures approximately 8" x 14" x 4" and weighs a tolerable 17 lbs.

Full specifications of the SA1000 series (which includes both the 1002 and 1004) can be seen from the data sheet reproduced nearby.

Shugart Associates, 435 Oakmead Prkwy., Sunnyvale, CA 94086. (408) 733-0100.



Shugart's low cost SA1000 series of 8" fixed disk drives offer 5 and 10 Mbytes of storage capacity. The PCB is in place. The SA851 double-side floppy and the SA1000 have the same physical dimensions and mounting holes.

Key Features

- 5.3 and 10.7 Mbyte (unformatted) storage capacity
- Identical mounting to either rack mounted or standard Shugart 8" floppy drives
- Lowest cost/megabyte 8" drive in its capacity range
- Winchester head and media technology
- Proprietary Fasflex III band actuator
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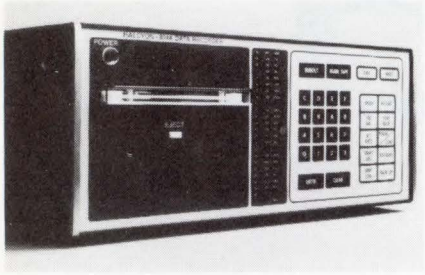
New Products

DATA RECORDER. The 804A allows recording an on-line data at speeds from 50 bps to 56 Kbps. Playback speed is independent of record rate.



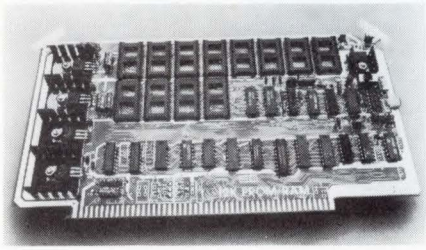
The recorder features a 18.4 Mbit storage capacity, and the standard four-track data cartridge can be used for continuous recording in any of three modes – continuous loop, record full tape and stop, or cue second recorder. The front panel of the 804A includes 16 special-function keys for entering special parameters and programming the instrument. In addition, it also includes an eight-character alphanumeric display. $6,720. **Halcyon,** 2121 Zanker Rd., San Jose, CA 95131.

Circle 201

PRINTER. The DC-1606B/DC2106D discharge printer prints 16 or 21 column alphanumerics in a 5 X 7 dot matrix format. Its MTBF is 3 million lines on 2.25" paper costing about $0.05/10'. 3.8" H X 5.4"W X 5.5" D. From $1200. **Hycom,** 16841 Armstrong Ave., Irvine, CA 92714.

Circle 135

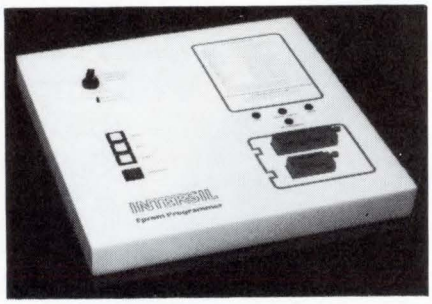
THE S-100 PROM/RAM board features a PROM programming capability for creating customized software programs. The board accommodates up to



12K of 2708 or 2704-type PROM with 1K of 2114 static RAM. Addressing is controlled by jumper options and special circuitry is incorporated for the reset-and-go function and to generate MWRITE. An on-board sliding switch allows one of the PROM sockets to be converted to a PROM-programming socket. $215. **Vector Graphic Inc.,** 31364 Via Colinas, Westlake Village, CA 91361. **Circle 198**

DMA LINE PRINTER CONTROLLER for Data General or equivalent minicomputers, the Model 370, is a single board controller that enables dot matrix, band, or impact printers from various manufacturers to interface directly to the computer memory. The controller minimizes the CPU overhead normally required by programmed I/O controllers. The Model 370 is fully compatible with the instruction set and operating systems software offered by Data General. $1500. **Custom Systems, Inc.,** 2415 Annapolis Lane, Minneapolis, MN 55441. **Circle 215**

THIS INTELLIGENT PROGRAMMER is designed for use with the IM87C48/C41 single chip μC and Intersil's IM6653 (1K x 4) and IM6654 (512 x 8) CMOS EPROMS, with expansion capability for up to three additional types of CMOS EPROMS provided in the hardware. The 6920 operates with

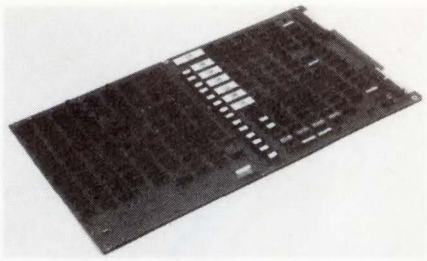


a terminal, as a standalone unit, or as a peripheral to a computer, and features built-in RS232C and 20mA current loop interfaces. The microprocessor firmware contains 16 different editing, loading, listing and programming commands. $950. **Intersil, Inc.,** 10710 N. Tantau Ave., Cupertino, CA 95014

Circle 199

"GOVERNMENT CONTRACTS", a 288-pg. hardcover by Herman Holtz, traces the development of a proposal from idea to final submission and serves as a handbook for all engineers involved in writing proposals. $19.50. **Plenum Publishing Corp.,** 227 W. 17th St., New York, NY 10011. **Circle 144**

μC BOARD. Designated the BLC-80/07, the board has an 8080A CPU, system clock, 24 programmable parallel I/O lines, 512 bytes of static RAM and sockets for 4K bytes of PROM. It can address 64K bytes of memory and has an access time of less than 500 nsec. $365. **National Semiconductor Corp.,** 2900 Semiconductor Dr., Santa Clara, CA 95051. **Circle 197**



DUAL-DENSITY TAPE FORMATTER, Model 9X00F, employs a bipolar bit-slice microprocessor, and has logic patterns and diagnostic routines programmed into on-board ROM. Using a signature analyzer, a technician can compare patterns generated by the μP with ROM-based patterns to ascertain malfunctions. The single-board provides all logic necessary for reading and writing both 1600 cpi phase-encoded and 800 cpi NRZI formats for ANSI and IBM compatible tape. It is designed for Kennedy 9000, 9100, 9300, 9700 and 9800 9-track transports. **Kennedy Co.,** 1600 S. Shamrock Ave., Monrovia, CA 91016.

Circle 193

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"6502 APPLICATIONS BOOK" by Rodnay Zaks includes over 50 exercises. Applications include alarms, motor speed-regulator, clock, traffic control system, industrial temperature control systems, etc. 284 pp. $12.95. **Sybex,** 2020 Milvia St., Berkeley, CA. 94704 **Circle 143**

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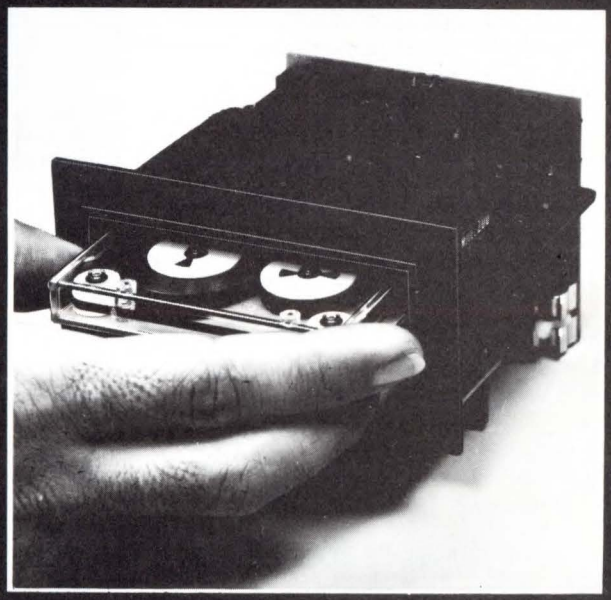

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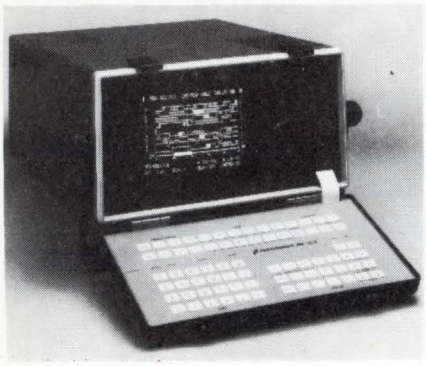
New Products

LOGIC ANALYSIS TOOL, System 5000, offers state, timing and waveform recording. Using a "systems" (not "dedicated intrument") approach, the 5000 handles logic state, logic timing and waveform recording functions. These functions can operate interactively as a total data system or as independent analysis units. For example, users can configure the system to collect 40 channels of state information, or 32 channels of state and 8

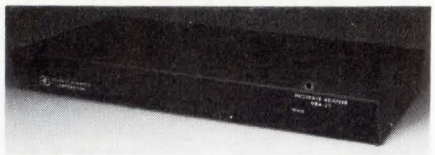


channels of timing, or 32 channels of state and 1 channel of waveform. The state section collects synchronous data from the system-under-test at 15 MHz; the timing and waveform recording sections operate asynchronously at 50 MHz. $5,000. – $8,000. **Paratronics, Inc.**, 122 Charcot Ave., San Jose, CA 95131 **Circle 140**

POWER SUPPLIES. 18 single, dual and triple output μP models have no EMI problems, and MTBF of 60,000 to 80,000 hours – all backed by a 6-yr. guarantee. Specs for all models include: output of 5V at 9, 12, 18, 25, 40A; 12V at 12, 18A; 15V at 11A, 16A; and 24V at 8, 12A. Dual output models are: ±12V at 6A and ±15V at 5.5A; triple-output μP models: 5V at 12A, ±12V at 2A and 5V at 18A, ±12V at 3A. **Adtech Power, Inc.** 1621 S. Sinclair St., Anaheim, CA 92806. **Circle 130**

CLUSTER CONTROL UNIT. The plug-to-plug compatibility of the TC 371 allows the user to initially replace an IBM 3270 compatible remote control unit and implement extended functions. In addition to standard 3270 features, the TC 371 provides the user with the benefits of local print, local format storage, store and forward, preliminary editing, and batch print capability. Up to 31 display and printer terminals may be attached to the TC 371. The TC 371 operates under BSC at transmission speeds up to 9600 bps. **Telex**, 6422 E. 41st St., Tulsa, OK 74135. **Circle 203**

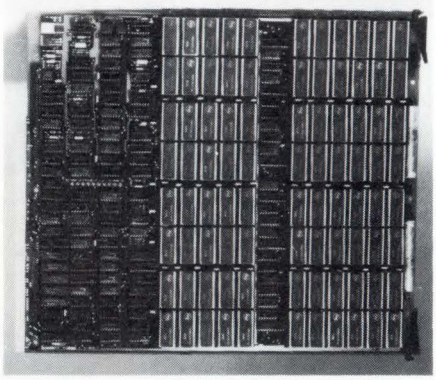
IFA SERIES INTERFACE CONVERTERS provide convenient adapters to convert the RS-232/V.24 electrical interface to either CCITT recommended RS-449, V.35, X.21 or Bell 303. The



IFA series features a design that allows the same converter to fit either a standard 19-inch rack mount or a desk-top enclosure. All converters are fully interchangeable and different converters may be installed in the same rack. A second unique feature of these units is that the RS-232 connector may be replaced with a TTL interface. **Atlantic Research Corp.**, 5390 Cherokee Ave., Alexandria, VA 22314. **Circle 214**

LINE PRINTER CONTROLLER is said to interface popular printers to Perkin-Elmer Interdata processors. The controller handles any printer up to 500 kbytes/s (3700 lpm), and the board can be plugged directly into any available I/O slot in either 16 or 32 Perkin-Elmer computers. $650. **Macrolink**, 1740-E South Anaheim Blvd., Anaheim, CA. **Circle 194**

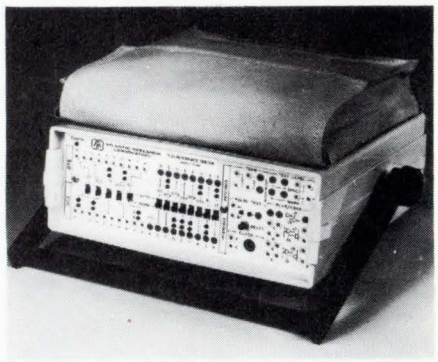
ONE MEG BOARD. The Hypak, based on 128K bit hybrid memory modules, packages 1 Mbyte of high speed dynamic RAM with full 6-bit error correction on a single 13 by 15 inch memory board. Each Hypak module contains eight commercially available 16K



dice, mounted on a ceramic substrate. Miniature multilayer thick film circuits provide the pin to die interconnects, and high precision automated bonding is used to make die to substrate connections. Hypak memory systems with 200 NS access times utilize 6-bit error correction to improve reliabilty. All single bit errors are detected and corrected, and all dual bit errors detected, so memory performance can be monitored continuously to ensure maximum system uptime. **General Automation**, 1055 S. East St., Anaheim, CA 92803. **Circle 207**

PRINTER/PLOTTER. An E-sized drawing in 13.5 sec? With a paper width of 36" and a speed of 3.25"/sec, the 5400 generates over 48 S.F. of hard copy per minute. Designed for applications where fast turn-around and high throughput rates are important, the 5400 is for CAD, seismic data plotting, and business graphic applications such as PERT/CPM, Gantt and others. The patented negative-pressure, closed loop toning system ensures high-contrast dry hardcopy even at the maximum plotting speed. Print resolution is 100 dots 1 in. horiz. and vert. **Gould Inc. Inst. Div.** 3631 Perkins Ave., Cleveland, OH 44114 **Circle 138**

INTERFACE TESTER IFT-680 is a combination breakout box and interface analyzer designed for testing the CCITT V.35 interface between modem and terminal. A built-in clock enables the IFT-680 to operate as a modem eliminator by direct cross patching on



the unit's front panel. The IFT-680 combines light weight and ease of operation which makes it ideal for field servicing. The unit is put into operation by plugging the modem end of the terminal-modem cable into the DTE on the IFT-680 and connecting the 3-foot test cable, supplied with the unit, between the DCE connector on the IFT-680 and the modem. **Atlantic Research Corp.**, 5390 Cherokee Ave., Alexandria, VA 22314. **Circle 213**

WIRE WRAP. Eliminating cutting, stripping and slitting, the JW-1 ($14.95) wrap tool wraps AWG 30 wire on 0.025" square posts with daisy chain or point-to-point wrap. Features include built-in cut off, easy wire loading and blu, wht, red and yel colors. **OK Machine & Tool Corp.**, 3455 Conner St., Bronx, NY 10475. **Circle 136**

8K CACHE. Designed for the 11/34, 11/35 and 11/40, the Cache/434 and 440 has byte and address parity, upper/lower limit switches, on-line/off-line manual switch control, activity indicator lights, 8K bytes of memory (4K words). **Able Computer Technology.** 1751 Langley Ave., Irvine, CA 92714. **Circle 300**

C. Itoh's Model 8300 printer looks superb.

It works even better.

C. Itoh offers you the perfect OEM printer for general purpose computers, communication terminals, data loggers and micro computers: the Model 8300. This quiet and low-cost unit features a straightforward, reliable design and a continuous-duty 7-wire head with a life expectancy of 100 million characters. Designed with a 7-bit parallel interface, the 80-column, dot matrix Model 8300 prints bi-directionally at 125 CPS. Its sprocket paper feed mechanism accepts multi-ply pin-feed paper in any width from 4.5″ to 9.5″; paper can be loaded from the bottom or rear; and print line position is readily adjustable. The Model 8300 works even better than it looks. Would you expect anything less from C. Itoh? Write today for detailed specifications.

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C. Itoh means excellence in printers.

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C. Itoh Electronics is part of the 119-year-old C. Itoh & Co., Ltd., world-wide trading organization.

Circle 44 on Reader Inquiry Card

New Products

DOUBLE-SIDED DISKETTES. The 742 Diskette is compatible with single density diskette drives and is for IBM 5110 and compatible systems. 7430 Diskettes, for double-density applications, may be obtained unformatted or in 256, 512 and 1024 formats for IBM System 34, 5110 and compati-

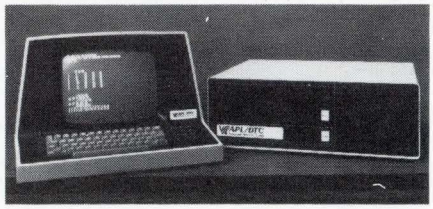
ble systems. 743-2 Diskettes are available for use on Shugart 850 drives and other compatible systems. **3M,** Box 33600, St. Paul, MN. **Circle 128**

A MEMORY CARD using 16K bits of 2708-type EPROM memory permits expansion of S-100 systems. The card's 16K of memory are addressable in four 4K groups. A bank select feature, which controls up to eight banks of memory, allows any 4K group to be addressed to any 4K boundary. Features of the card include fully buffered data and address lines; onboard regulators and heat sinks that allow cool, problem-free operation; and switch-selectable wait states (0-4). $300 with 16K of 2708-type memory. **Artec,** 605 Old County Rd., San Carlos, CA 94070. **Circle 204**

FASTER FIBER OPTIC data links to 150 kbits/sec – provide signal isolation in electrically noisy environments. The DC coupled receiver accepts asynchronous data. Compatible with many process designs, the link maintains high sensitivy and long link lengths. $125. **Burr-Brown,** Box 11400, Tucson, AZ 85734. **Circle 192**

THIS FAST 6800 is capable of executing an instruction in 800 ns. Designated the S68H00, it utilizes a 2.5 MHz clock and can execute one data access instruction per 2 clock cycles. In all functional respects the S68H00 is identical to slower versions of the 6800. However, its processing speed is two and a half times the speed of the standard 6800. $83.85 (ceramic); $49.95 (plastic). **American Microsystems, Inc.,** 3800 Homestead Rd., Santa Clara, CA 95051. **Circle 200**

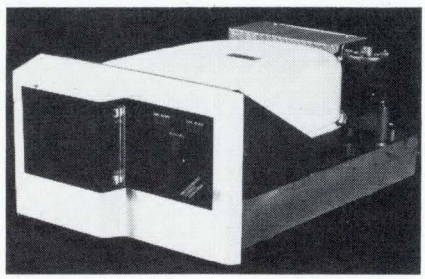
APL/DTC DESKTOP μC, a complete hardware/software configuration, a 4MHz Z80, two quad-density mini-disk drives, video terminal, APL character generator, object code disk, and documentation. The system gives users 24K



bytes of usable active APL workspace. The APL includes standard APL arithmetic functions, plus boolean, relational, selectional, structural, and general functions such as execute and format. The languge also contains system variables and system functions, such as canonical representation, function fix, share offer, and share retract. **Vanguard Systems Corp.,** 6812 San Pedro, San Antonio, TX 78216. **Circle 205**

"SOFTWARE TESTING", a two-volume (analysis and bibliography, and invited papers) covers strategies, techniques, symbolic and dynamic testing, code analysis tools and exercises, test data generators, testing real-time software systems and Pascal-like languages, etc. **Infotech International Ltd.,** Nicholson House, Maidenhead, Berkshire, SL6, 1LD, England. **Circle 145**

WINCHESTER FAILSAFE FEATURE. This data storage system combines Winchester type drive technology, backup tape cartridge and smart controller into a compact package. The MSC-5900 provides as much as 87.8 Mbytes of sealed module storage as well as 17.1 Mbytes of removable tape storage. A built-in μP controls drive functions, data formatting and buffering, dump and restore operations for

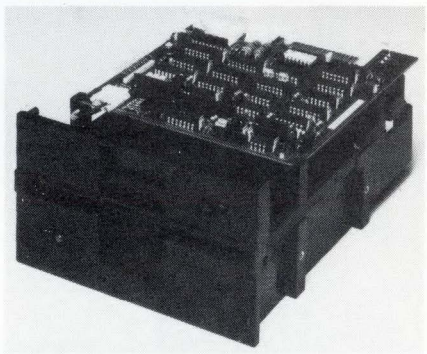


the tape cartridge and communications with the CPU. Microdiagnosis functions include self-prognosis by monitoring trends in increased seek-time and error correction rises. Models are available with 2, 6, 10 and 14 heads, and have storage capacities of 12.5, 37.6, 62.7 and 87.8 Mbyte, respectively. **Microcomputer Systems Corp.,** 432 Lakeside Drive, Sunnyvale, CA 94086. **Circle 212**

CODE CONVERTER READER is designed to read perforated tape in any 5, 6, 7 or 8-level code and output in any 5, 6, 7 or 8-level code via its RS-232C serial interface. Baud rates and operating modes are switch-selectable. The μP controller is normally programmed to convert 5 level Baudot Code (US or CCITT) to 8 level ASCII. Other codes are available upon request. **Data Science,** 1189 Oddstad Dr., Redwood City, CA 94063. **Circle 195**

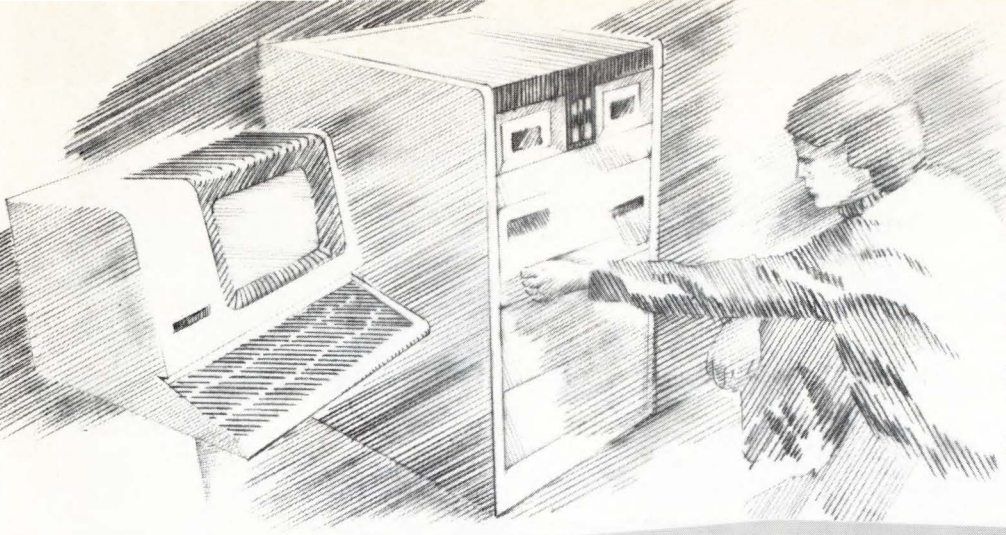
IMPACT PRINTER, AIP-40, a miniature, panel-mounting 20-col. alphanumeric printer, uses non-impact thermal printing to print the full ASCII char. set of U & L-case letters, numerals, punctuation, etc. in 20 col. across 2¼" wide thermal paper. A dot-line thermal printhead forms 5 X 7 matrix characters which are 0.11" high. Printing is 11/2 lpm. **Datel Systems, Inc., (Intersil),** 11 Cabot Blvd., Mansfield, MA 02048. **Circle 126**

MINI DISK DRIVE. Conventional mini disk drives must return to track 00 before accessing a new track. The FD-50A, however, moves directly to the selected track, the same method used by large hard-disk systems. This



direct seek method gives the drive a track-to-track access time of 25 ms and an average access time of 298 ms. In its basic 35-track configuration the capacity of the FD-50A is 109.4Kbytes (unformatted). The FD-50A is fully plug-to-plug and media compatible with the Shugart SA-400. **Teac Corp.** 11.1 Chome, Tsukiji, Chuo-ku, Tokyo 104, Japan. **Circle 211**

μP-BASED VIDEO DISPLAY TERMINAL In addition to numeric pad, upper/lower case, editing, current loop, cursor addressing, columnar field tab, etc., the Visual 200 has detachable keyboard, smooth scroll, tilt screen (10° to 15° viewing angle), and large 7 x 9 dot matrix characters. A switch on the rear panel programs the terminal for code-for-code emulation of a Hazeltine 1500, ADDS 520, Lear Siegler ADM-3A or DEC VT-52. **Visual Technology, Inc.,** Railroad Ave., Dundee Park, Andover, MA 01810. **Circle 216**



TI Silent 700® or ANSI Compatible

Emulates paper tape with DEC software at up to 9600 baud

The Raycorder Cassette Terminal Model 6801

The Model 6801 Raycorder Cassette Terminal is a dual-cassette operating system capable of reading, writing, and copying data at switch selectable rates from 110 to 9,600 baud through a full duplex, asynchronous RS232C interface.

Operating under the control of a microprocessor with up to 4K of firmware, the Model 6801 has designed-in versatility never before available in a system of this type.

Connected to a serial port of a DEC PDP8 or PDP11 and given the proper address, it will emulate the typical paper tape reader/punch and perform the functions of program load, data logging, assembly, edit or duplication. Select one of two Texas Instruments Silent 700® modes, and tapes can be written, read, or copied that are completely compatible with the 733ASR but at much higher data rates.

With its extension connector, the Model 6801 can be connected to any RS232C port without disturbing the device formerly connected there. With this feature, for example, tape storage can be added where only hard copy print out or CRT display had previously existed.

Utilizing two of Raymond's time-proven 6406 Raycorder cassette drives, the Model 6801 provides the ultimate in a reliable, flexible data storage and handling device for a multitude of applications. Detailed specifications will be provided on request.

For the OEM

Raymond's small tape drives, long the standard of the industry, are now available with all new electronics that make interfacing a cinch.

Model 6406 for Philips Cassettes, redesigned with many new features at a lower cost.

Model 6409 for Mini-Data Cassettes, now has a parallel interface and other changes you'll appreciate.

Model 6413 for ¼-inch Data Cartridges, the newest member of the team is catching on fast.

Raycorder Products Division

Raymond Engineering Inc.

217 Smith Street
Middletown, Connecticut 06457
(203) 632-1000

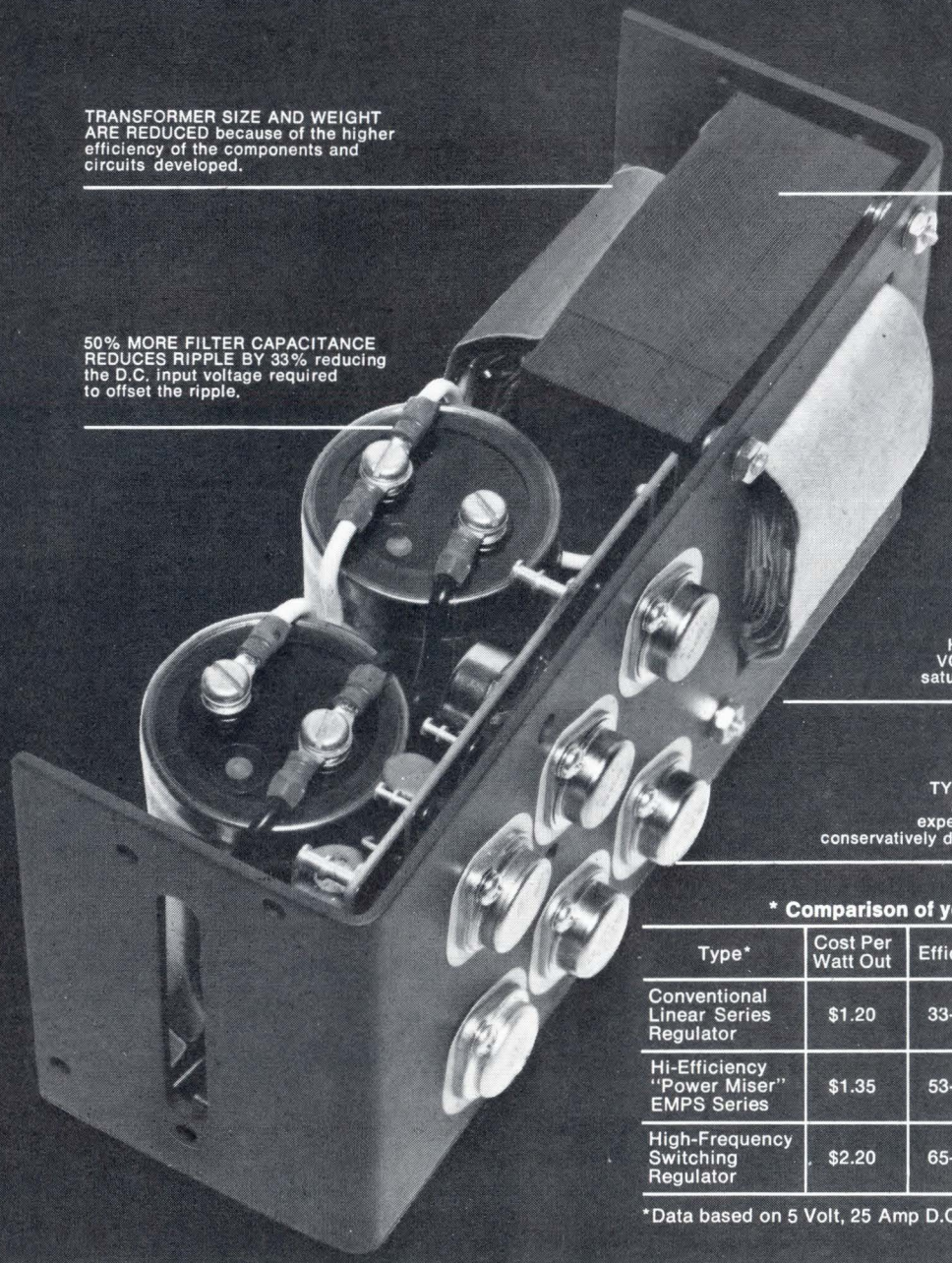
a subsidiary of Raymond Industries

Circle 78 on Reader Inquiry Card

'Power Misers:'

Adtech Power's new high efficiency linear DC Power Supplies.

30-40% more efficient and 30-45% smaller than series regulators.. half the cost of less reliable switchers!



TRANSFORMER SIZE AND WEIGHT ARE REDUCED because of the higher efficiency of the components and circuits developed.

TRANSFORMER LOSSES HAVE BEEN REDUCED 13% through the use of higher grade steel and square copper magnet wire.

50% MORE FILTER CAPACITANCE REDUCES RIPPLE BY 33% reducing the D.C. input voltage required to offset the ripple.

THE EMPS 5-18 (5V/18A) PICTURED IS THE SAME SIZE AS A CONVENTIONAL 5V/12A SERIES REGULATED UNIT.

HIGHER POWER. LOWER SATURATION VOLTAGE SERIES TRANSISTORS reduce saturation voltage drop dissipation by 40%.

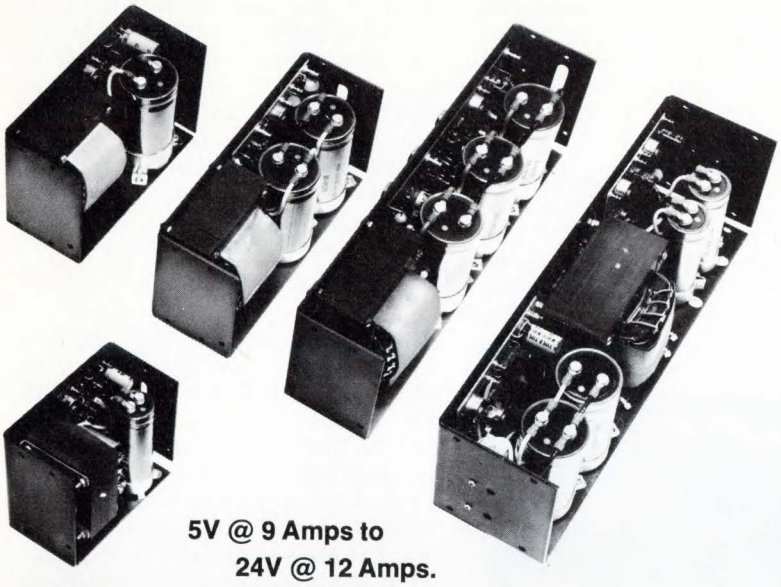
TYPICAL RECTIFIER LOSSES OF 20-25% ARE REDUCED 50% by the use of more expensive, high powered Schottky rectifiers conservatively derated 50% in both current and voltage.

*** Comparison of your three alternatives.**

Type*	Cost Per Watt Out	Efficiency	Volume Per Watt Out	Power Density Per Watt Out
Conventional Linear Series Regulator	$1.20	33-43%	3.74 Cu. In./W.	0.27 W/Cu. In.
Hi-Efficiency "Power Miser" EMPS Series	$1.35	53-56%	1.91 Cu. In./W.	0.52 W/Cu. In.
High-Frequency Switching Regulator	$2.20	65-71%	1.34-1.62 Cu. In./W.	0.61-0.74 W/Cu. In.

*Data based on 5 Volt, 25 Amp D.C. Output Rating.

A complete series of 18 Single Output, Dual Output and Triple Output Microprocessor Models with no EMI problems...an MTBF of 60,000 to 80,000 hours...backed by a 6-year guarantee!



5V @ 9 Amps to 24V @ 12 Amps.

18 Models/ 7 Configurations

D.C. RATING	EFFICIENCY	MODEL NO.	POWER SUPPLY PRICES 1-9	10-24	25-49	50-99	100-249
Single Output Models							
5V @ 9A	54% ±2%	EMPS 5-9	99.00	94.00	90.30	87.60	85.80
5V @ 12A	54% ±2%	EMPS 5-12	109.00	103.55	99.40	96.40	94.50
5V @ 18A	54% ±2%	EMPS 5-18	135.00	127.95	122.80	119.15	116.75
5V @ 25A	54% ±2%	EMPS 5-25	180.00	171.00	164.00	159.25	156.00
5V @ 40A	54% ±2%	EMPS 5-40	220.00	209.00	200.60	194.60	190.00
12V @ 12A	59% ±1%	EMPS 12-12	170.00	161.00	154.00	149.25	146.00
12V @ 18A	59% ±1%	EMPS 12-18	210.00	199.00	190.00	184.60	180.00
15V @ 11A	65% ±1%	EMPS 15-11	170.00	161.00	154.00	149.25	146.00
15V @ 16A	65% ±1%	EMPS 15-16	210.00	199.00	190.60	184.60	180.00
24V @ 8A	68% ±1%	EMPS 24-8	170.00	161.00	154.00	149.25	146.00
24V @ 12A	68% ±1%	EMPS 24-12	210.00	199.00	190.60	184.60	180.00
Dual Output Models							
±12V @ 6A	OVER 50%	DEMPS 12-6	190.00	188.10	180.60	175.15	171.65
±15V @ 5.5A	OVER 50%	DEMPS 15-5.5	190.00	188.10	180.60	175.15	171.65
Triple Output Microprocessor Models							
5V @ 12A ±12V @ 2A	OVER 50%	TEMPS-3	185.00	175.75	168.70	163.65	160.40
5V @ 18A ±12V @ 3A	OVER 50%	TEMPS-4	230.00	218.50	209.75	203.50	199.40

*For ±15V add "-2" suffix to model no.
Overvoltage protection standard on TEMPS-3 & 4, 5V. output

Specifications: All Models

A.C. Input:
5 V.D.C. OUTPUT UNITS: 105-125 Vac. 47-440Hz (derate 10% for 50Hz operation)
ALL OTHERS: 105-125/210-250 Vac, 47/440Hz

Extended A.C. Input: 100-130 Vac (derate 20%)

D.C. Outputs: See Tabulation of Models

Control: ± 5% Voltage Adjustment (Screwdriver adjust pot.)

Regulation: ± 0.05% Line or Load

Remote Sensing:
Standard on all models, (includes open sense lead protection.)

Ripple: 5mV Peak to Peak

Reserve Power:
+5% of output available for external load line drop on 5V. and 12V. units; +0.6V. on all others.

Temperature Coefficient: 0.02%/°C.

Stability:
± 0.1% for 24 hour period after 30 minute warmup

Overshoot:
No turn-on, turn-off or power failure overshoots.

Transient Response:
Output recovers to regulation band within 50 microseconds after an instantaneous load change of 50 to 100%.

Operating Temperature:
-25° to +70°C. (derate linearly above +50°C. to 40% at +70°C.; derate linearly below -5°C. to 70% at -25°C.)

Cooling:
Convection cooled for full power rating at 50°C. ambient. Forced air cooling extends full power rating to 60°C.

Protection:
Overload and short circuits: Automatic recovery foldback current limiting fully protects against overloads and short circuits.
Reverse Polarity Protection: Prevents damage from reverse voltage swings.
Inductive Load Protection: Prevents damage due to inductive voltage swings.

Overvoltage:
Optional crowbar overvoltage protection. (Standard on 5V. output TEMPS)

Transformer:
Electrostatically shielded for better line noise immunity.

All Models Meet U.L. Recognition Requirements.

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Colorado, Denver
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Florida, Coral Springs
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Kansas, Wichita
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New York, Syracuse
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North Carolina, Hayesville
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Pennsylvania, Philadelphia
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Pennsylvania, Pittsburgh
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Texas, Dallas
Phone: (214) 387-2489

Texas, Houston
Phone: (713) 988-0991

Washington, Seattle
Phone: (206) 641-3535

Washington, D.C.
Phone: (202) 363-9417

Wisconsin, Milwaukee
Phone: (414) 527-1500

ADTECH POWER

Europe: ADTECH INTERNATIONAL, Subsidiary of Adtech Power, 46 BD, Roger Salengro, 78200 Mantes La Ville, France. Tel. 4775301+

DISTRIBUTORS: Call Kathy Nelson, Distributor Products Group, (714) 634-9211, for the name of a distributor near you.

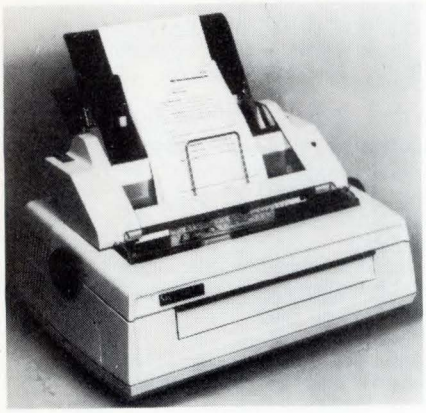
Power Misers are also manufactured in Europe.

ADTECH POWER, INC., 1621 S. SINCLAIR ST., ANAHEIM,CA 92806. (714) 634-9211 ● TELEX 68-1498

Circle 64 on Reader Inquiry Card

New Products

FIVE FORMS HANDLING DEVICES more than double the paper handling capabilities of the Spinwriter printers. The twinfeeder is a cartridge-type cut sheet feeder that feeds a piece of paper from either of two bins. First and successive sheet selection is automatic



under program control. The single input bin cut sheet feeder is a μP-controlled forms module that provides automatic insertion and stacking of up to 200 forms. The horizontal forms tractor is used in printing applications where many different sizes of continuous forms are required. The bidirectional forms tractor is designed for continuous forms applications where reverse paper motion is required. Designed for demand document applications where single cut forms, bottom glued forms, and ledger cards are used, the front inserter also can be combined with the horizontal forms tractor to accomodate continuous forms applications. **NEC Information Systems, Inc.**, 5 Militia Dr., Lexington, MA 02173. **Circle 232**

DESKTOP SYSTEM UPGRADE. Through a package of PCC 2000 enhancements users can expand peripheral disk capacity by up to 40 Mbyte of rigid disk storage and attach up to four more CRT terminals to this small business system. A high-speed data transfer utility is used with the floppy disk drives to back-up and restore data files on the hard disk. A hard-disk controller transfers data via direct memory access at 750 kbyte/s providing increases in overall system speed while expanding storage capacity as well. **Pertec Computer Corp.**, Computer Systems Division, 20630 Nordoff St., Chatsworth, CA 91311. **Circle 206**

PASCAL FOR INTEL. UCSD Pascal for users of Intel development systems (MDS800 or Series II) is supplied on a single diskette (single or double density) and will run without the need for other operating systems on a 48K byte or larger system. The diskette contains a Pascal compiler, P code interpreter for Z80/8080 microprocessors, cursor driven screen editor which uses the cursor control keys of the Development Systems' CRT, menu driven operating system, Z80/8080 assembly and linker/librarian which allows assembly language procedures to be linked into Pascal programs. **Novar Associates**, P.O. Box 265, Wallingford, PA 19086. **Circle 237**

SMALL OEM PRINTER assures positive identification and correlation of large masses of analog or digital data through time-of-day and stop-time printouts, and automatic, fixed-interval printout. A built-in 8-bit μP controls all data entry and formatting functions as well as the output to the

non-impact, 5 X 7 dot matrix type printer. It also operates as a 24-hour day-time and stop-time (clock) with 10-ms resolution. Under μP control, the DDP 5080 prints input data, a 3-digit numerator, the actual time of day, stop-time, and an up-to-four-character alphabetical comment. **Kontron Electronic, Inc.**, 700 So. Claremont St., San Mateo, CA 94402. **Circle 234**

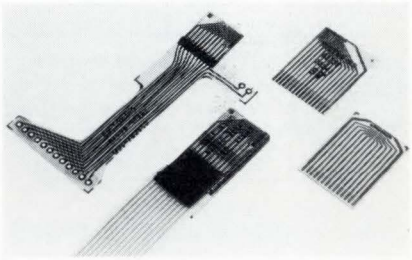
GRAPHICS PRINTERS. Microprocessor-controlled matrix printers are available with a choice of 100 X 100, 70 X 72, 60 X 72 and 60 X 60 dot per inch (horizontal by vertical) densities. The graphics option is available on the 125 and 250 lpm models of the Slimline Series. The printers can reproduce anything that can be displayed on a CRT screen including areas of solid black. The Slimline Series includes 125, 160, 250 and 300 lpm models. All feature program-controlled font selection,

stored program diagnostics and a 500 million-character head warranty. **Okidata Corp.**, 111 Gaither Dr., Mount Laurel, NJ 08054. **Circle 231**

PROGRAMMABLE TERMINAL. Standalone series 116 features a powerful GA16/110 processor, solid-state detached keyboard with typewriter alphanumeric layout and up to 35 programmable keys, separate 4KB display refresh memory, program memory combinations that allow up to 16KB ROM or 128 KB RAM configurations, self-contained desktop design, 12" flicker-free, non-glare 128-char. U & L-case char. set, parallel printer interface, external package mini-diskette, asyn. communications interface, audible alarm and sense switch address recognition. **Computek, Inc.**, 63 Second Ave., Burlington, MA 01802. **Circle 127**

BUBBLE BOARD. The MBB-11 Bubbl-Pac is a companion unit to the MBC-11 Bubbl-Board magnetic-bubble memory devices, and provides 40,960 bytes of formatted, non-volatile data storage. As many as 16 MBB-11 modules can be controlled with one MBC-11 Bubbl-Board controller module. The MBB-11 Bubbl-Pac and MBC-11 Bubbl-Board are both components of the Bubbl-Machine series of magnetic-bubble memory modules for the DEC LSI-11. This bubble-memory system is command compatible with the DEC RXV11/RX01 floppy-disk system. **PC/M, Inc.**, Bubbl-Tec Division, 3120 Crow Canyon Rd., San Ramon, CA 94583. **Circle 220**

PRINT/PLOT MATRIX PRINTHEADS. The DL110/DLP110 dot matrix thermal printhead contains a single column of 10 standard dots and one larger size "plotting" dot. The standard 10 dots allow generation of 5 X 5, 5 X 7, up through 8 X 10 dot



matrix character fonts along with subscript for immediate visibility of the printed character. The DLP110 special version contains a larger size dot specifically designed for use in the plotting function. **Gulton Industries Inc.**, 212 Durham Ave., Metuchen, NJ 08840. **Circle 229**

INSTRUMENTATION BUS ADAPTORS. The BTC-201 and BTC-202 allow Perkin-Elmer minicomputers to communicate with instruments having an IEEE bus interface. The BTC-201 provides an implementation of all 10

IEEE bus functions. The BTC-202 is a BTC-201 minus the controller (IEEE 488 bus function) logic. Applications for the two boards include use in automated test systems, processor to processor communications, and as a peripheral controller. Comprehensive documentation and software support are provided. **BGL Technology Corp.**, Warner Victory Centre, Suite 307, 6355 Topanga Canyon Blvd., Woodland Hills, CA 91367. **Circle 240**

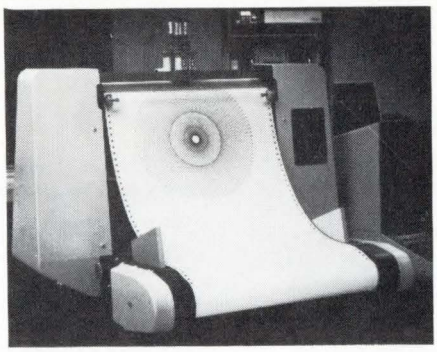
FACTORY DATA COLLECTION TERMINALS. The μP-based 2802 terminals, encased in rugged steel cabinets, offer a full data input capability, including an alphabetical key pad, 10-digit numeric key pad, and 24 programmable function keys to speed transactions by minimizing routine message formatting and data entry. The remainder of the operator interface is provided by a 32-character alphanumeric display with integral time clock and fast card/badge reader. The reader accom-

modates badges of 10 to 22 alphanumeric characters, as well as 80-column punch cards for data entry flexibility. $5000. **General Automation,** 1055 S. East St., Anaheim, CA 92803. **Circle 208**

DIGITAL IMAGE PROCESSING systems, Vision One/20 allows users to enhance an image's brightness, color and definition so data inherent in it becomes more visible. A real-time, interactive, stand-alone system, it provides film-level images on its high-resolution raster monitor. Minimum configuration consists of one B/W image on a 512 X 512 pixel display with no roam capability; The fully extended version has 134 Mbits of memory, color capability, a 1024 X 1024 pixel display and 4096 X 4096 pixel capability. **Comtal Corp.** Box 5087, Pasadena, CA 91107 **Circle 141**

MATRIX PRINTER. This 165-cps printer is programmable from computer or optional keyboard. Bidirectional printing and paper feed gives true graphics capabilities. Special char. sets, including foreign language alphabets, provide flexibility. Adding optional keyboard creates a remote communications terminal. **Microdata Corp.**, 17481 Red Hill Ave., Box 19501, Irvine, CA 92713 **Circle 131**

SERIES OF PLOTTERS. Said to be faster and more flexible than any other plotter line, these plotters are designed to allow both roll and fanfold



paper, and range in width size from 15 to 48 in. with up to four plotter pens. The plotter controller hardware and software is designed to accept logic inputs of 16-bit parallel, 8-bit parallel (GPIB) and RS-232C serial. Compatibility is maintained with Gerber, Tektronix and CalComp data formats. **Logic Systems,** 437A Aldo Ave., Santa Clara, CA 95050. **Circle 228**

FLOPPY DISK DRIVE CONTROLLER is an IBM 3740 compatible controller/interface for Interdata computers. Designed around a state-of-the-art MOS/LSI floppy controller chip, the BTC-101 is fully contained on a single half board. Single sector reads and writes can be fully buffered eliminating the need for a selector channel. The BTC-101 is specifically intended to handle from 1 to 8 Shugart SA800 drives (or equivalent). **BGL Technology Corp.**, Warner Victory Centre, Suite 307, 6355 Topanga Canyon Blvd., Woodland Hills, CA 91367 . **Circle 238**

SERIAL MATRIX PRINTER, the Microline 80, features program-controlled font selection, a 200-million

character head warranty and μP controlled interfaces. The 14 lbs. printer will operate continuously at 80 cps with no duty cycle limitations, producing 9 x 7 upper and lower case characters across an 80 col. page. It will also print condensed characters at 16.5 char/in. accommodating 132 col. formats. Line spacing at 6 or 8 lpi, character spacing and font selection are all under program control. $760. **Okidata Corp.**, 111 Gaither Dr., Mount Laurel, NJ 08054. **Circle 222**

New Products

DISK CONTROLLER. The iSBC 206 disk controller permits designers and users of Multibus-compatible systems to implement very large storage capacities, allowing them to access up to 40 Mbytes of disk storage. The 206 controller can accommodate 8- or 16-bit data transfers, and can handle 16- or 20-bit address-bus structures. The 206 controller can also be used with 8-bit μP-based computer systems using 8080A or 8085A CPUs and compatible with Multibus architecture. The controller will support from one to four standard disk drives including: Diablo 44B; Pertec D3422; Wangco (Perkin-Elmer) ST2222; Caelus 306 R; CDC 9472 "Hawk"; and other drives. **Intel Corp.**, 3065 Bowers Ave., Santa Clara, CA 95051. **Circle 185**

DEC-10 GETS SEMI. Up to 12 Mbytes of MOS memory can be installed in a DECsystem-1091-S configuration. The first 6 Mbytes can be installed in a basic system cabinet; a separate cabinet provides room for the additional memory. The same type of cabinet can be used in DECsystem-2040 and -2060 configurations for memory expansion to a total system capacity of 12 Mbyte. Basic system configurations for the DECsystem-2040 and -2060, and the DECsystem-1091-S, including 1 Mbyte of memory, are $324,600, $399,100, and $440,700 respectively.

PASCAL COLOR. This color graphics computer system is able to be programmed in Pascal or assembler language, and is capable of either stand-alone applications or operation with a host computer. The 6114 Colorgraphic Computer, in its Pascal configuration, consists of a Z-80 operating at 4 MHz with 64K programmable memory, floppy disk controller, a 250 Kbyte single density floppy disk drive, pedestal display unit and the Pascal operating system. Additional features include a CRT-oriented editor to create and update text files, and a file manager which provides for creation and control of files on the floppy disks. $12,000. **Ramtek Corp.**, 2211 Lawson Lane, Santa Clara, CA 95050. **Circle 183**

TEXT PROCESSING SOFTWARE simplifies the preparation, editing and production of documents with the Miniterm Model 1206/DOS portable computer system. The software allows the user to create, edit, manipulate, paginate and print documents on the Miniterm, and/or transmit completed documents over dial-up telephone lines to a copy processing system or phototypesetter for final production. Miniterm includes a 64K processor programmable Basic; a 128-character ASCII keyboard; 80/132 column, 50 cps thermal printer; disk controller and communications interface enclosed in a carrying case. The disk controller in Model 1206/DOS supports up to four double density minifloppy disk drives, for up to 1.44 Mbytes. **Computer Devices, Inc.**, 25 North Ave., Burlington, MA 01803. **Circle 187**

CARTRIDGE DRIVE/S100. The Control Data CMD 16/16 cartridge drive has been interfaced to North Star and Alpha Micro-based systems. The 26 Mbyte drive, S-100 controller, software interface and disk pack are included in a single package. On-line formatted storage capacity of 104 Mbyte can be achieved by a daisy chain of 4 units with an S-100 controller. $9995. **MicroAge**, 1425 W 12th Place, Tempe, AZ 85281. **Circle 191**

TOUCH SCREEN DIGITIZER enables completely untrained personnel to gain access to a data base by simply touching the screen with a finger. The controller provides a convenient interface between the Touch Screen and other computer equipment. It is intended for users who wish to operate the Touch Screen without the delay and the expense of designing their own custom interface. The Digital Controller performs four functions: It provides all digital timing signals required by the screen; measures the time delay between the transmitted signal and the reflected signal from an object touching the glass and allows the resulting data to be adjusted to overlay the display behind the Touch Screen; processes and filters the echo times to produce clean XY position data; and formats the XY data into either parallel or serial form. **TSD Display Products, Inc.**, 35 Orville Drive, Bohemia, NY 11716. **Circle 181**

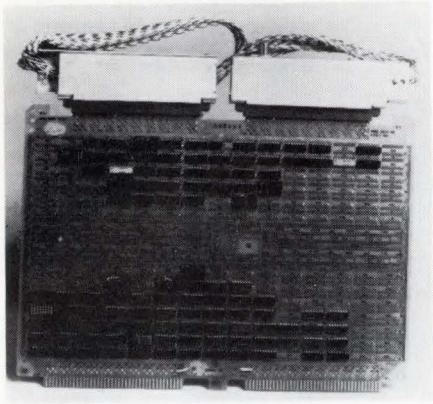
PASCAL ON DG. Regional Data Systems has extended Pascal to make it suitable for commercial applications on all Data General computers. The extensions include STRING and DECIMAL variables, special file handling features for programs that use interactive terminals, random access of files, program segmentation to permit the execution of very large programs, and a generalized interface to the host operating system. Advanced Operating System version, $3500. Single-user RDOS/DOS version, $2500. **Rational Data Systems**, 245 W. 55th St., New York, NY 10019. **Circle 186**

MULTI-USER, MULTI-TASKING small business computer, System 40, comes standard with the multi-tasking operating system Famos and a compiled Basic. The System 40 also includes 64K bytes of memory, two dual sided/double density 8″ floppy disk drives, six serial RS-232 I/O ports, vectored interrupt, real time clock in a 27″ high EAI cabinet with Formica top. The system accommodates up to 5 CRTs and a printer. In addition to supporting multiple CRTs, the System 40 can run additional jobs in background. **Integrated Business Computers**, 22010 S. Wilmington Ave., Carson, CA 90745. **Circle 190**

CROSS ASSEMBLER is designed to assemble Z80 and 8080 Source Programs into machine code for Z80 and 8080 - Intel, Zilog, National and AMD Microprocessor. Designated the EXOR 80/XASM, it permits the user to assemble Z80/8080 code on the Motorola EXORterm terminal and EXORciser development systems products thus expanding the useage and flexibility for software development. The EXOR80/XASM runs under MDOS I, II and III; object and source remain on the development system for changes and efficient handling. Editing and PROM programming can be handled with standard EXORcisor software. $395. **Phoenix Digital Corp.**, 3027 N. 33rd Drive, Phoenix, AZ 85017 . **Circle 176**

4-CHANNEL ANALOG OUTPUT. MP1104 analog putput peripheral board is electrically and mechanically compatible with and interfaces directly to DEC's "Q" bus. It is plug-in compatible with LSI-11, LSI-11/2, LSI-11/23, PDP-11/03 and PDP-11/23. MP1104 consists of four 12-bit D/A converters plus address decoding and control logic. The MP1104's 4-channel output system accepts 12-bit inputs from the data bus and converts them to analog outputs with an accuracy of ±0.025% FSR. Output ranges are strap selectable at ±10V, 0 to 10V, ±5V, 0 to 5V and ±2.5V at 5mA. Temperature coefficient of accuracy drift is ±30ppm of FSR/°C. $550. **Burr-Brown**, Tucson, AZ 85734. **Circle 180**

New Products



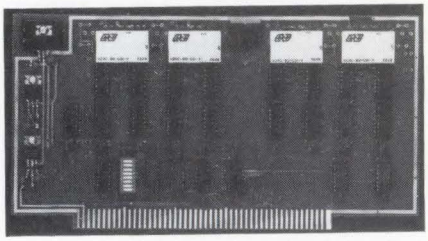
TI DATA ACQUISITION. The IFM-TI 990/10 is a Direct Memory Access (DMA) computer interface module assembled on a TI Universal Wire Wrap Board. It plugs directly into the TI990 mainframe or any remote Tiline Bus Chassis – only a single card slot is required. The interface is designed for data acquisition systems with thruput rates up to 1 MHz per channel. Modes of operation include single cycle and two jumper programmable modes – burst and block-to reduce the effects of bus latency. $6500. **Phoenix Data, Inc.**, 3384 W. Osborn Rd., Phoenix, AZ 85017. **Circle 219**

A COBOL-BASED TRANSACTION PROCESSING system for Perkin-Elmer Series 3200 minicomputers consists of Cobol, data management, and transaction processing software. "Reliance" supports up to 128 transaction processing users and provides integrity, security, and reliability. $12,500. Reliance assures data integrity through unique automatic record locking, on-line transaction rollback, and system-wide recovery features. Test time is reduced through facilities that provide batch simulation of anticipated transactions. In addition, RPG II ($2,500) enhances the Reliance environment with a batch-oriented report generating facility. **Perkin-Elmer**, Computer Systems Division, 2 Crescent Place, Oceanport, NJ 07757. **Circle 218**

CARD READER/S-100 interface, MR-500, accepts cards of any length marked with a standard number two pencil. The card is hand-fed into the unit which turns on automatically. Output consists of both card image (two bytes per column) and one byte of the Hollerith converted to ASCII data. Other interfaces are available for TRS-80, Apple II and PET computers. MR-500 with S-100 Buss Interface, $895. **Chatsworth Data Corp.**, 20710 Lassen St., Chatsworth, CA 91311 **Circle 225**

SBC has 6800 MPU, 6850 serial I/O, 2 6820 parallel I/O (32 lines), 512 RAM, socket for 2708, 2716, EROM. Interface modules for industrial control, data acquisition, lab instrumentation, on 44 pin 4½" X 6½" PCB's. RAM, ROM, CMOS RAM/battery, A/D, D/A, Driver/Sensor, Serial I/O, Parallel I/O, Counter/Timer, IEEE 488 GPIB, floppy controller. $99.5 (500). **Wintek Corp.** 902 N. 9th St., Lafayette, IN 47904. **Circle 134**

S-100 D/A BOARD is designed for applications requiring high speed D/A conversion including real time applications. This board supports four inde-

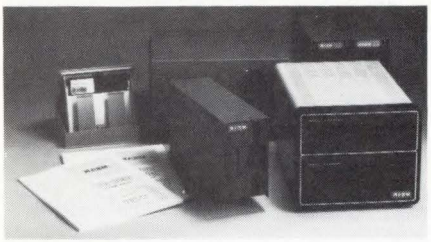


pendent high speed DACs with associated latches. Each DAC operates completely independent of the rest. The DACs have a conversion time of 3 μsec which enables them to operate at maximum computer speed. A 12 bit latch drives the inputs of each DAC. $395. **Tecmar, Inc.**, 23414 Greenlawn Ave., Cleveland, OH 44122 **Circle 224**

COMMUNICATIONS STORAGE UNIT, the Comm-Stor II, consists of a single or dual drive diskette system which can be used to store messages received on-line or to prepare messages off-line for transmission. The unit has a capacity of 255 kchar. for the single drive and 512 kchar. for the dual drive system. Both single and dual drive systems are equipped with three ports to interface with an asynchronous terminal, a data set and a printer. Optional features will be available to provide

extensive forms prompting, message storage features, editing and message file management capabilities. Each diskette of the Comm-Stor II contains a directory which lists all messages stored on the diskette. **AT&T**, 195 Broadway, New York, NY 10007. **Circle 209**

MINI-DISKS FOR 6800/6809. The LFD-800 stores 200 Kbyte in single-density format on 77 tracks, and is available in one-, two- and three-drive configurations. The LFD-1000 is a



dual-drive system that stores 400 Kbyte per disk – 800 Kbytes per system – in double-density format on 77-track disks. Two LFD-1000 systems provide the user a total of 1.6 Mbytes of on-line storage. A system is supplied complete with an SS-50 bus controller/interface PC card, an operating system on EPROM, an operator's manual and an interconnecting cable. **Percom Data Co.**, 211 N. Kirby, Garland, TX 75042. **Circle 230**

DATA COMM TESTER. The 833 weighs only 12 lbs. and is completely self-contained in a compact, rugged carrying case. It provides 80 to 90% of the functions supplied in data comm analyzers costing 3 to 4 times as

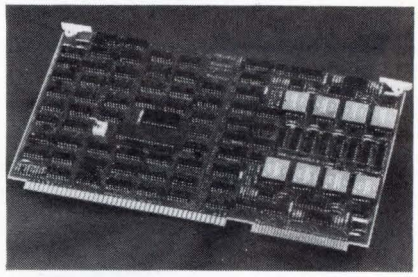
much while freeing up service specialists time for more in-depth analysis, the company said. The 833 efficiently isolates the equipment that is malfunctioning in a network by simulating the data communications equipment (DCE) to verify correct operation of the terminals or CPU, or by performing standard BERT/BLERT tests on the entire transmission link to verify correct operation of the modems or phone line. $2,750. **Tektronix, Inc.**, M. S. 63-635, P.O. Box 500, Beaverton, OR 97077. **Circle 236**

ADDRESSABLE SEVEN SEGMENT LED features data read directly from μP I/O bus, on-board 8 X 8 RAM and MUX logic. Data may be displayed directly (8 bits/digit) or automatically decoded from four bit Hexadecimal or Code-B to seven segments, right-hand decimal point at each digit. Single supply 5 Vdc power requirement, and very low power stand-by mode. **I.C.I.**, Box 17927, Irvine, CA 92713.
Circle 226

F6802 μP offers an on-chip power-on reset function, on-board clock for easier use and on-board 128 X 8 RAM with options of 8-byte or 32-byte power-down. Now you no longer need an additional RAM with battery back-up systems. F6802 features a memory-ready line for slow or fast memory. So you can use memories in synchronous or asynchronous mode. And F6802 is bus-compatible for easy use with all other F6800 peripherals. **Fairchild Camera and Instr.** Box 880A, Mountain View, CA 94042 **Circle 137**

SWAPPING MEMORY was created to provide Perkin-Elmer computer users with a low cost means of greatly increasing throughput of a disk access bound system. Any system which uses an overlayed OS, or task overlays, or CSS, or the Roll option, or scratch/temporary files will exhibit a significant increase in execution speed when critical files are moved from slower hard or floppy disks into the Swapping Memory's semiconductor memory. The average access time (head movement and rotational delays) on the hard disk is 50.5 ms. There is no such access delay for the swapping memory. Even once the sector is found, the swapping memory transfers bytes at 320% of the rate of the disk. And this percentage is assuming only a one ms main memory. Some processors will support higher rates for the swapping memory. **BGL Technology Corp.**, Warner Victory Centre, Suite 307, 6355 Topanga Canyon Blvd., Woodland Hills, CA 91367. **Circle 239**

BUBBLE MEMORIES. The PBM 8OS memory is a 'Multibus' compatible 500K bit card configured with 64K bit devices. The unit offers a 100K bytes data rate when operated as a program loader or backing store. The PBM 8OM memory is expandable up to 2M byte. An average access time of 7ms gives the 2M-bit memory card a speed advantage over disk and tape memory when interfaced to the Multibus via the PBM 8OMC controller card. Up to eight memory cards can be



bussed from one controller. **Plessey Microsystems Inc.** 19546 Clubhouse Road, Gaithersburg, MD 20760.
Circle 129

New Products

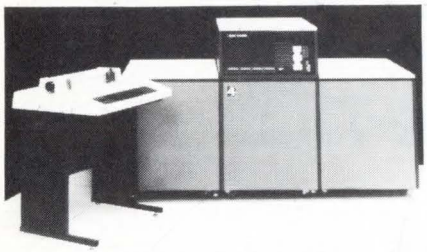
DIGITAL CASSETTE SYSTEM, MT-2, provides low-cost alternative to floppy disk in mass storage applications requiring high-speed data transfer and high reliability. A fast search function allows forward searching on the tape at 45 ips. The only moving parts are the two reel motors and a disk encoder – so maintenance is kept to a minimum. Four versions of the MT-2 are available,

two of which incorporate a unique built-in micro-controller. The MT-2 is compatible with ISO, ANSI, JIS and ECMA phase encoding standards. **Teac Corp.**, 11.1 Chome, Tsukiji, Chuo-ku, Tokyo 104, Japan. **Circle 210**

DESKTOP SYSTEM/TERMINAL. Microterm II enhancements include a floppy disk drive with quadrupled storage capacity. Three diskette drives are now contained within the desktop cabinet. In addition, formats for the CRT screen can now be simply prepared by the operator. Microterm II's Extended Business Basic is also extended to include six added functions to increase its scientific capabilities, improve throughput speed, facilitate local and remote interactive operations, optimize the use of subroutines, shorten software development time, and aid in developing structured programs. **Digi-Log Systems, Inc.**, Babylon Road, Horsham, PA 19004. **Circle 227**

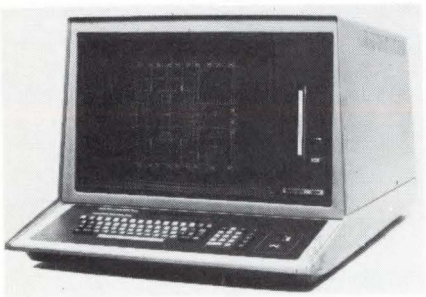
THE IMAGE PROCESSING LIBRARY is composed of 11 2-dimensional filtering, convolution and Fast Fourier Transform (FFT) routines. The routines provide array processor users with the computational tools to filter and enhance monochrome color, and multi-spectral scanner images. These routines are written in AP Assembly Language but callable from host Fortran. $500. **Floating Point Systems, Inc.**, P.O. Box 23489, Portland, OR 97223. **Circle 202**

THE META 4/5030 is based on a microprogrammed minicomputer. Over 2 Mbyte of 500 ns semiconductor memory can be added. A memory interfacing technique nearly halves the time required for an I/O device to gain direct access to me-



mory. Other standard hardware features include memory protection, memory error detection, and the Sentry system monitor, a watchdog that warns users of any variances in AC or DC voltages, or system cooling parameters through visual and audio alarms. The DNA Multiprogramming Time-Sharing Operating System supports concurrent time-sharing, teleprocessing, and batch mode processing. High-level languages supported include Cobol, Fortran, Basic, APL, and RPG-II. **Digital Scientific,** 11425 Sorrento Valley Rd., San Diego, CA 92121. **Circle 221**

DYNAMIC GRAPHICS provides 4054 terminal users with the power to work directly with the graphic elements of a design problem, in addition to points and lines. With Basic language commands, dynamic graphics allows the user to quickly and easily create and manipulate complex graphics objects. μP rapidly retraces from dynamic memory those objects selected by the user for display, adding non-stored images and alphanumerics to the storage display. With over 13 million addressable points, the 4054's 19-inch direct view storage tube offers the high resolution graphics. Refresh objects can be moved around the screen either under program control or interactively with the thumbwheels or an optional graphic input device, such as the Joystick or Graphic Tablet. An object stored in the dynamic memory can be displayed on the screen up to 100



times faster than by drawing it directly from a program onto the screen. **Tektronics, Inc.,** M. S. 63-635, P.O. Box 500, Beaverton, OR 97077. **Circle 235**

★ In Half the Space ★ Up to 25% Savings ★

RX02-Compatible Double Density Floppies for the LSI-11/2

And Have it Your Way

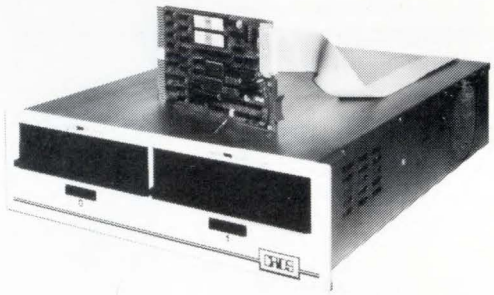
With the LSI-11/2 built-in: The MF-211 Dual Floppy/LSI-11/2 does everything the 11V03-L will do . . .

The MF-211 Dual Floppy/LSI-11/2 System, using the CRDS Double Density Controller, is functionally identical to the DEC 11V03-L, but using only 10½" rack space. The MF-211 is the perfect low-cost answer to your 11V03-L requirement.

Check These Additional Features:

- Functionally identical to DEC's 11V03-L
- Double and Single Density Operation
- Complete Software/Media Compatibility with LSI-11/2
- Over One Megabyte Storage Per System
- Available with 4 Quad Slot or 8 Quad Slot Backplane
- DEC Software and Interface Cards available as options
- 30K Addressable Memory
- Considerable Dollar Savings

To go with your LSI-11/2: The FD-211 Dual Floppy System is the perfect plug replacement for your RX02 . . .



The FD-211 Double Density Floppy Disk System, using the CRDS Double-Density Controller, is totally software/media compatible with the Digital Equipment RX02 Floppy Disk System. It provides a compact, low-cost and highly reliable solution for all RX02 applications.

Check These Additional Features:

- 5¼" Low Profile Chassis
- Dual Shugart Drives
- 512K Bytes Per Drive
- Front Panel Write Protect Switches
- Photocell Write Protect
- Complete Instruction Manual

Why CRDS Products Give You So Much:

In addition to providing complete RX02 instruction set compatibility, the CRDS floppy disk controller card offers DMA data transfer by sector, bootstrap loader (eliminating need for DEC's REV-11 or BDV-11), IBM 3740 formatter, self-diagnostic, and interface electronics, all contained on a single dual-height card which plugs directly into the H9270 backplane. To design and package sophisticated controller electronics on a single dual-height card is a unique CRDS achievement, unmatched by any other controller supplier in the industry.

- RX02 Double Density and Single Density Operation
- Complete RX02 Software/Media Compatibility with LSI-11/2
- Integral Bootstrap Loader
- Built-In Self-Diagnostic, Formatter
- Dual-Height Controller for LSI-11 or LSI-11/2 Backplane

For more info on our FD-211 and MF-211 Double-Density Floppy Disk Systems, just call or write:

Charles River Data Systems, Inc.

CRDS

4 Tech Circle, Natick, MA 01760 Tel. 617 655-1800 TWX 710 386 0523

Circle 100 on Reader Inquiry Card

New Products

CAPACITIVE KEYBOARDS. Longer life, greater reliability is offered by the "Golden Touch" capacitive keyboard, hinged-moving plate design. It creates a capacitive effect with a hinged moving plate and one fixed plate, both attached to the PCB. This gives the keyswitch greater capacitance, at any given displacement, than the sponge-on-a-stick design used in other capacitive keyboards. It's rated at 250,000,000 MCBF with a 2-year warranty. **Digitran Corp.**, 855 South Arroyo Pkwy., Pasadena, CA 91105. **Circle 142**

S-100 A/D BOARD is designed for applications requiring high speed A/D conversion including real time applications. This board interfaces the Analogic MP 6812 Complete Data Acquisition System to the S-100 bus. The board accepts 16 single ended inputs and can be used to do A/D conversion for data throughputs up to 30 KHz with 12 bit accuracy. The board provides two's complement right justified outputs. The input ranges are ±10V, ±5V, 0 to +10V, or 0 to +5V. The board may be strapped to act as an I/O device (requiring four I/O ports) or to act as a memory mapped device (requiring four memory locations). $495. **Tecmar, Inc.**, 23414 Greenlawn Ave., Cleveland, OH 44122. **Circle 223**

MATRIX PRINTER. This μP-compatible (accepts BCD, RS-232 and parallel/serial ASCII) alphanumeric printer uses "spanning hammers". Each hammer impacts the steel drum to form the characters in three columns. There are no needles to bend, break or jam. Only 7 hammers handle for 21 columns. It has 54 char., 2-color printing in all columns. Speeds to 90 lpm; paper feed, 10 lps. $325. **Sodeco**, part of Landis & Gyr, 4 Westchester Plaza, Elmsford, NY 10523 **Circle 132**

TWO 256KB ADD-IN memory systems are the 256KB DR-123S for Data General's Nova 3 series and the 256KB DR-125S for the Data General Eclipse. Packaged on 15″ x 15″ board are 32KB, 64KB, 192KB, and 256KB DR-123S configurations. Parity is standard. Cycle and access times are 500 and 325 ns, respectively. The 128KB (64K x 17) DR 123S, $3,000; the 256KB (128K x 17), $5,090. The DR-125S is available in capacities of 64KB, 128KB, 192KB, and 256KB. Single bit error correction is standard. The DR-125S cycle time for a read cycle is 500 ns and a write cycle is 700 ns. Access time is 350 ns. **Dataram Corp.**, Princeton-Hightstown Rd., Cranbury, NJ 08512. **Circle 258**

New Products

Z-80 DART (Dual Asynchronous Receiver/Transmitter), a multi-function peripheral component offers two independent full-duplex channels with separate modem controls. Used as a serial-to-parallel, parallel-to-serial converter/controller, it is suitable for applications in smart and dumb terminals, peripheral controllers, and any controllers requiring only asynchronous protocol. **Zilog**, 10340 Bubb Rd., Cupertino, CA 95014. **Circle 189**

WIDE-RANGE MULTIPLEXER SYSTEM consists of a multiplexer, programmable gain amplifier, sample and hold amplifier and an analog-to-digital converter (ADC). The Mod 3000 accepts differential or single-ended signals, or both. It functions in the range of ±5 mV to ±10.240 V full-scale, making it suitable for operation with such low level sources as strain gages and thermocouples, and with potentiometers and other high level sources. $3600 for a multiplexer/ADC system, $1,600 for a multiplexer only. **Tustin Electronics Co.**, 1431 E. St. Andres Place, Santa Ana, CA 92705. **Circle 159**

18-BIT RESOLUTION D to A converter provides 16 bits of accuracy, offer integral nonlinearity and differential nonlinearity TCs of ±0.5ppm/°C, offset TC of ±0.5ppm/°C and gain TC of ±0.5ppm/°C. Long-term offset and gain stability is specified at ±8ppm for 1,000 hrs. DAC 1137 settling times are 8μs to ±1/2 LSB in voltage mode. Outputs are 0 to +5V, 0 to +10V, ±V, ±10V, or -2mA to 0mA. Inputs are TTL-compatible, in binary or 2's complement coding schemes. $460 (1-9). **Analog Devices, Inc.**, Box 280, Rte. 1 Industrial Park, Norwood, MA 02062. **Circle 296**

DEC ADD-IN. Compatible with DEC's LSI-11/23, the 94123 add-in also has downward compatibility with DEC's existing LSI-11/2 and LSI-11 models and is available in either a 64 or 128 KB capacity. Other features include on-board parity and refresh circuitry. Maximum memory expansion can be achieved using only two instead of four boards. 64 KB 94123, $1,050. **Control Data Corp.**, Box O, Minneapolis, MN 55440. **Circle 177**

"8080 MICROCOMPUTER EXPERIMENTS", a 354-pg. book by Howard Boyet, provides over 80 hands-on experiments for E & L Instruments MMD-1 trainer. Software, hardware and interfacing are presented, but the paperback intentionally doesn't cover complete theory of architecture, logic design or languages. $13.95. **Dilithium Press**, Box 555, Forest Grove, OR 97116. **Circle 116**

ALPHANUMERIC PRINTER is available as an accessory for the Betascopes, TC 2000 and TC 1500, provides the user with a permanent record of his measurements, and of all measuring parameters. Used with the TC 2000, it also provides complete statistical data based on measurement results. The electrostatic printer uses aluminized paper, is capable of speeds up to 120 lpm, and has three column widths of 20, 40 or 80 char. per line. **Twin City Testing Corp.**, P.O. Box 552, N. Tonawanda, N.Y. 14120. **Circle 146**

RAM FAMILY. The BLC-032, BLC-048 and BLC-064 provide 32K bytes, 48K bytes and 64K bytes of dynamic RAM respectively. Each board includes all refresh, timing, control and buffering circuitry, and 20-bit address decode, which allows use in a 1 Mbytes memory. Access time is 430 ns. **National Semiconductor**, 2900 Semiconductor Drive, Santa Clara, CA 95051. **Circle 188**

BATTERY BACKUP options permit the microNova MP/100 and MP/200 μCs to operate during a temporary power failure. With the addition of the Model 4315 battery backup board and either the optional Model 4316 battery pack or two ordinary car batteries, users can keep MP/100 or MP/200 computers – not just main memory – operating when the main AC power isn't. All voltages are maintained and fans kept operating so that all chassis-mounted components can operate in a normal manner. 4315, $400; 4316, $100. **Data General,** Route 9, Westboro, MA 01581. **Circle 178**

LINE PRINTER CONTROLLER. The Model 370 is a single board controller that enables dot matrix, band, or impact printers from various manufacturers to interface directly to Data General computers. The controller minimizes the CPU overhead normally required by programmed I/O controllers. Differing interface techniques by printer manufacturers are accommodated within the controller by selecting appropriate jumper conditions for data and status polarity command code decoding or inhibit and tabbing operations. The Model 370 is fully compatible with the instruction set and operating systems software offered by Data General. **Custom Systems, Inc.,** 2415 Annapolis Lane. Minneapolis, MN 55441. **Circle 165**

μPGRAPHICS SOFTWARE. A demonstration disk fully integrates the Hi-Pad Digitizer from Houston Instruments with any North Star-based computer and Vector Graphic's High Resolution Video Display. The Hi-Pad Digitizer allows graphics input on a microcomputer with both serial and parallel interfaces as standard features. In addition to resolution by inch, metric measurement is also included on the Hi-Pad. Demonstration disk, $35; Hi-Pad Digitizer, $795. **Micro-Age Wholesale,** 1425 W. 12th Place, Tempe, AZ 85281. **Circle 182**

16K-BYTE RAM, the BLC-8016, has an access time of 430 ns and a full read or write cycle of 660 ns. Its maximum power requirements are 82% of those of the BLC-016. The new board operates as either an 8-bit or 16-bit memory, allowing on-board operation in 16-bit systems. The BLC-8016 operates in either advanced or delayed write modes. It has logic circuitry for battery backup and memory protection as well as for user-installed byte parity. It decodes 20 address bits, allowing use in 1 Mbyte systems. $822. **National Semiconductor,** 2900 Semiconductor Drive, Santa Clara, CA 95051. **Circle 184**

16KBYTE STATIC RAM memory boards are described in two data sheets. The new memories feature on-board memory management system which allows working memory to be expanded to greater than 64K. Memory access time is quoted at either 250 or 450 ms. Other features of this S-100 bus board include a dedicated ROM option – shunt selectable – to disable from 1 to 15 Kbytes in 1K increments from either end of memory. **Industrial Micro Systems, Inc.,** 628 N. Eckhoff, Orange, CA 92668. **Circle 107**

TRI-DENSITY MAGNETIC TAPE DRIVE and tri-density formatter-controller provides 800, 1600 and 6250 bpi, nine track data formats. Any of the three formats can be selected manually, or automatically under program control. Tape speeds of 45, 75, or 125 ips can be specified and an optional dual speed capability allows selection of two different operating densities. The tri-density drive also features automatic tape loading, and the Telex Supr-Lite capstan, with low inertia for fast starts, stops, and rewinding at 500 ips. **Telex,** 6422 E. 41st St., Tulsa, OK 74135. **Circle 179**

Programmable Devices:

Their Advantages and Disadvantages, and Equipment to Program Them – Part 2

William E. Gundling and Peter A. Schade
International Microsystems

Field service PROM programmer, Kontron Electronics.

One of the easiest and most cost-effective methods of programming PROMs involves using a commercial PROM programmer. Let's look at the different types of commercially available PROM programmers in terms of their functions and end use.

Five types of PROM programmers are available: dedicated, development system, quasi-universal, full-universal and production system. Each type possesses a distinguishing set of capabilities to fit specific applications.

1. Dedicated PROM Programmers program only one type of device and usually only handle very limited amounts of data and sometimes require external DC power sources. They are advantageous when you must program only a few PROMs and manipulate very little data, and also foresee no future requirements for different PROMs or device types. Dedicated programmers are usually low-priced and find their widest acceptance in the personal computer market.

2. Development System Programmers. Many development system manufacturers offer PROM programming options for their equipment. These programmers usually rely on the development system for PROM data source and manipulation. Most development systems can program a very limited number and type of PROMs; and since they usually take a long time to program the parts, they tie up the development system too much. However, you need only one piece of equipment for the development system and PROM programmer.

Gang PROM programmer, Shepardson Microsystems.

3. Quasi-Universal Programmers. If a PROM programmer cannot program most of the available devices, we call it a quasi-universal instrument. For example, it may program all the different chips of one type of device, such as UV-erasable PROMs. These programmers usually offer some data manipulation and interfacing capabilities. Although they generally cost almost as much as a full-universal PROM programmer, they are not as flexible in operation and application.

4. Full-Universal PROM Programmers are most popular of PROM programmers. The universal not only programs PROMs, but also other types of programmable devices. They also usually offer the best data handling and data manipulation capabilities, plus interfacing ports as standard features or as options. Their manufacturers, who do keep up with the state-of-the-art in

Universal PROM programmer, Sunrise Electronics.

programmable devices, keep their units capable of programming new devices. Users most often choose universals for flexible, all-around PROM programming systems.

5. Production PROM Programmers come in two different forms: one for MOS devices, the other for bipolar. It takes a relatively long time to program MOS PROMs – 100 to 400 seconds/part. If programming requires an average of two minutes, and if you allow some overhead time for inserting and extracting the part, a single-socket programmer can process about 25 parts/hr. Programming a number of parts simultaneously can supply more throughput.

Therefore, makers market production MOS programmers capable of programming between 8 and 16 PROMs at once. However, because these gang systems require a significant amount of operator parts handling, the instruments must perform various error checks not only on the devices under test, but on operator performance. Also, the production environment makes simple and easily-performed maintenance mandatory.

Production PROM programmers for bipolar PROMs must overcome a different set of problems. First, unlike MOS PROMs, very few bipolar PROMs share the same programming algorithms (though they may offer the same pin-for-pin functions); and thus, production bipolar programmers should be universal. Second, because bipolar PROMs are programmable in relatively short times, typically between 1 and 10 seconds, a single-socket instrument can program about 300 parts/hr. A bipolar production programmer, equipped with an automatic IC inserter and extractor, reduces operator parts handling.

PROM programmer applications

The type of PROM programmer required and the features desired depend largely on individual applications. How do you determine which PROM programmer you need for these three applications: field servicing, manufacturing (programming large numbers of PROMs) and development work?

Field Service. When PROMs are used for program or data storage, field service personnel need a PROM programmer, because the instruments to be serviced may require custom changes in the program or field updating.

Here's six purchasing questions for field service PROM programmers. (1) Is it portable? Will the carrying case fit under an airplane seat? (2) Is the unit sturdy enough to be checked on an airplane? (3) Can the instrument program all the devices needed? (4) Can the unit transfer files via a modem over a telephone line? (5) Does it provide good editing capabilities? (6) Are the editing and other functions easy to use?

Interfacing the instrument to a telephone line for file transfers can become an important capability. The growing complexity of microprocessor applications can make program chang-

International Microsystems PROM programmer interfaced with an Exatron IC handler.

ing in the field a major obstacle. The ability to transfer information over a phone line allows programming changes to be made at a central location, plus immediate verification by the field service engineer at the customer site. The editing capability of field service PROM programmers is also important for making PROM corrections and updating them efficiently. The more powerful the editing system in the PROM programmer, the easier it is for field service engineers to make the required changes.

Manufacturing. Purchasing questions for the manufacturer who wants to program large quantities of PROMs are as follows: (1) Does the instrument program PROMs to the device manufacturer's specifications? (2) Does each device manufacturer qualify the instrument for programming its parts? (3) How fast does the instrument program the devices? (4) Can you interface the unit with IC handling equipment? (5) Can it program all the devices used? (6) Can nontechnical personnel operate the unit? (7) Does the unit provide error-checking signals for backward insertion and missing pins? (8) Can you repair it easily in-house, when necessary?

Since nontechnical personnel almost always operate production PROM programming instruments, they must be made to understand that the parts being processed range in price from $10-$100. Therefore, they must prevent part destruction, as well as help identify bad devices. They must be taught to eliminate one of the most common of operator errors of inserting parts backwards. A good production PROM programming instrument should inform the operator that parts have been inserted backwards or are unacceptable for a number of reasons, such as missing pins.

The production department must also know how easy it is to repair the programmer. The supervisor must decide whether his personnel can repair the equipment in house to prevent long down times.

Development. Purchasing questions to ask when purchasing a PROM programmer for development are as follows: (1) Does the instrument program a wide range of programmable devices, including bipolar PROMs, MOS PROMs and programmable microcomputer chips? (2) Will it program new devices as they are introduced? How will it do it? (3) Can you interface the programmer easily with a computer or development system to down-load PROM data? (4) How easy is it to use? Is the keyboard and display of high quality? (5) Does the programmer provide the desired editing capabilities?

In development work, the engineer is typically interested in programming many different types of devices, in getting the PROM data easily from a computer to the PROM programmer and in editing the PROM data quickly. An engineering development instrument must handle future types of programmable devices – not just current types. An instrument that uses "personality" modules usually will be adaptable to new types of programmable devices; they won't become obsolete in the near future.

The nearby "PROM Programming Instrument Buying Guide" lists various manufacturers of PROM programmers and products they market for field service, production and development. For addresses, refer to the "PROM Programmer Manufacturers."

Other Considerations

In addition to the main requirements for specific applications, consider other factors when selecting a PROM programmer. For example, the specific method by which an instrument performs its chief task of programming PROMs can affect the user in the following ways: (1) certain instruments need frequent user calibration (a requirement usually detectable by a short warranty period), (2) instruments which program PROMs via a μP that controls the programming algorithms can adjust to the continually changing specifications; instruments which program PROMs with hardware logic cannot, and (3) since IC manufacturers are constantly introducing new programmable devices, instruments with personality modules can keep abreast of these developments; instruments without personality modules cannot.

One important function many users require of a PROM programmer is ability to interface to other peripherals. Is it simple? Yes and no. It may be as simple to accomplish as connecting a paper tape reader to the PROM programmer – or as complicated as interfacing with a computer. Get this information by asking these questions:

- Can the PROM programmer accept file transfers? If so, what is the required data format and are other formats available? If file transfer format you use is unique, you may have to change your format or find out whether the PROM programmer can be set up to receive your file.
- Can the PROM programmer be operated remotely? Remote operation can add greatly to the flexibility of your system and make data transfers easier.
- How easy is the PROM programmer to interface? Are the interface ports standard items or extra-cost options? How many are there? Do they meet your needs?

Some programmers provide very little editing capabilities; others, many. The important questions to ask are:

- What are the editing commands and are they easy to use? Can you operate over the whole area of the PROM or RAM, or only at particular locations? The larger the area you can work, the more flexible the unit.
- Do editing commands, such as INSERT or DELETE, work over limited fields or do they always affect the entire RAM? If you cannot protect blocks of data, the editor can be difficult and confusing to use.

Although PROM programmer manufacturers seldom advertise that they are willing to design new instruments or modify existing units, many vendors will undertake custom requirements for OEMs. For example, International Microsystems has produced a custom PROM programmer for a large manufacturer of numerical controllers. This instrument retains all the standard capabilities, plus allowing the generation of special controller commands to be entered into a PROM.

While all PROM programmers chiefly program PROMs, major differences exist in how they function. Begin the selection process by first reading the data sheets; then, determine which instruments fit your needs. Be sure to ask for a demonstration from the manufacturers of the programmers that interest you. At minimum, ask to see two different programmers. A demo can show you how easy each of the chosen PROM programmers is to operate and gives you added assurance that the instrument can solve your specific needs. If your instrument uses them, how would you change personality modules? Find out! Make sure the display is easy to read; and operate the unit yourself to get a feeling for its smoothness of operation. Most of all, make sure that it does what you want it to do.

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PROM Programming Instrument Buying Guide

Manufacturer	Application	Model	Type	Comments
Curtis Electro	Field Service	PD3000S	Dedicated	Manual Unit Programs Signetics Bipolar PROMs
		PD3000T	Dedicated	Manual Unit Programs TI Bipolar PROMs
	Manufacturing	PD2000S	Dedicated	Duplicator Programs TI Bipolar PROMs
	Development	PD3000S	Dedicated	
		PD3000T	Dedicated	
Data I/O	Field Service	System 19	Universal	
	Manufacturing	System 17	Universal	
		Model 5	Universal	IC Handler Interface option
		Model 16	Quasi Universal	16 Gang PROM Programmer Programs most of the MOS PROMs
	Development	System 19	Universal	
E-H International	Field Service	Model 4 & BPS-4	Quasi Universal	Programs most of the MOS EPROMs and some Bipolars
	Manufacturing	Model 4 & BPS-4	Quasi Universal	IC Handler Interface option
		Model 16B	Quasi Universal	16 Gang PROM Programmer Programs most of the MOS EPROMs
	Development	Model 4 & BPS-4	Quasi Universal	
International Microsystems, Inc.	Field Service	IM1010	Universal	
	Manufacturing	IM1010	Universal	IC Handler Interface option
		IM2020		16 Gang PROM Programmer Programs most of the MOS EPROMs
	Development	IM1010	Universal	
Kontron	Field Service	MPP80S	Universal	
	Manufacturing	MPP80P	Universal	Personality Modules to Gang 8 EPROMs
	Development	MPP80E	Universal	
Oliver Advanced Engineering	Field Service			
	Manufacturing	UPP2700	Quasi Universal	16 Gang PROM Programmer Programs most of the MOS EPROMs
	Development	PP Series	Dedicated	Connects to Development Systems
Prolog	Field Service	M900-M900B	Universal	
	Manufacturing	M910	Universal	Personality Modules to Gang 8 EPROMs IC Handler Interface option
	Development	SM12708	Dedicated	
Stag	Field Service			
	Manufacturing	PPG	Quasi Universal	15 Gang PROM Programmer Programs most of the MOS EPROMs
	Development	PPX, PPX Plus	Universal	
Sunrise Electronics	Field Service	Smarty	Universal	
	Manufacturing	Smarty	Universal	16 Gang Personality Modules IC Handler Interface option
	Development	Smarty	Universal	

PROM Programmer Manufacturers

Curtis Electro Devices
P.O. Box 4090
Mountain View, CA 94040
415/964-3136

Data I/O
P.O. Box 308
Issaquah, WA 98027
206/455-3990

E-H International, Inc.
515 Eleventh Street
Oakland, CA 94604
415/834-3030

International Microsystems, Inc.
11554 C Avenue
Auburn, CA 95603
916/885-7262

Kontron Electronic, Inc.
700 South Claremont Street
San Mateo, CA 94402
415/348-7291

OAE, Inc.
676 West Wilson Avenue
Glendale, CA 91203
213/242-0080

Pro-Log Corp.
2411 Garden Road
Monterey, CA 93940
408/257-9900

Shepardson Microsystems, Inc.
20823 Stevens Creek Blvd., Bldg C4-H
Cupertino, CA 95014
408/257-9900

Stag Systems
2465 E. Bayshore, #329
Palo Alto, CA 94303
415/324-1564

Sunrise Electronics
307-H South Vermont Ave.
Glendora, CA 91740
213/963-8775

Product Index

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Principles of Data Acquisition and Conversion – Part 4

Eugene L. Zuch,
Datel Systems, Inc.

In the first three parts, we covered quantisizing and sampling theory, amplifiers and filters, settling time, digital coding, DACs and ADCs. Using multiple A/D converters raises systems costs, so analog multiplexers make sense.

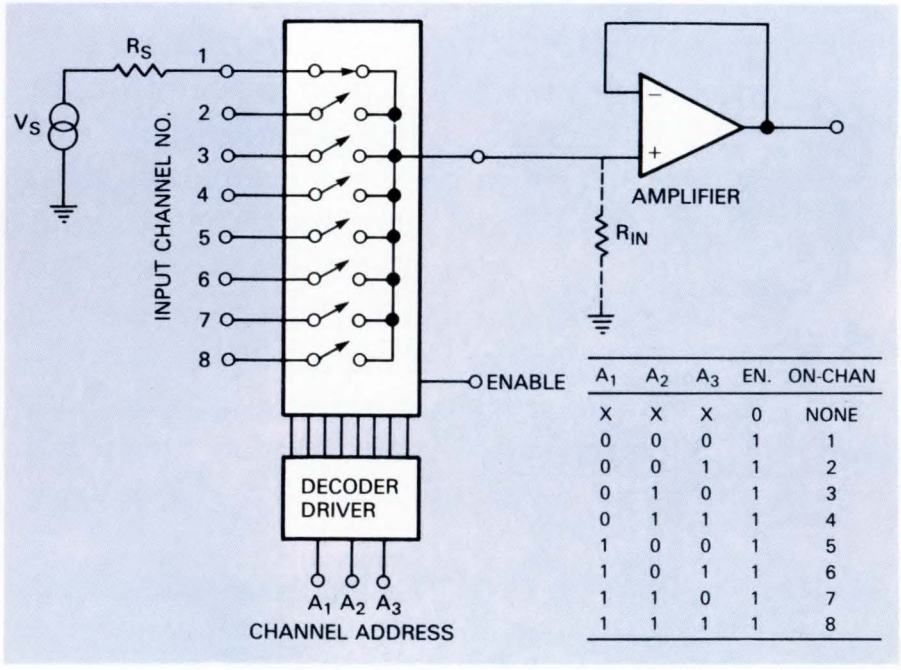
Analog Multiplexers

Analog multiplexers are the circuits that time-share an A/D converter among a number of different analog channels. Since the A/D converter in many cases is the most expensive component in a data acquisition system, multiplexing analog inputs to the A/D is an economical approach. Usually the analog multiplexer operates into a sample-hold circuit which holds the required analog voltage long enough for A/D conversion.

As shown in **Fig 1**, an analog multiplexer consists of an array of parallel electronic switches connected to a common output line. Only one switch is turned on at a time. Popular switch configurations include 4, 8, and 16 channels which are connected in single (single-ended) or dual (differential) configurations.

The multiplexer also contains a decoder-driver circuit which decodes a binary input word and turns on the appropriate switch. This circuit interfaces with standard TTL inputs and drives the multiplexer switches with the proper control voltages. For the 8-channel analog multiplexer shown, a one-of-eight decoder circuit is used.

Most analog multiplexers today employ the CMOS switch circuit shown in **Fig 2**. A CMOS driver controls the gates of parallel-connected P-channel and N-channel MOSFET's. Both switches turn on together with the parallel connection giving relatively uniform on-resistance over the required analog input voltage range. The resulting on-resistance may vary from about 50 ohms to 2K ohms depending on the multiplexer; this resistance increases with temperature.



A_1	A_2	A_3	EN.	ON-CHAN
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Fig 1 Analog multiplexer circuit.

Because of the series resistance, it is common practice to operate an analog multiplexer into a very high load resistance such as the input of a unity gain buffer amplifier shown in the diagram. The load impedance must be large compared with the switch-on resistance and any series source resistance in order to maintain high transfer accuracy. *Transfer error* is the input to output error of the multiplexer with the source and load connected; error is expressed as a percent of input voltage.

Transfer errors of 0.1% to 0.01% or less are required in most data acquisition systems. This is readily achieved by using operational amplifier buffers with typical input impedances from 10^8 to 10^{12} ohms. Many sample-hold circuits also have very high input impedances.

Another important characteristic of analog multiplexers is *break-before-make* switching. There is a small time delay between disconnection from the previous channel and connection to the next channel which assures that two adjacent input channels are never instantaneously connected together.

Settling time is another important specification for analog multiplexers; it is the same definition previously given for amplifiers except that it is measured from the time the channel is switched on. *Throughput rate* is

the highest rate at which a multiplexer can switch from channel to channel with the output settling to its specified accuracy. *Crosstalk* is the ratio of output voltage to input voltage with all channels connected in parallel and off; it is generally expressed as an input to output attenuation ratio in dB.

As shown in the representative equivalent circuit of **Fig 3**, analog multiplexer switches have a number of leakage currents and capacitances associated with their operation. These parameters are specified on data sheets and must be considered in the operation of the devices. Leakage currents, generally in picoamperes at room temperature, become troublesome only at high temperatures. Capacitances affect crosstalk and settling time of the multiplexer.

Analog multiplexers are employed in two basic types of operation: low-level and high-level. In *high-level multiplexing*, the most popular type, the analog signal is amplified to the 1 to 10V range ahead of the multiplexer. This has the advantage of reducing the effects of noise on the signal during the remaining analog processing. In *low-level multiplexing* the signal is amplified after multiplexing; therefore great care must be exercised in handling the low-level signal up to the multiplexer. Low-level multiplexers generally use two-wire differential switches in order to minimize noise pick-up. Redd relays, because of essentially zero series resistance and absence of switching spikes, are frequently employed in low-level multiplexing systems. They are also useful for high common-mode voltages.

A useful specialized analog mutliplexer is the *flying-capacitor* type. This circuit, shown as a single channel in **Fig 4**, has differential inputs and is particularly useful with high common-mode voltages. The capacitor connects first to the differential analog input, charging up to the input voltage, and is then switched to the differential output which goes to a high input impedance instrumentation amplifier. The differential signal is therefore transferred to the amplifier input without the common mode voltage and is then further processed up to A/D conversion.

In order to realize large numbers of multiplexed channels, you can connect analog multiplexers in parallel using the enable input to control each device. This is called *single-level multiplexing*. You can also connect the out-

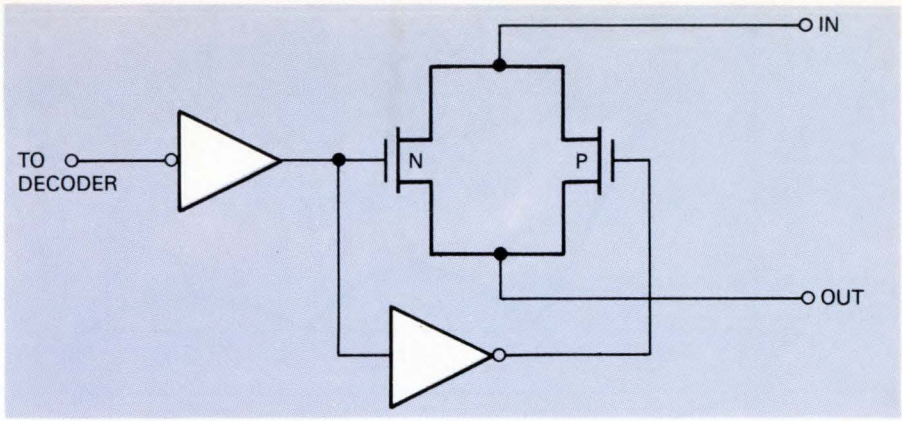


Fig 2 CMOS Analog switch circuit.

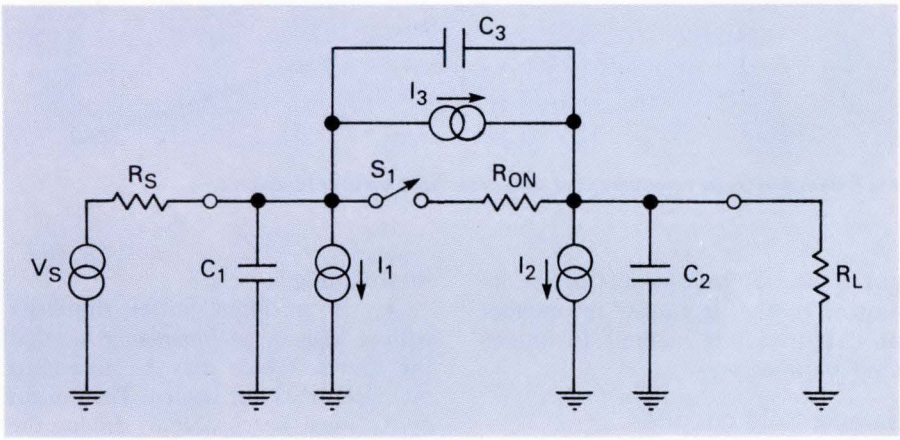


Fig 3 Equivalent circuit of analog multiplexer switch.

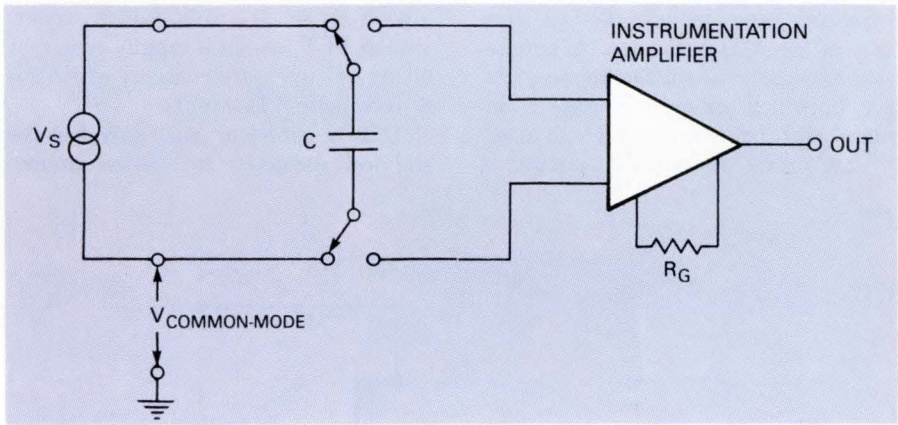


Fig 4 Flying capacitor multiplexer switch.

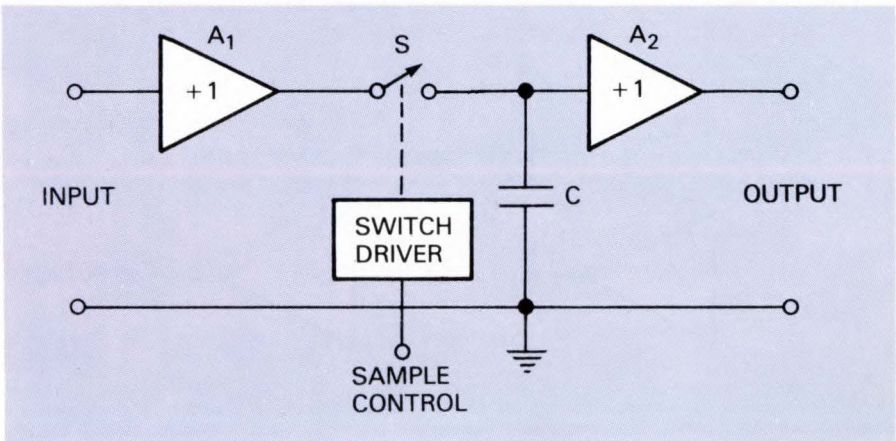


Fig 5 Popular sample-hold circuit.

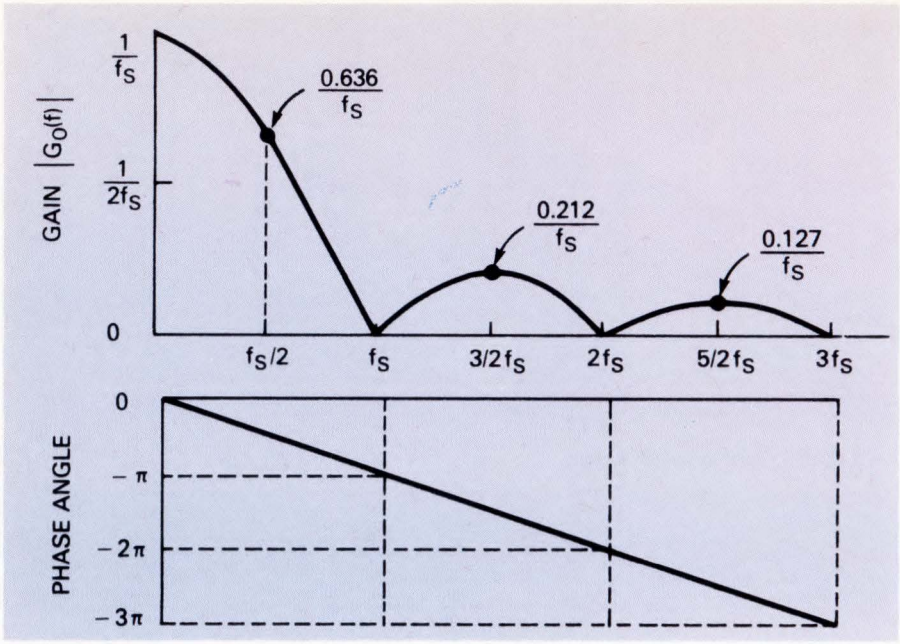


Fig 6 Gain and phase components of zero-order hold transfer function.

put of several multiplexers to the inputs of another to expand the number of channels; this method is *double-level multiplexing.*

Sample-hold circuits

Sample-hold circuits, discussed earlier, are the devices which store analog information and reduce the aperture time of an A/D converter. A sample-hold is simply a voltage-memory device in which an input voltage is acquired and then stored on a high quality capacitor. A popular circuit is shown in **Fig 5**.

A_1 is an input buffer simplifier with a high input impedance so that the source, which may be an analog multiplexer, is not loaded. The output of A_1 must be capable of driving the hold capacitor with stability and enough drive current to charge it rapidly. S_1 is an electronic switch, generally an FET, which is rapidly switched on or off by a drive circuit which interfaces with TTL inputs.

C is a capacitor with low leakage and low dielectric absorption characteristics; it is a polystyrene, polycarbonate, polypropylene, or teflon type. In the case of hybrid sample-holds, the MOS type capacitor is frequently used.

A_2 is the output amplifier which buffers the voltage on the hold capacitor. It must therefore have extremely low input bias current, and for this reason a FET input amplifier is required.

There are two modes of operation for a sample-hold: *sample* (or tracking) *mode,* when the switch is closed; and *hold mode,* when the switch is open. Sample-holds are usually operated in one of two basic ways. The device can continuously track the input signal and be switched into the hold mode only at certain specified times, spending most of the time in tracking modes. This is the case for a sample-hold employed as a deglitcher at the output of a D/A converter, for example.

Alternatively, the device can stay in the hold mode most of the time and go to the sample mode just to acquire a new input signal level. This is the case for a sample-hold used in a data acquisition system following the multiplexer.

A common application for sample-hold circuits is *data recovery,* or *signal reconstruction, filters.* The problem is to reconstruct a train of analog samples into the original signal; when used as a recovery filter, the sample-hold is known as a *zero-order hold.* It is a useful filter because it fills in the space between samples, providing data smoothing.

As with other filter circuits, the gain and phase components of the transfer function are of interest. By an analysis based on the impulse response of a sample-hold and use of the Laplace transform, the transfer function is found to be: $G_0(f) = f_s^{-1}\,[\sin\pi(f/f_s)/(\pi f/f_s)]\; e^{-j\pi(f/f_s)}$, where f_s is the sampling frequency. This function contains the familiar (sin x)/x term plus a phase term, both of which are plotted in **Fig 6**.

The sample-hold is therefore a low pass filter with a cut-off frequency slightly less than $f_s/2$ and a linear phase response which results in a constant delay time of T/2, where T is the time between samples. Notice that the gain function also has significant response lobes beyond f_s. For this reason a sample-hold reconstruction filter is frequently followed by another conventional low-pass filter.

In addition to the basic circuit of **Fig 5**, there are several other sample-

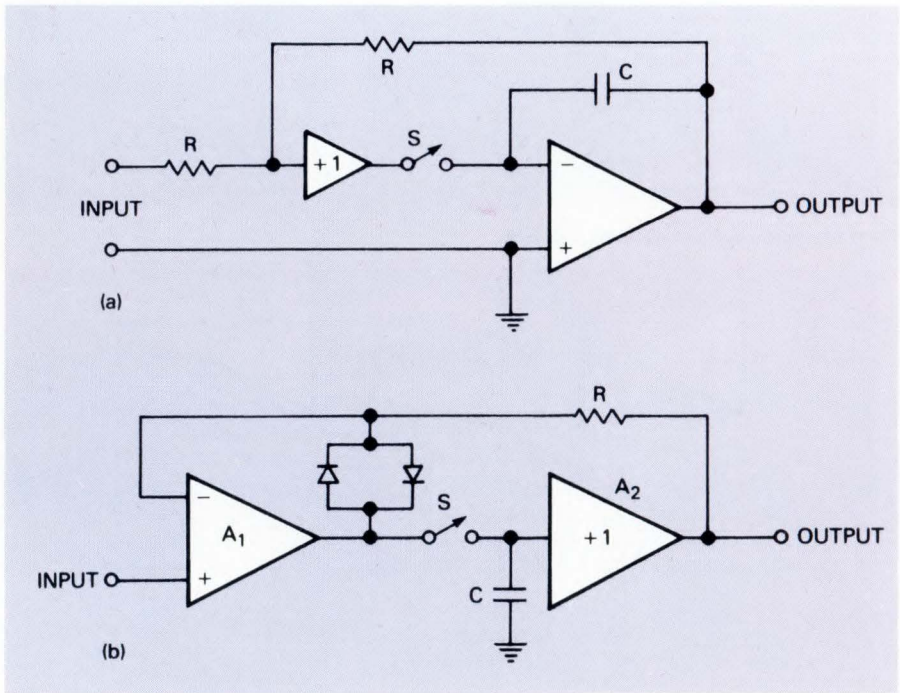


Fig 7 Two closed loop sample-hold circuits.

hold circuit configurations which are frequently used. **Fig 7** shows two such circuits which are closed loop circuits as contrasted with the open loop circuit of **Fig 5**. **Fig 7 (a)** uses an operational integrator and another amplifier to make a fast, accurate inverting sample-hold. A buffer amplifier is sometimes added in front of this circuit to give high input impedance. **Fig 7 (b)** shows a high input impedance noninverting sample-hold circuit.

The circuit in **Fig 5**, although generally not as accurate as those in **Fig 7**, can be used with a diode-bridge switch to realize ultrafast acquisition sample-holds.

A number of parameters are important in characterizing sample-hold performance. Probably most important of these is *acquisition time*. The definition is similar to that of settling time for an amplifier. It is the time required, after the sample-command is given, for the hold capacitor to charge to a full-scale voltage change and remain within a specified error band around final value.

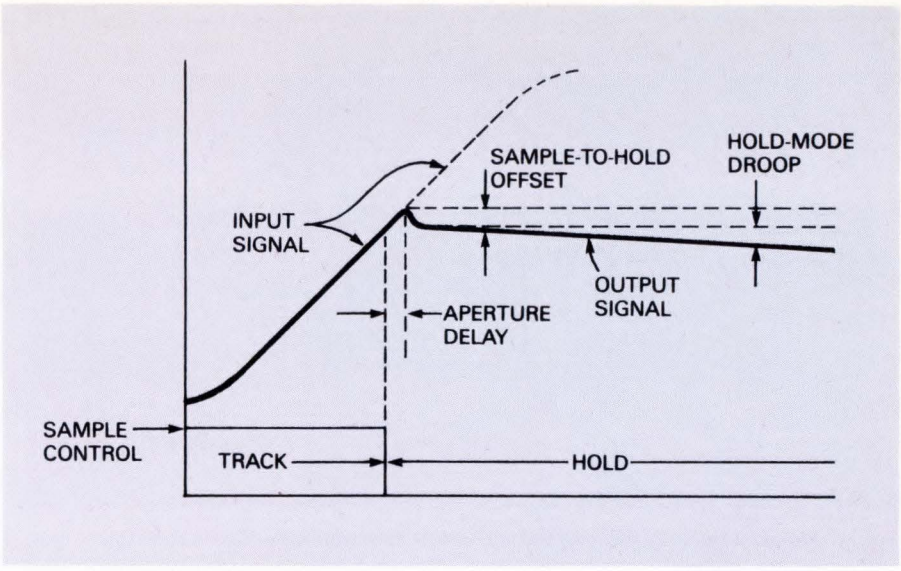


Fig 8 Some sample-hold characteristics.

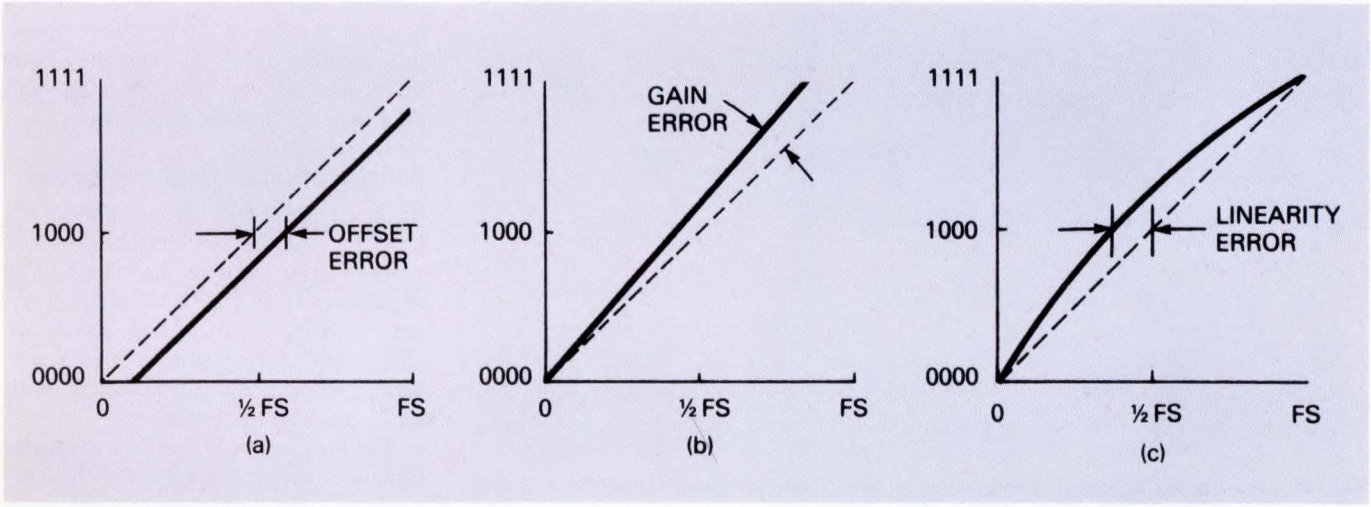


Fig 9 Offset (a), gain (b), and linearity (c) errors for an aid converter.

Several hold-mode specifications are also important. *Hold-mode droop* is the output voltage change per unit time when the sample switch is open. This droop is caused by the leakage currents of the capacitor and switch, and the output amplifier bias current. *Hold-mode feedthrough* is the percentage of input signal transferred to the output when the sample switch is open. It is measured with a sinusoidal input signal and caused by capacitive coupling.

The most critical phase of sample-hold operation is the transition from the sample mode to the hold mode. Several important parameters charac-

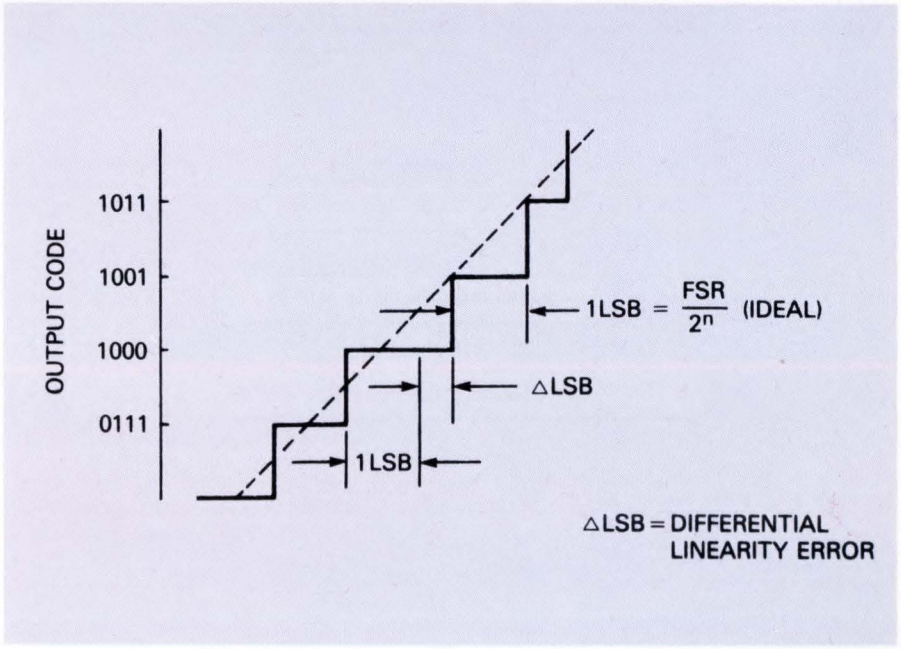


Fig 10 Defining differential linearity error.

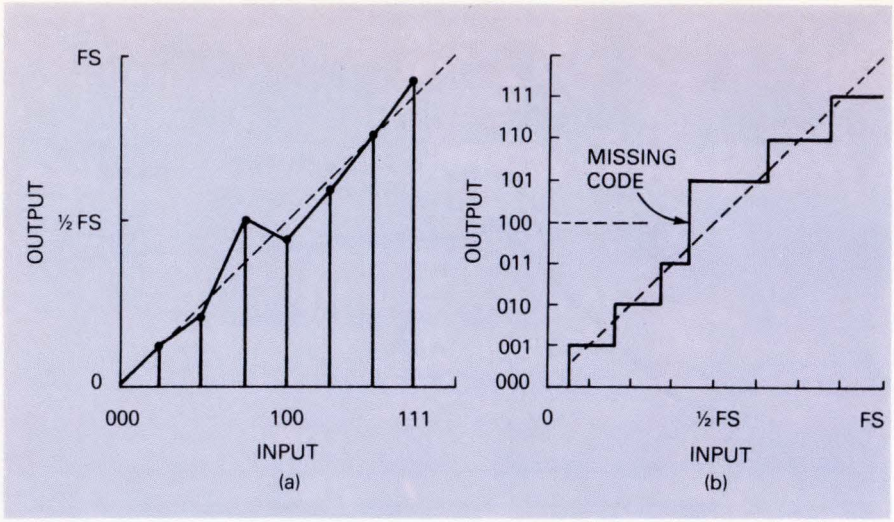


Fig 11 Nonmonotonic D/A converter (a) and A/D converter with missing code (b).

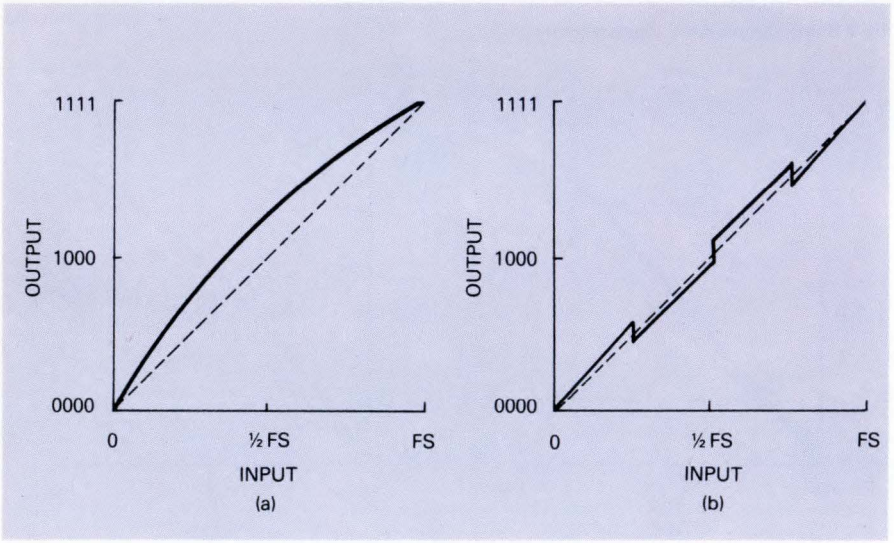


Fig 12 Linearity characteristics of integrating (a) and successive approximation (b) A/D converters.

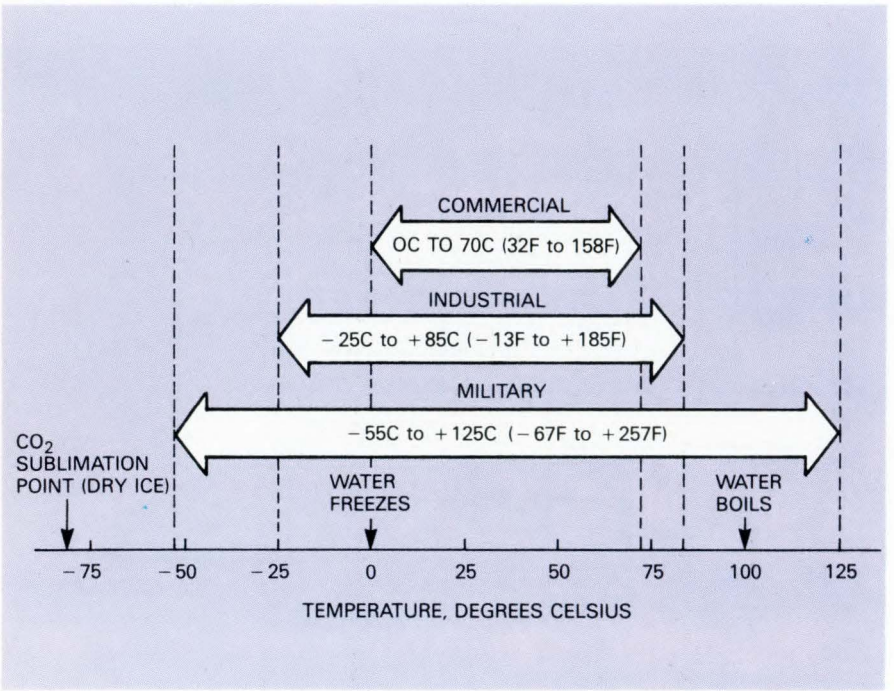


Fig 13 Standard operating temperature ranges for data converters.

terize this transition. *Sample-to-hold offset* (or step) *error* is the change in output voltage from the sample mode to the hold mode, with a constant input voltage. It is caused by the switch transferring charge onto the hold capacitor as it turns off.

Aperture delay is the time elapsed from the hold command to when the switch actually opens; it is generally much less than a micro-second. *Aperture uncertainty* (or *aperture jitter*) is the time variation, from sample to sample, of the aperture delay. It is the limit on how precise is the point in time of opening the switch. Aperture uncertainty is the time used to determine the aperture error due to rate of change of the input signal. Several of the above specifications are illustrated in the diagram of **Fig 9**.

Sample-hold circuits are simple in concept, but generally difficult to fully understand and apply. Their operation is full of subtleties, and they must therefore be carefully selected and then tested in a given application.

Specification of data converters

Real A/D and D/A converters do not have the ideal transfer functions discussed earlier. There are three basic departures from the ideal: offset, gain, and linearity errors. These errors are all present at the same time in a converter; in addition they change with both time and temperature.

Fig 8 shows A/D converter transfer functions which illustrate the three error types. **Fig 9 (a)** shows *offset error,* the analog error by which the transfer function fails to pass through zero. Next, in **Fig 9 (b)** is *gain error,* also called *scale factor error;* it is the difference in slope between the actual transfer function and the ideal, expressed as a percent of analog magnitude.

In **Fig 9 (c)** *linearity error,* or nonlinearity, is shown; this is defined as the maximum deviation of the actual transfer function from the ideal straight line at any point along the function. It is expressed as a percent of full scale or in LSB size, such as ±1/2 LSB, and assumes that offset and gain errors have been adjusted to zero.

Most A/D and D/A converters available today have provision for external trimming of offset and gain errors. By careful adjustment these two errors can be reduced to zero, at least at ambient temperature. Linearity error, on the other hand, is the remaining error that cannot be adjusted out and is an inherent characteristic of the con-

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The SOROC IQ 120 is the result of an industry-wide demand for a capable remote video display terminal which provides a multiple of features at a low affordable price. The IQ 120 terminal is a simple self-contained, operator / computer unit.

The IQ 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IQ 120 terminal incorporates a 12-inch, CRT formatted to display 24 lines with 80 characters per line.

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verter.

Basically there are only two ways to reduce linearity error in a given application. First, a better-quality, higher-cost converter with smaller linearity error can be procured. Second, a computer or microprocessor can be programmed to perform error correction on the converter. Both alternatives may be expensive in terms of hardware or software cost.

The linearity error discussed above is actually more precisely termed *integral linearity error.* Another important type of linearity error is known as *differential linearity error.* This is defined as the maximum amount of deviation of any quantum (or LSB change) in the entire transfer function from its ideal size of $FSR/2^n$. **Fig 11** shows that the actual quantum size may be larger or smaller than the ideal; for example, a converter with a maximum differential linearity error of ±1/2 LSB can have a quantum size between 1/2 LSB and 1-1/2 LSB anywhere in its transfer function. In other words, any given analog step size is 1 (±1/2) LSB. Integral and differential linearities can be thought of as macro- and micro-linearities, respectively.

Two other important data converter characteristics are closely related to the differential linearity specification. The first is *monotonicity,* which applies to D/A converters. Monotonicity is the characteristics whereby the output of a circuit is a continuously increasing function of the input. **Fig 12 (a)** shows a *nonmonotonic* D/A converter output where at one point, the output decreases as the input increases. A D/A converter may go nonmonotonic if its differential linearity error exceeds 1 LSB; if it is always less than 1 LSB, it assures that the device will be monotonic.

The term *missing code,* or *skipped code,* applies to D/A converters. If the differential linearity error of an A/D converter exceeds 1 LSB, its output can miss a code as shown in **Fig 11 (b).** On the other hand, if the differential linearity error is always less than 1 LSB, this assures that the converter will not miss any codes. Missing codes are the result of the A/D converter's internal D/A converter becoming nonmonotonic.

For A/D converters the character of the linearity error depends on the technique of conversion. **Fig 12 (a),** for example, shows the linearity characteristic of an integrating type A/D converter. The transfer function exhibits a smooth curvature between zero and full scale. The predominant type of error is integral linearity error, while differential linearity error is virtually nonexistent.

Fig 12 (b), on the other hand, shows the linearity characteristic of a successive approximation A/D converter; in this case differential linearity error is the predominant type, and the largest errors occur at the specific transitions at 1/2, 1/4, and 3/4 scale. This result is caused by the internal D/A converter nonlinearity; the weight of the MSB and bit 2 current sources is critical in relation to all the other weighted current sources in order to achieve ±1/2 LSB maximum differential linearity error.

Part 5, our next installment, concludes this series on data acquisition and conversion.

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Technology Trends

Continued from p. 22

Disk Controller Increases Multibus μC System Storage Tenfold

The iSBC 206 disk controller brings an order-of-magnitude increase in storage capability to Multibus microcomputer systems. It allows Multibus-compatible systems to implement very large storage capacities, accessing up to 40 Mbytes of disk storage.

The iSBC 206 is compatible with 8- or 16-bit SBCs, is fully software-supported by Intel, has on-board diagnostic routines, is compatible with industry standard disk drives, has on-board buffers and operates from single 5V supply.

Protects original software

The iSBC 206 controller accommodates 8- or 16-bit data transfers and handles 16- or 20-bit address-bus structures. The iSBC 206 controller can also be used with 8-bit μP-based computer systems using 8080A or 8085A CPUs and compatible with Multibus architecture.

The iSBC 206 controller is also fully supported by Intel's RMX/80 Real Time Multitasking Executive. Software developed for RMX/80-based systems using diskette storage can be upgraded to hard disk usage by configuring the iSBC 206 controller driver (in place of iSBC 201, 202 or 204 controllers) into the RMX/80 system. The OEM/VEU users of the iSBC 206 can quickly reconfigure their software on the Intellec system for transfer to their SBC system to meet changing product or applications requirements while still protecting their original software development investment. An RMX/80 driver is available for the iSBC 206 controller user at introduction time and is available to all current and future users of RMX/80 at no cost.

Overcoming one of the major problems of rotating memory systems – fault location – Intel supplies the iSBC 206 controller with its own diagnostic routines in on-board ROM memory.

Supports standard drives

OEM designers using presently available diskette drives ("floppies") will immediately realize an order of magnitude increase in storage capacity over double-sided, double-density diskette systems (10 Mbytes vs 1 Mbyte/drive), while significantly upgrading the performance levels and storage-medium life of their systems.

Developed for the more sophisticated OEM user, the iSBC 206 controller will support from one to four OEM standard disk drives including: Diablo 44B, Pertec D3422, Wangco (Perkin-Elmer) ST2222, Caelus 306 R, CDC 9427 "Hawk" and other drives.

The iSBC 206 controller, supplied as a two-board set, operates from a single 5V supply, drawing 5.5A to 6.5A, and board size conforms to Multibus standard layout dimensions of 6.75″ x 12″. $2500.

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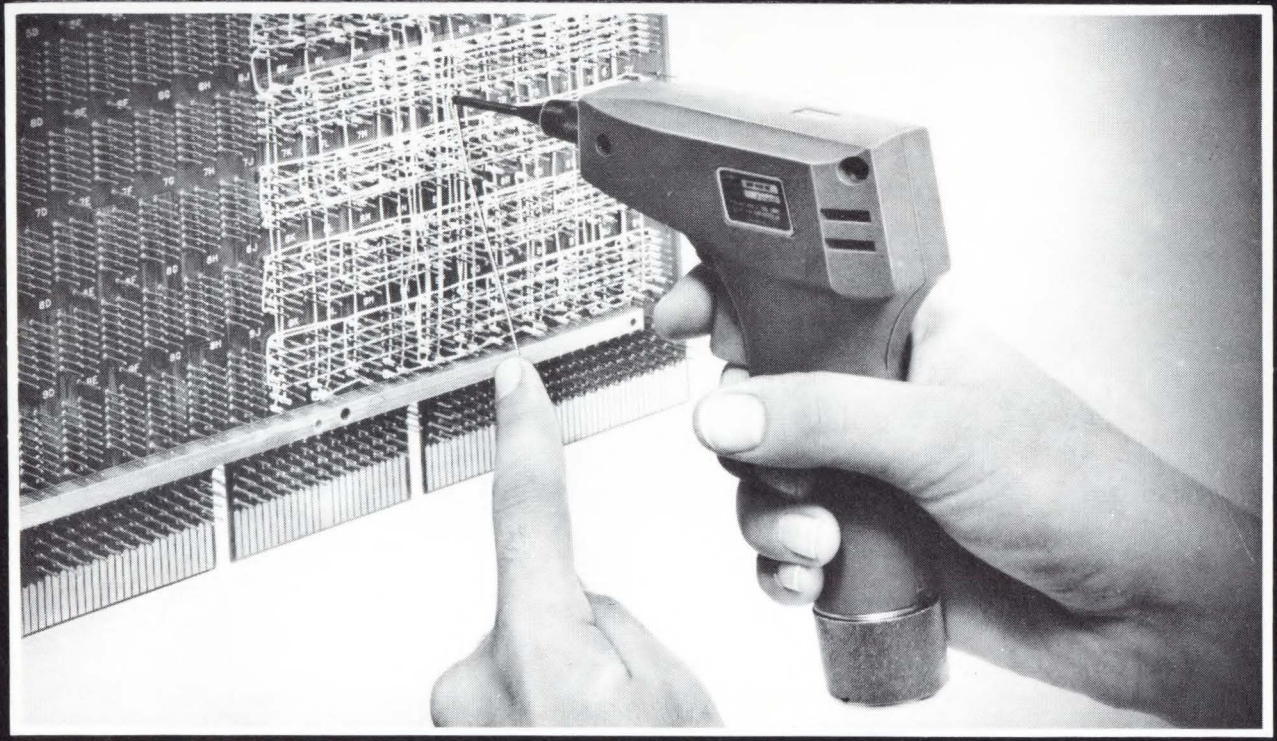

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Designers' Notebook

Programmable Counter

A push-button programmable low frequency counter with a digital LED readout can come to the rescue of a consultant or designer who needs to produce such a device with little advanced notice. The heart of the counter is an under-$10 calculator purchasable almost anywhere. This makes the device excellent for on-the-spot turn around. Since the calculator contains the LED readouts and push-buttons already encased, most of the project construction is complete at the time the calculator is purchased.

To turn the calculator into a programmable counter, simply solder wires across the 'equals' key terminals and connect the other end of the wires to an external switch. Almost any external switching mechanism may be used, from straight mechanical to optical to magnetic, since switch debounce is inherent in the calculator chip. Interchangeability of switching transducers is easily accomplished by attaching a microphone plug to the calculator case. Switchcraft part #'s TR2A and 880 are ideally suited to this purpose.

Programming the counter is straightforward. To count up by integers follow these programming steps:

1. Press the 'minus' key
2. Press the digit '1' key
3. Press the 'plus' key
4. Press the digit '1' key
5. Press the 'equals' key

This brings the display to zero and sets the counter to increment by one each time the transducer is activated.

The system may also be similarly programmed to count down from any designated number. Decoding circuits attached to the LED display will provide alarm indication when the appropriate count is reached.

To program the count down sequence proceed as follows: (1) load in the starting number plus one, (2) press the 'minus' key, (3) press the digit '1' key and (4) press the 'equal' key.

A unique feature of the counter is its totally programmable count value. For example, when used in production line applications, a floor manager may obtain a continuous display of the number of items passing a checkpoint either by counting the number of boxes or by programming the counter to count the total number of items per box. A box containing 48 items would use the following program: (1) press the 'minus' key, (2) press the digits '48' keys, (3) press the 'plus' key, (4) press the digits '48' keys and (5) press the 'equals' key.

Richard L. White, Computer Business Systems, Inc., 167 Morre Rd., E. Weymouth, CA 02189

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8080 Routine Displays Console Messages

This technique is especially useful when writing short (''quick and dirty'') test routines for a microprocessor development system, as opposed to larger structured programs for a computer system. Although it may not be ''structured'', it saves a lot of programming time and flow of a program, and to be displayed on the operator's console with an absolute minimum of overhead.

The example shown is written in Intel standard 8080 mnemonics. It uses two subroutines: MSGXP as shown, and CO which is the console output routine supplied with the development system hardware.

```
        .
        PUSH   H          ; SAVE INDEX (OPTIONAL)
ERRMS   CALL   MSGXP      ; DISPLAY ERROR MESSAGE
        DB     'READ ERROR'
        DB     0
        POP    H          ; RESTORE INDEX (OPTIONAL)
        .
        .
MSGXP   POP    H          ; 'RETURN ADRS' TO INDEX
MSGX1   MOV    A,M        ; GET MESSAGE CHARACTER
        CPI    00         ; TEST FOR END OF MESSAGE
        JZ     MSGEX      ; EXIT IF END
        CALL   CO         ; CHARACTER TO CONSOLE
                          OUTPUT
        INX    H          ; POINT TO NEXT CHARACTER
        JMP    MSGXI      ; CONTINUE MESSAGE
MSGEX   INX    H          ; POINT TO REAL RETURN ADRS
        PCHL              ; RETURN THROUGH INDEX
```

MSGXP will output a message embedded in the middle of a program and return to the calling program at the instruction immediately following the message test. The programmer does not have to keep track of the length of his messages, nor provide a separate message buffer for them. He simply places the test immediately following the CALL MSGXP instruction. The subroutine will then output the text beginning with the first memory location following the CALL, and continuing until the first zero location, created by the DB 0 instruction, signaling end of message text.

The subroutine then increments the index (a MSGEX) to point to the next location in the calling program, and returns to that location by the Program Counter from index instruction, PCHL. This allows messages to be displayed with a minimum of overhead.

Ken Barbier, Borrego Engineering, Box 1253, Borrego Springs, CA 92004.

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BCD Divide-by-N Counter With Symmetrical Output

Divide-by-N counters usually provide asymmetrical output for odd divisors. Although various circuits are suggested to obtain symmetrical output for all divisors, they are either not programmable or do not accept direct BCD programming inputs. The circuit suggested here has all the advantages of programming with BCD inputs, and provides symmetrical square-wave outputs for all divisors.

The circuit shown in **Fig 1** consists of frequency doublers, programmable divide-by-n counter and flipflop for divide-by-2 operation. The frequency doubler is used to obtain narrow pulses at both the leading and trailing edges of the input waveform. Thus the input frequency is doubled. The programmable divide-by-n counter consists of decade counters (7490s) and 4-bit magnitude comparators (7485s). The counter outputs and the BCD number corresponding to any divisor n are applied to "A" and "B" inputs of the magnitude comparators.

These two inputs are continuously compared as the counter advances. The comparator gives "1" level at its "A = B" output when counter reaches a value equal to the set value n. This "1" level resets the counter to zero. As soon as the counter is reset to zero, the "A = B" output assumes "0" level. Thus a narrow pulse is generated at the "A = B" output for every n counts, resulting in a pulse train of frequency 2f/n. This is further divided in a flip-flop to obtain a square-wave output of frequency f/n.

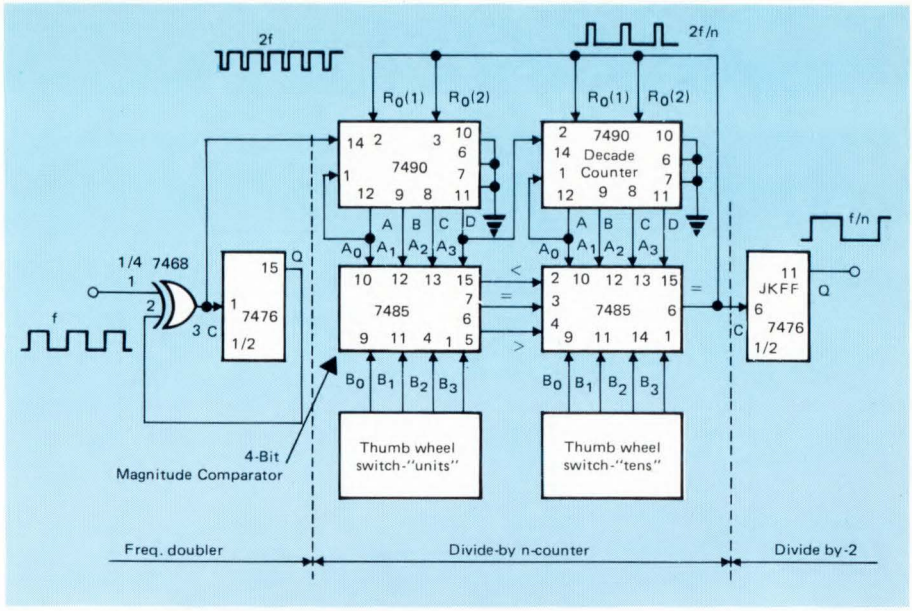

Fig 1 Providing symmetrical square-wave outputs, this divide-by-n accepts direct BCD programming inputs.

M.V. Subba Rao and V.L. Patil, Central Electronics Engineering Research Institute, Pilani (Rajasthan), India 333031.

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Monolithic Fiber Optic Drivers/Receivers Use Existing ICs

Suitable interface circuits until recently were a serious limitation to many fiber optic designs, and , often, severe constraints imposed on these circuits by rather subtle electro-optical considerations weren't immediately obvious to the uninitiated fiber optics designer.

Some manufacturers solved the problem in high performance systems by combining transmitter and receiver circuitry into small compact hybrid modules for use with one type of cable and connector. But functionality in this modular approach came at the expense of flexibility. However, more design flexibility comes from using existing linear and digital ICs to implement the transmitter and receiver functions at the expense of size and/or performance.

The ideal solution would be monolithic fiber optic line drivers and receivers compatible at the optical signal ports with a variety of optical transducers (ie LEDs, APDs, etc.), and electrically compatible with standard analog interfaces or digital logic families. For this application requirement, we used the Spectronics SPX 3619 and SPX 3620.

Before we describe our application, a word about the circuits. The transmitter circuit is a high-speed current driver and can be used as a pre-driver or combined with an LED or laser diode can constitute a complete functional transmitter; the companion circuit transforms low-level photocurrent signals from a PIN or avalanche photodiode into a logic level output. Both networks feature 20Mb/s bi-phases data rate capability, TTL compatible interfaces, and single 5V supply operation. Devices are available in leadless chip carriers or 14-pin ceramic dual inline packages.

The SPX 3619 Transmitter is a direct-coupled, switched, regulated current sink. Its intended purpose is intensity modulation of solid-state sources — either spontaneous LEDs or injection lasers. By selectively connecting "programming" terminals, the output current can be set at any multiple of 25mA up through 150mA. Alternately, an external current-limiting resistor can be employed. Output stage design is such that a speed-up (peaking) network can be used if required. There are two gate inputs, one of which can be used for enable/inhibit mode control. Each represents one standard unit load to a signal source. Propagation and transition times are typically 7 nsec and 5 nsec, respectively. **Fig 1** shows a typical transmitter connection scheme we used to achieve the full 150mA peak current output. No restrictions on the optical source is imposed by the transmitter circuit other than sufficiently short rise and fall times to realize the 20MB/s data rate. Although transmitter output current is almost independent of the signal shape supplied at its input, input rise or fall times greater than 100 nsec are not recommended. Output current temperature coefficient is essentially zero over an operating range of 0°C to 70°C utilizing

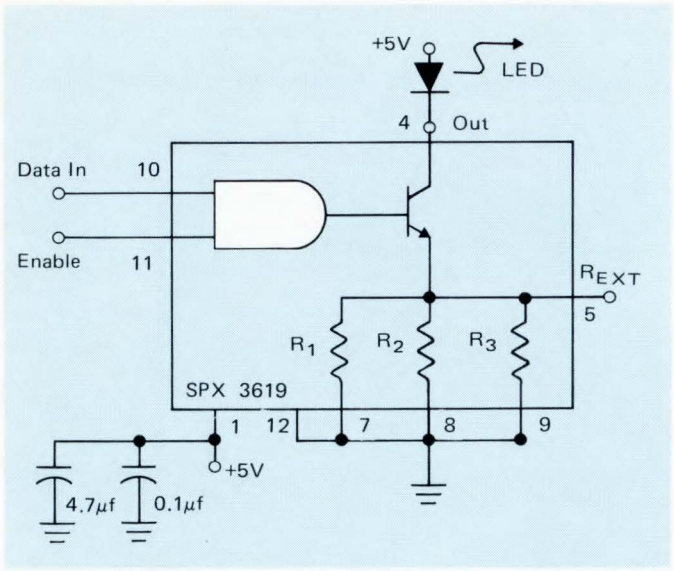

Fig 1 This SPX 3619 Transmitter Connection circuit achieved 150 mA peak current output.

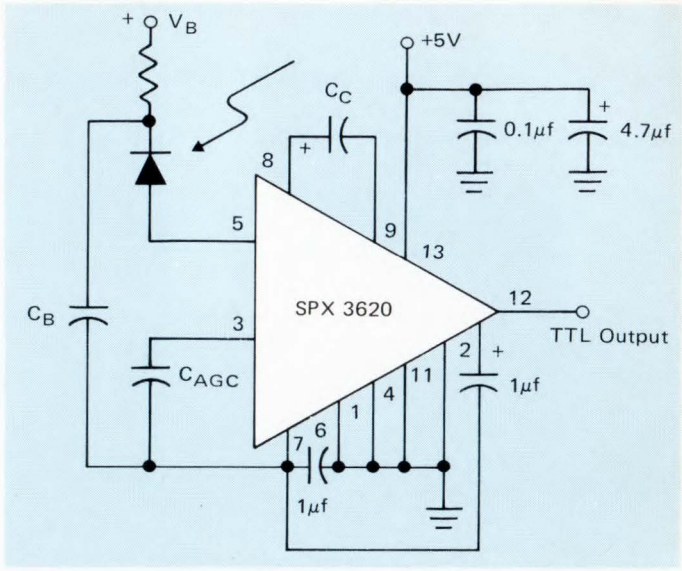

Fig 2 This Receiver circuit operates from 10 Kb/s to 10 Mb/s data rates. Output can interface to any suitable TTL circuitry.

the internal current limiting resistors and approximately 0.12%/°C using external current limiting.

In one application, the SPX 3620 Receiver circuit was used in conjunction with a PIN or avalanche photodiode. It comprises a transimpedance preamplifier with AGC followed by a post-amplifier, comparator and buffer. Signal coupling from the preamp to the postamp was via an external capacitor. A second external capacitor was required for AGC filtering. Being able to choose appropriate values for these two components, other systems integrators and desigers are afforded the flexibility to apply this device in a variety of situations. The circuit was designed for detection of Manchester-coded data in a point-to-point link. Sensitivity (for 10^{-8} bit error ratio) is 200nA at 10Mb/s. Dynamic range extends to 0.2mA. Maximum usuable data rate, depending on clock recovery requirements, is at least 10Mb/s over a temperature range of 0°C to 70°C. Fan-out to ten standard loads is permissible. **Fig 2** illustrates typical receiver connection providing operation from 10kb/s to 10Mb/s.

As with all high gain wideband ICs, adequate bypassing is imperative and care must be exercised to isolate output lines from input lines, and to carefully shield the input node from EMI pickup. **Fig 3** shows a typical high-performance fiber optic data link utilizing the SPX 3619/3620 ICs. The link will operate at data rates up to 10Mb/s (Manchester data) and distances to 2Km (1.24 mi) with the LEDs, detectors, cable and connectors shown with no external "tweaking" required over a temperature range of 0°C to 70°C. Other opto-components and/or cables may be substituted to achieve a lower cost design with a resulting lower maximum data rate, shorter transmission distance, or both.

One drawback to the 3620 receiver, we found, especially for low cost applications, is the requirement that data be bi-phased encoded. Several approaches have been suggested for implementing a "transparent" code transmitter/receiver pair, but to date, the only known available version of this is a hybrid modle. In the future high volume applications, a complete line of monolithic interface devices will be required, including serial high-speed communications adapters, and must be economically attractive if the fiber optic transmission medium is to survive in markets now served totally by wire and coaxial cable.

Bill Stephens and Tom Bunch, Spectronics Corp., (Honeywell), Richardson, TX.

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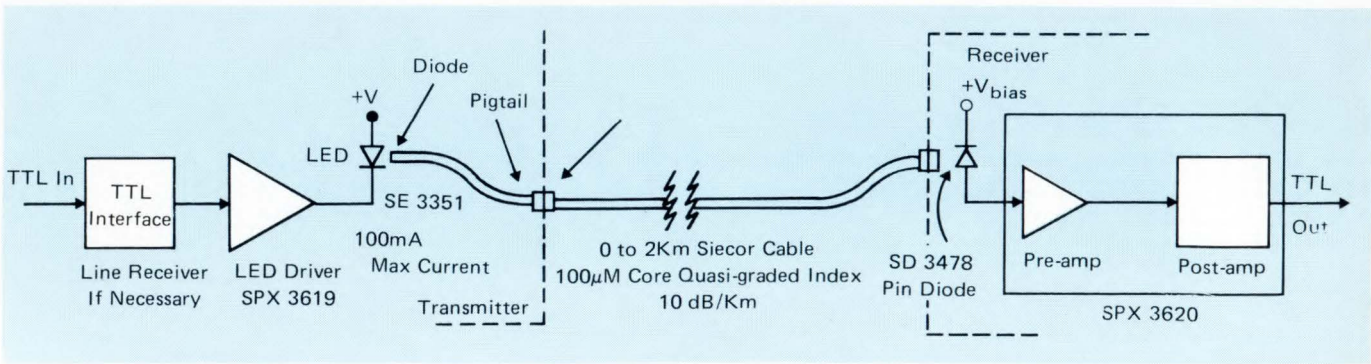

Fig 3 10 MBit/Sec Manchester 10^{-8} per Digital channel. This fiber optics link operates at up to 10 Mb/s data rate with a maximum fiber optic cable length of 2 km. The two connectors are SMA-type Amphenol 906 Series connectors.

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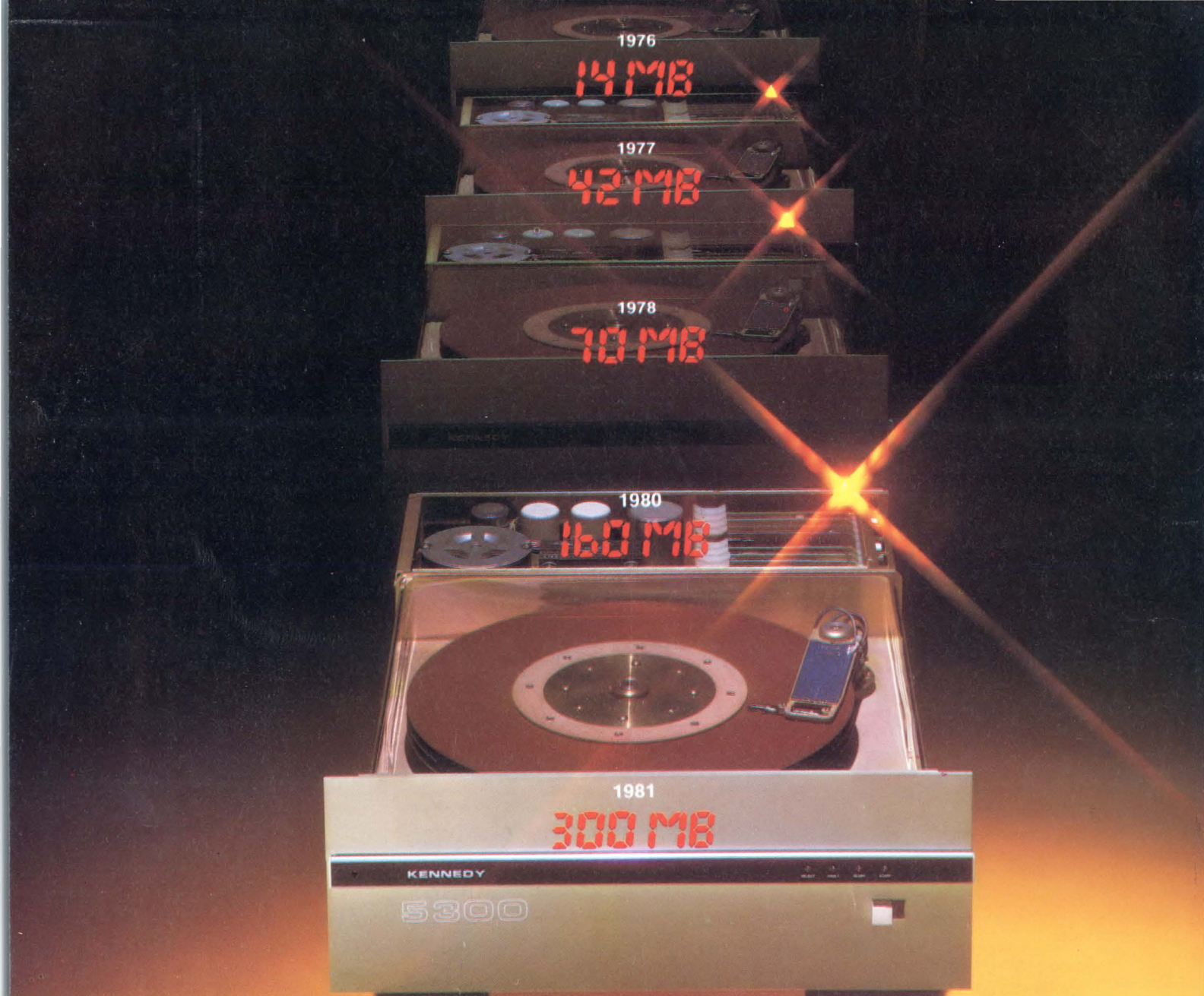

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