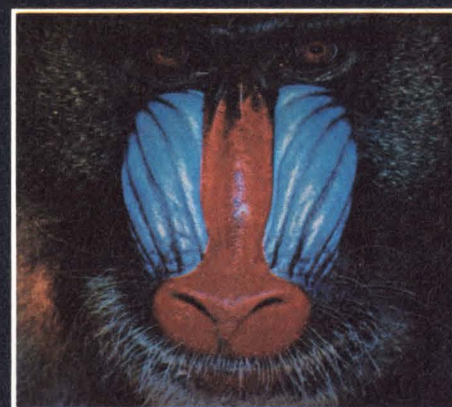
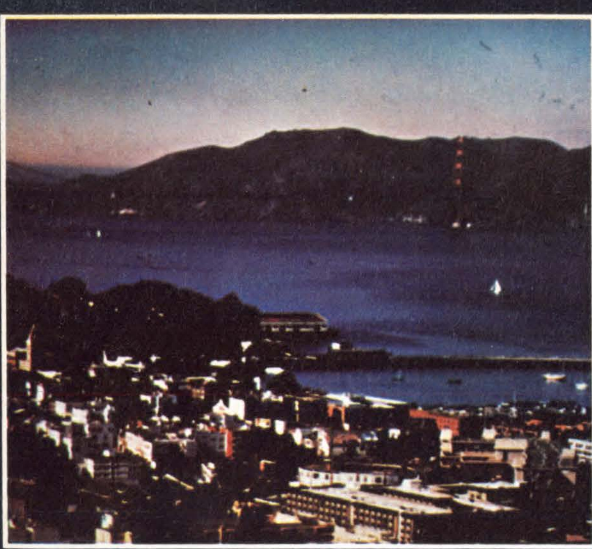
VOLUME 9, NO. 6 JUNE 1979

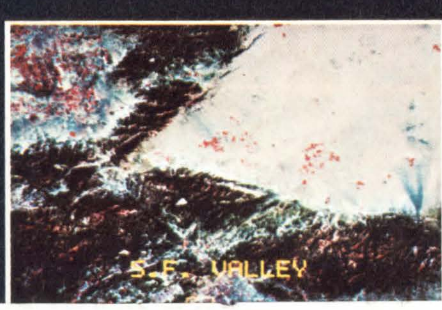
Digital Design

The Magazine of Systems Electronics



Quantitative Evaluation of Soft Copy Displays





Data Entry Peripherals

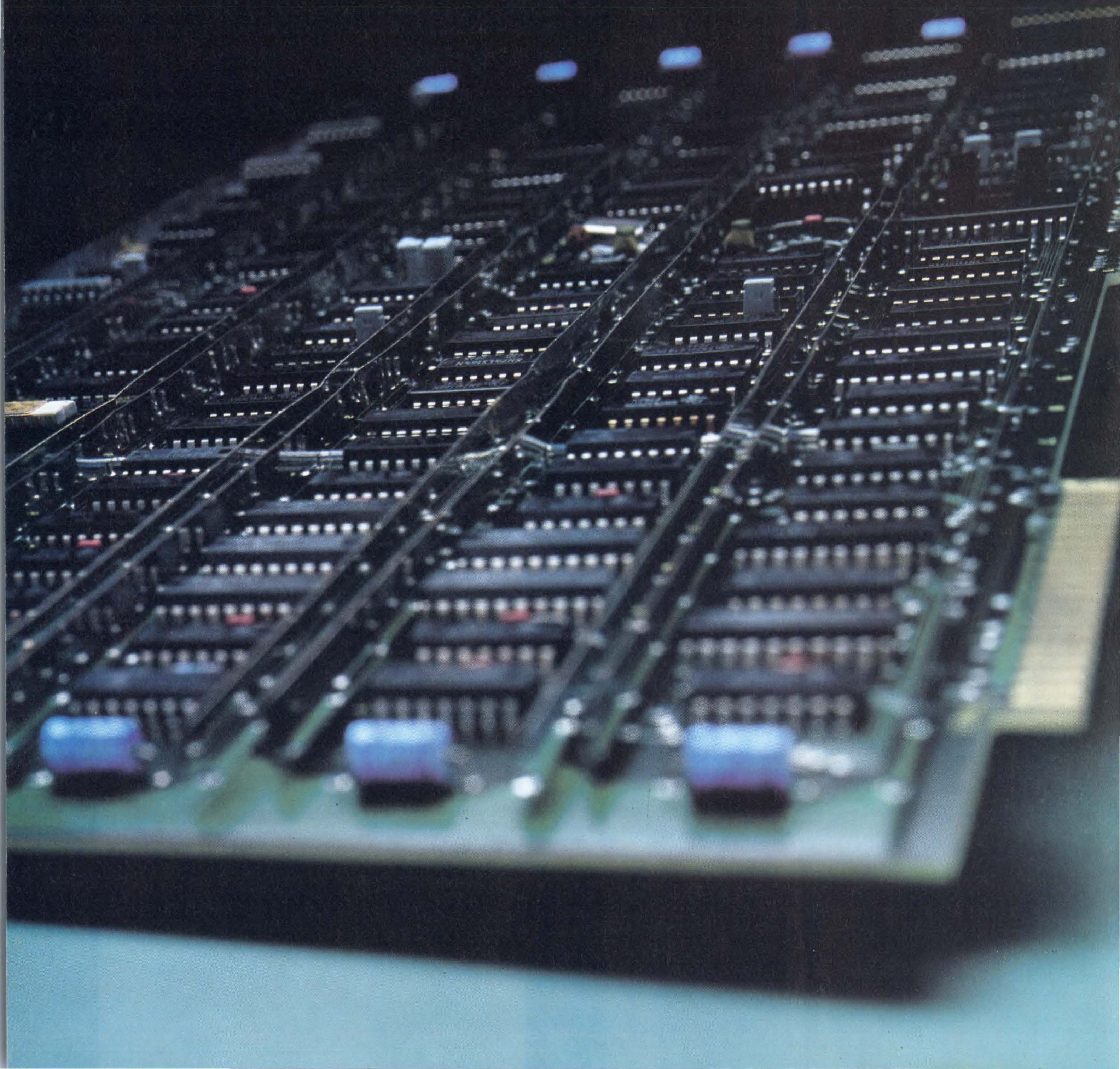
Logic Analyzer

Low-Cost Terminals

Minis in Small Businesses

The Inner Game of Intelligent Formatting

by Tandberg Data, Inc.



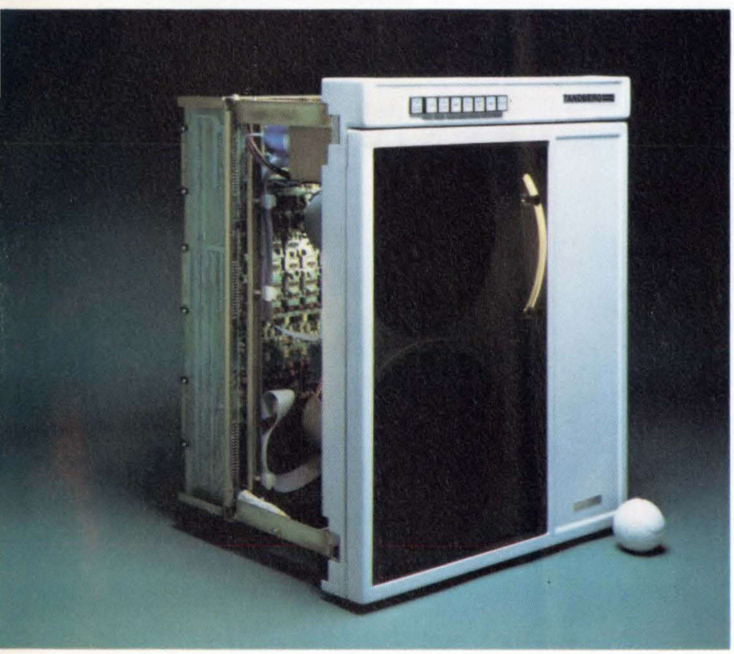
Get it together . . . and everything comes easier.

Put tape transport intelligence on the inside, and watch your game improve. It's possible with Tandberg Data's TDF 4050 (microprocessor-based) Formatter — now installed *internally* in the industry-proven, dual-format TDI 1050 Synchronous Tape Transport.

No more need for an external formatter to control the reading and writing of data. The interfacing task is naturally a whole lot simpler. And real savings follow with only one system to ship, handle, and mount, rather than two. Cost of ownership is resultantly the lowest currently obtainable.

The internal TDF 4050 Formatter reads and writes ANSI, IBM, and ECMA compatible tapes. It is designed to work with 9-track 1600 bpi PE and 800 bpi NRZI tape drives and 7-track 200/556/800 bpi NRZI tape drives.

Contained on one 19″ x 10″ PC board, the new Tandberg dual formatter can control from one to four tape transports — either the same or half speed or a mix of different formats with dual stack heads.



The TDF 4050 can handle six different tape drive speeds. It can read and write PE and NRZI at the specified speed or one-half that speed when drives of different speeds are connected.

The TDF 4050 executes all standard commands, as well as other customer-specified commands.

Tandberg's TDI 1050 dual-format Synchronous Tape Transport utilizes 10½-inch reels. With the TDF 4050 Formatter, users may easily daisy-chain up to four transports simultaneously, thus saving rack space and cost by freeing slots formerly occupied by an external formatter.

The TDF 4050 and the TDI 1050 are microprocessor-based systems. Using the test program designed into the TDI 1050 firmware and the optionally available test ROM set for the TDF 4050, the magnetic tape system can have initial set-up and be trouble-shot in the field without external test boxes, without tying up expensive computer time and without special tools.

Impeccable quality in engineering and fabrication has long been the hallmark of the Tandberg name worldwide. But Tandberg's globe-girdling facilities also mean immediate delivery and service responsiveness wherever needed, 24 hours a day, seven days a week, 365 days of the year.

WHAT CAN THE INNER GAME OF FORMATTING DO FOR MY GAME?

1. Simplify interfacing.
2. Reduce integration time.
3. Eliminate redesign.
4. Facilitate daisy-chaining.
5. Cut shipping and handling costs.
6. Cut rack space and costs.

OKAY. BUT DO I GET THE WHOLE RANGE OF COMMANDS?

Here's the whole slew — and let us know if you require any others.

- Read Forward
- Read Reverse
- Write Forward (Normal)
- Read Reverse Edit
- Write Forward Edit
- Write File Mark
- Erase Forward (Fixed Length)
- Erase Forward (Variable Length)
- Space Forward
- Space Reverse
- File Search Forward
- File Search Reverse
- File Search Forward (Ignore Data)
- File Search Reverse (Ignore Data)
- Load-On-Line
- Rewind
- Off-Line

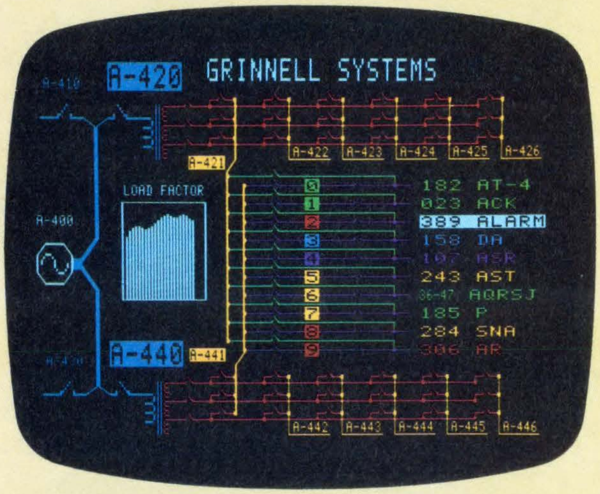
Now with Tandberg's new TDF 4050 *internal* Formatter you'll get your inner game together. And start finding the competition is a whole lot easier to handle.

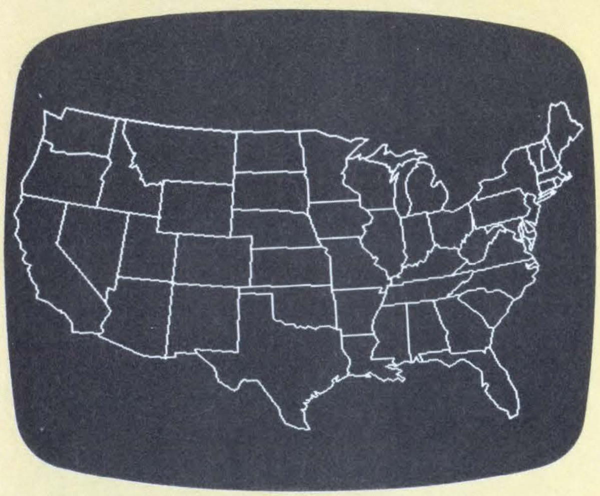
TANDBERG DATA INC.
4060 Morena Blvd.
San Diego, CA 92117
(714) 270-3990

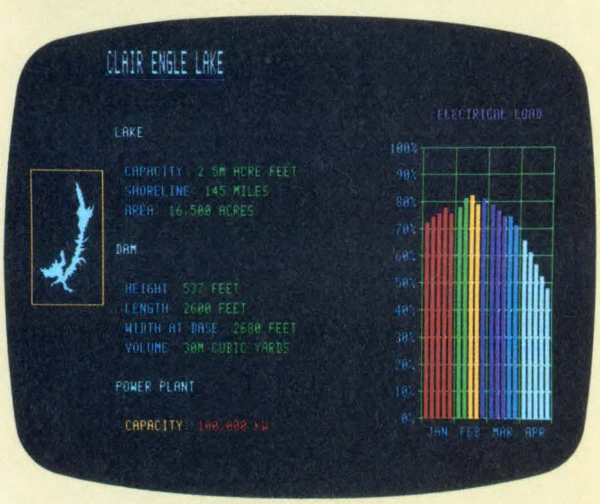
TANDBERG

Circle 23 on Reader Inquiry Card

Vector graphics. OEM prices.







Now, with Grinnell's GMR-37 graphic display systems, you can have the resolution and input advantages of dot matrix television for about the same price as more limited character-based systems.

And, every GMR-37 display is a complete operating system: display generator, MOS refresh memory, vector and rectilinear graphics, alphanumerics in 4 sizes, bi-directional RS-232 computer interface and RS-170 video interface. Systems, including power supplies, are housed in a 7", rack-mountable chassis and drive standard closed circuit monitors.

Four basic GMR-37 models can be tailored to fit into almost any computer-based system. Here are just a few examples. (Prices are F.O.B. San Jose, and quantity discounts are available. TV monitors are extra.):

GMR 37-10: $3300

256 x 256 resolution, one channel RGB color plus blink. (Two channels: $3700)

GMR 37-20: $3700

256 x 512 resolution, one channel RGB color plus blink. (Two channels: $4500)

GMR 37-30: $4500

512 x 512 resolution, one channel RGB color plus blink.

GMR 37-60: $4700

1024 x 1024 resolution, one channel B/W.

In addition, you can also have several economical options: independent cursors, joysticks, keyboards, special character sets and 16 bit, plug-compatible parallel minicomputer interfaces.

Further, if you ever want to move up, Grinnell has a complete line of larger systems—all software compatible with the GMR-37—to do things like animation, image processing and real-time frame grabbing.

So, if quality graphic displays are important to your product, look at the GMR-37 line. For a quotation on the system that meets your specific requirements, call or write.

GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

Circle 24 on Reader Inquiry Card

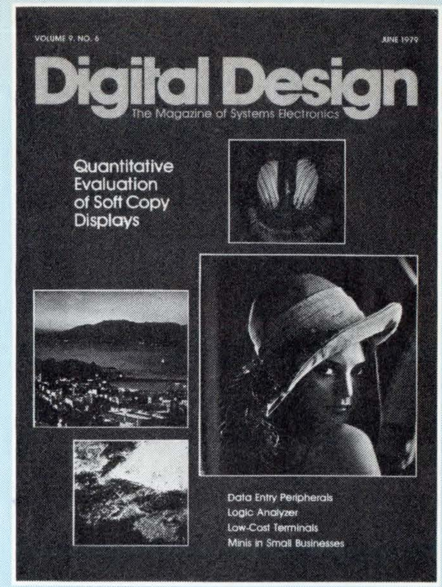
VOLUME 9, NO. 6 JUNE 1979

Digital Design

The Magazine of Systems Electronics

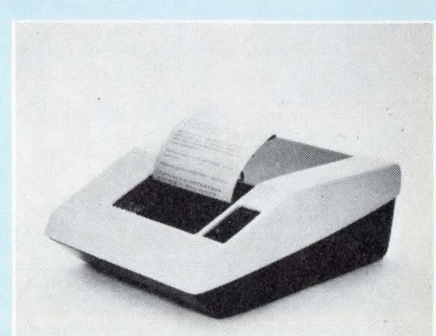
Features

Departments



ON OUR COVER
New architectures and designs permit improved graphics and greater resolution, as shown on our cover. To find out more, turn to pg. 54. Cover design by Richard D. Sarno and photos courtesy of Comtal Corp.

LOGIC ANALYZERS



MICRO SOFTWARE

DIGITAL DESIGN
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every two hours of every working day somebody puts a TC-130 on a PDP-11 computer

Here are just a few of the reasons why more people put TC-130's on their PDP-11 systems than any other magtape controller:

- Software compatible – embedded design
- Mixed density – 1600 bpi PE and 800, 556, 200 bpi NRZ
- Intermix 9 track and 7 track, up to 8 drives
- Fits all PDP-11 Series Computers
- Dual speed – switch selectable, 12.5 to 125 ips

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*Trade name of Digital Equipment Corp.

Circle 9 on Reader Inquiry Card

Letters

Array Processors

Dear Editor:
I would like to respond to the letter from Philip Blake of CSP Inc. which appeared in the March issue in the "Letters To The Editor" column.

First, communication between any array processor and the "outside world," such as a host computer, must be asynchronous. Talking between two systems that operate from different clocks always requires a means of coordination, including appropriate handshaking. However, within an array processor, different logic section need not operate from independent clocks. In fact, good logic design minimizes the number of places where asynchronous signals must be coordinated.

Analogics array processor incorporates asynchronous interfacing logic for talking to the host computer and to devices attached to its auxiliary port. Within the unit itself, however, all logic is clock synchronous — an approach that allows Analogic to make firm statements about execution speeds and about interaction time losses, when overlapping processing and I/O.

Second, the number of buses within an array processor is generally irrelevant to the user. All buses do the same thing: they tie together different parts of the processor. The key question is not the number of buses used but, rather, the effect on throughput rates when arithmetic processing overlaps I/O operations.

Furthermore, fewer physical connections between the cards of an array processor leads to better system reliability. How those physical inter-card connections are grouped into buses is a logic designer's job, not the system user's proper concern.

Third, Analogic's array processor operates with its executive and application programs resident in its own program memory. The AP400 can handle DMA interfacing under its own steam, both to/from the host memory and to/from devices connected to its auxiliary port. We agree that keeping the host computer as free as possible from the burden of managing an array processor is important to avoid paying part of the price of an array processor for an expensive host.

Finally, the AP400 application library can be invoked via Fortran calls, Host Assembly language. Analogic's AP400 Assembly language resembles that for any modern minicomputer because of its narrow-width, register-oriented instructions. Ease of use at any coding level is designed directly into the AP400. Thus no additional level of coding is required.

Gerald N. Shapiro
Analogic Corp.
Wakefield, MA

Major Improvement

Dear Editor:

There seems to be a major improvement in this issue (February) in many ways. The article evaluation and balloting idea in your Speakout are terriffic.

I. Moskowitz
Project Elec. Eng.
Bethlehem Steel Corp.
Sparrows Pt., MD

Want Reforms

Of the hundreds of readers who wrote to us about the February Speakout, most were in favor of reforming the IEEE. Judging from the unexpectedly large response (and the polarized views), it seems we touched a sensitive nerve. We published some of the pro and con responses last month. Here are several more that couldn't run due to space requirements.

Dear Editor:

Regarding question 25 in the February Speakout, I was a faithful IEEE member, but finally allowed my membership to expire out of frustration. The IEEE cannot, now or ever, represent or realistically deal with the problems of the working engineer.

J.B.
Middletown, RI

Dear Editor:

I was an IEEE member for many years but quit in disgust.

C.F.
St. Louis, MI

Dear Editor:

With reference to the IEEE, collectively we are getting what we deserve. This will probably be my last year as a member of IEEE.

A.Q.
Rochester, NY

Dear Editor:

With reference to item 25 in your February Speakout, I was in the IEEE for several years, and was editor of a section magazine. I dropped my membership because the IEEE offered nothing but magazines and a $50 tax deduction. The IEEE is useless to me.

Name Witheld

Dear Editor:

Engineers must have a professional organization. Without a doubt, major aerospace firms chase the young engineers and push out the older engineers at completion of projects. It's always easier to let the hard-working "no-flair", 8-6 pm engineer go because he won't give the boss a hard time about it.

R.O.
Waltham, MA

Dear Editor:

I quit the IEEE in 1972. A new organization is the only answer.

S.C.
Houston, TX

Dear Editor:

While I do not agree completely with Feerst's positions, I believe there is a lot of truth in what he has been saying about the IEEE board of directors.

J.D.
Melbourne, FL

Dear Editor:

More than 80% of your readership are working EE's. Less than 10% of these people are IEEE members. Is IEEE an engineering organization?

D.W.
Cherry Hill, NJ

Dear Editor:

The IEEE is nothing more than a technology reporting society and a forum for college professors seeking acclaim for technical efforts (also to survive under the publish or perish system). The IEEE has not, and will not ever perform any service toward uplifting engineers.

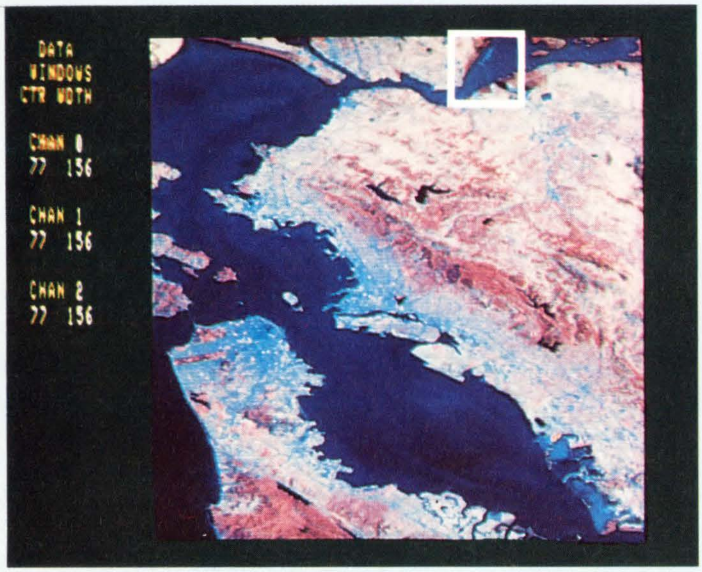
N.N.
Tampa, FL

Dear Editor:

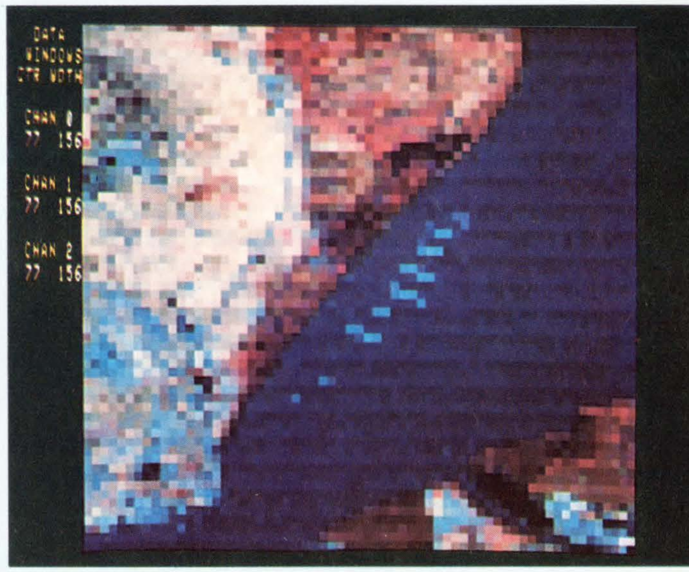
I think engineers are too conservative. It's time to speak up: a new organization is the way.

S.G.
Greenlawn, NY

THE IMAGE ARRAY PROCESSING SYSTEM



Three band LANDSAT image of San Francisco Bay



Eight-to-one zoom of Suisun Bay

If image analysis and aquisition is your problem, you need the IP 5000 Image Array Processor.

The display system that:

- Stores up to one megabyte of data for single or multiple image arrays.
- Has complete independence between refresh memory (raster scan output) and host computer addressability of memory.
- Includes memory management and data control for direct high speed access to refresh memory.
- Includes a powerful, pipe-line processor to perform high speed image array processing and statistical analysis.
- Performs pixel replica zoom of 2:1, 4:1 or 8:1 in real time.
- Can selectively change format between 525 line and 559 line video formats with external sync capability for 525 line formats.
- Is capable of scrolling, in any direction, a pixel or line at a time or multiple pixels and lines without causing tearing of the visible image.
- Digitizes video signals up to 8-megahertz bandwidth with true 8-bit precision.
- Has multiple intensity transformation tables for grey scale, color or pseudo color displays.
- Has proven reliability with field installation at some of the top names involved in image processing and display.

For further information and a list of satisfied users, contact DeAnza Systems, Inc., 118 Charcot Ave., San Jose, CA., 95131, (408) 263-7155.

De Anza Systems Incorporated

GIVE YOURSELF A BETTER IMAGE

Circle 10 on Reader Inquiry Card

A Question of Conviction?

Several months ago we decided to increase feedback from Digital Design's readers. Since we were introducing a new Reader Inquiry Card in February—permitting you to rate our articles, to vote for Designers' Notebook entries and to tell us what you wanted to see more (or less) of—we didn't expect great voter participation at the start. As a test, we ran an editorial Speakout, "What Next?" But when the cards were sorted and tabulated, 412 readers had voted.

As for the poll, most readers answered all five questions, and one in seven added comments on the subject. Here is how Digital Design's readers voted:

	YES	NO	UNDECIDED
1. Does IEEE need a major reform?	93.5	6.1	0.4
2. Is there much chance of reform?	1.9	73.0	25.1
3. Should reform efforts be abandoned?	18.7	75.0	6.3
4. Would you favor a new organization?	58.1	22.4	19.5
5. Are you an IEEE member?	40.1	59.9	

Everyone agreed (15.4-to-1) that IEEE needs a major reform, but voted 38.4-to-1 that there isn't much chance for reform! Although by a 4.0-to-1 vote, they wanted reform efforts continued, when it came to favoring a new organization, it was a different story: the ratio was in favor, but dropped to 2.6-to-1.

We went further and divided members from nonmembers. Did they vote differently? Yes. Although they agreed on all issues, there was a difference in magnitude. After weighting data to account for differences in proportion, we discovered that in the first question, about 26.0 times more members voted for reform than against; for nonmembers, 19.2 times voted for than against reform. In the third question, 3.4 times more members voted for continued reform efforts than against; for nonmembers, 4.0 times more voted for continued effort than against. The fourth question surprised our editors: only 1.3 times more members voted in favor of a new organization than against (almost a split vote); although for nonmembers, it was a different story — 7.82 times more voted in favor of a new organization than against it (or about 8 to 1!) Numerous comments received from our readers suggest a possible explanation: former IEEE members, disatisfied with IEEE policy, dropped out and those remaining in the IEEE are more conservative voters (and, probably less likely to vote for Feerst of any other reform candidate.)

Members were somewhat more likely to vote undecided on issues than nonmembers, except on question one, where only two voters were undecided. Members were more likely to vote than nonmembers. Nearly 40% of the voters who voted were members, which is much higher than is representative in our readership.

Conclusions? Interpreting any poll data for causes and errects proves risky. What's left unanswered is the type of reform EEs want and how they should carry it out — a point several readers brought up. Other readers suggested more detailed questions. Still others brought up the subject of "willingness to do something," that is, told us that this was not a subject for polls to answer but "a question of conviction."

Note: Looking for product ideas and software information from our New Product section or ads? Simply tear out one of the Reader Inquiry Cards, circle those numbers for products on which you would like more information. There is no limit to the number of items you can circle.

The view from the top...
Our customers put us up to it!
"The high resolution and accuracy of the Talos lets the designer work to any level of detail at any scale without fear of error."
Computer Graphics, Inc.
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11 Main Street
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Hughes Aircraft Company
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Telephone (216) 672-2680
"P.S. We have also used (Brand X) tablets and have found the Talos to be far superior – keep up the good work. (You'll make mine easier!)"
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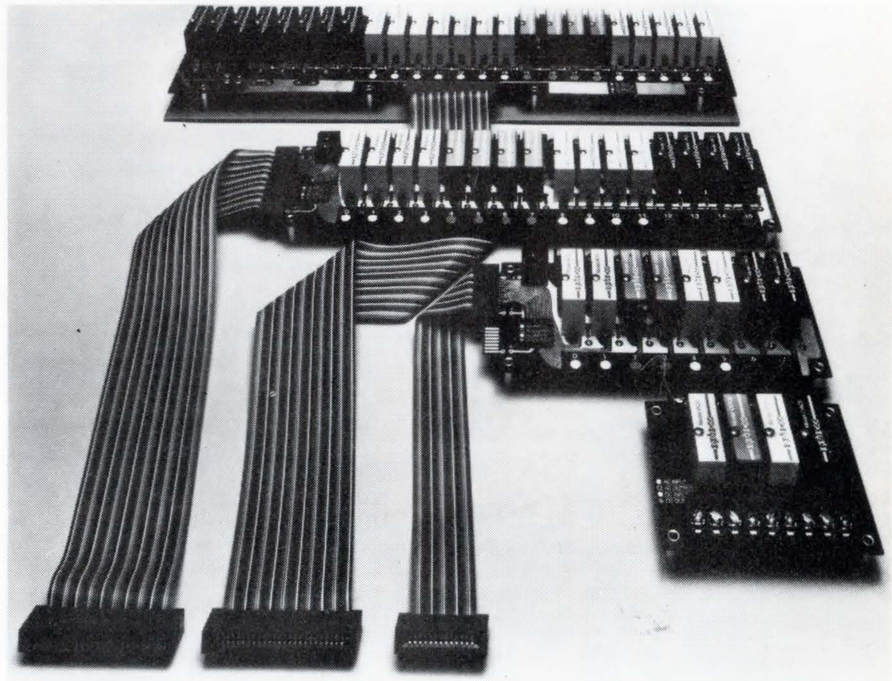
Circle 4 on Reader Inquiry Card

Technology Trends

Microprocessor Power I/O Interface System for Industrial Control



μP Power I/O Interface System for Industrial Control

The availability of microprocessors at astonishingly low prices has spawned a myriad of microprocessor based control systems. To support the microprocessor, peripheral equipment such as memories, displays, and a variety of terminals, have been developed. These have generally been well designed and highly compatible with the basic microprocessors, and well suited for their intended use. One facet that lagged, however, was development of the I/O interface between the microcomputer and the outside world.

The I/O interface is vital for two reasons: first, the microprocessor must be protected against transients, noise surges, et cetera, from the outside power system, and second, the microprocessor itself does not provide the power needed to perform work. While system designers or users once had to rely on a custom designed system, there are now systems which are not only more versatile, but are much more economical to utilize than a tailored, in-house design.

In the beginning, power I/O interfacing was generally accomplished by a dedicated system which the designer would customize for each project. These systems were quite limited in flexibility. Frequently, problems arose due to the electronic designers' lack of familiarity with the characteristics of the power system the microprocessor was driving. The microcomputer is highly vulnerable to noise, transients, and other anomalies of the electrical power of the system it controls. Often, the customized design systems did not take these factors into consideration and this resulted in malfunction of, or damage to the microcomputer.

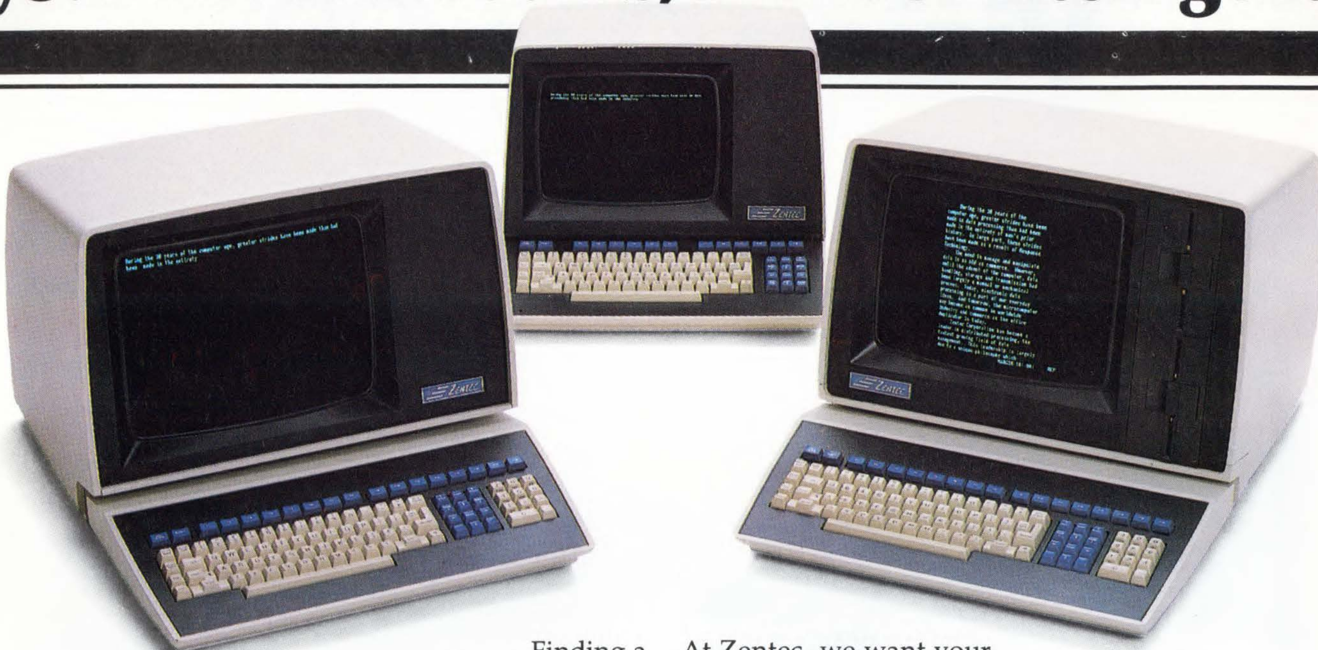
To put this into perspective, consider the differences between the two disciplines. The microcomputer on one hand uses power in the micro watt range, exists in a system which is well ordered, protected, and even pampered not only from the standpoint of electrical design, but also from problems of temperature, humidity, dust, dirt, et cetera. On the other hand, it controls power to equipment which can be subjected to great extremes of temperature, humidity, sand, dirt and most importantly, extreme fluctuations in the power system itself. Further, controllers are sometimes used in systems where the power is generated on site. Anomalies of these power systems can greatly exceed those encountered in the public utilities, even under such conditions as brown out, et cetera.

Clearly, an interface was needed which would satisfy the following requirements: (1) provide isolation of the microprocessor from the electrical power system it was controlling, (2) a design which would be easy to install, service and modify, if necessary, (3) the system should be flexible enough to accommodate a wide variety of functions, (4) it should be engineered to minimize operator and installation error and (5) it should be reasonable in cost.

Universal mounting boards

The I/O system which resulted from this consists of a universal mounting rack and a variety of plug in modules for the various functions. The mounting rack consists of an epoxy filled, glass fiber, dual sided, PC board in various sizes to accommodate four, eight, sixteen, or 24 modules. Power terminations are provided by means of a barrier strip at the side of the board. Logic signals are typically transmitted through an edge plug which is compatible with the standard 50 pin ribbon cable. This plug is used by the majority of microcomputer board manufacturers. The board itself is a universal, non-dedicated board. The function of each input or output is determined entirely by the module and includes AC input of 120 or 240 volts, AC output or 120 or 240 volts, DC input of 10 to 32 volts, and DC output of 60 volts or 200 volts. The board has the capability to utilize any combination of these modules in any order and this order can be changed at any time. The board contains a fuse for each module. These fuses are mounted on the board and are plug in type fuses which can be easily replaced if required. LED's have been added to

Considering alphanumeric terminals? Our I.Q. test can determine whether your needs are dumb, smart or intelligent.



Finding a source for alphanumeric terminals is relatively easy. Finding the right terminal isn't necessarily so easy.

That's where our I.Q. Test can help.

Numerous questions must be answered before you can specify the optimum terminal for your data or word processing system. Should it be dumb? Smart? Or intelligent? Clustered or stand alone? Do you need local processing capability? Expansion RAM, ROM or PROM? Should it be user programmable? Or can you pre-program it to satisfy your system's requirements? The handy I.Q. Test inside our new ZMS Family brochure can help us help you find the

	Dumb	Smart	Intelligent	Your Requirements
Local CPU Processing	No	No	Some	
User Programmability	No	No	Some	
Expansion RAM	No	No	Some	
Expansion ROM/PROM	No	Some	Yes	
Displayable Characters	64	64–96	128–256	
Video Attributes	Limited	Some	Some	
Screen Character Matrix Resolution	5×7	7×8	7×9	
"Soft-Font"	No	No	Some	
Down Load Capability	No	No	Some	
Printer Capability	Some	Some	Yes	
Mass Storage Capability	No	No	Some	
Protected Data	No	Some	Yes	
Higher Level Languages	No	No	Some	

answers to these basic questions. And more. Here, you'll also find detailed information on our new ZMS Family of intelligent terminals: the ZMS-50, ZMS-70 and ZMS-90 . . . three intelligent solutions to your system design problems.

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provide the status of the signal between the microprocessor and the module. Pull up resistors have also been added to the board to provide a path for the leakage current on the logic side.

The 8, 16 and 24 module boards terminate in a 50-pin connector which is compatible with the major microprocessor board manufacturers. It is pin for pin compatible with the Intel 8010 and by simply reversing the odd and even pins, i.e., by turning the plug over, it is compatible with the 8020, 8030 and other Intel boards. To minimize noise, a large portion of the underside of the board is devoted to the ground plain. The logic bus is designed so that a ground line is always adjacent to the data lines, thus, providing shielding for the logic data transmission.

Switching for the output modules is accomplished by sinking the V_{cc} current through a photocoupler into the open collector of the control transistor and to ground. Logic power can be provided to the board either through the two terminal barrier strips adjacent to the edge connector or through the ribbon cable from the microcomputer itself, by utilizing a jumper consisting or the fuse, in the appropriate socket.

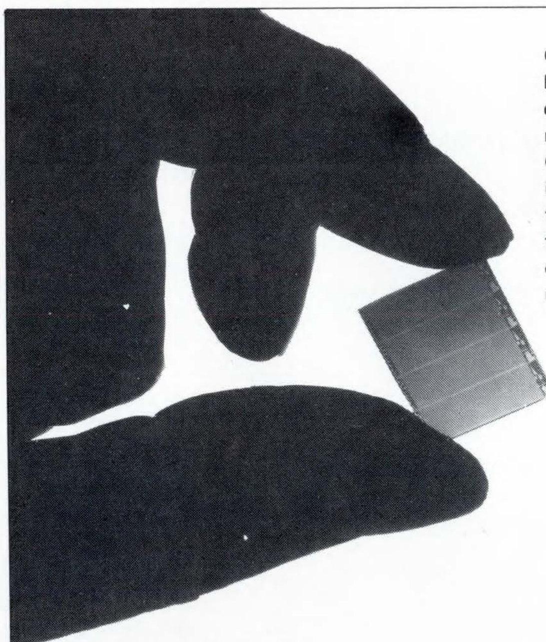
The four terminal board utilizes a barrier strip for logic signals instead of the typical edge connector. Since only six leads are required, the use of the 50 lead cable was not practical. Initial cost of this system in medium sized applications is $12 — $15 per point. This includes both the amortized cost of the board plus the cost of the modules. Subsequent costs are substantially lower than dedicated systems since individual modules can be replaced or functions changed as desired. This contrasts with hard wired dedicated systems where a change requires an entire board, and a change of function may not be possible. The versatility of this system results in lower costs which, although intangible, are nevertheless real.

Jim Pancake
Opto 22, Huntington Beach, CA

First 1 Mbit Bubble Memory Targeted at Micros

The world's first commercially available megabit memory device — the Magnetics 7110, a 1,048,576-bit Magnetic Bubble Memory — can go immediately into system development without becoming involved in the intracacies of bubble memory technology.

Like previous R/W memories, the 7110 bubble memory enables data to be stored and retrieved or modified online. It combines R/W features with non-volatility, yet is competitive in storage density with tape and disk drives.

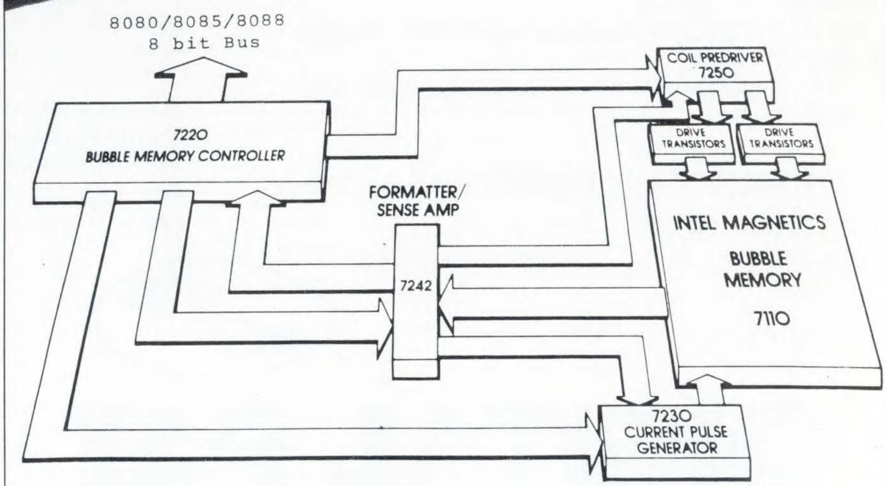


FIRST MILLION-BIT MEMORY DEVICE – Magnetic bubbles store over a million bits of data in this new memory component from Intel Magnetics of Santa Clara, California. Intel Magnetics is a subsidiary of Intel Corporation, which developed the first thousand-bit semiconductor memory device in 1970, and the first microcomputer in 1971.

Device organiztion

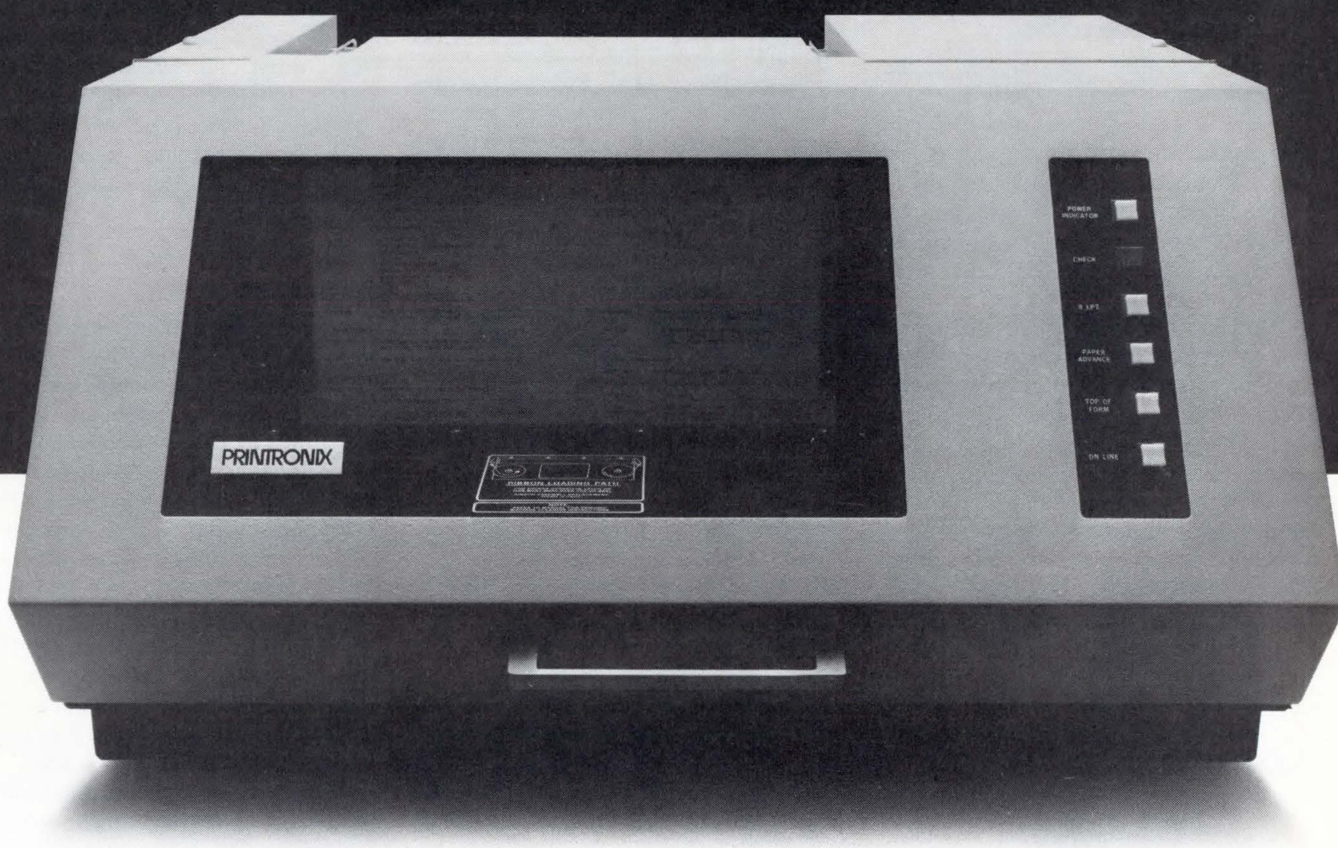
The 7110 bubble memory is organized as a serial in — parallel loop storage — serial out, shift register (block replicate architecture). It stores 2048 pages of 512 bits each, formed by combinig two 256-bit registers with serial output channels and each page is processed as 64 8-bit bytes.

In system operation, a page or a burst of pages up to the entire 2048 can be read or written at one system request. Pages are so located that after reading or writing one page, the next page is immediately available. The device can also be started and stopped between sequential pages to give controlled rapid access — an aspect of particular importance to system designers and integrators.



Support LSI circuits available with the Intel Magnetics 7110 turn this Magnetic Bubble Memory into a complete memory system.

BEFORE OTHERS CAN PRINT A WARRANTY LIKE OURS, THEY'VE GOT TO MAKE PRINTERS LIKE OURS.



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The reason: *Unequalled reliability.*

Our reliability comes not only from what we put into our printers, but also because of what we leave out. For instance, Printronix printers have 50 percent fewer components than mechanical font printers. So there's less to go wrong!

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So, before you buy a printer, read the fine print on their warranty. If they're not giving you the same full one-year warranty that Printronix offers, then it's a sure bet they're not giving you the same solid reliability that Printronix gives.

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PRINTRONIX

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Based on the standard shift rate of 50 kHz, the average random access time of the 7110 is 40 msec; the maximum data rate, twice the shift rate, is 100 kHz. A page read or write requires 327 shift cycles so that the R/W time is 6.5 msec and average data rate is 78 kHz. These data rates can be multiplied at the system level by parallel operation.

Built-in error correction

Additional storage, not counted in the data capacity, is also built into the 7110; and part of it is used for error correction: the error code can detect and correct burst errors up to 5 bits in length in each channel. Thus, you may bypass this built in feature and have 32 bits available to implement other error correction codes.

The memory also includes extra storage to increase the production yield of good devices by permitting some defective loops. 48 redundant loops are included for this purpose and the device carries an internal code that is passed to the 7242 formatter to make unused loops user transparent.

Because code is carried within 7110's memory, a 7110 can be removed, another plugged in its place, and the system automatically adjusts to the new device. In fact, the system adjusts itself each time power is turned on, and the controller is given the initialize command.

New system configurations

For increased capacity, 7110 bubble memory systems can be assembled in several ways. One 7220 controller can operate up to 8 7110 devices in parallel, or 8 multiplexed 1,2 or 4 at a time. Parallel operation increases speed while multiplexed operation conserves power.

Controllers can also be operated in parallel to give 16-bit and wider bus widths, with up to 8 7110 devices in each bank. Further, such subsystems can be multiplexed using normal memory expansion techniques to multiply total system storage capacity.

The bubble memory system can transfer data to the system bus through Polled I/O, Interrupt Driven I/O or Direct Memory Access. DMA will often be used for medium and high performance systems operation. The DMA mode allows data to be transferred to RAM faster than the μP itself can transfer data into memory.

Reliability improvements

Mass memory storage systems such as tapes and disks are electromechanical and usually operate in moderate environments. In contrast, this bubble memory family exhibits high reliability that extends to the storage media (unlike tapes and disks, magnetic media is sealed from contamination).

Other specs? The 7110 has high resistance to shock, vibration, humidity and radiation, an operating temperature range of 0° to 70° and can be stored with data retained from -40° to 100°C. It is a mass memory suitable for environments too harsh for electromechanical systems.

The system operates from standard +12 and +5 V supplies. Power consumption for the system is 6 W when active; 1.3 W on standby. And when turned off, it retains data with zero power consumption.

Support ICs

User interface is provided by the 7220 Bubble Memory Controller (BMC). From a practical standpoint, the 7229 interface makes the system look like a peripheral to the μP system bus.

The HMOS BMC 40-pin device provides bus interface, generates all memory system timing and control, maintains memory address information and interprets and executes user requests for data transfers.

The 7242 Formatter/Sense Amplifier (FSA) is a dual-channel unit that interfaces with both channels of the bubble memory. It is a 20-pin device built with NMOS technology that senses the low-level bubble signals, handles redundant loops and buffers data, and contains the burst error detection and correction circuits for each channel.

The 22-pin 7230 Current Pulse Generator (CPG), a Schottky bipolar TTL device, supplies the relatively high peak currents required by the bubble memory and also contains a power-down circuit to shutoff current sources when the device is deselected — shutting everything down in an orderly manner.

High currents with peaks beyond the capacity of standard ICs are required to drive the coils. Therefore the 7250 Coil Predriver (CPD) interfaces the 7220 BMC to driver transistors, such as quad bipolar transistor packs or quad VMOS FET transistor packs (this CMOS device comes in a 16-pin package).

What do these support circuits do? By providing all the complex control and interface between the system bus and the bubble memory array in a simple-but-flexible manner, the support circuits let you start with a compact development board or connect his system board components with minimal effort. These LSI circuits replace what would otherwise be a board full of control electronics; they make it practical for you, the OEM, to use the 7110 in production products.

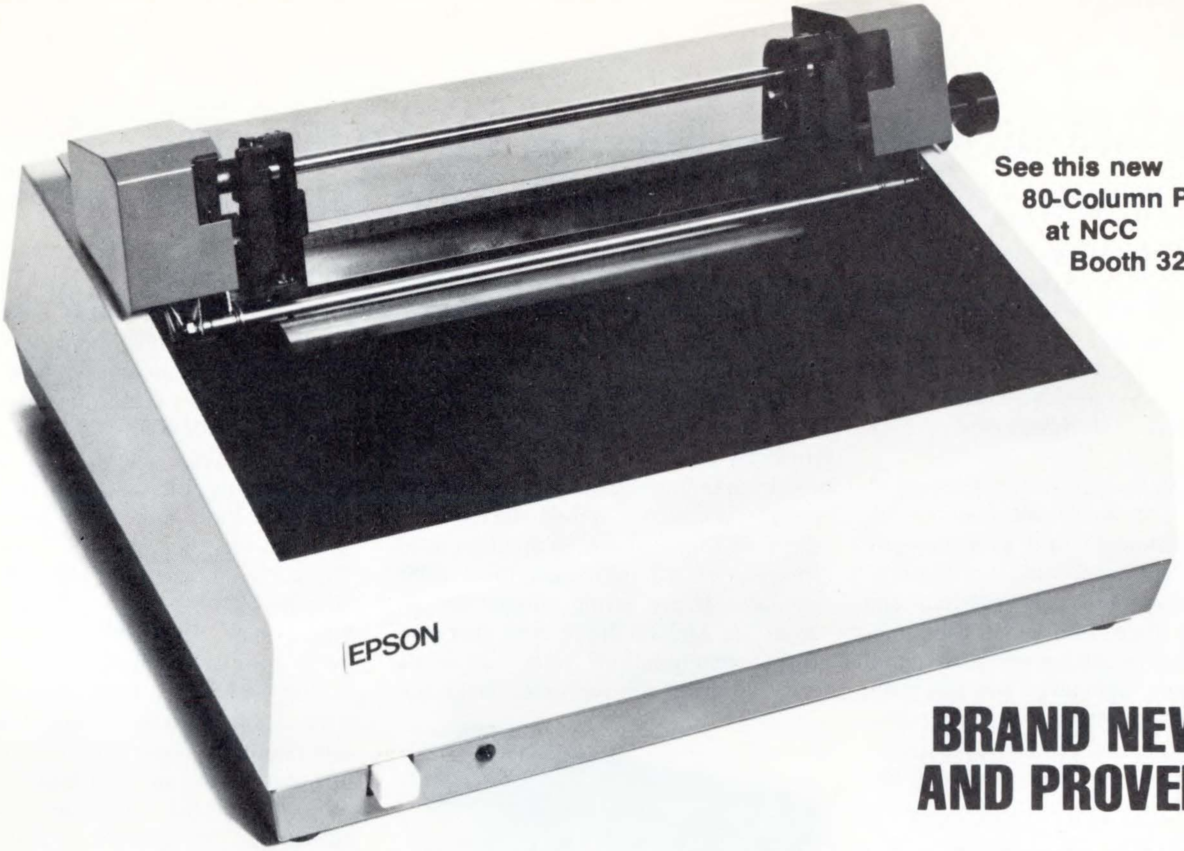
Micros first?

Immediate applications exist for high-density bubble memory systems in μCs, while large computer architectures should go through an evolution in the 1980s to utilize bubble memory.

What does the megabit capacity of such bubble memories mean to microcomputer design? They complement recent micro trends: capability to address megabyte memories, use of high-level languages, longer and more complex applications programs, larger data bases (storage of business and other data), and continued emphasis on reducing the size and increasing the portability of micro-based products.

What μC systems are these devices suited for? Data terminals, word processing and other business systems, industrial control systems and telecommunications systems — these and other systems often require peripheral read-write memories storing 128 kbytes to around 2 Mbytes (the capacity range of most tape and diskette peripherals). With the magnetic bubble memory components family, such memories can be easily built into the basic μC system and the systems integrator or designer can eliminate large supplies, motors and other costly and maintenance-prone electromechanical devices.

You can immediately order a 7110 prototype kit which allows equipments designers to build a magnetic bubble memory system into new products. The price? Approximately $2,000. Deliveries begin this Fall. **Intel Magnetics,** 3000 Oakmead Village Dr., Santa Clara, CA 95051. (408) 987-7700.



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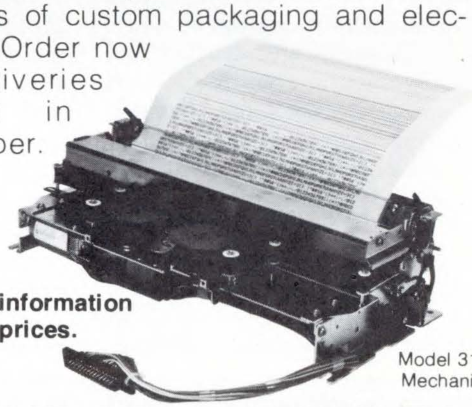

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Powerful 8-Bit 8088 Houses 8086's 16-Bit Architecture

Intel's 8088 promises to become the hottest 8-bit micro of 1979. It contains the 16-bit internal architecture of the 8086 combined with the 8-bit bus interface of the 8085A. What does the 16-bit internal structure do? It provides performance far surpassing any current 8-bit device, yet its 8-bit format makes it compatible with most of today's μP system designs.

The 8088 is 100% software compatible with the 8086 and features advanced arithmetic and alphanumeric (ASCII) data capabilities so that programs require fewer instructions and run faster than with other 8-bit machines. The instruction set is structured for efficient high level and assembly language programming which shortens development times, allowing users to bring their 8-bit products to market faster.

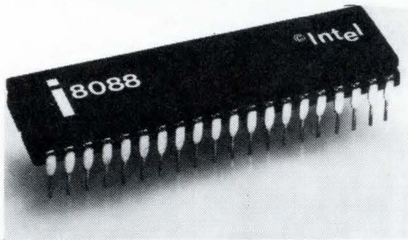
Minicomputer performance?

How does the 8088 differ from other 8-bit micros? In six ways: • megabyte addressing, • flexible addressing modes — two levels of indexing plus displacement possible in a single operaton, • 8/16-bit hardware multiply/divide, signed or unsigned, • extensive string handling instructions, • instruction look ahead and • dynamic program relocation capabilities.

The internal architecture enables it to process 8- or 16-bit data in single, string or block form. Sixteen bit quantities are automatically fetched and written a byte at a time buy the CPU. Its special control lines facilitate operation with multiple processors and shared resources, as well interfacing easily with Intel's MASSBUS architecture.

With its 20-bit addressing, the 8088 can directly address up to a byte of memory. Memory space is addressed in segments of 64K bytes with a very flexible address development structure. The device has 24 addressing modes including those with three levels of indexing (base register value, index register value and displacement) summed then added to the appropriate segment register to create addresses. These modes make it easy to perform string, table and metric operations within the basic instruction set. Segmentation allows program code and data to be dynamically relocated by moving the code or data and changing the segment register's value. Program branches can be made relative to the current program counter to provide position independent and relocatable code — making it easier for the programmer to write more efficient code.

The 8088 contains its own hardware 8-bit and 16-bit signed and unsigned multiply and divide instuctions. Arithmetic operations can be used with binary, ASCII or packed decimal (2-digits/byte) numbers. In addition to its number crunching capabilities, 8088 includes many string operations for handling alphanumeric data that perform manipulations such as block moves, string comparisons, data scans



Intel's 8088 contains the 16-bit internal architecture of the 8086 combined with the 8-bit bus interface of the 8085A.

and data translations. In short, the processor is as useful in word processing and business equipment as it is in mathematical computation and control application.

Inside, the 8088 is divided into two processors — a bus interface unit (BIU) and execution unit (EU). The BIU handles I/O data transfers and interfaces with memory. It continually fetches instructions and stores them in a 4 byte queue. EU, which includes the ALU, executes the instruction stream from the queue and manipulates the internal registers. This concurrent operation improves bus efficiency by eliminating much bus dead time. It permits the memory access time to be a healthy 460 nsec (110 nsec longer than permitted by the 5 MHz 8085A). The long memory access is compatible with all of the common μP memories, keeping memory costs low.

The 8088 operates at 5 MHz and uses a four-clock (800 nsecs) bus cycle. A 16-bit register move takes only 400 nsec to execute when the instruction is waiting in the queue. It executes 8-bit multiplies in 15 μsec and 16-bit multiples in 26 μsec, with full 32-bit results.

High performance

Since a 16-bit bus has twice the bandwidth of an 8-bit bus, the wider bus has considerably higher throughput and is suited for higher performance systems. However, both 8088 and 8086 include instruction fetch ahead. This instruction queuing increases efficient data bus utilization and makes bandwidth-comparisons applications dependent. Typically, 8088 throughput is between 70 and 80% of the 8086 — significantly higher than indicated by the bus bandwidth comparison alone.

Why retain an 8-bit bus structure when designing a new system? Because this maintains compatibility with existing hardware: an 8-bit board can be redesigned and upgraded without changing backplanes, connectors, memory structure or peripheral controllers. It also offers savings in drivers, transceivers and board space. Furthermore, when building minimum component count systems, there are multiple-function devices available in the family,, e.g., 8755A EPROM and I/0; 8155 RAM, I/0 and timer; or 8185 1K×8 RAM memories, that allow an 8088 system to be assembled with as few as four devices. Character oriented applications where the data handling is normally done at the 8-bit level (especially those involving CRTs, keyboards or word processing) are good candidates for an 8-bit structure.

Family compatibility

Both 8088 and 8086 CPUs share a full line of compatible support components available now. Software runs on Intel's Intellec Microcomputer Development System, and the same development software works for the 8088 and 8086. It includes the ASM-86 Assembler, PL/M-86 structured high-level programming language compiler, CONV-86 converter program to translate 8080A/8085A assembly code to 8086/8088 assembly code and many other software aids. Both products are also complemented by a coordinated array of latches, transceivers, memories and peripherals, so the systems integrator and designer can pick and choose to optimize his product.

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Software Maintenance: How to Plan For It

We are now entering the second stage in the evolution of microprocessor-based products. The first stage emphasized design and development, during which engineers, technicians and programmers had to learn to use microprocessors. Short courses provided brief introductions and numerous articles and books described de-

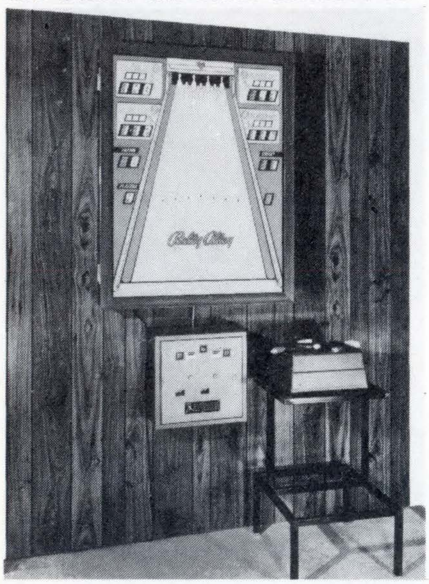

Fig 1 The Bally Alley electronic bowling game, a microprocessor-based amusement product from Bally Manufacturing Co., Chicago, IL.

vices, programs, circuits and methodology **(Refs 1-4)** Obviously, this stage continues to this day, because new industries and new companies are getting into microprocessors. Consequently education in basic design and development will remain important in industries and in universities for the foreseeable future.

In the second stage, during which substantial number of microprocessor-based products are actually in use, our attention turns from design and development to maintenance and repair. Over the life cycle of most products, more time and money goes into these tasks than went into design, development, test and all the other work done during the first stage. The Bally Alley Electronic Bowling Game, the Gnat Computers Floppy Disk Microcomputer **(Fig 2),** The Micom Communications Microcomputer **(Fig 3)** and the Axiom EX-801 Microcomputer **(Fig 4)** represent microprocessor-based products that have entered the second stage. We will discuss how to maintain the microcomputer software that performs many of the functions in these systems.

What Is Software Maintenance?

To maintain software, do you have to send someone out to oil all the branches in a program or to check whether two subroutines have shorted together? Does a program loop begin to fray at the ends or does a jump instruction begin to wear from excessive use? The answer fortunately is no. The program will continue to operate in the same way as long as the memories, processor and connections last. Wear and tear seldom represent the same problems in software that they do in mechanical or electrical hardware. Software maintenance involves diagnosing and correcting software problems that are only recognized in field use. It may also consist of updating and changing what customers may want or need, what competition may require, or what new standards may make necessary.

A Typical Maintenance Problem

Let us then look at a typical software maintenance problem. Let's assume that the product is a microprocessor-based test system from an unspecified manufacturer and product under test. System sales are high, because the product cost is not only reasonable, but provides numerous desirable capabilities. Moreover, these testers are now key machines in any plants. However, one purchaser reports a strange problem: in one particular kind of test (an uncommon one, but vital for this installation), the system will only accept 31 test points; when the thirty-second point is read, lights flash, buzzers sound and the only way to stop the commotion is to reset the system and start over agin. This oc-

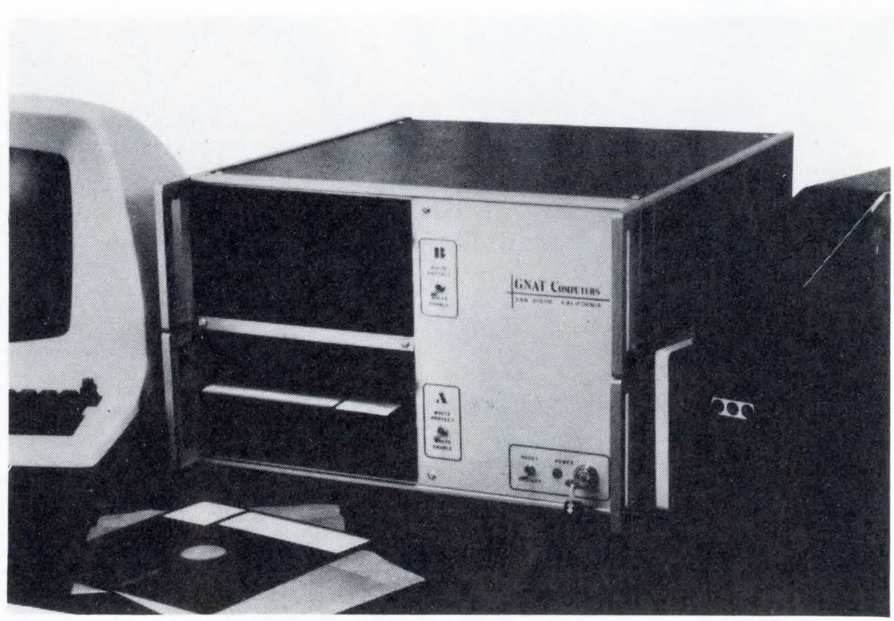

Fig 2 The Gnat floppy disk microcomputer, an 8080-based computer and development system from Gnat Computers, San Diego, CA.

currence should lead you to suspect a software error, since there is no reason for the hardware to even recognize such a situation.

FACT #1. The customer does not know and does not care whether the problem exists in the hardware or in the software. He only wants the system to work. Therefore, the software must be just as maintainable as the hardware or else you're sure to have unhappy customers (regardless of good excuses).

Finding Current Documentation

First, let's assume (over the protests of the programmers) that a software error has appeared. How do we fix it? The first step, of course, dictates that we find the documentation. Is the

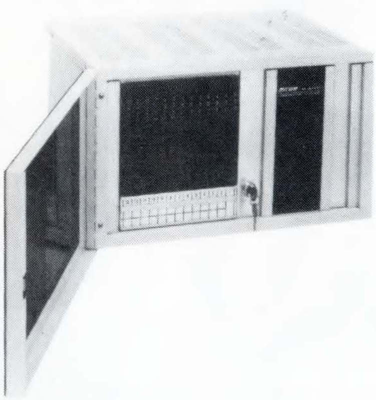

Fig 3 The Micom communications microcomputer from Micom Inc., Chatsworth, CA.

software documentation filed with the hardware documentation? Is it in the development system files? Is it at the bottom of somebody's desk or in the heap that was in somebody's desk before he or she left the company?

FACT #2. Software documentation is useless, if you can't find it. You must handle it as carefully as hardware documentation. Otherwise, you can waste a large amount of time just searching for the material that you need. Remember that an unhappy customer is waiting for a solution to his problem — a situation that differs very much from design and development.

Assume now that we have managed to find the documentation (presumably at the back of a file or in somebody's stack of scrap paper). Is it really the latest version? Is the listing the one that you used to burn the ROM or PROM or is it the one just before the final one? Does it include those last-minute changes that someone made? Did anyone put a date on any of the documentation?

FACT #3. Unless documentation is up-to-date, it's useless. The final documentation must be dated, verified and checked by all concerned to be sure that it contains the latest information. Otherwise, you'll need an expensive brainstorming session to recreate the final stages of product development.

Understanding Documentation

Let us now assume that we have managed to find or updated the current documentation. Can anyone understand what it says? Does anyone remember precisely how an 8K (or even a 1K) program worked? Remember that we're talking about a task that was completed some time ago and the participants have long since moved on to other projects or to other companies.

FACT #4. Documentation is useless if no one can understand it. The person in charge of maintaining the product must understand the software as well as the hardware. The documentation must exist in a form that is comprehensible for maintenance purposes.

In past installments of this series, we have mentioned some techniques that can help, such as:

- Using high-level languages that are standard and, at least, partly self-documenting
- Providing two sets of flowcharts that describe how the program operates and how data flows through the program
- Using complete comments, meaningful names, organized definition lists, simple structures and repetitive logic
- Stressing simplicity and comprehensibility, even at the cost of some wasted time and memory.

Note that, in maintenance, you will pay for all the shortcuts that you may have used during design and development. How about that clever program which saved ten bytes of memory, but which no one now understands? Was it worth the extra week that you must spend to determine whether it works correctly? Was it worth the extra week that you must spend to determine whether it works correctly? How about the decision to code at the assembly or at the machine level rather than in a high-level language? Are the savings real or is the time spent checking complex assembly or machine language programs overwhelming them? How about the inexpensive development system that was inconvenient to use? Did it really save money or are you wasting the savings by searching for errors in programs that were inadequately doc-

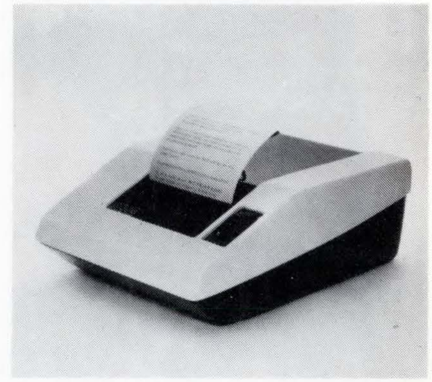

Fig 4 The Axion EX-801 microprinter, a small printer based on a single-chip microcomputer from Axiom Inc., Glendale, CA.

umented or were heavily patched at the machine code level?

FACT #5. Maintenance is an important factor in determining the total cost of a design and development effort. A minimum cost effort can result in tremendous expense (and customer ill will), when the time comes to maintain the products in the field. The advantages of using standrd high-level languages and a consistent methodology begin to appear when maintenance becomes the major issue. Developers of software and hardware for large-scale computers have long ago discovered this fact; that is why we're stressing so much the economics (Ref 5) and standardized software development methodology (Refs 6 and 7). You must make field maintenance an important consideration early in the design stage and test, quality control and maintenance personnel must become involved from the start.

Something Borrowed, Something Bought

What happens when some of the documentation may not be available at all? Where are those routines that someone borrowed from the monitor, from a book of programs, or from a users' library? How useful is the standard PROM that was purchased or how good are the programs that were written by a consultant? Were any of these ever documented and does anyone know whether they really work? Software may come in many different forms, however all require adequate

documentation and support.

FACT #6. Buying or borrowing unmaintainable software is a useless act. Either a local person must fully understand that software or the vendor must provide adequate maintenance. (Obviously such maintenance will cost extra and may well make the purchase far less of a bargain.) An obvious problem exists here, and because few microcomputer manufacturers even verify their users' libraries, much less maintain them.

Finding the Error

So far, we have only gotten to the point where someone can start to determine the source of the error. correcting it may be another story. Obviously, the customer will be very unhappy, if startup alone has taken weeks and months and other problems still remain, such as:

- Isolating the error, which may require time and a large amount of special equipment. The error may not even be reproducible on a development system and there may be no way to trace it in the product.
- Correcting the error
- Testing the corrected system to verify its operation
- Documenting the correction and the test procedure.

You can solve these problems in much the same way that you corrected similar problems in the design and development stage. But note that you can add to future troubles, if you make a quick undocumented fix that makes the next maintenance problem even more difficult to solve.

Conclusion

Software maintenance is a new task for many companies. Most project and product managers learn the hard way that the task can use a large amount of time and money. Software maintenance may sound like a joke now, but it can surely become less of one as more resources are expended in maintaining products that involve hardware and software. You can only solve the problem by planning an organization that starts operating at the vert earliest stages of products design and development.

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Designing a Low-Cost

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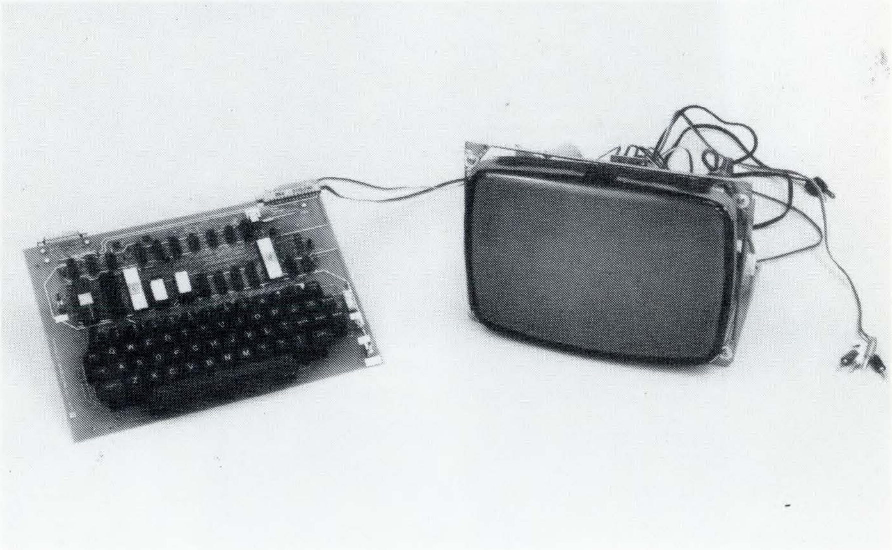

Fig 1 Low-cost, not-so-dumb data terminal electronic subassemblies consists of the video tube and only one circuit/keyboard. The terminal provides the smart functions of screen scroll, RS-232 interface and adjustable baud rate.

Dramatic and continuing reductions in the cost of transmitting data and the availability of low cost computing power has skyrocketed the demand for inexpensive data terminals. Responding to this demand, terminal manufacturers have attempted to lower costs by reducing component count with the introduction of LSI devices, such as microprocessors, CRT controllers, character generators, communications interface devices and keyboard encoders. However, only high-end units, the so-called smart and intelligent terminals, have taken advantage of the sophisticated functions of these advanced LSI device. Smart terminals that offer via keyboard control some internal intelligence and internal edit capability, may store and rearrange data within themselves. Intelligent terminals possess computerlike capabilities, internally programmable functions that provide display scrolling, full cursor control, and upper and lower case characters, as well as floppy disk and tape storage.

To date, advances in LSI technology have improved the largest category of data terminals — the so-called "dumb" devices — only slightly. These terminals, which possess no internal intelligence, supply limited control functions, such as carriage return and line feed. They are low in cost and easily adaptable to most computer systems. Even though present-day LSIs somewhat reduce total component count in dumb terminals, the terminals use a small fraction of power in these chips. Frequency limitations restrict much of the logic — the dot rate crystal oscillator, dot counter and associated logic, as well as character generation, dot shift logic and buffering — to SSI and MSI logic implementation. Particularly indumb terminals, character generation, dot shift logic and buffering often constitute the major part of the system.

However, selecting LSI devices that are now and soon-to-be available and implementing them into an optimum system architecture a minimum chip, not-so-dumb terminal on a single PC card is possible. Such a system retains the low cost and easy adaptability of

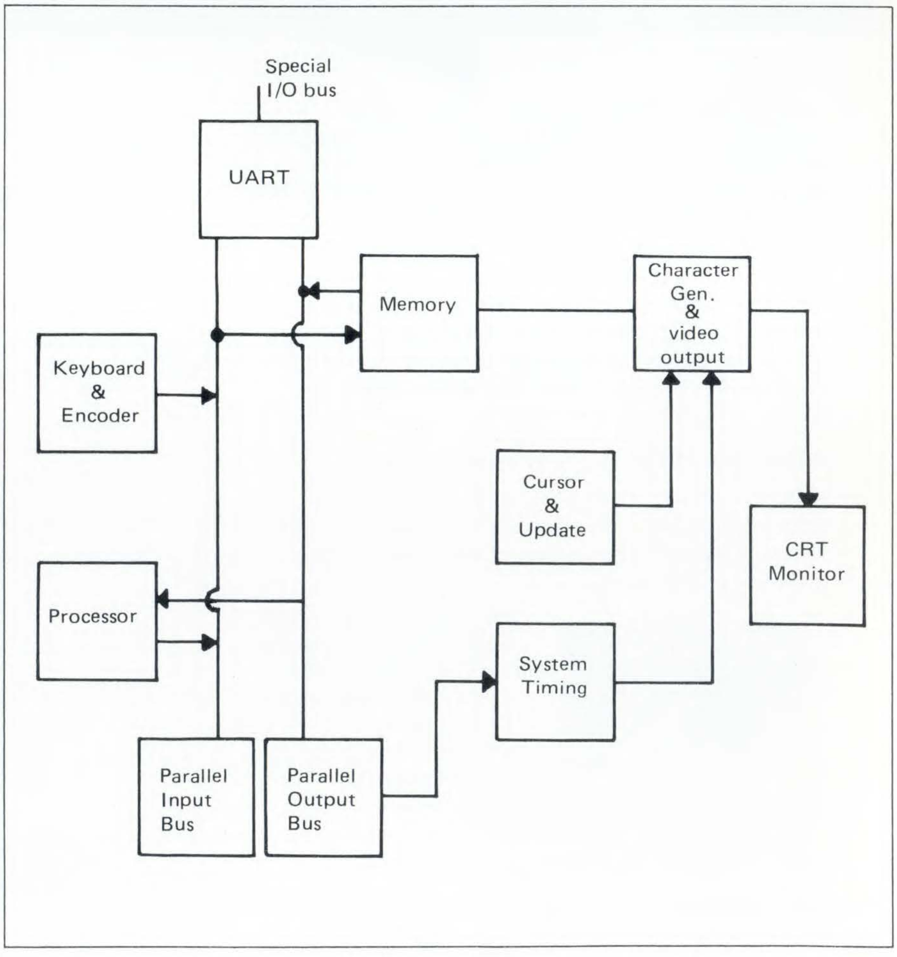

Fig 2 Diagram shows the functions blocks of circuitry needed to generate character displays on the face of the video tube.

Terminal with LSI Chips

dumb designs, but at the same time utilizes more of the microprocessor and its peripheral chips capabilities to provide some smart functions, such as screen scroll, RS-232 interface and adjustable baud rate **(Fig 1).**

CRT terminal fundamentals

The main function of CRT terminals is to convert stored, compactly coded characters located in memory into a repetitive form that a cathode ray tube can understand and use. Data terminals usually employ a raster scan. Conversion helps put a dot of light on the screen and move it around to generate a composite picture. Moving rapidly in an orderly manner called a scan, the dot starts in the upper left hand corner and goes rapidly to the right and slowly downward. Unlike standard TV sets, which use an interlaced raster scan, most CRTs use a non-interlaced approach. The TV horizontal scan rate is 15, 750 Hz for black and white and 15, 735 Hz for color. Two trips, or fields, down the screen generate one composite frame. One field which starts at the upper left and another in the upper center, overlaps or interlaces the two fields into a single frame. Each frame consists of 262-1/2 horizontal lines per field and a total of 512 lines. The field rate is 60 Hz and the frame rate is 30 Hz. Interlacing minimizes flicker and blur, especially when generating fast screen motions.

Non-interlaced scanning used in most CRTs uses 262 or 264 horizontal lines per scan. Since the frame rate, which equals the field rate, is 60 Hz, the horizontal scan rate changes to 15, 720 or 15, 840 Hz.

Scanning circuits that deflect the spot to a particular desired position on the screen, control dot motions in a CRT monitor. Although scanning is usually continuous, the start of each horizontal scan can be synchronized with the start of each frame by sync signals. Normally, these horizontal and vertical sync signals which must be relatively stable must be locked together. They don't start or stop the scan — they just shorten or lengthen the existing scan motions to lock them to an input for synchronization. Video and blanking circuits control the brightness. Blanking turns the spot off for the return trip on each horizontal scan and frame. Commercial TV set video circuits which determine spot brightness usually include video amplifier circuitry to provide gray levels. Instead, CRT monitors supply simple on-off or black-white levels to provide dots or no dots as necessary.

Data terminals generate characters with a dot-matrix system which displays each character as a group of dots or undots. Most CRT terminal monitors use either a 35-dot character, five dots

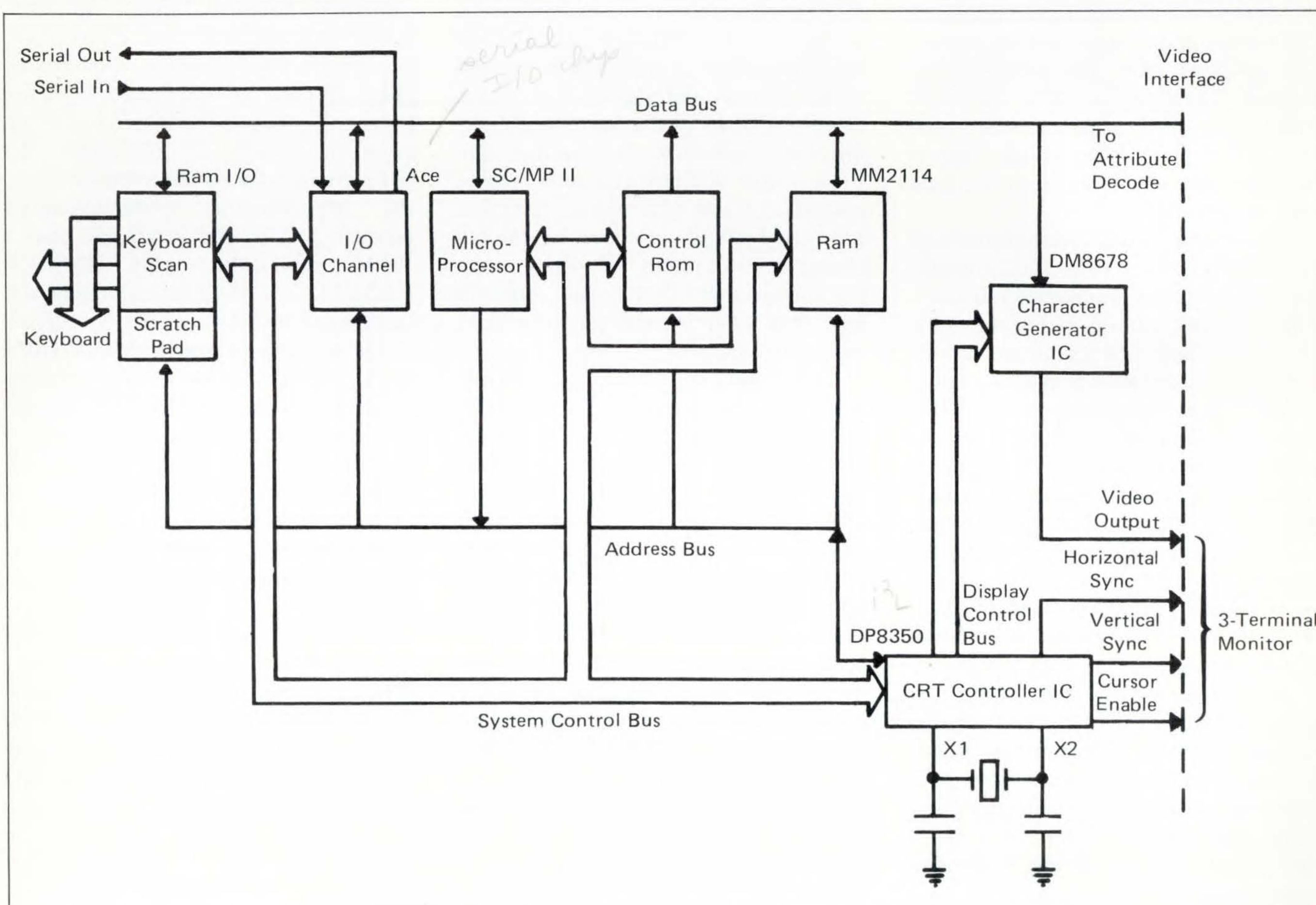

Fig 3 System block schematic of the low-cost, not-so-dumb terminal indicates the devices used to implement the design.

TABLE I. TERMINAL SPECIFICATIONS

Keyboard	
Style	Typewriter
Characters/code set	64/ASCII
Cursor controls	6
Keyboard encoder	Software
Communication	
Mode	Full duplex, half duplex option
Technique	Asynchronous
Communications Protocol	ASCII
Code	ASCII
Bits/character	10/11
Speed, bits/second	110 to 1200 (19,200 word-by-word)
Operator selectable speeds	4
Format	Character
Terminal interface	RS-232, 20 mA current loop
Display	
Display positions, characters/display	1920
Display arrangement (line x characters)	24 x 80
Total display symbols	64
Symbol formation	5 x 7 dot matrix
Reverse video	Cursor and whole screen
Scrolling	Yes
Cursor type	Block, reverse video
Cursor position	Down, left, right, home and return, back space.

wide and seven dots high, or a 63-dot character, seven by nine dots, plus the necessary extra undots between the characters and character lines. Any particular horizontal scan begins with the top five dots or undots of the first character laid down. In the next step, one or more dot/undots are skipped, and then the next set of character dot/undots are laid down, and so on across the screen. Laying down dots and undots in the vertical direction on each scan continues until all the characters are complete. It usually takes about eight to twelve raster lines to present a single row of characters.

The interaction of several functional blocks of circuitry **(Fig 2)** coordinates the generation of the character display. The essential memory block stores the characters and delivers them to the screen as needed to generate the desired display. It is often arranged as 1,024 words of 8 bits each, with one memory word associated with each displayed character or close grouping of display dots. The system uses about 2K bytes, the equivalent of one video page, for storage.

A system timing and control block converts and presents the information in such a way that the CRT can use it. This section, which includes the dot logic circuitry, the character and line counter sections, character row counters and memory address counters, generates the control pulses for the character generator and video output block for supplying vertical and horizontal sync to the CRT.

The character generator and video output block converts the six to eight bits of character stored in the memory into the group of data seen on the screen as a character. Making use of a diverse array of circuitry, including input address latches, character generation ROMs and parallel-to-serial shift registers, takes the input from the keyboard of serial interface, converts it into ASCII code, stores it and then outputs it to the CRT. A cursor and update circuit block takes care of adding new material to the memory and display. The cursor usually appears in the form of a blinking box, underline or overline that shows where the new character is to be placed. A frame rate system that takes 1/30 or 1/60 of a second to enter a character or a system with direct memory address that fills the entire screen in less than 1/60 second can provide a cursor and updating.

Communicating with the outside world also usually requires an I/O section that incorporates a UART, a baud rate generator, and line driver and receiver circuitry. Normally, CRT terminals are set up to accept input words in parallel form, not only because they cost less and are faster, but are convenient to use with keyboards and μP data buses. Interfacing the monitor with a serial operating device, such as a modem, requires a UART for serial-to--parallel and back again conversion. Baud rate generators provide the reference frequencies needed by the serial interface devices and line drivers and receivers amplify 1s and 0s so that loads can be driven and so that wiring capacitance and cable runs do not adversely slow down system speeds. They also can send signals long distances over wired serial interfaces. Communication with the keyboard also needs an encoder block. This circuit samples the keys and provides a parallel ASCII output with parity.

The processor block operates with an associated group of control ROM circuits. It performs such functions as updating the CRT display memory, controlling communications with peripherals and other elements in the system.

Single CRT

Designing a "dumb" terminal with all these elements in the past required as many as 100 to 150 MSI and SSI devices. In most cases, this large number of components required three to four boards. By using one of the standard μPs and surrounding it with support chips, designers cut component count by about 50%. This parts count typically needed only two boards.

You can reduce component count by yet another 50 to 75%. You can also increase intelligence by the proper selection of a number of advanced LSI circuits which are now becoming available.

We have designed a compact not-so-dumb terminal complying with the specifications listed in Table 1. Self-contained on a single 9" by 12" card (except for the CRT monitor), the terminal **(Fig 3)** uses an integrated injection logic controller (DP8350); a single chip eight-bit NMOS μP (INS8060 SC/MP); two advanced μP interface parts, the asynchronous communications element (ACE) for serial I/0, and a RAM input/output chip (INS8356 RAM I/0) for keyboard scanning and scratchpad memory. A 2K-byte video RAM is implemented with four 1,024 by 4 bit static RAMs (MM2114s) and an advanced bipolar 7 by 9 LSI character generator. The character generator IC also contains keyboard and monitor interface circuitry that can accommodate monitors requiring separate video and sync signals (Ball Brothers) and those requiring composite video signals (Motorola).

By using a sophisticated bipolar LSI technique that combines I^2L, Schottky TTL and linear circuitry on the same IC, the DP8350 replaces most of the 30 to 40 MSI and SSI devices previously required to implement the timing and control block functions. Housed in a single 40-pin package, it provides an internal dot rate crystal controlled oscillator, 11 character generation related timing outputs, 12 bits of bi-directional Tri-State character memory

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addressing for direct interface to character memory. Three on-chip registers provide for external loading of the row starting address, cursor address and top of page system. The available set of video outputs includes cursor enable, programmable vertical sync. It also provides sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock and character generator program. The INS8285 character generator IC combines input address latches with a character generator ROM and parallel-to-serial shift register functions onto a single chip. As a result, keyboard scanning, in particular, is considerably simplified, because it is implemented only in software. Even the keyboard encoding is "computed" rather than "looked up" in ROM.

The ACE (INS8250) performs serial-to-parallel conversion on data characters received from peripheral equipment via a modem, and parallel-to-serial conversion of data characters received from the CPU — in this case an 8060. The 8060 can read the complete ACE status at any time during operation. Status information reported includes the type and condition of transfer operations performed by the ACE, as well as any error conditions. In addition, it includes a programmable baud generator that can divide the timing of the reference clock by devisors of 1 to (2^{16} - 1), and produce a 16X clock for driving the internal overhead penalty normally associated with the data communications link in a data terminal. These terminals which traditionally utilize a UART require a considerable amount of extra circuitry for running the communications link. The ACE now contains this circuitry on-chip. Also, in the CRT display block, the simple and straightforwardly designed CRT controller chip, with its direct memory access capability, supports the display block and eliminates the need for a DMA controller.

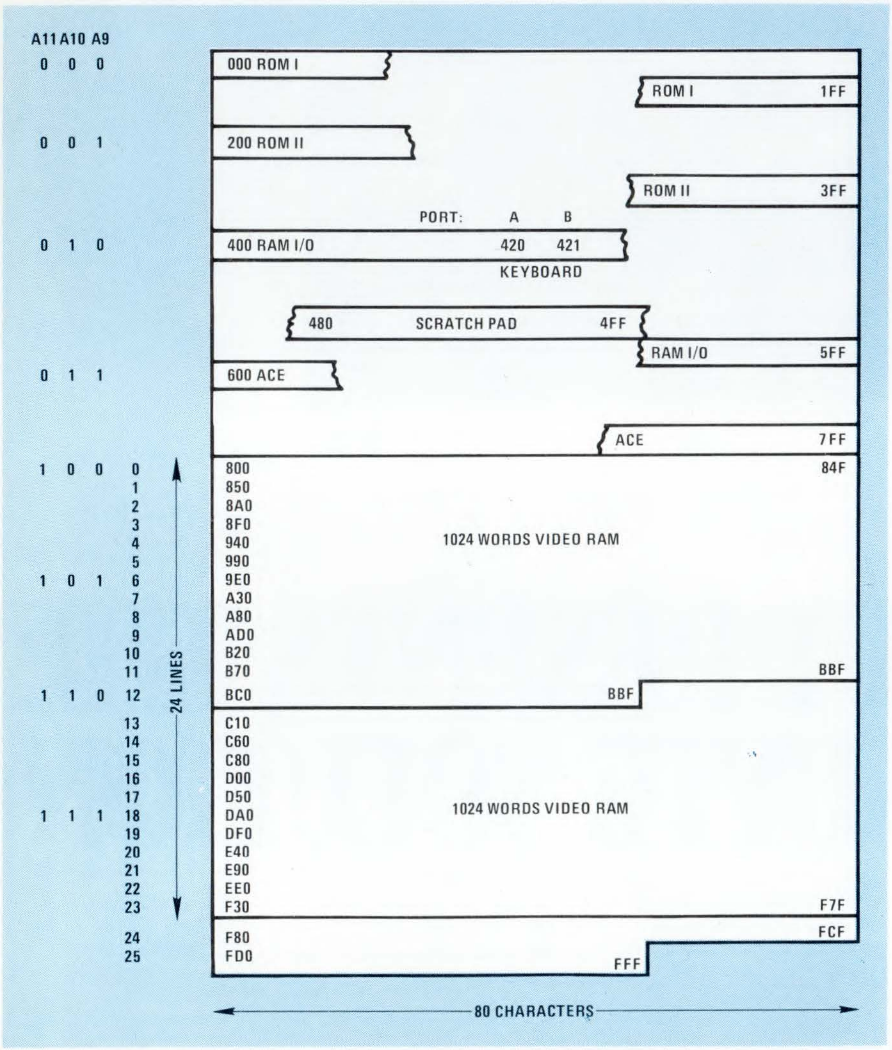

Fig 4 Detailed map shows how memory space is utilized. Video RAM is 80 characters wide by 24 lines high.

The design of this "not-so-dumb" terminal board also allows the incorporation of a standard teletypewriter-type keyboard with a two-key rollover.

System architecture

The Microbus structure uses the Tri-State concept extensively and makes designing this single-board data terminal much easier. The Microbus provides a universal system bus for communicating with the microprocessor, memory and peripherals. The bus structure consists of three functional elements: the data bus of eight bidirectional lines (D_7 - D_0) for parallel transfer of data and commands; the address bus of 12 address lines (A_{12} – A_0) that allow generating 4,096 addresses used for memory locations or peripheral device addresses; the control bus used for timing and control signals to govern data transfer. Common to most μPs, these signals are the generalized Read (RD) and (WR) strobes and are combined with the Chip Select signal (CS), set up by external logic, to control actual data transfer.

Because the data and address buses link the system together, you must define a priority scheme for their use. Experimental information indicates that any bus access with non-displayable data during video time shows up as a flicker on the screen. Giving the CRT controller IC first priority on the system buses eliminates this phenomenon. At character display time, the microprocessor is taken off the buses after the bus has gained access. It is also very important to service the I/0 channel quickly after receiving data to make room in the ACE receiver register for the next data word. Unfortunately this event is asynchronous and may happen at display time or when the microprocessor is using the bus for a keyboard scan. If the event occurs during display time, the interrupt request from the I/0 channel (ACE) has to wait until the current display cycle is complete, because the microprocessor has no access to the system buses. If the event occurs during microprocessor bus use, it only interrupts a keyboard scanning sequence or ASCII code generation. Both are relatively slow and therefore are low-priority events. It is easy for the program to come back and pick up the depressed keys on the keyboard after servicing the I/0 channel interrupt request, because a key is depressed a very long time (sec) compared to I/0 data handling (msec).

The combination of the Tri-State bus

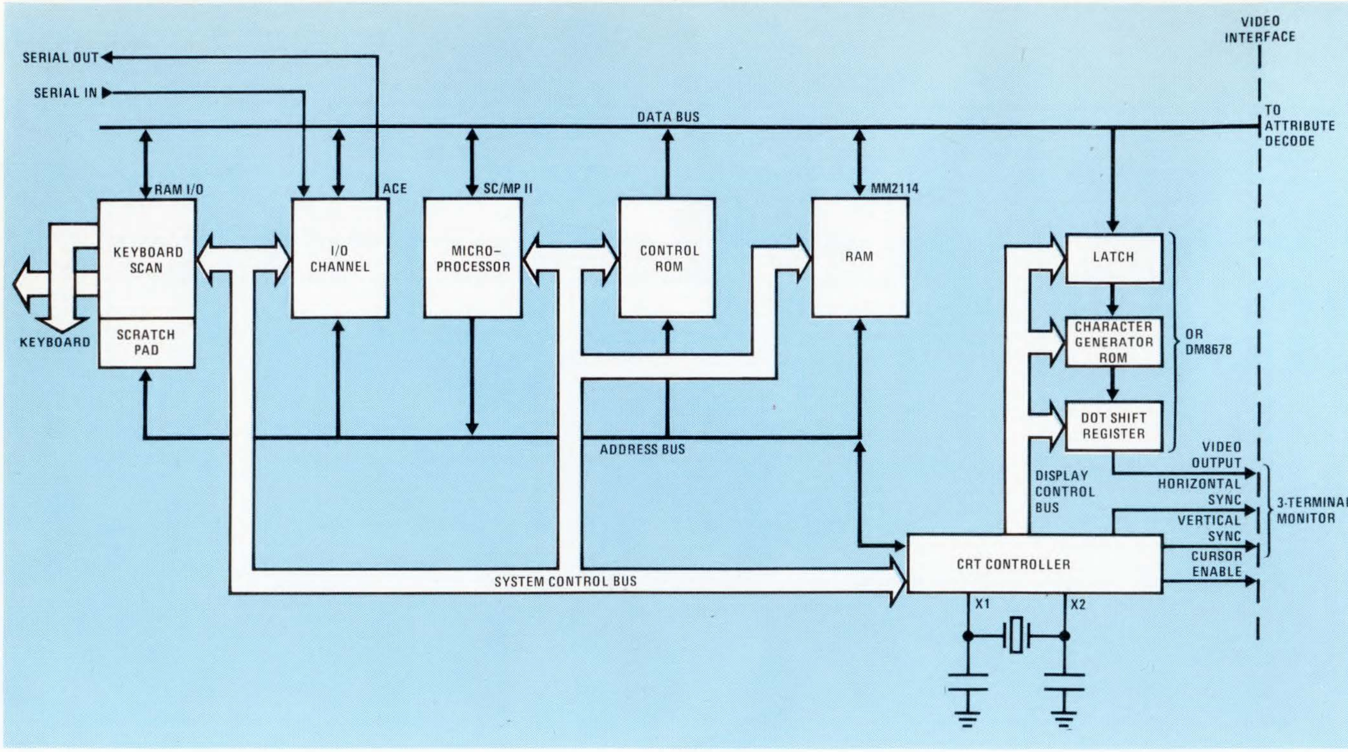

Fig 5 System block schematic shows a terminal that uses a line buffer and an address and data buffer.

structure and newer LSI devices, such as the CRT controller, makes possible a simple decoding scheme for memory address space utilization, in which the processor memory is partitioned into 500-byte pages. The detailed memory map appears in **Fig 4.** In addition, address bits 12 and 13, multiplexed on the data bus, are used to map 4K-byte pages. The first page is dedicated to processor peripherals and the other three to register loading of the CRT controller. The three CRT controller registers to be loaded are "top of page," "row start" and "cursor."

Some functions

Some of the newer LSI devices used in this design make possible a number of functions not normally associated with so-called dumb terminals. Two examples are scrolling and the ability to adjust the baud rate.

Scrolling The CRT controller may use one of several screen scrolling methods. The most straightforward one uses a rewrite of memory. It requires a long processing time and bus access is not feasible with the minimum hardware shown in **Fig 3.** For example, sensing when the CRT is scanning character row 24 and loading a new "row start" requires additional overhead circuitry. An alternative approach loads a new "top of page" address for each scroll and possesses the video RAM "wrapped around" when accessed by the CRT.

In top-of-the-page loading, the processor needs only to clear a row in video RAM and load one register in the CRT controller to perform a total screen scroll. The remaining problem involves the location of the scratchpad in the video RAM address space. The RAM I/O chip used for keyboard scanning and as a scratchpad RAM, solves the problem. The software programmers benefit from an additional capability: the keyboard and the RAM are addressable within the reach of one 9-bit index register.

Adjustable Baud Rate If you assume that the processor can access the bus only during the vertical blanking period and that the ACE interrupt service routine is executed in less than this time (1.3 ms), the system could process only one received data word per frame. Therefore, the processor's task consists of transferring the word from ACE to scratchpad memory, checking for terminal or control system functions, writing into the proper locations of video RAM, and checking the keyboard for Break (BRK) results in establishing 600 bps as the maximum baud rate. The processor must be able to access the bus during video time for improved communication speed.

Three of the 10 scan lines that make up a character row are blanked except during cursor times. Using two of these lines (no decoding required) for processor bus access during video time allows communication at 1200 baud.

Note that the frame rate in rewrite memory scrolling limits the baud rate. In top-of-the-page loading, the limitation is the real time required to execute the service routine. You can perform time calculations as follows: Estimate the execution time for a service routine with 100% availability of the bus as 1.3 ms. However, bus access is only granted during the time interval of three video lines in each character row — 192 ms. In terms of video time, 10 character rows are needed to finish the routine and to be ready for the next interrupt. Display time for 10 character rows equals 6.4 ms, which, in turn, is the time required for on 10-bit word. This rate translates into a 1600-baud maximum capability.

Some timing considerations

An unfortunate side effect, limited bus access, appeared on the single-board design of this not-so-dumb terminal. It had to be rememdied because it, in turn, affected the time-critical functions, such as scroll and high baud rate. A normal bus structure allows this limitation to occur, because all data handling devices require access.

Because the CRT controller performs the CRT display refresh function, it must have access to a memory containing current data for display. In previous configurations **(Fig 5),** this

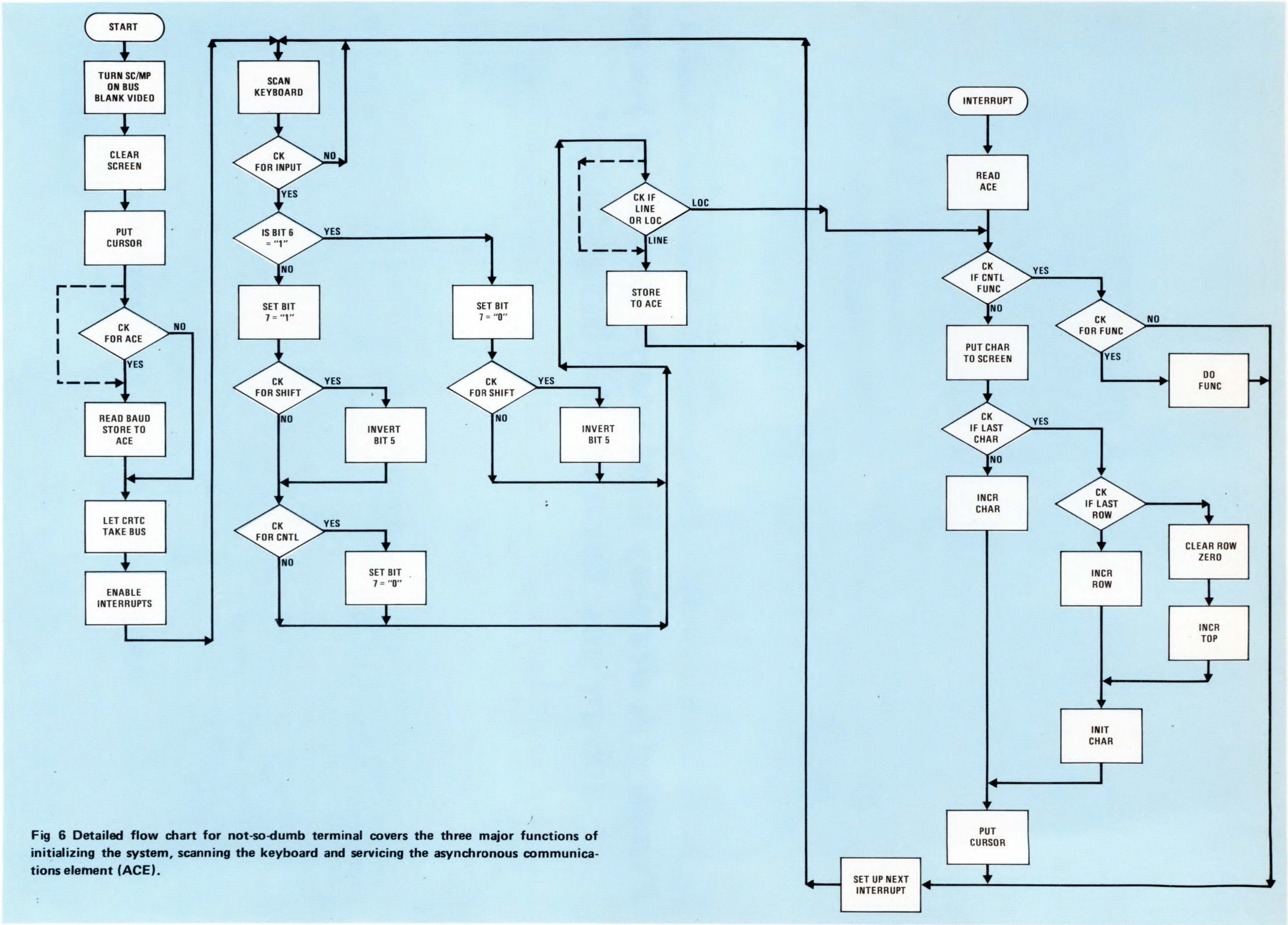

Fig 6 Detailed flow chart for not-so-dumb terminal covers the three major functions of initializing the system, scanning the keyboard and servicing the asynchronous communications element (ACE).

memory may be a shift register (an octal 80-bit line buffer) which is loaded at the first video line in a character row and then recirculated for the number of video lines in that character row. Such a line buffer allows the microprocessor access to the system buses for more than 90% of the video time. Consequently, removing the line buffer (**Fig 3**) gives the refresh circuit the needed direct memory access (DMA) during video display time.

However, taking the bidirectional data buffer and the Tri-State address buffer out of the system prevents the 8060 microprocessor on the not-so-dumb boad from updating video RAM or from using the scratchpad during character display time. Instruction fetch (ROM) and keyboard scanning are not affected. However, the removal of the data buffer and address buffer makes a well-oragaized time-sharing of the system mandatory.

Operating the system

When the system is initiated (power-up), the on-chip programmable baud rate generator is loaded with the desired baud rate (switch selectable). Depending on the data flow direction, stop, start and parity bits are appended or deleted in this block of the system. All control signals for the standard RS-232 interface parts makes the system meet standard electrical specifications for RS-232 and 20 mA current loops.

After the data is received from the computer, it is stored in the video RAM. The CRT controller refreshes the display at 70 Hz by sequentially addressing the video RAM; 1920 addresses are generated to fetch data for 24 lines of 80 characters. A 5×7 dot matrix block for each character displays the standard 64 character ASCII. Data enters from left to right, from top to bottom, until the screen is full. After that, upward scrolling, with top line overflow and newly cleared bottom line, takes place with line feed.

The processor scans the keys of the keyboard at all times. It translates any key closure into a unique code (ASCII) which is sent to the I/O channel for serial transmission to the computer.

During operation of the terminals, the CRT controller grants the 8060 μP bus access during blanked scanlines and vertical blanking intervals by logically ORing line counter outputs with the vertical blanking pulse and using this signal as a bus-available signal. Disabling the Tri-State address output holds the CRT controller off the bus. The 8060 then takes the bus as needed, by applying a logical "O" to the RAM address enable pin of the controller.

Sensing a signal at port A of the 8060 is used as an interrupt request input whenever received data is available in the receiver buffer register of the ACE. The interrupt service routine is executed during the blanking of the vertical and "inactive" video time as indicated previously. On the other hand, the keyboard is sensed for "any key down" (under program control) by reading port B of the RAM I/O chip. A positive result allows the keys to be scanned by a special sequence for key identification and coding.

System software

Software is arranged to provide a fast and effective service of the data communication link. Instead of idling the processor between data handling tasks, it puts the system to work scanning the keyboard and generating ASCII codes for the I/O channel.

Fig 6 contains a detailed flow chart of the software. It is set up to service these three major functions: initializing the system, scanning the keyboard and servicing the ACE upon interrupt request.

Initialization The video RAM is cleared and the cursor is loaded at the upper right hand corner of the screen. ACE is set up with the desired baud rate and the interrupt enable flag is armed.

Keyboard Scan The keyboard is first checked for any key down status. A positive status causes the keyboard to be scanned and the binary code (ASCII) to be computed by the program and to be read into the ACE.

ACE Interrupt When its receiver buffer is full, the ACE puts out an interrupt request. The 8060 immediately suspends keyboard scanning and reads the buffer register. The main portion of this routine checks incoming data for control functions and updates the video RAM and CRT controller registers. Note that the need for executing this routine is what limits high baud rates in data communications.

The bottom line

Implementing the circuitry of a video data entry terminal with the latest LSI chips gives the unit important advantages. First, the redesigned terminal uses only one circuit board instead of a number of them. Second, the PCB uses far fewer devices. And finally, the terminal provides more intelligence (capabilities) than the unit it replaces at a very competitive price.

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The Role of The Minicomputer in the Small Business Marketplace

The minicomputer is experiencing substantial growth. The estimates vary widely — from 20 to 35% per year — due partly to the market segment being reviewed (**Fig 1**) and how a minicomputer is defined.

One of the fastest growing portions of the minicomputer market is the so-called "small business system," which is growing at a rate approaching 40% per year. Certain portions of that market, such as desk-top computer systems are expected to grow as much as 90% annually.

The difficulty in obtaining accurate estimates of the minicomputer market, let alone the small business system market, should not be surprising since existing estimates are skewed due to a number of uncertainties, including: (1) lack of agreement as to what a minicomputer is, (2) a fast moving hardware and software technology, (3) the rapidly dropping price of minicomputer hardware, (4) the replacement of programming techniques by minicomputer, hardware techniques, (5) progress in programming techniques, which reduce software costs, (6) the degree to which microcomputers penetrate the traditional market for minicomputers (where a general purpose minicomputer cost in the range of $25,000 a few years ago, a microcomputer today can do the same job and cost only $2,000 to $5,000), (7) the degree to which minicomputer makers participate in the burgeoning microcomputer market as assemblers and manufacturers of board level and box level systems, (8) the degree to which semiconductor manufacturers integrate upwards from the manufacture of microcomputers to the production of larger systems, including minicomputers and (9) duplication and overlap in the gathering of statistics on computers, since manufacturers sell computers to other suppliers who then include them in equipment such as small business systems.

If the manufacturers and vendors of minicomputers and small business computer systems are a little uncertain about their definitions, where does that leave the systems integrators and designer or user who wants to purchase a minicomputer?

	MILLIONS OF DOLLARS			
	1977	1978	1979	1982
	8,035	9,842	12,303	19,620
Desktop Computers	150	262	460	1, 150
Small (less than $10,000)	2,655	3,800	5,320	9,800
Medium (up to $1 million)	2,730	3,030	3,360	4,470
Micros & Minis Total	925	1,274	1,635	3,001
OEM Micros	355	476	637	1,274
OEM Minis	570	798	998	1,727

Fig 1 Estimates of minicomputer growth

Micros, minis and superminis

A good starting point might be to define the term minicomputer and delineate differences between other types of computers, both larger and smaller. It's difficult to do this in a way that uniquely distinguishes it from other computers, since all computers are the same functionally.

While only a few year ago, a distinction existed between microcomputers and minicomputers, that distinction has become increasingly vague. At one time, microcomputers could be clearly differentiated from minicomputers, since the former were available on a single chip or at most a single board, were less expensive, not as fast and addressed less memory than minis. This gap has narrowed to the point where in many cases the distinction between minis and micros is one created by marketing.

Pricewise, although in general microcomputers are less expensive than minicomputers, there is overlap here as well. Where microcomputers and microcomputer-based systems are generally in the $1,000 to $8,000 price range, minicomputers and minicom-

puter-based systems are priced anywhere from \$2,000 to \$250,000. And at the high end, there is now a new entry in the market — the "super-mini" which is beginning to narrow the gap between minicomputers and mainframes.

In terms of performance, the mini generally outstrips the micro in terms of cycle time, instruction execution and throughput (**Fig 2**). But with adequate support chips, the microcomputer can approach the performance of a minicomputer — another area where the rule, if it still applies, is at least not quite precise.

	Cycle Speed (microseconds)	I/O transfer rate (megabytes/second)	Minimum add time for 2 digit # (microseconds)	Memory Capacity (Kilobytes)	Purchase Price (\$1,000s)
DEC PDP 11/45	16 – 124	0.3	3.8	0.3	38
DG Eclipse C/300	32 – 128	0.2	1.25	0.2	30.7
GA 16/330	4 – 65	0.45	2.5	0.78	4.0
Honeywell 6/36	8 – 128	0.65	1.5	1.9	5.6
IBM Series One	16 – 128	0.80	1.6	1.32	5
Interdata 8/16	16 – 64	0.75	2.66	0.75	6.25
Microdata 3200	4 – 128	0.35	5.0	0.4	9.63
Lear Siegler 1000	64 – 128	0.6			2.1
TI 990-10	8 – 1,024	0.75	6.0	3.6	2.2
Varian V-76	16 – 1,024	0.66	6.0	1.32	8.6

Fig 2 CPU characteristics of various minicomputers.

And where there were distinctions in terms of software support and the type of software available, as well as in bit structure and the amount of addressable memory, there no longer exists any good, concrete definitions which separate microcomputers and minicomputers.

Perhaps the best approach is to look at the problem somewhat simplistically, and consider a minicomputer as a CPU made by a traditional minicomputer manufacturer. Beyond that the user should choose a computer system on the basis of his requirements and his budget. To that end, some general guidelines are outlined in **Fig 3.** Remember, they are just that — guidelines — because there are exceptions at both ends of the spectrum.

Minicomputer in business

Small businesses are investigating the possibilities of using in-house minicomputers to replace time sharing or service bureaus and are finding that because of the low price tag, the small computers do so to an economic advantage.

The cost of a minicomputer-based business system is often less than a single clerk's salary. A typical system could have several terminals for data input, magnetic tapes or disk devices for storage of data, and printers for hard copy output. And because it is time-consuming to enter programs and information via a keyboard terminal, often there is also a card reader and punch card or paper tape device for loading and maintaining the programs. A sophisticated business system, such as a communication minicomputer configuration with mulitple disks, printers and communications devices costs between \$100,000 and \$200,000 at a minimum. **Fig 4** shows such a system.

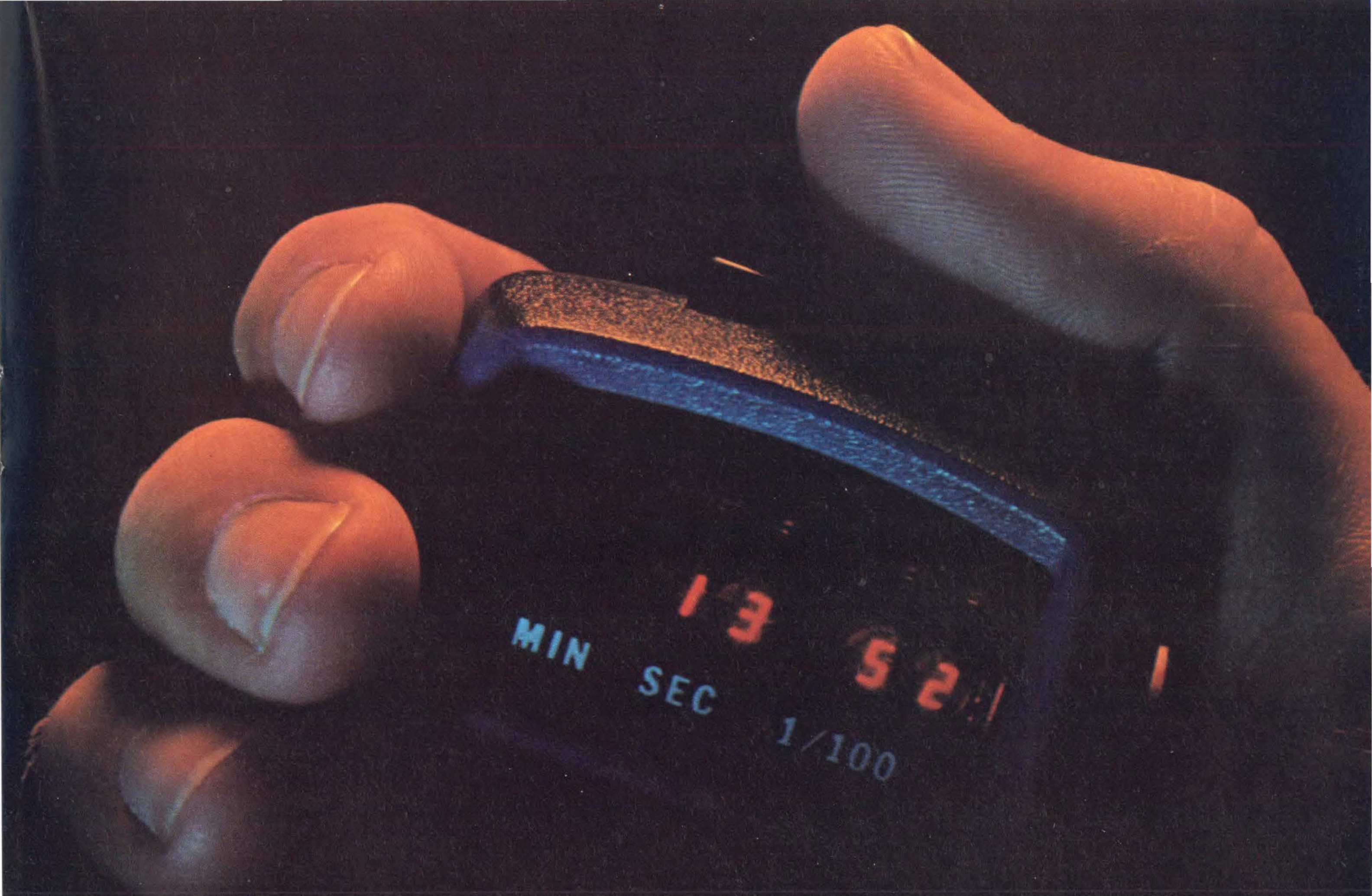
A more common configuration for the small business environment is a simple stand alone system based on a minicomputer, with one terminal, a CRT/keyboard display and a disk file that can store up to half a million characters of data. It has a printer terminal as well. This simple system, illustrated in **Fig 5**is basically an information retrieval system for use in such applications as personnel, sales reporting, management information and inventory control. It can be programmed to store, update, select, retrieve and display personnel records, or to select and display or print a list of employes with a particular type of experience, or salesmen who have reached a certain level in sales.

The difference in capability between a general purpose minicomputer and a small business computer system is the lack of flexibility of the latter. Indeed, the small business computer is in many respects simply a scaled down, customized version of the minicomputer, since it is common for manufacturers to design the systems for specific classes of business applications. As a result some of the capability needed for applications other than the strictly business-oriented ones are lost. The operating system that controls the operation of the computer is also modified to handle heavy input and output duties, also at the sacrifice of other capabilities.

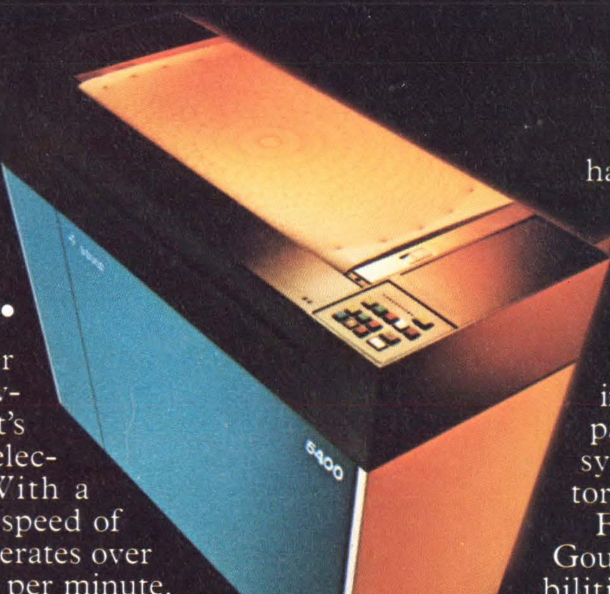
Such computers also perform basic business operations such as general accounting, accounts receivable, payroll, accounts payable, inventory control, general ledger and so on through the use of the packaged software generally supplied with the systems. They are generally easy to use, with first time users frequently installing a packaged application in a very short period of time without systems analysts and programming that usually accompanies such installations.

Buying and tradeoffs

Where should you buy and why? There are tradeoffs to consider. Where does the businessman start, if he has made up his mind to computerize his operation? The most obvious thing to do is go out and buy all the elements he needs, piecemeal. In most cases, however, the user will have to pay more than he really needs to. The small to medium OEM, because of volume, may gain some price advantage in buying piecemeal, but he and the single unit user will usually have to pay a somewhat higher overall system price, if system integration, support, and service are taken into account. Also, compatibility problems may occur in integrating system components from different manufacturers.



An E-sized drawing in 13.5 seconds.



Gould's 5400 printer/plotter will produce an E-sized drawing in 13.5 seconds. That's faster than any competing electrostatic printer/plotter. With a paper width of 36" and a speed of 3.25"/second, the 5400 generates over 48 square feet of hardcopy per minute.

Designed for applications where fast turn-around and high throughput rates are important, the 5400 is ideal for computer-aided-design, seismic data plotting, and business graphic applications such as PERT/CPM, Gantt, and others.

Gould's patented negative-pressure, closed loop toning system ensures high contrast dry hardcopy even at the maximum plotting speed of the 5400. Print resolution is 100 dots per inch, horizontal and vertical. In addition, a staggered image head produces overlapping dots for high contrast images. A user-oriented control panel features a unique LED system for continuously monitoring paper supply.

For additional information on Gould 5400 printer/plotter capabilities, software, interfaces and special application packages contact your Gould representative. Or write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, Ohio 44114 (216) 361-3315. For brochure call toll free: (800) 325-6400, ext 77. In Missouri: (800) 342-6600.

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	Micro	Mini	Super Mini
Word Size	8-bit	8-, 12-, 16-bit	24-, 32-bit
Instruction set	⩾100	⩽100 instruction	⩾150 instruction (upward compatible to mini's)
Memory Capacity	4K – 512K	8K – 512K	⩾512 bytes
Address Range		1 m byte	1 G byte (30 bits)
Instruction execution increases across the range			
Arithmetic	Fixed Point H/W	Fixed Point (Std) Floating Point (Opt)	Fixed & Floating Point Hardware
	–	–	Double Precision Arithmetic
	Micro programmable (not by user)	Micro programmable	Micro programmable
Cycle Time	100 ns	100-1500 ns	200 ns
Applications	Hardware Control small business applications	Small Scientific business applications, process control	Large Scientific and business applications
	Bus Architecture	Bus Architecture	Bus Architecture
Internal Bus Speed	10-100K bytes/sec	M bytes/sec	30M bytes/sec
Interrupt System	Single Interrupt	Single Interrupt or vector	Faster than mainframe

Fig 3 General minicomputer guidelines.

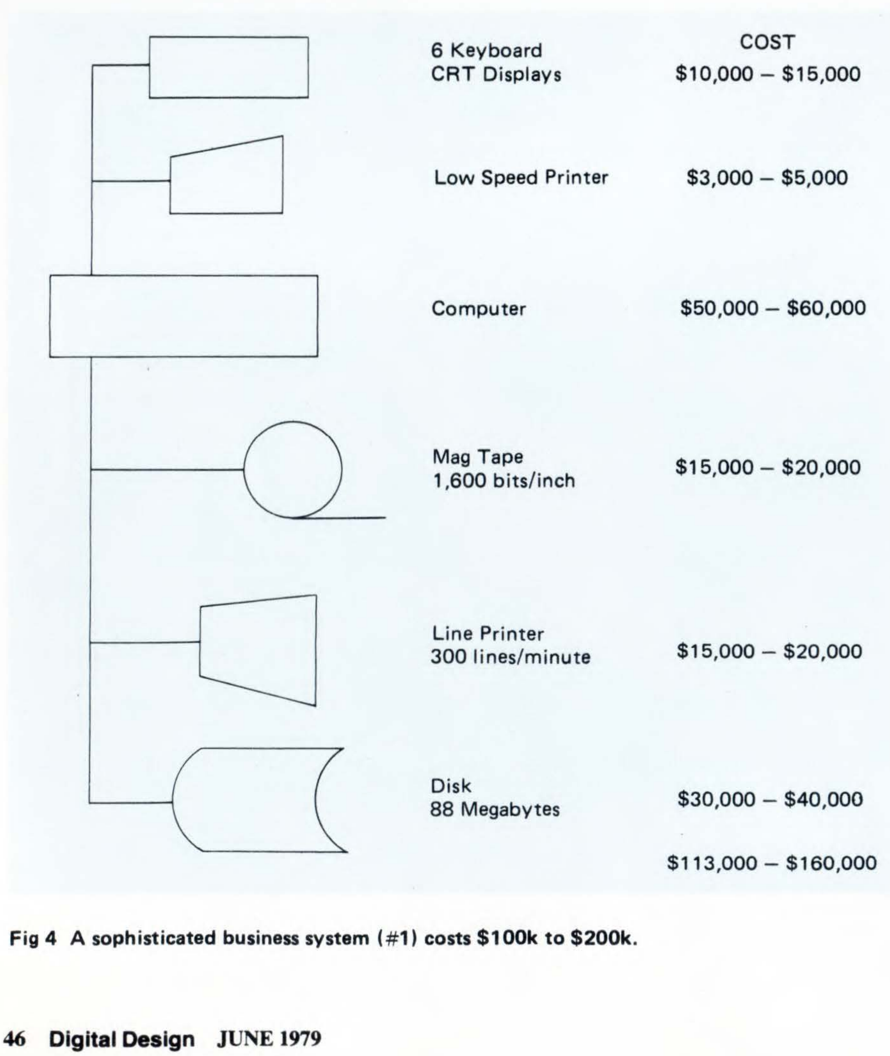

Fig 4 A sophisticated business system (#1) costs $100k to $200k.

Except for the most sophisticated and computer-wise businessman, the best approach is the total system approach, and for this the potential user has his choice of about 200 sources for this kind of product. Generally, they fall into four broad categories.

First, there are the large computer manufacturers such as Burroughs, NCR, Sperry Univac and IBM. They offer small business computers as a part of a very broad range of computer products. Second are the major minicomputer manufacturers, such as Digital Equipment Corp., Data General, General Automation, Computer Automation, Hewlett-Packard, and Lear Siegler. These companies supply minicomputers for small business applications, and also address the general purpose minicomputer market directly. And with the exploding market for small business computers, they are packaging the minicomputers with peripherals, and applications software and selling them as complete systems. Included with such systems are high level software languages such as BASIC, FORTRAN, PASCAL and COBOL that allow the user to program his own business applications.

A third group of suppliers of small business systems consists of systems houses, software houses, and service bureaus. They do not make minicomputers, but bring together computers and peripherals from many vendors, supply the application software, and sell the complete package. The appeal of this approach is that here the vendor supplies a complete turn-key system relieving the users of the hardware/software integration task.

A fourth group consists of semiconductor firms who specialize in manufacturing ICs and microprocessor chips that are used in both microcomputers and minicomputers and who have now integrated upward to supply full applications-oriented systems. Because of the tremendous investment in software and support required, they sell their systems to the third group, where the complete system is fashioned from the barebones equipment.

In choosing a business computer system vendor, several factors should be taken into consideration. First of all, the stability of the company offering the product. A minicomputer will operate for many years, so realistically speaking, a vendor should be selected who is capable of handling the needs of the users company or application for at least three to five years. Other things should be considered in the choice of

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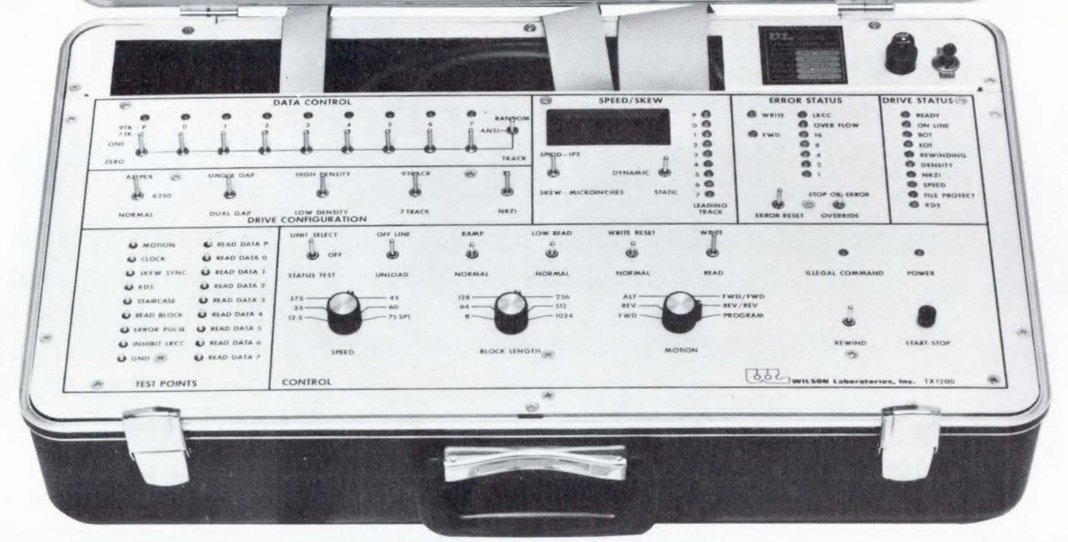

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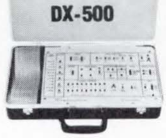

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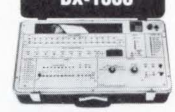

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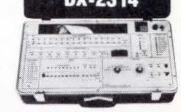

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The F6802 microprocessor. It sends your design problems to the minors.

And that's where they'll stay, thanks to this enhanced version of the F6800 central processing unit. The F6802 offers an on-chip power-on reset function, on-board clock for easier use and on-board 128 x 8 RAM with options of 8-byte or 32-byte power-down. Now you no longer need an additional RAM with battery backup systems.

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The F6846 is a user-defined ROM-based peripheral element. It features 2K x 8 ROM, a powerful programmable binary timer, and eight bidirectional input/output ports on the same circuit. It's also F6800 series bus-compatible.

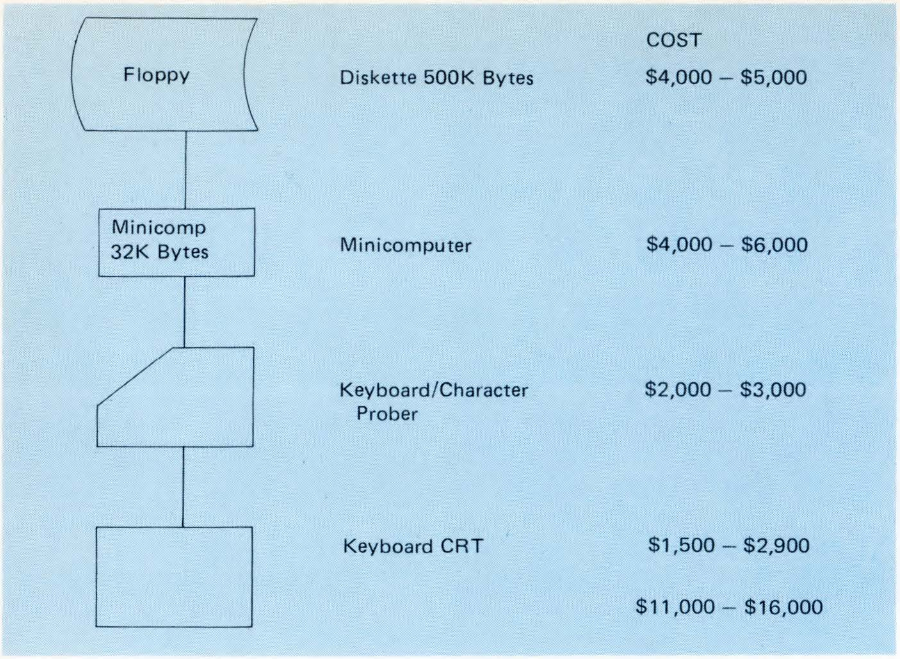

Fig 5 Simple standalone business system (#2) has a minicomputer and one terminal, plus printer and stores up to 0.5M characters of data.

the company: (1) the number of applications and software development engineers, support personnel; in short, can the companu really support the potential customer's needs? (2) company knowledge of the user's industry; (3) will the company customize software? (4) does the company own the source code; if not, company engineers cannot customize or even make changes in the software when necessitated by changes in the user's industry; and (5) does the company provide hardware and software service support or is this available through a third party?

Many of the small OEMs who integrate minicomputer hardware and software into turnkey systems also provide on-site hardware service — either on their own or through contracts with the manufacturer — and complete software support. This is one of the best sources for the unsophisticated user. It provides one-stop shopping for hardware, software, service and support. And most of these small OEMs are dedicated to one, or a few, vertical markets, so it's knowledge of a a particular industry will be good.

Comparing and choosing

Comparing and choosing the right minicomputer involves making many comparisons. Minicomputers are not created equal. They have different architectures, different instructions and different capabilities. One of the most important parameters used to compare performance is the speed systems. And as will become clear there is an enormous range of capability even when this single parameter is analyzed.

Minicomputers operate with cycle times in the 400 nsec to 2 μsec range. More important is the instruction execution time. This is evaluated by means of a standard benchmark program. The benchmark in this case is searching an 80-item string of characters for a given character. Fig 6 compares several commonly available minis and micros running this benchmark. The importance of such benchmarks and their results varies with the application the minicomputer is intended for. If the user has no other peripheral than a teletypwriter, and all the programs are heavily I/O oriented, then almost any computer will do. If the job is "number crunching" and very little I/O, then instruction execution time is all important. And the benchmarks chosen will vary depending on the type of calculations to be performed. If the user requires BASIC of FORTRAN in his application, it is important to remember that the speed with which these high level computer languages perform their job is a direct function of instructon speed.

Another key consideration in comparing minicomputers is in the efficiency of the system in the use of memory. That is, to perform a certain function, how much memory is required. In one minicomputer, all instructions may be 16-bit words, in another both 16- and 32-bit. The relative efficiency in terms of the number of eight-bit bytes for the benchmark chosen is shown in Fig 7 for the various minicomputer and microcomputers chosen. There are numerous other differences between the various minicomputers. For the small business computer user, the best way to make the evaluation is to list the various features of the system that will be important, assign them a value and then score the various systems. As far as the minicomputer system itself is concerned, the factors to be considered include: how suitable it is for the user's purpose, price/performance, simplicity, compatibility, ease of installation, training required and documentation available.

Software considerations to assess include: suitability to the problem, modularity, ease of revision, ease of maintenance, versatility, report capacity, printing capacity, file capacity and record keeping capacity.

The hardware needs to be looked at in terms of: suitability for the job, performance, reliability, number in use, in-house experience, ease with which configuration changes and manufacturing support.

Choosing software

When purchasing a minicomputer system, the software evaluation should be very thorough. Software is basically a labor intensive product. Therefore as labor costs rise, the price of software can also be expected to rise. With this, the small business computer user is forced to use more or less prepackaged

Instruction Speed Benchmarks

CAI LSI-3/05	1248.75 μsec
Interdata 6/16	390.5 "
MCS 6502	440.0 "
PDP-8/E	668.8 "
MC 6800	807.0 "
Fairchild F-8	899.0 "
Nova 800	252.6 "
8080	3546.0 "

Fig 6 Comparison of several commonly available minis and micros.

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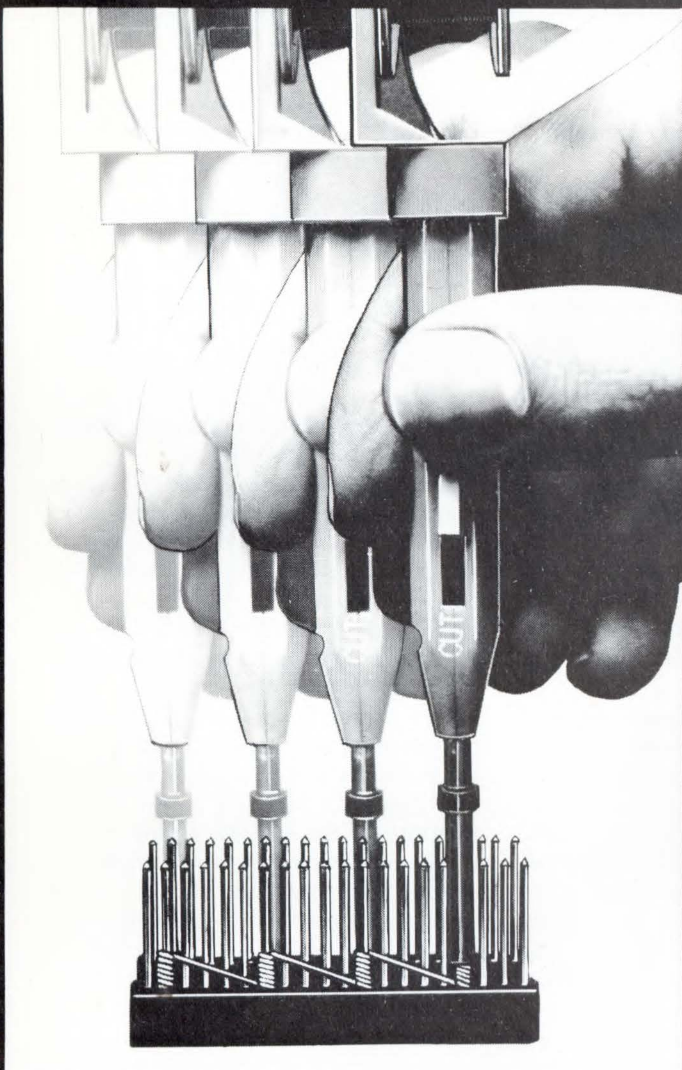

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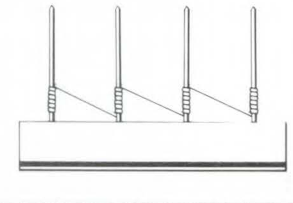

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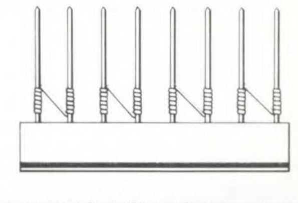

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PDP-8/E	45
MC 6800	16
F-8	13
Nova 800	42
8080	18

Measured in number of 8-bit bytes required.

Fig 7 Memory storage benchmark comparisons.

software instead of customized software to reduce the cost of applications programs.

Although application software is not the strong point of most minicomputer suppliers, several alternatives are available to the first time small business computer user, including industry application programs, accounting packages, and turnkey packages. As an aid in marketing, most small business computer vendors supply basic industry application programs, which can perform the main functions for companies in a number of specific industries.

Vendor support varies. Some companies do not make modifications. Other vendors and almost all systems houses assume that additional programming will be required and offer assistance.

Most suppliers of small business computers provide a number of programs for standard accounting applications, including general ledger, accounts payable, accounts receivable, payroll, and others. Some companies have a library of several hundred accounting packages, and are usually available for either a single one-time charge or on a monthly rental basis. Others are available at no charge.

Still another alternative is to have a systems house provide the entire system hardware as well as software — a turnkey system. The packaged software approach helps the new business computer system user to get important applications on his minicomputer in a short ime, at a relatively low cost and with complete certainty of success.

Reliability, maintenance and life expectancy

Minicomputers, in small business applications, require extreme reliability. But reliability depends on the application. In one, it means the system will operate on a continuous basis. In another, it means no long periods during which it is not available.

In general, though, studies of downtime indicate that hardware problems account for only 25% of the system failures. Fig 8 illustrates the mean time between failures, for the computer, the system itself with no redundancy and the system with redundancy. To a large extent as the chart show, hardware reliability can be built in, through careful design initially, extensive testing prior to introduction, and in-house testing by the manufacturer and vendor. The majority of the reliability problems in minicomputers are software related — about 75% of the cases. Some are due to program bugs, and some due to a failure of the computer's operating system in allocating and scheduling internal memory and other resources.

The key to reliability, however, is maintenance. If properly maintained, a small business computer system's lifetime is "forever," and will only be obsoleted by the user's needs and technology advances.

		MONTHS TO FAILURE		FAILURES PER YEAR
	MTBF (hrs)	7 days/ 24 hr. day	5 days/ 8 hr. day	7 days/ 24 hr. day
Computer with 28K of memory	3,500	4.5 – 5.0	20 – 21	2 – 3
Computer system with no redundancy	475	0.60 – 0.70	2 – 3	18 – 20
Computer system with redundancy	2,200	2 – 4	10 – 11	3 – 5

Fig 8 This illustrates MTBFs for the computer and system with/without redundancy.

As a result, maintenance is one of the most important factors in the selection of a vendor.. There are three approaches: third party, direct service, or the customer providing his own service.

The advantages of third party maintenance are broad coverage, no initial and ongoing investment in people, no investment in test equipment by the user. With direct service, technicians have more specific expertise because they only work on one manufacturer's product. And if the installation is large enough, the small business system maintenance can be amortized over the total product base. Result: less cost to maintain per unit for the customer. The disadvantges to this approach however are cost and lack of broad coverage. The last option, the customer providing his own maintennce, is, most of the time, not feasible, especially for the relatively inexperienced small business computer user. Among other things the initial investment in people, training, test equipment and spare parts would dwarf the cost of the system itself. And, in any case, the user could not provide adequate maintenance.

The future

Minicomputers are not only impacted by advances in intergrated circuit technology, but by developments in peripheral hardware and software, also. Over the next few years, we can expect to see advances in processor and memory technology which will increase the capability of minicomputers while at the same time reducing cost.

Specifically, memories can be expected to become more dense. 64K ROMs were introduced last year and random access memories of the same density this year. In the nest two to three years, 256k to 1 magabit chips will emerge, depending on process technology. In addition, fixed refresh will be replaced by pseudo-refresh, allowing the less expensive dynamic RAMs with on-chip refresh to ape and replace more expensive and slower static RAMs. The standard memory cycle of 200ns will be reduced to less than 100ns with the end result being a lower cost/bit for faster more efficient memory.

Processor speeds will increase from about 10 MHz now, to 15MHz, partly due to the use of faster schottky MSI circuitry, as well as high speed bit slice bipolar microprocessors.

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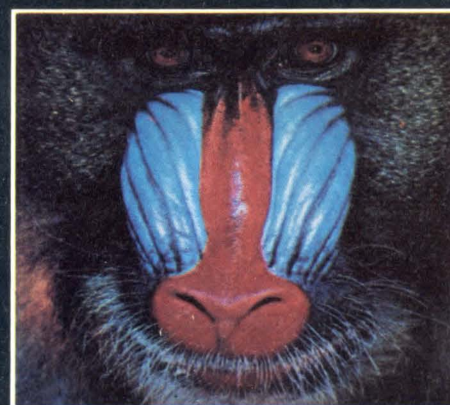

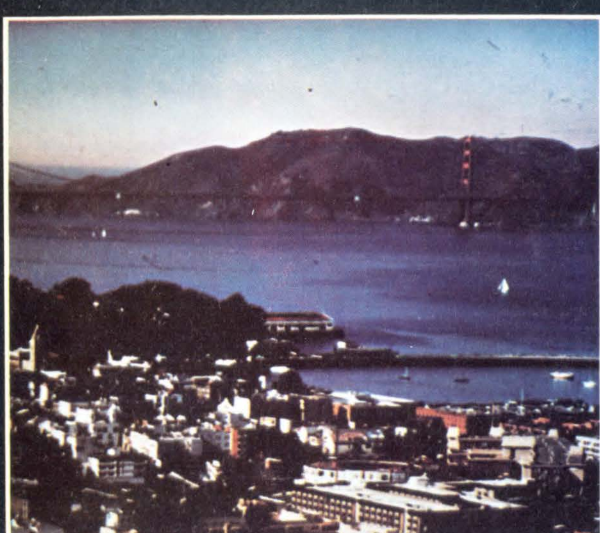

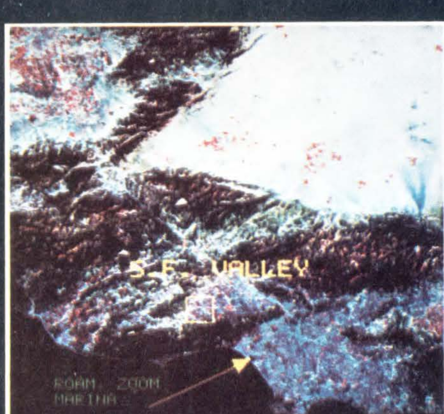
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Quantitative Evaluation of Software Copy Displays

Dr. Harry C. Andrews, Vice President
Comtal, Pasadena, CA

As digital image processing systems proliferate and exploitation facilities become commonplace, more and more reliance will be placed on results obtained from real-time interaction with softcopy displays. The repeatibility of specific scenarios and resulting visual processes at such work stations necomes particulartly important, and, consequently the need exists for a means of quantitative evaluation of such softcopy displays. This specification, then, is motivated by the desire to generate a testplan, implementation procedure, and experimental results directed at quantitatively evaluating high resolution digital display devices operating in a visual digital real-time mode for stationary imagery. The procedure concentrates on measurement techniques strictly from the display surface, does not require access to electronic signals, and couples the ground truth of computer generated test charts with absolute light level measuring devices to quantitatively evaluate the display system.

The test procedure described herein is based upon the assumption that the display system will be optimally adjusted only once prior to the data gathering aspects. Thus the device will be optimized with repect to gun bias, contrast, brightness, etc. parameters once and then left in such a state for all subsequent measurements.

Measurements

There are a variety of measurements desired from the test plan, some of which are listed below:

Astigmatism: This defect refers to the spot size, shape and orientation and its changes as it moves around the monitor. Traditionally, monitors will be tuned up to have optimal spot characteristics on axis, but poor performance elsewhere. This performance will inherently degrade the point spread function as a function of position, and as such, will manifest itself in the spatial frequency measurement portion of the test plan.

Brightness-Shading: Quite often the absolute brightness changes considerably across the face of a display even with a constant amplitude modulation signal applied. Such defects are referred to as shading or vignetting. The test plan explicitly addresses measuring the degree of degradation due to shading.

Contrast Ratios: Here contrast ratios will be measured as a function of spatial position and reported in percentage of depth of modulation. Various spatial frequency modulation patterns are presented in the computer generated test image to provide depth of modulation measurements as a function of both absolute modulation via COMTAL function memories and spatial position.

Geometrical Distortion: This is a defect which is unavoidable for non-flat faced displays. In addition, measurement of geometrical distortion is often difficult because it requires an external geometric reference for comparison.

MTF-PSF: This is probably the most important measurement to be made by this test plan for it defines the response of

the display as a function of spatial frequency. Indeed, with the cost of digital fast access storage, it is illogical to waste the effect of high resolution storage with a low resolution display. The modulation transfer function measurement (MTF) is really a point spread function (PSF) measurement

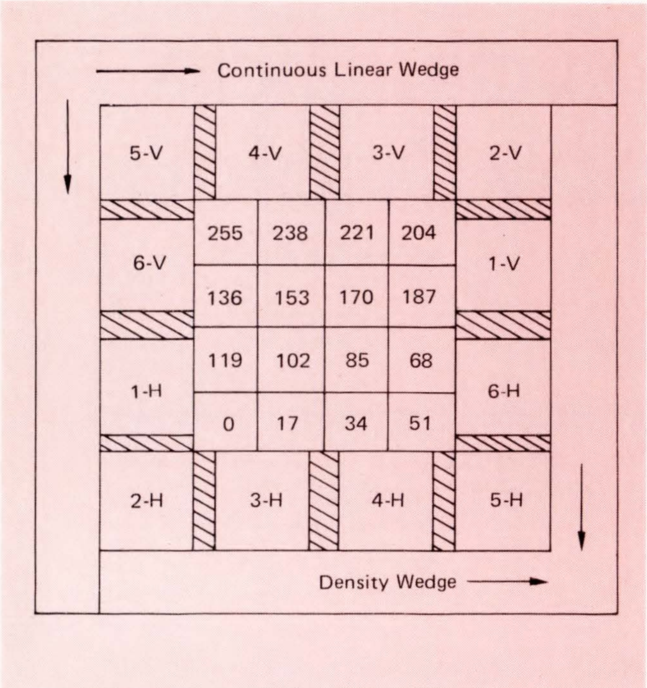

Fig 1 256x256 Microstructure of the test image. 1-V = 1 pixel on, 1 pixel off in the vertical

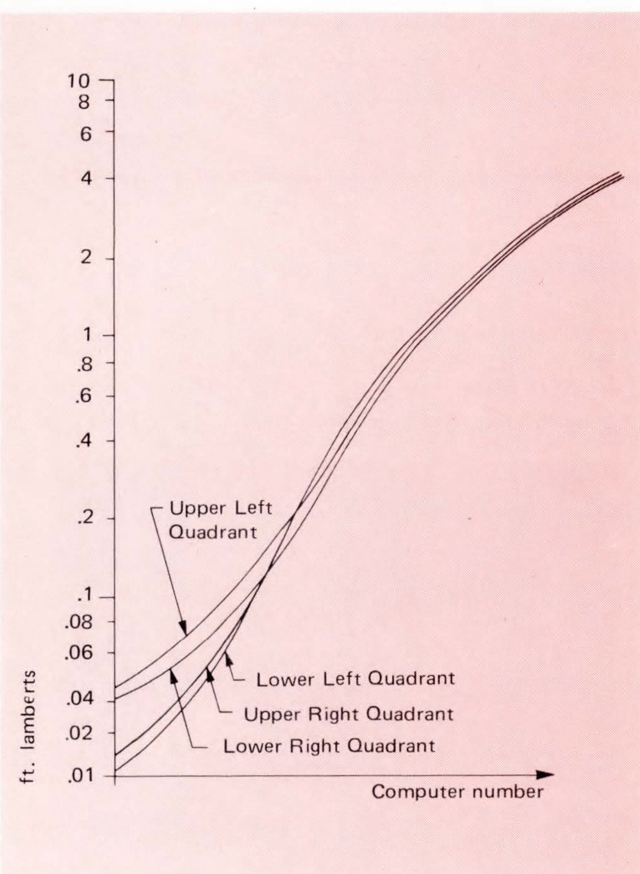

Fig 2 Brightness Linearity for four monitor quadrants

because it is clear that the display will be a space-variant device. Specifically MTF implies a "Fourier" type of measurement which in turn implies a space invariant MTF. In fact we expect the MTF will be measured in terms of percentage depth of modulation and one might expect this measurement to also be a function of the absolute modulation being applied to the display.

Phosphor Persistence: This characteristic of display tubes is of interest only if one is concerned with nonstationary imagery (i.e. real-time TV versus single images displayed at TV rates). However, for long persistence phosphors, flicker may be less noticeable. In addition *wide-angle* photometers cannot be used for MTF measurements via electronic signals.

Z-Axis Linearity: This measurement is of considerable concern in quantitative evaluation of the display devices as it addresses the brightness nonlinearities inhrent in wide dynamic range displays. Unfortunately the Z-axis nonlinearities will also change with position, and consequently a space variant Z-axis linearity test has been devised into the test image. Linear (rather than logarithmic) values are presented to the display and absolute light readings will be taken off the monitor. The curves, as a function of position, resulting from this test, can then be used to judge the linearity of the monitor.

Test chart

The test chart is designed to provide the measurements discussed in the previous section in as complete a fashion as is possible obtaining positional, frequency, and brightness information in as few a set of measurements as is reasonable. **Fig 1** presents the 256×256 substructure of the test image in which basic cycles as well as amplitude patterns are presented. Two outside edges are a 16-pixel wide intensity wedge with 1 pixel long intensity values ranging from 0 through 255. The remaining two edges are a 16 step 16×16 pixel logarithmic wedge. The center 128×128 portion of the section is divided into 4×4 regions in which 16 unique constant brightness amplitudes are presented for Z-axis and absolute brightness linearity measurements. (Naturally the wedges could also be used for this test but it would probably be too tedious to measure 256 values on the monitor.) The remaining portion of **Fig 1** is broken into 12 48×48 pixel squares separated by zero background (crosshatched) intervals. These squares are labeled 1-H through 6-H and 1-V through 6-V referring to the number of pixel replications per half cycle of horizontal or vertical slits. Slits rather than checkerboards are utilized to facilitate possible *slit* photometer apertures for maximum signal to noise measurements. These 12 squares can be modulated with COMTAL function memories to produce any desired ground truth computer generated depth ofmodulation values for complete specification of the display. For a 512×512 system, the test image is replicated 4 times and for a 1024×1024 system, the test image is replicated 16 times for space variant measurements.

Evaluation equipment

Many different types of equipment are available to perform the required measurements on the display test image. The general approach used in the selection described here is to simplify all measurements to reduce operator error and fatigue.

Notice the consistently high depth of modulation values for the "2 pixel on 2 pixel off" cases. At 25%, 50%, and 75% modulations, these values are consistently greater than all other points in their respective curves. This phenomena is due to the inherent 2:1 raster scan interlace technique of U.S.

For the measurements, a Photo Research Spectra Pritchard Photometer System, Model 1980A was used. The complete system consists of a Model 1980A-OP optical head, a Model 1980-CD photometer control system and LF-19 four element supplementary lens. This system provides calibrated measurements with a wide dynamic range and a direct digital readout. No clumsy conversion factors are needed to obtain the units. Alignment on the measured area of the CRT is very easy because the surface is viewed directly through selectable apertures to a photomultiplier system, and apertures much smaller than single pixel sizes can be used. Another major feature of this device is that it can be readily adapted to color display measurements. Filters are available for tristimulus measurements and other spectral characteristics. The Photo Research system can easily be used to measure luminance values in foot-lamberts for comparison of all the factors mentioned previously in the application note. The minimum spot measurement size of 0.02 mm is much smaller than the single pixel spot size of 0.3 to 0.4 mm expected from the display. **Fig 3** shows the experimental set up of the Photo Research equipment in position for monitor evaluation.

Table I

DEPTH OF MODULATION	COMPUTER NUMBER
25%	063
	64,127
	128,191
	192,255
50%	0,127
	64,191
	128,255
75%	0,191
	64,255
100%	0,255

Experimental results

The test equipment described in the previous section was utilized to quantitatively evaluate the COMTAL 8000-S Processing System. The evaluation procedure takes approximately 8 hours to obtain the results described in this section. However for the purist, additional measurements would be necessary for evaluation of the space variant nature ofthe PSF on the display surface as well as any geometrical distortion.

There are two coupled aspects of the evaluation procedure which must be emphasized. The first is the Z-axis brightness measurement and the second is the modulation transfer function (MTF) measurement. The two measurements are coupled together in the sense that for repeatability it is necessary to match the Z-axis curves prior to making MTF measurements during pre-test monitor set-up. In fact once the system is adjusted for a given brightness curve, such adjustment must be maintained (at least not re-adjusted) during the MTF measurements, thus the inherent coupling between the two tests.

Brightness linearity: This test was developed for the four different quadrants of the display using the 16 different grey values in the center of **Fig 1**. The four different quadrants were measured to evaluate uniformity of brightness linearity over the surface of the monitor. The measurements taken were in absolute foot-lamberts providing greater than two orders of magnitude in dynamic range. A three degree circular aperture was utilized and the large dynamic range of the system required various neutral density filters at the higher extremes of the display. Because of the large dynamic range, the experimental results are presented on semilogarithm paper. **Fig 2** presents the results of this experiment in which the four curves (representing four different monitor quadrants) are superimposed together. There is excellent consistency over the brightest 1-1/2 orders of magnitude dynamic range with some deviation at the very low brightness regions. This would be expected as noise measurements and stray reflections will begin to dominate at such low light levels. It is impossible to compute an approximate gamma from these curves by measuring the general slope of the results in **Fig 2**. Bearing in mind that this is the gamma of linear computer number *in* versus log brightness *out*, we find a slope of between approximately 1.20 and 1.45. Such parameter is probably not of too significant a value as the curves tend to be at a variance from straight lines. The solid consistency of the upper portion of the curves over the four different quadrants is indeed encouraging from a stability view point and it is this stability that lends credence to the resulting MTF curves developed below.

MTF measurements

A very complete series of MTF measurements are described herein, but due to time limitations only one quadrant was evaluated. Both horizontal MTF and vertical MTF curves are developed, consistent with the test image of **Fig 1.** The depth of modulation technique is utilized here with maximum and minimum readings defining a particular point on the curve. To place the curves in a "percentage depth of modulation" framework, the (maximum - minimum)/(maximum + minimum) reading was calculated for pixel cycles of 1 on 1 off, 2 on 2 off, 3 on 3 off, 4 on 4 off, 5 on 5 off, and 6 on 6 off. These modulation values are "constant on constant off", with absolute computer numbers being defined by the COMTAL function memory settings. Because of the wide versatility of ground truth computer modulations available with the function memories, four different modulations were developed. These are listed in **Table 1**. From the table it is apparent that 10 different curve result both for the vertical and the horizontal directions.

Fig 3 presents the results of the measurements taken in the direction of the raster scan to measure vertical MTF. Both 100%, 75%, 50%, and 25% modulation curves are presented in the figure. Probably the first apparent observation from these results is that at the greater modulations, there exists greater roll-off at the higher frequencies. This would naturally be expected as the stronger signals would cause greater mixing of light between the "on"and "off" stages of the display. Other immediate observations include the fact that at lower modulation signals, the absolute depth of modulation drops proportionately (as would be expected) but the curves remain much flatter (which is desirable).

Fig 4 presents the results of the measurements taken in the direction across the raster scan to measure horizontal MTF. Again 100%, 75%, 50%, and 25% modulation curves are presented in the figure. The general observations of the previous paragraph hold here as well, with the greater roll-off occuring at the greater modulated signals. An additional observation should be made from these from these curves.

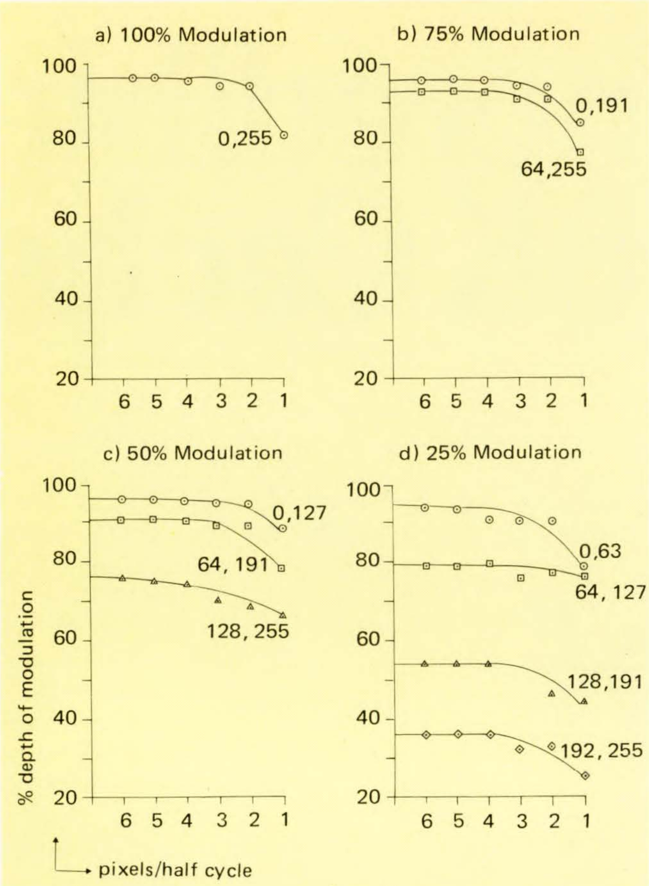

Fig 3 Vertical MTF Curves (along raster line)

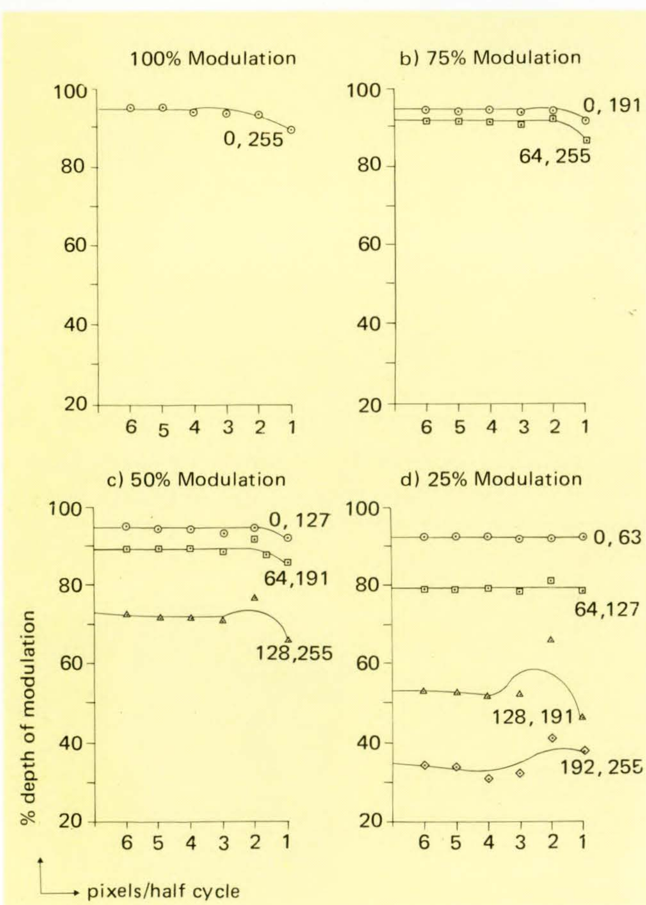

Fig 4 Horizontal MTF Curves (across raster line)

television systems. As such there exists an inherent, and rather strong, modulation due to this rater interlace display which clearly should be detected by our softcopy test procedures.

Conclusions

Although a large number of detailed objective measurements have been described in this specification, these factors by themselves may not be sufficient to completely judge display system quality. It may happen that two systems are objectively very similar, yet a subjective human evaluation may show well defined differences. A brief description of the human visual system and its responses for photographic purposes off of CRT displays was discussed in the Application Note by Dr. Frei. In brief, the human visual system is highly sensitive to sharp, well-defined changes in contrast, but is very poor at judging absolute brightness. The eye is also roughly logarithmically sensitive, so that steps of grey going in a logarithmic progression over 1.5 to 1.6 or more decades of dynamic range (30:1 or more on a linear scale) will provide a pleasing contrast range to the observer. Any display should provide these capabilities, and logarithmic grey scales are provided in the test chart for quick visual evaluation. These log scales are in addition to the linear brightness scales included for instrument measurements.

Another factor that can quickly be determined visually is geometrical distortion. The 4×4 grid of lines on the test pattern can be quickly examined for gross defects. Uniformity of spatial frequency responses is an effect which shows up as a fuzziness on the bar targets of higher spatial frequencies. This response generally drops off at the corners of the display, and a fast evaluation can be made visually.

In summary, the human generally likes to see uniformly bright, sharply focused crisp images with a range of contrast exceeding 30:1 in brightness. Various displays should be evaluated with these factors in mind by human observation in addition to the numerical tests given.

In concluding this specification, attention might properly be drawn to the fact that many other measurements are possible (which have not been made) and which would make the evaluation procedure more complete. However, the measurements and results described herein do serve as a strong foundation upon which to base other tests. In addition there are two aspects of the evaluation procedure described in this specification that are worthy of emphasis. First, by using a computer generated test chart we have eliminated sources of scanning noise and have obtained a ground truth which is conceptually (and actually) noise free in terms of computer representation. Second, by using the evaluation equipment described above, we are measuring absolute possible time history decay processes. Consequently, the combination of noise free test imagery and absolute comparisons to evaluate possible time history decay processes. Consequently, the combination of noise free test imagery and absolute measuring units provides a unique and inherently superb test procedure for quantitative evaluation of softcopy displays that can only be implemented in real-time digital image processing exploitation facilities. Hopefully the time is coming when specification of such systems can be based on quantitative measurements rather than the art of display technology.

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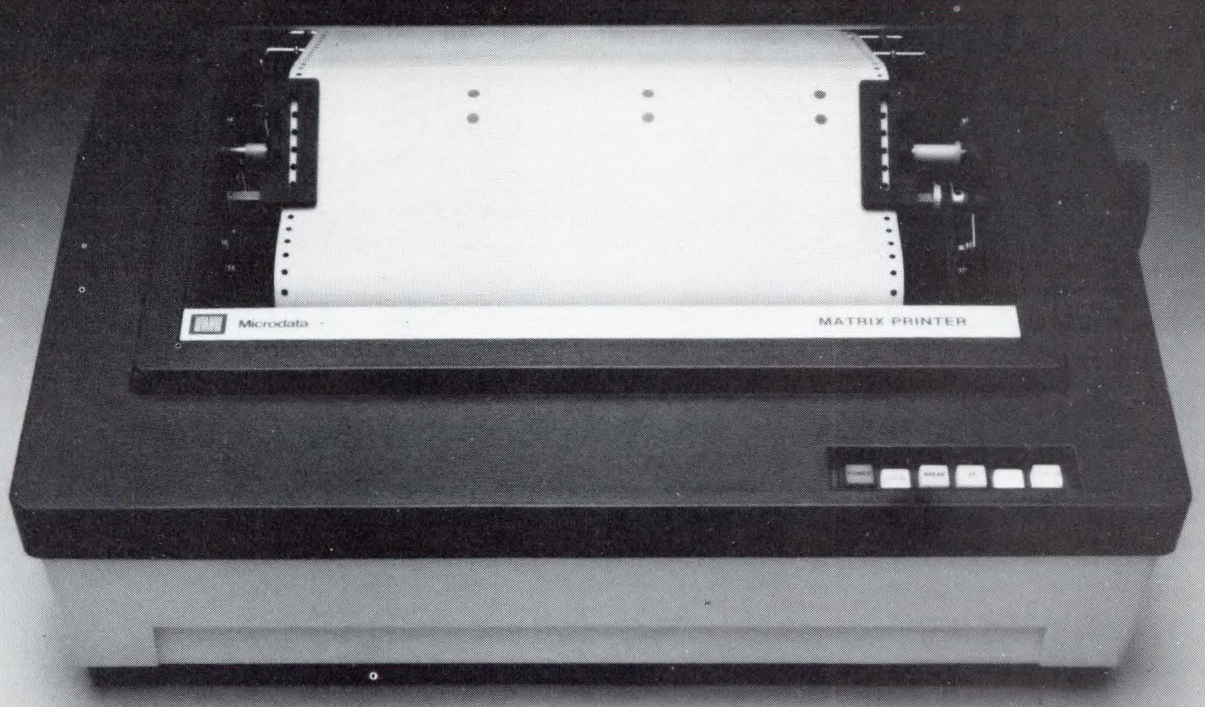

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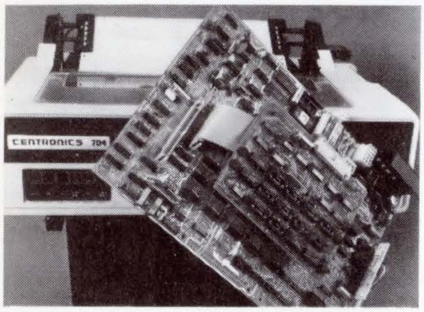


The model 704's nine-pin free-flight print head is said to be the first of its kind ever offered in a data communications printer. $2,350. **Centronics Data Computer Corp.,** Hudson, NH 03051. **Circle 143**

DEBUGGING AID

A simple table-top device to facilitate program debugging for Data General's NOVA 3 series computers, the Model 2001 programmer's aide operates by use of functional control which interrupts program execution after: 1. An instruction has been fetched from a single user-specified address; 2. A single user-specified address has been read; or 3. A single user-specified address has been written. After program execution is terminated, the unit displays the last 64 successive memory locations and provides dynamic monitoring within a single user--specified address during program execution. $3,500. **Mini-Computer Systems, Inc.,** 399 Fairview Park Dr., Elmsford, NY 10523. **Circle 147**

STEPPING MOTORS

Models with 800, 1000, 1600 or 2000 steps/rev. provide step accuracies of 3.5 arc minutes; settling times, 1-2 ms; start/stop rates, 5000 steps/sec; and torques, 400in-oz. **Enerex, Inc.,** Box 262, Newton, MA 02159. **Circle 135**

LOW COST DISK BACKUP

The model IU 1650, a low cost magnetic tape unit for backing up non-removable hard disk drives, has a storage capacity of 56 Mbytes (unformatted) at 6400 BPI on 9 tracks with a transfer rate of 250 KBPS. The drive utilizes a single motor in a simple, low cost mechanism which automatically self-threads the tape and is a reliable tape handler. It reads and writes at 40 IPS and has high speed search. Interdyne's Unireel tape package is a removable, self protecting, 650 ft. reel of ½″ magnetic tape, which fits in the palm of your hand. **Interdyne Co.,** 14761 Califa St., Van Nuys, CA 91411. **Circle 157**

HIGH SPEED STATIC RAMS

The 2115H/2125H 1K bit and 2147H 4K bit static memories are fabricated using a new patented generation process called HMOS II to achieve maximum access times of 20 ns and 35 ns respectively. The new devices are faster than bipolar memories of equivalent storage, and they use considerably less power, according to the manufacturer. 2115H/2125H (30ns): $9.85 (100); 2147H (35ns): $62.60 (100). **Circle 155**

6502 PROGRAMMING

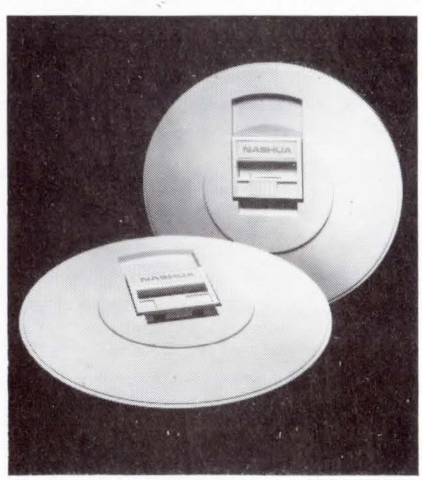
"Programming the 6502" by Rodney Zaks is an educational text designed to teach programming from the ground up. It uses the 6502 to show you its advantages and disadvantages. The text is structured from simple to complex. Many exercises are included. 304 pg. $9.95. **Sybex, Inc.,** 2020 Milbia St., Berkley, CA 94704.

MICRO INTERFACING

"Interfacing and Scientific Data Communications Experiments," by P. Rony, D. Larsen, J. Titus and C. Titus, introduces the engineering reader to principles involved in the transfer of data using the asynchronous-serial data transfer technique. Numerous experiments are involved take the reader through a step-by-step procedure. Appendices provide data sheets for several common UARTs. $5.95. **Howard W. Sams & Co., Inc.,** 4300 W. 62nd St., Indianapolis, IN 46268.

HARD DISK CARTRIDGES

The model 4442 disk cartridge series features a .075″ disk, utilizing 408 cylinders and certified at 4400 BPI and 200 TPI. A 10 Mbyte cartridge with 24 sectors is available for use with the Data General 6070



drive. There is also a 12.5 Mbyte cartridge with a variety of sector configurations for use with Wangco ST2422 and Datapoint 9374 disk drives. $140. **Nashua Corp.,** Computer Products Div., Nashua, NH 03061. **Circle 144**

INTER-PROCESSOR ADAPTER

High speed transmission of data between CPU's via a full duplex buss, is achieved by the Model 2004 Inter-processor Adapter (IPA). The 2004 IPA employs a master/-slave concept for the associated control in the establishment of the transmission process. The full duplex buss permits each CPU to be a "Host" computer at the same time, permitting two separate and unrelated data transfer operations to execute simultaneously. The "Slave" CPU will passively transfer data by IPA operation in either direction; the host/slave designation is independent of data transmission direction. IPA has two PC boards imbedded in each of the Nova computers with a dual cable connection to accommodate the full duplex buss. **Mini-Computer Systems, Inc.,** 2259 Via Burton, Anaheim, CA 92806. **Circle 193**

MAG TAPE SUBSYSTEM

The new Telex Series 80 features a "down-sized" column frame appearance that consumes less power, reduces heat emissions and requires less floor space. Series 80 is compatible with IBM 3420 series tape systems and encompasses 800/1600/6250 BPI data densities. Present Telex 6000 Series tape subsystems can be intermixed with the Series 80. Several new patented features including the low inertia Spur-Lite capstan and the Telex tape path, which eliminates large unsupported spans of tape, bring new reliability and performance to this new generation of Telex tape subsystems. **Telex Computer Products, Inc.,** 6422 E. 41st St., Tulsa, OK 74135. **Circle 191**

MICROBENCH 8048/8748 SOFTWARE

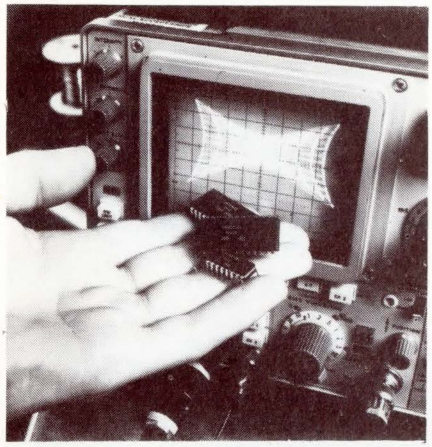
A series of computer programs to support applications development for the 8048/8748 family, Microbench 8048/8748, operates on LSI-11s and PDP-11s to provide an economical program development facility for this μP family.

Included in Microbench 8048/8748 are a relocating assembler, linking loader, librarian and object file formatter. The assembler supports extensive macro and conditional assembly facilities, cross reference listings and provides for relocatable object modules. The linking loader provides linkage facilities, selective loadng from libraries, and directives for specifying ROM/RAM alignment.

The object file formatter produces absolute binaries in compatible formats for use with PROM programmers and emulation systems, including equipment manufactured by Data I/O, Prolog, SMS, Intel, Motorola and Tektronix. Perpetual license fees start at $1,695, including documentation and first year's maintenance. **Virtual Systems, Inc.** 1500 Newell Av., #406, Walnut Creek, CA 94596, **Circle 300**

MONOLITHIC CRT GEOMETRY/FOCUS CORRECTOR

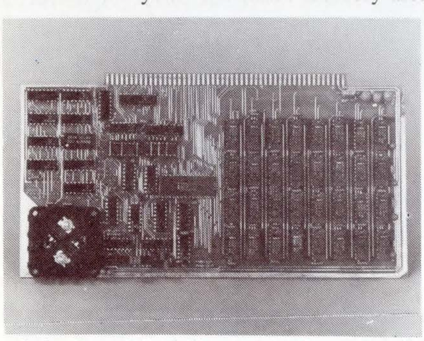
C310/C410, industry's first monolithic geometry/focus corrector, is a single IC that offers a cost effective solution to distortion in CRT displays giving the user reliability that only a single monolithic chip can offer, while still maintaining the flexibility, if required, to adjust for different tube geometries and system types. Applications include high precision alphanumeric and hyrid dis-



plays, photo-typesetting systems, computer-output microfilming, heads up and heads down displays, photoelectronic image-stabilization image-enhancement systems and closed-circuit TV systems used in surgical monitoring and remote observation of hazardous processes. **Intronics,** 57 Chapel St.,Newton, MA 02158. **Circle 137**

S-100 MEMORY PRICE REDUCTIONS

Due to the decrease in memory prices, Central Data is announcing a substantial price reduction in its 16K-64K memory boards. All boards come completely assembled, tested, and burned-in. The warrantee on the boards is one year. The entire memory area



of the board is fully socketed, so that the user can expand his board without returning it to the factory. The new prices are: 16K — \$249, 32K — \$375, 48K — \$500, and 64K — \$625. These reductions amount to over 20% on some boards. **Central Data Corp.,** PO Box 2484, Station A, Champaign, IL 61820. **Circle 150**

BASIC SOFTWARE

BASIC ETC, a Basic language interpreter for 8080/Z-80 systems using cassette storage, was developed by the co-authors of the original Tiny Basic, and is suitable for business, scientific and games programming. The program requires 9.5K bytes of RAM. Features include: integer, real and string variables capability; integer constants range of -32,767 to +32,767 (0 to 65,536 as array subscripts or memory references); real constants from n × 10^{-62} to n × 10^{62} with the number of significant digits selectable from 6 to 72 (default = 6); 11 string commands and functions; n-dimensional arrays; program line numbers from 1 to 65,567; direct memory and I/O addressing; detects error conditions; outputs 27 errror messages; and character and line erasure during input.

BASIC ETC includes EDIT, FN(n) and 18 other functions. Transcendental functions return values accurate to 0.001%. \$35. **Percom Data Company,** 211 N. Kirby, Garland, TX 75042. **Circle 148**

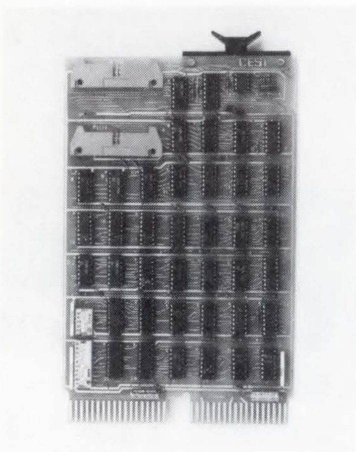
ELECTRONIC DISPLAYS

"Electronic Displays" by Sol Sherr, a 636-pg. hardcover, covers aspects of human perception that affect display system design and performance: performance characteristics of CRT, matrix, numeric and alphanumeric devices, performance testing and evaluation complete display systems. \$35. **John Wiley & Sons, Inc.,** 1 Wiley Dr., Somerset, NJ 08873.

New Products

LSI 11 PAPER TAPE CONTROLLER

The PTCL11 paper tape controller is completely hardware and PC11 software compatible with DEC LSI11, LSI11/2, and PDP11/03 computers. Designed specifically for the Data Specialties, Inc. "S" series, high performance systems it offers



on board DIP switches allow easy address and vector selection. The controller occupies one option slot and requires 600 ma at 5 Vdc. $600.00. **Computer Extension Systems, Inc.,** 17511 El Camino Real, Houston, TX 77058. **Circle 146**

64 I/O LINE μMODULE

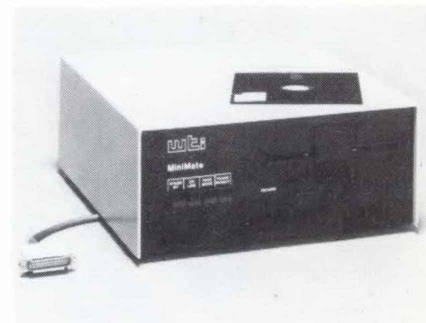
Industrial applications of micros require many inputs for sensing system states and outputs for controlling switches, solenoids, displays, etc. This parallel I/O module allows up to 64 I/O lines organized as 8 8-bit ports on a 4½" × 6" module. Each 8-bit port is programmable as input or output; for each port there are 2 programmable control lines for automatic handshake protocols including maskable or unmaskable interrupts. Each output line is fully buffered for 15 TTL loads. The module can be supplied with 2, 4, 6 or 8 ports at $59, $89, $119, $149 (100 qty.). **Wintek Corp.,** 902 N. 9th Street, Lafayette, IN 47904. **Circle 198**

STAND-ALONE TAPE TERMINAL

This desk-top unit is built around two independently operable cartridge transports and has 672,000 bytes capacity plus RS-232 interface for data rates to 9,6000 Baud. Series 1000 communications terminals (of which there are four versions), can be controlled from front-panel push buttons, or placed under full remote control. Remote control permits operation from a nearby CRT terminal or other keyboard, or alternatively, from a distant computer or centralized EDP facility. The tape transports incorporate read-after write heads plus CRC technology (Cyclic Redundancy Character) to ensure error free operation. **North Atlantic Industries, Inc.,** 60 Plant Ave., Hauppauge, NY 11787. **Circle 197**

RS232 MINI FLOPPY TERMINAL

Designated MiniMate, the unit is designed as an attachment to intelligent CRT or hard copy terminals to handle store and forward applications effectively and efficiently. It also includes character edit capability. The MiniMate provides over 71K characters of working storage. It is capable of communicating with a host computer in either batch or interactive mode at speeds up to 9600 baud. The unit can also be remotely acti-



vated by an Auto Answer Data Set. Switch selectable baud rates from 110 to 9600 baud, and full X-ON/X-OFF control are also provided. MiniMate's character edit features include backspace-erase, delete, modify, link and stop. Plus, a "GOTO" command allows jumping to random file locations for repeat and linking applications. $1,295. **Western Telematic Inc.,** 2435 S. Anne St., Santa Ana, CA 92704. **Circle 154**

NEW 990 MINI

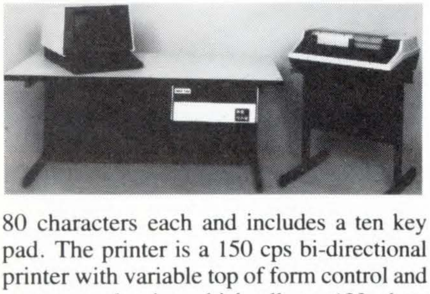
Minicomputer 990/12 utilizes the broad-based and established 990/10 software, existing 990 peripherals, and extends the upper performance range of the established 990 product family. The 990/12 executes all software written for the 990/10 and provides an average performance increase on the order of two to three times that of the 990/10. Improvements beyond this average depend on the application and on the features selected by the customer. Performance increases over prior 990s include overlapped operations, faster LSI devices, a workspace cache on the CPU, a TILINE cache option on the memory and an improved memory cycle; with new features — addition of 71 instructions, error-trace memory and extensions in memory protection. The 990/12 computer with 256K-bytes of error-correcting memory is priced at $19,598 without cache and at $22,948 with cache for OEM qty. (25). **Texas Instruments Inc.,** Digital Systems Div., Box 1444, Houston, TX 77001. **Circle 178**

APPLICATION SOFTWARE

Applications software for the Digi-kit-izer graphic tablet is available. This software package includes programs written in Applesoft Basic for the Apple II computer. In addition to X-Y coordinate location output, users may have their own CAD system by capturing, moving and rotating preprogrammed logic symbols to construct circuit diagrams. By tracing any curves or polygons, both perimeter of these irregular shapes are calculated. Other interesting programs included in this one package include music generation by pen location, HIres graphics and LOres color graphics. $49.95. **Talos Systems, Inc.,** 7419 E. Helm Dr.,Scottsdate, AZ 85260 **Circle 127**

HARD DISK STORAGE

A 10 million character hard disk computer system for the small business user includes a single board CPU with 65K bytes of 800 nsec MOS memory. The CPU utilizes the 2901 μc to emulate the 16 bit instruction set of the Data General Nova. The disk is a top loading unit with one fixed disk and one removable disk, each of 5 million characters. The video display is a full 24 lines of



80 characters each and includes a ten key pad. The printer is a 150 cps bi-directional printer with variable top of form control and compressed print which allows 132 characters to be printed on an 8½″ size paper. The complete system is packaged in a desk with a separate printer stand. Complete systems are priced at $15,995. Basic Time, 1215 E. El Segundo Blvd., El Segundo, CA 90245. **Circle 156**

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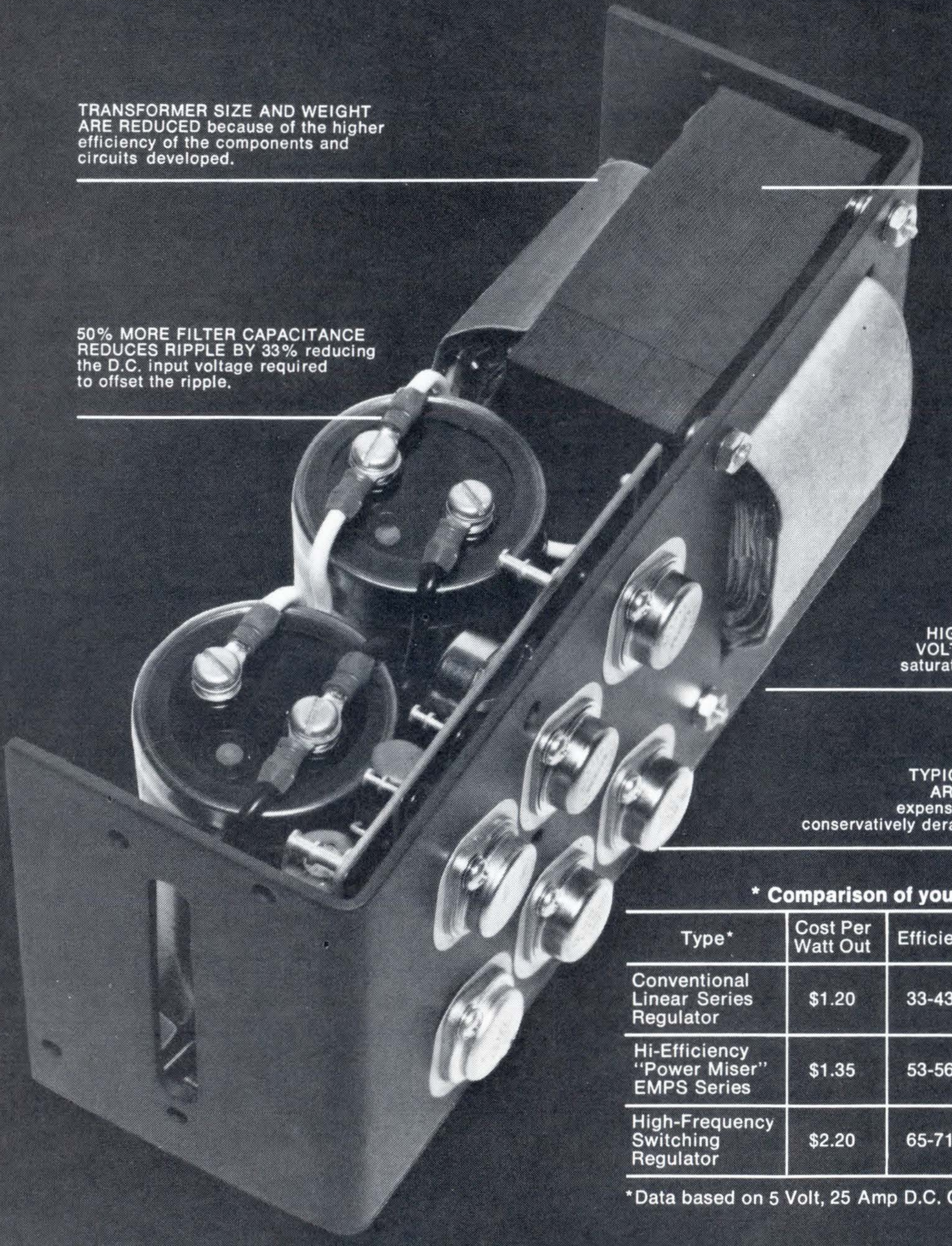

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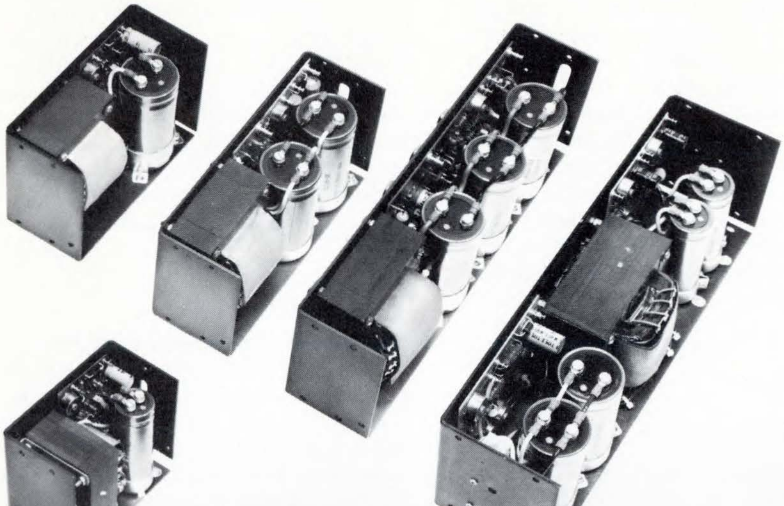

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Single Output Models							
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5V @ 12A	54% ±2%	EMPS 5-12	109.00	103.55	99.40	96.40	94.50
5V @ 18A	54% ±2%	EMPS 5-18	135.00	127.95	122.80	119.15	116.75
5V @ 25A	54% ±2%	EMPS 5-25	180.00	171.00	164.00	159.25	156.00
5V @ 40A	54% ±2%	EMPS 5-40	220.00	209.00	200.60	194.60	190.00
12V @ 12A	59% ±1%	EMPS 12-12	170.00	161.00	154.00	149.25	146.00
12V @ 18A	59% ±1%	EMPS 12-18	210.00	199.00	190.00	184.60	180.00
15V @ 11A	65% ±1%	EMPS 15-11	170.00	161.00	154.00	149.25	146.00
15V @ 16A	65% ±1%	EMPS 15-16	210.00	199.00	190.60	184.60	180.00
24V @ 8A	68% ±1%	EMPS 24-8	170.00	161.00	154.00	149.25	146.00
24V @ 12A	68% ±1%	EMPS 24-12	210.00	199.00	190.60	184.60	180.00
Dual Output Models							
±12V @ 6A	OVER 50%	DEMPS 12-6	190.00	188.10	180.60	175.15	171.65
±15V @ 5.5A	OVER 50%	DEMPS 15-5.5	190.00	188.10	180.60	175.15	171.65
Triple Output Microprocessor Models							
5V @ 12A ±12V @ 2A	OVER 50%	TEMPS-3	185.00	175.75	168.70	163.65	160.40
5V @ 18A ±12V @ 3A	OVER 50%	TEMPS-4	230.00	218.50	209.75	203.50	199.40

*For ±15V add "-2" suffix to model no.
Overvoltage protection standard on TEMPS-3 & 4, 5V. output

Specifications: All Models

A.C. Input:
5 V.D.C. OUTPUT UNITS: 105-125 Vac. 47-440Hz (derate 10% for 50Hz operation)
ALL OTHERS: 105-125/210-250 Vac, 47/440Hz

Extended A.C. Input: 100-130 Vac (derate 20%)

D.C. Outputs: See Tabulation of Models

Control: ± 5% Voltage Adjustment (Screwdriver adjust pot.)

Regulation: ± 0.05% Line or Load

Remote Sensing:
Standard on all models, (includes open sense lead protection.)

Ripple: 5mV Peak to Peak

Reserve Power:
+5% of output available for external load line drop on 5V. and 12V. units; +0.6V. on all others.

Temperature Coefficient: 0.02%/° C.

Stability:
± 0.1% for 24 hour period after 30 minute warmup

Overshoot:
No turn-on, turn-off or power failure overshoots.

Transient Response:
Output recovers to regulation band within 50 microseconds after an instantaneous load change of 50 to 100%.

Operating Temperature:
-25° to +70° C. (derate linearly above +50° C. to 40% at +70° C.; derate linearly below -5° C. to 70% at -25° C.)

Cooling:
Convection cooled for full power rating at 50° C. ambient. Forced air cooling extends full power rating to 60° C.

Protection:
Overload and short circuits: Automatic recovery foldback current limiting fully protects against overloads and short circuits.
Reverse Polarity Protection: Prevents damage from reverse voltage swings.
Inductive Load Protection: Prevents damage due to inductive voltage swings.

Overvoltage:
Optional crowbar overvoltage protection. (Standard on 5V. output TEMPS)

Transformer:
Electrostatically shielded for better line noise immunity.

All Models Meet U.L. Recognition Requirements.

CALL OUR ENGINEERING SALES OFFICE IN YOUR AREA FOR COMPLETE DATA AND PRICES

Arizona, Phoenix
Phone: (602) 894-2335

California, Anaheim
Phone: (714) 634-9211

California: Long Beach
Phone: (213) 426-7375

California, Los Gatos
Phone: (408) 354-6496

California, San Diego
Phone: (714) 560-1009

Colorado, Denver
Phone: (303) 688-4154

Connecticut, Meriden
Phone: (203) 237-9232

Florida, Coral Springs
Phone: (305) 752-7520

Florida, Largo
Phone: (813) 536-8536

Georgia, Atlanta
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(404) 981-9753

Illinois, Chicago
Phone: (312) 437-2700

Indiana, Indianapolis
Phone: (317) 844-2800

Iowa, Cedar Rapids
Phone: (319) 362-9177

Kansas, Kansas City
Phone: (913) 381-0004

Kansas, Wichita
Phone: (316) 264-2662

Massachusetts, Boston
Phone: (617) 245-0250

Michigan, Detroit
Phone: (313) 576-4706

Minnesota, Minneapolis
Phone: (612) 861-3343

Missouri, St. Louis
Phone: (314) 569-1220

New Mexico, Albuquerque
Phone: (505) 294-8408

New Mexico, Las Cruces
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New York, Albany
Phone: (518) 456-6667

New York, Buffalo
Phone: (716) 632-7880

New York, New York
Phone: (516) 487-3966

New York, Rochester
Phone: (716) 482-3000

New York, Syracuse
Phone: (315) 637-9383

North Carolina, Hayesville
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Pennsylvania, Philadelphia
Phone: (215) 825-9515

Pennsylvania, Pittsburgh
Phone: (412) 961-0414

Texas, Dallas
Phone: (214) 387-2489

Texas, Houston
Phone: (713) 988-0991

Washington, Seattle
Phone: (206) 641-3535

Washington, D.C.
Phone: (202) 363-9417

Wisconsin, Milwaukee
Phone: (414) 527-1500

ADTECH POWER

Europe: ADTECH INTERNATIONAL, Subsidiary of Adtech Power, 46 BD, Roger Salengro, 78200 Mantes La Ville, France. Tel. 4775301+
DISTRIBUTORS: Call Kathy Nelson, Distributor Products Group, (714) 634-9211, for the name of a distributor near you.

Power Misers are also manufactured in Europe.

ADTECH POWER, INC., 1621 S. SINCLAIR ST., ANAHEIM, CA 92806. (714) 634-9211 ● TELEX 68-1498

Circle 64 on Reader Inquiry Card

LOW-PRICED MINIPRINTERS

Designed to meet needs of professional and very small business applications and priced from $995, Models 730-1 through 730-7 offer a 3-in-1 paper handling system and use the same heavy-duty, free-flight print head technology found in the 700 Series. All models also include such standard features as 50 cps print speed, 80-col line length at 10 cpi, a full line buffer, high speed carriage return and high-quality 7 × 7 dot matrix printing. Smaller and lighter than the average-sized portable typewriter, these units weigh less than 10 lbs. and measure only 14.5″ wide by less than a foot deep and less than 5″ tall. All 730s come with a built-in ability to handle multipart plain paper in any 1-of-3 operator-selectable ways. The printers' typewriter-like platen takes hand-fed 8-1/2″ wide sheets in letter, legal size or longer lengths. Standard international-sized A4 sheets may also be used. Fixed pins on the platen automatically accept standard computer-grade multipart or single-part fanfold paper nine inches wide from pin to pin. And, this system also allows the use of 8-1/2″ wide roll paper up to 5″ diameter. **Centronics Data Computer Corp.**, 1 Hall St., Hudson, NH 03051. **Circle 176**

NEXT-GENERATION DISKETTES

Model 288, said to be industry's first μP-controlled (8048) diskette drive, is the first drive to incorporate a new dual-head design which lends itself to high-yield manufacture. It employs "big disk" electronic techniques to eliminate the need for write pre-compensation in double density and offers performance advantages of voice coil positioning and dual diskette technology in a drive which is a direct replacement and cost competitor for Shugart Models 850/851. Model 288 is a dual-head, dual-density, dual-diskette drive; it reads and writes data on both sides of 2 diskettes (a total of 4 heads and 4 diskette sides) in IBM compatible or expanded capacity single and double density formats. Data capacity is as high as 3.2 Mbytes in a single industry standard size 8″ drive. $925 (OEM qty.). **PerSci, Inc.**, 12210 Nebraska Ave., West Los Angeles, CA 90025. **Circle 190**

IBM 4300 SERIES

An 18-pg report, "IBM 4300 Series," discusses IBM's "E series" product line in terms of price/performance, technology employed, accompanying changes in software pricing and support policies. It lists a detailed review of operating characteristics, processors and peripherals, software and support, I/O control, configuration rules, mass storage, communications control and comprehensive price lists. **Datapro Research Corp.**, 1805 Underwood Blvd., Delran, NJ 08075. **Circle 199**

RS232 DUAL CASSETTE TERMINAL

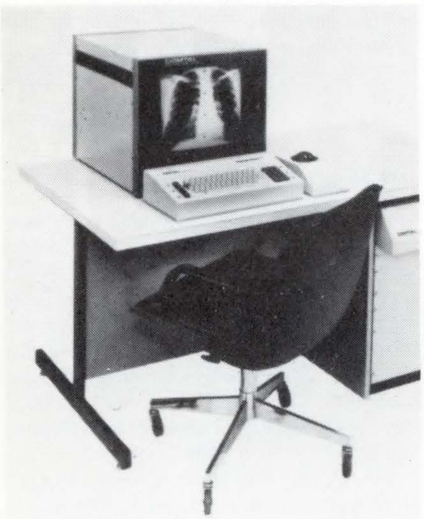
Model 6801 Raycorder dual cassette terminal, designed around a Motorola 6800 microprocessor and two Raymond Model 6406 cassette drives, reads, writes or copies data in ANSI X3.48-1977/ECMA34 format or can be switched to a format compatible with existing T.I. terminals. The serial, full duplex RS232C or current loop interface is switch-selectable in 8 steps for data transfer rates of 110 to 9600 baud. It emulates punched paper tape and operates with PDP-8 or PDP-11 operating systems. **Raymond Engineering Inc.**, Raycorder Products Div., 217 Smith St., Middletown, CT 06457. **Circle 180.**

DS-80 DIGISECTOR

The Micro Works Digisector, a random access video digitizer, provides resolution and speed said to be unmatched. Since operation is straightforward, you need not be a software wizard to utilize the DS-80's extensive capabilities. The Micro Works Digisector board provides the following exclusive features: high resolution — a 256 × 256 picture element scan; precision — 64 levels of grey scale; speed — conversion times as low as 4 μsec/pixel; versatility — accepts either interlaced (NTSC) or non-interlaced (industrial) video input; and compatibility — uses 1 bus slot in any S-100 system conforming to IEEE standards. $349.95. **The Micro Works**, Box 1110, Del Mar, CA 92014. **Circle 201**

VISION ONE/20 DIGITAL IMAGE PROCESSING

Said to be a major advancement in state-of-the-art, digital image processing, Vision One/20 provides (on its high-resolution raster monitor) images of film-level or better photographic-quality on a real-time, interactive, stand-alone basis. The combination of a large (up to 134 M bits) image-refresh data base memory, a powerful operating system implemented in firmware, and a resident μP controller is claimed to make Vision One/20 the most versatile stand-alone exploitation system available. Vision One/20 can support up to 4 simultaneous



users stations that share the same data base and can handle input from multiple sensors that share the system's processor. Interconnecting it to a host computer via one of a dozen different interface control cards makes the system even more powerful. The system can process images stored both in analog form on film and in digital form from sensors and scanners. These provide a large dynamic range and high quality which film cannot handle. Memory stores up to 64 images of 512 × 512 pixels or 16 images of 1024 × 1024 pixels, 8 bits deep for B/W and 24 bits deep for color. The system provides 256 gray shades and 16 million colors/pixel. **Comtal Corp.**, Box 5087, Pasadena, CA 91107. **Circle 177**

GRAPHIC DISPLAYS

"All About Graphic Display Devices" summarizes characteristics of 72 display devices and systems from 22 manufacturers. The 24-pg. report, a reprint from the Feb. 1979 subscriber's supplement to "Datapro 70" looseleaf information service, is a comprehensive survey of graphic display equipment. Its comparison charts describe configuration, display characteristics, software support, pricing, delivery status and special features of 72 devices and systems. Describing general characteristics and limitations of today's graphic display equipment, it provides guidance in equipment selection, and summarizes experience of 37 users of 163 graphic displays. $12. **Datapro Corp.**, 1805 Underwood Blvd., Delran, NJ 08075. **Circle 200**

PICCOLO 8" DISK CERTIFIER

Model 3PX358 disk tester, a fully automatic, μP-controlled system, provides disk manufacturers and OEM suppliers full test and certification capability for the newly announced IBM Piccolo 8" disk. This test system tests 8" disks and is adaptable for testing all prior generations of IBM compatible "hard" disks. It's a totally self-contained, internally programmed single-disk certification system with μP-controlled automatic and manual test capability. A 16K random access memory provides program and test data storage. Program loading and generation of modified program tapes is done by a Three Phoenix TCT-300A Tape Cartridge Unit, with automatic program loading upon system initialization. For Data or Servo disk testing, 3 automatic operating test modes can be selected — Automatic Reject, Stop On Error, and Continue On Error. For versatility, a Manual mode allowstest engineers to evaluate disk performance during disk development or analysis programs. **Three Phoenix Co.,** 21639 North 14th Ave.,Phoenix, AZ 85027. **Circle 179**

TSX/DBL/RTSORT

DEC PDP-11 users are offered enhanced versions of TSX, multi-terminal RT-11 support system, and DBL, the DIBOL-11 compatible compiler. TSX, enhanced to use extended memory (above 64K bytes) as a high-speed swapping area, increases throughput up to 100%. ISAM (Indexed Sequential Access Method), added to the DBL compiler, speeds program development. Special reduced price license fees for single user version of DBL for users of small PDP-11s and PDTs are available. **Mini-Computer Business Applications,** 4929 Wilshire Blvd., 9th Floor, Los Angeles, CA 90010. **Circle 192**

FLOPPY FOR DR-12/25

A floppy disc option for Adar's DR-12/25 memory test system gives DR-12/25 users greatly expanded mass storage capacity and faster access to stored data. Each IBM-compatible diskette provides an additional 256K bytes of memory. Stored data is accessed by the system's computer in less than 650 msec. Transfer rate is 15k wps. Executive software can be boot-strapped directly from the diskette, cutting program loading time from minutes (with a standard digital cassette) to secs. DR-12/25 comes with the system — or as a field retrofit. **Adar Assoc., Inc.,** 154 Middlesex Tpke., Burlington, MA 01803. **Circle 194.**

FASTER EPROMS

Mostek's high performance upgrades include the MK2716T-6 at 350ns and MK2716T-7 at 390ns. Mostek's 2716 is a 2K × 8 bit electrically programmable/ultraviolet erasable ROM. The MK2716 is pin out compatible with all 5V only 16K EPROMS. Prices for the MK2716 family start at $32.75 (100). **Mostek Corp.,** 1215 W. Crosby Rd., Carrollton, TX 75006. **Circle 217**

New Products

PROGRAMMABLE VRAM

The Matrox PV-1 is a 4.5'' x 6'' module controlling a standard TV monitor and interfacing to any μC bus. 96 ASCII characters and 32 graphics symbols may be displayed in either 8 or 16 lines of test. Each line may have from 16 to 64 characters. Internal/external sync as well as analog and digital mixers satisfy applications in CCTV, security, mass information displays as well as conventional terminal requirements. The flexibility of the PV-1 will interest a wide range of engineers using mini and micros and TV monitors as the display medium. $295. **Matrox,** Electronic Systems Ltd., 2795 Bates Rd., Montreal, QUE. H3S 1B5, Canada **Circle 141**

I/O PRODUCTS

Opto 22 has two "Intelligent" products for use with their power I/O μP systems. A parallel addressable board allows a μP to communicate with up to 1632 points and 64 control stations through an 18 conductor "daisy chain" signal cable. One parallel addressable board (PAB) is used for each I/O station and mounts under the I/O board to conserve mounting space. The system provides th basis for a simple distributed cotrol system using existing microprocessor boards where the system stations are within 50 ft. of the host controller. For distributed control systems where the stations are more remote (up to 1000 ft.), Opto 22 announces a serial addressable board (SAB-1). **Opto 22,** 5842 Research Dr., Huntington Beach, CA 92649 **Circle 139**

I/O SOLUTIONS

CRT and printing terminals available for purchase, rent or lease are covered in this 8-pg., full-color catalog. It lists equipment from major manufacturers including DEC, IBM, Hazeltine, Lear Siegler, Centronics, TI, etc. **Electro Rent,** 4131 Vanowen Pl., Burbank, CA 91505. **Circle 126**

μP SYSTEM DESIGN

Intended for use in conjunction with a detailed manufacturer's μP, "Introduction to Micro Processor System Design" by Harry Garind covers basic micro hardware and machine language, as well as assembly and higher-level languages. The final three chapters of this ten-chapter book covers μP arithmetic, analog interfaces and interface standards. Answers are provided to all odd-numbered problems. $10.95. **McGraw-Hill Book Co.,** 221 Ave. of the Americas, New York, NY 10020.

ENHANCEMENTS SERIES 21

Extended capabilites for the Mohawk Series 21 line of distributed data processing systems include an increase in memory, price redutions for add-on memory, and concurrency software for the low-end Series 21 systems. Basic memory systems and memory maximums have been increased on all systems. The entry-level System 21/20 now has a basic memory of 48K, expandable in 16K and 32K increments to 96K; the basic memory of the System 21/40 has been increased from 32K to 48K, expandable in 16K and 32K increments to 96K; and the basic memory of the high-performance System 21/50 has been increased from 64K to 96K, expandable in 32K increments to 256K. The price of 16K and 32K add-on memory modules for all systems has been reduced by 50%, the result of new memory technology incorporated in the Series 21 systems. **Mohawk Data Sciences Corp.,** 1599 Littleton Road, Parsippany, N.J. 07054. **Circle 140**

HIGH SPEED CASSETTE

The model 3783HV system is oriented towards program loading where it is necessary to frequently load programs quickly and without error. This system offers a loading rate of 9600 Baud and handles tape with minimum wear. Tapes may be recorded on one system and read by any other with equal reliability. The 3783HV is said to assure very high resistance to tape imperfections and environmental EMI.

The Model 3783HV is a complete stand-alone unit with power supplies, I/O connections and all controls for operating either manually or by computer command. \$1,995. **Memodyne Corp.,** 220 Reservoir Street, Needham Heights, MA 02194. **Circle 151**

MICRO I/O SYSTEM

This system's mother boards incorporate I/O modules to provide photo-isolation between the micro and loads. Four basic types include AC input, AC output, DC input and DC output. The logic signals are TTL, CMOS, DTL or HTL compatible and are available with a choice of three voltage levels, 5, 15, or 24 Vdc. Additionally, a choice of 120 or 240 Vac is available with the AC modules and the DC modules is available in a 10-32 V or 200 V input and a choice of 60V or 250V output. Both the AC and DC output modules contain snubber filters to enhance performance when used with inductive loads. 2500 Volt RMS photo-isolation which provides immunity to the microprocessor from transients, RFI, etc. \$10.50 **OPTO 22, Huntington Beach, CA 92649.** **Circle 131**

M68000 SUPPORT PRODUCTS

The first software support products for the M68000 — the M68KSAMC Cross Macro Assembler and M68KEMLC Simulator — come on magnetic tape and permit designers to develop and debug M68000 programs using an IBM 360/370. The M68KSAMC Cross Macro Assembler is a program that anslates source statements written in M68000 assembly language into M68000 machine language. In addition, it is upward compatible with the resident Structured Macro Assembler scheduled for release with the M68000 development system. The M68000 Cross Macro Assembler provides the programmer with extensive capabilities and outputs, including: numerous pseudo-operations, conditional assembly capability, macro directives and assembler output listings. \$1500. **Motorola Semiconductor Products, Inc.,** Box 20912, Phoenix, AZ 85036 (602) 244-6900. **Circle 136**

NCR COMPATIBLE CASSETTE TERMINAL

The MFE 5450VRL μP cassette terminal is an 8080-based memory storage system that features an optional variable record length read capability for compatibility with

NCR's variable block length systems. The standard 5450 is compatible with Sweda, TI, and all other RS232 compatible systems. Accommodating ANSI/EMCA-compatible cassettes, all MFE terminals automatically perform Read After Write, CRC, and parity error checks to insure data integrity. Dual RS232C I/O interfaces are standard; 20 ma current loop is optional. 5000 and 5450: from \$1995; 2500: from \$1190.**MFE Corp.,** Keewaydin Drive, Salem, NH 03079. **Circle 152**

8086 KIT

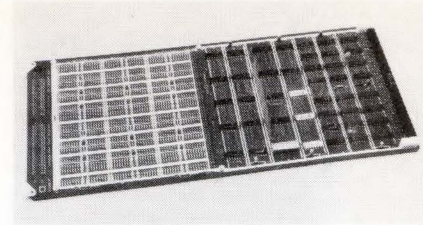
The SDK-86, a complete 8086 system on a board withmemory and I/O systems in kit form includes an 8-digit LED display, a 24-key keyboard, and all other necessary components from resistors and crystal to CPU.

For data memory, there are 2K bytes of 2142 RAM. This can be double by implementing additional devices in the positions provided. There is also room for 8K bytes of program memory using either or both of the keyboard and TTY/CRT 4K ROM-resident software monitors included in the kit, or a 2716/2316E EPROM/ROM combination. A complete design library is provided with the kit which includes both the assembly and users manual, plus an MCS-86 User's Manual and 8086 Assembly Language Reference Manual. \$780. **Intel. Corp.,** 3065 Bowers Ave., Santa Clara, CA 95051 **Circle 142**

New Products

UNIVERSAL LOGIC MODULE

Universal Logic Module on a half-board provides an interface between any model Perkin-Elmer (Interdata) computer and a peripheral device. The module features switch selectable ten bit device address, a 16-bit register and a 16-bit output register; fory-two 14 or 16 pin IC positions are provided for user designed logic, and can accomodate larger IC's on .3, .4, .5, or .6 inch centers. The bus side of the module provides device addressing, handshake, status and interrupt control to the Interdata Multiplexor or Selector channel bus. It also contains the 16-bit output register and the 16-bit input register. The user side of the module contains the 42 IC positions for 14 or 16 pin integrated circuits for user designed logic for interconnection on two-level wire wrap posts. Lo-profile DIP sockets are optional. All IC positions have ground connected to pin 8 and +5V connected to pin 16. Eighteen of the IC positions can accommodate larger IC's from 18 to 40 pins. Optional provision for 40 to 50 pin ribbon cable connectors are on the front edge of the board;



smaller configurations can be specified.

The MDB ULM half-board is priced at $495 with pins, or $550 with both pins and sockets mounted. **MDB Systems, Inc.,** 1995 N. Batavia St., Orange, CA 92665. **Circle 164**

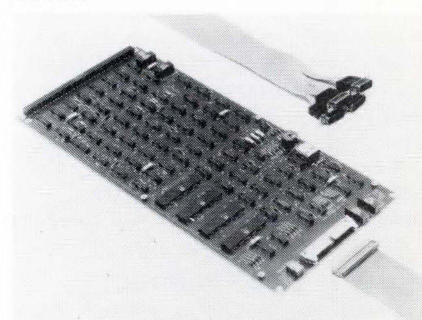
MODEL 40 PRINTER INTERFACE

This universal printer interface adapter for the Teletype Model 40 printer, Model SP-40, interconnects the Teletype simplified EIA-like interface to a variety of serial and parallel computer and/or communication interfaces. Simple DIP-Switch positions are used to select the required interface. The SP-40 has audible and flashing lamp system alarm indicators; printer, logic and communication interface fault diagnostic indicators; test pattern generator; and an operator selectable 'thumbwheel' vertical tab. The SP-40 is designed to mount inside the Local Data QUIET 300 acoustic enclosure or below the printer in the Teletype cabinet. **Local Data Company,** 2741 Toledo St., Suite 214, Torrance, CA 90503. **Circle 129**

4-CH. LOCAL COMMUNICATIONS INTERFACE

The Qualta (Quad Asynchronous Local Terminal Adapter) is a plug-in four-channel interface board to directly replace the single-channel adapter in Perkin-Elmer's Interdata processors.

By omitting data functions not normally used for local communications on standard PASLA and PALMS channels, Qualta provides users with four times as many local channels in half the space and at lower cost. By conserving plug-in space within the processor, it allows more interfaces to be used, thus forestalling the necessity of purchasing one or more expensive PALMS add-on chassis.



Four channels, half- or full-duplex, operating at rates from 50 to 19,200 baud are furnished on QUALTA's single Interdata-compatible half-board which plugs into any available slot in the CPU. $675. **MACROLINK,** 1740-E South Aanaheim Blvd., Anaheim, CA 92805. **Circle 133**

S100 MAINFRAME

The UC2000 System A combines a 12″ CRT, keyboard, S100mainframe, 18 amp power supply, and axial blower in a textured IBM-off-white enclosure. Space is available within the enclosure for a mini floppy drive or other customer supplied device. A rear panel provides for external interface connection, CRT controls, and power fusing. $795. **Infinite Inc.,** 1924 Waverly Place, Melbourne, FL 32901.

μC MODEM

The Micromodem II can transmit data between an Apple II and another Apple II, a terminal, another μc, an mc or even a large time-sharing computer anywhere in North America over regular telephone lines. The

System includes serial I/O, 1K byte of firmware, a 103 compatible modem and an FCC registered interface. It can operate at either 110 or 300 baud. **D. C. Hayes Associates, Inc.,** 16 Perimeter Park Dr., PO Box 9884, Atlanta, GA 30319. **Circle 153**

MICROBENCH 8048/8748 SOFTWARE

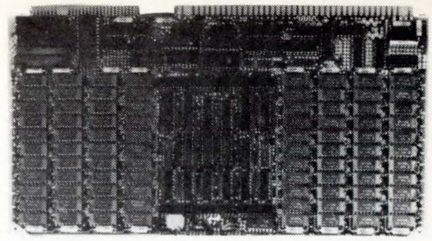
A series of computer programs to support applications development for the 8048/8748 family, Microbench 8048/8748, operates on LSI-11s and PDP-11s to provide an economical program development facility for this μP family.

Included in Microbench 8048/8748 are a relocating assembler, linking loader, librarian and object file formatter. The assembler supports extensive macro and conditional assembly facilities, cross reference listings and provides for relocatable object modules. The linking loader provides linkage facilities, selective loadng from libraries, and directives for specifying ROM/RAM alignment.

The object file formatter produces absolute binaries in compatible formats for use with PROM programmers and emulation systems, including equipment manufactured by Data I/O, Prolog, SMS, Intel, Motorola and Tektronix. Perpetual license fees start at $1,695, including documentation and first year's maintenance. **Virtual Systems, Inc.** 1500 Newell Av., #406, Walnut Creek, CA 94596, **Circle 134**

MULTIBUS MEMORY

MUPRO's iSBC compatible memory guarantees increased system uptime, reduced power consumption, reduced maintenance expense and reduced overall system cost. It features: Compatible with iSBC Multibus, Extended Mulibus, Multiprocessor Operation, and Series II Development Systems; available in 10 memory sizes — 16K — 512K bytes; high speed access and cycle times; accomodates both 8-bit byte and 16-bit word transfers; minimizes power requirements for reduced supply cost; provides power-fail recovery capability



with protection and control lines to ensure memory integrity; and special backup power bus for minimum stand-by power drain. **Mupro, Inc.,** 424 Oakmead Pkwy, Sunnyvale, CA 94086, (408) 737-0500. **Circle 138**

New Products

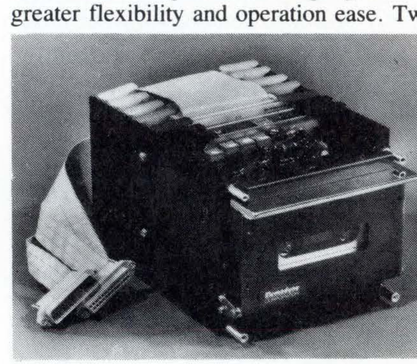
T-100 PRINTER/PLOTTER

The T-100 impact dot matrix plotter, a versatile, low-cost alternative to electrostatic printer/plotters interfaces with Printronix plot software and has plug compatibility with Printronix, Centronics and Data Products printers. It utilizes raster matrix technology to plot at 15 ipm with a dot density of 100 dots/in. Operating costs are reduced by 75% compared to electrostatic methods because the T-100 uses standard fanfold paper at a cost of 0.5 ¢/sheet, opposed to 2¢ or more for special sensitized paper needed for electrostatic operations.

TRILOG's T-100 accommodates forms from 4″ to 16″ wide and up to six parts. Printing speed is 250 lpm with a standard 96-character set. Additional features include underlining, double high characters, either 6 or 8 lines per inch and lower case characters with descenders. The $7230 list price insludes Data Products or Centronics compatible interface, ASCII standard 96-character set, built-in self-test diagnostics, pedestal and paper catcher, installation, and 90-day on-site service. **TRILOG, Inc.,** 16705 Hale Ave., Irvine, CA 92714. **Circle 130**

CASSETTE COMPUTER

With a data capacity of 500K formatted bytes, computer-controlled cassette recorder system M80 can transfer data at programmed rates up to 19,200 baud. All potential errors are automatically retried and rewritten if the tape medium is at fault. M80 interfaces through RS-232C and TTY current loop serial ports. All recorder controls and communication functions are interrupt driven and transparent to user programs for greater flexibility and operation ease. Two



spare bus slots permit additonal chips of dynamic RAM to be used for interfacing other peripherals such as keyboards, displays, complete terminals, printers, etc. Suited as an automatic storage device for data acquisition systems, data communication systems, intelligent terminals, any data processing system. Under $2k. **Memodyne Corp.,** 220 Reservoir St., Needham Heights, MA 02194. **Circle 128**

FULL CHARACTER PRINTER

This line printer with full characters, featuring a Teletype model 40 print mechanism. The Quiet 300 132-column unit is priced at $4595. The mechanism is a heavy-duty, line-at-a-time, hard-copy, impact printer. It prints crisply on up to six part forms and offers either friction or tractor feed with the 80-column unit and tractor feed with the 132-column unit. The 300 is capable of 300 LPM with ASCII 63 character set and 500 LPM with the 48 character set. This printer features a Centronics or Dataproducts compatible parallel interface. It also has a Buffered-Serial interface with a 1 to 4K memory with x-on, x-off option. **Local Data Co.,** 2741 Toledo St., Suite 214, Torrance, CA 90503. **Circle 132**

New Products

DISK DRIVE

The Diskos 3350 drive uses a fully servoed voice coil positioner to achieve a capacity of 33 Mbytes on a single 14-inch disc. Succeeding versions of the DISKOS 3350 will have capacities of 66 and 154 Mbytes using the same basic mechanical and electronic design. A brushless dc spindle drive motor eliminates the mechanical brake common to Winchester disc drives and permits the unit to be used in systems requiring all-dc power. A proprietary internal air-filtering system and breather filter design prevent contamination of the system by external air, even if the head-disc cavity seals were to leak. The drive measures 7" by 17.5" by 20"; weight is 33 lbs. An optional power supply can be included in the drive envelope. In the 33 megabyte capacity version, the DISKOS 3350 sells for an OEM price of $1800 per unit. **Priam,** 20730 Valley Green Dr., Cupertino, CA 95014. **Circle 215**

VIDEO DIGITIZER

μP-based image analyzer, the Model 2000 can simultaneously digitize and store (on-board) video from a TV camera or other image source in real time, enter it into any host Data General computer, and display it on a TV monitor. The self-testing, 15⅜ × 15⅜ card also performs graphics generation, image processing, and archival image storage (when used with a disc memory). If used with a modem, it can transmit TV images over voice grade telephone lines. With a host computer access time of 800 ns per pixel, the Model 2000 offers a resolution of 320 pixels (x-axis) by 240 pixels (y-axis). To emphasize or deemphasize image features, the 16-level gray scale is modifiable by an I/O computer programmable video lookup table. $4700 each, including RDOS software driver. **Octek Inc.,** John E. Trombly, 121 Middlesex Turnpike, Burlington, MA 01803. **Circle 210**

SCROLL AND ZOOM MODULE

Labeled the GCT-3037-1, a new dual-function scroll and zoom module allows a Genisco high resolution (512^2 or 1024^2) raster graphics color or monochrome computerized display to scroll pixel-by-pixel horizontally and line-by-line vertically, or zoom to twice, four times or eight times the original picture size, all without changing the contents of the system's refresh memory. Data can be vertically scrolled on an individual line-by-line basis and pixel-by-pixel, horizontally. The display can also be wrapped around in both vertical and horizontal modes to provide up, down, left or right scrolling motion — a "waterfall effect." The GCT-3037-1 scroll/zoom plug-in module board option is immediately available from the factory. Approximately $1,000. **Genisco Computers,** 17805 Sky Park Circle Dr., Irvine, CA 92714. **Circle 211**

SIMULATOR MODULE FOR MC6805

The MC6805 simulator module was developed to serve as a tool for systems designers and programmers who wish to familiarize themselves with Motorola's MC6805 microcomputer. The MEX6805-SIM simulator operates in non-real-time, using an M6800 firmware resident program designed to execute MC6805 object code.

Features of the MC6805 Simulator (MEX6805SIM) include: Accurate simulation of the entire MC6805 instruction set; Simulation of interrupt-driven routines with provisions for MC6805 User Reset, INT, and Timer Interrupt signals; Full trace capability, including such capability through any user interrupt; Instruction mnemonic, effective address, addressing mode, and immediate byte printout during trace operations; Firmware cycle counting for timing of MC6805 routines; Traps all invalid instructions, effective addresses, stack pointer over-and-under-flows and program counter overflows; Switch array for convenient generation of MC6805 external signals, including User Reset, INT and Timer; and Three I/O ports (20 bits of I/O). A diskette containing the MC6805 Macro Assembler, and a program to demonstrate the various switch functions on the module, is supplied as part of the MEX6805SIM. $2500. **Motorola Microsystems,** P.O. Box 20912, Phoenix, AZ 85036. **Circle 212**

You're Fired

Even though all the advertisers in this issue are offering strictly free information on the latest products in their ads, 7-out-of-10 people will not respond. Perhaps they're concerned about some "catch" – permit me to tell you there is none. Our advertisers desire one thing: a chance to show you their products data at no cost and no obligation to you.

Can you afford not to take advantage of such an offer? Not if you expect to keep your job three years from now. Those engineers who don't keep up with the latest advertised products will find themselves behind the eight ball two years from now. With numerous products entering the marketplace at a blinding rate, it's no news to you that it's no longer easy to keep up – or even be aware of what's available! It just doesn't make sense for an engineer who expects to keep his job not to circle advertisement circle numbers on the cards. Frankly, it puzzles me.

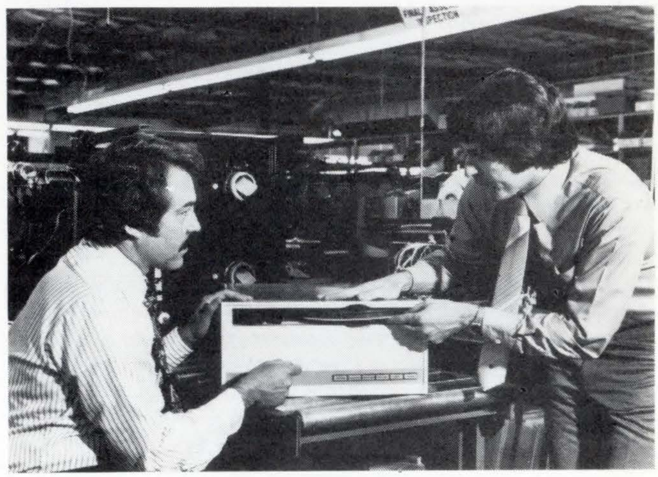
With obsolescence and engineering half-life at two years, do a little something extra to keep up. Yes, books and courses are fine, but to get really practical information, nothing beats advertisements as a source of information. Remember, it only takes a few minutes to circle the ad numbers on the cards to keep up – the practical way – with Reader Inquiry Card circle numbers. Do you have the time? Others do.

Paul Snigier, *Editor*

New Products

LOW-COST/HIGH-SPEED

Cipher's Low Profile Streaming Tape Drive measuring only 8-¾″ high by 19″ wide, functions in a "streaming" mode, taking data in large blocks on-the-fly at 100 ips without stops and starts. Because the low profile drive employs 10.5″ tape reels and has a capacity of more than 37 Mbytes of formatted data, the entire capacity of many disk files can be "dumped" into the tape drive in one continuous high-speed operation. This is a major cost/effective alternative to cartridge drives, flexible disks and removable hard disks. Under $1.8k. **Cipher Data Products,** 5630 Kearny Mesa Rd., San Diego, CA 92111. **Circle 188**



$400 INTELLIGENT PRINTER

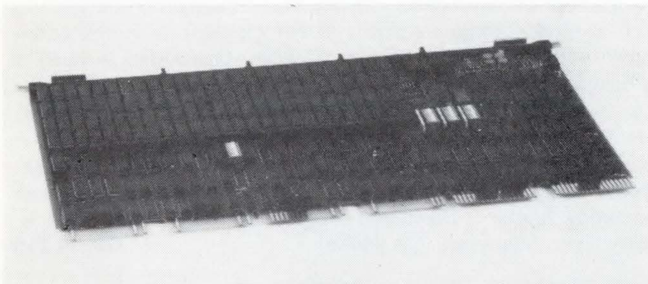
Trendcom 100 intelligent printer provides the micro user with 40-col. hard copy on 4½″ wide paper. Interfaces are available for TRS-80, Apple II, PET and Sorcerer. It prints bidirectional 40 cps with a full 96-char. ASCII set, including U&L case letters, numerals and punctuation. The 5 by 7 dot-matrix char. are printed with either black or blue images, depending upon paper. $375. **Trendcom,** 484 Oakmead Pkwy., Sunnyvale, CA 94086. **Circle 183**

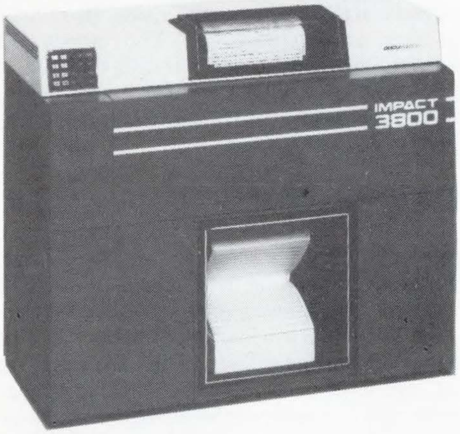
PLASMA DISPLAY SCREEN

Model 801M forms information by loading columns, 7 bits high, and shifting in the loaded columns as the next column is loaded. Thus, it has a graphic range within a field of 7 dot positions high by 480 dot positions wide. Potential applications include: 1 line of 80 characters if a dot space is used between characters; 1 line of 40 characters if double dot spacing is used; 1 line of graphic information such as a bar graph or square wave to which an identifier message could be added. Model 801M capabilities include backspacing at the same speed as forward load and rotation to yield right hand, left hand or vertical load. An INPUT end enters all dots. Interface consists of 7 bit high column data and control, TTL compatible. **Modern Controls, Inc.,** 19228 Industrial Blvd., Elk River, MN 55330. **Circle 213**

PDP-11/34 64K MEMORY

Error-corrective single board 64K word (128K byte) dynamic RAM for DEC's, PDP-11/34, NS11/34E, has single voltage power requirements and features single-bit error correct/multiple-bit error detect circuitry (ECC) which make the NS11/34E suitable for applications that demand maximum system uptime and minimal user maintenance. Since all logic and memory are included on a single card, only one card-type need be spared, further easing field maintenance and support. The error correcting NS11/34E has the performance characteristics of other high-speed memories without ECC capabilities. NS11/34E significantly outperforms DEC's MS11-L memory. Typ. write access time for the NS11/34E is 100ns, 50% faster than the MS11-L. $4325. **National Semiconductor Corp.,** 2900 Semiconductor Dr., Santa Clara, CA 95051.
Circle 186





3800 LPM IMPACT PRINTER

Impact 3800 prints at 3,800 lpm, its rated 95% faster than competitive models, and incorporates many feature found. in Impact 3000. Offering all the advantages of impact printing at non-impact speeds, the 3800 enables you to print up to 6-part forms with high slew and throughput rates. It can print 57 std. 11 × 14-pages (150 or 132-char. lines) at 6 lpi in 1 min — the equivalent of 9,500 cps. **Documation Inc.,** Box 1240, Melbourne, FL 32901. **Circle 185**

FRONT END SWITCH

A fully electronic data switching system (Front End Switch) is capable of connecting a number of asynchronous terminals to any of several sources of computing service. System switching is controlled by the DTR signal(s) of the connected service and switching to a back-up system occurs automatically when DTR goes false on the primary system. The front end switch is modularly designed allowing easy expansion. A number of switching configurations are available. For example, a 1:4 switching configuration allows 64 incoming terminals to be switched to any of 4 computing services. Plug-in circuit boards carry asynchronous channels and can be mixed within the system. Other features include operational speeds up to 9600 bps asynchronous, complete transparency to data, status indicators for all channels and standard EIA RS 232C interfaces. Statistical information on each change occuring in the system is automatically provided at a separate control and monitor port. **Gandalf Data Inc.,** 1019 South Noel, Wheeling, IL 60090.
Circle 214

Circle 73 on Reader Inquiry Card

Circle 74 on Reader Inquiry Card

New Products

LARGE-SCREEN PROJECTION SYSTEM

Consisting of a receiver/projector console and seven foot (diagonal) screen, the GM-301 projection system achieves unusually high optical efficiency through its use of ultra-wide-aperture Schmidt optics with a speed of f0.7. The device focuses an image by means of three LightGuide projection tubes, one for each of the red, blue and green signals that make up the picture. The tubes produce no distracting or resolution-limiting phosphor dot or stripe patterns, with resolution limited only by the video bandwidth. A completely dark room is not required, because the picture is brighter than the intensity specified for commercial movie theaters. Computer interface positions on the GM-301 allow input of direct digital television (RGB) sources, with either external or internal composite sync, as well as monochrome composite video outputs from computer terminals with special video outputs. Features of the system in the RGB or data mode include selective underscan, alternate horizontal scan rate, sync level control, and Back Porch or Sync-Tip clamping. Options are available that allow the projected image to be enlarged to ten (diagonal) feet or reduced to five feet. The brightness of the image varies in proportion to its size, with smaller projections becoming brighter. Basic unit: $8,200. **Ramtek Corp.,** 585 N. Mary Ave., Sunnyvale, CA 94086. **Circle 218**

LARGE PRINT VIDEO TERMINAL

"LPVT" — a Large Print Video Terminal — can be used by the visually impaired and those with normal vision. Its suited for facilities that must meet Federal Affirmative Action computer accessibility requirements, because one device will suffice for all. LPVT is a stand-alone, RS232C-compatible CRT with 3 user-selectable print sizes up to 1.5" high. $9k. **Arts Associates, Inc.,** 80 Boylston St., Suite 1260, Boston, MA 02116. **Circle 182**

MICRONOVA OS/SOFTWARE

Reportedly the industry's first advanced operating system designed and developed specifically for 16-bit μC technology, the Micron operating system meets growing need of sophisticated 16-bit μC users for increased programming productivity and lower maintenance costs. The Micron system improves programmer productivity through system development facilities and utilities like its interactive debugger and high-level structured programming language, MP/Pascal. It can be used efficiently for both program development and runtime environments. In addition, the Micron operating system is compatible with Data General's Advanced Operating System (AOS), used by scientific Eclipse data systems. **Data General Corp.,** Route 9, Westboro, MA 01581. **Circle 181**

OHIO MICRO

The C3-C fills price/performance gaps between floppy systems and large disk systems and uses the new mid-range 29 Mbyte Shuggart Winchester technology disk, offering greatly increased performance over floppy based systems. A standard configuration includes the Challenger III processor, 48K of memory, the 29 Megabyte Winchester technology disc drive, and a pair of floppy discs for file system back up. Under $10k. C3-C is software compatible with other Challenger III family members, and its software library includes Basic, Fortran, Cobol, a word processor and information management system and a multi-user operating system (OS-65U Level 3). **Ohio Scientific,** 1333 Chillicothe Rd., Aurora, OH. **Circle 195**

PDP-11/70 CONTROLLERS

The SC70 family of software-transparent microprogrammed controllers meet a large disk storage requirements of PDP-11/70 users. The SC70/B1 controller emulates the DEC RH70/RM03 subsystems; the SC70/B2, the RH70/RP06. Both versions accommodate 80 and 300 Mbyte disk drives; SC70/B2 also handles a 200 Mbyte drive. Later versions will cover anticipated larger drives in the 600 Mbyte range. $5,150 (50). **Emulex Corp.,** 17785 D Sky Park Circle, Irvine, CA 92714. **Circle 189**

Systems Design Guide

Data Entry Peripherals: Criteria for Selecting CRT Terminals

Staff Report *RCA Service Co.*

The Data Services Group of the RCA Service Company became involved initially with CRT terminals because of a need for this type of equipment by a major customer in the communication industry. A further analysis by the Marketing Research Department then determined that the company could use these terminals, if flexible enough, in a wide range of marketplaces. In early March 1978, Marketing requested the Engineering Department to become involved. That's when the selection process began.

An initial survey of the marketplace revealed a very large number of vendors and an enormous range of video terminal offerings. Because of the number of pieces of equipment available, management organized the project into three phases in an attempt to systematize the search and focus on a final selection. Briefly, Phase I consisted of a paper study over a broad range of vendors and types of equipment. Phase II involved issuing engineering specifications to vendors whose equipment seemed most suitable, and Phase III involved the submission of terminals for testing by the Engineering Department.

Phase I

Engineering first investigated several sources before contacting vendors. These sources included Data Pro reports, trade magazines, results of an EDN questionnaire on CRT terminals, and the reputation of and experience with vendors by RCA engineers and engineers from several other companies engaged in the communications industry.

Then, Engineering sent a request for product literature to several dozen of the most reputable vendors supplying the entire spectrum of CRT product offerings (dumb, smart and intelligent). The department gave vendors two weeks to respond.

A study of the information in the submitted catalogs, plus the availability of the product in large quantities and the location of the vendor's headquarters (U.S. or foreign), reduced the list to a manageable size. Engineering then recontacted the reduced list of vendors with a request for more literature and a visit by a sales representative.

One selection criterion of Phase I involved a more precise definition of the primary product types that would most closely meet the requirements of RCA's customer and also meet flexibility standards to enable RCA to enter other marketplaces with the product offering.

Depending on the degree of programmability, CRT terminals are commonly defined as dumb, smart or intelligent, but RCA soon discovered that microprocessor technology has changed these standard definitions. For example, limiting a system's software capability can downgrade a μP-based terminal from intelligent to smart — or even dumb.

Although RCA engineers were initially interested in system applications involving a large number of terminals, they decided that microcomputer-based terminal could address various marketplaces and market needs by varying the unit program. This flexibility in the programmable units reduced th evaluation program to a consideration of only micro processor-controlled terminals.

Four factors complicated the selection process at this stage of the investigation: terminal performance characteristics, price, flexibility and product obsolescence.

Terminal capabilities are increasing even as prices are dropping on a year-to-year basis. Flexibility allows RCA engineers to program the video terminal selected to meet most of today's common protocols in industry by making only minor modifications to the software and firmware. This flexibility permits terminal adaptation to the data entry display and editing requirements of a variety of user applications. Obsolescence implies that after a certain period a product no longer meets market needs. (The CRT terminal period is generally assumed to be five years.) Since a change in software can provide the means for applying a programmable intelligent terminal to meet different needs, it therefore prolongs the life cycle. Consequently, RCA placed heavy emphasis on the criterion of product obsolescence in the selection process.

Phase II

This phase began with the preparation of preliminary engineering specifications based on an actual customer requirement. RCA then issued specifications to vendors selected from Phase I. It used the following judgment criteria to select the vendors for Phase III analysis: meet or exceed engineering specs, cost of product, product mix/flexibility, delivery —prototype/production units, documentation for engineering/marketing, departments, training — length, cost, location, space for inventory — cost, availability and support offered to RCA — engineering, marketing, field.

After determining whether a terminal met the engineering specifications, RCA next considered the primary criterion of cost. Since previous financial analysis had determined at what price the unit would cease to be cost effective, RCA set a ceiling. All of the vendors who met the overall specifications and criteria were then carried over into the Phase III engineering evaluation.

Phase III

The final phase consisted of carrying forth all criteria from Phase II, plus a more detailed engineering analysis. Among other things, the analysis examined: serviceability of the product, engineering support offered by the vendor, MTTR, MTBF statistics, product reliability, environmental behavior, functional and physical characteristics and product expandability.

As previously mentioned, RCA made flexibility and obsolescence factors most important in the final selection of a CRT terminal. According to Mansur Alwan, who headed the video terminal selection project, the unit had to be capable of supporting word processing systems. Therefore, it had to be able to operate with floppy disk drives and printers capable of producing office letters.

RCA extensively tested the submitted terminals for modular serviceability of hardware, serviceability of software, ease of upgrading by RCA technicians, and resistance to static electricity. In addition, the project group evaluated vendor support with respect to documentation, engineering follow-up on problems and training.

Testing and evaluation led to the selection of Zentec Model 50 by the marketing and engineering groups by addition to the RCA line of telecommunications equipment. Deliveries of the Zentec unit have begun. Total purchase of the units is expected to amount to several million dollars over the next few years. RCA leases the terminal for between $100 and $120 a month, including RCA service, for a wide variety of applications, ranging from taking orders and making reservations to priority interoffice communications.

RCA Data Services leases a complete line of telecommunications equipment. In addition to the ZMS-50 CRT, it has also just introduced the Teletype Model 43 and the Termi-Net 200 terminals. RCA technicians maintain the equipment from 180 nationwide locations.

Determining Serviceability

A number of factors determine serviceability. The terminal should be repairable with standard tools to eliminate the need to invest in new servicing equipment. Time to repair should be quite short. The terminal should be easy to program for internal self-diagnostics. The mechanical design should allow easy disassembly and reassembly. The terminal should preferrably contain one main logic function board to minimize parts count and improve reliability and serviceability.

After placing each terminal in an office environment and running it for several days, RCA engineers compared the results with vendor statistics. In addition, they contacted consumers who were using the different terminals to find out what they had learned from operating them. From what RCA learned from its customers and from a judgment of terminal performance in its own plant, RCA came up with an estimate of MTBF and MTTR.

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The Future of Data Entry Peripherals: Revolution, Evolution – or the Doldrums?

R. E. Kelton,
TEC, Inc., Tuscon, AZ

The intelligent CRT is finding itself caught in a stage where manufacturers are wondering if they should devote their R&D, and as a result a large portion of my product line, to solely a CRT with intelligence or bypass this phase and build a small business system. Just how long can a company grow at a profit making and selling intelligent CRT's. Today's cost of sales are soaring while the customers' dictates are for a low price terminal. The move toward "system manufacturing" and "system selling" is gaining tremendous support among many of the historical OEM manufacturing operations. I believe that today, in most OEM manufactuer's long-range planning meetings, where for their company's history, one product, whether it be a CRT, printer or disk, prevailed and accounted for all of their sales — this one product theory is being replaced by a "one system" plan.

Here's a scenario of the future: (1) it will be the same as today from a marketplace standpoint, that is, the numbers of qualified and large users has remained the same, (2) The competition in the industry will force prices lower, thus making it imperative for manufacturers to have a solid sales plan for capturing their part of the marketplace, (3) there will be dramatically difference from previous years due to the main frame companies realizing that by building their own CRT, they are losing money and they (CDC, Univacs, Honeywells, and possibly IBM) will reopen the doors to OEM manufactures that want to bid on CRT quotations.

As I said above, the answers certainly aren't direct, but it is like "crystal balling" a forecast in the computer industry; the odds of being close are great, to say the least. However, I do offer the following, and that is the number of new entries into the CRT manufacturing club will be less than five percent of what it is today, and the number of existing "members of the club" will decrease about 10-15% in numbers. Some reasons for this are two basic requirements which the end-user market must deal with constantly — service and financing.

It goes without saying that financing the company properly is a golden rule and those that usually own the gold have successfully carried out their financial planning on a successful note. The oncoming danger in this area for a number of OEM suppliers is that more Fortune 1000 companies are looking at building their own small systems and terminals, and thus will become OEM prospects and customers in their own right. When this takes place they will not give up the perogative of leasing their equipment; and, here lies the danger for poorly financed companies or companies which have never had to lease their goods out to customers. The alternative to entering this market is simply not to. But the number of potential orders and volume of machines will tempt even the poorest sales person.

The result may be that the only way to stay in the OEM business is to sell to the traditional commercial and end-user; and, the only way for a firm to do this is by being financially prepared.

In addition to leasing aspects mentioned above, another area which will "separate the men from the boys" is the ability of the OEM to service the end-user in a manner which he is typically accustomed to. The cost of this to the OEM must be apportioned to the growth in sales — in no way an easy accomplishment. Ask the smaller independents or even the larger successful peripheral/terminal suppliers.

This "new service area" has all the earmarks of disaster for those companies who fail to properly evaluate and plan for its growth within profitable guidelines. To those companies who are successful in this area, their road to overall success will be easier.

As to the OEM arena which CRT and small system competitors will wage wars in the future, the price factor will yield to corporate image and plans to support their customers. (This assumes, as mentioned earlier, that functional differences will be minor.)

Although the OEM market as we know it today will never die, it will fade away and be replaced by a new image which emphasizes customer support in a much more acute manner than just words.

In conclusion, it is only a matter of time when the Fortune 1000 Corporations (end-users) swing back to the centralization of data processing. The cost of so-called low-cost terminals/systems has reached the point which they are now costing as much money as the CPU which they replaced. So, I believe, it is back to the drawing board for many of those users who requested a low-cost terminal to replace those "small" main frame systems. What I believe will be the end result will be an opening to the OEM manufacturing world, which should provide new avenues to successful financial rewards. However as someone once said, "only the strong will survive," I would like to add "the strong will be the well prepared."

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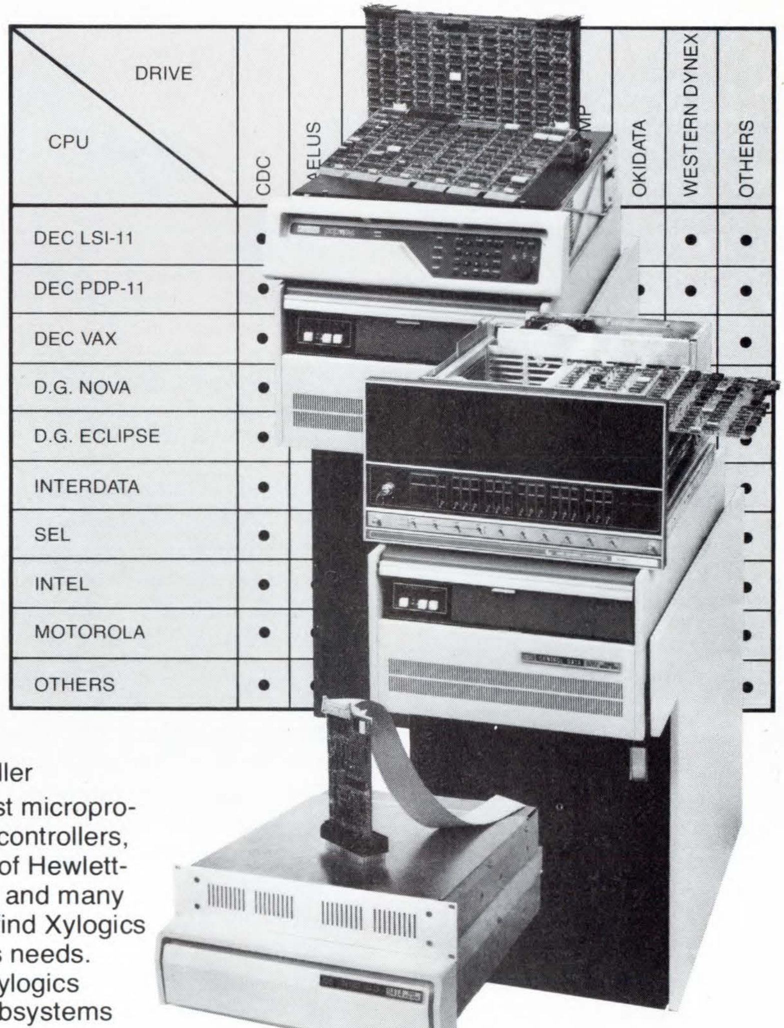
- Model 510 DEC LSI-11® Cartridge Disk Controller
- Model 610 DEC PDP-11® Cartridge Disk Controller
- Model 810 Data General Nova/ Eclipse Cartridge Disk Controller
- Model 211 DEC PDP-11 Storage Module Disk Controller
- Model 850 Data General Nova/ Eclipse Storage Module Disk Controller



Systems designers know that the latest microprocessor technology goes into Xylogics controllers, insuring superior performance. Users of Hewlett-Packard, Varian, Interdata, Honeywell and many other mini/microprocessors may also find Xylogics technology applicable to their systems needs.

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Product Highlight

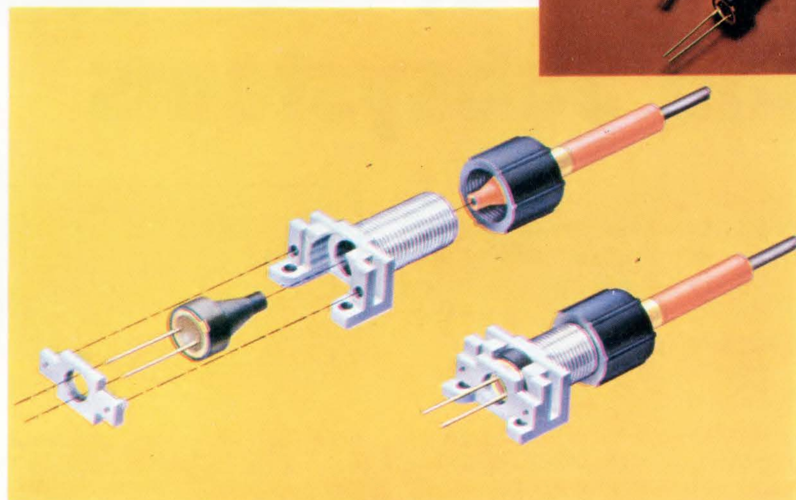
30 Mbits/Sec Packaging Concept Facilitates Fiber Optics Use

A coordinated development effort by Motorola and AMP Inc. has yielded electro-optics packaging to speed up the implementation of fiber optics technology. Results from the program include the imminent introduction of a line of solid state light sources and detectors (by Motorola) and a series of connectors (by AMP) — a combination of components matched to hurdle three main impediments to increased fiber optics use — coupling efficiency, cost and serviceability.

The interconnecting method is said to increase the coupling efficiency of active devices to optical fibers up to 50 times over some current systems. Measured performance includes speeds up to 30 Mbits/sec and systems of one kilometer length have been demonstrated.

In the system Motorola's semiconductor chips, mounted on a sturdy header, are packaged in a resilient plastic ferrule that is an integral part of the optical interconnecting system. An optical fiber contained in the ferrule package extends directly from the active area of the semiconductor die to the highly polished surface of the ferrule for maximum light transfer. An AMP Optimate fiber optic connector mates directly with the new Motorola semiconductor package and provides efficient coupling to all major commercially available fiber cables, the firm said.

Motorola, in assembling the active devices, controls all variables that affect the amount of light exiting an emitter or the sensitivity of a detector. All variables that affect connection losses due to concentricity, end spacing, and angular alignment are under the control of AMP who manufactures the resilient plastic ferrule used by Motorola and the corresponding connector. The only remaining variables are the diameter, and NA (Numerical aperture) of the fiber optic cables being used.



Designed for optimum couplinf to a fiber optic cable with an NA of .48 and a core diameter of 204 μ, these sources and detectors function as an integral part of the AMP Optimate fiber optic connector system which accommodates fiber diameters from 125 to 1145 μ.

The light-coupling aperture of the new Motorola semiconductors is a 0.008 in. diameter core (204 microns) with an NA of .48 for efficient coupling to small fibers. Connector coupling losses to a similar fiber are typically 2 dB. Coupling losses due to mismatched diameters of NA's are easily calculated, and the engineer can readily determine the amount of light coupled into the fiber optic cable from the emitter, or into the detector from the cable, the firm said.

The AMP Optimate connector compatible with these new semiconductors can be bulkhead mounted or pc board mounted and is less than 0.300 in. high for use between pc boards located on 0.500 in. centers typical of computer applications. The connector is metal to provide effective electrical shielding and accepts snap-on shields for further EMI/RFI protection of critical receiver circuitry.

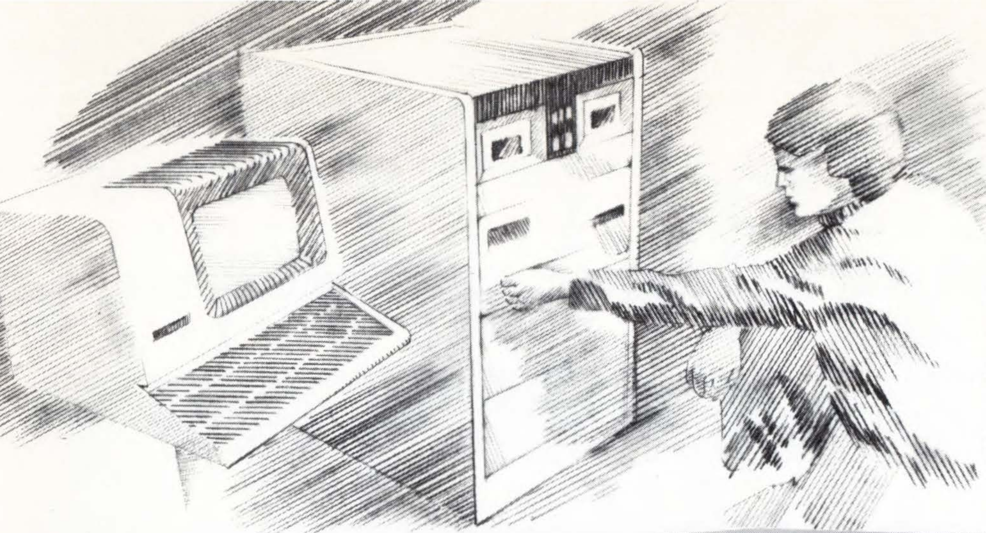
Both the standard plastic Optimate cable connector line, and the new high performance metal versions mate with the metal PC board connector. When the metal connector is used, additional shielding is provided by the connector body itself. This new high-performance metal connector accepts all-glass and plastic clad silica fibers down to 125 microns diameter. The assembly method provides a strain-relief feature that grips the protective strength members common in high-performance cables.

The Motorola devices (available in production quantities in the second quarter of 1979) include one light emitting diode and four detectors — as follows:

MFOD102F	Light Emitting Diode	P_0=40μW (min)(@40mA)
MFOD102F	PIN Diode Detector	Responsivity=0.15 (min) μA/μW
MFOD202F	Transistor Detector	Responsivity=70 (min) μA/μW
MFOD302F	Darlington Detector	Responsivity=2000 (min) μA/μW
MFOD402F	Detector w. IC Preamp	Responsivity=0.6 (min) mV/μW

The emitter and detectors are spectrally matched for maximum responsivity.

Motorola Inc., Box 20906, Phoenix, AZ 85036. (602) 962-3561 (602) 962-3561.



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Emulates paper tape with DEC software at up to 9600 baud

The Raycorder Cassette Terminal Model 6801

The Model 6801 Raycorder Cassette Terminal is a dual-cassette operating system capable of reading, writing, and copying data at switch selectable rates from 110 to 9,600 baud through a full duplex, asynchronous RS232C interface.

Operating under the control of a microprocessor with up to 4K of firmware, the Model 6801 has designed-in versatility never before available in a system of this type.

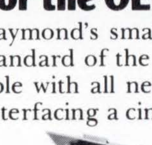
Connected to a serial port of a DEC PDP8 or PDP11 and given the proper address, it will emulate the typical paper tape reader/punch and perform the functions of program load, data logging, assembly, edit or duplication. Select one of two Texas Instruments Silent 700® modes, and tapes can be written, read, or copied that are completely compatible with the 733ASR but at much higher data rates.

With its extension connector, the Model 6801 can be connected to any RS232C port without disturbing the device formerly connected there. With this feature, for example, tape storage can be added where only hard copy print out or CRT display had previously existed.

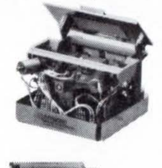
Utilizing two of Raymond's time-proven 6406 Raycorder cassette drives, the Model 6801 provides the ultimate in a reliable, flexible data storage and handling device for a multitude of applications. Detailed specifications will be provided on request.

For the OEM

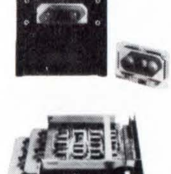
Raymond's small tape drives, long the standard of the industry, are now available with all new electronics that make interfacing a cinch.



Model 6406 for Philips Cassettes, redesigned with many new features at a lower cost.



Model 6409 for Mini-Data Cassettes, now has a parallel interface and other changes you'll appreciate.



Model 6413 for ¼-inch Data Cartridges, the newest member of the team is catching on fast.

Raycorder Products Division
Raymond Engineering Inc.
217 Smith Street
Middletown, Connecticut 06457
(203) 632-1000

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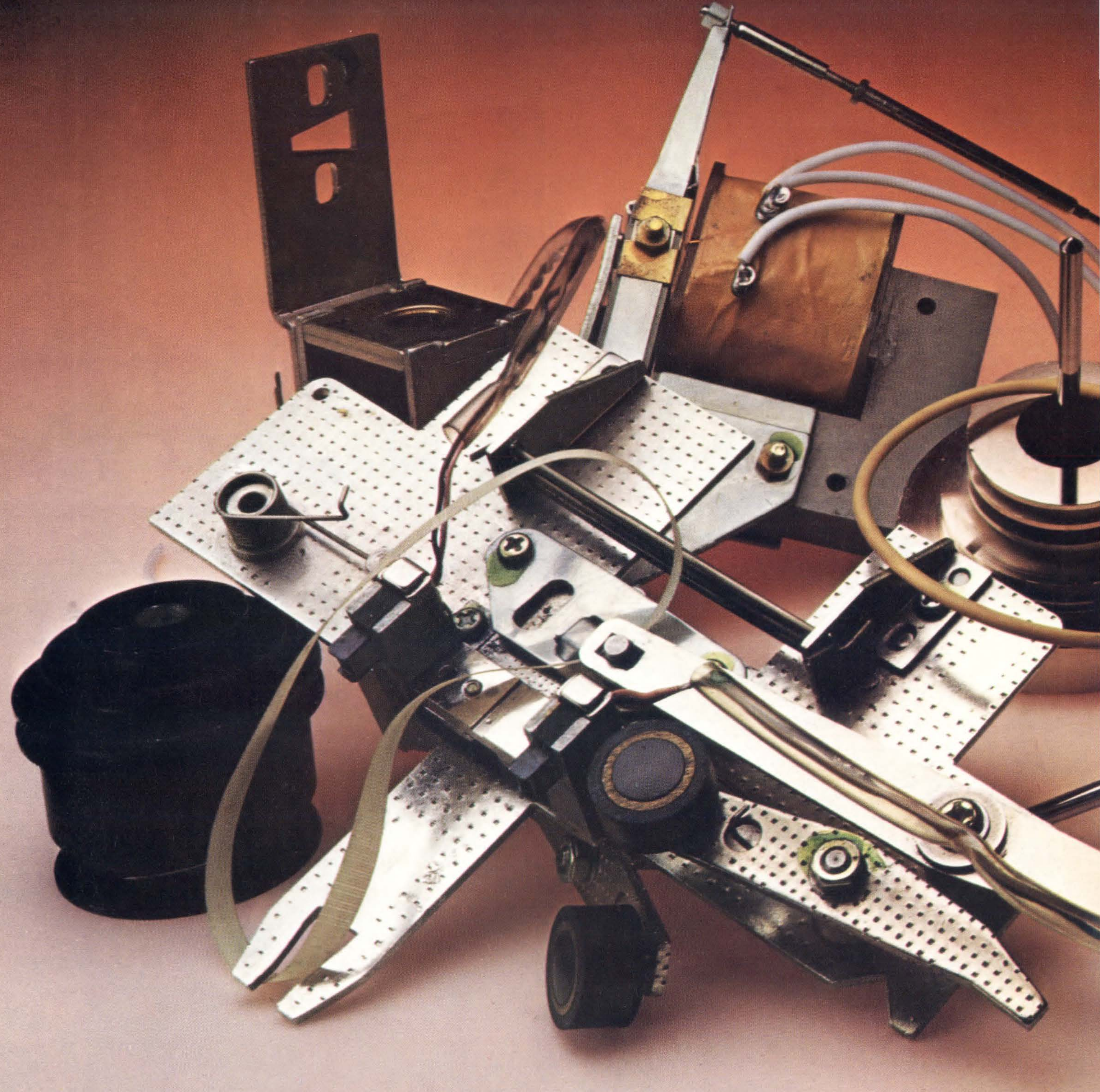
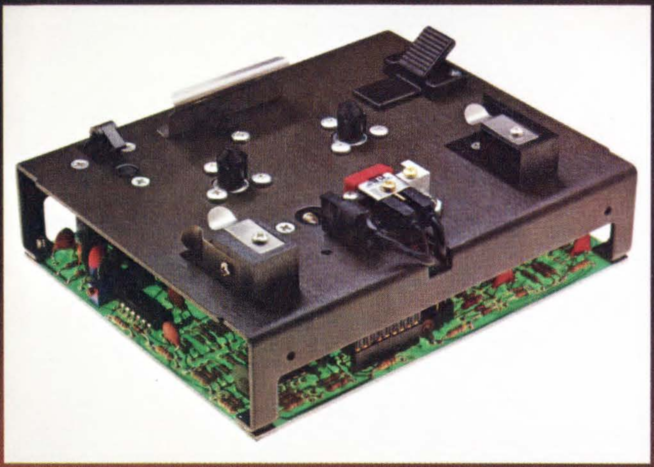
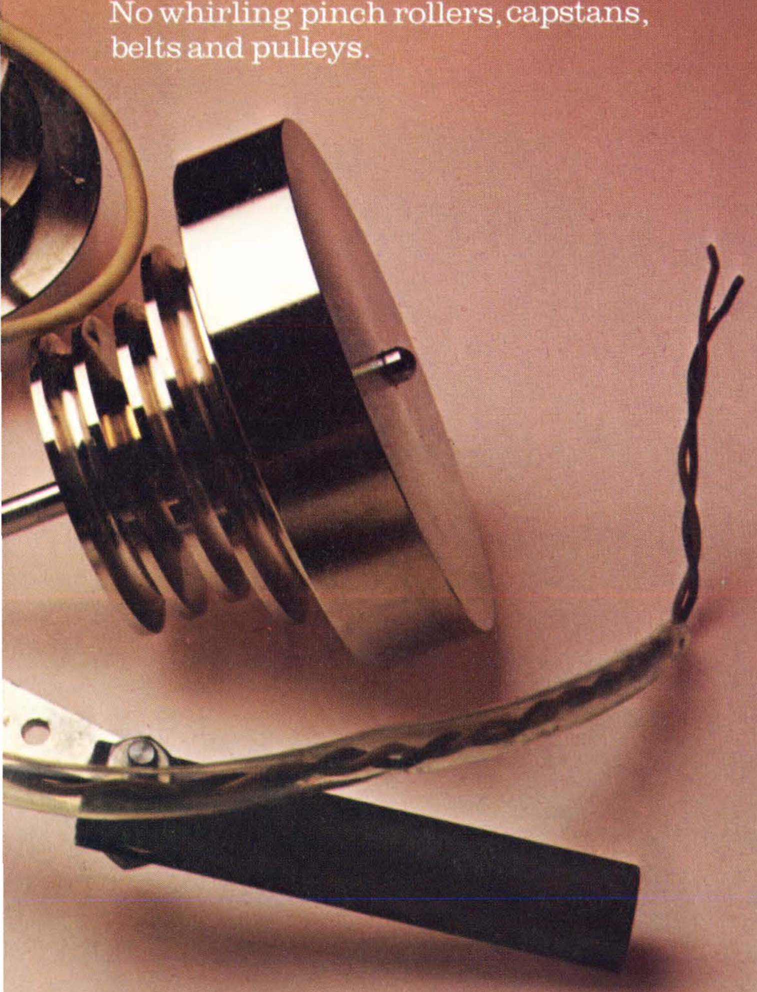
We looked at all the things you hate about cassettes.

And threw them out.








DELAY COUNT
PAGE
CHANNEL A
CHANNEL B
MODEL 532 Logic State Analyzer
PARATRONICS INC
MODEL 70
Serial Interface Probe
BAUD RATE
RTS
CTS
DSR
CD
DTR
RCV DATA
CHAR LENGTH
PARITY
STOP
XMT DATA
PARATRONICS INC.

A.

Selecting A Logic State Analyzer

How Fast, How Wide, How Deep and How Much

Stephen A. Rickman
Paratronics Inc.

Choosing a logic analyzer from the incredible variety of instruments on the market today can bend your mind. Just a first-approximation analysis would have to include categories for timing analyzers, state analyzers, signature analyzers and microprocessor-dedicated analyzers — at the very least. The appearance of multiple function analyzers has marked a recent trend. Some timing analyzers can also display data — for example, the BP Model 50D16 with display formatter. At least one state analyzer, the Paratronics Model 532, offers a form of signature analysis, too.

As a prospective buyer, you may wish to make useful capability-for-capability comparisons between analyzers. Your necessary first step is to narrow the field of selection. Are you concerned with catching hardware problems in a variety of digital equipment? Or do you need primarily an efficient method of tracing data errors in microprocessor-based system? A "yes" to catching hardware problems would point toward an analyzer with a timing display. A "yes" to tracing data errors would indicate some form of state analyzer. If your needs lie between these two extremes, you may want to consider carefully an advanced state analyzer operated in parallel with a moderately-priced timing analyzer as the most cost-effective choice.

Why no all-in-one?

At first a timing analyzer capable of data display might seem to be the best choice. But several trade-offs are involved here. For good state analysis work, you need a wide and deep memory and versatile triggering modes. For good timing analysis, you need a fast and deep memory and special capabilities, such as glitch detection. Asking for everything in one instrument is asking a lot. Besides, the cost shoots up quickly. It is quite possible to buy an advanced state analyzer plus a modest timing analyzer for a lower price than some combined units. Moreover, the state analyzer will probably offer better data-domain performance.

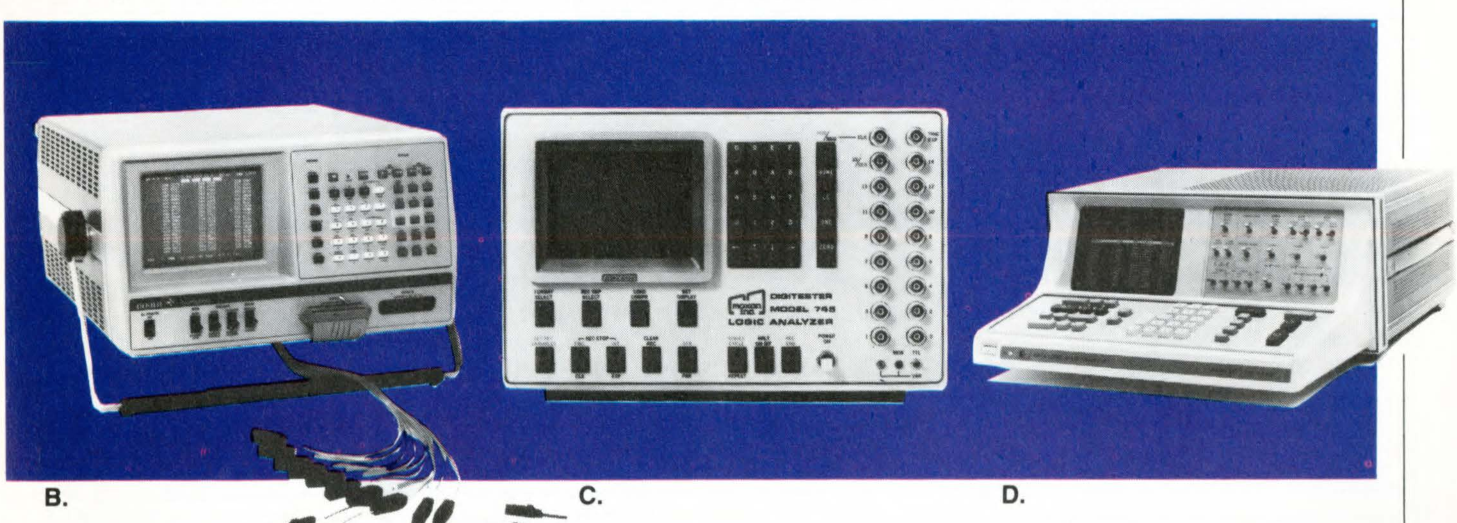
When you need high-quality signal information rather than data analysis, a timing analyzer capable of displaying data may be the best buy. But if your priorities are reversed, you will want to consider an advanced state analyzer, perhaps backed up with a less-expensive timing analyzer. If that is so,

A. Model serial interface probe allows the Paratronics Model 532 intelligent logic state analyzer to test asynchronous RS-232 and 20-mA current loop interfaces.

B. Model K100-D logic analyzer, marketed by Gould's Biomation Div., can handle 16 or 32 signal inputs, offers 100-Mhz clocking, contains a 1024-word memory and provides time and data domain analyses.

C. Moxon's Model 745 logic analyzer contains three separate memories capable of handling 16 parallel channels of 1024 bits or 16,384 bits serially. The depth of memory and the 20-MHz clock rate is useful in diagnosing propagation delay problems that can occur in RAMs.

D. When outfitted with the general-purpose 1026A module, this Hewlett-Packard logic state analyzer allows the user to follow the real-time operation of almost any microprocessor.



B. C. D.

GLOSSARY

Automatic test — a capability of some analyzers that allows the storage of a partial or complete test procedure, plus the expected results, in an auxiliary memory. Tests are then executed with minimal user intervention.

Auxiliary memory — space in memory in addition to the active recording memory. It may include RAM and PROM and is used in comparing data, halting on difference, automatic testing and other functions.

Compare data — any form of display in which a captured data record is manipulated with the data set in an auxiliary memory in such a way as to make differences conspicuous. Two examples: the "exclusive-OR" display and rapid alternation of the display between recording and auxiliary memories.

Data complementation — logical negation of the data at the inputs.

Data compression — any display technique intended to reduce the time or effort required to examine an entire data record. The simplest form converts binary words into hexadecimal words. More effective techniques include:

Address trace — the lot on an oscilloscope/CRT of the value of each word in the record (Y-coordinate) against the sequential position of the word in the record (X-coordinate). A rapid sweep gives a continuous trace characteristic of the data record.

Signature analysis — technique for data compression, in which the entire data record is compacted into one or more hexadecimal words through an algorithm that weights each bit equally. For all practical purposes, this signature is unique to the data and may be compared to a known-good signature.

Data rate — the clock rate for synchronous systems. it must not exceed the specified maximum clock rate of the analyzer.

Delay — user-set for an N-count of selected events. *With parallel or single-event triggering*: After the triggring event has occurred, the analyzer counts down N events before initiating the selected triggering routine. In this type of triggering, the delay is used to offset in time the position of the final data record with respect to the triggering event. *With sequential triggering*: After A occurs, B must occur N events later to initiate a trigger.

Display — provided by most analyzers on a video screen, either through an integral monitor or an external display CRT, frequently an oscilloscope. The data may appear formatted in binary, hexadecimal or decimal words, or in a graphic representation. Some analyzers offer integral LED or hard-copy displays.

Dual-clocking — input organized as two words, each with its own clock input. User may select positive- or negative-going edges for each clock — a necessary capability when the analyzer is used with a microprocessor that multiplexes data and address information on the same bus (for example, the Intel 8085).

Event — a general term for any occurrence originating in the system under test or in the analyzer. It may be used to trigger or to advance the count in the delay function, particularly for data words and clock pulses.

Expansion port — for allowing the user to concatenate analyzers and thereby to increase the input word width.

Halt on difference — the trigger caused by any detected difference, when incoming data is continually compared to the contents of an auxiliary memory.

Memory space — the number of input channels (not counting clock and qualifier inputs), which is the width of the memory and the width of the data word.

Probe — the mechanical interface to the system under test. A basic probe consists of a ribbon cable terminating in a pod with flying leads. The pod contains input buffers and sometimes other circuitry, which can, for example, set the logic threshold.

Qualifier — an additional input, not recorded as data, but used to enable the trigger or the analyzer's clock input.

Record — *used as a noun*: a captured set of data words in memory, available for display; *as a verb*: to store incoming data in memory, including transient storage.

Self-test — the capability provided by some analyzers for verifying quickly that the instrument itself is operating correctly — usually through a form of the automatic test.

Trigger — to initiate the capture of a data record. Loosely, it may refer to the triggering event. *Pre-trigger* means that the captured record consists of data, all or most of which occurred before the trigger. *Post-trigger* means the captured record consists of data, all or most of which occurred after the trigger. Some of the more common types of triggering are:

Parallel triggering — the event caused by the occurrence of a selected word (or simultaneous occurence of two words, like address and data) at the inputs.

Sequential triggering — the event caused when and only when data word B folows data word A by N selected events. N is usually set by the delay function.

Non-occurence triggering — in the sequential triggering mode, means trigger, if any word *other* than B occurs N events after A. It can have meaning for parallel triggering, if the inputs are organized as two words. Then the term means trigger if one word and anything but the other word occur simultaneously.

Trigger output — a synchronizing signal from the analyzer on trigger. It may be used to drive an oscilloscope or any other device.

Variable threshold — a type of probe that allows user-adjustment of the logic threshold voltage reference. User can adapt the analyzer to different logic families or to test noise immunity.

then you will need the nearby state analyzer selection guide, for you aren't out of the woods yet.

The intelligent state analyzer

Logic state analyzers have come a long way from the hard-wired four- or eight-channel data recorders of some five years ago. Microprocessor control of some of the new state analyzers place them in the ranks of "intelligent" instruments. That type of control means programmed functions plus versatility. An engineer at one instrument manufacturer confesses that their latest model offers "solutions to which there are as yet no problems."

Intelligent state analyzers offer these new capabilities: remote operation over telephone lines, automatic- and self-testing, and user-defined functions, which could include microprocessor emulation and printer testing. For example, Paratronics recently introduced its Model 70 serial interface probe that allows its 532 analyzer to record and process data transmitted on an RS-232 line or 20-mA loop.

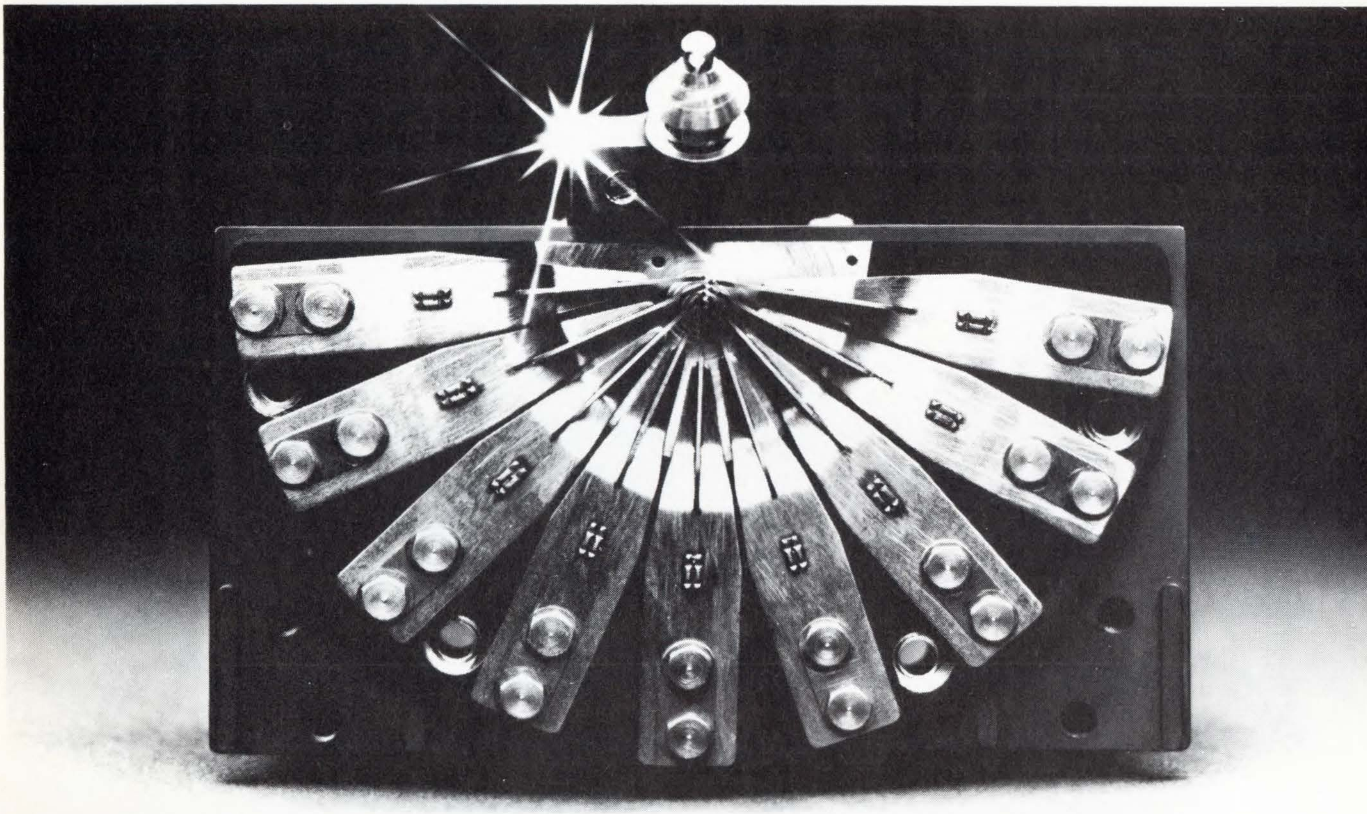
What's it called and who's got it?

But for the comparison shopper, specification sheets glowing with detailed explanations of special capabilities can sometimes perplex the comparison shopper more than they can help. Is the capability really special, or is it just a slightly different version of something everyone else offers?

The lack of a standard terminology adds to the problem. For instance, different makers may give a different name to a particular mode of triggering. Take the phrase "digital delay." In some instrument, this phrase means the ability to introduce into a function a delay of N clock pulses, where N is set by the user. But in other instruments, the "digital delay" can be counted in clock pulses or in selected data words — a significant advantage.

Adoption by the IEC of a recently-proposed standard terminology for logic analyzers should alleviate this mild state

LET'S PUT OUR HEADS TOGETHER.



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Facit 4540 extends this tradition.

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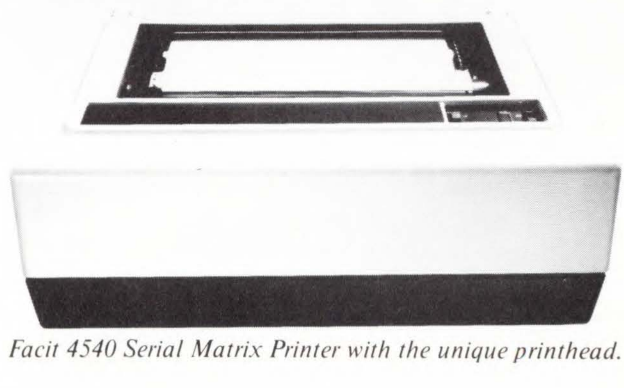

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A Capability and Performance Cheklist for Logic State Analyzers

How to use the checklist: Entries with a question mark require a yes or no answer: others require a word or number. If the capability is optional, also enter the price of the option.

MAKER/MODEL #

RECORDING CAPACITY

No. input channels
Memory depth (no. words)
Max. data rate (Mwords/sec.)
Qualifiers: -Clock (no.)
-Trigger (no.)

TRIGGERING

Pre- and post-trigger?
Sequential triggering?
Non-occurence triggering?
Halt on difference?
Dual clocking?
Delay: -N clock pulses?
-N data events?
-Max. N (no.)

DISPLAY

Scope/CRT (integral or ext.)
CRT formats: -Binary?
-Hex?
-Decimal?
Other integral displays (type)
Data compression (type)
Compare data (type)

SYSTEM INTERFACE

Probes: -Flying lead?
-Card-edge connect?
-DIP connect?
-Other (type)
Probe Z and C
Data complementation?
Variable/settable threshold?
Serial data monitoring?

OTHER FEATURES

Remote operation: -RS-232?
-IEEE 488?
-20 mA loop?
Automatic test execution?
Self-test provision?
User-programmable?
Other desirable features:

PRICE, WITH DESIRED OPTIONS

of confusion a little. Until then, you must read the maker literature with great care to compare instruments.

The nearby do-it-yourself selection chart can help you by directing attention to the most fundamental and the most useful capabilities of logic state analyzers. The nearby glossary defines key terms used in the chart. As you fill in the blanks, keep in mind the four basic yardsticks suggested in the title of this article:

- How fast? At what maximum data rate will the system under test operate?
- How wide? How many channels will you need to catch meaningful data?
- How deep? How much data will you need to capture?
- How much? What will it cost?

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RX02-Compatible Double Density Floppies for the LSI-11/2

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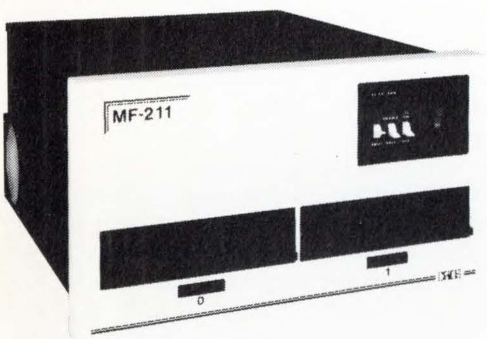

The MF-211 Dual Floppy/LSI-11/2 System, using the CRDS Double Density Controller, is functionally identical to the DEC 11V03-L, but using only 10½″ rack space. The MF-211 is the perfect low-cost answer to your 11V03-L requirement.

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- 30K Addressable Memory
- Considerable Dollar Savings

To go with your LSI-11/2: The FD-211 Dual Floppy System is the perfect plug replacement for your RX02 . . .

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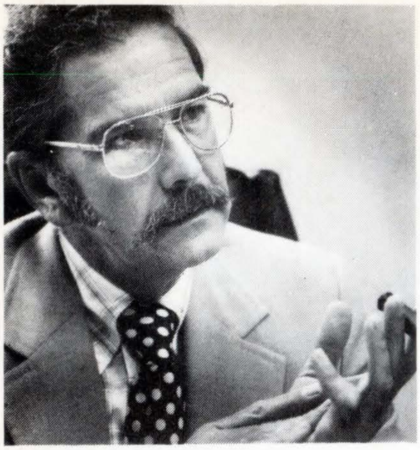


Viewpoint

Charles E. Sporck, President
National Semiconductor Corp.

Predatory Pricing Threatens Our Industry

Japanese companies, operating unfairly in the form of government-supported groups, intend to dominate the U.S. semiconductor and computer industry just as similar efforts have overtaken many other American industries. Unless the U.S. Federal Goverment institutes and enforces fair, free-trade rules for Japanese products, the U. S. semiconductor and computer industry could be destroyed.

Successful domination of markets by Japanese companies has weakened or destroyed the corresponding industry in the U.S. Consider steel, motorcycles, CB radios, television receivers, high-fidelity electronics, sewing machines, calculators and various passive electronic components. They were once thriving segments of the U.S. economy but are now dominated by **Japanese companies which gained control through predatory pricing of goods exported to the U.S.**

Why did these industries fail? Current speculation on the reasons for failure of some of these industries, particularly steel, is grossly unfair. Why criticize steel companies for not investing sufficiently in new plants and processes? Their profit margins were eroded and undercut by predatory pricing of imported steel — pricing which made capital investments impossible! We cannot forget that American companies must either be profitable or cease to exist; and profit was simply not possible when prices of foreign steel were pegged below cost. **Will the computer industry be next?**

Japan's prime economic target today is the U.S. data processing industry. Domination of the U. S. semiconductor market is only part of an overall strategy to gain control of the U. S. computer industry. Japan's Ministry of International Trade and Industry (MITI) organized the computer industry into two groups. Clearly, IBM and every other computer manufacturer in the U. S. is under attack.

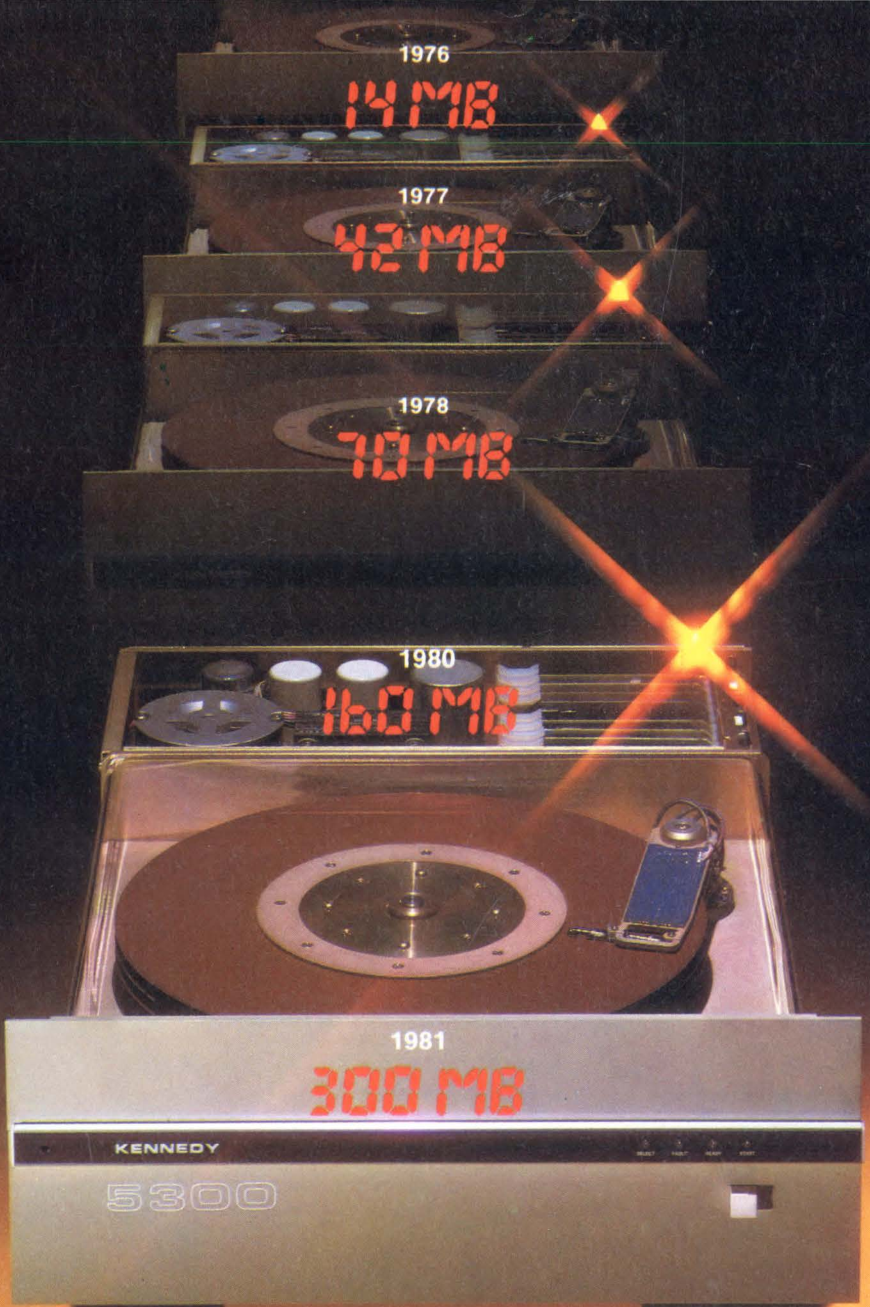
The Japanese semiconductor industry is a formidable competitor because it enjoys business advantages denied to its U.S. counterpart. These unfair advantages include: 1) Higher import tariff in Japan vs. a significantly lower import tariff in the U.S. 2) Japanese firms have easy access to the U.S. market because well-developed and non-captive marketing organizations already exist in this country; on the other hand, our access to the Japanese market is restricted because marketing organizations in Japan are limited, poorly financed and difficult to staff. 3) Since 1973, imports into Japan have increased very little, while exports to the U.S. have multiplied. This imbalance of trade is worsened because imports into Japan are generally restricted to raw materials, while exports to the U.S. consist largely of manufactured goods. 4) Japanese companies are free to establish small developmental companies in the U.S. *for the sole purpose of gaining access to American Technology;* it is next to impossible for U.S. firms to operate this way in Japan. 5) Japanese firms also have easy access to American technology because U.S. patent policies are liberal; Japan's patent procedures, difficult and restrictive. 6) In Japan, semiconductor industry business and technological developments are coordinated by the Japanese government to minimize duplication. In the U.S., no such coordination exists. 7) Large subsidies are provided to semiconductor companies for development work consistent with Japanese government policy and goals. No such subsidies are available from the U.S. Government. 8) Profitability of Japanese companies is not necessary as long as their efforts are consistent with government policy. American companies must either be profitable or cease to exist.

What should we do about this? I advocate equality of trade rules and a balance in conditions rather than protectionism. The U.S. electronics industry is a strong proponent of free trade and therefore is not directly asking for an increase in tariffs on Japanese-made semiconductors. Nor do we favor a government-enforced "Buy American" policy. *We only want all competitors to do business by the same rules.*

Existing trade rules that apply to Japanese products should be modified. A balance of trade agreement should be made in which imports of Japanese-made semiconductor products are equal to exports of the same type of product to Japan. In no case should anything less than equivalency be required.

Our government must convince Japan to equalize the tariff which it levies on semiconductor imports. Furthermore, the capital gains tax structure in the U.S. should be liberalized to provide incentives for companies to take risks on innovative technologies that would otherwise go untried. Tax credits and accelerated depreciaton schedules should be provided for increased R & D and capital investment. In addition, funds should be granted for development of advanced production equipment.

These responses by Government would help but not resolve the fundamental problem: our economy — based historically on free non-monopolistic trade — is faced with a planned, controlled economy as a direct competitor. The disadvantage is formidable. No less formidable is the disadvantage faced by semiconductor users, particularly firms operating in the computer industry. It is unwise for equipment manufacturers in the U.S. to do business with Japanese companies which intend to become formidable competitors bent on capturing their markets. If your firm is doing business under these conditions, it is especially dangerous because your suppliers are also your competitors — but who can operate with an unfair trade advantage.



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