VOLUME 9, NO. 4

APRIL 1979

# Digital Design

The Magazine of Systems Electronics


## Capacitance Keyboards:
## A Look Beyond μPs

**Software: μCs vs. Minis**

**μP Selections: Do's and Don'ts**

**Pro**

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CIRCLE 1


µSA READY
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# THIS MONTH

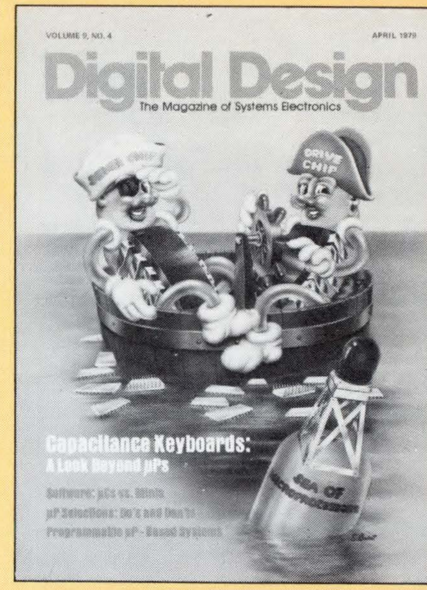
April 1979
Volume 9, No. 4

## Features

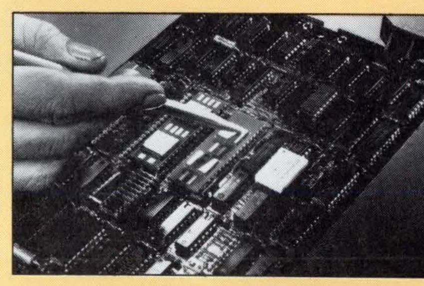


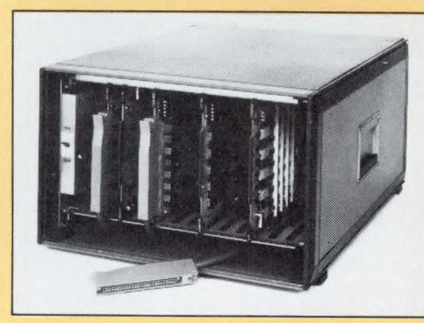
## Departments

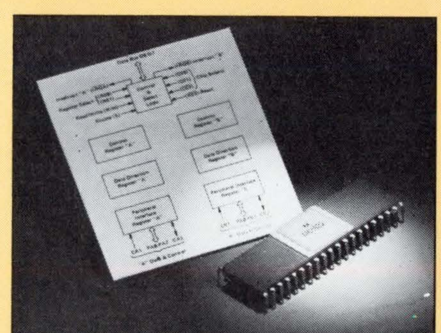





**ON OUR COVER**
We thank Key Tronic for this month's imaginative cover.







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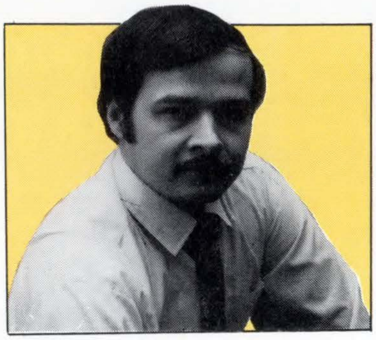
# SPEAKOUT

Paul Snigier, *Editor*

# CAN YOU AFFORD NOT TO?



As an editor, I miss designing circuits and seeing design prototypes finally function successfully. Keeping up with the state-of-the-art took a lot of effort. Although graduate courses and books available three years ago were mediocre and of little practical value for shirt-sleeve designers, I found the magazines were far better; and for a time, the only lucid and reliable design information on microprocessors came from electronic magazines.

But electronic magazines can provide you with other benefits: product information through New Product writeups and advertisements from a valuable-but-free editorial service — **Reader Inquiry Cards**. Take advantage of it.

Why do I say this? By methodically setting up a deliberate procedure to use electronic magazines to your advantage and using Reader Inquiry Cards (RICs), you can systematically build up invaluable and comprehensive subject files. Do this systematically. Before looking at the table of contents or reading any article, first look at the New Products and product advertisements and circle the number (on each page) of those you're interested in. Do this as you quickly page through the magazine from cover to cover. Next, tear out the RIC, go back to the front of this magazine and flip through the pages, circling the corresponding RIC numbers on the card. Since you will have already circled the ad numbers on our pages, this procedure will be quick.

So, how should you decide to circle New Product or advertisement numbers? It begins with your priorities. By setting long and short range design priorities continually, you should already know what is important to you; and it will then be easy to mentally divide hardware and software products into the following three categories — A, B or C — depending upon order of importance.

**A-Priority Products** are products of immediate interest to a present or impending application. There is no question about A-Priority Products: these attention-getters stand out clearly in contrast. Since you need an immediate response, call direct to the phone number listed in the advertisement (or New Product).

**B-Priority Products**, although of less immediate value to your project, hold a strong interest. Circle these numbers. When this material arrives, place it into a folder in your files. By experience, I found duplex-numeric filing (by digits and letters with a card index) best, as it gave unlimited expansion and cross filing capability without the limitations of alphabetic filing. You may find another filing system better, so this is an individual matter.

**C-Priority Products** are of marginal interest. Should you neglect them? No! Here you should follow an inflexible rule on circling advertisement (and New Product) numbers — "When in doubt, circle it." Why agonize over a decision. Remember, any danger of getting irrelevant material is far offset by the mere ten seconds that it takes to circle that number. Why gamble?

Do other engineers know something that you don't? They do if they're building up reference/data files and you're not. Can you afford not to?

Paul Snigier

# TECHNOLOGY TRENDS

## Electro 79: µCs Will Predominate

This year Electro returns to New York City on Tuesday, Wednesday and Thursday, April 24-26. Electronics in the opening years of the 1980's and its expected impact on industry and individuals will be the focus of Electro/79. The high-technology show and convention, including three days of exhibits and technical presentations preceded by a day long marketing seminar, will be staged at the New York Coliseum and the Sheraton Centre (previously known as the Americana Hotel).

More than 30,000 design engineers, managers and technical executives are expected to attend hearing over 100 presentation and visiting exhibits on three floors of the Coliseum and professional program sessions in the Sheraton Center.

The Professional Program, with an average of four speaker presentations at each technical session, will delve into subjects such as communications satellites, memory, fiber-optics, energy management, LSI, computer imagery and microprocessing. Microprocessors will steal the show; more presentations are on micros than any other topic. The technical program has been developed and organized and will be presented by engineers, scientists and professional experts. Professional program sessions will be held at 10 AM and 2 PM Tuesday through Thursday.

Exhibit booths will total more than 700 with over 400 companies introducing and displaying products and systems — from microelectronics, EDP peripherals, fiber-optics, components, instrumentation and control systems to production, packaging and test equipment and mini and microcomputers.

Exhibit show hours will be from 9:30 AM to 6 PM, Tuesday, April 24; 9:30 AM to 7 PM, Wednesday, April 25; and 9:30 AM to 5 PM, Thursday, April 26.

And if your feet get tired from covering the exhibits, why not stop by the Electro Film Theater? Scientific and engineering motion pictues will be shown from 10 AM to 4 PM each day of Electro. The Film Theater offers a series of motion pictures on technology — from space to the microprocessor — which have been produced by electronics companies and selected by a panel of judges.

The Electro special theme exhibit — Microprocessor Applications Awards — will feature winners and finalists in competition to determine effective usage of the µP in industrial and consumer products. The exhibit, on the third floor of the Coliseum, should prove interesting; it will display µPs in a wide range of functions —from office equipment, automotive use, production controls, and medical applications to sports, home appliances, research and testing, and energy conservation.

Entries are expected in many areas, including:

- office equipment and devices
- automotive and motor sport
- process and quality controls
- home computers
- medical applications
- marine, aviation, navigation
- sports and leisure time
- commercial applications
- home appliances and devices
- production controls
- energy conservation applications
- games, toys and recreational
- communications
- research and test instruments
- computer peripherals
- educational and teaching
- software and programs

A panel of judges, drawn from industry and public life, will select products for awards of excellence and merit. Criteria includes effectiveness, popularity, state-of-the-art, originality, inventiveness and cleverness.

Emphasis will be on the buyer of electronic products at the Electro Marketing Conference to be held on Monday, April 23, at the Sheraton Centre. An all-day seminar will explore the buyer's role and how he operates with manufacturers, distributors and representatives.

In the morning session, buyers will explain problems and procedures for making purchasing decisions. In the afternoon, presentations by manufacturers, distributors and representatives on their approaches and their methods of helping their customers will include examples of when the buyer can better go directly to the manufacturer and when he can benefit by working with a distributor or rep.

Conversely, the Conference will examine circumstances when a distributor or rep should deal with a buying problem and when the purchasing agent should be advised to contact the manufacturer directly. Participating in the Marketing Conference will be the Electronic Representatives Association, National Electronic Distributors Association and the Electronic Industry Association.

The Conference will begin with a continental breakfast at 8 AM and the first seminar session at 9 AM. The afternoon meeting, starting at 2 PM, will follow the Electro Keynote Luncheon, which is included in Marketing Conference registration.

"Shuttle Into the Eighties" sets the tone for the Electro All-Industry Reception Tuesday, April 24. The traditional party, expected to attract 700 to 800 Electro attendees, will feature aerospace equipment, space games and a robot attuned to the new space programs of the coming decade. The Sheraton Centre's Imperial Ballroom will be turned into its own version of a space shuttle for the 6:30 to 8:30 PM. Reception which salutes the technology on display at Electro. Tickets ($10 each) will be available at the door.

The Electro sessions will cover quote a spectrum of topics, from micros to management. Here is a rundown of the sessions.

Session 1, "Keys to Successful Engineering Management," focuses on four important topics to the engineer/manager: The problems of stress, motivating creativity, cost controls, and management of personnel. The program has been prepared for Electro by the IEEE Engineering Management Society.

Session 2, A/D LSI, covers a new type of semiconductor device — one which combines complex linear and digital functions on the same chip. One chip micros with on-board ADC, microprocessor-compatible A/Ds, and Codecs are representative of these new products. This session will cover processes (CMOS, NMOS, $I^2L$, laser trimming) and circuits (A/D, D/A converters, comparitors, amplifiers). The speakers will also discuss existing and future applications, economics considerations, accuracy and performance.

Session 3, Marketing Personal Computers, identifies the potential market, designing the product to fit the need, and merchandising high-technology machines in retail stores represent the new challenges in personal computing. Financial, manufacturing and retail experts offer their insights into a potential billion-dollar marketing puzzle.

Session 4, Software Manufacturing in the Distributed Environment — Theory and Practice, is based on reasons why "methods of software generation will have to change from "customized" or "packaged" approaches to manufactured items". Methods of manufacturing software will be discussed.

Session 5, Space Surveillance Technology, describes a major progam testing feasibility of radar operations from space in a multimission, wide-geography surveillance system, including work in both optical and microwave technologies.

Session 6, Plastic Packaging for EMI Shielding, shows how the EMI problem in electronic devices packaged in plastic enclosures has become of increasing importance. In many cases, it is impossible to predict accurately the working environment to which a device might be subjected during its lifetime. A major purpose of this session will be to provide background informatoin to enable designers of electronic devices packaged in plastic cabinets to shield effectively on the design end, in order to preclude an EMI problem later.

Special Session: The Electro International Leadership Panel is an Electronics Executive Forum On World-Wide Problems and Opportunities. Major electronics executives from the United States, Germany, Holland, Japan, and other countries will participate in a panel session covering state-of-the-art electronic devcies and systems development in their respective countries and regions.

Session 7 is The Engineer and Public Policy: Servant, Guardian, or Gadfly? Most engineers are employees, and their professional responsibilities lie in designing products or performing particular services. How can engineers, therefore, safeguard the health, safety, and welfare of the public? How can they influence policy in these areas?

Session 8 is Advances in Digital Signal Processing: Hardware and Techniques. In the course of the past three years a significant migration has begun from the classical analog techniques of signal processing to their digital counterparts. While the advantages of working in the digital domain have been well-known for many years, the scope of applications has been limited until very recently when LSI capability made the concepts physically and economically viable. This movement represents a revolution in many fields, especially telecommunications, radar, sonar, voice and video processing and medicine, to name a few.

**Electro/79 Sessions at a Glance**

| | | | | | | |
|---|---|---|---|---|---|---|
| **Tues., April 24 10 a.m.** | 1. Keys to Successful Engineering Management | 2. A/D LSI | 3. Marketing Personal Computers | 4. Software Manufacturing in a Distributed Environment | 5. Space Surveillance Technology | Plastic Packaging for EMI Shielding |
| **Tues., 1 p.m. Special Session: International Electronics Executives' Forum** | | | | | | |
| **Tues., April 24 2 p.m.** | 7. The Engineer and Public Policy | 8. Advances in Digital Signal Processing | 9. The Personal Computer: Hobby Horse or Work Horse | 10. $\mu$C Data Base Systems | 11. Adaptive Antennas | 12. Non-Ionizing Radiation on Man |
| **Wed., April 25 10 a.m.** | 13. Engineering and Purchasing: Chaos or Co-Existence? | 14. Logic Analyzers as Tools in Developing Processor Systems | 15. Desktop Computers | 16. Reducing Risks in $\mu$C Development | 17. Edison Centennial | 18. Bomb and Weapon Detection Technology |
| **Wed., April 25 2 p.m.** | 19. Corporate Ventrue Capital | 20. Impact of 64K RAMs on the Computer Indus. | 21. Electronics in the Graphic Arts | 22. Self-Testing Instrumentation | 23. RF Communications, Present and Future | 24. Environmental Monitoring and Assessment |
| **Thurs.. April 26 10 a.m.** | 25. Women on the Steps of the Electronics Pyramid | 26. Non-Volatile Storage for Small Processors | 27. $\mu$C Industrial Control Networks | 28. Batteries for Modern Applications | 29. Interactive Telecommunications Systems in Social Uses | 30. Engineering and Economics |
| **Thurs., April 26 2 p.m.** | 31. Minorities in Engineering | 32. Testing Bubble Memory Devices | 33. Advanced Automation | 34. The Future of Switching Power Supplies | 35. Latest Advances in PCB Testing | |

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| Nova 1220 | PDP-8/F | PDP-11/40 | 620/L-100 |
| Nova 1230 | PDP-8/M | PDP-11/45 | 622/i |
| Nova 2/4 | PDP-11/04 | PDP-11/50 | V-71 |
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Session 9, The Personal Computer: Hobby-Horse or Work-Horse? Sales of personal computers have gone from nowhere four years ago to in excess of 200,000 units in 1978. Sales in 1985 are projected to be 5 billion dollars. The most often asked question today is "But what are people doing with those things?". That's what this panel session is all about. First there will be a brief overview of the range of applications for personal computers and where they are being used. Next our panel members will describe what they are doing with their computers, followed by questions from the audience.

Session 10, Database Management Systems on Microcomputers, the emergence of microcomputers has brought low-cost dispersed application to data processing. This session reviews the impact of microcomputers on database management systems. Several research and commercially available database systems on microcomputers will be reviewed. The application of these systems to distributed processing, front-end/back-end architectures, and office automation will also be assessed.

Session 11, Adaptive Antennas, discusses trends and applications of analog, digital, and hybrid array processing techniques, development of adaptive algorithms, circuit and component design, and implementatin of adaptive antenna systems.

Session 12 is Non-Ionizing Radiation on Man. There is a great deal of interest and controversy about the effects of electromagnetic energy on man. This session will present the facts on all aspects of the subject.

Session 13, Engineering and Purchasing: Chaos or Coexistence? is a panel, and the objective of this session is to develop suggestions for improving cooperation between the engineering function and the procurement function to enable firms to bring to market high quality products with the best price/delivery. Representatives from design engineering, manufacturing, and purchasing will participate.

Session 14, Use of Logic Analyzer Tools in Development of Processor Systems, covers the role of logic analyzers in the development of processor systems (from minis to mainframes) in three case histories — plus a projection of how logic analyzers will affect both software and hardware development in the future.

Session 15 is Desktop Computers. Demand for low-cost, versatile desktop computers for small-business and engineering applications is growing almost faster than the industry can respond. The burgeoning market, the technology, and the wide range of applications are presented in this session.

Session 16, Reducing Risks in Microcomputer Development, claims that these risks are getting larger — not smaller. The problems being addressed are more difficult: LSI devices are growing more complex and software complexities are rival to those of larger minicomputer systems! However, there are ways to manage the risks. This session will address what some of the major risks are and offer practical suggestions for minimizing those risks (or, at least, their impact).

Session 17, Thomas Edison: Magician, Electrician or Engineer?, is part of the Centennial of Light Celebration, commemorating the 100th anniversary of Edison's invention of an electrical lighting system.

Session 18, Bomb and Weapon Detection Technology, should increase awareness in the technical community of the requirements, problems, state--of-the-art and opportunities for innovative products in the areas of bomb and weapon detection technology. The session will present a concise statement of the requirements followed by summaries of the state-of-the-art in several areas of current research and development.

Session 19 is Corporate Venture Capital. For a variety of reasons, more US companies have become active as risk/venture capitalists in new electronics enterprises. This session explores the differing motivations for these investment moves, both from the corporate manager's viewpoint and that of the employed engineer with entrepreneurial ambitions.

Session 20 is Impact of the 64K Dynamic RAM on the Computer Industry. In the past, density increases in RAMs have resulted in significant changes in the computer industry. The resultant cost decrease and density increase has broadened the products available as well as increasing the tasks performed. This session will discuss the impact of memory on the evolution of computer architecture as well as the impact of the 64K generation.

Session 21, The Role of Electronics in the Graphic Arts, covers the revolution in the printing industry. Mechanical crafts have been superseded by electronic typesetting, electronic press controls, with communications used for the transmission of images to be printed. This session will provide a detailed overview of the contemporary printing industry.

Session 22 is Self-Testing, Checking, and Calibration in Instrumentation. Self-testing, checking, and calibrating instruments offer three basic features — economy, confidence and reliability. The first paper will stress the economy of the self-testing approach and is followed by three examples of the implementation (including both hardware and software).

Session 23, Modern Design and Concepts for RF Communications, will impart circuit and concept data of importance to engineers involved in RF communications design and application, both military and civilian. The material treats modern and future trends in design and application from low frequency to the microwave spectrum. Visual graphics will be employed during each paper, illustrating the subject matter in a clear and persuasive manner.

Session 24, Environmental Monitoring and Assessment, reviews on-going work in monitoring and assessment of airport noise, low-level radiation, satellite data acquisition, particulates in the atmosphere, and "acid rain".

Session 25, Women on the Steps of the Electronics Pyramid, asks: "Have women in electronics really come a long way?" Four accomplished professionals in electronics engineering, technical marketing, and product management will address the many problems and not-so-many opportunities in reaching higher levels on the pyramid. The session is planned for audience participation. Short papers will be followed by a panel session.

Session 26, Nonvolatile Storage for Very Small Processor, deals with the problem of providing nonvolatile storage for micro- or small miniprocessors for which total system cost must be kept low. Topics to be included are EPROM, NMOS, battery backup of volatile semiconductors, bubbles, minicassettes, and minifloppies.

Session 27, Microcomputer Industrial Control Networks, brings to the forefront some of the problems systems architects face when designing an industrial control network now that microcomputer products are becoming relatively inexpensive to incorporate into a network. It is important that management-level executives be made cognizant of the wave of network applications expected in the 1980's, the class of problems that might be encountered, and the increased productivity envisioned utilizing the network concepts.

Session 28, Batteries for Modern Applications, offers useful application information on portable battery power from the relatively mature, proven and well established technology of sealed nickel-cadmium to a unique and innovative approach to lead-acid in the rechargeable battery field and to the very recently developed technologies of zinc-air and lithium batteries for practical applications.

Session 29 is Interactive Telecommunications Systems in Social Uses. Many efforts have been made to realize the potential for non-broadcast telecommunications in business, education, health care, and government services. But there have been more failures than successes. This session suggests answers to the key problems and presents some case-histories.

Session 30 is Engineering and Economics: You Can't Have One Without the Other. The economic viability of a product or system is often won or lost on the design engineering drawing board. Understanding the axioms and the tools of economics is an essential ingredient in career advancement; and how the engineering dollar is spent can make or break almost any project. This session focuses on the essential interfacing between engineering and economics — what every engineer needs to know and often doesn't.

Session 31 is Developing Minority Participation in Electrical Engineering. Present and emerging plans and programs for making electrical engineering education available to promising minority students, and development of career opportunities for them after graduation, will be discussed by company, foundation, government and educational specialists in this field.

Session 32, Testing Bubble Memory Devices, defines problems and solutions. Testing bubble memories presents very different problems than those encountered in test procedures for present-day semiconductor memories.

Session 33 is Advanced Automation. Programmable systems to assemble manufactured products, development of a two-level language as a task-organizer for manufacturing "manipulators"; work in control automation using smart sensors; and development of data structures for sensor-controlled industrial robots, will be covevered in this session. A color film will be included,

*Continued on p. 79*

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# SOFTWARE: MICROS VS. MINIS

**Ken Schroeder**
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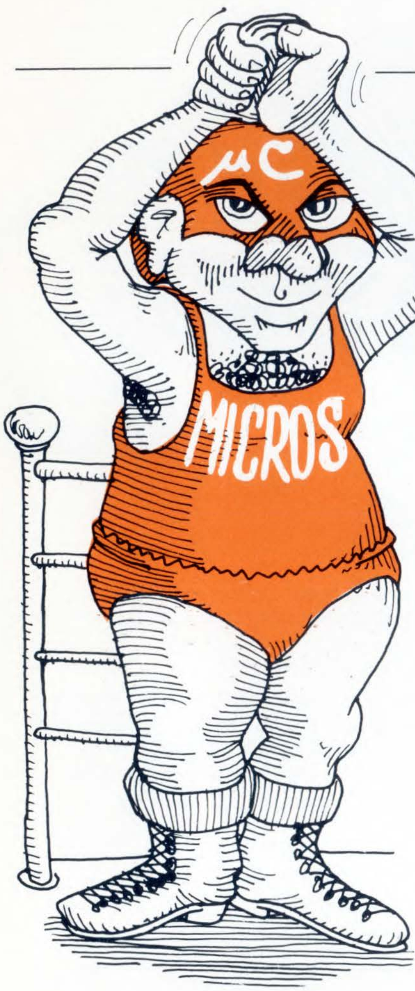


Designing and implementing software for the microcomputer and the minicomputer are significantly different activities. Underlying the obvious similarities in the primary function of the software are important differences. Specifically, these two kinds of software are required to run on appreciably different hardware **(Table 1).** They are required to perform applications of considerably different character. Also, they are written, edited, and debugged using different methodologies. The importance of these differences is not necessarily obvious to the uninitiated and the effects can become more or less significant, depending upon the specific hardware systems and applications under consideration. However, it is useful to generalize about these differences to understand what one may face when attempting to program a microcomputer for the first time after having had experience in programming minicomputer (or midi-computer) systems.

## Hardware differences affect software

Microcomputers have traded computing power for economic and size advantages. Microcomputers are generally less expensive and smaller hardware systems than minis, and therein lies their utility. Micros can bring intelligent control to applications that either do not need, or cannot justify, a larger, more expensive minicomputer **(Fig 1).** However, this economic and size advantage is gained at the expense of computing power and hardware facility. This sacrifice is reflected in the microcomputer's software. A microcomputer programmer must often compensate for hardware limitations in software. Often the most significant hardware limitation is execution speed. However, even in applications requiring only modest computational speed, many other missing hardware resources must be compensated for in software, thereby lengthening and complicating the programming task.

Micros predominantly have shorter data words than minis do. A computer's data-word size is its fundamental data representation. It specifies the number of bits that can be stored into or retrieved from its main memory during a single memory cycle. (Even "bit" manipulations are usually word-addressed.) Generally, the larger the data word, the greater the efficiency and power of a processor's internal operations.

The majority of microcomputers have either 4-, 8- or 16-bit data-word lengths. The 8-bit version presently dominates both the marketplace in dollar sales volume and current microprocessor-based design. This is partially because a byte (8 bits) is a convenient data representation for many micro applications. More significantly, however, the 4-bit versions have very limited data-handling capabilities and the 16-bit versions are considerably more expensive. Sixteen-bit micros are primarily selected to provide software compatibility with minicomputers for which software has already been written or for applications in which software compatibility with a mini is of paramount importance. However, as

microcomputer prices continue to decline, the 16-bit machines will become more competitive and will become more widely used.

The minicomputer is commonly available in 12-, 16-, 18- and 32-bit versions. The 16-bit-version mini dominates the market because it conveniently allows a larger data representation than the 8-bit micro, yet allows efficient byte handling when required by packing two bytes per data word. Many minis also facilitate byte addressing of memory to enhance their byte-handling capabilities.

Micros characteristically have smaller instruction sets. Normally, a machine's instruction size is a small multiple (1, 2 or 3) of its data-word size. The instruction size is a direct indication of the computational power and size of a machine's instruction set. (This is the set of instructions directly executed by the hardware.)

The microcomputer, usually having a smaller data word, thus also has a smaller instruction size, limiting the power of its instruction set. The micro usually has fewer instructions, less powerful instructions, fewer memory addressing modes, and fewer data types that can be handled directly by the hardware. Thus, the microcomputer program requires more assembly-language instructions than the equivalent program implemented on a mini. This makes assembly-language programming a more tedious, less efficient, and more error-prone task for the micro than for the mini.

Memory addressing can be inefficient with micros. One memory-addressing limitation problem encountered with micros and not with minis is "out-of-page" reference errors. A microcomputer often has "paged" memory, i.e., memory is divided up, for addressing, into blocks or "pages" and some of the micro instruction formats can only reference memory locations within the same page as the instruction. This technique of addressing is used to limit the number of bits required to specify an operand's address. However, when an attempt is made to reference, within one of these short instructions, a location outside the current page of memory, an "out-of-page" reference error occurs. This restriction can be avoided by using indirect addressing or using full-address instructions. These techniques, however, create inefficiencies in execution speed or memory space and may not be desirable to use throughout a program. Anticipating and compensating for this addressing restriction complicates the writing of micro software.

Because micros have fewer general-purpose registers, intermediate results must often be swapped back and forth to memory. Another feature of microprocessors that limits their computational power in comparison to the mini is their limited internal register sets. Normally, the micro has fewer hardware registers for use as accumulators or index registers. This can necessitate frequent saving and re-storing register contents into main memory to save intermediate data results or address pointers. This required swapping of information not only slows down execution speed, but forces the programmer to keep track of where such information is being stored and determine what allocation of those registers will minimize that program overhead.

Since micros have less computational hardware, more operations must be done in software. The micro usually lacks other computational hardware features that many minis use to speed execution of complex numerical calculations. Such hardware includes hardware multiply and divide (single and double precision) and multiple position shift facilities. Also missing are floating-point hardware facilities. Such operations must be done in software and become the responsibility of the programmer, thereby complicating his task. This added code can also considerably lengthen the program.

The stack facility available on many micros is limited, in contrast to the ones on standard minicomputers. The micro's stack often requires the explicit handling of both the stacking data and the stack pointer register. A few micros implement a stack pointer register. A few micros implement a stack in a separate small memory space within an organization that effectively has an open bottom. Once the stack is filled, any attempt to push additional

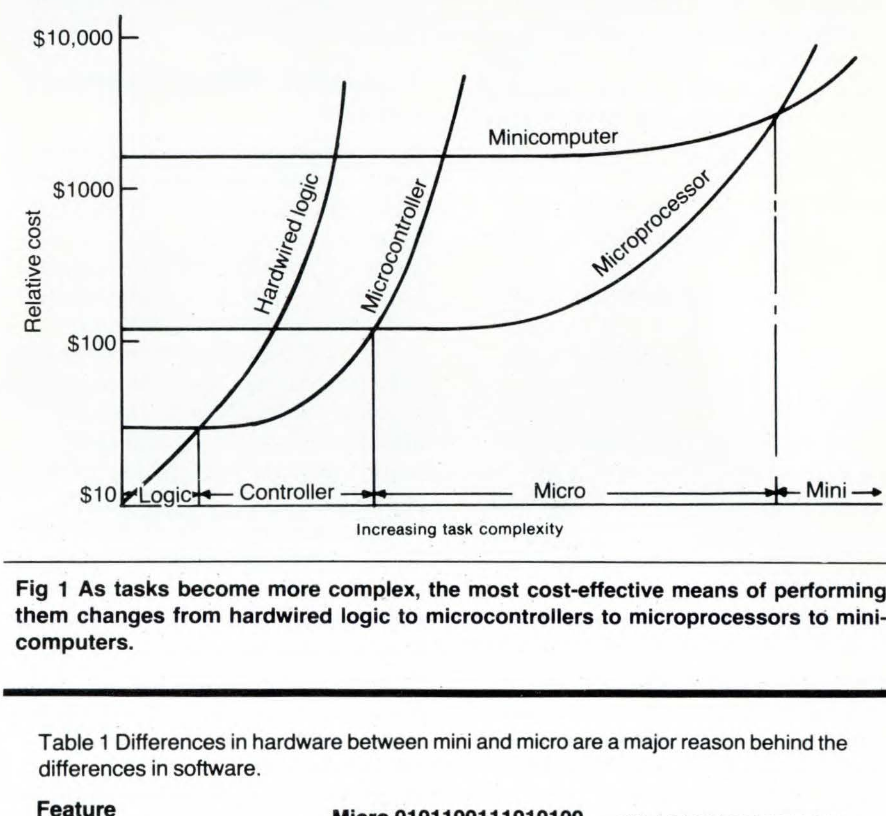


**Fig 1 As tasks become more complex, the most cost-effective means of performing them changes from hardwired logic to microcontrollers to microprocessors to minicomputers.**

Table 1 Differences in hardware between mini and micro are a major reason behind the differences in software.

| Feature | Micro 0101100111010100 | Mini 010110011010110 |
|---|---|---|
| Data-word size (bits) | 4, 8, 16 | 12, 16, 18, 32 |
| Execution speed (cycle time) | Slow (500 ns - 10 $\mu$s) | Medium-fast 200 ns - 1 $\mu$s) |
| Addressable memory | Small-medium (512-64k bytes) | Medium-large (4k-128k words) |
| Instruction repertoire size | Smaller (30-150 typical) | Larger (70-300 typical) |
| Assembly-language programming | Tedious, slower | More efficient, faster |
| Interrupt capability | Single-level static priority | Multi-level dynamic priority |

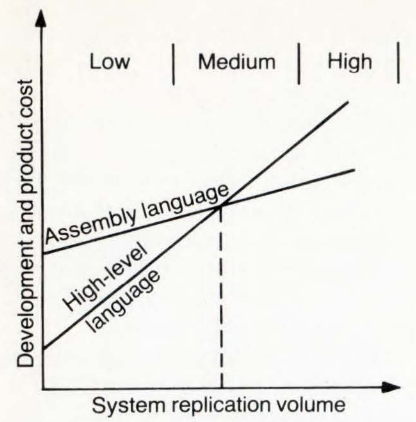


**Fig 2 The choice of language level used in a software system depends on replication volume of system. Assembly language generates more efficient code than high-level languages, and so requires less memory. Assembly language, however, requires more programming effort.**

data onto the stack will destroy the first entry on the stack without any warning or hardware protection. In this organization, the size of the stack memory absolutely limits the depth of the stack. This stack limitation may restrict subroutine call nesting or the permitted level of context switching that the computer can handle, since these actions normally require entries on the stack.

In contrast, minis normally implement their stacks in main memory, which gives virtually unlimited stack depth. On many minis, when an attempt is made to overflow the permitted stack area, a hardware indication is generated. This permits software to detect such an occurence and take appropriate action. Many minis have implicit stack-handling and will adjust stack pointers automatically. Some minis have facilities that automatically stack the program state upon interrupt or other context switching. Thus, using a stack facility on a micro generally requires more code and is more complex to program than on a mini.

Microcomputers generally have relatively primitive interrupt-handling structures. Micros commonly only have a single level of hardware priority and often lack a vector-generation capability. In contrast, minis commonly have multi-level dynamic priority-arbitration schemes and also frequently have vector-driven response systems. When implementing an application requiring significant interrupt-response capability using a micro, the programmer must make up for this lack of hardware facilities in software, thereby complicating his programming task.

Microcomputer systems usually need external equipment for debugging. Certain computer hardware features are often helpful when debugging software and diagnosing software failures. One of these is a hardware "trap" – vectoring the program to a specific address in memory upon the occurence of a predefined machine state. The attempt to execute an illegal instruction or address nonexistent memory are examples of "trap"-generating occurences. These "trap" features are standard on minis but are lacking on micros. The microcomputer programmer cannot, however, really compensate for them in software, so this function in the debug phase of software usually must be replaced by the use of a logic "analyzer" or other external debug hardware. The microcomputer programmer should become familiar with the use of such devices.

## Application differences affect software

Attempts to save memory costs often lead to complicated unstructured programs. Microcomputers are customarily applied in very cost-sensitive applications. Typically, these are applications with moderate-to-high-volume system-replication requirements, where small individual economies reap large total savings. Minis, in contrast, are more typically used in low-to-medium-replication-volume applications, which are not typically as cost-sensitive.

Approximately 60% of the cost of the average microcomputer system, in final application configuration, is memory cost. Since assembly-language programming can generate code that is more memory-efficient than compiler-generated code, it tends to dominate micro programming **(Fig 2)**. A determined effort is usually made to squeeze the required software into the minimum amount of memory. This activity is commonly called "bit-bumming." However, recent efforts to bring modern engineering techniques to the "art" of writing software has led to the foundation of a new branch of study called "software engineering." This new discipline has shown that "bit-bumming" and other software techniques that sacrifice code clarity and structure to minimize program space have serious side effects in programs of any significant size. Specifically, such efforts lead to the production of unstructured programs, which are difficult to debug, difficult to understand. Such programs can create very expensive support problems and can only be cost-effective in applications with very large replication volumes and applications that will remain very stable and will not be modified or extended after initial completion. Since this is the environment in which many microcomputers are used, "bit-bumming" is a skill often required by microcomputer programmers. This is especially true since saving a few bytes can potentially reduce the number of memory chips required **(Fig 3)**. Memory efficiency is not as crucial in typical mini applications. Additionally, memory for minis normally is only available in 4-k word quantities, so unless this increment boundary is avoided, no cost savings are realized by reducing memory requirements.

Because microcomputers usually work in a dedicated task environment, the programmer must write software normally handled by the mini's supervisory software.

Microcomputers are primarily used in dedicated single-task programming applications. Normally, software in such an environment controls the base-machine hardware and is not integrated into an existing operating system or standardized software monitor. The microcomputer programmer dir-

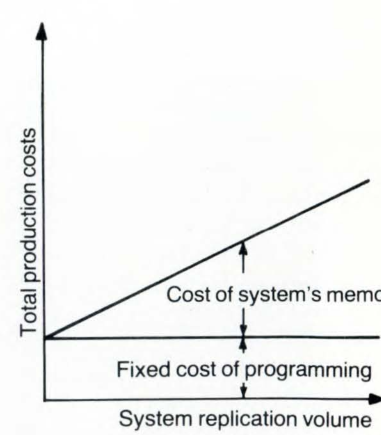


**Fig 3 Cost to deliver a system depends on both programming and memory costs. (Slope of memory costs may vary with price breaks for volume purchases.) Since saving a few bytes can potentially reduce the number of chips required, "bit-bumming" becomes a necessary evil for microcomputer programmers.**

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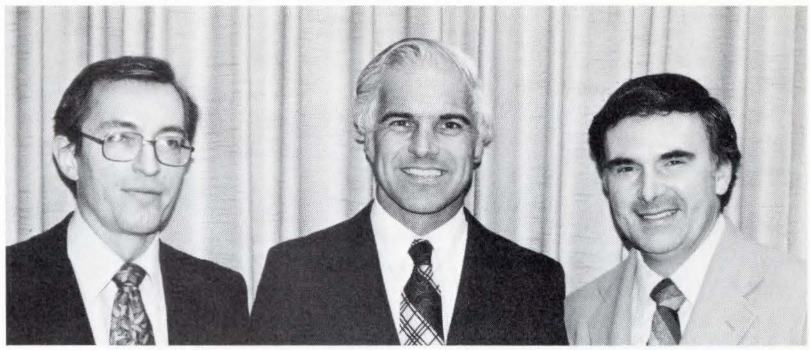

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ectly programs all software functions normally handled in a mini by such supervisory software. For example, the maintenance of the system clock and the control of all peripheral devices are the programmer's responsibility. Normally, a microcomputer system has fewer computer peripherals to handle than a typical mini system; however, the nature of these peripherals is appreciably different. Typical minicomputer interfaces make peripherals appear logical and time-independent, i.e., all the software operations required are clearly logically related to obvious functions of the device. Typical micro devices have simple controllers, which require more detailed software control and can impose serious timing constraints upon the program in controlling the hardware – constraints which, if violated, can cause serious and difficult-to-isolate intermittent problems.

Suitable "off-the-shelf" application program packages are not often used with micros.

Applications involving minis often use various mathematical and application software packages available from the hardware manufacturer to facilitate system implementation. Also, many mini programmers write general-purpose software packages for a particular application area and use them repeatedly in subsequent applications to improve software-development efficiency. In the micro world, such generalized packages are rarely used in final product configurations. More characteristically, concise and efficient code is written for each application and is customized for maximum efficiency for the individual case, thus making programming less efficient and driving up software development costs.

Programmers have to make sure that the relatively slow micro systems are not too slow for the task at hand.

Micros are generally put to work in applications for the monitoring, analysis, and control of time-dependent (real-time) processes. Since micros have slow execution rates, it is often necessary to write very efficient programs to meet performance requirements. Programming in high-level languages has been shown to be much more efficient than programming in assembly language and so is rapidly dominating mini software. Assembly language, however, still dominates microcomputer programming in order to meet execution-speed requirements, since compilers do not yet generate very efficient code. The attempt to save execution time has an equivalent activity to "bit-bumming" – using similar unstructured programming techniques that minimize the execution time of programs but at the expense of clarity. This approach has the same inherent program-debugging and product life-cycle support problems as "bit-bumming" and thus should only be a last-ditch attempt to save an effort about to fail to meet required speed specifications. Intelligent system design dictates that a projected 50% of capacity throughput surplus be included to both facilitate unexpected system growth and anticipate throughput-requirement and load-fluctuation estimation errors. This philosophy should preclude the need for such unstructured code optimization. Compromises in these design guidelines may be necessary in applications with large replication volumes and correspondingly high cost sensitivities.

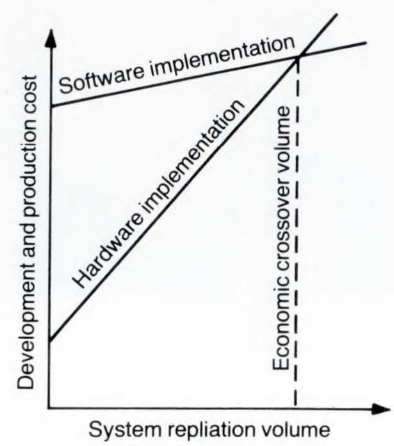


**Fig 4 Hardware/Software interface for microcomputers often has the possibility of tradeoff. In this example, a serial input-output port a terminal device can be done in software (high initial cost) or a USART chip (increasing cost with volume).**

## System Implementation differences affect software

Microcomputer programmers have to be more careful with addressing memory, which is allocated in disjointed segments. To gain reliability and cost efficiency, a microcomputer's (final-product) program is held in primary memory and is not kept in mass-storage peripherals. Primary memory is normally segmented into a nonvolatile read-only memory (ROM) program-storage area and volatile (read/write) random-access memory (RAM) scratchpad area. This partitioning of memory space imposes another constraint on the programmer – the program must be partitioned into disjointed ROM and RAM sections. Programming must not attempt to write into ROM space nor execute code in RAM space inadvertently. Additionally, the stack area must be maintained in RAM. Observing the boundaries of these memory areas is the programmer's responsibility. This is in contrast to minicomputer systems, where typically the program is loaded from some mass-storage peripheral device into memory composed uniformly of nonvolatile core memory, in which no such partitions exist.

The hardware-software interface is much closer for the microcomputer. Because microcomputer hardware systems are custom-made for specific applications – in contrast to the general nature of minicomputer system hardware – the two systems have major differences in the integration of hardware and software. In microcomputer systems, the hardware/software interface is closely coupled, i.e., one is often directly traded off for the other. In contrast, the fundamental hardware is much more standardized with the minicomputer, so software is written to run on that hardware without substantial change. In the micro's case, for example, a serial input-output port to a terminal device customarily may either be implemented in software or done in hardware external to the CPU by a Universal Synchronous-Asynchronous Receiver Transmitter (USART) chip. In a mini system, such an interface is almost always performed by a standardized serial interface board. The engineer who implements a microcomputer system must understand such hardware/software tradeoffs **(Fig 4)**. Thus, a microcomputer programmer must be more familiar with hardware than his minicomputer counterpart.

Software development is harder in micro systems because of the lack of peripherals so useful in debugging and simulation.

Custom microcomputer systems are very well suited for efficiently performing well-defined relatively-fixed tasks. Unlike minicomputers, they are not well suited for general-purpose computation or software

They generally lack three important system development tools: 1) the large secondary storage (disks, tape drives, etc.) required to hold utility programs; 2) language translators (assemblers and compilers); and 3) high-speed hard-copy devices (line printers, etc.),

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Table 2 Software development tools are considerably more primitive for the micro. Of the applicable tools listed here that are used extensively with minis, many are nonexistent or less powerful with micros.

| | |
|---|---|
| **Text Editor** | For composing and modifying program source. |
| **Assembler** | Translates assembly-language programs into machine code. |
| **Macro assembler** | An assembler that permits the representation of commonly appearing sequences of instruction with shorthand "macro" names. |
| **Cross-assembler** | An assembler that executes on one (host) computer, but generates machine code for another (target) computer. |
| **Compiler** | Translates a high-level-language program into a language suitable for a particular computer. |
| **Cross-Compiler** | A compiler that executes on one (host) computer, but generates code for another (target) computer. |
| **Loader** | For loading an executable module from some peripheral device into memory. |
| **Linking-loader** | A loader that combines many relocatable object modules into an executable module. It makes appropriate modification to each module for resolving change in references between the modules. |
| **Cross-reference listing** | An assembler output that lists all references made to each label or other symbol in the program. |
| **Debugger** | Permits the testing and verification of a program's operation by observing intermediate results at various stages of execution. |
| **Debugger-simulation** | A debugger that uses simulation to run on one machine and facilitate the debugging of a program written to run on another machine. |

which are desirable during program development, but are rarely required in a microprocessor's final configuration. These facilities are required in any significant software development effort. Thus, microcomputer software is often developed, simulated, and initially debugged on alternate computer systems – timeshared systems, minicomputer systems, and specially-configured (typically more expensive) microcomputer-based development systems.

In these development systems not based on the micro, the language-translation programs used to convert programs into micro machine code are called "cross-assemblers" and "cross-compilers." These programs run on one machine, the larger "host" development computer, and produce code for the microcomputer or "target" machine. Additionally, these "host" machines often also have "simulator-debuggers," programs that simulate the running of the "target" processor and help debug the machine code by using the significant resources of the "host" system. In contrast, most mini software is developed on the mini itself. The software tools **(Table 2)** available to help develop software for micros are considerably more primitive than those available for minicomputer software development. The text-editing systems available for micros are considerably less powerful. Many micros lack the availability of macro-assemblers and linking loader facilities. Also, few high-level-language processors generate code for micros. In fact, many micros have no compiled high-level languages at all (but this is rapidly changing). Many manufacturers only provide cross-compilers which must be run on "host" development computer systems and have no resident versions that run on the micro itself. Resident software is, however, becoming more common as language processors and text editors can be stored on a single chip. The most popular high-level language in the micro world at present is BASIC, an interpretive language. This is a reflection of the efficient use of memory characteristic of interpretive language implementations. Interpreters are, however, often not acceptable in real-time applications because they execute programs slowly, so assembly language still dominates the programming of micros.

## Conclusions

A large number of contributing factors makes programming microcomputers different from programming minicomputers. The relatively limited hardware facilities of the micro requires software to perform functions normally available in hardware on the mini. The lack of efficient high-level languages for the micro makes assembly-language programming dominate micro applications, whereas high-level languages dominate mini applications. The limited instruction set of the micro relative to the mini makes assembly-language programming more tedious and complex on the micro. The typical area of application of micros gives these systems higher cost sensitivity than typical mini applications. This leads to extensive custom hardware in micros and also to an increased degree of interaction between hardware and software design not found in typical mini systems. The software tools available for developing software for the micro are appreciably different and less powerful, requiring the programmer to develop different implementation methodologies. Thus, aside from the obvious similarities of the primary function of the software, devloping software for the micro and the mini can be appreciably different activities.

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## ABOUT THE AUTHOR


Ken Schroeder has eight years of software experience in both minicomputer and microcomputer systems. Now working on microcomputer-based consumer products, he has also worked with software for medical instrumentation, laboratory automation, and navigation satellites.


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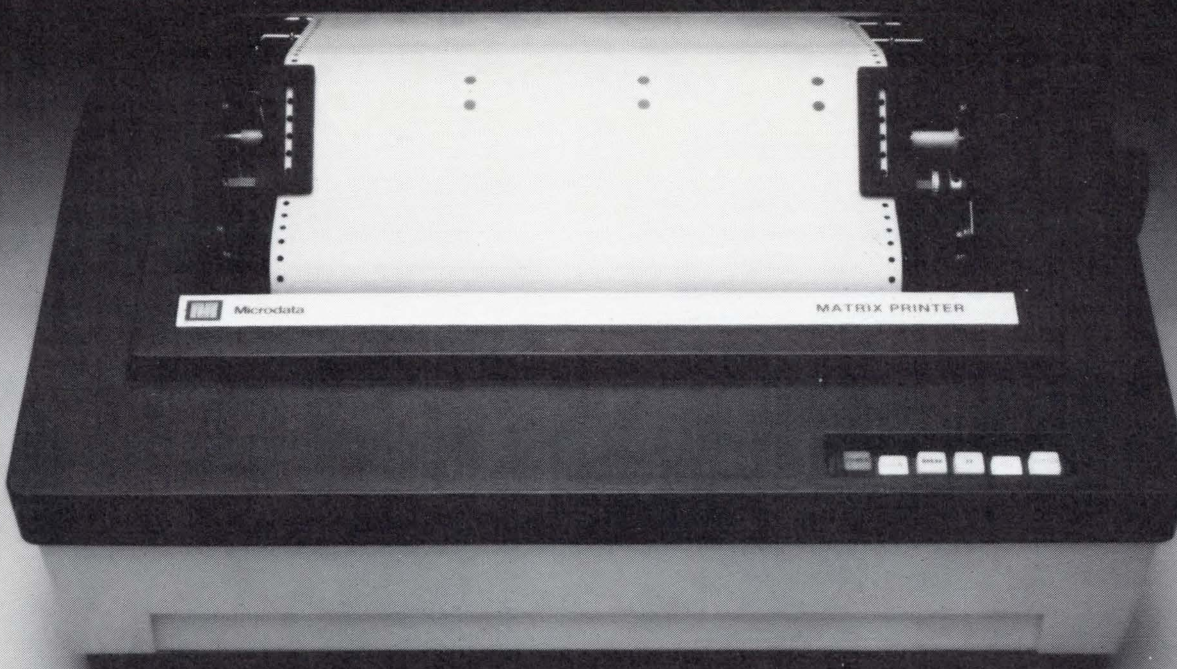


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# μP SELECTION
## Some Do's and Don'ts

**Paul Snigier,** *Editor*

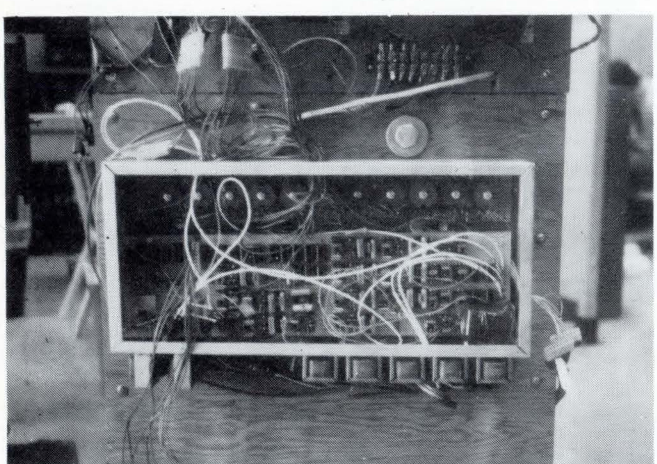
EEs who select a microprocessor that isn't commonly-used (less than 10% of the market) better think twice; it's quite possible that this lack of use will soon result in less support — in terms of aids, support chips, boards, documentation and in terms of sales effort and marketing strategy. Marketing departments will support the superior profit-making micros, to the detriment of other micros (even if superior). To select these micros is to bet against the marketplace: you have everything to lose and nothing to gain. Why risk it?

Despite the rapid entry of the bewildering array of chips, choosing the future winners is not as difficult as you might think. To this end, we will first look at a number of well-known contestants in the μP/μC arena and provide you with guidelines to follow before you select a micro that is best suited for your applications.

### 8-bit versus 16-bit: which is better?

Commonly used micros fall into two general categories by word length — 8- and 16-bit. The 8-bit class includes the 8080A, 8085, F8, SC/MP, 6800, 6502, 8048 and 3870. In the 16-bit class are the PACE, TMS9900, TMS9985, TMS9940, 6809 and 8086. In this article we'll use these devices as examples of available device classes.

Should you select an 8- or 16-bit microprocessor? Generally speaking, the application in which a μP is used determines whether an 8- or 16-bit micro is called for. Examples of 8-bit applications are a triac surge cycle tester, a typewriter, intelligent CRT terminal, keyboard/printer, process control functions (such as traffic signals and electronic scales), POS terminals with barcode scanners. In these applications, the micro performs basically logic operations (testing the position of a switch or key and setting output switches such as relays and contactors which control devices such as valves, motors and lights). Since little data processing is required, most 8-bit processors can accomplish the results within the time constraints. This is especially true of process control applications where physical devices are extremely slow compared to the computational speed of modern microprocessors.



This portion of a fully programmable triac surge tester and monitoring system, designed by the author four years ago, contains 47 SSI/MSI ICs, but today could be designed more easily with a single-chip μCs lend themselves to low volume designs with a minimum of hardware/software design effort.

Applications which require computation and general data processing, on the other hand, usually require a 16-bit processor because they require movement of relatively large amounts of data from the memory, through the processor's ALU and back to memory again. Arrays of data are often compared, scanned, modified or combined via lengthy algo rithms. Character strings might be processed to locate a specific character or string of characters, then groups of characters read and analyzed, etc. This type of application is usually given to a 16-bit micro.

But microprocessors sometimes include enough on-chip memory to perform simple applications. These devices are called microcomputers because they contain the memory and I/O circuits as well as the ALU and control. Examples are the 8048, 3870 and TMS9940. So three categories of devices should be reviewed for any application: the microcomputers, the 8-bit microprocessors and the 16-bit microprocessors.

Data processing applications, however, involve moving large amounts of data into the processor's arithmetic and logic unit and performing mathematical or logical operations on that data. An array of data might be entered for summation or for comparison with still another array of data, and a number of character strings might be entered into the μP and each searched for a specific character, etc. Since these data processing type applications involve processing large amounts of data, they are better suited for 16-bit micros.

### Single-chip μCs promise a revolution

The single-chip microcomputer promises to become the most popular micro of the 1980s. Even more than the mid-range class, the single-chip micro is well suited to process control applications, a fact illustrated in its architecture. One-chip μCs include all program and data storage on-chip, freeing pins for I/O control. Except for the 8048, they're hard to program. They contain either on-chip ROM or eraserable

EPROM. (Because of on-board memory, the single-chip device is a $\mu$C, not a $\mu$P.) Its on-chip programmed memory reduces components required to implement a control application which can be programmed in under 2K-4K bytes of memory, an important feature for volume producers of $\mu$C-based products. EPROM is well suited for initial prototypes of applications which require only one version. Despite the limited amount of on-chip ROM, single-chip $\mu$Cs accept external ROM-RAM memory and address up to 64K bytes of program memory.

Besides the 1024 bytes of program memory on board the 8048 (other versions have 2084 bytes of ROM), there are 64 bytes of RAM, with a 128-byte version also available. Sixteen bytes of the RAM comprise two banks of 8-bit working registers. These facilities interrupt processing and afford the micro much data handling ability. Another 16 bytes of RAM form an 8-level, 16-bit-wide stack for storing the state of $\mu$P register during interrupt processing or calls to subroutines; the remaining 32 bytes of RAM are available for temporary storage of data being processed. The relatively small amount of program and RAM memory (1024/2048 and 64/128, respectively) indicates the small program size and small data quantity handled in a single-chip micro.

Beyond the built-in memory, there are 96 instructions to handle control type functions. At least 50% of instructions are one-byte long, with the rest two bytes long. In addition, within the set, a number of instructions can manipulate individual bits of a byte, which is particularly useful if your control-type $\mu$C must examine the ON/OFF state of a switch or indicator and make a decision based on its state. Complimenting this capability, a variety of conditional branch instructions make decisions based on the condition of individual bits within a word, thus permitting you to more easily implement a logic flow for a process control function.

Like the 8048, Mostek's 3870 (second-sourced by Fairchild and Motorola) is a single-chip micro with a similar process control type architecture, and also has 64 bytes (or 128 bytes) of RAM and 2K (or 4K) of ROM program memory, although it has no EPROM versions — a disadvantage for custom designs. The 3870 instructions have strong points: many accumulator operations decrease RAM access times, speeds instruction execution and also performs memory/accumulator arithmetic and logic operations . However, designers criticize its instruction set as generally more difficult to use than that of the 8048.

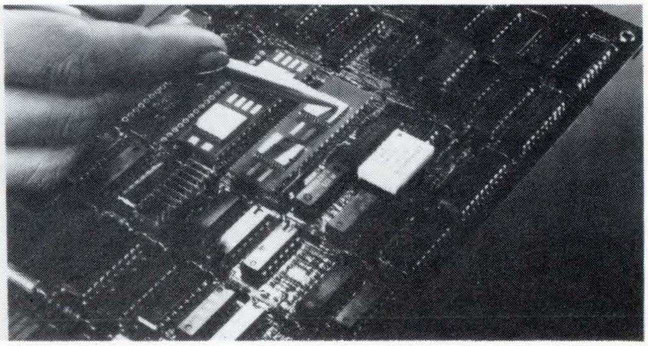
In the earlier microcomputers, the features of the CPU were somewhat reduced to make space for additional memory and I/O. This is not the case with Motorola's MC6801, an expandable one-chip version of the 6800, which in addition to 2K of ROM, 128 bytes of RAM, a 3-function 16-bit timer, a full duplex, double buffered serial I/O port and 33 I/O lines, provides an enhanced instruction set. The instruction set is the complete MC6800 instruction with 10 additional instructions, including an 8-by-8 multiply and eight 16-bit instructions such as Add, Subtract, Load, Store, Shift and so on. The 6801 can also be expanded to 64 K bytes of address space. The 6801 expands the range of applications available to $\mu$Cs to also include the applications covered by the mid-range class of micros. The 6805, a non-expandable version of the 6800, is stripped down for small chip size and minimum cost. The simpler CMOS 6805, like the 6801, are aimed at high volume, high-reliability applications. Both TI and Motorola have high-volume contracts with the auto makers.

A delayed late entry into the crowded single-chip, high-speed controller market, Z8 possesses an architecture similar to the Z8000. It has on-chip 2K bytes of mask programmable ROM. Powered by a single 5V supply 8MHz clock, Z8 executes instructions in 1.5-2.25 $\mu$sec; and is claimed to have twice 8048's throughput. It possesses 124 general purpose 8-bit registers, and all are usuable as accumulators, index registers or pointers. Not only that, but with 6 vectored interrupts that can be masked in order of priority, Z8 provides more interrupt capability than other $\mu$Ps

Also, various control registers and four I/O registers are mapped into the register file, providing flexibility and easier interface control.

Z8's communications capability should suit it to distributed systems. For example, in a phone it would act as a distant member or intelligent terminal for a large computer network system — a factor which could position the Z8 in an explosive market in light of personal computers in the home and electronic office of the early 1980s.

Present offerings include: 8048, PIC 1650, PPS-4/1, Z8, 8022, 6801/05, 9940, 8070(8060), 3870, 1804, 6500/1, and on the lower end, one-chip $\mu$Cs like the popular TMS-1000, S2000, COP420 and 1872.

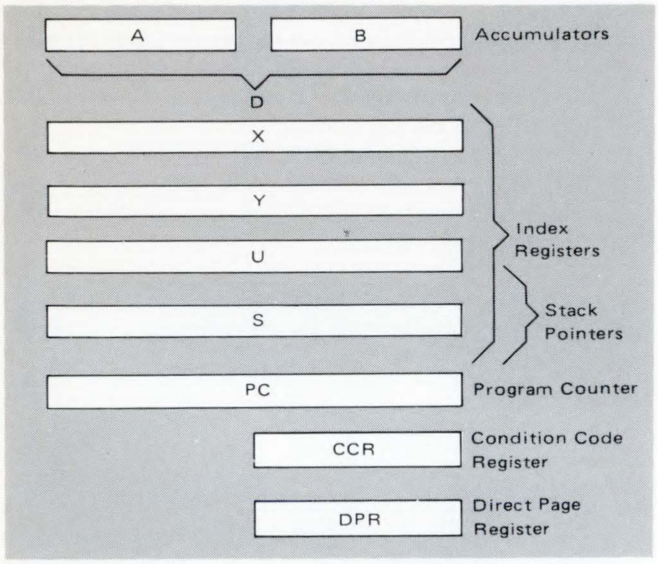


**Said to be the most powerful micro available, DEC's processor board LSI-11/23 $\mu$C incorporates a 16-bit wordlength $\mu$P with the functionality of a midrange PDP-11 mC. The new processor has 2.5 times the speed of the entry-level LSI-11/2 $\mu$C and incorporates a memory management chip to permit four times greater memory capacity. An optional floating-point processor chip permits five times faster operations than software floating point. The LSI-11/23 is software compatible with other LSI-11 models and with PDP-11 software.**

Several drawbacks hold back single-chip $\mu$Cs. Since the basic architectures were originally intended for mask-program storage, these single-chips $\mu$Cs require complex off-chip augmentation for program storage. The 8748, Intel's EPROM version of its 8046, makes it easier on low-volume designers, who will be more concerned with ease of design and development. Also, more single-chip micros will find themselves in cost-sensitive products, such as hand-held drills, blenders and other applications that are economically absurd today. Examples include vibration signature analysis in a hand-held drill (and anywhere simple sensors can be used with the micro applying statistical techniques), speed-torque control of drills and small power saws, and other unanticipated applications.

What applications are suited to single-chip $\mu$Cs? Video games (such as Fairchild's F-8-based cartridge game), microwave ovens and sewing machines — these and other such high-volume applications will profit best. Most single-chip micros come with ROM; it must be programmed during production, which makes if difficult if you're a low volume designer, although you can program EPROM devices, which isn't all that great an advantage here. No doubt, future use of single-chip $\mu$Cs will involve elementary applications bec use of falling costs.

One additional single chip device is the powerful TMS9940 which contains 2k bytes of ROM or EPROM and 128 bytes of RAM. The 9940 architecture is quite sophisticated. The 9940 provides the user with the opportunity to use the 16-bit architecture of the TMS9900 in a format. The instruction set is the same as the TMS9900 with a few additions to facilitate BCD arithmetic. Moreover, the multiprocessor I/O feature makes the TMS9940 a natural choice for systems in which several processors control separate units yet communication between processors is needed for overall control.




**The MC6809 has 16-bit processing capability with 50% more throughput than its parent, the MC6800. It operates at 2 MHz, adds 16 new addressing modes, utilizes an expanded instruction set with high-level language capability, and adds a host of other refinements while maintaining compatibility with the M6800 Component family.**

## Mid-range μPs offer more flexible architecture

The mid-range μP differs from single-chip μCs in two ways — by lack of on-board program memory or RAM and more general-purpose architecture. These mid-range devices address up to 64K of either ROM or RAM, and the instruction set contains more general-purpose instructions to handle both control-type functions and data processing-type functions.

Examples of mid-range μPs include the 8080A, 8085, 6802, 6800 and others. All have an 8-bit data bus, 16-bit address bus and accumulator-oriented instruction set. Beyond these features, they differ greatly. If we look at the 8080 and 6800, we see the difference is quite pronounced in several areas.

First, the 8080 has six 8-bit or three 16-bit general purpose registers, while the 6800 has two 8-bit general purpose registers used as accumulators and a 16-bit index register. Second, the 8080 has six addressing modes and the 6800 has seven. Third, the 8080 can use specific I/O instructions; the 6800, memory mapped I/O with the I/O device treated like a memory location.

The consequence of the first two of these differences is this: the 6800 uses memory to a greater extent than the 8080 during instruction execution, which could make it difficult for the 6800 to support reentrant code (essential for interrrupt processing). The ability to support reentrant code means that, for example, during execution of a multiply subroutine, an interrupt occurs which halts execution of the present program and commences execution of appropriate interrupt routine. For illustration purpose, suppose that the interrupt routine also called for execution of the multiply subroutine which had just been interrupted. A micro which supports reentrant code would permit the multiply subroutine to be reentered and reexecuted for the interrupt program without disrupting, in any way, the operation previously being performed. Thus, after the multiply subroutine has been reentered and reexecuted and the interrupt program completes, operation of the multiply subroutine can resume in exactly the same place as if it was never interrupted. More importantly, the result produced by the subroutine is the same as though the interruption never occurred.

Reentrancy in the 6800 is somewhat more difficult because during program execution the device might be using memory to hold temporary values, e.g., addresses to be modified or data to be processed. If a program is interrupted and later reentered, these temporary values could easily be overlayed. In the 8080, this problem is avoided, if all the temporary values will fit in the registers. Both processors can push onto a memory stack all registers, upon the occurance of an interrupt, and retrieve them after interrupt processing concludes to permit unaltered completion of the interrupted task. The 6800 does this faster; it has less registers to push and pull from its stack.

The second of the differences deals with how the two devices process interrupts. The 8080 has a vectored structure which permits the interrupting device to identify itself and thereby call its interrupt handling routine into execution. Thus, for each interrupting device there resides in memory a handler routine called into execution by its associated device.

In the 6800 there is typically one interrupt routine called into execution when any of several possible interrupts occur. The interrupt routine must then identify the device wanting service by polling the devices or using the 6828 Priority Interrupt Controller. Thereafter, with other interrupts disabled, the appropriate software is called to service the device.

The third difference — that the 6800 has seven addressing modes to the six of the 8080 — provides an extra mode that adds to the flexibility of the 6800 in addressing memory. Where this directly impacts the user is in the amount of assembly language code produced for a given application, which is usually less for the 6800. Both micros have the following addressing modes: implied, immediate, register and direct. Implied addressing means that the instruction op code also specifies the address to be used; thus, instruction and address occupy only one memory byte. An immediate address, on the other hand, requires either two or three bytes since the operand is located in the first (1-byte immediate address) or the first and second memory (2-byte immediate address) locations immediately following the operation code.

As the name implies, register addressing specifies a register, and requires only one byte of memory. Direct addressing uses three bytes of memory and contains in the two bytes following the operation code of the instruction the address of the operand.

Beyond these four modes, the 6800 has three modes: a modified form of direct addressing, indexed addressing and relative addressing. In the modified direct address, only one byte is used to contain the address of the operand, thus permitting 256 bytes to be addressed while only taking up two bytes of memory to contain operation code and address. Flexibility in programming comes with the indexed addressing and relative addressing modes. Indexed addressing

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means that the address in the second byte of the instruction is added to the low order bits of the index register with any carry propagating into the index register high order bits. The result then becomes the address to be accessed during instruction execution. This facility is very useful in handling elements in arrays and tables. In relative addressing, an offset, contained in the second byte of the instruction, is added to the program counter's low order bits. While this method is used for program jumps, it finds its greatest appeal in facilitating relocatable program code, code that can be loaded into any memory locations and relocated without altering or changing the code. Besides the four addressing modes it has in common with the 6800, the 8080 has register indirect; and I/O addressing. In register indirect addressing, the one-byte instruction specifies a 16-bit register which contains the address in memory to be accessed.

The final 8080 addressing mode, I/O addressing, also points up the fourth difference between the 8080 and 6800: their respective methods of handling I/O. With the 8080, there are separate instructions (IN and OUT) which address I/O device and either sends it, or receives from it a byte of data. In the 6800, an I/O device is treated as a memory location, a technique referred to as memory mapped I/O. The 6800 method is more like the large mainframe computers, such as DEC PDP series machines, than the 8080.

Another member of the 8080 class, Zilog's Z80 is used a lot in mid-range data processing applications. Boasting additional registers, fifty extra instructions (advanced block-move and block-search "macros", etc) over 8080A's 78 basic instructions, and higher speed for the programmer, Z80 is also attractive to designers because of extras like on-board refresh logic for dynamic memory subsystems. Although not pin-for-pin 8080/85 compatable, it can use 8080 software and peripherals, although to do this doesn't take advantage of the Z80's power (but is done for Z80-to-8080 software transportability).

As I said earlier, the 6800 suffers versus the 8080A electronically, but its instruction set makes up for this. Motorola's 6802 alleviates some designer's objections by two changes: (1) placing the complex clock circuitry on-chip and (2) to permit 6802 to use slow memories (without slowing up the clock for everything else), Motorola wisely added wait logic.

While the 8-bit processors are generally adequate for logical decisions and simple I/O functions, there is one additional alternative to consider. An 8-bit version of a 16-bit processor is available: the TMS 9985 is essentially a TMS 9900 in a 40-pin package with a few minor modifications to the architecture. Like the TMS 9940, it includes the same instruction set as the TMS 9900 plus the additional ones for BCD arithmetic. The user has all the advantages of 16-bit architecture with the added advantage of the 40-pin package and the 8-bit data format. The primary advantage of the TMS 9985 over the 8080 and the 6800 is the minicomputer architecture and instruction set which provide substantially superior computing power, better efficiency of memory usage and faster execution. The TMS 9985 is software compatible with the TMS 9900 because it is built with the same 16-bit architecture.

In the next half of this two-part series, I will discuss the (dis)advantages of 16-bit micros and provide guidelines for selecting a micro. DD

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# SOFTWARE
## DESIGN SERIES

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# Programmable Interface Chips

One problem in the development of software for microprocessor-based systems involves the increasing use of programmable interface chips. These devices greatly expand the flexibility and usefulness of the designed boards, reduce parts count, and simplify changes and modifications. However, their lack of standardization leads to programming and documentation problems. Furthermore, since their widespread use in microcomputers does not parallel application in larger machines, very little software or hardware support is available. This discussion presents the history, justification, typical characteristics and uses of these devices, and then describes some of the problems that designers must resolve.

When microprocessors were first introduced, few associated circuits other than memories were available. Since users had to implement input/ouput sections in standard logic, the cost and complexity of those sections quickly exceeded the cost of CPU and memory, except in very simple applications. The introduction of 8-bit (or byte-wide) parts, including latches, buffers, drivers and registers, simplified I/O sections somewhat, but still left them far more complex than the other parts of the microcomputer. Furthermore, I/O sections implemented in standard logic contained all the disadvantages of logic design, including a lack of flexibility, difficulty of implementing changes and high parts count. The higher speed of logic was typically wasted, since the I/O section could not very well outstrip the central microprocessor.

When Motorola introduced the 6800 microprocessor in 1975, it also introduced two compatible MOS I/O parts — a parallel interface (called the peripheral interface adapter or PIA) and a serial interface (called the asynchronous serial interface adapter or ACIA). These two parts offered the advantage of programmability — that is, they had sets of logic connections which the designer could select by storing a particular value in a control or command register. Note that this kind of programmability differs from the programmability achieved by tying pins on I/O ports, timers and other devices. That kind of programmability increases the usefulness of a particular part, but does not increase the flexibility of a printed circuit board, since its wiring is fixed.

What then does this new kind of programmability mean? Let us examine the Motorola 6820 parallel interface **(Fig 1).** The part consists of two 8-bit ports, each of which includes two associated control lines and a control register. Typical control register bits possess the following functions:

- Bit 0 determines whether transitions on one of the control lines enable an interrupt to output.
- Bit 1 determines whether the active transition on one control line is low-to-high (leading edge) or high-to-low (trailing edge).
- Bit 5 determines whether the other control line is an input or an output.

The other control register bits have similar functions which we will not describe here.

Note the following advantages of this kind of programmability:

- A circuit board with a PIA can be used in many applications without any hardware changes. Having the program store different values in the control register during startup implements the minor differences.
- Such changes as incorrectly specified transitions can be made in software rather than in hardware.
- The same part can be used in many different applications, thus increasing volume and simplifying testing and other procedures.

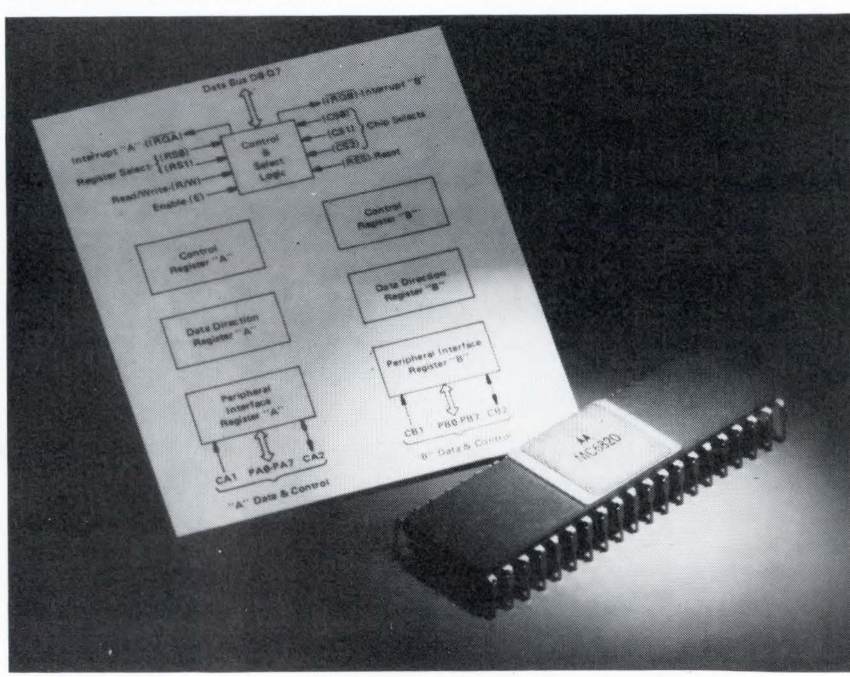
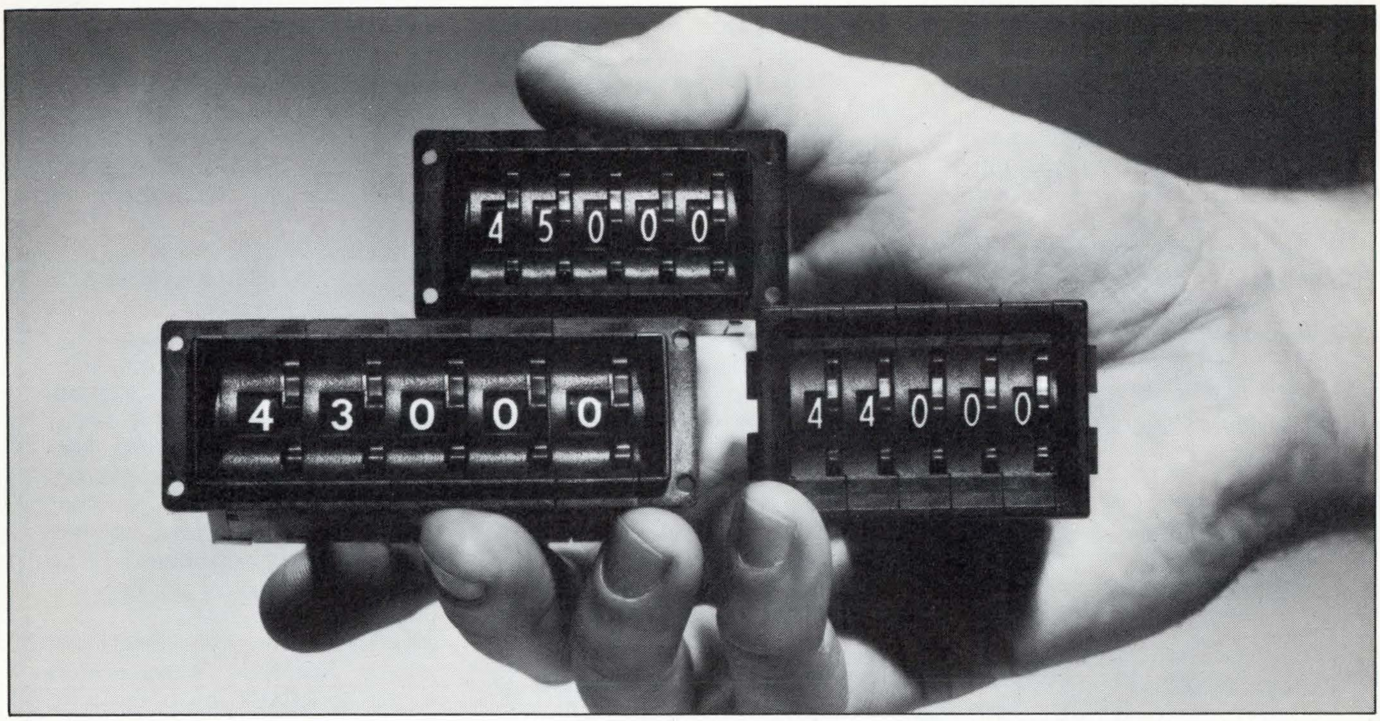


**Fig 1 Motorola 6820 peripheral interface adaptor (PIA) provides parallel interfacing with two 8-bit ports.**

# A BUCK A SWITCH!*

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## SOFTWARE
DESIGN SERIES

Note that the advantage of programming makes it possible for manufacturers to supply flexible microcomputer boards capable of reducing the need for expensive hardware design in low-volume applications.

How does the user take advantage of this programmability?

• First, he must determine the control register values required for a particular application. Unfortunately, since no standards for assigning bit positions or functions in programmable devices exist, the user is faced with understanding a set of arbitrary features.

• Then, he must write a startup routine that configures the programmable device correctly. This operation is comparable to picking a numbered circuit from a designer's casebook. Note that most applications do not require reprogramming of devices. The devices are programmable across applications, but not usually within a single application.

Note that in the PIA example a control line might be used as an input in some applications and as an output in others, but seldom as both in a single application.

At the present time, microcomputer boards usually contain many programmable devices. A PIA Motorola board, for example, includes a programmable parallel and serial interfaces and a programmable timer. The Intel iSBC 86/12 board also incorporates a programmable interupt controller. Other programmable forms of available chips include DMA controllers, arithmetic devices, keyboard/display interfaces, CRT controllers, data link controllers, printer controllers and floppy disk controllers. Board-level configurations like the Motorola MEX 6821-2 input/output module of Fig 2 include the programmable devices and interfacing circuitry in a form suitable for system use.

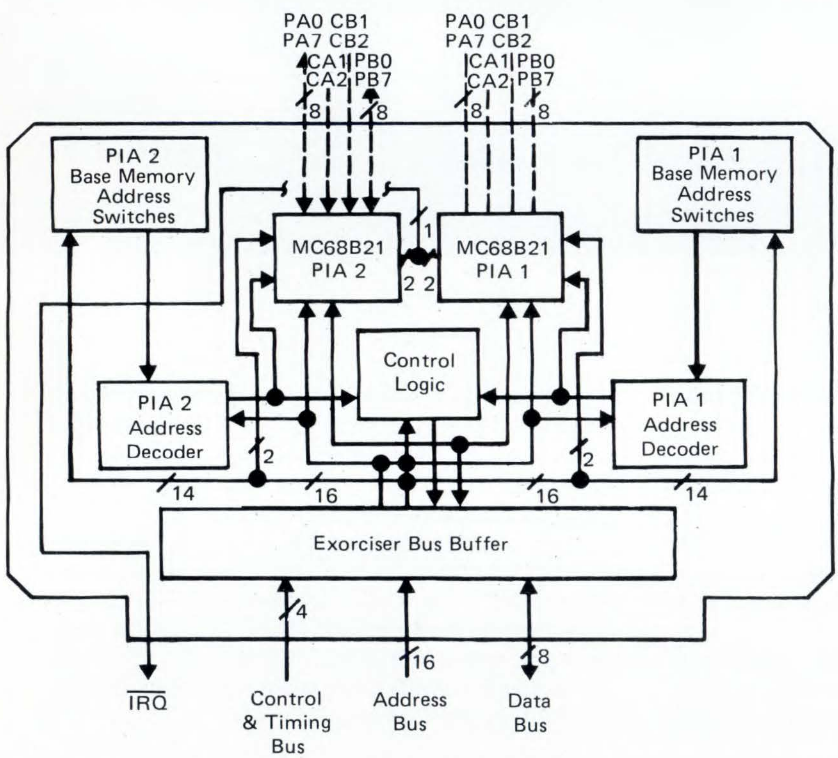


**Fig 2 Motorola MEX6821-2 I/O module provides four 8-bit I/O ports for peripheral interfacing, 8 individually controlled interrupt lines, four of which may act as peripheral control lines. The part also offers a program-controlled capability with each of the two PIAs addressable as a memory, a switch-selectable base memory for each PIA, a jumper-selectable user address and up to 2.0 MHz operation.**

Note some of the problems involved in the use of programmable devices:

• Each programmable device is unique. The Intel 8255, the parallel interface equivalent to the PIA for 8080/8085-based systems, contains entirely different control registers and options than the Motorola PIA.

• The programming of the device is arbitrary. Program instructions merely load a bit pattern into a control register. Obviously, the system documentation must describe the programmable device and the codes used, since those who must maintain the system can hardly be expected to understand a particular device.

• No support for these devices in any high-level language exists. Most are programmed with simple, but essentially meaningless, assembly language sequences. Also, there are no models for use with simulation packages or the equivalent of in-circuit emulators.

• The device options may be very difficult to understand and poorly documented. More recent devices, such as programmable timers, interrupt controllers, data/link controllers, CRT controllers and floppy disk controllers, often offer hundreds or thousands of possible configurations. For example, the Zilog S10, an advanced serial interface with data/link capabilities, incorporates eight control registers that the user must program.

• Initial states and transitional states may be undefined. Many devices supply no RESET inputs and come up in an undefined state. Extra circuitry is often required to take care of this problem. Similarly the specifications seldom consider even a substantial percentage of the possible situations. The user may well need to determine reasonable tests for the devices.

The programmable devices represent a distribution of computing power. The Intel UPI-41 (or universal peripheral interface) is, in fact, an entire ROM- or EPROM-based microcomputer that serves as a custom programmble interface for more complex peripherals **(Ref 5,6)**. Preprogrammed versions of the device are available as data encryption units, printer controllers and other functions. As always, distributed computing power is a useful catchword that is far from fully explored at the design, development, test and maintenance levels. Programmable peripheral devices represent only a taste of the problems that are to come in the development of software and computer-based electronic systems.

# CAPACITANCE KEYBOARDS:

## A Look Beyond Microprocessors


**Walter Z. Davis**
*Key Tronic*

In selecting a keyboard, the first design decision is "which type of switch offers the lowest potential keyboard cost structure?" The choice is purely economic. The consideration is trading a relatively fixed electronic cost against the variable cost of some 70 to 80 switches. The least costly switches are the non-contacting capacitive or core designs, followed by contact types, and finally by active device (i.e., hall effect) types. However, the circuitry surrounding the switch matrix is inversely complex. Contact and active switches use only the simplest decoder/drivers while the non-contact passive switches require rather sophisticated drive/sense designs.

The decision process is straight forward. Pick the least costly switch element (comensarate with reliability requirements) at the expense of sophisticated surrounding circuitry. Material costs are inflationary by nature, while electronic costs are going down more than enough to offset and decrease the cost of surrounding circuitry. With "drive and sense" chip-sets such as the one featured later in this article, indications are that the cost structure of capacitive keyboards (in particular the non-soldered variety) are significantly lower than active device designs and approaching the cost of contact designs. Also, capacitive switch life is equal to the life of any solid-state designs and 5 to 10 times longer than the contact varieties. It's no wonder that capacitive keyboards are becoming dominant in today's terminal designs.

Attempts at making capacitive technology work had been going on for at least a decade when Key Tronic Corporation, in early 1974, married the foam capacitive pad to a current sensing detection scheme. The foam pad cured earlier problems with PCB/switch irregularities, but the real breakthrough came with the development of a detection scheme, insensitive to the stray capacitance characteristic of a dense trace and pad layout.

With grounding traces isolating individual sense lines, shunt capacitance often exceeds switch capacitance. The goal was a detector which caused little or no voltage change on the line being sensed (this, rendering the design insensitive to a "capative-voltage divider"). Of the six vendors currently offering capacitive keyboards, at least half of them possess monolithic detectors.

Once you've come to the conclusion that the non-soldered capacitive switch concept offers the lowest possible keyboard cost structure, the only significant question is: "Does the switch work?". We were always convinced that the switch was potentially as good as our life tests indicated, but the real proof came from the field. Results from over 500,000 keyboards and 5 years, demonstrated the reliability neces-

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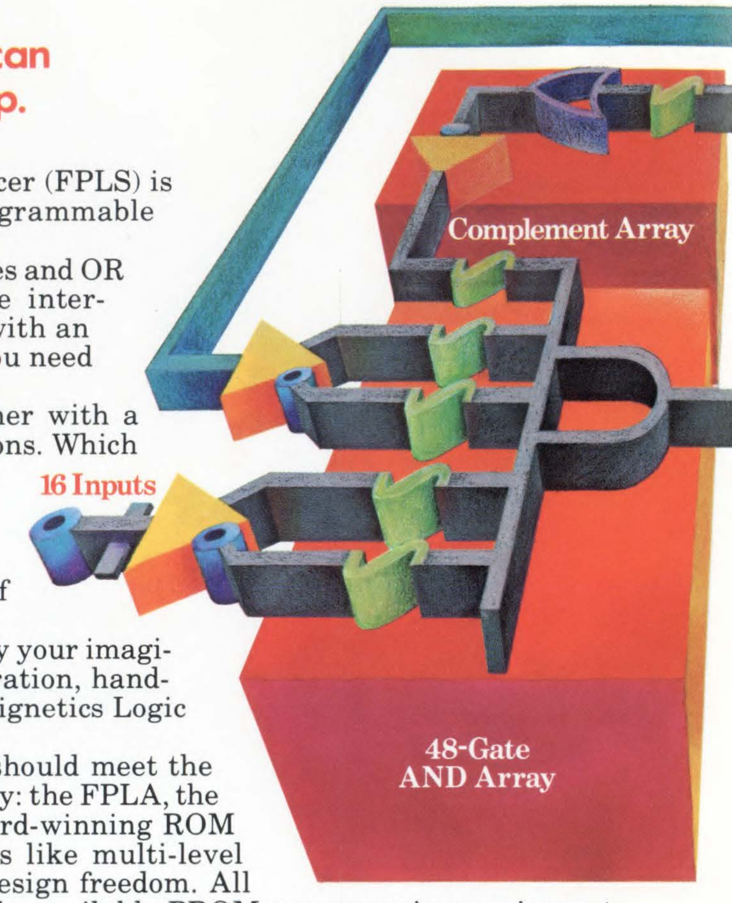
# Design Flexibility in

## Introducing the LSI Logic Sequencer. Now your complete state diagram can become hardware with a single chip.




Our new Field Programmable Logic Sequencer (FPLS) is simply the most sophisticated device in programmable logic you can put your hands on.

And here's why: it has LSI arrays of AND gates and OR gates—all with nichrome-link programmable interconnects. This, plus an on-chip state register with an internal feedback loop, provides everything you need to implement any synchronous state machine.

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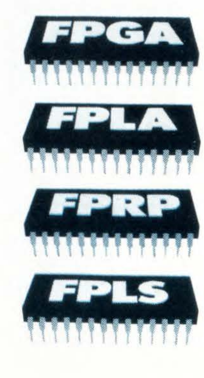
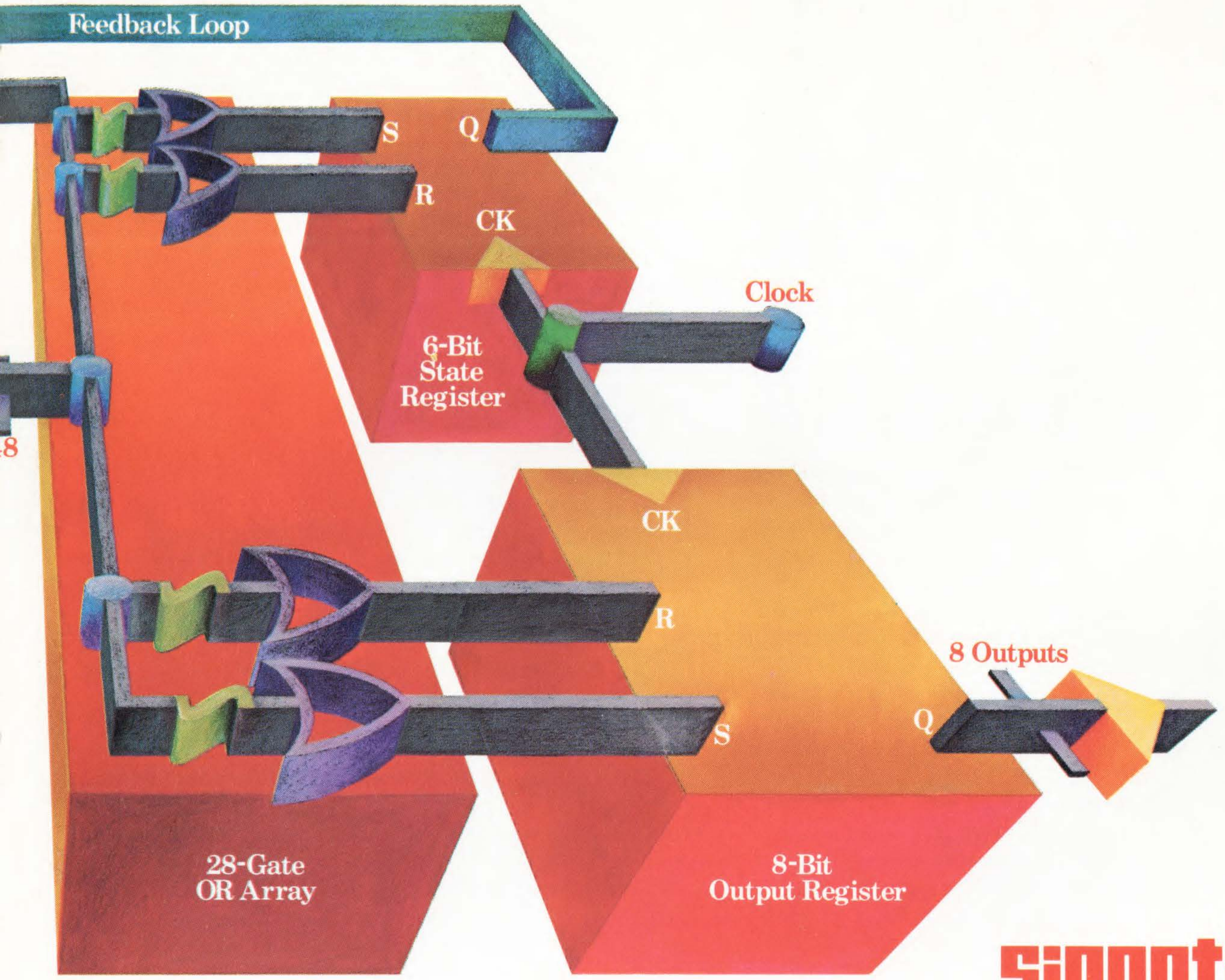
With greater design flexibility as close as the coupon, don't wait. Send it today. We'll rush you complete information on the new Logic Sequencer as well as the rest of the family. You may also contact your local Signetics sales office or franchised distributor.



# Programmable Logic.

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**811 East Arques Avenue**
**Sunnyvale, California 94086**
**Telephone 408/739-7700**


The 82S104/105 is available now in sample quantity directly from Signetics. For production quantity, contact your local distributor in third quarter, 1979.

**FIELD PROGRAMMABLE LOGIC FAMILY**

| Device | Inputs | Outputs | Speed (ns max) | Power (mW typ) | Mil-Spec Versions | Organization |
|---|---|---|---|---|---|---|
| Gate Array (82S102/103)* | 16 | 9 | 35 | 600 | Now | 9 AND/NAND gates; programmable output polarity. |
| Logic Array (82S100/101)* | 16 | 8 | 50 | 600 | Now | 48 AND terms; programmable OR array; programmable output polarity. |
| ROM Patch (82S106/107)* | 16 | 9 | 70 | 600 | mid-79 | 48 patch words; self-enable output flag. |
| Logic Sequencer (82S104/105)* | 16 | 8 | 90 | 600 | 4th Qtr. | 48 transition terms; 6-bit R/S FF state register; 8-bit R/S FF output register; complement array. |

*Two models available for each device: Open collector or three-state.

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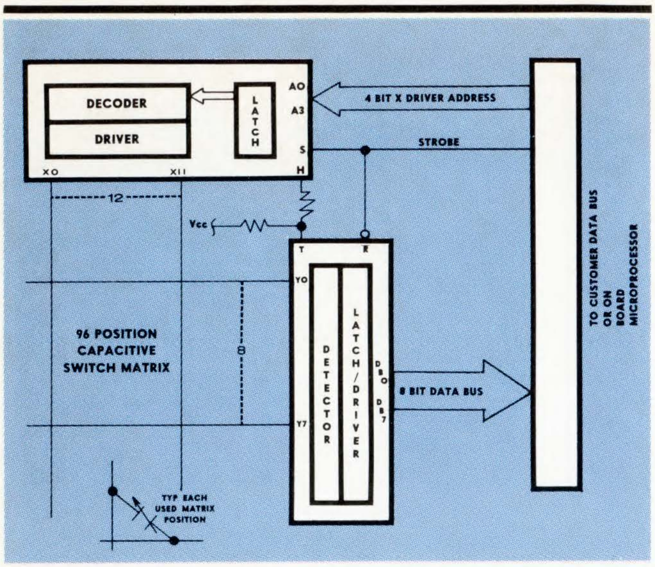



**Key Tronic Corporation's two-chip set capacitive switch interface.**

sary to achieve over 40,000 hour MTBFs.

Once past the analog problems of switch detection, validation and encoding are simply digital processes. It became evident to Key Tronic engineers over a year ago, that high volume pricing on the newly emerging single chip processors (8048 families) would fall below that of dedicated keyboard encoder chips in the near future. With this in mind, they set out to design a simple, economic interface between a capacitive-switch matrix and a microprocessor.

The original design (on paper) was a single 40 pin $I^2L$ part. The $I^2L$ technology allowed Key Tronic to mix the analog and digital portions of the design in a single chip. They soon found out that a lot of people were talking about $I^2L$ but not many were willing to quote full custom programs at the time. Those that did were a long way from meeting competitive price and delivery goals.

This led them to the two chip solution. By using two 20-pin parts and a semi-custom design approach they were able to meet price and performance goals and retain in-house control over the design and layout of both parts. For those of you that have been involved in full custom MOS programs you can understand why this approach was a welcome opportunity.

## Operation

In order to make efficient use of the microprocessor, it is necessary to be able to interrogate the entire matix very rapidly. This requires simultaneous examination of more than one key — ruling out the old method of decoders and multiplexers using a synchronous one-key-at-a-time interrogation system.

Since they were designing a bus-oriented processor interface chip, it made sense to use an 8 bit system. The final design of the detector chip (**Fig. 1)** allows examination of 8 keys at a time and provides latched data onto the output bus. With one pin dedicated to set the threshold current of the detectors and another for a latch reset/output enable, two for power and 16 for I/O, they were able to use a standard 20-pin package. This allows for easy automatic insertion and is significantly less expensive than 22- or 24-pin packages.

The decoder/drive chip is also packaged as a 20-pin part. With 4 address lines, one strobe, one latched output (for hysteresis control), and 2 for power they were left with 12 pins for matix drivers. This results in a 96 position matrix. The original design criteria called for an 8 x 14 matrix or up to 112 keys. To make tradeoff decisions regarding 96 vs 112 keys (or 20- vs 22-pin package) they examined the last one hundred custom keyboard designs that they had done and found that only 26% had greater than 96-key positions. About one half of those had over 112 positions and many were large complex control applications that tend to be higher cost, low volume designs.

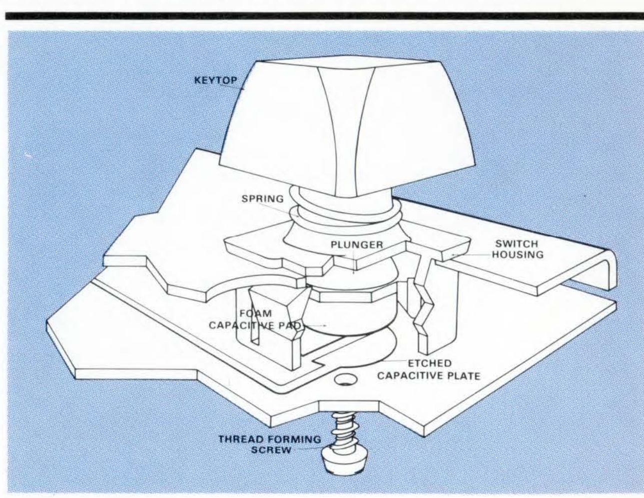
Based on this information and the fact that a second decoder driver chip could easily be added for applications greater than 96 keys they decided that 12 matrix drive lines and a 20-pin package was the best answer.

Since both chips utilize bipolar technologies they inherently offer good resistance to static damage. The matrix drive and sense lines of each device have been designed to exhibit low impedance to the supply in their normal mode of operation. Although ground line isolation is stil required between X and Y lines (to keep the key up capacitance as low as possible) this low impedance concept reduces the amount of grounding required and also provides good immunity to EMI. Care was taken with the design of both arts to eliminate the requirement for external termination or biasing networks on the matrix lines that have become a common part of most capacitive switch designs.

A typical interrogation would begin by bringing the strobe line low. This resets the data latches of the detector chip and places its output in a passively pulled up state. (The address lines can be brought in separately as shown in Figure 1 or can be tied to four of the data lines to provide a true 8 bit bi-directional bus). A four bit address is set up on A0-A3 to select a particular matrix drive line. The strobe line is brought high which latches the address into the decoder driver. The decoder then selects the appropriate line and drives it to a logic 1. After an internally created delay has expired the line driven to logic 0.

This 1 to 0 transition causes a current pulse on each Y sense line that has a key closed in common with the driven X line. The detector senses these current pulses and sets each corresponding latch output to a logic 0. The status of the 8 keys on the interrogated line can now be read from the data bus.

Using an Intel 8048 microprocessor, a complete 96-key interrogation can be accomplished in less than one half millisecond. This is particularly important if you're trying to input or output serial data with routines that cannot be interrupted for periodic matrix interrogation. It is even more important when using slower processors like the 8021.




**Simple capacitive switch design.**

**The photograph shows a custom capacitive keyboard — features include 4 levels of coding, serial output, and LED lighted shift lock key. Seventy-five to eighty percent of the cost of the assembly is custom in nature — printed circuit board, metal plate, keytops, and masked microprocessor. Only the capacitive drive/sense circuitry, switches and some other parts are common to other designs.**

Key Tronic has a standard that requires detection and validation of ten millisecond minimum key closures. If one scan requires 0.5 msec, and validation and output of each new key an additional 0.75 msec, the processor could be doing something else for 80% of the time. Thus, the keyboard would be scanned every 8 msec for a minimum of one half and a maximum of 2 msec (assuming only two new keys down per scan).

The customer can take advantage of this periodic interrogation idea by using a minimum interface keyboard and connecting it to the use of the processor in his system that is already handling other duties (the I/O for instance). The point is that it doesn't require a dedicated microprocessor to run the keyboard.

In summary, the most significant aspects of this new chip set are: (1) a comlete analog keyboard interface has been realized using two IC's and only 2 discreet parts (2) a 96 key capacitive switch fully encoded keyboard with auto repeat and serial output can be produced using only three IC's (2) with annual volumes of 25,000 per year, minimum interface capacitive switch keyboard pricing rapidly approaches that of hard contact switch arrays, while offering solid state reliability.

The primary significance of the "two-chip" design is that it allows the terminal designer to decide where the validation and encoding intelligence resides. In the simplest of terminals, a single processor can easily handle the keyboard in addition to its other duties. In multiprocessor designs, the keyboard and other "peripheral" activities may share a second, slower processor. Of course, complicated designs and those featuring detached keyboards, will often specify a single-chip processor residing on the keyboard. The point is that the 2-chip set allows the terminal designer the choice.

With capacitive keyboards as simple as a plate, switches, keytops, two to three chips, and a circuit board, it's not hard to understand why the capacitive keyboard is, by far, the most attractive combination of price and reliability."

**Rate this Article: 3L, 3M or 3H on Reader Inquiry Card.**

# PRODUCT HIGHLIGHT

New Product Development

# Distributed Automatic Test Equipment

A plug-in microprocessor-based communications PCB, an addition to the family of "smart" cards for the 53A ASCII party line system, allows a central computer to down-load and run BASIC language programs in the 53A system. This card frees the CPU, while the $\mu$P controls the instrumentation.

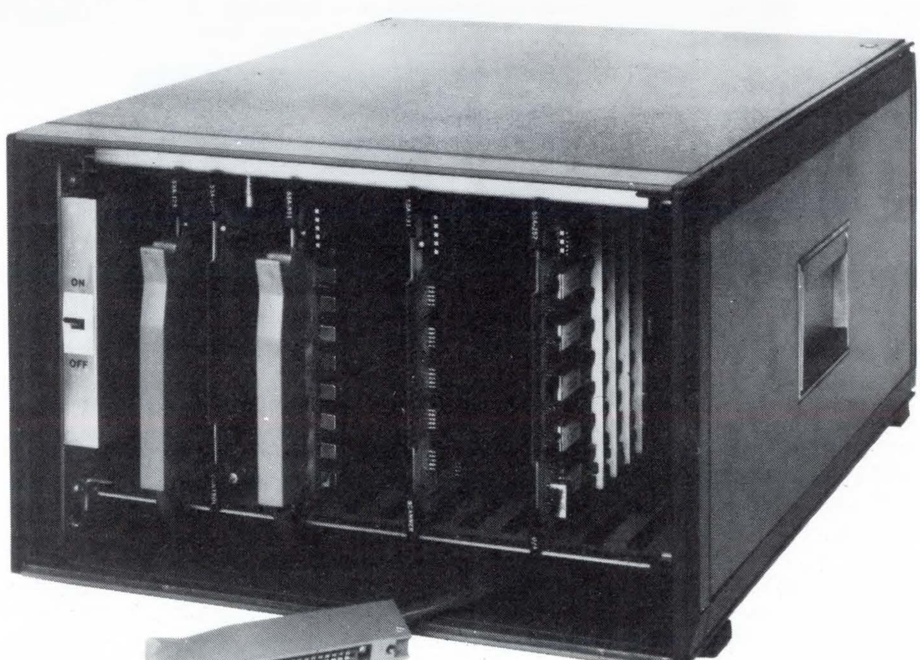
Essentially a multiprogrammer or data coupler with a lot more capability, the 53A system uses a card cage to house a family of programmable plug-in "smart" printed circuit cards. In general, these cards provide D/A converters, counters, stepping motor controllers, relays, resistance programming and digital data coupling such as IEEE-488 bus EIA RS-232C or BCD to IEEE-488 bus. These "smart" cards always communicate with the system controller (calculator or computer) via preformatted ASCII characters using the decimal notation expected by the user's application program. Since the individual cards are smart, a user can add cards to the card cage, delete them from it or rearrange them in it without writing a new software driver.

The $\mu$P-based communications card allows the 53A ASCII party line system to act as a stand alone data acquisition and control system or as an intelligent satellite in a distributed computer system. When performing as a remote satellite, the 53A system can be hardwired or connected via modems for synchronous or asynchronous operation. When used with modems, the 53A system can operate on a multi-drop line with up to sixteen intelligent satellites connected to a single phone circuit.

A comprehensive communication executive in the firmware package allows the central computer to download and run BASIC language programs in remote satellites. Input and output communication buffers store data for transfer when the receiver (53A system or central computer) is not busy. This arrangement prevents the central computer and the 53A system from delaying each other.

The design of the communications card meets the special requirements imposed on remote satellites in distributed system. For example, the card provides dual independent serial communications ports capable of handling asynchronous, synchronous and synchronous bit-oriented protocols such as IBM BiSync, HDLC, SDLC and virtually any other serial protocol. It can generate CRC codes in any synchronous mode and can be programmed for any traditional asynchronous format. The card also supplies four modem control outputs and four sense inputs.

The Z-80 is supplied with up to 20K bytes of EPROM and 10K bytes of RAM. The EPROM contains the BASIC language interpreter and the communication executive. An optional PROM programmer card makes it easy for users to add their own assembly language routines that can be accessed by the BASIC language CALL statement. Price of $2,900 includes card cage and $\mu$P communications card. **Computer Data Systems, Inc.,** 186-58 Homestead, Morrison, CO 80465, (303) 687-8014.



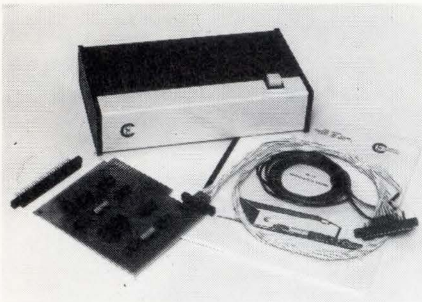

**Communications card in this CDS 53A ASCII party line system which uses smart hardware allows a CPU to download and run BASIC programs in distributed test system equipment.**

# NEW PRODUCTS

### TRS-80, PET CONTROL SYSTEM

Able to sense up to 24 inputs and drive 16 medium power outputs, the SY-16 is a plug compatible turnkey control system with all software and hardware furnished.

The 16 output devices can be any 6 V or less On/Off mechanism using less than 1/4 A.



Input devices can be TTL gates, or any form of switch contacts, including thermostats, reed switches, microswitches, joysticks, keyswitches and numeric keypads. The SY-16 can sense for open or closed condition.

A software timing and control program (STAC) lets the user specify and execute complex timing, sensing and control sequences without having to program, or lets him write programs which call STAC as a soubroutine. $289. **Cooper Computing,** Box 16082, Clayton, MO 63105. **Circle 126**

### 12-BIT A/D CONVERTER FOR μP

The ICL7109 A/D converter chip features a three-state output which enables it to be directly interfaced to virtually any microprocessor data bus which is 8 to 16 bits wide. The device may also be used for remote serial data logging applications.

In the byte-organized parallel mode, the ICL7109 can interface with the data busses of the Intersil 6100, the Motorola MC6800, or the Intel 8080 and 8048. There are 14 data output lines, providing 12 magnitude bits plus polarity and out-of-range bits. The output lines can be grouped in two 8-bit bytes, each activated by its own byte-enable signal, plus a master chip-enable line.

The ICL7109 is available in 40-pin plastic or ceramic dual-in-line packages. $10 and $19.80 (100) **Intersil, Inc.,** 10710 N. Tantau Ave., Cupertino, CA 95014. **Circle 128**

### TRS-80 HANDBOOK

The 108-pg. "TRS-80 Microcomputer Technical Reference Handbook" gives a practical knowledge of TRS-80 hardware system operation. This book shows why there are only 7 address inputs to a 4K RAM, shows when the CPU inputs data from the KB, how the CRT screen is scrolled and much more. Lucid and well written. (But remember, doing any work on your TRS-80 still voids the warranty.) **Radio Shack,** One Fort Worth, TX 76102. **Circle 143**

### TELECOMMUNICATION SERVICES

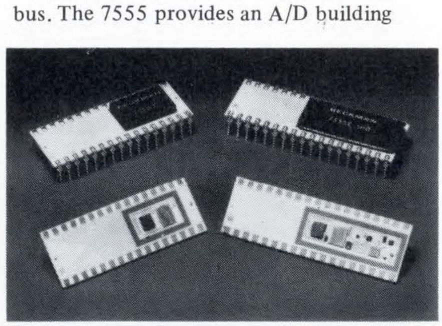
This sourcebook, "Evaluating New Telecommunications Services," is intended for both corporate management and technical specialists. Edited by Martin Elton, this 798 pg. volume is No. 6 in the NATO Conference Series. It explores theoretical developments in information systems. Among the many topics discussed are information retrieval, pattern, recognition, software systems, data base management and data structures. ISBN 0-306-35134-X, $59.50. **Plenum Publishing Corp.,** 227 West 17th St., New York, NY 10011. **Circle 142**

### MULTI-OUTPUT SWITCHING SUPPLY

The Conver 6000 series features PC board construction and standardized modules, with 1300 W in 3 independent outputs of 600, 600 and 350 W. A 6 yr. guarantee backs this multi-output power supply. **Conver Corp.,** 10631 Bandley Dr., Cupertino, CA 95014. **Circle 137**

### μC-COMPATIBLE ADCs

Two CMOS Hybrid 12-bit successive approximation analog-to-digital converters offer guaranteed 12-bit accuracy, 8-bit μP compatibility and TTL or CMOS logic output. Available in both commercial and military models, Series 7555 and 7556 ADCs have 3-state outputs that facilitate a variety of busing schemes for the data bit outputs, as well as a serial register output and an end-of-conversion output. Each data-bit output is separated into a 4-bit MSB and 8-bit LSB byte. Each bit grouping has a separate inhibit line – Low Byte Inhibit (LBI) for LSB's and High Byte Inhibit (HBI) for MSB's – to control when each group drives the data bus. The 7555 provides an A/D building

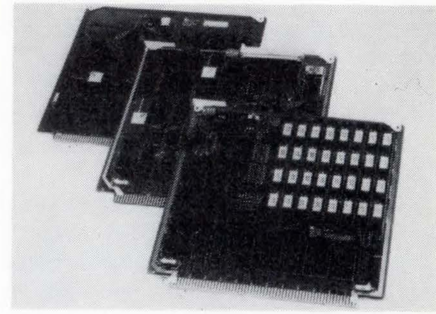


block that includes a successive approximation register, switch and clock chip, thin film ladder network and input scaling resistor, and allows external addition of a comparator and any reference between +10 and -10V. The 7556 is a complete ADC, including 7555 circuitry plus a high-speed comparator and precision -10V reference. The 7556 provides a full 12-bit conversion in 50 μs and consuming 200 mW (typ). 7555, $26.60; 7556, $54.80 (100). **Beckman Instruments, Inc.,** Technical Information Section, Adv. Electro-Prod. Div., 2500 Harbor Blvd., Box 3100, Fullerton, CA 92634. **Circle 127**

### 4 MHz MICROCOMPUTER BOARDS

Four microcomputer boards designed to operate at 4 MHz are for use in OEM computer subassemblies and industrial control.

The principal board in the new series is the Z-80A microprocessor-based board. It contains four Zilog input/output peripheral



components configured to support a line printer interface, direct memory access control, and two independent full-duplex serial communication channels implemented with the Z-80A SIO (Serial Input/Output) and buffered for RS422 or RS423 interface.

The Z80A RAM/ROM memory board is available with either 16K or 64K bytes of dynamic RAM memory. It includes sockets for up to 8K bytes of non-volatile PROM or EPROM.

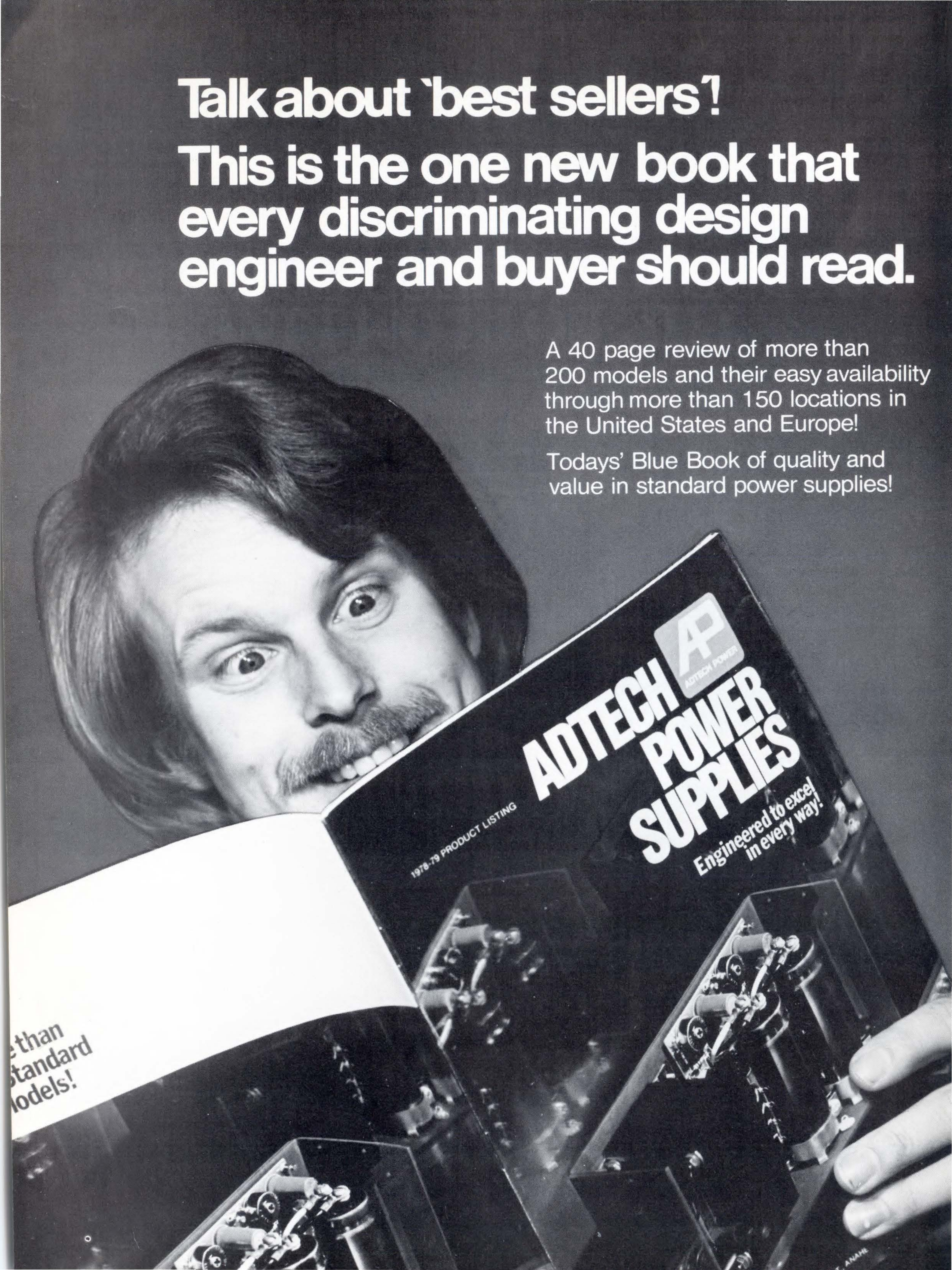
The Z-80A IOB, designed to provide the 4 MHz boards with programmable I/O port capability, has four uncommitted Z-80 PIO (Parallel Input/Output) circuits to support 64 bi-directional I/O lines. $295. **Zilog,** 10340 Bubb Rd., Cupertino, CA 95014. **Circle 129**

### PHASE LOCKED LOOPS

Using TTL and CMOS ICs, this text/workbook covers PLL operation. In addition, over 15 experiments demonstrate the concepts presented. **Bugbooks,** Box 715, Blacksburg, VA 24060. **Circle 140**

### MULTICOLOR GRAPHICS TERMINAL

512 X 512 pixels, 256 simultaneous colors from a pallette of over 16 million colors, ASCII keyboard, programmable function keys, joystick, cursor, zoom, pan, horizontal and vertical scroll, RS-232C or current loop interface – all comprise the AED 512 Graphics Terminal. This high resolution graphics subsystem is intended for OEM's with requirements for sophisticated multicolor or gray scale image processing on computers such as the PDP-11, LSI-11 and Nova/Eclipse. Fully software compatible as a B/W terminal with Tektronix Plot 10, AED 512 utilizes Fortran-callable routines and software drivers for DEC and Data General OS. A typical configuration with 8 simultaneous colors and color monitor sells for $9,920 (79+). **Advanced Electronics Design,** 440 Potrero Ave., Sunnyvale, CA 94086. **Circle 132**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This is the one new book that every discriminating design engineer and buyer should read.
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# NEW PRODUCTS

### TOUCH INPUT DISPLAY PANEL

Unplug your old CRT, plug in a VuePoint, and have computer communication at your fingertips. Only 2-1/2" thick, VuePoint's 12 line by 40 character flat-panel also provides a unique touch input capability. This approach permits operator interaction using

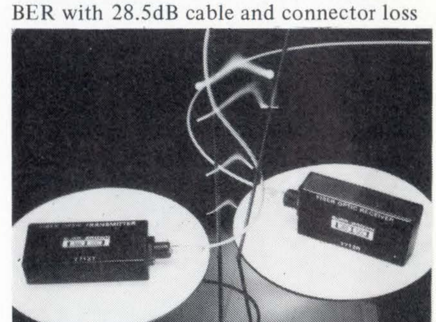
menu driven displays. VuePoint's microprocessor based controller provides all standard "smart CRT" features plus the following: touch response in matrix or screen echo modes; multiple display buffers; and alternate character sets. Communication is by standard 300-19200 BAUD asynchronous RS 232 protocol. Options include wall, or rack mount, auxillary printer and 128 character ASCII keyboard. $3500. **General Digital Corp.,** 700 Burnside Ave., East Hartford, CT 06108. **Circle 130**

### OPTOELECTRONICS HANDBOOK

Titled "Light Sense," this 174-pg. handbook includes chapters on: The Detection Process, Integrating Detection, Light Activated Switches, Photodetectors, Self-Scanned Photodiode Arrays, Camera Systems, Space and Special Applications and Product Data. $6.95. **Integrated Photomatrix, Inc.,** (Muirhead, Inc.), 1101 Bristol Rd., Mountainside, NJ 07092. **Circle 144**

### FIBEROPTIC DATA LINK

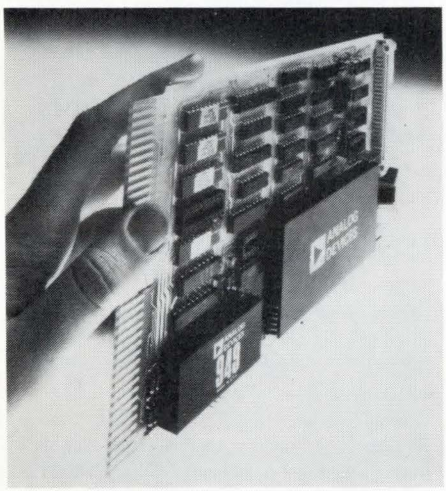
Separately packaged 3712T transmitter (TTL In/Light Out) and 3712R receivers (Light In/TTL Out), when used together with a fiber optic cable, form a low-cost simplex TTL-to-Light-to-TTL data link. The link provides 20k bit operation. Max. link length depends on the type of fiber optic cable used. The units operate with a $10^{-9}$ BER with 28.5dB cable and connector loss



when used with large diameter (40 mil) plastic cable. The link functions properly over distances in excess of 1.5km when low loss silica fiber is used. Units are housed in 1.6 X 3.0 X 0.6" metal packages. Seven pins, located in the bottom of each unit, are suitable for direct PC board mounting and mate with 2800MC connectors. 3712T, $32; 3712R, $100; 2800MC connector, $7.35 (1-9). Complete transmitter receiver combination, under $100 (100). **Burr-Brown,** Box 11400, Tucson, AZ 85734. **Circle 138**

### LSI 11/2 - COMPATIBLE I/O BOARD

For the first time, analog I/O functions have been combined on a single board compatible with the DEC LSI 11/2. The RTI-1250 series of 12-bit input, I/O and output boards offers unique capabilities which include the industry's first analog input and output functions for the LSI-11/2 to be combined on a single card, the first input card to offer up to 32 single-ended (16 differential) inputs, and the first output board which is user-expandable. The complete 12-bit family brings LSI 11/2 users a complete choice



of analog I/O functions on a single card which needs only to be plugged into the LSI 11/2 card cage. All of the boards include a compact DC/DC converter and feature convenient selection of input ranges and operating modes by simple wire wrap methods. RTI-1250, $560; RTI-1251, $695; RTI-1252, $460 (1 - 9). **Analog Devices, Inc.,** Box 280, Norwood, MA 02062. **Circle 135**

### GRAPHIC HARDCOPY MEGRAPHIC 7000

The "Rastorizer" is a vector-to-raster converter and electrostatic printer/plotter interface that produces hardcopy for the Megraphic 7000 vector refresh terminal in 10-15 sec.

There is no need for host computer software preparation to order the vectors – the Rastorizer relieves the host computer of this burden and, at the same time, accepts non-order vector lists. The vector-to-raster conversion proceeds at the maximum output rate of the electrostatic unit producing the hardcopy – approximately 10-15 sec. If the user prefers, the hardware-implemented vector-to-raster conversion still allows the electrostatic unit to be operated as a software controlled plotter, with the user-supplied programs generating the raster bit map. Delivery:60-90 days, $3k. **Megatek Corp.,** 3931 Sorrento Valley Blvd., San Diego, CA 92121. **Circle 131**

### TI $\mu$P DESIGN MANUAL

The soft-cover "9900 Family Systems Design and Data Book" offers over 1,000 pages of both hardware and software information for both engineers doing advanced $\mu$P design work and beginners. It is a complete refer-

ence book containing basic knowledge and data a novice needs to become better acquainted with $\mu$Ps, and carries that knowledge through into complete technical and systems design data needed to use TI's 9900 family of 16-bit $\mu P/\mu C$ circuit boards. **Texas Instruments Inc.,** Learning Center Marketing, Mail Station 54, Box 225012, Dallas, TX 75265. **Circle 133**

### PROGRAMMABLE DATA ACQUISITION SYSTEM

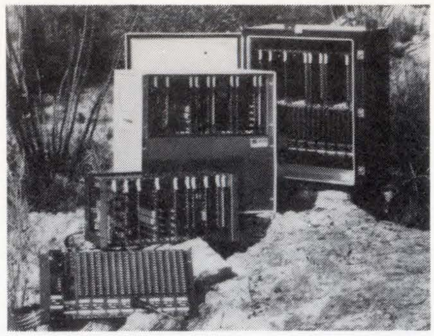
The Dalogger Plus 6200 series MP data system is a hardware and software programmable multipurpose data acquisition system that permits a wide operational latitude in

formatting the data to be outp or recorded. Handling both analog and digital inputs, the M6800-based system provides RS232 and parallel outputs. An on-board tape cassette transport carries programs and records data. The DataloggerPlus provides 16 channels, expandable in 16 or 32 channel increments up to 128 in the basic unit, and 256 additional in each remote unit. Other signifacant features include 4K memory expandable to 32K; gain programmable inputs for each channel; digital calendar clock; high/low alarm capability for each channel; and 20 column alphanumeric printer. **Dynatech R/D Company,** Microsystems Dept., Frank M. Kenney, Vice President, 99 Erie Street, Cambridge, MA 02139. **Circle 208**

# NEW PRODUCTS

## REMOTE INTELLIGENCE I/O SYSTEM

IOS2000, an intelligent I/O system that offers new concepts in distributed I/O systems, uses its on-board preprogrammed microprocessor to function remotely as the sensory center of industrial control and measurement systems. Fully expandable, it is transparant to the CPU and operator and handles all forms of analog and digital I/O.



Application engineering and software development is greatly simplified by the IOS2000 which performs a variety of calibration adjustments, signal conditioning and linearization functions.

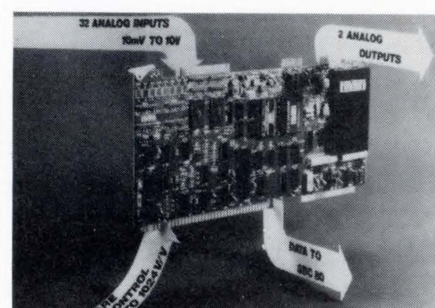
Full capacity of the largest NEMA-4 enclosure and its card file is 256 digital points or 128 analog channels in any combination. **Burr-Brown Research Corp.,** International Airport Industrial Park, Box 11400, Tucson, AZ 85734. (602) 746-1111 **Circle 139**

## DATA ACQUISITION SYSTEM

Guaranteed operation with low level signals and gains to 2000 are offered by the SDM-858, a 12-bit Data Acquisition System. While capable of handling high level inputs, the unit is designed expressly for very low level sensor inputs: Thermocouples, RDT's, strain gages, etc.; SDM858's error at G = 100 is only ±0.25% FS. Analog inputs can range from ±5mV to ±10V and equivalent digital output resolution from 2.4$\mu$V to 4.88mV for this 8- or 16-channel data acquisition system. Accuracy is ±0.025% at throughput rates up to 2000 samples/sec. SDM858 operates from ±15V and +5 V supplies from 0 to 70°C. The metal encased package, designed for PCB mounting, measures 4.6 x 3.0 x 0.375." $170 (100). **Burr-Brown,** Box 11400, Tucson, AZ 85734. **Circle 146**

## $\mu$C-COMPATIBLE ANALOG I/O BOARD

This intel SBC80 MULTIBUS compatible analog I/O system is designed for high and low level inputs. The plug-in compatible MP8418 microperipheral offers 12-bit resolution with 31 channel analog input and 2 channel analog output. A unique option offered on the board is a software programmable amplifier offering 11 binary weighted gains from 1 to 1024V/V. An on-board RAM – part of the option – allows each channel's gain to be set automatically (without use or software involvement) when the channel is addressed.




MP8418 is memory mapped and easily programmed. With gain ranges to 1024V/V, low signal level applications become practical. Complex amplification and software steps are eliminated and system costs reduced. $450 with resistor programmed gain; $550, with software programmed gain. **Burr-Brown,** Box 11400, Tucson, AZ 85734. **Circle 145**

### STANDARD REFERENCE ALIGNMENT CASSETTE

This alignment reference metal cassette is used in calibrating digital and word processing equipment. It is prerecorded at 1600 flux changes/inch on an optical alignment

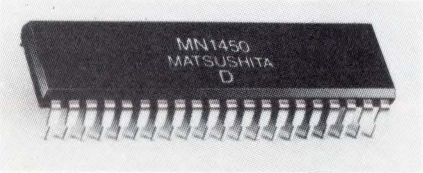

recorder which employs precision magnetic heads. The magnetic tape used is especially made for the digital reference tape application. \$12.50. They are available in several special configurations, allowing them to be compatible with most OEM decks. **Magnetic Information Systems, Inc.,** 415 Howe Ave., Shelton, CT 06484. **Circle 136**

### FREE CATALOG OF REPORTS

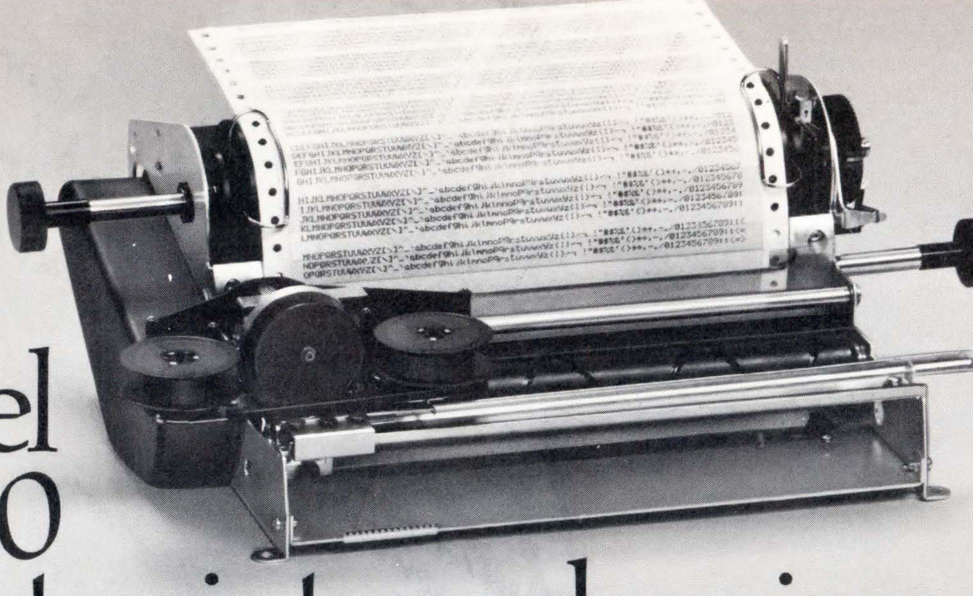
Information processing professionals can look to the revised 1979 Datapro report catalog for compact, objective information comparing thousands of EDP, word processing, office and data communications products. Datapro Research Corporation's free catalog of \$12 reports describes reports on 56 classes of popular equipment and management methods. Datapro feature reports contain informative narratives, comparison charts, prices, specifications and characteristics on currently available information processing products and services. User ratings are included in many reports, adding to their usefulness as planning and buying guides. **Datapro Research Corp.,** 1805 Underwood Blvd., Delran, NJ 08075. **Circle 159**

### ULTRA-LOW POWER CMOS

A new single-chip, ultra-low power (2 MW typical) CMOS 4-bit MC designated as "MN1450," is a low-power version of the previously introduced MN1400. It comes in a 40-pin plastic dip offering a number of "on-chip" functions. These include the ALU, IK x 8 ROM, 64 x 4 RAM with 4 words that are directly addressable, 8-bit counter/timer, two 4-bit



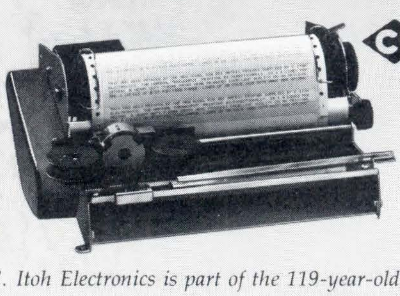

parallel input ports and two sense lines, one 4-bit parallel (with latch) output port, 8-bit PLA (programmable logic array), one 12-bit discrete output port. The MN1450 offers a 75-instruction instruction set, a 10 $\mu$ cycle tiem, and operates from a single +5 Vdc supply. Its I/O is fully TTL compatible. **Panasonic,** 1 Panasonic Way, Secaucus, NJ 07094. **Circle 198**



# The new Model 830 impact print mechanism has something extra going for it.

The new Model 830 bi-directional impact print mechanism may be just what you've been waiting for. It's a low-cost, 80-column dot-matrix mechanism with a printing speed of 125 CPS and a continuous-duty 7-wire head with a life expectancy of 100 million characters. Its straightforward, simple design makes it both highly reliable and cost efficient. In fact, it's just about the perfect OEM unit for general purpose computers, communication terminals, data loggers and micro computers. Its sprocket paper-feed mechanism accepts multi-ply pin feed paper in any width from 4.5″ to 9.5″; paper can be loaded from the bottom or rear; and print line position is readily adjustable. The Model 830 is also available as a self-contained printer. Furthermore, it's from C. Itoh Electronics, Inc. — a name synonymous with excellence in printers. Write for detailed specifications today.

# It's from C. Itoh.



*Model 820, 150 cps and 9.5″ paper width, also available.*

**C. Itoh Electronics, Inc.**

5301 Beethoven Street, Los Angeles, CA 90066
Call: (213) 390-7778 • Telex: WU 65-2451

*East Coast*
280 Park Avenue, New York, NY 10017
Call: (212) 682-0420 • Telex: WU 12-5059

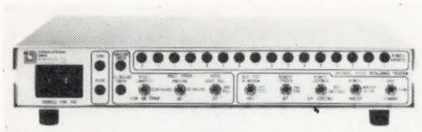
*C. Itoh Electronics is part of the 119-year-old C. Itoh & Co. Ltd., world-wide trading organization.*

**Circle 33 on Reader Inquiry Card**

# NEW PRODUCTS

### POLLING TESTER

The Model 1700 is a $\mu$P-based unit designed to test the polling performance of asynchronous and synchronous data modems. It can be used to test modems over either sim-



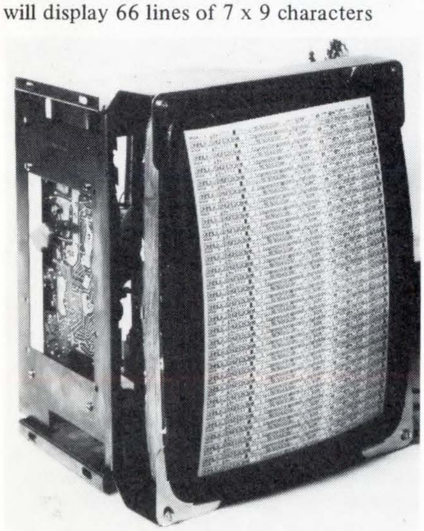
ulated or actual switched networks; private line point-to-point networks; or private line multidrop networks. The Model 1700 can distinguish between outbound and inbound polling message errors and permits the deliberate injection of outbound and inbound polling message errors. $1800. **International Data Sciences, Inc.,** 7 Wellington Road, Lincoln, RI 02865. **Circle 165**

### DISK CARTRIDGE CONTROLLER

The model 2152 Disk Cartridge Control is a single, quad-height 4-layer PC board that provides 2.5 to 20 Mbyte storage. Transparent to the DEC RT-11 and RSX-11S operating systems, the $\mu$C controlled model 152 is media compatible with RKV11/RK05 disk drives. Accommodating 100 or 200 track-per-inch densities, the model 2152 controls up to four 1500 rpm drives and requires a single +5 Vdc power supply. The board performs the basic control and sequencing of data transfers between a $\mu$C and disk drive, measures 10.5" x 8.9" and mounts into any available quad LSI-11 Q-bus slot. **GEN/COMP, INC.,** 6 Algonquin Rd., Canton, MA 02021 **Circle 164**

### FULL PAGE CRT DISPLAY

The VR-800 raster scan monitor is non-interlaced, has a horizontal scan rate of 50 KHz and a video band width of 65 MHz. It will display 66 lines of 7 x 9 characters

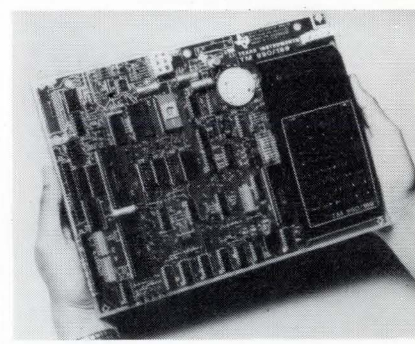


on black and white high speed phosphors. The VR-800 is intended for use in word processing, graphics, and other high density, high resolution applications. **Moniterm Corp.,** Long Lake, MINN 55356. **Circle 163**

## NEW PRODUCTS

### SINGLE-BOARD $\mu$C SYSTEM BY TI

A single-board 16-bit $\mu$C system – the TM 990/189M – is designed as a low-cost, completely assembled learning aid for hands-on experience plus instruction in $\mu$C fundamentals, assembly and machine language and $\mu$C interfacing. A user's guide and detailed applications textbook are included. The textbook is a self-contained learning guide. The board is self-contained with 1K bytes of RAM (expandable on board to 2K) and 4K bytes ROM (expandable on board to 6K). The 4K of ROM contains the system monitor (UNIBUG) and a symbolic assembler. Mass memory storage can be accomplished via the audio cassette interface. Built into the TM990/189M is a 45 key alphanumeric keyboard and a 10 digit, seven segment display. The display has a 32 character buffer. It may be shifted right or left to view any 10 digits of the 32 character buffer. Provisions are on the board to externally add a standard EIA terminal or TTY interface.

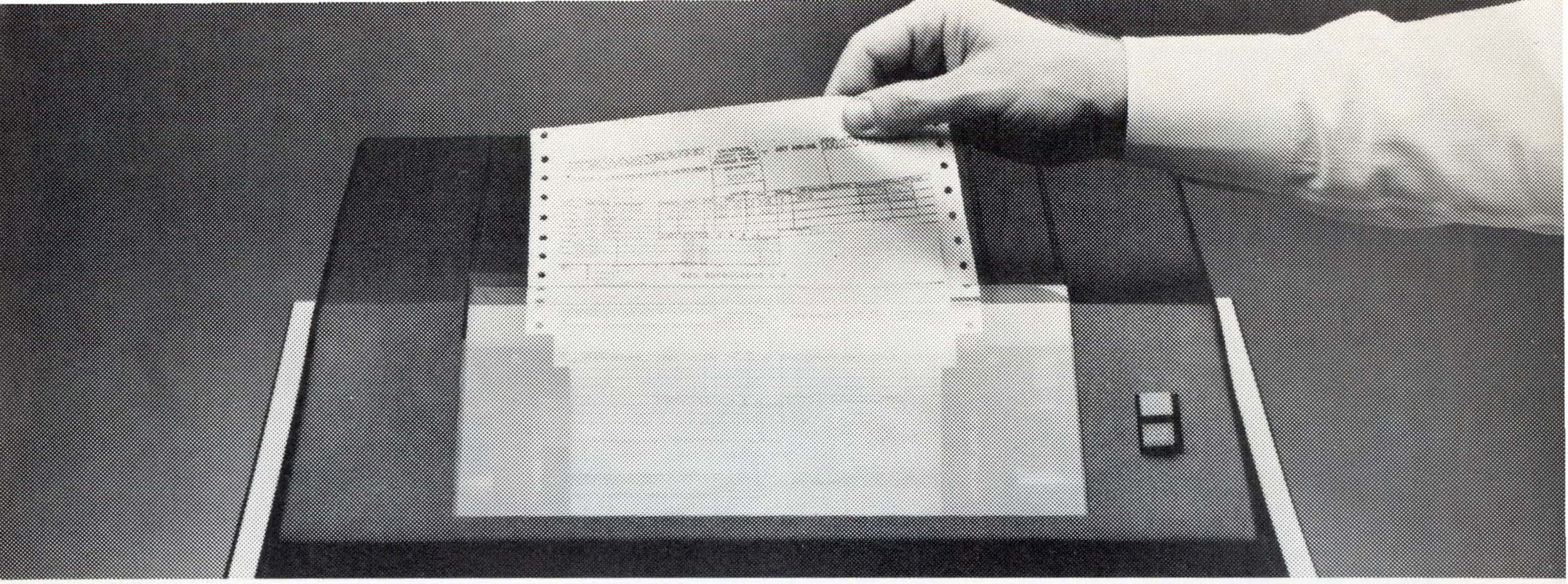


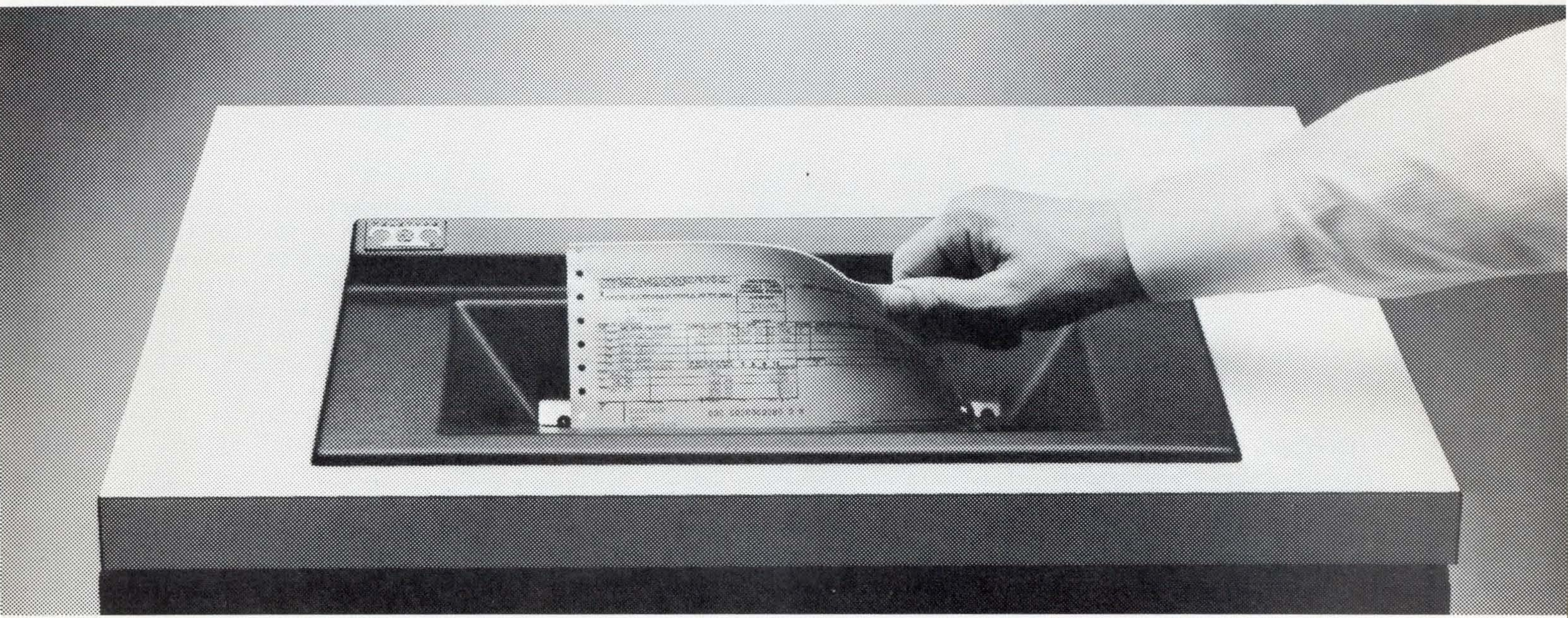
Other features of the TM990/189M include a series of addressable LED's and a piezoelectric speaker. Powering up the $\mu$C not only clears the system, but it also serves for self-diagnosis. $299; power supply $65. **Texas Instruments Inc.,** P.O. Box 1443 M/S 653, (Attn: TM990/189), Houston, TX 77001. **Circle 147**

### HIGH-SPEED BUS CONTROLLER

Using a unique high-speed bus controller design, the RH-70 emulator provides a capability for up to 800 megabytes of disk storage, with total large system capacity ranging up to 2,400 megabytes when used in conjunction with the company's 9400 disk systems. In addition, fully transparent software allows the RH-70 to plug directly into an existing system and go on-line immediately without additional programming.

The 9400 disk storage system also offers microdiagnostics capability for automatic checking of all internal registers. Optional features include the ability to attach multiple CPUs to a common data base. $35,000 for 300 megabytes of storage, controller and all associated interfaces and cables. **System Industries,** 525 Oakmead Parkway, P.O. Box 9025, Sunnyvale, CA 94086. **Circle 134**



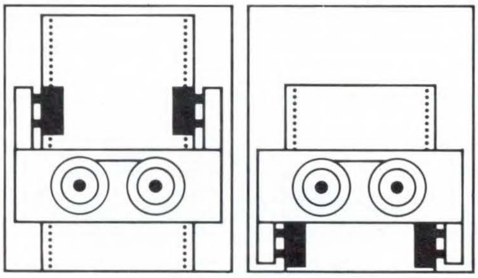


# THE BOTTOM LINE ON FORMS ACCESS PRINTERS.

Why can the Teletype* model 40 printer give you the bottom line when most other printers can't?

Because with the Teletype model 40 printer, you can print from the very top to the very bottom line of any form, tear it off, and never waste or destroy the next form.

<u>It saves paper.</u>
We designed our Forms Access printer with the tractor feed mechanism mounted below the print line. The paper is pushed up through the printer, so you never have to feed a second form through to get at the one you just printed.



Theirs. Ours.

<u>It makes money.</u>
And, while your customers save paper, you make money. Teletype Corporation's low price on the remarkable model 40 makes it extremely cost efficient. Plus our proven LSI circuitry assures you of high reliability.

<u>And it's ready to go to work now.</u>
The model 40 unit includes everything you need to go on-line right now. There's also handsome cabinetry or modification kits available to make packaging quick and simple. Plus technical assistance if you need it.

And that's the bottom line on the Forms Access printer. No wonder we're getting a reputation as the printer people.

Teletype Corporation
5555 Touhy Avenue, Dept. 3185, Skokie, IL 60076.
Telephone (312) 982-2000.

**Circle 35 on Reader Inquiry Card**

*Teletype is a trademark and service mark of the Teletype Corporation.

# NEW PRODUCTS

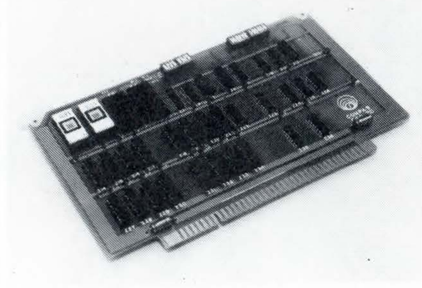
### HARD DISK CONTROLLER

The 211 disk controller is now available for the Control Data Model 9448 cartridge module drive configured into Digital Equipment Corp. (DEC) system. The controller is available in 32 Mbyte and 96 Mbyte versions. Features include: rotational position sens-

ing, automatic position verification, word transfer to 64K block length, buffer storage memory to 512 words, and unique director memory access throttle control. The Xylogics 211 and CDC Model 9448 are available as subsystems at $12,350 for S211/32MB, and $16,250 for S211/96MB. **Xylogics, Inc.,** 42 Third Ave., Burlington, MA 01803. **Circle 153**

### 6500 FAMILY EQUIPMENT

CSB 20 is a RAM/ROM/EPROM card designed for systems based on a CSB processor card or as an additional memory card to the System 65 development system. CSB 20 includes 8K bytes of static RAM provided by 2114 chips, and four sockets are provided for mounting Intel compatible EPROM/RAM chips. All memories are switch selectable for address range and may be disabled under switch control. RAM addresses are switchable in banks of 4K bytes. RAM memory may be write protected. CSB 1 includes a 6502 processor, 2K bytes static RAM, four sockets for mounting INTEL compatible EPROM/ROM chips, two PIA chips, one VIA chip, connector and three sockets for I/O. CSB 1 provides 50 input or



output lines with optional pull-up/pull-down or pull-up resistors, 10 buffered output lines, two interval timers, a serial to parallel/parallel to serial shift register and input put latching on peripheral ports.

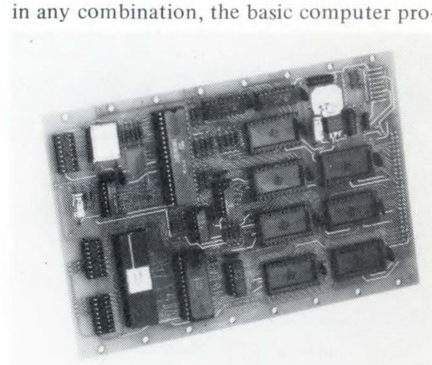
The MINmic cross assembler for 6500 programs is available for any PDP-11 using the RT-11 operating system. New features include: macro expansion, symbolic debugging, a message at end of assembly which indicates how much free room is left in the symbol table, support for multiplication, division and logical AND and OR, parenthetical expressions, and cross reference. CSB 20: $495? CSB1: $594; MINmic: $600. **Compas Microsystems,** 224 S.E. 16th St., Ames, IA 50010. **Circle 183**

### ASCII INTERFACE

The SL111 ASCII interface asynchronously handshakes between computers, $\mu$P's, Teletypes, display terminals, and the Sanlab Series 100 analog scanner line. Data format is serial ASCII with both RS232C and 20 mA current loop transmission standards built in and jumper selectable by the user. Data transmission and reception between the SL111 and the user's data port is in a simple protocol: a "W" prefix writes data to the unit, a single "S" starts an encoding, and an "R" reads data from the system. Transmitted measurement data is prefixed with a "D" by the SL111. The SL111's $\mu$C contains a transmission error analysis routine in nonvolatile memory which tells the host computer or terminal any command errors made in writing or starting. It also conducts a diagnostic subroutine, testing the unit's internal circuitry and all external transmission lines. Onboard jumpers allow user programming of word length, parity, and baud rate. $698. **San Diego Instrument Laboratory,** 7969 Engineer Road, San Diego, CA 92111. **Circle 185**

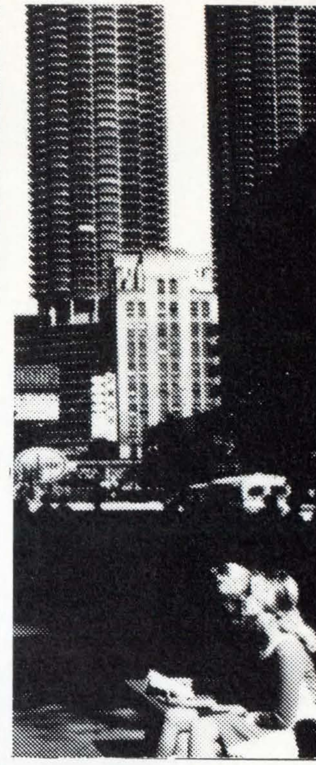
### BUILDING-BLOCK $\mu$C

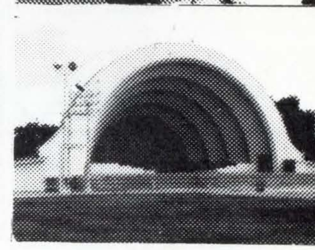
The MCS $\mu$C system features an 8080A-based single board computer that can be incrementally expanded in simple building-block fashion to provide only the functions required. Expandable to 32K of RAM/ROM in any combination, the basic computer pro-



vides 1K of RAM, sockets for 7K of ROM (8708 or equivalent), 24 bits of parallel I/O, 32K of I/O address, and a 2 MHz crystal controlled oscillator. The MCS system needs no card racks, and utilizes ribbon cabling for all signal and power interconnections. All chips are socket mounted. Expansion modules include parallel and serial adaptors, A/D and D/A converters, printers, keyboards, and displays. **Bedford Computer Systems, Inc.,** 3 Preston Ct., Bedford, MA 01730. **Circle 157**

# Northrop Engineers are into state-of-the-art living...and technology!





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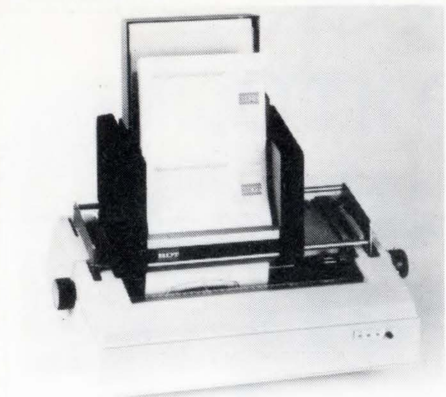
Circle 37 on Reader Inquiry Card

# NEW PRODUCTS

## SHEET FEEDER AND FORM TRACTOR

The Model BDT 160 automatic sheet feeder requires no external interface so it can be easily installed on existing systems that include either Qume or Diablo daisy wheel printers. Up to 250 sheets of 20 pound paper can be fed automatically from the interchangeable 11" and 14" feed trays. A special chute allows the operator to interupt a continuous feed operation at any time to insert a different type of document. Also available is a type of forms tractor that provides continuous form feeding in both directions. The tractors on the BDT Model FT210 engage the continuous paper on both the in-feed and out-feed so the paper can be positively positioned in either direction. Plotting, graphing and variable insertion are allowed by the bi-directional features of the FT210. Continuous forms from four inches to fourteen inches wide can be handled through the FT210, and disengagement switch allows front feeding of cut forms or ledger cards without removal of the continuous forms. BBT 160: $1025; FT210: $230, **MQI Computer Products,** 2315 So. Otis St., Santa Ana, CA 92704. **Circle 180**



## μP I/O MODULE SYSTEMS

An I/O module system with industry-standard pin configuration includes four optically coupled, color-coded modules and four PC module boards (4, 8, 16 or 24 positions). The I/O systems can be interfaced with any 5 V logic unit. The two output modules (ac or dc) will drive a 3 A load, while the two input modules (ac or dc) translate their respective load inputs into standard logic levels. The 8, 16, and 24 position module boards feature plug compatible logic contacts, while the four position board has screw-terminal logic connections. **Gordos Arkansas, Inc.,** 1000 N. Second St., Rogers, AR 72756. **Circle 154**

## APPLICATIONS LIBRARY

Release 1.0 of the timesharing applications library is available for users of Honeywell series 60, level 66 large-scale, computer systems. The library contains 292 pre-written problem solving programs and routines. The library contains such major programs as: CPM, for project control; TCAST, for time series forecasting; SMLRP, for stepwise multiple regression, and GASP IIA, for discrete simulation. The library has programs dealing with the following categories: mathematics, 77; statistics, 70; management science and optimization, 37; engineering, 14; geometry and plotting, 9; demonstration, 12; business and finance, 31, and utility and miscellaneous, 42. The library is available for an initial license fee of $2,628, or a monthly license fee of $60. **Honeywell Inc.,** P.O. Box 6000, Phoenix, AZ 85005. **Circle 167**

## 16 MEGABYTE μC

The Mk-16, a new high speed 16 bit μC, features. 14 general registers; 23 address modes; 16 Mbyte addressability; dynamic writable control store; concurrent Pascal compiler; and cross and resident software. The system uses the philosophy of bit slice microprogrammability in a single chip processor. Mikros is offering a Pascal development system (PDS-1) which includes a video display terminal, 56 Kbyte computer system, floppy disk, monitor program and Pascal P-Code software for $12,500. **Mikros Systems Corp.** 845 Central Ave., Albany, NY 12206. **Circle 160**

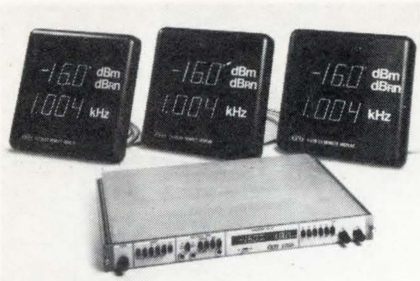
## TELEPRINTER WITH BUFFER

The TermiNet 1232 teleprinter, featuring 132 columns, is designed for use at rates to 1200 baud and includes a 1K buffer. It is available in Keyboard Send-Receive (KSR), Receive-Only (RO), Automatic Send-Receive (paper tape) or Magnetic Send-Receive (magnetic tape) configurations.

Front or rear paper handling is a standard feature while six pin tractors handle one to six part forms. Paper widths from 3 to 15 inches can be accommodated. Horizontal tab and vertical formatting are standard with 10 cpi horizontally and six lines per inch vertically. Operator selectable six or eight lines per inch is available optionally. Speeds are switch selectable, 10, 20, 30, and 120 cps. $5155. **General Electric Co.,** Data Communication Products Business Dept., Waynesboro, VA 22980. **Circle 159**

## TEST SET WITH REMOTE READOUTS

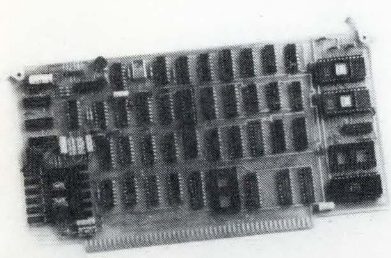
A digital transmission test set with remote readouts, displays frequency and level, or frequency and noise simulateneously. The microprocessor-based TTI 1122B drives mul-



tiple remotes at distances up to 600 ft. via a simple 2-wire cable. The mainframe panel is 1-3/4" high and weighs 7 lbs. The test set checks and diagnoses itself in 12 sec under microprocessor control – testing display functions, log converter, autoranging, control circuitry and all major digital functions. $1395 for the mainframe and $495 for each remote dual display. **Telecommunications Technology, Inc.,** 555 Del Rey Ave., Sunnyvale, CA 94086. **Circle 181**

## 32K MEMORY BOARD

The model 370 is a 32 Kbyte static RAM board that operates on the S-100 bus. The board's starting address can be selected at 4K boundaries. Memory mapping capability is included so that more than 64 Kbytes of



memory can be utilized in a system. Processor Write or Memory Write signals can be selected for writing data into memory, and Phantom Line capability is included. **Industrial Micro Systems,** 628 N. Eckhoff St., Orange, CA 92668. **Circle 162**

## GRAPHIC TERMINALS DATA

A new section, designed to provide comprehensive coverage of the graphics display terminal market, has been added to the Auerbach Business Minicomputer Systems Reports (a monthly updated reference). Contained in the two-volume loose-leaf service, the graphics display terminal reports include complete information. As well as the graphics display terminal coverage, additional reports on terminals contain the latest data on teleprinters, alphanumeric displays, remote batch terminals and intelligent terminals. More than 450 models of terminals from over 130 different manufacturers are included in these sections. **Auerbach Publishers, Inc.,** 6560 North Park Dr., Pennsauken, NJ 08109. **Circle 155**

## HF μP MODEM

A programmable Sylvania high-frequency μP modem employs fast Fourier transform and digital filtering techniques to form multitone audio signals, and performs digital operations with a minimal amount of logic. It features large scale integrated circuit TTL four-bit slice arithmetic and logic units, time shared under program control, to perform required arithmetic and logic operations. It also includes a program memory, data memory, power supply, A/D and D/A converters, analog interface modules and digital interface logic. Its internal computational accuracy is normally 16 bits although double precision (32 bits) and block floating point techniques are utilized for certain functions. **General Telephone and Electronics,** 1 Stamford Forum, Stamford, CT 06904. **Circle 169**

## IMAGE ANALYSIS SYSTEM

The Polyprocessor C1285 image analysis system provides automated analysis of discrete objects in any image which can be viewed by a video camera. The Polyprocessor system analyzes information from images, using a combination of optical, video, and computer hardware to measure, analyze and tabulate height, width, diameter, total area, inner area, outer area, perimeter, percent area and location of up to several hundred discrete objects in each image. Features include: digital noise reduction, interactive image editing, image storage, and shading correction. The C1285 is easily interfaced to optical microscopes, macroviewers, film viewers and other optical systems. An RS232C printer output allows production of hard copy. **Hamamatsu Systems, Inc.,** 332 Second Ave., Waltham, MA 02154. **Circle 166**

## EPROM-ERASING UV CABINETS

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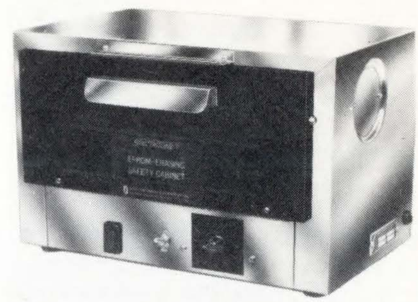

intensity, ozone-free grid tubes and specially-designed specular reflectors to provide broad, intense, uniform UV distribution. A conductive foam pad holds the chips in place during exposure and prevents electrostatic build-up, while protecting the chips from possible static charge. PC-1000: $895; PC-2000: $1,345. **Spectronics Corporation,** 956 Brush Hollow Rd., PO Box 483, Westbury, NY 11590. **Circle 158**

# µP APPLICATION

# 6800 Replaces Minicomputers and Controls Elevators

C. Halatsis and A. Sokos
*Computer Center, NRC*
*Demokritos, Aghia Paraskevi Attikis, Athens*

Microcomputers and microprocessors are solutions looking for problems. Many applications that withstood the impact of electronics are ripe for solution. We looked for such an application and found one — elevator control.

Minicomputers in elevator control aren't new. But cost restricted them to the group control of multi-car elevator systems in multi-floor buildings. The mini provides traffic supervisory control, monitoring the incoming traffic, selecting the appropriate control algorithm and allocating the elevator cars to the floor-call requests in the most efficient way.

We felt that we could successfully employ a micro in the control of common elevator systems in an economical way. For this reason, we considered a single-car four-floors elevator system, controlled by the Motorola 6800. Though such an elevator system usually uses a single button collective con-

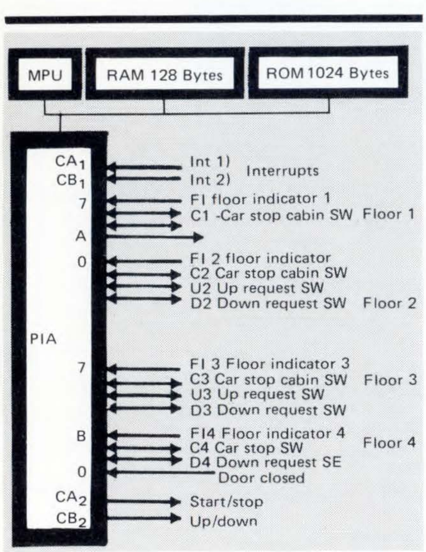


**Fig 1 Elevator control microcomputer, PIA matches I/O MPU channels with peripherals.**

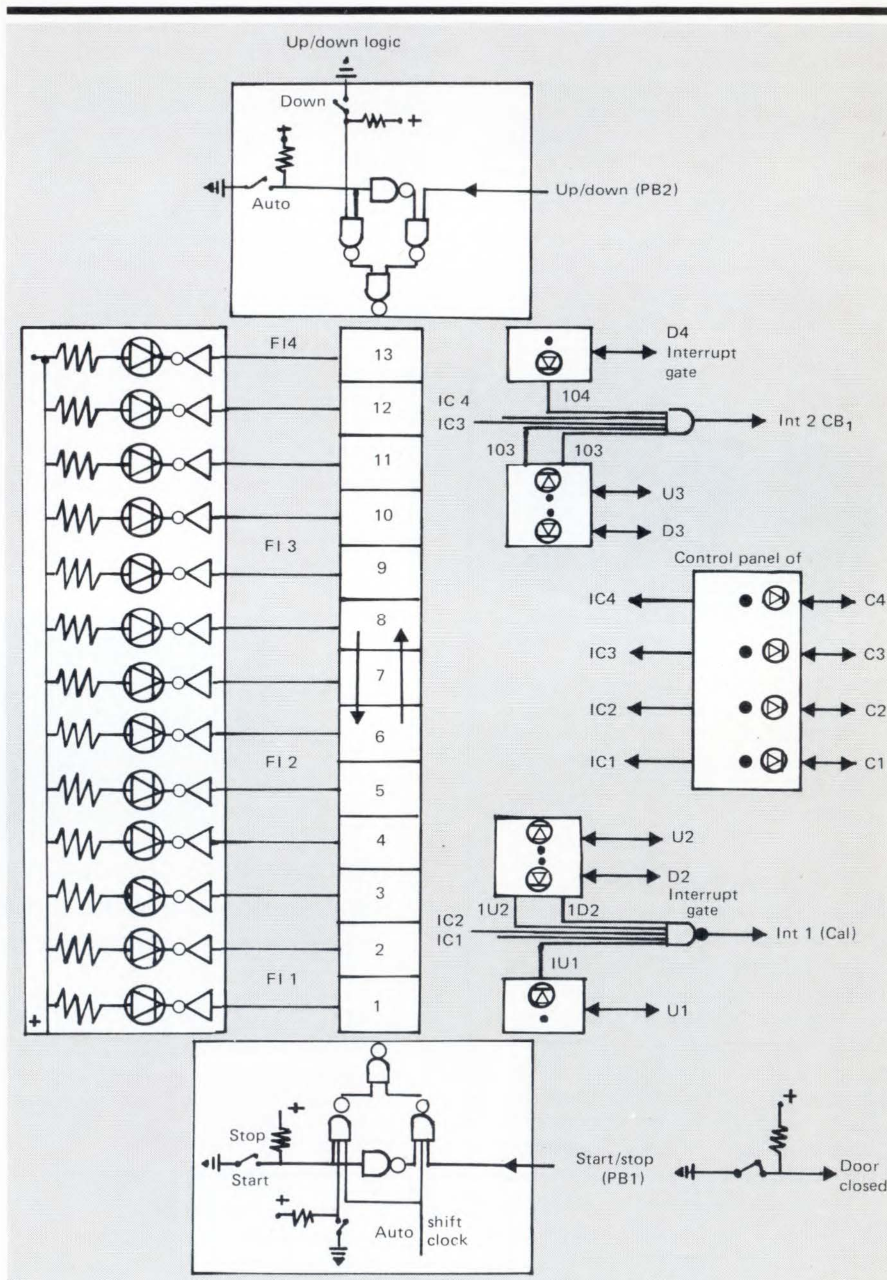


**Fig 2 Digital model block diagram shows logic involved in elevator car control.**

trol, we implemented a directional or full (two button) collective control in order to demonstrate that the facilities and features of a $\mu$P-based elevator control algorithm is mainly limited by the imagination and ingenuity of the designer — not economics.

The system operation was first tested on a simplified elevator digital model. The model was interfaced to the Motorola Evaluation System and operated under the control algorithm.

**Fig 1** shows the block diagram of the elevator control microcomputer. It consists of a microprocessor unit (MPU), a 128 bytes RAM, a 1 k bytes ROM and a peripheral interface adapter (PIA). The ROM holds the traffic supervisory control algorithm. The RAM is used as working store of the algorithm and as stack area for subroutine nesting and interrupts. A single PIA is used to interface the various elevator control signals to the $\mu$C. The various control signals used are as follows:

FI1 to FI4: Floor indicators for floors 1 to 4, signalling the arrival of the car to a floor. These signals are generated from switches located in the shaft of the elevator and activated by the car as it passes by.

C1 to C4: Car stop requests for floors 1 to 4, signalling the intention of a passenger to get off the car. These signals are generated by push buttons in the control panel inside the car.

U1 to U3 and D2 to D4: Car call requests for floors 1 to 4, signalling the need and the intended direction of travel. One UP and one DOWN push button are located at each floor (floor 1 has only an UP switch and floor 4 only a DOWN switch). A passenger at a floor calls the car by pressing the appropriate switch for the intended direction of travel.

START/STOP and UP/DOWN: These two lines control the movement of the car.

LOCK/UNLOCK DOOR and DOOR CLOSED: These two lines control the opening and closing of the elevator's doors. It is assumed that the doors are operated manually by the passengers. The microcomputer merely locks (0) or unlocks (1) the doors and checks whether a door is opened or closed. The LOCK/UNLOCK DOOR signal unlocks only the door of the floor at which the car stands. The DOOR CLOSED signal indicates whether all doors are closed (0) or one of them is open (1).

INT 1 and INT 2: These lines carry external interrupt requests whenever any UP, DOWN or car stop push buttons are pressed.

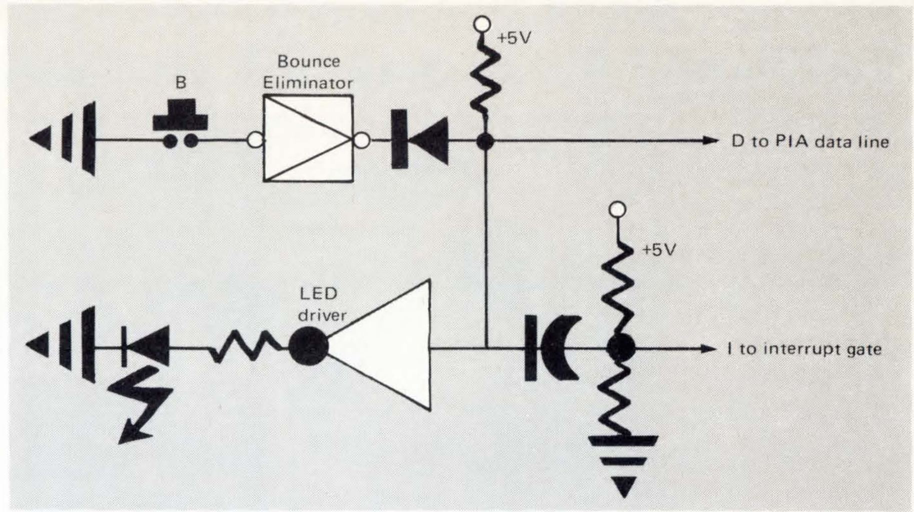


**Fig 3 Pushbutton and LED indicator interface circuit.**

**Fig 2** gives the block diagram of the digital model of elevator used to test the performance of the $\mu$P-based control. The main part of the model consists of a 13-stage bi-directional shift-register used to simulate the elevator shaft. Four stages of the shift-register are used for each storey except the last. A "1" going up and down in the shift register simulates the car of the elevator. LED indicators connected at each stage of the shift register give a visual indication of the position of the car in the shaft. Stages 1, 5, 9 and 13 are the floor levels at which the car is normally stopped.

Push buttons are provided for the car stop requests and the car call up and down requests. Each button is accompanied by a LED indicator which is used by the $\mu$P to acknowledge the request. The interfacing circuit of the push button to the $\mu$C and the LED drive logic is kept to a minimum by

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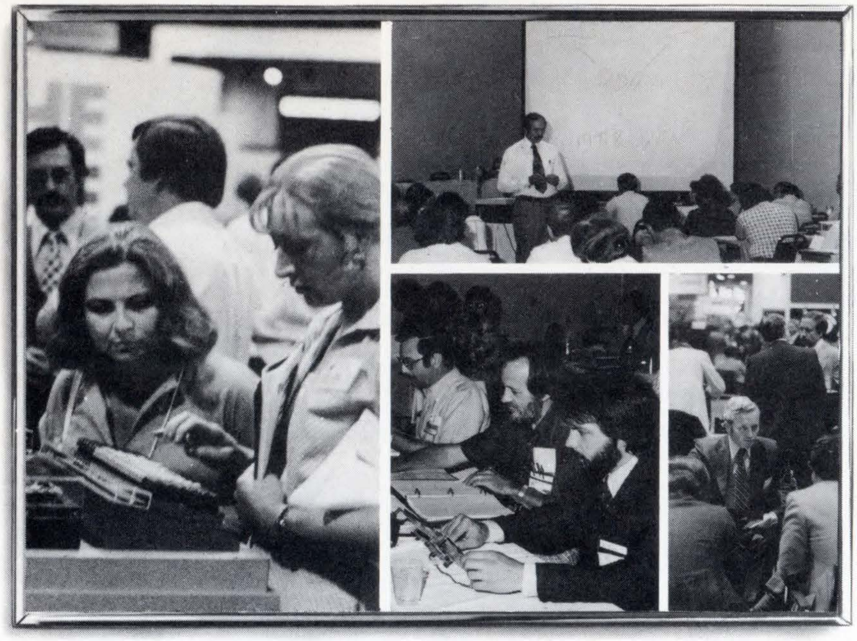

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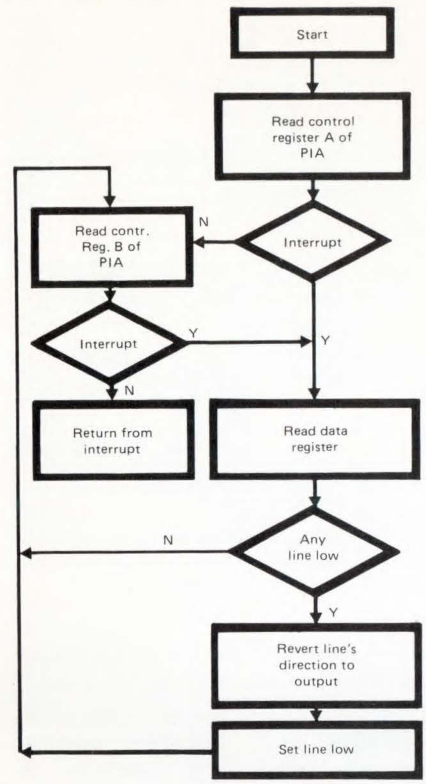


**Fig. 4 Flow chart for interrupt service routine.**

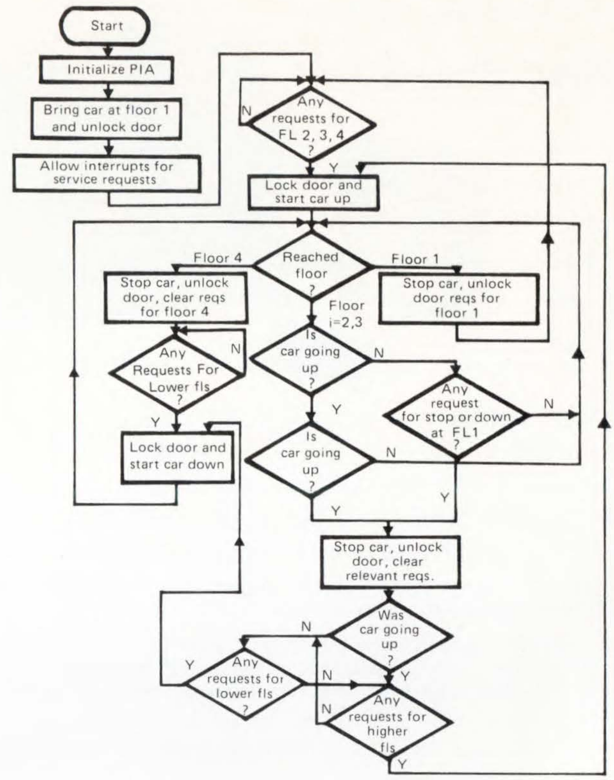


**Fig. 5 Flow chart for main service program begins by initializing the peripheral interface adapter before bringing the car to level 1. Flow chart is self evident.**

exploiting the bi-directional characteristics of the PIA data lines. **Fig 3** shows the interface circuit.

The operation of the circuit is as follows. The PIA data line D is initially programmed as an input line. When push button B is pressed the D line is brought to a low state and the LED lights up temporarily. At the same time a pulse appears on line 1 which through an interrupt gate of **Fig 2** causes an external interrupt to the microprocessor. The interrupt service routine of the control program scans the PIA ports, finds D low and reverts it to a low output line. This causes the LED to light up even after the release of the button, informing the passenger that his request has been registered for service. When the request has been serviced the D line reverts back to an input line. This exploitation of the PIA not only reduces the number of lines required to interface the elevator to the microcomputer but also eliminates the need to provide the push-button logic with local memory. Observe also in **Fig 3** that, once a request has been acknowledged, subsequent pressing of the push button — something which passengers have a tendency to do — does not cause further interrupts.

The movement of the car ("1") in the model is controlled by the START/

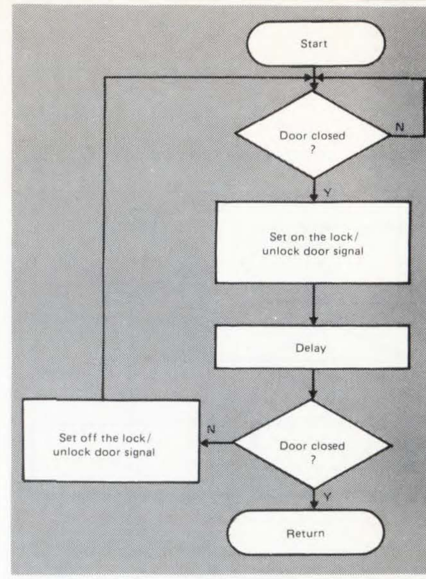


**Fig 6 "Lock door" procedure.**

STOP logic and the UP/DOWN logic (see **Fig 2**). The control signals coming from the microcomputer control are combined with manually operated switches which may override the microcomputer control, in the event of a failure, for example. Lastly, a switch in the model provides the DOOR CLOSED signal.

The model does not provide any "car loaded" and/or "car overloaded" signals, as may be found in a real elevator. However, these signals could be combined with the DOOR CLOSED signal in a way that the door looks closed when it is actually closed and the car is loaded and not overloaded. Another approach to cope with these signals as well as other refinements — such as motor-controlled doors with light beams — would be to provide separate I/O lines to the microcomputer control.

The operation of the system is governed by the control program which in a real situation will be stored permanently in a ROM or EPROM. As stated in the introduction, the control program implements a directional collective control algorithm. In this, the car stops to answer both car stop requests and car call requests registered in the car direction of travel, in floor sequence. When no more requests of either type are registered in the direction ahead of the car, the car moves to the furthest floor at which a car call for travelling in the opposite direction is registered, if any, reverses its direction of travel and starts answering calls in the new direction. DD

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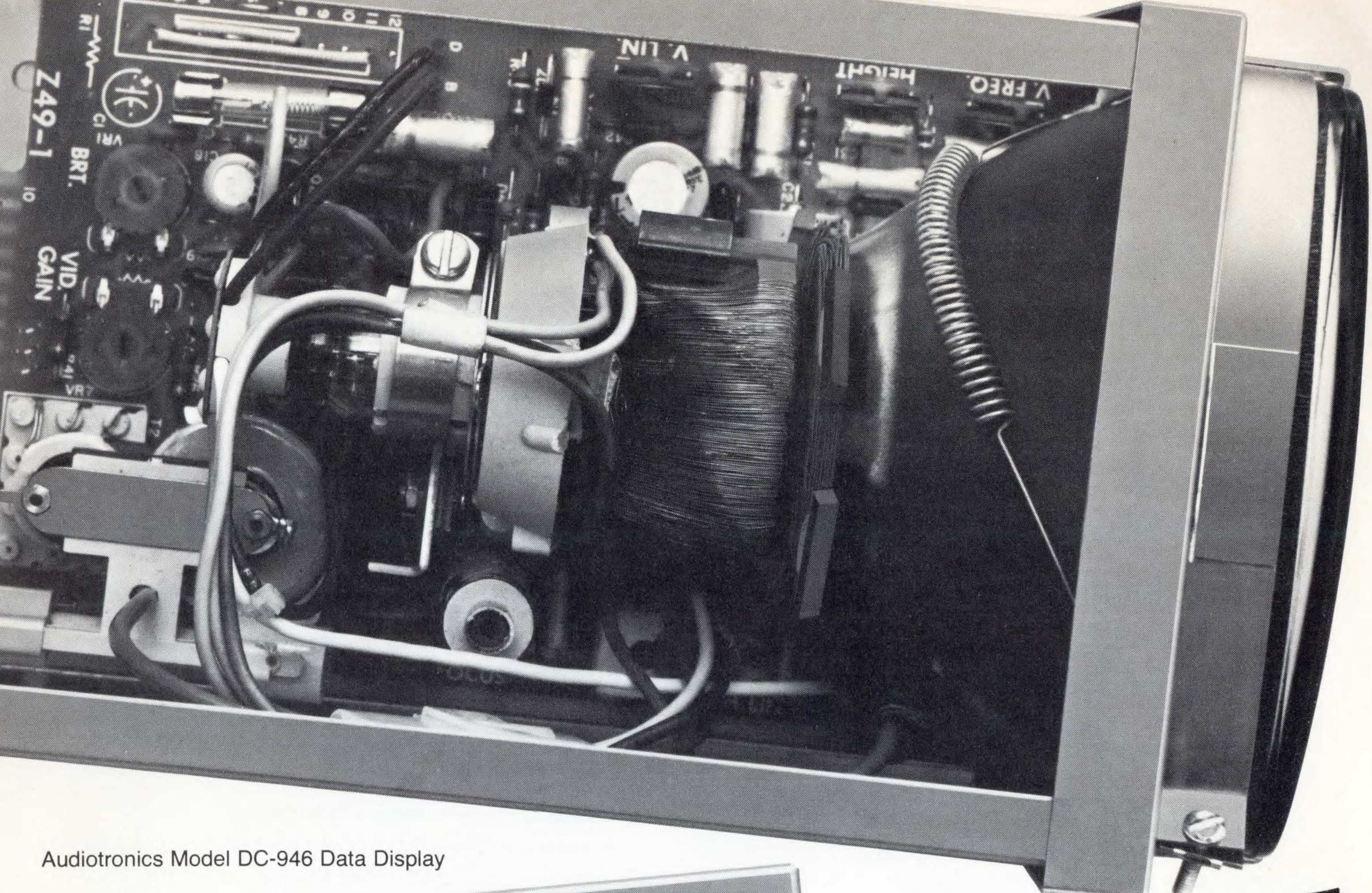


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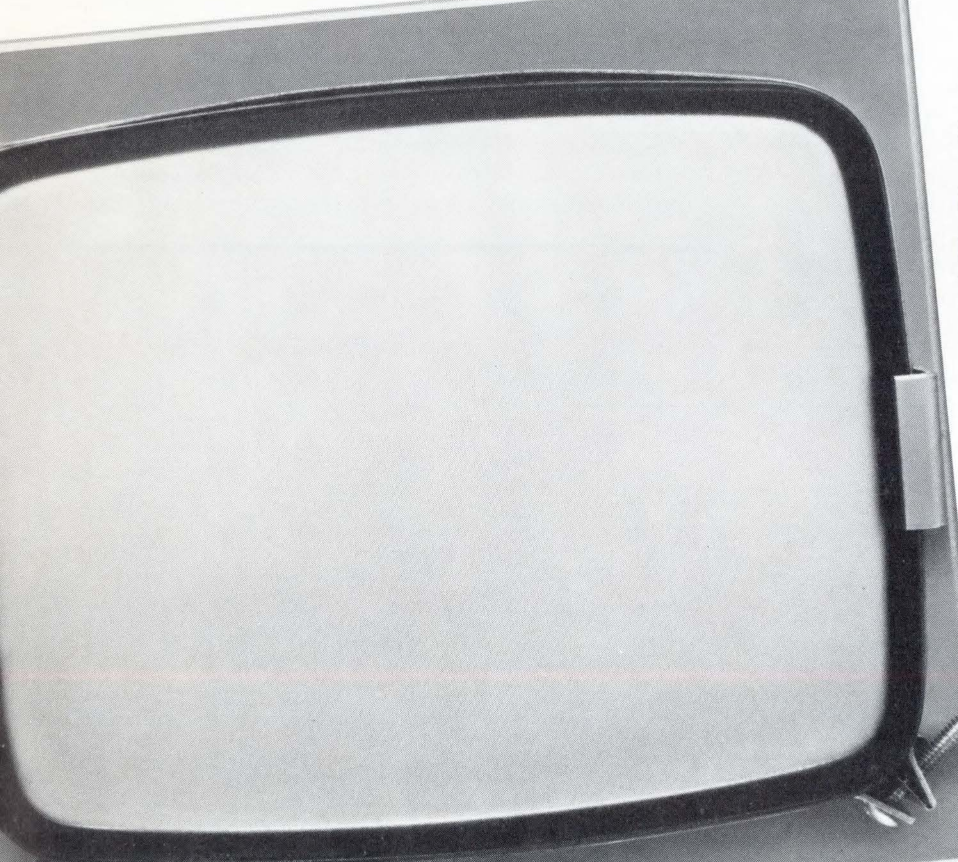

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# PROGRAMMABLE µP-BASED SYSTEM
## Provides Total Energy Management

**Staff Report**
*Sunkeeper Corp., Andover, MA*

There are many potential applications for microprocessors at today's hardware prices, but there are not enough programmers to develop software to handle them. This lack of trained programmers is a major problem limiting the microprocessor market. One solution is to shift the programming burden to the end user by providing computer languages which can be learned easily. When the customer takes over the programming, the vendor is not involved in tailoring systems for specific applications. Furthermore, customers discover unexpected applications, which greatly expand the market.

The Sunkeeper controller – the first µP-based, programmable system designed for total energy management – is an excellent example of a µP controller incorporating a special purpose language. Solar systems require sophisticated control mechanisms, and control procedures differ from installation to installation at the whim of the owner. We designed an M-6800-based energy system controller with 32 analog inputs, 32 digital inputs and 32 digital output drivers.

If Sunkeeper had written conventional control software, a programmer would have been required to modify the software for each installation, and for each change in the way the building was run. This would have placed severe restrictions on the controller's marketability. Instead, Sunkeeper decided to commission a proprietary user-oriented language.

### Sunkeeper language concept

The problem was to define a language which was natural enough to be learned quickly by heating contractors. Also, to minimize confusion among many engineers working on a building over a period of time, it was necessary that the language constrain its users to write programs which could be readily understood by others. This "plumbing" language had not only to be intuitive, it had to prevent its users from writing programs which were difficult to understand.

After much wrangling, a language based on sequence drums emerged. Sequence drums have been around for a long time and, being mechanical devices, are readily understood during training sessions. A sequence drum is built like a Swiss music box, with a lot of pins stuck in lines of holes in the drum. As the drum rotates, the pins hit switches, causing things to happen. Master drums are usually driven at a constant rate, and slave drums can be started and stopped by switches on master drums.

The drum analogy illustrates one of the most important aspects of designing a computer language. The language must have an underlying concept which is easy to understand. User's questions can usually be answered by referring back to the fundamental imagery, and deducing how the real system would work. This ability to visualize the computer language in terms of a real device helps greatly with user acceptance.

Choosing an image determines most other aspects of the language. Training aids, language syntax, debugging aids, error messages, communication facilities, and all other points of contact between the user and the language must be implemented in a manner consistent with the idea, in this case, of sequence drums. It is not easy to choose an image which is both simple enough to be taught easily and powerful enough to cover the requirements of real world problems.

### Making the hardware act like drums

Although the hardware is nothing at all like a real sequence drum, a Control Program (CP) was written which acted as if the microprocessor contained 40 drums of up to 99 lines each.

Customers were intended to use different drums to control separate parts of the heating system. For example, one drum could control a solar collector, another the energy storage system, and another the air conditioner. It is necessary for information about each subsystem to be available to control other subsystems, and 64 communication bits

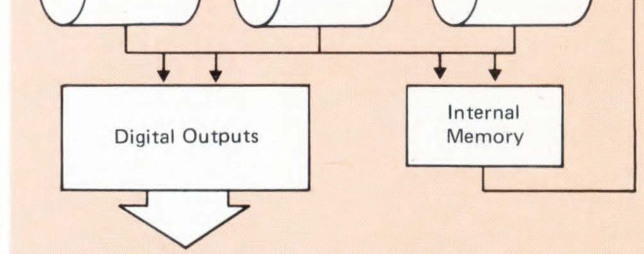


**Fig 1 Sunkeeper's "drum" concept enables input signals to be introduced selectively to any of 100 data lines on eight standard operations drums and a ninth emergency operations drum. If conditions are satisfied, the inputs will either be transferred to other data lines for further processing per internal instructions or exited as output signals.**

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# Total Energy Management

Total energy management – the conservative use of energy to preserve scarce supplies and to reduce operating expenses – requires a versatile, manageable control device capable of performing those functions necessary to supervise and select the best choices. Said to be the first commercially-available system specifically designed for user control of conventional energy sources and integration of all energy sources (including solar energy) on a cost-effective basis, the 6800-based Sunkeeper Controller gives users direct, immediate, personal control over energy consumption. It provides a means of scheduling and directing energy usage through the establishment of programmed instructions and capability to modify those instructions instantaneously to meet changing conditions or achieve further efficiencies.

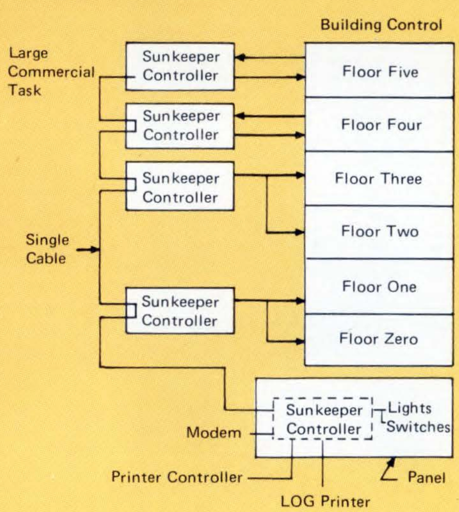


**Fig 2 Systems can be configured to virtually any situation. Here, locations with more critical environmental or functional demands are assigned to individual Controllers, while others are accommodated on a shared-Controller basis.**

Demand-limiting and timed duty cycling can be user programmed both to normal turn on/turn-off requirements and to variations in building usage and occupancy. Heating, ventilating and air conditioning can also be regulated automatically in response to sensor data as well as to pre-set date/time conditions. Enthalpy control, outdoor re-set, night set-back and weekend skip are all within the capabilities of the Sunkeeper.

Process equipment start-up and shut-down, integrated into a total building energy usage program, will increase power factor efficiency and reduce energy costs.

This system also permits introduction of supplementary or alternate energy sources at the proper times without imbalance or interruption. Off-peak power usage and solar heating usage can be optimized when included in an overall management system.

The simplicity, low-cost and flexibility of such a system make it universally adaptable to industrial, commercial and institutional applications.

are provided to let the drums communicate with one another without affecting the output drivers. These bits are turned ON or OFF or examined by the drums, but have no direct effect on the external system.

Information flow within the CP is shown in **Fig 1**. At the beginning of each control cycle, the CP records the state of the digital inputs, memory bits, and analog inputs. Then it processes one line for each drum. Each line specifies settings for output drivers and memory bits, and may define two sets of conditions for rotating the drum to another line. After setting the outputs as specified in the line, the CP examines the conditions for leaving the line. If the conditions are met, the CP changes the line number for that drum so that the new line is evaluated during the next control cycle. Unless the operator manually "rotates" it, a drum remains on a line until one of its exit conditions is satisfied.

## Additional features

In order to successfully utilize the sequence drum concept, it was necessary to provide features attuned to building management. Just as a real sequence drum is augmented with relays, switches, and thermostats in order to be useful, simulated drums need building management facilities such as a built-in clock and calendar, because buildings follow a daily or weekly cycle. The CP must also be proof against power failure. This requires battery backup for the clock and for the memory which holds the customer's control sequence. In addition, a telephone interface is provided to let the customer call up the unit to determine its status or change the program without visiting the building. This minimizes service calls. In order to help sell advanced heating systems, the CP records data and averages them over a period of time. This log can be printed out over the telephone line, showing how much energy has been saved by the system.

All quantities are converted from binary into user units such as degrees Fahrenheit, percentage of the time that a heater is in use, etc. Such features added significantly to the complexity and cost of the software, but have had a great deal to do with the system's commercial success. Such facilities are expensive to add not only because of the programming involved, but because of the added design time needed to merge these features into the overall language philosophy. Because sequence drums do not have calendars, the sequence drum concept does not provide hints for calendar management. Integrating features which have no real world analog can be difficult. The only criterion for success is user acceptance.

## Sunkeeper language

Once the overall structure was chosen, the next problem was to select an operator terminal. Most interaction between the user and the system takes place via the terminal, and the choice of terminal strongly affects the ultimate viability of the interface.

Because of its high bandwidth, a CRT makes a much better human interface than a typing terminal. In addition, the user could change a control sequence by typing over drum lines which were to be changed. However, none of the available CRT terminals were portable enough to make a plausible addition to a plumber's tool kit. Small rugged teletypewriter equivalents were available, and it was reluctantly decided to structure the language around a teletypewriter. This constrained the human interface to a stimulus-response strategy, where the user types a command, and the computer responds to it. Placing the initiative on

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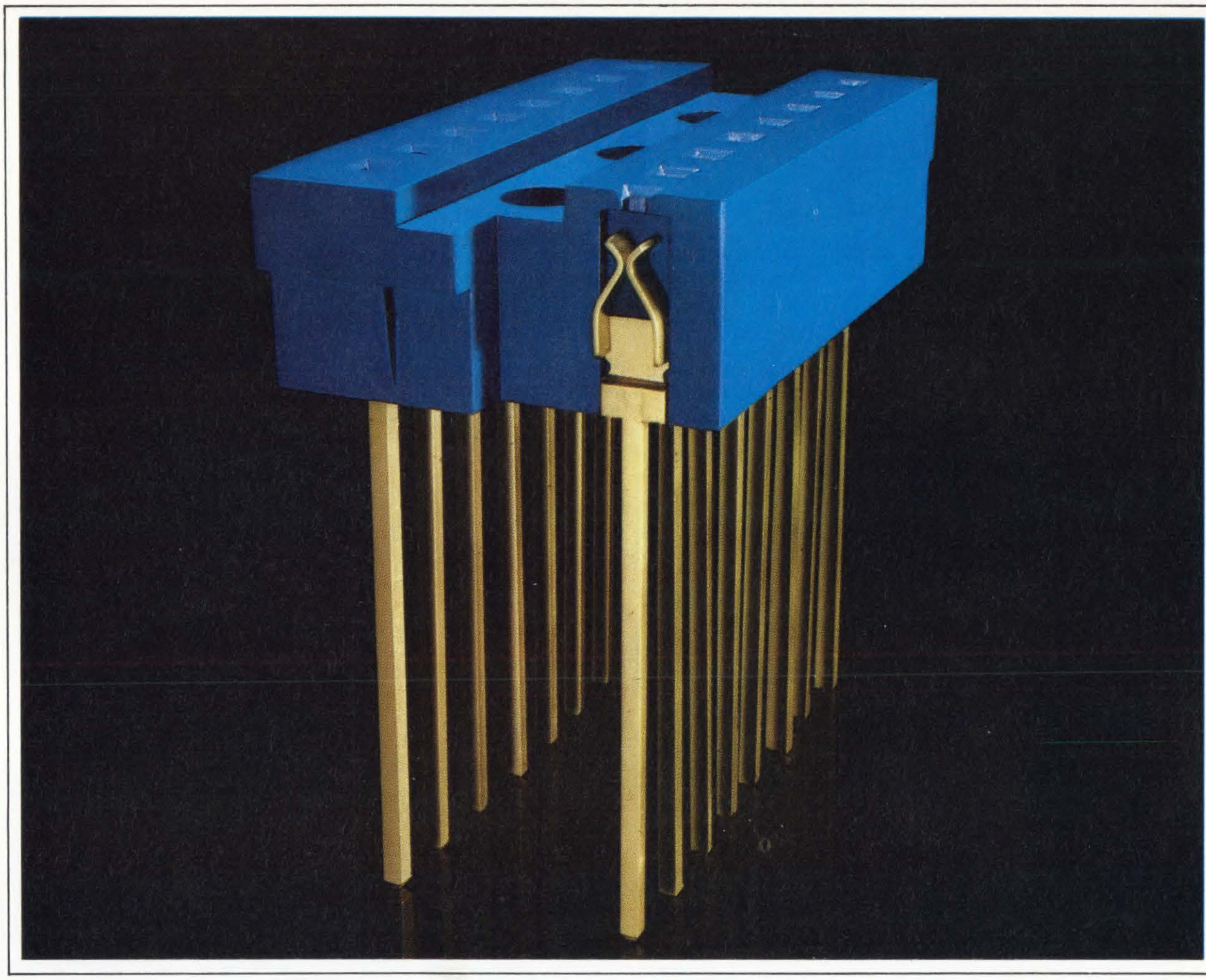

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the user makes it much more difficult to achieve an intuitive language.

The next difficulty was command names. Long mnemonic names are easier to remember, but are tedious to type. In addition, storing long names in a command table requires more memory than storing short names. The language finally evolved to a set of single letter commands such as "P" for Print, "O" for ON, and "F" for OFF. These commands are followed by another letter indicating what type of data the command is to operate on, such as "M" for drum, "D" for output driver, "B" for communication bit, and "I" for digital input. Thus, the command PI prints the status of the digital inputs while OB 2, 4, 6 turns ON bits 2, 4, and 6.

From the point of view of the processor, these constructs can be treated as if they were two character commands, and the internal command table structured accordingly. It is not a coincidence that the architecture of the M-6800 processor makes it easy to search command tables of two characters or less.

This illustrates the difference between overall language concept and details of language implementation. The drum concept determined the kinds of things which the user would be able to say and the flavor of the responses from the controller. The capabilities of the terminal determined the way in which information would pass between the controller and the user. Finally, the list of commands tells precisely what the user can say.

## Editing drum lines

The most important user activity is specifying a control sequence by entering drum lines. It is forbidden to stop the controller while modifying the control sequence, so the CP allows changes to parts of a drum line without affecting the system until the changes are complete. A drum is selected for change using the select drum (SM) command, and a line is opened for editing by the OP command. Once the line is entered, the Close command places the new line in the drum, replacing the original if there is one. Each of the three parts of a line – the action field, the first exit, and the second exit – can be changed separately.

## Action field

The action field records a list of commands to be done when the line is processed. OB 1, 4 FB, 6 OD 1, 4 FD 3, 6 turns output drivers 1 and 4 and communications bits 1 and 4 ON, and turns bits 3 and 6 and output drivers 3 and 6 OFF.

## Exit field

Exit fields can rotate the drum to another line within that drum based on multiple tests of analog or digital variables. An XL field rotates if all of the conditions are met, and an XY field rotates if any conditions are met. Exit fields test memory bits, digital inputs and output drivers by using the "O" and "F" commands and test analog variables by using algebraic expressions

XL 20 OI 5 OB 3 OD 2 A4 > 72, A5 - A7 < 12

rotates the drum to line 20 if input 5, bit 3 and driver 2 are all on, and if the temperature on analog input 4 is greater than 72 degrees, and if the difference between analogs 5 and 7 is less than 12 degrees.

XY 20 FI 5 FB 3 FD 2

transfers to line 20 if either input 5 or bit 3 or driver 2 are off.

## Timers

Exit specifications can include the length of time a drum has spent on a line. TS is time in seconds, TM is time in minutes, TH is time in hours, TD is time in days.

XY 40 TM = 5

transfers to line 40 after the drum has spent 5 minutes on the line.

## Calendar

The calendar caused major discussion. Although people can identify months of the year by number, it was unrealistic to number the days of the week. Protracted search failed to yield a plausible set of two letter abbreviations for the days of the week. Once the code to search a three character table had been written, names of the months could be provided at an additional cost of only 36 bytes, and users could refer to months and days of the week by name. Since the values which the calendar variables could take had grown to three letters, it was necessary to give the variables three letter names for consistency. Accordingly, OUR is the hour of the day, DOM is the day of the month, WKD is the weekday, and MTH is the month of the year.

XL 40 WKD=FRI, DOM=13

rotates to line 40 on Friday the 13th.

## An example makes it clear

This example illustrates how these language facilities can be used. Control sequences for real buildings tend to run to hundreds of drum lines, and it is necessary to present an artificial example, in this case, an electric hot water heater. The following conditions must be met by the control system.

1. During the interval June through August inclusive, the water termperature is kept between 175 and 180 degrees.

2. During the rest of the year, the water temperature is kept between 195 and 200 degrees.

3. Whenever the water level is too low, the heater is shut off, and a valve opened to restore the water level. A warning light is lighted while the tank is being re-filled.

4. If the water level is not restored within 5 minutes, an alarm sounds.

5. The normal control sequence is resumed after the water level is restored.

6. The alarm and warning light are tested for 10 seconds at noon of the first day of each month.

Inputs and outputs are wired as follows: Analog input 1 is the temperature of the water scaled to degrees. Digital input 1 is ON if water must be added to the tank, OFF otherwise. Digital input 2 is wired to a switch which the repairman turns ON after fixing an emergency condition. This restarts the control sequence.
Output driver 3 is driven ON to put water in the tank, OFF to shut off the valve.
Output driver 4 is driven ON to light the warning light, OFF otherwise.
Output driver 2 is driven ON to sound the alarm.
Output driver 1 is driven ON to activate the water heater.

The program to do this is shown in **Fig 2**. The format has been chosen to make the program logic clear. Drum lines are shown horizontally, and take as many lines as necessary to list each of the different things done in each part of each drum line. The action field comes first, followed by the first exit, and then the second exit. In the example, line 1 of drum 1 takes two lines, because the action field has both an "FB" and an "FD". Line 2 takes only one line, because no field names more than one kind of data.

The CP scans lines from left to right, first performing the action field, then testing the exits one at a time. If the first exit succeeds, the second is not examined.

```
SM 1  1  FB  1   XL  2  MTH>AUG    XL  20  MTH<SEP
         FD  2-4
      2  OD  1   XL  3  A1>198     XL  40  OI 1
      3  FD  1   XL  1  A1<196     XL  40  OI 1
     20          XL 30  MTH>MAY    XL  2   MTH<JUN
     30  OD  1   XL 31  A1>178     XL  40  OI 1
     31  FD  1   XL  1  A1<176     XL  40  OI 1
     40  OD  3,4 XL  1  FI1        XL  50  TM>4
         OB  1          OI2
         FD  1
     50  OD  2   XY  1  FD1
                        OI2
SM 2
      1          XL  2  DAY=12
      2          XL  3  CUR=12
                        FB 1
      3  OD  2,4 XL  4  TS>9
      4  FD  2,4 XL  5
      5          XL  1  DAY=2
```

**Fig 2 Drum lines are listed horizontally the action field comes first, followed by the first exit and the second exit.**

Drum one controls the water heater. Lines 1 and 20 determine the appropriate set of temperature limits. When the heater is turned OFF, lines 2 and 30 return to line 1 to check the month again. If the water level drops too low, input 1 turns ON, and the second tests on line 2, 3, 30 and 31 force drum one to line 40. Line 40 turns the heater OFF, turns the refill valve and the warning light ON, and turns bit 1 ON to indicate that the valve is ON. The first exit of line 40 rotates back to line 1 if the water level is restored. The second exit rotates to line 50 after five minutes. Line 50 turns on the alarm.

The only way out of line 50 is for the plumber to restore the water level or to push the "repair" button. Either event transfers back to line 1.

When line 1 gets control, bit 1 is turned OFF, freeing drum 2. If the low water has not really been corrected, low water is detected, the light turns ON, and the alarm sounds again after another five minute interval.

Drum 2 tests the warning light and alarm. Line 1 transfers control to line 2 at midnight on the first of each month. Line 2 waits for the time to equal noon, and transfers control to line 3. Bit 1 prevents alarm testing from interfering with a real emergency. The bit was used only for illustration, as Drum 2 could test driver 3 instead. Line 3 drives the alarm for more than 9 seconds, and transfers control to line 4, where the alarm is shut off. Line 5 waits until the end of DAY 1, and rotates back to Line 1.

## Debugging aids

No language design can prevent the customer from eventually realizing that telling a computer what to do is programming. It would have been unrealistic to expect a heating engineer to cope with the usual frustrations of program debugging, and it was imperative to provide facilities which would let engineers find and correct bugs without destroying the heating system.

The drum analogy suggested an approach to debugging. Traditional sequence drum systems are shaken down by manual rotation. Critical outputs are disconnected, and sometimes dummy inputs are supplied. In the Sunkeeper, the O and F commands are capable of turning things on and off, but unless the external system is disconnected, it is unwise to do this carelessly. Plugging and unplugging wires is an error prone process, so the language provides the ability to logically disconnect the controller from the system, and test the control sequence in splendid isolation.

The "D" command Disables an I/O line, and the "E" command Enables it again. By first disabling an input, the OI or FI command can set any input to any desired value. The user generates fake inputs for the drums to see what they do. Drivers, Bits, and Analogs can be disabled by DD, DB, or DA commands. The user sets the real output drivers to some benign state, disables the drivers, and runs the sequence to see what the drums would have done if they were permitted to affect the system.

A plumber installing the controller to monitor the electric heater discussed in the example prevents damage to the heating coil by typing

OD 1
DD 1

to turn the driver OFF and then disable it.

DI 1
DA 1

disables the water level input indicator and the temperature on analog input 1 to 100 degrees.

Once the inputs are faked in this manner, the plumber changes the values of the inputs and prints the states of the driver to step through the control sequence. Once the program logic works, reenabling the inputs and outputs lets the controller take over.

As it turned out, the debugging mnemonics were not well thought out. "Disable" and "enable" are computer buzzwords, and plumbers would have preferred terms such as "disconnect" or "unplug". Also, "ON" and "OFF" have no meaning for analog inputs, and it was necessary to define the command "A" for "alter" to change the analog inputs.

**Fig 3** augments **Fig 1** to show the complexity added to the information flow by the debugging facilities. Two sets of values are maintained for each type of data. One set reflects the state of the external system, and one set the values seen by the drums. The Disable and Enable commands determine whether the external values are fed through to the values the drums see. The ON and OFF commands change the values seen by the drums. If a variable is not disabled, the external system controls the value.

## Summary of strengths and weaknesses

The first version of the CP had 8 drums and about 100 lines. As any hardware engineer knows, programmers' appetites are infinite in all directions, and plumbers are no exception. The second version had 40 drums and 300 lines, and that is sometimes not enough.

The M6800 is not very fast, and it spends up to half a second grinding through 40 drums. The system needs external registers and counters for handling rapidly changing data. All applications to date need at least one more input or out-

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**FILL IN THE BUSINESS REPLY CARD FOR PREREGISTRATION DETAILS** **(SEE PAGE 69)**

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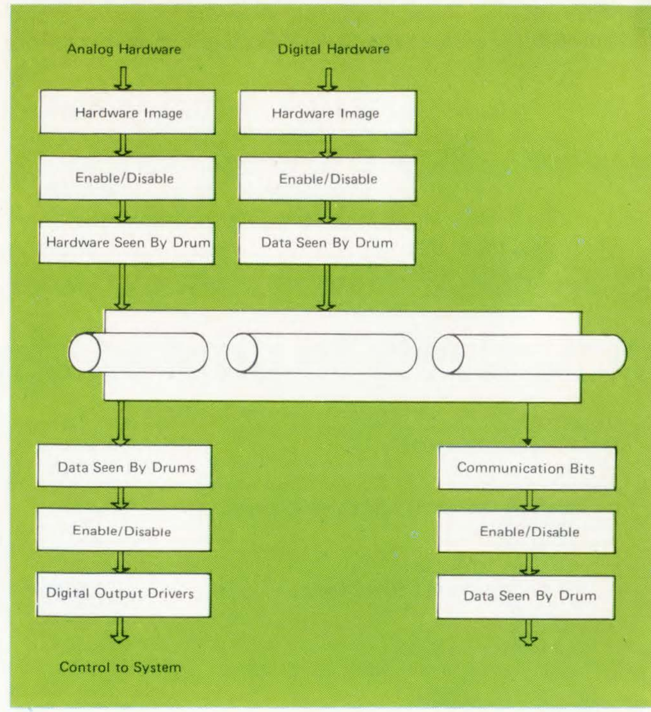


**Fig. 3. Two sets of values are maintained for each type of data. One effects external factors; the others, values seen by the drums.**

put than is available.

In spite of these problems, the Sunkeeper language has had significant commercial success. Although the system was originally designed as a component of a solar energy system which was intended to be the main product, the controller has sold so well by itself that Sunkeeper has renamed itself Andover Controls. Heating contractors, with no knowledge of computers have been known to program a building in two or three days. Some of the reasons the language has been so quickly accepted by non-programmers are:

- **Appropriateness.** The language has just about enough features in it to control a building, and no more. This minimizes learning.
- **Consistency.** I always means "Digital input" whether it is in a PI, DI, EI, OI or FI command. O always means ON, whether in an action field, exit test, or in a command to change a value.
- **Few commands.** Users can get by with O, I, P, D, E, and X, except for commands dealing with editing. Editing commands would have been eliminated with a CRT terminal.
- **Reasonableness.** The language can be compared with an existing artifact, the sequence drum. Although it turned out that few plumbers had ever seen one, drums are sufficiently concrete to be a great help in getting the idea across.

Considerable effect was expended to develop the language, and even more to implement it. However, it would have been much more expensive to write and document individual programs for all the controllers now in the field. The effort of designing and implementing the plumbing language has already paid off in a net reduction in overall programming effort by the manufacturer. It has also opened a previously unsuspected market for microprocessor controller. DD

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# LETTERS

## Here Come the µDisks

Dear Editor:
I was quite interested in the two articles on microdisks in your January issue. It's the first I've seen on this latest development in any electronics magazine.

We investigated the handling of several simultaneous users of floppy disk drives but encountered slow operating speeds. The long rotational delays and head positioning times, and increased cost, don't lend themselves to increasing file storage demands.

With the 16-bit micros coming into use, the demand for suitable mass storage should worsen, and the 14-inch hard disk, despite its storage, is not cost effective. With initial 8-inch microdisks storing 7M bytes unformatted or 5M bytes formatted, the 8-inch microdisk should provide adequate data storage for small business microcomputer systems. Two questions remain. Will it be cost effective? And, if so, what will this mean to the future of floppy disk drives? It could be perilous, or at the least, not as bright as once predicted.

Sincerely
Robert Lurie
Dallas, TX

## The Best of Digital

Dear Editor:
Congratulations on your December issue. The special Review/Preview issue is one of the best, if not the best, of any issue in any electronics magazine. Digital Design has consistently informed me of developments that others only come up with later — or never at all. Keep up the good work.

Christopher G. Warner
IBM
White Plains, NY

## Likes Circuit

Dear Editor:
I read with interest the January Designer's Notebook article (p. 70) entitled "Pulse Time Delay for Digital Lock-Out" by Suinin Wong. This simple lock-out circuit in a system has only one central logic system and several I/O terminals, and this is what we needed in our situation.

I have only two criticisms of Digital Design. First, why was Designers' Notebook omitted for several months last year? I'm sure other engineers find these circuits and software programs useful in their work. Second, I wish you would publish more microcomputer hardware and software applications articles (such as the 8086).

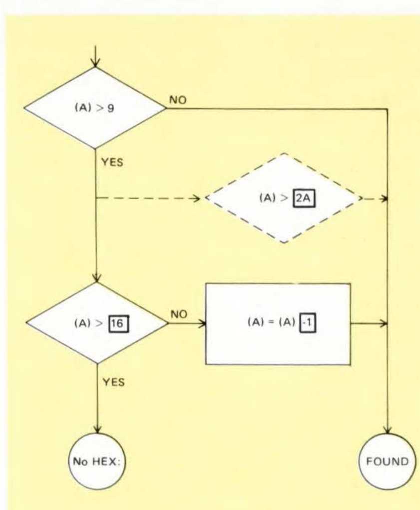
David Weissberger
Mississauga, Ontario

## µP Program Not Minimum

Dear Editor:
The Designers' Notebook article "Hex-to-Binary Converter Runs on 8080/6800 (January 1979, p. 68) contains several errors. Mr. Gupta's program assumes that the ASCII character in the accumulator is alphanumeric since there is no check made for (A) < 30 or 39 < (A) < 41 (all numbers are hexadecimal). With this assumption the program is not minimum as stated since one instruction can be eliminated and one other byte saved by making the following changes as indicated by the three boxed items (16, 2A, −1) and the double flowline from the (A) > 9 decision block.

| LABEL | OPERATION | | OPERAND |
|---|---|---|---|
| | 8080 | 6800 | |
| FIND | SUI | SUBA# | '3ϕ' |
| | CPI | CMPA# | 'ϕA' |
| | JC | BCS | FOUND |
| ALPHA | CPI | CMPA# | 'Y' |
| Comment: Compare (A) with | | '17' | or '20' |
| | JNC | BCC | No HEX |
| | DCR A | DEC A | |
| FOUND | | | |
| No HEX | | | |

*Note: one additional byte is saved by decrementing the accumulator rather than adding an immediate value.*




Walter Martynenko
Senior Programmer
Sperry Univac
Blue Bell, PA

## TECHNOLOGY TRENDS

*Continued from p. 18*
illustrating work on the Teleoperator Project at Jet Propulsion Labratories.

Session 34, The Future of Switching Power Supplies, warns that opportunities for better performance, smaller size and less weight, greater reliability and reduced cost are being challenged by tighter government regulations and society-written safety codes. This session reports on both the great opportunities and the tough design problems.

Session 35 is Latest Advances in PC Board Testing. With new and faster µPs and proliferation of complex circuitry, it's necessary to keep the electronics industry informed of the latest PCB test methods and techniques. This session presents the PCB designer and manufacturer with the greatest number of options from the broadest spectrum of ATE suppliers. It will cover a broad area of methods from static to dynamic testing and various board connection approaches.

### International exhibitors honored

A special focal point of Electro for foreign registrants will be the International Visitors Center at the Coliseum. The Center will include a hospitality suite, interpreter services and free registration all three days of the exhibition and technical convention. A special reception is scheduled on Wednesday to honor international exhibitors, attendees and commercial attaches and counsels from foreign governments. Under the sponsorship of El Tronics International of Rockport, MA, the Center will have available electronics specialists in technical, sales and marketing and purchasing fields to answer questions and provide guidance to foreign companies entering the US market and American firms expanding overseas.

Life Members of the IEEE will participate in a special professional program session at Electro commemmorating the centennial of the invention of the incandescent light by Thomas A. Edison. The session, part of the convention's Professional Program, is scheduled Wednesday, April 25, and will feature talks on the implications of Edison's invention and an evaluation of its effects on modern society. A hospitality suite at the Sheraton Centre Hotel will be maintained for Life Members during the three days of the exhibition and convention.

# VIEWPOINT

Charles C. Herwood,
*President, Signetics Corp.,*
*Sunnyvale, CA*

# Future Shock: The Changing IC Industry

Last month we saw how only a handful of semiconductor manufacturers have made a decent return on investment and asked if there was a need for system companies to make their own volume ICs. To gain insight into these questions, we traced the industry to the present (1975 - 1985) stage – exploiting the elements of success.

In this stage, industry structure is changing. The major companies are getting bigger, but in most of them the IC sector is becoming a smaller portion of total sales. Second tier companies are becoming specialists and are becoming part of (or are forming alliances with) larger organizations. Some Japanese companies (NEC, Hitachi, Fujitsu) and one European company (Philips) have become successful in their home markets and are now ac--tivly contributing to worldwide IC technology. Governments (other than the US) are becoming very interested in developing their own IC industry. Some are Japan, Germany, China, France, United Kingdom, Australia, India, Brazil and Algeria. Some of these governments will ask our US industry to do one or more of the following: a) provide know-how to local firms, b) establish local companies with a total capability from research through production and/or c) take minority positions in companies that have majority local ownership.

The decade 1985 - 1995 will see the start of maturity. The maturing electronics business will be characterized by several things. Extremely complex circuits will be integrated into products for every imaginable use. A very close relationship between systems expertise and IC expertise will emerge, and applications technology will become as dominant as product and process technology. Business relationships between supplier and user will be based more on trust from past experience and mutual knowledge, rather than on the current hot new product.

What will the industry structure look like in 1985? Imagine a pyramid showing the industry structure as it will appear in 1985. At the top will be fewer companies, but having a much larger market share. Later, we will see the market share for each segment. Up to ten multinational companies will be at the top, and will have broad product lines, broad technology, worldwide production centers, worldwide sales, marketing and applications, and the trust of their customers to be super suppliers

Next we will have the volume specialists. They will most likely be application oriented rather than product oriented. In this group will be about 10 to 20 copanies worldwide.

Next, we have small volume specialists or independent custom suppliers that will provide small quantities of high performance functions to critical high performance applications. (For example, for such products as instrumentation, medical equipment and communications.)

These are companies who make integrated circuits with an economic rationale. In other words, they are in business to make money – selling ICs. But volume insurance policy holders and small volume insurance policy holders will make ICs because of a psychological rationale.

What are psychological reasons for making ICs rather than buy them from a freely competitive industry? System manufacturers might not believe their IC suppliers will look after them in the future as to products, or prices, or quality or delivery. These **volume insurance policy holders** feel that priorities of the IC suppliers are not the same as the system manufacturers. They may want to do some manufacturing to know what's going on, believing ICs are very critical to their future. But there are other reasons: Some believe they can manufacture as well as their suppliers, or can't buy the exact design they want, or want to do some manufacturing (and not just be an assembler). Others feel they have some unique ideas that they want to keep secret. Some feel that their IC suppliers are trying to compete with them. And, of course, some feel that the system-IC interface is becoming critical and cannot be adequately covered with a vendor-supplier relationship. The "I can afford it" reason is straightforward. Finally, for countries wishing to establish a local IC industry, you can add only one reason: it is too critical to their electronic systems plans not to have a viable local IC industry.

These will be the volume insurance policy holders – the system companies that will make volume ICs for their own use. They won't sell these outside their own company, but they will buy a substantial portion of their ICs, and some of these companies will make industry standard ICs. Some will make their own designs. Some of the companies already here are Western Electric, IBM, Hewlett-Packard (with SOS) and DELCO. In this group will be companies that receive government support and attempt to supply at worldwide prices.

Then there will be **small volume insurance policy holders** – in-house development labs that make a few production items. This will also include small volume specialists that receive government support to serve the local market only.

Although, I won't speculate on who the players in the game will be in 1985 - 1995 (that's too risky), I will speculate that the next 10 - 15 years will see a great deal of amalgamation and rationalization of present companies. Very few players in the psychological group will be economic successes. But, since they do believe their own psychological reasons, this group will be here.

In 1985 the split should be as follows: multi-nationals, 55%; volume suppliers, 35%; and small volume suppliers 10%. After 1985, the insurance policy holders will decline as they realize two inevitable facts – that their suppliers are specialists in ICs in a highly competitive industry (and, therefore, are good suppliers) and from an economic viewpoint, they will discover that they cannot compete.

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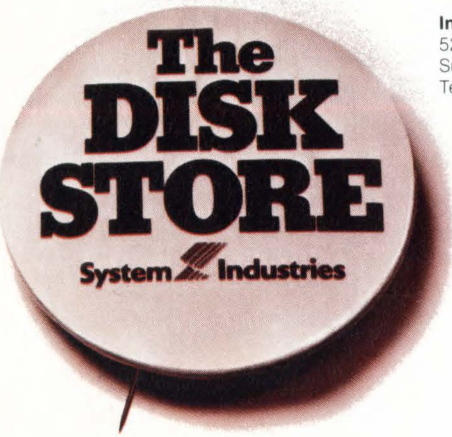


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