VOLUME 9, NO. 3



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**MARCH 1979** 



Circle 1 on Reader Inquiry Card

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# Now Tandberg's TDC 3000 Digital Cartridge Recorder communicates with every computer. <u>Every</u> computer.

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With total communications compatibility, the microprocessor-based RS-232 controller/interface from Tandberg Data is engineered according to EIA Standard RS-232-C, type D and E, and a "teletype-compatible current loop," recording in ANSI/ECMA/ ISO-compatible format.

And from the substantial savings in line charges alone, the TDC 3000 with the RS-232 controller/ interface will recoup its modest cost in a matter of months. It's hard to beat that kind of costeffectiveness.



The Tandberg controller/interface is contained on one p.c. board which mounts inside the Recorder. Power is internal from the TDC 3000 built-in power supply. Two interface connectors are provided so that the Recorder can be connected both to a local I/O terminal (such as the Tandberg TDV 2100 Series CRT terminals) and a modem for remote operation.

Thirteen standard baud rates, 75-9600, are user selectable. Data buffers range from a minimum of 256 bytes up to 1024 bytes. The controller/interface responds to all ASCII command codes. Read and write speed is 30 ips and search speed 90 ips.

And for special communications requirements, the 6800 microprocessor allows the Tandberg controller/interface to be OEM-customer programmed.

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ment. The TDC 3000 is engineered to roll with environmental punches.

You might ask us about some of our more difficult applications. Modular construction of the TDC 3000 enables the user to configure a system to individual needs. Applications include minicomputer input/output, minicomputer peripheral storage, terminal peripheral storage, software distribution, data entry via keyboard, local data collection, data transmission, and text editing. And a few other things yet to be dreamed up.

Besides RS-232, Tandberg Data provides TDC 3000 interfaces for HP 21MX, PDP 11, 8080 Microprocessor, AN/UYK-20 and 8-bit parallel general purpose. All give up to 48K bits transfer rate.

> Tandberg Data Inc. 4060 Morena Blvd. San Diego, California 92117 (714) 270-3990



Gary E. Pyles, Sales Mgr., Tandberg Data inc. 4060 Morena Blvd., San Diego, CA 92117

I'd like to know more about the RS-232 controller/interface for your TDC 3000. Please send me the RS-232 data sheet and have a Tandberg engineer give me a call to discuss my needs.

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So before you choose a display system, let our experts show you how to maximize performance and minimize cost. For details, and/or a quote, call or write.



# THIS MONTH

March 1979 Volume 9, No. 3

#### Features

- 22 Alternatives Abound when Assembling Flexible Disk Systems With more capability in smaller packages, today's floppy disk systems offer higher capacity and lower cost. In this article, an industry expert tells what to look for in buying or assembling a flexible disk system.
- 32 Power Supply Systems for Computer-Based Applications Low power supply reliability lowers computer reliability. If you are designing or specifying a power supply system, here are critical criteria to consider.
- 50 Matrix Printing Optimizing LSI, Mechanics. . .Cost Performance – Cover Feature Although the advent of matrix printing isn't new new developments

Although the advent of matrix printing isn't new, new developments continue to add enhancements and place this technology in the forefront.

58 μP Development Systems Required Tools for Digital Designers

Microprocessor development systems have advanced rapidly, enabling designers to develop their systems faster and move into the production phase more quickly. Here is what to look for in present MDSs - and those of the future.

66 Software Approach to Data Acquisitions

The interface between  $\mu$ Cs and analog converters is similar to purely digital systems. However, the architecture of analog systems and the use to which their data is put requires reconsidering traditional approaches.

#### **Departments**

#### 9 Letters

10 Speakout The Changing Silicon Industry

#### 12 Technology Trends

- 64K-Byte EPROM/ROM Board for iSBC Single-Board μC
- Color Display Growth: the Sky's the Limit
- Will Bubble Memories Replace Floppy Disks in 1982?
- 4K RAM Shortage Will Persist
- Graphic Memory Costs Plunge
- Software Patent Woes Bedevil the μC/mC Industry.

72 Software Design Series Writing a Useful Program

... that others can use, too

- 77 Product Highlight 32-Bit Supermini Offers Performance, Lower Cost
- 78 New Products
- 95 Advertiser's Index
- 96 Viewpoint Future Shock: the Changing IC Industry



#### ON OUR COVER

This matrix printing assembly from Printronix demonstrates the simple, but effective, electro-mechanical components required for printing a wide variety of standard as well as graphic outputs. Our thanks to Printronix for this photo.





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# MFM flopp 1 head or 2

AED's field-proven 6200 Series floppy disk system has recently been expanded to provide the minicomputer user with a wider choice of disk drive capability. The AED6200 Series now offers double density (MFM) systems in four configurations: 2 drives with single head  $(5\frac{1}{4})$ " and 7" cabinets), 4 drives with single head (10)" cabinet), 2 drives with dual head (7" cabinet) and 4 drives with dual head (two 7" cabinets). All systems come complete with formatter, power supply, drive electronics and CPU interface. Interfaces for LSI-11, PDP-8 and 11, Nova/Eclipse, Varian, Interdata and CAI are all available from AED.

Here is a checklist of the AED6200's outstanding user benefits:

- Iow cost, fast access storage
- 1.2 megabytes/diskette
- industry standard 8" media
- programmable formatter for ideal record size
- multiple source drives
- 8 computer interfaces available
- expandable to 4 drives
- CRC and IPL for easier loading
- delivery from stock on all popular models
- Get all the facts by calling or writing our Marketing Manager today.

#### Advanced Electronics Design, Inc.

COMPUTER PERIPHERALS DIVISION 440 Potrero Ave., Sunnyvale, CA 94086 Phone 408-733-3555, Boston 617-275-6400 Fullerton 714-738-6688. Telex 357498.

gives you more for your mini



## \_/IBMable / disk

AED's low-priced 3100 Series floppy disk drive unit is fully compatible with Nova/Eclipse and µNova computers from DGC in addition to IBM3740/3600 diskettes, AED3100 Series drives, which have been field-tested for over four years, use either side of your diskette for double capacity storage providing Read/Write data at less than \$18 per megabyte. Programmable formatter permits ideal record size compatible with OEM's operating system. This economical drive unit can be used as a system device or for auxiliary storage, and will interface with one or two CPU's simultaneously. Available in 4-drive or 2-drive cabinets, the AED3100 is the ideal answer to reliable, low-cost data storage problems for DGC users who require IBM-compatible diskette media.

Check this list of AED3100 user benefits:

- programmable formatter permits ideal record size compatible with your operating system
- used with RDOS, IRIS, BLIS/COBOL, etc.
- provides random access data at \$18/MB
- **DMA** interface
- built-in bootstrap loader
- double-sided disk capability
- available completely packaged or in kit form
- includes diagnostics and documentation
- immediate delivery from stock

#### Advanced Electronics Design, Inc.

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munications 8225 Mercury Ct., San Diego, California 92111 Circle 9 on Reader Inquiry Card

### LETTERS

#### **Looking Forward**

Dear Editor:

I would like to commend your staff for another fine series of survey articles in the December issue.



Being responsible for the selection and implementation of microcomputer systems and software, I found the articles "Microprocessors" by Ian LeMair and Al Moore and " $\mu$ C Software" by Lance Leventhal and William Walsh particularly valuable.

Your track record in this area has been excellent. I am looking forward to the '79 Review/'80 Preview.

Dan D. Gutierrez President ROMTECH Consultants Box 84227 Los Angeles, CA 90073

#### **AIOU Strikes Again**

#### Dear Editor:

In regard to your idealistic editorial (November 1978) asking if we should see more of mail-order degrees from American International Open University, I don't think there's any choice. With several top IEEE officials on the AIOU staff, lending the AIOU semilegitimacy, it's only a question of time before others jump into this moneymaking business.

I just received a booklet titled, "You'll Never Make Any Money Working for a Living," from the International Entrepreneurs's Association. This booklet tells of the most profitable businesses now known. "What kinds of businesses does IEA recommend to its members?" asks the booklet on page 7. "Only those businesses that have a provable track record for making their owners impressive profits with minimal problems."

After listing several of the hottest new businesses and ground floor opportunities, it then states: "Free-Style University – Now anyone can open their own college, and if you study our research reports learn how to make upwards to \$150,000 (in a major metropolitan market) for helping men and women alike – learn how to enjoy life better. Imagine – making a bundle by becoming a self-proclaimed 'educator!' "

IEA is not a whooly-brained, con outfit. The Mayor of Los Angeles and the former Mayor of San Francisco, among others, have spoken favorable of IEA, as has the Wall Street Journal, which said that "IEA investigates moneymaking opportunities for budding young businessmen."

IEA shows you how to start your own open university, such as AIOU, and gives "exact step-by-step details ... exact costs ... how much profit to expect and when ..." and shows "how to avoid all the pitfalls ... advertising and promotion ... how to locate customers for your open university..."

I wonder where the former head of the IEEE and other top IEEE members on AIOU (and others) got their advice and degrees? No, your editorial didn't say. And your asking if we

#### **Array Processors**

Dear Editor:

With regard to the Product Highlight, "Array Processor Opens New Applications," in your January issue, both the FPS Model AP120B and Analogic's AP-400 extensively use synchronously clocked hardware, an architecture form that does not accommodate that well to problems involving concurrent arithmetic and asynchronous I/O.Our MAP-200/-300 array processors utilizes an asynchronous three-bus architecture to handle real-time problems of simultaneous processing input data or arithmetic operations and output data along with inevitable interrupts.

MAP does not rely on host-resident software to execute commands: pro-

should see more of open universities such as AIOU is not "a noble concept." It's naive.

Why doesn't AIOU offer medical degrees for medical students? Or law degrees? Because the AMA and ABA, unlike the IEEE, take a dim view of this and enforce tough legal action to protect their members' best interests.

As for open universitites, a few years ago New York municipalities were forced to pressure certain public school administrators and local officials into resigning after a series of New York Times articles exposed too many of these officials as having degrees from open universitites (the most notorious named by the NY Times was in Ontario, Canada). Many of these officials were given good recommendations, so they could leave with as little ripples as possible, and went to other states.

AIOU members (several who are top officials) don't care about us or they wouldn't put such semi-mail order degrees on the market. When will the working engineer wake up?

Robert Andrade Dayton, OH 45414

#### We Get Letters

Do you agree with us? Disagree? Have an opinion on issues we've raised? Address letters to Letters, Digital Design, 1050 Commonwealth Ave., Boston, MA 02215..All letters must be signed, but we will withold names upon request.

grams are resident in MAP. Peripheral device interfacing, handled directly by MAP, frees the host for higher level tasks. It is this feature that so dramatically lowers host overhead time, as well as acquisition bottle necks, thus making real-time processing easier.

The basic MAP has an internal CPU, 32-bit floating point arithmetic processor, three memory busses, chassis and supply.

As for software, MAP's extensive signal processing library of FORTRAN callable subroutines may be programmed directly in assembly language – not microcode. Finally, MAP is the only array processor with its own internal operating system.

Philip Blake CSP, Inc. Burlington, MA 01803



Satellite data of the San Francisco Bay Area from 23,000 feet Video digitized data through A to D Conversion



After all that's what you see. DeAnza Systems ID 5000 makes the most of what you have. The ID 5000 family of displays provide a versatile low cost, high resolution color or grey scale image with 8 or 12 bits per pixel with 512 by 512 pixels. A high speed Analog to Digital Converter, 26.8 million samples per second is available to digitize high frequency video signals. Optional cursors, trackball, light pen and Joystick are available.

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- sity Transformation Tables
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### The Changing Silicon Industry

Two factors are about to alter the electronics industry — the growing complexity of ICs and skyrocketing semiconductor fabrication costs. So great is the cost of starting a semiconductor fabrication facility, which must offer complete chip families and requires a large market to survive, that only the largest semiconductor companies can manufacture ICs economically. As a result, tomorrow may see only a few giant silicon manufacturers left.

As semiconductor houses shoehorn more electronics into chips, the very nature of the electronics industry is about to undergo a cataclysmic change; and with it, a change in corporate philosophy. Firms using a great deal of electronics in their products or systems must change from a design and production to software and marketing orientation. For example, when TV and stereo makers find all their electonics on one chip (and it will take place), what will happen to these manufacturers? Design and manufacturing will assume less significance. It's already happened in calculators when they became one-chip units. Remember those smaller firms that entered the initially lucrative calculator markets? Few, like MOS Technology, were lucky enough to escape with their hides intact and move into other fields. Despite attempts to set up their own semiconductor fabrication facilities, the Swiss watch industry couldn't successfully compete with the semiconductor giants. The result? Their new niche now is in quality jewelry. There are other fatalities - and more about to come.

What does all this mean? Many companies will find the ball game changed and be forced to move into software, firmware, marketing and into high-technology product areas that lack sufficient volume to attract the semiconductor giants.

Because of the increasing functions/chip and dropping IC costs, the growing semiconductor giants are beginning to pursue end-product business (in fact, they have no choice) and will make it rough on equipment makers and others who purchase ICs. In the long run, can an IC purchaser compete with chip manufacturers? Hardly.

If the logic or decision-making functions of your electromechanical, electronic or mechanical products or systems are extensive, then your firm needs significant reorientation in management philosophy to survive the decade ahead. Make no mistake about it: what exists today is a temporary state about to change. Those equipment and other firms who bought devices from semiconductor manufacturers, and made these IC makers great, may soon find these giants as their new competitors.

Note. Looking for new product ideas and software information? Simply tear out one of the Reader Inquiry Cards, circle those numbers for products on which you would like more information.

Circle 10 on Reader Inquiry Card

### A low-cost DC/DC Converter is something worthy of protection



Etatech has a complete line of single and multiple output units, ranging in input voltage from 12 to 125VDC, output voltage from 5 to 48VDC and output power from 40 to 126 watts. Our exclusive "Univerter"<sup>TM</sup> design lowers parts counts so drastically (71 parts, Model B5D10) that our medium power density "B" and "D" series units are offered at the lowest prices available anywhere. As indicated in the table below, Etatech is your answer for low price and reliable performance in modular and open frame DC/DC converters.

For complete specifications and prices on 71 other modular DC/DC converter models, plus information on Etatech's new open frame line, circle the reader service number and receive our new 28-page catalog. Or, for more immediate action, give us a call. Incidentally, Etatech's variety of AC input units are priced below the competition too.

ETATECH	ETATECH, INC. 187-M W. Orangethorpe Ave.
INC.	Placentia, CA 92670. (714) 996-0981

MODEL NO.	INPUT VOLTS (VDC)	OUTPUT VOLTS (VDC)	OUTPUT CURRENT (ADC)	PACKAGE SIZE	MIN. EFFICIENCY (%)	217B MTBF @ 80° C BASEPLATE	UNIT
OA5D10	28	5	10	4.87 x 7.50 x 2.12	69%	68K Hours	\$149.
B12E5	48	12	5	4.87 x 7.00 x 1.75	75%	68K Hours	\$195.
D5H20	125	5	20	5.00 x 9.00 x 2.25	71%	68K Hours	\$233.

A 5 Year Warranty is standard on all Etatech products.

Circle 11 on Reader Inquiry Card

### TECHNOLOGY TRENDS

### 64K-Byte EPROM/ROM Board for iSBC Single-Board µC

Compatible with Intel's MULTIBUS architecture, Intel's \$495 iSBC 464/ Board is the first EPROM/ROM board that can be used with the high-performance 16-bit iSBC 86 or iSBC 80 singleboard micro computers or with both in a multiprocessor environment.

While compatible with the 16-bit words and 20-bit addressing of the iSBC 86/12 board, the memory board easily accommodates the 8-bit words of Intel's existing line of 8-bit single-board  $\mu$ Cs. The iSBC 464 board is the first iSBC expansion board to use Intel's new high-density 2732 EPROMs. Total memory capacity can be tailored to meet system needs using Intel's 2758, 2716, and 2732 EPROMs or 2316E ROMs. The iSBC 464 board takes advantage of the standby power mode and 5V only features of these Intel components. As a result, power consumption of the iSBC 464 board is reduced by up to 40% and it operates from a single 5V supply.

#### The iSBC 464/iSBC 86/12 Boards

The iSBC 86/12 board, introduced last October, greatly improves single-board  $\mu$ Cs. Two enhancements of the iSBC 86/12 board beyond the capabilities of previous  $\mu$ C systems are an 8086 CPU with a 16-bit data and instruction word size, and ability to address a full megabyte of program and data memory over the MULTIBUS system bus. The iSBC 464 board was designed with these enhancements in mind.

To be fully compatible with the iSBC 86/12 single-board computer, a memory expansion board must be able to place a 16-bit word or just one byte of that word on the MULTIBUS data lines. In addition, the memory board must respond to a 20-bit address code, so that it can be located anywhere within a one megabyte address space. Currently, the iSBC 464 board is the only EPROM/ ROM expansion board with this capability.

#### **MULTIBUS** architecture compatibility

Since the iSBC 464 board is a member of a complete line of MULTIBUS system-bus compatible expansion boards, the iSBC 464 board is fully compatible with the iSBC 86/12 board and with the iSBC 80 family of single board computers. In fact, the iSBC 464 board can easily be designed into a multiprocessor environment that includes both iSBC 80 and iSBC 86 CPU boards. For a detailed article on Intel's MULTIBUS architecture, see the May 1978 issue of Digital Design.

#### **Memory configurations**

The iSBC 464 board contains 16 sockets which provide a maximum of 64K bytes of non-volatile memory expansion. The actual board capacity is determined by the type and quantity of EPROM/ROM components installed by the user.

The available EPROM/ROM devices are the 8K-bit 2758 EPROM, 16K-bit 2716 EPROM/2316E ROM, and the 32K-bit 2732 EPROM – all standard components. Although only one device size may be used, EPROM and ROM can be mixed on the same board.

Since the iSBC 464 board operates with one of 15 switch-selectable memory access times ranging from 35 to 1550 nsec, the board can be tailored to the performance of the installed components.

#### Mode of operation? 8- or 16/8-bit.

The iSBC 464 board operates in one of two modes – the 8-bit-only mode and the 16/8-bit mode. The 8-bit-only mode provides the most efficient memory configuration for systems limited to 8-bit data; the 16/8-bit mode allows 16-bit words to be accessed by 16-bit processors. In this mode, 16-bit and 8-bit  $\mu$ Cs may also access either the high- or the low-order byte of a 16-bit word. Operation mode is selected by placing two option jumper blocks in the appropriate sockets.

#### Memory bank capacity varies

The iSBC 464 board's memory space is organized into four banks, each consisting of 25% the total capacity of the board as determined by components used. Each bank can contain a maximum of 4K, 8K or 16K bytes of ROM. If not all of an iSBC 464 board's memory capacity is to be used, the unused memory sockets can be deselected, thereby freeing those memory addresses to be used elsewhere in the system. Thus, board configurations using fewer than 16 memory components do not fill memory address space with unaddressable blocks.



This block diagram shows the iSBC 464 interface with the MULTIBUS system bus and clearly indicates the 20-bit address and 16-bit data busses.

# Don't settle for a `half printer. A whole Printronix costs no more!

Today, you can choose from several alphanumeric impact printers. Compare ours with the others. You'll find that Printronix impact matrix line printers offer print quality and reliability that no other matrix, drum, chain or belt line printer can match. We think you'll agree: it's the better printer ... it's your best buy!

> But we believe that alphanumeric printing meets only half of the distributed data processing needs of today... and especially tomorrow.

The other half has to do with printing graphics that can compact pages of printed data into simple, easy-to-understand forms. Printronix printers can plot almost anything. Graphs. Charts. Large Characters. Labels. Bar Codes. In fact, they offer a full plotting capability that no other impact drum, chain or belt line printer can provide!

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Both "halfs" that DEFGHIJKLMN make a whole FGHIJKLMND lot of difference!

ABCDEFGHIJK

PRINTRONIX



Circle 12 on Reader Inquiry Card

#### TECHNOLOGY TRENDS

#### Will Bubble Memories Replace Floppy Disks in 1982?

The magnetic domain (bubble) memory storm has threatened to break for over ten years, ever since Bell Labs developed the first bubble memories in 1967. The bubble industry's most rapid growth should occur in 1980 when the total market will increase from \$11 million in 1979 to \$58 million in 1980; and by 1983, sales should hit \$231 million. This forecast by Venture Development Corp. is based on an estimate of the probable price/performance improvement - not on such optimistic estimates as TI's predictions of 92 Kbit chips for \$20 by the end of 1978 (which would provide a 10-1 improvement factor). Although prices were cut in half, nine bubbles/penny is not a terribly exciting price.

#### Lower cost is the key

Can producers make the bubble domain memory a true economic success? They can if they make good on their promises to reduce memory price levels, as nothing else will influence bubble memory market growth like low prices. The Bell Lab creators of the bubble memory believe that it will become the most reliable computer memory ever



This chart, which plots cost/bit as a function of access time for present memory technologies on log-log coordinates, dramatically illustrates cost-performance tradeoffs.





#### Base Price \$1800.00

# Unexpected

When unexpected or out-of-sequence events occur in your system, the Model 532 Intelligent Logic State Analyzer can show you exactly what happened.

But that's not all. As an intelligent analysis tool, the Model 532 contains an unexpected number of powerful features in its compact, 10-pound package:

Broad Monitoring 32 channels with 250 words of storage.

Display Versatility Hexadecimal or binary: use a scope, video terminal, or LED readouts.

Triggering Flexibility 21 different modes. Signature Analysis

Signature Analysis Computes signature of data collected.

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Jim Feit

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#### TECHNOLOGY TRENDS

developed, with error rates orders of magnitude better than competing disk memories. But will most potential users pay high premiums for that extra relia-



Pie graphs show percent of bubble memory systems in terms of units sold and dollar volume by memory size.

bility? Probably not. And, although other bubble virtues (low weight, small size and ruggedness) are important in certain military and mobile applications, price is still the key to large markets. Bubbles have lost some of their glamor: users won't pay more simply to say they own a bubble memory device; the bubble must do something. For all that has been written about bubbles, most engineers still have vague ideas about what a bubble memory really is.

#### Bubbles are "floating" cylinders

A bubble is so called because it seemed to the Bell Lab people, who developed it, to behave "like a bubble floating in a magnetic sea." Actually, bubbles are cylinders of magnetic material that are "floating" in a film of magnetic material. The bubbles are polarized in the opposite direction from the rest of the material. With the proper magnetic bias, which is provided by external permanent magnets, the bubbles are astonishingly stable; they do not dis-

appear or appear unless they are supposed to. Methods have been developed for creating and destroying bubbles and for moving them around. It is important to emphasize that although the bubbles move, the magnetic material does not. There are no moving parts, and no wear and tear. In terms of what they accomplish, bubble memories are closer to disks than to the semiconductors which they resemble. A number of metal paths are laid on top of the bubble chip in loops. Bubbles are switched about the chips like trains on tracks. Each loop can be thought of as corresponding to a track on a disk. With faster access than a disk drive, the bubble memory is not nearly as fast as a semiconductor RAM. If one long loop is used, the bubble memory tends to resemble a magnetic tape drive.

#### Will bubbles KO floppies?

Except for fixed head disks, the bubble memory is not about to knock out any of the established technologies. What about those initial predictions by Texas Instruments and Rockwell? The initial publicity implied that floppy disks would quickly go the way of the buggy whip. They forgot that floppy disks are a replaceable media. Since 35 diskettes were sold for every floppy disk drive in 1978, for one cent of additional diskette cost, 10,000 bits (equivalent to that many bubbles) can be added. By contrast, bubble memory drive and media are virtually the same: bubble memories can be removed and stored. but the cost is that of the whole bubble memory. Much has also been said of the possibility of reducing the cost of the bubble memory system by producing a smaller memory at a correspondingly lower price, because the floppy disk drive has an irreducible minimum cost. However, for a very small memory, a RAM can be used without the need for coils, magnets and special power requirements for bubbles. So, the niche here for bubbles is narrow. Nor is there a significant requirement for a  $\mu$ C "backup" memory.

#### Bubbles will hurt nonremovable diskettes

Although bubbles won't destroy the floppy disk market, they will cut into that portion of the diskette market where the floppy is not used as a removable medium. This portion of the bubble memory market will total \$40 million by 1983, out of a total bubble memory market of \$231 million. Much as moving head disks are now offering a fixed head section, bubbles can be used in a hybrid combination with either floppy disks or hard disks. Although they will constitute only 2% of unit volume in 1983, larger memories of more than a megabyte will make up more than 70% of the dollar volume. Fixed head disks are the natural target for bubble memories of more than a megabyte during the next five years. What is IBM doing in bubble memory development? IBM's development efforts, estimated in excess of \$100 million, indicate that IBM has a long-term target that may be more than just fixed head disks: the bubble storm may displace moving head disks after 1985.

Want more information on the *Bubble Domain Memory Markets?* Contact Edward Ross, Senior Consultant at Venture Development Corp., 1 Washington St., Wellesley, MA 02181.

### **4K RAM Shortage Will Persist**

The feeling among top semiconductor makers is that the shortage of 4K dynamic RAMs we saw in 1978 will persist throughout this year, with supply catching up with the unexpected demand only at the end of 1979. This higher-than-expected demand for lowcost (\$1.50-\$3.00, OEM qty) 4K RAMs has produced lead times of 8-19 weeks, with the worst delivery times for 22-pin RAMs.

Meanwhile, users' preferences continue to break the static RAM market into two very distinct segments. On one hand, high-speed static RAMs (Intel's 75 nsec 2147, etc.) should continue to take over more of the mainfrome market. But, on the other hand, the far bigger market for static RAMs will be in  $\mu$ C-based systems, since there is far greater potential in terms of volume. Despite higher costs and three-or four-fold less complexity over dynamic RAMs (and since dynamic RAMs require refresh control circuits), designers will continue using them when designing small,  $\mu$ C-based memory systems.

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#### **Graphic Memory Costs Plunge**

Graphic memory costs continue to drop. As just one example of this trend, Megatek's 64KB dynamic RAM memory module (for use in the Megraphic 7000 refresh vector graphics terminal) cuts 64KB memory in half – \$6K for the new 64KB dynamic RAM module compared to \$12K for four 16KB static RAM modules. This is the second price decrease since last August, when the price of 16KB static RAM memory modules fell from \$16K to \$12K for 64KB.

Besides substantially reducing the cost of adding memory, the new memory option provides several performance features as well. Because of 64KB of memory is contained in one rather than four modules, power requirements and slots needed to hold memory modules are reduced. Prior to announcing the 64KB option, Megatek referred to its memory as 16K 32-bit word memory, but will now refer to it as 64KB MOS, in line with industry standards. The Megraphic 7000 graphics system provides self-contained refresh memory, 12-bit resolution and a unique 32-bit microcontroller and wordlength. Selective erase, hardware translation, blinking and dashed line are standard provisions with hardware rotate scale, clip and zoom optional.

#### Software Patent Woes Bedevil the µC/mC Industry

Software proprietary problems bedevil both large and small firms. On one hand, some large firms have become embroiled in legal controversy. Fairchild's recent lawsuit against Data General for \$30M in damages and injunction relief against DG's software license agreement is just one example. Emulating the Nova 1200, Fairchild's 16-bit single-chip Microflame (9440) lets Nova 1200 users run programs on the lower-cost and faster devices. Unhappy about this situation, Data General allegedly threatened to cease dealing with customers who bought the 9440 for such uses, and also instituted their own suit. The suits are still pending as of this moment, and the outcome is clouded.

Microflame, fabricated by currentinjection logic, and a bipolar chip housed in a 40-pin DIP, is configured on a board or comes in component form. The system includes computing boards and system software – called FIRE or Fairchild Integrated Realtime Executive – with programs for loading, editing, assembly and debugging. A SPARK 16 board system contains a Microflame CPU, 2K words of FIRE-BUG PROM, 4K words of RAM; while its more powerful cousin, BLAZE 16, contains 16K words or more of RAM.

Are large firms the only ones involved? Hardly. Although many smallfirm users have become embroiled, many cases go undisputed, undetected or unacknowledged.

As if legalities aren't difficult and confusing as is, another problem occurs too often – surreptitious use, with users not above borrowing software. In one recent case we personally know of, two EEs developed  $\mu$ C software on their firm's respective development systems (not to mention some outright pirating of portions) before they left to begin their own firm, with a jump ahead – their software development was finished before they started their firm full time. Another engineer, reimbursed to pirate his firm's software, made regular contributions to the first two and was discovered only by chance by his manager, who notified his boss. Without the slightest accusation being made, this engineer was layed off. It was only a chance conversation with an individual from another firm that aroused the manager's suspicions. How many more such scenarios are never discovered? Or publicized?

#### **Color Display Growth: The Sky's the Limit**

The market for computer graphics devices and systems shipped by US manufacturers will grow at a compound annual rate of 25.9% reaching \$1.8 billion by 1983, according to a market research report on the computer graphics industry just released by Creative Strategies International (CSI) of San Jose, CA. Sparked by the advent of low-cost RAM, color graphics displays will enjoy the spotlight in this dramatically growing industry.

Computer graphics, long considered exclusive to the scientific and engineering design world, will begin to appear in business offices during the next five years, opening up significant new marketplaces for equipment and systems. Graphics will become increasingly important as non-technical personnel struggle to find meaningful ways to display vast quantities of computer information.

Creative Strategies pegs the growth of the raster scan segment (encompassing image processing and raster scan graphic display) at 29% compounded annually, through 1983. Raster scan technology, made economically feasible by the current availability of low-cost memory, will be the primary beneficiary of the push toward color graphics. Lower costs will lead the way for graphic displays beyond the traditional applications in engineering design and scientific research. Emerging areas will include business graphics, medical imaging, process control, mapping and satellite data manipulation.

Color displays should grow rapidly in the next few years, spurred by low-cost RAM and interest in color from business and engineering communities. The prime beneficiary of this increased marketplace? It will be raster scan displays, which can provide excellent color and shading and now offer exciting color capability with increasingly improved resolution.

Hewlett-Packard has just developed a three-color display using a beam pene-tration/electrostatic deflection technology in a 7" random scan display device — an event that may mark the beginning of lower-cost, higher resolution limited color displays.

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### Alternatives Abound when Assembling FLEXIBLE DISK SYSTEMS

Woody Floyd Ex-Cell-O Corp., Remex Div.

In 1976, floppy disk drives were new. At that time, design engineers and purchasing agents questioned mainly the technology. Is IBM compatibility necessary? Double density requires what drive characteristics? Which of the techniques positions the head best?

Today, the flexible disk drive has gone through a shakedown. While many controversies still rage – dualhead design, micro-size versus full-size – the floppy disk drive has evolved from IBM's program loading device into the most popular low-cost memory on the market.

Questions designers now ask also have multiplied. OEMs want to know the most efficient way to design floppy disk drives into a mini or microcomputer system. Should you build or buy the controller? How do you get maximum data capacity without paying a very high price? How can you avoid a heavy software burden on the computer? In other words, design engineers are now asking how to buy a flexible disk system – the subject of this discussion.

#### A system by any other name. . .

The name floppy disk "system" as it is used in the industry today can refer to any of several levels of diskette memories. A complete system includes from one to eight diskette drives, consisting of a formatter/controller including interface, a power supply and cabling, plus driver and diagnostic software. Some systems also incorporate an operating system. Other systems, more correctly called subsystems, offer drives plus formatter without interface or a formatter/controller with interface. These subsystems may be packaged in a chassis with or without power supply, or may be obtained in kit form. The OEM develops all software. The most "bare bones" configuration, still sometimes called a system, packages a drive plus power supply in a box. A separate controller/ formatter is available but not included in the system price.

Regardless of configuration, these contemporary flexible disk systems differ substantially from earlier products of only three or four years ago. The industry treated the original floppy systems much like small, low-cost, hard disk drives. Users who set them to making 16-bit data transfers rather than byte-oriented transfers employed them as mass memories (admittedly of small mass) rather than as I/O devices. The controllers of the diskette systems employed hardwired logic and the host system software controlled most operating tasks. The search for every sector required computer intervention.

But as floppies came of age so, too, did  $\mu$ P and LSI technology which radically changed the characteristics of diskette systems. Many of the systems today contain built-in  $\mu P$  intelligence - 8080, 6800, Z-80 or on the drawing board, 6502 - which allows the system to assume in firmware much of the burden originally assigned to the CPU software. Floppy disk controller chips, such as the popular Western Digital devices, perform some of the drive control function while occupying minimal board space. All in all, today's systems are smart (at least) and small and available in a sufficiently large number of variations to confuse many prospective buyers.

#### Supply and demand

When selecting a floppy disk system, the designer wants to buy as complete a product in terms of controller, interface and software as is available for his application. Even for a large quantity buyer, at the outset at least, it's never cheaper to do it yourself. However, the host CPU largely determines the level of system that the systems designer may require.

By far the largest number of interface-complete flexible disk systems available today are compatible with DEC PDP-11, PDP-8 and LSI-11 computers. If the designer is using one of the less popular CPUs, he may need to design his own interface and, possibly, controller. In this case, subsystems limit his selections.

#### More than one way to be

Just because a designer uses one of the very popular CPUs and, therefore, can choose from a wide range of complete floppy systems, it doesn't make the selection process simple, for he soon finds that there is more than one way to be CPU-compatible. First, some software transparent flexible disk systems run on the host operating system with no alterations - plug them in and away they go. While these plug-compatible systems generally offer the lowest performance of all available types – for example, a DEC PDP-11 compatible system stores 252, 928 bytes of data at a throughput of 10 Kbytes/sec – for the designer with an extensive commitment to the host software, it's the most desirable choice. The computer manufacturer, as well as a number of independents, market these systems. Since by definition these drives must function identically. the buyer should look for price advantages and for such costly features as boot-strapping, an option on some systems and standard on others. While most computer manufacturers offer single source sales and service to the buyer, independents generally sell at a lower price that includes extras, such as front panel switches and indicators. diskette reinitialize function and a more compact chassis.

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dependents can generally deliver faster than the big CPU manufacturers by at least several months.

For the designer who wants more capability than plug-compatible systems offer but still wants media interchange, he can select a so-called "media-compatible" system. Available from a limited number of sources, such a system offers expanded data capacity by allowing an increased number of drives incorporated into the system and by speeding throughput via multiple word transfers and an expanded data buffer. The addition of device handlers to the host disk op-

#### Get the format

Once the designer has selected a floppy system with the correct interface compatibility, he next must consider the format — the way the data is arranged on the diskette. For maximum interchange with other systems, the standard is still IBM. Although the original IBM 3740 format of 26 sectors per track, 128 bytes per sector is the most widely used in systems today, it employs so much overhead in the form of CRC checks, address marks, that the total data capacity is greatly reduced. A single-sided, single-density diskette can store 1.9 Mbits of data.



Fig 1 Schematic of ball leadscrew head positioner shows R/W head, diskette and head load arm configuration.

erating system implements this increased performance. A software transparent diskette system can read media prepared on such a system and viceversa, because they employ the same format and file structure.

The expanded performance system, the last category of more-or-less compatible systems, can work with the computer company's operating system with the addition of the system manufacturer's drivers and handlers. You cannot use media written on such systems in other systems (except those like themselves), because they employ special sectoring techniques (for example, Remex's 16-sector-per-track format) to expand storage capacity by as much as 25%. Contiguous file allocation increases throughput up to 50% over "plain vanilla" systems. To increase this capacity while still retaining the IBM scheme, some buyers choose a floppy system capable of the newer IBM 15 sectors-per-track, 256 bytes-per-sector format used by IBM's series 1 systems. This format stores 2.36 Mbits in single-density recording. However, IBM-compatible format for double density systems is similar to the 3740 single-density format, but offers double data capacity due to the IBM encoding technique.

When IBM interchange is not required, the buyer can find a number of diskette systems that offer selectable soft-sector formats. These systems allow the designer to choose to format data in from one to 32 sectors - in some cases by simply flipping a switch. For a special application, such as military data logging, this capability can be very advantageous.

In soft-sectored formatting, pulses recorded on the altered media apportion the data electronically. The alternative to electronic sectoring, hard sectoring, separates data on a diskette by means of actual holes in the mylar. A few years ago, hard-sectoring provided a number of advantages, the most important of which was that it required considerably less electronics to implement the controller. The advent of floppy disk controller chips, however, virtually eliminated this advantage. Hard-sectoring also offers greater data storage, 30% more than the IBM 3740 format. The new IBM 15-sector format, however, comes within 5% of providing hard-sectored capacity. When you weigh the disadvantages of hard sectoring (non-standard media, no IBM-compatibility, lack of flexibility in formatting) against this small increase, hard sectoring comes up a loser. One major computer company. Data General, is currently using the hard-sectored format. This fact accounts for the limited number of Data General-compatible systems offered by independents.

#### The littlest floppy

Before getting into hardware factors, let's consider the system advantages of the much discussed micro-sized floppy drives. If the designer is building a micro-computer-oriented system, the  $5\frac{1}{4}$ " size and low cost of these units becomes most attractive - with some cautions. While some form of the smaller floppy drives will no doubt appear successfully in future systems, the technology has not completed its shakedown at this point. Since no standards exist for mini-sized floppy recording, each manufacturer feels obliged to do it better than his competitors. This condition makes for a hodgepodge of formats and hardware designs which may offer a buyer some advantages, if he is designing a dedicated system and is willing (and able) to design his own controller, interface and software. However, such a user must prepare himself against the possibility of a new standard being set by the entrance of IBM (or another superstar) into the marketplace. This standard may differ markedly from the one he is employing. At present, a very limited number of 5<sup>1</sup>/<sub>4</sub> "floppy drives are available with controllers and/or in total system configurations – generally with S-100 buscompatibility. Total capacity is 110 Kbytes with a throughput rate of 15.6 Kbytes.

>



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#### Hardware helps

Fortunately for the buyer, the reliability of virtually all traditional singleheaded diskette drives today is excellent. The designer may want to evaluate such features as: IBM-compatible tunnel-erase versus straddle-erase which may create fewer timing problems in erase turn-off, but is not totally compatible with IBM recorded disks; the ballbearing positioner (Fig 1) as opposed to the standard Acme lead screw, the former providing more uniform wear and, therefore, proponents say, more accurate positioning over time; and the design of R/W electronics with regard to noise immunity.

point, since IBM's use of the band on its dual-head drive means that the band is here to stay.

Even IBM's leadership in design has not quelled the controversy over the dual-head floppy disk drive. Without doubt, dual-head technology (wherein two read/write heads mounted on a single carriage record data on both sides of a diskette) is the next step in floppy system design. System builders need larger data capacity in the same (or less) space and, since floppy media cannot yet operate at double the number of tracks per inch, dual-head design is the only logical step. The raging question is, how will it be implemented?



Fig 2 Schematic of band head positioning drive that replaces the slower lead screw position mechanisms.

Some of the newer drive hardware incorporates non-traditional technology which the buyer should evaluate. One mechanical change, available on 5-1/4" and 8" drives, replaces the leadscrew position with a faster band drive positioning system (Fig 2). The band drive provides 3-ms track-to-track access versus 6 to 10 ms for the lead screw, a substantial time saving when totaled over 76 tracks. Critics claim that the metal band positioner is more apt to collect contaminates and, therefore, is more prone to inaccuracy than the lead screw. Proponents solve the problem by covering the band in a protective housing and/or provide band wipers and they retort that the lead screw gets just as gummed up. The argument has become rhetorical at this

IBM's entry into the market in 1977 with a dual-head design seemed to end the guesswork until independent designers, working with the same principle as the IBM unit, discovered the design didn't work. IBM-type drives encountered data reliability problems and caused severe media wear. Designers went back to their drawing boards and have since entered the market with about five major design variations, all IBM-compatible, but not IBM-identical. The major difference appears to be that one type employs two flexure heads a la IBM and the other uses one flexure and one stationary button head. Beyond this distinction in designs, the differences from one drive to another, though subtle, are very important. To describe them

all would require a separate article. Suffice it to say that the buyer should carefully check whether a dual-head drive system successfully passes the "tap-tap" media wear test and meets MTBF and data reliability criteria.

Another major change in flexible disk hardware design involves the extensive use by some manufacturers of FRP (fiberglass reinforced polyester) or other forms of plastic in the drive. Although manufacturers executed their original drive designs for the most part in cast aluminum, they have gradually replaced the metal in major assemblies such as the head carriage with lightweight, economical plastic. The replacement has succeeded and now one manufacturer markets a drive with a completely plastic mainframe. More of these drives will soon become available. To the critics who maintain that plastic cannot provide the reliability of metal, floppy drive designers point out that since FRP and mylar (the diskette material) expand at the same rate, the FRP significantly reduces the possibility of read errors that aluminum mainframe units could experience. In truth, only time and test can settle that argument.

#### Getting it under control

Of course, the controller makes the difference between a dumb piece of hardware and a working diskette system. The designer has three choices. He may choose to buy a controller marketed by an OEM manufacturer, buy a specially designed and built unit from a system house, or build his own. The decision to build, assuming a systems designer with the necessary inhouse expertise, depends largely on the need for a unique non-IBM-compatible format or the enlargement of a format structure beyond the readily available 256- or 512-byte sector size. However, if the designer's format and file requirements are reasonably standard, he can find a variety of controller models to choose from.

One early decision in buying a controller involves physical placement. Most available floppy drive systems mount the controller within the system enclosure. The size and number of cards required determine to some degree the size of the final system package. Subsystem configurations generally offer a naked controller and cables. The system builder decides where to put them. Those few controllers which are available embedded within the drive housing offer a considerable advantage to the designer, because they

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C. Itoh Electronics is part of the 118-year-old C. Itoh & Co. Ltd. world-wide trading organization. Circle 19 on Reader Inquiry Card make an extremely compact package for system integration. These so-called "intelligent" drives (full- and minisized) are available at present only from peripheral manufacturers, because the consolidation of electronics required to create one built-in board can only happen when the drive and controller are designed together.

The designer must also determine how much intelligence he needs in the controller. As previously noted, many controllers today use a microprocessor to perform a large number of functions previously accomplished in the computer software. Because manufacturers can take advantage of quantity cost discounts of the microprocessors used in these controllers, a systems designer can afford to buy intelligent controllers as little more than the cost of LSI/MSI-based boards. Even if the intelligent board can supply more power than his system requires at present, he can anticipate future system expansion and parts compatibility, as well as provide his system with some very elegant capabilities. The newer intelligent controllers offer multi-sector data transfers. This function allows transferring the data on the entire diskette or any part of it with a single command rather than on the sector-by-sector Lasis of older systems. This capability also significantly improves throughput and reduces the I/O load on the host processor.

Another single-command function available on some systems is diskette copying. The command initiates the transfer of all or any part of the contents of a diskette from one drive to another within the system off-line to the computer. Microprocessor-based controllers can also provide the ability to initialize a diskette according to the required format at a single command without use of host software and without operator intervention. The format to be initialized on the diskette is part of the controller command structure. Some systems provide a choice of three formats (26-, 15- or 8-sector) and others can furnish up to six. A simple change in firmware can accommodate customized formats (for example, one sector per track).

No doubt, the most long-awaited controller capability is double-density recording. Although we have previously discussed this topic, its importance bears repeating. Even though double density (employing an encoding technique to double the number of data bits on a diskette) has been around for years, the lack of an industry standard

has made every double density system application - or, at least, manufacturer - specific. To escape the difficulties of double density controller design, engineers made most systems hardsectored. Then, last year IBM came out with a soft-sectored, dual-density (and double-head) diskette drive system - dual density because the identification track is encoded in FM (single density) while the remainder of the diskette is encoded in MFM (double density). Independents have not been too swift to become IBM-compatible, because the circuitry required to implement the code and format costs at least 75% more than a single-density controller. These double-density boards are prohibitively large and complex. For this reason, most OEM manufacturers have been waiting for Western Digital (or any other chip house) to come out with the anticipated IBM-compatible, double-density floppy disk controller chip which will simplify design considerably (one LSI chip versus 25-50 TTL). When they arrive, expect double-density controllers to offer many of the same functions and features of single density.

One unusual system uses two floppies with a controller of unique capabilities as back-up for a 20-Mbyte Winchester disk drive. The communications technique employed between the controller and host adapts the protocol called "channel command" used in large computer systems. This technique permits the transfer of all data and command structures via DMA (direct memory access) to and from the host computer to minimize the communications required between the disk and CPU and to speed data throughput by 40% over standard disk systems.

An engineer can save money in designing multi-floppy drives by employing a master/slave configuration in his system. A full electronics "intelligent" drive can control up to three minimum electronics (and minimum cost) slave drives. More than just assuming controller functions, the master drive also incorporates some of the read/ write circuitry for the slaves. As the slaves do not function as free standing units, single-drive systems use the master only.

#### Interfaceability

The evaluation of a controller should also depend on its interfaceability. If the buyer's system calls for one of the readily available interfaces, such as PDP-11, PDP-8, LSI-11 or the microcomputer oriented S-100 bus, then there's no problem for all he has to do is buy a system with the correct interface, no matter how complex that interface may be. However, if the designer must build his own interface for a less widely used computer, then he should look closely at the configuration of the controller/formatter of a proposed floppy system and consider the ease with which he can interface it to his minicomputer. He may want to make some trade-offs.

High throughput word transfers require more hardware at the interface than systems that transfer bytes. If the buyer expects to design the interface in house, the buyer may want to select one of the byte transfer-oriented subsystems designed for a simple interface with a total of only eight bidirectional data lines plus seven or so status lines. This kind of subsystem allows you to design an interface for virtually any mini or microcomputer with a dozen chips or less. The design involves only the microprocessor parallel interface chip, plus line drivers and receivers.

Some  $\mu$ P-based subsystems allow the command structure to be transferred across data lines rather than requiring separate lines as in earlier designs. This multiplexing technique provides a greater flexibility in speed, as well as a simplified interface. When considering interfaceability of a proposed subsystem, the designer must also determine whether he requires the speed of DMA or he can use programmed I/O (PIO). DMA requires more hardware at the interface than PIO, but frees the processor for other tasks during most of the data transfer operation between the processor and the flexible disk subsystem. Since a DMA interface can "steal" a memory cycle when it is ready for a data transfer, it affects the program running in the processor very little. A PIO interface can interrupt the processor and cause it to jump to a data transfer program for each word that is to be transferred. Depending on the processor, the device and the software handler. this operation can take 10-20 or more memory cycles.

A unique approach to interfacing uses PIO and DMA. Ideally, this combination is set up with software using a channel command approach. The channel command (sometimes called device control block) is assembled in memory. All information necessary for an operation is presented in successive words of memory. This information includes the command, device number,

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status data, disk track and sector data memory locations for data transfer. The processor sends the beginning memory address for this channel command to the interface via PIO. The controller then takes over and transfers the channel command via DMA to the device. All required operations are performed and data transferred via DMA. The controller then signals the processor when it has completed the operation. Provision can also be made for chaining together several commands to result in even less interfacing with processor operation. The intelligent master/slave subsystem can operate in this way with appropriate interfacing.

#### And then there's software

Most buyers of flexible disk systems and subsystems already own OS (operating system) software obtained from the CPU manufacturer -- a DEC RT-11, for example. If the buyer's dedicated application calls for a system capability beyond that of the CPU OS, then he needs a good software designer or he can get hold of one of the "expanded capability" operating systems available on the market. While a description of the specific features of these software packages is too large for this article, the buyer should at least ask these questions: How well is the OS established? Is the software house or he responsible for support and maintenance? How long has it been in the field? Have the bugs been eliminated?

Most buyers are concerned with a second level of software - drivers and diagnostics. Most complete floppy systems provide diagnostics and some provide drivers transparent to the major operating systems. If the buyer must design his own driver, he should look for a system with a minimum number of interface lines and a macrocommand structure, which transmits all of the data required for a complete operation in one command, such as a single read command rather than a string of seek commands and then a read. This structure greatly simplifies driver design.

#### Doubling track density

As you can see, flexible disk system technology is coming of age. More and more capability in smaller packages with less computer intervention is the order of the day. Tomorrow's systems will operate faster due to new positioning devices, command protocols and greater use of DMA. Tomorrow's systems will provide higher capacity with double the number of tracks per inch and perhaps with even further improved encoding systems. Tomorrow's systems will be smaller in size due to more compact mechanicals and greater use of LSI in the controller. And tomorrow's systems will find still newer applications, such as back-up for bubble memory.

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Woody Floyd is Director of New Product Development at the Remex Division of Ex-Cell-O Corporation in Irvine, Ca. With degrees in electrical engineering and business from the Univ. of Colorado and UCLA, Woody holds seven patents in machine tool control, punched tape circuitry and mechanics. Woody is a family man who lists his hobbies as golf and history.

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### **POWER SUPPLY SYSTEMS** For Computer-Based Applications

J. F. McNulty Adtech Power, Inc.

The heart of any computer is its power supply. What many engineers do not realize is that the power supply can drastically affect the reliability of a computer — even if the power supply never fails. Later in this article we will point out why this is so and what can be done about it. In addition to power supply reliability and its effect on the computer's reliability, we must consider a number of other factors in designing or specifying power supply systems for computers. These are as follows.



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#### System and wiring configurations

Circuitry selection. Use low-power consumption circuitry whenever possible. This will substantially reduce power supply cost and greatly reduce heat rise within the unit, the biggest enemy of reliability. Each 10°C reduction of internal temperature will nearly double reliability. Be careful of noise immunity thresholds on some of the low-powered circuits. The use of voltage tolerant circuitry such as CMOS will slightly reduce power supply cost by permitting looser specifications and will frequently prevent marginal problems on lower quality supplies. The use of microprocessor chips that require only one supply voltage or two supply voltages rather than three will greatly reduce power supply cost. Design your system to

minimize the number of different voltage levels required. This will have the greatest effect on supply cost for a given total power, due to the fact that usually the entire regulator circuitry must be duplicated for each output even if overall power goes down.

**Board layouts.** Do not concentrate high heat sources such as drivers near each other. This will reduce reliability. Within practical circuit layout constraints, spread the heat distribution of the circuitry as evenly as possible over the entire area.

Calculate the worst case maximum heat rise of each IC and transistor using  $\Theta$  J-C and maximum voltage and current levels. Since the internal ambient temperature of your system can readily reach 40°C and often as high as 50°C any IC with a junction temperature rise over 20°C is approaching the danger area. If an IC rise calculates over 20°C, PC mounted heat sinks should be employed to reduce temperature rise. Conversly, the power calculation may be done by using the IC's temperature derating curve to ambient, assuming a 50°C ambient rise and a maximum power input. For plastic transistor a maximum rise of 75°C may be used before resorting to heat sinking; however, if the device is handling high peak powers at a 50% or lower duty cycle the rise should be limited to 50% for best reliability. For hermetically sealed metal cased transistors, 100°C junction rises are permissible.

Use ground plane techniques on your PC board layout to minimize lead inductance and maximize by-pass capacitance. Locate power busses directly over ground plane. Make power conductors as wide as possible to reduce IR drops and reduce copper heating. If several strings of IC's or transistors are on one board run separate power runs from the input connector to each string. Do not tie together at other points in the board. Install a separate tantalum bypass capacitor (5 to 200 MFD) near the connector end of each string to avoid noise problems. In some cases, an aluminum electrolytic by passed by a 0.1  $\mu$ F to 0.5  $\mu$ F disc capacitor may be substituted for the tantalum at lower cost. Keep power runs as short as possible. If current levels over 4A will be carried for appreciable distances on the PC board use 2 oz. copper; if over 6A per run use 3 oz. copper. Note: High frequency noise generating curcuits, such as drivers, clocks, oscillators, etc., may require separate bypassing in addition to the main buss bypass. In general for frequencies under 10 KHZ tantalum capacitors should be used. Above 100 KHZ usually ceramic discs will be adequate. In some cases where very fast rise times are involved snubber networks consisting of a 10 to  $100\Omega$  resistor and a 0.1  $\mu$ F to 0.5  $\mu$ F disc capacitor may be required.



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PC boards should be of UL approved material with a 94 VO flame rating to avoid safety agency approval problems. Also voltages above 30V should be kept off the PC board. If for example it is necessary to run AC line



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voltage on a PC board ¼ in. spacing should be allowed to all low voltage conductors and to the opposite side of the line.

Wiring. Wire sizes should be adequate to prevent the wire IR drop from exceeding 0.1V at maximum current since most power supplies have only 0.25V of reserve for wire voltage drop (both lines) and may have less. 50 mV should be allowed for connector drops. Calculate the maximum permissible resistance at maximum current using Ohm's law and divide by the number of feet of wire per run. Find the appropriate resistance per foot in the wire tables (usually given per thousand feet) and use at least one size larger wire to allow for temperature rise. If wire sizes greater than #12 AWG are indicated it may be better to run lighter parallel wires equal to or greater than the required cross section for ease of wiring. For currents in excess of 20A laminated buss bar should be employed (this can be fabricated from two separate copper busses, one positive and one negative, separated by a sheet of insulation).

For multiple board assemblies, the power lines from each board in a card cage should be bussed together and the power supply leads connected to the mid point to minimize differential drop. Individual lines should be run from each card cage to the supply, or in some cases individual lines from each board may be employed. Where there is a wide differential in the current drawn by each board it may be desirable to locate the high current drain board near the outside edge of the cabinet and lay out the other boards in descending order of current with the supply lines tied in at the high current board end.

Power supply lines should be kept as short as possible and twisted pair (or laminated buss) should be employed to minimize noise pick up. Avoid running ac leads in the same cable bundle as dc leads. If wire lengths exceed three ft. and current levels exceed 8A, remote sense lines should be employed, connected to the central distribution point to provide tight load regulation at that point. General layout. The power supply should be located against an outside surface for maximum heat conduction and in a well ventilated area for good convection cooling. The supply should be located so the power transformer is as far away from magnetically sensitive components, such as CRTs and tape heads, as possible. Do not locate heat sensitive boards or

components directly over the power supply nor directly adjacent to it.

Consider heat distribution and cooling in all phases of your layout.

Be sure all ac components such as switches, fuse holders, line cords, fans and motors are UL approved. If your unit is to meet European requirements both sides of the line must be fused and fuse holders must be screw type, not fingertype. They must be rated for twice the fuse current at 230V and clearly labeled. For European use, an electrostatically shielded transformer with safety ground tied to the shield is required.

#### The power supplies

UL. Generally the computer supply will be required to meet UL 478, and if sold outside the US, will frequently be required to meet CSA and VDE or CEE requirements. In the latter case



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it is extremely useful to select a power supply manufacturer that also has a European field service back up as well as to have the intimate knowledge of the European facility in Spain, while Adtech Power has a full manufacturing facility in France. Most other American houses do not have European houses, but may have sales representatives with some repair capability. European safety requirements are generally much more stringent than UL in terms of transformer design, grounding and ac hardware.

Standard or custom? Most computer manufacturers presently specify custom power supplies in the mistaken belief that they are lower in cost than standard supplies. As a result, they consistently run into delivery and logistics problems. Frequently they run into reliability problems due to using products that are not field proven, and in spite of "dual sourcing" either wind up with a single source or, because of splitting quantity, a considerably higher price. If your production

quantity is over 5,000 units/year, a custom will indeed be lower cost and as reliable as a standard if care is taken in specifying the supply and selecting the vendors. If your quantity is under 1,000 units per year, it will usually be beneficial to specify standard off-theshelf power supplies (available in single output, dual output and triple output) even if several supplies must be used. The result of using standard supplies is lower overall cost, higher reliability (the units have been field proven for years in many environments and thoroughly debugged), immediate highly competitive multiple sources, off the shelf delivery, world-wide emergency availability through distributors, and lower safety agency approval cost. The cost will be lower even though you may have to use slightly higher powered units than you might actually need and, of course, the derating further improves the reliability. In quantities from 1,000 to 5,000 each case should be individually examined to determine whether custom or standard supplies would be best. Size. In my twenty years in the business, I have found that the number one problem in computer power systems is inadequate size allowance. The result of forgetting about the power supply until after the computer is designed is generally a left over area of about half the size needed, in an odd shape, frequently in the worst possible location from a heat stand-point. The result is a very costly, odd-shaped power supply, running too hot, with marginal reliability, and heat problems with the computer, or at worst an even more costly and less reliable switching power supply. The power system should be considered at the start of the computer design. Initial power requirements should be multiplied by 1.25 or 1.3 to allow for the system growth that always occurs and sufficient space allocated to allow for standard catalog supplies to meet the anticipated requirements plus one inch should be allowed around each supply for adequate convection. Location. Many systems reliability

2

problems as well as power supply reliability problems can be avoided by carefully considering the location of the power supply system. The power supply will have the highest concentration of heat in your system (even if you use a switching power supply or the new high efficiency linears), be sure in your layout that no heat sensitive boards or components are located over the power supply nor directly
adjacent to it. Be sure there is adequate area around the power supply for good ventilation. Be sure there are air vents below (or near the bottom) of the power supply chassis edges or heatsink and above the supply to allow good convection air flow. Mount the power supplies with their longest surface against an outside cabinet wall to permit good conduction to an outside surface (heat sink compound between the supply and the cabinet surface can further improve heat transfer lowering temperature 5-10°C). Careful attention to these details can lower your internal cabinet temperature by 20 to 30°C improving reliability of both the supply and the system by four to eight times. Of course, forced air cooling (fans) can also be employed to obtain the same result in less space but the noise and reliability of the fan as well as inlet and outlet blockage must be considered.

Efficiency. Linear series regulated supplies, contribute substantially to system heating especially at 5V levels. However they do vary from Lambda's 25% efficiency rating for their LO Series to about 40% (Adtech Power's APS Series is 38% efficient at nominal line, full load). A 50W 5V Lambda supply would add 150W of heat to your cabinet while a 50W Adtech APS unit would only add 82W. A switching supply would be 65 to 70% efficient at 5 V adding only 33W of heat. However the cost of the supply would more than double and reliability would be much lower. There is now a new type of power supply (using several old proven techniques) that combines the best of both worlds that is the high efficiency linear series regulator such as the Adtech EMPS Power Miser series. This type of supply attains a 5V efficiency of 54% at nominal line full load. A 50W EMPS unit would only add 43W of heat to the cabinet but would not have the EMI, reliability, slow response, high ripple and high cost problems of the switcher. This higher efficiency also permits a size reduction of 30 to 40%. If size or heat are problems, consider the EMPS highefficiency linear supply as a solution. This is also an excellent way to upgrade system reliability or to obtain more power without increased system size. Hold up time (or storage time). In many cases, computers require some time to go through a shutdown routine

to save memory on a power outage. Most linear series-regulated power supplies will provide 8 msec of energy storage at nominal line and 2 msec at low line on a power outage. This is adequate for many systems to go through their shutdown routine. It is quite practical to obtain 8 msec at low line with a series regulated supply at some sacrifice in efficiency. A rectifier diode off of a transformer secondary and a simple under voltage detrector chip provide the necessary signal to command the computer to start it's shutdown routine. It is more economical for the computer manufacturer to provide this detection than the power supply manufacturer (due to markups). However power supply manufacturers do provide the feature frequently on customs. If more than 8 msec of hold up time or memory save is required a switching power supply should be used. Switchers will generally provide 20 to 30 msec of storage. For longer times battery back up with a high efficiency linear series regulator is recommended. Specifications. Most computer manufacturers that get in trouble buying outside power supplies do so in one of three ways: (1) choose an unreliable or

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incompetent vendor to get a bargain, (2) do not consider size and cooling adequately, or (3) do not properly specify their requirements. The major discrepancy in most specifications is in the areas of operating temperature and reliability.

The ambient operating temperature specified must be the measured (or calculated) internal ambient temperature in the vicinity of the power supply with the average ambient heat rise caused by the power supply considered. To estimate the heat rise caused by the power supply, assume the following efficiency figures:

Due to variations in air flow, a measured value is preferred. A 50°C internal ambient is not uncommon. If the internal ambient exceeds 55°C steps should be taken to drastically improve the cooling since every 10°C rise in temperature decreases reliability by 2:1.

Reliability is usually specified in Mean Time Between Failure. But usually the manufacturer does not specify by what method or under what conditions it is to be calculated, making the number totally useless. Since reducing temperature 10°C will double the MTBF and since lowering line voltage by 10% will reduce temperature by 20 or 30°C the power supply vendor can obtain nearly any number he wishes if you do not specify the ambient temperature, line voltage and load condition at which he is to perform the calculations. Further there are several military reliability handbooks from which to obtain failure rates. Unscrupulous vendors will use military part failure rates (MIL-HOBK-217A) while using low quality commercial parts. Specify "calculations are to be per component stress method using MIL-HBK-217B 1976 Revision (includes commercial and plastic part rates) using the appropriate commercial parts failure rates." A number of companies normally calculate MTBF at 40°C ambient, full load, high line per MIL-HDBK-217B 1976 Revision.

Vendor selection. Be sure you pick a reputable, reliable vendor for your power supply needs. Be sure the vendor has been in business more than three years and is doing at least 2 million a year to assure a stable source that can back your needs. A reputable vendor will be glad to provide references. Has the vendor had UL approval on at least some of his lines so you know his plant is under U.L. surveillance? Does the vendor have a standard product line to provide well proven circuitry and components at minimum engineering cost? Does the vendor sell through distribution and/or advertise nationally? Are their engineers familiar with your type products and their environments? If you wish to build your own supplies, do you have a full time experienced power supply engineer, components engineer, and mechanical design people familiar with thermal analysis? Do you have procurement experience in power supply components to get high quality at lowest cost? Do you have the test facilities and reliability analysis capabilities to assure a proven product?

Now let us consider the prime requirement, reliability, and its affect on design and specifications.



These AC/DC CM-Series chassis-mount regulated power supplies from Intronics are available in 11 models: single-output 5VDC at 500, 1000 or 2000 mA and Dual-Output  $\pm$ 12 or  $\pm$ 15 VDC at 60, 100, 200 or 300 mA.

Many people feel that reliability means high cost and also that a power supply is a power supply and they are all about the same. I hope to explode both of these myths. Many engineers are not even aware than an improperly selected power supply can double the failure rate of their computer, even though the power supply never fails.

The five major causes of catastrophic failure in computers are: infant mortality failure, heat induced failure, erratic operator due to random line noise, high line failure due to increased surge current and voltage stresses, and failure of electromechanical components.

Infant mortality component failures. Most computer manufacturers have found that a 48-hour burn-in of the completed system will practically eliminate these failures, while buying from reputable manufacturers (including the power supply) will greatly reduce the number of failures (and the high rework costs) during burn-in.

Heat induced failures. While most com-

puters use metal cases for good heat transfer and have adequate venting for good convection cooling, many microcomputers operate in a totally enclosed plastic cabinet with little or no venting. This is done to prevent spillage into the unit and for esthetics. As a result, the heat environment of the unit is considerably worse than that of most main frame computers with heat rises of 20 to 40°C not uncommon. Heat induced failures generally occur as a function of both time and temperature and will usually occur after weeks or even months of operation. This is the major cause of power supply failure in microcomputers.

A prime cause of heat failures among manufacturers who attempt to build their own power supplies (on the mistaken assumption that it is more economical) is the use of three-terminal regulators. The three-terminal regulator is usually used to reduce the engineering time and design cost of the power supply; and many companies think this great invention eliminates the need for a power supply expert on their staff ("After all, any engineer can design a power supply"). Any engineer can design a supersonic transport too - if he knows what he's doing - and if not, I would not book passage on the first flight!

Let us take a look at this little jewel called the three-terminal regulator and see it's impact on reliability. We will consider one of the better ones, a 78H05 5V 5A metal cased TO-3 regulator. First lets look at worst case tolerances:  $\Delta$  V set tolerance is  $\pm 4\%$ ;  $\Delta$  V line,  $\pm 1\%$ ; and  $\Delta$  V load,  $\pm 1\%$ .  $\Delta$  TC (for 35°C case rise AMB rise) is 0.5%, I/O differential is 3.5V and thermal resistance junction to case is 2.0°C/W.

Our  $T^2L$  logic has an input voltage tolerance of ±5%, some circuits require even tighter tolerances. Before we can get the voltage to our ICs, we must consider some additional drops in the system as well. Each connector will drop about 50 mV or 1% at this current and wiring drops in a well-designed system will account for an additional 100 mV to 200 mV or 2 to 4%.

For the 10 to 20% of our three terminal regulators that are at their low set tolerance, we can therefore expect a voltage deviation of -9.5% to

-12.5% at low line full load more than twice the allowable deviation for guaranteed operation of our chips. Surprisingly, many manufacturers will replace logic chips as defective in test when they are actually within manufacturer's tolerances, but will not work



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Easy to read display	Display set deep in hood to reduce glare	Yes	No	No	No	No
	Full 24 x 80 display	Yes	Yes	Yes	Yes	Yes
	Full upper and lower case	Yes	Option	No	Yes	Yes
	Non-glare screen	Option	Yes	No	Yes	Yes
	Tab stops/tab key	Yes	No	No	Yes	Yes
High operator	Backspace key	Yes	No	No	Yes	Yes
High operator throughput, low operator fatigue	Repeat key	Yes	Yes	No	No	Yes
	Shiftlock key	Yes	No	No	No	No
	Separate print key	Yes	No	No	No	Yes
Convenient switching Local/on-line	Local-remote key	Yes	No	Option	Option	Yes
International Character sets	French/German/ Swedish/Danish/ British/Spanish	Option	Option	No	Option	Option
High speed numeric	Integrated numeric pad	Yes	Option	No	Yes	Yes
Convenient system	RS-232/CCITT-V24	Yes	Yes	Yes	Yes	Yes
interfacing	Current loop	Option	Yes	No	Yes	Yes
Simplified program debugging	Transparent mode and displayable control characters	Yes	No	No	No	No
Faster maintenance	Self-test	Yes	No	Yes	No	Yes
Minimum desk space	Small size	15Wx 19Dx 14H	15.5Wx 20.2Dx 13.5H	15.5Wx 20.5Dx 13.5H	15.5Wx 20.5Dx 13.5H	21Wx 23Dx 14.5H
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with their out-of-tolerance power supply. ("But, we did save money on the power supply, didn't we?")

Maybe we can solve this problem. Let's put the three-terminal regulator right on the logic board. This will eliminate the 1% connector drops and cut the wiring drop from 2 to 4% to less than 1%. Now, if we select our three-terminal regulators and eliminate all of the low tolerance ones which will only increase our cost by 20% (and if we're lucky enough to get a typical batch), our tolerance is +4% to -5.3% and most of our units will work even at low line.

Sorry, but we have just created a monster; we have essentially eliminated the erratic operation problem, but we have created another problem that will show up weeks or months from now. Remember that I/O differential of 3.5V? This means that our regulator has a dissipation of 17.5W at low line and 26.9W at high line, and we have just put this heat in the worst possible place right on our logic board. Since the output load on our supply is only 25Ws, we have doubled the heat on our logic board. If this increases the average heat rise by 10°C (a conservative figure), our logic chip failure rate of chips in the close vicinity of the regulator may increase two to four times.

Now that we have determined that the logic or processor board is not the place for the power supply's heat, let's see what other solutions we have. We can use an adjustable four-terminal regulator to eliminate our ±4% tolerance and now we can adjust our supply to offset our wiring drops and hold an overall regulation of  $\pm 2.5\%$ . We can now remove the regulator and it's heat from the logic or games board area; however, the heat is still going to contribute to overall cabinet temperature use. We can considerably reduce this heat contribution and the power supply stresses by using a better quality regulator with a 2.6V I/O differential instead of 3.5V. Of course, this higher quality four-terminal regulator sells for over \$10.00 in 1,000 qty., which is well above the cost of a good quality discreet IC regulator section of a commercial power supply – even after the power supply manufacturers mark up. Of course, the transformer, rectifier/ filter and heatsink are required in both cases, with the three-terminal and fourterminal regulators requiring 30% to 50% more heatsink than the commercial supply (for a given reliability level), due to their lower temperature rating and higher  $\theta$ J-C.

Even if we are willing to pay the higher cost for the four-terminal regulator (about \$2 higher cost) for the dubious privilege of "building inhouse," we are still faced with another reliability problem. Even though the literature on the three- and four-terminal regulators claim "virtually indestructable", "essentially indestructible", etc., based on the fact that these devices have built in current limiting and thermal shut down, we who have used them find that they actually have



Utilizing the VMOS Power FET, Advanced Electronic Design's AED301 reduces switching time to one tenth of that achieved by conventional power supplies, while reducing component count and achieving higher reliability. The new VMOS power supply is also smaller in size and lighter in weight than a bipolar power supply.

a failure rate of about 5% if operated near their ratings - a failure rate considerably higher than that of a good quality, low cost commercial supply and is caused by two major factors in addition to infant mortality. The first factor is second breakdown. Experience shows that when these devices are operated hot, at high line and full load (but well within their ratings) and are abruptly shorted they will frequently fail instead of current limiting. This is due to the high energy (simultaneous high voltage and high current) surge punching a hole in the chip, the lack of consistent control of second breakdown energy levels in these chips is a major drawback. The second major problem is more subtle and causes field failure problems months after installation. There really is a wearout mechanism in all semiconductors and this, of course, is thermal cycling which eventually causes a mechanical fatigue failure of the device or of a lead attachment. These failures can occur after only a few thousand cycles, of load change on-off cycling, or after many hundreds of thousands of cycles depending on the temperature excursion of the cycle and the size, complexity and construction of the device. In the discrete IC commercial power supply, the IC regulator which consists of about 20 elements is located away from the prime heat source and is operated at extremely low-power levels. The power transistor is a large and simple chip operating at high but uniform temperature. Extremely high thermal cycle life is consistently attained with this arrangement. In the three- and four-terminal regulator, the complex IC regulator is in the high temperature package on the substrate with the power transistor with temperature gradients across the chips also due to the higher  $\theta$ J-C (often double that of the discreet power transistor) - and the temperature excursion of the thermal cycle is considerably higher. The result is a much lower thermal cycle life and higher failure rate.

By now it may sound as if I am against three-terminal regulators. Not really; I use thousands of them. But I feel they are unsuited for 5V logic circuits or high power applications. However, they do have their place, and when properly employed, give reliable and economical service. When operating voltage-tolerant circuitry such as MOS circuits, and when operating at voltages above 10V where the I/O differential is a smaller proportion of total power, and when operating at half or less of their rated power to reduce the thermal cycling stresses, they can be quite reliable – if properly cooled. Under these conditions, they can considerably reduce cost over that of discrete regulators at lower power levels, with only a slight reduction in reliability.

We have seen in this example how the power supply can impact the overall system reliability far beyond its own failure rate. We have also seen that the more reliable solution can actually cost considerably less.

There is another problem that the power supply can solve. While it does not result in failures, I would definitely consider it a reliability problem. That is sporadic erratic operation due to high frequency line noise which will pass through any regulator due to their

limited bandpass and the inductance of the electrolytic capacitors. This problem is often resolved by incorporation of a commercial line filter ahead of the power supply at a cost of \$3 to \$20 depending on application. A much simpler and less costly (about \$1) solu-

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tion is to incorporate an electrostatic (Faraday) shield in the power supply transformer and ground this shield to the third wire ground. All our supplies incorporate this electrostatic shield plus a secondary high frequency bypass filtering, thus eliminating the need for the line filter, and again improving reliability while reducing cost.

Now that we have our voltage tolerance, line noise immunity, and heat dissipation under control, we have made all of the major contributions to the computer reliability that the power supply can make without increasing cost. Next, let's look at the power supplies' own reliability.

Field experience of the major manufacturers who build their own supplies indicate that 50% or more of all field failures are due to power supply failure. Therefore, any improvement in power supply reliability will have a drastic effect on overall system reliability.

The efficiency of the power supply that we previously discussed has a major effect on the power supplies reliability with every 10°C reduction in operating temperature doubling the reliability.

Since the a unit that runs more than 30°C hotter than another, it would be eight times more reliable than the hotter unit, all other things being equal. In such a case, published reliability figures of the two units could realistically be 5,000 hours MTBF for the hotter units and 50,000 hours MTBF for the others. I should point out what these MTBF numers mean. In both of the above cases, the figures would be derived from MIL-HDBK-217B using commercial parts failure rates at a 40°C ambient at full load high line. They do not mean all units will go the prescribed hours without failure and have no relationship to life expectancy. What they do mean is that over any given period of time after infant mortality elimination, you will get ten times the number of failures with the 5,000 hours supply as you get with the 50,000 hours MTBF supply. This may make the difference between a 0.5% field failure rate and a 5.0% field failure rate over the first two years.

Efficiency, although a major reliability factor, is by far not the only factor we must consider in power supply design for reliability. In some instances a lower efficiency design can be offset by using more heat-sinking, since it is actually temperature rise rather than actual efficiency that causes our reliability problems. Other major reliability problems are rectifier failure, capacitor failure and transistor failures.

Most OEM power supplies use a minimum amount of heat sinking depending on the excellent thermal conduction and good convection cooling of most electronic equipment for their cooling. A 5V 6A supply that will operate at full power for years in a wellcooled computer, will frequently fail at 5A operation after a few weeks in a plastic-cased microcomputer. The failure most frequently is rectification,



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and pass transistor or filter capacitor failure in the better designed units. To overcome this problem, Adtech Power used 30% more heat sink, a pass transistor with twice the power rating, rectifiers with up to five times higher rating, and a larger ten-year life filter capacitor. Another solution is to use a power supply with at least 50% higher rating than that required, i.e. a 5V 9A power supply for the 6A application. However, this would adversely affect overall system efficiency.

Let us now consider the design criteria for a cost effective reliable power supply.

**Chassis or heatsink.** The chassis or heatsink should be designed to provide at least  $3 \text{ in}^2/W$  of dissipation expected (4-5 in<sup>2</sup>/W for three- or four-terminal regulators). This will provide an average 40°C temperature rise with good convection.

**Protection**. Foldback current limiting should be employed in the design to insure that short circuit current is reduced sufficiently and that the dissipation on the series pass transistor during short circuit is no higher than at normal full load high line operation. Straight current limiting would result in much higher failure rates, since short circuit dissipation would increase two to three times, causing thermal

failure. Fuse protection is totally inadequate to protect transistors against abrupt overloads.

Series pass transistors. The power transistor required must be rated for a voltage of 2 x V in nominal and a current of at least 1.5 x the required current with adequate worst case dc current gain to require less than 25 mA of drive current. The power requirements will be met if the transistor meets these requirements: Tj-c +  $\theta$ jc x P<sub>max</sub>, Tj-c, 60 + 40°C. chassis rise + 20°C. safety margin, and (0.5 x P<sub>max</sub>) + Ths-c.

If this requirement is not met, a higher powered transistor with lower  $\theta$ J-c or parallel transistors must be employed. The transistor parameters must also be checked to assure that all combinations of voltage and current through the overload and short circuit points fall within the safe operating area of the transistor.

In high temperature environments it is generally undesirable to use plastic power resistors at high power levels. If the transistor is mounted to the chassis and the pins are into a PC Board, this places mechanical stress on the lead junction and thermal cycling may eventually fracture the seal, causing failure. On low power levels where there are no mechanical stresses on the transistor there is no objection to plastic devices.

Rectifier failure. One of the most neglected areas of power supply design is the rectifier filter requirements. Even many OEM manufacturers will attempt to use parallel 3A rectifiers in a 6A supply. During the initial turn on of a power supply, the discharged filter capacitor appears as a short circuit and the peak rectifier current is limited only by the source impedance of the transformer. This first half cycle surge will usually be about 10 x the rated dc current, and on heavy supplies, can approach 20 x the dc rating. The surge current rating of a rectifier decreases with temperature in accordance with its power derating curve. 3A diodes with surge current ratings as high as 200A at 25°C (derated to 50A at 125°C. where the rectifier is usually working) are available; however, the lower cost 3A diodes have surge ratings as low as 50 A at 25°C. The most common failure on these supplies is rectifier failure when the supply is repeatedly switched on and off while hot. For this reason, Adtech uses large 30A dual rectifiers with a surge rating of 250A at 100°C. even on their 6A supplies. To avoid this problem, be sure your rectifiers are rated for a 1/2

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The IO 120 offers such features as: 1920 character screen memory, lower case, RS232C extension, switch selectable transmission rates from 75 to 19,200 bps, cursor control, addressable cursor, erase functions and protect mode. Expansion options presently available are: block mode and hard copy capability with printer interface. The IO 120 terminal incorporates a 12-inch, CRT formatted to display 24 lines with 80 characters per line.



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cycle surge of 20 x the dc current at the expected diode max. junction temperature. The Peak Inverse Voltage (PIV) of the rectifiers must be at least 3 x the V in dc value to assure safe operation.

Capacitor failure. Most filter capacitor failures are caused by inadequate consideration of ripple current rating. The current on a well-designed power supply will generally be 1.3 to 1.5 x the dc current. Using an underated capacitor for economy (or due to ignorance) will lead to excess capacitor heating and premature failure. Always be sure your main filter capacitors have a RMS ripple current rating of at least 1.5 x dc current at the lowest frequency of operation and the maximum operating temperature expected. The continuous operating voltage rating of the filter capacitor should be at least 1.5 x (V in nom. x 1.1) to allow for no load peak charging and should not exceed 2 x V in. nom., since a higher rated electrolytic would eventually reform to the operating voltage in any event.

The capacitance of the main filter is determined by the allowable ripple. For worst case ripple of 5% RMS CRL for full wave rectification would be 15, therefore C =  $\omega 15/RC$ , where Capacitance is in farads.

On supplies with current levels below 3A a higher ripple can be tolerated and offset by a higher dc voltage since low dissipation is not as important. In these cases, capacitance as low as 2,000  $\mu$ F/A is permissible, providing the capacitor has adequate ripple current rating.

We have covered the major factors that have prime impacts on the general reliability of power supplies. Of course, all components used should be of good quality and conservatively derated. If we carefully consider the above steps and take care that we have met all worst case conditions and tolerances and have a stable system over the entire temperature and expected load ranges, we will have a very reliable and cost effective power supply. The well designed supply will not cost more than about 10% more than the poorly designed supply - and in many cases will cost less. Yet by careful design, we can obtain reliability improvements of 20 to 40 times, and similar reduction in warranty repair cost and sustaining engineering and quality control cost.

There are other reliability considerations for specific applications that should be considered: Inductive load protection. If the power supply is to operate inductive loads such as solenoids, relays or motors, inductive voltage spikes can raise the dc buss well above its normal level, often momentarily reversing the voltage across the series pass transistor and causing destruction. This can be prevented by connecting a diode in reverse polarity across the pass transistor. The voltage spike is then directly bypassed and absorbed by the main filter capacitor



Triple output supplies from ACDC Electronics provide outputs isolated from each other (to 250 VRMS).

**Reverse Polarity Protection**. If multiple output supplies of opposite polarity are used, there is a definite danger of accidentally shorting the two opposing supply lines together during test and servicing. In many cases certain external circuit failures can tie the busses together. While this is almost guaranteed to cause at least one of the supplies to fail catastrophically, it can readily be prevented from damaging either supply merely by connecting a reverse polarity diode (of adequate capacity to handle the short circuit current of the opposite supply) across each supply.

**Overvoltage protection**. In the early days of transistorized supplies, failures were frequent due to the low quality of components available and the crude circuitry involved. Also the ICs and transistors used in circuits being supplied by the power supply were very expensive. Overvoltage protection was nearly a necessity on 5V supplies since the most common failure was shorting of the series pass transistor, which could more than double the voltage on the output buss, destroying many load IC's.

Today, well designed highly reliable supplies have MTBF of 75,000 to 100,000 hours. Even the dual supplies exceed 50,000 hours. Field failure experience shows much less than 1% failure rates on the well proven standard supplies and under 0.1% in most applications. Also, the cost of the load ICs has dropped considerably. In order to protect the load against even a 1% failure, 100 overvoltage protectors would have to be purchased for each protection. Since the OVP costs from \$5 to \$15 each (depending on supply size), it is seldom economically justified unless we are protecting an extremely expensive circuit.

However, there are some extenuating circumstances. If multiple supplies of the same polarity are used and there is a likelihood of a higher voltage supply being tied to the 5V buss, an OVP may be justified. If a very low cost and crude power supply with a very low MTBF (under 10,000 hours) is used, OVP may be necessary, although it would make more sense to put the cost of the OVP into building a more reliable power supply. If a new unproven power supply design is used, it would be wise to use overvoltage protection on early runs until a field failure history is established. If the repair cost of the board to be protected exceeds \$500 (excluding the service call that would be necessary to replace or repair the failed supply) an OVP would generally be justified.

You may wonder, since I have shown that heat and efficiency are prime factors in reliability, why I have not advocated switching regulators in all cases as a solution to the problem. After all, with their 65-70% efficiency, we would eliminate additional heat from our unit. The reason I have not advocated switchers is mainly one of cost effectiveness. At high powers above 250W, the switching regulator is cost competitive with the linear series regulator is increasing in complexity and/ or stress level and dropping rapidly in reliability. However, at under 100W the switcher is no longer cost effective; and due to the higher circuit complexity and higher component stress levels, it is only one-half to one quarter as reliable as a well designed series regulator in spite of the higher efficiency. For our 30W unit, a well-designed switcher would cost two-to-three times the cost of our linear series regulator and would have two to three times the failure rate – not to mention the problems of high EMI noise generation, slow response time and high ripple. Even our high efficiency EMPS linear series regulator (which is 54% efficient and would reduce our losses by 44%) would not be cost effective at this low level. although it would greatly improve reliability.

3

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After your drum has been completely inspected according to your blueprint to insure its quality, it is packaged carefully and shipped.



## **MATRIX PRINTING** Optimizing LSI, Mechanics ... Cost Performance

Staff Report Printronix, Inc.

**COVER FEATURE** 

The red Queen said to Alice, "It takes all the running you can do to keep in the same place. If you want to get somewhere else, you must run at least twice as fast as that!"

Alice wasn't in Wonderland when the Red Queen said that, she was in the computer industry. Our industry has been a technology race from the beginning, spurred by the rapid developments in the semiconductor industry going from transistors to integrated circuits, to Large Scale Integration and finally to microprocessors.

The more stable segment of the industry has been the electro-mechanical peripherals, but these too, have benefited from semiconductor technology.

The problem in our distributed processing oriented world is that peripherals have not dropped in cost as rapidly as the computer, and so peripherals — particularly the printer, represent a disproportionate cost of the system. This has created a strong need for low cost, reliable, medium speed printers.

In the 1960s the only ROMs were large, magnetic, core memories, some were called "waffle iron memories", some were called "braided wire" memories, but they were all expensive – around  $50\phi$ /bit. Semiconductors solved that problem – ROM's and PROM's are now available for under  $1/2\phi$ /bit. This created the opportunity to build a new type of printer – the matrix printer – and the cost of the electronics for a 64 character set using a 9 x 7 matrix is under \$20.

#### More Than an Expedient

Many people think matrix printing is simply an expedient -a way of making printers at lower cost, but not an

otherwise desireable way to go. There are many reasons why matrix printing is in fact better, an attractive solution to some of the persistent problems of belt and chain printers. The movement of complexity from the mechanics to the electronics is not only a cost saving measure, it is a significant contribution to the inherent reliability of the ma-



Overlapping dots in the 9 x 7 matrix forms clean letters.

chine. Such items include the elimination of the belt or drum. . . a significant cost reduction in itself. There is a substantial difference between the hammers which are used to strike full font characters and those which are needed to simply strike a dot. The energy needed is an order of magnitude less, the mechanical construction is simpler, and the drive circuit much less complex. The limiting factor in the speed of a drum printer is the smear and misregistration caused by drum movement during hammer flight time and impact. Flight time controls are found on most conventional printer hammer drive circuits. But because a moving hammer head of a matrix printer moves at 1/10 the speed of a chain or drum, there is no necessity for flight time adjustments to control misregistration, and there is no problem with smear.

#### Work Smart Not Hard

In order to print one character with a drum printer it is necessary to sequentially present to the print station all the 64 characters from which one is to be selected. The characters may be spaced 0.15 inch apart, making a total movement of about 10 in., to print one character. In a matrix printer, using a single hammer, it is necessary to scan the width of a character, about 80 thousandths of an inch, 7 times to create a character. This is a total movement of a little more than 0.5". If the printers create characters at the same speed, there is an order of magnitude difference between the speed of the two motions, and for this reason smear and misregistration is not a problem in matrix printers. In many cases a 64 character set is quite adequate, but some users require additional symbols, perhaps lower case characters, or Katakana, Japanese characters. For a 128 character font, a drum printer would have to present to the print station 128 characters, taking twice as long, with a large drum. This means a 300 LPM drum printer would have to run closer to 150 LPM with a 128 character set. In the case of the matrix printer increasing the character set increases the size of ROM storage, but has no effect on the speed of the printer. The reason for the higher speed is that the matrix printer prints

# 



Other people make them, of course. But you can't get them in volume. Unless you're willing to wait a very long time. And in this business a printer you can't get is about as useful as all those wonderful products that haven't been invented yet.

Even if you did have a wide variety to choose from, you'd probably choose our Matrix printer anyway. Microprocessor control makes it efficient, fast and reliable. And it's programmable from your computer or optional keyboard.

Bidirectional printing and paper feed gives you true graphics capabilities. Special character sets, including foreign language alphabets, provide incredible flexibility. And when you add the optional keyboard, it becomes a remote communications terminal.

Matrix is compatible with all industry standard RS-232-C or parallel interfaces, so you can plug it in just about anywhere.

If you need a good matrix printer in volume and you can't wait forever, contact one of our local sales offices or the Director of OEM Sales, Microdata Corporation, 17481 Red Hill Avenue, P.O. Box 19501, Irvine, CA 92713. Telephone: 714/540-6730, TWX: 910-595-1764.

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Circle 31 on Reader Inquiry Card



The simple electromechanical design of a matrix line printer eliminates high mechanical dependence on moving drums, chains or print elements.

by Electronic Random Access whereas the drum printer prints by Sequential Mechanical Access. Any number of characters can be stored in a matrix printer without slowing the printer because they are electronically accessed. In the Printronix 300 printer, for example, there is storage for 160 characters. A matrix printer makes about 10 times the number of hammer impacts that a comparable drum or chain printer makes, but with about 1/10 the energy. These higher generated frequencies are much more easily damped, resulting in much quieter operation than drum or chain printers. The designer of a full font printer is always faced with the problem of the hammer energy compromise. The "M" or "W" has an area of about ten times that of a period or a comma, and yet the hammer energy used to strike them is the same. This frequently causes "M"'s to be printed too lightly, and for periods and commas to emboss through the paper. In a matrix printer which prints dots only, the hammer energy is optimized for that purpose alone.

#### Noise Propagation

The propagation of noise through the paper, in both directions, is a severe problem in conventional printers. The ribbon is spaced away from the rotating drum, the paper is spaced from the ribbon. To print, the hammer moves forward, contacts the paper and moves it toward the ribbon and drum until it impacts.

This sudden lateral movement of the paper radiates as noise in both directions and creates a difficult noise suppression problem at the paper entrance and exit. In contrast, in a matrix printer the paper is in tension around a solid platen, and there is no paper movement when the hammer impacts it to make a dot.

The 5 x 7 dot matrix (5 dot positions horizontally x 7 dot positionsvertically) was the first matrix to be used because it uses the minimum number of dots to adequately display a character. However, the characters are not as attractive as a normal type. The logical upgrade was the 7 x 9 matrix which allows greater flexibility in the design of the character because it has almost twice the dot positions. The big disadvantage is that more dots take longer to print, so the printer will be slower.

The ingenious solution to the problem lies in the idea of placing dots on half-dot positions. This allows the choice of two diagonal slopes, and much greater flexibility in the design of character fonts.

The real advantage is that no more dots are used than in the 5 x 7 matrix and the printer runs just as fast. Because a dot can be placed in any of 9 half-dot positions horizontally, the matrix became known as the 9 x 7 dot matrix, although it is only possible to print a total of 5 dots horizontally on one line.

Most matrix printers today use this matrix. We can also optimize the shape and readability of the characters even further.

#### Two matrix mechanisms

There are basically two types of matrix printer, those with a set of hammers arranged vertically and those with a set of hammers arranged horizontally. With a vertically oriented print head there are seven hammers arranged vertically which traverse the paper from left to right making dots as they go. The "A" is completed before the "B" is started and so on. The Centronics printers are good examples of this technique, and are called serial or character printers.

With the horizontally oriented print head the horizontal row of hammers generate one dot row at a time, the



Complete control of the matrix hammer tip allows overlapping of dots even to the point of printing a solid black.

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Circle 34 on Reader Inquiry Card





paper advances one dot separation and the next dot row is printed. With this method, all characters in one line are constructed together, and are finished together. The Printronix and Tally printers are examples of horizontal printing and are correctly called line printers.

Since the paper in horizontal printing can be incremented one dot row at a time, it becomes possible with this type of printer to print lower case characters, such as g, j, p, and y, with the decenders or tails below the character line and printed in the space between lines.

Matrix printing in the last five years has made rapid growth in the computer industry. This is not just because it is an inherently lower cost technology it really has advantages which the belt, band and drum printers cannot offer.



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## **PDEVELOPMENT SYSTEMS** Required tools for Digital Designers

#### Charles Kondrath E-H International

In large mainframe computer systems (prior to mini and microcomputers) debugging through the interactive console was simple. Minicomputers were debugged throughout the software development process by simply tying in a CRT terminal or Teletype station. But microcomputers require a development system to do the same thing.

Software generation and debugging was relatively easy with minis because users had access to working registers (program counters, accumulators, etc) on the front panel. If a simple tape loader bootstrap was needed, the program could be entered via the switch register and stored in memory. The starting address could be loaded in the program counter and executed by placing the computer in the run mode.

By contrast the  $\mu P$  designer needs at least a simple I/O driver, memory modification, loader, etc, resident in PROM or ROM. To execute anything within the monitor, the  $\mu P$  must be reset. During a reset operation, interupt vectors are put on the address bus to access the monitor. Data at these memory locations is loaded into the program counter (PC). Once this occurs, the PC places the monitor program's starting address on the bus, data is inputed (fetched) into the MPU and the instructions are decoded and executed. Fig 1 illustrates the minimum MPU system. Fig 2 shows a reset cycle. Assuming monitor software was written correctly, if any device in the minimum system should be defective or wired incorrectly, the program won't run; and you now have the classical software/hardware problem: is the software or hardware at fault? Trying to find out what module is not

working is very difficult using a scope or logic analyzer. Although MPU manufacturers offer monitor ROMs with software known to be good (which helps solve half of the problem), checking for correct address decoding or wiring errors is still difficult.

A development system simplifies hardware checkout and debugging by allowing you to insert a device (an "incircuit emulator") that looks and acts exactly like the  $\mu P$  it's emulating. Once inserted, your prototype software can be exercised within the development system, debugged and executed.

Another benefit of a development system is the ability to map memory, that is, allowing a division of memory between your prototype and memory inside the development system. For example, if the prototype memory is questionable, you could execute your

4



Figure 2 shows the initialization of the microprocessor after restart. Reset must be held low for at least eight clock periods after  $V_{CC}$  reaches 4.75 volts. If Reset goes high prior to the leading edge of  $\emptyset$  2, on the next  $\emptyset$ 1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

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![](_page_58_Picture_15.jpeg)

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program on system memory and still access your I/O and clock. Memory could then be mapped out in small segments and tested – a process that simplifies integration of software and hardware.

Fig 3 shows a typical development system. Using a development system lets you display the contents of each register plus memory *during* program execution.

Typically, software development is performed simultaneously with hardware design. After both modules are finished, the integration cycle begins (Fig 4). Development systems provide

the next few years, the available manpower, the project's development speed and trouble-shooting capabilities needed to minimize design time. Powerful systems speed project design cycles, although it's hard to justify buy ing a \$20,000 system for one-time use. Until recently, most MDS were themselves  $\mu$ P-based; and the vendor had to painstakingly develop the specialized software for the operating systems. But today, with costs dropping, it is economical to use a powerful mini with cross-software and powerful, readily-available operating systems to do the development.

![](_page_59_Figure_4.jpeg)

Fig 3 Typical development system shows in-circuit emulator cable, CRT, dual floppy drive, printer and other elements.

a text editor and an assembler for program generation. Usually, the assembler offers a linking loader so code can be generated and tested in modules – a feature that also provides for software library creation.

If you're in the market for a  $\mu$ P development system (MDS), you can choose from three types: 1) The lowest cost option is the dedicated system, allowing you to develop software for a single  $\mu$ P, 2), The next level of sophistication is the general purpose system, permitting you to develop software and hardware for multiple processor types (but is still single-user oriented); and 3) the highest level system, permitting multiple users to develop software for many different processors simultaneously.

Which system is best for your application? This decision requires you to decide in advance the number of different processor types you will use over

#### What is a development system?

Regardless of the MDS type you choose, it must meet these criteria: 1) it must help develop software in the language most efficient for your application; 2) it must translate the developed program into source code loadable directly into the prototype system; and 3) it must allow integrating hardware and software, and debug the final code.

What does it take to do this job? You need a powerful central processor with an operating system that can control large bulk memory (hard or floppy disk) and peripherals like CRTs and line printers. You'll also need debug tools like an in-circuit emulator. This sort of ideal system(Fig 5) is the goal most MDS vendors are after.

The MDS software, usually highlevel language, is stored on disks. On the disks you might find program libraries of already-available software routines, such as simple I/O subroutines or other peripheral handlers, and assembly code. Of course, development systems are only as powerful as their software, and there's a variety of software available, which differs between vendor. You can choose from three language levels. Machine code, wellsuited for short and highly efficient routines, is difficult to use; you have almost no indication of what each instruction is unless you memorize almost 100 operation codes! Assembly code uses mnemonic and symbolic form, providing near-readable programs and lets you annotate programs, making debugging simpler. But if the program isn't extremely well annotated, it gets very difficult to follow program flow. High-level languages from Basic to Pascal, and all in-between offshoots, are English-like; and although less efficient in code generation, do permit rapid program development and very simple debugging procedures. The debugging is easy because the programs can be modularized easily and are extremely readable even without comments.

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The trend in most development systems is offering users a choice of high level languages with which he can develop his programs.

Although assembly and high-level languages are generally the best, the real question is which to use when -a choice that is often product-dependent. For example, if the program will be used for just one product and only a few systems will be built, a high-level language is economical, and using an off-the-shelf  $\mu$ C saves hardware debugging time.

However, for a fairly large production run, small savings on each unit add up. To keep the system memory small, use assembly language programs to minimize the number of ROM, PROM or RAM chips. Memory size will be smaller and assembly code will run fasfaster;

Many applications fall between these two, and they can be decided on other factors such as the turnaround time of the project and the actual amount of memory space available. In some cases, high-level languages won't have the necessary extensions (I/O operations, data types and other bitmanipulation type operations) that are commonplace in many microprocessor operations. Some of the newer versions of high-level languages have taken these extensions into account and do provide powerful development routines.

![](_page_60_Figure_0.jpeg)

Fig 4 An ideal development approach should contain the correct hardware software development combination. Microprocessor software programmers must be familiar with hardware.

When a high-level language is desired, the most difficult problem is selecting which to use. For instance, an interpreter might be called for if the user will be making changes to his program, especially if time is not a major factor. Fortran might be the one for a group of numerical routines. Pascal, a good system implementation language, would fit nicely if the application is to perform real-time operations or manipulation of data, especially at the bit level. Structuring a program is easy with the new Fortran 77 standard, and Pascal can help here, too. Both also are useful for program maintenance and ensuring program accura-CV.

To take advantage of the software the ideal system has to contain the right combination of hardware and software (Fig 4). The central processor of such a system acts as an overall controller coordinating the peripheral devices all under control of the operating system kernel. This kernel would contain basic routines for input-output, disk control, file storage and memory allocation.

Depending on the language used to develop the program the rest of the system software might include such programs as assemblers, compilers, editors, debug routines, and libraries. Additional software-controlled features would include debuggers, memory trace capabilities, in-circuit emulators, etc.

The speed at which any of these programs can be executed depends on the processor at the heart of the system. This processor, though, can be independent of the target processor used in the prototype system.

When the processors are different the development software is referred to as "cross software." The system it is being developed on must translate the code into its own language first and finally output the target microprocessor code. Most development systems that use a microprocessor as the CPU are often throughput limited by its 8bit word size. By going to a 16-bit processor minicomputer, all aspects of program development and debugging can be expedited.

If your applications call for just two unrelated chips, you probably could do well by buying two specialized development systems rather than a single general purpose development system. You will, of course, have to jump from one system to the other, and all that bouncing from one editor and system commands can sometimes be more trouble than it's all worth.

Once you've narrowed down your choice of systems, you ought to take a close look at the system's editor. Often it's the weakest link in a development system. One key consideration of the editor is that it allows you to move whole blocks of code.

Besides deciding if you'll need a single chip dedicated system or a general purpose system, you'll have to determine if your applications needs can be met best by a single-user or a multiuser system. The latter is obviously more cost-effective since it allows more than one user to share the highpriced peripherals like printers and disk drives. But be sure the system doesn't become bound to one user.

Don't run in circles on program development. The program development process is not only a multistep one. It is also very iterative. The process can be split into two sections, the more time consuming half of which is software development. But you must also remember that the software must run on the hardware. So you can't forget the hardware.

Once the systems specifications and software/hardware tradeoffs have been finalized the development can begin. One team can put the basic hardware together, while the other starts to develop the software (Fig 4).

Depending on the size of the programs, you can either develop the program in assembly mnemonics or in a high-level language. A fairly good rule of thumb today would break the development at about 1000 lines of code – if the program is expected to be below a 1000 lines use assembly mnemonics, above that use a high-level language. (Of course, if you don't want to work in assembly or have a rapid turn around requirement, high-

![](_page_60_Figure_15.jpeg)

Fig 5 Users today prefer a powerful control processor with an operating system that controls large bulk memory.

level languages can be used regardless of the length of the program.)

Writing programs in assembly code permits rapid and compact development if you've mastered the mnemonics. Typical cycle would be to write the code, assemble it, try running it in a simulated system, and if it doesn't run, debugging it until it does. Once it runs the final code can be loaded into a PROM and plugged into the garget system. Now you're ready to turn on the system and see if it performs. If it works, you're home free; if not, you've got to find the demon. And then iterate.

The debugging process first requires that you determine whether the gremlin is hardware or software related – and you may find it's actually both.

The difference between using assembly and high-level language for program development is just one extra step after the program is written. Since a high-level language was used the program must be translated into the object code compatible with the target microprocessor.

#### What about problems?

When the system you've developed doesn't perform as you planned, you're going to have to think about debugging both the hardware and software. To do this, the development system must be adequate in order to be part of the solution rather than part of the problem.

On the software side, the development system should be able to examine the prototype system's memory and display executed program steps (a history). It should do this in a form that is easy to understand. Since the processor operates the machine code, a disassembler program would help considerably since it can convert the code into assembly mnemonics which are easier to deal with than hexadecimal displays.

To aid the hardware debug procedure, emulators and logic probes are handy additions to any development system. Instruction-by-instruction execution should help to resolve the problem rapidly. The ability of the software to handle breakpoints is another procedure than can speed system debugging.

The in-circuit emulator, when available to the designer, can speed troubleshooting. This device looks and acts exactly like the target microprocessor in the system and once inserted the user's prototype software can be exercised from within the system. This permits simple debugging since the code is now stored in RAM rather than EPROM.

Another feature a development system should have is a memory mapping capability, mentioned earlier. This permits division of the system memory between prototype and the development system memory. If, for example, the user's prototype memory was questionable, the mapping capability permits the program to execute on the development system memory yet have it appear as if the memory was on the prototype. By doing this mapping in small sections, a faulty section of the memory can be isolated.

#### Who makes what?

With over two dozen manufacturers offering development systems the choice of which system to buy is difficult. However, not all manufacturers offer systems to fill every need. Some systems are dedicated to a specific microprocessor or family of processors, and permit only one designer to use it at a given time. Other systems are a little more general purpose but are still limited to a single user at a time. The most general system offered by a very small number of companies, not only permits multiple families of microprocessors to be programmed but also allows multiple users to access the system simultaneously.

Most of the development systems available are offered by the microprocessor manufacturers themselves, with Intel and National Semiconductor offering perhaps the most general purpose systems of the lot. Most of the other manufacturer's systems are limited to only one or two processors each. Systems are offered by non-microprocessor vendors. Among these are systems from FutureData, Control Logic and Tektronix, to name a few. Many of these systems are as powerful, and some cases even more so, than those offered by the microprocessor vendors.

Let's take a comparative look at some of the more powerful microprocessor development systems available today, and then look ahead to the next logical step in the state of the art. The Tektronix 8002, the Intel Intellec Series 2, and the National Semiconductor Starplex, are interesting examples on the current generation. Of the three, the Tektronix is the most universal, offering the ability of develop software for over half a dozen different microprocessor families. It is, however, also the most expensive. The 8002's memory is partitioned — the user memory is separate so that the operating system has its own memory and does not overlap into the user workspace. This system currently supports only Basic as a high-level language, and supports machine code and assembly language programming.

In comparison, the Intel Intellec Series 2 is a bit more limited in that it only allows program development for Intel chips. However, it does offer high-level language capability for almost every processor Intel makes. The system is slightly lower in cost than the Tektronix 8002 and permits in-circuit emulation for every processor, from the single chip microcomputers to the 8086 16-bit product.

The recently introduced Starplex system from National Semiconductor doesn't offer the variety of processors of either the Intel or Tektronix but it does provide an extremely modularized construction and very "friendly" software. This particular system is also available without the software for OEMs willing to write their own.

These systems have taken advantage of all the power microprocessor-based CPUs have to do the job. The next logical step is to go beyond the microprocessor and use a full-blown minicomputer as the central processor/controller in a microprocessor development system.

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That's the course we follow in preparing a new generation system for the marketplace, and a logical course for others. But why a mini? The reason is simple: speed. A 16-bit mini (like the Nova, for example) can assemble 1000 lines of code in under five seconds. On the other hand, a Z-80 might require four or five minutes to do that same job. Not only is execution faster, but, by using a developed minicomputer, very wise database and well documented operating systems are available. Also, with a minicomputer-based system, a hard disk interface is readily available, and this permits extremely large amounts of online library and program storage.

One of the major limitations of all current development systems is the inability to do development on multiple processor types simultaneously. Except for general purpose systems, to change from one  $\mu$ P family to another, the user must invest in a new development aid and learn a new software system. The basic system then should consist of a powerful CPU with multi-station expansion capabilities, general purpose software to permit development in one language and provide translator to each specific  $\mu P$ .

Our new system will provide all these features. As all new generation products should, it will permit in-circuit emulation, include a powerful text editor, a linkage editor, universal Pascal, as well as interfaces for a CRT terminal, floppy disk drives, a hard disk and multiple work stations.

Initially, this will support the 8080, 8085, 8048, Z-80, 6800, 6802, 6502 and soon the 8086 and others. Tying all the hardware together on this new generation system will be our disk operating system, EHDOS.

There will be three progressive option levels, which will permit expansion from a single user system to a multiuser multiprocessor development system.

The simplest level of the new

must be capable of creating files on the disk storage medium, recalling these files, duplicating all files onto another diskette, comparing them, indicating blocks of memory used and available, good and bad. Once a file is stored on disk, the system should be able to recall it, edit it, delete it, expand it, assemble, and load it into user memory.

The system should also be able to assemble source statements in the processor's mnemonics, print error messages, list the label table in alphabetical order of cross-reference the labels, or both, and this should be controlled by user-entered directives. Furthermore, global labels should be provided for the linking loader, the software must contain macro-programming for user convenience.

![](_page_62_Figure_7.jpeg)

Fig 6 Each user has all resources of mainframe system - plus independent device support.

system will be the emulator processor. This system permits the program that has been created and filed in object code to be run, tested, traced and debugged on an emulator processor identical to the target processor on the user system. The next level up provides in-circuit emulator probes that connect the emulator processor into the system prototype, thus allowing the designer to monitor in detail the interaction of hardware with software.

The top level of performance with the system of the future will include multiple work stations as well as stepby-step transfers of executable software into the user's target system. Such a system will be capable of performing all development tasks associated with a microprocessor-based system design. To accomplish this, the system Included in the "ideal" software should be a symbolic debugger, an automatic file backup capability and ability to a file update. This last feature is handy when files are transferred from disk to disk, and because it eliminates the tedious copying of each file individually. All commands in the operating systems should be the same for each  $\mu$ P supported, and the system will have one universal language that can be used for all program development. Pascal is our choice for this purpose.

The debug capability of the system will permit users to set software breakpoints, display the contents of each register, the address and data files, plus disassemble the machine code and display the instruction mnemonics. Another capability it should have is to single-step through a program so that instruction-by-instruction execution can be displayed. Additional capabilities should include a "trace" function to permit the user to examine a defined range of instructions, trace jumps, trace branches and trace I/O instructions. **Fig. 6** outlines this new generation system.

System options should start with basic logic analysis capabilities provided by a real-time prototype module. This function can set very complex breakpoints based on the address, data, logic probe inputs, number of pattern occurrances, real-time delay, and/or machine cycles and status of other breakpoints. Additionally, the analyzer must be able to capture data in real-time and have the option of qualifying which type of machine operations should be captured. The format of the captured data, when displayed, will be - address field, data, mneomincs, logic probe inputs (formatted if selected), bus operation, and breakpoint status.

The major option of the future system, though, should be the ability to add up to eight additional user work stations. This capability can be provided by an eight-channel multiplexer that that can plug into the mainframe. Since the mC-based operating software has a timeshare capability, each work station will have all the power of the main system. All stations will thus be able to edit, assemble, debug, and emulate. The emulator will be a selected module with a target microprocessor installed on it. An option for each of the work stations can include additional memory capacity, up to 65K.

The last option for the system consists of an eight-input logic probe with a clock line and signal ground. Software packages for each target processor wil will be supplied on a diskette that contains the disk operating system, the assembler, editor, debugger and other functions for the target processor.

Future options for such a system include a hard disk system that will have certain files protected so the operating system can never be destroyed.

Another option will be an expansion chassis allowing addition of such features as high-speed line printers, various forms of magnetic tape storage and other peripherals.

#### **Future Debug**

A typical example of using the future system compared with other develop-

![](_page_63_Picture_0.jpeg)

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ment systems might include the advantages of future system shown as follows:

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  - d. Support more than one project simultaneously
  - e. Increased throughput, faster development
- 3. Technical Benefits
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  - b. Ability to set complex breakpoints
  - c. Multi-megabyte data storage
  - d. Supports 16-bit microprocessors
  - e. Multi-user operating system

Development systems, like all products in the fast-moving electronics and data processing worlds, will advance at increasing levels of intensity. That means the systems they develop will move into the production process even faster. Development systems are a more important link in the chain of data processing sophistication than most engineers realize — until they use one and see how small upgrades will make big differences in cost effectiveness through time savings.

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![](_page_64_Picture_22.jpeg)

Charles Kondrath, business unit manager for  $\mu$ C development systems division of E-H International, Inc., Oakland, CA, is responsible for developing, manufacturing and marketing development systems. Prior to joining E-H International, Charles was a  $\mu$ P specialist with Tektronix, Inc. He holds a BSEE from California State Univ., Long Beach.

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## DATA ACQUISITIONS A Software Approach

Robert L. Morrison Burr-Brown Research Corp.

The classical approach to data acquisition isn't the only method: today, with the advent of the low cost voltage-to-frequency converter (VFC), analog data acquisition can be accomplished with the digital conversion performed at each source – a method that relies upon the VFC's ability to linearily translate an input voltage into a defined period of its output pulse train.

In the receiving portion of such a system, the pulse train period must be converted into a corresponding digital word. This is easily performed by either counting the number of output pulses for a given time or actually measuring one or more periods. In a typical system, this function is normally shared among several converters that are multiplexed with a low-cost digital multiplexer in a manner similar to the classical data acquisition approach. An n-stage counter follows the multiplexer, and in the example below, it counts pulses for a given period of time. It is important that this gate time be precisely controlled to preserve system accuracy and should ideally be derived from a crystal oscillator. In this example (Fig 1) a 12-bit counter has been used so that the gate oscillator frequency should be 1/4095 of the maximum VFC output, thus assuring that maximum voltage input will produce maximum counter output.

One of the largest advantages in using a VFC is that data is transmitted in digital form. A digital signal is inherently much more immune to noise than an analog signal and can easily traverse long transmission paths without adverse deterioration. The digital output is particularly convenient when high common made voltages are encountered. Rather than resort to protection schemes required for the classical data acquisition approach, the VFC-based system requires only a single digital isolator for each channel. This is economical, easy to implement and provides full interchannel protection. After the low-level analog input passes through an instrumentation amplifier and VFC, it is isolated by an optically-coupled isolator (OCI). The OCI collector is tied into the counter.

### Interfacing analog Data Acquisition and Distribution to a $\mu$ C

The interface between the digital processor and analog converters is similar to purely digital systems. However, the architecture of analog systems and the use to which their data is put requires reconsidering traditional approaches.

In almost any processor system, a basic decision must be made as to whether the analog converters are to be connected to the S/O bus or treated as memory and mapped into its address field. From a software point of view, it is almost always easier to treat each analog channel as a separate address. Therefore, in a system of any complexity, the normally limited add address field of the I/O bus would be quickly exhausted. This in itself would dictate memory mapped operation; but an even more compelling reason for choosing memory mapping lies in the abundance of memory reference instructions. In most processors these instructions permit much greater versatility in I/O operations than do those controlling the I/O bus. For ex-

![](_page_65_Figure_9.jpeg)

Fig 1 A practical voltage-to-frequency conversion data acquisition system. In a voltage-tofrequency conversion, input voltage is a function of output frequency, so that for higher voltages, output pulse train period is less. ample, a group of analog channels can be treated as a table referenced through an index register or a stack pointer.

Whether memory mapped or I/O bus transfers are selected the manner in which the timing of the analog to digital conversion is handled must be considered. The simplest method requires the program, after starting the process, to continually check the end of conversion signal to determine when the conversion is finished. This is inefficient and wastes valuable processor time, since nothing else is accomplished during this period.

A better method relies upon the processor's interrupt system to report the end of conversion. During the conta transfers while considerably reducing the electrical noise generated by the digital system. An additional benefit can be found in those processors that can be halted in mid-cycle to wait for slow memory. With these processors the entire conversion process is carried out during the course of a single memory read instruction with the timing of the operation totally transparent to the programmer. For all of its merits this method has one serious drawback: the processor is totally blind to any other outside events during the conversion. Where processor response times to external events are required to be shorter than the conversion time this method cannot be used.

![](_page_66_Figure_4.jpeg)

Fig 2 Parallel digital bus interface to the processor bus. ANDing the R/W signals with Valid Address signal presents prevents transmission of invalid data.

version time other segments of the program can be executed until the end of conversion signal pulls the interrupt line. Although this approach may appear efficient, caution should be used when interfacing very fast A/D systems. The overhead time associated with servicing the interrupt may take the processor longer than the time required for the conversion. The net effect would be that the overall throughput would be slower than when looping and waiting for the end of conversion signal.

This problem can be overcome by using a method that is as simple as it is radical. Connect the analog system in such a way that it places the processor in a wait state during the conversion process. This provides the highest throughput speed for programmed da-

When a number of channels are to be converted before the data is processed or a block of channels must be continually scanned, direct memory access should be considered as the interfacing method. Although the most complicated from a hardware point of view, this method maximizes channel throughput with a minimum of software. In one mode of operation, a segment of memory can be continually updated by continuous automatic operation of the analog system and the transfer of digital data performed between processor cycles. Only a slight reduction in software execution speed will be noticed and data can be fetched from memory without regard to the details of operating the analog interface. Another mode of operation might allow several channels to be

processed and then an interrupt generated to signal the software that the block of data is available.

An example of the digital circuitry required to interface to the processor bus can be seen in Fig 2. The Address Decoder's function is to detect when the processor wishes to communicate with the interface. At the time the interface's address is placed on the Address Bus, the Valid Address signal is produced by the decoder. The Timing Decoder determines from the signals on the timing bus whether the operation is a read or write and when it is appropriate to transfer data. The resulting Read and Write signals are "Anded" with the Valid Address signal to produce the proper strobes for transferring data to or from the data bus. The Data Bus Drivers and Data Bus Receivers are necessary to electrically interface with the processors Data Bus.

The processor bus interface circuit can be assembled from several discrete logic circuits. However, today most of the leading microcomputer manufacturers offer a large scale IC to perform this task with their own particular processor. A number of data acquisition and distribution systems that contain all of the digital interface circuitry needed for a specific processor are available.

## Specific analog interface applications

So that a complete picture can be shown of the hardware and software in involved in analog applications, two application examples will be considered.

Thermocouple interfacing. Thermocouples are low-level, nonlinear devices for the conversion of temperature to voltage. For the purpose of this example, the thermocouple will be connected to an Intel SBC80 single board microcomputer via a MP8408 microcomputer data acquisition system.

The system software has two basic parts – those instructions involved with the actual reading of data and those responsible to the data's linearization. The interface within the MP84 MP8408 is of the type that forces the processor to wait during conversion. Therefore, only a single LHLD instruction is required to specify the particular thermocouple channel, start the conversion and read the data when the conversion is complete.

The linearization of the data can be performed in a variety of ways. The basic problem is to straighten the

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AS 15-4	15.00 ±0.2%	4 A	78%	17
AS 28-2.25	28.00 ±0.2%	2.25 A	80%	16
AS 48-1.5	48.00 ±0.2%	1.5 A	80%	18

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2 DS 5-10	28	5.25	10 A	70%	22.5
4 DS 5-10	48	5.25	10 A	72%	20.5
1 DS 12-5	12	12	4.5 A	63%	32
2 DS 12-5	28	12	5 A	73%	22
4 DS 12-5	48	12	5 A	75%	20
1 DS 15	12	15	3.6 A	63%	32
2 DS 15	28	15	4 A	74%	21
4 DS 15	48	15	4 A	76%	19
1 DS 28	12	28	2 A	64%	32
2 DS 28	28	28	2.25 A	76%	20
4 DS 28	48	28	2.25 A	78%	18
1 DS 48	12	48	1.2 A	64%	32
2 DS 48	28	48	1.3 A	78%	17.5
4 DS 48	48	48	1.3 A	80%	15.5

\*Optional voltage features available. See Literature.

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![](_page_69_Figure_0.jpeg)

Fig 3 Thermocouple interface software. Thermocouples are nonlinear and low-level devices. Linearization is accomplished by interpolation between successive points on the voltage-temperature curve.

curve of the thermocouple's actual response into the desired response. This can be accomplished by evaluating a linearizing polynomial or, as an easier to implement approach, interpolating between points on a piecewise linear approximation. It is this latter method that will be used in the flow chart (Fig 3).

### Successive approximation A/D Conversion via software

If a DAC and an analog comparator are available in a processor-based system, it is possible to construct an ADC with the processor providing the successive approximation logic. Fig 4 shows such an implementation using a MP11 dual analog output interface with a Motorola 6800.

The software that provides the successive approximation logic could be written from the accompanying flow chart (Fig 5).

### $\mu$ C-Based Data Acquisition and Control Systems

The microcomputer's application to analog data systems has become so pervasive that highly automated systems are available today that range in size from bench top lab systems to large industrial process control systems. An interesting example of a small analog-centered system designed for lab or industrial testing applications is our CS200 (Fig 6). Housed in a package no larger than a terminal, the system is equipped with both analog and digital input and output for its internal microcomputer. The CS200's micro is programmed in Basic and communicates with the operator via an integral keyboard, display, printer and magnetic tape cassette.

At the other end of the capability range is the IOS 2000 - a system that when fully implemented provides a large number of J10 channels for in-

![](_page_69_Figure_11.jpeg)

Fig 4 In a microcomputer-based successive approximation analog-A/D converter, the processor provides the successive approximation logic.

![](_page_70_Figure_0.jpeg)

![](_page_70_Figure_1.jpeg)

![](_page_70_Figure_2.jpeg)

Fig 6 CS200 block diagram. The CS200's micro is programmed in BASIC and communicates with the operator through an integral keyboard, display, printer and mag tape cassette.

dustrial control. Fully automatic in its operation, the IOS 2000 can accept almost any signal as an input, locally process the data, make control decisions and then, when necessary, communicate with other systems arranged in an heirarchical manner. The packaging and design of the IOS 2000 allow it to be configured for very small to very large applications.

The Micromux is a remote data acquisition system that can be used with any computer system — the CS200 or the IOS2000. Micromux's primary advantage is that its transmitter can acquire up to 16 channels of analog data and then transmit the data back to a

remote point over a single wire pair. Since this is the same cable that provides the transmitter its power, only one wire pair is used where normally sixteen would have been required. Over long distances, the savings in wiring costs can be quite significant. The data is transmitted in a digital form that must be received by a Micromux receiver. Each receiver can handle up to four transmitters and provides the interface to the host computer system. A Micromux receiver is easily connected any computer since its internal microcomputer and associated circuits make it appear to the host as another terminal

![](_page_70_Picture_7.jpeg)

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![](_page_71_Picture_0.jpeg)

## Writing a Useful Program ... That Others Can Use, Too

A standing joke in the software industry is the programmer whose job is guaranteed forever because he (or she) is the only living person who understands or can use a particularly vital program. Obviously, as software becomes a major part of more products and a larger item in their cost, few companies can tolerate such jokes. At the same time, the current shortage of qualified programmers and engineers both reduces the need for this strategy and increases the likelihood that a program will be used by others besides the original writer. The usefulness of a program is, of course, a key factor when the program is itself a product or acts as the operator interface for a product.

The question then arises of how to write a program that others can use. The users may be other members of the product development team, those involved in other projects or later revisions, maintenance personnel, or customers. What makes one program easy to use and another next to impossible? Answers here are important not only to those who must develop software or manage its development, but also to those who purchase software or software-based products or sell those items.

#### The role of documentation

One factor in making a program useful is good documentation. We have discussed documentation practices in a previous article in this series and we will not repeat that material here. Good documentation will provide the user with information about the program in an easily accessible form and at a level of detail that is adequate but not excessive. However, documentation is far from the whole story. Like an instrument, a test system, or a computer, a program that is basically difficult or awkward to use does not improve because it is accompanied by a wellwritten manual. Documentation can reveal the worst. Documentation is no substitute for good design practices or attention to human factors.

#### Two levels of usefulness

Let us look at usefulness at two levels: (1) The module or subroutine level where the question is whether others can use the module in their programs, and (2) the entire program or package level where the question is whether those who must use, maintain or extend the program find their tasks to be simple or difficult. Certainly there is some interdependence here, since a useful program will surely consist of useful modules. But there are also systemlevel considerations that do not enter into the design of a single module. We still start by characterizing a useful module and will then characterize a useful program. We assume here that all programs are adequately documented according to some standard form.

#### A useful module

A module is useful if it has the following features:

- 1) Performs a single function.
- 2) Is reasonably general.
- 3) Accepts input in a simple form.
- 4) Provides clear, useful outputs.5) Has as few incidental or "side"
- effects as possible.

6) Is relocatable and reentrant.7) Acts reasonably in cases where the

data is improperly specified.

8) Does not use non-standard features of a language or configuration.
9) Provides indications of error conditions.

10) Offers a simple linkage to other routines with which it might commonly be used.

11) Performs its operations in a straightforward manner with few jumps.

12) Does tasks one at a time in a logical order.

13) Does not take advantage of leftover results or accidental relationships.

![](_page_71_Picture_24.jpeg)

Fig 1 The Mark Williams Co. XYBASIC Interpreter for 8080-based systems has been specially designed for process control jobs. (Courtesy of Mark Williams Co., Chicago, IL)


# In the Electronic Industry's No.1 Marketplace/New York

Electro takes a penetrating look at the technology, products and ideas that will dominate the industry in the approaching decade of the 80's. It begins Monday, April 23, with an allday marketing seminar and a keynote address by Charles L. Brown, Chairman of the Board of the American Telephone and Telegraph Company.

Then, three days of exhibits and professional program sessions. There will be more than 700 exhibit booths and 120 technical presentations exploring topics like microprocessing, fiber optics, memory, minicomputers, testing, LSI, home computing and others.



Electro / 79 in New York April 24, 25 and 26, 1979 New York Coliseum / Exhibition Americana Hotel / Professional Program

## SOFTWARE DESIGN SERIES

14) Clearly identifies its parameters and constants.

15) Uses the same logic throughout.16) Handles similar data items in the same way and different items in different ways.

The emphasis here is on ease of use. The user should not have to read every line of code, separate logically distinct tasks or figure out clever but obscure methods. The program should do what a reasonable user expects and wants. There are enough surprises around anyway in each stage of product development.

Note that the routines that satisfy these criteria will seldom be the most efficient for a particular application. Typical problems include distinguishing between data and addresses, handling signs and overflow, determining the number of operands and the order in which they appear, and responding to meaningless parameter values. Validity or limit checks on operands are generally neglected outside of business programs.

## A useful program

At the program level there are other considerations beyond those that we have discussed at the module level. Among the new considerations are: 1) Is the program modular, that is, divided into separate and clearly recognizable functions?

2) Is the flow of control as simple as possible, with modules having a single entry and a single exit?



Fig 2 The Cromemco System Three Microcomputer. (Courtesy of Cromemco Inc, Mountain View, CA)

But this inefficiency should be more than balanced by their generality. A later article in this series will describe how to make programs run faster and use less memory when such improvements are necessary and justified.

The question here is "what will the reasonable user expect?" Surely the user will not expect data to be entered upside-down, backwards, or in other unusual forms. Nor will the user expect to find changes in data structures or storage areas that are completely unrelated to the program. Note that you may assume that the user has a certain level of expertise there is no reason for a program to insult the user's intelligence.

Inputs and outputs are particularly important since they are the interface between the module and the outside world. Too frequently, inputs and outputs are either obscured, misspecified or identified incorrectly. 3) Are all data entries clearly specified and can the user easily check to be sure that they were entered and handled properly?

4) Does the program tolerate minor variations in input formats such as spacing and punctuation?

5) Does the program have a limited flow of information so that specific implementations and procedures are only used in a single module? This reduces the number of incidental effects and simplifies changes.
6) Are all outputs clearly identified and related to the corresponding inputs?

7) Are all error messages recognizable and comprehensible?8) Can changes in the input/output device configuration be easily achieved?

9) Are all errors identified without causing system disruption?10) Can new procedures or other

changes be introduced without great difficulty?

11) Does the program degrade gracefully in the event of partial system failure?

12) Are the inputs checked for reasonableness?

13) Is the program written at the proper level of abstraction? If it is a high-level task with complex data structures, it should be written in a high-level language<sup>1</sup>. If it is a low-level task that is machine-dependent, it should be written in a low-level language.

14) Does the program employ widely used starting, ending, and control procedures? The basic control structure should be easy to understand.

15) Is there a way to easily terminate execution when the situation gets completely out of hand?
16) Does the program fit the structure of the data? If not, one or the other should be changed.
17) Does the program suit the application for which it is intended? A program should use the terminology and methods of its application

area.

The last point is a continual problem for professional programmers. Too often, they know how to write the program, but not how to make it really useful. The intended users find the language and methods far different from what is standard in their fields. A package like Mark Williams' XYBASIC (Fig 1), intended for automatic testing and data acquisition, must be very different from a business package intended for the Cromemco System Three of Fig 2. The software in a system like Gnat Computers' FOR-TRAN Workstation (Fig 3) must use the techniques and terminology to which FORTRAN programmers are accustomed. The end user may find a less efficient program written by a specialist in the application area to be far more valuable than an elegant program written by a professional programmer.

Note that even good programming design practices are not the complete answer. The use of down design and structured programming will make programs simpler and more comprehensible, but these techniques do not necessarily result in a satisfactory user interface. Many of the considerations

## SOFTWARE





Fig 3 The Gnat Computers FORTRAN Workstation. (Coursey of GNAT Computers, San Diego, CA)

that we have mentioned require sound engineering judgement and insight into the user's needs and methods. Of course, no program will ever fully satisfy all users or all of our considerations. However, ease of use can be encouraged and specified by programmers, managers and customers. Books (Ref 2,4) and courses (Ref 3) now stress good programming practices that make programs easier to use. Recent increases in the numbers of computers and programmers, the variety of computer applications and use of software will make such practices more essential than ever before.

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# **PRODUCT HIGHLIGHT**

Claimed to Rival DEC's VAX 11/780

## **32-Bit Supermini Offers Performance, Lower Cost**

Low cost and overall system performance — including low operating system overhead, high throughput, large user program space, multiprocessor capability and quality software — make the Perkin-Elmer Model 3220, 32-bit minicomputer effective in military/aerospace, real-time simulation and data acquisition applications. The 3220, also targeted at scientific number crunching applications, is a high-performance processor, along with the powerful Fortran VII and special support software.

Model 3220 offers lower implementation costs through quality, easy-to-use software and systems performance features – transaction processing software, COBOL, file management software, communications support and hardware commercial instruction set.

The first processor in the new Perkin-Elmer Series, Model 3220, is a full 32-bit superminicomputer that is priced like a 16-bit mini with performance in the super-mini class. In Fortran applications, it is claimed to rival the much more expensive VAX 11/780.

With 256KB of high-speed MOS memory, the 3220 has a single unit price of \$33.5K; with an Mbyte of memory, \$59K.

First systems are available with a

maximum of one Mbyte of memory. Model 3220 is optionally field expandable, later this year, to 4 Mbytes.

Suited for any application that demands 32-bit mini performance and reliable software, the 3220 offers high-performance features. It provides all the traditional features of the prior Perkin-Elmer 32-bit Series while including new instructions and facilities for optimum performance in both development and real-time applications. Some 3220 features are: full 32-bit architecture, 8MB direct memory access bandwidth, four external priority interrupt levels supporting 1023 devices, eight sets of 16 32-bit general purpose registers and memory expansion to 4MB of high speed MOS memory. The 3220 uses an optional 1KB of bipolar cache memory to significantly improve memory access time.

The impact of P-E's RAS (reliability, availability and serviceability) program are visible in the Model 3220. The OS/32 MT software contains fault tolerant/error logging features. the 3220 CPU has a comprehensive memory system along with self test and fault reporting capabilities, and the MOS memory system has error correction and logging capabilities.



The Model 3220, a full 32-bit super-minicomputer, is the lowest-cost hardware available to execute some of the industry's best software; and in FORTRAN applications, it is said to rival the VAX 11/780.

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## SOFTWARE ON E & S DISPLAY

Structural Dynamics Research Corporation has announced that its SDRC modal analysis testing software is fully compatible with the Evans & Sutherland Picture System, an advanced, high quality graphics display. The display is flicker-free and offers the user interactive control. Dial control, for ex-



ample, permits rotations of a model in three-dimensional space or zooming into any section. Lines in foreground are bright, background lines are dim, making models easier to see. Cutting planes can also remove any part of the model to further aid visualization of complex three-dimensional structures. The picture system and SDRC software are compatible with existing modal analysis systems supplied by SDRC, Gen-Rad, Spectral Dynamics and Zonic Technical Labs. SDRC, 2000 Eastman Drive, Milford, OH 45150. Circle 211

## **4 MHz BOARDS**

Zilog, Inc., has introduced four MC boards designed to operate at 4 MHz. The new family of boards includes the Z-80A MC board (Z-80A MPB), the RAM/ROM memory board (Z-80A RRM), the floppy disk controller board (Z-80A FDC), and the I/O board (Z-80A IOB). The principal board is the Z-80A MP-based MPB. It contains four Zilog I/O peripheral components configured to support a line printer interface, direct memory access control, and two independent full-duplex serial communication channels implemented with the Z-80A SIO (Serial I/O) and buffered for RS422 or RS423 interface. \$695 (1-9). The Z80A RAM/ROM memory board is available with either 16K or 64K bytes of dynamic RAM memory. It cincludes sockets for up to 8K bytes of non-volatile PROM or EPROM. (16K-byte version) \$850, or (64K-byte version \$2050 (1-9). The Z-80A FDC is a versatile single-board disk controller permitting direct control of up to eight single-density floppy or mini floppy disk drives; doublesided drives are also supported. Although this board is designed to interface to Shugart 400, 450, 800 and 850 series floppy disk drives, its control and data

port bits are I/O programmable to meet the user's needs. Functionally compatible with the Z-80 MDC, the Z-80A \$495 (1-9). The Z-80A IOB, designed to provide the 4 MHz boards with programmable I/O port capability, has four uncommitted Z-80 PIO (Parallel I/O) circuits to support 64 bi-directional I/O lines. Unused space on the board contains plated holes for insertion of wire wrap devices. **ZILOG**, 10340 Bubb Road, Cupertino, CA 95014. **Circle 199** 

## COMPUTER GRAPHIC TERMINAL

Using the power of beam addressed solidstate image memory, the 8500M graphics terminal contains over four million microcapacitor elements providing high resolution performance. The terminal offers smooth, continuous, graphics without stairstepping. It uses a 4K x 3K viewable window and has an addressable field of 8K x 8K points. Other features include: 16X panoramic zoom and preview window for selective magnification; µP minimization of burden on host computer; stroke written alphanumerics, symbols, conics and vectors; expandable RAM for user designed characters and symbols; and selective erase of graphics and alphanumerics. Options range from floppy disk, MT cassette, digitizer, APL keyboard, additional image memories, high speed gray scale interfacing, additional character RAM, etc. Princeton Electronic Products, P.O. Box 101, North Brunswick, NJ 08902. Circle 204

## S-100 I/O BOARD

The SWITCHBOARD, an I/O board for S-100 systems, has four parallel ports and two RS232/TTY serial ports plus strobe and attention ports. In addition, there are options for 4K of RAM and 4K of EROM.



Each parallel port can be switched for input or latched output. Both serial ports can be switched to any of sixteen baud rates from 110 to 19K. Each strobe and attention port flip-flop can be switched for positive or negative pulsing. The eight I/O addresses of the SWITCH-BOARD can be located on any boundary divisible by eight. \$199.00 kit; \$259.00 assembled. Thinker Toys, 1201 10th St., Berkeley, CA 94710 Circle 195

## **ERASES 96 EPROMS IN 7 MINUTES**

Offering fast complete ultraviolet erasure of up to 96 EPROMS in one batch in under 7 minutes, the C-91 Memorase uses over 7-feet of pure quartz tubing to give maximum output at 254nm without destructive hot spots. The C-91 occupies less than 14 sq. in. of counter space and can be stacked for multiple runs. Housed in heavy duty aluminum plate, the unit is finished in baked enamel. The unit also features a one-hour exposure time, cumulative 2-hour recorder, and viewing ports.



Safety features include a unique interlock device for accident-free operation and ozone-free transmission. Ultra-Violet Products, Inc., 5100 Walnut Grove Ave., San Gabriel, CA 91778. Circle 203

## INCREASED DISK CAPACITY FOR SYSTEM/38

The 3370 direct access storage device for IBM's System/38 and 4331 and 4341 processors is an advanced fixed-media disk unit that provides 571.3 Mbytes of auxiliary storage. Up to four 3370 devices can be attached to any System/38 Model 5 for an additional 2,285.5 Mbytes of auxiliary storage. Supported by System/38's singlelevel storage management, the new units are compatible with thesystem's previously announced disk capacities ranging from 64.5 to 387.1 megabytes. Average seek time is 20 milliseconds. Nominal data rate is 1.859 Mbytes per second. Two 3370 models will be available in February 1980 for attachment to System/38: Model A 11 attaches to the IBM 5381 system unit model 5, and up to three model B 11's can be connected through an A 11 unit. Model A 11 can be leased for \$900 a month, rented for \$1,058 a month or purchased for \$35,100. Corresponding charges for each B 11 unit are \$600, \$705 and \$23,400, A 3370 Model A 11 Disk Storage Attachment (6303) are required on the 5381 System Unit Model 5. The attachment feature can be leased for \$145 a month, rented for \$167 a month, or purchased for \$5,850. Corresponding charges for the processor unit expansion features are \$15, \$17, and \$585. IBM Corp., General Systems Div., P.O. Box C-1645, Atlanta, GA 30301. Circle 197

#### BURST ERROR ANALYZER

The MK-4A error analyzer offers the system designer ability to analyze burst errors at data rates to 50 Mb/s. Every error burst is captured and measured for distance between bursts, burst length and errors per burst. The definition of the "error-free gap" between bursts can be set by the user from 2 bits to 256 bits. Maximum data rate is derated below 16 bit gaps, to 5 Mb/s for 2 bit gaps. A printer/computer output is provided for data logging. All data is buffered by a 255 word FIFO, which permits printers as slow as 10 lps to be used in systems with moderate error burst activity. It is a full size module requiring a TMI miniframe for power and cooling. \$8800. Tau-Tron Inc., 11 Esquire Rd., North Billerica MA 01682. Circle 207

## MULTIBUS MEMORY PRICE REDUCTION

MUPRO Corp. has reduced prices on its series of 16K memory boards, which are MULTIBUS compatible. The MBC-016 16Kx8 standard memory board has been reduced from \$985 to \$795. The MBC-016 16Kx8 memory board has been reduced from \$1050 to \$850. The MBC-016C 16Kx8 memory board featuring full error checking and corrections (ECC) has been reduced from \$1395 to \$1175. The MBC-016C board also features LED indicators which pinpoint any failing memory chip. These new prices are single quantity with OEM discounts available. MUPRO, 424 Oakmead Parkway, Sunnyvale, CA 94086. Circle 212

## GRAPHICS TERMINAL CAPABILITY

The MEGADATA 700/UETS (Universal Emulating Terminal System) terminal can now be supplied with full graphics capability. Buffer storage is provided for all



graphics that originate at the computer or are generated at the terminal. As a minimum, the graphic matrix has 512 horizontal and 480 vertical dots. Dot, vector, and sequential graphics from the computer can be displayed by the terminal. The vector lines can be generated in any quantities and at any length, position, and angle desired - limited only by the capability of the graphics memory. Conversely, the operator can initiate the same type of graphics at the terminal for transmission to the computer. Special editing facilities permit the operator to erase any dot or vector. Megadata Corp., 35 Orville Dr., Bohemia, NY 11716. Circle 210





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## INDUSTRIAL CONTROL/DISPLAY UNIT

The Termiflex HT/7 Control/Display unit incorporates 2 line display of twenty 0.15"H characters per line and a buffer that permits display of up to 960 characters. The message can be scrolled at the touch of a switch. Packaged in 7 x 4¼ x 2¼" Lexan case, the HT/7 operates on +5 Vdc only, and internally develops ±12 Vdc needed for the unit's RS232C interface. Besides selectable formatting, the unit has adjustable speed and parity, and will operate at full or half duplex. The HT/7 has a simple keyboard and trasmits/displays all 128 ASCII



characters and codes. \$2595 (1 - 9). Termiflex Corp., 17 Airport Rd., Nashua, NH 03060. Circle 183

## TWO NEW MOTOROLA MICROMODULES

Motorola Microsystems has introduced two new monoboard microcomputer micromodules - the M68MM01B and the M68MM01B1A. The M68MM01B is a stand-alone that has all of the processing and control power of an MC6802 MPU with its self-contained clock circuit and 128 bytes of static RAM. Additionally, the module contains sockets for up to 4K of EROM or ROM for programming, a peripheral interface adapter (PIA) for parallel data transfers and a programmable timer module (PTM). The M68MM01B1A is a more fullypopulated version of M68MM01B, with an additional 256 bytes of static RAM, provisions for off-board dynamic memory refresh, an asynchronous communications interface adapter (ACIA) with RS-232C interface circuits, an audio tape cassette interface circuit and bus drivers for the address, data and control bus signals. Additional devices can be added, external to the M68MM01B1A monoboard, unlike the M68MM01B which does not have the address, data or control signals available for interfacing with other modules. Micromodule M68MM01B1A is also bus compatible with the M6800 EXORciser. Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix AZ 85036. Circle 193

## DISK SYSTEMS FOR DG USERS

The new Supermini DSG Series of removable disk subsystems provide storage capacity of 24, 48, 68.9, 182.4 or 261.6 megabytes of data. Storage capacity of each system may be increased with the addition of up to three drives (of the same capacity as the subsystem). The systems have a track to track access time of 6 msec, and average access time of 30 msec and transfer data to or from the Nova or Eclipse computer at a rate of 1209K bytes per second. Automatic Programs Loading (APL) is standard, and the systems are fully buffered with an internal RAM memory. Software support for Data General's Realtime Disk Operating System (RDOS) is also provided. From \$16,900 to \$33,900, including installation. California Computer Products Inc., 2411 West La Palma Ave., Anaheim, CA 92801.

Circle 185

## HARD SECTOR DATA HANDLER

The FDC 3400, an MOS IC floppy disk hard sector data handler (HSDH), performs all the data handling required for hard-sectored floppy disk operation, and is for use in low cost floppy disk controller systems. The FDC 3400 HSDH detects and flags overrun and underrun conditions. Read and write registers are separated allowing simultaneous read and write operations on two different drives for enhanced system throughput. All inputs and outputs are TTL compatible. The HSDH is double buffered, and is usable with single or double density minifloppy or standard floppy disks. Standard Microsystems Corp., 35 Marcus Blvd,, Hauppauge, NY 11787. Circle 186

## ECL DRIVER

The Model PM-501M, ultra wide band programmable driver features wide-band D.C. coupling, excellent pulse fidelity over wide programming ranges and small size. The PM-501M can drive a 50 ohm terminated coaxial cable at rates in excess of 500 MHz with a minimum input pulse width of 1nsec. Rise and fall times are typically 500 picoseconds



with one volt output. Propagation delay is 900 picoseconds. The output offset can be programmed continuously from +0.5 volts to -2.0 volts and amplitude programming is 0.5 volts to 1.5 volts peak-to-peak. The PM-501M, which utilizes thin-film hybrid techniques, is packaged in a 12 pin TO-8 can. The operating temperature range is 0°C to 50°C. \$250. Tau-Tron Inc., 11 Esquire Rd., North Billerica, MA 01862. Circle 190

## **DUAL PRINTER**

Dual printer prints 3 lines per second and has 11 character locations per column with a dual capacity of 6 - 10 columns – up to 22 columns as a single. A large library of characters is available. Among the features are a small print mechanism, self-inking ribbon and a variable paper space control. Tape rewind (one or both sides) is available. The Addmaster dual printer operates with



117V, 60Hz., 1.3 amp drive motor. Other voltages are available. \$66 (quantity) for some configurations. Addmaster Corp., 416 Junipero Serra Dr., San Gabriel, CA 91776. Circle 189

## INTERFACE CONNECTS SEVERAL COMPUTERS

The Digital 3R universal junction unit is a compact connection box that permits direct communication between serial



devices. It incorporates three ports; each has switches to interchange transmit and receive signals, and establish operation in the RS232C or 20 mA mode. Additional switches provide 63 possible communications connections between I/O devices. Measuring 5.3"W x 2.3"H x 7"L, the unit has a built-in power supply and weighs 3.5 lbs. Data flow is monitored by an LED and transmission speeds up to 9600 baud can be accommodated. An indefinite number of communications connections are possible by connecting several units in series. Digital Laboratories Inc., William M. Kahn 600 Pleasant Street, Watertown, MA 02172. Circle 200

## The DP-8 36" Digital Plotter gives you more

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#### HIGH DENSITY VIDEO RAM MODULE

The MTX-2064 or the MMD-2480 provides an interface between any  $\mu$ P and a TV monitor. On the input side the VRAM's look like a 1280 or 4K x 8 bit static RAM with an access time of 500 nsec. The output of



the MTX-2064 is a video signal providing a display of 20 lines by 64 upper and lower case characters. The MMD-2480 provides 24 lines of 80 characters and limited graphics capability. Any character may be displayed as normal, inverse or blink. A universal phase lock loop module permits the MMD-2480 to be locked to an external sync source such as a TV camera. Another option available for both models is a choice of American and European TV standard field rates. The units are completely self-contained including sync generator, RAM, ROM, and bus interface. They are housed in pin compatible 4.5 x 6 x 5" modules and draw under 800 mA from a single +5V supply. Both devices are said to be the highest density video display subsystems ever put into a module, MTX-2064, \$295 (1), \$190 (100); MMO-2480, \$395 (1), \$290 (100). Matrox Electronic Systems Ltd., 2795 Bates Rd., Montreal, Que, H3S 1B5 Canada. Circle 181

## ADD-IN FOR INTEL'S SBC 80

A single-board 16K x 8 non-volatile core for use with Intel's SBC 80/10 and SBC 80/20 computers, the DR-181 can also be used



with computers from other manufacturers that offer SBC 80 compatible products. The DR-181 has the same mechanical outline dimensions as the SBC 80 series and operates from +5 volts and +12 volts. Cycle and access times are 900 nsec and 265 nsec, respectively. The DR-181 allows: a block of memory within the DR-181 to be write protected; address strapping achieved with an on-board DIP switch; and on-board data save. Operation is from 0°C to 55°C. \$880. Datatrom Corp., Princeton-Hightstown Rd., Cranbury, NJ 08512. Circle 191

## MULTIBUS TIMEKEEPING MODULE

For timekeeping applications in MULTI-BUS systems, the MC1460 clock/calendar module provides date and time data through input ports. Fully compatible with any Intel SBC or National BLC series system, the MC1460 uses low power circuitry to allow the date and time to be powered by an external source during system power down. In addition to providing month, day, hours, minutes, and seconds data, the MC1460 can satisfy many interval timer requirements with range from every 10 milliseconds to once per day. Power fail interrupts can be generated by the MC1460 using either the on-board power monitor, or an external power status signal. Canada Systems Inc., La Canada, CA 91011 Circle 196

## **RASTER SCAN GRAPHICS MONITOR**

A new, high resolution, high density CRT display module is now available in OEM quantities from CPT Corporation. The module, the HRD-15, uses a 15" CRT to display a 1024 x 768 non-interlaced raster. With a band width of 105 MHz the non-interlaced system scans at up to 64,000 scan lines per second. The entire image is updated at 60 frames per second. Dot resolution is rated at .01 inch with clear definition, since rise/fall times are less than 3 nanoseconds. The standard



phosphor is P-104 with others available on request. The high resolution screen is human engineered for 8 hours per day use without eyestrain. **CPT Corp.**, 1001 Second St. So., Hopkins, MN 55343 **Circle 194** 

## LIQUID CRYSTAL DISPLAYS

The FE0101 liquid crystal display features a .3" digit height. 4 digits, 3 decimal points, 1 colon, a minus sign and 5 "arrow-head pointers." Available in the transmissive, reflective and transflective modes, it can be purchased only in a pinless version for use with elastomeric connectors. The overall size of the liquid crystal display is 1.570" x 0.700". Liquid crystal materials are available in two operating termperature ranges: --10°C to +55°C, and -5°C to +90°C. Red, blue and green readouts are available through special order. \$9.95 in quantities of 100 units and delivery is from stock in small quantities. And, 770 Airport Blvd., Burlingame CA 94010. Circle 192

### REMOTE DATA ACQUISITION SYSTEM

The ASC remote data acquisition and control system provides extended logical/ arithmetic and control programming capabilities and is expandable to over 256 analog I/O or controller functions. The system utilizes a MP featuring 8/16 bit architecture,



a 1 usec. instruction cycle, multi-level priority interrupts, fast multiply-divide arithmetic commands and interfacing for both high-speed analog to digital conversion and serial communications modules. Features include plug-in cards for the MP unit, memory modules, analog and digital I/O and optional data displays, plus provisions for operator control panel and AC or DC power supplies. I/O capabilities include high-speed A/D Converters with 8, 12, or 14 bits precision, analog multiplexers for up to 256 inputs with ± 50mv. to ± 10V.D.C. signal range, digital I/O expanders for up to 1024 lines, and Asynchronous/Synchronous serial communications adapters offering data rates from 1200 to 240K baud. Custom I/O adapters can also be provided. The system affords compatability with the Intel 8085/ 8086 micro-processor components and system software. Applied Systems Corp., 2640 Harper Ave., St. Clair Shores, MI 48081. Circle 205

#### **RS232 MONITOR/TESTER**

SAM, Expandor's Status Activity Monitor, can be used as a testing device, or can be mounted onto the interface circuit as a temporary or permanent monitor. A third connector is provided for additional testing of terminal equipment. SAM's nine LEDs indicate activity on the 7 most common RS-232 leads. Two additional LEDs indicate high or low level, or positive clock indication. RS-232 lead identification is printed on the unit, and full operational (diagnostic) isstructions are included. Expandor Incorporated, 400 St. Claire Plaza, Upper St., Clair, PA 15241. Circle 201



## G-TAPE

THE UNIVERSAL TAPE THE CRITICAL APPLICATION TAPE THE HI SPEED TAPE THE LOW SPEED TAPE THE VIRGIN TAPE THE ENVIRONMENTAL TAPE THE 556/800 TAPE THE 1600/6250 TAPE THE STORAGE TAPE THE STORAGE TAPE THE 25 YEAR TAPE

G TAPE

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United States Wabash Tape Corporation, 2700 Des Plaines Ave., Des Plaines, III. 60018, Tel. (800) 323-9868 Telex 9106511800 Canada Wabash Tape Canada Ltd. 3135 Universal Drive. Mississauga, Ontario. Canada L4X2E6 Tel. (416) 625-9533 Telex 06961345 Europe Wabash Tape (U.K.) Ltd., Crown Rd., Cold Norton, Chelmsford, Essex, England CM36J F Tel. (STD062185) 8181 Telex 995455

## TAPE READER MANUAL

Manual for the computer compatible standalone Model 612 describes the operation of this new model and details the characteristics of the options available, including an RS232C interface. The principles of operation are explained and installation and checkout described. Schematics and logic diagrams are provided. Addmaster Corp., 416 Junipero Serra Dr., San Gabriel, CA 91776. Circle 188

### SINGLE BOARD MICROCOMPUTER WITH FLOPPY DISK CONTROLLER

The 90F/MPS microcomputer is a single board OEM product, based on the Z80  $\mu$ P. Board-resident facilities include: multi-density DMA floppy disk controller, up to 65 Kbytes dynamic RAM, up to 14 Kbytes of ultraviolet erasable PROM with programmer, 1 Kbyte of static RAM, up to four 8-bit programmable I/O ports (two Z80-PIO's), four programmable counter/timer channels



(Z80-CTC), an RS232C or 20 milliampere serial port with selectable baud rates, 2.5 or 4 MHz. operation and, PROM-resident system monitor with debug capabilities. Features of the floppy disk controller include: DMA-based disk access, support of up to four 5 ¼" or 8" single/double density drives, multi-track transfers and data scanning. Price with 16KB dynamic RAM and two parallel ports is \$1,295. Quay Corp., P.O. Box 386, Freehold, NJ 07728.

#### Circle 182 DIGITAL DECLAB-11/MNC

The DEClab-11/MNC system design permits the user to customize the system's configuration through use of up to eight plug-in "MINC modules", which can include various combinations of the seven different functional module types. The central subassembly incorporates a PDP-11/03  $\mu$ C with 64K bytes of semiconductor memory. Other system elements of the DEClab-11/MNC include the twin removable storage disks, a 4port terminal interface, a read-only memory (ROM) diagnostic bootstrap, and either an LA36 DECwriter II or a VT105 video terminal. Standard software for the DEClab-11/ LA36 DECwriter II or a VT105 video terminal. Standard software for the DEClab-11/ MNC system includes ANSI-standard FOR-TRAN-IV, a laboratory subroutine package, and a scientific subroutine package. From \$21,000. Digital Equipment Corp., Maynard MA 01754. Circle 184

### HIGH VOLTAGE MEASURING SYSTEM

Using fiber optics and FM carrier modulation, Pulsar Model 710 makes it possible to accurately measure high voltage without making any electrical connections to the meter. The Model 710 system consists of a high voltage probe (with optical transmitter) and a receiver unit. The probe, and the opti-



cal transmitter enclosed in the probe, are electrically isolated from the receiver and from laboratory ground. Information is transmitted by an FM light signal on a fiber optic cable to the receiver unit. The meter is liquid crystal display. The Model 710 transmitter and receiver are both powered with rechargeable batteries. Two external battery charger units are supplied with each system. The 710 receiver unit can be connected to an oscilloscope. The fiber optic link protects the oscilloscope from unexpected transients occurring at the probe. Singer Products Company, Inc., 875 Merrick Ave. Westbury, NY 11590. Circle 179

## P.C. CARD GUIDE SYSTEM

DIGI-STRUT along with the MC-10 DIGI-GUIDE offers low cost, light weight printed circuit mounted card cage assemblies, which give rigid mechanical support to the plug in cards. DIGI-GUIDES and DIGI-STRUTS are made from .012" thick brass stock, which is tin plated to provide excellent solderability for easy assembly. Each DIGI-GUIDE mounts in three .055" dia. holes in the



mother board and are then wave-soldered. The DIGI-STRUTS are clamped to the outside of each row of DIGI-GUIDES and sodered in place. DIGI-GUIDES are available in lengths from 3/8" up to 1 3/8" above board, and DIGI-STRUTS are available in any length up to 12". Components Corp., 6 Kinsey Pl., Denville, NJ 07834. Circle 178

## FOUR LOW-POWER 4K RAMs

Four new low-power fully-static randomaccess memory (RAM) ICs are types TMS-40L44 and TMS40L46, organized as 4K x 1, and type TMS40L45 and TMS40L47, organized as 1K x 4. Each comes in three speed ranges - 450, 250 and 200 nsec maximum access times. All RAMs are fully static. The RAMs operate from single +5 volt supplies and are fully TTL compatible. A three-state output and a chip select makes memory expansion simple. Typical operating power dissipation for the 200 nsec versions of the 40L44 and 40L45 is 200 mW and 250 mW respectively. All other types offer virtually identical performance, with the TMS40L46 and TMS40L47 series offering an additional feature of power down operation with a very low power consumption of 6 mW typical. Typical standby power for the 200 nsec TMS40L44 and 40L45 is less than 85 mW at reduced VCC. The TMS 40L44 and 40L45 are packaged in an 18-pin package, the TMS 40L46 and 40L47 are in a 20-pin package. All the RAMs have fully decoded direct addressing and are available in plastic or ceramic DIP rated over a temperature



range of 0°C to 70°C. 450 nsec maximum access times \$6.90 (100); 200 nsec access times \$11.40 (100). Texas Instruments Inc., P.O. Box 1443, M/S 669 (Attn: 4K Static) Houston, TX 77001. Circle 177

## **µC PROTOTYPING SYSTEM**

A Eurocard width (100mm) universal prototyping card for microcomputer and other bus-oriented designs has been announced by Cybertek, Inc. The 4" x 6" board, designated the LP-12U, accommodates a dense mix of DIP packaged IC's of all sizes (it will hold 20 16-pin DIPs). The board has 60 goldplated edgeboard connector fingers at each end. LP-12U cards can be interconnected without chassis wiring using one of Cybertek's generalized motherboards. Two styles of motherboard are available: one for openframe mounting on a 5" x 9.5" chassis and one for use with card-cages. Either style is available with 1 inch (8 position) or 0.625 inch (12 position) connector spacing. Prototyping boards can also be interconnected via the top-of-the-board connector using 60conductor flat-wire cable and 60-position flat-wire edgeboard connectors. The motherboard also accommodates wirewrap sockets which permit bus extension to a second chassis. Extension cards are also available. Cyberteck, Inc., P.O.Box 3467, Seminole, FL 33542. Circle 180

## M6800 EXORTERM 220 2 MHZ DEVELOPMENT SYSTEM

EXORterm\* 220 display terminal and console, for use as a development support system for the M6800 family (MC6800, MC68-A00 and MC68B00), is designed for soft-ware and hardware system development for all Motorola and second-source M6800 family micros and single-chip micros operating at speeds up to 2.0 MHz. EXORterm 220 facilitates data exchange between user and system via a high-quality video interface in conjunction with a keyboard. To further enhance interface efficiency, special keys



have been encoded to invoke functions unique to the development system in each of its command levels - EXbug and DOS. A basic EXORterm 220 incorporates a CRT chassis with a keyboard and isolated motherboard, MPU II Module, DEbug II module, two 16K RAM Modules, Resident Relocatable Macro Assembler/Linking Loader and CRT Editor to provide basic control and interface functions of a micro, and house the system's EXbug II development and diagnostic programs, along with capability of preparing M6800 programs. With provisions for up to four more EXORciser modules or Micromodules, a system of almost any complexity can be quickly assembled. M68SXS2201DM, \$8600. Motorola Semiconductor Products, Inc., Box 20912, Phoenix, AZ 85036. Circle 175

## VOICE RESPONSE SYSTEM

The PTC BT-1 Voice Response System enables a computer to communicate in natural human sentences or phrases. Plug and software compatible with the DEC PDP-8 and PDP-11, the system utilizes compressed and



prestored telephone quality human speech; voice responses are not computer synthessized. Including speaker, amplifier, cable, and standard 13 word vocabulary \$1200; each additional word typically costs \$20 -\$30. Perception Technology Corp., 95 Cross St.. Winchester, MA 01890.

Circle 172



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MARCH 1979 Digital Design 87

## PUSHBUTTON LOCK IN LSI CHIP

Model 7220 keyless lock is said to be the first MOS/LSI chip form. Its tiny size, 14 pin DIP, makes possible the manufacture of digital locks to a new level of compactness. Marketability and reliability are enhanced for applications in automotive, residential, commercial and area access control security. Model 7220 highlights: 5,040 possible 4 digit combinations, out-of-sequence detection logic; very low current consumption (less than 14 uA standby); "Save" mode, for valet parking, which can be set in "unlock" after proper sequence has been set; and builtin convenience delay. \$1.25 (1,000) LSI Computer Systems Inc., 1235 Walt Whitman Rd., Melville, NY 11747. Circle 173

#### **SERIAL RS232 PROBE**

The Model 70 serial interface probe offers a cost-effective way to convert the Model 532 intelligent logic state analyzer into a powerful tool for testing asynchronous RS-232 and 20mA current loop interfaces. The Model 70 is plugged into the Model 532's A channel input port. If desired, the B port can be connected to monitor 16 channels of related parallel information. The Model 70 can simultaneously receive and transmit data. To support the Receive mode, all that is required is a standard Model 532. The user can then trigger on any character and store a 250-character sequence along with the as-



sociated handshaking signals. The resulting data can be displayed on the Model 532's readouts in hexadecimal, or on an optional oscilloscope or terminal in hex or binarry. For the Transmit mode, the Model 70 software option is required. This software resides in PROM in the Model 532's User's Program Memory Board and permits the Model 70 to send "canned" tests to a terminal or other serial device. The software also allows hex entry of custom messages of up to 256 characters directly from the Model 532's keyboard. \$390 (software option \$125). Paratronics Inc., 800 Charcot Ave., San Jose, CA 95131. Circle 170



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Raymond's new Model 6413 Cartridge Recorder is the result of our years of experience building thousands of recorders for the 1/4-inch data cartridge. Our experience means that you get the best. For complete information:

Raycorder Products Division Raymond Engineering Inc. 217 Smith Street, Middletown, Connecticut 06457 (203) 632-1000

a subsidiary of Raymond Industries

## FLOPPY CONTROLLER

A double density floppy disk controller for SBC-80 computers is on a single-board controller with DMA channel It features compatability with IBM 3740 single density and both IBM 2D and Intel SBC-202 double density formats. The intelligent controller incorporates an 8085 processor to direct diskette operations. Disk data is buffered in a one Kbyte RAM buffer. Data is transferred to or from the system by DMA data transfer at a rate of over 1 Mbyte/sec. A phase-lock-oscillator and write precompensation circuitry are included, as well as CRC error detection logic. A hardware UART with RS-232 interface is also on the board to facilitate communication with a system console device. Bus arbitration and Master control logic coordinate the DMA transfer. \$995. Micromation Inc., 524 Union St., San Francisco, CA 94133. Circle 166

## **48 VDC MINICOMPUTER MAG TAPE**

The Series 40 line of minicomputer magnetic tape peripherals includes a 48 VDC option in place of the standard AC power circuitry for battery operated or backup applications. The DC option incorporates a high-frequency (20 kHz), transformercoupled, DC to DC converter to provide all



operating power for the tape drive and its imbedded formatter. The 48 VDC option is available on all tape drives in the Series 40 family. Circuitry for the option is mounted internally for the 1749 (101/2" reel) and 1649 (81/2" reel) machines and in a small outrigger box for the 1149 (7" reel), \$300, Digi-Data Corp., 8580 Dorsey Run Rd., Jessup, MD 20794. Circle 162

### **16K RAM FOR MICROCOMPUTERS**

Organized as 2K x 8 for wide word applications, the MK4816 +5 V 16 KRAM offers a collection of features to simplify system design and operation. The memory replaces four 2114-6-type static RAMs. Access time of 150 nsec and cycle time of 270 nsec meet the needs of all microprocessor sockets. This memory uses a dynamic periphery and a one transistor storage cell to reduce die size to just 31,000 mils<sup>2</sup> as well as power dissipation to only 150 mW. On-chip logic, refresh and interface circuits make the 2K x 8 RAM as easy to use as the static RAM it is designed to replace, the company said. Other features include on-chip substrate bias generator, automatic precharge for mini-

Circle 51 on Reader Inquiry Card



mum cycle time and complete TTL compatibility. Once accessed, this intelligent RAM can maintain data for indefinite per periods of time to eliminate the need for output latches and permit single step operation for system debug. \$48.05 (150 msec) (100): \$35.16 (300 nsec) (100). Mostek Corp., 1215 W. Crosby Rd., Carrollton, TX 75006. Circle 169

## COMPACT OCR SYSTEM

The Scan-Data 1150 OCR system can read alphanumeric OCR-A, OCR-B and, optionally. numeric handprint. Throughput rate is five 8½" x 11" pages per minute. Features include an alphanumeric font, a magnetic tape unit, on-line display for reject handling, automatic feeder, two-pocket stacker, and an RS-232C communications interface. Also included is a programmable format controller, which allows the user to create parameter sheets directing the 1150 to selectively read only the desired segments of forms. \$41,000. Scan Data Corp., 800 E. Main St., Norristown, PA 19401. Circle 165

## SERIES/80 SYSTEM PACKAGE

The RMC 660 consists of two system board chassis, power supply and front panel with control switches mounted in a standard RETMA enclosure. It accepts up to eight boards and may be used either to assemble a Series/80 board-level computer system or as an expansion chassis on existing systems. Power, bus and control lines are interconnected with etched back-plane circuits. Designed for either National or Intel board-level computers, the RMC 660 has a heavyduty regulated power supply providing -12V, 1.5A, +5V, 30.0A, -5V, 1.75A and -12V @ 1.75A. The RMC 660, including power supply and dual fans, measures 7.00" x 19.00" x 20.00"; weight is 49 lbs. \$1250. National Semiconductor Corp., Computer Products Group, 2900 Semiconductor Dr., Santa Clara, CA 95051. Circle 174



### HP/DEC PAPER TAPE REPLACEMENTS

Two models of the FDS-100 family represent exact paper tape replacement for HP-2100 and HP-21MX and PDP-11 minis. They are self-contained minifloppy (5.25 inch) disk drive, power supply, intelligent controller and interface in a box. The FDS-100 has powerful, firmware resident file management controlled through front panel numeric keyboard. For example, instead of loading paper tape into a reader, a simple keyboard operation like 2\*37# will open for reading (code 2) file number 37. Each file corresponds to one paper tape, up to 50 files can be maintained in the directory, and file length can be from one byte up to total



diskette capacity. \$1,795. Guc Products, 11815 Sorrento Valley Rd. P.O. Box 22615, San Diego, CA 92122. Circle 171



Circle 52 on Reader Inquiry Card

## **TP-3150 THERMAL PRINTER**

The TP-3150 thermal printer features microprocessor control with complete interface electronics and printer mechanism. The TP-3150 requires only power supplies and ASCII input. With fully automatic 18



character capacity, the solid state moving thermal printhead prints 5x5 matrix characters. Also featured are user controlled print direction and character rotation, ASCII data acceptance in synchronous parallel or asynchronous bit-serial format, and acceptance of the standard 64 character ASCII subset while all other codes are ignored. Input signals included on the TP-3150 are Data Ready, Character Inversion, Left Justification, Serial Data, Logic Reset, Local Paper Advance and Parallel Data Mode. \$270. Bowmar Instrument Corp., Commercial Products Division, 8000 Bluffton Rd., Circle 164 Fort Wayne, IN 46809.

### MONOBOARD MICROCOMPUTER MICROMODULES

The M68MM01B and M68MM01B1A monoboards are added to Motorola's existing micromodule product line and offer several additional features, primarily the programmable timer function for process controls. The M68MM01B is a stand-alone microcomputer that has all of the processing and con-

trol power of an MC6802 MPU with its selfcontained clock circuit and 128 bytes of static RAM. Additionally, the module contains sockets for up to 4K of EROM or ROM for programming, a peripheral interface adapter (PIA) for parallel data transfers and a programmable timer module (PTM). The M68MM01B1A is a more fully-populated version of the M68MM01B, with an additional 256 bytes of static RAM, provisions for off-board dynamic memory refresh, as asynchronous communications interface adapter (ACIA- with RS-232C interface circuits, an audio tape cassette interface circuit and bus drivers for the address, data and control bus signals. For greater memory and I/O capacity, additional devices can be added, external to the M68MM01B1A mo monoboard, unlike the M68MM01B which does not have the address, data or control signals available for interfacing with other modules. M68MM01B \$286; M68MM)1B1A \$495. Motorola, P.O. Box 20912, Phoenix, AZ 85036. Circle 157

### HARRIS BOOSTS 1600 SPEED

The 1600-02 Model II processor, a 16-bit minicomputer is capable of improving the performance of Harris' 1600 remote batch and distributed data processing systems by 200 to 300%. The Model II expands the memory of the older 1600-00 processor to 188K bytes. The speed of the processor allows faster cursor positioning; 9 higher line speeds for keystations and disk access, and less chance of over-runs. Concurrent multiple remote job entry and data entry are made possible by the expanded capacity of the Model II. The Model II can execute 1.2 to 1.4 million instructions per second that was made possible by a unique instruction execution architecture and memory transfer. The double-width 32-byte memory transfer is capable of transferring two 16-byte words from memory simultaneously. Harris

Corp., Data Communications Division, 16001 Dallas Parkway, P.O. Box 400010, Dallas, TX 75240. Circle 202

#### DEC-COMPATIBLE FLEXIBLE DISK

The DSD 440 offers DEC users software and diagnostic compatibility with the DEC RX02. Available with interfaces to LSI-11, PDP-11 and PDP-8 computers, the system is capable of recording data in either DEC double density format or IBM 3740 single density format. The DSD 440 is packaged in a low profile chassis. The DSD 440 requires only half as much rack space as the DEC RX02 while providing the same storage capacity. A 512-word bootstrap program is



built into the LSI-11 and PDP-11 DMA interfaces. In addition to its normal function, this bootstrap program also performs diagnostics on the interface, controller and CPU memory. \$3695. Data Systems Design, Inc., 3130 Coronado Dr., Santa Clara, CA 95051. Circle 187

## INDUSTRIAL USER S100 PROCESSOR

Designed especially to work in industrial environments the INMOD-885 features a 3MHz 8085A CPU, powerful EPROM monitor, 20 digit keyboard and 8 digit prompting hex display. The 8085A CPU executes all 8080 progams at 50% faster speed even though the system chip count ad power supply requirements are reduced. By replacing the confusing binary front panel with hex keyboard/displays the user gains speed and versatility in programming and debugging. The powerful conversational monitor provides usual I/O functions plus memory protect/unprotect, and two power-



Circle 53 on Reader Inquiry Card



ful debugging aids. Multi-Step allows you to define the numer of instructions to be executed before control is returned to the monitor. In addition, you can program the number of break-points "hits" before returning to minitor control. Industrial Modules, Inc., P.O. Box 2985, Santa Clara, CA 95051. Circle 160

## CODE CONVERTER PERFORATOR

The Model 5071 code converter perforator is an intelligent tape punch designed to serve the inter-code needs in data communications, word processing and numerical control applications. The 75 cps, asynchronous Facit 4070 punch mechanism is used. Using  $\mu C$  in the interface, it is possible to convert from any 5, 6, 7 or 8 level code to another 5, 6, 7 or 8 level code by change of the control memory. Current versions include ASCII to Baudot, Baudot to ASCII, HEX to EIA and EIA to HEX. Both RS-232C and current loop (20-60 ma) are provided as input circuits. Power requirements are: 110/127/220/240 VAC, 48-62 Hz. Data Science, 1189 Oddstad Dr., Redwood City, CA 94063. Circle 158

## A/D BOARD FOR LSI-11/2

The SineTrac LSI2 A/D board for the LSI-11/2 microcomputer has all the interface controller logic, plus 16 A/D channels on one half-quad (8.5" x 5") board. In addition there are a programmable gain amplifier, the DC/DC Power Converter, an on-board Pacer Start Clock with 16 programmable timebases, and a full diagnostic program on paper tape plus program listing. Input impedance is typically 100 Mohms with 30 picoA typical bias current. Overall accuracy at +25° C is  $\pm 0.025\%$  of the full scale range,  $\pm 1/2$  LSB. Temperature drifts are held to  $\pm 30$  ppm of FSR/°C (gain) and  $\pm 20 \ \mu$ V/°C



(zero). Common mode rejection of differential inputs is 100 dB at 60 Hz over  $\pm 12V$ common mode range. The total A/D throughput period is 20 µsec. The differential Programmable Gain Amplifier is standard with bit-selected gains of X1, X2, X4 and X8 for expanded dynamic range. Standard input ranges are  $\pm 10V, \pm 5V, \pm 2.5V, \pm 1.25$  using the PGA and 5V or unipolar ranges may be jumper-selected by the user. PC Board pads are left for 8 optional shunt resistors selected by the user for differential current inputs. \$595. Including the DC/DC power converter, PGA and pacer clock. Optional DMA/Interrupt board is \$495. Datel Systems, Inc., J20 Turnpike St., Canton, MA. Circle 163

#### SOCKET PIN PANEL DRAWERS

Designed as DG2 and DG5, two panel drawers offer an efficient means of packaging a socketpin panel wiring system. The DG2 holds up to 4 panels while the half-drawer DG5 holds 1 or 2 panels. These drawers use the EECO-14G frame for mounting the panels in the drawers. Featured are solid top and bottom covers, solid front and back panels and provisions for mounting slides. DG2, \$65; DG5, \$55. EECO, 1441 E. Chestnut Ave., Santa Ana, CA 92701. Circle 161



- To ald In isolating system manufactions, an on-board AOTOMATIC SELF TEST relative monitors the controller for proper operation. A green DIAGNOSTIC indicator on the edge of the controller board remains lighted as long as the controller is functioning properly. If self-test fails, the controller has an AUTOMATIC DATA PROTECT feature that stops the CPU from interacting with the disc or tape, and thus prevents writing erroneous information into critical data base areas.
- All controllers are software compatible with DEC\* operating systems.
- Various levels of system support are available factory integration of customer-supplied peripherals, complete peripheral subsystems including a DILOG-selected peripheral, engineer/systems analyst consultation for special applications involving DILOG controllers.

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Come meet the current family members and let us introduce you to the newest arrival at NCC 79 in Booth 351 at the New York Hilton. But don't wait until then to let us hear from you; write or call SALES MANAGER, Distributed Logic, Inc., 12800G Garden Grove Blvd., Garden Grove, California 92643. TELEPHONE (714) 534-8950.

\*DEC, PDP-11, LSI-11 are registered trademarks of Digital Equipment Corporation.

#### Circle 54 on Reader Inquiry Card

MARCH 1979 Digital Design 91

## DRAWER SYSTEM

A drawer system that packages standard Augat IC Wire Wrap panels comes in two sizes: one or two boards accommodating up to 720 16-pin devices, the other handles three boards with up to 1080 16-pin devices. Backplanes, with feed-through I/O, are mounted in the rear of the drawers for cabling access to the boards. Front panels and covers are perforated to allow proper air flow; and the drawers have provisions for mounting fans, filter, and DC power entry



in a standard 19 in. cabinet. A new family of Augat mating boards are used for the drawer system to provide for the mounting of IC and other components and the pins for wire-wrapped interconnections. TTL, ECL, and Schottky boards are available for the drawer system. Augat Inc., 33 Perry Ave., P.O. Box 779, Attleboro, MA 02703. Circle 168

#### ADDITION FOR DATASYSTEM LINE

The Datasystem 150 has a starting price of \$10,900 and is designed as an intelligent network node for large corporations or stand-alone computer system for small companies. It uses a dual-drive flexible disk unit for storage of up to 512,000 characters. The disk unit and LSI-11 are contained in a small cabinet that may be placed on top of the workstation/desk adjacent to the system's VT100 terminal. The system runs under CTS-300 (Commercial Transaction System 300) operating software, permitting processing of business applications such as payroll, accounts payable and receivable, general ledger and inventory in high-level DIBOL (DIgital Business-Oriented Language). CTS-300 offers sequential, indexed sequential and random file access methods. D150 programs will also run on Digital's D320 and D350 computers, the multi-terminal members of the family that are capable of supporting up to eight terminals. Datasystem 150 systems are available with memory sizes of either 32K or 60K bytes,

and use a 180-character-per-second dot matrix printer. Digital Equipment Corp., Maynard, MA. Circle 176

### **ON-CARD MULTICHANNEL A/D**

Designed for data acquisition and direct control applications, the MLZ-DAQ sports ADAC Adam-12 or 12APG A/D module providing 16/32 12 bit channels of analog input. Input voltage ranges may be -5V to +5V, 0V to +5V, -10V to +10V, and 0V to +10V. Inputs may be paired for monitoring differential analog signals. Four software selectable gains allow a mixture of both high and low level signals to be monitored. Avail-



able in 2MHz and 4MHz configurations, other standard features include Zilog Z-80 CPU, two RS232C ports, dual baud rate generator, four 8 bit ports, four counter/timers, 1K static RAM and sockets for 4/8K bytes EPROM. Mounting holes in each corner and auxiliary power input are provided for single board applications. Designed for Intel Multibus users, cards and systems are available. \$545. Heurikon Corp., 700 W. Badger Rd., Madison, WI 53713.

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## SERIES/80 DATABOOK

National Semiconductor Corp. offers, free of charge, its new Databook on the Series/80 family of microcomputer products. The databook includes descriptions, photographs and conceptual diagrams of six board level computers, three rack mounted computer systems and three prototyping systems, all based on the 8080A. More than 30 supporting products are described, including memory boards with RAM or ROM/PROM, I/O Expansion Boards, Combination Memory and I/O Boards, Analog I/O Boards, Peripheral Controllers, and system chassis and power supplies. In addition, the databook and its supporting software. Write on company letterhead to National Semiconductor Corp., C.P.G. Marketing Services, MS/10A190, 2900 Semiconductor Dr., Santa, CA 95051.

#### SINGLE CHIP NMOS µCs

A uniquely configured family of single-chip microcomputer devices with a bus-oriented architecture, the 70-Series family, are intended for use in systems requiring the economy of a single chip, the flexibility of multiprocessing bus architecture and the power of a comprehensive set of 16-bit arithmetic operations. Designed for ease of implementation in stand-alone, direct memory access and multiprocessing applications, first members of the INS8070 family include: the INS8070, minimum system containing 64 bytes of RAM and no on-chip ROM; the INS8072, containing 64 bytes of RAM and 2.5K bytes (20K bits) of ROM; and, the INS8074, containing 64 bytes of RAM and 4K bytes (32K bits) of ROM. The instruction set is especially suited to control system applications, as well as high level language execution; while the multiprocessing bus architecture makes the design of DMA systems such as terminals, home computers and word processors very simple. Communications between INS8070 devices and external memory and/or peripheral devices are effected via a 16-bit dedicated address bus and an 8-bit bidirectional data bus. Major features of the family include: simplified programming, with multiple addressing modes, including counter-relative, immediate data, indexed, auto-indexed, implied and single byte subroutine calls; stack operation, with a comprehensive set of 16-bit instructions, including load, store, add, subtract, multiply, divide, exchange, shift and stack push/pop; unique features of the 8070 include an ASCII to BCD conversion in one instruction and the character search instruction both of which are especially useful for high level language; large system capability, with address capability up to 65K bytes memory; handshake bus-access control on-chip, for multiprocessing and DMA operations; system flexibility, with the ability to interface with memories of peripherals of any speed; on-chip generation, two interrupt/sense inputs, and three user accessible control-flag outputs. National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051. Circle 218

#### **20 MBS FIBEROPTIC LINK**

The 20 Mbps Fiberoptic Digital Communication Link is a full-duplex link with simplex versions also available. The digital communication link modules are capable of operating up to a 20 Mbps (NRZ) data transfer rate over a commercially available fiberoptic cable. The links have been designed to transmit serial data over a distance of 3,000 feet (1 kilometer) with a typical operational bit error rate exceeding 10<sup>-9</sup>. Electrical interface to the communication link is provided by a 30-pin edge connector. Electrical I/O (input/output) interface is TTL compatible, which makes the communication link very easily adaptable to all existing communication ports utilizing a TTL output. By having an input/output compatibility with TTL sources, the unit can also supply customers with a fiberoptic communication I/O port for any custom interface that they may wish to produce. Because the link has been designed around the fiberoptic technology, the user benefits from the added features that transmission gives him, such as elimination of electromagnetic interference, electrical equipment isolation, ground loop avoidance, data transmission security, etc. The cost of the 20 Mbps Fiberoptic Digital Communication Link in a full-duplex application is \$475. The rack mount chassis is also available through Canoga Data Systems, pre-wired for 16 data links, and with power supply, for \$750. Canoga Data Systems, 6740 Eton Ave., Canoga Park, CA 91303. Circle 221



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## **ONE-CHIP UNIVERSAL TIMER CONTROLLER**

Designated the TMS 1121, the TMS 1121 is a pre-programmed (firmware) version of the TMS 1000 single chip microcomputer. The TMS 1121 features 18 daily or weekly selectable timer settings, four independent switched outputs for control of external devices, 50 Hz or 60 Hz line synchronization, and display signal driver input for both day of the week and time of the day. When the universal timer/controller is connected to a keyboard, drivers, an LED display, and a single 9-volt power supply, the combination forms an accurate low-cost timer control module. Examples of possible applications are kitchen appliances, home security systems, and VTR timer controls. The TMS 1121 is offered in a 28-pin plastic DIP. Price in 100-piece quantities is \$8.61 each. Texas Instruments Inc., Box 1443 M/S 6406 (Attn: TMS 1121) Houston, TX 77001.

Circle 217

## LSI SUBSET

Model FSM-86A single channel LSI Subset has been designed to provide a low cost, highly reliable state-of-the-art programmable Frequency Division Multiplex (FDM) stand-alone unit employing unique MOS/LSI techniques. This allows individual channel frequency selection of any channel within a specific baud rate by simple dip switch settings. Primary application is for transmission and reception of FSK data over voice frequency transmission media, such as telephone lines, HF radio, microwave or satellite circuits. Channelization and frequency assignments are available for compatability with relevant CCITT, CCIR and Bell System recommendations. Coherent Communications System Corp., 85D Hoffman La. South, Hauppage, NY 11787.

#### 4 MHz 16-BIT MPU

A four megahertz 16-bit microprocessor from Texas Instruments Incorporated provides a 33 percent increase in throughput. Performance of the new MPU, designated the TMS9900-40, is maximized by using separate address and data buses to avoid multiplexing delays. The TMS9900-40 is a full 16-bit microprocessor featuring a minicomputer instruction set and memory-to-memory architecture. Three separate I/O techniques are supported, including DMA, Memory-mapped and CRU (providing optimum control line manipulation without using memory space). The CRU provides a simple, single command page switching capability for memories larger than 65K bytes. The TMS9900-40 is fully supported by a new universal emulator for the Advanced Microprocessor Prototyping Laboratory (AMPL). Both floppy disk and hard disk based systems with high level language development options are available. Pricing: TMS-9900 J-40 JL CPU, \$41.25; TMS9902 N-40 NL ACC, \$5.63; TMS-9904 N-40 NL CLK. DR., \$7.20 (100 qty). Texas Instruments Inc., Box 1443 M/S 653 (Attn: TMS9900-40) Houston, TX 77001. Circle 213

#### **KMW VECTOR PROCESSOR**

The VP Series random vector processor accepts random vectors and symbols from a host mainframe, reduces the information to raster form, and outputs it to a wide variety of popular electrostatic and matrix plotters, including most Versatec, Gould, Houston Instruments, and Trilog models. The VP system design incorporates LSI technology, with reliable MOS memory for vector and symbol storage. Microprocessor-controlled ROM storage provides system logic, with high-speed arithmetic implemented in TTL logic. The wide variety of available data input options includes mag tape, serial asynchronous RS-232, IBM bisync, and 8-bit parallel. The VP system also accepts data in "line printer" format, outputting it to the attached printer/plotter operating in hardware print mode. Random vector and symbol output from the mainframe is produced by a machine-independent FORTRAN driver program provided by KMW and integrated into the user's graphics application software. This software simply reformats random vectors and symbols from internal "floating point" format to KMW output format. KMW Systems Corp., 8307 Highway 71 West, Austin, TX 78735. Circle 219

## **ADVERTISER'S INDEX**

ADD MASTER	
ADTECH POWER	.68-69, 71
APPLIED DATA COMMUNICATIONS	
ASSOCIATED COMPUTER CONSULTANTS	
BALL BROTHERS	
BEEHIVE INTERNATIONAL	
CEC Div./BELL & HOWELL	
DATA CARD/Troy Computer Products	47-49
DATACQ	
DATAFLUX	
DATARAM	
DE ANZA	
DIGITAL DESIGN MAGAZINE	.56, 64, 93
DIGITAL PATHWAYS	
DIGITKAN	
FLECTRO'79	73
ELGAR	
ELPAC POWER SYSTEMS	
ЕТАТЕСН	
FUJITSU AMERICA	
GOULD/Printer/Plotter	
НУСОМ	
HOUSTON INSTRUMENTS	
INTERDESIGN	17
KEYTRONIC	53
LAVEZZI MACHINE WORKS	
LH RESEARCH	
MAGNETIC SHIELD Div./PERFECTION MICA	
M.D.B. SYSTEMS	
	C-4
NCC '70	76
PARATRONICS	14
PERKIN—ELMER	
POWERTEC	
PRINTRONIX	
RAYMOND ENGINEERING	
HOWARD W. SAMS	
SD SYSTEMS	C-3
STANFORD TECHNOLOGY	
TANDBERG DATA	
TELETYPE	
WESTERN PERIPHERALS Div./WESPERCORP	
ZETA RESEARCH	C-2

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## Future Shock: The Changing IC Industry

Where is the IC semiconductor industry heading? Changes are taking place quite rapidly, and in the near future, the industry will change drastically. Six years from now there will be only three types of companies left in the IC semiconductor industry: several multi-national companies, untold specialists and "insurance policy" holders.

First, up to ten multi-national companies will exist, and each will serve the total market-with broad product lines – worldwide sales, marketing and applications help. They will provide multi-country production-broad cooperation with users in many markets with an extremely flexible systems IC interface. Second, there will be untold specialists – both IC companies and users making specials for themselves. I will use the term "IC companies" interchangeably with "IC division of a company." Third, two categories of insurance policy holder companies will include: a) system companies who wish to manufacture volume and special ICs for themselves, and b) companies that are being subsidized by national governments to develop a local IC industry.

The IC business is an open industry; everything is available to everyone and no barriers exist. No knowledge or patent barriers exist, since free international flow of knowledge takes place and no one is denied a patent license. With the exception of Japan, there are negligible trade and tariff barriers today. There are no real barriers to worldwide production since shipping costs are so low. There are no capital barriers nor any barriers to hiring talented people. And there are no barriers to anyone getting raw materials or production and research tools. Finally, there are no product barriers; all new products are available to everybody.

Now, there is the hurdle of experience – the learning curve – attracting talent and building an effective team. Although it's not an easy business to enter, there are no barriers. The IC industry is almost the textbook case of a freely competitive industry, which means customers must benefit.

Why should anybody want to enter this industry? There is one reason – to make low volume specials for themselves. But, others continuously enter the industry. Why? To answer this paradox, let's look at two points of view. First, "Can people who enter make any money?" Only a handful of companies have made a decent return on investment and very few have done extremely well. From the industry's beginning over 15 years ago, it not only does not have a positive retained earnings, it is cyclical, chews up people, prevents innovators from keeping special knowledge for very long, and there are risks inherent in high technology change.

As for the second point of view, "Is there a *need* for system companies to make their own volume ICs?" Or, for that matter, we may ask, "Is there a *need* for national governments to have their own IC industry?"

As we saw earlier, it is truly an open industry. There are many suppliers, many products (at attractive prices, delivery and quality). No new products have been withheld from customers, and in more than a few cases the the IC technology has *led* users (as shown by IC companies making finished products). And, as a generalization, ICs are only about 5% of a system company's total costs.

A common sense economic rationale says no one should *want* to get in. Why do they? At a meeting of the Semiconductor Equipment and Materials Institute awhile back, I addressed "The Structure of the IC Industry in 1985," and in it I attempted to answer that question. The answer to the apparent paradox is a psychological rationale that pushes people to get in. We will look at this psychological rationale in greater detail But, before we can do this, we need to carefully analyze the stages that the IC industry went through to see where it's going and what this means.

The years 1965 - 1975 gathered the elements of success. This was the period when marrying the process. production and applications was the key to success. In the mainstream, there were three successive developments: DTL in SSI for the military, TTL in SSI/MSI for EDP and MOS in LSI for memory. Since the learning curve required very large volume to be competitive, six major companies emerged – all USA based-dominated because large volume applications were there.

But there were many opportunities to the right and to the left of the mainstream. Some were: ECL for large computers, power circuits for audio, P MOS for calculators, C MOS for watches, N MOS for microprocessors. This stage was the Gold Rush era, with many entrants, ruinous competition and few successful victors. In this era, technology was believed more important than management.

Exploiting the elements of success, the stage we are now in (1975 - 1985), will see technology change become more evolutionary than revolutionary. Exploiting the elements of success will be the key. There will be broad classes of process technology with heavy capital investment – such processes as MOS and bipolar with advanced optical and electron beam lithography. Design times will shrink and product introduction will be more timely. Good customer interaction will exist through understanding of applications. Another event will occur: complex organizations will be handled with emphasis on research and development, strategic planning, organization development and teamwork.

Part 2 will appear in the April Viewpoint and will cover the impact of foreign manufacturers, as well as predicting the overall future of the maturing IC industry over the next 15 years.

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