MAY 1977

digital design

the magazine of digital systems

NCC Product Preview

magnetic bubble memories

SPECIAL REPORT

past · present · future

Introducing push-button microprocessor system debugging.

HP's 1611A Logic State Analyzer ... Dedicated to all 8080 or 6800 based systems.*

View program flow in mnemonics. *With CRT data and addresses selectable in either hexadecimal or octal formats and external lines in 1's and 0's.*

Maintain testing control. *LED indicators show status at all times. You can monitor system operation at normal speed or stop the microprocessor and give control to the 1611A for single or multiple keyed steps.*

Enter data quickly and easily. *The hexadecimal keyboard makes trigger and qualifier data entry as easy as operating a calculator. And the CRT display gives you a quick visual check on your entries.*

Choose your display. *Either mnemonic or absolute (op codes). Roll the display to view any 16-line slice of the 64-byte memory.*

Pinpoint virtually any specific event. *Trigger on address, data, or external signals... or on any combination of the three. You can also qualify the trigger by bracketing the address and opting to trigger on the nth occurrence of the trigger word. TRIGGER ENABLE and DISABLE keys act as arm and disarm circuits providing unparalleled pinpointing flexibility.*

Move the display window. *Delay up to 65,472 qualified clocks or memory transactions from the trigger word. Or, pre-trigger to see up to 63 bytes leading up to the trigger word (negative time).*

Obtain program and timing data. *Qualify the display with TRACE TRIGGER and see only those bytes that match your trigger inputs . . . all write instructions, for example. Press COUNT TRIGGERS and the 1611A displays the number of trigger occurrences between the TRIGGER ENABLE and TRIGGER DISABLE entries. Push TIME INTERVAL and you get a display of actual elapsed time between selected points in your program on your hardware.*

The 1611A should be on hand when you start up your microprocessor-based system. Imagine the time you'll save with push-button operation and an unparalleled view of your system's operation; viewing things dynamically that you never could see before. And there's more . . . self test; trigger outputs to drive external equipment; error messages to warn of improper operation or setup; and the choice of two initial "μP personality modules" that let you tailor the 1611A to either 8080 or 6800 based systems.

Let HP's 1611A, priced at $5,000**, help you speed development, production-line testing or service. Ask your local HP field engineer for all the details. Ask him about HP's digital seminars too. He can tell you when one will be held in your area and how you can attend.

*and more modules for other microprocessors to come.
**Domestic U.S.A. price only.

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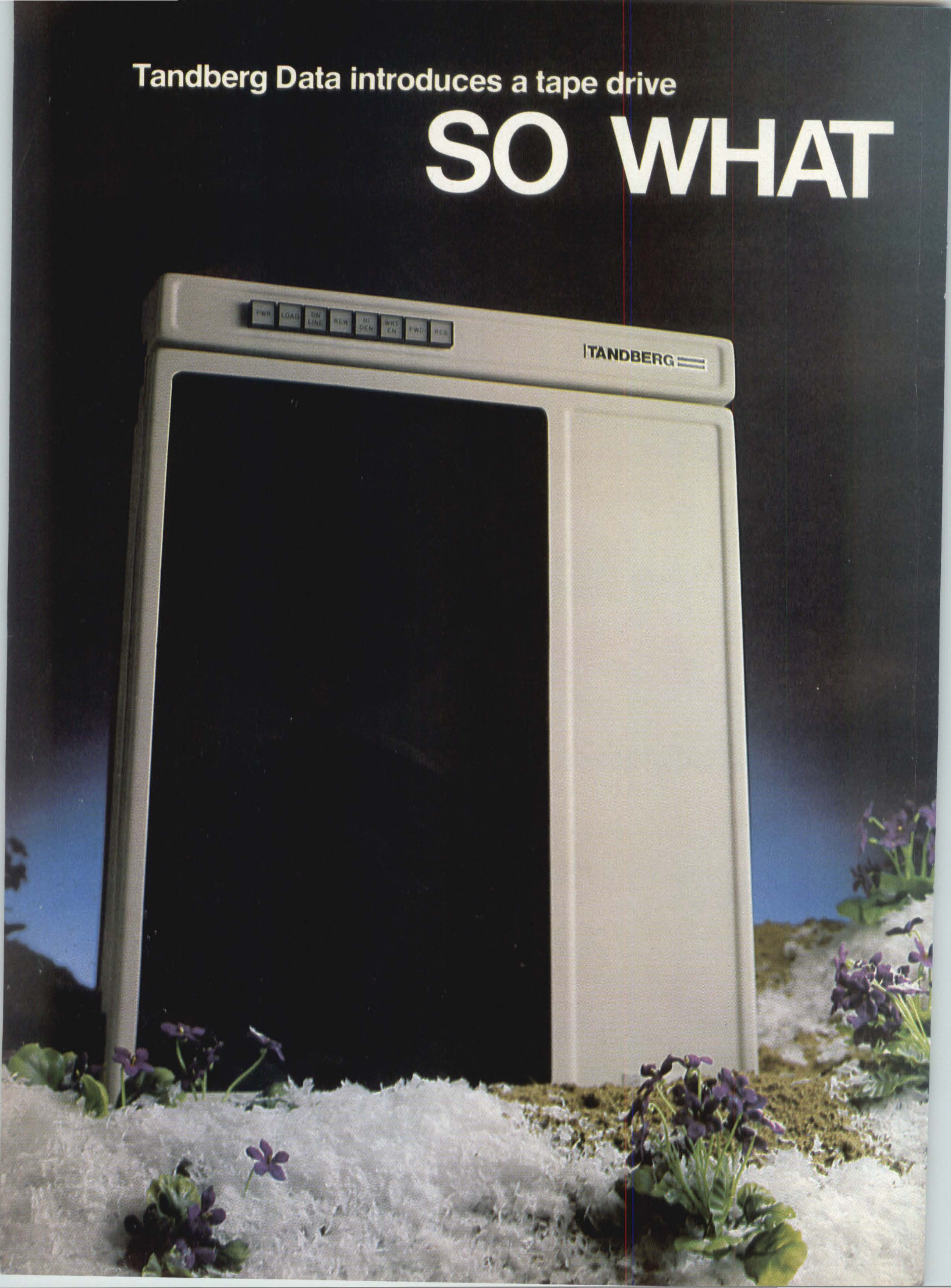
086/15

CIRCLE 1


Tandberg Data introduces a tape drive
SO WHAT
TANDBERG

ELSE IS NEW?

Performance. On an absolutely new level.

With the name Tandberg you expect top performance. And innovation. And being a little ahead of the competition in certain fresh and subtle ways. Ditto our new TDI 1050 Synchronous Tape Transport.

When you're a Johnny-Come-Lately with a product line you *better* try harder.

We did!

Your benefit? Greater reliability, maintainability, and programability as a result of our microprocessor-based control logic. With its optional *internal* formatter, the 10½-inch-reel TDI 1050 makes your interfacing task a whole lot easier, giving unprecedented flexibility and performance when controlling the reading and writing of data.

With Tandberg's dual-format tape drive, you get both 1600 cpi PE and 800 cpi NRZI at speeds of 12.5 to 45 ips, with rewind speed of 200 ips. And there's no need for customer redesign with the industry-wide compatibility of our interface.

For those who'd like multiple-drive capability in their system, our interface enables you to hook up *four* drives without the need for an outside power source.

Not only is the TDI 1050 less costly at the outset, but its built-in microprocessor is likely to reduce your operating costs. Its attractive design is another appealing plus for systems builders.

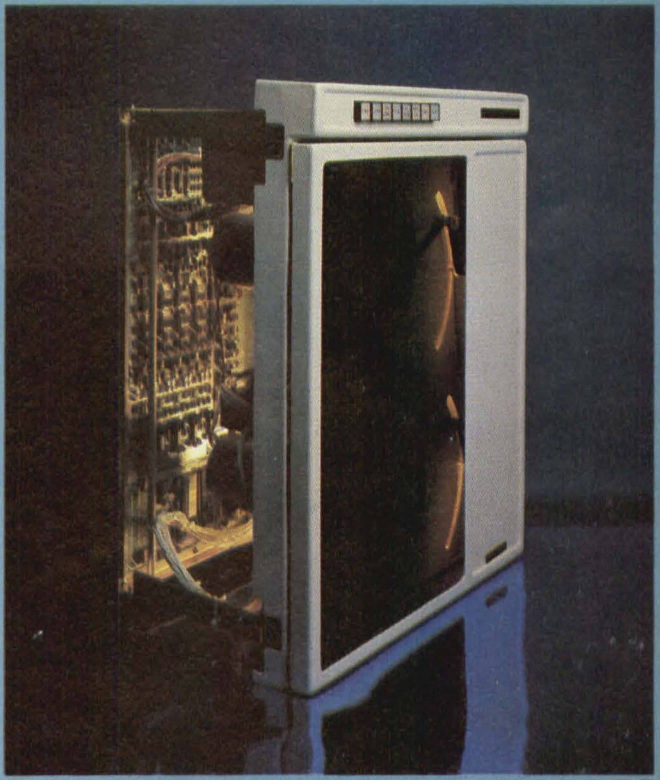
A few other goodies are our 5,000-hour MTBF, a dual ceramic-blade tape cleaner, and our proven microprocessor control system. A choice of 7 or 9 track. And IBM geometry provides minimal dynamic skew. Also, a fully documented maintenance manual with all the data and schematics necessary for easy and economical upkeep.

Ensuring you get the performance we specified for our drive, we put each unit through an exacting series of computer tests and burn-in, far tougher than any challenges it's likely to encounter on the job.

Just another tape drive? Yes and no. The task it performs has been around a while. A lot of horses ran a mile and a quarter and then along came Secretariat. Refinements count a lot, regardless of the track. Check out the TDI 1050. It'll change your ideas about what a tape transport can do.

The best job yet at less cost. Why not clip and mail our coupon and let us prove it.

Tandberg Data Inc.
4060 Morena Blvd.
San Diego, California 92117
Telephone (714) 270-3990



Mr. Peter A. Gilbody, Vice President, Tandberg Data Inc.
4060 Morena Blvd., San Diego, CA 92117

I'd like to know more about the NEW TDI 1050 Synchronous Tape Transport from Tandberg Data. Please send me the TDI 1050 data sheet ☐ and have a Tandberg engineer give me a call to discuss my needs ☐.

Name ________ Position ________

Company ________

Address ________

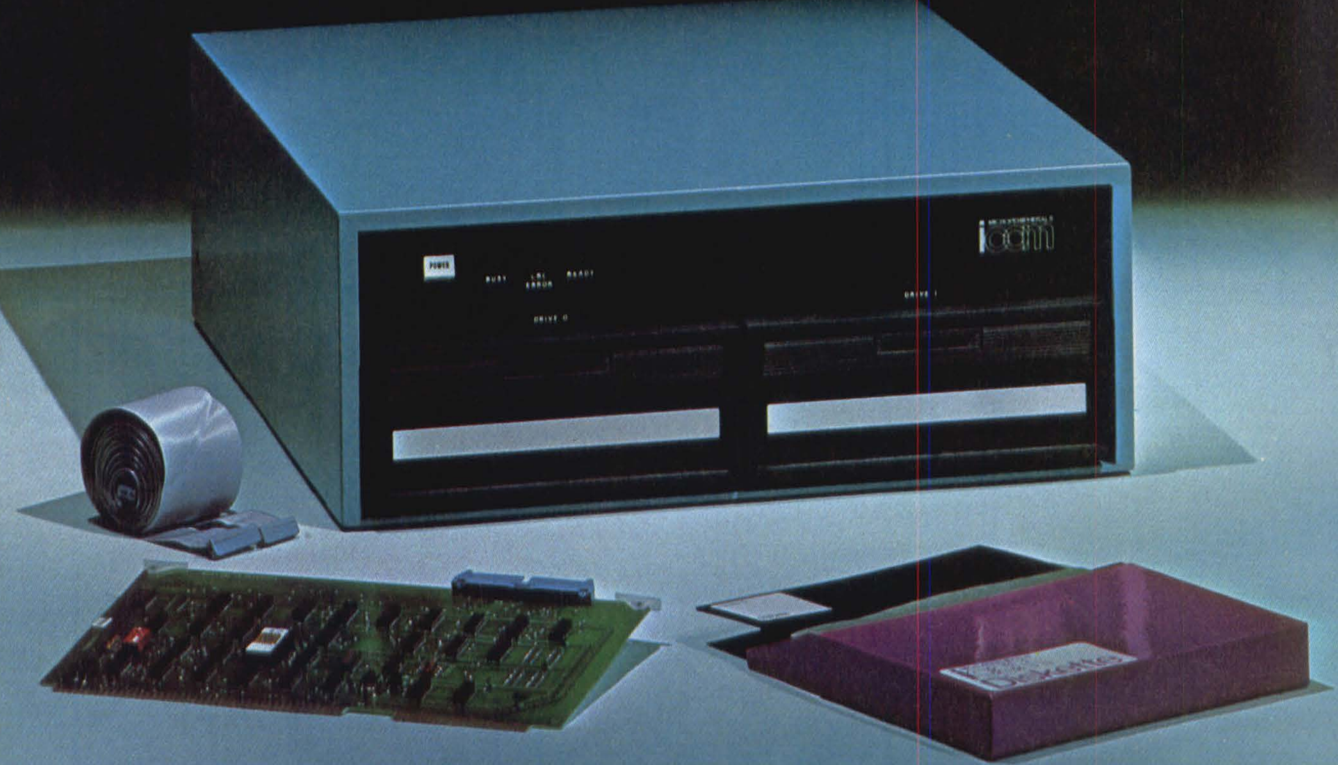
City ________ State ________ Zip ________

Phone ________

Computer type ________

TANDBERG

Save $650 on iCOM's New Dual Floppy Disk System.



At the regular price of $3,300, our new dual floppy is a great buy. It's priced less than competitive models, with features found on no other machine.

At the special $2,650* single quantity price, it's a super value.

Why the low introductory price?

Quite frankly, to make your buying decision easy. We're betting you'll design the iCOM®dual floppy into your system. Many of the largest companies have. And by the way, our OEM quantity prices are right, too. Even more savings.

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The $2,650 price includes the iCOM Dual Floppy and your choice of interface to any of these microcomputers: Intellec 8, Intel SBC-80/10 or 80/20, Intellec-800 or Motorola's EXORciser. You also get our powerful FDOS-II development software with macro assembler and string text editor. And for only $50 more, our new Disk BASIC-M is available for most models.

Another savings

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digital design

Volume 7 Number 5 May 1977

FEATURES

Feature of the Month

DEPARTMENTS

Published monthly by Benwill Publishing Corp., 167 Corey Rd., Brookline, MA 02146. Controlled Circulation postage paid at Long Prairie, MN.

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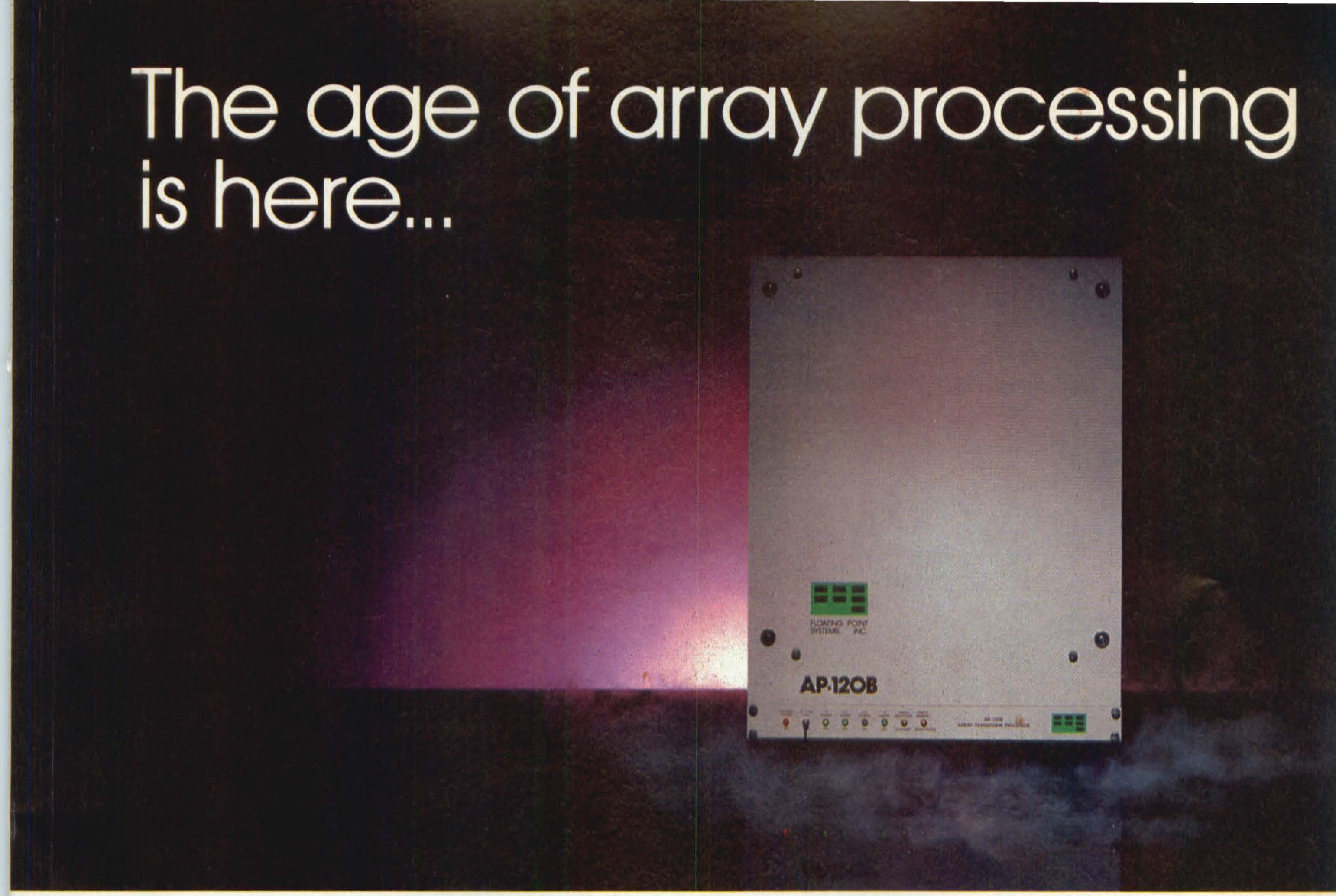
◀ CIRCLE 7

CIRCLE 8 ▶

The age of array processing is here...



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FAST: 167 nanosecond multiply/add...2.7 millisecond 1024 FFT. Throughput 100 to 200 times greater than most computers.

EASY PROGRAMMING: Over 95 routines callable from FORTRAN. Its symbolic cross-assembler and simulator/debugger helps you create new routines.

COMPATIBLE: Interfaced to all popular computers and their operating systems. A flexible format converter translates data to and from the host CPU. And a high speed DMA port is available to use with other peripherals.

CAPACITY: 167 or 333 nanosecond 38-bit memories from 8K to 1 megaword.

PRECISION: 38-bit floating-point arithmetic, **normalized and convergently rounded,** produces eight decimal digit accuracy, not just six.

RELIABLE: Goes where your CPU goes—computer room, lab, or in the field. More than two years of operation logged.

ECONOMY: A complete system less than $40K. That's a small fraction of what you must spend for comparable computing power.

Discover how the AP-120B has brought **The Age of Array Processing.** Hundreds are in use. Send for our data pack and find out what the AP-120B can do for you.

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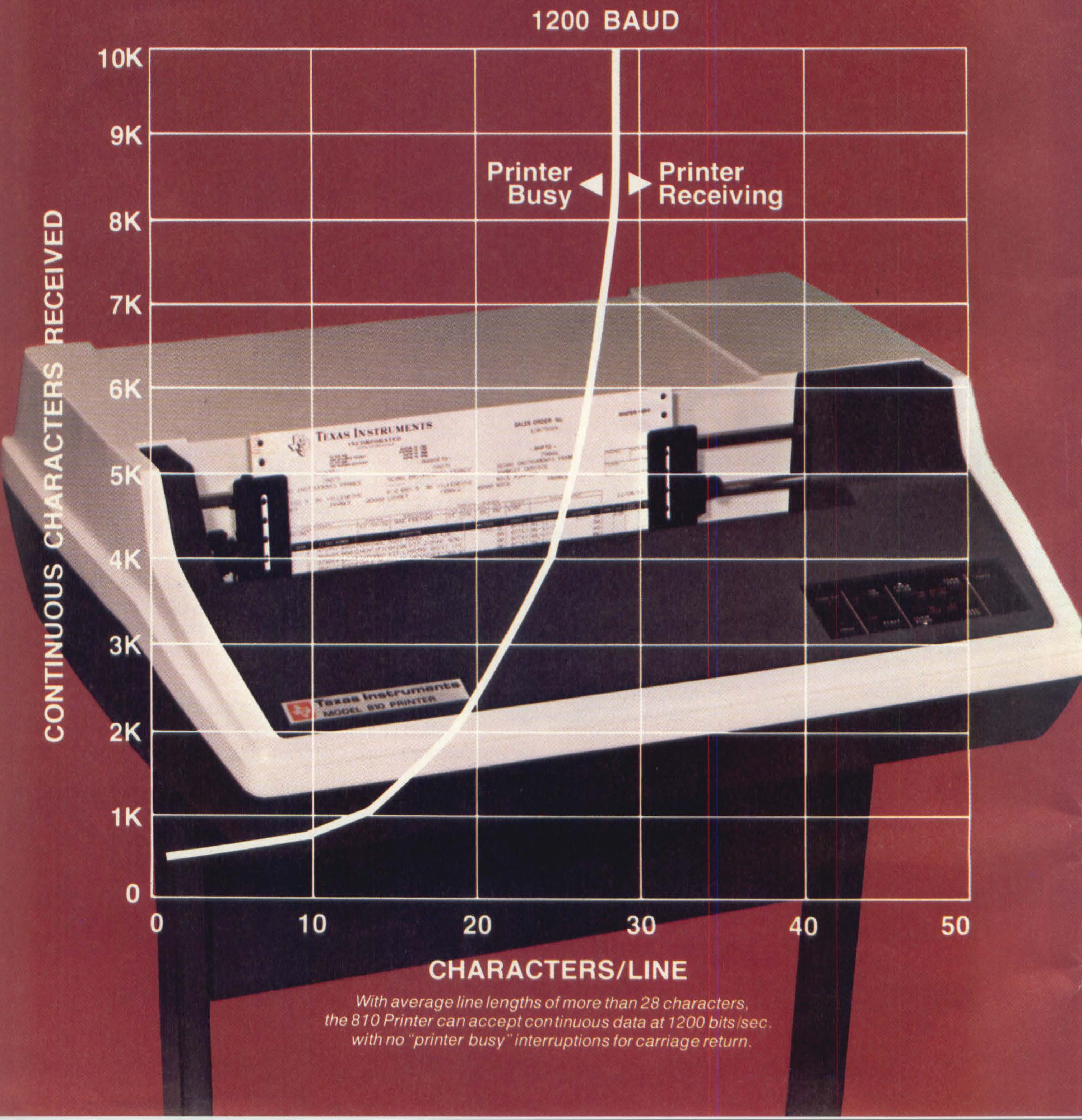
City________ State________ Zip________
My Computer System is ________ My application is ________

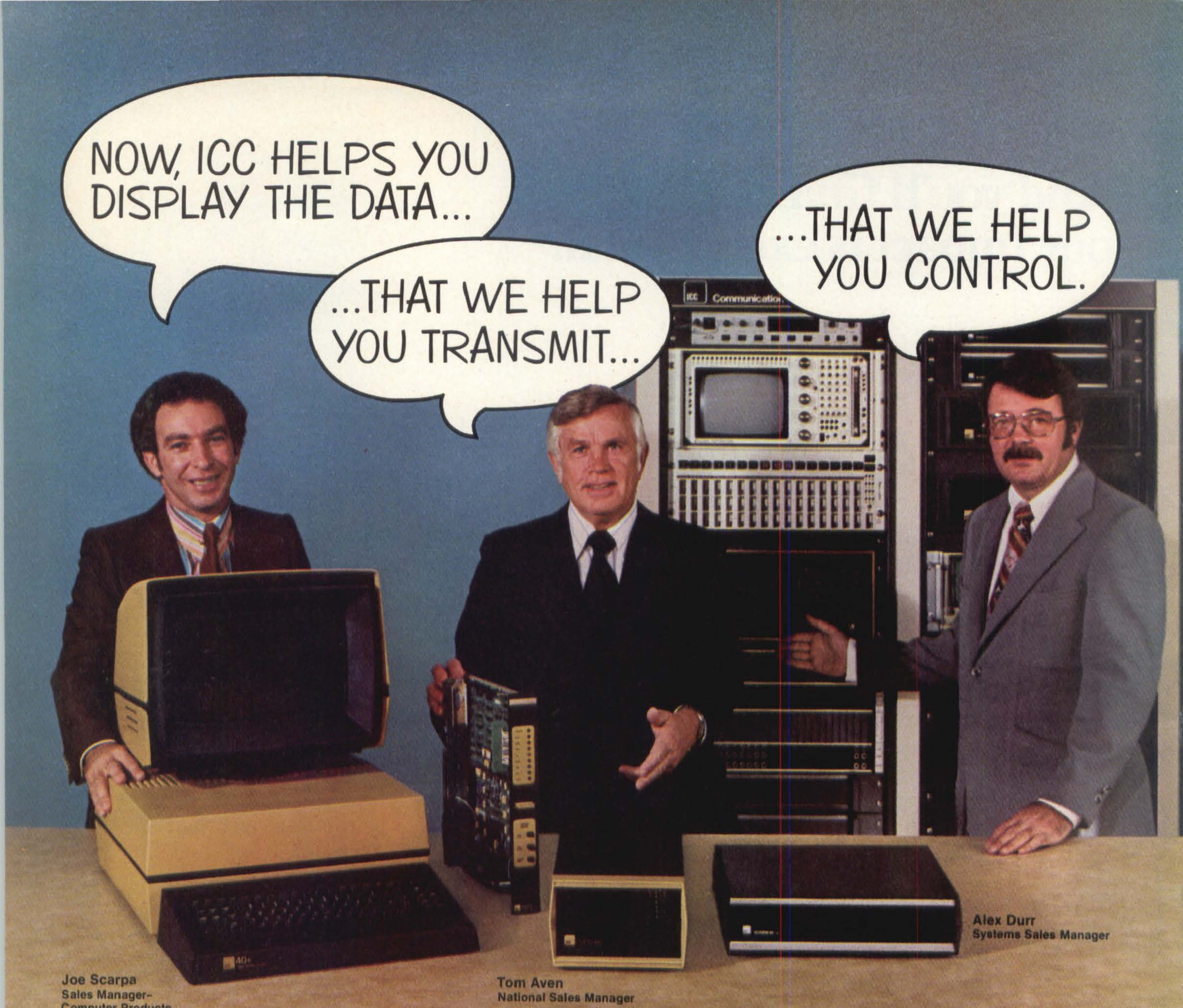
M77 5 **See us at NCC Booth 1571-73**

New from TI.

Plot the performance of the Model 810 Printer against any other printer on the market.



With average line lengths of more than 28 characters, the 810 Printer can accept continuous data at 1200 bits/sec. with no "printer busy" interruptions for carriage return.



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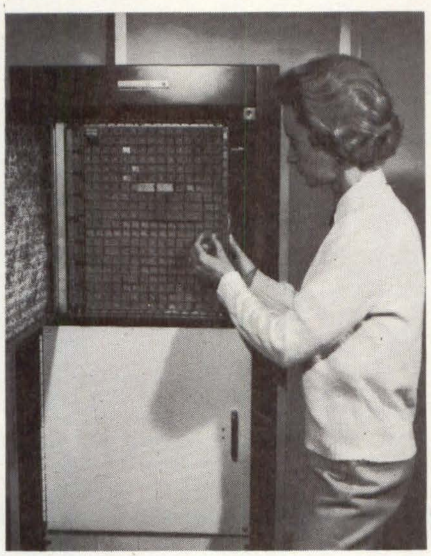
letters

technology transfer dep't: rediscovery division

• *Dear Editor:* We read the design note on Hinged Frames (Designers Notebook) in your April issue with considerable interest. We agree with Mr. Naess that the packaging method illustrated in his article has all the advantages he claims. In fact, we can attest to this from first-hand experience, because the technique was invented here at Lockheed about 1964, and has been used in several forms since then.

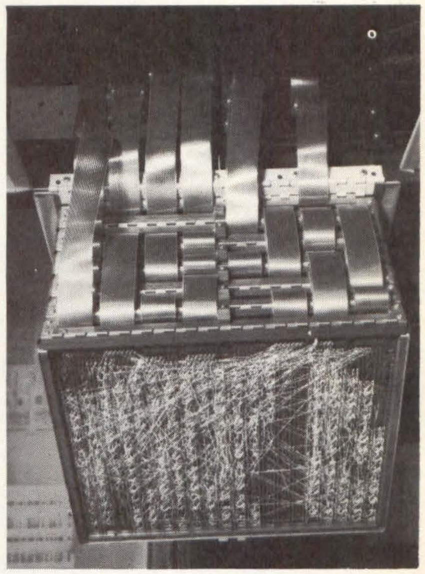
Enclosed are some early photos showing prototype equipment that used the book/page packaging technique. We used a single large motherboard with a wrapped wire backplane interconnect. The photos show equipment that was designed before the days of dual-in-line integrated circuits. We mounted IC's (packaged in TO-99 type cans) on small plug-in wafers and plugged these into connectors on the



motherboard. Since then, motherboards have been designed and built with receptacles that accept dual-in-line integrated circuits.

One photo shows the page-to-page cabling technique. These were self coiling tape cables. Not only did they solve the cable retracting problem, but they also cancelled most of their own line inductance by virtue of the fact that they doubled back on themselves as they coiled up.

Lockheed has built many successful systems with this package, and we have found it to be exceptionally easy to build, to check out and to maintain. Extensive details on the technique



were presented in a prize-winning paper given by the author at NEPCON (New York) in June of 1966. The Title of that paper is, "TEC-2, A Packaging Scheme for Special Purpose Data Processors Using Integrated Circuits". It appears in the proceedings for that conference.

R. JOSEPH RANSIL
Staff Engineer
Lockheed Missiles & Space Co.
P.O. Box 504
Sunnyvale, CA 94088

got a 1200 baud coupler?

• After I read "Update: Modems" (October) a question was raised in my mind. Are there acoustic coupler modems available on the market for speeds greater than 300 baud, preferably around 1200 baud? I would appreciate it if you would send me a list of manufacturers that might make such high-speed acoustic couplers . . . I am currently using a CRT at 150 baud; the machine is capable of much greater speed, and I would prefer to utilize that potential.

SCOTT T. KELLOGG
University of Hawaii at Manoa
Dept. of Microbiology
Snyder Hall 207
2538 The Mall
Honolulu, HI 96822

Editor's note: Can anyone help Mr. Kellogg?

If you really compare design, specs, component quality, construction, price, delivery and guarantees, these are the power supplies you'll buy!

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U. L. Recognized glass-epoxy circuit board.

Universal application: 115/230 VAC ±10% 47-440 Hz (no derating for operation on 50 Hz).

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IC-zener protected against overvoltage.

Integrated circuit regulation and integrated Darlington TO—3 output stage provide much simpler circuitry, higher reliability

No overshoot on turn-on turn-off, or power failure.

Automatic foldback current limiting overload and short circuit protection

TO—3 can is mounted directly to frame to minimize wiring

Electrostatically shielded transformers reduce noise better than 4:1.

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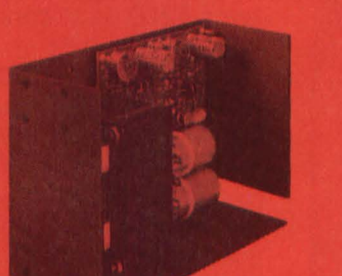
New Multiple Output Microprocessor Power Supplies.



DUAL OUTPUT MICROPROCESSOR SERIES

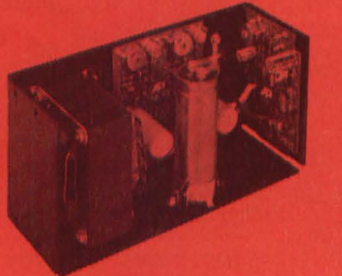
U. L. Recognized. (File No. E58512)

MODEL NUMBER	RATING		QUANTITY PRICES						
	Vdc	Amps	1-4	5-9	10-24	25-49	50-99	100-249	250-499
DAPS 5.8	±5	0.8	43.00	41.95	40.70	39.80	38.00	36.80	33.00
DAPS 9-12.5	±9 to 12	0.5	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 12-.75	±12	0.75	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 15-.60	±15	0.60	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 5112.5	+5 −12	1.0 0.5	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 12-1.5	±12	1.5	59.00	57.60	55.90	53.30	50.65	47.60	43.80
DAPS 15-1.3	±15	1.3	59.00	57.60	55.90	53.30	50.65	47.60	43.80
DAPS 53121.5	+5 −12	3.0 1.5	59.00	57.60	55.90	53.30	50.65	47.60	43.80

REGULATION: ±0.05% Line, ±0.1% Load. RIPPLE (PK/PK) 3mV.

DIMENSIONS: (Small unit) 4"x2.75"x4.87" (Large Unit) 7"x3.40"x4.87"

REQUEST BULLETIN DAPS - 976



TRIPLE OUTPUT "TAPS" MICROPROCESSOR/GENERAL PURPOSE SERIES

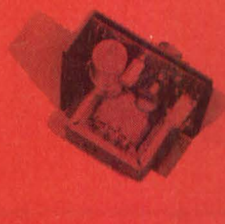
MODEL NUMBER	RATING		QUANTITY PRICES						
	Vdc	Amps	1-4	5-9	10-24	25-49	50-99	100-249	250-499
TAPS 1	5V ±9 - 12*	4.0 0.5	94.15	91.85	89.20	85.05	80.85	75.90	71.00
TAPS 2*	5V ±9 - 12*	6.0 1.0	107.00	104.60	101.60	96.85	92.10	89.00	87.50
TAPS 3	5V ±9 - 12*	9.0 1.5	137.00	134.00	129.80	127.80	125.00	123.75	113.85
TAPS 4	5V ±9 - 12*	12.0 3.0	163.00	159.00	154.45	151.50	149.00	148.00	147.00

* Also available with ±12-15V output. Specify if desired.

REGULATION: ±0.1% Line, ±0.1% Load. RIPPLE (PK/PK) 5mV

DIMENSIONS: 8.62"x3.65"x4.87" to 15"x4.5"x4.87". REQUEST BULLETIN TAPS - 377

Single Output Microcomputer Power Supplies.

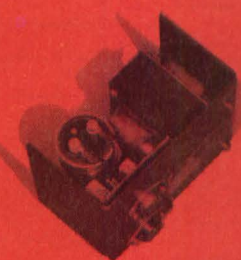


15 TO 24 WATT "RED BARON" SERIES. SINGLE OUTPUT

* U. L. Recognized (File No. E58512)

MODEL NUMBER	RATING		REGULATION		RIPPLE (PK/PK)	OVP MODEL SUFFIX	PRICES-ALL MODELS		
	Vdc	Amps	Line	Load			QTY	POWER SUPPLY	OVP UNIT
APS 5-3*	5	3	±0.05%	±0.1%	3mV	OV1-53	1-4	34.00	7.00
APS 6-2.5	6	2.5	±0.05%	±0.1%	3mV	OV1-63	5-9	33.15	6.90
APS 12-1.6*	12	1.6	±0.05%	±0.1%	3mV	OV1-122	10-24	32.20	6.70
APS 15-1.5*	15	1.5	±0.05%	±0.1%	3mV	OV1-152	25-49	30.70	6.40
APS 20-1	20	1.0	±0.05%	±0.1%	5mV	OV1-201	50-99	29.20	6.05
APS 24-1*	24	1.0	±0.05%	±0.1%	5mV	OV1-241	100-249	27.00	5.70
APS 28-0.8*	28	0.8	±0.05%	±0.1%	5mV	OV1-281	250-499	25.20	5.25

DIMENSIONS: 4" x 2.75" x 4.87 REQUEST BULLETIN APS-277



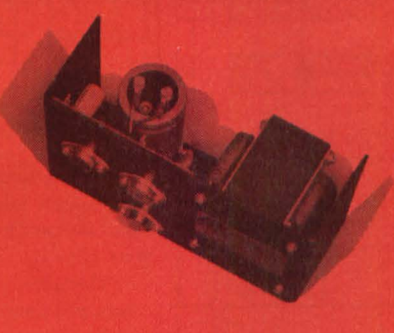
30 TO 60 WATT "GREEN HORNET" SERIES. SINGLE OUTPUT

† U. L. Recognized (File No. E58512)

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 48-1	ALL OTHERS	
APS 5-6†	5	6.0	±0.05%	±0.1%	OV2-56	1-4	68.00	55.00	15.00
APS 6-5	6	5.0	±0.05%	±0.1%	OV2-65	5-9	66.70	53.65	14.85
APS 12-4†	12	4.0	±0.05%	±0.1%	OV2-124	10-24	64.75	52.10	14.40
APS 15-3†	15	3.0	±0.05%	±0.1%	OV2-153	25-49	61.75	49.65	13.75
APS 20-2.4*	20	2.4	±0.05%	±0.1%	OV2-203	50-99	58.75	47.25	13.05
APS 24-2.2*†	24	2.2	±0.05%	±0.1%	OV2-245	100-249	55.15	44.35	12.25
APS 28-2 *†	28	2.0	±0.05%	±0.1%	OV2-284	250-499	50.75	42.00	11.30
APS 48-1 *	48	1.0	±0.05%	±0.1%	OV2-481	500-999	49.60	40.00	11.05

* RIPPLE: (PK/PK) 5mV. All others 3mV.

DIMENSIONS: 5.62"x3.40"x4.87" REQUEST BULLETIN APS-277



50 TO 120 WATT "BLACK BEAUTY" SERIES. SINGLE OUTPUT

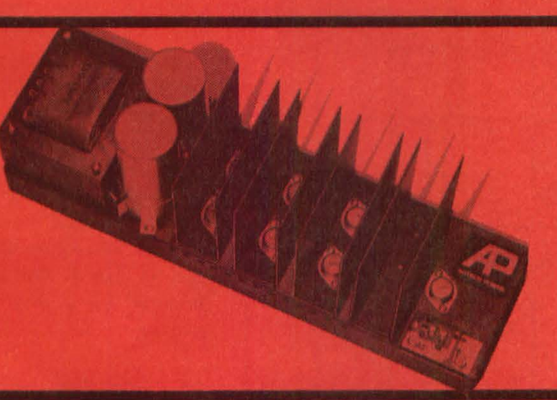
5 Vdc @ 9 Amps to 28 Vdc @ 4 Amps. U. L. Recognized. (File No. E58512) *

MODEL NUMBER	RATING		OVP MODEL SUFFIX	POWER SUPPLY PRICES					OVP PRICES
	Vdc	Amps		QTY.	APS 5-9	APS 5-12	APS 5-18	ALL OTHERS	
APS 5-9	5	9	OV2-510	1-4	71.00	85.00	108.00	75.20	15.00
APS 5-10*	5	10	OV2-510	5-9	68.75	82.95	104.50	73.40	14.85
APS 5-12	5	12	OV2-512	10-24	66.74	80.55	101.45	71.30	14.40
APS 5-18	5	18	OV2-518	25-49	63.90	76.80	96.70	67.95	13.75
APS 12-7*	12	7	OV2-127	50-99	61.05	73.00	91.95	64.60	13.05
APS 15-6*	15	6	OV2-156	100-249	57.30	68.55	86.35	60.65	12.25
APS 24-5*	24	5	OV2-245	250-499	52.75	65.00	79.45	55.80	11.30
APS 28-4*	28	4	OV2-284	500-999	51.60	57.90	77.70	54.60	11.05

REGULATION: Line ±0.05% Load ±0.1%. RIPPLE (PK/PK) 3mV on 5, 12, 15V models. 5mV on 24, 28V.

DIMENSIONS: 9"x3.65"x4.87"

APS 5-18 DIMENSIONS: 14"x3.65"x4.87" REQUEST BULLETIN APS-277



125 TO 250 WATT "BLUE MAX" SERIES. SINGLE OUTPUT

5 Vdc @ 25 Amps to 28 Vdc @ 9 Amps.

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 5-30	ALL OTHERS	
APS 5-25	5	25	±0.05%	±0.0.1%	OV3-525	1-4	163.00	158.00	25.00
APS 5-30	5	30	±0.05%	±0.0.1%	OV3-530	5-9	159.25	154.40	24.50
APS 6-22	6	22	±0.05%	±0.0.1%	OV3-622	10-24	154.65	149.95	24.25
APS 12-17	12	17	±0.05%	±0.0.1%	OV3-1217	25-49	147.45	142.95	23.15
APS 15-15	15	15	±0.05%	±0.0.1%	OV3-1515	50-99	140.20	135.90	22.00
APS 20-11	20	11	±0.05%	±0.0.1%	OV3-2011	100-249	131.65	127.60	20.65
APS 24-10	24	10	±0.05%	±0.0.1%	OV3-2410	250-499	121.10	117.40	19.00
APS 28-9	28	9	±0.05%	±0.0.1%	OV3-289	500-999	118.50	114.85	18.60

RIPPLE (PK/PK): 3mV on 5,6,12,15V models. 5mV on 20,24,28V models.

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CIRCLE 20

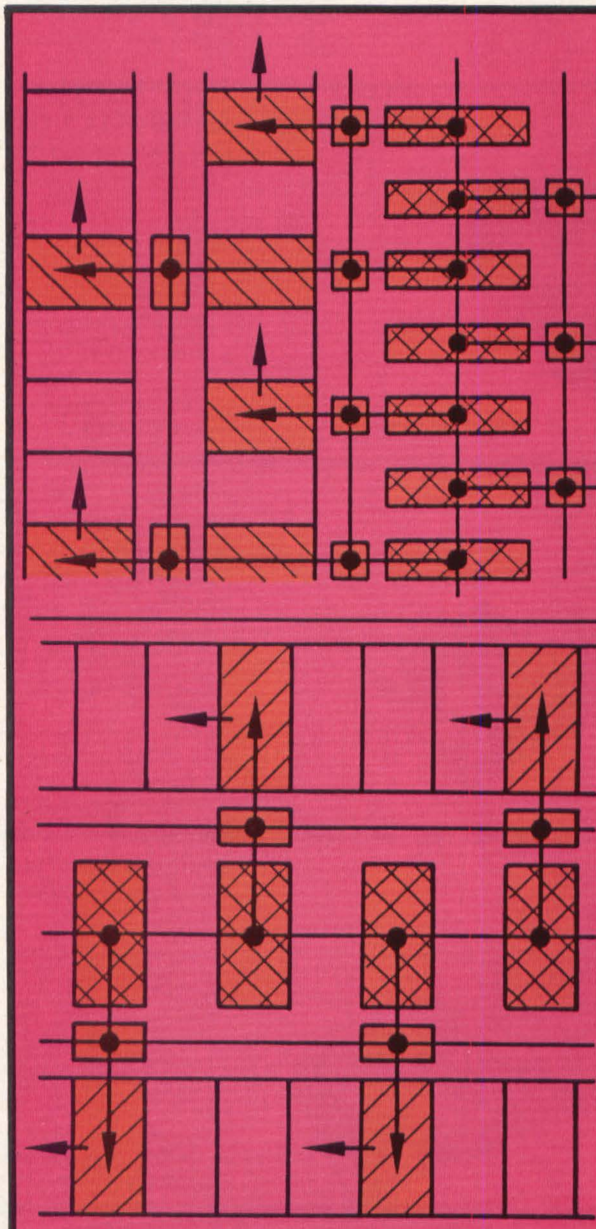
Semiconductor circuits scan pictures

Semiconductor circuits with light-sensitive sensor elements are already capable of scanning originals, element by element, one line after the other. Readout registers convey the information scanned by the snesor array as electrical charges to an electronic evaluator circuit. With a new circuit developed in the Siemens Research Laboratories including four registers per sensor array now instead of two, company engineers claim it is possible to double the number of picture elements per line. As a result, they say, a variety of units such as facsimile transmitters and photocopying equipment which reproduce originals far more clearly than before can be built.

The quality of a picture transmission improves as the number of elements a line can be broken down into increases. Transmitting a DIN A4 sized page as 1728 picture elements requires a circuit length of around 25 mm; it is one of the largest semiconductor circuits implemented to date. For reasons of signal accuracy – each shift step in the readout register unfailingly produces a small error – the number of register stages cannot be increased any further.

This circuit developed by Siemens research workers reads out the picture-related charge pattern of a sensor array with four CCD shift registers instead of two. Halving the number of shift steps in the readout register increased the number of picture elements of a sensor circuit to 3000. The four readout registers are arranged in pairs on each side of the sensor array. Each sensor element is assigned a CCD element: on the left-hand side for every 1st and 3rd sensor element, on the right-hand side for every 2nd and 4th sensor element.

During the first readout step, the contents of all sensor elements are transferred to the two inner readout registers. During the second step, the contents of the 1st and 2nd sensor elements only are shifted from the inner to the outer readout registers.

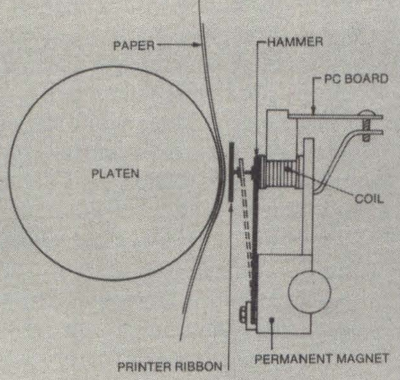


These semiconductor circuits are capable of scanning originals element by element one line after the other. The sensor elements in the center of the top supply picture-related charges which are transferred to the CCD readout registers. Instead of one such register on each side of the sensor array, the circuit concept incorporates a total of four CCD registers arranged in pairs on either side of the array. In this way, the possible number of picture elements can be nearly doubled, improving the quality of the picture.

The third step transports all the information towards the output, where the electronic evaluator circuit scans the charge pattern sequentially.

This circuit concept, says Siemens, has already been tested successfully in the laboratory. In accordance with this concept, the 1728 picture elements required for facsimile transmission can be handled bv a circuit with a length of only 17.5 mm. If the original length of 25 mm is retained, over 2500 picture elements can be read out. This increase in resolution is particularly advantageous for photocopying equipment. Siemens reports, because such a high number of picture elements could so far only be achieved with bulk CCDs which are considerably more complex to manufacture than surface CCDs.

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.



Like the far greater MTBF this elegantly simple mechanism assures.

Downtime frays nerves. It costs money, too. But take heart. You'll see a lot less of it with a Printronix 300. That's assured by its elegantly simple mechanism based on a flat strip of spring steel with a hardened tip, pictured below. Forty-four springs, or hammers, are mounted to a hammer bank. Each is fastened at one end and normally held retracted by a permanent magnet. (See the diagram.) A pulse of current thru a coil at the tip end of the hammer releases it to print a dot. The hammer bank is shuttled horizontally 0.3″, enabling each hammer to cover the space between its tip and the tip of the next one, so that the total field covered is 132 columns. Aside from paper and ribbon feed, that is the only mechanical motion in the printer.

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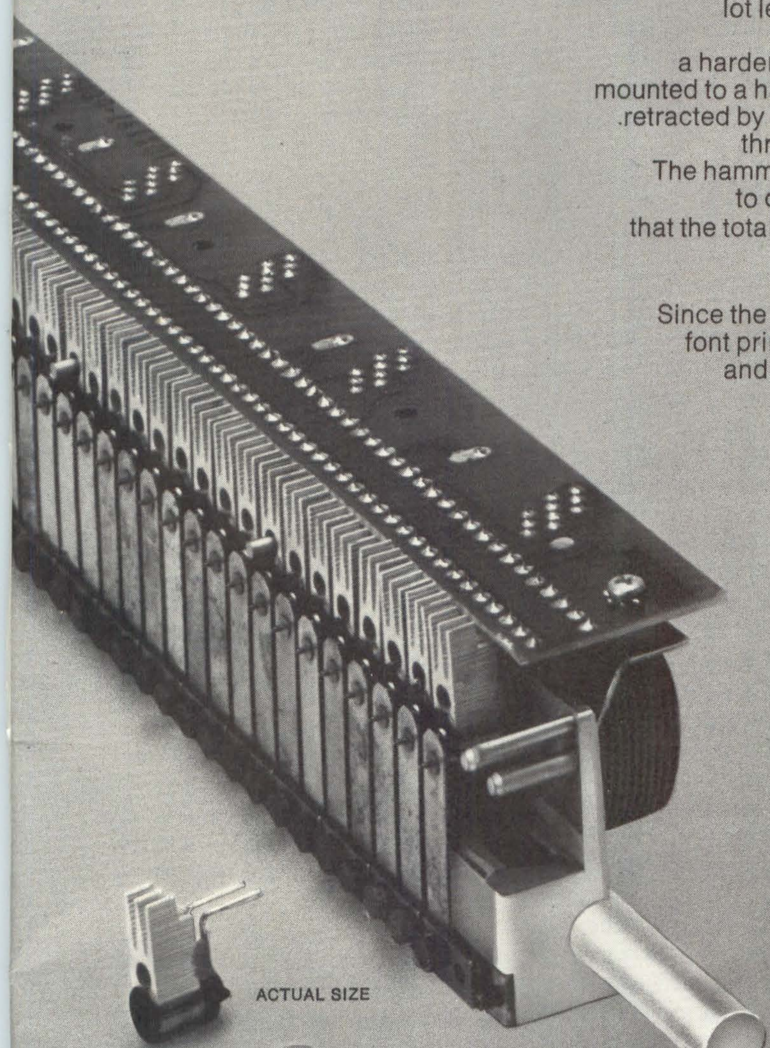


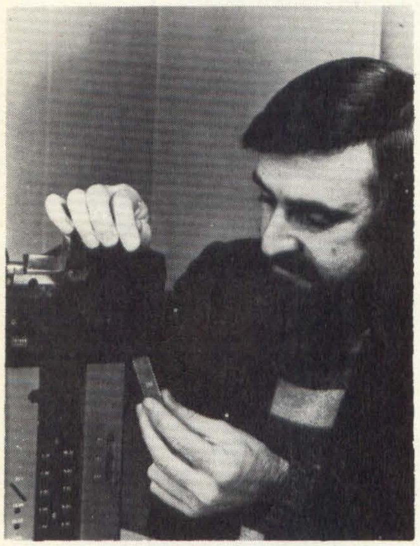
PRINTRONIX 300

It's your best buy!

Custom LSI chip tests for counterfeits in all-electronic coin changer

Replacing the rails, fingers, switches, deflectors, motors, cams, flippers and magnets used in conventional vending-machine coin changers, an all-electronic coin changer incorporates a custom designed LSI chip that lets it accept and dispense any country's currency. Implementing the changer's functions, which include a self-calibration capability to adjust for slight coin variations, would have cost 10 to 100 times more if the changer used standard circuits, claims the equipment's developer.

Fred Heiman, president of Mars Money Systems, Folcroft, PA, adds that standard circuitry couldn't have achieved the firm's design goals in the space the designers had allotted themselves. The system's custom 40-pin LSI chip, manufactured by American Microsystems, Inc. (AMI), Santa Clara, CA, measures 0.194" x 0.198".



Fred Heiman, president of Mars Money Systems, examines his firm's all-electronic coin changer, whose functions are implemented in the custom LSI microcircuit he holds in his hand. The microcircuit tracks the changer's money calculations, determines coin validity and triggers change return.

63 prices. The 3500-transistor, ion-implanted PMOS chip, whose development cost Heiman claims will be borne by the firm's anticipated high-volume use, incorporates a 1-bit microprocessor that keeps track of the coin changer's money calculations and a factory programmed PROM that allows adaptation to any currency. Factory programming also accommodates up to 63 prices ranging from $0.05 to $3.15.

When a customer makes a selection, the coin changer generates a binary-coded signal that represents the selection's price. The chip credits and accumulates the deposited coins, compares the total with the selected item's price and signals the vending machine when the deposits have occurred.

The 40-pin, ion-implanted PMOS chip replaces electromechanical elements that often jam.

If a sensor input tells the chip that some of the coin-return tubes from which the system makes change are empty, the chip calculates whether it can return correct change with available coins. If not, it returns the deposited coins and lights the machine's "exact change" indicator.

Self-calibrating coin validation. Mounted in the changer's coin-passageway walls, three inductive coils output information that the chip uses to accept or reject a coin. Oriented in different directions, the sensors measure the frequency shift associated with a coin to determine the coin's thickness, diameter, composition and embossing depth. The chip then compares this 10- to 100-kHz frequency-shift information with stored tolerances to determine coin validity.

The chip may accept a coin even if one of these three validation outputs is negative. A self-calibration feature allows for slight frequency variations caused by temperature changes; the chip can adjust its tolerances to accommodate the negative validation output.

CT Scanning

by **George King**
Digital Design

LOS ANGELES – Image processing systems change many traditional black and white worlds into ones of brilliant color. Recently, only such esoteric areas as satellite data interpretation and the analysis/enhancement of reconnaissance photos used image processing systems. But now, these systems are moving into other areas of application.

In medicine these systems prove to be powerful diagnostic tools in early detection of tumors. "The addition of color to monochromatic x-ray images is an exciting development and may well prove to be one of the more significant diagnostic advances in recent years," says A. Franklin Turner, M.D., professor of radiology and medicine, University of Southern California School of Medicine.

Adding color to normal monochromatic images improves the viewer's perception of the image, for the eye can distinguish more shades of color than shades of gray. USC's Schools of Medicine and Engineering use a Data General Nova 1200 and image enhancement systems developed by Comtal Corp., Pasadena, CA, in conjunction with computed tomography (CT) or body scanning. Described as the biggest development in diagnostic medicine since Wilhelm Roentgen discovered x-rays in 1895, the CT scanner rotates a low intensity x-ray beam around the body 180° in a transaxial plane. Detectors, placed opposite the beam, monitor and digitally signal the varying degrees to which body tissues absorb radiation. A computer transforms this digital information into a cross-sectional, almost 3-D, image of the body.

This process differs from conventional x-ray units which use stationary x-ray sources to produce flat pictures of the body.

Turner explained that absorption coefficients of various parts of the body – soft tissue, bone, fat and air – differ and are critical elements in analysis. Scan KV levels affect the absorption coefficient. Turner explained that at 40KV, tissue and water are easy to distinguish from bone. However, 150KV make bone and soft tissue difficult to distinguish.

At USC, researchers operate the scanner at various KV levels to take advantage of absorption coefficient variations. The resulting image shows a complete body cross-section that contains added information on relative tissue densities.

"Density is the key element of any x-ray," Turner said. "When a change in density occurs, we know that an abnormality exists. But, we can't always tell the specific nature of the abnormality from a monochromatic x-ray image."

Researchers at USC have been able

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CIRCLE 22

to identify absorption coefficients for specific tumors based on data compiled through CT scanning.

Scanning

CT scanners on today's market measure minute changes in density within the human body; yet they only expose patients to low-level radiation doses. For example, a 20-second scan usually produces a radiation dose lower than a standard x-ray machine does during a typical upper gastrointestinal series.

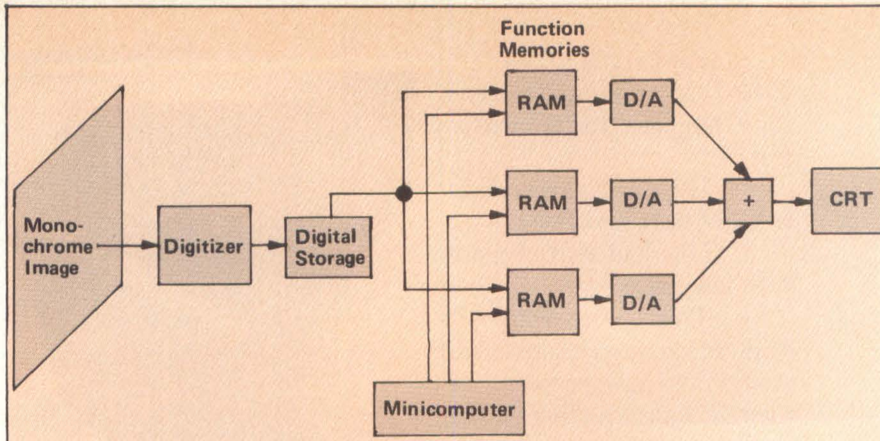
During a scan, radiologists assign values to elements present in the body. They may assign water a value of 0 and bone a value of +1000. Based on these comparative values, the CT scanner digitally records density variations as it scans the body. For example, a reading of +20 would indicate to the radiologist the presence of liquid blood. A reading of +30 would indicate clotted blood.

Now add color to the image. Then, with +20 assigned to the primary color red and +30 to a darker color, liquid blood appears different than clotted blood, which shows up as a darker shade of red.

Color Processing

The Comtal image processing system used at USC first stores the digital data provided by the CT scanner in an 8-million bit solid state memory called refresh storage. The system then retrieves image data from this storage and processes the information through two independent, sequential processors – a function and a pseudocolor processor – before it sends it to a high resolution CRT display. Equipped with separate memories, function and pseudocolor processors perform analysis and enhancement algorithms on the refresh storage data without changing or destroying the original information.

The system sends display data as individual picture elements (pixels), each of which contains digital representations of the full color data range. Comtal systems provide up to 1024 pixels per line horizontal resolution on up to 1024 lines of display. Additionally, 256 different brightness levels per pixel produce a bright, flicker-free display, with more than 4000 different color combi-



In this pseudocolor display system, the digital storage unit contains the gray-tone image in pixels. Each gray pixel reads from storage then passes through RAM function memories to be transformed into a color pixel. As these digital pixels go through the D/As, they become video signals for the color CRT.

Everyone totally happy with their head-per-track discs may go on to the next page.

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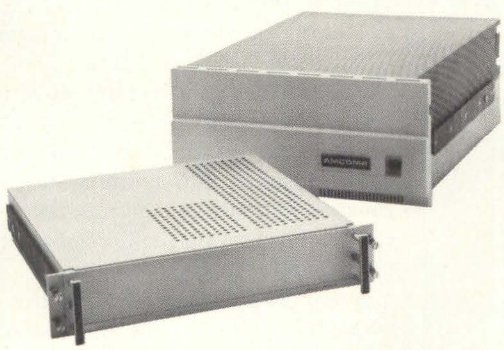

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Now, aren't you happy you didn't turn the page?

AMCOMP

CIRCLE 24

nations possible.

The system colors the image in this way. The digital storage contains the gray-tone image for pseudocoloring. Each pixel is read from the digital storage and then passed to RAM function memories. A rapid table look-up generates the pixel according to preprogrammed pseudocolor mappings. The new digital pixel values then go to D/A circuits and become video signals for the tricolor CRT display. A minicomputer or microprocessor reloads the function memories to allow a rapid change from one pseudocolor scheme to another. USC combines a DG Nova 1200 with the Comtal image processing system.

Comtal systems make permanent records of color images possible. Because of the high resolution display and the pixel density, photographs provide high quality reproduction.

Systems can also provide graphic overlays for image identification. Graphics overlay data, stored in the refresh memory, are presented to the display simultaneously with the retrieval and display of image data. The graphics overlay is a matrix of one-bit per pixel data with the same spatial resolution as the image data. In addition to providing such simple information as patient name and date of scan, the graphics overlay can outline major organs within the body.

Zooming capabilities allow systems to magnify a selected portion of images for study. Systems can also minify images to present multiple pictures simultaneously for comparative study. Replication or linear interpolation decreases or increases image size by any integer factor between two and seven.

Pseudocolor enhances images with poor contrast and only a moderate amount of detail. Because of their usual contrast and resolution limitations, medical and industrial radiographic images can be enhanced by the Comtal system's pseudocolor processing.

Image processing systems are not necessarily limited to the more advanced CT units. Standard x-ray machines can be converted to digital data and enhanced with color.

Turner sees a number of future uses for this technique. According to the doctor, radiologists use radioactive isotopes to examine certain organs, but radioactivity can cause unpleasant side effects. A color system would permit use of a nonradioactive organ-specific element, such as a zinc histidine which travels to and collects in the prostate gland, and could enhance the image of the organ.

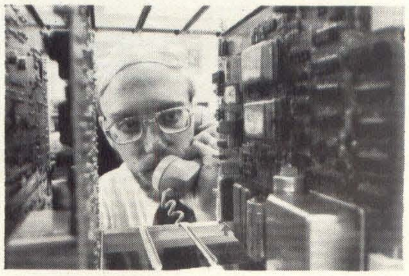
Bubbles debut in phone system announcer

Installed in a Detroit switching office, the Bell System's first application of magnetic-bubble technology stores and announces up to eight prerecorded, 12- or 24-second "call assist" messages. Simultaneously accessing as many as 500 telephones, the message unit replaces a single-message magnetic drum machine and will serve as a test installation for the bubble technology.

Unlike messages stored in the predecessor unit, recordings stored in the 13A message unit don't degrade with repeated use, according to Bell Labs, Murray Hill, NJ, which developed the new machine.

12-second speech packages. Each message in the 13A is stored on one PC board, which houses one or two magnetic-bubble packages. Each package contains four 68, 121-bit bubble chips and can store the equivalent of 12 seconds of digitized speech.

In operation, the machine digitally encodes speech and stores it in the bub-



Two magnetic-bubble packages (arrows) store a 24-second "call assist" message in this experimental message unit. Checked out by Bell Labs engineer Jim Rowley, the unit can store eight such messages, one per 2-package board; each package contains four 68,121-bit bubble chips.

ble devices; a decoder reconstructs a message when needed.

Single-step fabrication. Consisting of well-defined domains in thin crystalline materials, magnetic bubbles can represent digital data and can move under the effect of a rotating magnetic field. They provide non-volatile storage and access in less than 2 ms – slower than semiconductor memories but ten times faster than disk drives.

Each 32-pin bubble memory package in the 13A announcement machine contains four garnet chips; it measures 1.2" x 2.2" x 0.6" and also contains a magnet to generate a uniform field over each chip and two conducting coils to generate a rotating field. A permalloy outer case shields the package from external magnetic fields.

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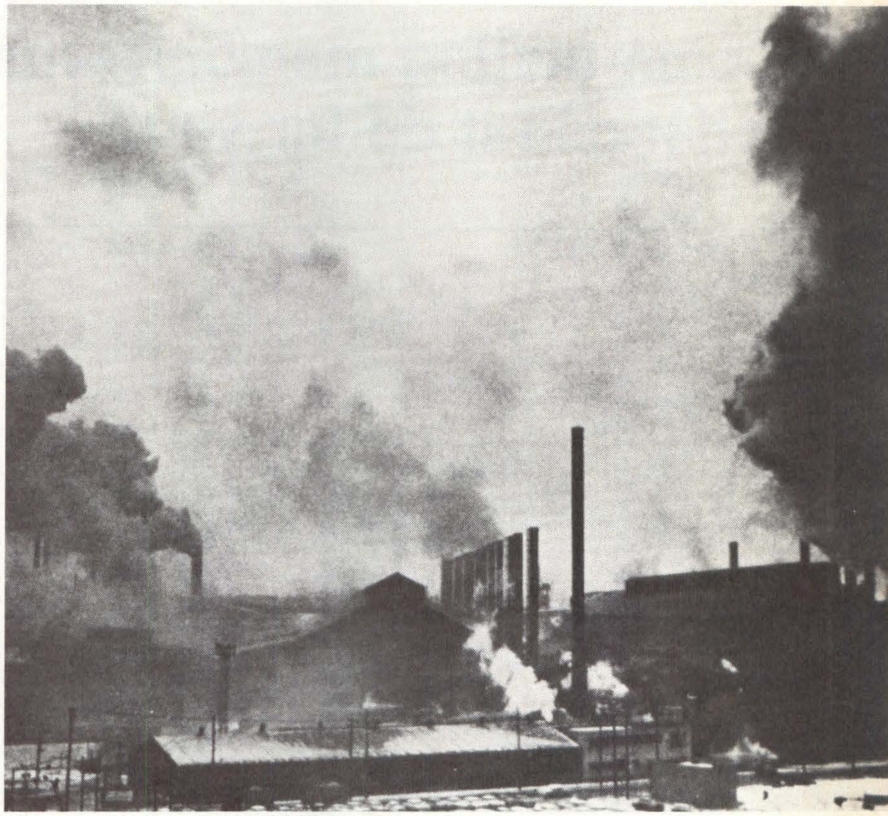

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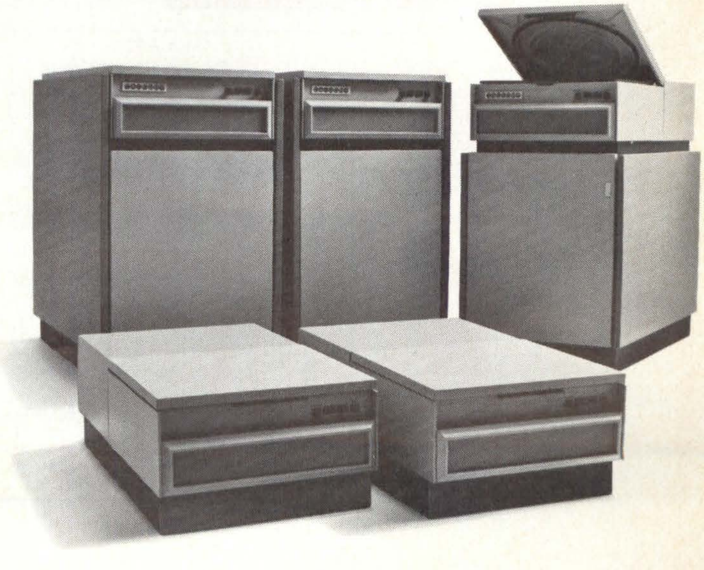
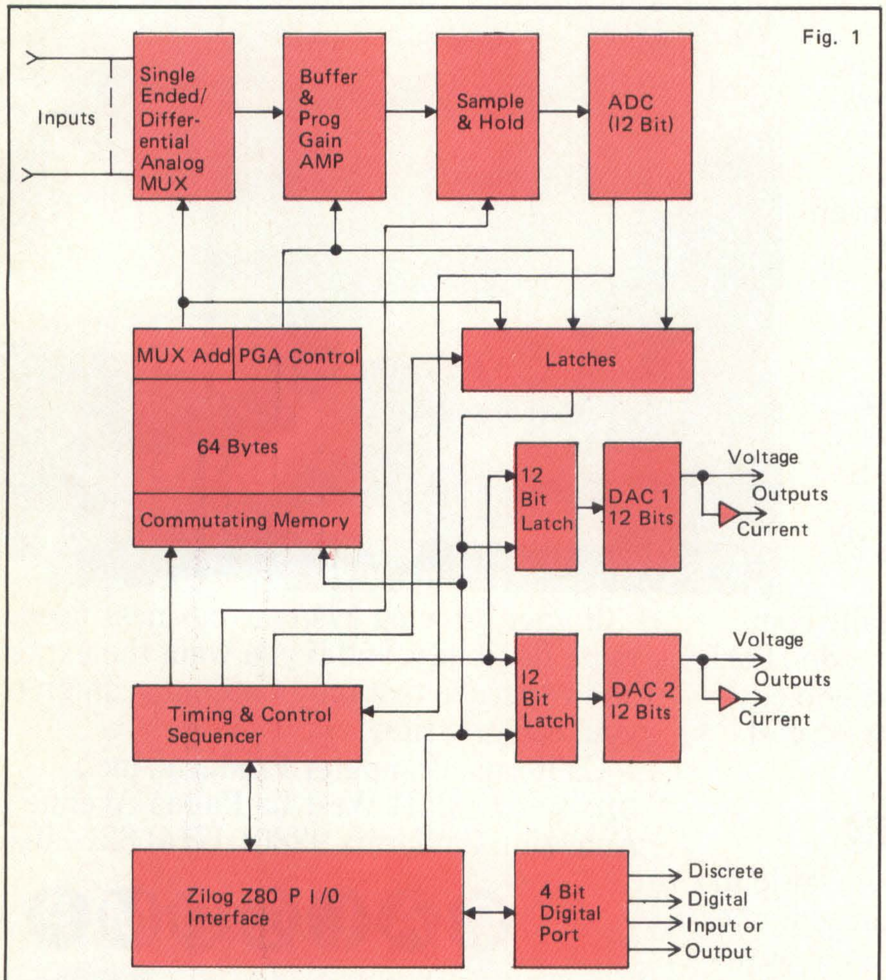
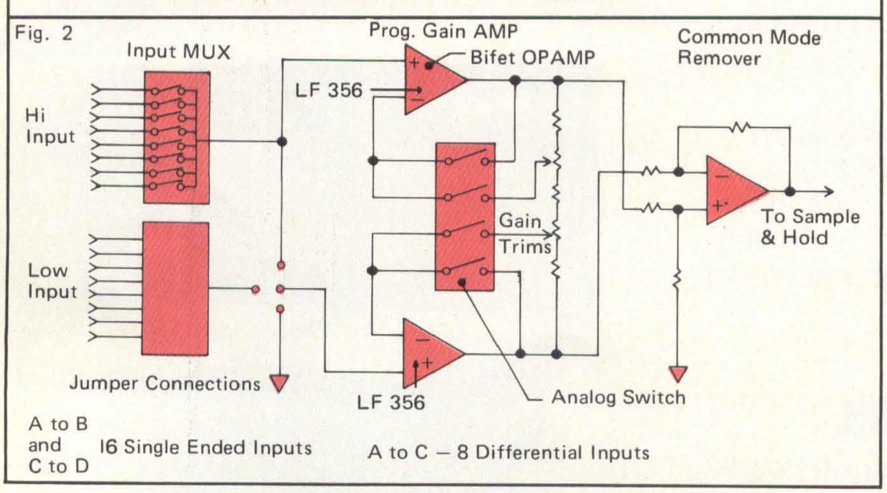


Commutating memory: what is it and what can it do for you?





In their design of a Smart Data Acquisition System, controlled by the Zilog Z80-MCB, Signal Laboratories of Orange, CA developed an Analog I/0 interface printed circuit card that incorprates a feature they call Commutating Memory (patent pending). This feature achieves a system microprocessor efficiency improvement on the order of 25-50% depending on the applications scenario resulting in a 25% or more increase in computations performed in real time. The entire analog I/0 subsystem, shown in Fig. 1, is called the MAD-One which stands for Multiplexer/A to D/D to A/model one.

The Commutating Memory, according to Del Flagg, V.P. of Engineering, evolved from their need to free the Zilog Z80-CPU from as much mundane control tasks as possible by transferring the most repetitious task from the Z80-MCB to the MAD-One. The MAD-One once initialized, cycles itself through any stored sequence of commands. The completion of the ADC cycle causes an interrupt request signal to be sent to the Z80 microprocessor and also advances the memory. This freedom from the control task, said Flagg, allows the Z80 to do other things while the MAD-One is telling itself where to go.

Look, first, at the overall operation of the MAD-One, he continued. The analog multiplexer accepts either single-ended or differential inputs. Address information for the multiplexer is received from the Commutating Memory. The output of the multiplexer is buffered with a programmable gain differential amplifier. The Gain commands are also supplied by the Commutating Memory synchronized with channel selection. Fig. 2 shows the details of the input, amplifier and buffer arrangement. This is followed by the sample and hold amplifier (Fig. 3). The "hold" command is coincident with the start of the analog to digital convert cycle and presents a very stable

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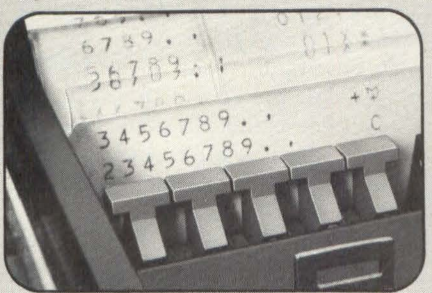

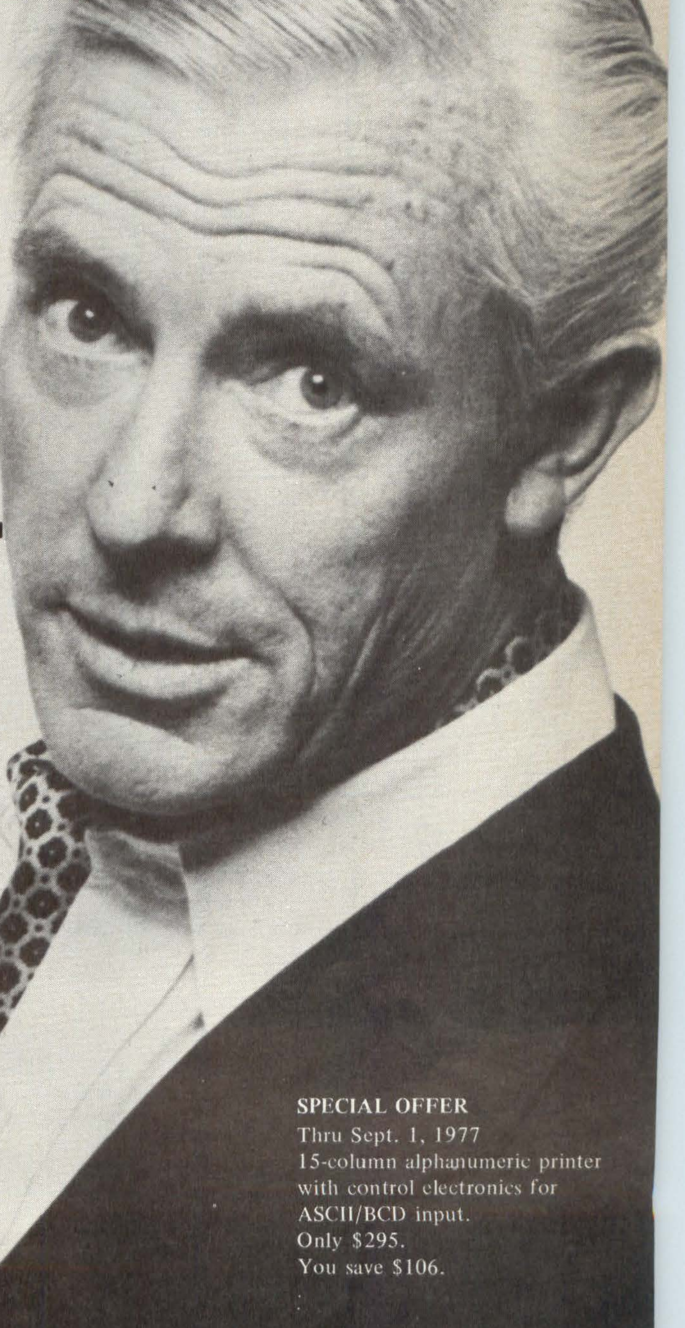

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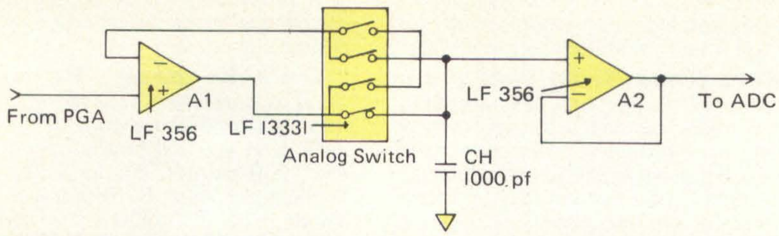
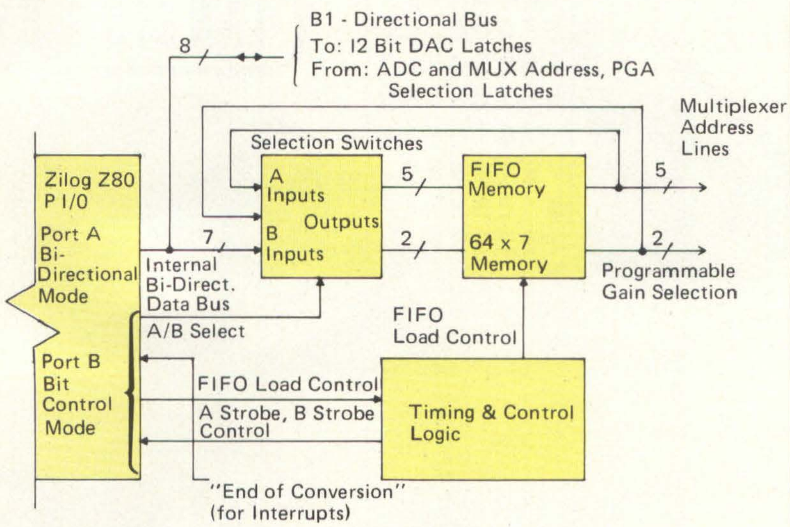
SAMPLE AND HOLD CIRCUIT

Fig. 3



COMMUTATING MEMORY BLOCK DIAGRAM

Fig. 4

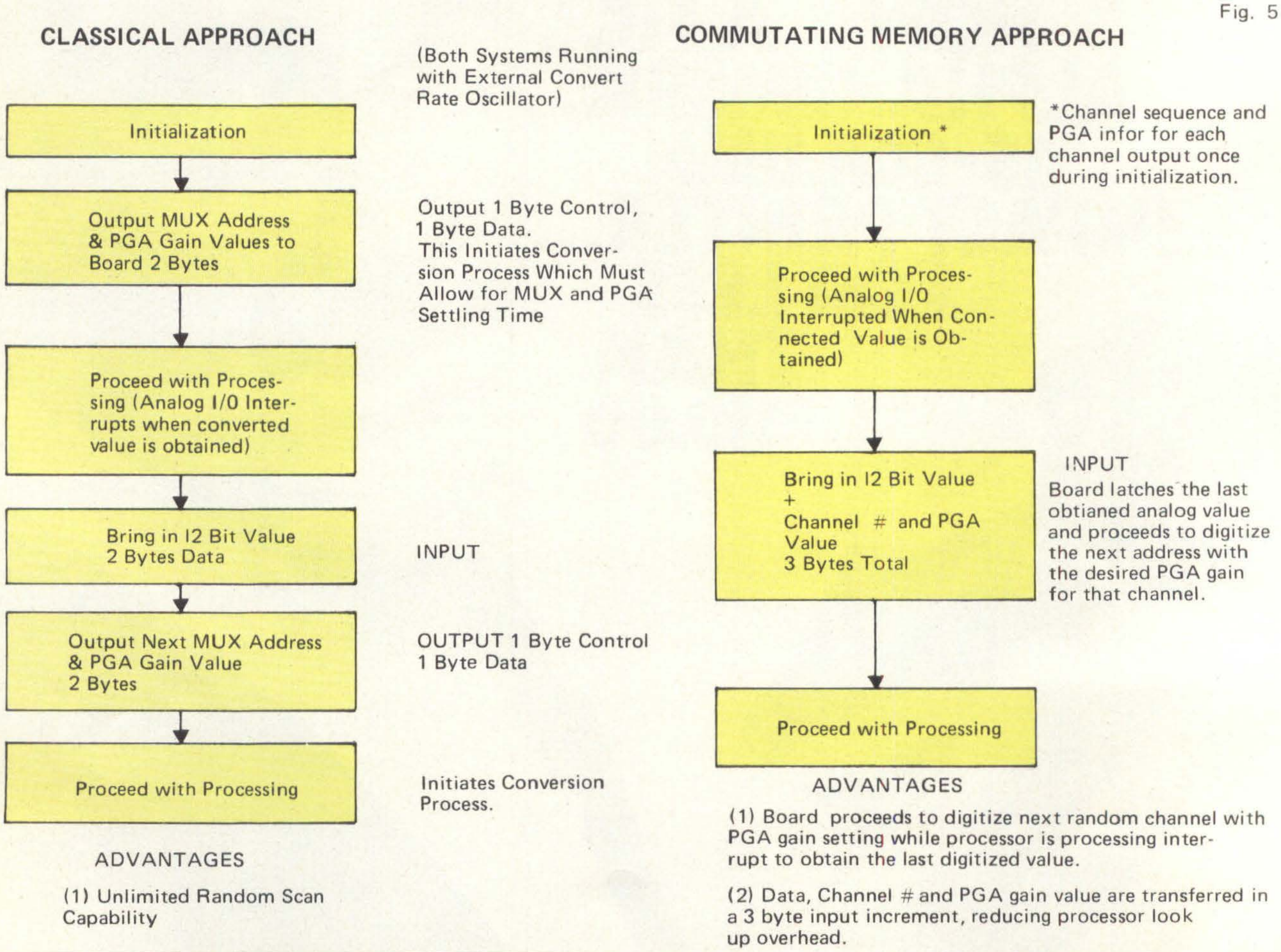


input to the A/D converter.

The end of convert signal from the A/D converter advances the Commutating Memory, latches data into the data register, sends an interrupt request to the processor and restores the sample and hold circuit to the sample mode. The MAD-One proceeds to process a new sample while the processor is responding to the interrupt signal, thus achieving a form of parallel processing, Flagg emphasized.

A closer look at the Commutating Memory (Fig. 4) shows it is composed of a First In, First Out Memory and a digital data source selection switch. This combination allows the FIFO to accept values for MUX Address and Amplifier Gain from the Z80-PIO. Once these values have been loaded, during initialization, the digital source selection switch is controlled to select the FIFO output as its own input, Flagg explained. This wrap-around effect allows the MAD-One to cycle on the predetermined scan sequence without further outputs from the processor. The FIFO output holds the MUX address and amplifier gain values as a normal register does during the digiti-

Fig. 5



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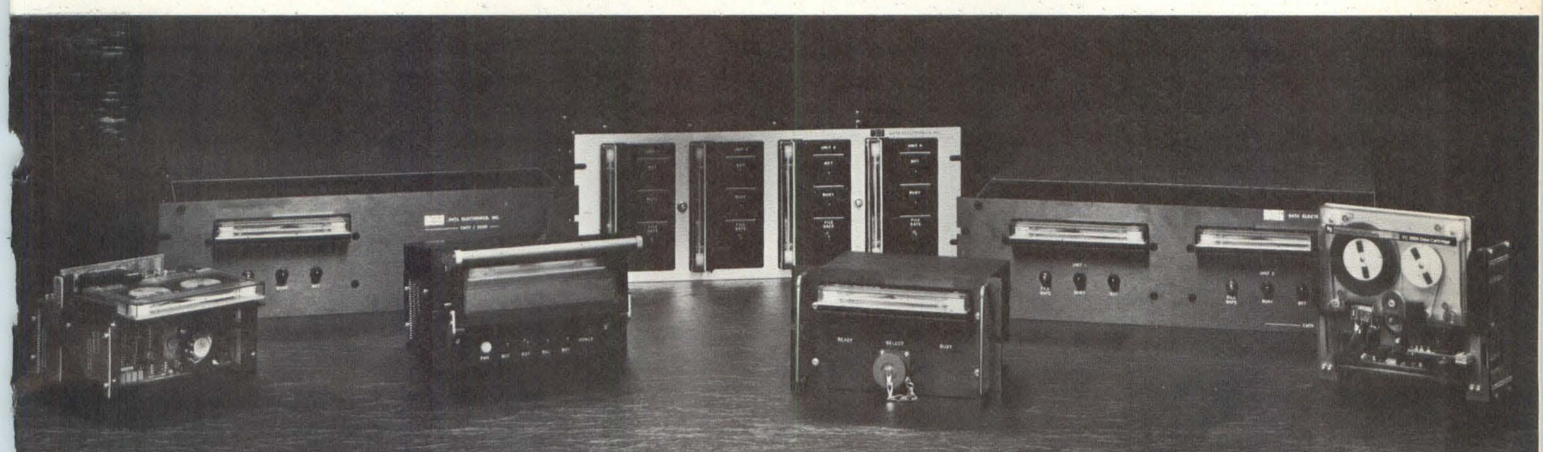

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CIRCLE 34

zing cycle. After that cycle is complete the FIFO input is strobed, thus restoring the channel and gain information. When the FIFO output is strobed, the next channel and the amplifier gain for that channel are brought up.

Flagg pointed out that up to 64 channels of any combination can be stored in the on-board memory of the MAD-One. The channels can be super or subcommutated within the cyclic limitations of the memory. In typical real world applications, some analog channels require greater bandwidths than others and consequently should be digitized more frequently. The Commutating Memory supports these real world applications very efficiently, according to Flagg.

How much can the Commutating Memory really mean in your application? To answer that question, Flagg compared the classical design approach to the Commutating Memory approach. Fig. 5 shows the normal program flow for each. Each approach has some initialization. However, the classical approach only initializes the logic on the analog I/0 board. The Commutating Memory extends the initialization to cover the transfer of channel scan sequence and amplifier gain selection values. Once these values have been transferred to the MAD-One's on-board Commutating Memory, the processor is freed of any further outputs to the analog I/0. The classical approach requires that the program has logic which determines the next channel in sequence. Because it must output that coincident with bringing data in, the analog I/0 board must wait on the processor, with its associated interrupt handler latency time, for the next MUX address and amplifier gain values. The Commutating Memory stores the data, the last MUX address and amplifier gain values in latches. It restores the FIFO output to the FIFO input, sends an interrupt request to the processor and automatically proceeds to digitize the next channel in sequence. In this way, Flagg stressed, parallelism is achieved in that the analog I/0 board digitizes the next channel while the processor handles the interrupt request and brings in the 3 byte data and channel information. As throughput rates increase, this could mean as much as a 50% time savings.

Flagg emphasized one final advantage of the Commutating Memory. The MAD-One with Commutating Memory is cost-effective. It costs no more than the classical approach.

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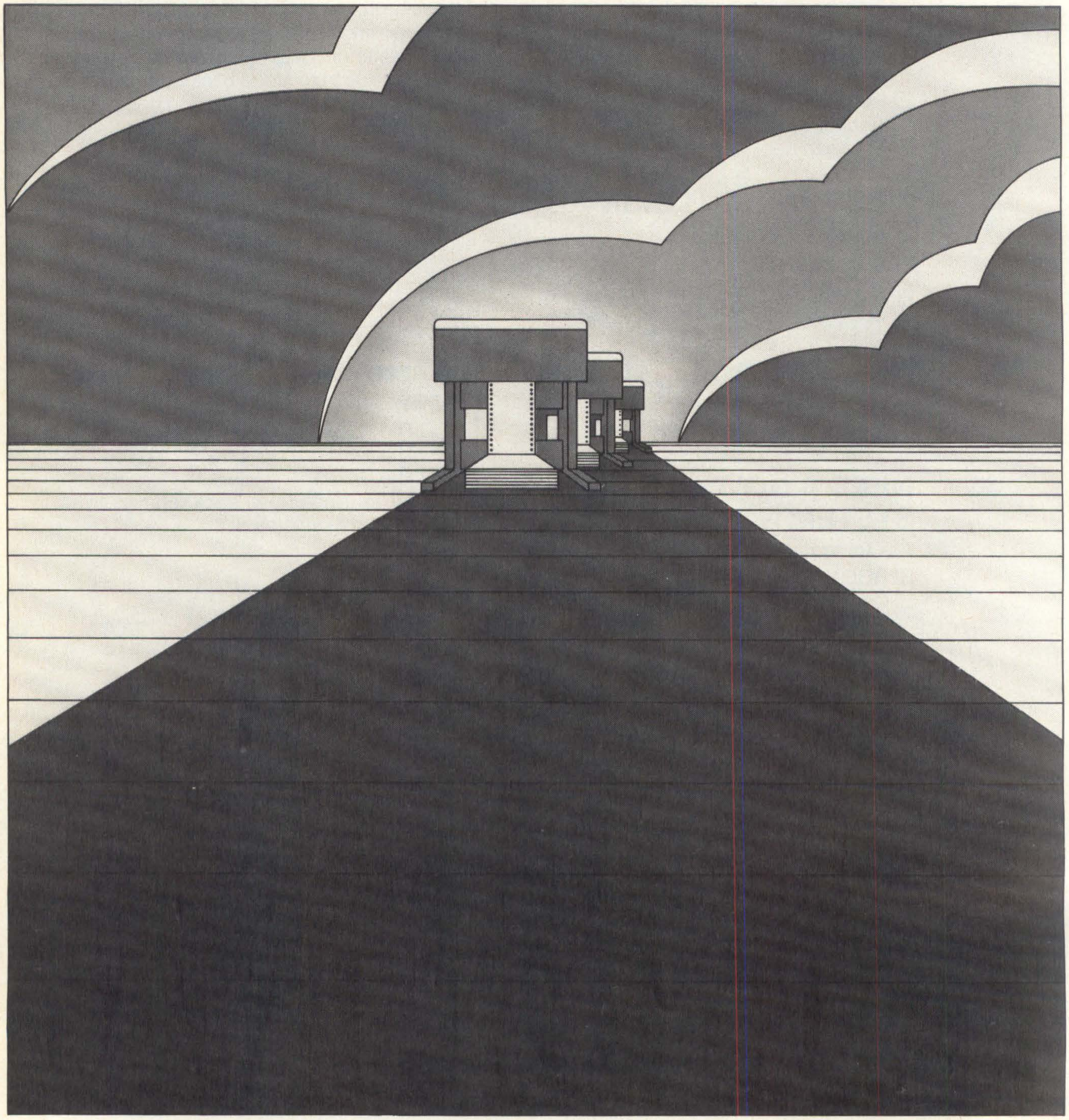

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Making a Semiconductor Memory Forget Stress and Adversity

Or how to design a 16K store to withstand military and industrial enviroments.

Class 2 requirements of MIL-E-5400 specify that electronic assemblies, such as semiconductor memories, intended for severe environment applications, must operate over a temperature range of -55 to +95°C, withstand up to 20-g sine vibrations and a 50-g crash safety shock. Assemblies that pass military humidity and salt spray tests, obviously can meet the needs of rugged commercial and industrial applications.

When called on recently to design a 16K semiconductor memory for military applications, the Severe Environment Products Division (SEPD) of Electronic Memories and Magnetics adopted a number of goals evolved from its existing line of core memories modules that generally offer a range of cycle times from 500 ns to 1.2 μs with worst case power consumptions from 50-90 W, said Donald Ballantyne, manager of systems and magnetics. In addition to the MIL-E-5400 Class 2 requirements, the new design specifications included:

- 16K x 18 storage capacity occupying half the volume of the same core memory of similar capacity;
- Twice the speed of the core memory;
- Lower power consumption.

electrical considerations

Most systems operating in a severe environment require power supplied with minimal transient voltage peaks and current fluctuations. Since core memories require much more current as a function of the data pattern being stored within the memory, the power source must be able to supply adequate current immediately for the worst case condition. On the other hand, semiconductor memory power usage more nearly resembles a dc load, provided that the short duration transient current spikes are adequately decoupled within the array. Therefore, semiconductor memories can use less costly power supplies.

The designers set a 5% tolerance for the basic supply voltage. This tolerance includes static and dynamic variations from normal voltage. Tolerances that exceed the 5% should be considered proof of end of life operation.

environmental problems

Extended Class 2 equipment specifications call for memory intermittent operation over -55 to +85°C and 95°C at its flange. SEPD's worst case design philosophy required that the memory should be able to perform its function with its mounting flange at 105°C, according to Ballantyne.

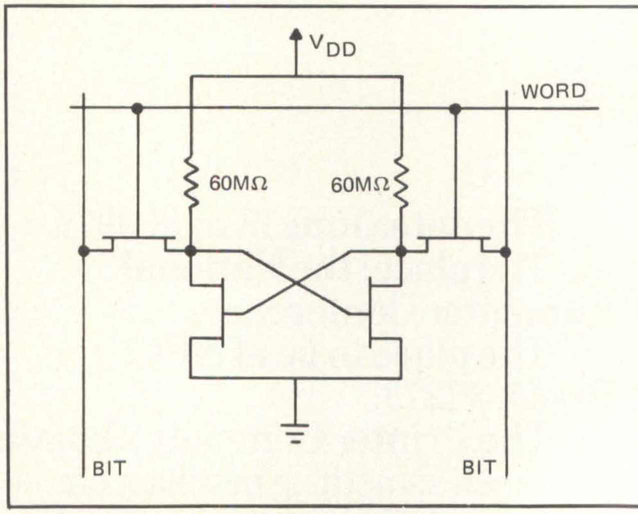


Fig 1 Static memory cell uses four transistors for the basic flip-flop and access ports. Two ion-implanted resistors serve as flip-flop loads. Depositing the resistors on top of the MOS transistors not only reduces the number of diffusions to one, but decreases the cell size considerably.

Severe environment memories must also withstand the shock of alternate exposure to -55 and +85°C without deterioration. Component mounting hardware ensures that semiconductor junctions never exceed 125°C under worst case conditions, yet remain flexible enough to withstand thermal shock. Humidity and salt spray requirements are met by conformal coatings to protect the soldered joints and components over the entire temperature range.

SEPD's engineers also found that the shock and vibration requirements of the design were easier to achieve in the semiconductor memory package, since the smaller board packages allowed for design tradeoffs to minimize bend radii that larger modules would have precluded. In consequence, the component mounting techniques employed became even more important.

semiconductor device

Many types of semiconductor devices were available for the application. However, Ballantyne cautioned that temperature extremes limit the performance of many devices — directly or as a secondary effect in some dynamic chips. In dynamic memory cells, he explained, the basic mechanism for storing information involves retaining the charge stored on an internal parasitic capacitance. Since leakage always

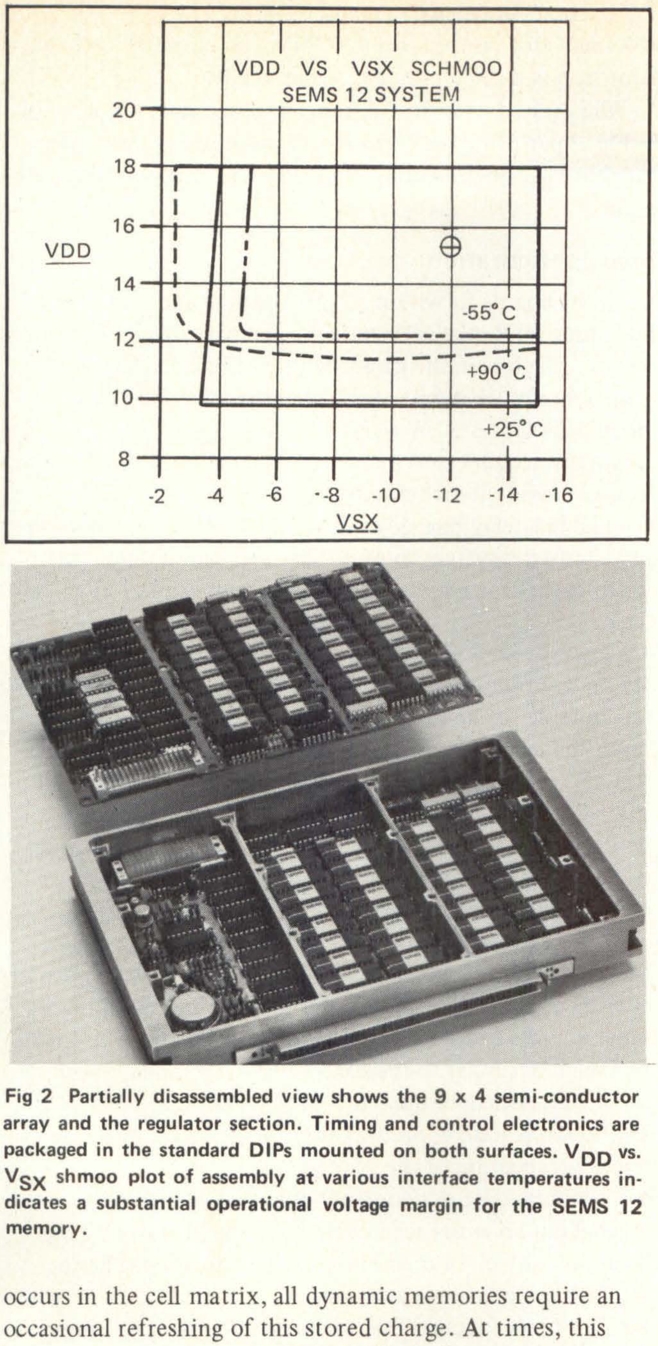


Fig 2 Partially disassembled view shows the 9 x 4 semi-conductor array and the regulator section. Timing and control electronics are packaged in the standard DIPs mounted on both surfaces. V_{DD} vs. V_{SX} shmoo plot of assembly at various interface temperatures indicates a substantial operational voltage margin for the SEMS 12 memory.

occurs in the cell matrix, all dynamic memories require an occasional refreshing of this stored charge. At times, this need makes the memory cell unavailable for processing or may cause occasional soft errors. In static memory cells, the familiar cross-coupled flip-flop stores a set state (information). They require no refreshing cycles to maintain that state. Consequently, the cell is available at all times for processing on demand.

The SEMI Division of EM & M chose the static concept as the better of the two. Its designers, said Ballantyne, worked hard at reducing chip and memory cell size and at increasing product reliability.

Even when the cell is in the set state, the load resistors drain current. Primarily a function of the resistor value and the chosen method of fabrication, this drain changes with temperature. The designers feel that this effect is a minor inconvenience compared with the resultant high-grade cell performance under all voltage and temperature conditions.

Static cells (see Fig 1 Cell Concept) are much less susceptible to the soft errors that occur in dynamic cells. These elusive, nonrepetitive failures are believed to be due to interference by random noise with the detection of low-level signals in the interior of dynamic cells. By contrast, voltage differences of the same level as the supply voltages represent data in static cells. This level is less susceptible to random noise effects.

Dynamic RAMs also suffer from another potential source of soft errors. The tighter the cell packing density, the more difficult it is to control metallization to minimize the capacitance of cell sensing interconnections.

Since soft errors do not always show up during dynamic RAM testing, can we explain why? Consider the fact, Ballantyne explained, that a dynamic RAM's worst case state is related to refresh timing. Immediately after refresh, strong charges on the parasitic storage capacitances represent the data. All testing done just after refresh is of limited value. Testing every cell just before refresh stretches the checking procedure to an impossible length. Consequently, a testing program may not uncover a weak cell that could generate a soft error. System testing may not be solution either, Ballantynes warned, because refresh systems usually operate asynchronously with respect to an applications program, and so subsequent program cycling may fail to repeat the worst case condition and the error may not reappear. This condition never shows up in static RAM cells, because they need no refreshing.

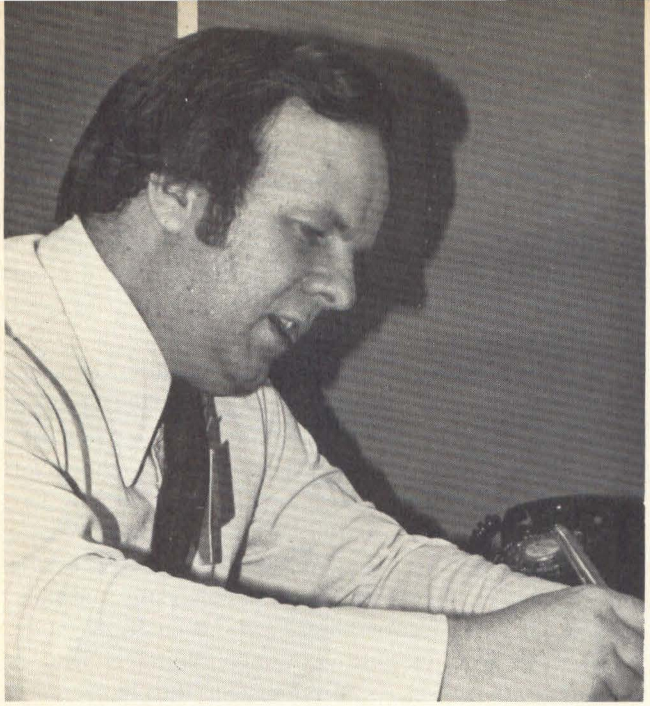
Static RAMs offer another advantage. They introduce into the system a low level of electrical noise. This lack of noise makes the system more reliable, reduces design debug time and cuts down the number of decoupling capacitors on the power lines. During the refresh cycle in a dynamic RAM system, all of the chips are accessed at the same time and they all simultaneously contribute to the overall system noise. In a static RAM system, on the other hand, only those chips that contain the required data are exercised at any given time. Therefore, the SEMI Division of EM & M chose to design 4K X 1 NMOS static RAM chips.

16K design

Semiconductor storage elements are arranged in two identical 16K x 9 arrays with the supporting electronics distributed equally between two boards. This arrangement of 9 x 4 arrays calls for the selection of nine chips in each array for any given address. It also calls for an output data buffer that must respond to output signals from four memory chips mounted in parallel.

SEPD designers used core memory techniques to ensure minimum chip selection rise and fall times – major factors in chip performance. Quiescently held at V_{DD}, the chip select node common to a particular 9 chip column, is conducted to ground by a 600-mA switch when the column is selected. This node, connected to a combination resistor-inductor, slowly starts to draw current after the initial current surge associated with chip-selection capacitance has been overcome. At the end of the chip selection time, the inductor becomes saturated and the current swith turns off, and forces the selection node rapidly positive. After the node is clamped to $+V_{DD}$, the inductor dissipates its current completely prior to the next cycle.

The SEMI 4200 chip contains an internal sense amplifier circuit that feeds an output buffer capable of driving Shottky TTL logic gates. In its quiescent state, the buffer pro-



Donald Ballantyne, manager of systems and magnetics for SEPD.

vides a high impedance that allows parallel chip connections to provide large bit configurations. Because the sense amplifier circuitry is close to the memory array, it assures full temperature performance, Ballantyne explained.

A preliminary test array, built to evaluate the chips and their overall performance under the range of temperatures and voltages, revealed two significant effects that determined the final design. The first of these involves the high coefficient of resistivity for the load resistors whose resistance drops as the operating termperature increases. The quiescent power drain at 125°C is approximately ten times higher than at room temperature. Since the RAM system contains 72 chips, the designers recognized that the initial power-on surge at +100°C into the memory could damage the chips or, in the worst case, overload the computer supplies and cause a power interrupt.

The second significant effect – chip access time varies with temperature – reveals that chip access time increased by about 40 ns as the temperature reaches 100°C. In addition, since increasing the V_{DD} level reduces the access time, this characteristic provides the major limit for high temperature chip operation. Although temperature effects are nearly linear, operation at -55°C did not become a problem. Chip operation speed increased and became more efficient in terms of power at the low temperature.

severe environment memory system – SEMS

With chip performance defined over the temperature range, SEPD engineers incorporated into their design of the severe environment memory system, called SEMS 12, the following characteristics:

- A positive voltage regulator, current-limited to prevent the chips from snatching excessive current at high-temperature turn-on, with a temperature dependency to compensate for the changing of access time with temperature
- A conservative thermal arrangement to minimize the temperature rise from the mounting flange to the worst case semiconductor chips
- A 400 ns total cycle time and a control scheme based on the existing core memory systems
- A small area reserved for a ROM for an automatic reload bootstrap and fixed program requirements.

When tested over the full temperature range, the assembly in Fig. 2 performed as expected, because the temperature-variable V_{DD} power supply compensates for access time variation.

final configuration

SEMS 12 boards fit within 9" x 6" outline and mount in a full width ATR case with enough room to provide thermal transfer passages in the case sidewalls. The clamping and control hardware is part of the memory. The 1.0" thich module dissipates 30 W worst case.

Variations built into memory system's control and timing section provide these options:

- An added delay line slows down the internal system timing and allows the system to wait 200 ns for input data. This added cycle time matches SEPD core memories of identical capacity.
- A high speed, 350 ns cycle and a 200 ns access time memory system that operates without a PROM. Delays which are attributable to the PROM decision paths are eliminated result in higher speeds.
- A 256 x 18 bit PROM page, located external or internal to the 16K x 18 bit RAM field, uses lower order addresses to determine word locations in the PROM and ignores higher order addresses. (For external control, a PROM interrogation requires an enable signal at the I/O.

If the PROM enable and write mode should appear at the start of the cycle, internal circuitry prevents the possible altering of RAM data. A hard-wired combination of higher order addresses selects the PROM internal to the RAM field. In a manner similar to the external control mode, lower order addresses determine the word location in the 256 x 18 PROM. A jumper on the timing and control board determines the location of the 256 words.

- A standard data-out control holds TTL signal levels throughout an entire read cycle, unless held active by the data-out control, or in another option allows configuring the data-out control is asserted.
- A low-power version that maintains the memory chips in their quiescent state, unless being accessed, and increases cycle time to 650 ns and access time to 250 ns and consumes a maximum of 10 W. (Standby power is reducible to 0.5 W, if data need not be maintained between memory cycles.)

one more benefit

Since the construction of static RAM cells makes them inherently independent of variations in internal threshold voltages and line transients, they resist radiation effects. On the other hand, dynamic RAM cells tolerate radiation very poorly, because nuclear particles produced by the nuclear event quickly dissipate the stored charge on the internal capacitances.

A semiconductor memory, typified by the SEMS 12, that can resist the severe environment conditions specified by MIL-E-5400 is useful for a wide range of applications. It passes the test for sensitivity to patterns usually associated with dynamic RAMs, and provides error-free storage for innumerable systems applications, Ballantyne concluded.

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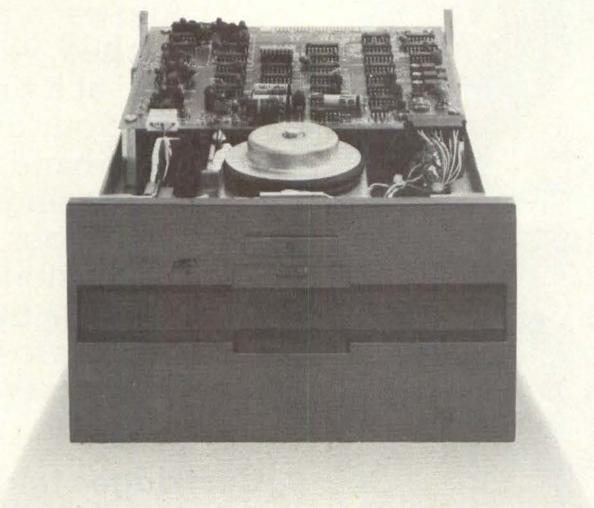

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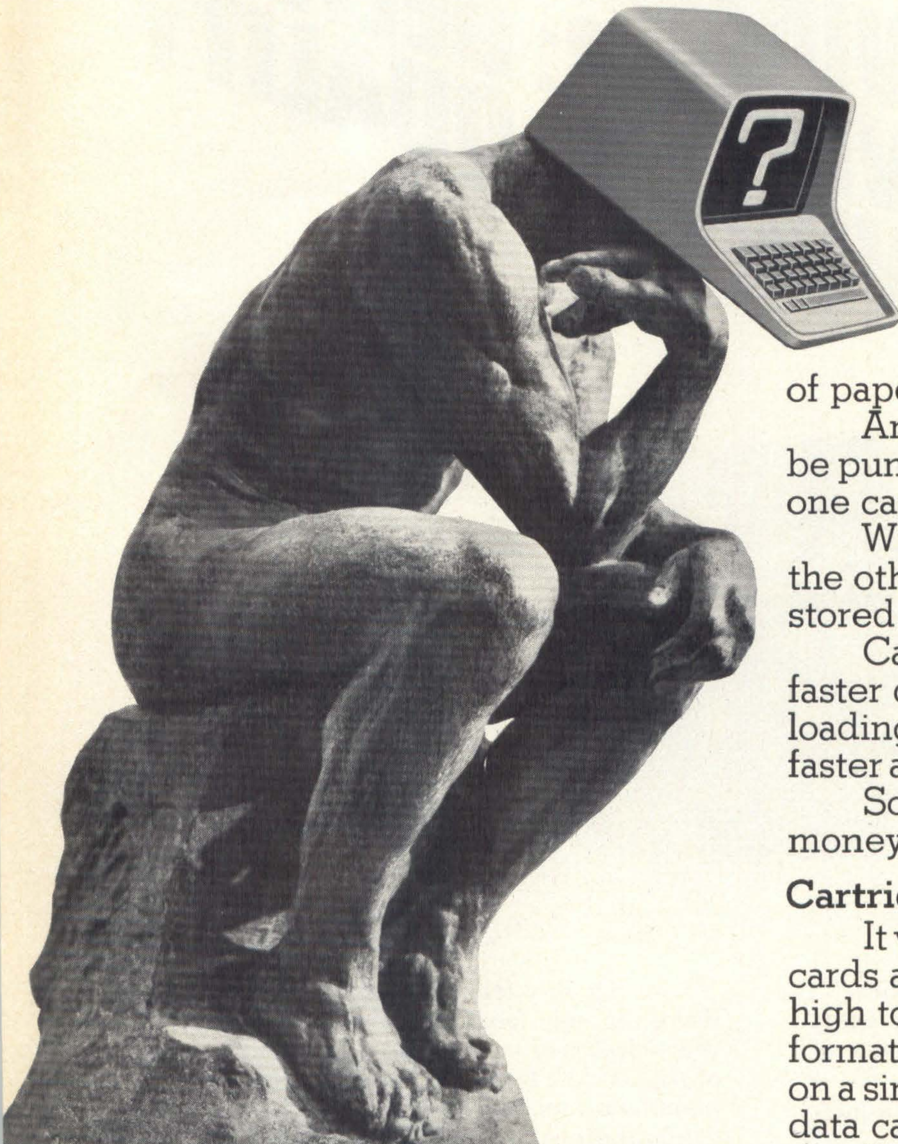
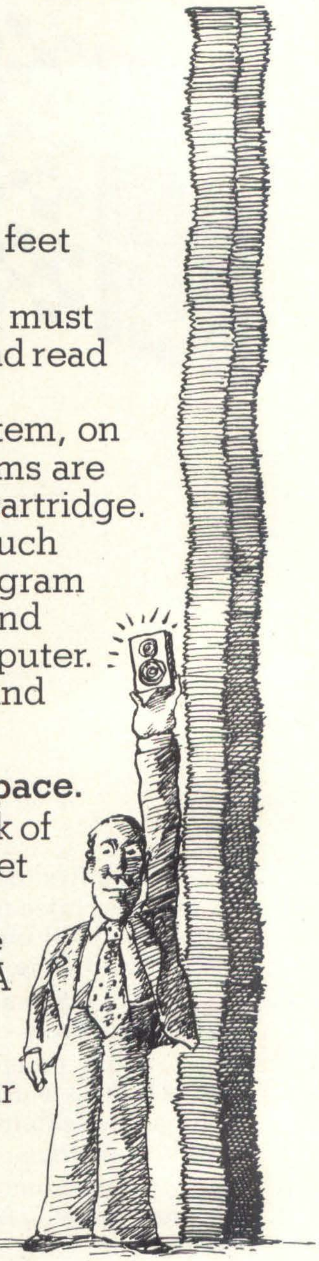
CIRCLE 40

Is your computer smart enough



One DC-300A cartridge equals almost 16 feet of cards.



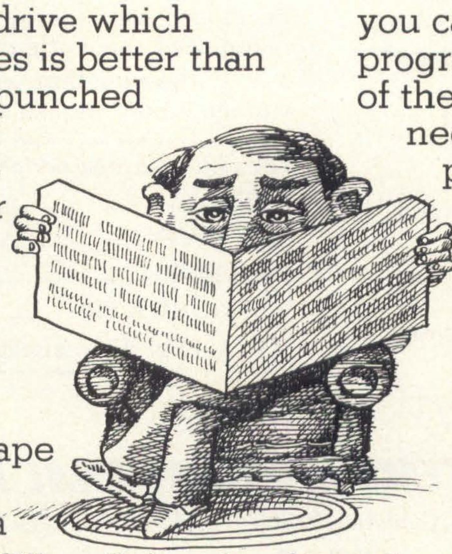
A 3M peripheral drive which uses 3M data cartridges is better than any drive which uses punched cards or paper tape.

And, if you'd take the time to ask it, your computer would probably tell you so.

It's simple logic.

Cartridges are faster than cards.

Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



Cards must be read one at a time.

Or hundreds of feet of paper tape.

And each program must be punched, verified and read one card at a time.

With our drive system, on the other hand, programs are stored on a single tape cartridge.

Cartridges offer much faster data storage, program loading, data transfer and faster access to the computer.

So you save time and money.

Cartridges take less space.

It would take a stack of cards almost sixteen feet high to store all the information you can store on a single 3M DC-300A data cartridge.

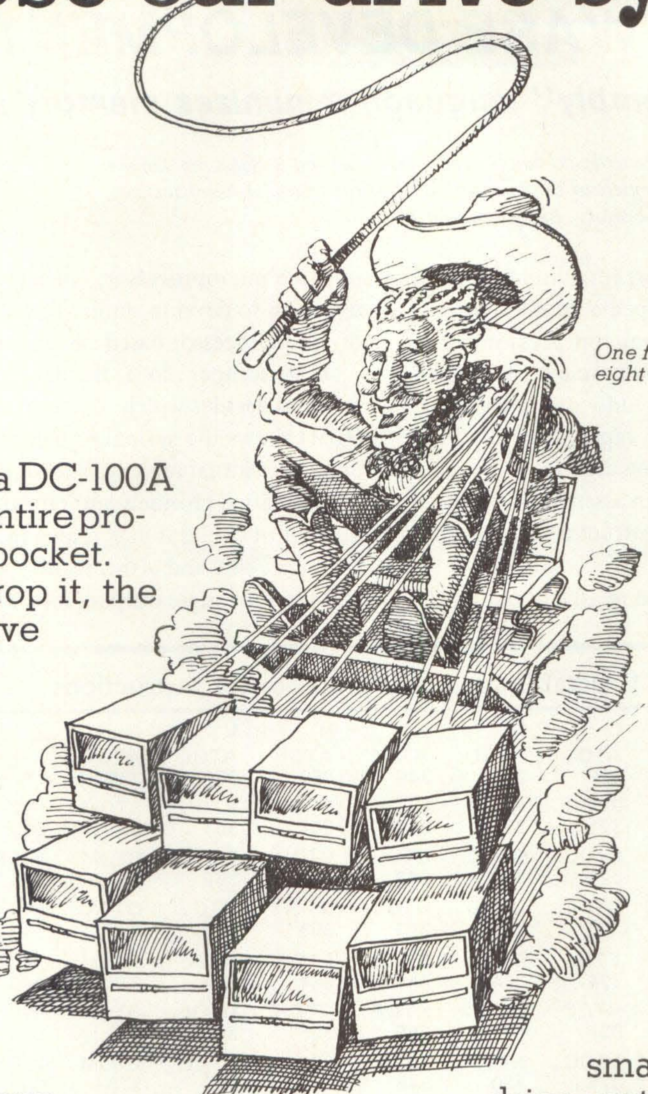
With cartridges, you can store all of your programs in a fraction of the space you'd need for cards or paper tape.

Your filing system is simplified and overhead is greatly reduced.

Cartridges won't fold, spindle or mutilate.

Unlike paper cards, you need never touch the media. It's well protected inside the cartridges, so it's virtually impossible to damage.

to choose our drive system?



One formatter can control eight drives at once.

You can carry a DC-100A cartridge with an entire program in your shirt pocket.

Even if you drop it, the program will survive unscathed.

Remember that the next time you drop a stack of cards!

Don't take our word for it. Ask your computer.

If you'll send us the coupon, we'll send you the specifications for all three of our drive systems.

Ask your computer to compare them with any other type of drive system.

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Maybe it'll choose our famous DCD-3 drive. It's people-proof, jam-proof and wear-resistant.

Or maybe your computer will decide upon our DCS-3000 series, an ANSI-formatted system that allows one formatter to control up to eight drives.

The DCS-3000 is extremely easy to integrate into your system. Only one cable to the user's logic is required.

But if you require compact size, your computer will probably choose our unique DCD-1. It offers many of the features of our bigger systems, yet it will fit inside a five-inch cube.

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CIRCLE 41

SPEEDING MICROPROCESSOR SOFTWARE DEVELOPMENT

"Pseudo assembly" language minimizes memory usage

S. Panchapakesan, H. Venkateswaran and S. Subramanian are members of the scientific staff of the National Aeronautical Laboratory, Bangalore, India.

As part of a software development effort for a microprocessor based data logger, we have developed a "pseudo assembly" language for the data logger's microprocessor and a pseudo assembler for this language. We have also developed a debug package for the system. The pseudo assembler has nearly all of the important features and capabilities of a full-fledged assembler and if necessary can be used to bootstrap such a self-assembler. But unlike such an assembler, it doesn't utilize large amounts of memory to construct and maintain symbol tables.

Though our data logger incorporates the relatively old Intel 8008 microprocessor, our techniques are general; you can use them to develop similar pseudo assemblers for other types of microprocessor based systems.

In its scanner mode, the data logger samples several channels and decides which to energize. An initial balance mode (IBM) allows the system to balance strain gauge bridge outputs, take initial readings and store them in RAM; it can also skip specified channels and repeat-scan a channel for a given number of cycles. Finally, an experimental mode provides a limit-checking and alarm facility and converts strain gauge and thermocouple outputs into engineering units.

Table 1. Octal Codes For Microprocessor Instructions

	A	B	C	D	E	H	L	M		
A	ATOA 300	ATOB 310	ATOC 320	ATOD 330	ATOE 340	ATOH 350	ATOL 360	ATOM 370		
B	BTOA 301	BTOB 311	BTOC 321	BTOD 331	BTOE 341	BOTH 351	BTOL 361	BTOM 371	INCRB 010	DECRB 011
C	CTOA 302	CTOB 312	CTOC 322	CTOD 332	CTOE 342	CTOH 352	CTOL 362	CTOM 372	INCRC 020	DECRC 021
D	DTOA 303	DTOB 313	DTOC 323	DTOD 333	DTOE 343	DTOH 353	DTOL 363	DTOM 373	INCRD 030	DECRD 031
E	ETOA 304	ETOB 314	ETOC 324	ETOD 334	ETOE 344	ETOH 354	ETOL 364	ETOM 374	INCRE 040	DECRE 041
H	HTOA 305	HTOB 315	HTOC 325	HTOD 335	HTOE 345	HTOH 355	HTOL 365	HTOM 375	INCRH 050	DECRH 051
L	LTOA 306	LTOB 316	LTOC 326	LTOD 336	LTOE 346	LTOH 356	LTOL 366	LTOM 376	INCRL 060	DECRL 061
M	MTOA 307	MTOB 317	MTOC 327	MTOD 337	MTOE 347	MTOH 357	MTOL 367			

Load Operations

LOAD	LOADA 006	LOADB 016	LOADC 026	LOADD 036	LOADE 046	LOADH 056	LOADL 066	LOADM 076

Shift operations (Accumulator)

Rotate left	ROTL	002	Rotate right	ROTR	012
Rotate left with carry	ROTLC	C22	Rotate right with carry	ROTRC	032

Accumulator Operations

Add	ADDA 200	ADDB 201	ADDC 202	ADDD 203	ADDE 204	ADDH 205	ADDL 206	ADDM 207	ADDI 004
Add with carry	ADDCA 210	ADDCB 211	ADDCC 212	ADDCD 213	ADDCE 214	ADDCH 215	ADDCL 216	ADDCM 217	ADDCI 014
Subtract	SUBA 220	SUBB 221	SUBC 222	SUBD 223	SUBE 224	SUBH 225	SUBL 226	SUBM 227	SUBI 024
Subtract with borrow	SUBBA 230	SUBBB 231	SUBBC 232	SUBBD 233	SUBBE 234	SUBBH 235	SUBBL 236	SUBBM 237	SUBBI 034
Logical AND	ANDA 240	ANDB 241	ANDC 242	ANDD 243	ANDE 244	ANDH 245	ANDL 246	ANDM 247	ANDI 044
Exclusive OR	EXORA 250	EXORB 251	EXORC 252	EXORD 253	EXORE 254	EXORH 255	EXORL 256	EXORM 257	EXORI 054
Inclusive OR	INORA 260	INORB 261	INORC 262	INORD 263	INORE 264	INORH 265	INORL 266	INORM 267	INORI 064
Compare	CMPA 270	CMPB 271	CMPC 272	CMPD 273	CMPE 274	CMPH 275	CMPL 276	CMPM 277	CMPi 074

Continued on p. 42

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PERKIN ELMER DATA SYSTEMS

The software that controls these operation modes operates interactively with the data logger; developing and testing it would not have been possible without the debug program and the capabilities offered by the pseudo assembly language.

Microprocessor-software development efforts generally utilize in-house computing facilities, but using a minicomputer or timesharing terminal this way can prove expensive. A simpler alternative involves interfacing a teleprinter or other low-cost I/O device with the microprocessor and storing a debug program in the microprocessor's memory to facilitate interactive program development.

octal codes simplify program loading

As the first step in developing such a debug program, we keyed an 8-byte loader program into the 8008-system's RAM; this loader allowed us to read in instructions and data from paper tape, using the microprocessor's interrupt logic and a specially built-in hardware I/O interface.

We then developed a set of octal codes for the microprocessor's instructions so that we could read instructions into the micro's memory without having to store a table of teleprinter characters there. Each 3-digit code breaks up this way: its leftmost digit corresponds to the two leftmost bits in the corresponding 8008 instruction; its middle digit corresponds to the middle three bits of the instruction, and its rightmost digit corresponds to the rightmost three bits of instruction.

The hardware I/O interface attached to the system identifies these octal codes and converts them into instruction or data bytes. The 8-byte loader program then loads the system's RAM with all the data that arrives at the microprocessor's input port; we can thus load any size octal-code program (up to the system's RAM capacity) from paper tape, starting at any desired memory location.

Table 1. Continued

Restarting Instructions									
Restart at Location		**0**	**8**	**16**	**24**	**32**	**40**	**48**	**56**
		CALM0 005	CALM1 015	CALM2 025	CALM3 035	CALM4 045	CALM5 055	CALM6 065	CALM7 075
Halt Instructions									
		HALT0 000	HALT1 001	HALT2 377					
Branch Instructions									
			Conditional				**Unconditional**		
		Carry	**Zero**	**Sign**	**Parity**				
		TJMPC 140	TJMPZ 150	TJMPS 160	TJMPP 170				
JUMP							UCJMP 104		
		FJMPC 100	FJMPZ 110	FJMPS 120	FJMPP 130				
		TCALC 142	TCALZ 152	TCALS 162	TCALP 172				
CALL							CALL 106		
		FCALC 102	FCALZ 112	FCALS 122	FCALP 132				
		TRETC 043	TRETZ 053	TRETS 063	TRETP 073		RETN 007		
RETURN									
		FRETC 003	FRETZ 013	FRETS 023	FRETP 033				
Input/Output Operations									
Input Port	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	
	INPT0 101	INPT1 103	INPT2 105	INPT3 107	INPT4 111	INPT5 113	INPT6 115	INPT7 117	
Output Port	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	
	OUT00 121	OUT01 123	OUT02 125	OUT03 127	OUT04 131	OUT05 133	OUT06 135	OUT07 137	
Output Port	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	
	OUT08 141	OUT09 143	OUT10 145	OUT11 147	OUT12 151	OUT13 153	OUT14 155	OUT15 157	
Output Port	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	
	OUT16 161	OUT17 163	OUT18 165	OUT19 167	OUT20 171	OUT21 173	OUT22 175	OUT23 177	

The next step in developing the debug program was to devise a set of mnemonics that have a one-to-one correspondence with the octal codes (Table 1). A Fortran IV program translates these mnemonics to their octal-code equivalents and then to the teleprinter's paper-tape codes.

pseudo assembler provides low-level programming

To provide a low-level programming language for the microprocessor, we then bootstrapped the pseudo assembly language from the mnemonics and coded the language's assembler using those mnemonics. The one-pass assembler, which occupies about 800 bytes, has a label field, an operation field and two operand fields. An important advantage over conventional assemblers is its disassembler function, which allows reconversion from machine language to pseudo assembly language.

In its current implementation, the pseudo assembly language has 100 labels, numbered from 00 to 99 and each preceded by an L directive. The L and label number can appear either in the label field or in the address field of a branch instruction.

The pseudo assembler provides forward referencing of labels this way: When a forward reference to a label appears in a program, the pseudo assembler compiles it as a JUMP order and stores this order's address in a Label Table. When a second forward reference to the same label appears, the pseudo assembler compiles it as an order whose address portion contains the Lable Table address of the first JUMP order. The pseudo assembler then replaces the first address in the Label Table with the address of the second JUMP order. Subsequent forward references to the same label compile similarly and form a chain of JUMP orders, each of which points to its predecessor.

When the label appears in the program, the final JUMP order in the chain is modified to jump to the correct location, the instruction at that location points to the next order in the chain, and so on. The address-replacement process continues until the last reference points to location 0.

Because the pseudo assembler doesn't recognize mnemonic operands, no mnemonics can appear in a program's operand fields. But certain directives – L, A, C and D – are mnemonic and indicate the nature of the operands. L followed by a 2-digit decimal number denotes a label, A tells that the decimal number following it is an absolute address, C says to acquire the contents of the absolute address that follows it and D informs the pseudo assembler that decimal data follows. The pseudo assembler also recognizes certain single- and two-letter symbols that represent the microprocessor's internal registers – A, B, C, D, E and M (or H,L) – and the contents of those registers – CA, CB, CC, CD, CE and CM.

Operation codes in the pseudo assembly language (Table 2) are three-letter mnemonics; they decide whether an instruction is one, two or three bytes long. In addition to the single-letter directives we've already described, three others can appear. DC defines data; the absolute address that appears to its left contains the values that appear to its right. BGN informs the pseudo assembler that a program unit follows; the unit is assembled from the location that follows the directive. Finally, FIN informs the pseudo assembler that the program unit being assembled contains no further instructions.

Because we can specify all absolute addresses with an A directive, relocating a program in memory presents no problem with this pseudo assembly language. The pseudo assembler collects all such absolute addresses and punches them on paper tape with the object program. When this object program goes to the relocating loader along with the required relocation information, the loader automatically adjusts all absolute-address references that appear in the program.

Using the pseudo assembly language's call (CAL) and return (RET) mnemonic operation codes, we can nest routines and subroutines in up to seven levels in the microprocessor's hardware stack. With this nesting capability, we can develop programs modularly so that each program unit can have up to 100 labels; units are assembled independently.

Table 2. Pseudo Assembly Instructions

IPT	Transfer data from input port to acc
OUT	Transfer data from acc to output port
TRN	Transfer (reg to reg)
LDA	Load register
INC	Increment contents of reg
DEC	Decrement contents of reg
ADD	Add to acc
ADI	Add immed data to acc
ADC	Add with carry to acc
ACI	Add with carry immed data to acc
SUB	Subtract from acc
SUI	Subtract immed data from acc
SBB	Subtract with borrow from acc
SBI	Subtract with borrow immed data from acc
AND	Logical AND with acc
NDI	AND immed data with acc
EXR	Exclusive OR with acc
XRI	Exclusive OR immed data with acc
INR	Inclusive OR with acc
IRI	Inclusive OR immed data with acc
CMP	Compare acc
CPI	Compare acc with immed data
RAL	Rotate acc left
RAR	Rotate acc right
RLC	Rotate acc left with carry
RRC	Rotate acc right with carry
BRA	Branch to
BCT	Branch if condition true
BCF	Branch if condition false
CAL	Call subroutine
CCT	Call subroutine if condition true
CCF	Call subroutine if condition is false
RET	Return
RCT	Return if condition true
RCF	Return if condition false
RST	Restart at
HLT	Halt2
HLZ	Halt0
H10	Halt1

Directives to pseudo assembler:

BGN	Begin	D	Decimal data
FIN	Finish	L	Label
A	Address (absolute)	DC	Define constant
C	Contents		

debug package speeds development

In response to one- or two-letter mnemonic codes, the debug package can

★ Display and/or change the contents of RAM locations
★ Display and/or change the contents of all CPU registers
★ Display and/or change CPU status
★ Input and/or output a block of instructions or data with a checksum to or from any specified RAM location
★ Set up breakpoints in the program and display and/or change register/memory contents at those breakpoints
★ Execute a program beginning at a specified RAM location.

We used the package to develop the data logger's programs, which we wrote in the pseudo assembly language. Primarily, the package tested parts of the programming and helped us integrate these parts.

Here's one example of the debug program's use. The data logger has access to two subroutines – BCD-Binary Convert and Binary-BCD Convert. The first transforms control information (channel address and selection) from CCITT-coded inputs into binary form for RAM storage and later use. The second transforms binary channel addresses into BCD form for use by the data logger.

In its scanning mode, the data logger hands over control to the debug package whenever a selected channel address or control information is required. The debug package gains control, invokes the appropriate subroutine, places the result in memory and returns control to the scanner program. The debug program also allows specification of such system requirements as single or cyclic scan.

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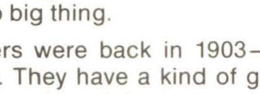

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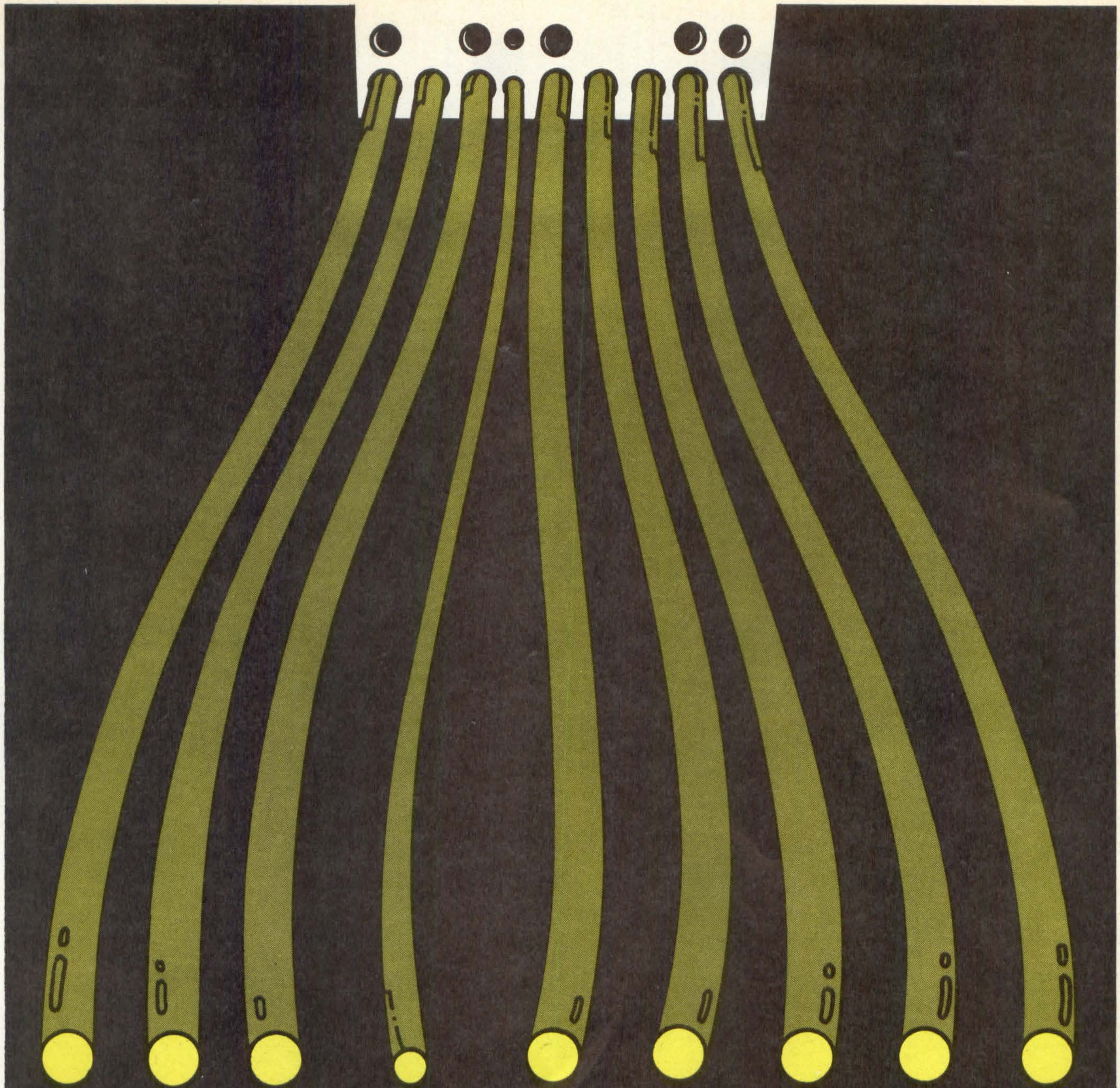

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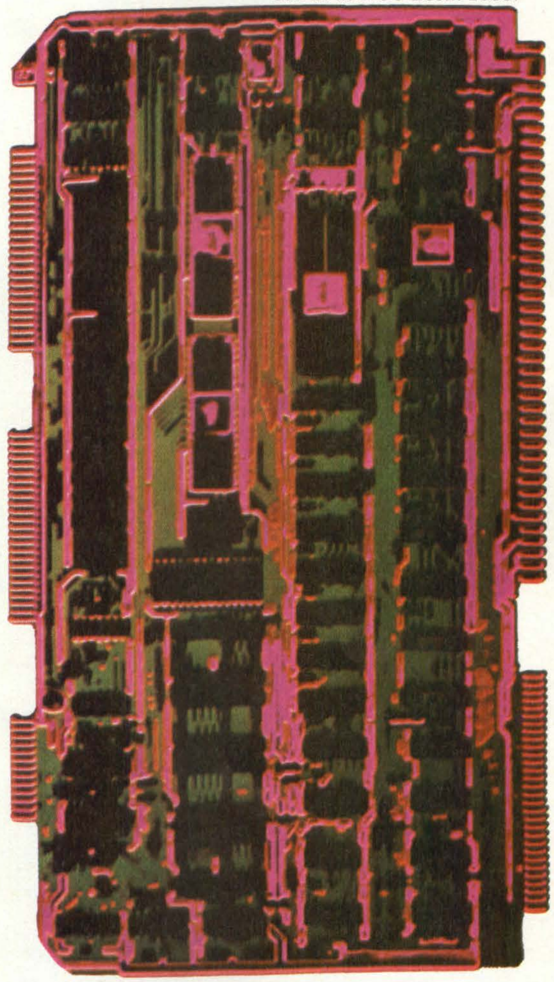

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magnetic bubble memories

past • present • future

A BENWILL/TECHNOCAST REPORT

Magnetic bubbles are single wall domains assuming the shape of right circular cylinders in a sheet of magnetic material, typically a rare earth orthoferrite, characterized by a preferred or easy axis of magnetization perpendicular to the plane of the sheet. The axis can be defined as a negative direction of magnetization out of the plane of the sheet while magnetic bubbles have a positive direction of magnetization normal to the sheet.

Magnetic fields move or propagate magnetic bubbles in the magnetic sheet. Since binary information can be represented by either different size bubbles, circulation direction of domain wall magnetization, or the presence and absence of bubble domains, all of which can correspond to a binary "1" or "0". Magnetic bubbles make excellent shift register or memory applications.

Fig 1a Encircled plus sign represents a domain in a magnetic sheet. The circle in the plane of the sheet represents the encompassing single wall of the domain.

The first patent suggesting magnetic bubbles for memory applications was granted to Bell Telephone Laboratories in 1969 (1). The potential of this new technology to provide low cost, high capacity memories, quickly realized, is reflected in recent patent activity. Over 53% of the U.S. patents in this technology have been granted during the most recent three year period, 1974-76 (estimated).

In terms of numbers of U.S. patents granted, the foreign activity in magnetic bubble memories, for the period 1974-76 (estimated) is only slightly less than the all technology foreign share average of 35.4%. About 31% of all U.S. patents in the area have been granted to foreign residents over the period 1974-76 (estimated). The country table shows, by patent grant date and patent application date, the country distribution of the patents in this field that were granted to foreign residents. *(See Table 1)*

description of the technology

Magnetic bubbles are usually formed in thin sheets of certain magnetic oxides. A basic requirement for formation of bubbles is that the sheet material possesses uniaxial magnetic anistropy with the easy direction of magnetization perpendicular to the plane of the sheet, achievable in crystals or orthoferrite, hexagonal ferrites and synthetic garnets. Another requirement is that the material be able to support a bubble of small diameter to make large density memories possible. Synthetic garnets seem to possess the most desirable characteristics for bubble memory applications since they have the capability to support the smallest stable bubble size at high mobility rates.

Magnetic bubbles are shaped by applying a biasing magnetic field perpendicular to the plane of the sheet. Increasing this field causes the natural serpentine domains of the sheet to shrink until most of them disappear. However, a few domains will shrink to a stable cylindrical volume or "bubble" of polarity opposite to the rest of the sheet, as shown in Fig 1a. These bubbles are stable over a variation of approximately 30% of the biasing field. However, if the bias is increased above critical strength, these stable bubbles will also collapse and be annihilated. Fig 1b shows the evolution of propogate structures.

Magnetic bubble propagation or movement is achieved by creating an unbalanced force on the bubble which drives it in the desired direction. This may be done by creating, in the vicinity of the bubbles, localized magnetic fields which, by magnetic attraction or repulsion, cause the bubble to propagate.

Basically, two methods are available for producing such fields: conductor-access and field-access. In the conductor-access technique, small current carrying loops are deposited on the sheet and the loops are sequentially energized by three phase currents. In the field-access approach, permalloy (soft magnetic material) patterns are deposited on the sheet and a transverse in-plane rotating field is used to change the magnetic polarities of these patterns to cause the bubbles to follow the changing pole patterns from input to output position. Three often used permalloy patterns are the chevron, T-I bar and Y-I bar configuration.

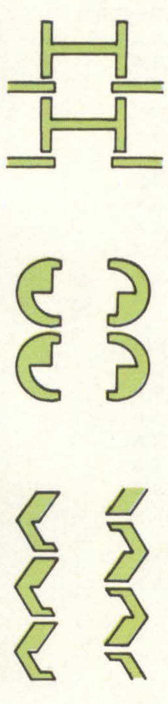
Fig 2 illustrates the propagation of a bubble using a permalloy T-bar pattern for supporting a pole pattern changing in response to a rotating transverse field in the plane of the sheet. To perform the necessary memory operations of writing, reading and erasing, the magnetic bubbles must, respectively, be generated, sensed and annihilated.

In addition to generation by nucleation, bubbles can be created by stretching a seed bubble and separating it into two bubbles, accomplished using permalloy patterns and the appropriate fields or current. In a typical bubble generator, the seed bubble rotates around a permalloy disc under the influence of a rotating driving field (patents 3, 4). As the bubble rotates, it is stretched by attraction to an adjacent T-bar pattern. When the field is in an upward direction, repulsion by the lower portion of the disc collapses the center of the domain leaving the seed bubble and a newly generated bubble.

A number of methods are available for bubble sensing: electromagnetic induction, Hall effect, optical sensing and magnetoresistance effect.

• In the electromagnetic induction method, the moving bubble acts as a magnetic dipole and induces a small voltage in a pickup coil. • In the Hall effect, a probe generates a voltage output at right angles to the direction of a direct sense current. • In optical sensing, the detector reacts to a change in the intensity of light when a bubble is observed through a polarizer. • In the magnetoresistive effect, the presence of a bubble lowers the resistance of a permalloy segment, providing a usable output signal.

EVOLUTION OF PROPAGATE STRUCTURES



T-BAR
- 1/16th Period Min Features
- Defect Sensitive Long and Narrow Bars
- Bars Interconnect Adjacent Channels

ASYMMETRIC HALF DISK
- 1/8th Period Min Features
- No Bars
- No Channel to Channel Interconnections
- 7/8th Period Disk Diameter

ASYMMETRIC CHEVRON
- Single Gap Per Period
- Gap Tolerant
- Intermeshed Adjacent Channels to Minimize Adjacent Path Interference

Fig 1b Half disk permitted four-fold increase in bit density over the T-bar with the same processing capability. Asymmetrical chevron adds another factor of improvement. The T-bar with 2 "gaps" per propogate period has been replaced in most labs by more efficient single gap structures. BTL uses the half-disk and its successor, the asymmetric chevron. ***(From A.H. Bobech, Development of Bubble Memory Devices, Electro 77.)***

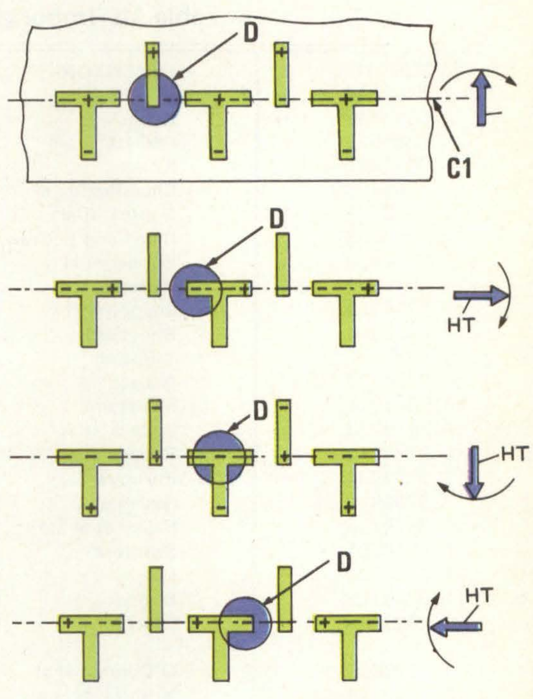


Fig 2. The transverse field, HT, rotates clockwise through 360 creating pole concentrations on the T-bar pattern. A domain, D, may occupy each position along the broken line, identified by the channel notation, C1, where a minus sign is shown. Minus signs represent the most intense pole concentration to which the domains are attracted. As the field rotates, the poles of the T-bar change according to the position of field HT, causing the domain D to be attracted to the minus sign and thus move to the right. Note that the same domain would move to the left if the transverse field is rotated counter clockwise.

Bubbles which are no longer to be used must be annihilated by increasing the bias field so that the total field exceeds the domain collapse threshold. The bias field can be increased by either applying an external current pulse or by inducing a collapsing field in a permalloy segment.

thrust of technology

Magnetic material limitations have presented significant obstacles to commercial realization of magnetic bubble devices. For example, very pure materials are necessary. Domains of less than 1 micron diameter, needed to obtain good memory density (up to 10^{10} bit/in^2), required that material imperfections affecting nucleation or propagation be smaller than the domain itself. This problem has been overcome through discovery of magnetic amorphous materials that do not contain structural imperfections that would impede the movement and nucleation of magnetic domains in the composition (patent 5).

Attempts to reduce stable bubble size at usual operating temperature have posed further problems. Operation near the magnetic reorientation temperature reduces bubble size but results in high magnetostriction, complicating both fabrication and operation. Operation near the reorientation temperature also results in a large temperature dependence of bubble size which in turn requires close temperature control. With garnet compositions, this temperature dependency can be reduced by partial substitution of the composition by Eu, Gd, Tb, Dy, Ho, Er or Tm ions in the dodecahedral sites (patent 6).

Yet another problem involving magnetic material limitations relates to finding materials that permit a required mobility, defined as an inherent speed factor of the magnetic medium. This factor, when multiplied by the applied field in the material results in a "velocity" term.

Table 1a Country Distribution of Patents

	By Patent Application Filing Date									Total	By Patent Grant Date										Total
	1965	66	67	68	69	70	71	72	73	65-73	1967	68	69	70	71	72	73	74	75	76E	67-76E
Total Patents	1	3	11	17	19	36	69	80	46	282			5	25	21	55	71	74	58	68	377
United States	1	3	11	17	19	35	60	52	36	234			5	25	21	51	55	55	42	52	306
Total Foreign						1	9	28	10	48						4	16	19	16	16	71
Japan						1	2	18	5	26						1	11	8	8	8	36
Netherlands								3	1	4								4	1	8	13
Canada							5	3	1	9						3	2	3	2		10
United Kingdom							2	3		5							3	2			5
Finland																			3		3
Switzerland								3	1	2								1	1		2
Germany									1	1								1			1
Italy									1	1									1		1

Table 1b Important Bubble Memory Patents

PATENT NO.	INVENTOR	ASSIGNEE	COUNTRY
1. 3460116	Bobeck et al	Bell Telephone Labs, Inc.	U.S.A.
2. 3543347	Bobeck	Bell Telephone Labs, Inc.	U.S.A.
3. 3555527	Perneski	Bell Telephone Labs, Inc.	U.S.A.
4. 3820091	Kohara	Nippon Electric Co., Ltd.	Japan
5. 3965463	Chaudhari et al	IBM Corp.	U.S.A.
6. 3646529	Bobeck et al	Bell Telephone Labs, Inc.	U.S.A.
7. 3964035	Blank and LeCraw	Bell Telephone Labs, Inc.	U.S.A.
8. 3886533	Bonner et al	Bell Telephone Labs, Inc.	U.S.A.
9. 3946372	Henry et al	Rockwell Int'l Corp.	U.S.A.
10. 3899779	Malozemoff	IBM Corp.	U.S.A.
11. 3618054	Bonyhard	Bell Telephone Labs, Inc.	U.S.A.
12. 3838407	Juliussen	Texas Instruments Inc.	U.S.A.
13. 3676870	Bobeck	Bell Telephone Labs, Inc.	U.S.A.
14. 3944991	Murakami	Nippon Electric Co., Ltd.	Japan
15. 3810133	Bobeck et al	Bell Telephone Labs, Inc.	U.S.A.
16. 3703712	Bobeck et al	Bell Telephone Labs, Inc.	U.S.A.
17. 3737882	Furuoya	Nippon Electric Co., Ltd.	Japan
18. 3909810	Naden et al	Texas Instruments	U.S.A.
19. 3879716	Bailey et al	Monsanto Co.	U.S.A.
20. 3940751	Sandfort	Monsanto Co.	U.S.A.
21. 3925768	Lin	IBM Corp.	U.S.A.
22. 3713119	Bobeck	Bell Telephone Labs, Inc.	U.S.A.
23. 3927398	Dimyan	Canadian Patents & Development Ltd.	U.S.A.
24. 3827036	O'Donnell et al	Rockwell Int'l Corp.	U.S.A.
25. 3763478	Yoshizawa et al	Hitachi Ltd.	Japan
26. 3943497	Yoshizawa	Hitachi Ltd.	Japan
27. 3934235	Bobeck et al	Bell Telephone Labs, Inc.	U.S.A.
28. 3946373	Moolenbeek et al	GTE Labs Inc.	U.S.A.
29. 3713120	Bobeck et al	Bell Telephone Labs, Inc.	U.S.A.
30. 3736419	Almasi et al	IBM Corp.	U.S.A.
31. 3953840	Cutler et al	Hewlett-Packard Co.	U.S.A.
32. 3840865	Holtzberg et al	IBM Corp.	U.S.A.
33. 3909809	Kinsner	Canadian Patents & Development Ltd.	U.S.A.
34. 3842407	Argyle	IBM Corp.	U.S.A.
35. 3936883	Heckler Jr.	Ampex Corp.	U.S.A.
36. 3798607	Minnick et al	Monsanto Co.	U.S.A.

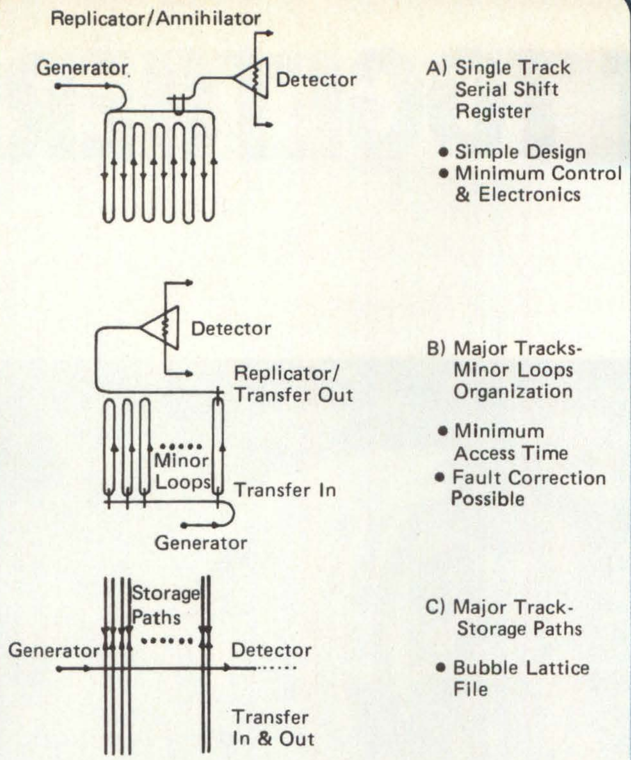
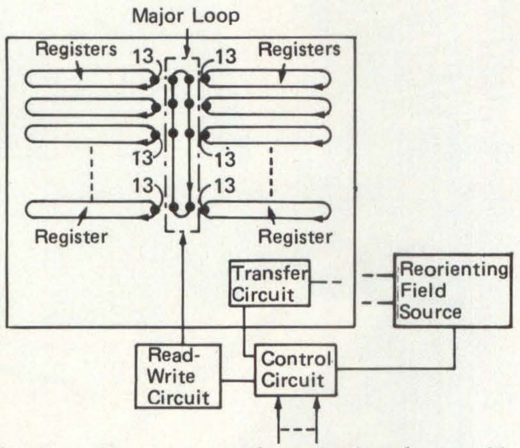


Fig 3a Field access chip organizations fall into three categories. Specific functions of bubble propagation, generation, detection and replication are generally used in serial shift register bubble chips. Advantages are a minimum of interface electronics, simple control logic and a relatively simple chip design. The main disadvantage is the access time although this is entirely adequate, for example, in an application such as voice storage. For applications requiring improved performmance the major/minor loop configuration isthe most frequent choice. Average access time with a 100kHz rotating field is 3.1 msec, a value comparable to that of a fixed head disk memory. This improvement in performance is obtained with an attendant increase in bubble chip complexity, interface electronics and control logic. (From A.H. Bobeck, Development of Bubble Memory Devices, Electro 77).



Popular major-minor type of organization of patent 11.

Fig 3b Memories of this type store information permanently in recirculating loops called minor loops. The information is selectively transferred to an accessing loop, called a major loop, where bubble generation, annihilation and sense operations occur through the use of an input-output circuit. The arrangement is such that the minor loops are a number of parallel channels to which the major loop is perpendicular. Subsequent to the generation or sense operation, information in the major loop is returned, via the transfer positions designated by numeral 13, to the minor loops for storage. Not only does this type of organization eliminate unnecessary external connections but it also reduce the ancillary control and utilization circuitry required.

This problem was overcome when a critically defined class of garnet compositions were found with sufficient high velocity to permit rapid movement of domain walls which results in high access rates. These compositions are characterized by the presence of europium in the crystallographic dodecahedral site and a reltively low magnetic movement contribution by the iron sublattices (patent 7). Garnet materials that exhibit both a high mobility and low temperature dependence of magnetization result from partial substitution of silicon or germanium for iron (patent 8).

While garnet materials have presently been found to be the most suitable for bubble memory applications, they form a domain that exhibits distinctly different behavior. These domains are called "hard bubbles". Hard bubbles have low mobilities and propagate at an angle to the applied bias field gradient. In addition, they strongly resist collapse, making them difficult to annihilate. Hard bubble suppression can be accomplished by selecting a composition based upon a characteristic temperature above which the bubbles are not generated (patent 9). However, a magnetic bubble system has been devised in which both hard and soft bubbles are used for the representation of information (patent 10).

One of the more important aspects of any memory unit is its organization. An efficient organization provides high packing density and fast access times. Many organizations have been presented, but one of the most popular is the major-minor type (patent 11), shown in Fig 3.

A number of modifications and improvements have been made to the basic major-minor configuration. For instance, one organization includes a major loop which does not close on itself, but which does pass each of the minor loops in the same order to provide two locations in each minor loop for bubble transfer (patent 12). Another configuration uses each transfer location by a conductor loop to ensure that a domain moves to the desired receiving positions and can later be returned to its original position (patent 13).

Still another major-minor loop memory is affected by selectively controlling the passage of bubbles through at least two gates provided between a bubble generator and the major loop in a two dimensionsal array (patent 14). A first gate of each memory in a selected row is conditioned for writing while a second gate in a selected column is conditioned in accordance with the data to be inserted. This arrangement permits new data to be inserted only into the memory of the array that is located at the intersection of the selected row and column. The result is the prevention, in a two-dimensional array, of an unnecessary transfer of bubbles in the major loops of an unselected magnetic domain memory unit. In some configurations a replication rather than a transfer operation is used, obviating the necessity of returning information to the minor loops and thus improving data rates (patent 15).

Mass memory units have been developed using a number of major-minor loop memories in an array. One such unit is operated in a word-organized block access fasion with noise cancellation detection (patent 16). Another magnetic domain memory, having a number of storage channels with major-minor loops, can be written into by one domain generating source, and read-out via one domain detecting means, without any relative time loss resulting from the distance of the storage channel from the detecting or generating means (patent 17). A redundancy bubble memory system has been developed which is composed of data chips having a major-minor loop organization and a flag chip which will prevent faulty loops from being read and used for data storage (patent 18).

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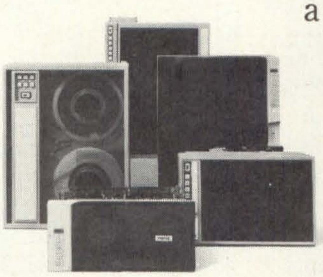

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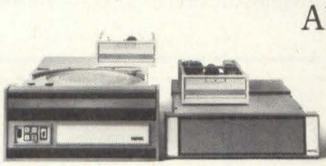

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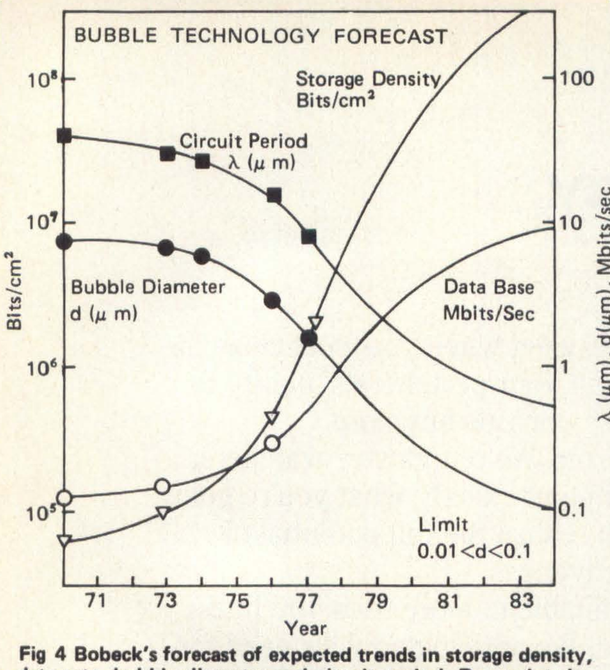

Fig 4 Bobeck's forecast of expected trends in storage density, data rate, bubble diameter and circuit period. Datapoints indicate achievements to date.

The need to propagate bubbles in one or more recirculating minor loops without operating other loops has led to the development of different types of propagating circuits. One such circuit is a mutually exclusive closed loop field-accessed type which uses a magnetic bubble overlay circuit element nicknamed the "crow-foot". This element has a straight bar or stem portion with a pair of angled arms in the form of staggered barb-like projections (patent 19). These "crow-foot" circuit elements can be used to build closed loop paths with parallel sides that propagate bubbles in opposite directions with the same set of pulsed drive fields (patent 20).

All propagation structures mentioned so far have gapped permalloy patterns; however, these patterns are characterized by a number of disadvantages. For one, the bubble diameter must be substantially larger than the gap width in order to traverse it. In addition, a bubble must be elevated to a higher energy state to traverse a gap which renders it momentarily less stable. To overcome these problems, a double-sided gapless propagation structure was developed. Propagation is achieved by using two identical disc circuits on opposite sides of the bubble material displaced from each other by one-half of periodicity (patent 21).

Other propagation structures have been disclosed. For example, enhanced operating characteristics are obtained if the extremes of the permalloy patterns are of enlarged geometry to concentrate flux (patent 22). Further examples are propagation structures consisting of magnetic material bars positioned over the bubble supporting material (patent 23). While yet in another example, a propagation circuit is defind by grooves extending partially into a thin film of magnetic bubble material (patent 24).

In propagating magnetic domains through the use of permalloy patterns and in plane rotating fields, power consumption of the driving circuits which produce such fields is of primary importance. The circuit for creating rotating magnetic fields commonly includes a pair of coils which are positioned perpendicular to each other and an AC current source for supplying current to these coils. A separate current is supplied to each of the coils which are 90 degrees out of phase. The total effect of the individual magnetic fields from the current in each coil is a rotating magnetic field vector which extends throughout a region into which the bubble memory is disposed. A driving system which reduces power consumption is formed by connecting resonating capacitors to the two coils that form the field (patent 25).

In a large bubble memory system which is divided into smaller memory elements, reduction of power consumption can be achieved by providing each smaller memory element with its own driving coils which are adapted to be selectively energized only when a memory-refer is made (patent 26).

Bubble memories are known to be nonvolatile. That is to say, bubble memories retain information even when a power failure occurs. It is important, however, to ensure the in-plane field stops and starts in the same reorientation to avoid loss of information. A reactive-coupled pair of tuned circuits can be used to drive a magnetic bubble memory. Refresh pulses can then be extracted conveniently from the parallel tuned circuits to ensure the same reorientation (patent 27). Another control circuit which insures such reorientation uses a DC current supplying circuit along with the AC current source at the beginning and end of the operating mode (patent 28).

Another difficult problem facing practical implementation of magnetic bubble devices is sensing the bubble. Despite ėfforts to minimize bubble readout or sensing by incorporating logic in the memory to enhance the informational content of each bit, a reliable sensing unit is still necessary. The basic problem is the small magnetic field associated with a single miniscule magnetic bubble. This field is barely distinguishable from the background noise which, by itself, represents the absence of a bubble. The magnetoresistive effect is perhaps the most effective method of bubble detection. A relatively large output signal can be achieved from an expanded magnetic domain by a relatively long magnetoresistance element in the path of the domain (patent 29). Noise cancellation is possible through the use of two magnetoresistive sensing elements

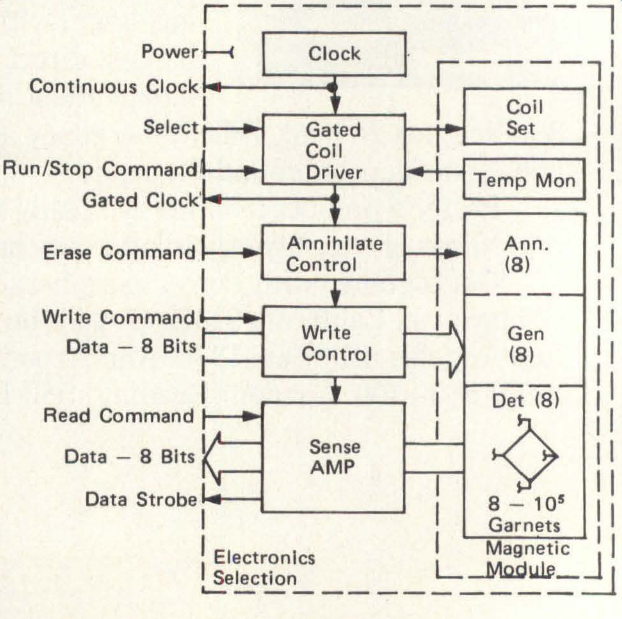

Fig 5 POS Block Diagram

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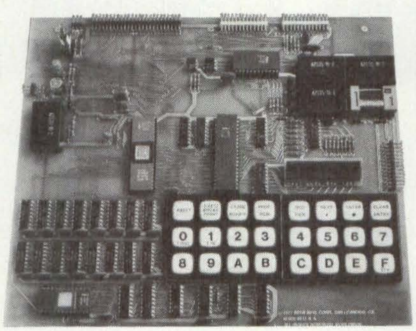

lines, 5 heavy duty relays, and Teletype and audio cassette interfaces. Plus, a 24 pad hexadecimal keyboard and a 9-digit LED hex display. All on one board.

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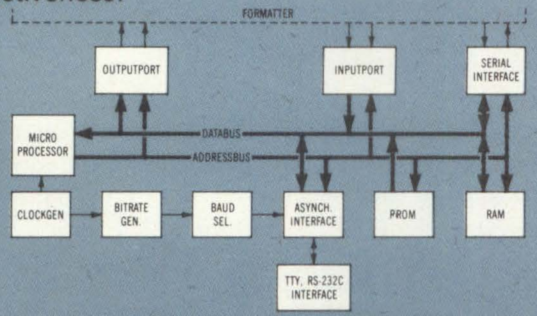
There's a complete family of interfaces for the Tandberg TDC 3000. From the original design conceived by Tandberg of Norway, the $150-million electronics firm that pioneered tape recorders internationally. The company that is to high quality electronic equipment what Rolls Royce is to automobiles. With a tradition of excellence that continues in a wide range of computer peripherals from Tandberg Data in the United States.

With total communications compatibility, the microprocessor-based RS-232 controller/interface from Tandberg Data is engineered according to EIA Standard RS-232-C, type D and E, and a "teletype-compatible current loop," recording in ANSI/ECMA/ISO-compatible format.

And from the substantial savings in line charges alone, the TDC 3000 with the RS-232 controller/interface will recoup its modest cost in a matter of months. It's hard to beat that kind of cost-effectiveness.



The Tandberg controller/interface is contained on one p.c. board which mounts inside the Recorder. Power is internal from the TDC 3000 built-in power supply. Two interface connectors are provided so that the Recorder can be connected both to a local I/O terminal (such as the Tandberg TDV 2100 Series CRT terminals) and a modem for remote operation.

Thirteen standard baud rates, 75-9600, are user selectable. Data buffers range from a minimum of 256 bytes up to 1024 bytes. The controller/interface responds to all ASCII command codes. Read and write speed is 30 ips and search speed 90 ips.

And for special communications requirements, the 6800 microprocessor allows the Tandberg controller/interface to be OEM-customer programmed.

Conceived in the rugged Norse heritage, the Tandberg TDC 3000 is no wilting lily when it comes to tough environments. Put it to work in subzero snow country or under a desert sun and don't worry about the bad vibes or emissions from nearby equipment. The TDC 3000 is engineered to roll with environmental punches.

You might ask us about some of our more difficult applications. Modular construction of the TDC 3000 enables the user to configure a system to individual needs. Applications include minicomputer input/output, minicomputer peripheral storage, terminal peripheral storage, software distribution, data entry via keyboard, local data collection, data transmission, and text editing. And a few other things yet to be dreamed up.

Besides RS-232, Tandberg Data provides TDC 3000 interfaces for HP 21MX, PDP 11, Alpha LSI 2, and 8-bit parallel general purpose. All give up to 48K bits transfer rate.

Tandberg Data Inc.
4060 Morena Blvd.
San Diego, California 92117
(714) 270-3990

Shown in test position.

Mr. Bruce B. Greenfield, Vice President, Tandberg Data Inc., 4060 Morena Blvd., San Diego, CA 92117

I'd like to know more about the RS-232 controller/interface for your TDC 3000. Please send me the RS-232 data sheet and have a Tandberg engineer give me a call to discuss my needs.

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Computer/terminal type__________

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whose combined voltage or current output is constant in the absence of a bubble domain (patent 30). In this respect, a differential detection device connected to a pair of adjacent permalloy columns is used to determine the presence or abasence of a bubble (patent 31).

Alternate methods of sensing the magnetic bubble have been investigated. In one case, detection of the domain is accomplished by using tunnel junctions in which the Fermi level of one or both the electrodes is changed due to the bubble (patent 32). Sensing can also be accomplished by first converting the energy associated with a bubble into mechanical energy, and secondly by converting the mechanical energy to electrical energy to indicate the presence of a domain (patent 33). In yet another sensor, the magnetic bubble is oscillated in size to cause a change in the self-conductance of a conductor loop which is used as the oscillator (patent 34).

technology trends

A little over 10 years ago – in October 1967 – the first article on the device applications of magnetic bubbles appeared in the Bell System's technical journal. It was authored by A.H. Bobeck, a frequent contributor to advances in magnetic bubble state-of-the-art. Since that time, magnetic bubble memory development has grown rapidly and will unquestionably continue to do so. Magnetic bubbles, like CCD memories, can find application in both central processor units and in-line bulk memories. Unlike CCD memories, however, this technology is expected to replace magnetic drum and disk memories. Magnetic bubbles, more versatile, are now used to write and read digitized signals of audio, Video and digital data as described in patent 35. And patent 36 describes a relatively recent magnetic bubble computer.

Last month at Electro '77, Bobeck, still at Bell Laboratories in Murray Hill, NJ contributed another paper on the development of bubble memory devices. He pointed out that Rockwell and BTL/WE have announced memory systems based on serial bubble shift register chips. And Hitachi, Fujitsu, NEC, Philips, HP, TI, Rockwell, Univac and BTL are among those developing designs based on major-minor organizations. Texas Instruments has pioneered the "fault tolerant approach" to memory system architecture.

Bobeck's extrapolation of the rate at which the bit storage density has increased from 1973 to 1977 forecasts that bit density 5×10^7 bit per cm^2 and 4×10^8 bits per cm^2 would be reached in 1980 and 1985 respectively. The latter implies a bubble diameter of 0.1 μm still considerably greater than the theoretical limit of approximately 0.01 μm. Advances into mid-1980 could be made with routine extensions of the presently used epitaxial garnet films and bubble circuitry. Bobeck reported that the anticipated limitation is expected to be in circuit patenting, and systems such as electronic beam exposure systems will require continued evolution to meet these needs. Single mask, self-structuring and lattice circuits may ease the lithographic requirements.

Bobeck forecasts that bubble chips with 10^8 bit capacity should be state-of-the-art by 1985. But he cautions that we need not wait that long for something useful to materialize for single chip packages equivalent in capacity to the floppy disk should appear this year and multi-chip packages of 10^7 bits or greater should be commonplace by 1979.

Bell Laboratories in Whippany, NJ is developing another bubble data storage system to meet the requirements for low-cost, non-volatile memory in micro processor-based systems. At Electro,'77 J.E. Williams reviewed the first Bell System application of magnetic bubbles in their 13A announcement system with emphasis on how they solved several long standing problems with recorded voice announcement systems. His paper describes a low cost, 272 kbit sequential memory system (Serial Bubble Store) and illustrates magnetic bubbles applied to satisfy requirements for nonvolatile, electrically alterable sequential memory.

systems applications

One of the major driving forces in developing bubble technology has been the needs of the U.S. National Aeronautical and Space Administration (NASA). Wm. C. Mavity of Rockwell International's Autonetics Group, reports that they are now designing for NASA Langley Research Center a space qualifiable 10^8 bit recorder which has the characteristics of Table 2. Composed of four basic modules, it contains 50 million bits. Completing the memory is one module for logic, timing, and control and one for the power supply. The "memory cell" which contains a bias structure/drive coil set and 16 chips, contains 1,638,000 bits. The complete memory contains 64 cells and has an estimated MTBF of 40,000 hours. Should any cell fail, the system loses only 1.5 percent of its capacity. Thus the usability of the memory extends far beyond the 40,000 hours. Among the features implemented are reconfiguration capabilities for one to four independent organizations (one memory of 100 million bits to 4 memories of 25 million bits), dual buses throughout, override of failed cells in steps of 1.5 percent of capacity, and full status monitoring. The flexibility of the system architecture allows the design to be utilized for over 95 percent of the missions now using a number of different recorders. Present schedules expect the first unit to be operational in early 1978. Full utilization is anticipated by users in 1979.

For the potential user who wants laboratory "hands-on" experience with bubbles, Mavity reported that Rockwell is

Table 2 Solid State Data Recorder Characteristics

Capacity	104,857,600 Bits
Format	
Serial	1-4 channels
Parallel	1, 8-Bit Byte
Data Rate/Channel	1.2 MHz
Max. Data Rate	2.4 MHz
Interface	TTL
Voltage	28V ± 4V
Power	103 Watts max. @ 100% duty cycle and Linearly variable with duty cycle and data rate
Volume	600 in^3 ≈ 0.01 cu. meter
Weight	40 lbs. ≈ 18.2 kg.

Table 3 POS/8 Characteristics

Capacity	819,200 bits
Format	Endless loop/byte parallel
Data Rate	100K Bytes/sec 800K Bits/sec
Interface	TTL
Voltages	+5, –5, +32V, ±2%
Power Dissipation	29W max. @ 100% duty cycle and linearly variable with duty cycle
Volume	50 cu. in. ≈ 820 c.c.
Temperature	0°to 50°C
Weight	2.5 lbs. ≈ 1.14 kg.

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Whether you buy an entire system up front or choose to expand gradually, it's easy to get the configuration you need with the complete family of Altair peripheral equipment, including floppy disk, line printer, audio cassette record interface, A/D converter, PROM programmer, serial and parallel I/O boards, choice of four different memory boards and many others.

Reli-ability:

The unique design features of the Altair 8800b, which have set the standard for the microcomputer industry, make it the most reliable unit of its kind. The Altair 100-pin bus, the now-standard design used by many imitators, has been "standard" all along at MITS. The unique Front Panel Interface Board on the Altair 8800b isolates and filters front panel noise before it can be transmitted to the bus. The all-new CPU board utilizes the 8080A microprocessor, Intel 8224 clock generator and 8216 bus drivers.

Flex-ability:

Meeting the diversified demands of an ever-increasing microprocessor market requires flexibility; not just hardware flexibility but software flexibility as well. MITS software including the innovative Altair BASIC lan guage, allows the full potential of the Alta 8800b computer to be realized.

8K ALTAIR BASIC has facilities for variabl length strings with LEFT$, RIGHT$, and MID functions, a concatenation operator, an VAL AND STR$ functions to convert betwee strings and numbers.

Extended ALTAIR BASIC allows integer, singl and double precision variables, automati line numbering and renumbering, use defined string functions, PRINT USING for fo matted output and a powerful EDIT com mand for editing program files during or aft entry. Extended statements and comman include IF . . . THEN . . . ELSE, LIST and DELET program lines, SWAP variables and Trace O and Off for debugging.

Disk ALTAIR BASIC has all the features Extended BASIC with the additional cap bility to maintain sequential and rando access disk files. Utilities are provided f formatting disks and printing directories.

In all versions of ALTAIR BASIC you get th ease and efficiency of BASIC for the solutio of real world problems.

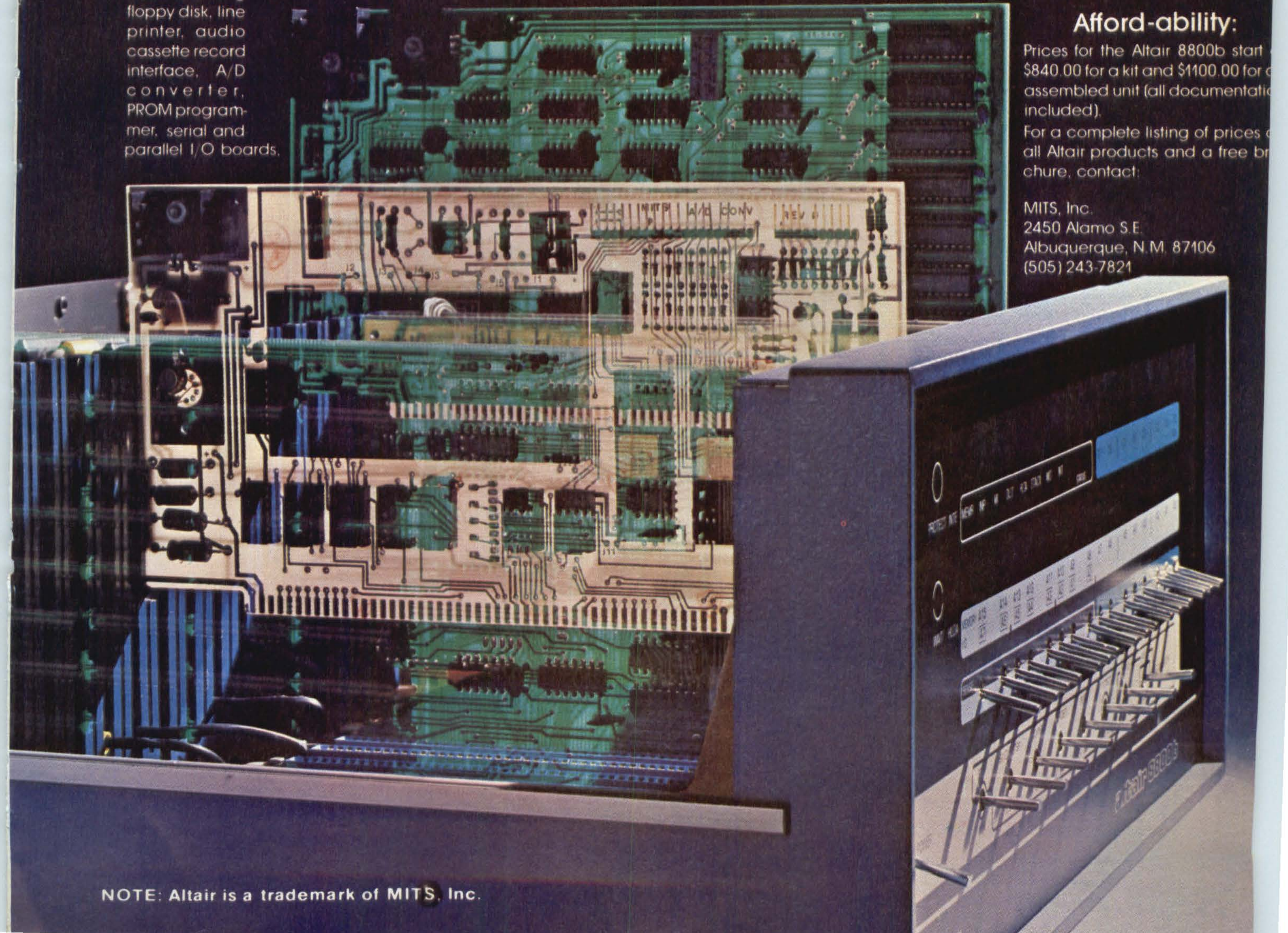
Package II, an assembly language develop ment system for the Altair 8800b, include system monitor, text editor, assembler an debug.

Afford-ability:

Prices for the Altair 8800b start $840.00 for a kit and $1100.00 for assembled unit (all documentatio included).

For a complete listing of prices all Altair products and a free br chure, contact:

MITS, Inc.
2450 Alamo S.E.
Albuquerque, N.M. 87106
(505) 243-7821



NOTE: Altair is a trademark of MITS, Inc.

now producing an 8 x 10^5 bit recorder organized as an endless loop of 10^5, eight-bit bytes. In addition to its usefulness as a technology proof article, it has direct application as the operating mass memory for microprocessor or microcomputer systems. Characteristics of this memory, the POS/8, are shown in Table 3. Of particular interest is the varied possibilities of power consumption. The peak power shown will completely fill or empty the memory in one second. In most situations the memory will be operated in bursts. When idle, the memory dissipates no power. The duty cycle of actual operation is an improtant item to linearly factor into long-term power dissipation, especially in applications utilizing a battery power supply. For many applications the duty cycle is much less than one percent.

A block diagram of the memory is shown in Fig 4. The operation of the memory is straightforward. Enabling the select line brings the memory to operational readiness and starts the clock. Start/stop set to true starts data circulating and enables a gated clock that occurs at the beginning of each cycle. Coincident "trues" on combinations of Read, Write, and/or Erase causes data to be placed on the Data Out bus with strobe, data to be written from the Data In bus, or data to be erased from the memory. As an endless loop of data the addressing is left to the user to format. Fixed, variable, or unique block addressing via data header or counters, can be implemented. A complete description of the memory and details on testing and achieved margins can be found in the recent paper by Ypma and Swanson.

pos/8 applications

In industrial applications the memory finds application as a large (relatively) memory for a desktop calculator where larger or many varied programs could be permanently stored for day to day use. The electronic notebook or electronic routebook could also utilize the POS/8 units. The routebook is of interest as it can be programmed each evening for the route a field sales representative would cover the next day. Order, inventory, and return information can be collected for use by the home office. Also in this general recorder application area would be a configuration where daily transaction records of commercial sales would be contained at a terminal via a POS/8. The POS/8 memory would provide the basic record that allows reconstruction of transactions in the event of system outages more central to the accounting function.

The POS/8 is the ideal operating mass memory for a mircroprocessor. Its usage is shown in Fig 6. In many instances the need for program ROMs is eliminated as the POS/8 can be bootstrapped during start-up and then program swaps can be utilized for operating programs. The multi-level hierarchies of many larger computer systems can now be implemented in a microprocessor system. Expensive main memory capacity can be reduced and replaced by inexpensive bubble secondary storage where access is controlled via a swapping algorithm. Many applications will continue to use flexible disks and cassettes for off-line storage. But a solid state secondary bulk memory, provided by bubbles, allows full system utilization with no concern for the maintenance of moving parts. The design is sufficiently flexible to allow unique user adaptation.

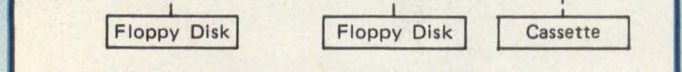


Fig 6 Microprocessor Application

One of the most interesting system applications is the stand alone terminal for small retail business firms. The one register operation of shoe stores, restaurants, "Mom & Pop" groceries, etc., will require non-volatile, on-line storage in their terminals. Price table lookup, transaction, and inventory control can be included in the terminal function via the secondary storage.

The automated office of the future will require on-line, high usage, non-volatile mass storage that, for reliability reasons, is best implemented in a solid-state technology. One can envision that the office typewriter will be soon replaced by the office terminal – complete with video display, keyboard, and prenter. Memos in process, appointment calendars, telephone and address records, travel arrangements, etc., will all be incorporated and it will be imperative to be able to swap data bases with the speed of a push button, Mavity emphasized.

The quickly growing personal computing technology will similarly require secondary storage that bubbles can provide – as will the other terminal applications based on the microprocessor.

controller considerations for the pos/8

Since the POS/8 is essentially an endless loop of 102, 400 eight-bit bytes operating at a fixed frequency of 100 KHz, the user can choose among many sets of options in organizing his data and usage. He can then design an appropriate controller to interface the POS/8 to his system.

The initial decision concerns the basic operating modes. Some users may want an incremental recorder where the unit is started, cycled once for reading or writing, and then stopped. Others may require a Block Record mode where the memory is started, cycled for a burst transfer, and then stopped. A sub-decision in this mode is whether the block length is fixed via hardware design or variable via software control. Also to be considered is the basic transfer method, i.e., via Programmed Input/Output where software moves data through the microprocessor or via Direct Memory Access (DMA) where non-CPU hardware functions as the transfer controller.

Another set of decisions must be made in organizing the data or blocks. Since the memory is an endless loop it may be desirable to have an overall index mark entered via software. In basic serial recorders they may not be necessary as the presence of a non-all-zero byte may be sufficient if the memory is not totally filled. In block oriented usage where ASCII is used there are definitive characters for Start of Data, End of Block, etc. that are sufficient. In those applications not using ASCII there are many other possibilities for record identification. Among them are counting cycles from an index mark, establishing a start-of-record (SOR) mark (8 bits) which is forbidden data; SOR followed by address or key word (a known combination of characters); or SOR, keyword and block length. If the memory is divided into fixed blocks an SOR character can also be identified by the repeatability of the character every known block length. In

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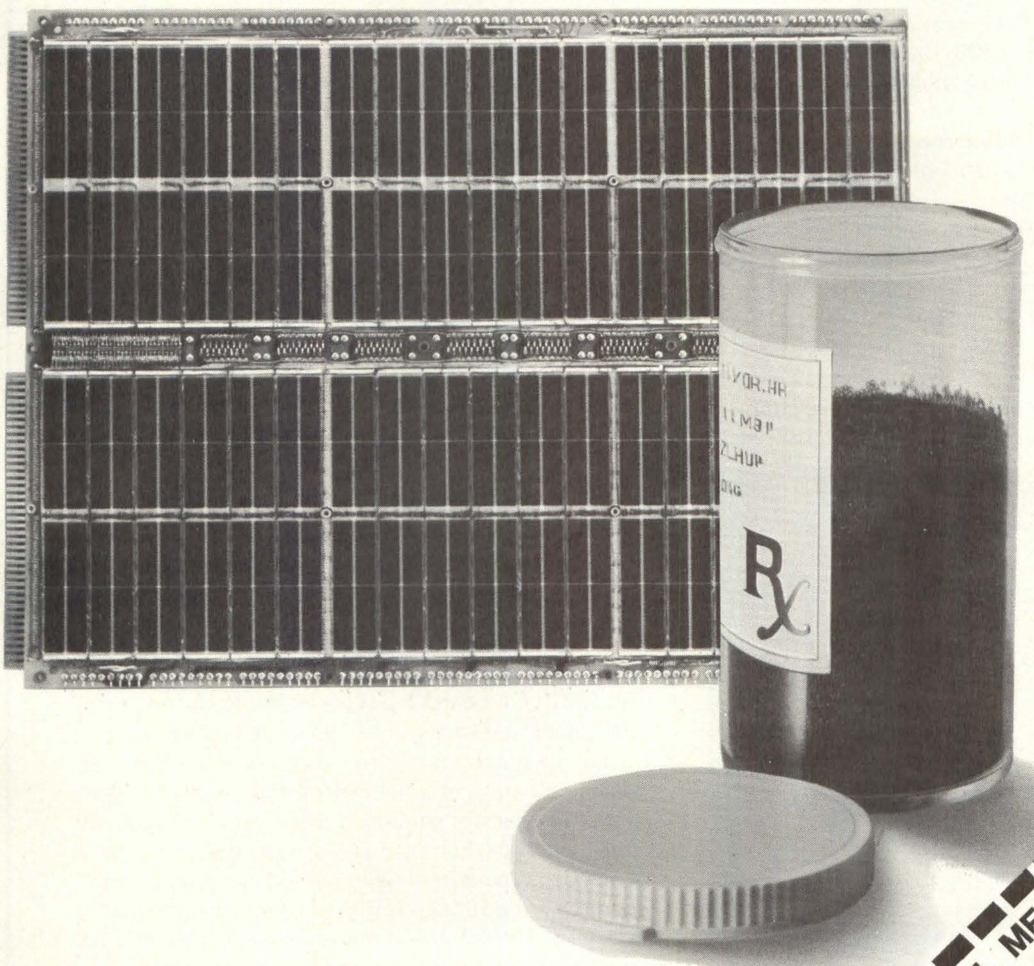

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this form the SOR can also be valid data with extremely low probability of misidentification.

In a block record system the user can also consider the addition of useful non-data characters to add features such as Longitudinal Party, Cyclic redundancy codes, write protection codes, supervisor key codes, etc. Some users may want this information sent to the using hardware, others may want it stripped and only valid "data" sent as in mapping or swapping into memory.

The above mentioned features make two requirements on the overall system application. First, data storage efficiency is decreased when non-data bytes are stored with the data. For example, if data is formatted in 256 byte blocks, the POS/8 can store 400 blocks. If an index mark is required, 399 blocks plus some slack are available. If each block had an address of 3 bytes (enough bits to code binary 400) appended to it; 395 blocks + 95 bytes (used for the memory index) would result. A memory block could be formatted as shown in Figure 7. This configuration allows SOR, address, data, Check Code and two null characters. The null characters are required only in the case where the memory is stopped at those points in the record. This results in a 268 character block. The memory could contain 382 blocks with 24 characters left over for an index pattern. A data efficiency of 95.5 percent results.

The second requirement is that the decision making or intelligence in the controller must be high speed. A bipolar bit slice processor and discrete hardware could do the job.

A more exhaustive discussion of controllers for the POS/8 can be found in the recent paper by Norton.

Mavity believes that future generations of bubble products are assured by the technical accomplishments to date in the research laboratories. Advances are being made to not only make the first generation of products even more cost effective, but also to show proofs of second generation technology

Here are Mavity's basic rules-of-thumb that can be used to assist in defining a technology generation:

• Bubble film thickness is approximately 0.8 of the bubble

Texas Instrument's First in Commercial Market

In the meantime, Texas Instruments has applied their TBM 0103 magnetic bubble memory to two data terminals trademarked Silent 700. Claiming them to be the first known commericial application of bubble memories in the computer industry, each terminal comes standard with 20,000 bytes of non-volatile bubble memory storage expandable to 80,000 bytes in 20,000-byte increments.

The memory data terminals combine TI Silent 700 experience with the advantages of magnetic bubbles to bring electronic data storage to terminals which heretofore required the use of larger, more expensive media such as cassettes, paper tape or floppy discs. The 763 or 765 terminal can access any indexed record in memory in less than 15 milliseconds, compared to a search time from several seconds to several minutes for a cassette system. If the data location in the 763 or 765 memory is not known (not indexed), the character string search speed is 1000 characters per second, about four times the speed of a cassette search. Compared to a floppy disc, the bubble memory indexed record access time is more than ten times faster, but total data transfer rates are lower.

Fig 7 Designed for portable use, TI's 765 terminal includes a carrying case and built-in acoustic coupler. Table-top version, the 763, is designed for office applications not requiring portability.

TI said that applications for the new terminals include timesharing, real estate inquiry, newspaper reporting, wholesale and retail order entry and credit verification, and insurance inquiry. TI also explained that any application can use data entry during daily use, off-line from the host computer. The stored data then can be transmitted to the home office computer over standard telephone lines at a speed of 30 characters per second (300 baud) via the built-in acoustic coupler on the 765 terminal, or at 120 characters per second (1200 baud) with either terminal when connected to an external modem. This off-line data entry and transmission speed reduces computer connect time and telephone line charges compared to on-line keyboard data entry.

At only 17 pounds, the Model 765 Portable Memory Terminal is a fully capable 30-cps terminal with a full ASCII keyboard, a built-in numeric cluster, a virtually silent thermal printer, acoustic coupler, carrying case and a powerful editing capability. TI added that the combination of a file management system and a powerful operator command mode provide excellent user flexibility. For example, an operator using the terminal's typewriter-like keyboard can select communications options, configure memory, and enter or edit text. The command mode also includes a self-test capability to minimize system downtime and reduce service calls.

Production deliveries of the new terminals are scheduled for the fourth quarter, 1977. Quantity one U.S. Domestic price with 20K bytes of bubble memory are $2995 for the Model 765 Portable Memory Terminal, and $2695 for the Model 763 Memory Send-Receive Terminal. Both terminals are expandable to 80K bytes of memory at $500 per 20K byte increment.

512K x 22 and you'll love every bit of it.

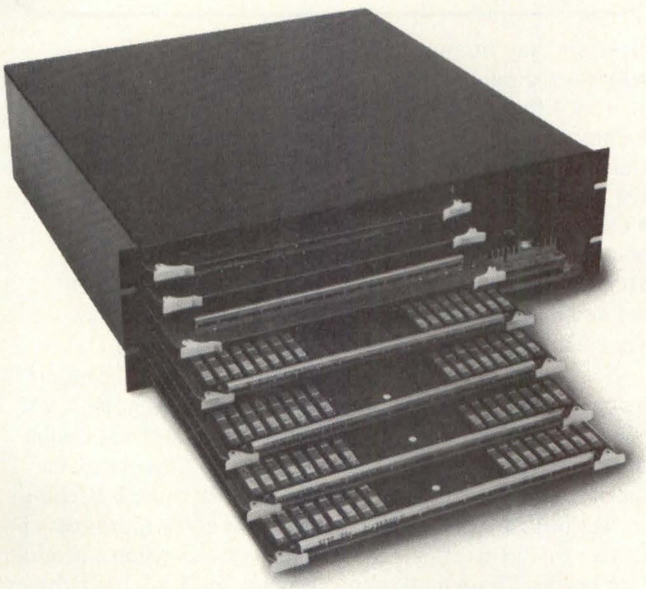

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Table 4 Mavity's Bubble Memory Applications Matrix

Chip	Type I	Type II
Type	Serial Loop 100,000 Bits	Block Access 65,536 Bits
Memory	100 kHz,	300 kHz,
System	1/2S Access Time	1-mS Access Time,
Size	1/4 in. x 1/4 in.	1/4 in. x 1/4 in.
TYPE A	Solid State cartridge recorder	Smart Terminal Mass Memory
	Small, severe-environ-ronment recorder	Distributed processing Memory
	Unattended data gatherer	Tactical message switching
$3x10^5 \rightarrow 3x10^6$	Microporcessor Mass Memory	Store and Forward Memory
TYPE B	Graphic display buffer	Minicomputer program and data file
	Re-entry test vehicle recorder	
$3x10^6 \rightarrow 3x10^7$	Interim STP experiment	Electronic Swapping Memory
TYPE C	Satellite data recorder	Fast auxiliary mass memory
$3x10^7 \rightarrow 3x10^8$		Electronic head-per-track disk
TYPE D $3x10^8 \rightarrow 3x10^9$	Second generation	Second generation

diameter they support.
- Bubbles should be constrained to be separated by approximately 4 to 4.5 bubble diameters.
- Conventional T-Bar storage elements require that the separation between elements, i.e., the gaps, be approximately 1/4 the bubble diameter.
- Conventional photo-lithography allows processing of a one micron gap.

Thus, 4 micron bubbles on 16 micron periods has been defined by Rockwell as its first generation technology. They have standardized on a chip size of (0.25 in).

The "gap tolerant" circuit elements reported separately by Gergis and Bonyhard, at the 1976 Joint Intermag/MMM conference allows gaps to be approximately 1/2 the bubble diameter. This property can be utilized to either relax the fabrication tolerance requirements or pack more bits/chip. In fact both are being done. Larger gaps allow more cost effective first generation products to evolve as volume production begins. These mask improvements for 4 micron bubbles are now in design.

Mavity feels that larger capacity chips will also be perfected based on several concepts. The concept of using block access chips composed of small loops which interconnect to an input/output track via replicate/transfer switches is well known. The major/minor loop chip was the first design using the principle. When the replication feature was added, the need for a major loop was negated. External ordering of data allowed for redundancy designs which further enhanced yield at the cost of electronics complexity. The concepts of gap tolerance, replication, and redundancy have recently been combined in the design of a one-million bit chip by Rockwell scientists.

Mavity says we can expect that these principles can be extended further to chips approaching 10 million bits capacity as techniques such as E-beam mask making and X-ray lithography are brought on-stream allowing sub-micron gaps to be fabricated. While systems using these advance design chips will not appear in the field until the early 1980's, it should be reassuring to all potential users that future generations of equipment will be forthcoming.

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Cheap Hardcopy For uP-Based Systems

Everything you need to know about low-cost impact line printers, including how they can provide reliable hardcopy capability without skyrocketing a microprocessor system's cost.

by **Peter Engstrom**

If you're designing a microprocessor based system that must provide alphanumeric hardcopy output at a cost that puts a computer-type line printer out of your system's ballpark, consider using a low-cost impact line printer (LCILP). Today's LCILPs cost less than $200 in unit quantities and can provide 15- to 40-column alphanumeric records at about 1.6 lps. Their reliability – proven in similar numeric printers – is high, and their interfacing costs are low, particularly in those cases where a microprocessor system's logic provides the required interface. In such systems the only additional hardware required is a few power transistors to drive the printer solenoids. As an additional advantage, an LCILP's printer mechanism often measures no more than 3"x6"x6", so you can often package the unit as a part of its host equipment.

With these major capabilities, alphanumeric LCILPs can serve many applications that don't require a full-fledged line printer. Such applications include point-of-sale terminals, weighing systems, data loggers, automated banking equipment, printing calculators and telecommunications recorders. I'll focus here on impact printers and won't discuss low-cost thermal and electrostatic printers, because those units form a separate class of devices.

what is an LCILP?

A typical LCILP (Fig 1) can have one of three kinds of basic print mechanisms; it can either use a matrix of individually driven "needles," a series of print wheels or a solid drum. Because I'll focus primarily on LCILPs that can find use in fairly demanding industrial environments, I'll only consider the two latter types.

A wheel printer (Fig 2) has one print wheel and one hammer for each column it prints. Around the circumference of each wheel lie between 12 and 20 characters or other symbols, a subset of the full alphanumeric alphabet. No one wheel contains the full character set, because the wheel diameter would become excessive and would create problems with speed, response time and power to drive the wheels (one solenoid typically drives each wheel).

Each line of data is printed sequentially; a wheel is positioned by its solenoid in steps until the desired character faces the corresponding hammer. Then the wheel is stopped and the hammer strikes the inking ribbon (or paper directly, if the printer uses the so-called "action" paper), and the struck character is printed. This operation repeats for each wheel (column) until a complete line of data is printed. Paper is then advanced and the whole process repeats.

In general, wheel printers suffer from two major disadvantages. They are slow, because stopping and starting each wheel forms part of each printing cycle. Some of the fastest wheel printers output about 1 lps. And their character sets are generally limited to about 20 symbols. So their use is largely restricted to applications that require mostly numeric data with limited alphanumerics.

In a solid-drum printer (Fig 3), fully formed characters or parts of characters ("line matrix" elements) are also arranged in rows around the circumference of a drum. If fully formed characters (symbols) are used, such drum printers suffer from the same character-set limitations as the print-wheel devices, because the drum diameter must remain small. If a line matrix is used, then with about a dozen elements (lines of the line matrix) a printer can generate a complete ASCII character set.

In such drum LCILPs that use a line matrix, the drum is continuously driven by a small (about 10W) motor. As the drum rotates, a drum-position encoder (typically a photoelectrical unit) tells the control electronics when the desired matrix element faces the corresponding hammer. The selected hammer strikes the ribbon when it receives a hammer-strike command from the control, and some part of the character is printed. This process continues until a complete character is printed.

One advantage of this approach is its higher speed – about 1.6 lps. Another is its simplicity – instead of using individual

Peter Engstrom *is product manager at the Sodeco Div. of Landis & Gyr, Elmsford, NY.*

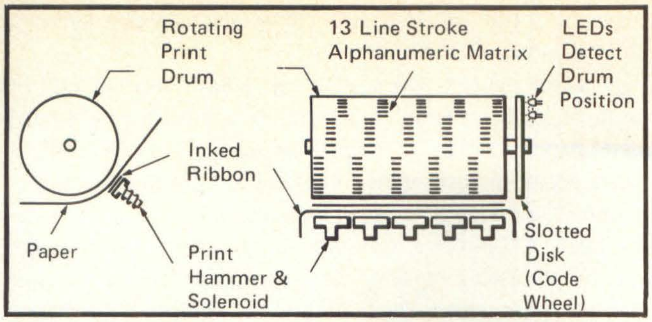


Fig 1(a) Typical solid-drum low cost impact line printer uses a line matrix to form characters by striking an inked ribbon when the desired matrix element faces the hammer. Printing occurs "on the fly," at about 3 lps. (b) Commercially available low-cost impact printer outputs 15-column lines in two colors.

coils to drive each wheel, the drum is driven by a single motor. Equipment simplicity, of course, translates into higher reliability.

Another advantage of this design is that it uses fewer hammers than columns. In our own 15-column printers we use only five; each hammer spans three rows of characters. This design also simplifies the hardware and the configuration of the interfacing logic, with an attendant increase in operating reliability. Finally, a drum printer is inherently more precise in terms of character-to-character positioning.

read messages loud and clear

Other considerations aside, any line printer must be able to form clear, easily readable characters. And in most applications, multiple copies are desirable, which is one reason why I'm not considering thermal and electrostatic LCILPs here. So you must understand how characters are formed before you consider purchasing an LCILP.

An alphanumeric LCILP can form characters either with a line matrix or a dot matrix. The latter method has an advantage in the sense that a standard 5 x 7 dot matrix can generate almost any character and can even be used to plot curves. But as I've pointed out, dot matrix printers are rather delicate instruments and thus cannot be used even in mildly severe environments. Thus, I'll concentrate on drum LCILPs.

Fig 4a shows elements of a line matrix used in our alphanumeric printers, while Fig 4b depicts the 54-symbol character set that can be produced from those elements. To understand how characters are formed, consider how an "E" is written.

Each element in Fig 4a has two associated timing slots, numbered zero through 25. Thus, certain elements can be printed in two positions, depending upon which timing slot generates the hammer-strike command. In each case, the first timing slot (#6 in the case of a horizontal bar that is used to form an "E") corresponds to the *leading* edge of the timing pulse generated by the corresponding slot in the encoder wheel. The second slot (timing slot #7) corresponds to the trailing edge of the same timing pulse. The time interval between the leading and trailing pulse edges is such that if the hammer strikes in response to slot #6, the horizontal bar is printed as shown in Fig 4a; that is, in its "normal" position. If the hammer strikes in response to a command produced by the pulse's trailing edge, the bar is printed in the middle of a given character space (in the case of letter "E" this corresponds to the center bar).

Thus, during the drum's first revolution, the upper bar (timing slots #24 and #25), the lower horizontal bar (timing slot #6), and the lower portion of the vertical side of letter "E" (timing slot #12) are printed. During the second revolution, the mid-portion bar (slot #7) and the upper part of the vertical side (slot #13) are formed, thus completing the "E."

Characters in a typical LCILP measure about 0.100" high by about 0.080" wide. In general, dot-matrix characters are somewhat larger, because the dot matrix inherently has some "holes" in it; each character is formed from dots, so for the same degree of legibility, each character must be a bit larger.

Paper width depends on the number of columns that the printer outputs. A typical 15-column LCILP accepts paper tape about 2.75" wide and about 4 mils thick. In most cases,

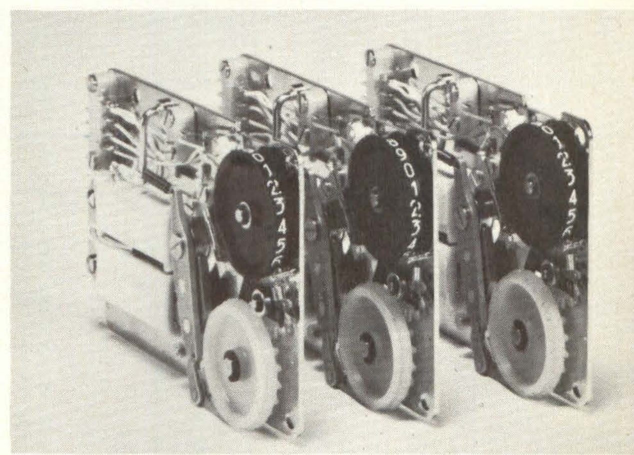


Fig 2 Wheel print mechanism has alphabetic or numeric symbols (up to 20 per wheel) arranged around each wheel's circumference. These printers are generally limited to numeric data applications and other uses requiring less than lps output.

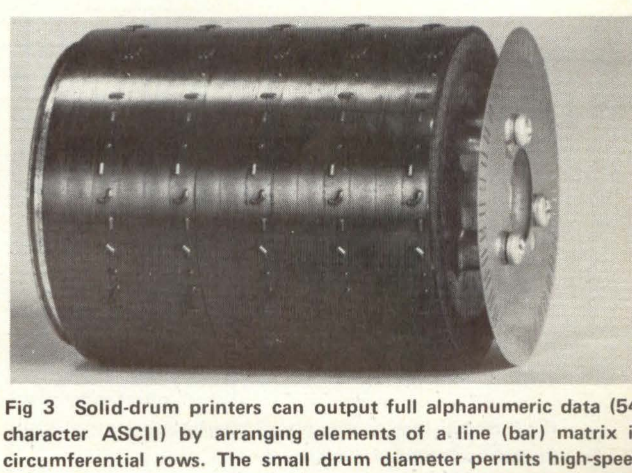


Fig 3 Solid-drum printers can output full alphanumeric data (54-character ASCII) by arranging elements of a line (bar) matrix in circumferential rows. The small drum diameter permits high-speed (1.6 lps) and fast start-up (less than 0.5 sec).

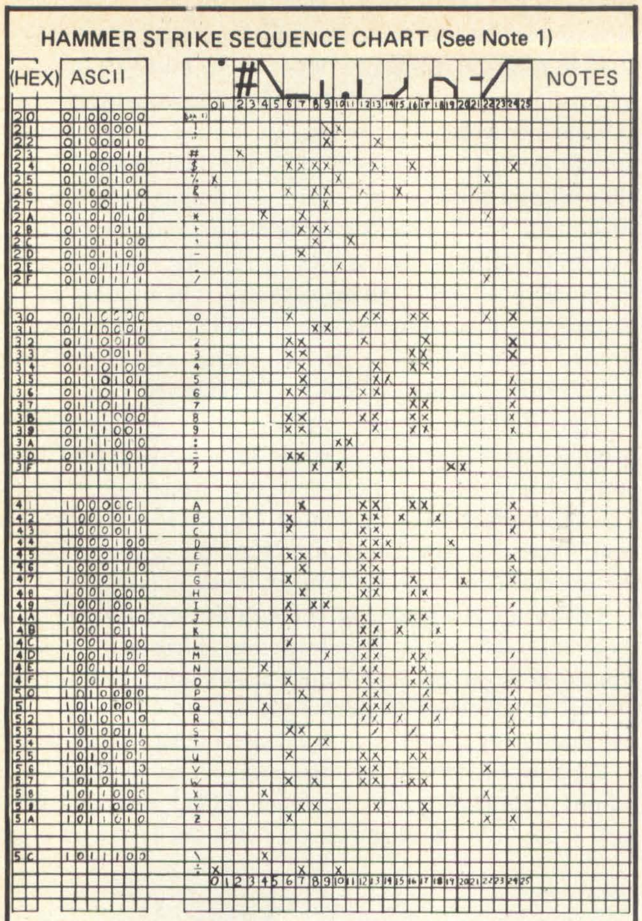


Fig 4 A 13-element bar matrix (a) and the character set obtainable with it (b).

an LCILP produces up to four simultaneous legible copies in addition to the original.

Because paper speed is relatively slow even when a printer outputs 1.6 lps, a simple solenoid drive is adequate. In most cases paper is fed by a straightforward friction drive, but when accurate positioning of data on pre-printed forms is required, a solenoid sprocket drive can be used.

Most LCILPs use a ribbon as an ink supply, and several commonly used arrangements can feed this ribbon. The most popular arrangement shifts the ribbon along with the paper advance, using the same solenoid to perform both tasks. Ribbons are generally made from nylon or carbon film; the former is strong and can be used for up to 500,000 characters before it must be changed. A carbon-film ribbon produces higher-quality symbols because each area of the ribbon is used only once, although copies have the same quality as those obtained in an LCILP equipped with a nylon ribbon).

Just as there are several types of inking ribbons, so are there several ribbon-feed methods. Most LCILPs use some type of endless loop; other methods include a two-spool arrangement, as in a typewriter, in which the ribbon direction reverses when the ribbon comes to the end of a cycle. Two-spool schemes that use endless loops are also possible. In general, however, ribbon cartridges appear to be gaining in popularity because of their simplicity of operation, ease of removal and replacement, and reliability. This last advantage is particularly important in applications where a printer is installed in a remote location or where it must be operated by the public (as in a bank's unattended night-deposit window). The cartridge also simplifies two-color printing; it is much simpler

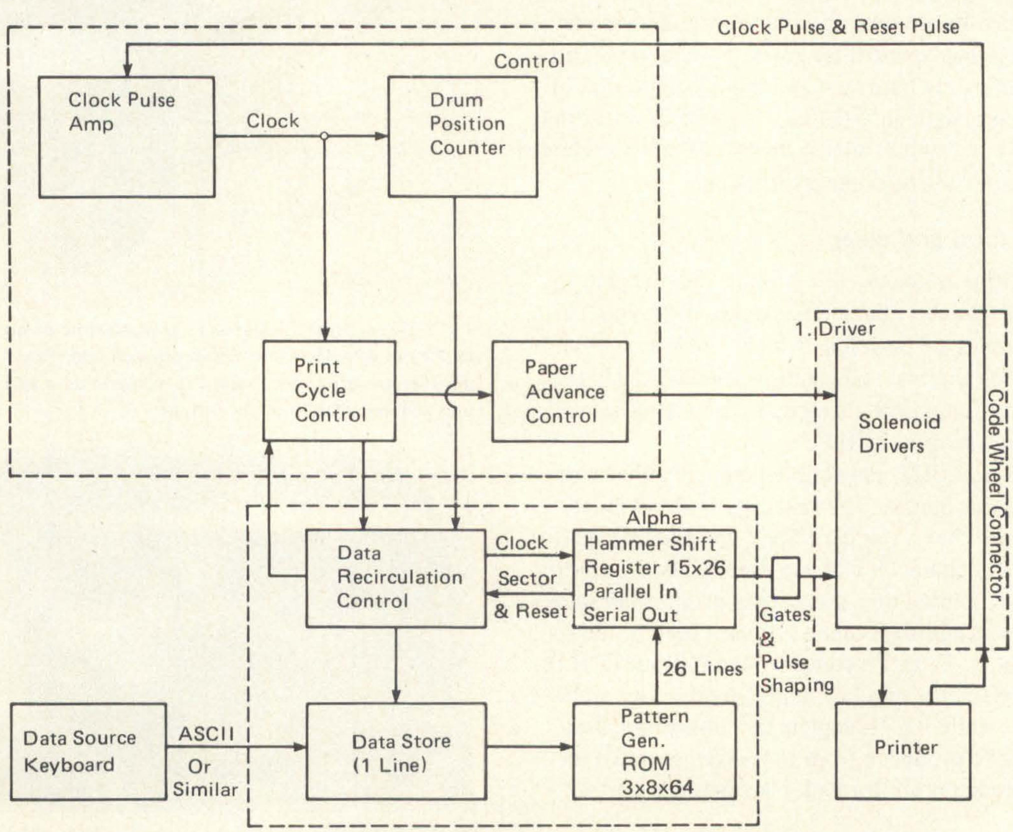
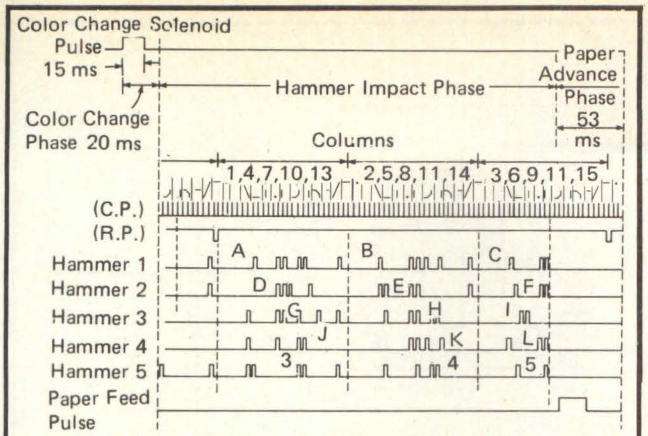


Fig 5 Simple logic is required to interface an LCILP with a data source. Patterns are generated in a ROM that can form part of the internal ROM of a microprocessor.



Hammer pulses are drawn for print sample "ABCDEFGHIJKL345" and are shown with all printing completed in one drum revolution for simplicity of representation only. Actual printing is done in two drum revolutions with odd numbered segments printed in one revolution and even numbered ones in a second revolution. (See figure 6.)

Fig 6 Electrical signals for printing the line ABCDEFGHIJK 345. While it appears as though the line is printed in a single drum revolution, it actually requires two.

to shift the ribbon when it is housed in a rigid cartridge than when it is loose. In applications that don't require two-color printing, you can get double life out of the ribbon by shifting it to a fresh, unused portion in place of the color.

Some low-cost LCILPs come without ribbon mechanisms and lock their users into printing on some kind of "action" paper. These units eliminate one of the basic advantages of an LCILP – no requirement for special paper. Almost any LCILP will print on action paper with or without the ribbon. When action paper is used, remember that the first (top) copy will typically be least legible, because it is subjected to the highest impact force of the hammers, resulting in "blossoming" of the impregnated ink.

drive it any way you please

A typical LCILP (particularly when it is shipped to an OEM) comes without any electronics; it has the required solenoids, hammers and printing drum but no control circuitry (unless specifically ordered by the customer). Typically, an LCILP is equipped with a connector for attaching external logic to solenoids, the power supply and the input of the circuit that looks at the timing pulse generated by the unit's photoelectric encoder (this is the only signal that the control electronics receives from the printer).

In a complete LCILP system (Fig 5) note that pattern generation (character forming) occurs through a ROM. This capability immediately suggests that if you use an LCILP with a microprocessor, you can use a portion of the microprocessor ROM for this purpose. (This is one reason why LCILPs come without their own electronics). A microprocessor can also simplify the logic interface right at the system's input, in the Data Store block; its memory can provide the required storage space (one line of ASCII or similar code).

The only signals generated by the printer mechanism are the series of timing pulses that tell the control electronics the drum's location at every instant. In return, the control generates a series of solenoid drive commands, paper shift signals, ribbon advance pulses and – in the more advanced units – a ribbon shift command for two-color printing. In certain LCILPs paper shift and ribbon advance are performed in a single motion by the same solenoid.

The block denoted as Data Source in Fig 5 generally constitutes some kind of alphanumeric code, usually ASCII. ASCII-encoded information is decoded by the character generator chip or a portion of a microprocessor ROM. This chip tells the proper hammer when to strike the appropriate line strokes to form the required character.

The information can input the printer either in parallel or serially, depending on the desires of the software designer. If the data comes in parallel, more wires are required but buffer storage requirements are reduced.

Sometimes the data source generates data faster than the printer can print. This operation mode requires some form of intermediate storage, so that while the printer outputs a line of data its electronics tells the data source: "Hey, I'm full; I can't take any more data in!"

In general, the data interfacing problem is really nonexistent; instructions for burning the ROM are available from printer manufacturers, and either the user or the ROM supplier can burn the ROM. The rest of the logic depicted in Fig 5 can be either supplied by the LCILP vendor or by the user, assisted by the printer vendor.

To appreciate the simplicity of an LCILP, examine a sequence of hammer strike commands required to print a line of information. Fig 6 depicts the hammer pulses, clock pulses (generated by a photoelectric circuit off the encoder wheel) and other signals that occur in a 15-column LCILP while printing, for example, the sequence ABCDEFGHIJKL345.

For simplicity, Fig 6 shows hammer pulses as if they're produced in a single drum revolution; in actuality, two revolutions are required to print this line. Note that there are only five hammers, one for every three columns.

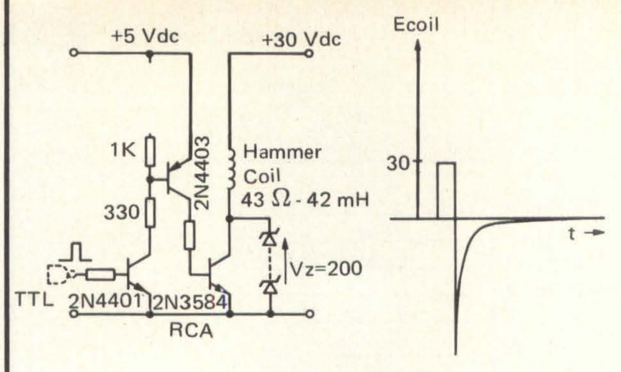


Fig 7 Solenoid driver circuit for each solenoid in a typical LCILP is often the only interfacing hardware the unit requires.

Earlier I noted that in applications involving microprocessors, the only additional interfacing hardware a user must provide is a few power transistors. More precisely, the user would have to provide one driver circuit for each solenoid. Thus a 5-hammer, 15-column printer would require seven driver circuits: five for the hammer solenoids, one for the paper and ribbon advance solenoid, and one for the color shift solenoid. Each of these driver circuits is rather simple (Fig 7). Note that the solenoid power supply can be very inexpensive because it need not be regulated. While the circuit depicted in Fig 7 is for a specific printer, the same general configuration could serve any printer that uses solenoids.

no job too small or too large

With the rapid penetration of many application areas by microprocessors, the possibility – and feasibility – of using LCILPs grows just as rapidly. Consider, for example, point-of-sale applications. Suppose a fast-food restaurant uses a 15-column printer to print out customer orders as they are placed. The equipment consists of a keyboard panel whose keys bear the names of various menu items. When a customer orders, the clerk immediately enters the ordered items and a 15-column printer within the keyboard panel prints out the order. Simultaneously, another printer in the kitchen prints out an identical record so the order can be prepared. Prices for all menu items are stored in the microprocessor memory of the point-of-sale system.

Once the order is completed, the customer pays the required amount. The system computes the right change and the printer prints the amount of change in red. Then the printer advances the paper so that the clerk can tear off the receipt. Both the clerk and the customer obtain copies of the order, and the customer and clerk can both check whether or not everything has been delivered.

Now consider a bulk weighing system, manufactured by Howe Richardson Scale Co., Clifton, NJ. In that system, an electronic control incorporates a microprocessor, which greatly simplifies a variety of functions for an operator. In this case, the only interfacing hardware required is the solenoid driver circuits depicted in Fig 7; all required logic is "borrowed" from the microprocessor. Using an inexpensive alphanumeric LCILP greatly enhanced the capabilities of the overall weighting system, because the system can print all kinds of information using normal English phrases. In previous systems, a variety of numerical codes had to be used and interpreted by the operators.

Another application for an LCILP is one that involves printing out hard copy for a microprocessor and a hand-held scientific programmable calculator (HP-65). In this application the printer outputs program listings as well as edited programs; the LCILP allowed designers to configure a true "microcomputer" system, whereas using a large-scale line printer would have priced the system too high.

In an automated banking equipment application, a printer operates with a 24-hour teller. A customer inserts an ID card into a slot and simultaneously indicates the desired transaction. Upon completion of the transaction, the printer outputs a complete record of the transaction and gives the customer a copy. The advantage of a full alphanumeric device in this application is obvious: Rather than use a variety of numerical codes (with explanations on the back of the receipt), all the required information is now printed right on the face of the receipt, thereby reducing errors and possible misinterpretations.

Numeric column printers have often been used for data logging. In process control systems, for instance, such data can include temperature, pressure, current, voltage and flow rates. The use of an alphanumeric printer – in the same price range as the purely numeric one – provides designers in this field with increased flexibility in data recording.

DIGITAL SEQUENCERS

by Angelo Yong

A Sequencer of State Machine can be defined as the device that controls a structure with the purpose of implementing a process. To illustrate this point, let's study the process of mixing two components and taking the mixture to a predetermined temperature. The structure, shown in Figure 1a, is composed of : a tank, two inlets controlled by valves V_1 and V_2, one outlet controlled by V_3, two level detectors N_1 and N_2, a temperature sensor T, a heater and a mixer to homogenize the solution. The components go into the tank through V_1 and V_2. The amount of each component is controlled by sensing levels N_1 and N_2. The mixture is heated up until it reaches the value T_d and leaves the tank through V_3. Valve V_3 is opened for a fixed time to empty the tank; discharge could be accomplished with another level detector as well. We desire to repeat this process n-times, and so use a counter module-n.

In Figure 1b we can observe that in addition to state R, the realization of this process requires a sequencer with six states: A, B, C, D, E and F. During each state a different operation is executed, except in state E where no command is emitted; but it is required because if the two minutes have not elapsed yet and the arrow coming out of the decision block is directed to state D, then the timer would be reset continuously forming, in this way, an infinite loop.

This simple example allows us to appreciate the usefulness of a state machine. Once the structure has been decided, the sequencer is the "intelligent" part that executes step by step and in a rational way the process that can be described, as in this case, by a flow diagram.

The base for the implementation of digital sequencers are the flip-flops (FF's); outputs can be either "O" or "1". The states of a sequencer are directly related to the outputs of FF's which become the binary state variables of the state machine. Eight states can be represented by three FF's, or eight FF's if each one is used to represent one of the eight states.

The transition from one state to another is determined by the present state and the values in the input lines to the machine. The simplest case is that of a counter that goes from one state to the next in response to an input pulse only (See Fig 2). In general, a state machine has several input lines that allow different paths in the flow through the distinct states that the machine can take. In Fig 3a, for example, from state q_A the next state would be q_E if X_1 were equal to "O" or q_A otherwise.

Note that in Figure 1c, there are several inputs to the sequencer. According to their origin, they can be classified as:

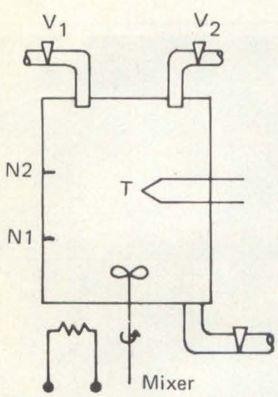


Fig 1a Tank schematic with inputs and outputs of a typical chemical process.

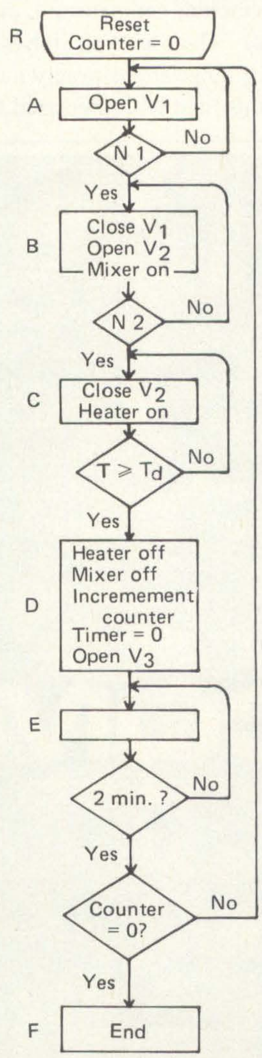


Fig 1b Flow diagram of chemical process with the procedure to obtain a solution from a mixing and heating tank.

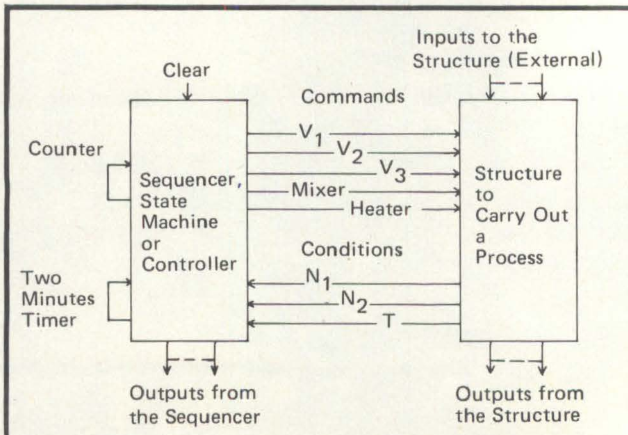


Fig 1c Inputs and outputs of the sequencer that relates to the structure.

You can use MSI shift registers to implement sequential circuits. The time for designing, mounting and debugging the circuit is small compared to other techniques – and the cost is about the same as circuits using one D-type bistable per state.

• Inputs coming from the structure. They reflect some condition of the structure and they are used by the sequencer to take pertinent action. For instance, in the case of Fig 1a the sequencer stays in state C until the temperature has reached a value T_d. Once T is equal or greater than T_d the state machine goes to state D and emits the corresponding commands.

• Inputs generated by the sequencer itself. As can be appreciated from Fig 1c, the timer and the counter have been considered as part of the sequencer.

• External inputs. They are generally designed for humans to act upon the sequencer behavior. The input "clear" falls into this category.

There exist several schemes to implement a digital sequencer. According to the actual circuit realization, the techniques can be classified as:

○ Using flip-flops (FF's). The design of state machines with FF's is a subject covered by almost all textbooks about Digital Systems (See reference 1). A nice treatment to obtain the excitation equations for the FF's can be found in reference 2.

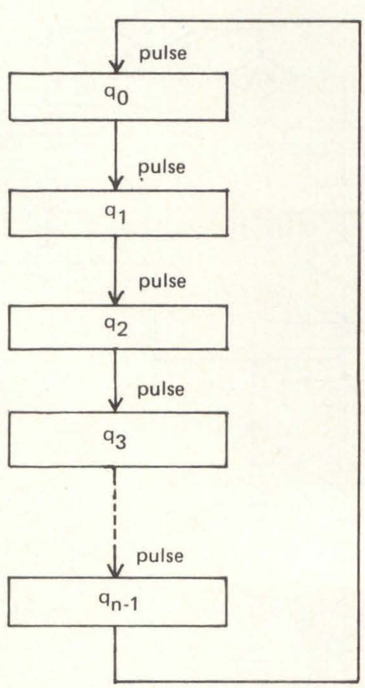


Fig 2 Flow diagram showing the states of a counter module-n.

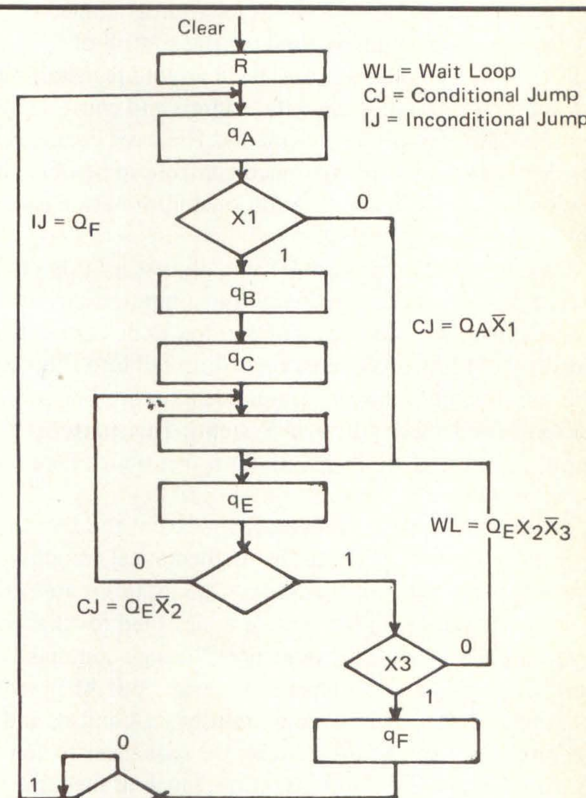


Fig 3a Flow diagram to carry out some process.

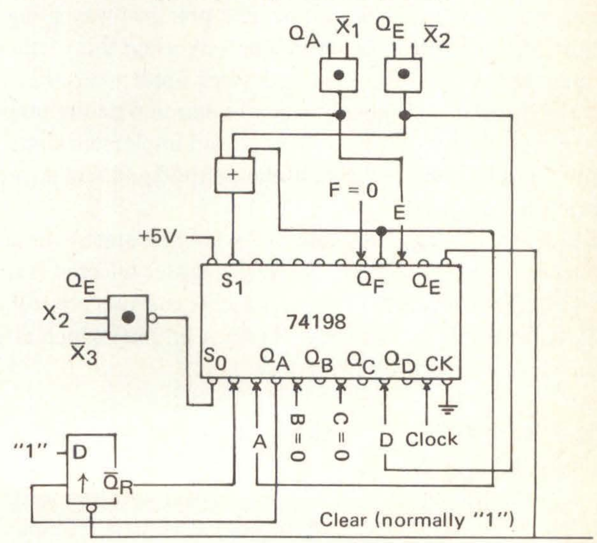


Fig 3b Sample flow diagram and state machine representing typical example of implementing – in a simple and practical way using MSI shift registers – digital sequencers for processes of relative complexity. See the sample problem in the text for equations for the above sequencer.

○ Using resetteable counters. This method appears in reference 3.

○ Using shift registers. This is the choice for processes of moderate complexity. Flip flops become cumbersome when the number of inputs and state variables are more than six and the same happens with counters when the number of states is large. In reference 1, chapter 15, D-type FF's are serially connected with additional gates to control the inputs to the FF's. This article shows how to do that with MSI shift registers.

○ Using a microprogrammed scheme – a read only memory or a programmable logic array. A microprogrammed sequencer is now commonly used for the control of the interal structure of a computer organized around registers, memories, functional units, and data, address and control lines that interconnect all these elements. The basic concepts for the design of a microprogrammed control can be obtained from references 4, 5 and 6. Additional information can be obtained from reference 9.

○ Programming a computer. When a process is fairly complex and/or it includes mathematical computations, then a micro, mini, midi or maxi computer has to be considered. Notice that Control Systems algorithms fall into this case. Microprocessors and microcomputers have become powerful tools for designing Logical Systems. This matter is beyond the scope of this paper and it is mentioned here only for completeness.

In any of the methods listed here, except the last, the sequencer does not perform the mathematical computations that a process may require. Computations are done by functional parts of the structure, designed for that purpose, interacting with the sequencer through commands and possibly status lines. Commands such as: "put #1 in register A", "put #2 in register B" and "multiply rA and rB and put the result back in rA" are used by the sequencer to control the functional units of the structure; much in the same way as the command "open valve V_1".

Digital sequencers, for processes of relative complexity, can be implemented in a simple and practical way using MSI shift registers. Advantages obtained by using this method are: minimum design time; easy and quick implementation with readily available components; and minimum debug time due to the characteristics of the design and implementation. A couple of examples will show the method and will also confirm points one and two.

Examples. For our first example, we'll implement the sequencer shown in Fig 3a. The shift register selected is the 74198 (Fig 3b) that has parallel access and two control lines S_1=L/S (load/shift) and S_0=CI (clock inhibit) which affect the register in the following way:

S_1	S_0	CK	Operation
1	1	↑	Load the register with the information present at its parallel inputs.
0	1	↑	Shift right.
0	0	x	Inhibit the clock input and hold the information.
1	0	↑	Not used in this application.

The basic idea of this technique is that each bistable of the register corresponds to one state and only one of them, at any time, has output "1" indicating what the present state is. The next state can be either the adjacent bistable to the right (this can be accomplished by shifting the "1" one position to the right) or any other bistable subject to the logical values present in the input lines X_i.

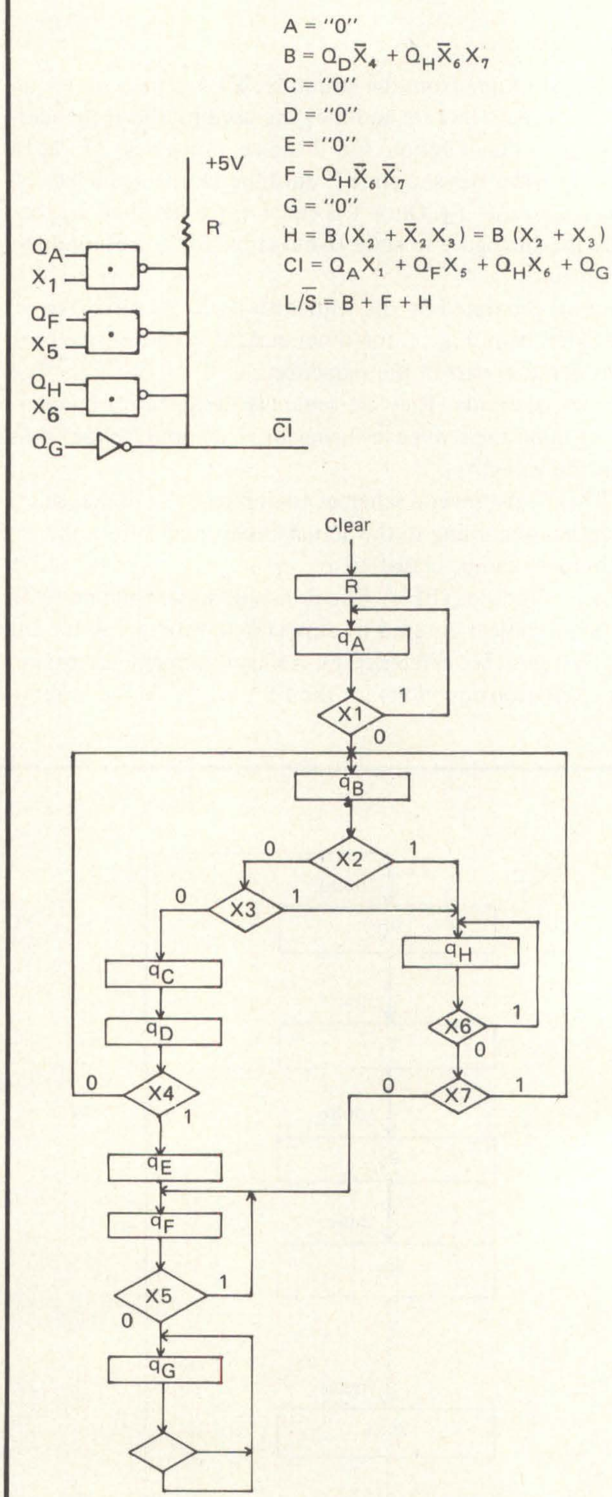


Fig 4 The procedure followed to get the equations for this digital sequencer is the same as in Example 1.

There are three situations for jumping around states in this problem, they are:

Wait Loop. That is, to remain in the same state until the condition that forces it disappears. For example, with $Q_E X_2 X_3$ applied to S_0 in Figure 3b, the clock input will be inhibited if the condition $X_2 X_3$ equals "1" and the present state is q_E.

Conditional Jump. Depending on the input lines X_i a branch to another state is wanted. This is done by applying a "1" to the input of the selected bistable (zeros to all others) and forcing a load by means of S_1. In Fig 3b, $Q_A X_1$ is connected to input E and also to S_1. In this way, when $Q_A X_1$ equals "1", Q_E will be "1" on the raising edge of the clock. The same criteria follows for the jump from state q_E to q_D.

Inconditional Jump. Disregarding the input lines X_i, the next bistable in the register; consequently, a load has to be forced. In this example, to jump from state q_F to q_A, the output Q_F is connected to A and also to S_1.

The flow diagram of the problem in equation form is:

Shift register's bistable inputs are

$A = Q_F$	$D = Q_E X_2$
$B = \text{"0"}$	$E = Q_A X_1$
$C = \text{"0"}$	$F = \text{"0"}$

and shift register's control lines are

$$S_0 = CI = \text{Clock inhibit} = Q_E X_2 X_3$$

$$S_1 = L/S = \text{Load/Shift} = A + D + E$$

For initializing the sequencer, the serial input of the 74198 (pin 2) is connected to the negated output of a FF. After a clear signal, Q_A goes to "1" on the rising edge of the clock and Q_R is forced to zero (See Fig 3b).

The second example is worked out in Fig 4. The same information contained in a flow diagram such as Fig 4 can be expressed by some form of a language and viceversa. An example of this is A Hardware Programming Language (AHPL). You can find reviews of this topic in references 1, 7 and 8.

A graduate of the University of Illinois, Angelo Yong currently teaches in the Electronics and Circuits Department of Simon Bolivar University in Sarteneja-Caracas, Venezuela.

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design dossier

Minifloppy disk drive more than triples its capacity by using 77 tracks

Storing information on 77 tracks just as an IBM compatible 8" floppy disk drive does, the 1043-Mod II system records 315 kbytes of formatted data on one side of a 5¼" diskette, according to Stuart N. Mabon, Micropolis Corp. president. Equivalent to about one-half of the information formatted on one side of an 8" diskette, but more than three to four times the amount formatted on a side of a 5¼" diskette, this quantity of data is recorded on 77 tracks per side instead of 35 or 40 tracks that most 5¼" disk drives use.

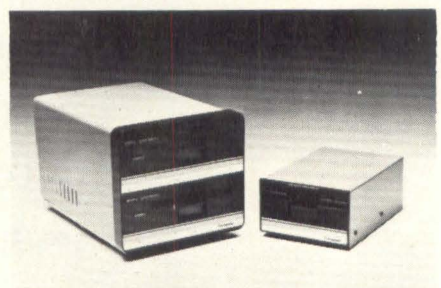
This member of the MetaFloppy family can record its high volume of data on a standard 5¼" diskette that contains 16 hard sectors of 256 kbytes capacity each, because an accurate lead screw positions the read/write head, explained Mabon. The $1095 price for the model includes a power supply, controller, interface cable and software written in BASIC.

A second family member, 1043-Mod I formats and records 143 kbytes on a 35-track diskette. Comparable units available in the industry perform single-density recording of 70 to under 100 kbytes. The quantity-one price of $945 for the second member also includes a power supply, controller, interface cable and BASIC software.

Two dual drives complete the family. The 1053-Mod I stores 286 kbytes and sells for $1545; the 1053-Mod II stores 630 kbytes and costs $1795. Both models include the same auxiliary components and software as the two previously described models.

An optional controller interface, consisting of cables and a built-in autoloading ROM, enable an operator to move data from a "cold start" to eliminate manually keying or taping bootstrap loaders. Since the interface is S-100 bus and 8080 microprocessor compatible, users may plug it directly into the S-100 bus of a MITS 8800, IMSAI 8080, COMPAL 80 or Polymorphic 88 microcomputer, Mabon declared.

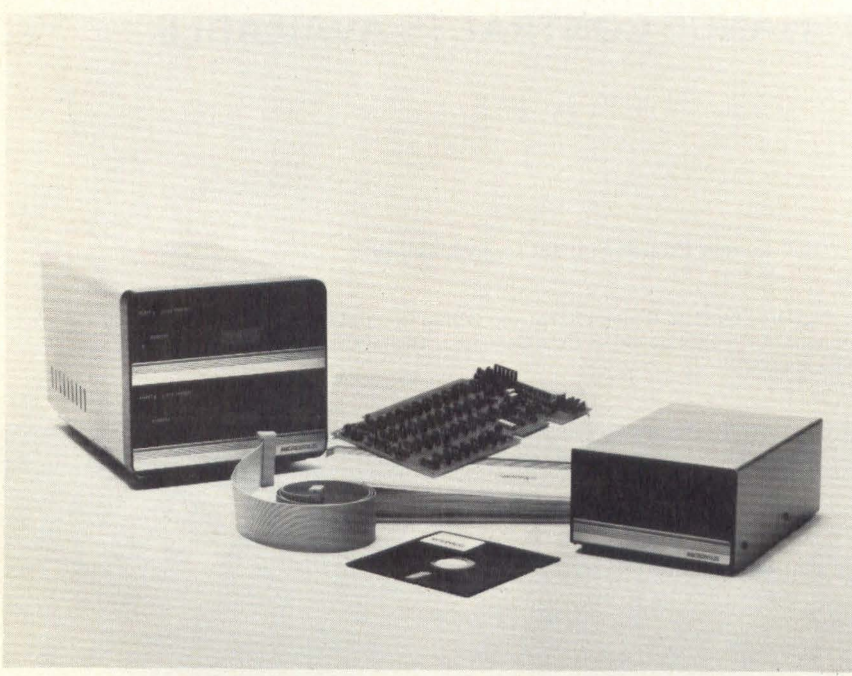
Each floppy disk drive provides a 30-ms track-to-track access time and a 10-ms settling time. They transfer data at 250 kbits/s.



MICROPOLIS MICRO-FLOPPIES – Pictured here are dual (left) and single MetaFloppy systems; all four models are plug-compatible with most popular microcomputers. They also offer a complete BASIC software package.

A phase-locked loop data separator reduces the error rate to one in 1×10^9 bits – an order of magnitude greater than the rate that one-shot separators provide, claimed Mabon. An automatic de-selectron capability, which relieves head pressure on the recording surface when the head has stopped reading or writing for about 1 ms, extends disk operating life beyond 1×10^6 passes per track. The hardware times this operation, not a software command. And a file protect indicator light prevents accidental data loss.

The smaller storage capacity provided by most 5¼" floppy disk drives has never been adequate for many applications, claimed Mabon. The industry needs more high-speed random access storage for bigger data files and to help host CPUs use larger programs than the resident memories. Micropolis Corp., 9017 Reseda Blvd., Northridge, CA 91324. (231) 349-2328.



Family of integrated floppy disk systems use 5¼-inch disks and offer capacities ranging from 143 to 630 kilobytes at the price of conventional 5¼-inch disks. All four models of the MetaFloppy family are plug-compatible with most popular microcomputers.

Liquid "O" Ring Seals Keep Disc Drives Operational

All computer disc storage devices face problems of critical magnitude. Contaminants in the form of a particulate may cause the read/write head, which rides on a self-generated air bearing less than 100 millionths above the disc surface, to "crash" and remove information storage media from the disc. The results are a loss of stored information and damage of the read/write head and the disc surface. The smallest of smoke particles, fingerprints, or oil films on the disc surface may assure this failure mode.

When computers are asked to perform in processing plants, or out in the field in portable systems, the hostile environments encountered spell trouble. But, even in the relatively clean, airconditioned computer rooms, the memory discs may not be safe. Besides the obvious problem of particulates such as dust and hair, contamination may come from within. In systems with fixed heads with nonremovable discs, the heads must not contact the disc surface. They will not "fly" over a disc which is contaminated by vaporized and deposited lubricant migrating from the drive ball bearings or from wear particles from elastomeric seals.

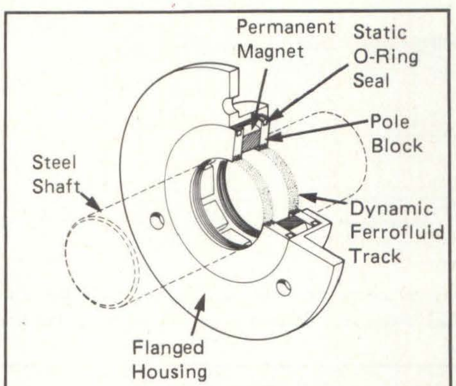


Fig 1 Aluminum casing houses two magnetic field focusing structures separated by a ring magnet. The 0.006 -- 0.007 inch diametral gap between the drive spindle and the focus structure is filled with ferromagnetic fluid. In operation, at speeds up to 6000 rpm, liquid "O" ring Ex-seal keeps helium atmosphere free of contaminants.

Digital Development Corporation, San Diego, California, has solved the "contamination from within" problems by establishing a positive pressure helium atmosphere inside their disc packages. A slight positive pressure is maintained in the disc/head chamber,

and particulate is excluded by employing Ferrometic® seals, manufactured by Ferrofluidics Corporation, Burlington, Massachusetts.

Mr. Carl Costantino, engineering supervisor for Digital Development Corporation, reports that previous attempts to keep contamination in bearing lubricant away from the disc using conventional seals were less than successful. "With both sealed or shielded bearings, outgassing of the lubricant deposited tenacious perticulate on the disc," said Mr. Constantino. "Lip seals were tried, but seal wear created dust that eventually migrated to the disc. Lip seal wear also shortened life expectancy of the unit."

Digital Development Corporation designs and manufactures a line of ruggedized fixed head (one head per track) computer memory discs. The head design contains all read/write logic and electronics in one shock-protected and thermally-protected package. The recording media is nonremovable.

In operation, the head – 60 microns away from the disc – rides on a gas bearing a helium environment. The low molecular weight of helium gas and the low drag Ferrometic® seal provide an added energy saving benefit, particularly important to extend the operational range of portable units. Power requirements are substantially less.

The disc chamber is purged and sealed and maintained at a slight positive pressure in one of two ways. The packages may include a sustaining helium supply that automatically makes up for any gas loss. Or, the discs are recharged on a once every six months program.

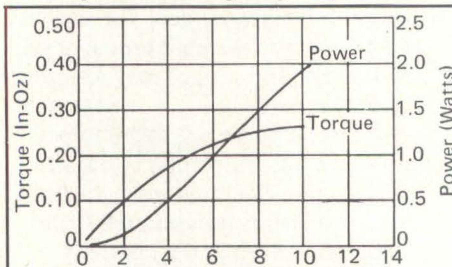
how clean is clean?

"Before and after" tests on the disc drives are impressive. Before Ferrometic® seals were installed, tests revealed a 100,000 ppm particle count of particulate larger than ½ micron. After the new seals were installed, particle count dramatically dropped to less than 100 ppm, considered to be an instrument noise level background.

liquid "o" rings in action

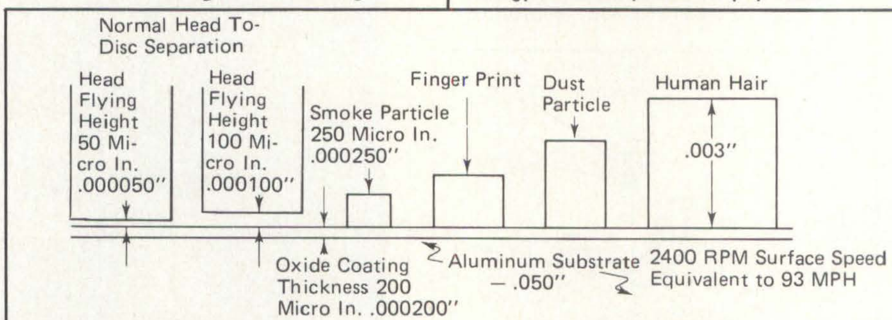
In this vertical spindle disc drive, the Ferrometic® seal fits close to the shaft – there's only a 0.006 - 0.007 inch diametral gap. The low strength magnetic field, which is isolated from the disc memory, has no detrimental effect on recorded strength or longevity.

The Ferrometic® exclusion rotary seal is hermetic, noncontacting, and stictionless. The basic seal consists of four parts: one ring magnet polarized axially, two magnetically permeable pole pieces of 400 Series SS that sandwich the magnet, and the ferrofluid (magnetic oil) sealant that forms the "liquid O-ring" dynamic seal.



Drag Torque & Power Consumption
1/2" Shaft Diameter 004" Radial Gap

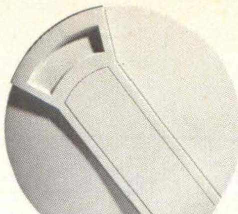
Fig 2 Combination of EX-seals and Helium atmosphere help reduce drag to conserve on energy needs for portable equipment.



Typical contaminants, that can reek havoc on computer memory diskdrives, may cause head-to-disk contact with resulting data loss. Note size of smoke particle and human hair in comparison to gap between head and disk.

When the seal is assembled, the magnet and pole pieces remain stationary with a mechanical clearance between the pole pieces and rotable shaft. The ferrofluid sealant completely fills the annulus between the shaft and the stationary pole pieces. Since the only contact with the rotating shaft is the ferrofluid, there is no wear. The liquid retains its properties even after standing for indefinite periods of time, thus preventing a "breakaway leak" on start-up, a problem common to elastomeric seals.

Many different families of liquids can be "ferrofluidized", allowing a wide selection of chemical and physi-



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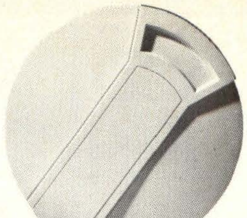

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All in the minicomputer family

price competitor to micros, mid- and high-performance models

Even though the lowest range model of a new 3-member family or minicomputers costs only $645 in single-unit lots, it delivers 16-bit performance because it incorporates two custom NMOS chips to reduce the component count, according to David H. Methvin, Computer Automation president. The NAKED MINI 4/10 unit mounts on a 7½" x 15" card and contains a 4K RAM plus an optional on-board battery backup, and 4 I/O channels.

The mid-range performance minicomputer in the family, the 4/30, offers better task execution than models in a predecessor series, Methvin continued. The top-performing member, the 4/90, runs at twice the speed of the 4/10. Equipped with a 64K, 550-ns RAM, chassis, operator console and power supply, it sells for $9950.

The family uses a common bus architecture to provide configuration flexibility and member compatibility. More registers, a more powerful instruction set and faster execution times improve family-wide performance, claimed Methvin. For example, all models use stack processing and multiply/divide instructions.

Often combining 3 or 4 instructions of predecessor minicomputers into one, the 4/10 uses a basic repertoire of 89 instructions. The 4/30 employs the same basic set plus 17 additional instructions for a total of 106; the 4/90 uses the basic 89 plus 30, for a total of 119 instructions. Methvin said that his company also offers optional expanded instruction sets.

Customers may use core add-on or semiconductor memories. Core modules come in 1, 4, 8 and 16K word sizes. Semiconductor memories with optional battery back-ups include combinations of only RAMs or RAM, ROM, PROM and EPROM devices in 256 to 32K words modules.

As in the predecessor family, the NAKED MINI models use a distributed I/O system consisting of firmware-controlled I/O processors with package attached to the connecting cables. A half-card I/O distributor can control up to 8 programmed I/O processors or 4 direct memory access devices. Multiple processors in a single system can control up to 8 programmed I/O processors or 4 direct memory access devices. Multiple processors in a single system can control large numbers of devices. The company supplies programmed devices to interface with most standard peripherals. A customer may also select user-programmable models for nonstandard equipment.

Because its two custom NMOS chips reduce component count, a $645 minicomputer delivers 16-bit performance.

The 4/10 is applicable to word processing systems, intelligent terminals, simple numerical control machines, medical, industrial and environmental control and point-of-sale equipment, Methvin continued. The 4/30 is aimed at the company's traditional market of automated banking, medical systems, environmental and process control, data acquisition and test equipment. The 4/90 can handle such high-performance multitask applications as industrial control and data communication systems. Computer Automation, Inc., 18651 Von Karman, Irvine, CA 92713. (714) 833-8830.

NCC

What you see on this month's cover is a pastel drawing by Jack Meditz of Jay Porter's arrangement of a new line of intelligent terminals introduced by Tandberg Data, Inc. of San Diego, CA. Peter A. Gilbody, Tandberg's Vice President-Marketing, explained that the unit is designed to serve as a teletype replacement, stand-alone processing system or intelligent terminal. Its microprocessor design facilitates change from one mode of operation to another by loading a program from cartridge or diskette. It can be equipped with up to 4 Tandberg digital cartridge recorders or up to 4 IBM-compatible diskette units that may be integrated in the unit itself, providing a maximum operator convenience and minimum space requirements for small systems.

Tandberg will also supply software to aid users in developing application programs. The software includes assembler, de-bug, editor, basic interpreter and TOS 21 operating system. Designated the TDV 2114, its minimum configuration consists of display hardware with 12-inch diagonal CRT faceplate and a microprocessor with 2k bytes of RAM and sockets for 8k bytes of ROM/Erasable PROM (expandable to 64k bytes of total memory). It also includes DMA controlled circuits, interrupt control and current loop interface for printers.

The anti-reflection screen displays 25 lines of 80 characters each, a total of 2000 characters, against either a dark background or in inverse mode. The set has upper and lower case for ease of text processing and more human-oriented usage. Tandberg Data head-quarters are at 4060 Morena Blvd., San Diego, CA **Circle 271**

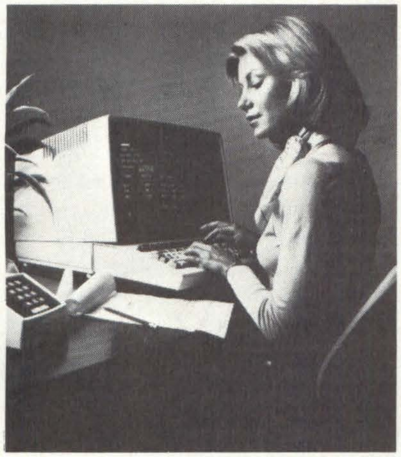
PRODUCT PREVIEW

NCC at Dallas, June 13-16 will probably have more new of everything on display than any other computer conference in the history of the computer industry as we know it. Low cost, powerful and efficient solid state devices have permitted design engineers to come up with more efficient, powerful and lower cost logic and control circuits that in turn have permitted the development of more efficient computing systems and associated peripherals, particularly for mini and micro computer applications. One of the most significant areas of growth for minicomputers and their peripherals will not necessarily be in extending current types of applications but in their application to the solution of problems in areas hitherto considered too expensive. Perhaps the best example of this fact is the great attention that engineering meeting and conferences – including NCC – now pay to the personal computing and small business application oriented people and markets.

The following display of products to be shown at NCC represents two types: products shown for the first time and products previously introduced but still viable and competitive. Space doesn't permit us to show everything. Our editors have contacted all known exhibitors; what we show here is what they have asked us to call to your attention. The solution to one of your problems may lie among the exhibits on the following pages; come in and browse awhile.

SYSTEM 7000 SUITS DISTRIBUTED PROCESSING

Inforex's System 7000 is a microcomputer-based family of standalone and clustered distributed processing systems, employing an interactive Cobol compiler enhanced for data entry. It



allows users with distributed operating facilities to perform data entry, data processing, file management and data communications functions, concurrently, at any local or remote site.

A 16-bit microcomputer provides intelligence for Model 7115 standalone and Model 7110 master control terminals. It features virtual memory, paging and overlapped I/O structures for high-speed multi-tasking operations.

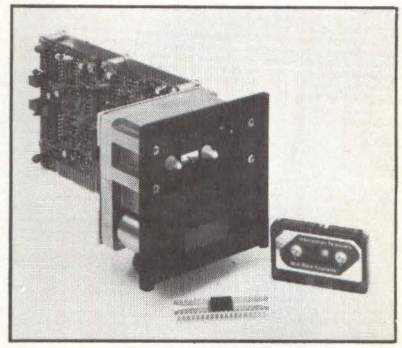
Master control terminals can support up to seven local or remote terminals. Master terminals include 64K bytes of semiconductor memory and can support four mass storage units and a variety of output printers. Multiple printers can be attached to a system 7000 cluster configuration. Inforex, Inc., 21 North Ave., Burlington, MA 01803. **Circle 252**

CART EQUIPMENT HAILS FROM ENGLAND

A firm whose equipment relates to the 3M type DC 300A data cartridge is Sintrom. An example is its cartridge dirve, which is complete with data electronics, and is said to be exceptionally simple and rugged. Other items include the Perifile 6000C minicomputer peripheral and the Perfile 6041 buffered tape emulator. Sintrom, 14 Akwright Rd., Reading, Berks RG2 OLS, England. **Circle 264**

MINI-RAYCORDER FOR MICRO APPLICATIONS

Raymond Engineering's Mini-Raycorder is designed to use the proposed ANSI standard Mini-Data cartridge. Model 6409 is specifically engineered for use with microprocessors – and other applications where size, weight, power consumption and cost are ma-



jor considerations. Its small size, less than 17 cubic inches, makes the Mini-Raycorder suitable for portable terminals, desktop calculators and portable test equipment. Minimal power requirements, less than 1.5 watts at 5 volts, make it suitable for battery operation. Raymond Engineering Inc., Middletown, CT 06457, (203) 632-1000 **Circle 246**

SECTION

PROM PROGRAMMER CAN GROW TOO

A portable Prom programmer, the model 7 from Data I/O Corp., is a universal Prom duplicator, capable of programming all commerically available Proms. By addition of options, the unit is capable of serial or parallel data communications in interchangeable data formats, remote control by another unit, and emulation of over 200 Proms. A front panel converts model 7 into the model 9 programmer configuration which provides a hexidecimal keyboard, hex address and data displays, insert/delete data editing, error message readout, and the ability to simultaneously access data from Ram, Prom and Rom emulator. Data I/O, P.O. Box 308, 1297 N.W. Mall, Issaquah, WA 98027 **Circle 260**

PRIME COMPUTER HAS BUSINESS SYSTEMS

A series of business-oriented data processing systems that provide large mainframe functionality at starting prices in the $100,000 to

$250,000 range come from Prime Computer, Inc., The new systems are a completely integrated mix of Prime's hardware, including the new top-of-the-line Prime 500 central processors and business software. The latter includes Prime's advanced Database Management System (DBMS), Multiple Index Access System (MIDAS), Forms Management System (FORMS), ANSI '74 COBOL, and IBM compatible RPG II. Prime Computer Company, Inc., 145 Pennsylvania Ave., Framingham, MA 01701. **Circle 257**

COMPACT TERMINAL

Microprocessor based terminal offers upper and lower case, programmable function keys, full editing package, protected format, blink fields, security field, and polling option. Packaging for the Micro-TEC Model 2455 is extremely compact. Unit interfaces with a floppy disk memory system, the Disco-TEC. TEC, Inc., 2727 N. Fairview Ave., Tucson, AZ 85705. **Circle 221**

NCC

ELECTROSTATIC PLOTTER CHALLENGES PEN PLOTTERS

Intelligent vector processor drives a 36-inch wide electrostatic plotter at speeds the manufacturer claims is much faster than comparable pen devises. Versatec reports its 36-inch unit creates 34" by 44" E-size draw-

ings in less than 30 seconds. An 11-inch model can plot directly from a display terminal and can also perform computer-directed work. Unit produces scientific graphs, business PERT charts, maps, production drawings, engineering simulations, and circuit designs. Shadings, tone patterns, and varied line widths can be combined with printing of captions, legends, and other alphanumeric data. Versatec, 2805 Bowers Ave., Santa Clara, CA 95051. (408) 988-2800. **Circle 209**

PRINTRONIX TO SHOW 300-LPM MATRIX PRINTER

The Printronix 300 is a raster matrix line printer capable of producing 132 character lines at a rate of 300 lines/minute. Print quality is achieved by the unit's ability to form characters one dot at a time, with sufficient and uniform hammer energy to produce clear, crisp dots on the first to last copy of 6 part forms. The unit's shuttle hammer assembly overlaps dots both horizontally and vertically to produce near solid lines in which the construction is hardly discernable. Characters are formed in a 9 x 7 matrix. Printronix, Inc., 1742 Derian Ave., Irvine, CA 92714, (714) 549-8272. **Circle 245**

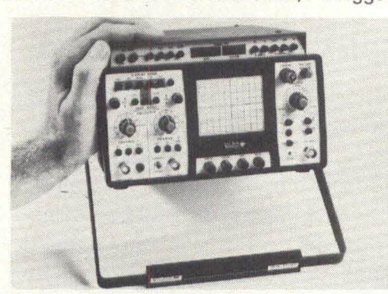
17 INCH MONITOR OFFERS 800-LINE RESOLUTION

A 17 inch monochrome video monitor by Setchell Carlson is suitable for VTR display. It features 100% solid state circuitry, 800-line horizontal resolution, front panel operating controls, regulated power supply, fast AFC action. All major components are incorporated in plug-in modules. The monitor also has a bleeder discharge system for CRT and back porch clamp DC restoration. Video response is better than 15 MHz linearity is 2% or better. Signal inputs are 0.5 to 2.5 volts peak-to-peak composite video with negative sync. SC Electronics, Inc., Sub. of Audotronics Corp., 530 5th Aven. N.W., New Brighton, MN 55112. (612) 633-3131. **Circle 206**

DUALTRACE OSCILLOSCOPE INCLUDES DMM, COUNTER

Vu-data's Model PS935/975 DMM-Counter-Miniscope is a dual-trace oscilloscope that includes a DMM and counter, each with its own dedicated display. The three "sub-instruments" can be employed simultaneously as complements to each other or they may be used independently.

Model PS935 Mini-scope is a 35 MHz bandwidth, triggered sweep, dual-trace oscilloscope. Vertical sensitivity is 5mV/div, risetime equals 10 nsec, and fastest sweep rate is 100 nsec/div (a X10 magnifier will increase that to 10 nsec/div). Trigger



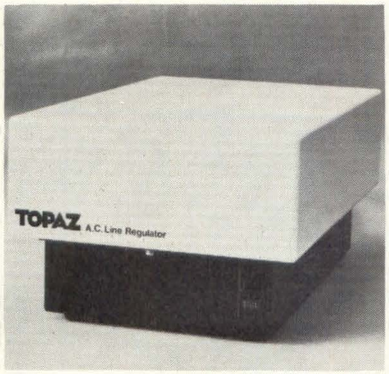
range is DC to 50 MHz. The CRT viewing area is 8 x 10 major divisions, with each division equal to ¼ inch.

Model 975 DMM-Counter includes a 3½ digit, auto-ranging digital multimeter (AC volts, DC volts and Kohms), as well as a four digit, 50 MHz frequency counter.

Model PS935 without the Model 975 DMM-Counter sells for $1,495, and the total price, is $1,875. Vu-data Corp., 7170 Convoy Ct., San Diego, CA 92111. **Circle 255**

LINE REGULATORS PROTECT AGAINST BROWNOUTS

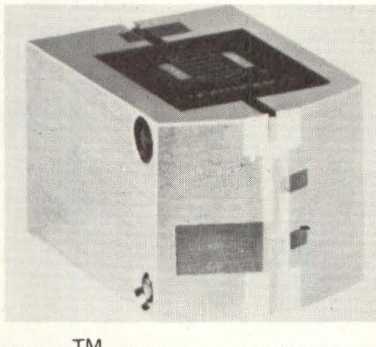
Line regulators feature dynamic responses of less than one cycle, efficiency greater than 98%, and less than 1% distortion. Topaz Electronics AC series are designed specifically to protect mini-computers and related equipment against brownouts and other severe voltage fluctuations.



Regulators are compact and lightweight; require only plug-in operation. Power ratings range from 600VA, to 1600VA, with other models available in ratings through 100kVA. Prices start at $265. Topaz Electronics, 3855 Ruffin Rd., San Diego, CA 92123. (714) 279-0111.
Circle 222

THRIFT HEADS KEEP CASH FLOWING

Magnetic heads for applications such as electronic funds transfer, teller terminals and constant cash terminal, are available from Nortronics constructed with DURA-



CORE™ a high permeability magnetic alloy. Called "thrift" heads, they provide a wear ratio at least 10 times greater than conventional Hi-Mu 80 materials, claims the manufacturer. Nortronics Co., Inc., 8101 Tenth Ave. N., Minneapolis, MN 55427. (612) 545-0401.
Circle 201

SCOTLAND YARD'S DATA ENTRY SYSTEM

The Datapad computer data entry system from Quest Automation is reported to eliminate the need for a centralized data preparation department based on manual punching equipment. It consists of a special writing pad, a small display and a minicomputer equipped with the firm's special software. Data is entered on the special pad with any pen or pencil using almost any free handwriting style. Because no special training is needed, data can be captured at source by the same staff who would otherwise be using ordinary pens and paper. Applications include telesales, order entry, sales accounts, purchase ledger input, file amendment and data collection. The system is in use at London's New Scotland Yard. Quest Automation Ltd., 26 Cobham Rd., Ferndown Industrial Estate, Stepehill Wimborne, Dorset BH21 7NP, England. **Circle 268**

NCC

DATACOM EQUIPMENT FROM BRITISH FIRM

British-based Modular Technology's Minimodem is acoustically coupled, portable and light. It operates at up to 300 baud. Another product, the Interfaker, the company describes

"an essential piece of diagnostic and patching equipment for anyone faced with modem or terminal problems." Modular Technology, P.O. Box 117, Watford WD1 4PD England.

Circle 248

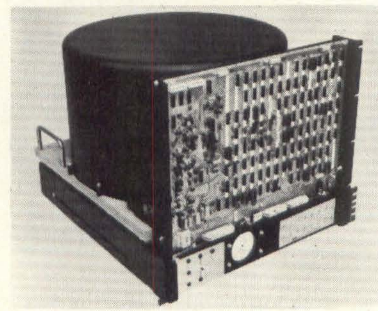
DESK-TOP TERMINAL FEATURES BOTH MEMORY AND TAPE

An automatic send/receive desk-top terminal includes both a built-in mini-cassette magnetic tape unit with 68,000 characters and an integral 8K RAM. The Miniterm 1204 by Computer Devises Inc. provides complete simultaneous transmit/re-

ceive capability; tape-to-tape memory, memory-to-tape, or either tape- or memory-to-line transmission. Unit features 1200 Baud transmission rates from tape, memory or keyboard to line; three-mode, operator selected keyboard including upper/lower case typewriter, TTY, APL, or integral 16 key numeric cluster; 35 character per second printing speed, fully buffered. It is compatible with all minicomputers and central processors via EIA standard and RS232 interface. It is ASCII or Binary code user selectable. Price is $3385. Computer Devices Inc., 25 North Ave., Burlington, MA 01803. (617) 273-1550. **Circle 218**

HEAD-PER-TRACK UNIT GUARANTEED FOR A YEAR

Digital Development Corp.'s model 7510 head-per-track memory unit stores from 9.6 to 76 million bits of data for a variety of fast access storage applications. Each unit includes



electronics for reading, writing, track selection and timing generation. The non-contact fixed head assembly can access data in an average of 8.5 milliseconds. Digital Development Corp., 8615 Balboa Ave., San Diego, CA 92123, (714) 278-9920. **Circle 256**

GRAPHICS TERMINAL DOESN'T RELY ON HOST COMPUTER

An intelligent interactive graphics terminal can pan, zoom, cursor track, generate grids, display black on white and white on black and such functions as alphanumeric display and write-thru (erase and aid), without relying on the host computer. Basic configuration of the Calcomp IGT is a processor, display screen, RS232-C interface and full ASCII keyboard which includes function and cursor controls. Full supporting software is included. The IGT offers three modes of operation: local, input from the computer, and interactive. Transitions to the three modes can be controlled by either the host computer or the terminal keyboard. Price is approximately $14,700 with first deliveries scheduled for this September. California Computer Products, Inc., 2411 W. La Palma Ave., Anaheim, CA 92801. (714) 821-2541.

Circle 211

MEMORY, PRINTERS EXPAND HARRIS 1600

Auxiliary memory and a new line of printers for the model 1600 family of remote communications processors from Harris Corp., allow users to expand the number of local and remote data entry terminals and programs that can run concurrently with batch operations. Auxiliary memory will come in 16K byte and 32K byte increments. The three new printers are designed mainly for hardcopy output of CRT terminal displays, but can also produce reports directly from a 1600 processor. Harris Corp., Data Communications Div., 11262 Indian Trail, P.O. Box 44076, Dallas, TX 75234. **Circle 258**

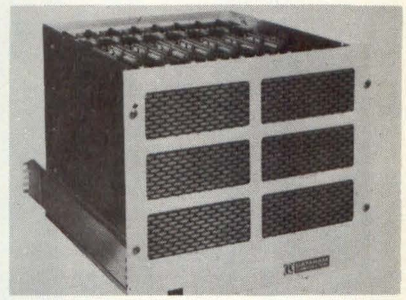
SMALL COMPUTER SYSTEM USES MINIDISKETTES

Direct access computing for the small user is centered around twin minidiskettes each of which contain up to 89,000 bytes of programs or data. The Wang PCS-II includes a 1,024-character CRT screen, a typewriter styled keyboard with separate numeric keypad and 32 special function keys for data entry and control, a high speed processor with two memories, and 8K bytes of user

memory. Price of the "deskette" computer is $6200. Wang Laboratories, Inc., 1 Industrial Ave., Lowell, MA 01851, (617) 851-4111. **Circle 217**

CORE STORAGE CONTROLLERS EMULATE PDP-11, NOVA FIXED-HEAD DISC SYSTEMS

An electronic equivalent to fixed-head disc (FHD) systems now comes with complete interfaces to emulate DEC and Data General FHD systems. Dataram supplies interfaces to make its BULK CORE storage hardware and software transparent to the host minicomputer. Rack mountable chassis can hold up to eight 128K word BULK CORE modules for a maximum capacity of one megaword (two megabytes). Chassis also contains the necessary interface, power supply, and fan assembly.



Dataram's interface is microprocessor controlled with access time ranging from 750 nanoseconds to 2.0 microseconds, depending on the system. The FHD-compatible systems have parity generate-and-check, built in off-line test capability, 0°C to 55°C operation, and operational fault indication. Dataram Corp., Princeton-Hightstown Rd., Cranbury, NJ 08512. (609) 799-0071. **Circle 202**

NCC

QANTEX'S MINIDRIVE INTERFACES TO MICROS

The model 200 Minidrive magnetic tape cartridge drive from Qantex can be directly interfaced with Motorola 6800s and Intel 8080s. It is compatible with Qantex's Model 600/650

and Formatters and can be interfaced to the PDP-11, LSI-11, Data General, Rolm, Interdata and Altair Computers.

Model 200 Minidrives are available with 800 bpi or optional 1600 bpi packing density resulting in a transfer rate of 24,000 or 48,000 bits per second. The storage capacity is from 168,000 bytes for a Minidrive with a single track head and 800 bpi packing density to 772,000 bytes of unformatted data for a Minidrive with dual track head and 1600 bpi packing density. Qantex, 200 Terminal Dr., Plainview, NY 11803.

Circle 263

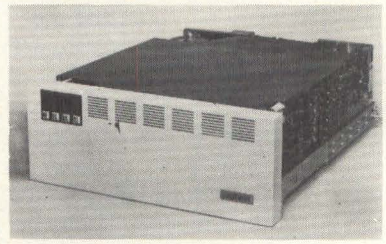
EX-800 SELLS FOR $655 AND PRINTS 160 CPS

Axiom Corp.'s EX-800 is an LSI-based 80-column line printer that operates at 160 characters per second and costs $655. The stand-alone non-impact printer includes case, power

supply, ASCII interface, character generator and paper roll holder. An RS232C serial interface, with a switch to provide plug compatability with Centronics or Tally input connectors, is available for $85. Grinnell Systems Corp., 2986 Scott Blvd., Santa Clara, CA 95050, (408) 988-2100. **Circle 247**

WINCHESTER-TYPE DISKS FROM OKIDATA

A family of Winchester-type disk drives that provide up to 74 megabytes of memory in a 7" rack hails from Okidata Corporation. Prices, in



OEM quantities, are as low as $46 per megabyte. The 3300 series comprises six models of moving head, fixed disk drives which range in capacity from 12.4 to 74.4 megabytes. Two models of fixed-head only provide capacities of 2.97 and 5.94 megabytes. Fixed heads can also be added to moving head models to a maximum of 2.2 megabytes. The fixed heads have an average access time of 10.1 msec and can be accessed while positioning the moving heads. Okidata Corp., 111 Gaither Dr., Mt. Laurel, N.J. 08054. **Circle 259**

NETWORK MONITOR TESTS AND MONITORS DATA LINES

ICC's System 180 Network Diagnostic Controller provides comprehensive, centralized, automatic monitoring and diagnostics for multipoint and point-to-point data communications networks. It can control up to 16 central lines and 254 remote devices per line in its basic configuration.

System 180 performs fault isolation in telecommunication networks of ICC modems equipped with a specialized multipoint test and control feature. In addition to network testing, System 180 performs automatic scanning, automatic fault reporting, restoration control and logging and printing. International Communications Corp., 8600 N.W. 41st St., Miami, FL 33166. **Circle 253**

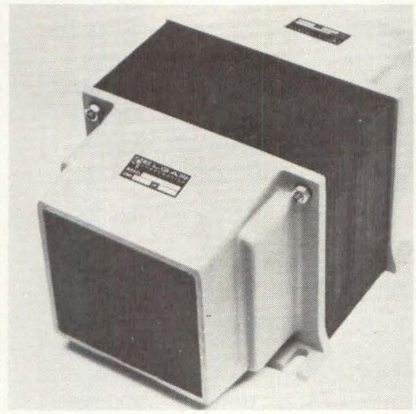
PORTABLE UNIT TESTS COMMUNICATIONS SYSTEMS

Data analyzer which fits under an airairplane seat pinpoints data communications system problems by identifying flawed characters with underlining, reverse imaging or flashing. The COMTEST microprocessor-

based unit from Universal Data Systems may be used in full or half duplex mode to monitor the entire system or can emulate either the CPU or various terminal devices. A 16-line, 512 character CRT display allows the dialog to be viewed at the RS232 interface. The unit has programmable search, trap, and display capability for any contiguous data string up to 16 characters. Universal Data Systems, 4900 Bradford Dr., Huntsville, AL 35805. (205) 837-8100. **Circle 216**

TRANSFORMERS QUIET NOISY POWER LINES

Equipment can be isolated from common mode noise and transverse mode noise caused by common mode transients greater than 125db with the high isolation transformers (HIT) offered by Elgar Corp.



Available in ratings from 1KVA they are connectable for 120VAC or 240 VAC inout or output and can be used as a combination step-down transformer and noise isolation device. All models are rated for either 50 or 60 Hz operation. Prices start at $290. Elgar Corp., 8225 Mercury Crt., San Diego, CA 92111. (714) 565-1155.

Circle 229

DATACOM TEST UNIT

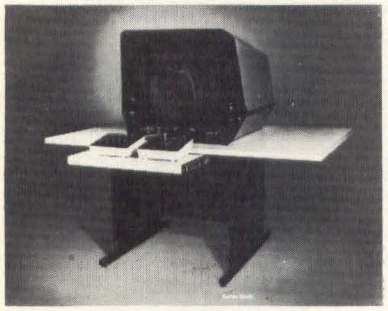
A data communications test unit, features high data rate testing. It handles all codes and line disciplines at speeds up to 64 Kbps with internal clock and up to 256 Kbps with external clock. In addition, it provides for all aspects of half and full duplex testing, including provision for display and for calculating the block check character for transmit and receive data of Bisync, SDLC and others. The Interview, a CRT monitor used for displaying data communications transmissions, provides the operator with a clear display of all data traffic, or only traffic from a selected terminal or location. Interview allows visual observation of up to 1,024 characters in either hex or octal. Atlantic Research Corporation.

Circle 270

NCC

REFRESH GRAPHIC DISPLAY MATCHES MOST MINIS

Capable of providing refresh graphics for any minicomputer with standard input/output configurations, the 3300 Series of high-speed interactive graphics displays write at speeds up to 16,667 short vectors



and 6,000 characters/second. Vector General introduces the line with two models: 3301, which displays two-dimensional graphics and alpha-numerics, and 3202, which adds image transformation and rotation capabilities to the basic 3301.

These microprogrammed units feature 2D digital transformations, variable speed vector and font generators, programmable graphic instructions, font transformations, optional refresh buffer and full subroutine stack capability. The microprocessor display I/O control unit accepts 16-bit data and control, and "front ends" the display generation hardware. Vector General Inc., 21241 Ventura Blvd., Suite 271, Woodland Hills, CA 91364, (213) 340-8731.

Circle 242

TALLY HAS NEW LINE PRINTER FAMILY

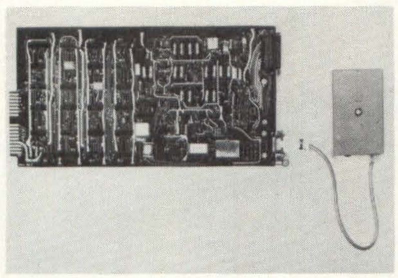
A family of matrix line printers with print speeds of 375 and 500 lines/minute from Tally Corporation features a 9 x 7 half-space matrix font for sharply defined characters, full line buffering, a 64-character set, 11-inch/second slew speed, scroll ribbon, 132 print positions at 10 characters/inch, dual adjustable tractors, 0 to 99 line forms length select and an acoustically designed low noise enclosure. The T-5000 series features the helix printing principle where

printing is produced by the controlled interaction of a constant speed rotating helix and 22 voice-coil-activated hammers. All printer functions and printed characters are electronically controlled by an integral microprocessor. Tally Corp., 8301 S. 180th St., Kent, WA 98031.

Circle 251

MODEM ALLOWS DIRECT CONNECTION TO SWITCHED TELEPHONE NETWORK

Operating at 300 bits per second in an automatic answer mode, VADIC's VA317S modem is FCC



registered and is a direct replacement for the Bell system model 113B. Recent FCC rulings permit the incorporation of the data access arrangement function as an integral part of the modem if tested under FCC rules. Model VA317S enables direct electrical connection of the modem to the telephone network without externally provided telephone company data access arrangement. Unit has analog and digital loopback as well as an 8 LED interface display and built-in data source for on-line testing. Modem is priced at $240 in 1 to 9 quantities. VADIC Corp., 505 F. Middlefield Rd., Mountain View, CA 94043. (415) 965-1620.
Circle 212

PAPER TAPE READER DESIGNED FOR NUMERICAL CONTROL

Paper tape reader/spooler operates at 1500 characters per second (stop-on-character) for numerical control equipment. Tape wear is kept to a minimum in the GMT Model 27 by the elimination of buffer arms and capstans. The spooling equipment is the sole source of tape movement. A semiconductor memory replaces the traditional tape buffer. Data is read automatically into the memory when it is less than half full and even at reading speeds of 250 characters per second the memory will not normally be emptied. GNT Automatic, Inc., 440 Totten Pond Rd., Waltham, MA 02154. (617) 890-3305. **Circle 273**

PARALLEL I/O BOARD

An 8-bit parallel I/O board provides an interface for almost all mini- and micro-computers and other parallel interfaces. The single board piggy back plugs into the MFE 250B Digital Cassette Transport, adding about 1" to its depth. The I/O connector to the interface is a 40-pin, 3M type 3432. It eliminates parallel-to-serial and serial-to-parallel conversion circuitry. The board includes: four speed control oneshots allowing programmed selection of Read/Write, Search, Low Rewind/Fast Forward (80 ips), and High Rewind/Fast Forward (120 ips); adjustable Write Oscillator for Write Clock generation; gap detection; optical EOT/BOT latch, and bi-phase-level encoder/decoder circuitry to provide ANSI/ECMA compatible recording at data rates up to 32,000 bits or 4,000 bytes per second, Single unit price is $325. MFE Corp., Keewaydin Dr , Salem, NH 03079. (603) 893-1921.
Circle 226

NCC

APPLICATIONS BROADEN FOR PERIPHERAL SWITCHES

Switches for almost every major minicomputer supplier provide the user with multiprocessor installation with the capability to quickly reconfigure computer/peripheral devices. Each computer switch produced by T-Bar Inc. is compatible with a specific computer type for both mainframe and minicomputer suppliers. Switching offers both back up for on-line systems and costs savings through more efficient use of equipment. All of these switches are suitable for remote control via manual instruction or by direct computer drive or address. T-Bar Inc., 141 Danbury Rd., Wilton, CT 06897. (203) 762-8351. **Cricle 219**

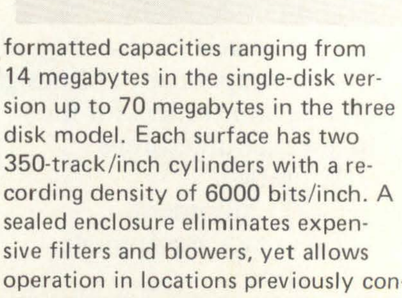
ROYTRON READER/PUNCH NOW PLUG COMPATIBLE

Serial interface compatibility via an RS232C interface has been added to Roytron's Paper Tape Reader/Punch. Model 1560-S is a combination desktop, compact, self-contained unit with integral electronics, power sup-

ply and asynchronous serial interface. It is designed to be connected between a terminal device and its associated modem or data coupler. It can also be connected to the serial port of most minicomputers and microprocessors. Sweda International, O.E.M. Products, 34 Maple Ave., Pine Brook NJ 07508, (201) 575-8100. **Circle 249**

THESE DISKS RECORD AT 6000 BITS/INCH

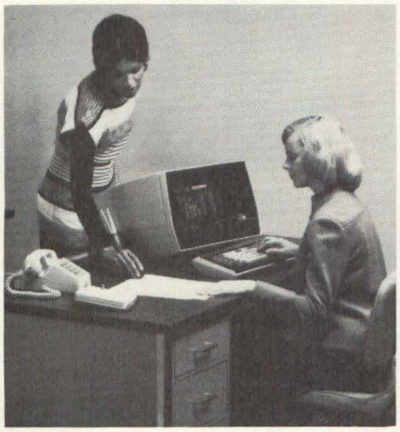
A line of fixed-cartridge, moving head disk drives – Winchester-type – from Kennedy Company stores up to 70 megabytes of data at rates of one megabyte/second. Termed the series 5300, the Kennedy drives have un-



formatted capacities ranging from 14 megabytes in the single-disk version up to 70 megabytes in the three disk model. Each surface has two 350-track/inch cylinders with a recording density of 6000 bits/inch. A sealed enclosure eliminates expensive filters and blowers, yet allows operation in locations previously considered unsuitable for disk drives. Kennedy Co., 540 W. Woodbury Rd., Altadena, CA 91001, (213)798-0953. **Circle 230**

SYSTEM GROWS FOR MODERATE VOLUME APPLICATION

User programmable system features multiple-unit configurations for a wide range of distributed tasks, from extended data validation to



full transaction processing. Mohawk Data Sciences is initially offering two versions of its Series 21, for data entry and application processing. Basic configuration consists of an op operator station with 1920 character CRT, keyboard and a processor with to four operator stations. Mohawk Data Sciences, 1599 Littleton Rd., Parsippany, NJ 07054, (201) 540-9080. **Circle 210**

TERMIDISK ACTS AS PERIPHERAL ACCESSORY

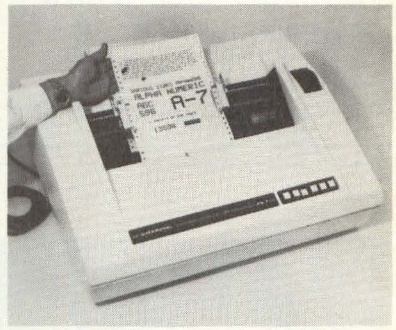
TD-1 TermiDisk is a communications oriented microcomputer system, intended as a peripheral accessory for either on site or remote data terminals. It is equipped with one to four standard IBM compatible diskette devices with a storage capacity of nearly one million bytes.

TermiDisk can be used in data collection, timesharing computer usage and business communications. Communications with terminals and modems is through two standardized serial ports (expandable to four), each capable of communication with 5, 6, 7, or 8 bit data at rates from 50 to 19,200 baud.

Delivery is 60 days ARO and systems start at $3,495, with OEM discounts. International Computer Products, Inc., 2925 Merrel Rd., Dallas, TX 75229. **Circle 266**

VARIABLE TYPE PRINTER IMPACTS HIGH AND WIDE

Medium speed dot matrix impact printer includes alphanumeric characters in multiples of one-ninth inch high as well as bar codes. An original and up to five copies are



printed on either carbon or carbonless/stock, from 4-7/8" wide to standard printout size, by Dataroyal IPS-7. Print head travels with no wasted motion in this microprocessor controlled bi-directional unit to the next actual printing location. Dataroyal Inc., 235 Main Dunstable Rd., Nashua, NH 03061. (603) 883-4157. **Circle 227**

NCC

INTERACTIVE CRT TERMINAL SUPERVISES OTHER PERIPHERALS

A logic partitioning system allows this programmable interactive CRT terminal to reserve ample computer time to supervise other peripherals in addition to its basic terminal function. Conrac Data Products Model 480/25 is microprocessor based (6800), switchable to 9600 Baud and has RS232 or current loop interfaces. It is fully buffered, stores and displays up to 25 80-character lines, is modular and fully programmable. The cursor can be both addressed and sensed remotely. A 26th line displays up to eight bright rectangles which are under program control and are generally used as status indicators. Add-on memory

is expandable to 49K bytes and character sets are on plug-in PROMS. Conrac Div., Conrac Corp., 600 N. Rimsdale Ave., Covina, CA 91722. (213) 966-3511. **Circle 207**

BI-DIRECTIONAL TAPE CARTRIDGE FITS INTO SHIRT POCKET

Data cartridge containing 140 feet of usable storage on computer grade magnetic tape measures just 2.4 x 3.2 x 0.5 inches. Scotch brand bi-directional unit has holes provided in tape for beginning of tape, load point early warning, and end of tape sensing. A manually operated sliding tab provides file protect capability. The DC100A is a smaller version of the DC300A data cartridge. Mincom Division of 3M also provides the DCD-1 Data

Cartridge drive using the new cartridge, in applications which require a compact unit. It stores in excess of 100,000 bytes, recording at full width, and can be battery operated. 3M Co., Mincom Div., 3M Center, Bldg. 224-BW, St. Paul, MN 55101. (612) 733-4518. **Circle 203**

CIRCLE 79

PICTURE SYSTEM 2 EXPANDS GRAPHICS

Evans & Sutherland Computer Corp.'s Picture System 2 can expand graphic application areas by providing faster update rates, increased line presentation (21,500 lines per 30th of a second), and a CRT display of 7000 characters per 30th of a second. Additional line textures, 64 levels of intensity and depth cueing are all features of the Picture System 2.

A high speed, microprogrammed Picture Processor allows for rapid hardware transformation, clipping and viewport mapping of two-, three- and four-dimensional (homogenous) coordinate data to provide realtime perspective display of complex objects.

A refresh controller allows data segmentation in refresh memory and independent update of selectable portions of the refresh memory, to increasing the throughput of the system.

A standard system, consisting of a picture processor, picture system memory, refresh controller, line generator, character generator, picture display, data tablet and work stations is priced at $65,000. Included in the price is the Fortran-callable Graphics Software Package. Evans & Sutherland, 580 Arapeen Dr., Salt Lake City, UT 84108. **Circle 267**

ALL KINDS OF TELEPRINTERS

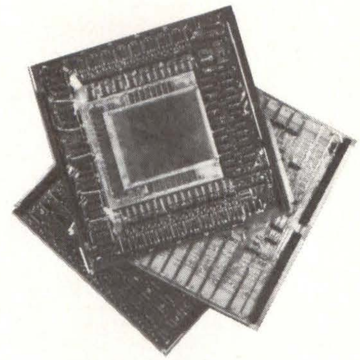
Extel will exhibit examples of its line of teleprinters. Included are: Model B305PS, an electronic ASR

impact dot matrix printer with 5 level code, up to 30 char/sec. speed, paper tape punch and reader and an electronic editable memory of up to 8000 characters. Model B208L, an electronic KSR impact dot matrix printer with 8 level code, up to 30 char/sec. speed. Model AH, Receive-only impact dot matrix printer, with 5, 6 or 8 level code, up to 30 char/sec. speed. and Model B400, Receive-only paper tape punch, featuring a quiet long-life punch mechanism, 5, 6, or 8 level code and serial or parallel bit interface. Extel Corp., 310 Anthony Trail, Northbrook, IL 60062. (312) 564-2600. **Circle 220**

PRINCETON ELECTRONICS TO DISPLAY EQUIPMENT

The Princeton 801 graphic computer terminal and PEP-400 image storage and scan converter terminals use the company's proprietary Lithocon silicon storage tube. The 801 is a stored image computer terminal that displays an unlimited amount of flicker-free information and features selective erase and large bright displays. The scan converters are used for display refresh memories and for storing and displaying images in slow scan and frame grabbing applications. Princeton Electronic Products, Inc., P.O. Box 101, North Brunswick, NJ 08902, (201) 297-4448. **Circle 244**

ms Capability



VIDEO DISPLAY TERMINAL
KERONIX MODEL K-4000

- FULL KEYBOARD (Optional 10-Key Pad Available)
- HIGH RESOLUTION, NON-REFLECTING SCREEN; 9" X 7" (12" Diagonal); SWIVEL BASE; EASY VIEWING UP TO 10 FEET; BRIGHTNESS CONTROL; REVERSE VIDEO (Black Characters on White Background, Selectable)
- 80 CHARACTERS PER LINE, 25 LINES, 2000 CHARACTER DISPLAY; STORE UP TO 51 LINES & 4080 CHARACTERS; BLINKING CHARACTERS AT 3Hz RATE
- CURSOR CONTROL (Non-Destructive)
- INTERCHANGEABLE WITH TELETYPE USES STANDARD ASCII CODE
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- VARIABLE BAUD RATE (75 to 9600 Bits Per Second); 10 OR 11 BIT CODE
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- 1023 EIA INTERFACE
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- 1038 MULTI-PROCESSOR COMMUNICATIONS ADAPTER
- 1046 DISK CONTROLLER
- 1146 FLEXIBLE DISK CONTROLLER
- 1054 EXTENDER BOARDS
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CIRCLE 80

TELEPRINTER SUSTAINS 1200 BAUD LINE RATE

A 132-column teleprinter that sustains a full 1200 baud line rate has been added to Tally's line of serial printers. Model T-1612 is available

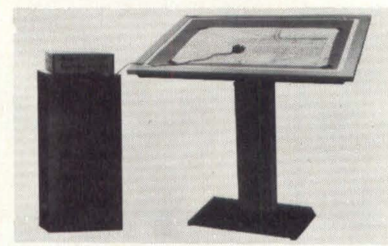
acters/second, uses an internal microprocessor that computes the shortest distance to the next print point. Standard features include switch selectable baud rates from 300 to 9600, parity checking, unattended operation, half or full duplex operation, 1K-byte character buffer and three serial interface connections. Tally Corp., 8301 S. 180th St., Kent, WA 98031. **Circle 250**

INTERACTIVE TERMINAL CAN ACCOMODATE 132 COLUMNS

By eliminating much of the data reformatting required by displays limited to 80 columns, a new interactive terminal, which can accomodate 132 columns, can provide savings in printout, processing, communication and programming time. Heart of the Datagraphix® 132A is the Charactron® CRT. It has the inherent advantage of instantly generating high quality alphanumeric characters and symbols. Character generation time remains independent of character complexity. Microprocessor controlled, the Datagraphix 132A offers a 96 upper and lower case ASCII character set, a 60 or 120 line buffer, cursor control, single line editing, tabbing, scrolling, multiple asynchronous transmission modes at 110-9600 bps in full or half duplex, and RS232C output to 132 column/serial printer. Initial price is $3950 for the Basic 8k unit. Datagraphix, Inc., P.O. Box 82449, San Diego, CA 92138. (714) 291-9960. **Circle 225**

MICRO-BASED DIGITIZER PREPROCESSES DATA

An 8080 microprocessor in Summagraphic's digitizer preprocesses all data which frees the user from programming his own computer. The digitizer can be modified to accept custom firmware. Current board



level firmware includes: relocatable origin, Binary/BCD conversion, metric output, incremental operation, scaling, rotational correction, area calculation, distance measurement and angle calculation. Summagraphics Corp., 35 Brentwood Ave., Box 781, Fairfield, CT 06430. **Circle 254**

digital design

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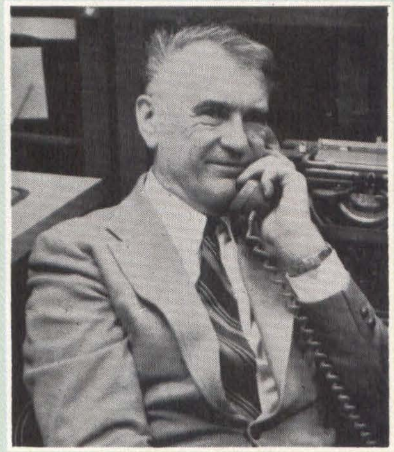


The No-Language: a modest proposal

Though it's the child of computer science, the microprocessor now also belongs to logic designer, whose training, techniques and requirements are different from those of computer people. The third revolution is more than just a new chip; it is also a new user group of people who must use that chip.

Circuit designers' stock-in-trade is chips – hardware. We make signals flow from chip to chip; the microprocessor lets us perform this task with small static charges rather than wire and wrap. In the microprocessor our signals travel between registers; internal registers are lettered (A, X, PC, etc.) and external ones are numbered (0000 to FFFF).

As we learn to use the microprocessor, we discover two annoyances. First, there is no simple way to tell the microprocessor what to do next. Second, there is no simple way to keep track of register numbers – when we use registers in a complex sequence, they grow hopelessly tangled.

To solve the first problem' in part, computer people have devised what they term "language." But their "machine language" or "object language" uses impossible-to-remember microprocessor code numbers. Their "assembly language" uses confusing and inconsistent 3-letter "mnemonics" (a work from Greek, probably meaning "difficult to remember"). They also have "higher-level" and "applications-oriented" languages, but there's currently some question as to how appropriate those languages are for some microprocessor based systems.

Computer people do have something explicit, easy to remember and universal, but they are coy about it – they don't even call it a language, and they haven't named it. In their instruction-set tables, they include a column, either labeled "operation," "functions," "description" or "Boolean arithmetic operation," or else unlabeled. The column succinctly states, in engineering terms, each possible signal transfer and operation.

This is the language for circuit designers. Because of neglect it needs a little pruning and bolstering, but it is all there, immediately available and useful. Perhaps the IEEE should convoke a standardizing conference of users to ensure that this "no-language" becomes universal for all current and future microprocessor chips.

The no-language also needs a new keyboard – one about the size of a typewriter/hex keyboard combination. Each key would signify either a register name or an operation symbol; to write a program you'd visualize what you want a signal to do next and then push the corresponding keys. Until such a special keyboard becomes available, you could assemble one from standard components.

Karl V Amatneek

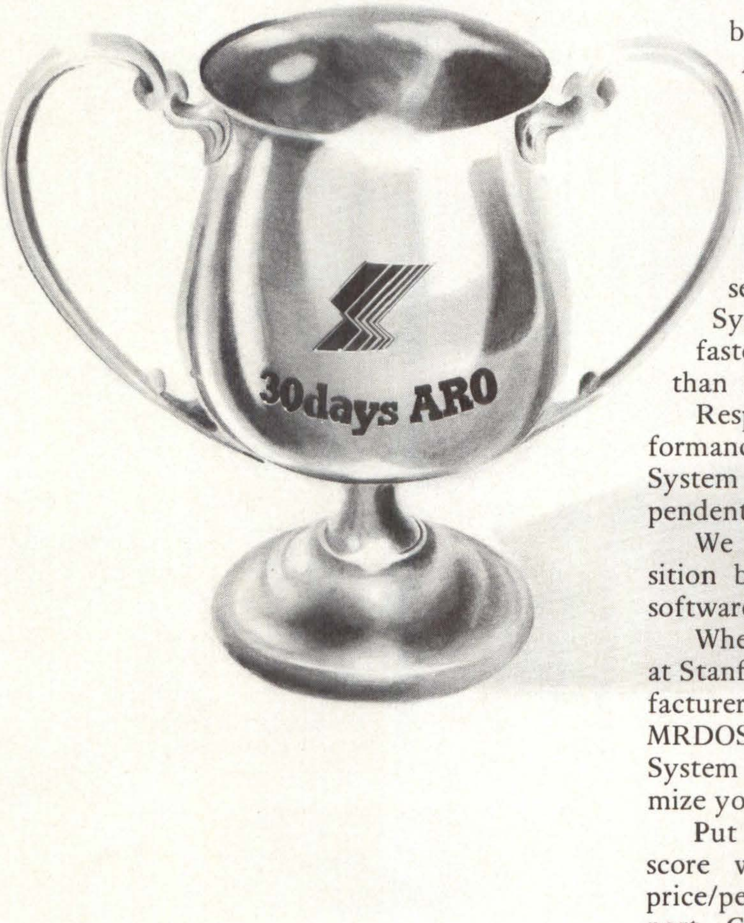
Karl V. Amatneek *is president of KVA Associates, Wyndmoor, PA, consultant at Hahnemann Medical College, Philadelphia, and chairman of the Philadelphia IEEE section's Committee on Professional Update. Next month, he'll propose one way of dealing with the second problem he's cited here. We will be pleased to provide space for opposing views.*

Stanford: 300 Mbytes
DEC: 0

We helped Stanford score a win against slow delivery of minicomputer disk storage.

When Stanford University's School of Earth Sciences needed a fast large-file disk system for its PDP-11/34 application, it found that the minicomputer manufacturer couldn't deliver.

That's when Professor Jon Claerbout began looking for other alternatives. And that's when we proved our capability to deliver the right system in just 30 days ARO.



But quick delivery wasn't the only reason the Stanford group chose our 300 Mbyte system for geophysical signal processing. In the words of Research Assistant Bob Mathews, "The System Industries disk is considerably faster at swapping full-size core images than most disks available."

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CIRCLE 2

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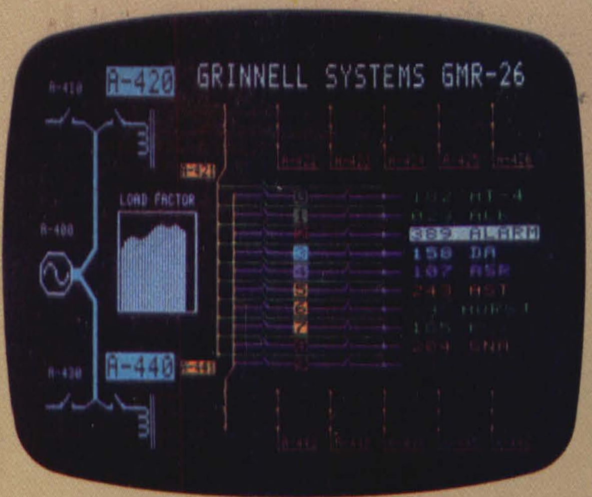

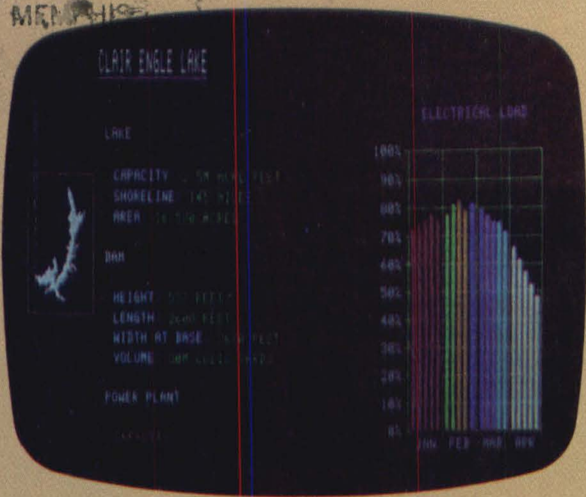

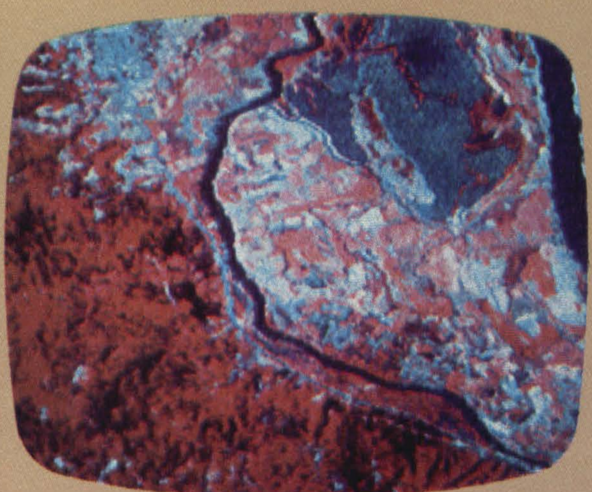

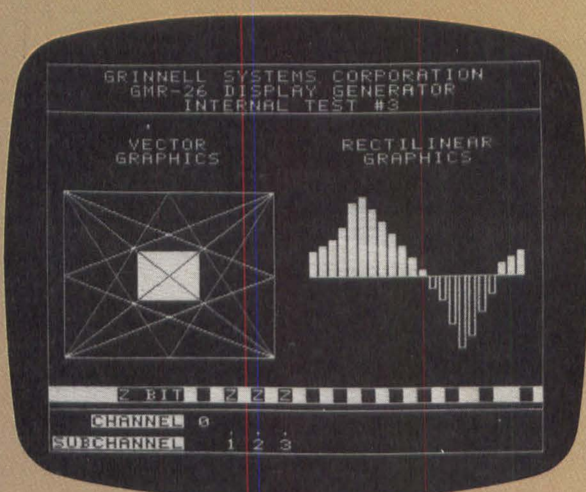

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