



Lou Mazzucchelli on:  
Software Engineering

# COMPUTER DESIGN

*Technology  
and Design  
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

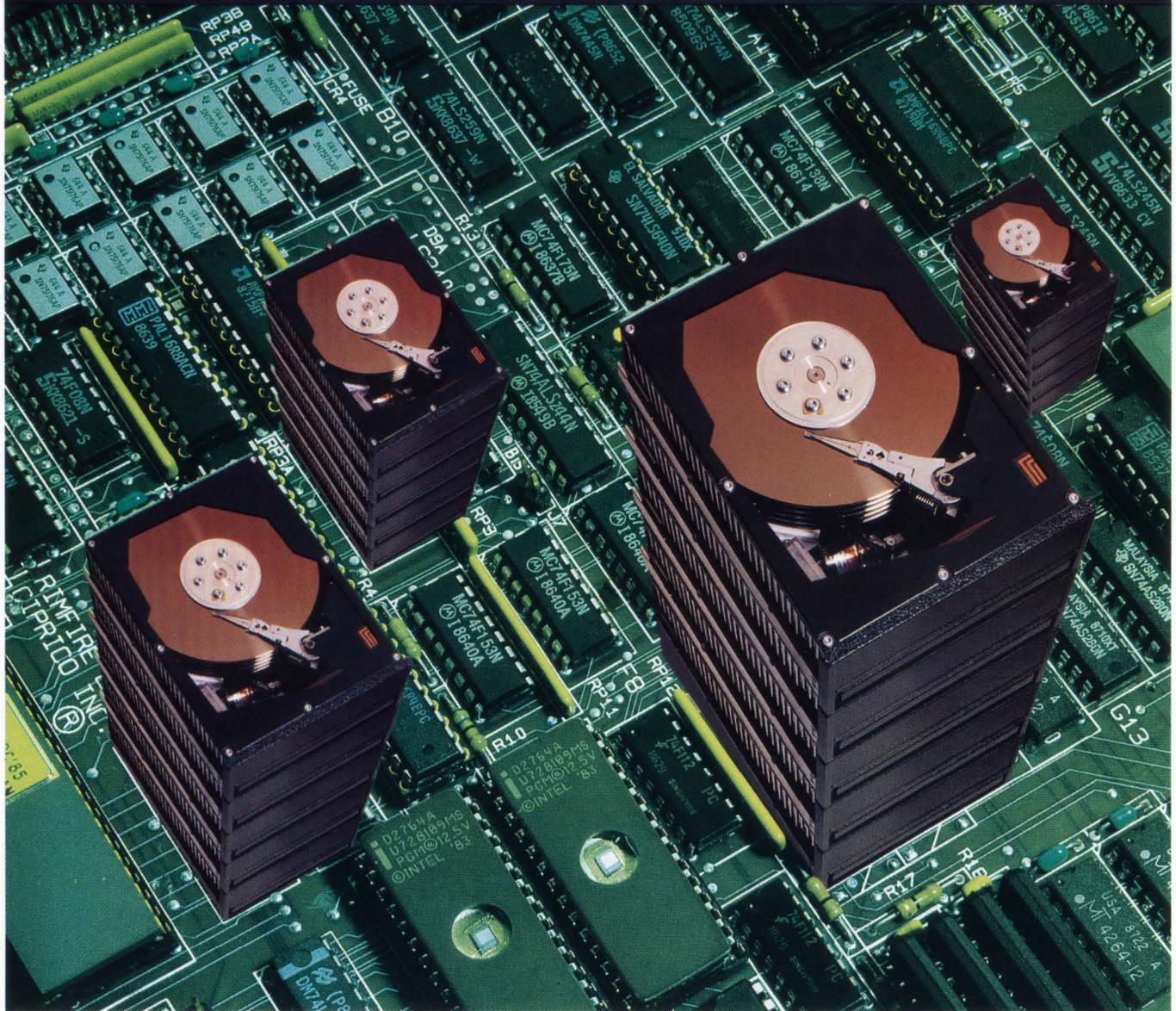
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Software tools integrate the management  
of complex design projects

X Windows terminal designers  
search for a single-processor solution



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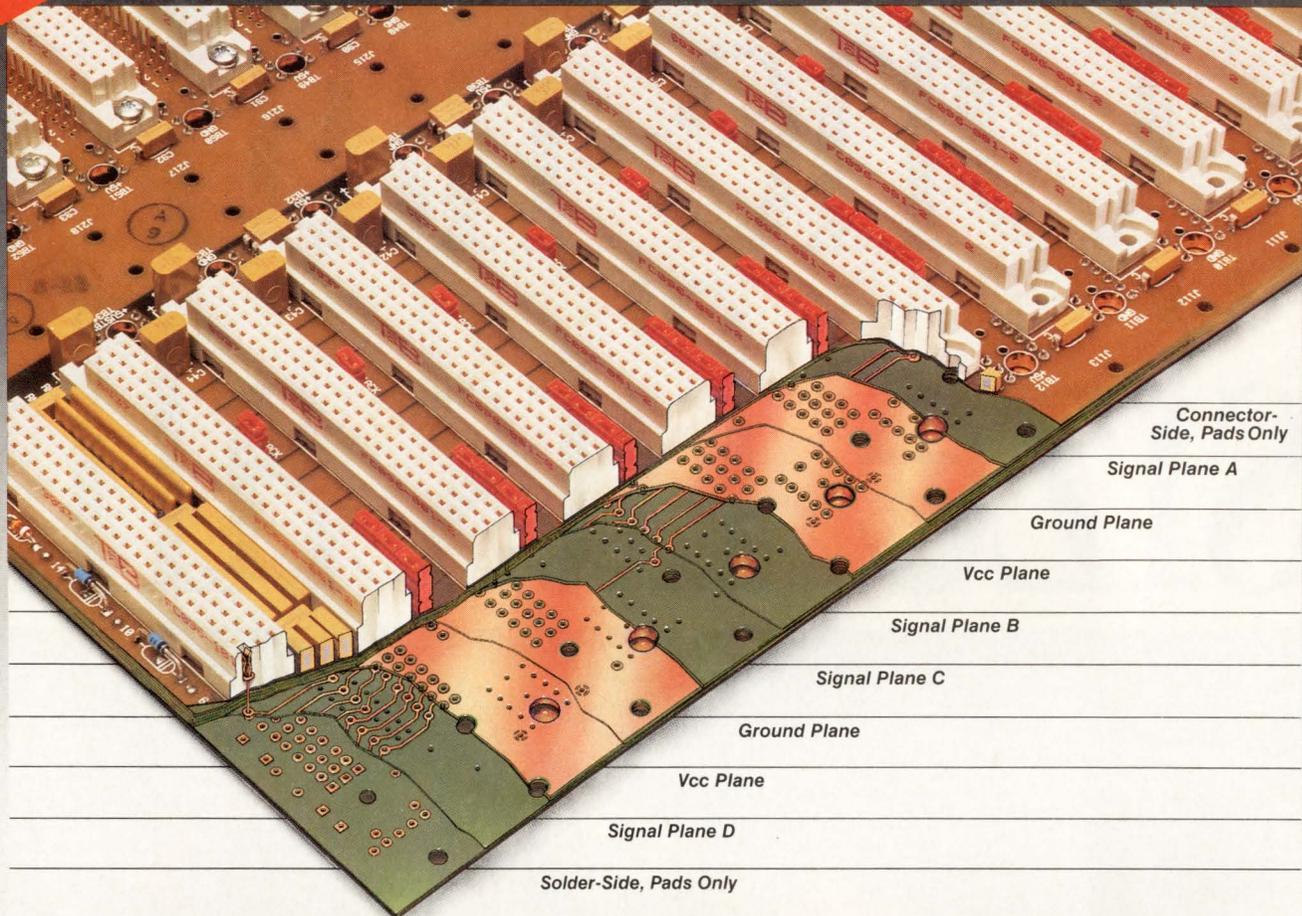
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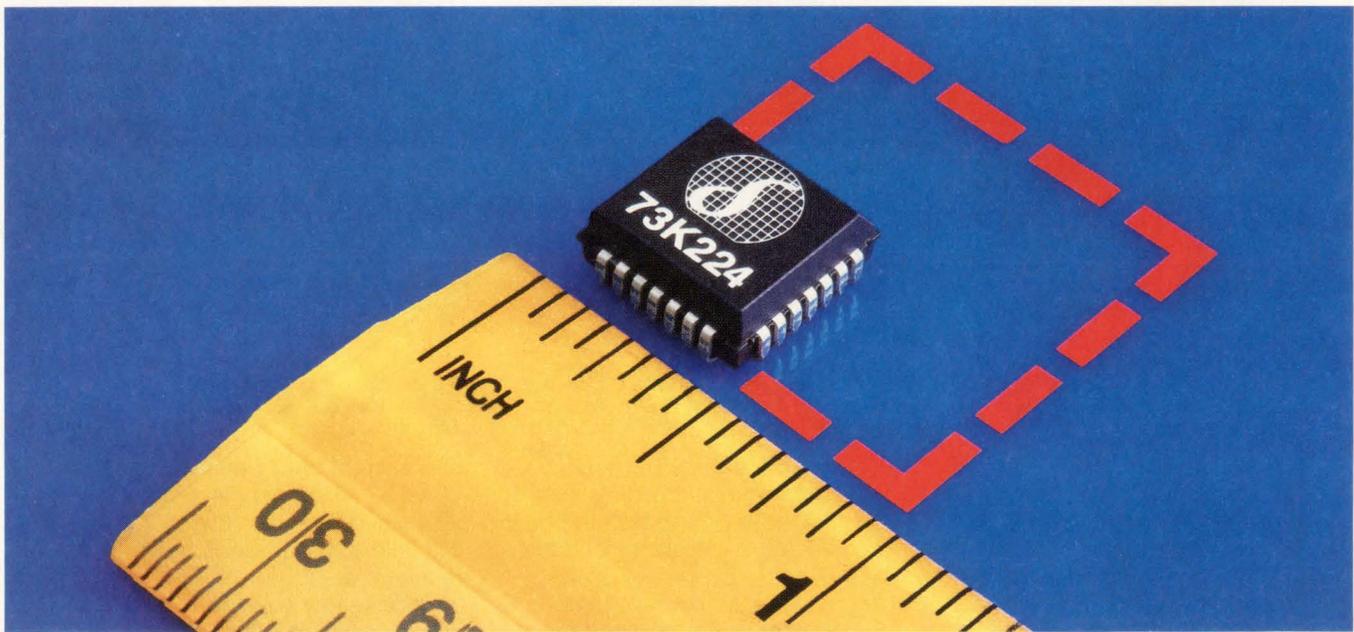


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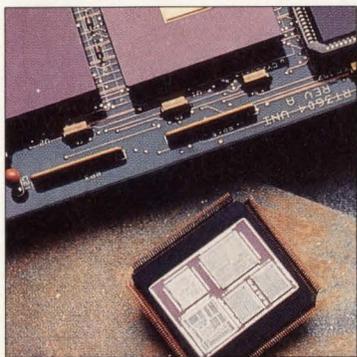


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# COMPUTER DESIGN

*Technology  
and Design  
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



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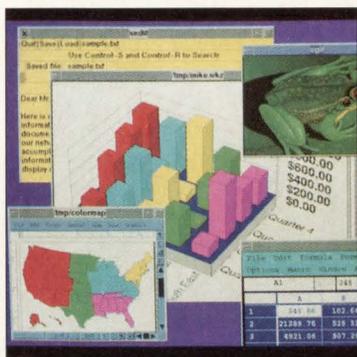
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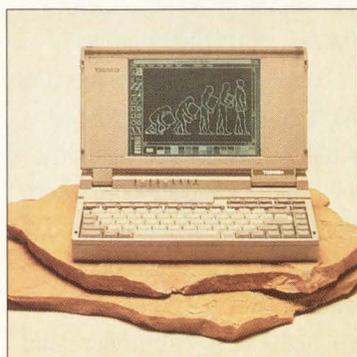
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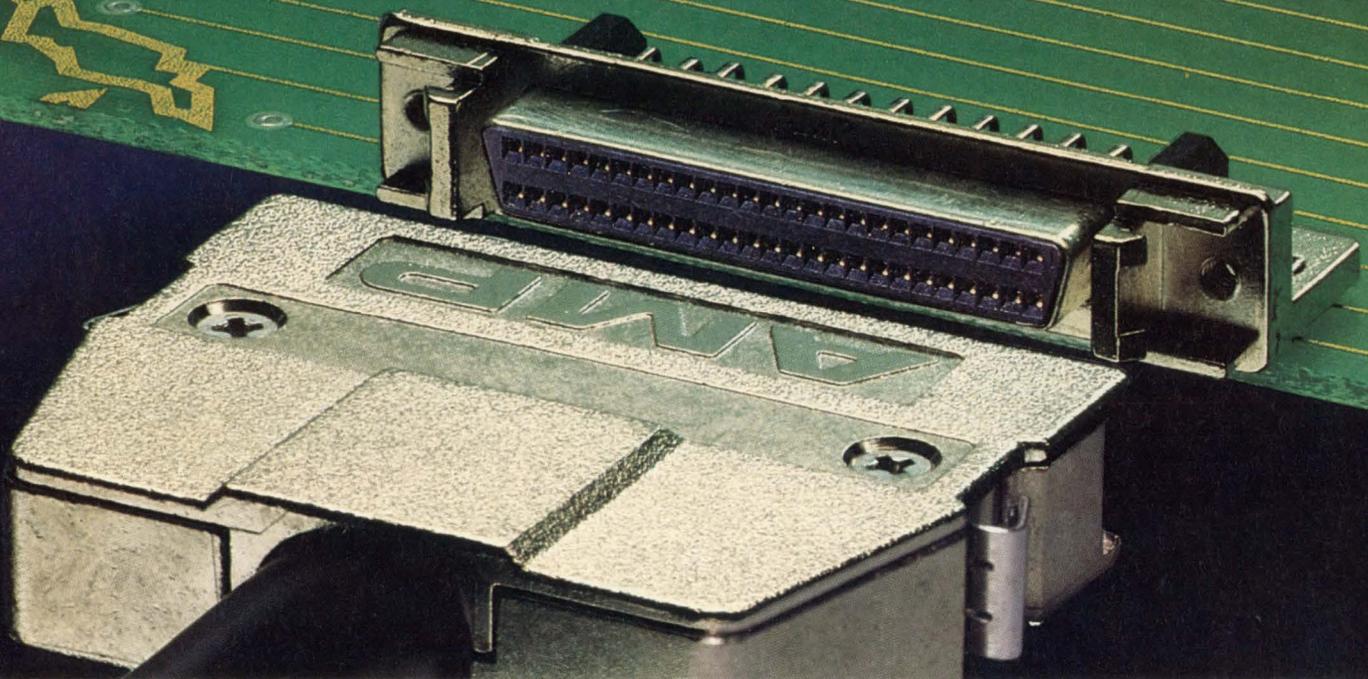
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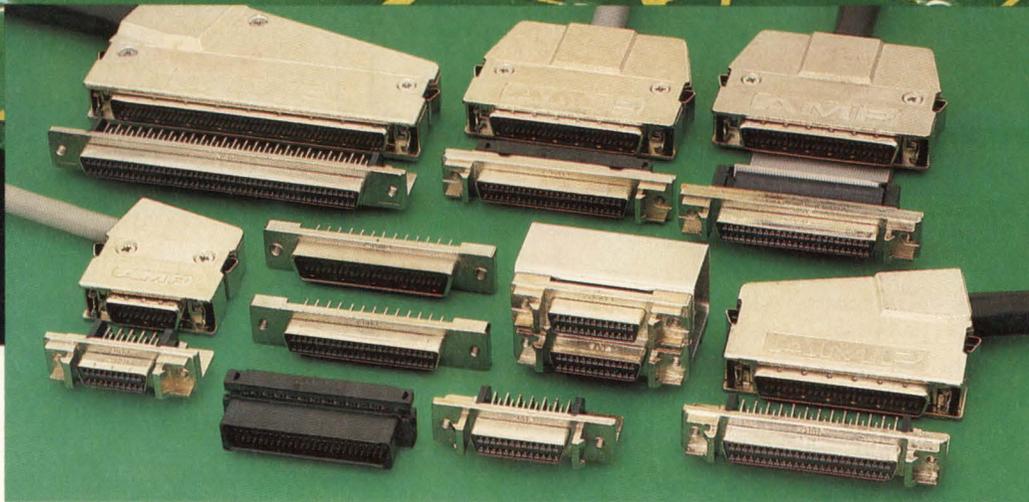


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## IBM/Apple marriage marked by uncertainties

After all the ballyhoo about the agreement between Apple and IBM under which the two companies will standardize on the IBM RS/6000 RISC architecture, a few words of caution may be in order. One is that the two were pretty vague about the software that's to come out of the "jointly owned, independently managed" company that will be set up. If it's to be successful, that company must aim not only at the higher-end versions of current machines, it must also address a large portion of the existing application base. The other industry standard consortium recently announced — the Advanced Computing Environment (ACE) — has vowed to do just that, basing their systems on the MIPS R4000 and Microsoft's version of OS/2. Another aspect of the announcement that's unclear is the networking agreement that appears to draw Apple into IBM's enterprise systems — will it exclude other vendors?

We are faced with two rival "open systems" efforts which represent the struggle between IBM and Microsoft and their respective allies, processor architectures and operating systems. The only common ground seems to be the vow by both groups to support Unix. But then the Unix world, too, is split into two "open systems" efforts.

— Tom Williams

## IBM/Apple/Moto deal sparks 88000 doubts

The announced cooperative agreement between Apple and IBM that will have Motorola manufacturing the IBM RS/6000 Power PC microprocessor has apparently sent shock waves through the ranks of users of Motorola's own 88000 RISC processor. The 88Open Consortium issued a statement that read in part, "We are confident that Motorola's commitment to its 88000-based customers is unabated." The statement doesn't have a very confident ring to it.

Since Motorola has stated publicly that it will offer the Power PC chip on the merchant market,

the 88000 could be in trouble in the long-term. And even if the Power PC confusion doesn't permanently hurt the 88000, there eventually will be a shake-out among RISC processors. With their combinations of design wins in embedded systems and workstations, the i960 and the Sparc are not likely to go away. Since being designated the follow-on to the military's 1750A, the MIPS R3000 is likely to be around a while, and MIPS' R4000 is the processor chosen by the Advanced Computing Environment (ACE) effort. Among other RISC contenders, the AMD AM29000 certainly has the edge over the 88000 in design wins. With entrenched competitors like these, how many more RISC processors can the market accommodate?

— Tom Williams

## New microcontrollers near release at Moto

Motorola (Austin, TX) is planning to release four new derivatives of its HC16 microcontroller family. Code-named "Cutthroat," "Tuna," "Walleye," and "Pike," the devices will be announced later in the year. All the devices will be based on an HC16-based CPU core and will borrow heavily from the peripheral functions now used in the Motorola 68300 family. These functions will include a time-processing unit (TPU) and a new 8-bit A-D converter. The 68300 family may also sprout a new member, code named "Orion" and sporting flash EPROM and SRAM, in the same time frame.

— Dave Wilson

## Group lays groundwork for lower-cost FDDI

A consortium of major FDDI (Fiber Distributed Data Interface) vendors is laying the groundwork for a new technology that will make FDDI's 100-Mbit/s bandwidth available over unshielded twisted-pair wiring. Dubbed the Unshielded Twisted-Pair Development Forum (UDF), the consortium will include Apple Computer (Santa Clara, CA), AT&T Microelectronics (Allentown, PA), Crescendo Communica-

tions (Sunnyvale, CA), Fibronics (Hyannis, MA) and Ungermann-Bass (Santa Clara, CA). Additional members are expected to join later this year.

On the week of August 19th, the UDF consortium plans to make its initial presentation to the ANSI X3T9.5 TP/physical medium dependent (PMD) working group. The consortium will offer a demonstration of the technology at the Interop conference in October.

The UDF consortium will propose a dual physical-media-dependent standard that supports both shielded and unshielded twisted-pair media. Both standards will be fully compliant with the current X3T9.5 FDDI physical layer and media-access layer specifications.

The ability to implement an FDDI network using unshielded twisted-pair wiring is expected to make FDDI cost effective in a much broader range of applications. Until now, high cost has restricted the use of FDDI primarily to backbone applications.

— Jeffrey Child

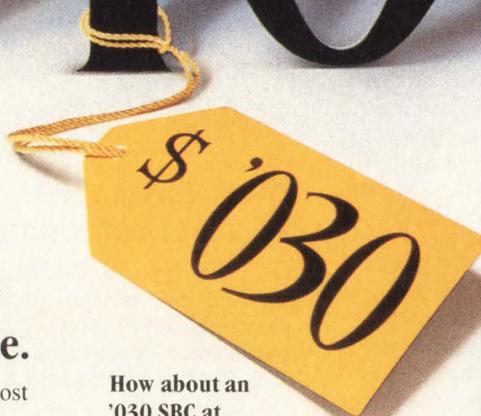
## One more step toward VME Rev. D

Early in August, VME vendors will be sitting down in Phoenix to take the next step in the finalization of Rev. D. Initially planned as the 64-bit extension, VME64, Rev. D has taken on new proportions as a number of vendors are pushing to include added features. The hot items on the agenda have become SSBLT (Source-Synchronized Block Transfer), open-boot PROM and the use of hardware semaphores. Of these, the item most discussed has been SSBLT.

As initially proposed, the high-speed block-transfer mechanism will boost VME performance to the 160- to 200-Mbytes/s range. An early conflict between the SSBLT proposal and the VME64 specification regarding the use of address-modifier codes has been resolved. But a number of other issues remain to be addressed. These include block size, fixed or programmable clock and a throttle mechanism.

Continued on page 10

# '040

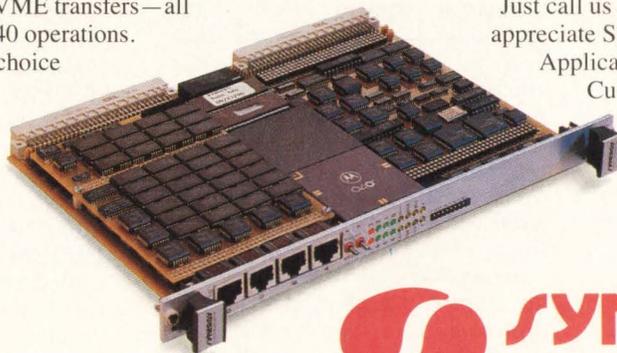


## Synergy brings you the power of an '040 SBC at an '030 price.

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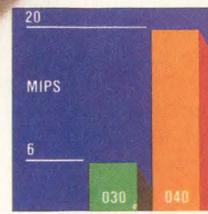
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CIRCLE NO. 7

*Continued from page 8*

Initially, proponents hoped to have all the details finalized in time to develop working models and have the spec on the books by the beginning of next year. It now appears likely that the details won't be settled for several months, delaying final approval until well into 1992.

— Warren Andrews

## Batteries are the focus of new environmental regulations

In a move to keep rechargeable batteries out of landfills and incinerators, many states are enacting or considering new environmental regulations affecting rechargeable products. Effective July 1993, all battery-operated consumer products sold in certain states will be required by law to have an "easily removable" battery feature. The purpose of the "easily removable" legislation is to make it possible for consumers to remove all batteries from appliances and electronic products before discarding them. Currently, Minnesota and Connecticut have passed "easily removable" laws.

An unforeseen result of the new regulations could lead to potentially hazardous operation of rechargeable products. The danger arises when a discharged rechargeable battery in a standard form factor, such as a C cell, is replaced with a non-rechargeable battery. If the product has an automatic recharging circuit, the non-rechargeable battery will be subjected to a recharging current, creating a potentially hazardous situation.

Helping to simplify the designer's task of complying with these laws, Gates Energy Products (Gainesville, FL) has developed a battery system called Intellilink, that allows throwaway batteries to discharge normally, yet would prevent recharging them. The system includes a battery/circuit interface that enables manufacturers to make batteries easily removable and replaceable, without sacrificing the convenience of automatic recharging.

The Intellilink technology will initially be available on the company's own AA, C, and D-sized batteries. According to Gates, the technology will be made available on other well-known brands of rechargeable batteries soon.

—Jeffrey Child

## Futurebus+ market projections rewritten

Rumors are starting to surface that a major Futurebus+ project is already in the works from a European telecommunications vendor. The project is said to call for some 300 systems.

If the rumors are confirmed and delivery is contracted before the end of 1991, it will obsolete all current estimates of Futurebus+ sales. If the total value of this contract is added to the few contracts from AT&T and others, the dollar volume in Futurebus+ could approach \$50 million for this year—more than twice the most optimistic estimates.

— Warren Andrews

## ASIC blocks for wireless communications

On its entry into the wireless communications market with a fully-packaged and tested G.721 transcoder application-specific standard product (ASSP), VLSI Technology (San Jose, CA) has also made the transcoder function available as a building block for ASIC implementation. The block complies with industry-standard specifications, such as CCITT and ETSI. The transcoder block may be combined with other communication-specific blocks, standard libraries, silicon compilation, and synthesis tools to produce a customer-specific, cell-based communications systems chip.

VLSI claims that its low-power transcoder for 32-kbits/s advanced differential pulse-code modulation (ADPCM) is just a first step into the wireless communications market. "We currently have development activities ongoing in digital cellular telephony as well as cordless telephone products," says Nick Kucharewski, vice-

president and general manager of VLSI's communication products division.

—Barbara Tuck

## Micro Linear to build wafer fab

Micro Linear (San Jose, CA) is building its own 6 in.-wafer fab to manufacture mixed-signal and analog ICs for applications such as 2.5-in. disk drives and FDDI (Fiber Distributed Data Interface) networks that require highly integrated systems-level solutions. Until now, Micro Linear's mixed-signal devices have been fabricated by outside manufacturers. The new 14,000-ft<sup>2</sup> facility will accommodate Micro Linear's advanced digital BiCMOS, CMOS and high-speed bipolar processes. Full production is expected by mid-1992.

— Barbara Tuck

## One vendor's attempt at media manipulation

One company considering a new RISC processor for an embedded application has informed *COMPUTER DESIGN* that the processor's vendor refused to part with preliminary information on its architecture until the design firm agreed to let its name be used in endorsements by the vendor. These endorsements were to appear in the vendor's press releases. Are we about to see a day when a designer's request for technical information must be approved by a vendor's public relations department?

— Dave Wilson

## Cheap Sparcs Fly

At less than \$6,000, the Sparcstation ELC is Sun Microsystems' (Mountain View, CA) cheapest Sparcstation. Based around a 33-MHz integrated integer/floating-point Sparc processor, the ELC supports up to 64-Mbyte memory and a SCSI port for disk, tape and CD ROM. Since the convection-cooled system board was housed inside the high-resolution monochrome monitor, no room was left over to support the SBus I/O Bus.

—Dave Wilson



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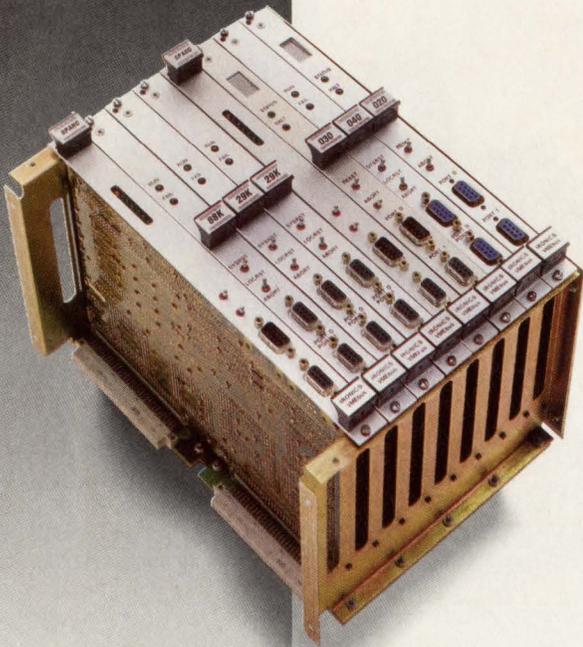
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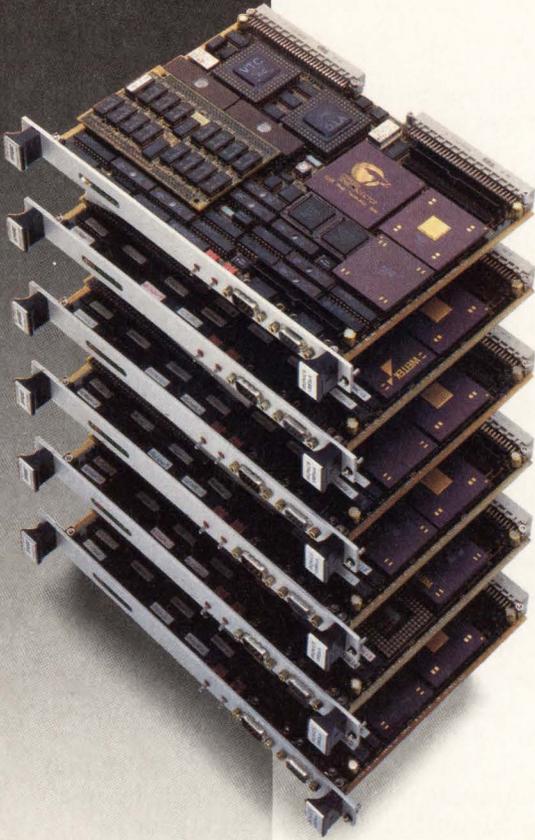
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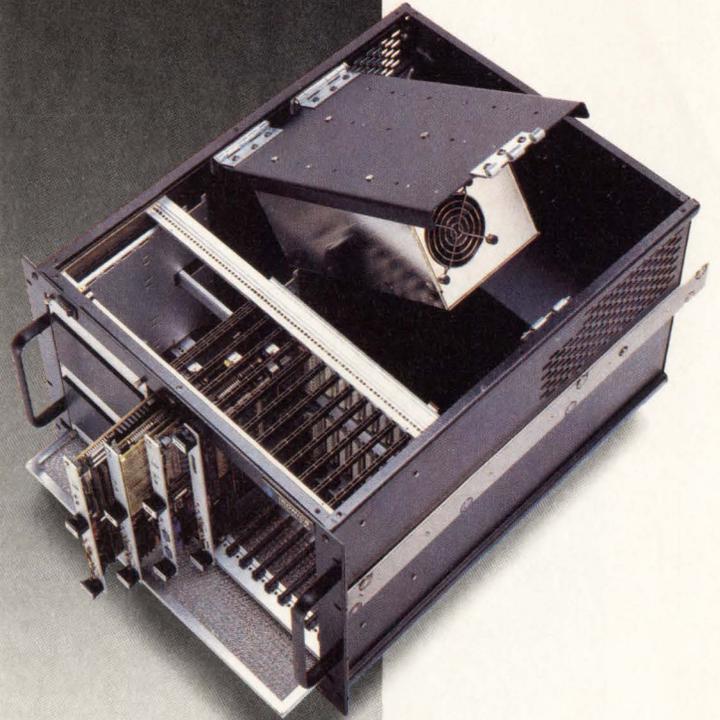
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CIRCLE NO. 11

CIRCLE NO. 12

## The dream is over

**By endorsing a version of IBM's RISC 6000 called Power PC, Apple has sold out to IBM.**



**Dave Wilson**  
Senior Editor

**T**he 1980s will be remembered as the decade that was wasted debating the relative merits of the Apple Macintosh and the IBM PC architecture. Apple has just ended the debate. By endorsing a version of IBM's RISC 6000 called Power PC, Apple has sold out to IBM. To prevent Motorola from sending all their Macs packing, and perhaps to kill off Moto's own RISC, Apple and IBM roped in Moto to manufacture the RISC 6000 chip. As an IBM strategy, it's clever enough, but fatally flawed.

Since its introduction of the PC, IBM has had its clock cleaned. It has totally lost control of the hardware and software architecture of the PC. When IBM attempted to make the PC more proprietary, through Micro Channel, the clone vendors designed EISA. Users continued to buy ATs. When IBM tried to introduce a new software standard like OS-2, Bill Gates (who preferred to make more money upgrading existing PCs with Windows/DOS) screwed up. Users continued to buy DOS. Then there were the clones. Taiwanese PCs made it attractive for users to purchase anything but IBM. IBM looked silly. And IBM got mad.

To make IBM's blood boil, fly-in-the-ointment Apple Computer built friendlier computers. Worse, Apple manufactured a proprietary product that no one cloned. IBM got envious. And why not? Here was a company that could get away with charging \$2,000 for a computer with a \$40 processor in it.

You'd have to be terminally naive not to see the motives behind this latest flight of IBM marketing fancy. IBM and Apple build a new PC architecture based on an IBM-designed chip made by Motorola. Motorola makes the processor available on the open market as a gesture to open systems — but (like the Mac) that doesn't necessarily mean the system will be open. Software is jointly developed by Apple and IBM. At last, IBM gets to tell Gates, the Taiwanese, the EISA bunch and the ACE group to go to Hades in a handbasket. IBM controls the chip, the software, and so they think, the market.

Will the new strategy work? Not outside the boardrooms of Apple and IBM. First, the installed base of DOS machines is huge. It has the greatest momentum in the history of computing. The 80X86 DOS architecture will not disappear overnight, or in ten years. Unlike IBM, Intel and Microsoft are not stupid enough to walk away from all those millions of DOS users. Intel will continue slashing prices on the 80X86 family, and Microsoft will make DOS friendlier. By the time DOS Version 6 comes along, it may even look like the Mac OS with a few Unix features thrown in. Intel's 586, expected far sooner than the 6000, will have the power of RISC and CISC combined on a die with three million transistors. Will you throw away your Intel/Microsoft/PC investment for a Unix-based IBM/Apple/Moto sales pitch? Don't laugh too loud.

Apple, once the innovative upstart, changed markedly when the Pepsi generation took the helm. Now they'll be wearing wingtips and reading the *Wall Street Journal* before *COMPUTER DESIGN*. Goodbye, Woz. Goodbye, Steve. The dream is over.

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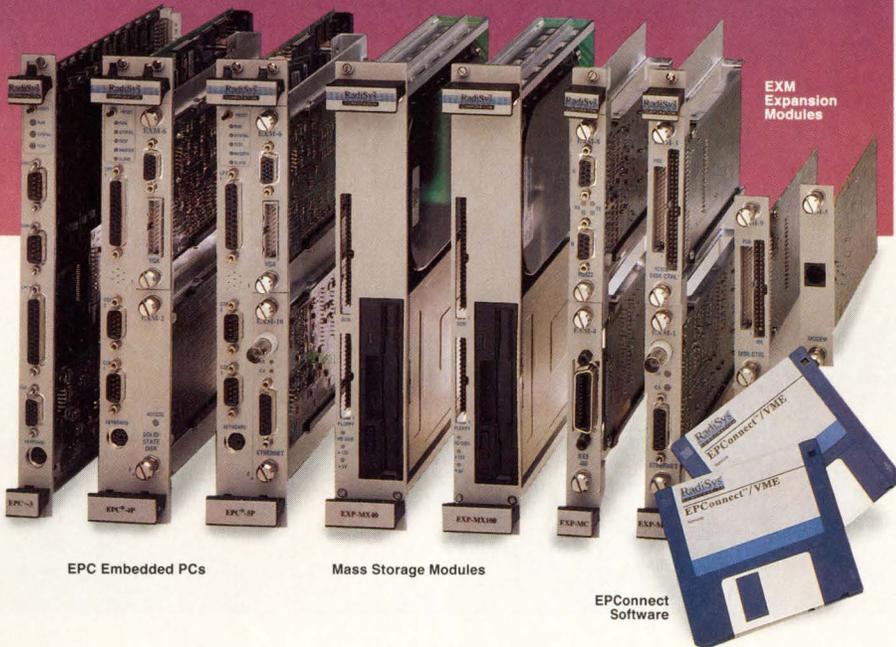
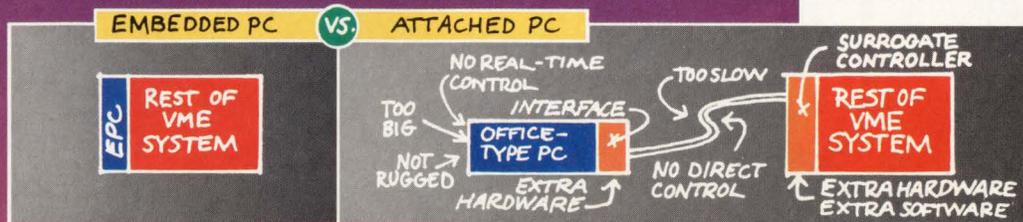
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Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
<b>Mass Storage Modules:</b>				
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Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
<b>Expansion Capabilities:</b>				
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EXMbus Expansion	N/A	EXM Expansion Modules:		
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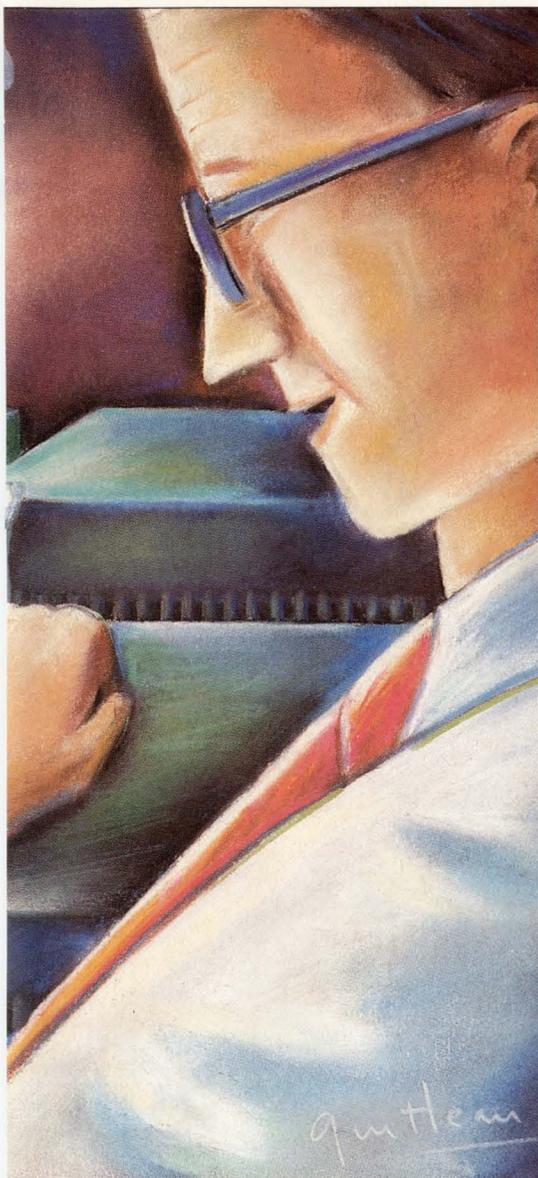
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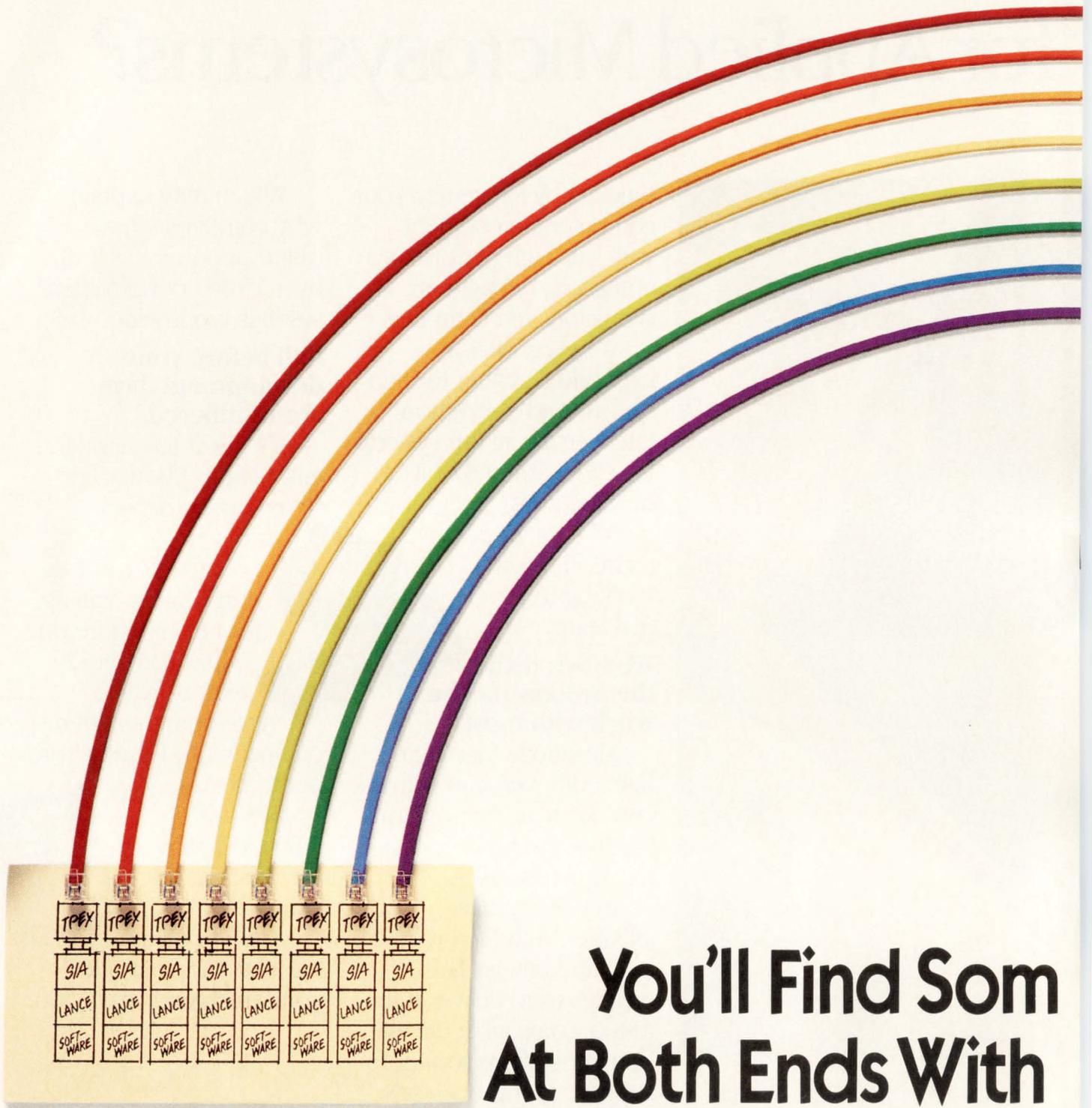
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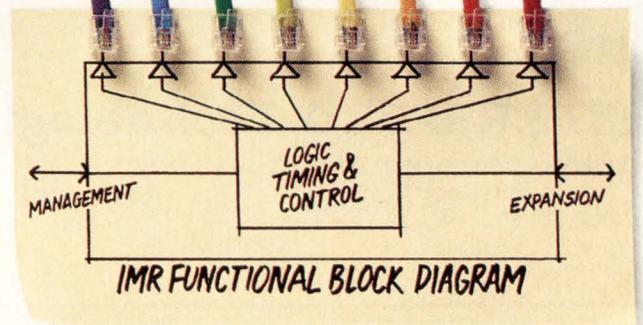
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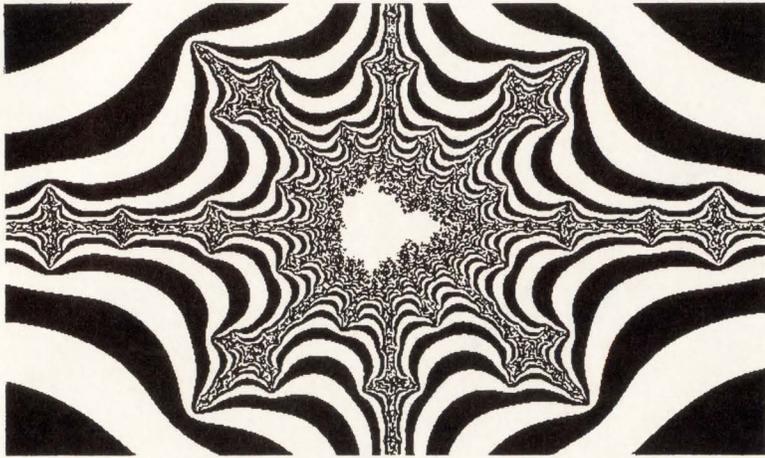
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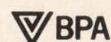
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## CALENDAR

### CONFERENCES

#### September 11 - 13 BUSCON/91-East

Omni-Shoreham Hotel, Washington, DC. The industry's leading board- and systems-level show makes its mid-Atlantic debut this year in Washington, DC. The first glimpse of advances in bus architecture, from Multibus II to VMEbus, Futurebus+, SBus and Turbochannel, plus the newest offerings among other elements of systems architecture—boards, backplanes, chips, embedded software and operating systems—will highlight the show. Information: Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856, (800) 243-3238, fax (203) 857-4075.



Circle 259

#### October 30 - November 1

#### Analog & Mixed-Signal Design Conference

Santa Clara Marriott, Santa Clara, CA. The Analog & Mixed-Signal Conference is dedicated to the unique needs of mixed-signal design. Over 50 lectures and workshops will focus on subjects including transmission line effects in high-speed design; mixed analog/digital design; modeling, simulation and test; and much more. Information: Angela Hoyte, Miller-Freeman, PO Box 7843, San Francisco, CA 94120-7843, (415) 905-2354, fax (415) 905-2630.

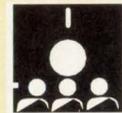


Circle 260

#### September 24 - 27

#### Embedded Systems Conference

Santa Clara Convention Center, Santa Clara, CA. The Third Annual Embedded Systems Conference will offer 75 intensive lectures, panel discussions and workshops on real-time programming, microprocessors, microcontrollers, CASE, embedded project management, programming languages, debugging and algorithms. Tutorials will be offered on building software teams and synthesis. Information: Angela Hoyte, Miller-Freeman, PO Box 7843, San Francisco, CA 94120-7843, (415) 905-2354, fax (415) 905-2630.



Circle 261

#### October 1 - 3

#### SysComp/91-East

Royal Plaza Trade Center, Marlborough, MA. The industry's first exclusive OEM systems/sub-systems components conference and exposition. Workshops and technical sessions will focus on technical solutions and directions involving microprocessor system architecture, OEM systems and software, power sources, interface technology, mass storage, systems packaging and manufacturability. Exhibitors will include vendors of critical systems building blocks including software, boards, complex microcircuits, power sources, storage systems, displays and other ancillary products. Information: Betsy Anderson, marketing specialist, COMPUTER DESIGN, One Technology Park Dr, PO Box 990, Westford, MA 01886, (508) 392-2209, fax (508) 692-0525.



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#### Would you like your event listed here?

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# Lou Mazzucchelli on: Software Engineering

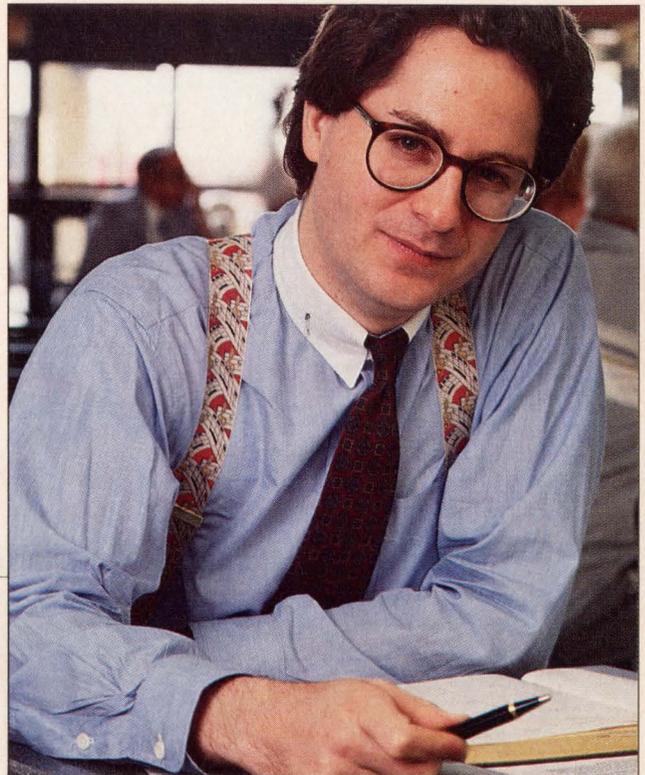
In the 21 years I've been involved with software development, everything has changed—and nothing has changed. Sure, people use different computers, programming languages, operating systems, user interfaces and applications software now than when I was a novice. But we're still struggling to develop systems. Software development is still basically a freestyle event in most organizations. Software consumers are not satisfied with either the quantity or the quality of our output. We continue to look for the breakthrough technologies that will obviate our problems, and have yet to agree on standard practices for most of our work. "Software engineering" describes what we aspire to, not what we do.

## ■ The problems in software engineering

Why can't we do better? When we face the issues of software development, we usually trace our problems to multiple sources, including (but not limited to) bad programming languages, bad operating systems, bad methods or methodologies, bad tools, and bad management. But our typical response to these problems is to invent new programming languages, operating systems, methods, methodologies and management techniques. When coupled with the tremendous rate of change in other fields, this adds up to a continual flood of new technologies. Many of these technologies affect our work as software developers, but do not themselves advance our discipline. Only a small portion of new technologies will be of lasting value.

Unlike other engineering disciplines, software engineering is based as much upon hope and persuasion as it is upon science. This should make anyone generally skeptical of advances in our field, but too often we're forced to suspend disbelief in the face of market pressures that have little to do with technical reality. This phenomenon creates tremendous distractions which inhibit our understanding and resolution of the key problems in our field, and keeps software engineering a poor relation to other forms of engineering.

Let's look at how this happens. A look at technology expectations and realities shows how market dynam-



ics lead to the creation of a "technology vacuum." When a new technology is first described to the world, it can be met with skepticism or open hostility (our expectations may be low—the diagram on the next page shows this as a negative "expectation" value against a positive "reality" value). As time passes, some systems or products are built using the technology. Given any proof of efficacy, our expectations take off at a very rapid rate. But rarely does the technology keep up with our growing expectations. The diagram shows that it might keep pace at first, but soon there's a tremendous difference between expectation and reality. This gap is a "technology vacuum."

Technology vacuums can apply to hardware or software technologies, but the strength of the vacuum is stronger for software. This is because physics applies to hardware, and tends to moderate our collective enthusiasm. There are exceptions, like the ex-CEO of a once-prominent Lisp machine company who blithely commented in the '80s that by the '90s, everybody would have a Lisp machine on their desks. And people actually believed it!

It's important to note that we all contribute to the creation of technology vacuums. Developers want their technologies to succeed. Entrepreneurs and venture capitalists want companies based on new technology to succeed. And consumers want to believe that we're just one technology away from greatness.

## ■ The impact of technology vacuums

You can imagine that some technology vacuums can be very strong indeed. They manage to suck in a lot of players who see a "market opportunity." In the mid-'80s we saw a profusion of new CASE companies responding to expectations that software productivity

could be improved by a factor of 10. Now many of these are extinct. In the '90s we're seeing a new wave of companies responding to the expectation that object-oriented technologies will solve our software problems.

The vertical drop from the crest of the wave of expectations, as shown on the diagram, reflects the fact that when the technology cannot meet our expectations, we tend to lose interest fast. Our expectations plummet. If our expectations are reasonable, this is a clear case of technology evolution in action. If, however, our expectations are overly inflated, we run the risk of losing potentially valuable technology. Note that development of the technology can continue for a while even after the general market loses interest, but not for long unless it's a key component of some other product or technology.

Inevitably, and usually quite soon, a new wave of

not evolve. First, let's look at the example of computer hardware technology evolution.

Even in first-generation computers, standardized components (tubes) let us build larger standardized components (gates) from which we could build larger (module) and larger (subsystem) components. Along the way, engineers and managers learned how to use subsystem components, and evolved some standard engineering practices.

### How technology affects management

Transistors eventually proved to be a better technology than vacuum tubes. Because of informal or formal standards at each level of system abstraction, engineers could replace the lowest-level technology (tubes) easily, without having to redevelop the higher levels. Engineering managers, who may not have been intimately familiar with the new technology, could still apply their knowledge of module and subsystem engineering to help keep the project on track.

With the advent of integrated circuits, a level of system abstraction was absorbed into a new component technology, letting most designers work at the module level rather than the gate level. An engineering manager who wasn't completely knowledgeable about integrated circuit design could still function effectively because the new low-level technologies did not affect the high-level system description.

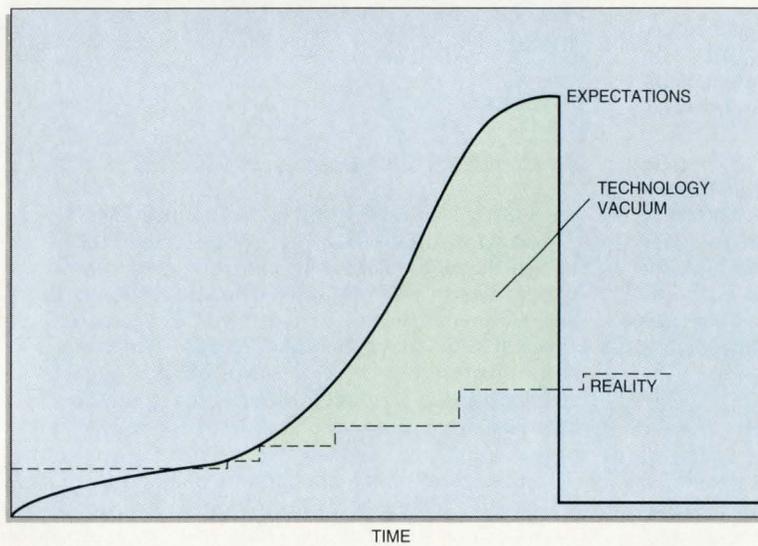
Software technology issues are very different from those of hardware. Our lowest-level software "materials" are programming language statements. There are hundreds of available programming languages to choose from. Some, like Ada, have a rigorously defined statement syntax. Others, like C, exhibit variations at the level of statement syntax. But this is the good news. The bad news is that, once above the instruction level, there are no standards for module, subsystem and system definitions.

Because of a lack of standardization above the instruction level, there's a tendency in software designs to have the entire system design influenced strongly by details of the lowest-level technology.

There are at least two serious problems with this. First, systems designed this way (dare we say badly?) are very difficult to migrate to newer implementation technologies when they become practical or popular. Secondly, those managing the development of such systems must be conversant in the lowest levels of technology to make effective design decisions. This places more-experienced managers at a disadvantage unless they are willing to become "technology surfers."

As the name implies, technology surfers ride technology waves. Technology surfing is fun and exciting.

## Technology Expectations And Realities



*Users' expectations for any new technology follow the pattern of a wave. When a new technology is first announced, the expectations of potential users are low. Initial skepticism typically keeps expectations below what the technology can actually deliver (the reality of its capabilities). But as the reports of any early successes circulate, expectations begin to rise rapidly, soon exceeding reality. The amount by which expectations exceed reality creates a technology vacuum and leads users to attempt applications beyond the technology's real capabilities. In the final stages, expectations plummet as reports of user failures become common.*

technology expectations begins to rise, a new vacuum is quickly created to occupy our interests, and the same cycle begins again. In the hardware world, most new technology expectations derive from advances in materials. In the software world, the situation is different, and much more pernicious.

Gerry Weinberg, author of several books on software management, likes to remind us that the biggest problem in software development is management. Software managers are at a serious disadvantage compared to hardware managers because of the way software technologies evolve, or more accurately, do

A technology surfer is always on the leading edge. Nonmanagement engineers who are technology surfers contribute to our industry. But engineering managers who are technology surfers are dangerous. They are always focused on implementation details (trying to stay on the wave), and rarely get time to think about the big picture (crossing the ocean). This lack of higher-level perspective leads to bad judgment when making design tradeoffs, especially when under pressure to fill a strong technology vacuum with the latest wonder technology.

### ■ Catching a wave

When a new technology wave begins to appear in the middle of a development cycle, technology surfers panic. Regardless of the state of the project, they'll find some way to jam this new technology into it. This would not be so bad if the impact were localized to the lowest layers of the system. But, because we don't have good standard practice for software design, more likely than not, the system architecture will be affected. This is a recipe for a project that will be, at the very least, late.

Earlier, we mentioned that new hardware technology waves were driven by advances in materials. Since the materials level is separate from other systems levels, but related to it in standard ways, much of our knowledge can be preserved across successive technology waves. But in software, most new technology waves are driven by changes in fashion. While a new hardware technology can and must demonstrate superiority in price, performance, power consumption or manufacturability before being widely used, a new software technology needs only the groundswell of public acclaim and the smallest proof-of-concept before being hailed as the next great thing.

Because new hardware technologies are very expensive to develop, companies are very selective about which technologies they choose to develop and release into the market. This tends to limit hardware engineers' technology choices to a manageable number. But because the initial cost to develop a new software technology is low, and anyone can develop one, software engineers are faced with an overwhelming number of competing technologies and no good way to evaluate them.

### ■ When is a wave all wet?

One way to evaluate a new technology would be to compare it incrementally against existing technologies. But most software technologists go for the revolutionary—the big hit. It also means that in espousing the revolutionary nature of the new technology, there will be few references made to prior technology, except disparaging ones. New terminology will litter the countryside. A thousand new concepts will bloom. Only later do we find that many of the revolutionary concepts are like new sheet metal on an old auto chassis, and the new terminology is just a different paint job. In the meantime, we've discarded many of our prior skills in our rush to embrace this new technology, and now must rehabilitate ourselves at considerable cost. Had these technologies been positioned as incremental advances in the first place, they might not have garnered as much interest from the marketplace, but they would

have been easily evaluated and added to our collective software engineering knowledge.

All engineers are under pressure to keep up with new technology. This pressure comes from the same sources that drive technology expectation curves up so quickly. Cadre recently did some market research to explore how many people were using a new technology. We were surprised by the high percentage of affirmative responses until one participant commented, "If I said I'm not using this new technology, I'd look like an idiot."

When a technology is demonstrated to deliver compelling economic advantages, migration is necessary and obvious. When a technology is only *claimed* to deliver compelling economic advantages, migration is neither necessary nor obvious. We need to examine it closely to see if it constitutes a material advance before embracing it. Otherwise, we're just responding to the pull of the technology vacuum.

### ■ Ask some hard questions

What are some of the questions we should ask of new software technologies? Any question with the words measurable or provable is a good start. For example, "What are the measurable advantages of using new language X instead of language Y?" Follow this quickly with, "Where did you get your data?" Questions about compatibility are useful: "How does this new software technology work with what we've already got?" If the answer is, "it doesn't, you must fully embrace the new," we may be doubly skeptical because it's unlikely we'll scrap all of our existing technology. And a new technology that's incompatible with the present is likely also to be incompatible with whatever shows up in the future.

Failing to ask hard questions of a new technology, and going with it anyway, makes us technology surfers. We are now on the development team for that technology. We'll inevitably spend precious resources and considerable effort developing that technology instead of developing our products. If the technology ultimately fails, this effort is wasted. If it's successful, there's still no guarantee that our product will be successful because much of our effort will have gone into mastering the new technology.

In the preface to their landmark book, *Computer Architecture, A Quantitative Approach*, (Morgan Kaufmann, 1990) Hennessy and Patterson describe "a new approach to demystifying computer architecture—it emphasizes a quantitative approach to cost/performance tradeoffs. This doesn't imply an overly formal approach, but simply one that's grounded in good engineering design." Until a quantitative approach is applied, technology waves will continue to pound away at the software technology base, changing it at random, and washing away much of what has gone before.

*Lou Mazzucchelli, is vice president and chief technical officer at Cadre Technologies (Providence, RI).*

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## Multimedia waits for faster video processing chips

Dave Wilson, Senior Editor

**D**ave House, senior vice president of Intel (Santa Clara, CA) disclosed recently that Intel is completing the development of a programmable video processor with PictureTel (Peabody, MA) that will offer 10 times the performance of Intel's i750 video processor. The new device will be capable of on-line, real-time compression and decompression and compatible with MPEG, JPEG, CCITT, and Intel's current PLV and RTV algorithms. Intel has already shown some details of the SIMD (single instruction multiple data) architecture under nondisclosure.

But Intel isn't the only vendor interested in building such a multimedia processor. Motorola, Brooktree, Texas Instruments, Integrated Information Technology, LSI Logic, C-Cube Microsystems, and Cypress Semiconductor to name some, all have MPEG research projects underway.

### Choose your standard

Two standards currently exist for the compression and decompression of motion video—MPEG and H.261 (P×64). While H.261 is devoted to teleconferencing applications, most silicon vendors are racing to build processors to meet the higher-performance MPEG "entertainment-quality" video standard. MPEG's charter is to develop standards for the coded representation of motion pictures and associated audio for storage and retrieval on digital media, such as CD-ROM and CD-I.

"Up until a year ago, MPEG1 was always talked about in the context of 1.5 Mbits/s, and a video format that was a 2:1 subsampled version of broadcast TV," says Cliff Reader, head of the US delegation to MPEG, and an engineering manager at Cypress Semiconductor (San Jose, CA). "People were working with pixel resolutions of 352 × 240 and 1.5-Mbit/s speeds." According to Reader, 1.5 Mbit/s was chosen because it was compatible with T1 transmission channels and the CD's transfer rate. "Then it was realized that the trans-

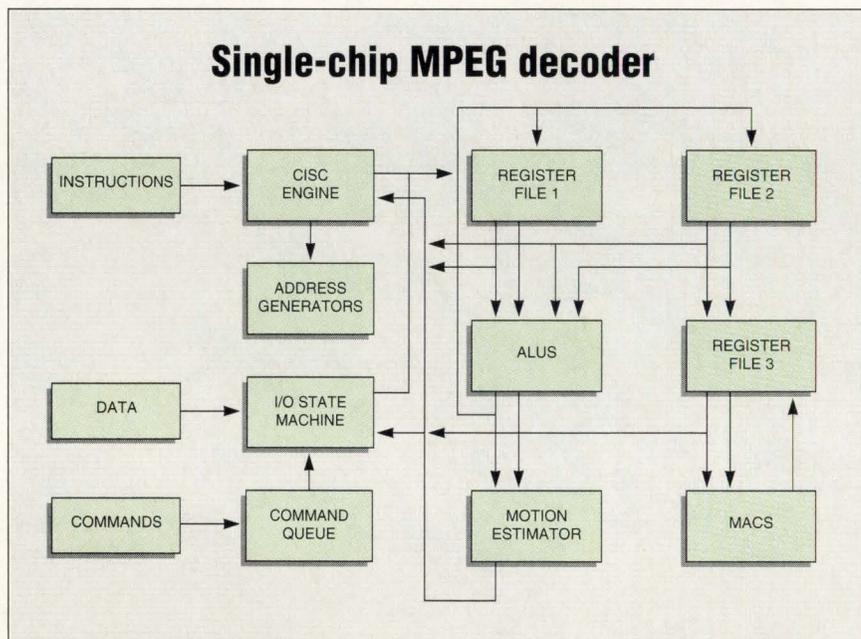
fer rate didn't need to be a hard restriction," he adds.

Hence, the MPEG standard has been written to allow higher bit rates and different formats of image data. The most computationally intensive problem faced by a multimedia MPEG processor is performing the encoding and decoding of images. Of these two, the encode function requires considerably more horsepower. "The biggest difference between MPEG and H.261 is how

that one frame be compared to a single prior frame for predictive motion-compression analysis, the number of frames MPEG compares isn't specified in the standard. "That makes MPEG a lot more difficult," says Teza. But the optional nature of the motion-prediction method means that MPEG encoders are likely to improve over time, as image-compression algorithms improve.

### Chips reflect MPEG complexity

Because the MPEG encoder is so complex, especially in real-time, many encoders on the market today are for H.261. "An MPEG encoder is about three to four times the processing complexity," of an MPEG decoder, says Zohar Raz, market development manager at Motorola



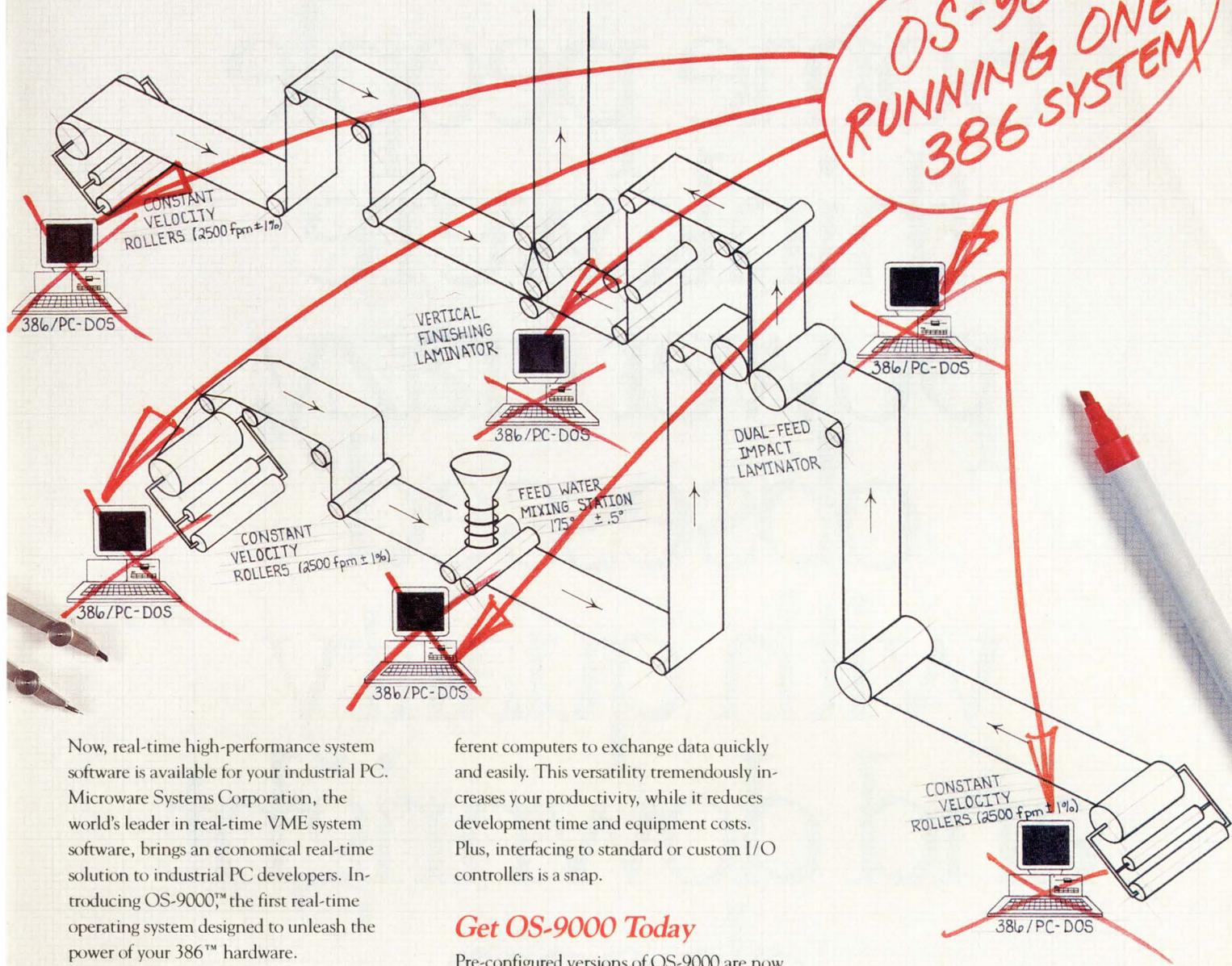
Integrated Information Technology's Vision processor comprises a single-instruction-per-cycle CISC machine and a bank of ALUs that is reconfigurable as eight 16-bit wide or sixteen 8-bit wide ALUs. With one of these processors, designers will be able to build a P×64 encoder.

motion compression is achieved," says Jeff Teza, vice president of corporate technology at Brooktree (San Diego, CA). Both use a JPEG-like technique to reduce the spatial redundancy in a single still image and achieve a 25:1 compression ratio. To get higher compression, motion-compression techniques must be used. MPEG uses more powerful temporal compression techniques than H.261. While H.261 specifies

(Phoenix, AZ), a company that is developing an MPEG full-motion video decoder as well as an MPEG audio decoder.

Most available image-compression/expansion devices either perform a dedicated function, like the JPEG-CL550 processor from C-Cube Microsystems or provide a building-block approach like those from LSI Logic (Milpitas, CA) and SGS-Thomson (Phoenix, AZ). LSI's

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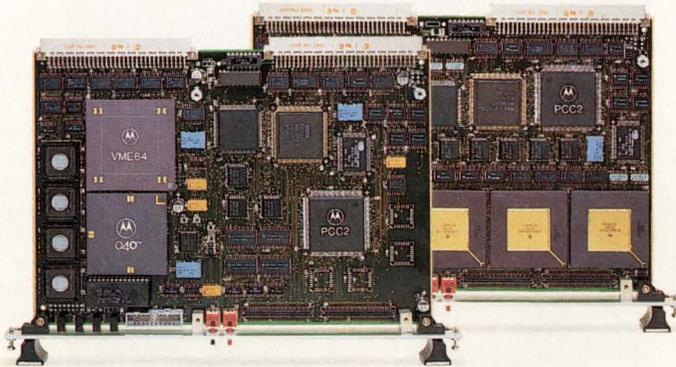
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INTEGRATED CIRCUITS

seven chip set, called the L64700 family, is aimed at the P×64 market. SGS-Thomson offers the IMS A121 discrete cosine transform processor.

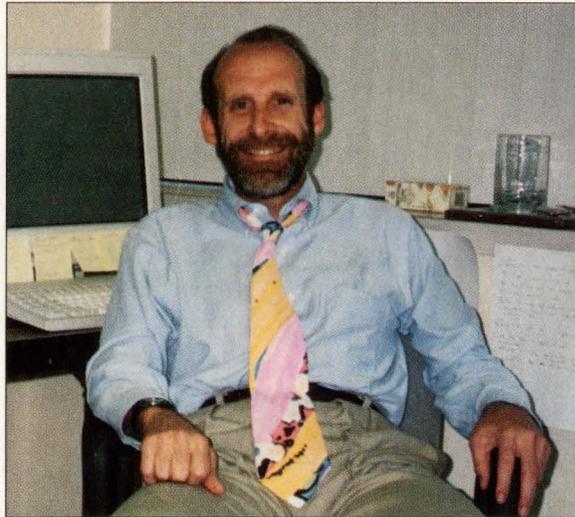
Integrated Information Technology (Santa Clara, CA) has taken a somewhat different approach with its Vision Processor, a programmable device that the company expects (at 40 MHz) to be sufficient to decode and encode a compressed MPEG picture. A single chip is expected to be sufficient to implement the encoder of a P×64 (H.261) CCITT teleconferencing system having a full CSIF (common source input format) resolution at 30 frames/s.

**Goodbye Mips, hello Bops**

How computationally intensive is the MPEG encode function? According to Dr. Pat Hays, director of VLSI engineering at PictureTel, the Intel processor will be capable of 1 Bops (billion operations per second). It will not only perform the decode, but also the MPEG encode function, at 30 frames/s in real-time. "The performance is achieved through architectural parallelism," says Hays. "We have no dedicated hardware on chip. Instead we have designed a more general data path that is highly programmable for functions like DCT and motion compensation." According to Hays, the data path can be programmed to achieve the same speed as dedicated processors and with higher video quality. The device also can be time-multiplexed between different functions.

Texas Instruments (Stafford, TX) has a multimedia chip project under way too. But image processing and multimedia program manager Walt Bonneau indicates that "the (multimedia) problem is into the 2 billion plus operations per second," rather than the 1-Bops figure mentioned by Intel. But Bonneau does agree with Hays that a programmable architecture makes the most sense. Despite this, Bonneau feels that the SIMD approach taken by Intel is limited. "When you structure yourself for only an SIMD operation, you have limited the parallelism aspects of the machine," he says. Bonneau

feels that a MIMD (multiple instruction multiple data) machine, or more specifically a synchronized MIMD machine would be a more effective solution. But it might not be possible to realize such a chip until late in 1992. By then, Bonneau claims that silicon may be available from a num-



Dr. Pat Hays, director of VLSI engineering at PictureTel, says the next generation of Intel video processors will be capable of 1 Bops and will be MPEG compatible. Hays says the new device is highly programmable.

ber of silicon vendors. "But," he concludes, "anyone that has taken a serious look at the demands of multimedia realizes that it's not a single processor function."

**Achieving broadcast quality**

So, even with all its Bops, will MPEG meet the needs of applications in computer, consumer and communications markets? Apparently, not. Brooktree's Teza feels that MPEG lacks capabilities for the broadcast field. The reasons—poor picture quality and lack of support in the specification for interlaced signals. "At 1.5 Mbit/s, MPEG1 is really not sufficient for broadcast quality," Teza claims.

"At 1.5 Mbit/s, MPEG1 gives performance somewhere very close to the decision point between acceptable and unacceptable," says Cypress' Reader. "We've seen some material that looked fine, and some where the quality was questionable." Reader says that there's a lot of research currently underway at many organizations into smart en-

coders to improve the quality of the video at 1.5 Mbit/s. "There are a number of things that you can vary in the encoder to make it work better," he says. "The principal tool is being able to dynamically vary the quantization of the data. People are using statistics gathered from the data to control the quantizer. That can be done on a very localized basis and has resulted in some noticeable improvements in quality."

Designers that demand more than MPEG1 currently has to offer might look to MPEG "JVC extended mode" supported by C-Cube (San Jose, CA) and JVC (Huntington Beach, CA). Robert Soderbery, Manager of System Design at C-Cube says that the MPEG1 bit stream is suitable for CD-ROM applications, where constrained bit rates and low resolution images are used. But JVC and C-Cube are interested in addressing broadcast TV and digital VCR applications as well. To do that, they've extended the MPEG syntax, and optimized the MPEG algorithm for higher resolution and higher bit rate. "Our CL-950 processor [an MPEG decoder running in JVC extended mode] will offer the 6 to 9 Mbits/s that are needed in these applications," says Soderbery. As for an MPEG encoder, Soderbery had no comment...yet. ■

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## Do Machine Visionaries Have Digit Eyes?

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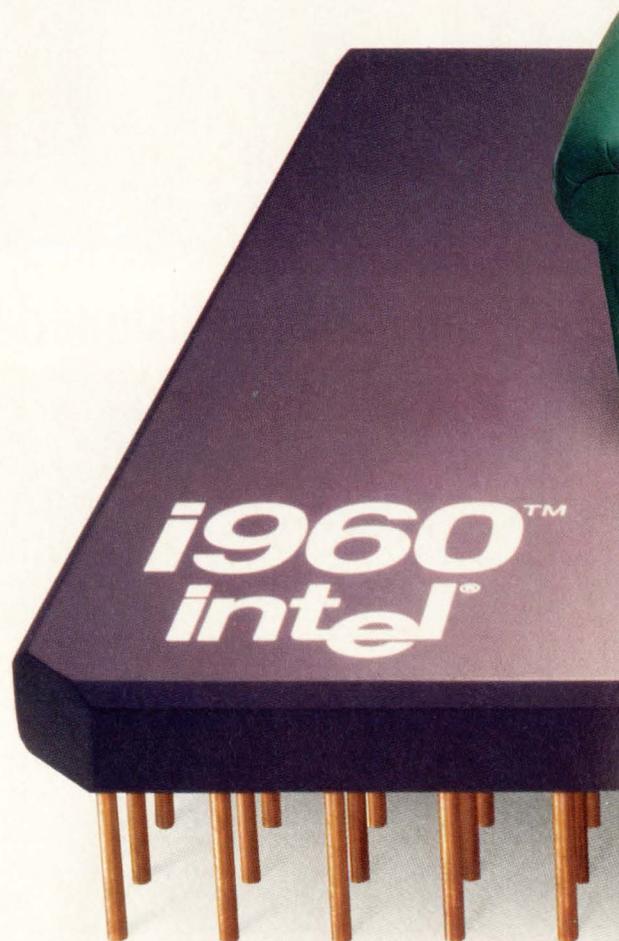
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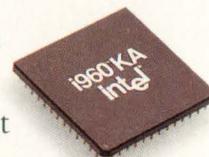
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## Multichip modules deliver high integration, high speeds and high cost

Dave Wilson, Senior Editor

System designers are faced with a problem. Even with today's million transistor chips allowing microprocessor vendors to integrate more functions, system designers can't get everything they need in a single package. When chip vendors make tradeoffs to meet their silicon budgets, there's always a set of customers who feel their needs got lost in the shuffle. Enter the multichip module (MCM).

By allowing a collection of bare die to be interconnected via a structure that resembles a large IC, the MCM holds the potential to let whole CPU subsystems (CPU, floating-point unit, cache controller, and large data and instruction caches) be integrated in a package no bigger than an Intel 486. MCMs also present the designer with the option of choosing functions from a number of silicon vendors and packaging them to meet the needs of a specific application. All of the preceding arguments for multichip modules have been true since the advent of reliable hybrid technology. Yet designers outside of the aerospace industries have steadfastly resisted multichip approaches. But the final argument for MCMs is the most compelling; at 50-MHz processor speeds and above, there appears to be no alternative to the MCM.

### Choices in MCM construction

There are a number of MCM technologies currently offered in the market. Thick film MCMs, like low-temperature co-fired ceramics, use a printed circuit board-like screen-printing technique to create an interconnection pattern. The resulting pattern has thicker features than thin-film MCMs, which use optical lithography to create the pattern image. Tradeoffs between the thick-film and the thin-film MCMs are influenced by circuit requirements such as frequency, speed, precision, and density. Thin film is better suited for high-frequency designs.

Thick film offers a cost advantage.

"There's talk that (MCMs) could be used in high-end PCs and RISC workstations," says Frank Gaughan, district sales manager at Kyocera America (San Jose, CA), an MCM vendor. Gaughan says that Kyocera is involved with approximately 20 MCM projects in the United States. Interestingly, not all of them are aiming for the highest possible system speed at once; some are focusing on operating at 40 MHz or 50 MHz, with plans for 100-MHz operation later.

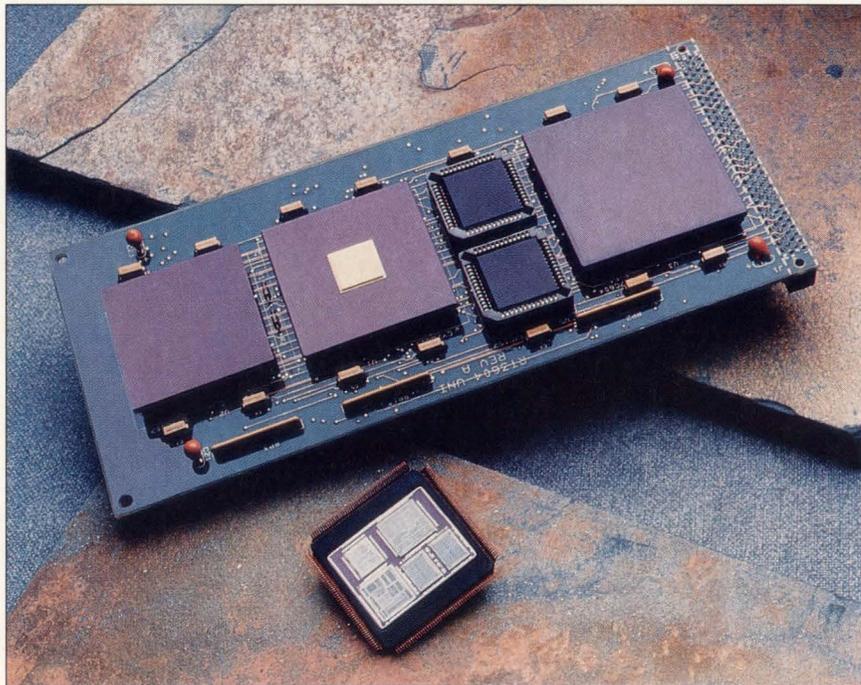
Another MCM vendor, nChip (San Jose, CA), integrates silicon substrate packaging and heatsink technologies with system engineering, module design, assembly, and manufacturing services. The company has developed a wirebonding technique for chip-to-substrate interconnection. By using wirebonding, die-

to-die spacing can be as close as 72 mils. Consequently, the company can cover up to 75 percent of its silicon substrate with chips. The company has already demonstrated this technology in a processor design.

But if MCMs are so great, why aren't more people using them? Steve Eliscu, subsystem marketing manager of IDT (Santa Clara, CA) has some answers. "Nobody has delivered an MCM in volume for an application like a workstation," he says, "because in a RISC-based system with a lot of SRAM and relatively few I/Os, the packaged die are not much bigger than the unpackaged die with wire bonds. You start asking yourself what benefit is there in mounting die on a substrate and then wirebonding?"

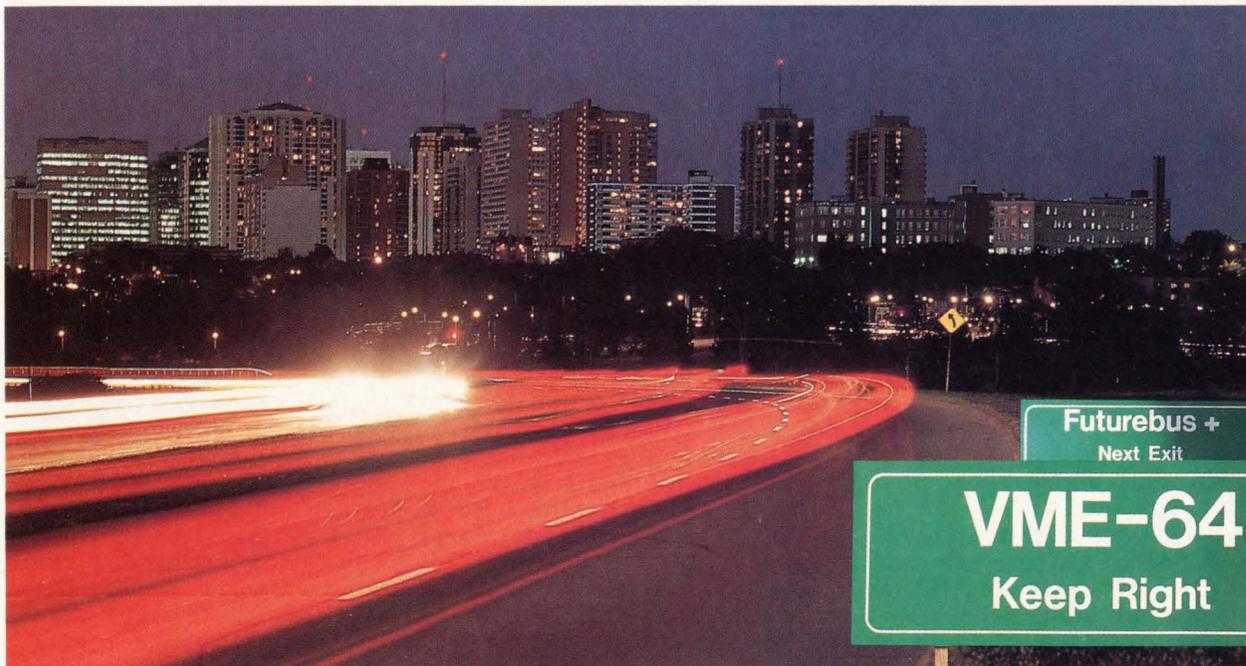
Dirk Smits, director of subsystems development at LSI Logic (Milpitas, CA) agrees. "If you're trying to interconnect four or five chips with 500-plus I/Os, multichip makes sense. We're evaluating similar technologies for those types of problems. But when you have 300 I/O pins and need to connect four or five chips, at speeds up to 40 or 50 MHz, chip-on-board gives you plenty of performance and better economics."

IDT's Eliscu also contends that in



This MCM holds a RISC CPU subsystem containing the same components as the board shown above it. Developed by nChip and Ross Technology (Austin, TX), bare processor and cache memory chips are interconnected on a silicon substrate.

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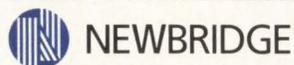
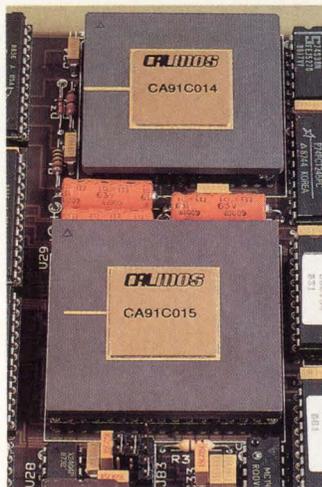
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terms of cost-effectiveness in the commercial marketplace, MCMs have some problems. "First you must bond chips on a substrate, then you have to burn the whole thing in. What happens when one die fails—which is extremely likely after burn-in? Why spend all this money on an exotic substrate, on a technology where the rework and yield issues aren't non-trivial."

Nevertheless, Eliscu feels there's hope. "MCMs will come into their own when the IC houses start changing the I/O structure of the microprocessor, memories, etc.," he says. "By removing the ESD protection structure on an SRAM, for example, or minimizing the size of it, you can increase the performance of the device." Eliscu quotes one SRAM supplier as indicating that 4 ns was lost on the access time of an SRAM when ESD protection needed to be increased. "However," Eliscu adds, "you must know before hand that

the device will be placed directly on an MCM and not handled by many people in the process."

**■ Ceramic rather than silicon**

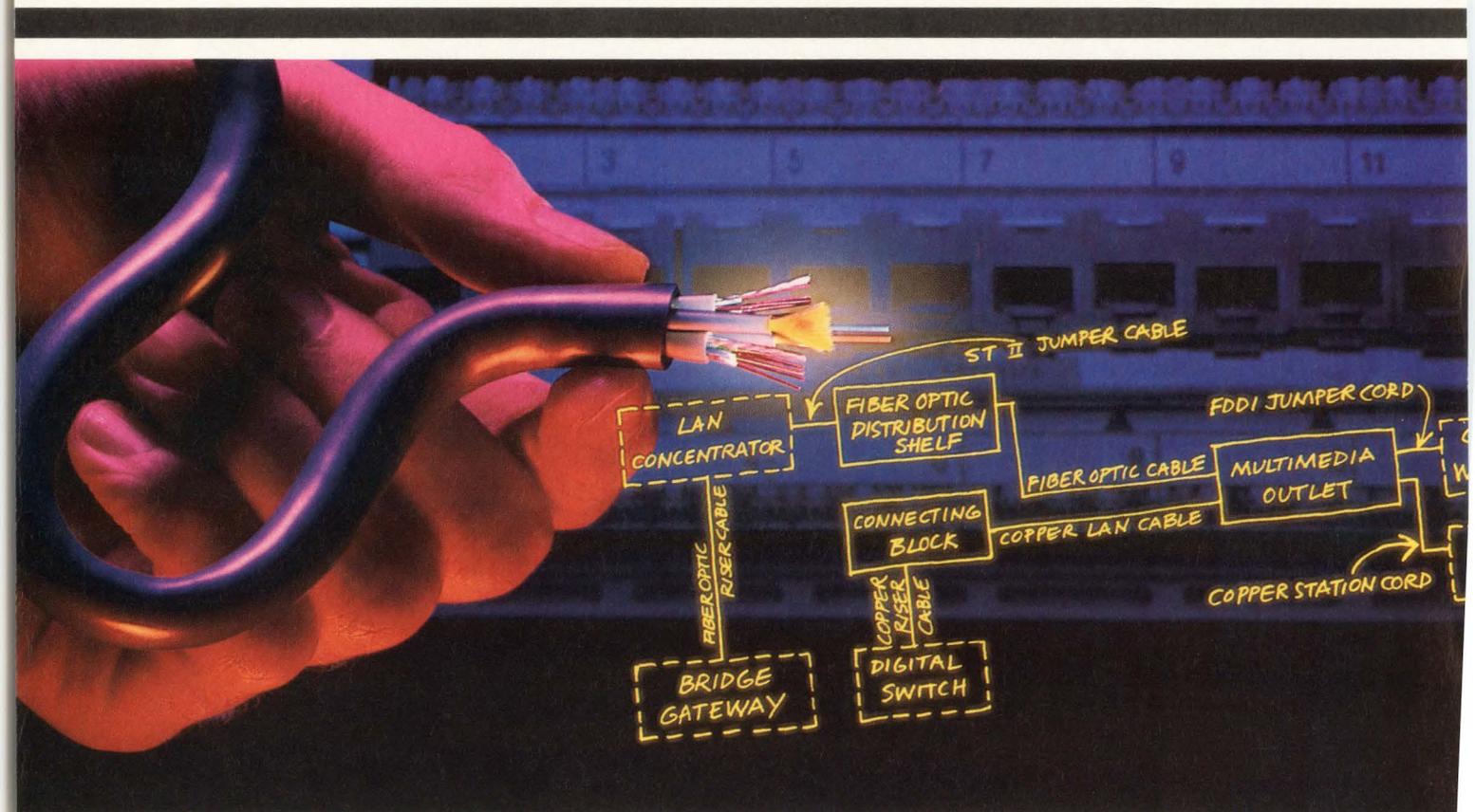
The silicon substrate technology developed by nChip represents only one MCM methodology. Other vendors may use a thin film ceramic substrate, rather than silicon. And tape automated bonding, and flip-chip offer alternative approaches to placing the die onto the surface of the substrate. For example, Kyocera offers an MCM that uses a multi-layered thin-film ceramic substrate. Bare die are mounted on the ceramic substrate and then wirebonded to the interconnection pattern. Despite differences in substrates, wirebonding appears to be widely accepted as the most cost-effective interconnection technology for multichip CPU modules intended for workstation applications.

Above 50 MHz, ground bounce be-

tween power and ground planes in MCMs becomes a concern. The nChip solution is to place a thin-film capacitor in the silicon itself. With ceramic, either decoupling capacitors are used or thin layers of ceramic materials with high-dielectric properties are built into the substrate.

Thermal expansion is more of a problem with a ceramic substrate than silicon. Wei-Tau Chiang, president of ACC Microelectronics (Santa Clara, CA) says that because silicon and ceramic have different coefficients of thermal expansion, a ceramic module will not be able to sustain as wide a temperature range as silicon-on-silicon. Furthermore, with a silicon substrate, there are no catastrophic failures due to the chip attachment to the substrate itself. The geometries that can be put down on silicon are finer than their ceramic counterparts. "On silicon substrates, line widths can go down

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to about 10  $\mu\text{m}$  while ceramic substrates don't allow lines finer than 25 to 30  $\mu\text{m}$ ," says Richard Sigliano, new product development and marketing manager at Kyocera America (San Diego, CA).

What the ceramic approach offers over silicon is that the substrate and package can be offered as a single structure—dubbed either an integrated structure or a convergent package. "You integrate the circuitry with the ceramic package in one monolithic package," Sigliano says. "When you use a silicon substrate, you have to use some kind of enclosure for the package. The nChip substrate is placed into a hybrid package."

Sigliano feels that for the mid-range workstation market, the price of the assembled MCM will have to be approximately 5 percent of the total system cost. "If you take a \$20,000 system, the MCM has to cost between \$500 to \$1000 dollars.

This means that the MCM's package cost should be about \$50," he says.

**MCMs still too pricey**

"The nChip pricing is about the same as our MCM—and they are both too high for that market," says Sigliano. Vendors are demanding that the cost of a high-performance convergent package for an MCM in a high-end (\$40,000 to \$50,000) workstation application has to be \$20/in.<sup>2</sup>

"Everyone wants that number. Major semiconductor manufacturers demand price levels between \$20 to \$25/in.<sup>2</sup>," Sigliano adds. But to get there, Sigliano feels that volumes will need to range from 50,000 to 100,000 pieces per year, with package production yields as high as 80 percent. Neither figure will be easily attained. He believes that it's more realistic to expect prices to stabilize around \$40/in.<sup>2</sup>—and that may be more than the market can bear. "You're talking

\$100 to \$200/in.<sup>2</sup>, for a high-performance MCM package today, perhaps as low as \$75 in volume. In five years, they will get to \$40, not \$20," he adds. "That's why we see a lot of people in the workstation market who don't want thin film ceramic, they demand co-fired ceramic for an MCM. That part is \$8 to \$10/in.<sup>2</sup> which is right in their price range today," he concludes. ■

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CIRCLE NO. 30

## Multichip modules push design tool limits

Mike Donlin, Senior Editor

**M**ultichip modules (MCMs) are moving from the domain of high-ticket military applications to mainstream products such as workstations and personal computers. And as MCMs make this transition, EDA vendors are scrambling to produce tools that will let engineers design and simulate an MCM before the expensive manufacturing stage. But the very nature of an MCM, namely a cluster of bare ICs on a common substrate, introduces some thorny design problems which, if not addressed early, will result in an expensive, untestable product.

Some of the required tools have already been released by EDA vendors; tools that predict the thermal characteristics of components or the transmission line effects that result from closely-packed traces carrying high-speed signals, for example. Routing tools also stand ready to tackle the intricate layering of nets that results when a design that occupied a 12-in.-square circuit board shrinks to a 4-in.-square MCM. Most MCM tools available today are reworked versions of existing design tools. Allegro MCM from Valid Logic Systems (San Jose, CA), for instance, is an outgrowth of Valid's Allegro printed circuit board design tool, although changes had to be made to address the fine geometries of MCMs. "Up until now, many MCM designers have been making hybrids that are characterized by 5- or 10-mil traces separated by 5- or 10-mil spaces," says Shiv Tasker, director of product marketing in the printed circuit board division of Valid. "CAD packages are, therefore, designed to work with these relatively large di-

mensions. To deal with the tight geometries of MCMs, we adapted and reworked Allegro. We changed the database, for instance, from a 32-bit integer capability to a double-precision floating-point, 64-bit design to handle the finer pitches," states Tasker.

Mentor Graphics (Wilsonville, OR) took a similar approach by adapting its Hybrid Station when it recently unveiled the MCM Station design tool. The similarities between hybrids and MCMs made this

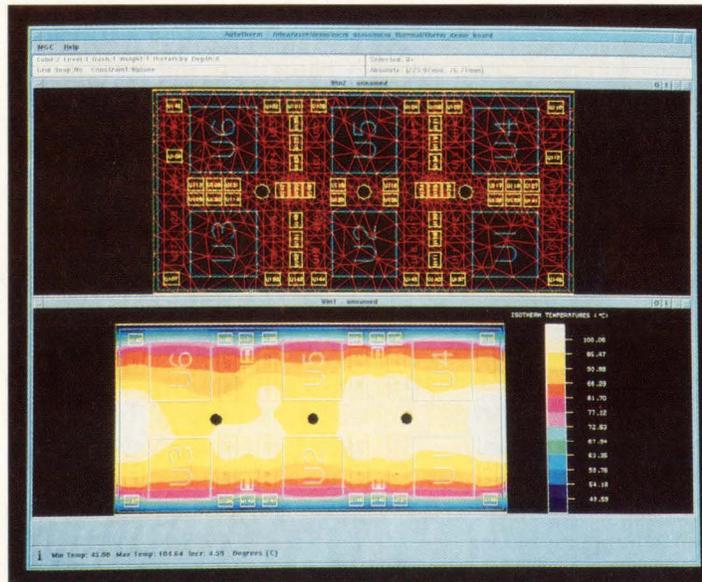
for either hybrids or MCMs," says Stan Drabac, director of marketing for nChip (San Jose, CA), an MCM manufacturer. "So you could call one the other and get away with it. But most people think of MCMs as a number of VLSI digital components on a substrate, whereas a hybrid has a much lower level of integration with a lot of discrete resistors, capacitors and transistors on it."

The high density of VLSI components on an MCM, however, poses problems that designers of hybrids or circuit boards rarely have to face. Component placement, for example, gets critical when 50 devices are placed on a 2-in. square substrate. Thermal characteristics must be back-annotated after placement and preferably before routing, because in such confined spaces even the routed traces can affect thermal behavior.

Dazix (Boulder, CO), a division of Intergraph (Huntsville, AL) has taken thermal analysis a step further than other EDA vendors by incorporating the 3-D features of its CAD tools into its MCM-Engineer design tool. As a result, the tool provides a 3-D thermal image, which models heat conduction between the different materials of the MCM. "Being able to view a 3-D model of an MCM has several advantages," says Ed Miccio, hybrid/MCM product marketing manager at Dazix. "In addition to letting an engineer visualize the thermal ramifications of device placement, the 3-D layout can be viewed

for manufacturing purposes. It gives a designer information about how the package will fit physically with the rest of the system in three dimensions. Placement can then be adjusted taking all these considerations into account."

Placement, of course, affects not only the thermal characteristics of an MCM but also routing efficiency, which translates directly into manufacturability and cost. Any discussion of routers, however, brings up



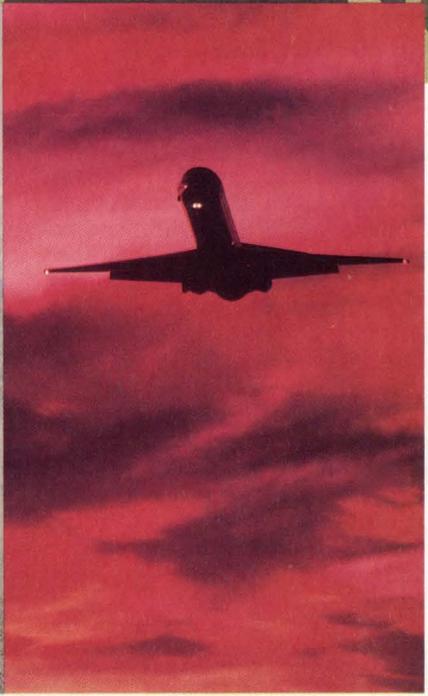
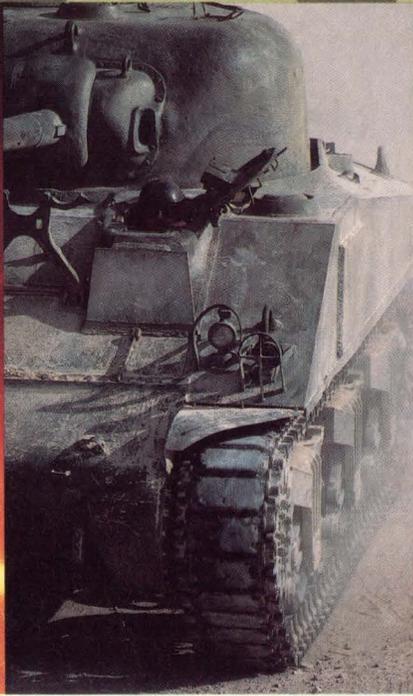
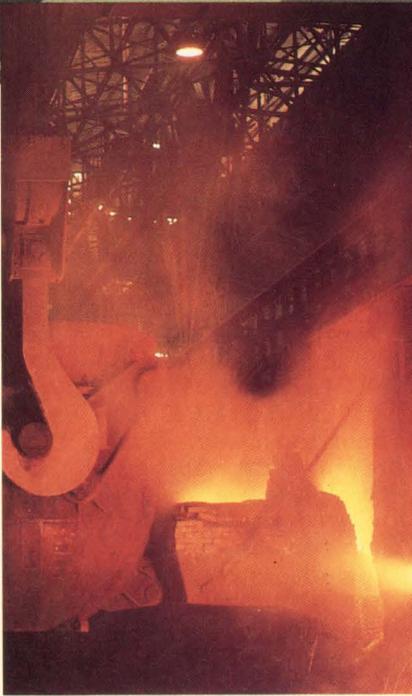
*Mentor Graphics' MCM station models the thermal characteristics of a multichip modules' devices and substrate by implementing a finite-element method to model 3-D heat transfer. The top half of this screen shows the finite-element analysis mesh, the bottom half the isotherm map of substrate temperature.*

a logical transition for Mentor, which tackled many of the design issues facing MCMs when it developed the hybrid design tool.

### ■ The MCM difference

Hybrids and MCMs are similar because they both house bare chips on a substrate, but there are differences in performance and in physical characteristics that must be considered in the design phase.

"There aren't precise definitions

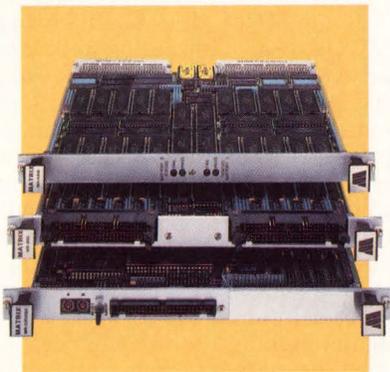


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the gridless vs. gridded debate, which has raged in the printed circuit board world for years. The debate heats up when the dense geometries of MCMs enter the fray.

Proponents of the gridded approach cite advances made in routing technology that let their tools stay flexible for the varying pitches of MCMs, while offering the advantages of interactive routing, which traditionally must be done with some sort of grid in the background. "Our router isn't gridless, but it can adapt to the pitches of the various devices," says John Isaac, advanced packaging product manager at Mentor Graphics. "We've overcome the

limitations associated with gridded routers in the past, which have the image of being inflexible. Many of these restrictions were addressed when the industry embraced surface mount devices and we had to adapt. Our router, for instance, doesn't demand that pads be on a grid. It routes on a grid and then can do a little jog over to the pad location, so it remains flexible."

**Simulation difficulties**

In spite of the host of tools available to designers of MCMs, there are still barriers to true behavioral simulation, mainly due to the lack of models for the mix of devices on a substrate. Silicon vendors are reluctant to re-

lease detailed models of their proprietary dies and EDA vendors generally don't want to get into the time-consuming and expensive business of writing them. Tool vendors do provide the software for users to create their own models, but this calls for close cooperation between the silicon vendor and the user. It also requires the user to have some modeling expertise.

Simulation, however, is a need that won't go away, mainly because it's the only way to avoid ending up

with an MCM that doesn't work. "MCMs pose simulation problems for everyone, but we have to solve the problem because traditional methods for debugging are inadequate," says Mentor's Isaac. "Many engineers have avoided total simulation of circuit boards by relying on breadboarding techniques, but that simply won't work with MCMs. After all, one of the principal driving forces behind MCMs is speed, which means making the interconnects as short as possible. You can't effectively simulate a 2-in.-square MCM with bare die on it by mapping it to a 10-in.-square breadboard with surface mount devices (SMDs),

through-hole devices and jumper wires. Simulation is the answer and for that you need accurate models."

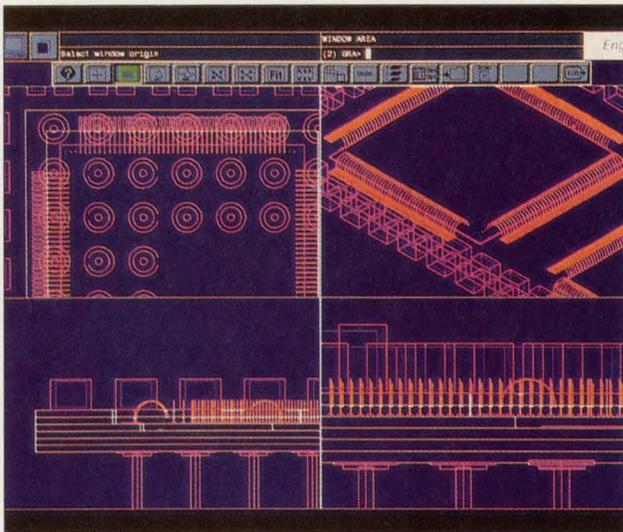
Undoubtedly, market pressure will force IC vendors to cooperate and provide these models, but until then, designers will have to use existing tools to predict as much of an MCM's behavior as possible.

If existing MCM tools have one thing in common it's this: they all require that substantial time be spent before a design is accepted, rejected or modified. As MCMs move into commercial applications, time-to-market pressures will make this leisurely design methodology unacceptable.

**Up the design cycle**

"If you go through placement and routing and run all kinds of thermal and signal integrity analysis, you've invested a great deal of time in a design," says Craig Palmer, manager in the systems division at Cadence Design Systems (San Jose, CA). "If anywhere along the line you find a major flaw in your design you have to start over, and that wastes a lot of time. We're taking the top-down approach and working on moving much of these analyses to the pre-layout phase of the design cycle. The people we're talking to want a way to simulate and analyze many of these physical and electrical effects at a high level, so they can proceed with their design using with a real set of design rules."

As printed circuit board technologies run out of gas, high speed, dense-I/O-count alternatives like MCMs will become a necessity. Finding ways to design, test and manufacture them will be one of the premier engineering challenges of the '90s. ■



Dazix has leveraged its CAD design expertise to integrate 3-D physical and thermal views of components into its multichip module (MCM) engineer tool. In addition to providing interference checking for pads, traces and vias, the tool can produce detailed shaded images for documentation.

limitations associated with gridded routers in the past, which have the image of being inflexible. Many of these restrictions were addressed when the industry embraced surface mount devices and we had to adapt. Our router, for instance, doesn't demand that pads be on a grid. It routes on a grid and then can do a little jog over to the pad location, so it remains flexible."

Critics of the gridded approach point out that grids can take large amounts of system memory to adequately model the multitude of points that an MCM's densely-packed nets necessitate. Gridded router advocates that say gridless

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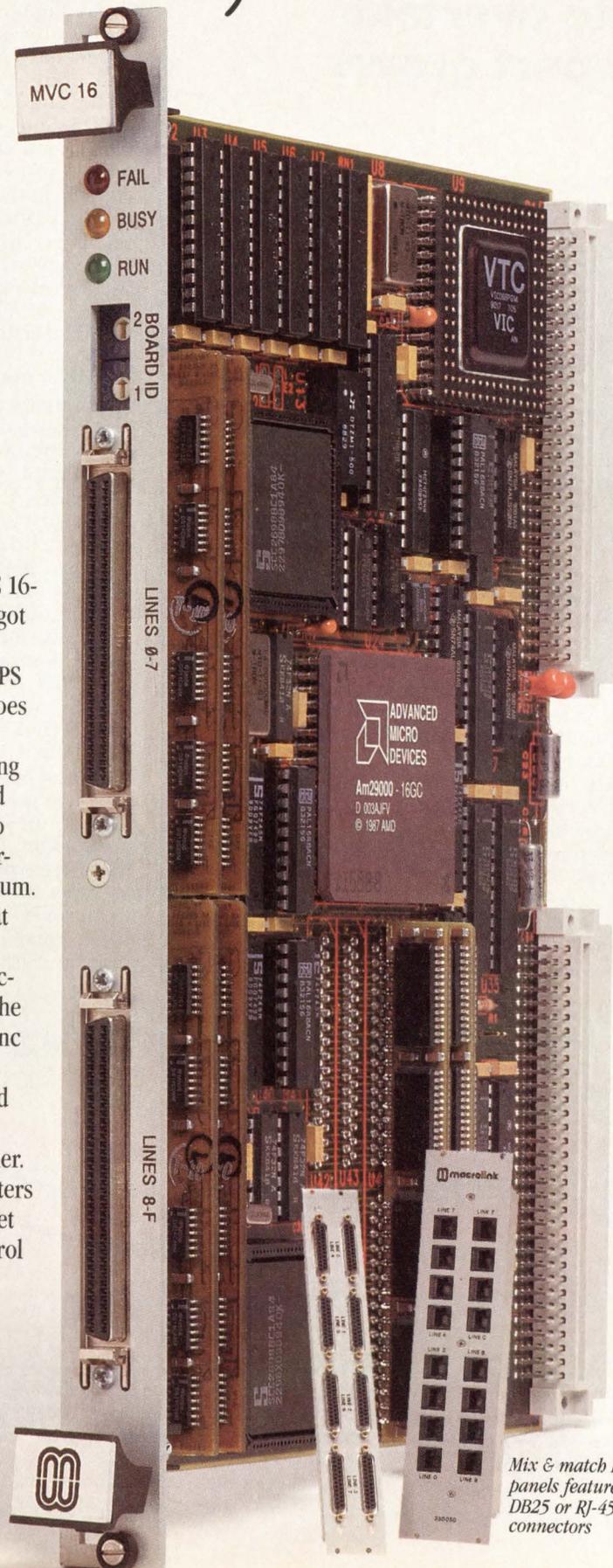
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## VHDL poised to overtake Verilog as support grows

Barbara Tuck, Senior Editor

So far, VHDL's user acceptance is still behind that of Verilog, which is perceived to be a de facto industry standard. Core issues such as the lack of tools and models, difficulties with tool interoperability and lack of verification compliance have hampered the acceptance of VHDL as the standard hardware description language worldwide.

Less than two months ago, a group of leading EDA and ASIC vendors formed VHDL International to advance VHDL as the standard for the design and description of electronic systems. The new organization has as founding members Compass Design Automation (San Jose, CA), LSI Logic (Milpitas, CA), Logic Automation (Beaverton, OR), Mentor Graphics (Wilsonville, OR), Synopsys (Mountain View, CA), VLSI Technology (San Jose, CA), Valid Logic Systems (San Jose, CA), Vantage Analysis Systems (Fremont, CA), and Viewlogic Systems (Marlboro, MA). Also endorsing VHDL International is the VHDL Users' Group which, as a subcommittee of the organization, is helping to define issues and recommend solutions.

The counterpart to VHDL International, Open Verilog International (OVI), established after Cadence Design Systems (San Jose, CA) opened the Verilog HDL to the public domain, is more user oriented than the VHDL group appeared to be at its inception. Yet the delicate balance Cadence has been striking between opening the language and hesitating to give away specifications to simulator clonemakers, has somewhat hampered the effectiveness of OVI. Though Cadence is a VHDL simulator supplier, it wasn't invited to be a founding member of VHDL International, no doubt because it's so

closely tied to Verilog. Nevertheless, Cadence says that if VHDL International's objectives are more user driven than they seem at first glance, and if the new organization takes on a more international perspective (to encompass Europe at least), then Cadence will accept a future invitation to join VHDL International at a high level. In the meantime, Cadence expects to strengthen its VHDL position with fourth-quarter shipments of its VHDL synthesis tool.

### Familiarity is comfortable

VHDL has had a tough time proving itself superior to designers already using Verilog, especially to those simulating with Verilog. Among backers of Verilog are large electronics manufacturers including Sun Microsystems, whose design groups are comfortable with Verilog and hesitant to suffer the productivity hits that would occur during a transition to VHDL. Very poor simulation performance at the gate level hasn't helped VHDL win over Verilog users. Neither has the scarcity of VHDL models increased the desirability of VHDL in the eyes of Verilog users (who now have all the models they need). Support for VHDL is, therefore, likely to come

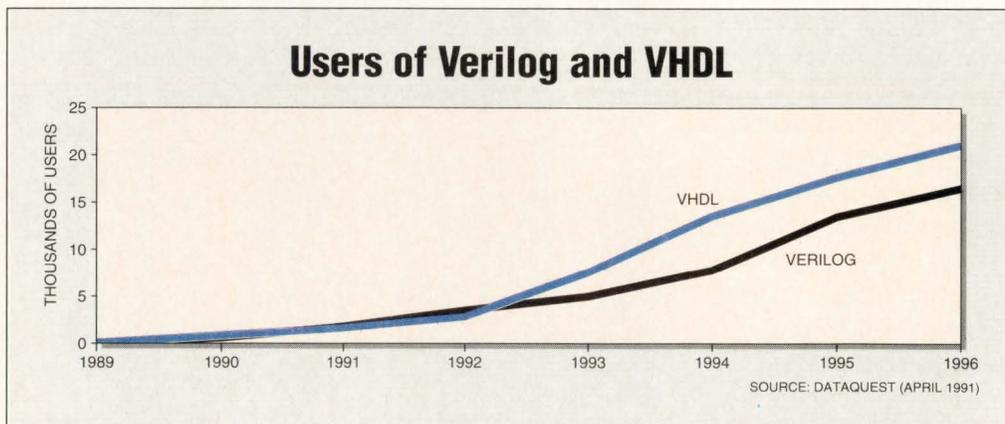
from users just adopting an HDL. But as shipments of VHDL tools pick up, it's also likely that even ardent Verilog backers, desiring to keep up with standards, will support both VHDL and Verilog simultaneously.

EDA and ASIC vendors backing VHDL as a standard have realized lately the need to do some standardizing of their own. Users have let vendors know that what they demand from VHDL is a commonality in approach, not a variety of products that either support different subsets of VHDL or interpret the VHDL specification differently.

### VHDL a matchmaker

The benefits of using a common language has led VHDL-simulator-vendor Vantage Analysis Systems (Fremont, CA) to create a Synthesis Associates' Program through which synthesis vendors and Vantage will cross-validate their respective software tools and thus make certain that a particular synthesis tool interprets VHDL consistently with the IEEE specification for the language. Vantage's intention is to ensure that a wide range of VHDL-based synthesis tools will produce results that match those of its VHDL simulator.

Dave Coelho, founder and executive vice president of Vantage says, "Designers require a coherent method of integrating all of the different synthesis tools with VHDL so they can simulate at the behavioral level, synthesize at the gate level, then recompile for resimulation, and be certain the tools work



The five-year projected growth rates for VHDL and Verilog HDL indicate that the number of VHDL users will surpass the number of Verilog HDL users in early 1992. Today's growth in VHDL use is credited to the availability of VHDL-based products from the major CAE vendors. (Source: Dataquest, April 1991)

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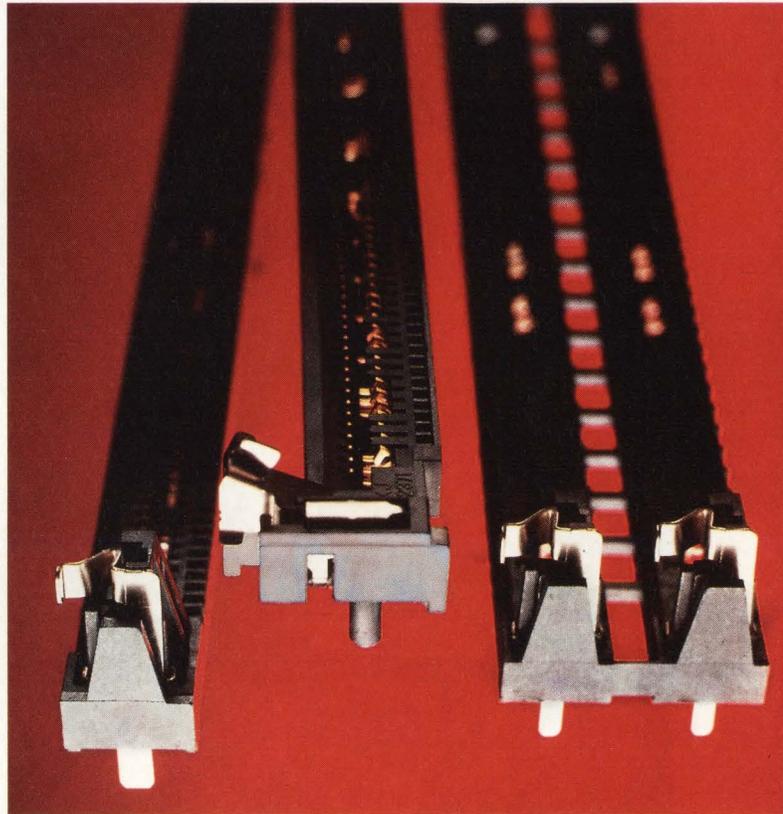
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together." Among VHDL synthesis vendors participating in the program are: Compass, which has released a VHDL-based version of its ASIC Synthesizer; Dassault Electronique (Saint-Cloud, France) which markets the VHDL-based Frenchip synthesizer; Exemplar

Logic (Berkeley, CA), which focuses on field programmable gate array (FPGA) synthesis through the use of architectural analysis in Release 1.0; LSI Logic, which offers the Vantage simulator, Synopsys synthesis, and proprietary synthesis as part of its Silicon 1076 VHDL design en-

vironment; Mentor Graphics, which expects to make its AutoLogic VHDL synthesis tool available to run on Release 7.0 next month and on the Falcon-Framework-based Release 8.0 in the fourth quarter; Racal-Redac (Westford, MA), which is shipping its VHDL synthesis with its ASIC Expert design system; and Teradyne (Boston, MA) which has signed an OEM agreement with Dassault to market Frenchip worldwide.

**A design dilemma**

Designers of FPGAs and complex programmable logic devices have been plagued with numerous proprietary languages and design tools, all sorely in need of a common thread to link them. Minc (Colorado Springs, CO) has finally shifted away from the exclusive use of its proprietary language and has entered into a relationship with CLSI Solutions (Rockville, MD), a leader in VHDL, to ease that dilemma. Minc is licensing CLSI's VHDL and plans to jointly develop a set of VHDL constructs for programmable-logic synthesis with CLSI. The goal is to give users a common set of design entry methods that spans all tools and methodologies. Minc plans to release a programmable-logic synthesis product within a few months that will accept design descriptions in VHDL and will also interface to back-end tools in VHDL.

Minc and CLSI will push for additional constructs to be added to the VHDL specification because VHDL was not written to be used as a synthesis language. More than three dozen EDA vendors and end users are rallying behind Minc and CLSI to support VHDL as the standard for programmable design, according to Minc.

Also joining the list of vendors interfacing design tools through VHDL are Ikos (Sunnyvale, CA) with Racal-Redac and Zycad (Menlo Park, CA) with Synopsys. Expected to ship in the fourth quarter, the Ikos VHDL accelerator combines Ikos' hardware-assisted mixed-level simulation technology with Racal-Redac's simulation, synthesis and object-oriented framework technologies. Ikos claims the VHDL accelerator simulates a design module with 1,000 lines of VHDL code 20 to 50 times faster than software simulators running on high-performance

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CIRCLE NO. 36

CAE/CAD TOOLS

workstations. A software/hardware mixed-level simulation environment that integrates the Synopsys VHDL System Simulator with Zycad's XP Simulation Accelerators went into beta site last month and is expected to ship in November. The combined technologies provide users with as much as 200x performance improvement in structural-level simulation of VHDL designs, according to Synopsys.

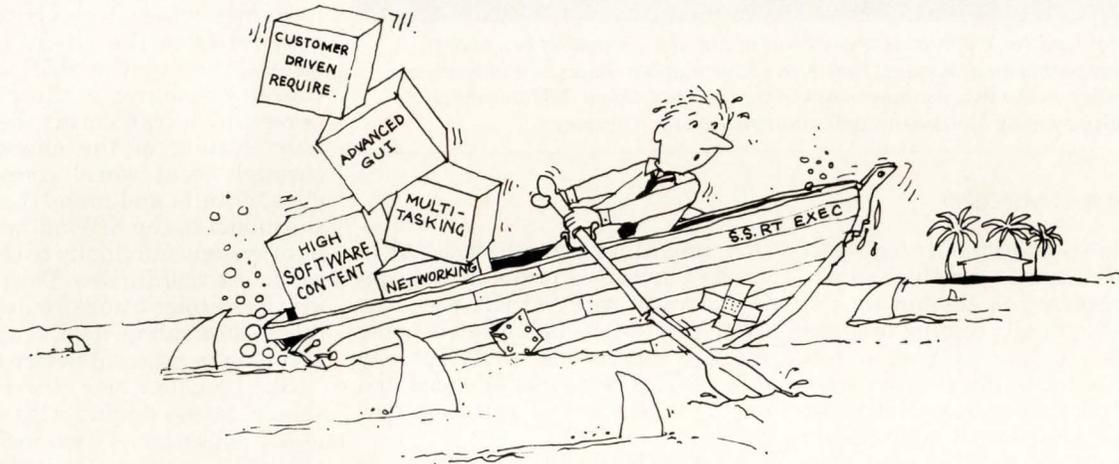
Also backing VHDL with a product that's about ready to ship is Valid Logic Systems. Valid has integrated VHDL language-entry capabilities and a VHDL simulator into its Logic Workbench TD top-down design environment. Built into the Valid design capture system for non-expert VHDL users are a VHDL language-sensitive editor, a check for conformance to a synthesizable subset, an integrated language analyzer, and the ability to automatically generate VHDL code from a schematic.

VHDL products may be shipping and vendor backing may be strong, but it will be some time before the new VHDL tools are production-proven. Verilog simulators will continue, at least for the short term, to be the trusted tools. The need to have the flexibility to use a variety of synthe-

sis tools will, perhaps more than any other factor, push users to adopt VHDL. For that reason, even die-hard Verilog users might find it beneficial to evaluate VHDL simulation and synthesis tools now and to participate in the resolution of VHDL modeling issues. ■

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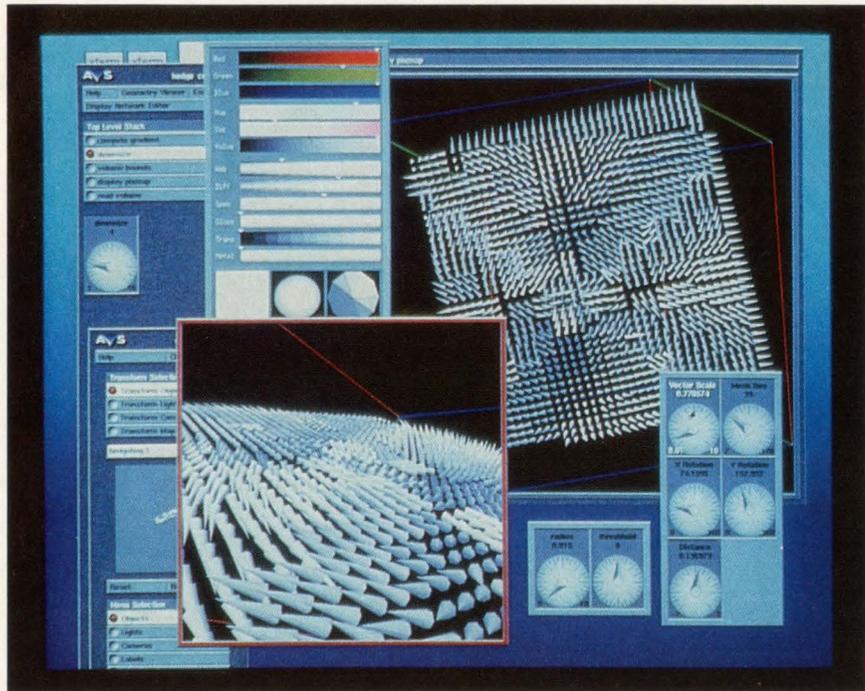
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## Protocol extensions bring 3-D to X Windows



The PEX protocols for X Windows allow distribution of 3-D graphics in a heterogeneous computing environment. They also allow multiple simultaneous views of data, as shown in the two window views of this computational fluid dynamics problem, displayed by Stardent's Application Visualization System.

Tom Williams, Senior Editor

The ability to distribute high-performance 3-D graphics in a heterogeneous computing environment is finally coming to users via the X Windows system. X has provided a basis for user-friendly graphical user interfaces (GUIs) that have made Unix-based applications accessible to a vast number of non-technical users, thus broadening the applications and market base of such systems. But, until PEX, X has lacked the ability to distribute 3-D objects around a heterogeneous environment.

### Defining PEX

PEX represents a set of extensions to the X protocols that provide the ability to distribute 3-D graphics objects in a heterogeneous environment. The term "PEX" is a bit confusing since it originally stood for Programmer's Hierarchical Interactive Graphics Standard (PHIGS) Extensions to X. PHIGS is an applica-

tion programming interface (API). An API invokes a protocol. The confusion arose because PHIGS was the first API to be implemented using the 3-D extensions to X. But any other 3-D API can be implemented on top of the set of protocols now referred to as PEX.

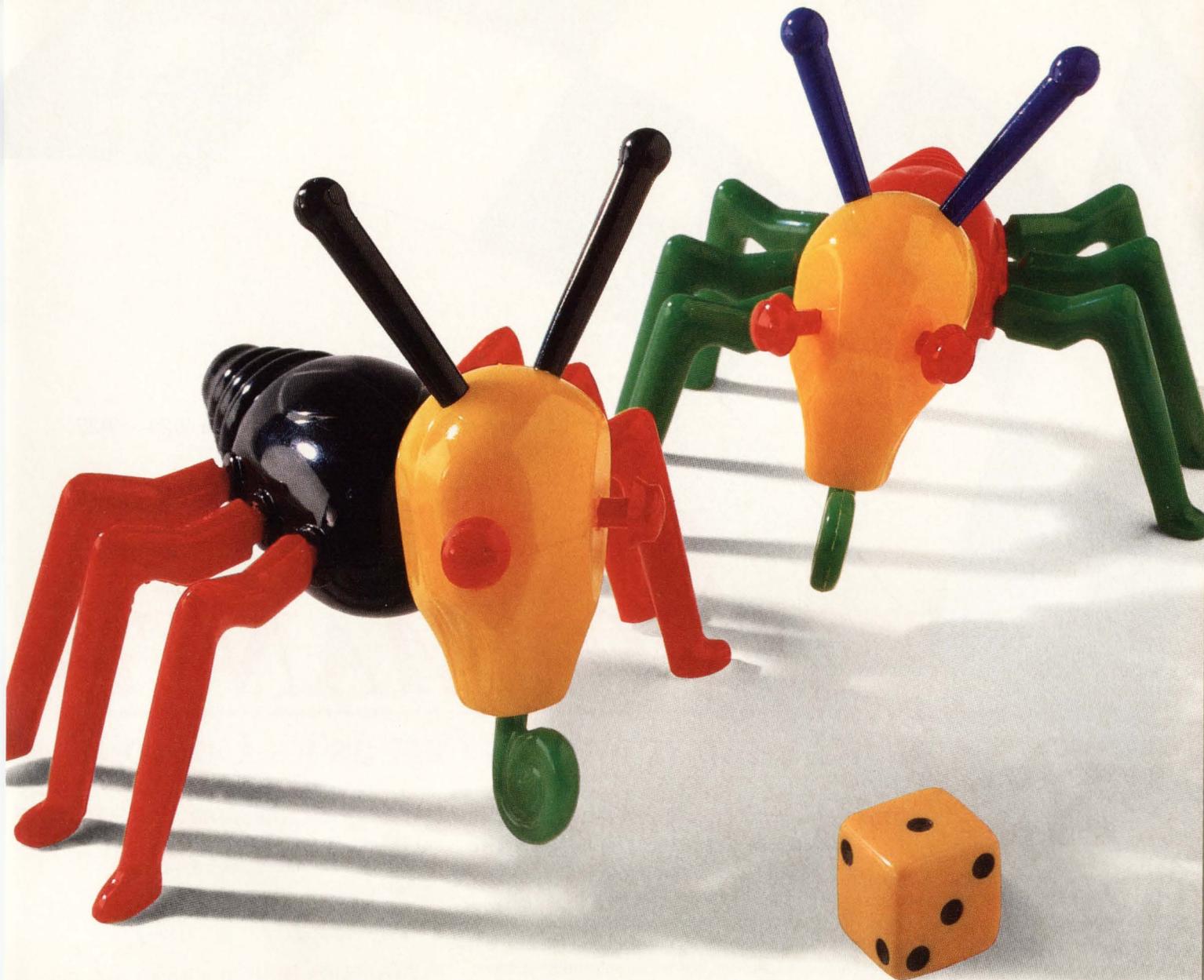
PEX is the result of the efforts of the PEX Interoperability Group, a group of 10 companies working with the blessings of the X Windows Consortium. The Companies include Sun Microsystems (Mountain View, CA), Hewlett-Packard (Palo Alto, CA), Digital Equipment Corp (Maynard, MA), Evans and Sutherland (Salt Lake City, UT), Convex Computer (Richardson, TX), IBM (Armonk, NY), Kubota (Sunnyvale, CA), ShoGraphics (Mountain View, CA), Stardent (Concord, MA), and Tektronix (Portland, OR). According to William Loesch, president of group member ShoGraphics, "Only

a protocol allows for interoperability. You can put any API you want on top of PEX."

The definition of a protocol, then, leaves vendors with wide ranges of options as to their individual implementations. One of the members of the group, Sun Microsystems, was chartered to create a sample implementation to demonstrate both the client and server side of handling the protocols. The sample implementation incorporates both the existing X Windows system, the PEX extensions and Stardent's Application Visualization System (AVS), a user application. Companies that are going to provide products will make decisions on which parts of an implementation they will optimize for specific price/performance goals.

PEX follows the client/server model of the X Windows system. On the server side is a layer of device-independent protocol handlers which interface to the hardware via a relatively large layer of device-dependent code. The core X protocol handler has the intelligence to recognize when it receives a PEX protocol from the client side and passes that to the PEX handler. One key resource is the PEX renderer which transforms the coordinate system of the client model through local world coordinates, clips, orients and maps the view of the model to the X Windows coordinate system and finally to the physical device coordinates. The renderer also has a color transformation pipeline to do shading, depth cueing and mapping to physical device colors.

On the client side, there can be several layers ending with the end-user application. These include the xlib calls, perhaps a toolkit with widgets such as scroll bars, menus, etc., and a GUI such as Open Software Foundation/Motif or Open Look. Finally, of course, there's the end-user application which sees none of this except the programming interface to the GUI or the API of the 3-D graphics system. In the case of the PHIGS implementation, there's an API to which an application makes calls. The API then generates the protocols that are sent across the network or backplane to the client. The client essentially performs the rendering of the commands sent by the server.

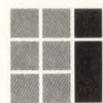


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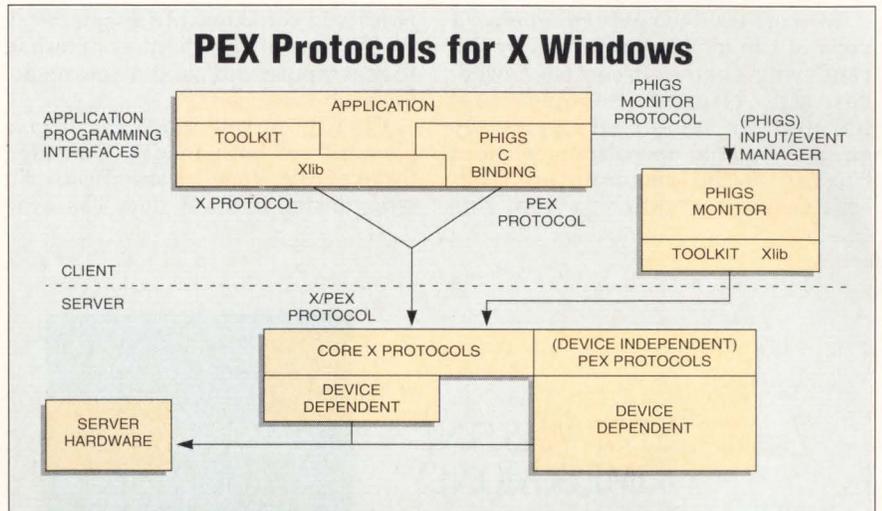
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One of the major differences between PEX and X is that where X is limited to a set of 2-D integer screen coordinates, PEX supports the creation and transmission of 3-D floating-point coordinates. PEX has wisely dealt with a problem that has long been an issue in 3-D graphics: the question of retained structure or immediate mode. PEX supports both retained-structure and immediate modes and a mixture of the two.

In the immediate mode, the compute engine may mathematically define a model of some object, such as an airplane wing, in terms of lines, surfaces, lighting models, etc., along with non-displayed data such as strength, weight and thermal characteristics. It would then send the displayable parts of that model to be rendered and displayed in a 3-D floating-point coordinate system to the rendering portion of the graphics pipeline.



The PEX sample implementation uses a PHIG's API as an example of how a 3-D X Windows system can be implemented. The API includes interfaces to PHIGS C bindings, toolkit and xlib which generate machine-independent protocols to send over the network or system backplane. The PHIGS monitor manages PHIGS-specific input and events and is specific to a PHIGS implementation. Protocols are received by the Core X server and executed as X functions or passed to the PEX portion where they are routed to the machine-dependent portion and executed.

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In retained-structure mode, a view of the model is retained by the rendering engine. It can be viewed, rotated, clipped, zoomed, and panned by means of relatively simple matrix operations without having to be recomputed from scratch for every different view. This

results in considerably less network traffic than if the client system had to recompute and send a new model for each view.

Finally, mixed mode may have elements of both modes. Consider, for example, viewing the effects of a wing design in an airflow. The wing

itself doesn't change, but the view might, and would use retained-structure mode. Changing the angle of attack changes the airflow, requiring recomputation for each frame and hence operation in the immediate mode.

ShoGraphic's Loesch stresses that PEX is designed to be flexible from both the hardware and software aspects. It's not tied to any specific rendering algorithms so that even within a server implementation, the vendor can be creative in firmware as well as hardware. Because of format conversions, rounding errors, etc., however, PEX images cannot be "pixel perfect," in that each image on a server will be exactly that generated by the client. Variations in screen resolution, depth of frame buffers, etc., will see to that.

PEX will also be extensible. As proposals for upgrades are presented to the X Consortium, they can be voted on and approved and included in future releases in an orderly way. The current version of PEX will be available this fall on the latest release tape X11R5 from the MIT X Consortium (Cambridge, MA).

It's hoped that PEX will bring to mechanical engineering the kinds of productivity gains that are starting to show up in disciplines where 2-D often is sufficient, such as EDA. ■

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CIRCLE NO. 50

# New bus and transceiver technologies aim to unlock high-end system performance

Warren Andrews, Senior Editor

**S**un Microsystems (Mountain View, CA), working in conjunction with the Xerox PARC (Palo Alto, CA), is reportedly about to release a new bus—and new transceiver logic to the market. The new bus is DynaBus—a synchronous, packet-switched bus designed to meet all the needs of a high-performance, shared-memory multiprocessor system. The new transceiver logic, GTL (Gunner transceiver logic, named after developer William Gunner), is a low-threshold-voltage switching design using differential drivers to implement high-performance transceivers that can be incorporated into larger VLSI devices—such as bus interface ICs. GTL is reported to be designed for use on backplanes and for chip-to-chip busing. LSI Logic (Milpitas, CA) has been working with Xerox in the development of the logic. The new transceivers operate in the 1- to 2-V range and use differential inputs and outputs. According to sources, LSI has had GTL standard cells in its library for almost a year.

## ■ Multichip Sparc modules

The entire project is being conducted quietly under the code name SunDragon, but additional participants are being mentioned. Texas Instruments (Dallas, TX) apparently has a CPU project under development which is code-named Viking. Considering TI's decision to become a Sparc supplier, Sun's decision not to use Fujitsu's next-generation processor Sparc H (whose development was subsequently cancelled), and the two names appearing together in a document about a next-generation workstation implies that TI will become a major Sun supplier.

Viking is only one of at least three CPU projects underway. All three CPU projects are Sparc-based multichip modules (MCMs). They all use MCM technology to achieve the desired levels of density and per-

formance. LSI Logic has code-named its project Lightning, while Ross Technologies (Austin, TX) is working on a project called Pinnacle. Little is known of the projects except that they include at least one Sparc processor, a cache controller, some amount of high-speed SRAM cache and perhaps a floating-point or vector processor.

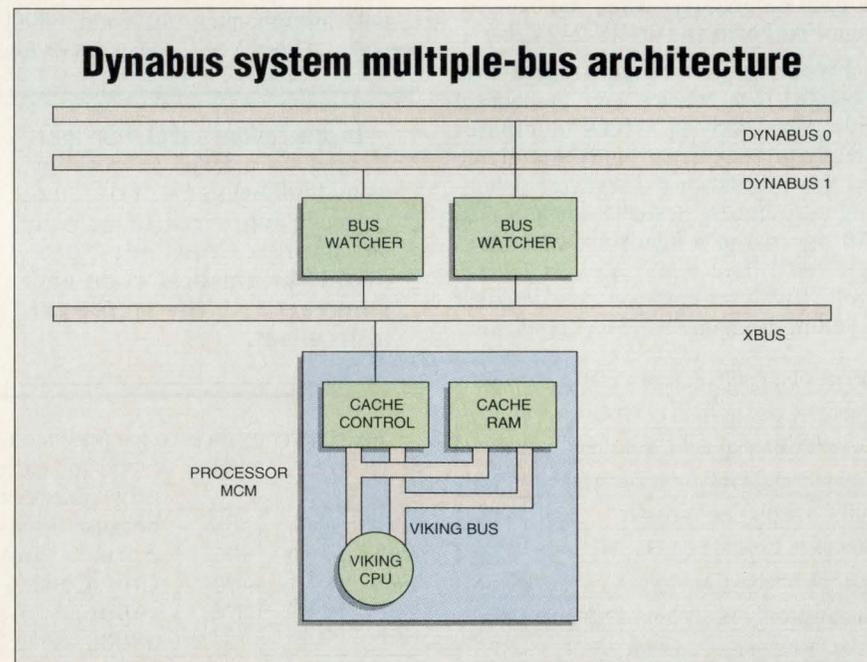
At this writing, the only hardware seen has been a silicon-on-silicon MCM assembled by nChip. The MCM comprises a processor, floating-point unit, two SRAMs, and a cache controller on a silicon substrate approximately one in. square. The whole thing is packaged in a large pin-grid array.

The MCM TI seems to be putting together (though it won't discuss the project—or even admit to its existence) comprises a processor, SRAM cache memory, and a cache controller interconnected with what TI refers to as its Viking Bus. There's no indication yet that the module contains either a floating-point unit or vector processor.

## ■ Single-chip interface and control

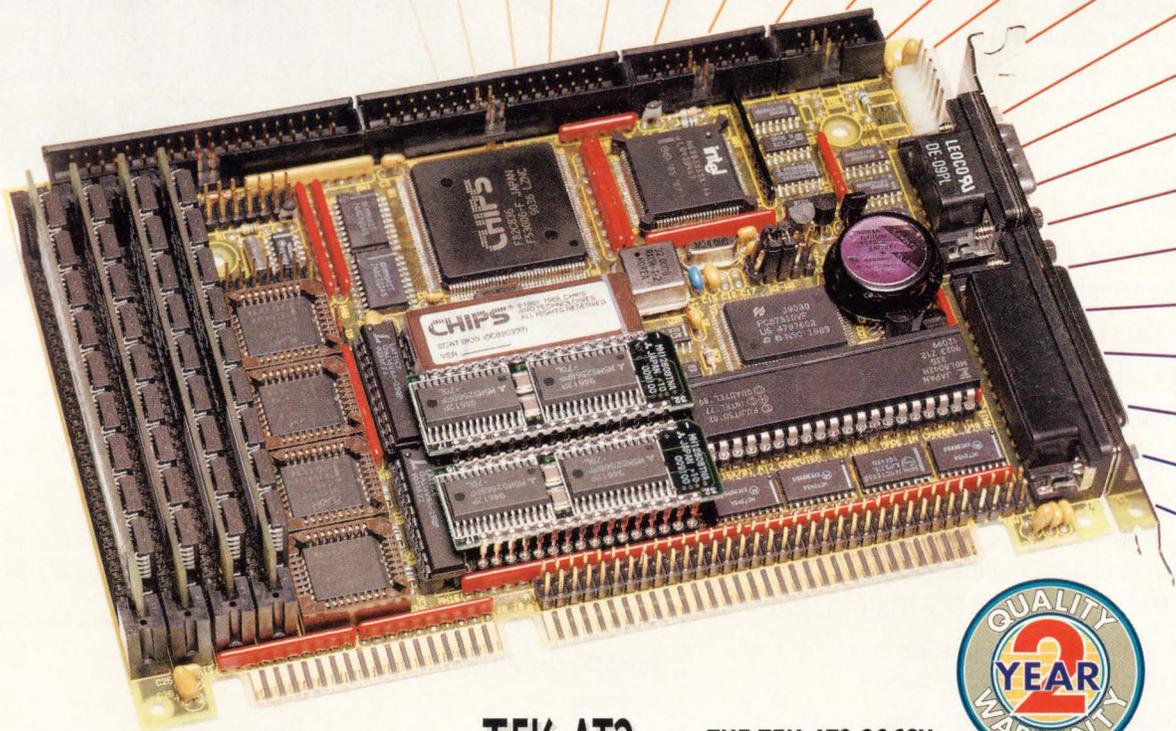
According to sources, the idea behind the physical structure and protocol of DynaBus is to allow direct interconnection of complex subsystems—everything from memory and graphic controllers to network and external bus controllers—with a single VLSI device type. A key element in the DynaBus strategy is to provide a power-stingy transceiver circuit so that all bus-interface and control functions can reside on a single chip.

Existing transceiver technology—including high-current TTL and even BTL (backplane transceiver logic)—dissipate enough power to



*The heart of the rumored new SunDragon computer is a hierarchy of high-performance buses based on new bus transceiver logic, GTL. The system bus, Dynabus, has a data-transfer capacity in the range of several hundred Mbytes/s. The processor technology depends on multichip modules comprising a Sparc-based processor, cache memory and a cache controller. All chips in the modules are connected through a GTL-based chip-interconnect bus called Viking Bus. Modules are interconnected through XBus, which is tied to Dynabus through bus-watcher interface circuitry. Multiple Dynabuses can be connected to the XBus and treated as separate logical entities, or as a single logical bus with separate electrical connections.*

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require that transceivers be packaged separately from control circuitry. In BTL implementations, for example, only six—or at most eight—transceivers can be put in a single package. Using a low-power transceiver technology, it may be possible to package 32—or even 64—transceivers in a single VLSI chip along with other interface and control circuitry.

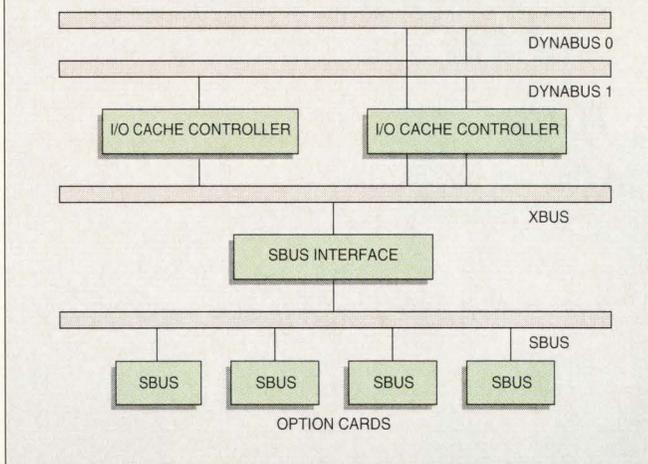
It's possible to configure DynaBus—or multiple DynaBuses—in a variety of ways. Depending on how they are interconnected, DynaBuses can be configured so that one logical bus can include multiple physical segments (separate backplanes, for example), or so that there are multiple buses that are totally independent.

**Bus Performance**

The bus provides a usable bandwidth in the range of several hundreds of megabytes per second, giving rise to speculation that it can be used on a broad range of machines—from high-performance computational servers to desktop workstations. One of the distinguishing features of DynaBus is that a conceptually-simple cache model is used to guarantee that each processor sees a consistent view of memory, one that reflects all caching and I/O transactions. The hardware ensures that multiple copies of read/write data in caches are consistent and that both input and output devices are able to access cached data.

According to sources, DynaBus comprises 88 signal lines, 64 of which are multiplexed data-and-address lines, the balance comprise control, arbitration, parity and clock signals. In operation, a requesting bus node must get DynaBus mastership from the arbiter before it puts its request packet on the bus. A transaction is completed when bus mastership is assumed by the bus node answering the request. The new master sends a reply packet to the requesting node. According to preliminary information, request and reply packets may be separated by an arbitrary number of cycles, during which time the bus is free to handle other traffic—provided a pre-defined timeout period has not been reached. Packet transmission, once begun, is uninterruptible (no other device can take the bus away during this time, regardless of priority).

**Typical Dynabus I/O configuration**



*The Dynabus system architecture provides connection to I/O through the XBus intermediate-level bus. Dedicated I/O cache controllers simplify I/O control and let common I/O serve the needs of multiple Dynabus systems. In this case, SBUS is shown as the system I/O bus.*

Also according to preliminary information, DynaBus defines a variety of transactions handling data transfer between caches and memory, data consistency, synchronization, input/output, interrupts,

and address mapping. Not unlike part of the Futurebus+ protocol, each transaction type is defined in the header information which precedes a transaction.

It appears the bus' transfer

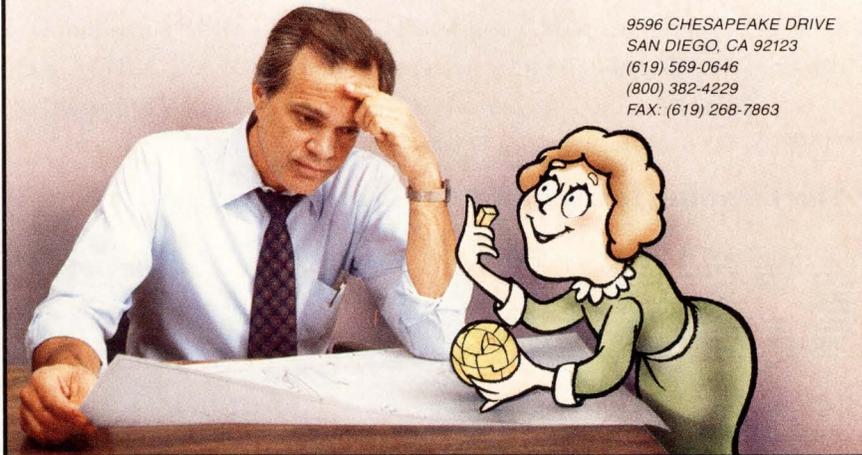
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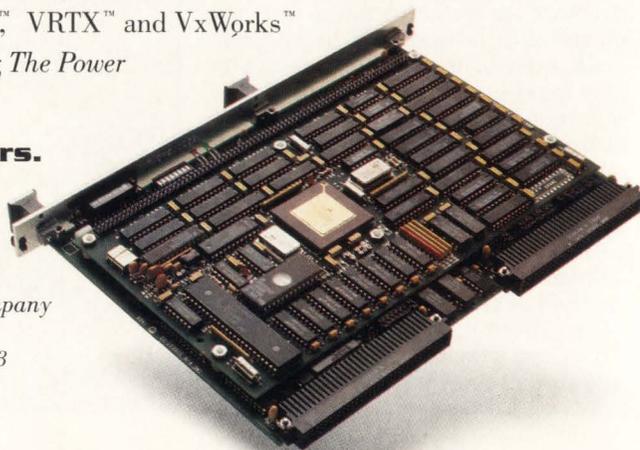


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**CIRCLE NO. 46**

mechanism is relatively efficient, with claims made to indicate data-transfer efficiency as high as 73 percent. An early overview document claims that the efficiency rating, "derives from the fact that eight of the 11 (clock) cycles of block-transfer transactions carry data."

**The XBus**

One of the keys to Sun's new architecture is silicon. At the processor module level, the interchip bus (Viking bus) handles the chips comprising the CPU/cache assembly. The advantage of the interchip bus is that it permits a standard silicon interface for all chips so that components can be changed independently; changing one component won't require changes to other components due to interface differences.

Modules are interconnected via XBus, which appears to be an intermediate bus with many of the same characteristics as DynaBus. XBus connects through bus-watching circuitry (snooping) to DynaBus and also serves to connect DynaBus systems to I/O. DynaBus connects through an I/O cache chip to XBus, which then connects to some I/O bus interface.

Using a hierarchy of buses allows the critical interchip bus to remain small and operate at higher frequencies than the backplane bus. Additional flexibility comes from the cache function being distributed to two chips—the module's cache controller and the XBus bus-watcher or snooper chips. Distributed cache control also lets larger caches than those provided by the processor MCM be implemented because it permits off-module cache memory to be accessed via XBus.

**Silicon Solutions**

Because of its tight timing parameters, XBus virtually demands an ASIC implementation. Standard logic, say the specification's authors, would require too complex a circuit board, imposing excessive on/off-chip delays and delays from long circuit board traces.

Similarly, it's expected that DynaBus will use monolithic interface and transceiver circuitry. Faster, lower-power logic has been an elusive "holy grail" of system architects for years. The use of GTL logic—or some variant thereof—may provide

some of the solution. If the technology proves out, it will undoubtedly be applied to other bus approaches, such as a GTL Futurebus+ profile. But the use of differential drivers poses its own problem because they require twice the pins of single-ended drivers. Doubling the number of signal pins may result in significant problems at the board and chip level.

It's been reported that there has already been some lobbying effort to modify the DynaBus logical protocol to match that of Futurebus+, leaving the physical and electrical implementation the same. The more likely scenario is that Sun will follow the same scheme it did with Sparc and SBus. Watch for Sun to start off with a proprietary approach, then just before—or simultaneous with—the emergence of competition, release the specification to the public domain. This would provide Sun with a proprietary hold on the technology at the onset, and a year-or-so lead time

once it opened up the specification.

According to some sources close to the project, some product based on the technology may be surfacing soon—late this year or early next. The first products likely to be using the technology are high-performance servers—a product area where Sun has recently been lagging. It's not unlikely, however, that the technology may surface in other product areas from large, massively parallel systems and servers to powerful desktop workstations. ■

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# Software tools integrate the management of complex design projects

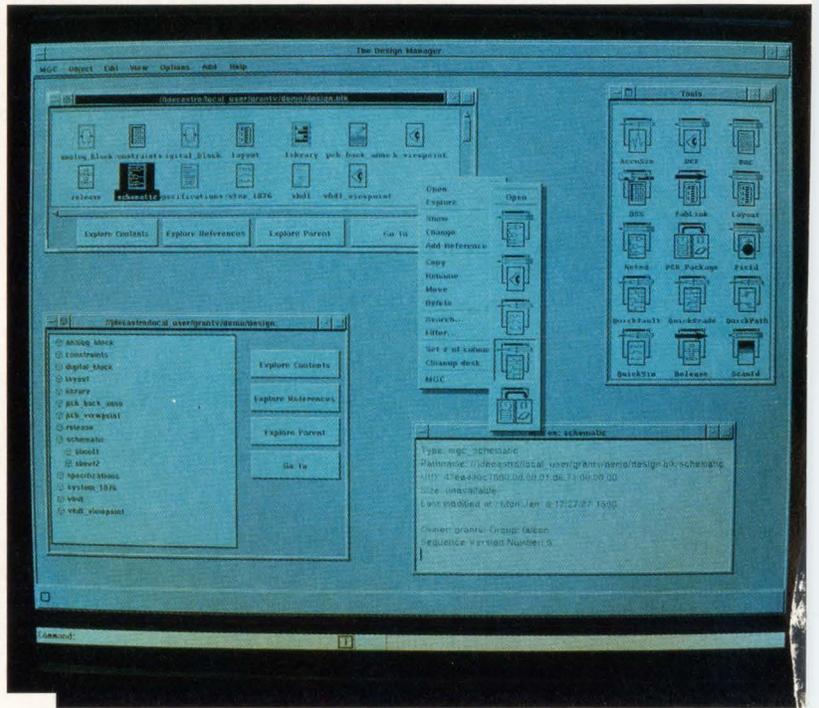
*Today's complex design projects demand more than just engineering tools. They also demand automated ways of coordinating teams and tracking projects to produce a concurrent engineering environment.*

Tom Williams  
Senior Editor

**S**imple tools are only as good as the hands that hold them and the eyes that guide them. The complex tools used today in support of design projects are similarly limited by the guiding vision of their users. No matter how advanced the tools at hand are, using them without an overview of their ultimate purpose doesn't help much. This is especially true when the goal of an organization is to achieve concurrent engineering of products that are developed by different teams of designers working on electrical, mechanical and software design simultaneously. Then the goal is to orchestrate the entire development process from initial concept to release to manufacturing, and even beyond to include product support and modifications.

Much emphasis has been placed on providing engineers with proper sets of tools and tool environments, such as the frameworks in CASE and in EDA, to aid individual productivity and to promote concurrent engineering. While such frameworks are indispensable, they must also include facilities for tracking and managing the design activities of individuals, work groups, and an entire organization. Design management is being addressed by such vendors as Digital Equipment Corp (Maynard, MA) with its VAX/VMS-based Electronic Data Control System (EDCS), and Intergraph/Dazix (Huntsville, AB) with its Simultaneous Engineering Environment (SEE) for Intergraph workstations.

But beyond bundled design-management systems oriented to a single vendor's hardware platform or environment, independent vendors are offering systems to help managers control and coordinate the activities of engineers and their tools. These product information management (PIM) systems—also called product data management (PDA) systems—are aimed at concurrent engineering. Some were initially conceived as general, enterprise-wide engineering-management tools while others began in one area of specialization and are now being tailored to play in an enterprise-wide



*Large design projects require automated help to manage their complexity. The Mentor Graphics Design Management Environment (DME) is an example of a graphical view into project status that allows management to set policies on access and work flow.*

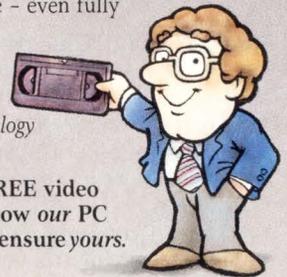
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## SOFTWARE TOOLS

data-management environment. Vendors of these systems include Atherton Technology (Sunnyvale, CA), Sherpa (Sunnyvale, CA), Mentor Graphics (Wilsonville, OR) and TeamOne Systems (Sunnyvale, CA).

### Dealing with human issues

Engineering may deal with hard technology, but engineering management deals with people and their foibles. In setting up a design operation, according to Atherton Technology's president Nick Copping, "Most people go straight to the hard technology and string all these tools together—editors, compilers, debuggers, etc. and say 'do it.' But

first time. They want to control information between groups, they want change control, they want to minimize resources and they want visibility into the project." Engineers, on the other hand, want to be left alone and they want an environment where they can get the job done. The two interests need not be mutually exclusive, computer aided tools can advance both of them.

### Managing complexity

The three most-important elements that engineering-management systems have in common are sharing of information among individuals and

controls user access to the design database based on policies defined by management. It also tracks versions, configurations and revisions to design files and alerts appropriate users of changes. The PIM also lets managers track the status of a project and set policies and procedures and program them into the project database.

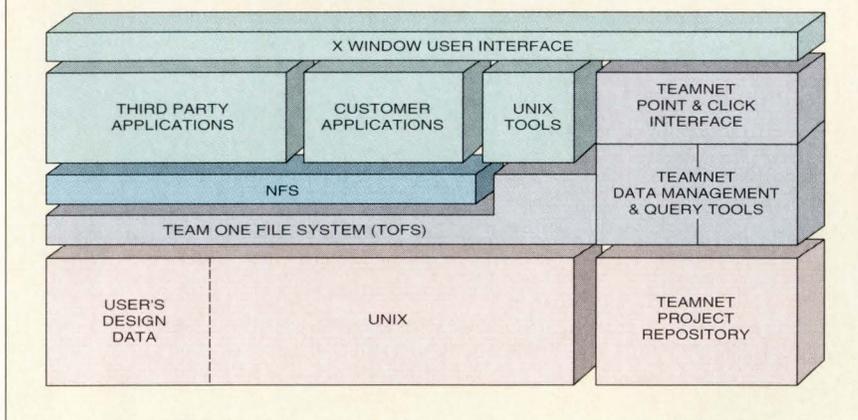
For example, the Sherpa Data Management System (DMS) has implemented the concept of a file vault from which designers can check out files, modify them and check them back in. The vault is not necessarily a physical place but is, as marketing director Stephen Wong puts it, "a kind of document police." The actual design files can reside on any node (or on multiple nodes) of the system; the PIM merely monitors activity on the system and controls access according to the defined policy. The "vault" is actually this enforcement procedure, which restricts a user's access if his or her actions don't conform to defined policy.

For example, if a designer wants to check out a design, the PIM first looks at his or her access privileges. If authorized, files can be checked out and copied to a workstation. While that file is checked out, all other users are blocked from checking out the same file for modifications, although they can read it. When the user wants to check the file back into the vault, he or she must meet certain requirements. These could be requirements to run certain tests, enter certain information in a header file, or get a supervisor's sign-off or approval, according to the company's policy.

"Everything is configurable," says Sherpa's Wong, "We don't want to tell you how many steps you need, who's to sign off or any of that." A package called Formview that comes with the system lets managers create screens that may either gently prompt a user (e.g., "Run build before check-in.") or present extensive project status information. For the most part, engineers don't want to know that a PIM is running in the background except for such policy prompts.

TeamOne has taken a somewhat more flexible approach than the vault concept to file access/revision control. Instead of copying files physically to a user's workstation, the TeamNet system creates a local work space and a "virtual copy" of the file that has been checked out.

## Teamnet product information management system



The TeamNet system by TeamOne intercepts file requests made over the network file system (NFS) and tracks them through its project repository, an object-oriented database that maintains audit and access information on a project. The management and query tools let management define policies for design updates, check-in/check-out procedures and monitor and control all activities associated with use of the design data.

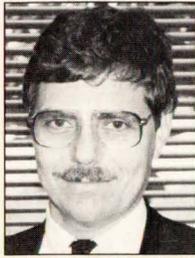
they're just building the wrong thing faster." While frameworks are mostly aimed at coordinating communication between tools and their data, management systems need to control and track the process—and they must do it without stepping on the toes of the engineers.

"There's a cultural consideration," says Copping, "in the way people see themselves doing their work and getting rewarded for it. So the mix of management issues ends up including policies, procedures, ethos, etc." David Hoffman, president of TeamOne Systems, notes that a management system must satisfy the concerns of both managers and engineers. "From the manager's perspective, they want to do it right the

groups, control of access to information, and workflow management. Workflow management includes version control, configuration control, methods of implementing data sharing and coordinating approval cycles for different phases of a product's development cycle. In short, it's the ability to define and enforce an organization's policies and procedures.

PIM systems, such as Sherpa's and TeamOne's, maintain a project database (also called a data repository), separate from the design database, which contains all the information about the organization's defined policies and procedures and all the audit trails of user activity on the networked system. The PIM con-

## How to implement CASE to support project team needs



**C**ASE has great potential to speed the software development process, and to ease the traditional bottlenecks of documentation and maintenance. Many

early CASE adopters, however, have been disappointed by tools and environments that just didn't perform in the "real world." A central problem is that the adoption of CASE was looked upon as a revolutionary concept. Most early CASE implementations grasped for the grail of a complete CASE environment from the start. As with the early engineering-design-oriented CAE frameworks, too much change had to take place and the support structure behind the tools had not been adequately developed.

In reality, adoption of CASE environments will be an evolutionary phenomenon. It must build upon practices and tools already in existence and allow groups to incrementally adopt improved design methodologies.

### ■ Building development strategies

The crux of any development strategy today is time-to-market. Each team wants to take advantage of the best tools available to meet project needs. The team needs to be productive and efficient. Team members need to know that they will be able to easily find and fix errors. They don't have time to install and learn an entirely new methodology. New tools need to be easy to use and adopt, complementing, rather than impeding, work in progress.

In implementing an effective CASE environment, one must focus on the relationship between the manager and the designer. The manager is looking for tools that improve time-to-market, improve individual productivity, track change, eliminate unnecessary resources, and control the work flow between design groups.

Designers, on the other hand, must be able to set up a work environment

easily, be assured of a stable environment in which to work, and manage a proliferation of data and complexity in the product design. They need an environment with nonintrusive program management, flexibility, and high performance. They need an integrated environment with the capability to freely mix and match tools, and they need easy-to-learn design-management products that also provide for ease in debugging and testing.

### ■ CASE considerations

To meet the needs of both of these groups, several criteria, based on the work by the CAD Framework Initiative, must be considered in designing or choosing a CASE environment.

First, does it facilitate large projects where many developers are working together in parallel? The sophisticated software being developed today requires the cooperative efforts of a team. It's no longer an individual activity, and as the team grows, the communication lines among team members—and team workgroups—become increasingly complex. The environment must facilitate group communications and allow groups to work concurrently, focused on reducing time-to-market.

Does it provide for cost-effective, efficient, seamless incorporation of the users' choice of tools into the environment? A project group isn't a static environment. It will require different tools, from different vendors, at different times. If the CASE environment is restrictive, or it makes the incorporation of new tools difficult and time-consuming, it doesn't support the team's requirement for facilitating a short development cycle.

Does it support the management, sharing, reuse and exchange of information, without negatively impacting the work of the group? Different elements of the project team have different requirements for information. Managers must be able to easily access information on team progress and performance. At the same time, the design group needs access to group data and ways of sharing information that don't sig-

nificantly increase development overhead.

Does it allow tool and environment portability across multiple platforms? Most projects today consist of one or more networked workgroups. These workgroups tend to collect a variety of hardware platforms. Single-vendor shops are becoming increasingly rare. To efficiently communicate, the design group's CASE environment must provide seamless access across heterogeneous environments. Standards are important in fulfilling this need. UNIX is already recognized as an important operating system for CASE tools and environments because of its availability on a broad number of platforms. Interoperability standards such as Sun's network file system (NFS) make it easy to pass information across a large number of platforms, transparently to the user, without the need for extensive application-specific coding.

Does it provide the means to incorporate a consistent user interface? The Macintosh phenomena proved that consistent user interfaces facilitated rapid acceptance and easy utilization of new tools. X-Windows, Microsoft Windows, and Sun's Open Look are all interface mechanisms that are facilitating consistent user interfaces.

Finally, does the CASE environment have the flexibility to extend easily to meet future needs of the group? An investment in a CASE environment isn't trivial, even if the implementation mechanism is evolutionary. Environments need to be technology independent, design methodology independent and able to scale with project complexity to justify the investment.

CASE offers project groups the opportunity to develop systems more quickly and more effectively, but, like any other technology, it must be harnessed to serve developers, and not become the master to which project teams must conform. Careful evaluation of the power, flexibility, modularity, and scalability of CASE environments prior to implementation is crucial to getting the most out of a CASE investment.

David M. Hoffman, President, TeamOne Systems

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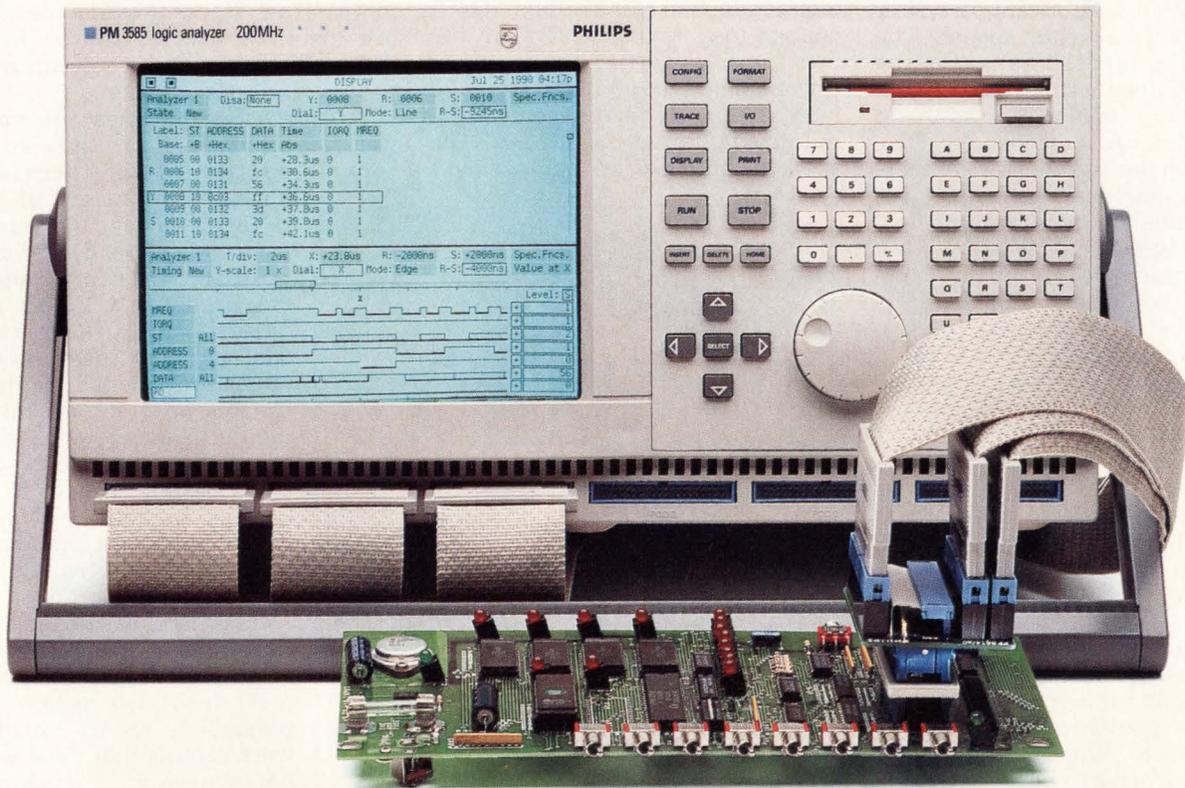
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CIRCLE NO. 48

## SOFTWARE TOOLS

Changes made by the user during a session are stored in the local workspace with pointers to the baseline file. When the file is checked back in, after necessary approval and sign-offs, the changes are incorporated into the baseline to create a new version baseline (all previous baseline versions are retained).

TeamOne supports two different check-out models: a single-writer and a multiple-writer model. The single-writer model, like the Sherpa system, blocks other users from modifying a file that has been checked out by someone else. The multiple-writer model, however, lets more than one user check out and modify the same file at the same time. The system has automated facilities to detect and help resolve conflicts between two people's versions of the same file when they try to check them in. Says TeamOne's Hoffman, "In a concurrent engineering environment people have to branch out to do their own jobs, but they also need something to help them integrate their changes."

When a file under the multiple-writer model is checked back in, it goes to a merge-resolution, or holding area. When the next person tries to check in his or her version of the file, the system will try to merge the two. If merge conflicts are detected, the system will notify the user that potential conflicts exist and the files will have to be inspected. When the user is satisfied that conflicts have been resolved, he or she can sign off and the file(s) go to a sign-off area. There, a project leader can inspect the resolutions, see who did what and discuss it with everyone concerned before finally signing off the new baseline version.

A supervisor would, like the engineers in the group, be working within the established policy programmed into the system. Criteria for signing off on a design may be a check list of requirements and the system will tell the manager if they have been met or not. For example, have certain tests been run, information logged, were there zero com-

pilation errors, etc.? The supervisor would not be able to promote the design to the next level until "yes" was answered to all the items on the list.

### Configuring the work culture

As a project progresses, people's roles change and at any given time, some users can have several different roles. A design is more than just a collection of individual files. A change to a schematic file can impact the board layout, the documentation, the bill of materials and more, perhaps even the actions of a purchasing agent in Taiwan. The product information management

connect all client workstations with the PIM environment. Network communications keep users up-to-date on project changes made by other users. If a software developer, for example, checks out a file and makes changes, the documentation person can know that the file is being worked on. When the new software version is signed off and promoted, the documentation people are instantly notified that a new version exists so that they can update their documentation.

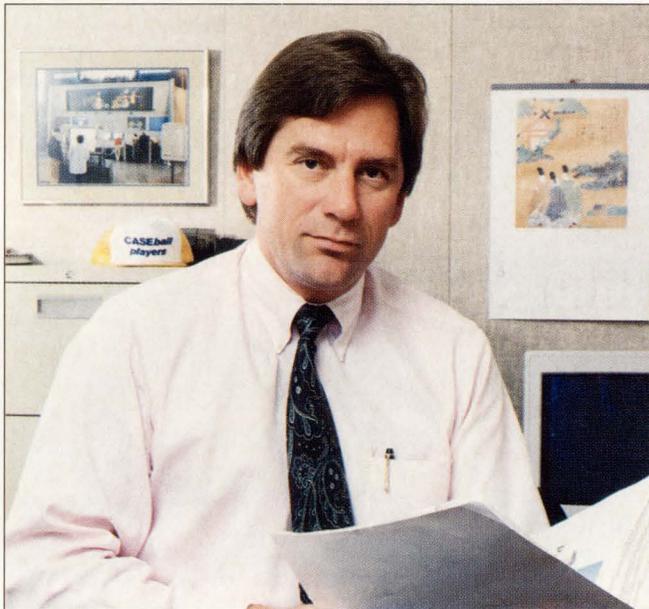
Similarly, Sherpa uses the network EMail facility to notify concerned parties of engineering changes. Notice of a change, such as a switch from round-head to flat-head screws, can be sent via predefined EMail to "alert" manufacturing (change screw inserters or other equipment), to purchasing people (start buying flathead screws as of a certain date) and even to the CEO if needed. The idea is to notify the affected people so they can plan their activities effectively.

Network communications and the ability to program policies into the project database make it possible to set up virtual work groups that need not be located in the same place. The Intergraph/Dazix SEE, for example, has a CAD conferencing feature that joins the visual display with voice communications. Users at remote locations can talk on a conference call and simultaneously display screen data for

viewing during discussions. Changes can be made on the screen as they are discussed, problems resolved and approval cycles completed in real-time.

### Getting a Handle on the Process

Can an organization just install a PIM system and start realizing productivity gains and cost savings? Nothing is that simple. Speaking from the point of view of the software-development process, but with implications for other design disciplines, Atherton's Copping sees the task of getting control of the software development process as a



*Nick Copping, Atherton Technology president says that while the integration of engineering tools is important, an equally important question is, "How do you have to view software development, mechanical engineering, or electrical engineering to really run a business?" Computer aids to complex project management that consider technology needs, human needs, business needs and "quality-of-life" needs are vital to an organization's success.*

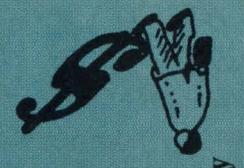
picture is a big one and not all companies are trying to address the enterprise-wide issues by themselves. Atherton Technologies is concentrating on the software development aspect while Mentor Graphics is concentrating on its expertise in EDA. Both are maintaining connections to the wider world because if the purchasing agent in Taiwan isn't notified of a change that affects purchasing, the effectiveness of the development project breaks down.

TeamNet utilizes the network file system (NFS) developed by Sun Microsystems (and now very widely used on Unix networks), to intercon-



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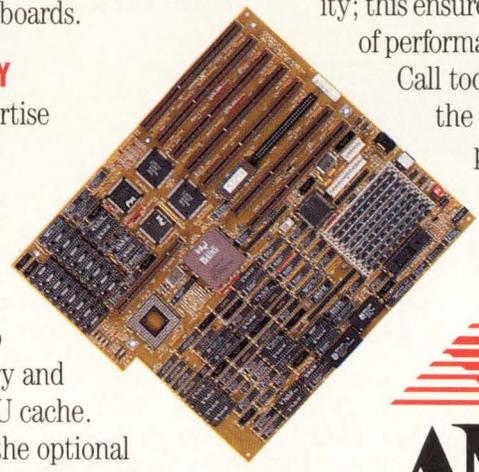
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## SOFTWARE TOOLS

matter of time. Citing a study done by the Software Engineering Institute (SEI) of Carnegie Mellon University, Copping notes that the software development process can be broken down into levels of maturity. At the first level, the development process is described as "ad hoc" or "chaotic"—planning and management are done pretty much by the seat of the pants. The second level is intuitive, that is, certain individuals are able to keep an over-

systems (Redmond, WA). Prior to the advent of the big engines, Jensen says, "We could all get away with not being better organized than the intuitive level." But complexity and size break down intuition, says Jensen, and when you get out of the intuitive level, you need a process to handle the complexity. "You have to set a policy and enforce it," he says.

At the first two levels, there's not much that management tools such

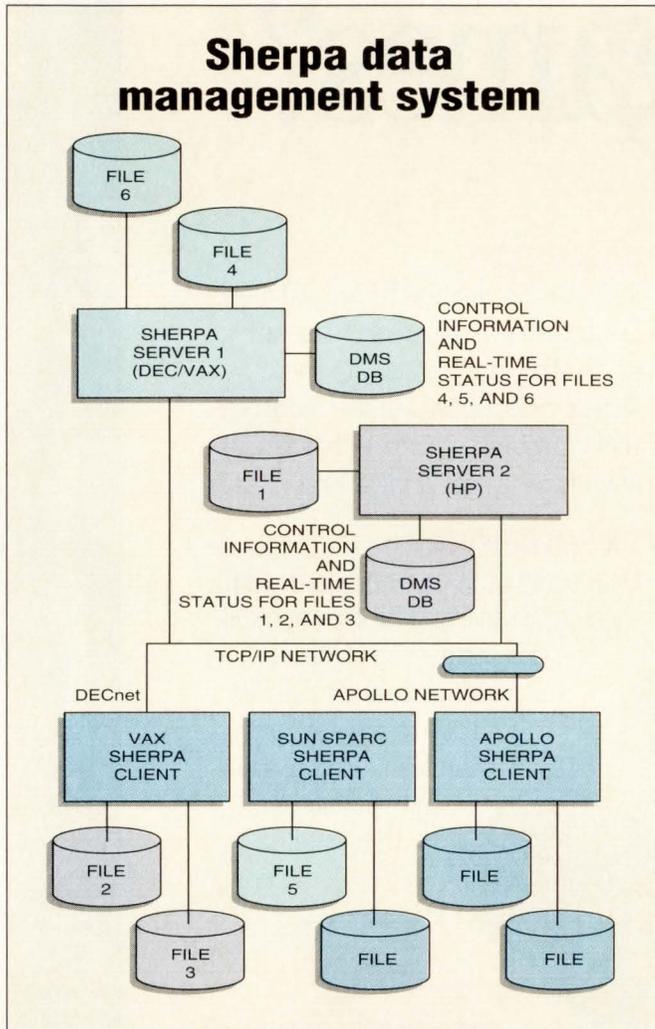
be enforced," says Copping.

It's at SEI level three—when the process is defined and institutionalized—that the introduction of new technology can aid the process. With policies stated and enforced, the effects of those policies on the design process can be measured and analyzed. With the technology in place, primarily the ability to program policies and procedures into the project database, there's a mechanism for change and a move to the fourth SEI level in which the process is not just enforced, but managed in terms of analyzing problems and the effects of changes.

Finally, at level five, achieved by only a very few projects according to Copping, improvements are fed back into the process to try to optimize it. The history of a project can be queried to answer questions like, "When was this defect introduced and how can we avoid similar problems?" Level five realizes that knowing how the data was built is as important as the data itself. If the origin of a fatal defect is buried somewhere in 50 file cabinets, says Copping, "it might be easier just to redesign the whole thing from scratch," than to try to find where a flaw was introduced. But moving from level one to five is a long-term commitment. It normally takes one to two years to move up one level of maturity, so getting to level five can be a ten-year proposition for a large organization.

### Gains for the bottom line

Productivity gains that can be realized from project-management systems, unlike design tools themselves, come mostly from attacking the non-value-added activities that go into product development. This includes such intangibles as "running around," looking for a piece of paper, figuring out what you're supposed to do first thing in the morning, etc. "Once policies and procedures are in place," says Copping, "people don't spend a lot of time trying to figure out what they're supposed to do and where they're supposed to do it. They don't have to worry about policies and procedures; the system will remind them." Applied Microsystems' Jensen agrees: "The perception that every time you put process overhead in place, it's costing money is not necessarily true. Every time you make mistakes because you don't have a process, it's costing money."



*The Sherpa DMS allows distributed and redundant file storage and management. Here, two different servers are managing files physically located on a server, one or more clients, or both. Files marked the project repository data and the numbered files contain design data. The HP-based server-2 can manage file one residing locally and files two and three residing on a remote VAX client.*

view of the process in their minds and direct it based on their experience and instincts.

In the case of embedded software, there's a crisis looming that has been brought on by the introduction of high-speed 32-bit processors with their gigabyte address spaces. "An engine that big requires a very different approach to embedded systems development," says Richard Jensen, vice president of new business development for Applied Micro-

as Atherton's Software Backplane can do for the process except to watch it unobtrusively. "But that's useful," Copping says, "because we can then decide we've got a policy or procedure we want to implement or that we want to change slightly what's going on." First you have to know what's going on, then it may become possible to articulate a policy. Once a policy has been articulated, management tools can come into their own. "If you can state a policy, it can

One company that's experiencing productivity gains is Sikorsky Aircraft, the helicopter division of United Technologies. In 1985, Sikorsky tried unsuccessfully to implement a system to manage its engineering data called Igor, named after helicopter inventor Igor Sikorsky. But management soon realized that the in-house effort required would be beyond them. Recently, however, the Igor project has been revived based on the facilities provided by the Sherpa DMS. These include the alert mechanisms mentioned above, version and revision control, electronic release facility, authorization levels for security and the user interface.

Coopers and Lybrand showed that an efficient data management system could reduce the overall engineering manpower budget by 20 percent. The systems achieved these results primarily by reducing the data-handling aspects of non-value-added activities by as much as one half. These non-value-added activities addressed by the study included processing engineering change orders (ECOs), tracking project status, the review and sign-off process, searching for parts information and retrieving and storing drawings.

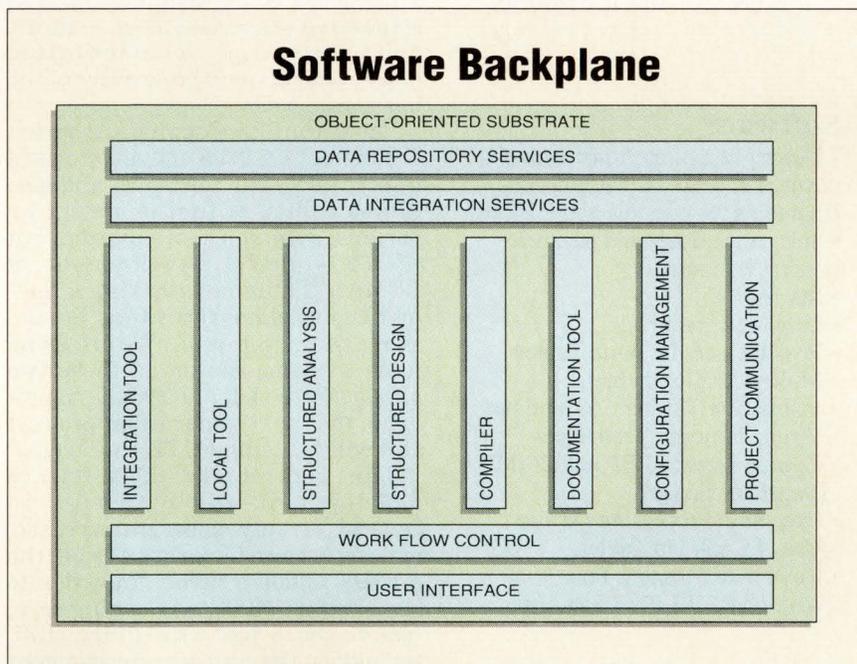
The study showed that other benefits could be expected in terms of reduced cost-of-quality, i.e. reduction in costs caused by scrap, the

nected via networks, comprehensive PIM systems tied to a single vendor's hardware are not going to have much of a future. Some vendors of PIM systems, such as Sherpa and TeamOne, have chosen to address the enterprise-wide concerns of an engineering operation. Others, such as Mentor Graphics and Ather-ton Technology, have chosen to first address the primary data-management concerns of their specialty (EDA and CASE, respectively) and to provide bridges, interfaces and avenues of growth to fit into the enterprise-wide environment.

The Sherpa Data Management System, for example, uses a client/server architecture in which a DMS server application and supervisor reside on a server node. The supervisor is a global network dictionary that keeps track of which server each database resides on. There's also a copy of the supervisor on each client node. In addition, the design files can reside on a server node, but can also reside as copies on whatever client nodes are convenient. This avoids having to send often-used files over the network each time they are called, but also maintains the integrity of the data management because the supervisor keeps track of all network transactions and policy events (e.g., meeting a requirement, sign-off, promotion to new level/version, etc.). Sherpa's Freedom architecture lets the system operate in a VAX/VMS environment, in an all-Unix environment, or across mixed VMS/Unix environments.

TeamOne's TeamNet has recently acquired a remote server option in which any system that can access NFS can be used to store engineering data managed by TeamNet. The mass storage of a large mainframe could be harnessed by the PIM system. Likewise, any client workstation that can connect to NFS can access and use design data managed by TeamNet. Actual data management takes place on the TeamNet server, which is a SunOS 4.X-based system, or on remote Sun clients running the TeamNet software. Project data is stored on the Sun server, but accessible via the NFS link by all client workstations (subject to access policy restrictions, of course).

The ability to operate in heterogeneous network environments is also vital to those PIM vendors who are concentrating on a specialty such as CASE or EDA because they



*Atherton Technology's Software Backplane is a set of management tools designed to comply with the ECMA model that consists of "horizontal" tools such as the user interface and repository and "vertical" tools such as compilers and debuggers. Software Backplane includes both horizontal and vertical services to manage the data associated with a software development project.*

Currently, about 250 users are accessing the new Igor system and the company soon hopes to have all 2,400 engineers and managers online soon. The goal, realistically anticipated by Sikorsky management, is for the mature engineering data-management system to reduce the costs associated with design engineering by 20 percent and reduce time-to-market by up to 25 percent.

These anticipated savings correspond to the results of a study commissioned by Sherpa to analyze return-on-investment for its engineering DMS. The study by

need to re-work products and service warranty claims. The combination of these cost reductions and increases in revenues resulting from reduced time-to-market could enhance the organization's overall bottom line by 15 to 20 percent. In many cases, these results let a PIM system that was widely used in a large organization pay for itself in less than a year.

#### ■ Mixing tools on a network

Because the computing environment for today's design organization is heterogeneous platforms con-

## SOFTWARE TOOLS

must be able to link and share their data with the enterprise-wide systems. Mentor Graphics, for example, has developed its Design Management Environment (DME) as an integral part of its Falcon Framework. But Mentor also realizes that there must be bridges that link to the wider world of EDA and plans to grow its own management system to address the enterprise-wide concerns.

According to Deme Clainos,

marketing manager for Mentor's PDM division, connections to the wider world have become imperative. "The first time a request is made for an engineering change order, the first thing a manager wants to know is what are the pluses and minuses. What's the effect on related designs?" In the past, Clainos says, companies like Mentor didn't worry about this because no one could solve the problems. "But as technology moves on, we're

capable of solving them and customers are pushing for solutions."

In the CASE arena, Atherton currently sells its Software Backplane as a management tool for CASE activities. The company is looking at fitting it more closely with Hewlett-Packard's Softbench, a growing de facto tools-environment standard for CASE. Software Backplane is a framework that can fit into the Softbench framework. And Softbench itself is modeled after the so-called "toaster model" devised by the European Computer Manufacturers Association (ECMA). In the ECMA model, there are horizontal tools such as a user interface, tool integration services and data repository. There are also vertical tools such as structured analysis tools, editors, debuggers, and documentation tools—that all use the services of the horizontal tools.

According to Copping, Atherton Technology will be moving toward integration with Softbench and also compatibility with the emerging portable common tool environment (PCTE)—also a development of ECMA—that aims at having a comprehensive data repository for design and project data. "We are going to do a harmonization of these two pieces (Softbench and PCTE) to produce the next-generation product and will be using PCTE as a basis."

The complexity of software development and of design in general is only going to increase, making it more imperative to get the process under control. "In order to have better software," Copping says, "you've got to deal with all the stuff, the uglies, the process improvement pieces, etc. The sobering news is that even Sony Handicams have software in them too, and probably more than the Patriot missile." ■

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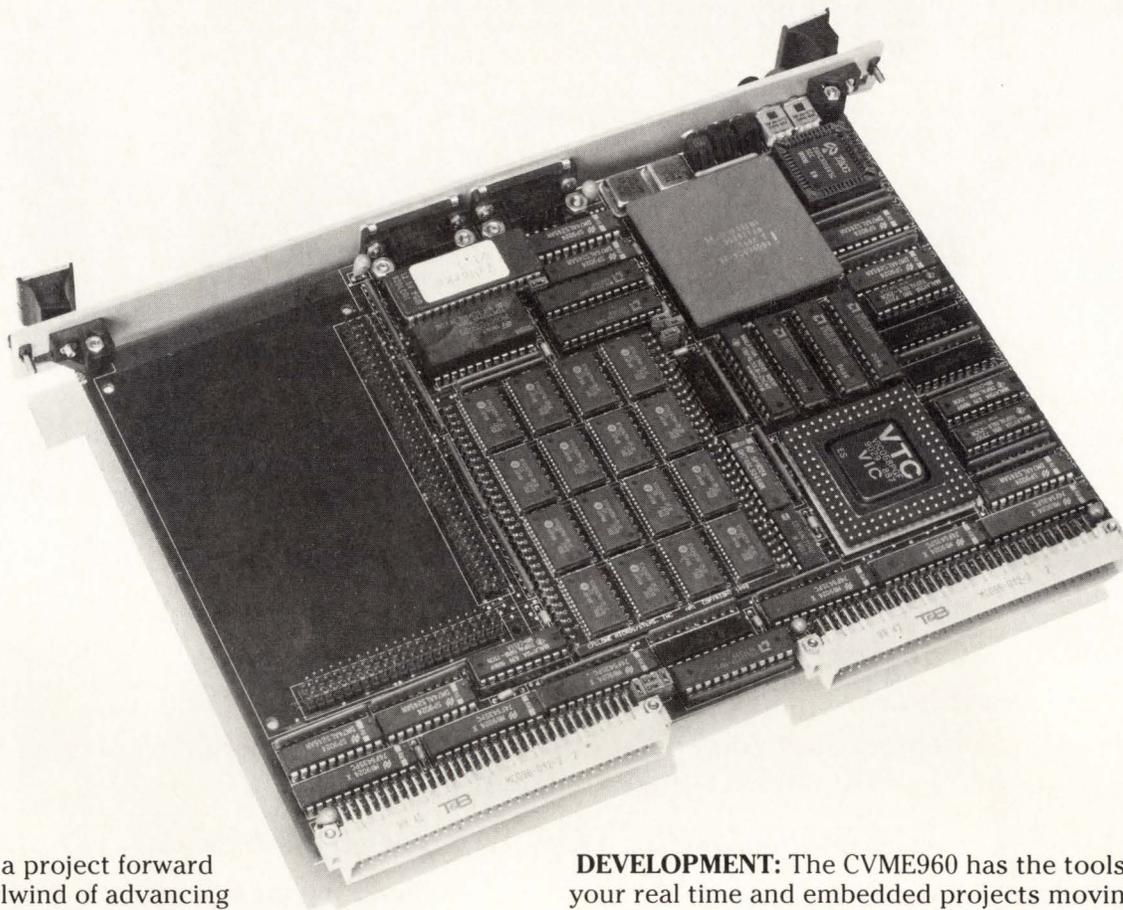
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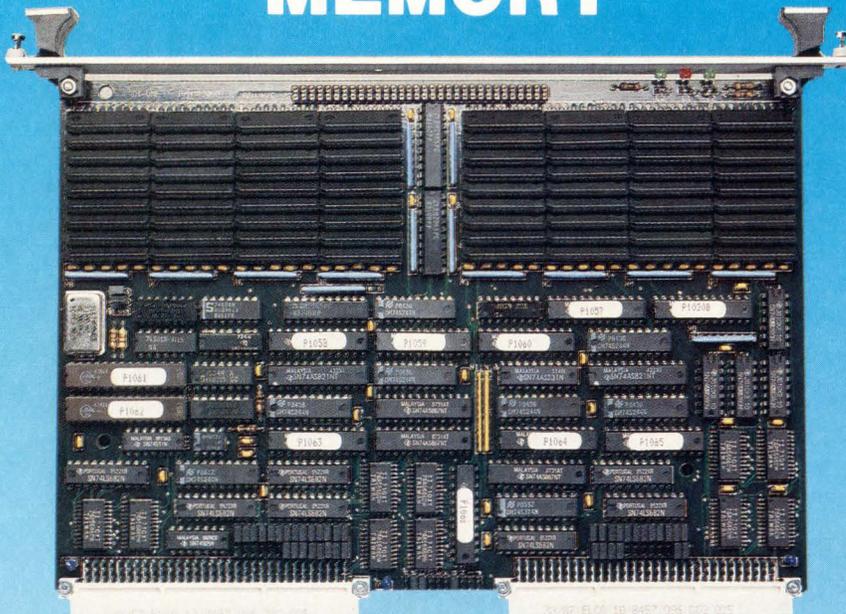
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CIRCLE NO. 53

# X Windows terminals designers search for a single-processor solution

*Many designs can deliver performance in X Windows terminals—but it may require a next-generation processor to get the cost down.*

Dave Wilson  
Senior Editor

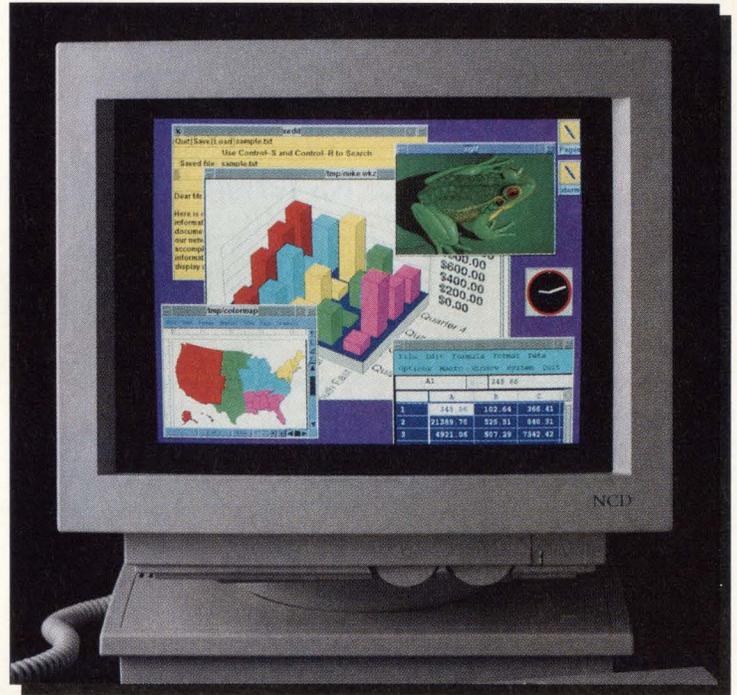
**S**omewhere between an ASCII terminal and a full-fledged workstation lives the X Windows terminal—promising workstation graphics at terminal prices. While the terminals provide an inviting graphics interface for users, they also represent an equally inviting market for chip vendors. Besides a local microprocessor, these terminals require quantities of other premium-priced devices: LAN controllers, memory controllers and video D-A converters. The chip volume represented by these terminals today is limited by their pricing, ranging from \$1,500 to \$5,000. The potential volume, forecast to unlock when terminal prices fall below \$1,000, has chip vendors waiting eagerly.

But while the chip vendors are waiting, it seems that terminal designers are determined to keep them guessing. Although all X Windows terminals look pretty much alike on the outside, it's difficult to find two that are built around the same design concepts.

The million dollar question is: which devices will emerge as the choice of X Windows terminal designers? The answer may have as much to do with company politics as it has with how effectively a specific hardware architecture can be optimized to run X Windows software.

## ■ Generic X

A generic X Windows terminal typically includes a CPU coupled with a graphics processor subsystem, a network controller, nonvolatile memory, and a peripheral controller. But the critical design decisions involve the CPU and graphics processor subsystem. And judging from the current crop of X terminals, these design decisions can lead in almost any direction. Hewlett-Packard (Palo Alto, CA) uses the superscalar i960CA RISC engine from Intel (Santa Clara, CA) as a general-purpose processor to perform both networking and graphics operations. Samsung (Andover, MA) chose the 29000 RISC processor from Advanced Micro Devices (Santa Clara, CA) to handle the same tasks. Network Computing Devices (Mountain View, CA),



*X Windows terminals require engineers to carefully balance graphics performance, end applications and price when designing new hardware architectures. The designers of this NCD14C chose a 20-MHz 68020 teamed with two custom graphics processors to drive the 14-in., 1024 x 768 color display.*

## X WINDOWS TERMINALS

on the other hand, opted for a 680X0 from Motorola (Austin, TX) to work with custom graphics controllers. Tektronix (Beaverton, OR) uses a combination of the TMS 34010/20 graphics processors from Texas Instruments (Dallas, TX) and the Motorola 68030. The X20 platform from Northwest Digital Systems (Seattle, WA) is simply based around a single TI 40-MHz 34020.

"Believe it or not, there's no one single approach that's best," according to Marco Thompson, president of Doctor Design Inc. (DDI), a design consulting firm based in San Diego, CA. "There are many divergent de-

sors) in an X terminal hardware design, it's important to understand the functions performed by the software running on the terminal. In an X terminal, a processor is responsible for performing two major tasks: handling network protocols and managing graphics functions. Concurrent with X protocol request processing, the software may also be handling inputs from the mouse or keyboard. The performance of the system can be optimized by examining the processor load for the different types of concurrent operations performed.

Depending on whom you talk to,

vendors offer software that conforms to the latest X Windows version from MIT, the added value comes in the enhancements that have been made to the software.

XSoftWare from AGE Logic (San Diego, CA) and TiX from X Technology (Derry, NH) are typical of software packages needed to build an X terminal. While XSoftWare runs on a number of processors, including the 29000 and i960 RISCs, X Technology has concentrated on the 34020 working with a PC host.

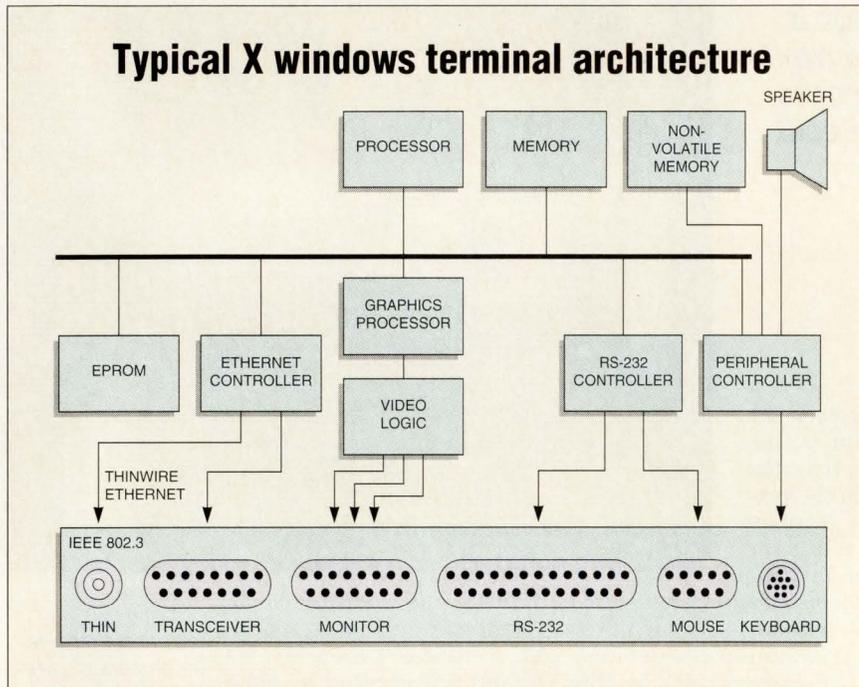
AGE's offering comprises the server code, networking software, boot ROM software and configuration menu software. A typical application mix might manage the network, decode the X protocols and maintain graphics contexts and draw pixels on the screen. Larry Hare, senior software architect for AGE Logic, agrees with DDI's Thompson that high performance is important for the general-purpose server and networking code, especially in light of new object oriented toolkits. These toolkits thoroughly exercise the non-graphics portions of the X server, he says.

### Duals or singles

Before deciding whether to design with a single graphics engine or use two processors, designers need to consider four factors, according to Charlie Jagow, project manager of Tektronix's X Windows Group (Wilsonville, OR). First is cost, second is time-to-market and third is performance. And last, but not least, is the familiarity of the designer with the software environment.

Dual-processor X terminal implementations fall into two categories. First, there are those that use a graphics processor, such as the 34020 for all graphics functions, and combine it with a slower general-purpose processor, such as the Motorola 68000 or Intel 80186 for networking. Many of the older X terminal designs used a dual-processor approach because the 34010 was not perceived to be powerful enough to handle both communication and graphics functions.

The second class of dual-processor designs is typified by the NCR (Lake Mary, FL) and Tektronix (Wilsonville, OR) terminals. Here, a 68020 or a 68030 is used as the main CPU. It runs the majority of the code with the exception of graphics routines that use the 34010 or 34020 micro-coded graphics processors. Tek-



A typical first generation X terminal includes a general-purpose processor, a graphics processor, a network controller and peripheral controllers. On second-generation X terminals, the trend is to use one processor for both graphics and network processing.

sign factors. They can include size of the monitor supported, whether or not color is involved and the performance that must be supported at a given price."

Thompson groups X Windows terminal designs into three generations. The first used a dual-processor approach. Today's second-generation products began the move to RISC technology for higher performance and lower cost. Third-generation products will be based on low-cost RISC processors that offer high performance and replace all the glue logic used in second-generation designs with ASICs.

To determine the suitability of a processor (or combination of proces-

X server code (which executes in the terminal) is somewhere between 50 and 60 percent general-purpose code and between 40 and 50 percent graphics code. General-purpose code performs networking and high-level graphics processing. The graphics software performs line drawing, pixel drawing, rectangle filling and block moving—the traditional graphics processor functions.

### Software provides the key

In designing X terminals, optimizing software performance with hardware is critical. X is partitioned such that there's a device-independent layer (DIX) and a device-dependent layer (DDX). While many

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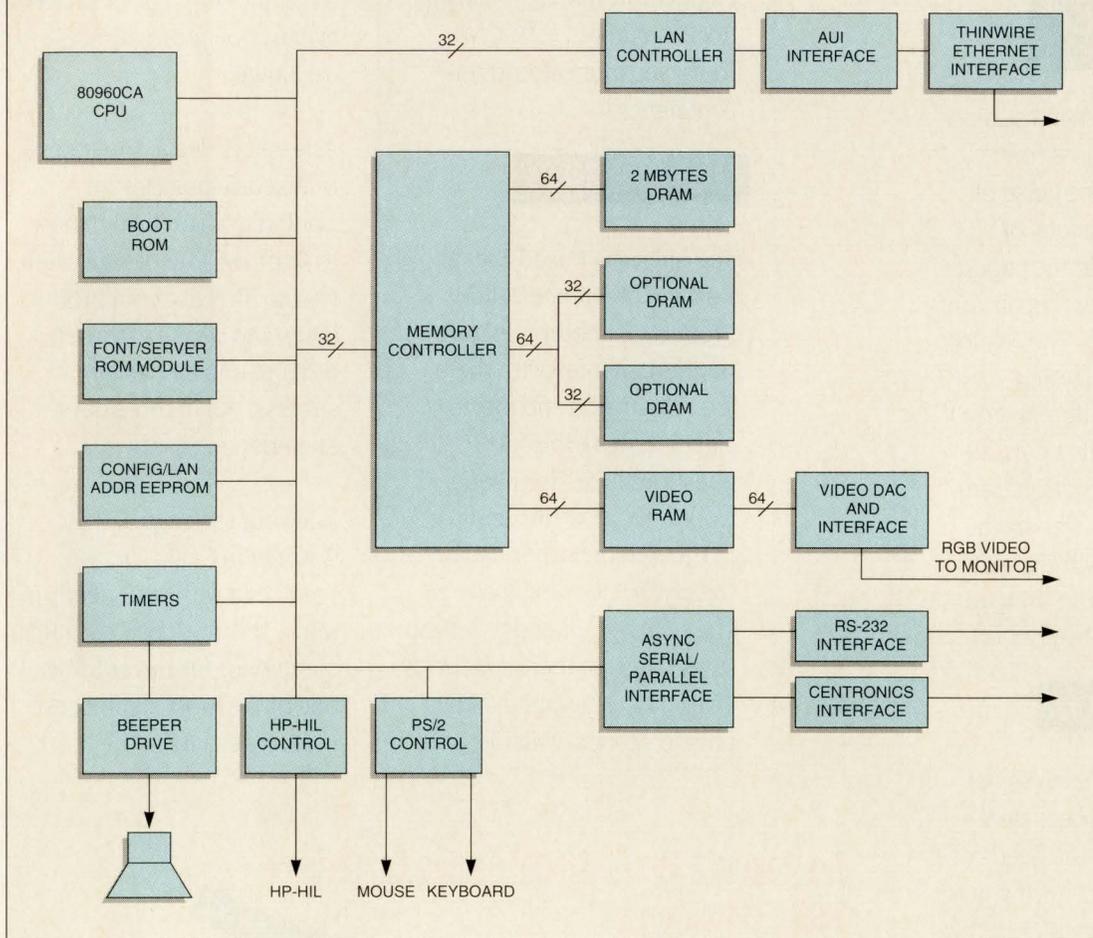
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## HP 700/RX architecture



*Hewlett-Packard's high-end 700/RX-CA X Windows terminal teams a superscalar Intel i960CA RISC processor with a custom memory controller that boosts graphics performance. Superscalar C code also helps the terminal perform faster.*

tronix's Jagow explains that in his design, the two processors can work asynchronously: while the 68030 is receiving X protocol requests, the TI processor can run the rendering code, generating pixel information from specific graphics requests. The Tektronix terminal also sports a custom gate array that handles positioning and moving of the X cursor.

Because the 68030 has a built-in MMU, Tektronix runs most of its X Server code on top of a Unix-like operating system. The use of a 68030 has given the company the ability to port the Motif window manager to run locally on the terminal. NCR, which also offers that capability, claims that bringing the function to the X terminal reduces network traffic. Some disagree. "A Windows manager in the terminal? It seems a bit silly to me", says Mark Champion, vice president of engineering at Northwest Digital Systems. "With the need for faster and faster X terminals, why start time

sharing the processor to run the window manager? What did you want — a fast X terminal or a window manager?" Champion feels that the attached computer is the place to perform Windows management functions, and hence NDS won't be jumping on the Tektronix/NCR bandwagon. Champion argues that network communication between the Windows manager and the X Windows terminal is insignificant.

While benchmark numbers may look reasonable, dual-processor terminals may not feel as "snappy" as a terminal designed around a good general-purpose CPU that performs both graphics and networking. Simply looking at benchmarks may not reveal why. Although most of the benchmarks used to rate the performance of X terminals may measure the effectiveness of line drawing operations, they do not represent real world applications.

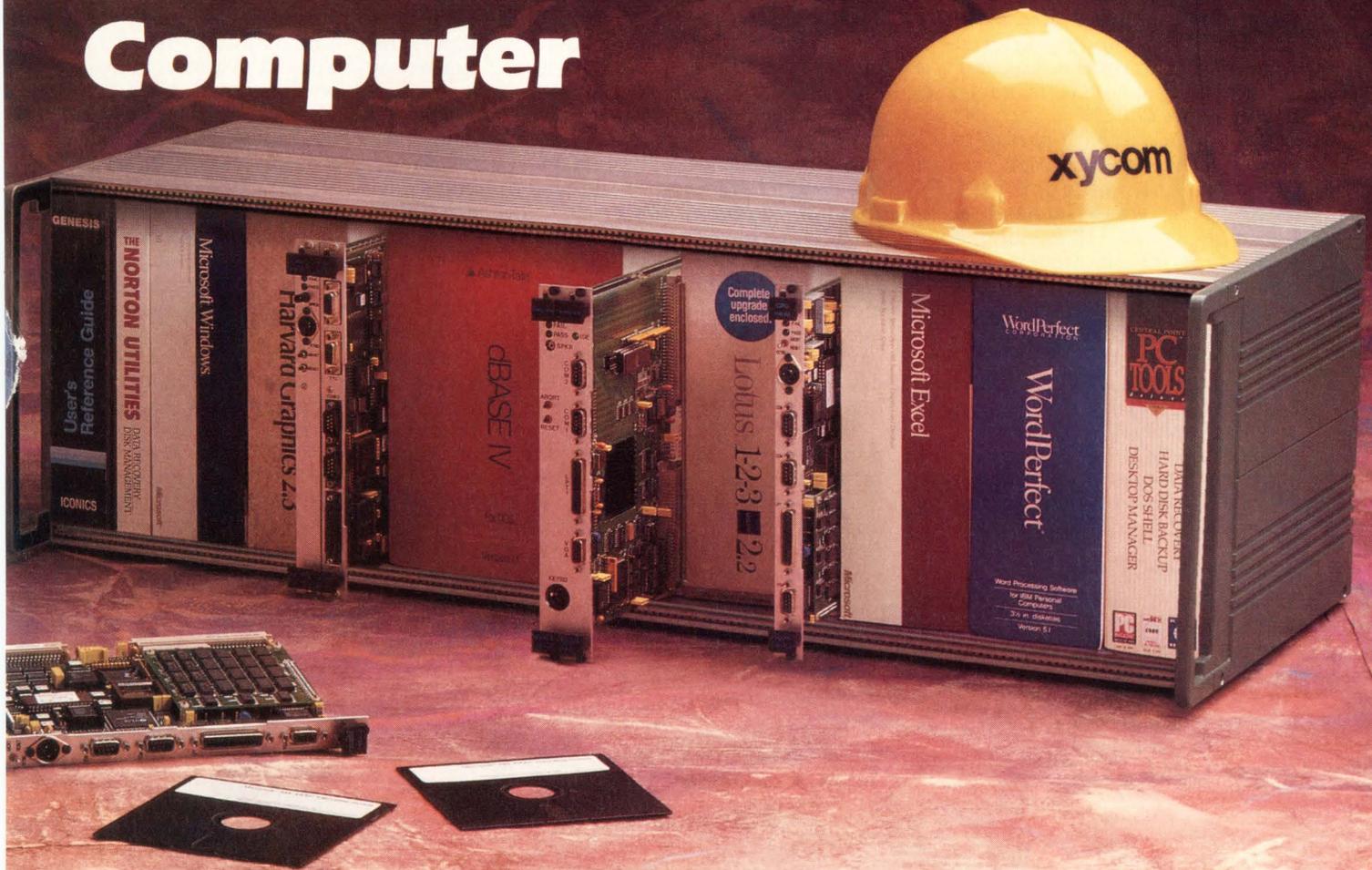
In an output-only operation, where the network simply feeds line

coordinates to the terminal which draws them, a dual-processor design can be an effective solution. But if the general-purpose networking processor is slow, it may be more effective to run the networking code directly on the 34020 graphics processor.

"Ultimately, the added overhead involved in synchronizing a general-purpose processor with a graphics processor that handles small graphics loops may actually result in wasting more time than performing the graphics operation on a fast general-purpose processor, like a RISC chip," says AGE's Hare. "Although both terminals may end up measuring the same in the benchmarks, the terminal with the dual-processor design may feel only half as fast to the user," he adds.

DDI's Thompson agrees. "We've found that the coprocessor approach doesn't take advantage of the performance of both processors, because we're dealing with a single-threaded

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## ■ X WINDOWS TERMINALS

software operation. In most dual-processor configurations, one processor tends to be waiting on the other. The only benefit of having a 68020 front-ending a product like a 34020 is that the graphics code is easier to write on the 020 and the general-purpose code is easier to write for the 68030."

"I would agree with part of that," says Tom Arthur, X Station product development manager at IBM (Austin, TX), whose latest X terminals support a 80186 in conjunction with a TI 34020 processor. Like others, the general-purpose code was easier for IBM to write on a 186, while the graphics code was easier on the 34020. "We had to concentrate on the area of synchronization, but to say that one processor is always waiting on the other is an overstatement. Our software is ported by AGE, and some of our efforts with them were aimed at making the synchronization work better."

### ■ i960 versus 29000

Most agree that a single-processor solution is more effective than a dual-processor implementation—at least in terms of cost, if not necessarily performance. But should designers choose a RISC processor implementation based on the 29000 or i960, or a standalone graphics processor implementation around TI's 40-MHz 34020? And even if designers settle upon a RISC processor to run all of the code, should they opt to design custom silicon to accelerate certain common graphics functions like scrolling, fills, and tiling operations? With a RISC CPU such as the 29000, designers should carefully weigh how much extra performance this approach will buy them.

Designers that have invested in RISC agree that it's important to choose a vendor with a family of devices, rather than just a single processor. In this way, software investment in the device can be preserved across a number of designs at different price/performance points. Both Intel and AMD currently have a range of derivatives in their i960 and 29000 families.

"Both are good embedded RISC processors," says IBM's Arthur.

"Each of them have pluses and minuses. But while the 29000 has an MMU, the i960 doesn't. And today's breed of programmer assumes that systems have virtual memory. So if your (X Windows) platform supports an MMU, porting of code will be far easier."

### ■ How do they handle memory?

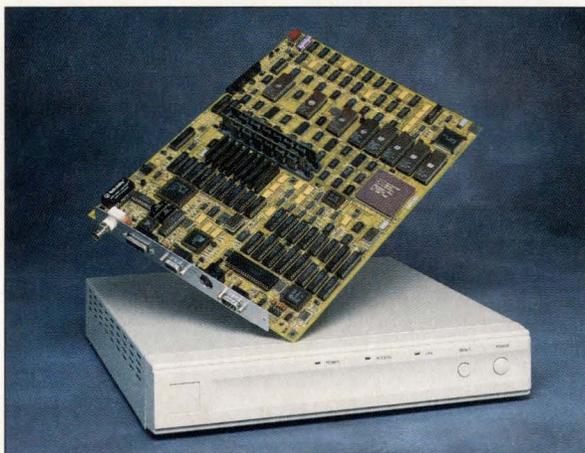
The effectiveness of the memory subsystem is very important in all X Windows designs. "We assume all RISC chips have (roughly) the same performance and make our choice based on availability and price, the availability of development tools, and how hard it is to interface to device," says Ed Basart, vice president of engineering at NCD the leading vendor of low-cost terminals.

While X and the i960CA may support different memory-interfacing techniques, they share some things in common. One of these is that load and store operations are decoupled from CPU execution. Once a load operation is initiated, for example,

the processors can continue executing if there are no other instructions that require the results of memory. Most other RISC processors don't offer capabilities such as these, so those processors may halt instruction execution until the load or store operations have completed.

The 29000 sports several features beneficial to designers of graphics terminals. For data accesses, for example, it will try to perform Load Multiple and Store Multiple operations using burst-mode accesses. Burst-mode accesses take advantage of sequential addressing patterns and let the processor operate with standard DRAM memories in page-mode, which improves the access time of the system and keeps costs down. Although the first burst-mode memory access may take four or five processor wait states, every memory access after that might only take one. Hence, the processor provides a capability that lets the designer control the memory bandwidth of the machine and get a single-cycle transfer on large pieces of memory.

DDI's Thompson feels that the



*Dr. Design's President Marco Thompson is designing two gate arrays for a next generation X Window's controller. He claims that the new board will be half the size of the current XQC-8200 controller (inset) and match the performance of the i960 CA-based Hewlett-Packard controller for about half the price.*

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## X WINDOWS TERMINALS

29000 has the edge over the i960 because of its triple-bus (data, instruction and address) architecture. "The most important feature of the 29000 processor is its ability to execute an instruction on every clock cycle while also performing a data transfer on every clock cycle to randomly access or burst access data from the video memory," he says. While Thompson agrees that the i960CA can do that, he feels it's limited in its ability compared with the 29000. "The i960CA doesn't allow these operations to be performed in parallel."

There are other, more detailed, reasons why Thompson likes the 29000. "The 29000 can barrel shift and merge a 64-bit entity into a 32-bit entity in a single instruction. This is a very important function if you're performing a bitblt on nonaligned boundaries. And a lot of an X terminal's performance is highly dependent on how effective windows can be moved around—in other words, how effective the bitblt function is."

Despite these problems, the i960CA has some advantages over the 29000, like a superscalar architecture that in some cases can allow more than one instruction per clock cycle. "Nevertheless," says Thompson, "when we looked at a product based on the 29000, and took into account the memory system, the external logic required for the memory system, and the processor, we found that we could get more performance for less money with a 29000 that with a i960."

But just how good is the 29000 in comparison to other approaches? According to DDI's Thompson, a 29000 can draw lines and move pixels, faster than a 34020. "Because of the serial nature of most X protocols, a single RISC processor that works faster than a 68030 or a 34020 is the right X Windows solution from a price/performance standpoint. AGE's Hare agrees. "With the 29000, you can write code that will do graphics operations such as tile patterns much faster than many graphics processors."

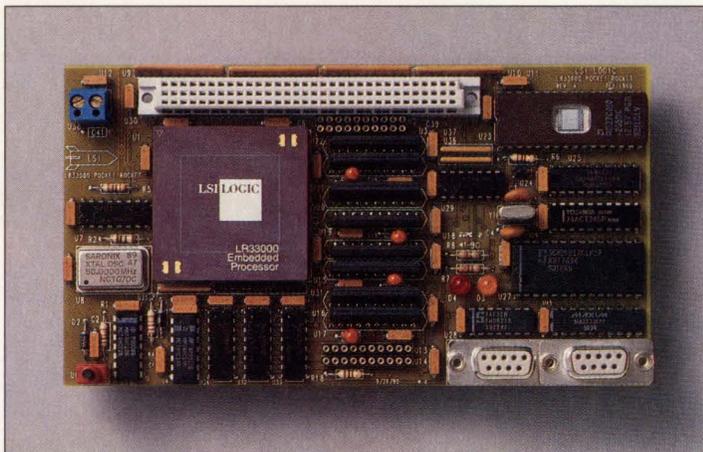
Like the 29000, the designers of the i960 RISC controller paid atten-

tion to supporting useful memory-interface features. These can be used to advantage by software designers. A multi-word memory access capability, for example, can provide a programmatic means to control burst-mode access to memory. According to AGE's Hare, by recoding graphics algorithms to use the processor's quad-word transfer capability, designers can reduce the average time required to

trollers for both Samsung and Arche Technology. The Samsung terminal is a 17-in. color unit based on DDI's XQC-8200 and priced at about \$3,500. To further reduce the size and cost of the XQC-8200 controller, the company is developing two ASICs (called the DDI-4129 and DDI-4029), that will work with the 29000 and effectively shrink the size of the XQC-8200 by 50 percent.

The DDI-4129 will support color resolutions up to 1280 × 1024, while the DDI-4029 supports lower resolutions up to 1024 × 1024. Both ASICs support monochrome resolutions up to 1600 × 1280. DDI will also sell the ASICs to interested third parties.

At the high end of the X terminals world, Hewlett-Packard (Waterloo, Ontario, Canada) is one company that chose the i960CA for the design of its HP 700/RX family of X-Stations. The terminals range in price from \$3,000 for monochrome to \$6,000 for the color version. Jeff Dawkins, project



*Some designers think that LSI Logic's LR33000 RISC chip may be the next wave for X terminals. The 33000 integrates 8 kbytes of instruction cache and 1 kbyte of data cache on chip. It also sports three counter/timers, a DRAM controller, write buffer, and wait state generators on-chip. Shown here is the "Pocket Rocket," a \$700 25-MHz evaluation module.*

transfer one 32-bit word from four wait states to two wait states, doubling the performance of the X software for that operation.

### Design ins, design wins

In May, DDI's XQC-8200, a color X Windows base unit and controller system based on the 20-MHz 29000, won a bid from CCL (Computer and Communications Laboratories), a government consortium based in Taiwan. The goal of the consortium is to standardize on an X terminal design that will be manufactured as a product for up to 17 Taiwan-based companies like Acer, Tatung, Qume, ADI, and CTX. The XQC-8200 technology license provides a complete package of design data, manufacturing and test data, documentation, and manufacturing rights to licensees. "The CCL win means that in the next year you will be seeing a whole variety of X Terminals based on our design and the 29000 processor," says Craig Schmidt, vice president of marketing at DDI.

DDI has already developed monochrome and color X Windows con-

manager for the X Windows terminals project says that one of the reasons the i960CA was chosen is that the design did not call for memory management or floating point capabilities. The 22.5-MHz speed of the i960CA is consistent across all the Hewlett-Packard designs. Performance differences in the family are due to different memory controllers. The high end of HP's family, the Ca X terminal, uses two HP-designed custom controllers that bank-interleave memory and achieve zero wait state burst-mode accesses at full CPU speed. HP's 16CI and 19MI terminals use a somewhat simpler memory controller. Engineers at HP designed the custom memory controllers when they couldn't find an off-the-shelf solution that met performance and time-to-market needs. "We wanted very high processor/memory bandwidth both for keeping the CPU running at maximum speed and for performing high-speed bitblt memory transfers," says Dawkins.

According to Marc Morin of Morin and Associates (Waterloo, Canada),



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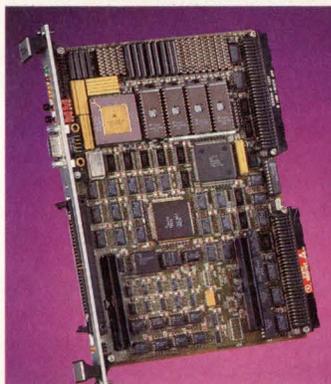
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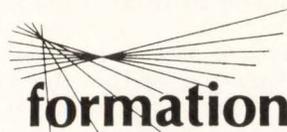
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## ■ X WINDOWS TERMINALS

a contractor to Hewlett-Packard that performed the i960CA work, the independent bus controller and register scoreboarding in the i960CA let the computation and memory subsystem operate in parallel. For bitblt operations, which are memory bound and not CPU bound, the memory system is driven at 100 percent bandwidth while the i960 is also executing two instructions per clock cycle. Multi-byte memory operations increase the memory bandwidth by performing a bus cycle that reads (or writes) two to four words at a time. With a zero wait state memory subsystem (with pipelining), the i960CA can read one long word per clock cycle and write four long words in five clock cycles continuously.

The 700/RX's 1 Kbyte of on-board SRAM is accessible in parallel with the external memory. This lets the i960CA access results within this area of memory without affecting the external bus controller. The SRAM has a 128-bit wide bus that lets the i960CA read or write a quad word on every clock cycle. The 700/RX uses this area as a scratchpad for graphics rendering. Finally, Morin says, the i960CA's extended-shift right instruction is very useful for rendering in X. It extracts a 32-bit value from a 64-bit quantity, which permits barrel shifting the data during a bitblt and for collecting bits from fonts when rendering text. According to Morin, this feature alone was responsible for doubling the speed of text rendering in the design.

### ■ Graphics processor advantages

The tradeoffs between a dedicated graphics and a RISC approach are many. Although RISC may have captured more attention in recent months, the 34020 has a lot going for it. Its first attraction is cost. A RISC processor may cost more than a dedicated graphics engine. The second attraction is software. With RISC, designers may have to write lengthy code to perform graphics operations, while the 34020 provides common routines, like pixblt, in microcode. The third plus is the memory interface. The TI design allows memory architectures that are simpler and less expensive than those required by many of the RISC processors.

Unlike a RISC processor, the 34020 has a set of general-purpose functions as well as graphics func-

tions that can be used to construct high-level functions. It also provides programmable control of the CRT interface as well as the memory interface (both standard and multi-ported DRAM). TI claims that a very effective X Windows terminal can be built based on the 34020 working with the 34075 video interface palette. One design can cover a range of resolutions (up to 1280 × 1024), pixel depths from monochrome to color, and support the PEX 3-D standard by adding the floating point 34082. Such a design might use as few as 50 ICs, or fewer in designs using gate arrays for bus control logic.

Northwest Digital Systems' NDS X20 controller is a single-board controller that uses the 34020 as a single chip to perform all graphics and networking functions. NDS' Mark Champion says that "although they got a bad rap in the past as single-chip solutions, when you really look at it, these processors don't have to do a heck of a lot. This is an embedded application, and the processors don't have to run a wide range of code."

NDS decided to go with a single processor because it was a less-complicated hardware solution. Like others in the business, NDS felt that a dual-processor design meant that it would need to build a communications protocol to allow two processors to communicate, and that the protocol had the potential of becoming a system bottleneck.

Having had some experience with earlier 34010 designs, NDS is pleased with the performance enhancements Texas Instruments has added to the 34020. First, the 34020 runs at twice the clock speed of the 34010. Second, it's a 32-bit, rather than a 16-bit, processor. And it has the ability to take advantage of page-mode memory, which the 34010 did not. Finally, the 34020 boasts a 512-byte instruction cache, double that of the 34010.

NDS used TI's optimizing C compiler on the X windows code the company wrote to maximize its performance. NDS also rewrote the inner graphics loops in assembly language. Not only did that help speed up performance, it also let the company run the loops out of the on-chip cache.

There are others, however, who aren't quite as sold on the TI approach. "You're not going to get good performance with an antiquated

part like the 34020." retorts NCD's Ed Basart. "It was invented 10 years ago and it takes a lot of clocks to get much done."

### ■ Is a single-chip solution coming?

Clearly, the RISC camps have squared off against Texas Instruments for "The Battle Of The Third-Generation Design Win." But with all the activity surrounding X Windows, it seems that a single-chip X Windows processor might soon emerge to compete with embedded RISC processors and graphics processors. Such a processor might be based on a RISC core, and would certainly embrace a feature-ridden, low-cost memory-interfacing strategy. "That's a very interesting idea," says IBM's Arthur. "The question is whether or not X is going to be pervasive enough to make it worthwhile building something dedicated to it."

Quite possibly, a better RISC for X already exists. "Neither the 29000 or the i960CA are anything compared to the LR33000 embedded RISC processor from LSI Logic (Milpitas, CA)" says NCD's Basart. Although no vendors have currently announced terminals using the chip, Basart is very enthusiastic. "It blows everything else away," he says. ■

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**MOTOROLA**

# What do digital designers need to master the art of analog design?

Barbara Tuck  
Senior Editor

*Real-world applications are forcing more engineers to include analog functions in their designs. But analog design is an arcane art form for many of today's engineers. Better tools from CAE and silicon vendors will help, but it will be a long time before tools can replace the skills of a seasoned analog designer.*

**A**nalog design is still an art because the sophisticated analog specialist is the only one aware of all the nuances and complexity of a design. But for digital and system designers, the vision of a mixed analog and digital design is anything but a pretty picture. Nonetheless, the real world is analog, and the demand for end products such as pacemakers, hearing aids, cellular phones, and disk drives is forcing designers to address the problems that surround mixed-signal design.

The growing requirements for mixed-signal design are increasing pressure for better design tools and support. Tool vendors and silicon vendors are developing new strategies to bring mixed-signal design capabilities to more users. One primary difference in these strategies is the degree to which they put design responsibility into the hands of the end user.

## ■ The two extremes

Perhaps the two companies which best illustrate the extremes in the degree to which mixed-signal devices can be customer-designed rather than customer-specified are Analog Devices (Norwood, MA) and SGS-Thomson Microelectronics

(with headquarters in Grenoble, France; Agrate, Italy; and Carrollton, TX). Analog Devices strictly adheres to the turnkey design approach while SGS-Thomson has installed design tools for its analog cells and arrays at 50 customer sites. Philippe Lambinet, SGS business manager of analog cells and arrays at Grenoble, reports that the 50 sites represent a 100 percent change from about two years ago. Half of the SGS customer sites are in Europe where users have been faster to accept mixed-signal design responsibility. SGS mixed-signal design activity is currently split on a 60/40 basis, with 60 percent of the designs being done externally.

SGS offers design flows, such as the Analog Design System based on the Design Framework from Cadence Design Systems (San Jose, CA). For simulation, SGS includes its own Mozart digital simulator and the Anacad (Grenoble, France) Eldo mixed-mode analog simulator, which has its own Spice circuit simulator. SGS handcrafts its standard cells and offers users of its Bi-CMOS STKM2000 standard-cells the ability to modify the behavior of analog and digital functions through the use of module generators. CMOS

standard-cell users are not offered that flexibility. By October, libraries will be ported to Eldo in the FAS analog behavioral language, which Lambinet says will cut simulation times from hours for transistor-level models to minutes for the new behavioral models.

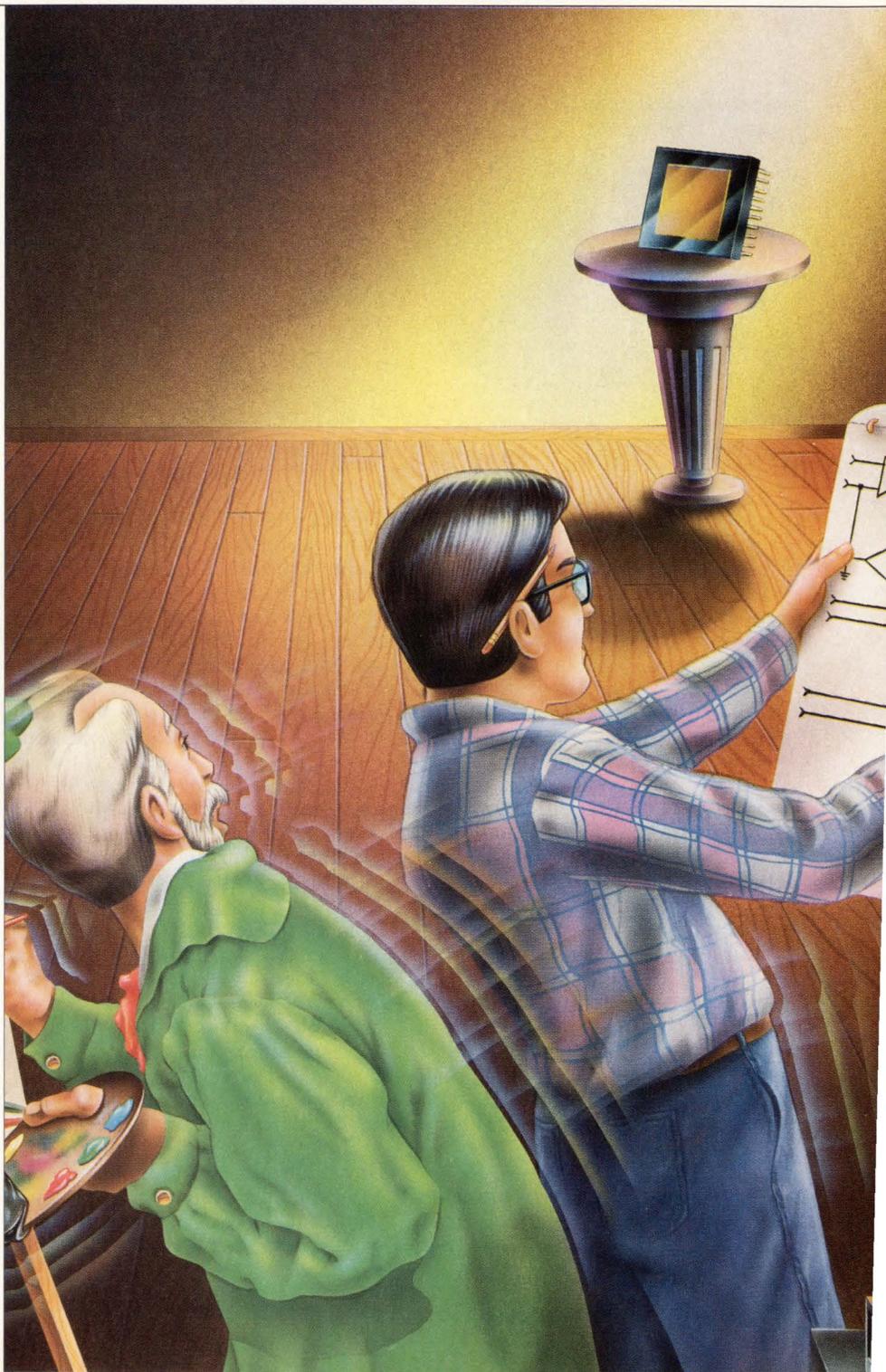
Analog Devices, highly respected for its precision analog products, is at the other extreme when it comes to putting tools into users' hands. Tremont Miao, Analog Device's ASIC strategy manager for mixed-signal ASICs, admits that, "We're not viewed by the industry as being very cooperative. We hold onto everything, some say." But Miao explains that, "At the 8-bit level, vendors may let people make their own mess. But beyond that, mixed-signal has to be accomplished as a turnkey custom design." According to Miao, modeling and simulation is lagging. "All model languages are too restrictive to let us do what we want to do. We don't have good transmission-line effect models, parasitic models, or crosstalk models." The system or instrumentation person moving into chip design lacks the ability to predict the interactions of analog and digital, explains Miao. "At design and layout reviews, customers ask

about parasitic phenomena and where to run power lines.”

#### ■ Modeling dilemmas

Miao thinks that in the future customers will use cells, models, and system-level simulators at their own sites, but that models will have to be prepackaged like data sheets. “We wouldn’t be able to guarantee manufacturability if users could modify models and cells,” he says. Miao distinguishes between Analog Devices’ modeling methodology and a “polygon-pushing” methodology. For example, to modify a particular cell to drive 10 mA instead of 2 mA, polygon pushers, according to Miao, “go in there and pull the design apart and open Pandora’s box.” In such an instance, Analog Devices would design a new cell and build a model, says Miao, because of all the yield-related issues involved. According to Miao, the results prove Analog’s approach; he claims that 80 to 90 percent of their mixed-signal designs go to production.

Analog Device’s Spectrum event-driven, mixed-signal simulator is based on a dynamic partitioning algorithm that, Analog claims, significantly reduces simulation time in mixed analog/digital circuits. Spec-



## ■ MIXED-SIGNAL TOOLS

trum's extensible framework lets multiple simulation algorithms be integrated to operate together. An automatic behavioral model generator analyzes circuit topology and creates switch-level behavioral models. Based on pattern recognition and signal flow, the algorithm currently generates CMOS and ECL logic models and

Jose, CA) and the Mentor Graphics (Wilsonville, OR) Lsim simulator. Sierra relies exclusively on behavioral models, developed using Spice. Mac Lennan says that, "The perception that behavioral models are not as accurate as transistor models is a fallacy if they've been developed for a specific application. We've never had a device fail," says

havioral models, but he relies on a breadboard for system-level simulation. Says Curtis, an analog designer for 25 years, "Tools have to be more accurate and faster than I am for me to use them, no machine knows the nuances of analog design. The tools will need artificial intelligence." On-Chip is a customer of Triquint Semiconductor (Newbury Park, CA) for mixed-signal designs fabricated in gallium-arsenide. "We use GaAs and anything else that supports analog or mixed-signal," he says.



*Cardiac Pacemakers depends on transistor-level models in Meta-Software's HSpice to provide the required accuracy in its analog designs for cardiac pacemakers and implantable defibrillators. Manager of IC design, Janet Babka, says her group is now using Viewlogic's digital simulator for the digital portions of their designs and considering VHDL behavioral modeling.*

## ■ Silicon breadboarding

Gary Kennedy, president of custom IC manufacturer Orbit Semiconductor (Sunnyvale, CA) offers a custom chip design program he refers to as Tiny Chip to mixed-signal designers who might not have analog expertise. Kennedy says that with Tiny Chip, designers partition the analog portion of a design right up front in the design cycle and send specifications to Orbit. For \$1,500, Orbit runs the critical analog section though the fab and returns a dozen silicon prototypes four or five weeks later. In the meantime, users can fully simulate the digital portion of the design. Though Tiny Chip delivers a working analog section, customers still face the obstacle of merging the analog with the digital and performing system-level simulation.

a wide range of analog models, such as differential pairs, current mirrors and integrators.

Modeling is the top priority of vendors and the major concern of users because there can be no simulation without models. Differing opinions as to the difficulty of modeling seems to be a function, at least in part, of how much of a mixed-signal design is digital and how much analog, as well as how complex and precise the analog functions are. Don Mac Lennan, vice president of marketing at Sierra Semiconductor, which made its Montage simulator available to customers years ago, says that, "Modeling is not a problem unless, of course, you're looking for the Holy Grail, for engineers to sit down and just bang out a design." Sierra works on a semicustom basis with its mass-storage customers, almost entirely on application-specific standard products (ASSP) for communications and graphics products.

## ■ Runtime vs. accuracy

In addition to its own Montage simulator, Sierra uses tools from Compass Design Automation (San

Jose, CA) and the Mentor Graphics (Wilsonville, OR) Lsim simulator. Sierra relies exclusively on behavioral models, developed using Spice. Mac Lennan says that, "The key here is time to market and accuracy."

Janet Babka, manager of IC design at Cardiac Pacemakers (St. Paul, MN), says that her group has to create all transistor-level Spice models because their designs operate in the weak-inversion area of the transistors. "It's very difficult to model," says Babka, "because the models have discontinuities when you're transitioning from one area to another." Babka's group, which develops pacemakers and implantable defibrillators to treat slow and abnormally fast heartbeats, uses the HSpice circuit simulator from Meta-Software (Campbell, CA) and the Viewsim digital simulator from Viewlogic (Marlboro, MA). Since the Viewsim/HSpice mixed-mode environment supports multi-level modeling with speed/accuracy tradeoffs, Babka's group is looking into using VHDL behavioral modeling for digital portions of the design.

To verify mixed-signal designs, Doug Curtis, president and engineering director at OnChip Systems (San Jose, CA), uses both Spice models and, to a limited extent, be-

## **Why the confusion about mixed-signal?**

**T**he practice of mixed-signal design today depends on a mixed technology base. Designs blend custom and semicustom methodologies, including ASIC, USIC, CSIC, ASSP, or just plain IC. And since mixed-signal requirements are encountered in such diverse applications and products, there are many different definitions of mixed-signal.

The result is that mixed-signal has about as many faces to it as analog design has variable parameters. Just as numerous are opinions on how effectively today's design tools can substitute for analog expertise.

It's important to note that, with so many variables in mixed-signal, the opinions and strategies of any vendor or user will be largely influenced by the particular technologies being supported or implemented.

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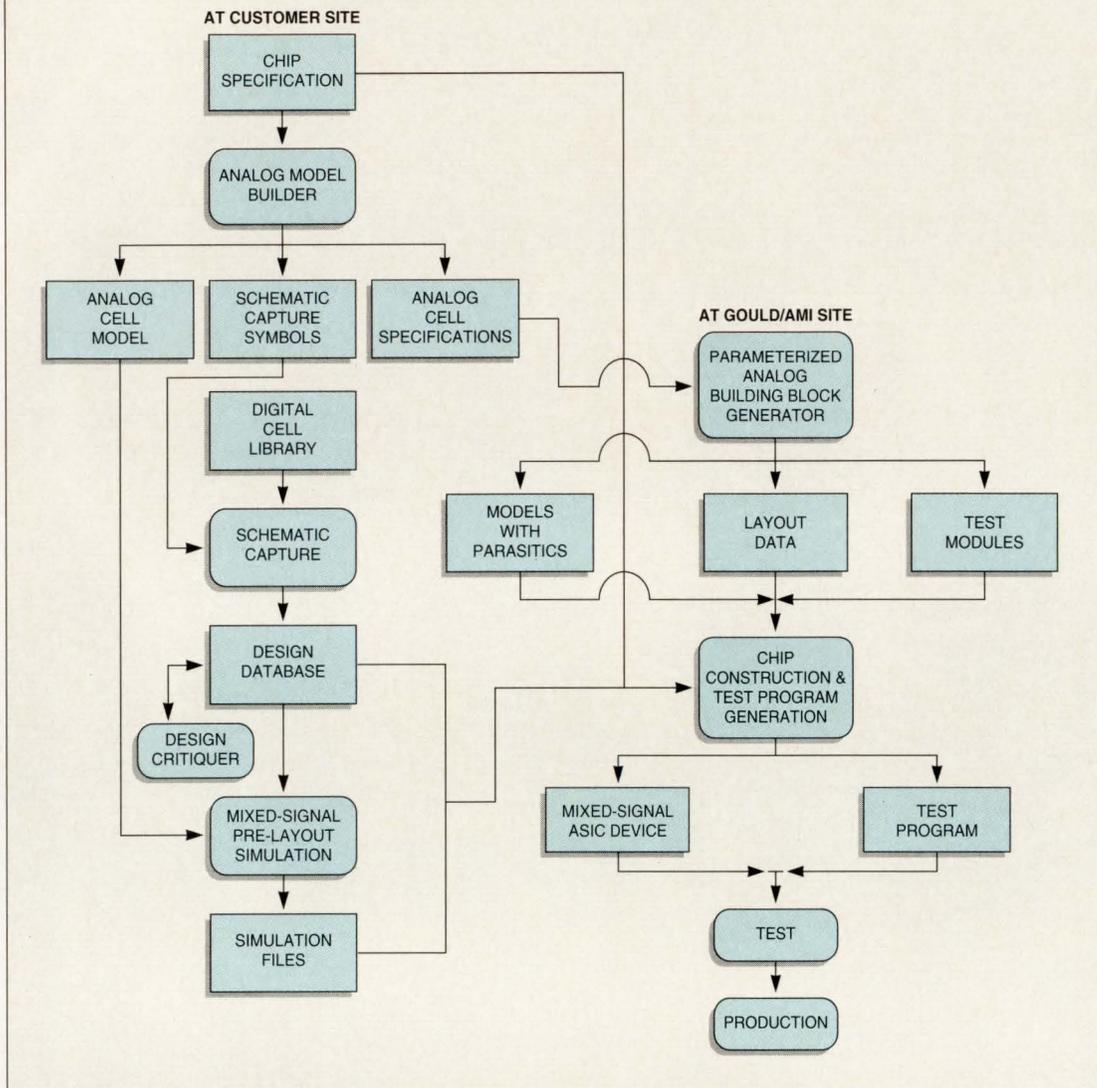
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## Mixed-signal design flow



*This design flow illustrates the complexity of mixed-signal design and the critical interactions of an on-site designer and an ASIC vendor. The flow diagrammed is typical for the enhanced toolset to be released next month by Gould/AMI for customers designing with its mixed-signal libraries.*

The accuracy of the model for the interface between analog and digital circuitry in a system-level mixed-signal simulator is a major customer concern. Viewlogic user, analog design engineer, Omer Kal, of LSI Logic (Milpitas, CA), is hesitant to trust the interface of the coupled HSpice and Viewsim. "I rely on Spice to verify those timing interfaces," Kal says. He wants to avoid any inaccuracies that might occur within the algorithm that converts the event-driven digital to time-based analog, so he works around the coupling. Kal's department handcrafts customer-specific, mixed-signal cells for LSI's strategic customers.

Sandra Hawley, manager of electronic technology at Rosemount (Eden Prairie, MN), a manufacturer

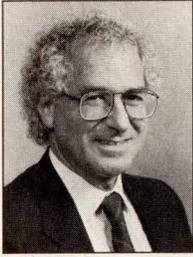
of industrial controls, shares Kal's cautious attitude with regard to the interaction of analog and digital simulators. "It hurts the design if we can't look at the relationship between analog and digital when simulating." As a result, she admits that, "It's not a really warm feeling going out of here with some of our designs." Hawley's design group is using libraries from NCR Microelectronic (Fort Collins, CO) to develop a cell-based 7,000-to-8,000-gate ASIC for a measurement system. The group uses HSpice for analog and Verilog for digital simulation. The biggest issue Hawley faces as a manager, she says, is having to work with tools that are not mature. "I don't think tools for mixed-signal design are there yet," she says. "It's not

an individual vendor's problem, but an industry problem."

### Built-in analog expertise

Among industry vendors addressing the concerns of designers is Gould/AMI (Pocatello, ID) which expects to release an enhanced mixed-signal toolset next month. Bryce Baker, computer-aided engineering manager, says that, "We take the analog expertise we have and build it into software such as our Model Builder tool." Because cells designed for one application are often not appropriate for another, Gould is offering a generator approach that will let users capture a specification and then generate a physical layout that matches the spec. Users will have access to a menu with min/max

## Multi-level analog modeling speeds mixed-signal simulation



**W**ith the growing complexity of mixed analog-digital products, it's becoming increasingly difficult to simulate a complete system, board or subsystem on a chip. Simula-

tion run times for mixed-signal applications are simply becoming too long to be practical, especially if simulation is approached in traditional ways using transistor-level Spice simulations or even available mixed-signal simulators.

What can the designer do to work around the problem of excessive simulation times? The most direct approach is to utilize high-level models for the circuitry that can speed up simulation times by one, two and, in some cases, three orders of magnitude. In the digital world, this is already an accepted practice, with wide use of logic and register-level representations of the circuitry, and, more recently, high-level behavioral (or functional) descriptions in the form of a language such as Verilog or VHDL. As the modeling for a digital circuit block is moved up a level from, for example, transistor-level (Spice) to logic, or resistor-transistor logic (RTL) to behavioral language, there's a significant reduction in simulation time, but there's a comparable reduction in the accuracy of the simulation. If care is taken to choose the appropriate level of modeling, it's possible to get very usable predictions of circuit and system behavior without exceeding practical limits on simulation time.

Today's mixed-signal simulators are

generally constructed using two simulation engines, a logic simulation engine (for example, Verilog or Lsim) and an analog simulation engine (for example, Spice or Spectre). It's important to note that in a typical mixed-signal simulation, analog simulation times are usually more than 100 times longer than the logic simulation times, so they dominate the simulation time. This time difference holds true even in the common situation where 80 percent of the circuitry is logic and 20 percent is analog. The time difference will only worsen if there's a higher percentage of analog circuitry. As a result, in a mixed-signal simulation situation it's highly important to find ways to reduce the simulation time for the analog part of the circuitry.

### ■ Using high-level models

Just as for digital simulations, there's a direct approach to reducing analog simulation time: the analog portions of the mixed-signal circuit must be represented by high level models. There are three reasonably distinct levels of analog modeling available today: Spice transistor-level models; Spice-based analog macromodels (which are approximate circuit models for often-used blocks such as an op amp, comparator, voltage regulator or digital-to-analog converter); and models written in an analog behavioral language.

Compared to Spice transistor models, macromodels and analog behavioral language models offer about the same speed-up, typically a factor of about five to 10 times. But the speed-up can be as high as 50 to 100 times if the system behavior is reasonably insensitive to a

circuit's behavior, allowing the designer to use a relatively simple (very high level) model for that circuit block.

As an example, suppose you are designing a data-acquisition system, and you have two op amps in it: one for dc level translation and the other to act as an output amplifier for a fast-settling 12-bit D-A converter. The model for the dc level-shift op amp can be quite simple; it doesn't need accurate representations of, for example, input or output voltage limiting, current limiting, excess phase shift, or slew rate effects. A simple high-level model (in macromodel or language form) can be used to represent this op amp and can be expected to run about 100 times faster than the transistor-level equivalent. On the other hand, the op amp used for fast-settling to 12-bits should be modeled with much higher accuracy, and should be expected to have only the 5- to 10-fold speed-up over a transistor-level model.

For board-level designers using off-the-shelf analog parts, the models should be supplied by the manufacturers of their semiconductors. Only recently have manufacturers started to supply such analog models and they still have a long way to go to cover even the high-volume sellers in their data books. In the meantime, the system designer can get the broadest model libraries from today's EDA vendors such as Cadence, Mentor and Valid. And as for the inevitable missing models needed to complete a typical system simulation, designers will have to generate their own models, until the manufacturers respond.

**James E. Solomon**, president of the Analog Division, Cadence Design Systems

parameters.

For mixed-signal simulation, both Gould/AMI and NCR have included Saber/Cadat in customer toolsets. The Saber circuit and system simulator from Analogy (Beaverton, OR) and the Cadat digital simulator from Racal-Redac (Mahwah, NJ) are synchronized via the Calaveras timing algorithm. Because one simulator reaches a specific point in time before the other, the simulators appear to leapfrog, thus the name Calaveras, after the county in California that hosts the famous frog

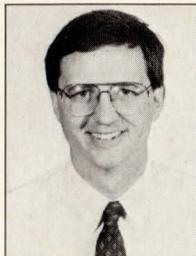
jumping contest. Analogy uses what it refers to as hypermodels to represent the analog operation of digital input/output pins.

Saber/Cadat supports models at behavioral, functional, gate, and switch levels for analog and digital, and at the primitive level for analog. All of Saber's models are written in Mast, Saber's analog behavioral language. According to Analogy, Mast is one of the languages being considered by the VHDL Users' Group committee, which is trying to tie an analog HDL to VHDL as an

extension.

A link between the Saber simulator and the Hewlett-Packard (Cupertino, CA) IC-CAP software for accurately characterizing user-defined analog models was recently announced by Analogy and HP. Analogy refers to the customer benefits of the link as a "prudent trade-off between model complexity and simulation speed." It happens too often that designers develop overly complex models that simulate poorly because they can not identify the critical design

**PCB simulation can help ASIC designers**



**S**ystem designers realize that the creation of a prototype board for complex printed circuit board designs is already a long and difficult process. The problem is magnified because ASICs are now "systems" which include both digital macrofunctions and analog functions. Simulation of the printed circuit board design before making a prototype is a powerful alternative that allows designers to improve the design and identify errors by performing worst-case analysis early in the design cycle, while the ASIC is still in development. Simulation will improve the first-pass success of the ASIC within the printed circuit board.

To achieve simulation of the printed circuit board including ASICs, designers require models for both the standard components and ASIC standard cells. The leading mixed-signal ASIC vendors now provide models for both analog and digital standard cell libraries for mixed-signal simulation.

The types of analog models determine the runtime, accuracy, and convergence of the mixed-signal simulation. The majority of vendors provide primitive models or macromodels of their analog standard cells. These models, however, may not be accurate, may not converge well (depending on the simulator), and have long runtimes for complex designs.

aspects of the model. With the Saber/IC-CAP link, once a new model is developed, customers can use IC-CAP to make measurements on the actual device and then invoke the new Saber model for the parameter-extraction process. IC-CAP ensures that both the measurement equipment and the Saber simulator run the same test.

**Don Cassidy, BSEE, Mixed-signal products manager, NCR**

■ **Digitize the analog?**

But even with a proven mixed-signal simulator like Saber/Cadat, users face the tough challenge of determining which portions of a design to model as analog and which

A less common approach is for the ASIC vendor to provide analog behavioral models in a primarily digital simulator. Such models typically have very fast runtimes and can achieve moderate accuracy. But there are problems with circuits containing local feedback, which is handled better by transistor and macromodeling approaches.

■ **Give designers what they need**

Providing customers with sets of models that offer tradeoffs of accuracy and runtime is a more effective approach. Fast simulation with approximate or unit-delay models are utilized to quickly verify design functionality; more detailed models are then used for accurate simulations. These can be accomplished utilizing an analog hardware description language that permits behavioral, macromodeling, and transistor techniques to be combined in a single model. Moreover, the analog HDL allows parameters to be passed into these models and device warning messages to be issued during simulation.

For example, NCR Microelectronics provides three models for the OA5001B operational amplifier in the VS1500 library. These analog models have been developed for Saber/Cadat and will also be available in Saber/Verilog using Analog's Mast analog HDL. The most detailed OA5001B model represents characteristics that accurately match worst-case characterized silicon. Another model provides approximate worst-case results and the third model provides ideal characteristics. A cus-

tommer may perform simulations with Saber using the most detailed models early in the design cycle to develop modules of the analog portion of the design. Then these modules are brought together into the mixed-signal design for very fast simulation of the complete design with the approximate and ideal simulation models. The particular model chosen is selected by simply changing a property on the schematic or with a command line option during netlisting for simulation.

One NCR customer recently performed mixed-signal simulation with Saber/Cadat of an ASIC that consisted of 6,000 digital gates and over 200 analog components. This very complex ASIC included a successive-approximation register A-D converter, 9 D-A converters, and 30 operational amplifiers. The simulations were performed using approximate worst-case models prior to fabrication and uncovered five design errors. The result was a first-pass functional success of a very complex ASIC.

Both users and semiconductor suppliers are beginning to utilize the advanced capabilities in today's mixed-technology, mixed-signal simulators. As the technology evolves, design groups will undoubtedly change their methodology to incorporate ASIC, printed circuit board, and full-system simulation to achieve better time-to-market with higher-quality products.

*Thanks to Mark Chadwick, Mixed-mode products manager, Analog.*

as digital. Should high-speed digital circuitry that exhibits analog behavior be modeled as analog? And if some analog is changed to digital to cut runtimes, will it retain the accuracy of analog? More than a few designers doing mixed-signal don't have the experience required to successfully resolve these conflicts.

Robert Bowman, president of ANAmation (Fairport, NY), claims that designers using the ANAsim mixed-signal simulator don't have to designate which portions of a design should be modeled as analog and which as digital. The simulator is based on research done at the Uni-

versity of Rochester. "The simulation happens implicitly, with the determining factor being the quality of the signal itself," says Bowman. Relaxation methods and event-driven methods have been integrated into ANAsim. In addition to analog models, a superset of Spice includes a model description for every logic element type in ECL, CMOS, and TTL. The user simply feeds the netlist to ANAsim and presents the system with a stimulus. A handful of major electronics manufacturers will begin beta testing the ANAsim simulator this month.

Rick Ross, CAD manager at Mo-

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# COMPUTER DESIGN

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## MIXED-SIGNAL TOOLS

torola's ASIC Division (Chandler, AZ) is not so sure he'd trust a simulator that solved the whether-to-simulate-as-analog-or-digital problem transparently. "Unless the simulator's given enough circuit design rules," says Ross, "it could designate a path as critical that you don't want to be a critical path."

Ross' group designs library elements, from small AND/OR gates to megacells, that can be embedded onto Motorola's BiCMOS H4C customer-defined arrays. The group has successfully integrated HSpice into Valid Logic Systems (San Jose, CA) Analog Workbench toolset. "The Analog Workbench was put together in such a way that, when you plug in a third-party tool like HSpice, the

system doesn't know the difference." For mixed-mode, Ross's group uses Mentor's Lsim simulator with the Adept algorithm for CMOS digital and plans to integrate HSpice into that simulation environment as well.

### More tools coming

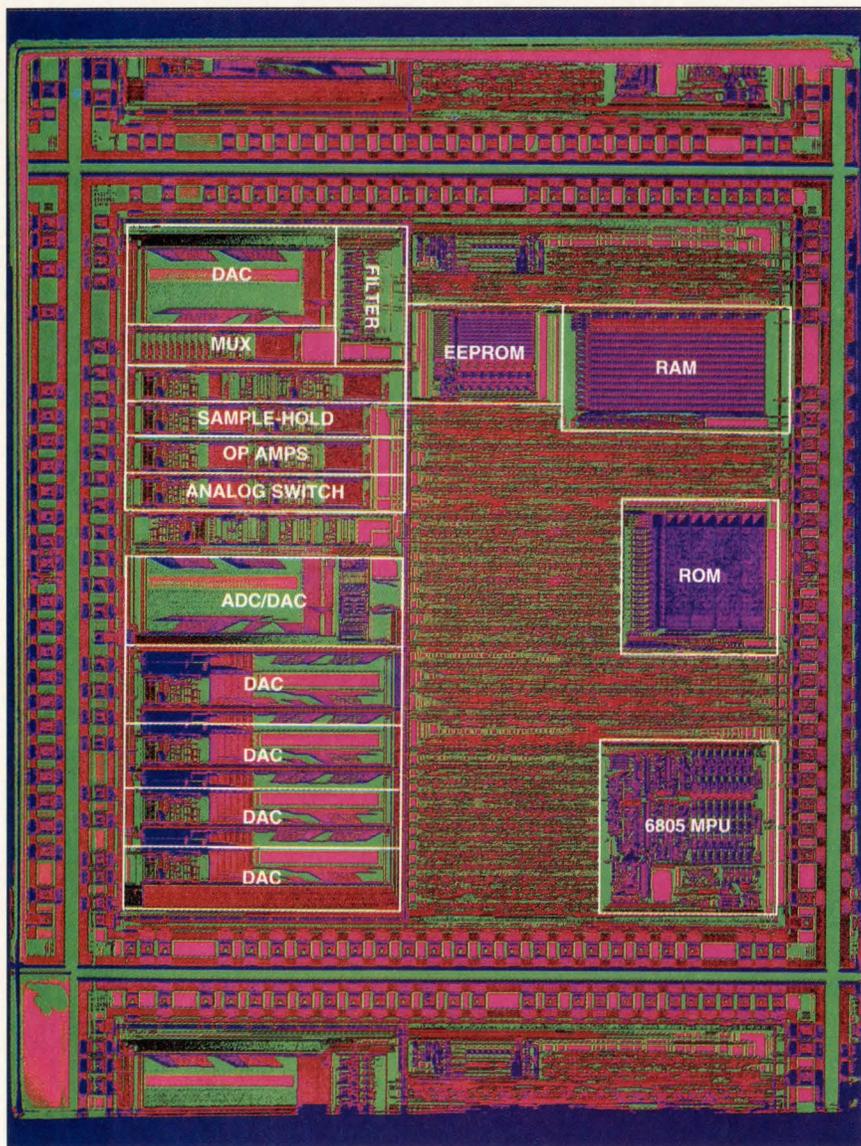
Valid is now working with several customers to develop its own mixed-signal, mixed-level simulation solution. In the meantime, the company has begun to ship its Profile behavioral analog solution and has introduced its top-down digital toolset, Logic Workbench TD. The simulation backplane that's part of the Logic Workbench is a key technology for the company's mixed A-D simula-

tion strategy, according to Dick Albright, Valid's CAE product marketing director.

Although Texas Instruments (Dallas, TX) does turnkey design for its customers, it's moving toward putting tools into customers' hands with its Flagship toolset (currently in beta site evaluation). TI has plugged its own version of Spice into Mentor's Lsim, which supports Mentor's M behavioral language and VHDL. Lsim acts as a simulation manager, tying together a number of simulators, including Saber. Paul Koch, LinASIC program manager, reports that TI will use this mixed-signal solution for the next generation of DRAMs. Because DRAM cells comprise a transistor and capacitor pair exhibiting primarily analog characteristics, they must be accurately modeled to predict memory device behavior.

Harris Semiconductor (Melbourne, FL) has been using its Fastrack design system internally for mixed-signal design as well as offering it to users. Director of design systems, Nick English says that, "Fastrack can take IC designers and change them into system designers, but they've got to be experienced in analog design." For mixed-signal simulation, Harris uses a Cadence version of Spice (part of the Analog Artist toolset) interfaced to Verilog. English says that Harris will switch to Cadence's Spectre advanced circuit simulator at a later date. According to Cadence, Spectre can handle designs with more than 50,000 transistors up to 10 times faster with equal or better accuracy than existing simulators.

Harris has very recently enhanced its toolset for customers designing with its mixed-signal libraries. Mixed-Signal Fastrack (MSF) now includes two more Harris-developed simulation algorithms that link to Cadence's new version of Spice, called cdsSpice, via subroutine calls. Harris customers now have access to the Switched Capacitor Analysis tool (Scan) for high-level simulation of switched-capacitor circuits, and the Automated Synthesis of Integrated Macro/Behavioral Models (ASIM) tool for simulating analog-intensive mixed-signal designs. Within MSF's mixed-signal simulator, the user selects a simulation algorithm for each block based on speed/accuracy tradeoffs. According to Harris, any combination of simulation algorithms and



*This mixed-signal 1.5- $\mu$ m CMOS cell-based ASIC, designed by NCR for Catelco A/S Denmark for a telecommunications application, is typical of designs that will benefit from Saber/Cadat.*

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## Sizing up silicon vendors



**A**pplication-specific mixed-signal cell-based IC design projects are most successful when the process technology and cell libraries meet the application require-

ments. Planning a mixed-signal project requires careful appraisal of the match between the customer's requirements and a supplier's capabilities.

The supplier's production capabilities, including process and packaging technologies, are obviously the first areas to evaluate. In addition to the basic capabilities, a supplier offering application-specific cells which provide proven compliance with application standards can decrease a user's time-to-market.

The supplier's development support must also be weighed. Cell libraries, design tools, design methodology, and engineering support are all important ingredients. These reduce the design risk, engineering effort, and cycle time associated with mixed-signal IC development.

### ■ Process technology

The capabilities of a process technology can be summarized by four things: the type of circuit components it allows, the performance of these components, their size, and the means available for interconnecting them. No single process technology meets the requirements of all applications, so suppliers may offer more than one.

Texas Instruments supports three primary technologies for designing application-specific mixed-signal ICs. Each is a modular technology, meaning that each has a basic range of electrical components and optional extensions to

meet application-specific requirements. Process modularity allows the product development team to make process complexity and cost trade-offs to meet design requirements. For example, our LinBiCMOS technology supports 15-V bipolar transistors with an  $f_T$  of 750 MHz. There are process options, however, which can extend the transistor performance to an  $f_T$  of 2,500 MHz or an operating voltage of 30 V. A similar option extends the range of the CMOS transistors from 15 to 30 V. Our 1- $\mu$ m LinEPIC technology is based on the same technology we use for our digital standard cells and several graphics and digital signal processors. These process extensions support the high precision resistors and capacitors needed in data converters and switched capacitor filters.

### ■ Cells and libraries

A collection of reusable cells is a cell series. The electronic representation of those cells is the cell library. One cell series may have multiple libraries, one for each supported workstation. The availability of a cell series reduces the effort required to complete a design and reduces design risk.

The logic cells supported in a process are the most frequently reused. An increasing number of customers participate in the design of the digital portion of mixed-signal ICs. Logic cell libraries for mixed-signal applications require both logic models and circuit descriptions. Some process technologies feature multiple applications-oriented logic series. For example, LinBiCMOS supports three logic series. One is designed for performance, another for functional density and low speed, and the third for higher operating voltage. Compatibility with familiar cell libraries is also important.

A basic set of general-purpose analog cells is beneficial because they may be usable directly from the library to meet application requirements. They also give users a means to evaluate the ability of a process technology to meet system requirements. Finally, they provide a starting point for the rapid development of new cells.

Cells which are designed for use in a single application or closely related set of applications are application-specific cells. A cell's differentiated performance in the application lowers design risk. The faster cycle times associated with these cells cut development time. This is particularly true where industry standards are part of the application's requirement.

TI's mixed-signal libraries contain several application-specific cells. In LinBiCMOS, we have worked with Digital Equipment Corp to develop a set of standard Ethernet interface cells. In the LinEPIC technology, we have worked with leading workstation, PC and telecom companies to design application-specific data conversion cells for high performance graphics, audio processing and digital communications. Typical applications combine these cells with 10,000 gates of logic from our 1- $\mu$ m ASIC logic library.

We have developed a cell especially for a hand-held video camera. We have also developed application-specific cells for hard disk drive and automotive applications.

Process technology and cell libraries play important roles in selecting a mixed-signal vendor and meeting high performance mixed-signal IC design objectives. Careful evaluation and selection will result in an IC development project yielding a competitive advantage and faster time-to-market.

**Delbert Whitaker**, senior vice president, Semiconductor Group, Texas Instruments

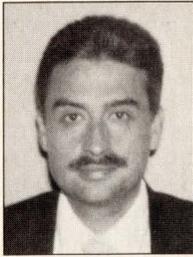
any number of blocks are allowable within one simulation run. With Scan and ASIM, a set of time-stepping algorithms links the simulators so that there is "continuous" input and output between simulation engines, claims Harris.

Simulating mixed-signal designs that go into multichip modules (MCMs) at a system level is still in the experimental stage. Neverthe-

less, it's inevitable that a good number of complex mixed-signal designs will go into MCMs because production volumes won't always justify the costs of single-wafer designs. Ed Shi, Head of the Design Automation Group at Hughes Aircraft (Newport Beach, CA), believes that, "System-level simulation is a big question mark for MCMs. They're larger, more complex, and thus more diffi-

cult to simulate than a single chip." From a simulation standpoint, it makes sense to treat a mixed-signal MCM like a big board, Shi says. His group recently used Mentor's Hybrid Station (Mentor has since introduced a more sophisticated toolset for MCMs called MCM Station) to design a seven-layer 2-x 4-in. mixed-signal module on polyimide dielectric for a space application. Because

## Test issues in mixed-signal ASICs



In the early eighties, test was a major barrier to the commercial acceptance of digital ASIC technology. Test program generation and debugging were the critical path limiters for design turns. Today, mixed-signal ASIC technology faces the same hurdle. For mixed-signal to follow a growth path similar to its digital counterpart, it must overcome a much more complicated set of test issues. Only after test issues are solved will cycle times, development costs and ultimately, product-to-market times decrease.

Design considerations related to mixed digital and analog on a single substrate include cross talk, subtle parasitics, and thermal interaction issues. Tied to these are the requirements for properly designed libraries and mixed-signal design capability. Digital simulators based upon well-defined threshold levels and on/off output states don't work with the continuously variable functions found in analog design. Parametrized, easy-to-use functions like op amps and current sources are important core functions which can be placed in design libraries to aid in the design process.

The final piece of the puzzle is a well-defined test methodology. Although digital ASIC test is certainly not trivial, true mixed-signal applications require attention to issues raised by the inclusion of analog circuitry.

Harris is addressing this problem by placing the test-creation activities concurrent with the design process. Test considerations need to be understood

and dealt with early in the process to avoid long debug cycles in production.

The degree of mixed-signal test impact depends on the type of mixed-signal circuit under consideration. Mixed-signal circuits optimized for digital are a short step removed from classic digital ASICs, with analog functionality limited to a few rudimentary comparators or op amps serving as output interfaces. For these all-CMOS circuits, 95 percent of the test program is automated, while test creation for the analog circuitry (the remaining 5 percent) is primarily manual.

### More analog, harder to test

Mixed ASICs optimized for either analog or power face more severe test-creation and validation issues. Circuits optimized for analog require high-performance analog components for low offsets (2mV) and high-gain bandwidths (from greater than 300 MHz to the GHz range). For these circuits, which may combine less than 5,000 gates of CMOS logic with analog via bipolar (NPN/PNP structures) at operating voltages greater than five volts, no automatic test stimuli or control program is available at present.

Mixed-signal circuits optimized for power (intelligent power), primarily Bi-CMOS analog ICs with either P or N DMOS devices for power, address applications requiring more than 50V or 2 amps or more than 2 watts. These circuits face the most-severe test challenges: bussing, high voltage, high current-induced crosstalk, and the subtleties of circuit and tester environment induced parasitics.

Software, hardware, and automatic test equipment form the test triumvirate. Digital test vectors are only a por-

tion of the inputs required to generate code. Definition of analog stimuli, control, and response are the real issues. This becomes acute in mixed signal devices that are optimized for analog/power. Harris is working in this area by expanding its Fastrack design system in the test areas through joint development with Cadence and three test equipment manufacturers. This included simulating the actual tester environment of Hewlett-Packard test equipment. The test validation prior to silicon was facilitated using ATE models derived by Hewlett-Packard. The ability to simulate the device, the hardware interface, and the tester early in the design process forms the foundation of a capability that can reduce time-to-market significantly.

The ultimate goal is a framework which includes rapid automatic mixed signal test program development. None of this is possible without a strong working relationship between IC manufacturers, CAD developers, ATE suppliers, and universities (University of California at Berkeley, Carnegie Mellon and the University of Texas). Although the complete solution is still in development, it's critical that the industry continue to make investments in the test areas to improve customer service. The universities, in particular are working to define the concepts that hopefully will create an accepted approach for analog and mixed signal testability (such as, failure modes, fault models, analysis methodologies and tools). Those vendors willing to make the investments necessary to drive down NREs (nonrecurring engineering expenses) and product-to-market cycles are the ones that will survive through the nineties and beyond.

**Dean F. Henderson**, Director of Strategic Marketing, Intelligent Power Products, Harris Semiconductor

the module contained numerous high-precision analog components, Hughes designers had to add an extra power and ground plane to maintain signal integrity and minimize noise.

### Layout requires experience

Though no mixed-signal simulator satisfies engineers at Exar (San Jose, CA), vice president of engineering and marketing, Ilhan

Refioglu, says that simulation is not the limiting factor when it comes to customer-designed mixed-signal projects. "Laying the design out with all those nitty-gritty details is what will make or break you," he says. "There are no guidelines to substitute for years of experience." Exar, which has upgraded its mixed-signal technology from array-based to cell-based for flexibility and performance, does 90 percent of its

designs on a custom basis with the other 10 percent done at customer sites or designed jointly with customers at Exar design centers. Exar combines analog and digital with memory storage in BiCMOS. Target applications include automotive, industrial, medical, and consumer.

As for putting tools into customers' hands, Refioglu explains that, "We're trying to break the ice, but design in the analog world is still an

## MIXED-SIGNAL TOOLS

art. Expecting customers to know how to partition a circuit, how to run ground lines, how to handle crosstalk and jitter is putting a burden on their shoulders. We have to walk before we run and build up the customers' expertise."

Laying out handcrafted analog cells and blocks is "never really a problem if you have a good netlist-driven layout editor and router," according to Tom Palomino, physical design manager at Level One (Folsom, CA). A Valid user, Palomino designs analog-intensive CMOS

cause analog is still custom," says Babka, "blocks are of varying sizes, and we have to preplace large blocks." Babka also reports that it's critical to isolate some lines. "After floorplanning, we have to do point-to-point routing before autorouting." Babka's group uses the SCII of Silver-Lisco (Sunnyvale, CA), the two-layer-metal version of the SL-Cell layout system for placing and routing analog and digital cells and blocks, as well as Cadence's Edge block place-and-route software. "There's room for improvement in

generation applications such as medical imaging.

### Test is the real nightmare

If modeling, simulation, and layout are bogey-men for mixed-signal designers, test is a real monster. Alan Morton, applications manager for Silicon Systems (Tustin, CA) says, "It would be an absolute disaster putting mixed-signal designs through test if tools were put into users' hands. There'd be a really serious efficiency problem with regard to the factory." Silicon Systems, which uses mixed-signal ASIC technology in its products, addresses the customer-involvement issue by selecting an extremely small number of customers to participate in what it refers to as the Key Account Design System (KADS) program. Only modem-maker Hayes and two other customers participate in the KADS program and design with Silicon Systems' tools at their own sites.

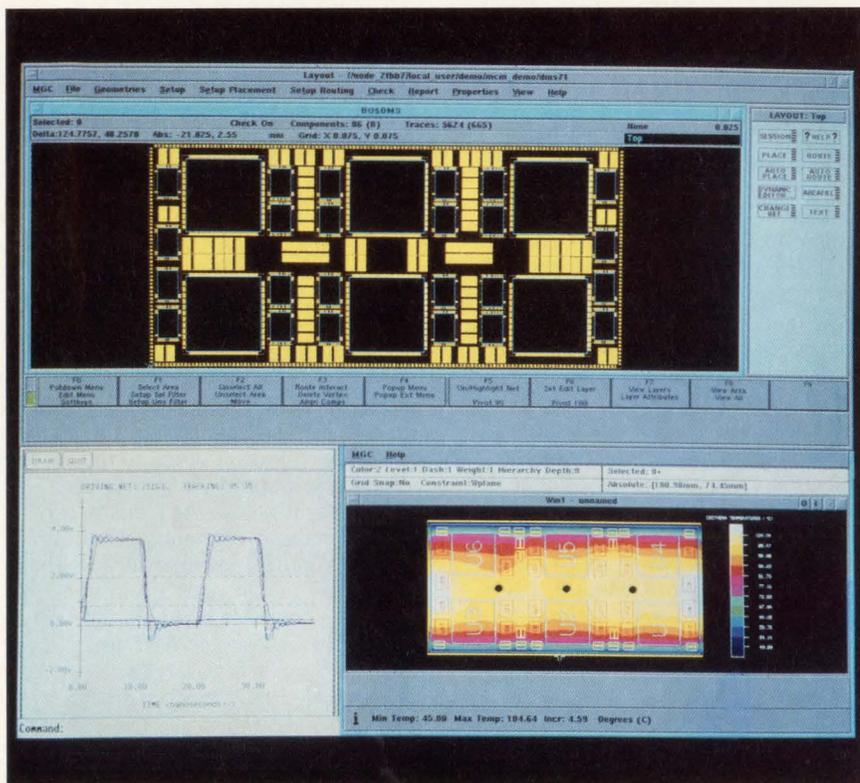
On designing for testability, Harris' Nick English says, "It's not even as if people understand the problem of mixed-signal test and don't know how to solve it. We don't even have the concepts yet."

According to English, Harris is working with Cadence, Teradyne, LTX, and Hewlett-Packard on analog and mixed-signal test creation. "Everyone understands design capture, now we're talking about test capture." English says that mixed-signal designers need very accurate simulation models of tester resources so that designs can be simulated in the same environment they'll see when they get to the test floor.

### Model tester resources

James Spoto, vice president of R & D at Cadence's Analog Division, says that the intent behind this push to verify the test configuration within the design environment will mean more design-for-test work for the designer. "But the designer will be ensured that the device under test will work within the test head and not just in an ideal environment," says Spoto. "We're still in the concept phase with partners. There are no release dates yet," Spoto reports.

Bruce Webster, manager of A500 systems applications engineering at Teradyne (Boston, MA), says that it takes a collective triumvirate of silicon, EDA, and automatic test equipment vendors to attack a prob-



This Mentor Graphics screen shows a mixed-signal multichip module (MCM) in design at Hughes Aircraft. The top window shows placement of the die on the MCM substrate. The bottom right window shows a thermal map of the module, and at bottom left is a view of high-speed analysis.

parts for T1 and local area network applications.

"I can crank out mixed-signal designs pretty quickly with Valid's Construct layout editor and Compose auto place and route software," Palomino says. Compose is able to route all power supplies, according to Palomino. "I can bring designs to 99 percent completion within layout. The tools are getting better and better, but you never really have all you need."

Cardiac Pacemakers' Babka reports the need for a great deal of interaction with layout tools. "Be-

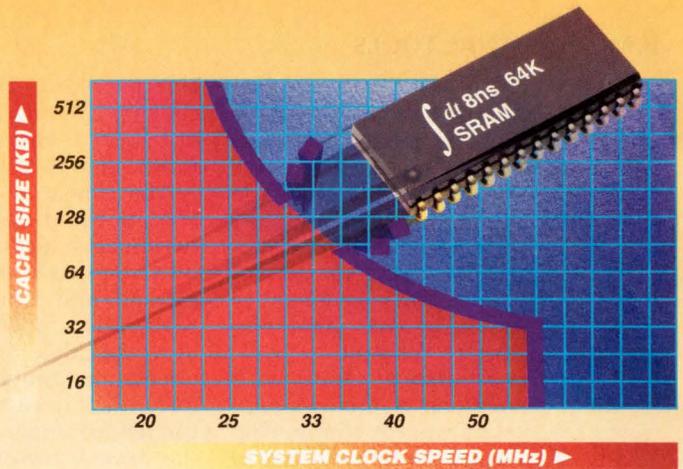
both," she says.

Problems involved in laying out mixed-signal designs naturally multiply for designs that go into MCMs. Giora Goldberg, vice president of Sciteq Electronics (San Diego, CA), reports that a Sciteq MCM with GaAs D-A converter, ALU, and memory on a ceramic substrate went through three layout iterations, incurring three NREs (non-recurring engineering expense). Sciteq sent specifications for the MCM to Triquint which did a turn-key custom design. Sciteq-developed MCMs are targeted at signal

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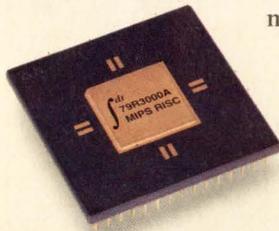
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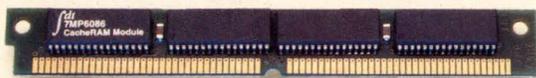
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## MIXED-SIGNAL TOOLS

lem like analog and digital testing. Webster reports that Teradyne is developing specific models with Cadence. "Cadence wants to give users the ability to draw a sketch of the test they want, and then add test instrumentation models from a separate palette of library elements." The maintenance and responsibility for libraries will lie with ATE vendors, according to Webster.

Teradyne is also working with Analog Devices on a mixed-signal test project that aims at eliminating many of the unknowns involved in the performance of a mixed-signal ASIC in the test environment. As the result of a joint engineering project, Analog and Teradyne have linked Analog's Spectrum mixed-signal simulator with Teradyne's Image test simulator, which is used on Teradyne's A500 family of analog VLSI test systems.

### Mixing simulators a problem

Michael McGonigle, technical operations manager for the Systems IC Products Division of Analog Devices, says that, "Integrating different simulators is a much harder proposition in the mixed-signal world because of the analog part of

the problem. But we're already seeing the payback in terms of shorter development cycles for mixed-signal ASICs."

The Image test simulator uses a special event-description language to convert a test program simulation into a series of discrete, tersely described and time-stamped events. Since the Image-generated events describe ideal state changes, the Spectrum simulator has to apply information from detailed models of the device under test and models of the target tester's instruments to bring the simulator's ideal test events into line with reality.

Webster says the ability of the tester simulator to hook into Analog's mixed-signal simulator allows designers to look at all implications at the pins of a device and within the device as well. The diagnosis of mixed-signal testability problems will probably be more automated in the future, according to Webster, but "stepping through a software simulation file to find problems during design is far easier and more economical than waiting until the fabricated device meets the tester to start debugging." ■

## Postscript

*If you're an analog IC designer doing mixed-signal, you have at least half a chance of putting your hands on a toolset that will help you achieve first-pass silicon success at your own site. But if you're a PC-board or digital designer hoping to find tools that substitute for analog IC expertise, hold on to that hope. And at the same time, hold on to your favorite fab for custom turnkey service, at least for the analog portion of your design.*

*Why can only good analog IC designers use today's tools? Because mixed-signal methodologies are so varied and in such a state of flux that it takes an expert to even define the analog problem well enough to knowledgeably explore possible solutions.*

*And what of the future? I don't think it's too much to expect that analog expertise will eventually be resident in design tools. If the R&D efforts underway at universities like Carnegie Mellon, Berkeley and the University of Rochester are on target, I expect we'll have tools a few years from now that will solve many of today's library, modeling and simulation problems. If academia's efforts collapse, silicon vendors will have to invest heavily in R&D to build these tools for their customers, because no vendor will have the facilities to accommodate the growing numbers of mixed-signal designs on a custom basis.*

*Barbara Tuck*



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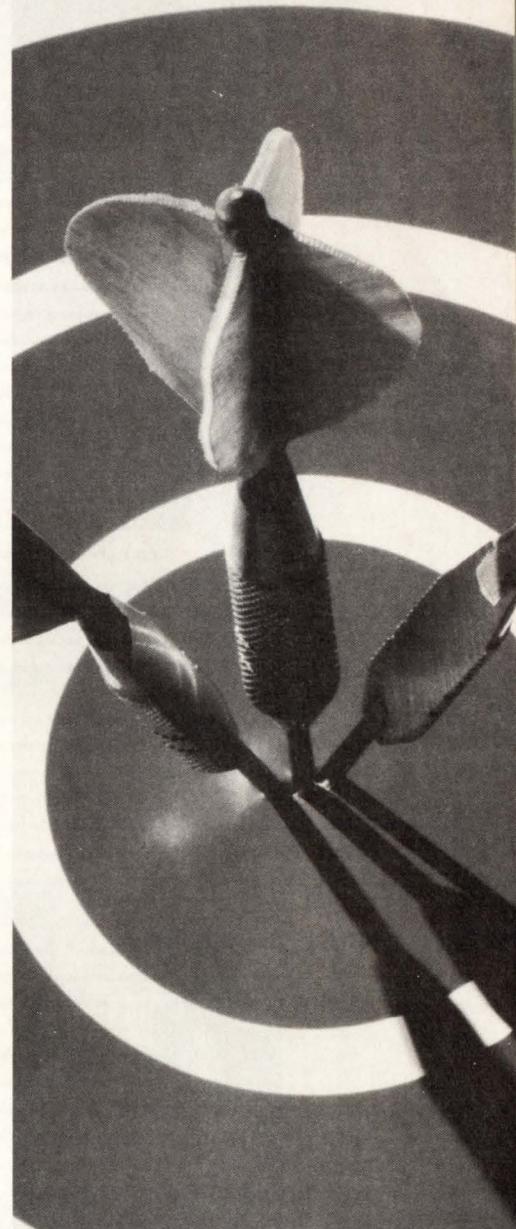
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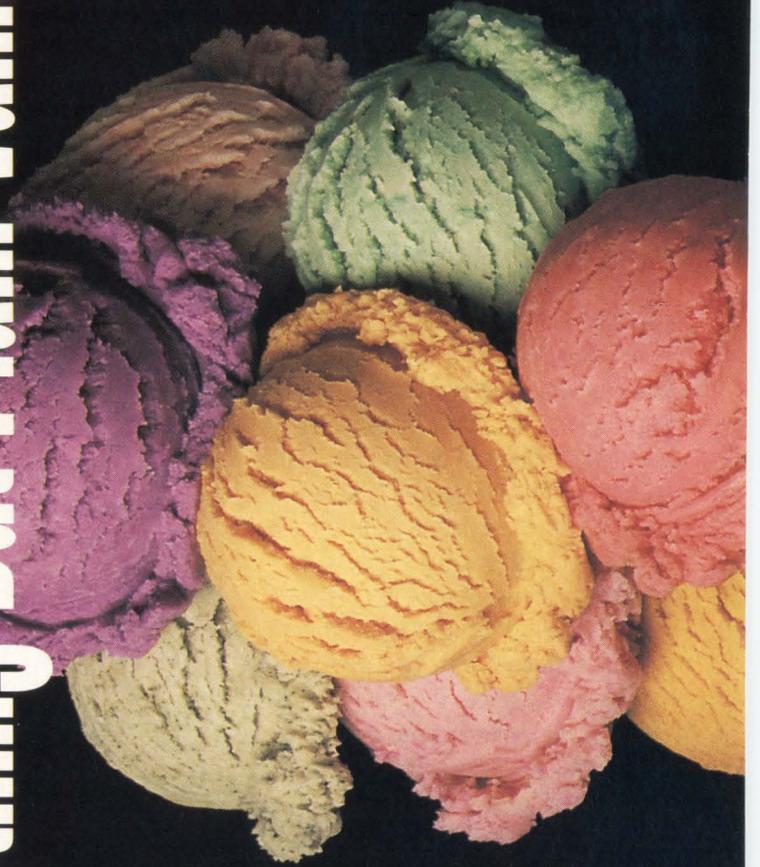
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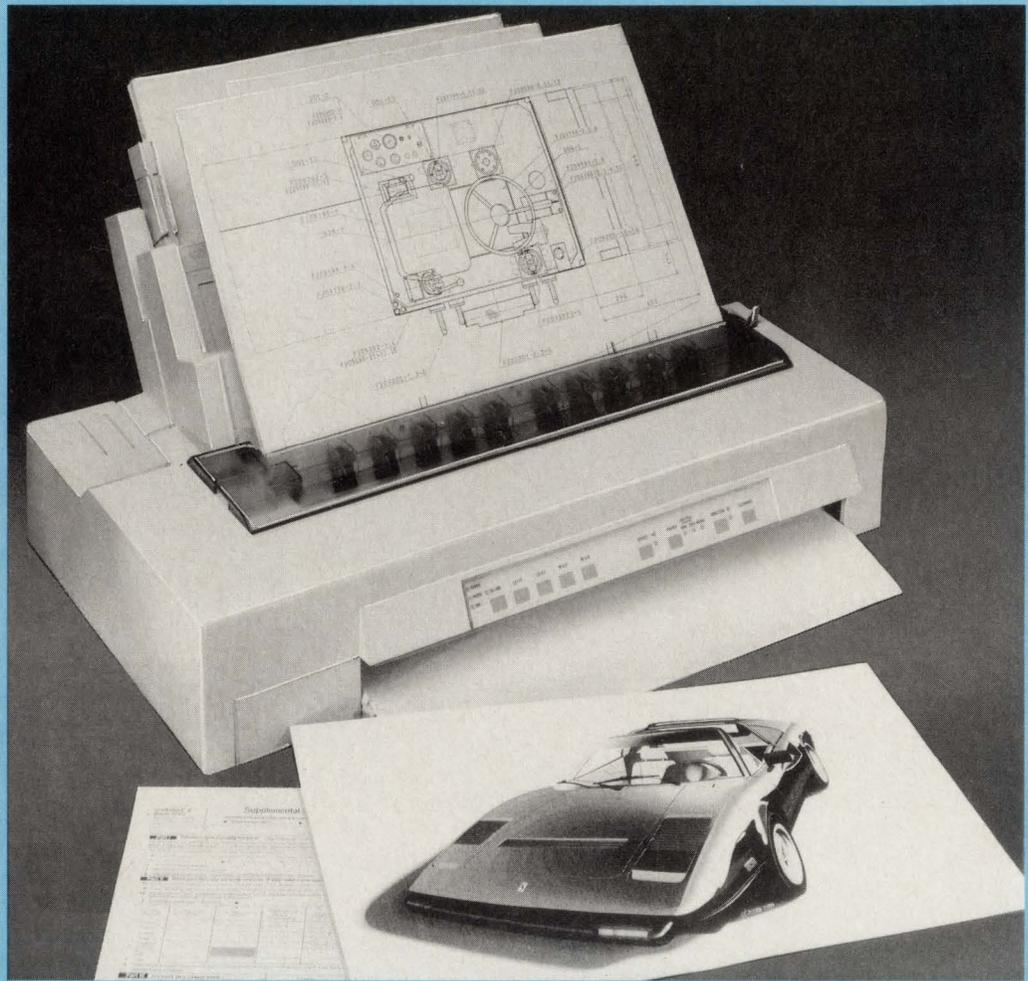
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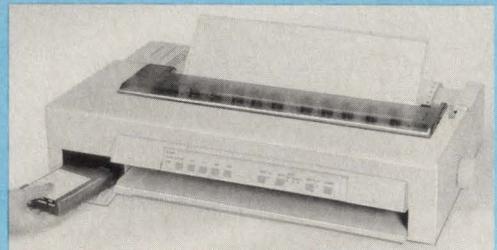
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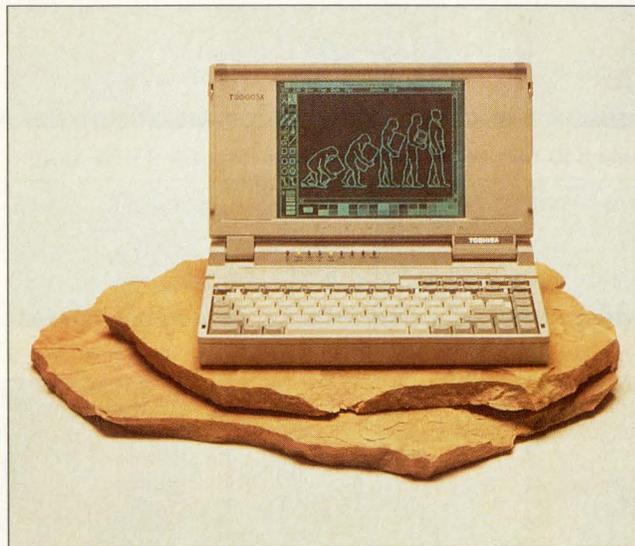
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Line-feed Speed:	40 ms/line		
Line-feed Pitch:	Min. n/360 in. (n = programmable)		
Paper Handling:	Plain paper; cut sheet (5.8 -14.3 in. wide ASF, 3.5 -17.0 in. wide manual feed), fanfold (4.0 -16.0 in. wide), envelope, transparency		
Paper Weight:	14 - 33 lbs. (cut sheet manual), 16 - 23 lbs. (cut sheet ASF), 14 - 23 lbs. (fanfold)		



Automatic capping and an encapsulated ink cartridge make the Canon P-670 virtually maintenance free.

INTEGRATED CIRCUITS

**Low-power DRAMs stretch battery life in portable systems**



*Laptop, notebook, and other battery-powered portable systems are driving the need for DRAMs that consume less power. This notebook uses Toshiba TC14800A DRAMs for its main memory. These DRAMs have a self-refresh capability which lets them refresh themselves only when needed.*

There was once only one significant trend in DRAM technology—every few years their storage capacity expanded. Today, driven by technology evolutions, competitive pressures, and demands from laptop and notebook computer designers, DRAM vendors are now offering products to meet specialized needs.

As each new generation of systems routinely appears with larger complements of DRAM-based system memory than its predecessors, power consumption has moved nearer to the top of the designer's list of concerns.

In the normal mode of operation power required by system memory, almost entirely drawn during the DRAM refresh cycle, represents a significant amount of the total power used in a system. In the standby power mode offered by many portable computer systems, DRAM-based memory becomes the largest user of power. And the need for lower-power DRAM devices isn't confined to laptop and notebook computers; it's a major concern for most battery-powered computer-based products.

**Please standby...**

Because the length of battery life is becoming a major selling point in battery-powered systems, designers are doing everything they can to avoid wasting power. One result is that many portable computers provide a low-power "standby" mode that disables certain power-hungry peripherals and other devices. Disabling a display, for example, when it's

not being used can save perhaps a third of the active system power. And turning off power to the disk drives when they're not being used may reduce system power by another third. To extend battery life still further, some portable systems also have a "suspend" or "sleep" mode. Critical system status data is copied to low-power DRAM, the CPU is disabled, and all clocks are stopped. System power remains enabled, refreshing the DRAM at less-frequent intervals.

***In the standby power mode offered by many portable computer systems, DRAM-based memory becomes the largest user of power.***



When a laptop or notebook computer is in full operation, the display and the disk drives draw more power than main memory. However, in standby mode the DRAM-based main memory draws the most power. And in sleep mode the DRAMs are practically the only devices that are drawing power.

To meet these requirements, DRAM vendors are offering parts with extended refresh intervals, battery-backup modes, and even self-refresh capabilities. Several

vendors have designed DRAMs specifically for low-power use and some of these are available now (or will be within the next year). To meet immediate needs, however, most DRAM vendors are selecting low-power devices from their standard DRAM lines.

**Selecting for low power**

Traditionally, low power has meant extended refresh time. By stretching out the refresh cycles, the power drain can be reduced. With this in mind, DRAM vendors are testing DRAMs from their standard product lines to find devices that have a high data-retention capacity and, therefore, don't need to be refreshed as often. "A capacitor in a DRAM cell is typically designed with a large engineering margin," says Gene Cloud, vice president of semiconductor marketing at Micron Technology (Boise, ID). "That capacitor can be tested for a much longer refresh specification than is guaranteed in a normal power data sheet."

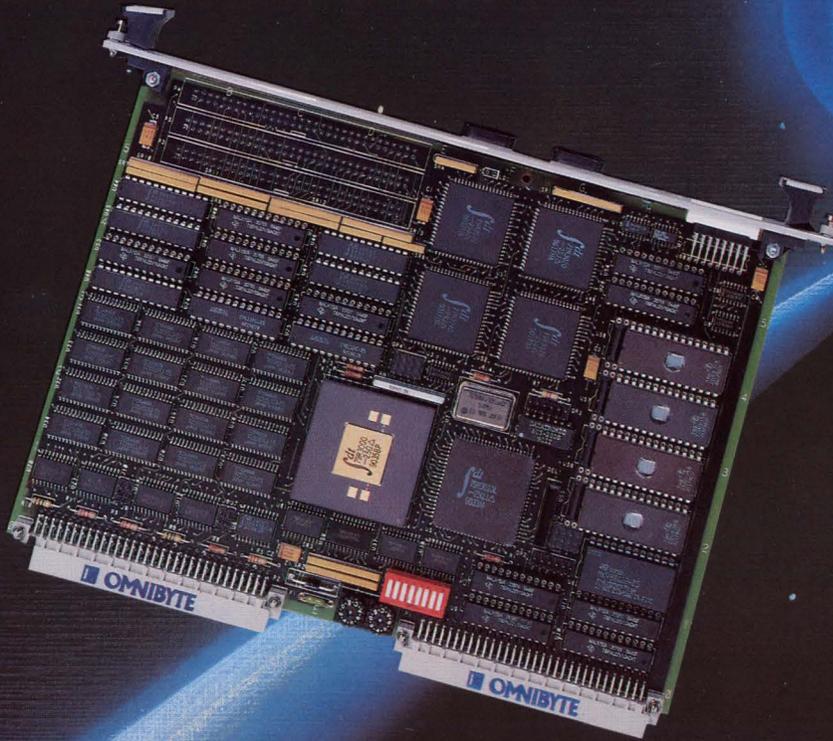
Selecting a part for low power is a matter of spending the time to test for that extended refresh specification. The trade-off is the added costs due to the extra test time. "In crude terms, it takes eight times longer to test a part in such a way because you have to guarantee a refresh that's extended by a factor of eight," says Cloud.

There are a number of advantages in selecting standard parts for extended refresh. For instance, such selection means low-power parts are

■ PRODUCT FOCUS/Low power DRAMs

Model	Organization (bits)	Access time (ns)	Power dissipation (active/inactive in mW)	Refresh interval (ms)	Battery back-up current ( $\mu$ A)	Modes	Availability	Price	Comments
<b>Fujitsu Microelectronics, IC Div</b> 3545 N First St, San Jose, CA 95134 (800) 642-7616 <b>Circle 301</b>									
MB814100-80L	4 Mx1	80	413/8.25	128	250	fast page	now	\$19.50	TSOP II package
MB814101-80L	4 Mx1	80	413/8.25	128	250	nibble	now	\$19.50	same as above
MB814400-80L	1 Mx4	80	413/8.25	128	250	fast page	now	\$19.50	same as above
<b>Hitachi America, Semiconductor &amp; IC Div</b> 2000 Sierra Point Pkwy, Brisbane, CA 94005 (800) 448-2244 <b>Circle 302</b>									
HM574100/400	4 Mx1 or 1 Mx4	35 40 45	170/5 150/5 130/5	8	—	static column	Q491	—	self refreshing
HM514100A/400A	4 Mx1 or 1 Mx1	60 70 80	110/2 100/2 90/2	16, 128, or 256	150	fast page nibble static column write per bit	—	\$27.19	ZIP and TSOP I & II packages available
HM514100L/400L	4 Mx1 or 1 Mx4	80	90/2	16	—	fast page nibble write per bit	now	\$27.19	—
HM514800/900	512 kx8 or 512 kx9	70 80	110/2 100/2	128	300	fast page	now	\$29.33-\$38.12	—
HM514170	256 kx16	70 80	140/2 120/2	16	—	—	now	\$38.66	—
HM514190	256 kx18	70 80	140/2 120/2	16	—	—	now	\$41	—
<b>Micron Technology</b> 2805 E Columbia Rd, Boise, ID 83706-9698 (208) 386-3900 <b>Circle 303</b>									
MT4C1004L	4 Mx1	60, 70, 80	225/3	16 or 128	600	fast page static column	4Q91	\$18	—
MT4C4001L	1 Mx4	60, 70, 80	225/3	16 or 128	600	fast page static column write per bit quad CAS	4Q91	\$19	—
MT4C16256L	256 kx16	60, 70, 80	350/3	8 or 64	300	fast page static column	2Q92	\$22	—
<b>Mitsubishi Electronics America</b> 1050 E Arques Ave, Sunnyvale, CA 94086 (408) 730-5900 <b>Circle 304</b>									
M5M44100	4 Mx1	70, 80	413/5.5	128	200	fast page nibble static column	now	\$26	—
M5M44400	1 Mx4	70, 80	413/5.5	128	200	fast page static column write per bit	now	\$26	—
M5M44800	512 kx8	70, 80	490/5.5	128	250	fast page	now	\$30	—
M5M44170	256 kx16	70, 80	578/5.5	128	250	fast page	now	\$30	—
<b>Motorola Semiconductor, DRAM Operations</b> 3501 Ed Bluestein Blvd, Austin, TX 78735 (512) 928-7343 <b>Circle 305</b>									
MCM514100	1 Mx4	60 70 80	660/1.1 550/1.1 468/1.1	128	—	fast page static column write per bit	now	—	SOJ and ZIP packages available
MCM514400	4 Mx1	60 70 80	660/1.1 550/1.1 468/1.1	128	—	fast page nibble static column	now	—	same as above

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SPP <sup>1</sup>	SPP/e with architecture & cache simulator
IDT/c <sup>2</sup>	IBM/SUN X-compiler
C EXECUTIVE <sup>3</sup>	Real time monitor
ADA <sup>4</sup>	ADA compiler
VxWorks <sup>5</sup>	Real time o.s.
RISC/os <sup>1</sup>	UNIX <sup>6</sup>

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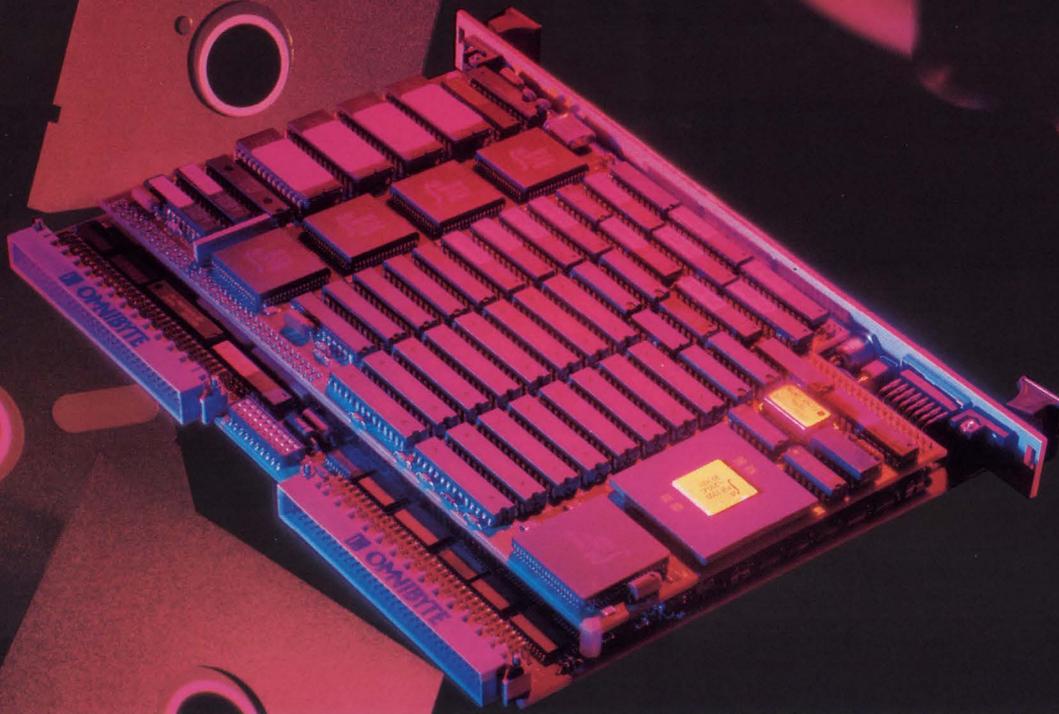
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- 32, 16, 8 or 4MB of DRAM
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And you can get the following software with the VR3000:

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SPP/e <sup>1</sup>	PROM monitor & debugger
SPP <sup>1</sup>	SPP/e plus architecture & cache simulator
IDT/c <sup>2</sup>	IBM/SUN X-compiler
C EXECUTIVE <sup>3</sup>	Real time monitor
ADA <sup>4</sup>	ADA compiler
VxWorks <sup>5</sup>	Real Time o.s.
RISC/os <sup>1</sup>	UNIX <sup>6</sup>

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Model	Organization (bits)	Access time (ns)	Power dissipation (active/inactive in mW)	Refresh interval (ms)	Battery back-up current ( $\mu$ A)	Modes	Availability	Price	Comments
<b>NEC Electronics</b> 401 Ellis St, PO Box 7241, Mountain View, CA 94039 (415) 960-6000 <b>Circle 306</b>									
424100-60/70/80	4 Mx1	60 70 80	660/11 550/11 495/11	16	300	fast page	now	\$17.75-\$19.50	—
<b>Oki Semiconductor</b> 785 N Mary Ave, Sunnyvale, CA 94086-2909 (408) 720-1900 <b>Circle 307</b>									
MSM514100AL/400AL	4 Mx1 or 1 Mx4	70 80	495/1.1 440/1.1	128	300	fast page static column	now	—	—
<b>Panasonic Industrial</b> Two Panasonic Way, Secaucus, NJ 07094 (201) 392-4819 <b>Circle 308</b>									
MN424100A	4 Mx1	70 80	550/5.5 495/5.5	—	—	fast page	now	—	SOJ, ZIP and TSOP I & II packages available
MN424400A	1 Mx4	70 80	550/5.5 495/5.5	—	—	fast page	now	—	same as above
<b>Samsung Semiconductor</b> 3725 N First St, San Jose, CA 95134 (408) 954-7229 <b>Circle 309</b>									
KM44C1000ASL/4000ASL	1 Mx4 or 4 Mx1	70 80	578/0.6 523/0.6	256	150	fast page	now	\$20	—
<b>Sharp</b> 5700 NW Pacific Rim Blvd, Suite 20, Camas, WA 98607 (206) 834-2500 <b>Circle 310</b>									
LH64400	1 Mx4	80	495/5.5	16	10	fast page	now	\$35	DIP, SOJ and ZIP packages available
<b>Texas Instruments, Semiconductor Group</b> PO Box 809066, Dallas, TX 75380 (800) 336-5236 <b>Circle 311</b>									
TMS44100L	4 Mx1	60 70 80	523/1.1 468/1.1 413/1.1	128	300	fast page	now	\$25	—
TMS44400L	1 Mx4	60 70 80	523/1.1 468/1.1 413/1.1	128	300	fast page	now	\$25	—
TMS44800L	512 kx8	60 70 80	660/1.1 605/1.1 550/1.1	128	300	fast page	3Q91	—	—
TMS44800S	512 kx8	60 70 80	660/1.1 605/1.1 550/1.1	16	—	fast page	3Q91	—	self refreshing
TMS45160L/65L	256 kx16	70 80	880/1.1 770/1.1	64	—	fast page	3Q91	—	—
TMS45160S/65S	256 kx16	70 80	880/1.1 770/1.1	8	—	fast page	3Q91	—	self refreshing
<b>Toshiba America Electronic Components</b> 9775 Toledo Way, Irvine, CA 92718 (714) 455-2000 <b>Circle 312</b>									
TC514100A/400A	4 Mx1 or 1 Mx4	60 70 80	660/1.1 550/1.1 468/1.1	128	300	fast page	now	\$23	—
TC14800A	512 kx8	70 80	578/1.1 495/1.1	128	300	fast page	now	\$26.50	self refresh version available
TC514900A	512 kx9	70 80	633/1.1 550/1.1	128	300	fast page	4Q91	\$30	self refresh version available
<b>Vitellic Semiconductor</b> 3910 N First St, San Jose, CA 95134 (408) 433-6000 <b>Circle 313</b>									
V53C400/404	4 Mx1 or 1 Mx4	60, 70, 80	350/2.2	16 or 64	600	fast page	Q391	\$21	—

INTEGRATED CIRCUITS

automatically available in common DRAM configurations. But as system designers grow ever more miserly about power consumption, DRAM architects are going back to the drawing boards to create DRAMs specifically designed for low power.

At present, Micron Technology's low-power 4-Mbit DRAM is selected from their standard production line. Within six months, the company will offer a DRAM that is specifically designed for low power. Based on a new mask set, this new design focuses on reducing power in the back-bias generator—a part of the DRAM which typically draws a lot of current. This DRAM will have a battery-back-up current of 300  $\mu$ A. Without specifying the yields of their DRAMs selected for low power, Micron expects to get significantly higher yields from a DRAM designed for low power.

Micron isn't the only vendor designing parts specifically for low-power. With the laptop and notebook

computer markets booming, the timing for low power is right for DRAM customers. But this isn't the only reason why DRAM vendors are doubling their efforts to reduce power.

**"We've now decided that we're at an adequate speed, so we're now concentrating on reducing power."**

—Ken Pope, Hitachi



"When we reduce the cell size of a DRAM, we can either reduce power or increase speed," says Ken Pope, group product marketing manager for memories and mass storage at

Hitachi (Brisbane, CA). With average DRAM access times of around 60 ns, boosting speed is becoming less of a concern. "We've now decided that we're at an adequate speed, so we're now concentrating on reducing power." As a result of these efforts, Hitachi's line of low-power DRAMs has the lowest active power in the industry, with power dissipation in the 100-mW range. To further reduce power, the company has developed some very high-quality oxides enabling their DRAMs to refresh in 512-ms cycles.

**Self-refresh**

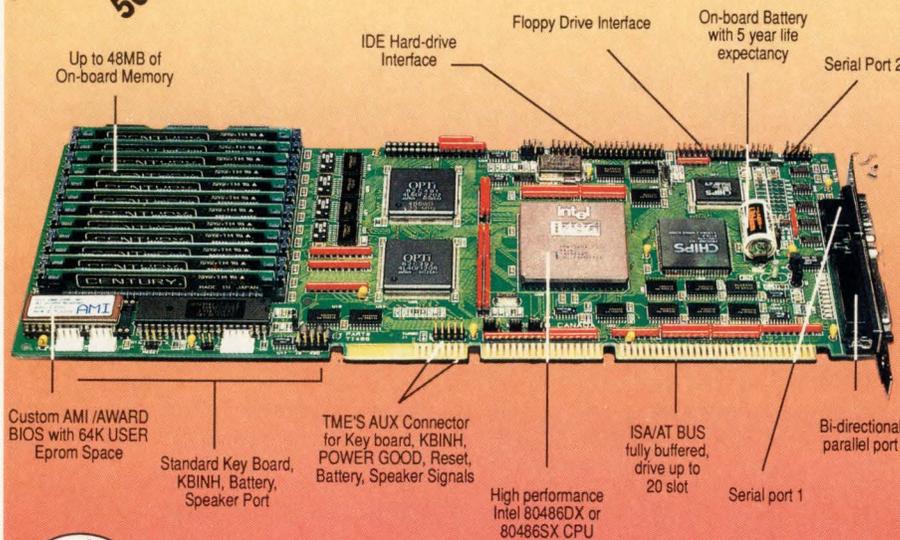
At the present time, most DRAMs are refreshed by some sort of external control. In a standard DRAM, a controller has to charge each cell every 15 ms. The most-recent trend among DRAM manufacturers is to design parts that can decide themselves when they need to be refreshed.

While a handful of vendors, in-

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✓ Under 7.8 Watt	No
✓ Two-Year Warranty	?
✓ 64K User EPROM	?
✓ Auto Configuration BIOS	No
✓ On-Board Battery with 5-year life expectancy	No
✓ Fully Buffered ISA/AT Bus, drive up to 20 slots	?

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**HQP386SXC**

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cluding Hitachi, Micron Technology, and Texas Instruments (Dallas, TX) have self-refreshing DRAM designs in the works, Toshiba (Irvine, CA) has the first self-refreshing part already in production.

When the self-refreshing DRAM is in standby mode, and it identifies that certain conditions are met, the DRAM puts itself into self-refresh mode. From then on, the refresh is controlled internally. During the battery back-up mode, these parts automatically put themselves into the self-refresh mode. In that mode, the 4-Mbit part draws less than 200 mA.

"When you put it in internal-refresh mode, the device will take care of its own refresh," says Avo Kanadjian, marketing manager at Toshiba. "Through its sensing scheme it will effectively do a refresh every 100 to 200 ms. That will obviously result in a drastic drop in power." Available now in volume, the TC14800A, Toshiba's 512x8-kbit,

self-refreshing DRAM is already being used in at least one notebook design—Toshiba America Information System's T2000SX notebook. A 512k x9 part will be available soon.

#### Lowering the voltage

The attack on power consumption will make its greatest strides when more-extreme changes occur. "The next step will be changing the power supply to 3.3 V," says Toshiba's Kanadjian. "The JEDEC standard calls for a change of the DRAM's supply voltage for devices of 64-Mbits or more capacity." While this reduction in voltage translates into drastic reductions in power consumption, the change probably has little to do with market demands for lower-power DRAMs. The primary concern was getting to the smaller geometries needed for the higher-density DRAMs to work at all. "At the 4-Mbit level we have an internal voltage converter which

takes the external voltage of 5 V and reduces it internally. We did this because the 0.7- $\mu$ m process could not handle 5 V internally."

Hitachi, now in the second generation with its 4-Mbit DRAMs, will soon bring out a third generation of 4-Mbit parts at 3.3 V. "In our third generation of 4-Mbit DRAMs we will be designing in a lot of things we learned from our 16-Mbit designs," says Hitachi's Pope. "Because we're making them at 3.3 V, there won't be any backwards-compatibility problems." According to Pope, Hitachi has a large number of customers that can use 3.3-V DRAMs right now.

Not all system designers will want 3.3-V DRAMs right away, however. "It's a little bit like 'the chicken and the egg' at this time," says Kanadjian. "It's more than a just a memory issue. The peripheral devices and glue logic that interface with memory also have to be converted to 3.3 V." ■

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## DRAM Expansion Memory Cards

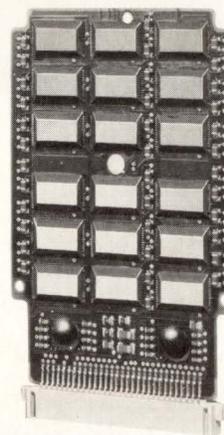
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## PCB toolset couples schematic capture and layout

As the clock speed of digital circuits increases, the critical impact of circuit board layout on signal integrity is forcing printed circuit board designers to tighten the integration between the schematic entry and the layout phase of a design. Printed circuit board tool vendors are answering these demands with tools that bring the layout process into the domain of the design engineer. The Visula High Performance Engineering (HPE) System from Racal-Redac is the latest suite of tools to provide

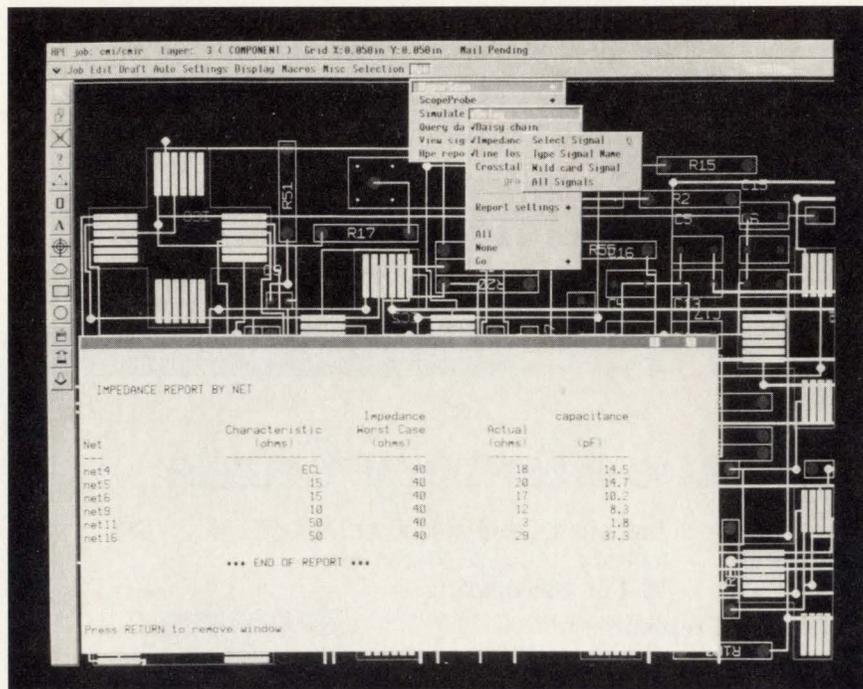
show up as layout-sensitive propagation delays, as crosstalk from adjacent lines or as signal attenuation. HPE also lets engineers visualize these parasitic effects on a specific net by invoking the Scope Probe simulator at any point during physical layout.

In addition, the limits for parasitic effects (for example, the maximum acceptable routing delay) can be specified as a constraint by the engineer during schematic capture. HPE users also have the ability to

Values calculated by HyperScan, Scope Probe or with Quantic Labs' Greenfield software can be included in a physical domain simulation. There the flat physical layout (as opposed to the hierarchical schematic) is passed to Racal-Redac's logic simulator, Cadat 2000, along with the calculated propagation delays. The result is a board-level worst-case timing simulation.

Visula HPE is available for Apollo, Sun-4 and DECstation platforms. The full suite costs \$75,000.

—Mike Donlin



The HyperScan circuit screener calculates layout interconnect parasitics and compares them to threshold limits defined by the design engineer.

this integration by linking the elements of physical layout (specific signal delay, impedance and manufacturing constraints) to high-level design rules.

The Visula HPE toolset includes schematic capture, printed circuit board layout, the HyperScan layout analyzer and an on-line transmission line simulator, Scope Probe, jointly developed by Quantic Laboratories and Racal-Redac. The suite lets the user specify, simulate and control—with graphical feedback—the effects of layout parasitics on the performance of digital circuits. These effects will typically

define pin and branch orders, the maximum acceptable crosstalk, the acceptable impedance range on pins, or the maximum acceptable attenuation as constraints on the system.

The HyperScan module checks all nets identified as critical, calculates the values of the parasitic electrical properties of those nets and compares them with specified values. This ensures that physical properties, such as stub length and pin order, can be correlated with electrical constraints such as signal crosstalk and attenuation. The tool produces a report that will identify any detected violations of the constraints.

### Visula HPE at a glance

- Integrated PCB design toolset
- Rules-driven layout and routing
- Transmission line simulator displays parasitic effects
- Layout analyzer checks all critical nets
- For Apollo, Sun-4 and DEC station platforms \$75,000

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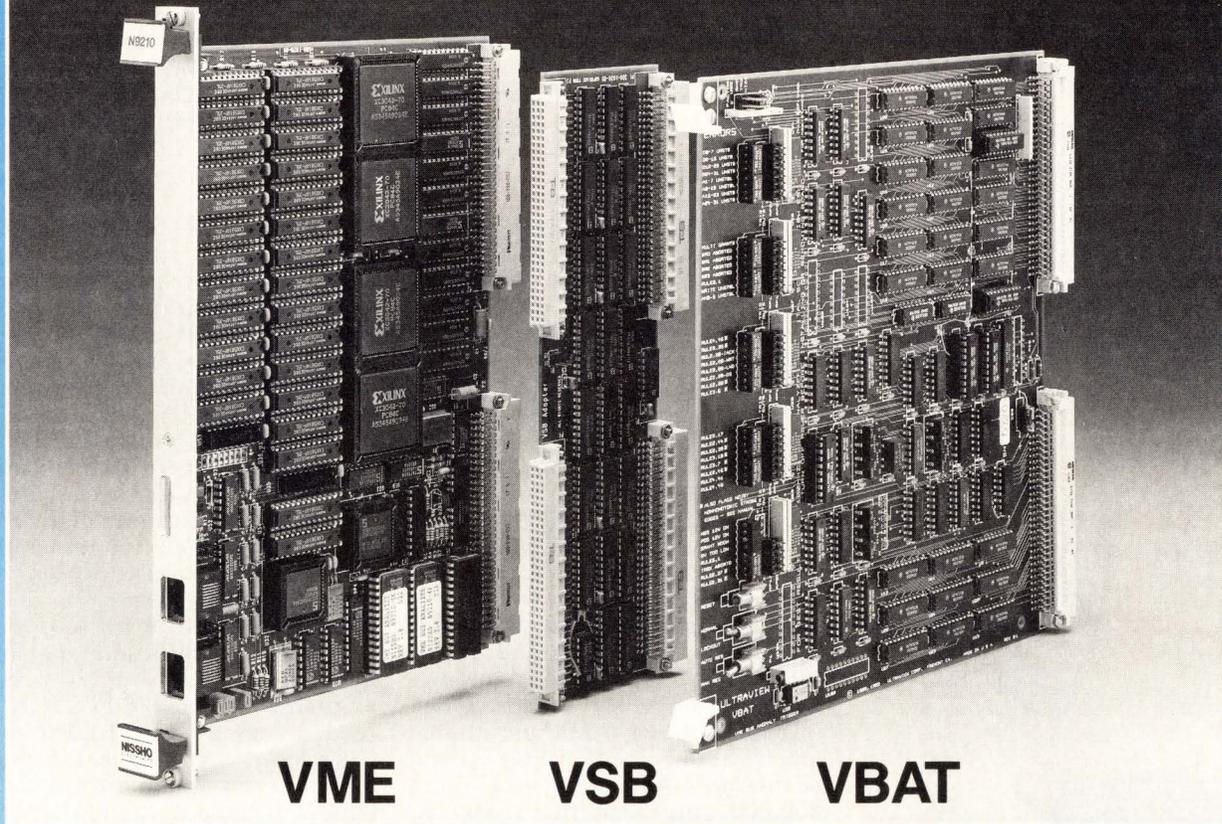
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**New algorithms, compact data structure speeds logic simulator**

Logic simulators have to sacrifice speed, accuracy or capacity as a simulated circuit's size increases. Users are reluctant to accept these tradeoffs, especially in accuracy. And though most designers acknowledge that speed must be sacrificed as circuit complexity increases, few are willing to accept days of simulation time for complex ASICs and printed circuit boards. Evaluations Per Second (EPS) has developed what it claims is the answer to this dilemma—the Simetri logic simulator.

According to EPS, the Simetri simulator can achieve speeds of up to 270,000 events/s on a 33-MHz 486-class machine. When the Sparstation and IBM RS 6000 versions of the simulator are released later this year, EPS promises even higher performance.

At the heart of the simulator are proprietary algorithms and an extremely compact data structure. "Most primitives can be represented in 64 bytes," says Michael Massa, president of EPS. "This has several advantages. A large circuit of up to 250,000 gates can fit in only 16 Mbytes of main memory. This also means that large portions of the simulation can remain in cache, which reduces cache misses."

**Separating events and evaluations**

According to Massa, Simetri's two-list, event-driven, timing-wheel algorithm provides superior simulation accuracy with full timing information. "The two-list approach—where events and evaluations are stored in separate lists—eliminates event-ordering dependencies that plague simulators relying on one-list algorithms," Massa points out. "This accuracy is especially important for electronic designs containing flip-flops, feedback paths and potential race conditions."

Though Simetri can run in unit-delay mode, it also handles typical timing parameters such as setup-and-hold times, rise and fall times and minimum pulse width. Users can set minimum and maximum values, but the simulator doesn't support dynamic worst-case timing analysis.

For the present, the Simetri simulator has no direct interface to any EDA toolsets but it does accept EDIF 200 netlist data. Though Simetri is presently strictly a gate-level simulator, EPS doesn't rule out support for VHDL and Verilog at a later date.

Simetri boasts an intuitive user interface with pull-down menus, multiple windows, on-line context-sensitive help and mouse support. The simulator also provides multiple overlapping output windows that display state information in tabular, event-trigger, snap-shot, and waveform representations. These multiple user-named output windows can simultaneously monitor the output response of different sections of the circuit under test. An event-driven display-processing feature allows the debugging of large electronic designs without the traditional performance penalties. Simetri will be available for 386/486 PCs with extended memory for \$10,000 in the third quarter of this year. Support for Sparstations and the IBM RS 6000 will come in the fourth quarter at a cost of \$25,000.

—Mike Donlin

**Simetri at a glance**

- Up to 270,000 events/s on a 33-MHz 486 PC
- Up to 250,000 gates can fit in 16 Mbytes of main memory
- Two-list algorithm eliminates event-ordering dependencies
- Multiple user-named windows display
- Available Q3 for 386/486 PCs; Q4 for Sparstations and IBM RS 6000s
- \$10,000 for PC version; \$25,000 for workstation version

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## FPGA synthesis tool has architecture-specific optimizers

The AutoLogic field-programmable gate array (FPGA) synthesis tool from Mentor Graphics offers architecture-specific optimization for Xilinx, Actel, and Altera FPGA technologies. Based on Mentor's AutoLogic synthesis product for ASIC and IC design, AutoLogic FPGA optimizes for area and speed, providing a mix of Boolean minimization and factorization, as well as state assignment and technology mapping algorithms for the logic optimization of supported FPGA devices.

Mentor claims that ASIC optimizers fall short when used to synthesize FPGAs since cost functions (measurements of circuit area and speed used when optimizing) of CMOS gate arrays do not correlate to FPGA logic elements. With regard to applying ASIC- or programmable logic device-specific optimization technology to FPGAs, director of marketing for Mentor's Design Synthesis Division, Rob Mendes da Costa, says, "These approaches lack architecture-specific optimization capabilities and often show worse, rather than better, results. Benchmarks have shown that AutoLogic FPGA achieves up to 50 percent better results than ASIC-specific optimizers."

Multi-level optimization algo-

rithms in AutoLogic FPGA minimize design logic and transform the structure of netlists. And the architectural-specific algorithms let users map directly into FPGA logic elements and thus, according to Mentor, ensure accurate cost correlation. Custom mapping rules address device-level architectural features. For instance, for Xilinx-specific technology mapping, lookup-table (LUT) synthesis elements emulate the Xilinx CLB (configurable logic block). AutoLogic FPGA contains special lookup-table primitives which cover all three- and four-input design functions and common five-input combinatorial logic functions. These special primitives are given a normalized cost of one, equivalent to the cost of any Xilinx library primitive (e.g. a two-input NAND). During technology mapping, logic functions that can be implemented in these elements are preserved and mapped directly into a LUT.

The AutoLogic family of Mentor's synthesis tools is integrated into the company's ASIC and IC design environments. AutoLogic Blocks, an optional product, allows users to graphically express design functionality using high-level macros, and AutoLogic VHDL will provide VHDL

synthesis for ASICs, FPGAs, ICs, and PLDs.

AutoLogic FPGA supports the Xilinx XC2000, XC3000, and XC4000 families, the Actel Act 1 and Act 2 families, and the Altera MAX 5000 family. Available now in Mentor's Software Release 7.0 design environment, AutoLogic FPGA is priced at \$5,000 per vendor supported. AutoLogic FPGA can also be purchased as an option to a standalone version of AutoLogic (for use in a mixed workstation/personal computer environment). Users can interface to EDA environments through EDIF, Xilinx XNF, and Actel ADL netlist formats.

— Barbara Tuck

### AutoLogic FPGA at a glance

- Support for Xilinx, Actel, and Altera
- Cost function correlation in FPGAs
- Custom technology mapping algorithms
- Interface to other tools via EDIF, XNF, and ADL writers

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## Dual-DSP architecture puts 100 MFlops on a single VME board

The first VMEbus board to offer Analog Devices (Norwood, MA) latest floating-point processor, the ADSP 21020, comes from Ixthos (Laurel, MD). The IXD7232 board boasts a pair of the new processors, each with a sustainable 50-MFlops performance. And the two processors can work together to make a full 100-MFlops board. Ixthos also includes three separate mezzanine buses to provide I/O and memory flexibility.

Ixthos' IXD7232 is designed to handle the I/O and processing rates required in many real-time applications. Each of the two processors includes its own digital signal processing chip, I/O mezzanine channel, 512 kbytes of data RAM and 192 kbytes of program RAM. All program and data RAM banks operate with zero wait states to take advantage of the ADSP 21020's modified Harvard architecture. Since there's no swapping or slaving between the two processor sections, each is free to run at optimum rates.

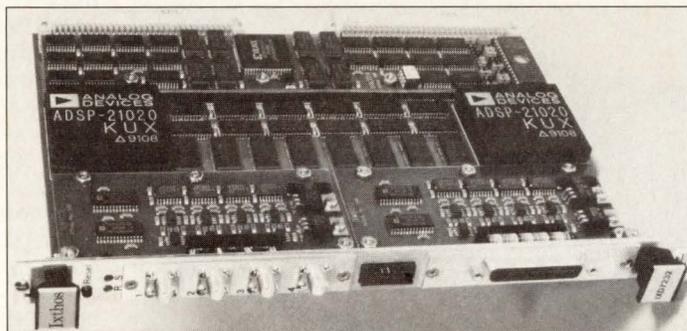
According to Ixthos, one of the keys to the board's performance in a system is found in the dual-mezzanine connectors. The two I/O connectors—essentially a pinout of the ADSP 2120—allow the board to be configured for processing almost any type of analog or digital signal while the memory mezzanine card provides reconfigurable global memory to let the board be optimized for a wide variety of algorithms and applications. In addition, multiple boards can be connected and still provide deterministic performance thanks to fast, parallel FIFOs which allow optimum transfer rates between DSPs.

### Tied together

While each ADSP 21020 can provide 50 MFlops independently, the two on-board processors can be combined using an internal 2 kbyte  $\times$  32 parallel BiFIFO which ties the two processors together such that the board yields 100 MFlops of processing power. Another advantage of the

mezzanine architecture, claims Ixthos, is that additional DSPs on adjacent boards can be added to the pipeline and contribute their full processing power. With this configuration, a two-board pipeline can perform 200 MFlops on a continuous real-time signal entering the system at 50 Mbytes/s. Additional processors will provide a linear increase in performance, up to the point where system constraints impede further advantage.

The ADSP 2120 is Analog Devices' latest entry into the floating-point chip market. Available with



either 40- or 50-ns cycle times, the ADSP 2120 claims to be one of the more-efficient floating-point DSP devices available. In a single cycle, each of the two chips on board can simultaneously perform an ALU operation, a multiply/accumulate, a barrel shift and two external fetches. A single 48-bit instruction directs all five operations. With multiple operations per cycle, each processor in the board is capable of peak performance of up to 125 MOPS.

In addition, the modified Harvard architecture of the chip allows simultaneous fetches from the program and data buses. This unique architectural approach lets data be stored in either program or data RAM. Coupling this architecture with on-chip, zero-overhead cache means the 2120 is particularly efficient on tightly looped code—a characteristic of many signal-processing algorithms.

Using the 40-ns version of the ADSP 21020, it's possible to complete a complex 1024-point fast Fourier transform in 0.77 ms. This is roughly 2.5 times faster than the

published benchmark of TI's 320C30/40 chip.

### Board integration

To limit the processors' overhead so they can run at optimum speed, the IXD7232 board incorporates many separate functions such as dedicated on-board I/O and DMA controllers. These take over tasks normally performed by the processor such as data movement, timing and synchronization. The zero-wait-state program and work-space RAM also isolate the DSPs from the effects of system overhead.

The board uses a standard D32/A32 VMEbus-master interface. It has provision for high-speed burst-data rates using the four DMA channels and block-transfer capability. In addition, the board can receive four mail-box interrupts in addition to generating or receiving any of the seven standard VMEbus interrupts. Multiple boards can easily be synchronized using the location-monitor feature.

The I/O mezzanine buses can accept any of a variety of options offered by Ixthos, or customers can figure their own custom mezzanine cards. At present, Ixthos offers two families of mezzanine boards: one comprises four filtered 18-bit data converters (four A-D converters, four D-A converters); the other, eight filtered 12-bit data converters with synchronous conversion rates to 29 kHz. Prices for the IXD7232 start at \$7,950. Mezzanine interfaces start at \$495.

— Warren Andrews

### IXD7232 at a glance

- 100-MFlops performance
- Dual ADSP 21020 DSPs
- Two mezzanine bus connectors
- Standard VMEbus interface

**Ixthos**  
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Circle 355

## Dual-processor VME card hits 40 Mips

Dual-processor VME cards promise significant performance advantages over single-processor boards, but outside of a handful of digital signal processor boards, they have been relatively scarce. The latest example is the SV420 from Synergy Microsystems (Encinitas, CA), which is based on two 68040 processors. "Motorola's 68040 is the first CISC processor with a large enough cache and enough intelligence to allow two on a 6U-VME board," says Tom Powell, Synergy's marketing director. The board can use the two processors in either a tightly coupled

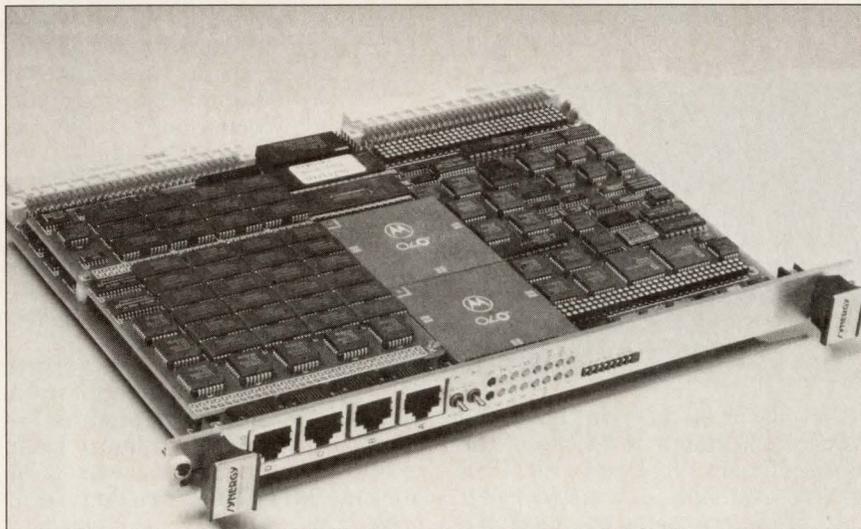
VME64 (D64) standard to help increase transfer rate. A proprietary controller with specially designed burst-mode circuitry lets the board sustain a transfer rate of 66 Mbytes/s. This transfer rate means that the board can move data nearly as fast as the on-board 68040s (80 Mbytes/s). Further, the board's memory design is tailored to the 68040's maximum data transfer rate of 80 Mbyte/s. It uses field-interchangeable DRAM modules configurable in 2, 4, 8, 16 or 32 Mbytes, which support single memory-wait-state reads, and zero wait-state

working on a multiprocessing version of Unix." Other evaluators are either running multiple versions of a single operating system, or running different operating systems on each processor. For example, Unix along with a real-time operating system simultaneously.

While the board boasts two high-powered processors, in many applications they operate like two processors on separate boards. The two major differences are the efficiency in communications between the two processors on a single card, and the fact that a single card can replace two. Having the two processors on a single board with direct communications eliminates much of the bottleneck usually encountered trying to move large amounts of data from one processor to another.

Multiple SV420 boards can be interconnected through the mezzanine bus—addressed by both processors—speeding transfers from one board to another. In one application, three SV420 boards are used to process radar information. Each of the six processors operates on a different portion of the incoming data. By using the dual-processor board, the customer has been able to double the performance of a system based on single-processor boards while cutting the number of boards in half. And because the two processors on the SV420 share the same on-board resources (VME interface, timers, clocks etc.), the cost for the dual-processor board is well below that of two single board computers.

—Warren Andrews



Synergy's SV420 is a dual-68040 board providing up to 40 Mips in a single VME slot. The two 25-MHz processors operate in a tightly- or loosely-coupled mode, while a DMA processor handles I/O independently. The mezzanine card on the left is a DRAM module, triple-ported 68040, VME and Synergy's EZ-bus mezzanine bus. EZ-bus can also interconnect multiple SV420s.

or loosely coupled mode, allowing the processors to either cooperate on a single task or operate independently on two separate tasks. The SV420 doesn't use either processor for I/O functions. Instead, the board provides an optional DMA coprocessor which supports SCSI, Ethernet and four additional synchronous serial ports. "This intelligent controller," says Powell, "lets all I/O operations take place in parallel with normal 040 operations increasing the board's efficiency."

### VME64 ups transfer speeds

The SV420 allows for 64-bit block transfers, using the proposed

writes. The modules, which are triple ported to the 68040, the VMEbus and Synergy's own mezzanine bus, EZ-bus, incorporate byte parity protection and support the 68040 cache burst fill with 3-1-1-1 burst reads and 2-1-1-1 burst writes.

The company claims that the board, with two 25-MHz 68040 processors and up to 32 Mbytes of DRAM, can provide up to 40 Mips of processing power. But while the Mips rating is impressive, it may not be that simple to put all that processing power to work on a single task. The company reports that there are presently a handful of beta sites for the board, "one of which is

### SV420 at a glance

- 40 Mips SBC for VMEbus
- Dual 25-MHz 68040s
- DMA coprocessor offloads I/O tasks from 68040s
- VME64 sustains 66 Mbyte/s
- Multiple SV420s boards can be linked through mezzanine bus

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## 1.25-GHz ECL array has on-chip phased-lock loop

The Q20P025 ECL array from Applied MicroCircuits offers users digital logic gates and an on-chip phased-lock loop (PLL), with operating frequencies from 200 MHz to 1.25 GHz, to serialize and de-serialize high-rate data in fiber-optic telecom and datacom applications. Peak-to-peak edge jitter for the PLL is from 50 to 100 ps. Typical gate delays range from 100 to 250 ps, and maximum total power is from 1.5 to 3 W (0.5 to 1 mW/gate). Frequency and clock-recovery macros are available for the on-chip PLL. For the digital portion of the array, a library of SSI and MSI macros includes encode/decode functions, high-speed shift registers and divide-down counters.

"In the video and graphics arena, speed requirements are increasing as screen size and number of colors expand. Combined with the trend of workstations moving onto the desktop, cost and power reductions are forcing greater integration, result-

ing in the need to combine the previously separate PLL and shift registers that feed video D-A converters," says Mike Hollabaugh, AMCC vice-president of marketing.

The basic PLL on the Q20P025 consists of a phase detector which compares the phase difference between a VCO and a reference input; a loop filter, which converts the phase detector output into a smooth DC voltage; and the VCO, which generates a frequency based on input voltage. Due to differences in reference inputs to the phase detector, metal pattern implementations on AMCC-provided PLL building blocks differ for frequency synthesis and clock recovery. The frequency synthesis PLL generates a high-frequency clock in phase with the input reference (typical frequency multiplication factor is 20, with extension as high as 64). The clock recovery PLL generates a clock which is at the same frequency and 180 degrees out of phase with the

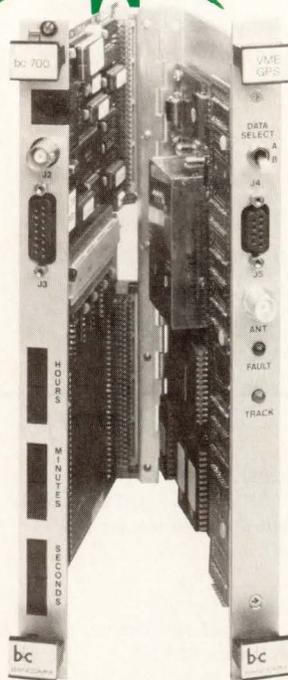
serial data reference input. For datacom and telecom applications, both local and link loopback are supported. At the designer's option, transmitter and receiver designs can be made to perform bit-error-rate measurement to verify fiber-optic link integrity.

Equivalent gate count for the Q20P025, based on AMCC's Q20000 series ECL/TTL logic arrays, is 3,000 by the full-adder method and 2,150 by the flip-flop method. I/O cells can be configured to interface with standard and positive reference (+5 V) 10K and 100K or TTL thresholds. Mixed ECL/TTL capabilities allows interface to both technologies on a single chip without the use of external translators. For dual power-supply devices, the I/O is also capable of a Darlington-type ECL output. And for designs involving external loop filters, selected pins with specified parasitics are predetermined.

Designers can use Mentor, Valid,



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and Dazix tools, as well as Verilog and Lasar simulators, to design AMCC's new array. The Q20P025 is available in surface-mount packages with loop-filter elements mounted on the package or with pin access directly to the filter nodes. Both commercial and military-grade devices will be available. AMCC is accepting orders now, with first prototypes expected next quarter. For commercial grade devices in 100-lead LDCC, the price is \$195 in quantities of 2,500.

— Barbara Tuck

### Q20P025 array at a glance

- On-chip PLL with 1.25-GHz capability
- Edge jitter as low as 50 ps
- Configurable I/Os
- Frequency synthesis and clock recovery macros for PLL
- SSI and MSI macros library

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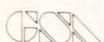
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## Ethernet interface delivered on one chip

With the announcement of the DP83902 Serial Network Interface Controller for Twisted Pair (ST-NIC), all of the functions of an Ethernet interface have been consolidated on one device. The chip includes a network interface controller (NIC), a serial network interface (SNI), and a coaxial transceiver interface (CTI). The ST-NIC solution provides the media access control (MAC) and endec (encoder/decoder) functions with an attachment unit interface (AUI) and 10Base-T interface in accordance with IEEE 802.3 standards. Designers using the company's earlier multi-chip Ethernet interfaces will appreciate the 20 percent reduction in board space as well as the 75 percent power reduction that the new device offers. Further, because the ST-NIC is compatible with National's DP8390 chip set architecture, upgrading to the new device can be achieved without redesigning network operating system software.

The ST-NIC is designed to support all IEEE 802.3 media options. These include Ethernet (10Base5), Thin Ethernet (10Base2) and twisted-pair Ethernet (10Base-T). The part's 10Base-T transceiver incorporates the receiver, transmitter, collision, loopback, heartbeat, jabber and link integrity functions defined by the standard. A complete physical interface from the endec module to the twisted-pair medium can be built using equalization resistors, transmit/receive filters, and pulse transformers.

The integrated endec allows Manchester encoding and decoding via a differential transceiver and phased-lock-loop decoder at 10 Mbit/s. Also included is an integrated crystal-controlled oscillator, collision-detect translator and diagnostic-loopback capability. The endec module interfaces directly to the transceiver module and provides a fully IEEE 802.3 compliant AUI for connection to other media transceivers. For example, fiber optic media can be supported through the AUI.

The MAC function provided by the NIC allows control of packet transmission and reception by means of dual 16-bit DMA channels and an internal FIFO. Bus arbitra-

tion and memory-control logic are integrated to reduce board cost.

To speed system development, National provides a 10Base-T daughterboard that can plug directly into a DP8390 socket. The daughterboard allows the existing Ethernet controller board to operate over twisted-pair wiring with no added hardware or software modifications. The company also has a \$480 evaluation board that can be inserted into a half-size AT bus slot. The evaluation board uses the ST-NIC device to interface to twisted-pair wiring, and can use the ST-NIC AUI port to interface to thick or thin coax Ethernet when a DP8392 Coaxial Interface Transceiver is added.

The ST-NIC also drives five network display LEDs that can be used to provide visual support. These announce Good Link, Transmit, Receive, Collision and Polarity. The display of the first four helps bring some network management functions to the node level. The polarity display indicator indicates the polarity of the twisted-pair wiring which the ST-NIC chip automatically accommodates.

The DP83902 ST-NIC is available now in production quantities. Price is \$42 each in 100-piece quantities. The device is offered in two package options: a standard 84-pin PLCC and a 100-pin PQFP.

— Dave Wilson

### ST-NIC at a glance

- Integrated Ethernet IC
- MAC and endec functions
- AUI and 10Base-T interface
- Supports all 802.3 Media
- Evaluation board available

#### National Semiconductor

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Tel: (408) 721-7020

Circle 360

## EISA chip set lowers system cost

If the cost of building a 486 EISA board was within a \$100 of the cost of building a 486 AT board, would many engineers opt for the EISA design? With the introduction of its new EISA chip set, Opti (Santa Clara, CA) is betting they will. The Opti EISAWB chip set operates with the 386DX, 486SX and 486 processors at clock rates from 20 MHz to 33 MHz. It comprises four VLSI devices, a memory cache controller (MCC), an EISA Bus controller (EBC), an integrated system peripheral (ISP), and a data bus controller (DBC). Each of them is contained in a 160-pin PQFP.

The MCC controls memory subsystem access for the host CPU, other EISA/ISA bus masters and a DMA controller. The memory subsystem consists of up to 16 Mbyte of

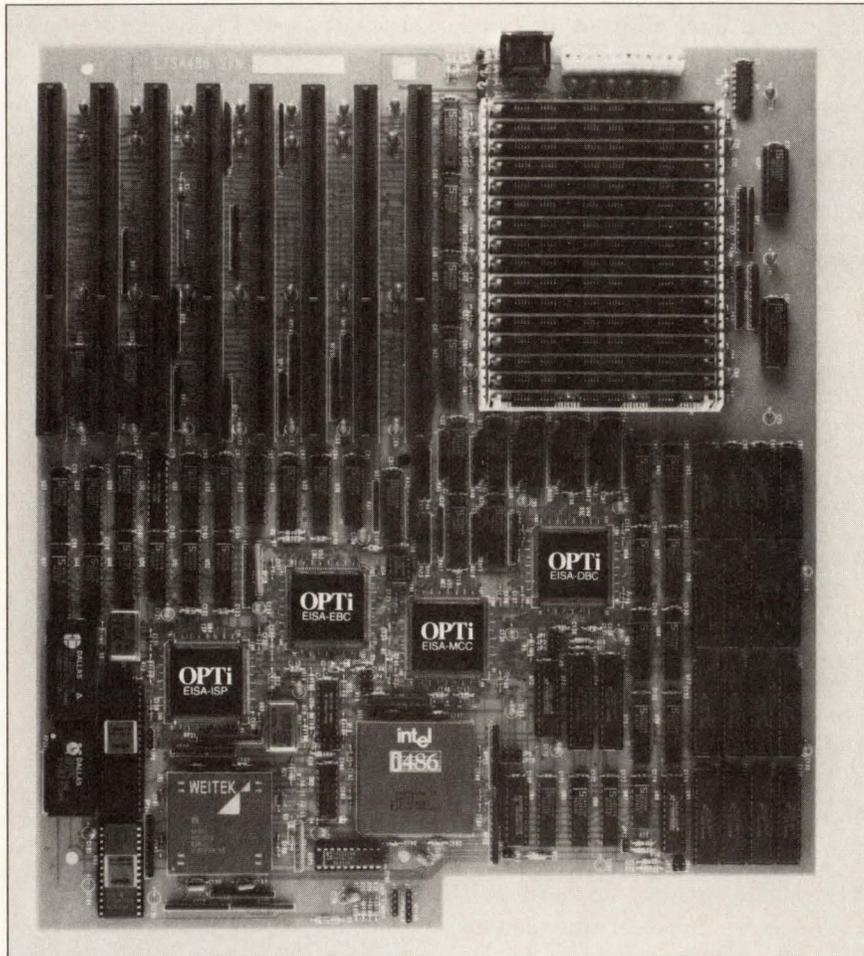
page-mode DRAMs with hidden refresh, and up to 512 kbytes of write-back cache. (Opti claims that it's the first EISA chip set with integrated write-back cache.) The cache is 2-way interleaved for operation with a 486 CPU.

The EBC translates bus control signals and addresses between the host, EISA, ISA and DMA masters and slaves. It generates clocks for the system board and EISA bus, system board resets, and latch buffer controls for EISA addresses and data. It also arbitrates between the host CPU and other masters on the EISA bus and refresh-requests for access to the EISA bus.

The ISP integrates two 8254 timers, EISA NMI/time-out logic, two modified 8259 interrupt controllers, an EISA/DRAM refresh con-

troller and an EISA system arbiter. The ISP connects directly to the EISA system data bus (the SD bus) and buffers the 8-bit peripheral bus (the XD bus). The DBC integrates data buffers, data buffer control, XD bus control, address-enable generation, decode logic for an external keyboard controller, a real-time clock and system-configuration RAM. The DBC provides two programmable I/O chip selects for embedded system peripherals.

Configured for 20-, 25- and 33-MHz systems, the chip set is priced at \$150 in quantities of 1,000. Evaluation kits with complete development support from Opti are priced at \$2,000. Currently sampling, the chip set will be available in quantity in September. —Dave Wilson



The cost of building a 486 EISA board can be close to that of an ISA board when Opti's integrated EISA chip set is used. The four PQFP devices on this board are controllers for the EISA bus, the data bus, the memory cache and system peripherals.

### Opti EISAWB at a glance

- Integrated EISA chip set
- Compatible with 386DX, 486SX and 486DX
- 20-MHz to 33-MHz operation
- Integrated write-back cache
- \$150 in 1000s

#### Opti

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## Tool automates test case generation from graphic design charts

The front-end analysis and design tools used in CASE environments help assure software quality by defining the functions of the finished code. But the software must still be tested to see that it conforms to the requirements set out in the definition and analysis stages of a project. A new tool, called Teamwork/TestCase, has been added to the Teamwork CASE environment by Cadre Technologies (Providence, RI) to automate the generation of test

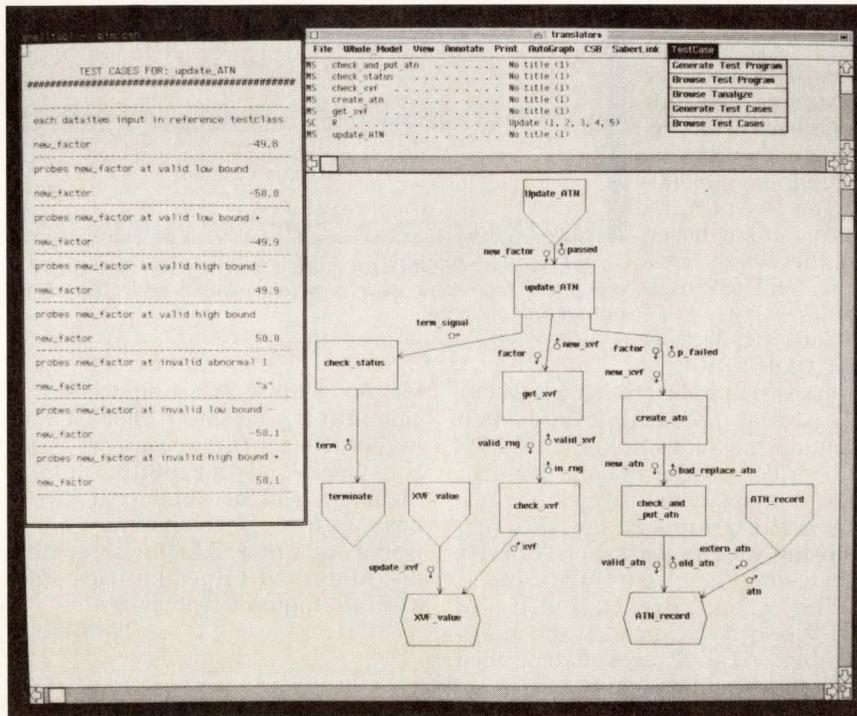
The first such translator, Test-Case/SD, translates module and data definitions within structure charts. Test cases generated from structure charts can be used to test single routines or multiple units of code at the same time. The second translator, TestCase/SA, interfaces with structured analysis diagrams to provide system-level tests based on the requirements specified in the requirements documents. Thus, software can be progressively tested

data elements to generate parameters for testing. For each specified requirement the program uses boundary-value analysis, equivalence class partitioning, cause-effect graphing and error guessing techniques.

The process of manually generating test cases was largely an ad hoc process, with very little record of what was tested and how it was tested. But Teamwork/TestCase documents each test case. And the documented test cases are completely repeatable. As requirements change, TestCase can be used to regenerate test cases based on the new requirements without having to modify them by hand. According to Cadre's product manager Bill Sundermeier, although CASE tools are supposed to provide organizations with reusable code, programmers have been reluctant to reuse code generated by others because they were not sure of its reliability. Thorough and documented test cases now make it possible for an organization to certify reusable code so there will be no doubts about the reliability of modules written by others. The test cases themselves are equally reusable and maintainable.

Teamwork/TestCase is available now for the Sun Sparstation and will be available in the fourth quarter of 1991 for the IBM RS/6000 and for Sun 3, Hewlett-Packard and other workstations. Pricing starts at \$9,995.

— Tom Williams



Teamwork/TestCase is able to generate test cases directly from a Cadre Teamwork/SD structured design chart. The small circles with arrows associated with each element in the chart are data items. The output of the test case generation is represented in the listing on the right.

cases from front-end structured design and analysis tools.

Teamwork/TestCase is based on T, a proven test-case generation tool developed by Programming Environments (Tinton Falls, NJ). T uses an English language interface to define test cases. Cadre has integrated T with its tool environment by creating two translators that can read the output of Cadre analysis tools and automatically translate them into the T input format.

at each phase of development. Test cases can be generated for testing each routine, the integration of routines, and for testing external functional requirements for system-level or acceptance testing.

Cadre's structured design tool not only specifies the structure of the modules within a program; it also defines the data elements (known as couples) that are the input and expected output of each module. The test case generator can use these

### TestCase at a glance

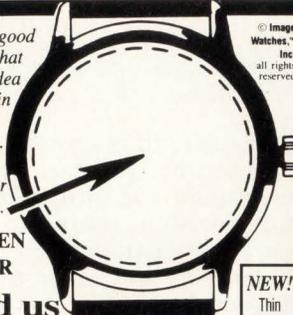
- Automates test case generation
- Uses proven test case generation methodologies
- Integrates with structured design and analysis tools
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## NEW PRODUCT HIGHLIGHTS

### SOFTWARE AND DEVELOPMENT TOOLS

## Cross development system builds real-time 68000 applications on PCs

A cross-development environment for developing real-time applications for the Motorola 68000 family of microprocessors runs on inexpensive PC computers using the MS-DOS operating system. VRTXvelocity DOS/68K by Ready Systems (Sunnyvale, CA) includes a runtime operating system, networking capabilities, system and source-level debugging tools, cross compiler and other cross-development tools. The system is intended to allow engineers to use existing PC platforms for high-end 68000-based real-time development based on the Ready Systems VRTX32 real-time kernel.

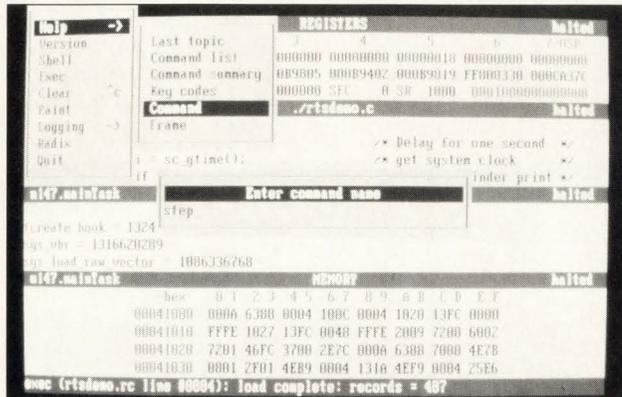
The VRTXvelocity DOS/68K environment is built around VRTX/OS, a real-time operating system that includes the VRTX32 kernel. VRTX/OS resides on the PC and includes IFX, a hierarchical target file system and I/O support; the TNX networking facility based on TCP/IP; and a set of run-time C libraries.

The debugging capability of VRTXvelocity is aimed at the multi-tasking VRTX32 executive. Called RTscope, the debugger resides on the target and serves both as a board-level monitor and a system-level debugger. In addition, VRTXvelocity DOS/68K has included a set of ANSI C tools by Microtec Research (Santa Clara, CA). These include a 68000 ANSI C cross compiler, C cross-reference utilities and Motorola-compatible assemblers, linkers, and libraries.

By combining proven compiler technology with its real-time kernel and debugging tools, Ready provides a development package that lets the user concentrate on the problem at hand and not hardware-specific issues. Ready also includes a number of board-support packages (BSPs) to support commercial CPU and controller boards by such manufac-

turers as Force, Radstone, Motorola, Heurikon and Tadpole. For custom boards, a support system called VES supplies a template for users to build their own BSPs by merely re-writing the hardware library.

VRTXvelocity DOS/68K is availa-



VRTXvelocity DOS/68K provides a multiple-window environment that lets users view registers, source code, command output and memory.

ble for 80386 PC computers and compatibles running DOS 3.3 or higher. Initial target support is for the 68020. Other 68000 family members will be supported in the near future. Development system prices start at \$12,500 with volume discounts and target licenses start at \$145 in quantities of 100.

—Tom Williams

### VRTXvelocity DOS/68K at a glance

- Real-time 68000 cross-development environment for PCs
- Includes VRTX/OS real-time operating system
- Integrated system-level debugger
- Includes ANSI C tool set

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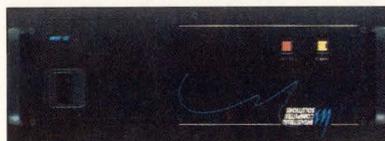
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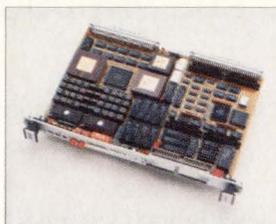


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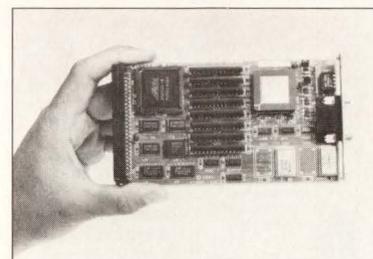
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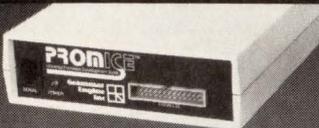
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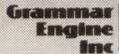
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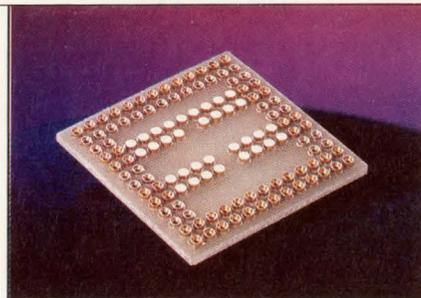
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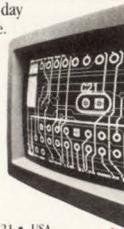
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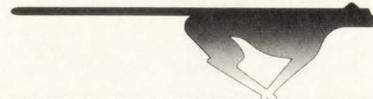
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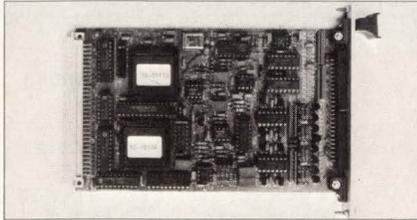
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## 357 MHz 14-Pin Clock Oscillator

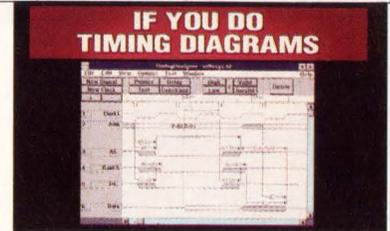
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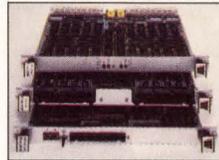
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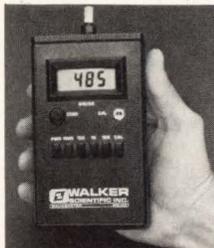


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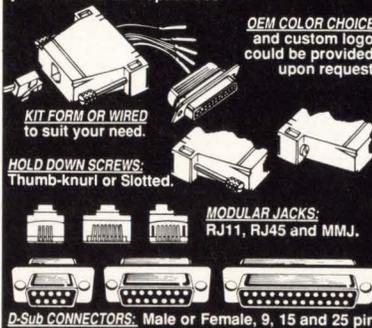
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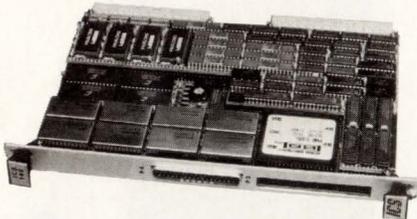
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