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COMPUTER DESIGN

MAY 1, 1987

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

BOARD-LEVEL SOLUTIONS BROADEN IMAGE-PROCESSING APPLICATIONS



**ISDN ICs MOVE TOWARD
SINGLE-CHIP MULTILAYER SUPPORT**

**HOST-BASED TOOLS EDGE OUT
CONVENTIONAL DEVELOPMENT SYSTEMS**

**SINGLE-CHIP PROCESSOR
RUNS LISP ENVIRONMENTS**

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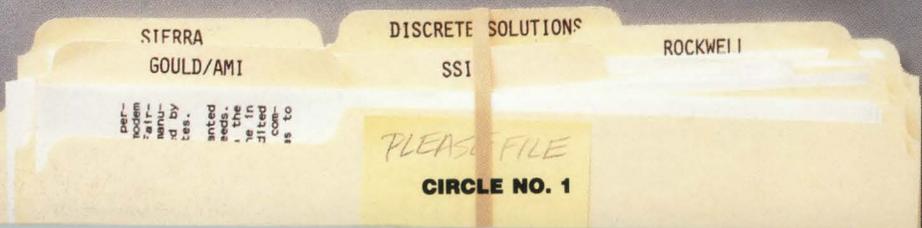
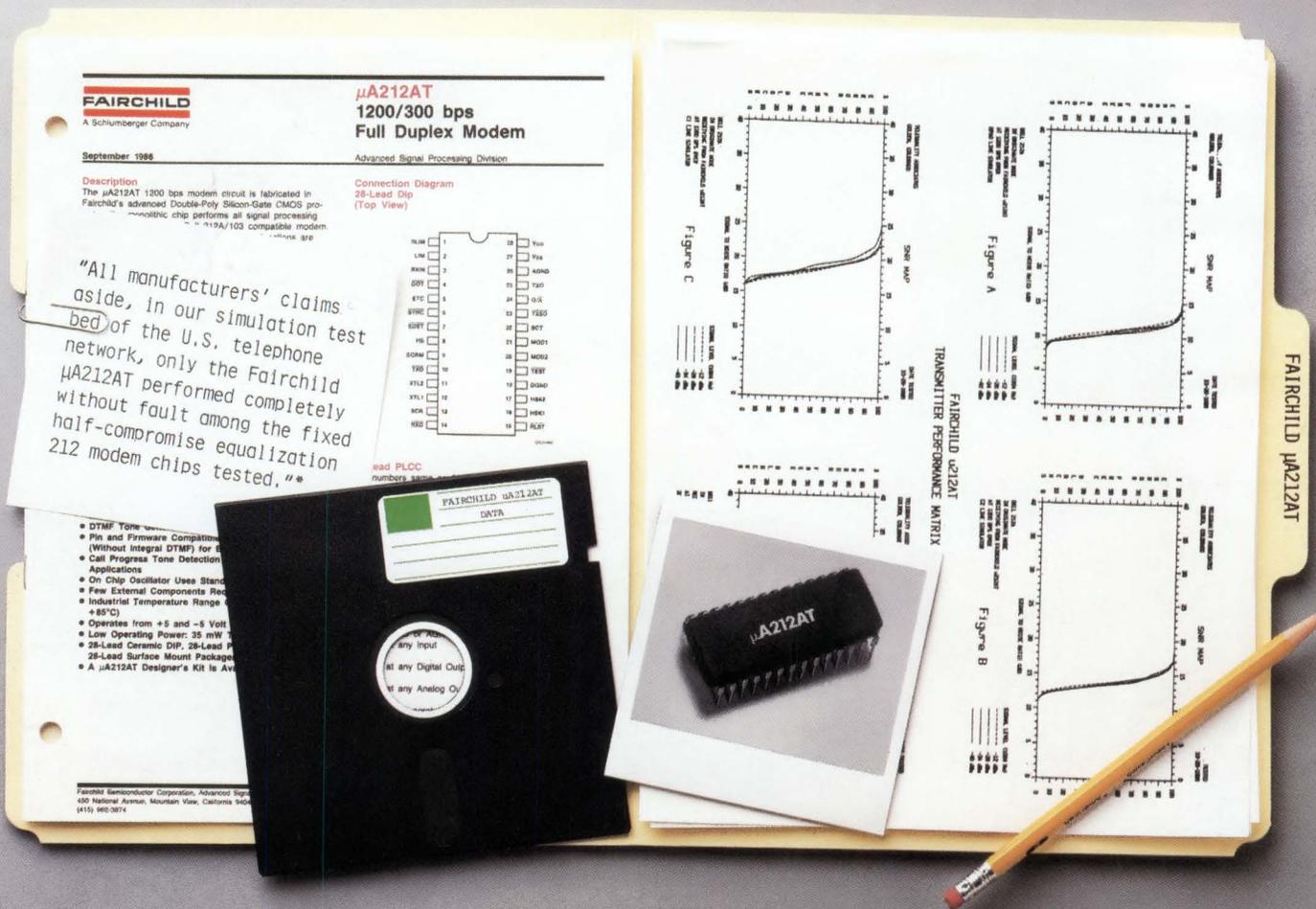
We'd also like to suggest comparing us to the competition. But there doesn't seem to be any.

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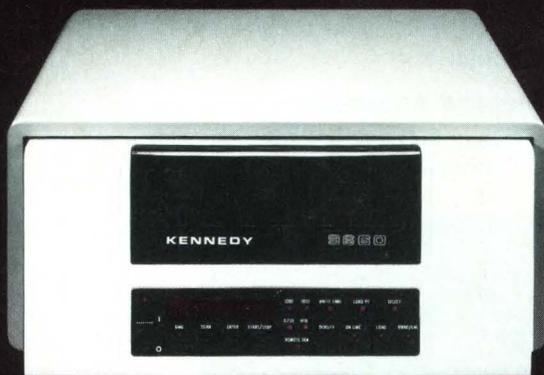
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What could possibly make the Kennedy 1/2" tape hybrid streamer even better? How about...

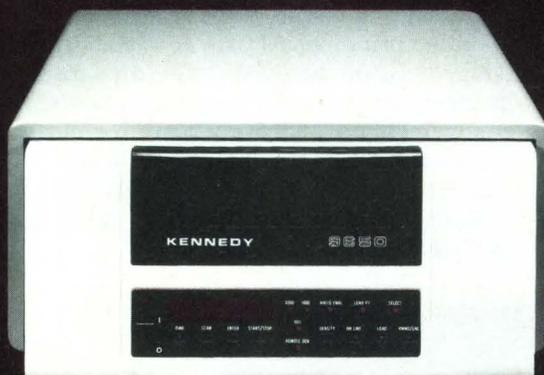
GCR



Model 9610/9660

Quad-density GCR 6250 BPI at 100/50 ips

- Inexpensive GCR storage with up to 270 Mb
- High speed streaming
- 50 ips true start/stop
- 800/1600/3200/6250 BPI
- .3" GCR IBG for maximum data capacity
- VLSI write/read logic
- Standard 8.75" height
- Front load
- Auto threading/loading
- Adaptive velocity control
- Automatic calibration of write current/read gains for each tape
- Automatic read gain control
- Rack mount or cabinet
- 50 MS reposition time in same direction at 100 ips
- 200 MS reposition time in opposite direction at 100 ips
- 12 MS ramp time at 100 ips



Model 9600/9650

Tri-density with 3200 BPI at 100/50 ips

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- High speed streaming
- 50 ips true start/stop
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- Standard 8.75" height
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- 200 MS reposition time in opposite direction at 100 ips
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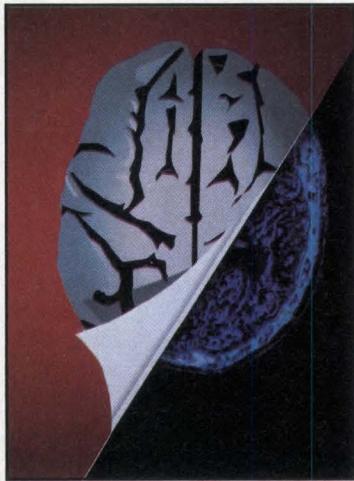
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COMPUTER DESIGN

THE MAGAZINE OF SYSTEM DESIGN AND INTEGRATION

SPECIAL REPORT ON IMAGE PROCESSING

- 53 Image processing was once confined to very expensive systems, but thanks to board-level accelerators, it's becoming more and more affordable. As a result, developers are finding new practical applications for image processing, including those in the manufacturing, visual arts and medical fields. Along with the hardware, the software used in these systems is also evolving. Although commercially available software for image processing isn't abundant, board-level manufacturers and third-party software vendors are recognizing the need for it and are beginning to supply it.



This issue's cover was designed by John Bonner. It was computer-drawn at Visual Conspiracy (Boston).

SYSTEM TECHNOLOGY

Integrated Circuits

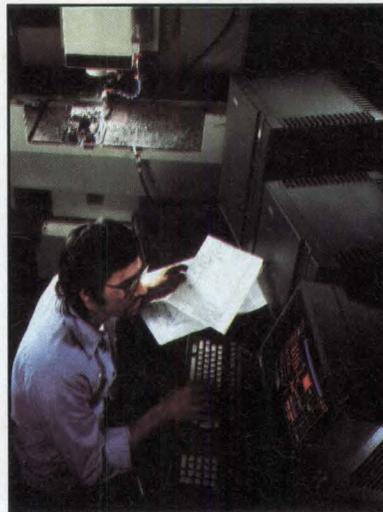
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Control and Automation

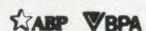
- 49 Single architecture integrates all levels of factory-floor control



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SYSTEM DESIGN

Computers and Computer Systems

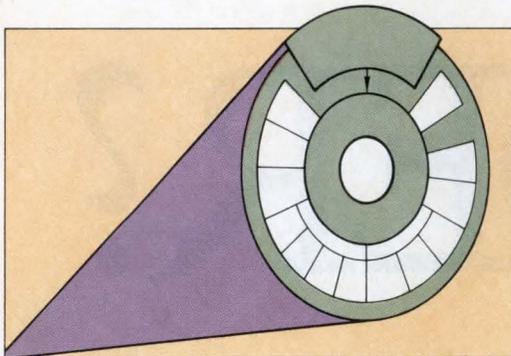
- 69 Busless workstation boosts speed, lowers cost**
No longer constrained by buses, a new VAX workstation provides a threefold performance improvement at half the cost of its predecessor without sacrificing flexibility and expandability.

Integrated Circuits

- 79 Single-chip processor runs Lisp environment**
With the new dedicated Lisp chip, intelligent Lisp/AI workstations can be made much smaller, easier to use, and more affordable as either applications development tools or delivery vehicles.

Software

- 89 Flexible environment supports Ada programming**
Designed to meet DOD requirements, the Ada Language system supports the entire Ada program life cycle while maximizing portability and allowing tailoring of the environment.



SYSTEM PRODUCTS

- 100** Plunging CAD/CAE prices drive multipen plotter advances



- 109** Emulation finds role in prototype board test
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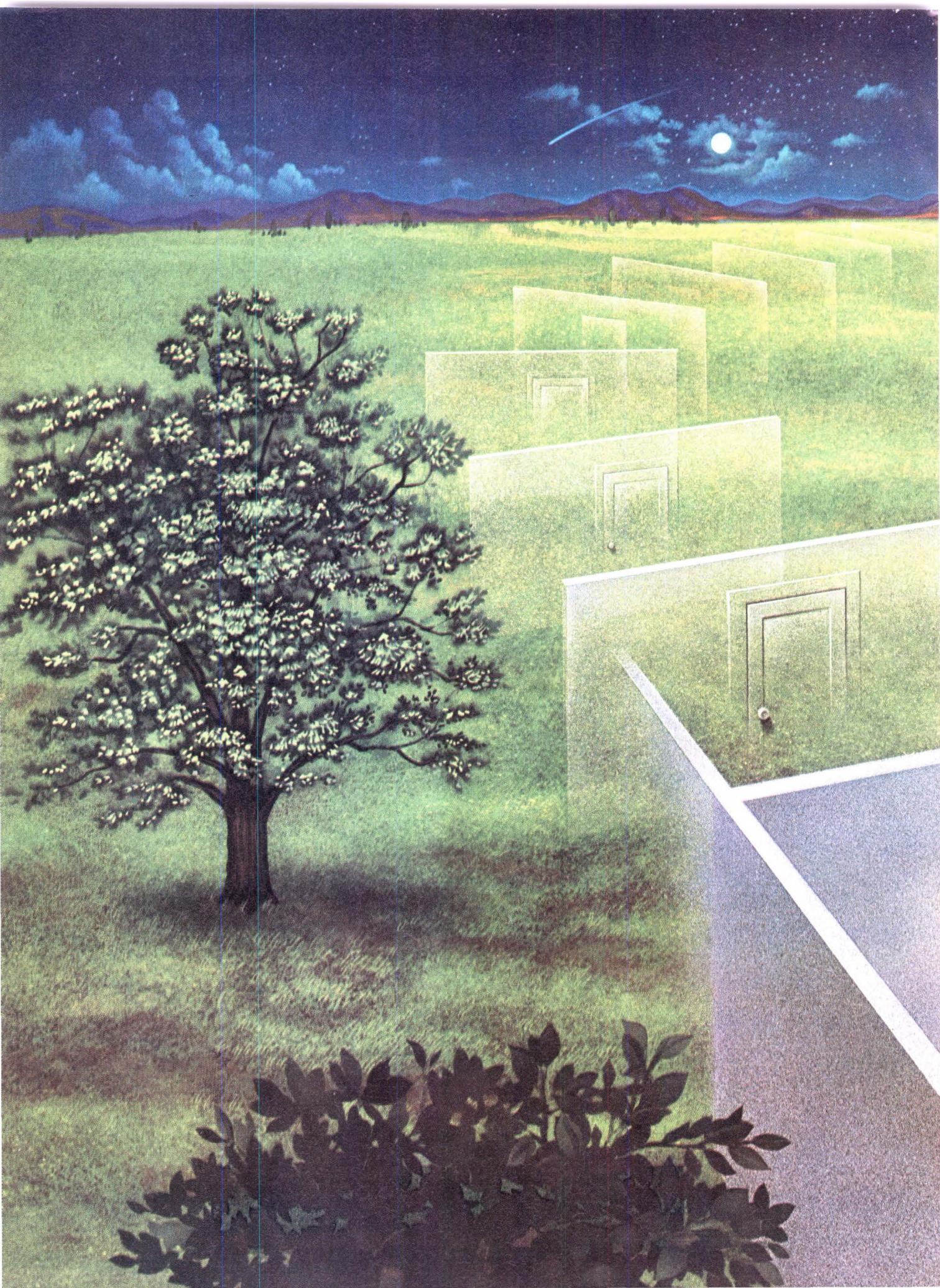
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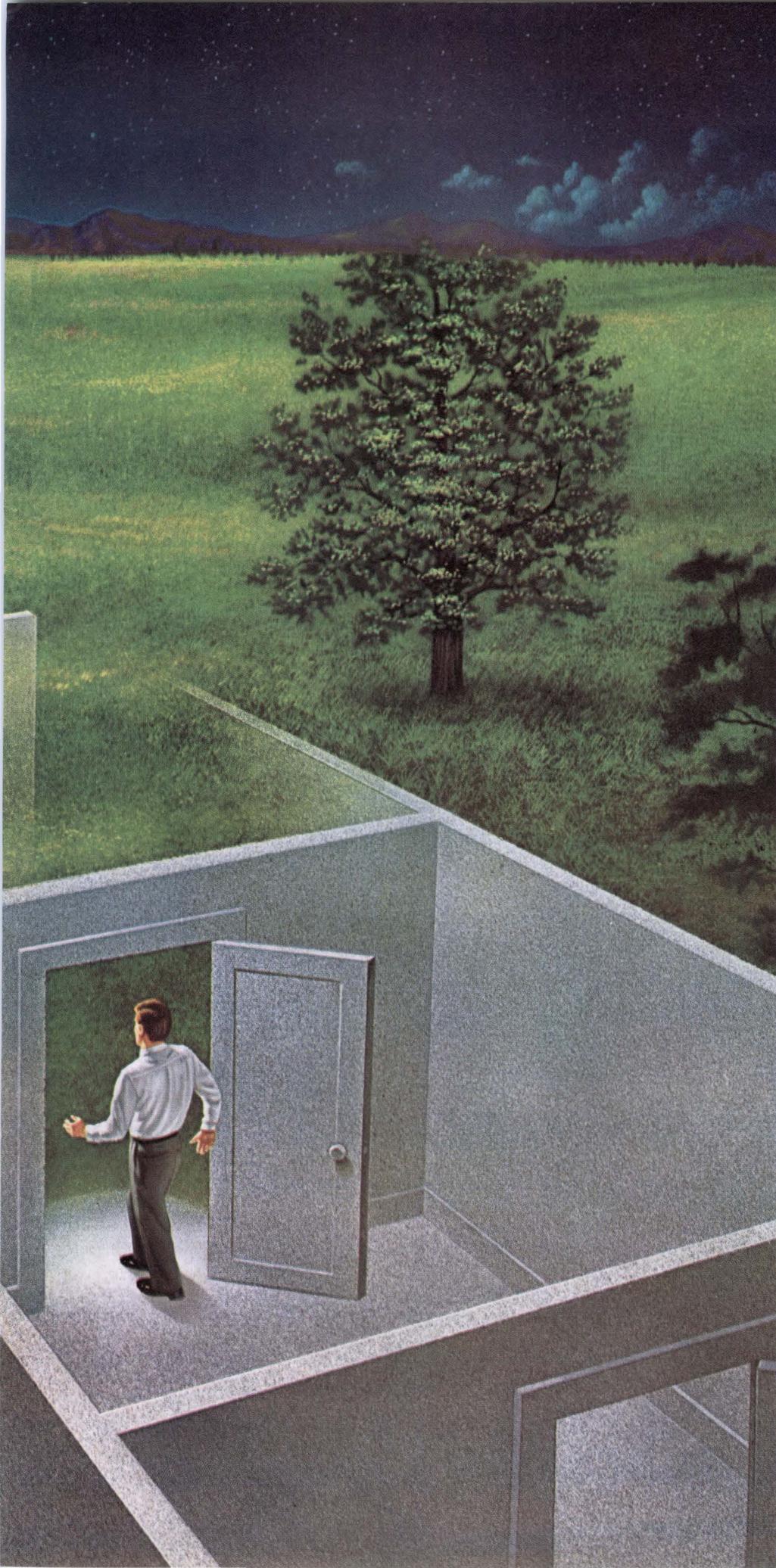
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CIRCLE NO. 3

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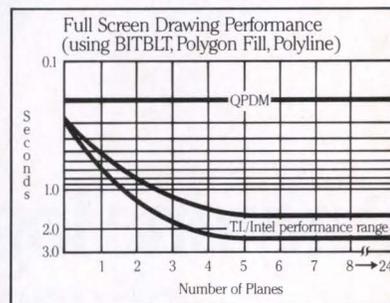
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OUTLOOK

CIRCLE NO. 6

UP FRONT

Chip data separators track higher bit rates

To get data on and off disk faster with fewer components, Adaptec (Milpitas, CA) will offer a monolithic data separator capable of 33-MHz bit rates. This bipolar chip will perform modified frequency-modulation (MFM) encoding and decoding. Other translation schemes such as 2.7 and 1.7 codes will be accommodated by external devices. Meanwhile, National Semiconductor (Santa Clara, CA) is readying a data separator that will accommodate both MFM and 2.7 encoding and decoding but will handle a 24-MHz bit stream.—*E.C.*

High-speed linear supercells to augment CMOS logic

A library of high-speed linear supercells under development by Barvon BiCMOS Technology (Milpitas, CA) to complement CMOS logic on-chip may soon ease the design of devices such as monolithic data separators. By leveraging its ability to execute merged bipolar and CMOS processes, Barvon intends to offer complex analog functions good for high frequencies as standard cells or possible optimized blocks within gate arrays.—*E.C.*

Foxboro backs MAP with process-control computer systems

After a hiatus of several years since its last major introduction of a computer system for the process-control industry, The Foxboro Co (Foxboro, MA) has announced an array of systems designed around an open communications architecture that's compatible with the Manufacturing Automation Protocol (MAP). Foxboro is committed to MAP and will represent the process-control industry in the 1988 MAP/TOP/COS demonstration of Version 3.0. Although 3.0 isn't fully defined, Foxboro is confident that its computer architecture is flexible enough to adjust to whatever the final format of 3.0. will be.—*S.F.S.*

Mini-mainframe combines RISC with multiple processors

Classifying the architecture of its new computer as a mini-mainframe—somewhere between that of a mainframe and a super-mini—Pyramid Technology (Mountain View, CA) has enhanced its 9000 family of reduced-instruction-set computers (RISC) with a three-processor 9830 and a four-processor 9840. These Unix-based systems have 29 Gbytes of disk space and support up to 512 direct-connect users and 14 different proprietary data base management systems. All models will be available this July. Pyramid is developing its next generation of machines—VLSI CMOS versions with even stronger adherence to RISC principles—that will be announced in 18 months.—*N.M.*

Consortium to study diamond films

In an effort that could lead to new high-speed processes surpassing gallium arsenide in performance, a team from Pennsylvania State University (University Park, PA) is forming a consortium to develop diamond deposition technology. Although diamond films were originally thought to be formed only under impossibly high temperatures and pressure, re-

(continued on page 10)

cent work shows increasing promise that diamond deposition can become a commercially viable technology, according to Russell Messier of the university's Department of Engineering Science and Mechanics. As a semiconductor, diamond may produce better high-frequency devices than are possible with either silicon or GaAs. Among the current 21 corporations in the consortium are Texas Instruments, Raytheon, GTE Labs and Eton.—*R. W.*

Timing analysis tool speeds ASIC simulation

A static timing analysis tool to be introduced this month by NCR Microelectronics (Ft Collins, CO) will streamline the timing-simulation process for application-specific ICs. The Vitat timing tool will be used before the logic simulation process and will let the user check marginal timing early in the design cycle. Problems detected by Vitat include race conditions, reconvergent fanout, clock skew problems and setup-and-hold violations. Timing simulation can then be run without multiple passes.—*R. G.*

VLIW supercomputer finally introduced

After seven years of development, first at Yale University and the last three years at Multiflow Computer (Branford, CT), the Trace, a supercomputer based on a very-long-instruction-word (VLIW) architecture and a trace scheduling compiler, has finally arrived. Three versions are available: the 7/200 compacts seven computer operations into a 256-bit instruction word; the 14/200 compacts 14 operations into a 512-bit instruction word; and the 28/200 compacts 28 operations into a 1,024-bit instruction word. Multiflow claims that the 7/200 is over 9 times more cost effective than the IBM 3090-200 and is over 3.5 times more so than the Convex C1-XP. A compiled 64-bit precision Linpack benchmark for 7/200 ran at 6 MFlops.—*N. M.*

High-level tool generates simulation vectors

A CAE tool introduced by Source III (Los Gatos, CA) is claimed to reduce test vector generation time by 80 percent. Vgen, a high-level interface similar to C or Pascal, lets users exercise and analyze critical circuit timing. Interfaces are available to simulators from Valid Logic, Tektronix CAE Systems, Genrad, Daisy Systems, Calma and Simucad. Interfaces to specific testers will be offered later.—*R. G.*

Apollo supports Ethernet, expands network independence

By making its token-ring-based Domain architecture available to Ethernet, Apollo Computer (Chelmsford, MA) will let other manufacturers' workstations connected to Ethernet be as accessible to Domain stations as if they were actually on the token-ring net. The Domain environment has been layered inside the seven-layer International Standard Organization (ISO) reference model so that it can be adapted to other emerging network standards using the model, such as the fiber distributed data interface (FDDI).—*T. W.*

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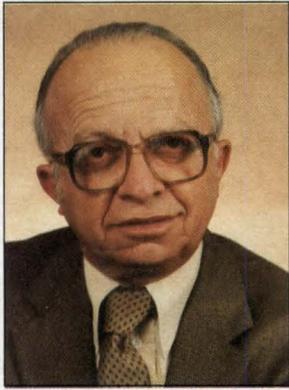


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CIRCLE NO. 8



Computer systems and the military

Computer Design's position as a leading magazine in the industrial system design arena is firmly established. Nearly 40 percent of our readers design or supervise the design of industrial automation systems, and over 30 percent perform the same design duties for process control and monitoring systems. With growth in the automation market ready to explode, these percentages will probably increase accordingly.

But an equally large portion of *Computer Design's* readers—36 percent—design or supervise the design of government, military and aerospace systems. Although designers targeting products at government/military/aerospace markets face issues and problems similar to those involved in targeting industrial markets, this community of designers has special requirements that we must address editorially.

How important are these designers? Nearly \$60 billion dollars were spent last year for government electronics. Despite Gramm-Rudman budget restrictions, NASA alone is expected to spend \$3 billion this year on electronics equipment. And huge sums will be allotted to other Department of Defense agencies. The Pentagon's research, development, test and evaluation budget, for example, is \$17 billion.

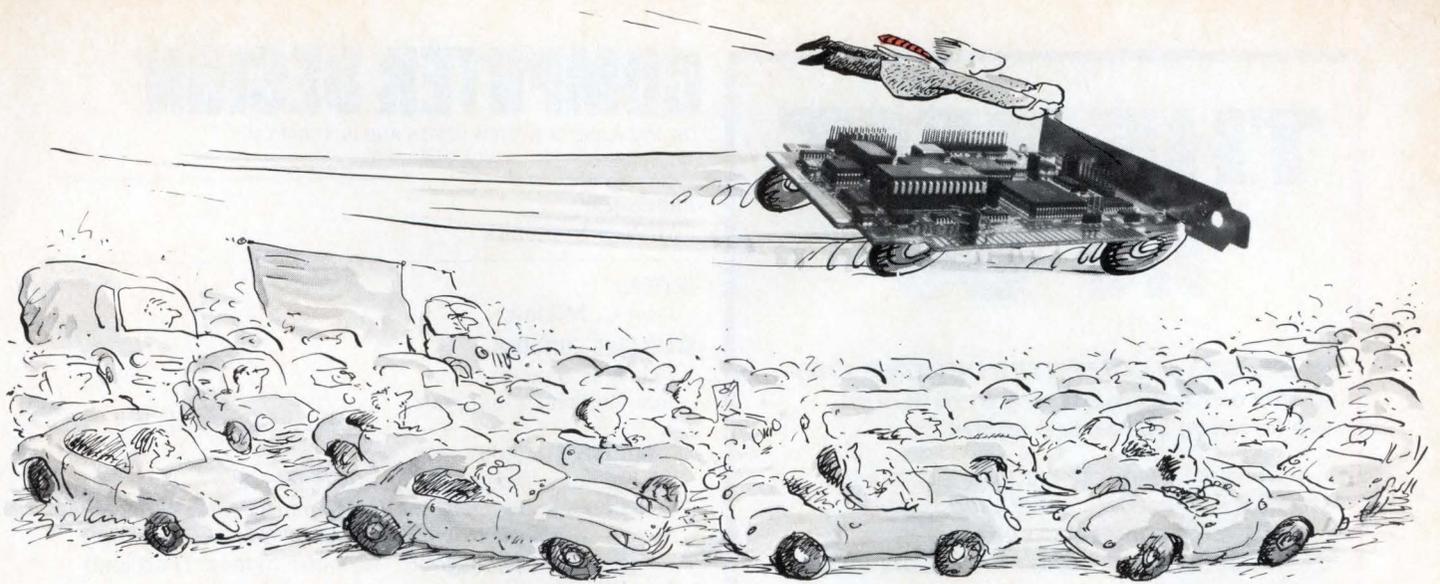
Last year, the U.S. Air Force spent \$10 billion on electronics—one-third of its entire procurement budget. The budget will be lower this year, but the amount still will be over \$8 billion. Almost one-half of the \$16 million spent by the Air Force for a single fighter aircraft is allotted to electronics.

The military/aerospace market isn't focused solely on weaponry. The Air Force Computer Acquisition Center at the Hanscom Air Force Base in Massachusetts will award a contract later this year for computer systems. These systems will include both processors and peripherals and will not require severe environment qualifications. The contracts have a potential worth of over \$3 billion.

Computer Design's editorial content has always reflected the concerns of its readers by providing them with the information they need to make intelligent decisions. Future issues of *Computer Design* will, therefore, contain much more information on government/military/aerospace electronics. Emphasis will be placed on the chip, board and system design levels, but we'll also cover other areas relevant to our readers. Your views on this major segment of the electronics industry are important to us. Any time that you believe that a particular area of the government/military/aerospace electronics complex should be stressed editorially, we would appreciate your input. Our charter is to serve our readers, and we can do so only if we know what they need. Call us anytime, or put your thoughts into writing and send us a letter. We're here to listen as well as to write.

A handwritten signature in cursive script that reads "Sydney F. Shapiro".

Sydney F. Shapiro
Managing Editor



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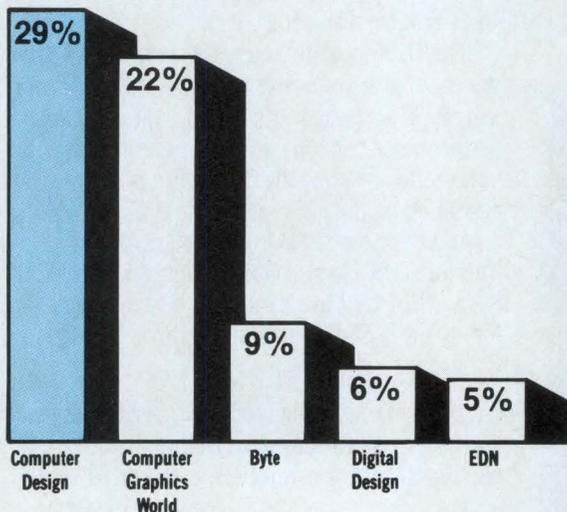
THE BEST IN '86

The results of **COMPUTER DESIGN'S** 1986 media enhancement study are in, and we've come out on top again!

Each year, we ask our electronics/computer system design readers to rate various aspects of the publications that are supposed to serve their technical information needs. We look for unbiased opinions and we're not looking for a pat on the back, so **COMPUTER DESIGN** isn't identified as the study's sponsor.

As in previous years, you rated us **best** in value to senior engineers, **best** in coverage of news on computer systems technology and **best** for a whole lot more.

Among that "whole lot more," more of you rated **COMPUTER DESIGN** best for technical information on **graphics systems** than any other competitive electronics/computer publication. Here's how we stacked up against the runners-up in the study:



These ratings are important to all of us at **COMPUTER DESIGN** because they tell us where we stand and how well we're meeting your information needs. Your answers tell our editors that their work is paying off and that we're on the right track.

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June 1-4

COMDEX/Spring, Georgia World Congress Center, Atlanta, GA. Computer industry trade show and conference geared to industry resellers, with over 600 exhibitors of computer systems, peripherals, software and related items. Includes 49 sessions on industry-critical issues.

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June 9-11

Vision '87, Cobo Hall, Detroit, MI. Conference sessions and exhibits focus on machine-vision technologies including optics, color, 3-D, robot guidance, cameras, sensors, software, and research and development. Sponsored by the Machine Vision Association of the Society of Manufacturing Engineers.

Information: Gerri Andrews, SME, PO Box 930, Dearborn, MI 48121, (313) 271-0777.

June 15-18

NCC '87, McCormick Place, Chicago, IL. National Computer Conference sessions concentrate on MIS and information processing as well as computer technology, exhibitor forums and special educational activities. Exhibitors span the entire gamut of the computer industry. Sponsored by the American Federation of Information Processing Societies, the IEEE Computer Society and other related groups.

Information: John Groundwater, NCC '87, AFIPS, 1899 Preston White Dr, Reston, VA 22091, (703) 620-8955.

June 28-July 1

Design Automation Conference, Miami Beach Convention Center, Miami, FL. Refereed papers, panels, tutorials and special topic sessions address all aspects of the use of computers as aids to the design process, from conceptual design through manufacturing. Sponsored by the Association of Computer Machinery and the IEEE Computer Society.

Information: Design Automation Conf, P.O. Pistilli, MP Associates, 7366 Old Mill Trail, Boulder, CO 80301, (303) 530-4562.

July 27-31

Siggraph '87, Anaheim Convention Center, Anaheim, CA. Technical sessions at 14th annual conference on computer graphics and interactive techniques will address graphics research developments, technology breakthroughs, application advancements and industry issues. Exhibits cover all areas of the graphics industry. Sponsored by the Association for Computing Machinery's Special Group on Computer Graphics.

Information: Siggraph '87 Conference Management, Smith Bucklin and Associates, Suite 600, Chicago, IL 60601, (312) 644-6610.

TECHNICAL COURSES

June 2-4

ISA Industrial Control Short Courses, Philadelphia Airport Hilton Inn, Philadelphia, PA. Choices of course subjects include data-acquisition systems, fiber-optic sensors, MAP networks and CIM data communications, machine vision, robotics and artificial intelligence, and expert systems. All courses are aimed at engineers and experimenters. Conducted by the Instrument Society of America.

Information: ISA Short Courses, PO Box 12277, Research Triangle Park, NC 27709, (919) 832-5599.

July 6-Sept 25

Knowledge Engineering Mentor Program, Pittsburgh, PA. Intensive 12-week course provides essentials of designing and implementing knowledge-based computer systems. First 6-week module concentrates on typical classes of problems that can be solved by artificial intelligence. The second 2-week module deals with design and implementation considerations. Participants in the final 4-week module will work in teams to use AI to solve their companies' problems.

Information: Valerie Tassari, Carnegie Group, 650 Commerce Court, Pittsburgh, PA 15219, (412) 642-6900.

July 13-15

Effective Implementation of Surface-Mount Technology, Univ. of Wisconsin-Milwaukee, Milwaukee, WI. Seminar will provide information for initiating surface-mount technology techniques at

either laboratory or factory levels, including what is needed to start, how to select equipment, what skills are needed and how to accommodate changes.

Information: Peter L. Tocups, Center for Continuing Engineering Education, Univ of Wisconsin-Milwaukee, 929 North Sixth St, Milwaukee, WI 53203, (414) 227-3125.

June & July

Seminars on Manufacturing Automation Protocol, various locations and dates. One-day MAP Management Overview is an introductory course on the technology; two-day MAP Technical Overview is an in-depth view of present and future technology; three-day MAP Network Planning & Design Workshop provides hands-on experience with software tools for the planning and design processes.

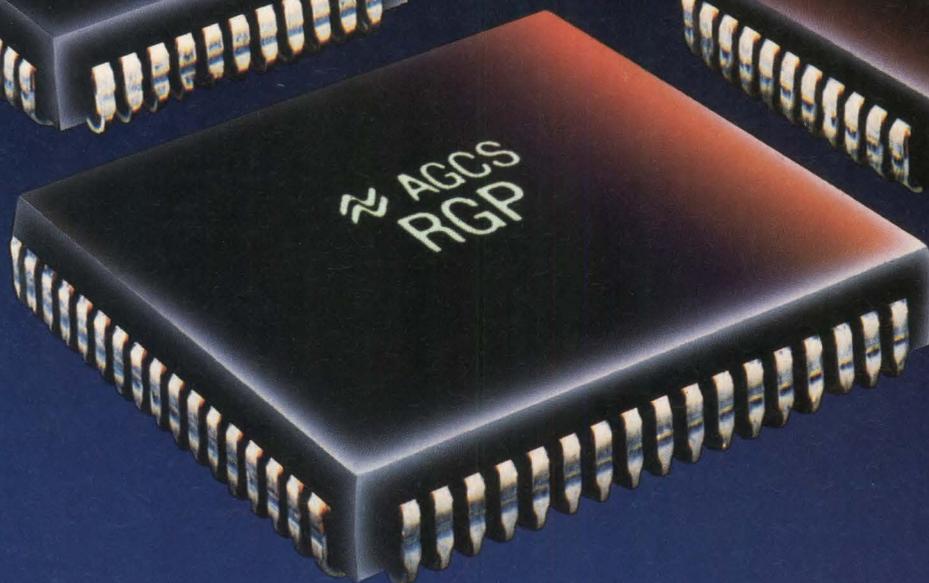
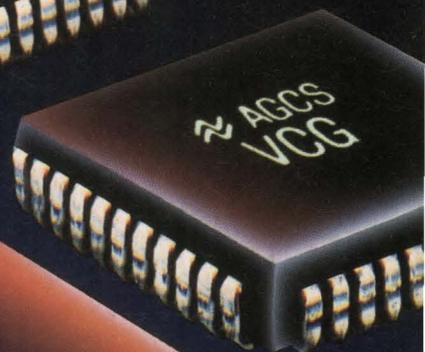
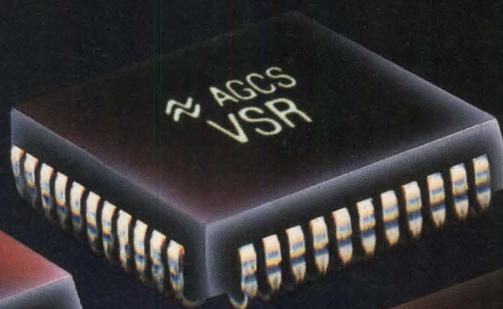
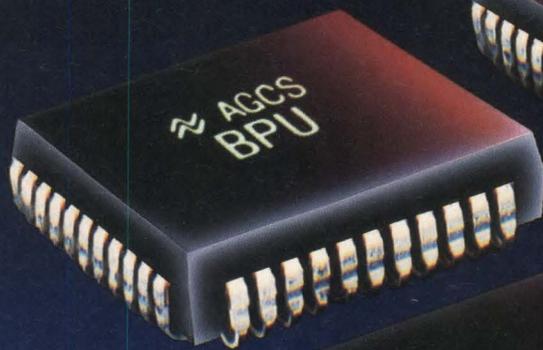
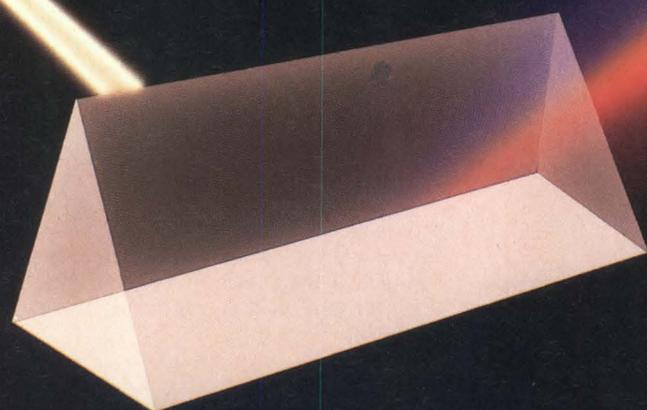
Information: C. Anthony Durham, Vice-President CIM Division, Youdon, 3221 West Big Beaver, Troy, MI 48084, (313) 643-8990.

June-Nov

Computer Network Design & Protocols, various locations and dates. Course emphasizes practical aspects of packet-switched network design and implementation using existing and evolving protocols. Coverage includes network requirements and design trade-offs, ISO protocol developments, layered network protocols, packet and message switching, gateway, hardware and software.

Information: Marilyn Martin, Integrated Computer Systems, PO Box 3614, Culver City, CA 90231-3614, (213) 417-8888.

Calendar announcements must be received at least three months prior to the date of the event and must contain full information, including specific location, description of the conference/course content and name, address and telephone number of person to supply further information. Programs and dates are subject to change.



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 **National Semiconductor**

CIRCLE NO. 11

Who's missing the boat?

I'd wager that I'm not the first or the last to respond to your March 15 editorial ("Taking the wrong tack," p 14). Dennis Conner's crew won because they used their feel, sailor skills and computer all together. The point you appear to be making is, Would the Stars and Stripes have won without a computer? Do some hypothesis testing: Would the vessel have won without a crew? Would it have won with a crew of people who never set foot on any ship in their lives?

You overlooked your own article. Their computer was a tool, probably connected to a great compass, a loran, a precision clock, and so forth.

Sailing the bounding main (or whatever it is) has come a long way. The navigator who used the astrolabe certainly had a tool over the one who gazed at the stars. And now we have satellite location devices.

Captain Kirk of Star Trek relied on the ship computer, Mr. Spock, and a band of superduper instrumentation as input, as tools. He, like Mr. Conner, used it to make the decisions. He had the intellect and the intuition of a true human sailor.

G.D. Peterson
Instrument Engineer
Ideal Basic Industries
Theodore, AL

I look forward to reading your editorial in each issue of *Computer Design*. Each editorial seems to broach some issue of consequence. By broach, I define it as "begin discussion of," which is the second definition listed in the Concise Oxford Dictionary, 7th edition. It is [in] this beginning of a discussion in my head that I find interest in your editorials.

Your March 15 editorial had two issues that I find worthy of comment to you. First, your use of the word "moot." Both my Oxford Dictionary and my College Edition Webster's New World Dictionary of the American Language define this word as meaning "subject to or open to discussion or debate." The Oxford edition also lists the word used in the context of law as "having no practical significance." From context, it would seem that you intend the latter interpretation. In any event, the use of this word without clearly defining it is in itself meaningless since it can have two precisely opposing meanings.

Second, your comment, "What happened to the sailor's instincts, the feel

of the wind and sea, and the ability to size up an opponent's boat and skills?" seems to be almost an exact replication of the comments that a scrivener or his supporters made when the printing press was first introduced. How, indeed, would the reading audience really appreciate a book that did not have the feel and hand of the scrivener? I regret that you are subjected to the lack of this feel in this letter since it was produced on electronic equipment and further copied with a Xerox machine to letterhead. Perhaps there is some virtue in marrying the sailor's instincts with the technology of the computer age. Maybe...

Dianna L. Adair
Technical Support Programmer,
Storage Systems Software
Unisys
Santa Clara, CA

John, we frequently disagree philosophically, but your editorial of March 15 completely missed the boat. The purpose of the exercise was to win the race. The techniques employed were directed to that purpose.

I am a computer buff and an ocean sailor. One of my first functions as a sailing crew member was to operate a magnificent Rolex watch so we'd have an edge at the start. Had we not been good sailors/seamen, we could not win regardless of how good my watch was.

Would you give up your terminal and text editor because it's supposed to be a test of magazine and editor? It's a tool, a willing slave that enables humans to express those things we do best—creativity, imagination, and agility. Pooh on you for not taking every advantage.

Bill Kennedy
W.L. Kennedy Jr. and Associates
Pipe Creek, TX

Who benefits from computers?

We whose interest and passions drive the computer revolution (to do the intellectual and robotic tasks that ought to free people from poverty and drudgery) see to date little of that freedom and less of that hope that science, in past years, engendered in the body politic.

Computer science advances at the speed of thought on the free enterprise express, yet its beneficial effects are slowed to a snail's pace by the unscien-

tific nature of the demand side of the distribution system, as well as the damage inflicted daily on the supply side by this deficiency.

We would all applaud the streamlining of work by and for the benefit of the operations and people involved in business. Yet, we make no explicit provision for the savings of effort to be passed on to the economy in general or to those who recognized and implemented the savings—if it was their own time and effort that was saved. The economy in general is made to contract if the savings are not immediately spent elsewhere. The individual is often made to suffer so much that no one in his right mind cooperates in such streamlining.

John Gelles
Ventura, CA

Mistaken identity

Thank you for your coverage of DY-4 products and capabilities in "Board-level systems set the trend in data acquisition" (April 1, pp 59-72). However, on behalf of our customer, Ursel Systems (Ottawa, Canada), I would like to draw your attention to a major error in the article.

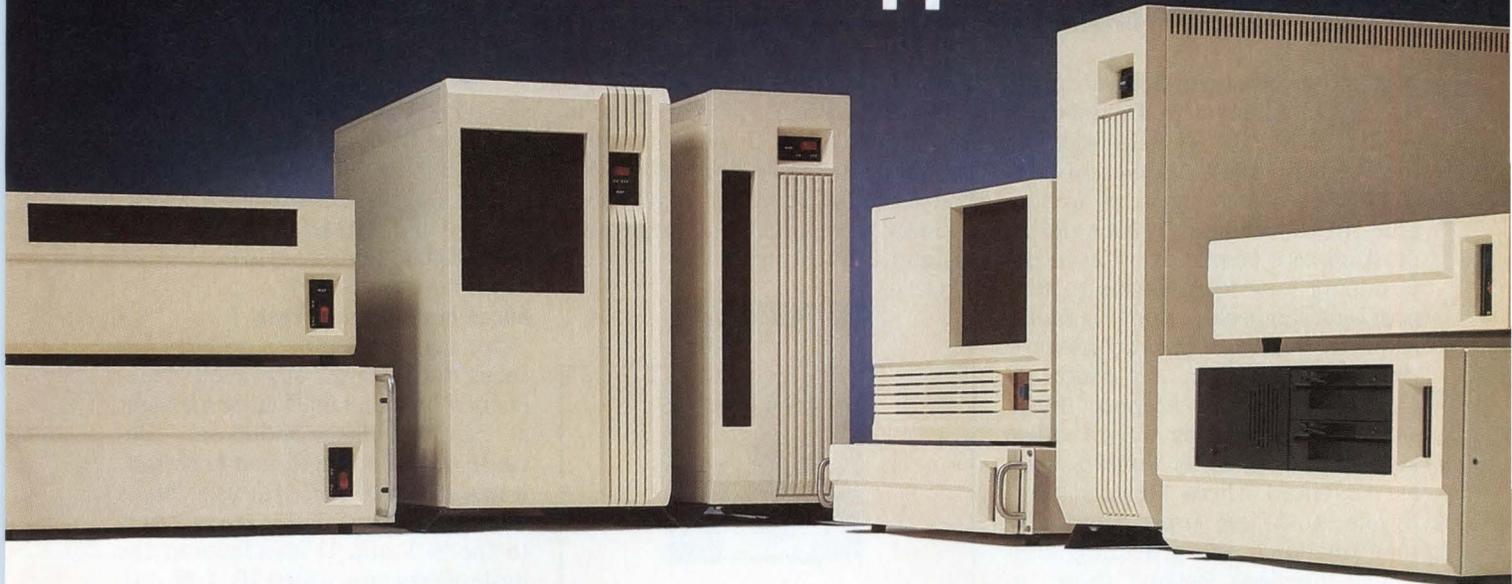
Ursel Systems is the prime system integrator of the air navigation system, with DY-4 providing the militarized computer subsystems based on the VMEbus. The photo on page 61 is of the Ursel system developed for its customers deHavilland Aircraft of Canada and Boeing.

Ann Dempsey
Manager, Marketing Services
& Corporate Communications
DY-4 Systems
Nepean, Ontario, Canada

Although the company name is clearly shown on the equipment, the failure to identify Ursel Systems as the prime contractor for the air navigation system shown in the photo was an inadvertent error. Our apologies to those concerned.

We also regret that another error appeared in that article in the caption to the chart on page 60. In reference to the market growth for data-acquisition systems, the caption should have indicated that the market for PC-based systems will more than triple between 1986 and 1993, while the market for minicomputer-based integrated systems will just about double.—Ed.

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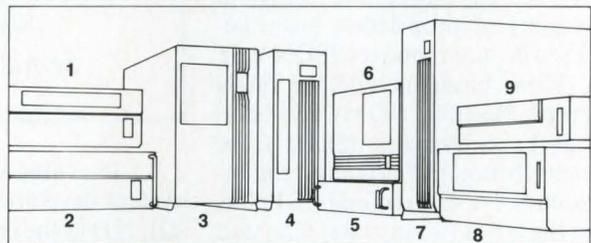
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6. Series 10 with 4 full- /8 half-height peripherals
12 slots VME; 10 slots Multibus II; 15 slots Multibus I
7. Series 7 DeskMate
7 slots VME, Multibus II; 10 slots Multibus I
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9. Series 3
3 slots VME, Multibus II; 4 slots Multibus I



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CIRCLE NO. 12

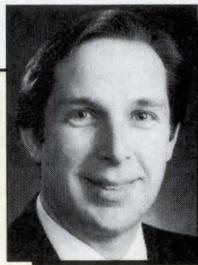
ISDN ICs move toward single-chip multilayer support

Of the seven layers defined in the Integrated Services Digital Network (ISDN), Layers 1 through 3—the Physical, Link Access and Network layers—are of primary importance to IC vendors. These vendors must make a crucial decision in determining how many layers to support on a single chip. Some vendors, such as National Semiconductor (Santa Clara, CA) and Motorola (Austin, TX), are keeping things simple by supporting only a single layer on a chip. Other vendors, such as Advanced Micro Devices (Sunnyvale, CA), are supporting more than one layer and providing additional functions beyond those included in the ISDN recommendations from the Consultative Committee on International Telephone and Telegraph (CCITT).

In addition to the different approaches taken toward layer support, other differences are evident in the variety of proprietary buses being used to interconnect ISDN chip sets. These buses include the ISDN Oriented Modules (IOM) and Subscriber Line Datalink (SLD) from Siemens (Munich, Germany), the Integrated Services Terminal (IST) bus from Signetics (Sunnyvale, CA) and the Serial Telcom (ST) bus from Mitel (Kanata, Canada). It's clear that even though ISDN sets a standard for global communications, in most cases, different chip sets won't be talking to each other because of the many different buses used.

IC vendors must also decide what part of the interface to support first. Most vendors have chosen to put their initial energies into the S/T interface because it's been completely defined, while the U interface has not. The U interface is a twisted pair of wires from a local central office—the local telephone company switching station—to a residence or

a business. When the U interface is fully defined, which it should be in 1988, then more U interface chips should be available. But availability will probably be influenced by subscribers' acceptance and implementation of the T1 interface.



"Because of our strength and expertise, it made a lot of sense for us to focus on basic access."
—Fred Wickersham
National Semiconductor

T1 is a high-speed digital carrier system developed by AT&T (Holmdel, NJ) in the early 1960s to concentrate the number of voices that can be carried over a pair of copper wires. T1 provides 24 channels of time-multiplexed information to be transmitted/received over a four-wire (two twisted-pair) connection at the rate of 1.5 Mbytes/s. Chip sets are emerging from companies such as Dallas Semiconductor, Exar and Mitel to handle this interface.

With T1 transceivers available on private branch exchanges (PBXs), the opportunities for bypassing the central office should increase, thereby placing increasing pressure on the central office to offer T1. The result may be a waning market for the U interface. Vendors such as AMD downplay the significance of the U interface for this reason.

The idea that device functions should be aligned with specific layers is key to National Semiconductor's ISDN chip set. The chip set currently includes three chips—the TP3400, TP3410 and TP3420—as well as the HPC16400 microprocessor.

Focus is on basic access

"Our strength has been on line-card focus in the past," says Fred Wickersham, product marketing manager at National Semiconductor. "Because of our strength and expertise, it made a lot of sense for us to focus on basic access." Basic access refers to the S/T and U interfaces at the basic access rate, called 2B + D. "In the PBX, that portion is going to turn into the S interface and will digitize the local loop. The central office environment will be focusing on the U interface and will digitize the longer subscriber loops." The S interface is a four-wire connection used inside of a building—usually a business—to connect local terminal equipment.

For the S interface, National Semiconductor's TP3420 will be available in samples later this year. The TP3420 can function at either end of the S interface, residing in the terminal equipment, terminal adaptor, network terminator or line terminator functional blocks. Configurations may be point-to-point or point-to-multipoint. In point-to-multipoint configurations, the device handles all contention resolution functions needed to control access to the D channel.

The TP3420 aligns only with Layer 1, the Physical Layer, and provides a digital, hard-wire connection only. For Layers 2 and 3, the company provides the HPC16400, which is a 16-bit controller specifically for use in National Semiconductor's telecommunications products.

"A significant portion of the TP3420 has been standardized by CCITT," Wickersham says. "The

Steven L. Martin
Contributing Editor

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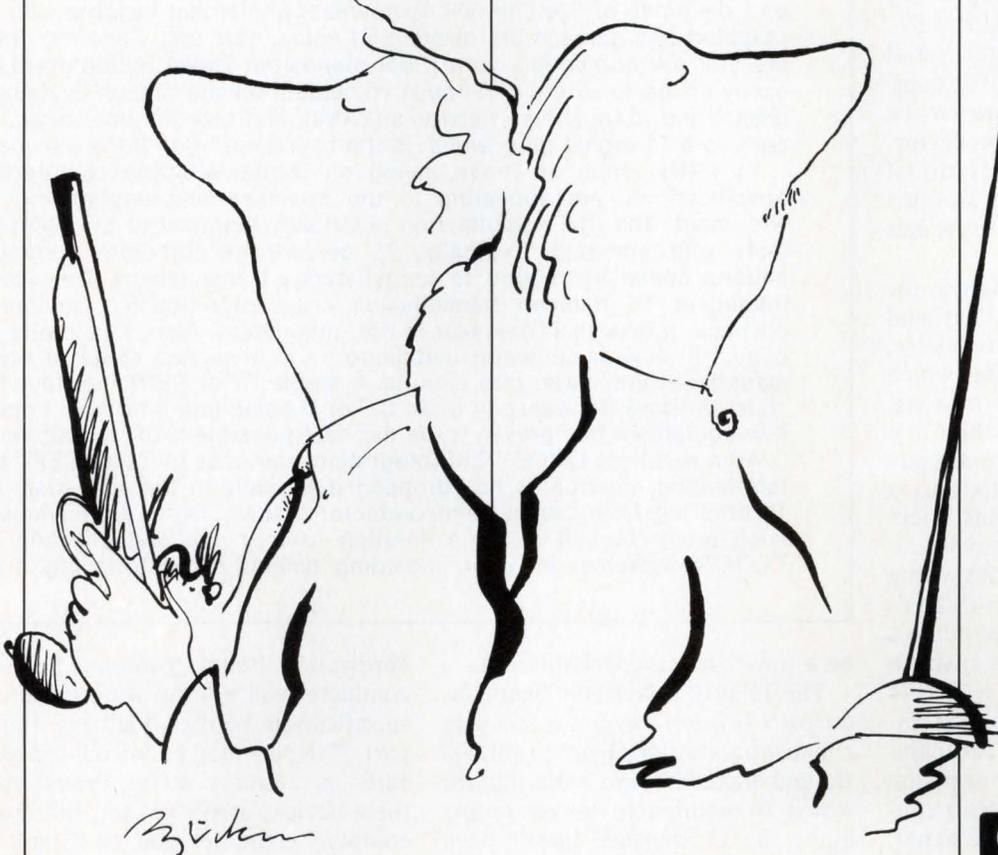
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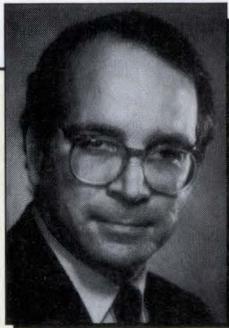


**HEWLETT
PACKARD**

differences come in when you say how much, if any, of the upper layers should be a part of the same Layer 1 chip. We've chosen to have Layer 1 completely separate from Layers 2 and 3. Others choose to put some portion of Layer 2 into the Layer 1 chip. We think that our approach provides a little more flexibility and allows advantages for the processor in terms of flow control and efficiency."

Another advantage to National Semiconductor's approach is the interface scheme chosen for communication with other chips in the set, according to Wickersham. There are two interfaces: one for synchronous transfer of B- and D-channel information, and one for control and status. The first interface features a selection (via a control register) of several different formats for the multiplexed B and D channels. This feature makes the chip-to-chip interface from National Semiconductor all-encompassing of proprietary schemes, such as SLD, IOM and ST. The second interface is the serial Microwire/Plus interface. The company claims that this interface can be easily emulated with any processor. Unlike other vendors, National Semiconductor emphasizes an open approach that doesn't lock users into the entire chip set.

The TP3400 Digital Adapter for Subscriber Loops from National Semiconductor is used for two-wire, short subscriber loops, for which there are no CCITT specifications. "Everybody knows that there's a significant amount of wire already installed for PBXs, and it's only a single twisted pair," explains Wickersham. "Ideally, a company would not have to replace the entire wiring system when it switched to ISDN." The TP3400 would accommodate a single twisted pair in a PBX environment. It supports the 2B + D (144 bits/s) data rate that ISDN requires, along with additional bits for maintenance, and it allows transmission up to 1.8 km. The twisted pair consists of a transmit and receive signal, so operation is full-duplex. It operates in burst mode and is designed to



*John Merritt
Product Manager
Dallas Semiconductor*

High-speed digital transport options now available

The Integrated Services Digital Network (ISDN) encompasses a wide range of data transport options, of which the most publicized is the basic rate interface—2B + D. Publicity has focused on the efforts of chip and system vendors to standardize the 2B + D interface for Customer Premise Equipment (CPE) interfaces. It will be many years, however, before basic rate services have a significant impact on worldwide communications due to the high installation cost of 2B + D. The initial installation of the basic rate will require a massive reworking of control and switching functions.

A higher capacity, primary rate standard (23B + D) is based on existing T1 technology. T1 is a twisted-pair, high-speed (1.544 MHz) digital carrier system developed by AT&T in the early 1960s to transport digitized pulse code modulation voice over long distances. Multiple T1s are bundled together for transmission over coax, optical fiber, microwave and satellite links. These circuits interconnect the regional Bell operating companies with long-distance carriers such as AT&T, MCI, LDS and Sprint. CEPT, at 2.048 MHz (30B + D), is the European equivalent to T1.

T1 is experiencing rapid growth fueled by the massive data-transport demands of Fortune 500 companies. Equipment vendors who anticipated this demand are offering T1 voice, data and video multiplexers that are compatible with ISDN standards. These multiplexers are easily linked to existing in-house voice/data private branch exchanges (PBXs) and to local area networks (LANs), and give the user direct access to a T1 digital pipe, which is the backbone of all ISDN services.

T1 LANs, such as those based on Digital Multiplexed Interface specifications, are appearing in the business and engineering environment. The DMI specification is virtually identical to the ISDN primary rate standard. Typically, 75 percent of corporate communications costs are related to long-distance transmission. The use of intelligent T1 reduces transmission costs significantly; equipment payback in less than one year is not uncommon. Also, T1 circuits are competitive with projected installation and in-service costs of equivalent-bandwidth basic rate circuits. A single T1 or CEPT interface has 10 to 15 times the capacity of an S, T or U basic rate interface. Primary rate equipment has proven to be the best possible ISDN investment.

As a result of CMOS VLSI integration, the cost of T1 or CEPT line termination electronics has dropped drastically in the last year. The T1 chip set from Dallas Semiconductor (Dallas, TX) is an example of such integration. It offers a solution to four challenges facing the T1/CEPT systems designer, including twisted-pair interfacing; fram-

be a low-cost, practical solution.

The TP3410 is National Semiconductor's U interface. It's a two-wire connection for loops up to 18,000 ft, and includes echo cancellation, which is required in longer loops. Since the U interface hasn't been completely specified by CCITT and the T1D1 committee (the U.S. stan-

dardization body), National Semiconductor will wait for the complete specification before finalizing this part. The part may be introduced as early as January 1989. Prices on these devices aren't yet set, but the company estimates that an S interface kit including an HPC16400 would cost \$40 to \$50.

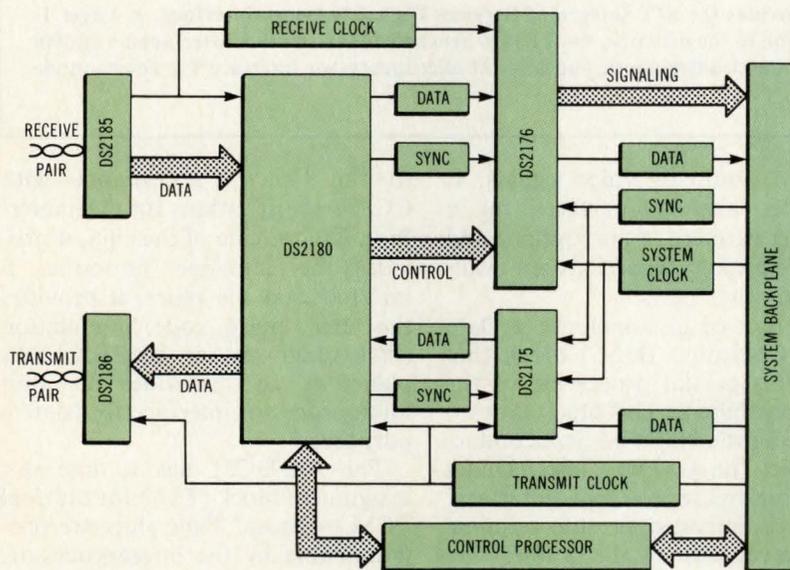
ing and synchronization; link monitoring and control; and rate buffering to equipment backplane.

The DS2186 Transmit and the DS2185 Receive Line interfaces eliminate off-chip precision components and manual tuning required in existing transmit-side wave shaping and in receive-side clock-extraction circuitry.

The DS2180 T1 and DS2181 CEPT transceivers perform link supervisory functions and are compatible with the latest T1 and CEPT network framing standards. These chips have a flexible feature set that allows for stand-alone operation, or they may be easily mated to host microcontrollers for enhanced control and monitoring capability.

Equipment backplanes usually run at rates different from the incoming T1 and CEPT lines. The DS2175 and DS2176 are special-purpose elastic buffers that adapt incoming and outgoing data to equipment clock frequencies.

This chip set reduces system design cycles from years to months and occupies less than 10 in.² of printed circuit board area.



In a joint development project, Motorola (Phoenix, AZ) and Northern Telecom (Minneapolis, MN) are developing three ISDN chips, one of which is the S/T interface chip. A second chip is the Dual-Data Link Controller (DDLC), which is the Link Access Protocol in the D channel (LAPD) chip. And the third chip

is the U interface. Prototype silicon is available on the S/T chip, which is undergoing ISDN field trials in Phoenix. The S/T interface and DDLC will be available early next year in samples, and the anticipated sample date for the U interface is late next year.

"We've taken a partitioning ap-

proach that goes along the open systems interconnection model for layer partitioning, in that our S/T chip is Layer 1 functions only," says Neil Wellenstein, communication segment strategic marketing manager for Motorola. The chips share a common serial bus—the Interchip Digital Link (IDL)—that carries 2B + D along with maintenance information. The bus clock rate is the same as the primary rate (the T1 rate). "That's one of the advantages we think our definition has over some of our competitors," says Burt Cutler, marketing engineer for Motorola. "Our bus structure supports both basic rate and primary rate data transfers, so you can have more than one transceiver sitting on the bus."

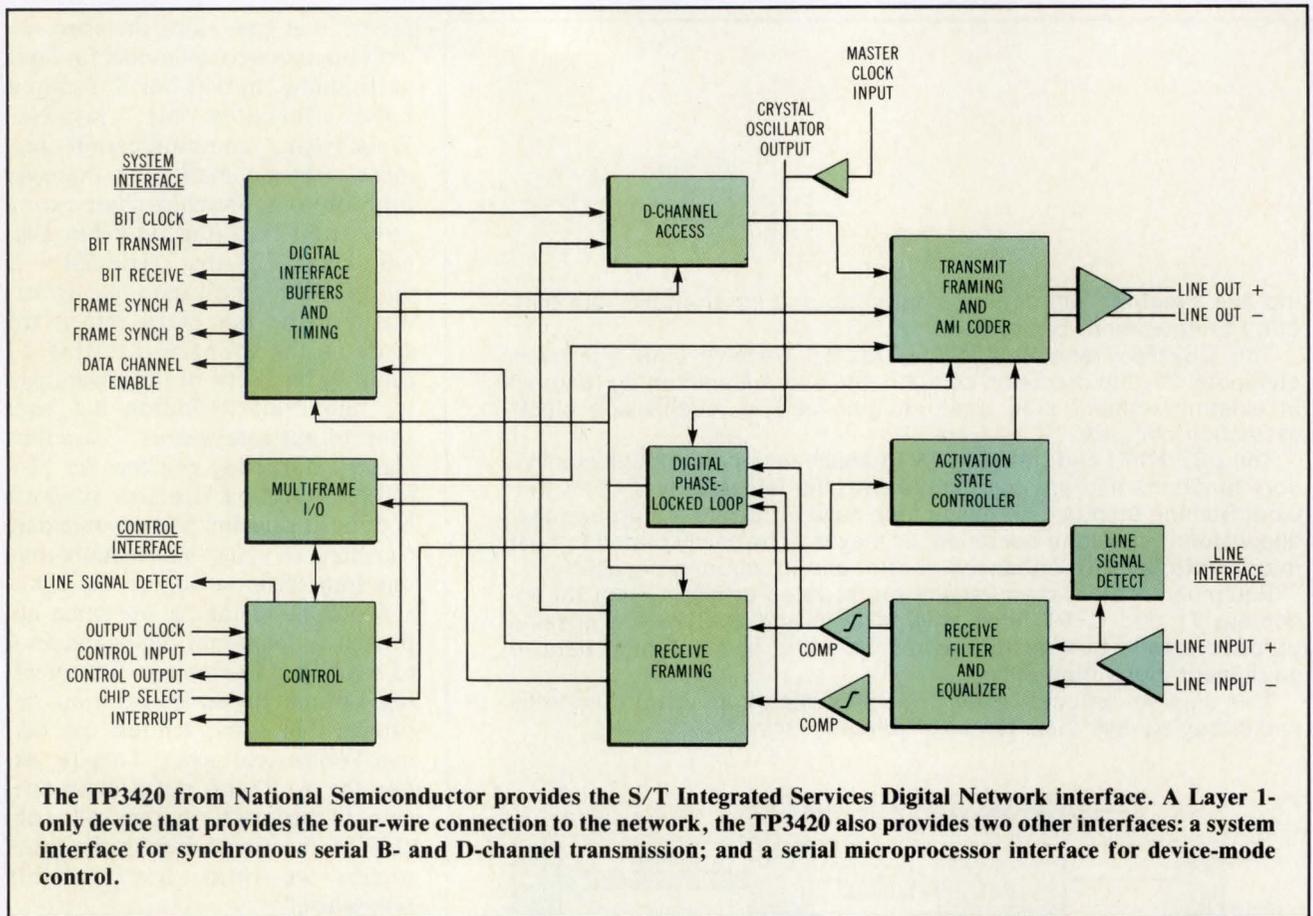
Motorola is taking the same approach as National Semiconductor to layered partitioning. Commenting on the higher integration approach that some vendors are taking, Wellenstein says, "They're taking the route of put-it-all-in-one-chip. In the long term, that will probably be the trend, but in the initial phases we think it's probably premature."

Motorola's U interface chip will meet the North American T1D1 definition of 2B1Q, which is still not definite. This will also be a Layer 1-only IC. The DDLC, a Layer 2 function with an interface into Layer 3, is a microprocessor peripheral part designed to work with the Motorola 68000. Motorola is the only vendor to offer a 16-bit microprocessor interface to its ISDN chip set.

Combining layers, adding features

AMD's focus is on the S/T interface. Four chips are offered to support functions at this interface point—the Am79C30 Digital Subscriber Controller, the Am79C31 Digital Exchange Controller, the Am7936 Subscriber Power Controller and the Am7938 Quad Exchange Power Controller.

"The key difference between us and the competition is the level of integration we have chosen to implement," says Ron Ruebusch, director of marketing at AMD. "For exam-



ple, if you take the line-card chip, the 7931, we do in a single device what others do in two or three devices. We focus on supporting industry-standard interfaces, and therefore we go from the S interface directly into the pulse code modulation backplane without proprietary interchip interfaces between the devices. It's all inside one part." Ruebusch claims that the differences are even more pronounced between the Am79C30 Subscriber Controller and competitive devices, such as the TP3420 from National Semiconductor. "From our perspective, the way you really get the cost out is to put it all on a single piece of silicon, and then you reduce the cost of that one thing," says Ruebusch.

The Dual-Tone Multifrequency (DTMF) function is built into the AMD Am79C30 as part of the main audio processor block. The main audio processor performs analog-to-digital and digital-to-analog conver-

sion of audio or voice signals. It provides analog interfaces for a handset earpiece, a microphone and a loud speaker—functions not available in other parts.

The device also includes a Data Link Controller (DLC) block that performs partial processing of the LAPD protocol. This block isn't included in the National Semiconductor part. The Am79C30 also includes an 8-bit microprocessor interface, which is intended for the terminal equipment side of the S interface, and provides both point-to-point and point-to-multipoint operation. AMD also offers the Am79C32, which is identical to the Am79C30 except that audio processing is omitted. The Am79C32 is intended for data-only applications.

On the PBX side, AMD offers the Am79C31, which provides the termination functions for one ISDN subscriber line. Up to eight pieces of terminal equipment may be connected

to the line in accordance with CCITT specifications for the S interface. On one side of the chip, it provides the four-line subscriber S interface; on the other, it provides the dual pulse code modulation (PCM) highway for the PBX backplane. It also provides an 8-bit microprocessor interface for control purposes.

The Am79C31 has a time slot assignment block (TSA) for the dual PCM highway. Time slots are programmable by the microprocessor. Control registers in the TSA permit selection of transmit or receive highways, specific time slots, and frame and D-channel offsets. The TSA can access up to 128 time slots occurring after the PCM frame synch pulse. The D channel can be processed for Layer 1 and partially for Layer 2 in the DLC block; the D channel may also be passed over the dual PCM highway for centralized handling. In quantities of 100, price per chip for

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the Am79C30 and Am7931 are \$39.25 and \$23.75, respectively.

AMD also offers two power controller chips, the Am7936 and the Am7938, both of which are bipolar. The Am7936 provides a regulated 5-V dc supply for the ICs contained in the terminal equipment. The Am7938 provides a regulated 40-V dc power supply for up to four S interfaces. "Power isn't a trivial function," asserts Ruebusch. "When the power fails at your house, you want to be able to make an emergency phone call and tell the power company that your power is out, or you want to be able to call the police. You expect your phone to work even when the local power is out." These chips provide that function.

How necessary is the U interface?

It will be some time before AMD offers the U interface, according to Ruebusch. Downplaying the immediate importance of the U interface, he says, "At some point you'll need a U interface—especially when you want to start serving a residential market—but from our perspective, it's going to be quite a while before there's a demand for ISDN in the residential market." He even questions the importance of the U interface in the business environment, since T1 appears to be gaining ground as the preferred PBX.

The problem with defining the U interface, Ruebusch points out, is that there are different equipment practices in different countries, and the loop lengths from central offices to houses and to businesses vary from country to country, depending on population density and so forth. This makes it very difficult to reach an agreement regarding the length of the loop. "We focused on the S interface for two reasons," says Ruebusch. "First of all, we felt it would standardize first, and it has. Second, we felt that the S interface was going to have the largest volume the earliest, because the key to ISDN is the ability to cleanly and efficiently transmit data on the same lines as you're transmitting voice. And who needs that data capability? The busi-

ness subscriber. They're using data in volume today."

Siemens has had ISDN chips in production for about a year. The CMOS chips are based on Siemens' IOM architecture. A goal of IOM architecture is flexible interconnection of devices for different applications, such as the use of identical devices in different applications by mode switching. Another goal is suitable partitioning in the initial phase of ISDN development into easily manageable units of complexity that can be forward integrated. Probably the most visible part of the IOM concept is the IOM bus and its predecessor, the SLD bus, which are used to interconnect Siemens' ISDN devices.

The SLD interface consists of three lines: the bidirectional data line, the 512-kHz clock line (SCL), and the 8-kHz data direction line (SDIR). In any transfer between devices, one device is defined as the master and the other as the slave. The master device then generates the clock and the direction control line. When SDIR is high, transfer of data is from the master to the slave; when SDIR is low, transfer is from the slave to the master. Thus, 32 bits are transferred in each direction during the 125- μ s frame period of SDIR. The 32 bits compose four 8-bit bytes—the B1 and B2 voice/data bytes, a control byte and a signaling or status byte.

The IOM bus is a four-wire connection that includes two data lines—one to transmit and the other to receive data. The direction of the data is from the subscriber perspective. Two other lines define data timing and frame synchronization. Serial bit timing is controlled by a 512-kHz clock. Frame timing is controlled by an 8-kHz frame synchronization clock.

The IOM bus is very similar to the SLD bus except that two data lines instead of one are used in the IOM, and the frame clock no longer serves as a direction toggle. The IOM bus represents an evolution from the SLD bus in that its frame structure includes address information and, therefore, it can be used in point-to-

multipoint applications. This capability makes it more suitable in certain portions of subscriber applications that require point-to-multipoint communications.

Siemens supports the S/T interface with the PEB2080, which can be used both in the terminal equipment and in the line card. The advantage to this is "when it comes to programming the device, you've got basically the same front-end drivers to program the various registers," says Alan Clark, telecommunications manager for Siemens. "All you do is program the device in slightly different modes to get it to operate either as a master or as a slave."

Separating the Layers

Siemens currently separates Layer 1 from Layer 2. The Layer 2 chip is the PEB2070 ISDN Communication Controller, which provides support for the LAPD protocol and includes a first-in, first-out buffer for efficient transfer of D-channel information. In addition to the IOM interface, it also includes an 8-bit processor interface. The advantage of this separation of functions becomes apparent when a company wants to build a piece of test equipment and needs to violate the D-channel codes, according to Clark. "Using our device, you can do that very easily. Our competitors' devices that have some of the Layer 2 functionality built into the Layer 1 chip will reject your sending that down the line."

Also available for supporting Layer 2 is the SAB82520 Serial Communication Controller, which is basically two PEB2070s, according to Clark. This means that two HDLC links can be put on the PCM highway, which is a requirement in a PBX switch since the highway is actually a dual highway that can carry error-checking information over one set of connections.

The PEB2095 ISDN Burst Transceiver Circuit is a two-wire connection that's essentially the same as the PEB2080, except that it works on two wires. The PEB2090 U interface, which is still being developed, will support the German and Euro-

pean standard line code (4B3T) from the central office. Siemens also has a commitment to develop a 2B1Q line code interface for the North American market.

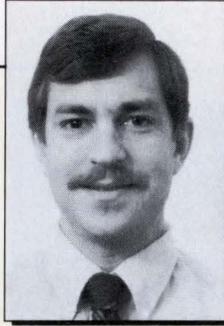
Regarding the possibility of higher integration devices, Clark says, "Our initial idea was to produce these modules to support the customers in a timely manner and then start doing more integration." Siemens has just produced silicon for a combined PEB2080/PEB2070, designated the PEB2085. The company also plans to integrate the codec/filter function (PEB2060) with the PEB2085 in a circuit, which will be called Digital Telephone Circuit. This would contain a comparable level of integration to AMD's Am79C30, but it won't be available until 1989. Samples are available for the PEB2085, and full production will begin in about nine months.

Signetics and its parent company, Philips (Eindhoven, the Netherlands), are working together on various levels of the ISDN interface. They have adopted the IOM architecture from Siemens, along with the IOM bus interface. Signetics also uses the SLD bus developed by Siemens.

In addition to the IOM and SLD buses, Signetics has added a wrinkle of its own in the form of its IST bus. The IST is a local highway for digital voice, data, text or images. It can link up to 31 terminals using twisted-pair cable up to 300 m long. The transmission speed is 1 Mbit/s, and the code scheme is Alternate Mark Inversion (AMI).

The IST's frame pulse is 8 kHz, which allows 128 bits/frame. An IST frame includes eight 64-kbit/s circuit-switched channels, B1 to B8. Each channel is equivalent to one of the ISDN B channels and can carry either voice or data. A frame also includes one simplified D channel, letting up to four terminals communicate in full-duplex mode simultaneously. The IST bus provides a low-cost solution using existing twisted-pair cable.

The PCB2310 IST bus interface, available in sample quantities, sup-



*Dale Gulick
Senior Engineer
Advanced Micro Devices*

Combining highly integrated ICs with shared memory interfaces

The central issues in designing terminal equipment, such as integrated voice/data workstations, include the division of functions among dedicated hardware and software running on a local communications processor, and software running on the system host CPU; and the need for shared memory (dual-port RAM) communications between the host and communications processor.

The first issue to consider when designing a voice/data workstation is partitioning. The communications function can be divided into tasks as specified by the ISO seven-layer model. At Layer 1 (Physical), the ISDN S interface is provided by the transceiver hardware. Layer 2 (Link) performs the packet protocol functions for the B and D channels. This task is subdivided between hardware at the low end and software at the high end. A data link controller (DLC), such as the Am8530, runs the software portion of the protocol. The Layer 3 (Network) functions for B and D channels are handled by software that runs on the communications processor. The Layer 4 (Transport) and higher functions are performed by software running on the host CPU.

The interface between the two processors is also a key issue in the design of terminal equipment. In order to provide a clean boundary between the third and fourth layers, Layer 4 software must be isolated from the hardware details of the processor running Layer 3. The cleanest way to provide this isolation is to use shared memory, which is subdivided into data buffer space and command mailboxes. User data is passed back and forth between the communications unit and the host system via the data buffer space. Control and command information is sent from one processor to the other by placing it in the other's mailbox and generating an interrupt, indicating that the mailbox needs to be read.

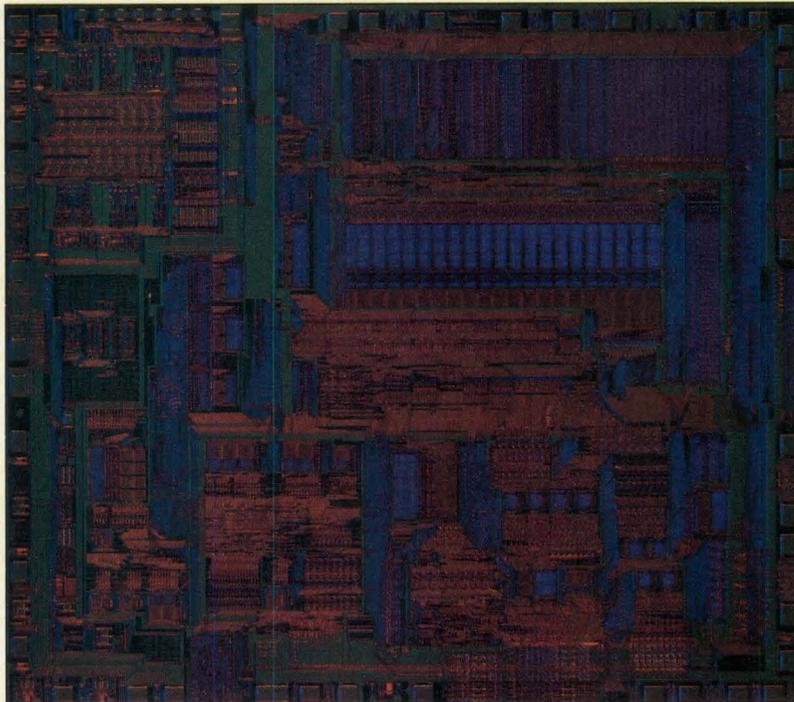
By dividing the hardware and software tasks along clearly defined boundaries, the host CPU isn't overburdened by the communications task, and the interface between the basic ISDN communications services and the user's applications software can be standardized.

An example of such a system is one that includes an Am79C30 Digital Subscriber Controller (DSC) and an 80188 processor. DSC provides the S interface transceiver (Layer 1) functions defined by International Telephone and Telegraph Consultative Committee standard I.430, the digital telephone functions and the D-channel packet protocol processing (DLC) functions. Also, a multiplexor that routes B- and D-channel data and a serial interface that connects to the B channel DLC are provided.

B-channel packet protocol processing is performed using a separate DLC. First-in, first-out buffers and direct memory access are required to reduce overhead associated with interrupt processing related to data movement.

The 80188 processor provides the CPU, three timers, two DMA channels (used to service the B-channel FIFOs) and an interrupt controller, all in a single package. The software for Layers 2 and 3 of both the B and D channels is run on the 80188. The arbitration of conflicting accesses to the shared RAM by the 80188 and the host CPU is performed by the dual-port memory control logic block.

This combination of highly integrated ICs with a shared-memory interprocessor interface provides a cost-efficient ISDN solution.



The Am79C30 Digital Subscriber Controller from Advanced Micro Devices is a high-integration device that supports the Link Access Protocol in the D channel and includes useful functions such as dual-tone multifrequency for dialing, codec and filter for audio processing, and an earpiece driver.

ports the IST interface. The PCB-2310 is an interface between the IST bus, an 8-bit microcontroller and the SLD bus or a PCM30 terminal highway (a 30-channel European standard PCM highway).

The PCB2390 is a line transmission termination device (a U interface), which will be available later this year. It will use 4B3T line code and include echo cancellation. The PCB2390 consists of two separate chips: one implements the analog functions, and the other implements the digital functions. "It wasn't easy to implement these functions on one chip," says Nabil Damouny, manager of applications engineering at Signetics. "We realized that from the very beginning. The next step will be to integrate the two chips."

Intel (Santa Clara, CA) offers two ISDN-related products—the 29C53 Digital Loop Controller and the 29C48 Feature Control Combo. The 29C53 is what other vendors call the

subscriber controller or the S/T transceiver or interface. The 29C48 is a coder/decoder (codec) with filters for voice conversion. Intel's family of telecommunications products is called the Subscriber Line Datalink (SLD). Intel uses the SLD bus to connect all its telecommunication components.

The 29C53 satisfies the CCITT recommendations for both the S and the T interfaces. It's a transceiver/controller with three major blocks and two internal buses. The blocks are the line interface block, the D-channel processor and the SLD interface unit. The device also includes an 8-bit microprocessor interface and an SLD status and peripheral interface. The microprocessor interface lets the 29C53 function as a peripheral to a microcontroller. All internal status and control registers are accessible via this interface and the SLD interface. The peripheral interface circuit is an

auxiliary port for controlling auxiliary peripherals, such as power controllers.

The D-channel processor has three basic sections: the high-level data link controller (HDLC) section; the FIFO section; and the control and status section. The HDLC section performs some of the basic LAPD protocol functions. The FIFO section consists of two 32-bit buffers—one for transmit, the other for receive. And the control and status section monitors the FIFO data levels and the HDLC section for progress. The SLD interface provides half-duplex, 512-kbit/s communication with other devices incorporating SLD interfaces. This SLD interface unit consists of shift registers and serial-to-parallel converters. Data from the internal serial bus and SLD interface are stored in the interface before being passed on.

While the 29C53 includes D-channel processing similar to the AMD Am79C30, it doesn't include the codec and filter function and other audio functions that the Am79C30 includes.

Intel also provides software with these chips. "What puts us in a unique position is that we have introduced a comprehensive solution," says Patrick Weston, ISDN marketing manager for Intel. "We haven't merely introduced an interface chip; we've brought to the market a software package as well." The ISDN standards call for a comprehensive protocol implementation for the signaling channel, and that protocol can represent a significant software development, according to Weston. The software supports Layers 2 and 3 of the ISO model, and was developed for Intel by Dale, Gesek, McWilliams and Sheridan (Mount Laurel, NJ). But Intel isn't the only vendor offering a software incentive. AMD also offers software. In fact, AMD wrote its own software so that it could gain greater knowledge of the ISDN market to better serve it.

Mitel, both a PBX manufacturer and a semiconductor house, is a long-time supplier of telecommuni-

cations ICs. The company offers an ISDN IC—the 8972 two-wire transceiver—that at least partially meets current U interface specifications.

The 8972 is capable of transporting 2B + D over 3 km on 26-gauge cable with no more than 40 dB of attenuation. The U interface is specified at 5.48 km, or 18,000 ft. This chip is part of Mitel's Digital Telecommunications product family, which isn't completely ISDN-compatible. "Being one of the first suppliers of silicon to come close to the requirements of the U interface market, we took a fairly leading role in determining the ultimate standards in the U.S. market," says Al Hawtin, assistant vice-president of semiconductor marketing at Mitel. From this beginning, Mitel has moved on to complete the family. Mitel has 22 products in its ISDN portfolio, including products that support ISDN but aren't, strictly speaking, a part of ISDN. The product family includes T1 and CEPT products. CEPT is the European version of T1. Its primary rate is 2.048 MHz.

The 8972 incorporates echo cancellation, but the device has "an inherent limitation in that the line code chosen for that implementation is fairly simplistic," says Hawtin. "Called biphasic, it has transitions at two levels, which limits the loop length you can achieve." Mitel is working on integrating the 2B1Q code into a new device that will be available early next year.

The 8930, which is the S interface from Mitel, is purely Layer 1 in scope, except for an HDLC. The S interface has two distinct operating modes: the microprocessor-interface mode, in which the microprocessor sets registers and accesses the D channel and HDLC; and the network termination mode, in which the 8930 runs the interface without microprocessor support. This mode can be used in relatively simple network termination applications, saving component count in the network termination, according to Hawtin.

"The approach that we took is pragmatic," Hawtin says. "We decided to develop transport chips and

then develop functions that generally fit in tight association with the transport chips. We considered AMD's approach, but abandoned it." The reasons for not using AMD's approach, according to Hawtin, include the immaturity of the ISDN market and the need to remain flexible at this point. "We want some real field experience before we integrate more onto our devices," he says.

Mitel uses the ST bus for interchip connections. The clock rate is the CEPT primary rate, which is also used on the backplane of Mitel PBXs. With the ST bus, the primary rate is subdivided by an 8-kHz clock, creating time slots of 32 8-bit pieces of information every 125 μ s. Since this is the sampling rate of voice, it allows compression of 32 voice conversations into one of these channels. The ST bus uses four lines—a transmit, a receive, a 4-MHz master clock and an 8-kHz frame pulse line.

NEC Electronics (Mountain View, CA) is developing four different ISDN products, one of which is a U interface chip that will be in production later this year. The second is a LAPD chip for Layer 2 protocol support, and the third is a LAPB chip, both of which will be available early next year. The fourth product is the S interface, which will be in full production early next year.

The top priority at NEC is the U interface. Although there's not much information available on this device, NEC refers to the U interface as a two-wire connection up to 3 km from the PBX to the terminal equipment on the subscriber's premises. This interface is the counterpart of National's TP3400.

Market changes spur growth

"There was a big transition in the growth of the market tied to divestiture, which occurred in 1984—the same year that our company started," says Michael Bolan, vice-president of marketing for Dallas Semiconductor (Dallas, TX). Because of the divestiture, AT&T was forced to reveal the T1 specifications, and as a result, smaller, inde-

pendent companies were allowed to flourish. "We took a cue from the divestiture and put a whole development team in our company—a team whose goal is to develop a complete silicon solution for getting on and off the T1 network," he says.

The T1 chip set from Dallas Semiconductor is now nearly complete. As the major control and monitor element of the T1 link, the DS2180 Serial T1 Transceiver is the first, and most important, product in the set. The DS2180 performs the formatting, signaling and framing insertion on the outgoing serial bit string, running at 1.544 MHz. On the transmit side, it takes a number of outputs from codecs or beta channels, formats them and inserts appropriate AT&T-compatible alarm, signaling and synchronization information. This is done under the control of a host processor. On the receive side, a search is performed on the incoming serial data stream to find the embedded protocol and to synchronize to it. The receive side also monitors the integrity of the link, to ensure that the proper signal is getting through.

Other chips in the set include two line interface chips and two buffers. The receive line interface, the DS2185, takes the receive pair of wires (Rx +, Rx -), terminates them in a characteristic impedance, and extracts clock and data, which are then presented to the DS2180.

The transmit line interface chip, the DS2186, takes the signals T +, T -, and Tclk as inputs and drives the T1 transmit pair (Tx + and Tx -). The DS2176 is a receive buffer that adapts the rate of the output from the DS2180 to the backplane. This is required because the clock generating the input may have been thousands of miles away, and the signal may have a lot of jitter and wander on it.

The DS2175 is a buffer/rate adapter for the transmit side. If the equipment on the backplane is running at the same clock rate as the DS2180, then the DS2175 isn't required. Otherwise, the DS2175 is needed to rate-adapt for equipment that doesn't run at this rate. **CD**

Host-based tools edge out conventional development systems

Although traditional development systems continue to be available, they no longer dominate the market. The emulator, once the centerpiece of such systems, is losing effectiveness as a software-development tool, since simulation of specific processor chips now lets a large part of real-time software development take place entirely within a host computer. Inexpensive mock targets are used as emulator substitutes to allow full-speed software debugging, and more software debugging is being done on the target systems.

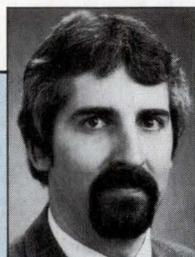
Traditionally, development systems were supposed to provide a unified facility for getting a prototype target to operate satisfactorily, whether the target under development was a conventional computer or an embedded part of some other system. Development systems were expected to let users bring the target hardware up, get its software functioning, and demonstrate that both could work together to carry out target system tasks.

In the past year, however, dramatic changes have occurred in computer hardware, bringing with them changes in development procedures. Processor chips have become more complex, sporting built-in development capabilities such as register-access commands. Processor clock speeds are also increasing, and the parts are becoming less easily manipulated by emulators. Meanwhile, system developers are finding that there are fewer hardware problems to solve during development.

Indeed, the number of software designers and engineers has continued to increase, and they, rather than hardware experts, have become the dominant group in microcomputer development. In fact, the ratio of software to hardware developers is now greater than five to one. As a result, demand for better software-development tools has been escalating, particularly for tools that meet

the requirements of real-time embedded systems.

There is increased acceptance by system developers of top-down, carefully defined software designs that start with requirements analysis and methodically blossom into pseudocode—even before any high-level language coding takes place. Real-



“Simulation is slow, often a thousand times slower than the actual target processor, and simulators give no insight into real-time asynchronous activity, such as interrupts.”

—Steve Dearden
Applied Microsystems

time procedures are being standardized and encapsulated in the form of software kernels. Debugging with source-code displays has also become widespread, and software debugging procedures are being refined and elaborated to ease the task of development.

Hosts dictate development

Traditional development system packages have included a host computer bundled with the emulator and software. While a few vendors still offer such computers, users now clearly prefer to provide their own hosts. The overwhelming choices are IBM PC ATs and Digital Equipment

Corp VAX/VMS systems.

Groups of software and hardware tools are being assembled into tailor-made development systems around these and other popular hosts. Because there are dozens of popular host computers, several important high-level languages and many processor chips to be considered, the number of specific tools needed to accommodate all the possibilities has mushroomed. No development-tool company would even pretend to be the originator of enough tools to satisfy all users. There are many companies, however, that specialize in one or another type of development tool. One may have a highly efficient C compiler, for example; another may have a cleverly engineered low-cost emulator or debugging software that greatly shortens the development cycle.

Through business agreements and an intricate network of cooperation, development tools are being interfaced, coordinated, and made available to users to meet their particular tastes and needs. Applied Microsystems (Redmond, WA), for example, offers compilers from at least four other vendors and debuggers from three vendors, as well as proprietary emulators. Other vendors, such as Oasis (Cambridge, MA), have become virtual supermarkets for software development tools, offering a selection of cross compilers, assemblers, linkers, debuggers, simulators, communications utilities and editors. “Many of our suppliers are very small companies,” says Gregory Kee, Oasis director of marketing. “They often have very elegant products but no concept of how to market them. Our technical staff’s expertise is in integration and porting to make products available on a variety of host systems. We make a compiler from one company work with an assembler from another.”

The trick in putting together a kit of development tools is not only to find those tools that are needed for a particular host and target system,

(continued on page 37)

Howard Falk
Contributing Editor

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The WY-30

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The WY-50

Our breakthrough 132 column display and ergonomic design made the WY-50 the world's best-selling ASCII terminal. It also features the comfortable Wyse keyboard feel and 16 dedicated function keys.

The WY-350 terminal is shown with a screen displaying a colorful bar chart and a keyboard in front of it.

The WY-350

This is the color version of our best-selling WY-50. Its big screen and range of 64 colors make complex data easy to read.

The WY-85 terminal is shown with a screen displaying a data table and a keyboard in front of it.

The WY-85

A dramatically better value in a VT-220 compatible: 14" tilt-and-swivel screen in your choice of green or amber, with fully compatible VT-220 keyboard.

The WY-99GT terminal is shown with a screen displaying a 3D pyramid graphic and a keyboard in front of it.

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*We make it better,
or we just don't make it.*

Host-based tools . . .

(continued from page 32)

but to get the tools to work together harmoniously. With target systems based on Intel processor chips, the need to have a debugger and a compiler specifically designed to work with each other is less critical than with Motorola targets. For Intel parts, OMS and OMS286 specifications are standard ways to transport information from the compiler to the debugger, and virtually any compiler and debugger adhering to these standards can be used together. There are no such standards for Motorola parts, so developers generally have to buy the compiler and debugger as a package.

Emulogic (Norwood, MA) sells a universal source-level debugging package, called Slice, with its in-circuit emulators. In addition, the company has written filter software that converts the output of specific compilers into information required by Slice. Compilers from Intermetrics Microtec Research, Green Hills Software, Aztek, Mannix, Whitesmith, Lattice, Software Development Systems and Intel can be accommodated in this manner.

Demands on emulation skyrocket

Using emulation to control and to track debugging and the execution of code in the target system is one of the cornerstones of the traditional development system. As the speed and power of new processor chips increases, however, it becomes more difficult and expensive to provide adequate emulation equipment.

Processor clock rates on several chips now exceed 25 MHz. Chips with clock rates above 50 MHz can be expected soon, and theoretically there is no barrier to clock rates of up to 500 MHz. The demands these clock rates make on emulator design and circuitry will result in a steep rise in equipment costs. At the same time, newer chips contain enhanced functions, such as cache memory and memory-management units, which make it increasingly difficult and expensive to read the internal state of the CPU by examining the

external pins connected to the chip.

As demands on emulation rise, chip manufacturers are embedding development capabilities in the processor chip itself. Some of the basic elements of the development system, including debugging routines, buses and arbitration mechanisms, are being incorporated directly on-chip in silicon. Specifications for chips such as the 80386, the V60, and the 68030 include built-in address comparators for software control. Motorola is expected to announce soon a new chip with a fuller set of on-chip debugging capabilities.

By using on-chip resources, software developers will be able to reach inside the new chips to debug, regardless of the clock speeds at which the chips run and despite the complexity and remoteness of the chips' architectures. Some vendors of software-development tools have recognized the on-chip movement.

Intermetrics (Cambridge, MA), for example, has initiated a drastic change in its strategy. Its original approach was to develop a broad line of assembler and compiler programs for popular chips, have those tools run on popular host computers, and have them work with any brand of emulation equipment that system designers were using. "We knew there were many potential customers using several different kinds of hosts, targets, and emulators, and that the cost of having engineers learn to use different equipment was high. Our approach was to provide software products that would work in the same way in all these different environments," explains Ronald Kole, director of software product development at Intermetrics.

That strategy was based on the idea that software would be developed on a host, while debugging and integration of the systems would be done through an in-circuit emulator. But Kole now believes the situation has radically changed. While software will still be put together on a host, additional development of the system will no longer take place through an emulator. Instead, resources on the target system will be

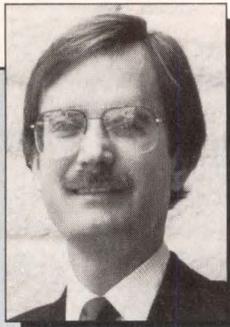
used to complete the development process. One of the key resources, Kole believes, is the real-time kernel. "We now support high-level control of low-level kernel operating systems, just as we previously supported high-level control of low-level emulators," says Kole. "From a technical point of view, both emulators and kernel operating systems offer a way for our products to communicate with an executing process in the target."

Why the Japanese favor kernels

The adoption of standard operating system kernels, dubbed Tron kernels by the Japanese, is part of the Japanese Sigma project to establish a single workstation standard. An ITron kernel targets industrial applications; a BTron kernel targets business machines. Under these standards, the designer of a new industrial real-time system would use a chip with the ITron kernel embedded in it, then proceed to develop the target system using a Sigma workstation. The government agency MITI is funding the Sigma project. NEC has proposed its V60 processor chip as the main computing engine for the Sigma workstation.

Tron kernels prepackage essential software functions, particularly those needed for real-time operation. To make such kernels effective development tools, standardization is needed. Through MITI's edict in Japan, the Tron kernels will control execution of code in target processors, and development will take place in the Sigma workstation environment. In the United States, no corresponding edict will be issued, but there are similar real-time kernels that are contenders for status as a de facto standard.

The VRTX kernel from Ready Systems (Palo Alto, CA) is among the contenders. Versions of VRTX are available for the Motorola 68000 series, the Intel 80286 and 80386, the National Semiconductor 32000 and Z80 chips, and the U.S. Air Force 1750 architecture. The latest version of VRTX handles up to 128 concurrent real-time tasks without slowing



*James F. Ready
Senior Vice-President
Ready Systems*

Multitasking kernels: the key to developing real-time systems

When developing real-time embedded computer systems, using a high-level language such as C or Pascal is only a partial solution because such languages weren't designed to address the special needs of real-time programming. To supplement high-level languages in many real-time systems, a multitasking kernel is now being used. The kernel manages the concurrent execution of various functions, or tasks, that the software must perform and it provides synchronization and communications between tasks in the system.

Stepping through the software development process illustrates the benefits of kernel-based real-time software design. Ideally, software requirements are developed with automated tools that use hierarchical functional decomposition or object-oriented methodologies. During the transformation of the requirements into a high-level design specification for software implementation, developers identify and group concurrently executing functions into tasks. Functions that execute periodically, such as a 40-Hz control loop, are examples of tasks found in real-time systems. With message queues and mailboxes, kernels also solve the problem of data flow from one task to another. Control flow can be mediated via kernel functions supporting event synchronization.

With concurrency and other real-time synchronization problems solved by a kernel-based design methodology, ordinary sequential programming techniques can be used within each of the concurrently executing tasks. Kernel calls, such as "wait for event" and "wait for message," appear at the beginning of the task code, for example, while the rest of the code is composed of standard high-level language statements. The kernel eliminates the need for additional complex user-written code to control and to synchronize real-time tasks.

Software module testing and functional testing can often be done on the host by taking advantage of the host's high-level language environment, if it's the same as the target language. If a kernel simulator is installed on the host, the simulator can assist limited multitasking testing. Queues, mailboxes, and other kernel features can be simulated. This simulation isn't equivalent to real-time operation yet, but problems with concurrent execution, such as resource contention and data-sharing conflicts between tasks, can be solved.

The basic criterion for concurrent programs is whether the correct result is obtained despite the order of execution. Problems such as race condi-

tions and uncontrolled use of shared resources can be uncovered during functional testing. The additional problems of meeting actual deadlines can be addressed during real-time operation.

A target processor chip, available on an off-the-shelf board, can be used as an interim execution target during kernel-aided debugging. S-records or hex-format object modules can be downloaded to the card, in addition to the real-time kernel. The real-time kernel can be downloaded to RAM on the interim target card. The Tracer debugging package from Ready Systems can be used for downloading. Many applications features can be tested in this environment before the actual target hardware is available.

The kernel presolves other problems, such as re-entrancy and synchronization problems. Though developers can still make design errors, adherence to the procedures and rules enforced by the kernel can reduce these errors. When a real-time system is interrupted while storing a 64-bit floating-point data item, for example, errors can occur if another piece of code runs before that item has been completely stored. With a kernel-based design methodology, problems of this kind are solved by design, rather than by eliminating bugs found in testing.

Kernel-based real-time system development also reduces the need for emulation. In many cases, emulators are overused today because programming practices are deficient. When developers apply sequential programming practices to concurrent, real-time system design, very subtle time-dependent errors are often built into the software, which makes debugging very difficult. Emulators and logic analyzers, however, will continue to be useful in detecting subtle bugs in the hardware-software interface.

A real-time kernel eases the task of multitasking design. But one last problem remains when traditional assembly-language debuggers, or even high-level language debuggers are used. These debuggers aren't able to take advantage of the capabilities of the real-time kernel. Debugging packages such as Tracer are used in conjunction with traditional debugging aids. Consequently, Tracer understands tasks, queues, mailboxes, and how a real-time kernel (such as Ready Systems' VRTX kernel, for example), maintains these data structures in memory. The user is shown the number of tasks waiting on a queue and the number of messages in it.

system performance. Additional features include 32-bit event flag signaling, semaphore counting, and a first-in, first-out option for communications queues.

Bridging the simulation-emulation gap

Simulators that run on host computers are becoming more widely used for development and partial software debugging for target systems. These simulators represent in software the functions of the target processor, and allow debugging of the programs that will eventually run on the actual target system. Such target system simulation lets software developers proceed independently without having to wait for operating target hardware or for access to a traditional, emulator-based development system.

Target simulation, however, isn't a panacea. Software operation can be observed under conditions that are similar, but not identical to, those in target hardware. The question is, how large and how important is the gap between software operation in a target simulator environment and actual operation in a target system?

If the gap is slight, and software bugs that remain after simulation are negligible, the use of emulator-based techniques for software development becomes irrelevant. If the gap is substantial, target software that performs satisfactorily during simulation will repeatedly fail to operate correctly in the target hardware. Hardware emulation that more closely approximates the final target system then becomes indispensable.

Target simulation lets software developers control the operation of a system without leaving the keyboard. There's no need to deal with components that could possibly be faulty or with physical connections. "You can do almost anything with our simulators," says R.T. Sarna, technical director at Avocet Systems (Rockport, ME). "The only thing we can't do is handle external real-time events. Our simulators will not know that one robot hand hasn't gotten there in time for the other hand to

```

15:   for (count = 1; count <= 100; count++)
16:   {
17:       beep();           /* 'Beep' at user.                */
18:       outscope();       /* Display ' ---> SOFT-SCOPE 2.0  */
19:       outlang();        /* Display ' ---> C-86 example    */
20:       outcount(count);  /* Display ' ---> Count = xx      */
21:       do_data();        /* Data reference demo.          */
22:       delay();          /* Slow display down.            */
23:   }
24: }
* reg
AX=0000 SP=0606 CS=2B44 IP=0000
BX=0000 BP=0000 DS=2B2B FL=0000 = 00 D0 I0 T0 S0 Z0 A0 P0 C0
CX=0000 SI=0000 SS=2AC6
DX=0000 DI=0000 ES=0000
* asm 12
12: main()
2A47:0000 56          PUSH  SI
2A47:0001 57          PUSH  DI
2A47:0002 55          PUSH  BP
2A47:0003 8BEC       MOV   BP,SP
* [ 'SUBMIT CTEST.CSD' completed ]
* -

```

Applied Microsystems' Validate/Soft-Scope debugger for IBM/PCs and compatibles handles target systems based on Intel processor chips, and works with the company's emulators. The upper portion of the display shows several lines of C source code, which is part of the code for the Validate/Soft-Scope debugger. The middle portion of the screen displays register contents, while the bottom portion of the screen displays assembly-language code.

shake it."

Avocet target simulators handle I/O by cycles. The value at a location, a port or a pin can be changed periodically after a certain number of cycles to ensure synchronization with the cycles of the simulated processor chip. I/O can alternatively be handled by polling. Whenever an input is taken from a given port, the next byte is taken from a designated file. Except for the slower time scale of simulation, these I/O modes correspond to those in actual hardware. Interrupts are handled in a similar fashion. A file is connected to a simulated interrupt pin. When the simulated interrupt occurs, a 0 bit is read from this file.

Simulation and debugging is done in assembly language. Users write their code, assemble it, and then put it on the simulator to find out if it will run. The simulators don't let target out-of-bounds memory locations be used. If errors occur, users can back up the execution to trace what has happened using an Undo key. When users want to know what

would happen if the value at a port, in a register, or in memory is changed, they key in a new value as if they were using a text editor. The screen contains data about the status of the simulated processor. Ports, pins, registers and memory locations are displayed, and the displayed values change as the simulation proceeds. Breakpoints can be set on instruction type, address range and many other criteria. Sarna says this approach is much faster for debugging and finding problems than is emulator-based software debugging.

Avocet software simulates chips such as the 6805, 6809, 8048, 8051, 6800, 8085 and Z80. Simulation of Texas Instrument's 16-bit 32010 and 32020 signal processing chips are next on Avocet's agenda. Avocet plans to support engineers who use small processor and controller chips. Recognizing the need for real-time debugging, Avocet sells Nicolet emulators together with software that uses the PC to communicate with emulator debugging commands and displays.

The new 64000UX development system from Hewlett-Packard (Colorado Springs, CO) is designed to include simulation-based software debuggers. Debuggers for 16- and 32-bit microprocessors will be introduced this year. The debugger for the 68020 will be out in a few months, followed by debuggers for other 68000 processors and the Intel 8086 family. HP is buying the basic software for these simulation-based software debuggers and will add its interface. The debuggers will also run in an emulation-based mode.

The necessity for emulation

In the eyes of emulator vendors, the shortcomings of simulation are enormous. "Simulation is slow, often a thousand times slower than the actual target processor, and simulators give no insight into real-time asynchronous activity, such as interrupts," says Steve Dearden, director

of product marketing at Applied Microsystems. "Emulators can be used for some code verification, but a point is reached when it's necessary to use target hardware."

Target systems may include two CPUs: one does the main computing, while the other handles controlling functions. In other systems, two or more complete processing units can be used in a multiprocessing mode. An important development task is controlling and observing communications between such processors. Simulation tools aren't available to handle this kind of task, but with an emulator on each processor, users can set triggering functions to break on communications.

During the past year, software tools for debugging, aided by emulators, have been refined for the user's convenience. Display of high-level source code during debugging is almost universally available, and a

mixed display of assembly language with high-level source-code lines is available from several vendors.

The Echo debugger from Arium (Anaheim, CA), for example, has one display mode that shows only a C source line. A second mode shows the source line followed by an expanded disassembly. The displayed source code is read from the original source file by a procedure that starts with the actual address from which the current instruction was fetched. The routine then looks into a debug tree, which was created in memory when the C source code was compiled, to find the source-code file and line number that produced the current piece of object code. In this way, a corresponding source-code line can be displayed for each element in a trace. If the code is looping, users can see the same line of C source code repeatedly displayed. The execution of C code through a dynamic display is visible, which differs greatly from a simple listing.

A window display formed by the XLD debugger from Motorola (Austin, TX) has a browse line that indicates the current point of execution in source code. About 15 lines of surrounding code are also displayed, with breakpoints marked on all code lines. Following any source-code line, the user can have a display of the assembler code generated by that line. Breakpoints will also be displayed in this assembler code, and they can be set on either type of code line. If users desire, the entire display can be assembler lines, and subroutine lines can be suppressed. Users can single step through either type of code lines, and move from one function to another function. The display can then immediately show the new function's source code.

Microtec Research, Northwest, and HP are among several other development-system vendors that now provide mixed debugging displays of high-level source code with the assembly language.

Switching from one language to another is simple with the Slice debugger from Emulogic. The user

This display of the Microtec Research XRAY68K debugger shows a line of assembler code in black, preceded by the line of C source code that produced it. The OUTCHR code module, an output facility for a program that calculates prime numbers, is being examined. The command window contains source-code and assembler-code lines (option symbols = on). In the data window, the values of source-code variables are displayed, including array flags. Hex code in the execution stack and the contents of registers are displayed in the two windows on the right. The debugger normally incorporates a software simulator for 68000 series processors, but versions are available that use emulated or board-mounted real targets.

can select whether code will be displayed in either C or assembly language. The screen will switch instantly from one choice to another, but there is no intermixed display of high- and assembly-language lines. A window shows target system status, registers and arguments as the user steps line-by-line through the source code. Users can step and trace by source-line instruction or by machine cycle and step over or into source-code call-to functions as well. A source-language debugger from Kontron Electronic (Mountain View, CA) has similar characteristics—user-defined windows and tracked variables.

Debuggers from compiler vendors

Some development-system vendors now feel that debuggers should originate with compiler vendors. "The number of man-years involved for us to write good source-level debuggers would be prohibitive," says Richard Leatherman, vice-president of marketing at Microcosm (Beaverton, OR). "Our best approach has been to ask the compiler vendors to write source-level debuggers."

These debuggers are written for software development only, but when debuggers are integrated into the Microcosm emulator, they have hardware breakpoints as well. Users can look directly into the target in which the software resides, so debugging can proceed in a real, rather than in a simulated, environment.

"For those compiler vendors who haven't written debuggers, we make the best accommodations we can," says Leatherman. "We're usually able to handle symbols in Tektronix extended hex and in the Intel object-module format. Unfortunately, that doesn't give us the ability to track items such as variables. But we can still get and use about 70 percent of the symbol information. For those who use Microsoft C and Lattice C, we haven't yet found any good source-level debuggers, but we do have linkers and locators that will at least let users load some symbol information."

As compilers become more effi-

cient, it becomes more difficult to build a good source-level debugger since efficient compilers use stack- and register-resident variables that are hard to handle. Microcosm's approach is to use a preprocessor that sifts through the source code and picks out the information required to handle such variables.

With the Arium Echo system, users can name the variable they want to observe during debugging. A display window opens and shows the named variable in its declared format (string, floating-point number, array or array of structures). No matter how complex the structure of the variable, it will be shown just as it was programmed. To provide the necessary information for this display, debug tables are set up at compile time. While the variable window is open, users can run the cursor across the displayed information and make any desired changes. The memory location used by that variable will be accessed by the debugger and indicated changes will be made. A variable can be corrected without having to trace through the various conversions it may have undergone.

A variable window available with the Motorola XLD debugger performs similar functions. This window is always updated to the present line of code, and as the code is run, the user can see the values of these variables change.

Recognizing that debugging software is powerful but often slow to use, Tektronix Software Development Products (Beaverton, OR) has implemented the TekDB debugger in firmware. Commands are complete English words, which the user has the option of abbreviating. Items in source code can be automatically located with the help of a Find command. An Unwind command pops activation records off the execution stack if a procedure has an error. Users can then manually make changes and continue with the debugging session without recompiling. With TekDB, users can go from function to function instead of from statement to statement, and they can step over subroutines.

Rationalizing the choice of a host

It has become clear that most users prefer to work with their own familiar host computers, which are also used for other tasks besides development. Though development tools are available for use with many different computers and workstations, the consensus has narrowed the choice to AT and VAX/VMS computers.

Developers who prefer AT hosts tend to use Intel chips; those who prefer VAX/VMS machines tend to use Motorola chips. Microcosm has used the PC as the host for its emulators since 1982. "We're proud of our foresight," boasts Leatherman of Microcosm. "Many engineers doubted the usefulness of the PC as a host. That attitude has changed dramatically." Many Microcosm customers who work with Motorola 68000 target chips, prefer to do their software development on VAX hosts or Apollo or Sun workstations.

Another factor contributing to a preference for VAX/VMS machines is if many workstations must frequently access central files. VAX computers offer good interconnection facilities between powerful central machines and workstations. In contrast, PC networking, has been less than satisfactory. Software developers accustomed to rapid compile and linking with VAX computers are dissatisfied with the slower AT operation.

Development tools from Tektronix, for example, are definitely oriented toward the VAX environment, from large VAXes to the VAXstation 2000. "With our Ethernet interface, which looks like any other peripheral on the network, the development system can be easily tied into the network," says Roger Crooks, marketing manager for Tektronix development products. "Tektronix tools are targeted toward large software-development projects, in which high-speed downloading is necessary. Support for other high-volume workstation, such as those from Sun, is under consideration."

Cadre Technologies (Providence, RI), a supplier of structured design

tools, initially made its product available only on Apollo workstations. Cadre now finds that whatever workstations are used by its customers, the workstations typically feed into a central VAX computer acting as a data base server. HP has adopted the company's Teamwork software as a 64000 development-system tool.

Among VAX users, single-user workstations (such as the Micro-VAX, which operates on a stand-alone basis) are gaining in popularity. At the same time, many development companies are moving up to more powerful VAX 8500 and 8600 central computers.

The HP 64000 development system has always had its own dedicated host, but the new 64000UX system is based on workstations from HP's Computer Division (Fort Collins, CO). The development hardware is housed in a separate card cage that connects to the workstation through a standard HP-IB instrumentation bus. Users still have to buy an HP workstation computer to get the development system to work, but that computer is no longer dedicated, so it can perform other tasks and can be network-connected to other hosts—including VAX/VMS and ATs.

PC software for 68000 targets

Until recently, PCs were used infrequently for development of target systems based on 68000-series chips because PC software for that purpose was unavailable. With Intel parts, however, users have had access to inexpensive compilers and to the linkers and the locators that are included with them. As a result, small development companies can do low-cost startups. Since competent low-cost PC development software has become available for Motorola parts, more system developers are working with them.

Quelo (Seattle, WA) specializes in software-development tools for the 68000 family. Quelo's customers typically generate code on a PC and then download it with Motorola S-records over a serial link to the target



"We expect performance analysis to be as important to software designers as emulators are to hardware designers."

*—Gordon Reid
Intel*

system. The company sees Amiga and Atari computers being used as hosts in the future, and it plans to offer tools for them. "Quelo is betting that Amiga and Atari will eventually become as important as the AT," says Patrick Adams, general manager at Quelo. "Because these computers are low-priced and 68000-based, users are able to do some software development on the host machine before they build their target machine." Adams also notes that another low-cost host, the Apple Macintosh, is 68000-based, and that Apple offers a \$100 set of software-development tools.

It's ironic that Motorola itself provides development software that runs only on the System 1131 Motorola host, a multiuser Xenix VMEbus computer. Driver routines let this host communicate with the Motorola HDS-300 development system. The software hasn't yet been ported to other hosts, and there appear to be no plans to do so, though Motorola's customers have urged the company to make its C source-level debugger available on other host computer systems.

Both Intel and Motorola offer performance-analysis tools, signaling the key importance of the software side of the development process. During the past year, Intel introduced the iPAT, (Performance

Analysis Tool) to meet the needs of embedded system developers. Unlike statistical performance analyzers, iPAT monitors and tracks every instruction and every line of code that is executed. It collects real-time data that are critical for embedded systems, and presents it in graphs, charts and histograms that change dynamically as the target system runs. In addition, iPAT will also produce a report that identifies each line of code that has been executed. Each high-level language statement is flagged by statement number, aiding the designer in building a test suite for the target system. The report tells designers the parts of the code that were executed and the parts that weren't used.

Accepting performance analysis

"The acceptance of performance analysis is still in its early stages," says Gordon Reid, marketing manager of development systems at Intel. "There was little interest last year, but it's picking up. We expect performance analysis to be as important to software designers as emulators are to hardware designers."

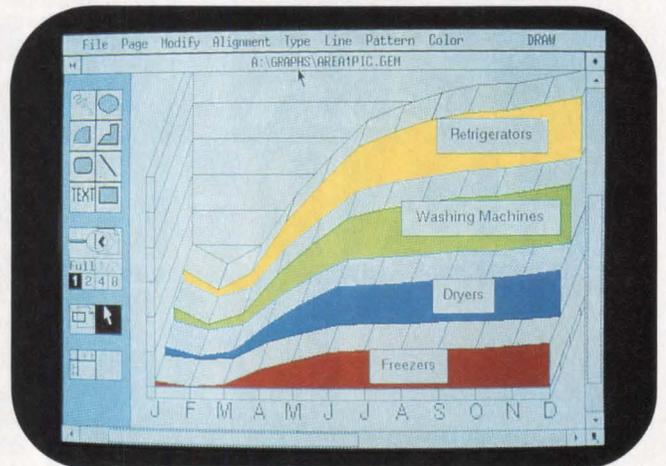
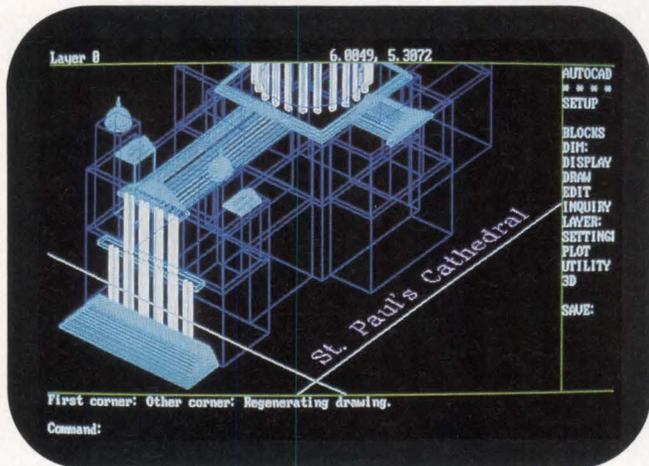
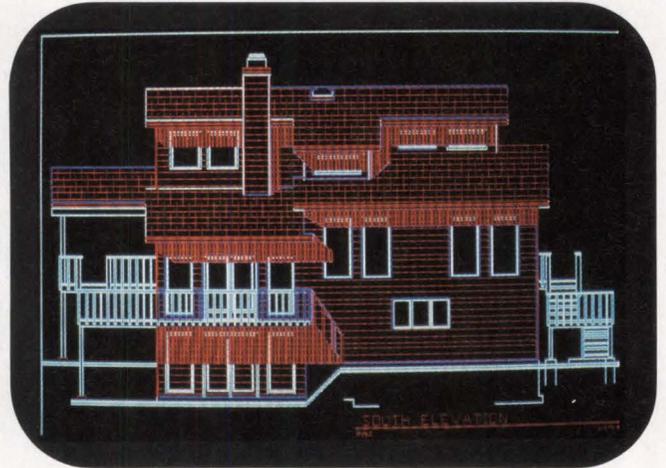
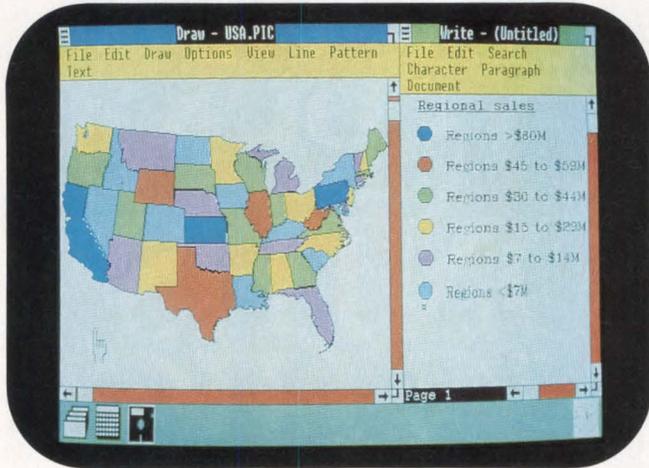
Motorola's System Performance Analyzer, which is a part of the HDS-300 development system, can be operated in a search and filter mode. In this search and filter mode, the analyzer can be given any combination (including AND and OR combinations) of address and data control lines or bit patterns. The information can also be viewed symbolically. There are four levels of triggering, and trigger events can be logically concatenated. Selected types of data can be captured, for example, only when interrupts from a particular peripheral device occur. The analyzer memory can be divided into four segments, and the user can send data that is taken before or after a trigger to any one of these four segments. **CD**

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<i>Maximum line drawing rate:</i>	<i>2.5M pixels/sec</i>
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CIRCLE NO. 19

Intelligent layout tools simplify gate array design

In an attempt to sell gate array layout to system designers, CAE vendors are beginning to offer intelligent systems that can select layout strategies for specific gate array families. By including such a capability, both the new Gate Array Worksystem from Tektronix CAE Systems (Santa Clara, CA) and the Gatemaster from Daisy Systems (Mountain View, CA) come close to making gate array layout a push-button task.

Introduced this month, the Gate Array Worksystem from Tektronix is the most recent of several systems that integrate schematic capture, simulation and automated gate array layout. One distinctive feature of the Gate Array Worksystem is that all layout parameters are entered directly on the schematic. This system also provides Turnchip modules, which are described as expert systems that drive the Merlyn-G layout

program for specific gate arrays. The Turnchip modules and the Merlyn-G are both from Tektronix. Similarly, Gatemaster's Autolayout feature provides foundry-developed layout runs for several gate array families.

Systems such as the Gate Station from Mentor Graphics (Beaverton, OR) and Gards from Silvar-Lisco (Menlo Park, CA) also provide schematic capture, simulation, and automatic placement and routing for gate arrays. Fred Cohen, director of IC layout for Mentor, claims that Mentor can support any two-level metal CMOS array and that the company doesn't really need software to customize its Gate Station tools for specific gate arrays. "We're the industry leaders in terms of gate utilization, and we consistently get 99 percent plus routing. Other vendors may supplement their tools because they don't get these results."

In response, Tektronix and Daisy representatives say generic layout tools force users to be layout ex-

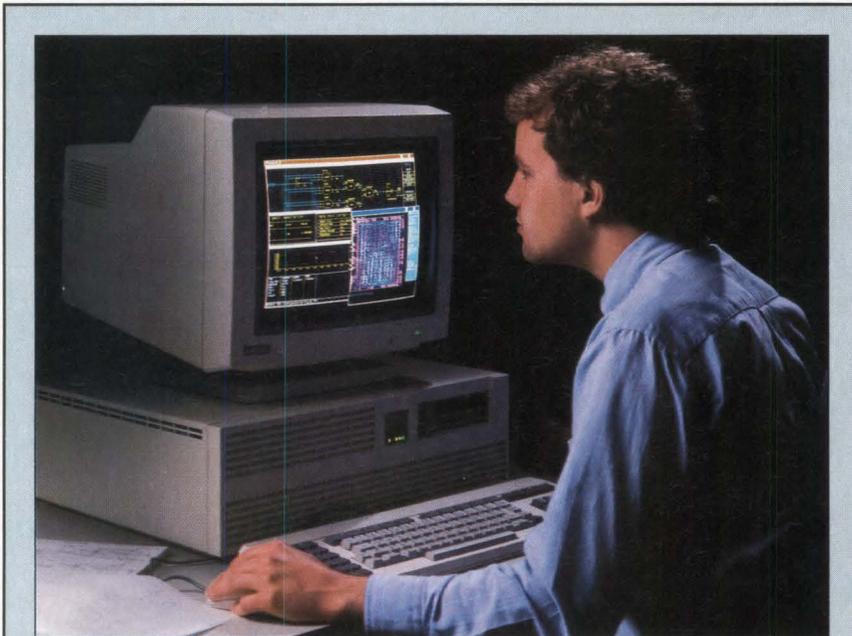
perts. "Merlyn-G is made up of a lot of separate tools, and each tool has its own processing options," explains Bob Harrison, product marketing manager for the Gate Array Worksystem. "That gives you a lot of flexibility but makes it difficult to run manually. So we've come up with an expert system that can drive a Merlyn subsystem, look at the results, and adjust the placement and routing strategy it's using."

A Turnchip module could, for example, direct Merlyn-G to run a quadratic placement algorithm with a given set of timing or wire length parameters. If not all components can be placed, the module could branch to a relaxed set of parameters or call up an iterative improvement placer. Or Turnchip might try a pin-assignment algorithm that can swap electrically equivalent pins. Turnchip can also take a layout all the way through routing, and then go back to placement without user intervention if 100 percent routing isn't achieved.

While Tektronix designs Turnchip modules in cooperation with foundries, Autolayout runs are put together directly by the foundry. As with Turnchip, the result is a rule-based placement and routing strategy for a specific gate array family. Both systems guarantee compliance with foundry design rules. "The user has only to push a button, and the layout follows all the rules set out by the foundry," says Peter Heller, marketing manager of Daisy's application-specific IC division.

Silvar-Lisco's Gards layout system lets users set up batch files that define parameters and strategies. "You can fine-tune specific layout tools with a priority file," says Steve Kompolt, product support manager for Gards. "You could optimize placement by choosing between a two-dimensional congestion algorithm and a net-length algorithm." Similarly, Mentor provides user-defined parameters that change the way placement will operate. But making such choices requires an understanding of the layout tool and

Richard Goering
Senior Editor



The Gate Array Worksystem from Tektronix provides Turnchip layout modules for specific gate array families. Users can enter schematics, select the gate array bonding package, view back annotation results, run simulations and view the automated layout in a multiwindow environment.

the foundry's requirements.

Although very similar conceptually, Turnchip and Autolayout are implemented in different ways. Turnchip differs from typical rule-based expert systems because it's not interpreted at run time. Instead, a compiled rule base is used to drive a state graph, which is basically a machine-readable table that stores all possible layout processes. At execution time, Turnchip may branch from one state to another, but it doesn't have to go through a CPU-intensive decision-making process.

"Our approach is more flexible because Autolayout is interpreted at run time," says Daisy's Heller. "That lets chip layout experts take what's provided by the foundry and modify it." With Autolayout, users can intervene at any point in the layout process and can review layout rules and even change them. Merlyn-G, on the other hand, is set up for totally automatic operation, although a graphics editor could be used to route a few critical nets.

Foundry support critical

Applied Micro Circuits (San Diego, CA) offers a Turnchip module—a bipolar emitter-coupled logic gate array with up to 3,500 gates—for the Q3500 Sierra family. Modules will soon be available for CMOS gate arrays from NEC Microelectronics and Fujitsu Microelectronics. Autolayout runs are available for such suppliers as California Devices, Matra-Harris, NEC, RCA and Thomson. The PA50000 series from RCA (Somerville, NJ)—a channeled CMOS array—is a second-source for the LSI Logic (Milpitas, CA) LL-5000 series.

Even without customized layout runs, qualified physical libraries from vendors are needed to support the layout process. These libraries differ from logical libraries, which provide schematic symbols and simulation models. A physical library includes a base array description, which provides a floor plan of the array, and a simplified physical representation of each of the cells in the logic library.

Mentor, for example, has worked with such foundries as Gould AMI, NEC and Siliconix to provide qualified physical libraries for Gate Station. When logical and physical libraries from a foundry are used, it's impossible for the user to violate that foundry's design rules, according to Cohen. Vendors such as Fairchild, Mostek and Texas Instruments support Silvar-Lisco's Gards with physical libraries.

Still needs direction

Regardless of how automated gate array layout tools are, they operate best when the user provides input. "You don't need to define anything to use Gatemaster," says Daisy's Heller. "But you'll typically want to identify I/O macros and fix a few things where there are time-critical relationships." Separate software provided by Daisy lets users identify the bonding package and the pin as-

signments for the gate array.

In the Gate Array Worksystem, the necessary parameters for layout are derived from the schematic. "The user has control of the layout directly from the schematic," says Harrison. Specification of the base array and bonding package is made directly on the title block of the schematic, while net priority specifications, device versions, device preplacement and I/O pin assignments are entered as part of the schematic. This information is passed to Merlyn-G by forward annotation.

One way to control layout is to give a priority weighting for a net. If users think the net will be time-critical, they can raise this weighting factor. The placement algorithm for Merlyn-G models circuits as "masses" connected by "strings." A higher weighting factor increases the strength of the string, pulling components closer together.

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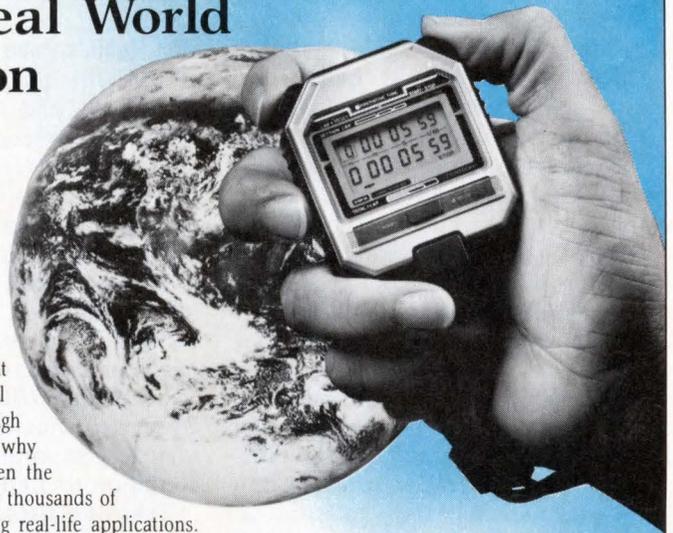
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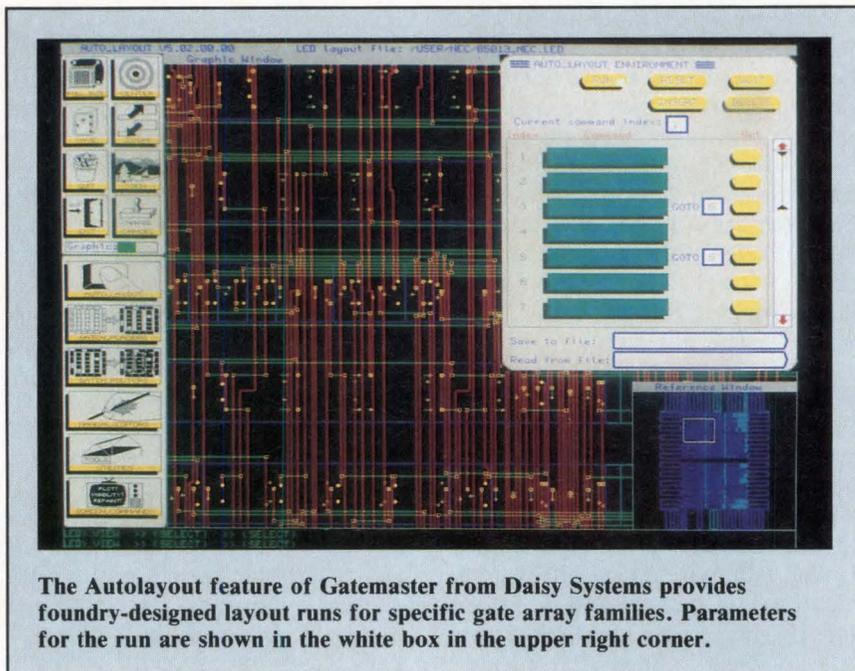
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The Autolayout feature of Megagamemaster from Daisy Systems provides foundry-designed layout runs for specific gate array families. Parameters for the run are shown in the white box in the upper right corner.

As in the Tektronix system, Mentor's Gate Station permits the entry of such parameters as critical nets and pin assignments directly into the schematic. In Silvar-Lisco's Gards system, however, I/O pads and critical nets are defined in batch files, although pin assignments can be made on the schematic.

Most gate array layout systems back annotate interconnect capacitance to logic simulation so that an accurate postlayout simulation can be run. The postlayout simulation tells the designer how the layout affected circuit performance. In the Gate Array Worksystem, this information is actually back annotated to the schematic, because both simulation and layout run off of the schematic data base. "You can view it in the schematic and see what your capacitance is. You can then run a simulation that takes that capacitance into account," says Harrison.

The Gate Array Worksystem includes the Hilo-3 logic and fault simulator from Genrad (Concord, MA). This simulator includes a hardware description language, worst-case timing verification and concurrent fault simulation. Daisy's Megagamemaster and Mentor's Gate Station include the proprietary logic

and fault simulators sold by those vendors. Silvar-Lisco's Gards gives users a choice of four proprietary simulators from Silvar-Lisco.

Like Rubik's cube

Automatic placement algorithms from Daisy and Tektronix generally follow the concept of simulated annealing, a process that makes repeated attempts to optimize a layout until the placement fits within some predefined metric, such as total wire length. Simulated annealing is analogous to solving Rubik's cube. The process starts with a layout, compares it to the desired metric, and reshuffles the layout to get closer to the metric. It may be necessary to temporarily go to a worse condition to find a better layout.

Tektronix uses three routing strategies to complete gate array layout. The first phase involves a traditional channel router, which identifies routing channels and routes connections within each channel. Then a maze router picks up connections that can't be made within a channel. If needed, Merlyn-G can then use a "rip-up and retry router" to complete the routing of the chip.

Daisy uses a similar combination of channel, maze, and rip-up and

retry routing. Acceleration is available with Daisy's MegaGatmaster. And while many gate array routers stop at 98 or 99 percent, leaving the hardest connections for the user, Daisy guarantees 100 percent routing when Autolayout is used. Tektronix's Harrison says, "We can't guarantee 100 percent routing because there are things you can do that would make it absolutely impossible to route. But if the chip can be routed, Turnchip will find a way."

Mentor initiates a global routing first and follows up with a channel router, a maze router and a rip-up and retry router. Silvar-Lisco uses a fast line probe algorithm and then cleans it up with a maze router. No rip-up and reroute algorithm is included, but Kompolt says completion rates usually reach 99 to 100 percent.

Why do layout?

By doing their own gate array layout, system designers gain control over the design project and can generally speed it up. Instead of waiting weeks to get a layout from the foundry, a layout can be implemented overnight, and the interconnect delays can be back annotated to simulation, letting the designer immediately see what the layout did to the performance goals.

While many foundries now encourage users to do their own gate array layout, the industry's largest gate array supplier, LSI Logic, takes exception. "We have a group with two IBM Sierra machines and 20 designers who do nothing but layout," says Rob Walker, vice-president at LSI Logic. "If the customer can do layout in a few days, we can do it in a couple of hours."

Another factor to consider is the cost of gate array layout software. The Gate Array Worksystem, for example, costs \$70,000 for software alone on the Apollo DN3000, and that doesn't include Turnchip modules. But those customers who design a number of gate arrays can probably recoup that cost relatively quickly by reducing the fees they pay to foundries.

CD

Single architecture integrates all levels of factory-floor control

Despite expectations that open system architecture, open system interconnection and the Manufacturing Automation Protocol will provide dependable communications among all levels of a computer-integrated manufacturing (CIM) facility even when the computers are from varying suppliers, practical implementations are still years away. Because of differences in their architectures, a manufacturer's computers at one level usually can't talk to computers from another manufacturer at one of the other levels.

But Digital Equipment Corp (Maynard, MA) has now moved toward its own version of integration with the introduction of a three-member family of industrial computers that cover multiple levels on the factory floor and are compatible with its VAX 8000 family of computers already in use for management levels. All of DEC's CIM-oriented industrial computers use the same architecture and, therefore, provide the necessary integration "from distributed real-time control on the factory floor to corporate information management," says David Copeland, manager of the company's manufacturing/CIM marketing group.

CIM operations are usually divided into five levels. Level 1 is the lowest area of control and includes the working elements: the valves, sensors, motors, robots and programmable logic controllers. Level 2 is the unit control area and includes the machine controllers, distribution systems and I/O devices. Level 3 is area or cell control, level 4 is plant control, and level 5 includes the corporate systems (often at a site other than the factory).

Historically, IBM mainframe computers have dominated level 5, the corporate headquarters. More recently, Hewlett-Packard and Digital Equipment Corp have made inroads at this level. DEC has more or

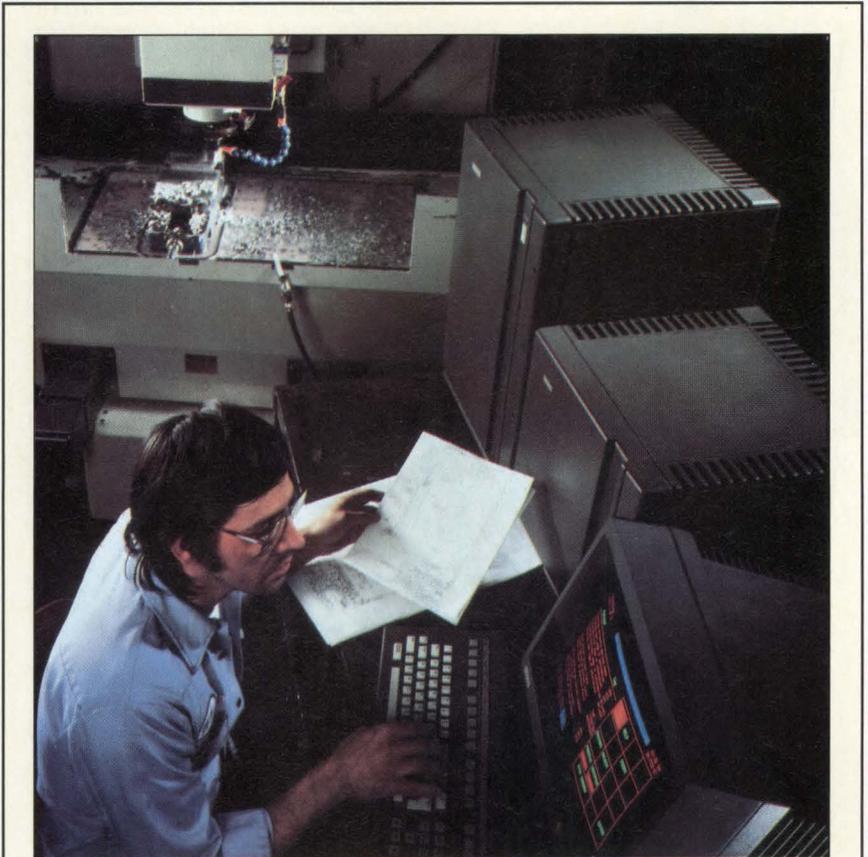
less been the dominant supplier of level 4 computers, the highest level within the factory itself. Levels 2 and 3 have been populated by computers from a variety of manufacturers.

DEC's Industrial VAX (IVAX) 630 is the most powerful member of the family. Based on a 32-bit MicroVAX II with a floating-point processor, this system supports from 5 to 16 Mbytes of main memory and up to 213 Mbytes of disk storage. A 5-Mbyte system housed in a standard 12-slot, 19-in. rack-mountable chassis includes a 71-Mbyte disk and a 95-Mbyte streaming-tape cartridge.

The IVAX 620, described by the company as its "first complete VAX system designed for dedicated real-time applications on the factory

floor," is available as either a diskless or a disk-based network node. Both versions run the VAXELN high-speed, real-time software kernel. Applications software can be developed and debugged on a host VMS system before being run on the IVAX 620. A diskless system includes a six-slot enclosure, the KA620 real-time 32-bit system with a floating-point processor, 1 Mbyte of memory, an Ethernet interface and a VAXELN run-time license. A disk-based system with a 12-slot enclosure also has a 71-Mbyte disk and 95-Mbyte streaming-tape cartridge.

The third member of the family, the IPDP-11, protects users' investment in PDP-11-based applications software. Because the same software



Digital Equipment Corp's Industrial VAX and Industrial PDP-11 computers are intended to extend its dominance from the plant-control level to the cell and unit-control levels of the factory floor. Computers at all three levels, as well as the corporate level, now have the same architecture.

Sydney F. Shapiro
Managing editor

can be used, the IPDP-11 lets users move RSX-11-M-Plus manufacturing applications from control rooms to factory floors. A 12-slot version of the IPDP-11, based on the Micro-PDP-11/83 with a floating-point processor, provides 2 Mbytes of memory, a 71-Mbyte disk and a 95-Mbyte streaming-tape cartridge.

Since environmental conditions vary, each member of this new industrial family is available in either an open-rack configuration for harsh environments or as sealed, passively cooled systems for protection against noncorrosive liquids or falling dirt. Installing the industrial computers next to the machine or

process being controlled also reduces cabling costs. Sealed companion terminals, available in either black and white or color versions, can be either wall- or rack-mounted.

DEC has also introduced a Baseway host system to accommodate factory-floor applications using programmable logic controllers (PLCs). Baseway permits both data collection and control from a variety of devices such as PLCs, robots and numerical-control units that might be supplied by a number of different manufacturers and could operate on proprietary networks.

A Baseway system consists of one IVAX Baseway cell supervisor, which is based on the IVAX 630 system, and from one to four IPDP-11 Baseway shop-floor servers. The latter are based on the MicroPDP-11/53 system. Each server supports multiple PLCs.

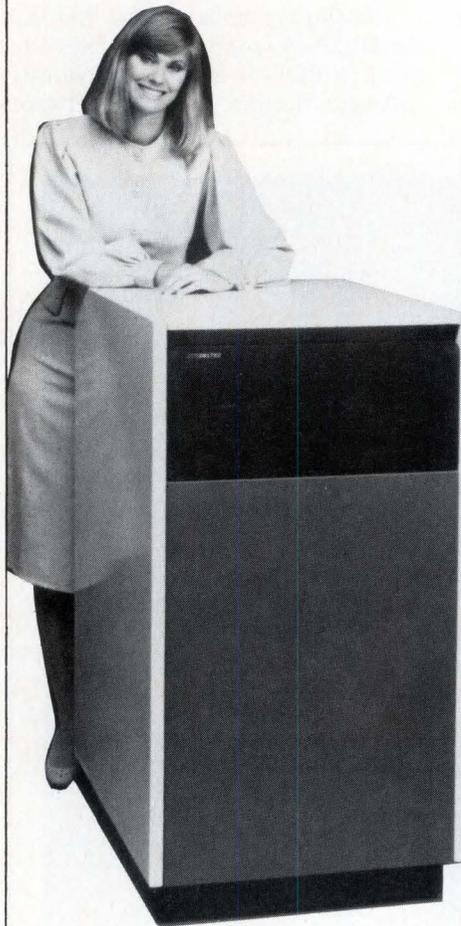
DEC has also introduced three integration tools: DECscan, VAX DEC/MAP and distributed numerical-control applications services. DECscan is an open architecture link that serves as a software toolkit for developing data-acquisition and control access to factory-floor devices.

DEC stands by Ethernet

Despite DEC's support for MAP, however, its local area network efforts, including the new IVAX family, continue to focus on Ethernet. And DEC president Kenneth Olsen expresses reservations regarding MAP. "We love MAP's goals, but why another network?" asks Olsen. "Ethernet works. We have built thousands of Ethernets that have never run out of capacity." Olsen also questions how MAP will be funded. "Who will pay for developing the software, hardware, testing, documentation and support?"

An enhanced MAP product for the Q-bus MicroVAX II and IVAX family is in the works, according to Don Jenkins, manufacturing/CIM product marketing manager. That product might be introduced at the Corporation for Open Systems demonstration of MAP Version 3.0, scheduled for next summer. **CD**

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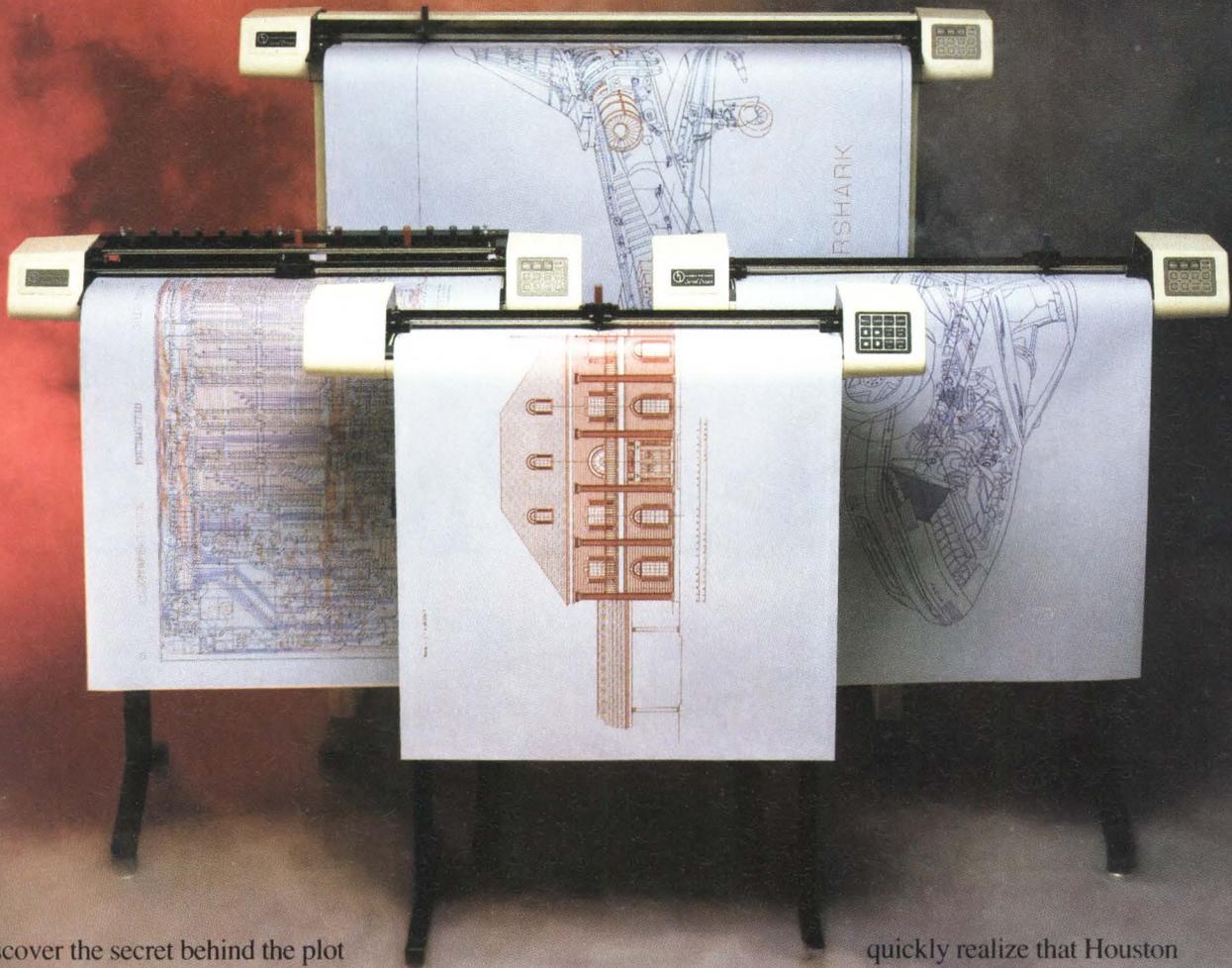
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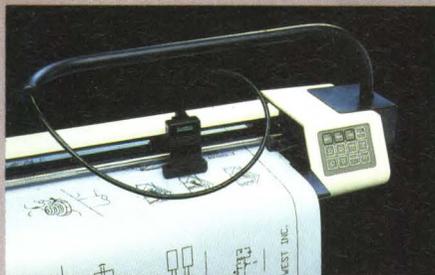
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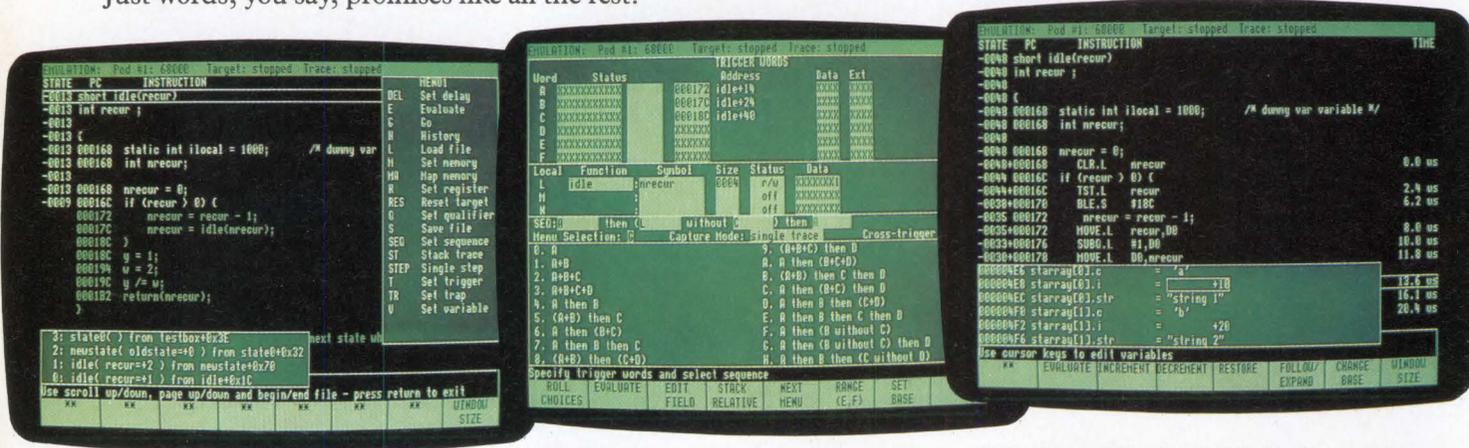
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CIRCLE NO. 22





Board-level solutions open new territory for image processing

Once the province of very expensive systems, image processing is now finding its way onto low-cost platforms, thanks to board-level accelerators. As a result, developers are exploring a host of new image-processing applications.

Tom Williams
Western Managing Editor

The more affordable a technology becomes, the more applications will continue to be found for it. This has been true of computers in general and is true of various subsystem technologies, such as graphics and data communications. Image processing, which was once confined to \$100,000-class systems, for example, is now finding practical uses in board-level systems priced between \$3,000 and \$10,000.

The pattern is familiar. Advances in silicon processors enable the technology to become smaller. As a result, new markets are discovered, which spur the efforts to shrink the system size and cost even further while retaining performance. And supplying the system environment for this evolution is a class of powerful, inexpensive platforms, including the IBM PC AT, the MicroVAX II and now the Macintosh II.

The term "image processing" has come to mean many different things. The main difference between computer imaging and computer graphics lies in the origin of the image. In imaging, the picture data is taken from an outside source and is manipulated, while in graphics, the picture is generated by the computer.

Now that low-cost, board-level products are available, a finer distinction is needed to differentiate image processing from image editing. Image processing applies algorithms to image data to get results the user might not foresee, such as bringing out hidden details. But image editing is the user "playing with the display, playing with memory," according to John Molinari, product marketing manager for Data Translation (Marlboro, MA). Both image processing and image editing are valuable to different user groups, and are increasingly supported by today's emerging products.

A complete image-processing system encompasses three basic activities: capturing the image, which includes scanning, digitizing



*Hon Wong
Marketing Manager
Computer Modules*

Building blocks for entry-level image-processing systems

There are many factory and laboratory applications that can benefit significantly from today's image-processing technology. But the potential for image processing hasn't yet been fulfilled. This is due largely to the high cost of image-processing systems and the lack of software packages that enable a nonexpert to use the hardware that's available on the market.

To bridge the gap between available technology and the technology that's actually being used, Computer Modules (Sunnyvale, CA) has integrated image-processing software from Automatic Visual Inspection (Mountain View, CA) with a set of available hardware components, resulting in an entry-level image-processing system. This imaging system is designed for two user groups: research scientists and production engineers. Research scientists need image processing primarily for the enhancement and storage of captured images. Production engineers are interested in image processing to perform automatic inspection by analyzing the texture and size of an object. For entry-level systems, both groups require similar capabilities to best solve inspection problems.

The proper selection of hardware is necessary to provide the required level of performance at a suitable price for an entry-level system. There are four major hardware components for such a system: a host computer, a camera, a video display monitor, and a frame grabber or digitizer board. The components that are chosen can make a substantial difference in the price and performance of the system.

The IBM PC AT makes an ideal platform for this application because of its attractive price/performance ratio and its wide compatibility with boards and software. In most applications, an AT with a standard frame buffer board will outperform a VAX-11/780 with a standard graphics box, performing similar image-processing functions.

There are two cameras that can be chosen for such a system: a vidicon, or vacuum-tube type, and a solid state camera, which is typically a charge-coupled device (CCD) camera. A CCD is supplied with Computer Modules' system because it closely matches the frame buffer board in both resolution (512×480 pixels) and in the amount of noise. The amount of noise—about one part in 256—is at a level well below what the eye can see. In addition, some cameras let the user choose automatic gain control, gray-level compensation and hardware image sharpening.

The monitor choice is also important. Computer

Modules chose a color, long-persistent monitor for this entry-level system. Even with a black-and-white camera, a color monitor can use the "false color" capability of this system to display additional information relating to the captured image. Furthermore, the long-persistence of the monitor also helps reduce flicker and eyestrain.

The frame grabber board, which digitizes an image from the camera, is the heart of an image-processing system. The PIP-1024 PC bus-based imaging board from Matrox Electronic Systems (Dorval, Quebec, Canada) was chosen for Computer Modules' system. This board handles up to 512×512 pixels of frame grab resolution at 8 bits per pixel. It also contains a 1,024×1,024×8-pixel frame buffer that can store up to four captured images to facilitate the efficient and flexible handling of the captured information. Computer Modules believes that this board best fits the price/performance criteria of an entry-level imaging system.

With this entry-level system in place, users can experiment with image processing without reading manuals or developing software. This is possible because of a built-in command interpreter with on-line help and key-word access. If users want to digitize, they command the system to digitize an image. If users are unaware of the available commands, they can ask the system about digitizing and the interpreter will instantly describe all of the available commands and the differences between those commands.

Over one hundred functions are included in the software toolbox. These functions include image sharpening (convolutions), contrast enhancements, color, positions, angles, dimensions, area, texture, and presence and absence. Any of the operations can be performed on the whole screen or on a part of it, as defined by a rectangular window, or on any closed polygon, positioned by a mouse or by keystrokes.

Future developments for such an entry-level system include interfacing to higher performance frame buffer boards, providing interfaces for motor and lighting controllers, and expanding upon the color analysis ability of the system. This system could be easily upgraded to provide color image processing via Matrox's MVP-AT color machine-vision board for the AT.

This integrated system provides the solution to a wide range of image-processing problems that formerly required hundreds of man hours and tens of thousands of dollars to solve.

and storing the image data; modifying the image by various processing algorithms or by providing the capability for users to edit it; and transforming the image. Transforming involves converting the image data into data that can be used by the computer for a specific application. In a machine-vision system, for instance, all the data may be reduced to a simple 1 or 0 to accept or reject a part under inspection. Or it may be used to position a robot arm for welding.

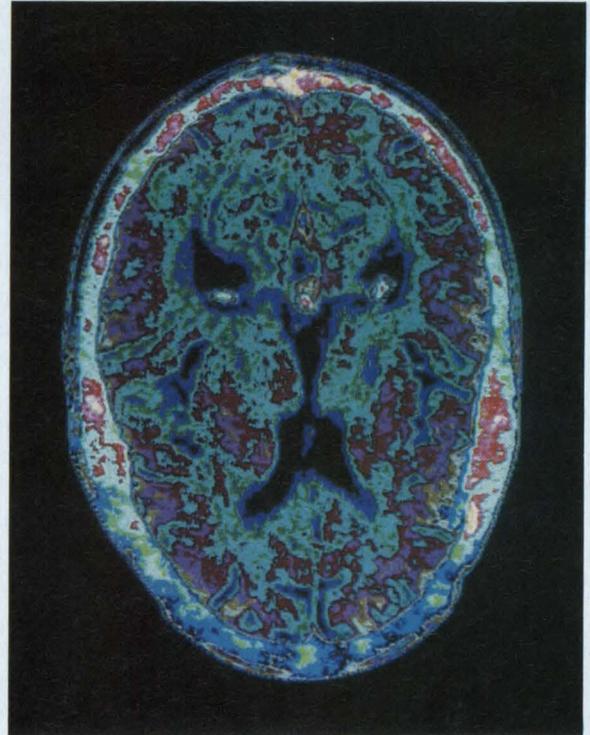
Board-level products for the Multibus I and the VMEbus have existed for several years. Examples of such products include the modular Maxvideo series from Datacube (Peabody, MA) and the Series 150 from Imaging Technology (Woburn, MA). These product lines continue to be expanded and to provide more capabilities. PC-based boards, which started primarily as image-capture devices, are also adding processing power.

Image capture is the first imaging function to migrate to the PC bus in the form of frame grabber boards. The simple ability to capture image data and make it available to the host processor has found immediate use in applications such as compressing and storing images in data bases or transmitting them over telecommunications networks. Other immediate applications are in the visual arts, such as animation and creation of video logos, and graphics for television news and sports events.

One low-cost frame grabber is the PC-Eye Series 1500 from Chorus Data Systems (Merrimack, NH). Available in monochrome or color versions, the PC-Eye can produce 256 gray levels (8 bits/pixel) monochrome, while the color version can provide 15 bits/pixel for 32k possible colors. Both versions can scan at a resolution of $320 \times 200 \times 8$ -bit pixels. Because PC-Eye doesn't have its own frame buffer, it must be used with another graphics controller board. The stored image can then be manipulated using the functions of the graphics controller.

Frame grabber boards that have their own frame buffers include the Targa series from AT&T (Holmdel, NJ), the Pepper Pro 16 from Number Nine Computer (Cambridge, MA), the DT2803 from Data Translation, and the Color Catcher from Diversified Technology (Ridgeland, MS). The Color Catcher digitizes an image of $768 \times 488 \times 8$ -bit pixels.

For visual arts applications, a frame grabber that lets the user overlay graphics on the image can be a great advantage. This capability, provided by the PC Graphover board from New Media Graphics (Burlington, MA), allows graphics overlays on top of 640×400 -pixel video images. AT&T's Targa 32 board can do graphics, and it has an "alpha channel," which lets the user store transparency infor-



Pseudocolor is added to gray-scale images by loading color values in output lookup tables to emphasize details the human eye might not notice. The Imaging Toolkit from Rapid Imaging can assign a basic color to a gray scale range and vary the density of that color over the range. This highlights variations in a distinct structure while setting it apart from the rest of the image, as shown in this computer axial tomography (CAT) scan of the human brain.

mation for merging pictures so a background image can show through a foreground scene.

For frame grabbers to be used for true image processing, image-processing software must be running on the host computer. While most frame grabbers are equipped with RS-170 video and/or RGB inputs that let them digitize and store color images, such color images have limited uses. The primary purpose of capturing color signals from cameras or other video sources is to use them in image editing, primarily for the visual arts or for picture bases. Image processing aimed at image analysis and machine vision uses monochrome data.

This isn't to say that color isn't important or that imaging systems can't make practical use of processing color images. There could be many applications in inspection and vision systems, such as those used for routine inspection of parts in manufacturing operations. But Data Translation's Molinari disagrees. "All frame grabbers that digitize color

are absolutely useless for image processing," he says. "The problem with color is that there are no algorithms that deal with RGB data." There are some algorithms that translate RGB into digital representations of hue, saturation and intensity, however. These algorithms extract the monochrome data so that it can be subjected to normal image-processing algorithms, while preserving the original color data from the scanned image. Hue refers to the color, saturation refers to the white light intensity that tends to wash out the color, and intensity refers to the original black-and-white data as it would look if the system had scanned the picture in monochrome.

By translating the RGB data into hue, saturation and intensity, the user can apply all the normal processing algorithms to the monochrome representation and still have the original color data available. Still, as Molinari points out, "There's a big future for color, but there are no algorithms that make sense of color today." At some point, for instance, subtle color variations may be detected and enhanced by yet-to-be developed algorithms. This will allow a greater degree of inspection and characterization for inspecting the purity of drugs, for example, than is possible with current monochrome processing technology.

The color techniques used in today's image processors from the low to the high end are known as false color, or pseudocolor. Pseudocolors are created by loading RGB values into lookup tables (LUTs) in the display output section of the board. A given binary-coded gray level can be assigned a false color for display purposes. Three digital-to-analog converters are then used to decode the values to display color. These false colors generally have little to do with the actual color of the object whose image has been captured. They are simply assigned to highlight gray levels that may not be readily perceptible to the user.

As features and intelligence are added to the basic frame grabber, it takes on an increasing number of true processing capabilities. One of the more desirable features for frame storage is having multiple frame buffers, or a large enough frame storage memory to let the user choose different buffer configurations. The VMEbus-based FB-150 from Imaging Technology, for example, can be configured as one $512 \times 512 \times 16$ -bit pixel buffer or as two $512 \times 512 \times 8$ -bit pixel buffers. The AT-428 from Datacube has four $384 \times 512 \times 8$ -bit pixel buffers. The 384 horizontal pixels are designed to match the 384-pixel horizontal resolution of solid-state charged-coupled device (CCD) cameras.

Multiple frame buffers aid both image acquisition and image processing that may be done by an auxiliary processor or the host CPU. These buffers let the system retain the original captured data and store the processed image as well. They also allow logical operations between two stored images. The ALU included on-board the 2851 frame grabber from Data Translation, for example, can subtract one image from another to determine the differences between the two that might be of interest, such as the change in an object's position. The 2851 features 50 logical and arithmetic operations.

Besides having output LUTs for pseudocolor, most advanced frame grabbers have input LUTs. Input LUTs allow preprocessing of incoming image data on the fly. As data are converted to 8-bit values in the DT2851, for example, they pass through one of eight user-configurable 8-bit LUTs. These LUTs can be used for controlling contrast, thresholding (storing the pixel only if it exceeds a given value), or for compensating for nonlinearity in the camera.

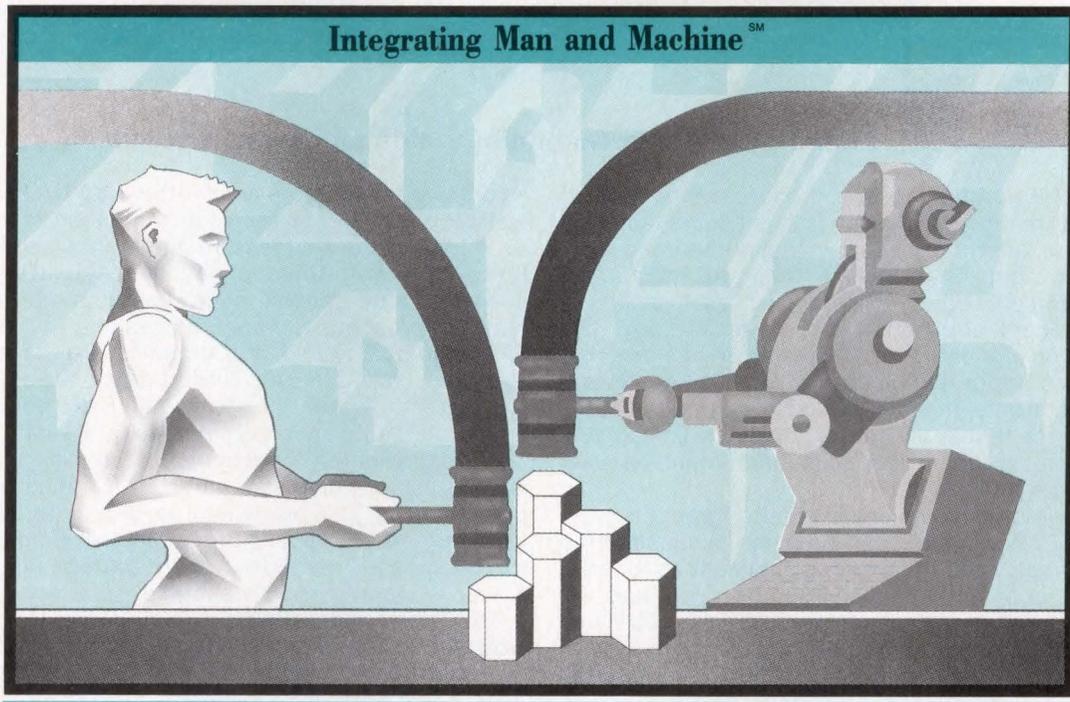
One useful function supported by multiple buffers is frame averaging, which eliminates random noise from the final stored image. The MVP-AT from Matrox Electronic Systems (Dorval, Quebec, Canada) can digitize an image up to 256 times. The images are added together and then divided to achieve the average. Since noise never occurs in the same place, the resulting image will show only what's in the same place all the time and will produce a clear image of the object being scanned.

Nonvideo inputs are increasingly in demand to handle data delivered from medical instruments, such as computer axial tomography (CAT) scanners, slow scan video devices, acoustic sources, and heat and pressure transducers. Datacube, for example, supplies the Maxscan module, an analog and digital acquisition module that can be programmed from dc to 20 MHz and supports synchronous interfaces to a variety of input devices.

Full image processing—applying mathematical and signal processing algorithms to the image data—will ultimately occur on a single board. Manufacturers are already cramming as much processing power as possible into their products, primarily because moving the data between boards over the system backplane bus is unacceptably slow. Multi-board systems have had to implement a dedicated image bus for this purpose. Also, image processing is compute-intensive and involves vast numbers of repetitive steps. Adding intelligence to the board, therefore, off-loads much of the computation from the CPU and speeds throughput.

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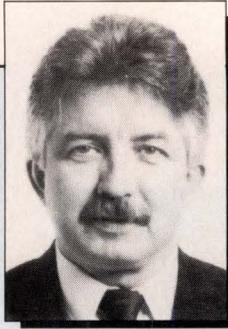
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Image-processing technology aids electronic publishing

Electronic imaging is a broad classification of technologies including image acquisition, processing, analysis, mass storage, display and hard-copy output. The ability to capture, manipulate and print photographic images as easily as line art is a recent application of this technology. The common denominators between image-processing technology and electronic publishing—a vertical electronic-imaging market—include the application of higher resolution displays, image processing, graphics hardware and improved user software interfaces.

Image-processing and computer graphics technology are sometimes intertwined because of the CRT display and the imaging applications for electronic publishing. Special-purpose compute engines, such as raster scan processors require high throughput. Raster scanning reassembles intersections with character and region pulses during linear scanning. The processor speed must be compatible with high scanning speed, and it shouldn't delay any character recognition driving the write and sort commands. Moreover, the scanned characters may be distorted, noisy and slightly rotated, requiring extensive searches by the processor among different font types. Editing requires raster-to-vector and vector-to-raster conversion—both of which must be carried out by the raster processor. Applications require a host CPU with a fast coprocessor.

Image processors enable nonimpact printers to act as high-quality text and graphics output devices. The trend for manufacturers to provide separate print engines and image processors stems from the inherent advantages of modular printing systems. Imagen (Santa Clara, CA) is one company that separates its marking engine from the image processor, letting a number of host processors be attached via different interfaces. In effect, the image processor is a special CPU that generates images electronically and controls printer system functions.

Page descriptions that come from the host CPU

as dots and characters are synthesized by the image processor. A raster scan technique is then used to print the synthesized dots on the page. Intermediate software-application languages are used to create concise page descriptions. Alternative approaches to image processing that combine high-quality text and graphics require a bit map to assemble the information. These approaches, however, increase the RAM requirements and, subsequently, increase the cost.

The application of sophisticated image-processing algorithms and hardware to electronic publishing is just beginning to take hold. Most image-processing applications require some form of geometric revisions or updating on the screen—sometimes to a subpixel accuracy.

The fast-paced activity in microcomputer- and workstation-based publishing systems will continue for at least two years. In fact, electronic publishing is considered to be the fastest growing electronic-imaging vertical market. Significant market growth is anticipated for applications such as technical manuals, military contract documentation and engineering documentation.

Companies are realizing the cost savings of electronic publishing in these areas. IBM, for example, has estimated that the cost to produce, maintain and store manuals and documents was about \$300 million per year. The company is now producing the documents electronically and then downloading them to the sales office after peak telephone cost periods. The information is reproduced on a laser printer at night and is available the next day for customer delivery.

This trend in document storage, retrieval and remote transmission represents only one opportunity in electronic publishing that's expected to fuel this market's growth. Potential exists for a raster image processor with vector, raster and bit-map conversion, remote image and page display after reconstruction at the customer site, and high-speed color scanners and even higher speed monochrome scanners to input picture data.

Imaging Technology's Series 150 has a video bus, and Datacube has a Maxbus to rapidly transfer picture data among modular, multiboard systems at 10 Mbytes/s. In fact, both companies have developed a technique of switching the path of the picture data among modules. Imaging Technology uses a cross-point switch IC on each of its modules, while Datacube uses a board called the Max-Mux to control its

picture bus. Image data can be routed among modules by software commands sent to the switching hardware.

High-speed transfer and switching ability is important in the modular approaches taken by Imaging Technology and Datacube. Imaging Technology's Series 150 has five modules: a digitizer, a frame buffer, a pipeline processor, a histogram/

feature extractor, and a real-time convolver for speeding up filtering and edge-enhancement operations. Datacube's Maxvideo family consists of 17 different modules aimed at tailoring the system exactly to the application. With crosspoint switching, the user can select price/performance levels by sending the data to several boards in parallel or circulating it several times through a single module. Also, the system can be configured for a specific application by software commands.

Even boards on the AT level have high-speed interfaces to auxiliary processors. Data Translations' DT2851 frame grabber and DT2858 auxiliary processor are functionally equivalent to the company's products for the VMEbus and MicroVax II. These products communicate picture data via external I/O ports. The Matrox MVP-AT has an on-board processing bus that allows connection of a neighborhood processor, the MVP-NP, which is an accelerator module.

The newest entry in AT-class image-processing systems is Visionlab II from Comtal/3M (Pasadena, CA). Visionlab consists of a frame grabber/display processor that transfers images at 36 million pixels/s over a dedicated video bus.

With the addition of auxiliary processors for ATs, image-enhancement and analysis applications become practical. Operations such as spatial filtering, region-of-interest processing, pixel-point and pixel-group processing are possible. In pixel-point processing, a given operation is carried out on each pixel in the display. Group processing involves a series of operations on a group of pixels associated with every pixel in the display or area of interest.

There are three primary applications areas for such board-level systems, according to Sylvio Jelocovich, product manager for Matrox. These areas include graphics arts, machine vision and robotics, and image enhancement and analysis. But he adds, "We're very exploratory. Our ads tell people who have interesting applications to call us."

Data Translation's Molinari points out, however, that the most popular algorithms are already supported by the class of hardware from Matrox, Data Translation and Comtal/3M, as well as by the higher level board products from Datacube and Imaging Technology or the single-board Cognex 2000 vision system from Cognex (Needham, MA).

These operations include various types of convolutions. Convolutions are pixel group operations in which each pixel surrounding the pixel of interest is multiplied by some integer and then summed to produce the result, which replaces the value of the pixel of interest. For example, a 3×3 convolution would do a multiply-accumulate operation on the

eight pixels surrounding the pixel of interest, as well as the pixel of interest itself. This is repeated for each pixel in the display. For a 512×512 display, a 3×3 convolution would require nearly 2.5 million multiply-accumulate operations. Use of a larger kernel would increase the processing load. A 7×7 kernel, for instance, would require over 128 million multiply-accumulate operations.

Different types of convolution kernels are used for spatial filtering for edge detection or high-pass filtering to sharpen an image. Low-pass filtering filters out high-frequency components of an image, blurring or softening the image. High-pass filtering does just the opposite, keeping the high-frequency components, and sharpening the image.

Other popular algorithms create histograms, which graph the statistical distribution of gray levels in an image. By changing the distribution curve of the gray levels, also called gamma correction, it's possible to bring out details that weren't readily visible before. The histogram algorithm essentially changes the contrast of an image so that details that weren't readily visible stand out. Simple arithmetic and logic operations, such as those used for frame averaging, can also be used to help position robot arms by locating a specific feature or an area between two points or lines. Both the contrast and arithmetic operations are examples of pixel-point operations.

Given the amount of raw processing involved in even the simplest spatial filtering algorithm, a word should be said about what "real time" means in relation to image processing. Credible performance claims use a frame time— $1/30$ s—as a reference. This is the amount of time it takes for a normal video signal to scan one frame. Any processing that can be accomplished within one frame time will not be noticed by the user and will appear to happen in "real time."

Of course, since some operations take more time than others, the reference of a frame time can be quite useful. The RTC-150 real-time convolver board from Imaging Technology, for instance, can do a convolution using a 3×3 or 4×4 kernel in less than one frame time. The MVP-AT from Matrox claims a 3×3 convolution on a 512×512 -pixel image in $1/3$ s, or 10 frame times, but it can add two images together in one frame time.

Processing can be accelerated by adding hardware resources. In modular approaches such as Datacube's, the user has the option of adding specialized processors such as the company's Max-SP module designed specifically for filtering algorithms. If multiple passes are needed on the data, the user also has the option of running it through

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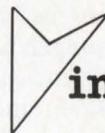
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multiple modules in parallel or recirculating it back through a single module. The first option gains speed but costs more, while the second sacrifices some speed for economy. Matrox's MVP-AT board can accept a piggyback accelerator module, called the neighborhood processor (MVP-NP), containing three custom VLSI chips that operate in parallel for a fivefold performance increase on convolutions and other complex algorithms.

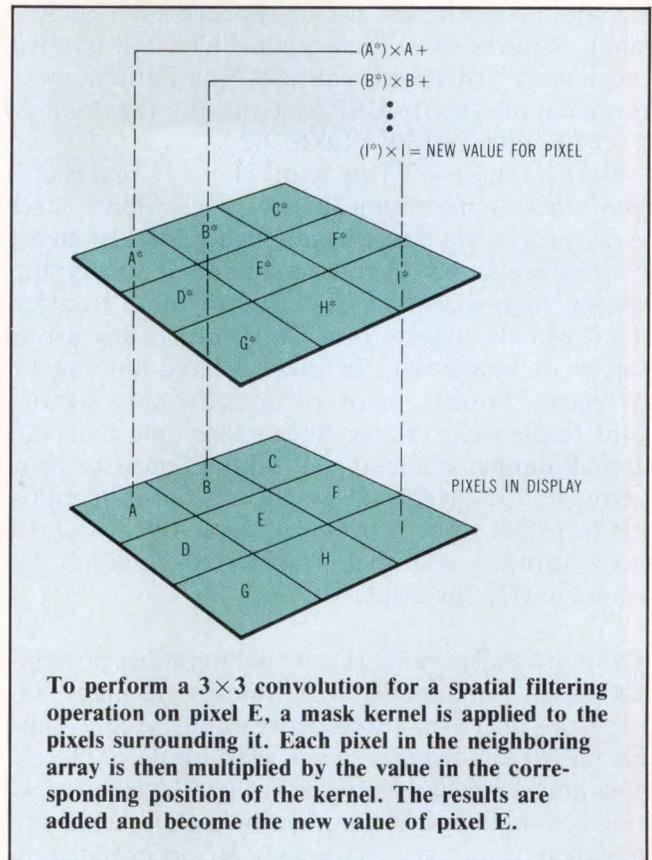
Another way to speed processing is through area-of-interest processing in which the user can select only a portion of the display for processing. The speed will increase in inverse ratio to the number of pixels processed. Now supported by all manufacturers of board-level image processors, this type of processing allows a truly interactive user interface even with boards that can't handle an entire display in one frame time. Users can use a mouse to select the area of interest, for example, try various algorithms until the results are satisfactory, and apply that algorithm to the entire screen.

As with most technologies, the demands placed on imaging systems vary with the application. For some systems, there can never be enough speed or resolution. This is particularly true in areas such as medical imaging for CAT scans and X-rays. Doctors are pushing for resolution approximating that of photographic emulsion—a drive that pushes the limits of imaging systems as well as displays. Ideally, doctors would like displays of $2k \times 2k$ pixels or more. Companies such as Pixar (San Rafael, CA), with its Imaging Computer system, and Azuray (Scotts Valley, CA), with its high-resolution display technology, are trying to meet that demand. But these end-user systems are priced between \$150,000 and \$200,000.

Many industrial applications, on the other hand, call for the least amount of resolution possible, because resolution is proportional to memory. "The more memory it takes to store an image, the more processing it takes to do anything with the image," notes Data Translation's Molinari. Indeed, many pass/fail inspection systems are doing fine with 256×256 resolution and simple logic operations that require only the resources provided by the frame grabber and host CPU.

Between the extremes, system designers need the flexibility to tailor their design for optimal price and performance. To stretch AT-based systems further than previously possible, there are board-level array processors capable of full 32-bit floating-point operations for advanced filtering algorithms such as fast Fourier transforms (FFTs).

An FFT is a mathematical operation that can



analyze any signal, including video signals, in terms of its frequency components. The FFT decomposes the signal into the composite frequencies that make up the original signal. When displayed on a screen, the results of an FFT generally don't look like the original object. Still, by representing the different frequencies, the user can choose to eliminate some, thus performing very selective filtering operations in the frequency domain. When the remaining frequency components are subjected to an inverse FFT, the result is the original image minus those frequencies that were eliminated. This allows for much more elegant filtering than is possible with convolutions.

FFTs also require orders of magnitude more processing and can't be done in real time. Products that perform FFTs include those from DSP Systems (Anaheim, CA) and Data Translation. DSP Systems supplies the Point-1, a 32-bit two-board array processor that plugs into one IBM PC, PC XT or AT slot. Data Translation makes the DT7010 array processor for the AT specifically for use with its data-acquisition and imaging products. DSP's processor is rated at 20 MFlops, and Data Translation's processor is rated at 6.5 MFlops. The boards can process 1,024-point complex FFTs in roughly 25 and 50 ms, respectively. The 1,024-point FFT is

a common benchmark for array processors, but imaging requires two-dimensional FFTs that involve much more processing, cautions Ron Pollum, vice-president of sales for DSP Systems. For the Point-I, a 1,024-point 2-D FFT takes 4.2 s.

Performing an FFT on a full 512- \times 512-pixel display requires processing 262,144 pixels. Board-level array processors don't have much on-board memory to store data being processed and don't support special high-speed ports, but they must transfer data over the system bus. Thus, processing a full screen of image data involves a large amount of overhead. In fact, the overhead is the most significant bottleneck, taking much more time than the actual number crunching. Pixel data must be converted to a 32-bit format, sent over the bus in multiple transfers to be processed, reconverted back to pixel format, and then transferred back to the frame buffer for display.

Commercially available software for image processing isn't abundant. Still, board-level manufacturers are increasingly recognizing the need to supply OEMs and users with software support. The algorithmic and mathematical basis of image processing is a topic understood by few people, while the practical uses of the technology are appreciated by

a growing number of potential users.

Because image-processing hardware is especially difficult to program from scratch, board manufacturers are understandably reluctant to get into the software business. Yet because each of their products has a unique architecture and instruction set, manufacturers must provide software that operates the basic functions of the hardware. A frame grabber, for instance, must have routines to digitize and store an image and to allocate buffers and display images.

Datacube, for example, supplies with each of its modules a library of C language-callable subroutines that are specific to the functions of the particular module. And Matrox supplies a subroutine library called Imager-AT for its MVP-AT board. Each routine can be called from the library and compiled in either C, Fortran or Pascal. Imager-AT can also be used as an interpreter to aid system developers in interactively developing code and customizing applications. Data Translation's DT-Iris exercises the functions of its frame grabber and auxiliary processor boards, and provides algorithms for convolutions, histogram generation and arithmetic functions supported by the hardware.

Because board-level imaging systems will ultimately be used in desktop workstations by sci-

“



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entists, engineers and medical researchers, it's vital that their functions be accessible to the nonprogrammer. Data Translation's PC Semper is an operating environment consisting of an interpretive command language, a file-management system and a system-expansion facility. Using the interpreter, the user can write macro commands by simply combining commands and parameters. The expansion facility lets a Fortran programmer add new routines to the Semper command library, which can be accessed by the end user.

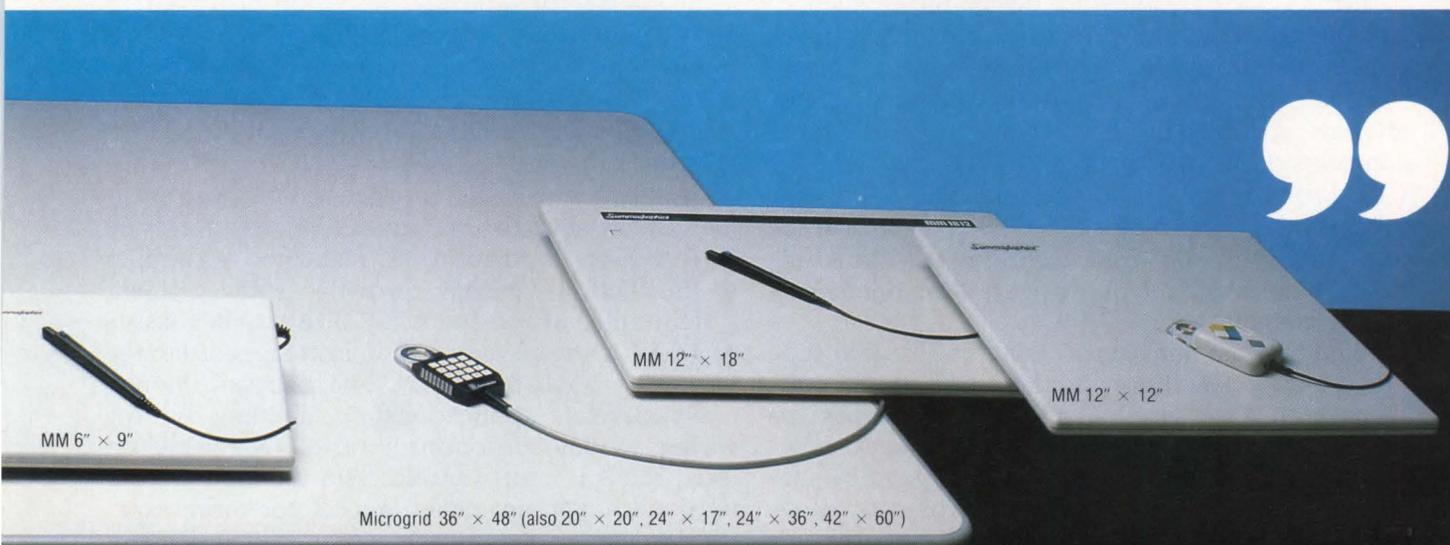
For higher level imaging environments, however, most manufacturers are looking to third-party independent software vendors. Several packages are available that can operate on different levels. Some packages, such as Publisher's Paintbrush from Z-Soft (Marietta, GA) or Lumina from Time Arts (Santa Rosa, CA) specialize in image editing. Publisher's Paintbrush, for example, is aimed at desktop publishing applications and lets the user scan in an image and then use the paint tools to change colors, do overlays or delete features. These programs are intended as electronic art aids and work well with frame grabber-type boards.

True image processing software for PC- and AT-level computers is provided by Image-Pro from Media Cybernetics (Silver Spring, MD) and by

Imaging Toolkit from Rapid Imaging Software (Tijeras, NM). Both software packages are able to work with frame grabber boards and execute their imaging routines on the host CPU—preferably with a math coprocessor. Both companies are also actively tracking developments in image-processing hardware and are adapting themselves to take advantage of the special hardware accelerators in the class of those from Data Translation and Matrox. Media Cybernetics is even reportedly adapting Image-Pro to run on Imaging Technologies' VME-bus-class board family.

Image-Pro provides a menu-driven interactive environment, which can also be altered to some extent by the user. In digital filtering, for example, the package supports 3×3 , 5×5 , and 7×7 pixel kernels for convolutions. It also comes with a library of popular filters—matrices of integers used in convolutions—including those for high- and low-pass and edge enhancement. In addition, users can display the matrix and edit the integers in the individual cells to create their own kernels.

Image-Pro has graphics capabilities that can be used to display the histogram of the contrast levels in an image, for example. The user can then interactively alter the distribution of the histogram or invoke one of the automatic histogram equalization



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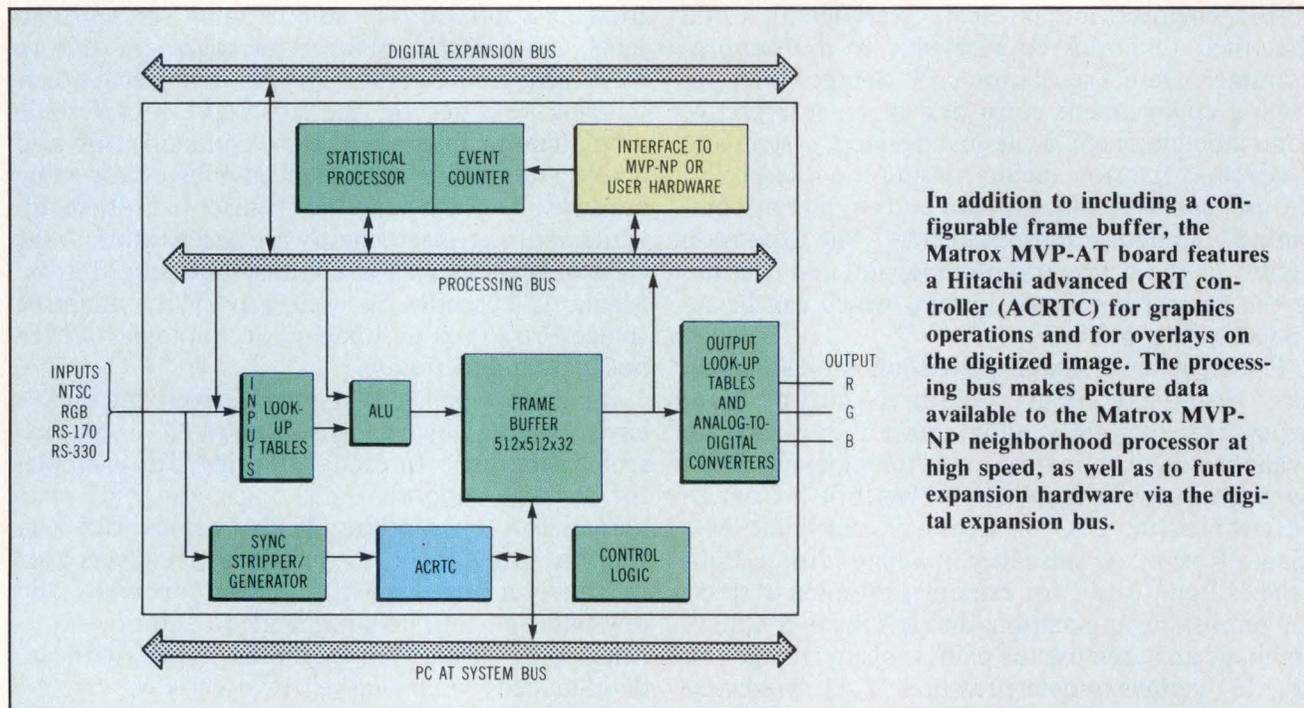
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In addition to including a configurable frame buffer, the Matrox MVP-AT board features a Hitachi advanced CRT controller (ACRTC) for graphics operations and for overlays on the digitized image. The processing bus makes picture data available to the Matrox MVP-NP neighborhood processor at high speed, as well as to future expansion hardware via the digital expansion bus.

operations. The contrast can then be distributed according to a desired curve (bell, cube, exponential, linear or log) for equalization.

The Imaging Toolkit stores its images in main-memory buffers where they are directly accessible to the AT's CPU, allowing device independence. The system can maintain and operate on 8-bit pixel data even if the display controller is only capable of handling 4-bit pixels. The image-processing and analysis portions of the package support image compression for storage and FFTs. Using an 80286 CPU with an 80287 coprocessor, the Toolkit can process a 2-D FFT on a 128- \times 128-pixel area of interest in a little over 1 min, according to Mike Abernathy, vice-president of software development at Rapid Imaging.

In addition to image processing, the Toolkit supports image generation in the form of three-dimensional color graphics. These capabilities include the ability to create ray-traced images showing the effects of light rays being reflected by surfaces or refracted by translucent objects. Ray-tracing techniques can be applied to captured images as well. A number of 2-D images made by a CAT scanner, for example, can be stacked and shown in perspective in 3-D space with portions of slices in the background showing through slices in the foreground.

Board suppliers addressing specific applications, such as machine vision, seldom need the entire variety of imaging operations. These manufacturers are interested in developing specific software functions

and putting as much of their functions as possible into hardware. The Cognex 2000 vision system incorporates specialized C-callable routines for searches for defined objects, character recognition and inspection. Cognex also supplies a development system for tailoring the vision processor to given applications. It includes the vision board in a stand-alone system, a camera, monitor and software. The software includes a C compiler, subroutine libraries, utilities, and recognition and inspection software.

Companies offering more general-purpose imaging systems have also recognized the need for more extensive development tools. Datacube, a supplier to the VMEbus market, provides a development system called Maxvision AT-1. The system consists of an AT with software and an interface card to the Maxvideo VME card cage. The user can interactively develop applications by building on the various module subroutine libraries. On the highest level, the AT-1 software accesses the module routines via a pop-up menu. Access for more experienced applications developers is still possible at the C calling level or the hardware primitives level.

More opportunities have opened for the application of image-processing technology than even those applications accessible by low-cost board-level products. The most immediate and potentially largest of these is in desktop publishing. The goal of computer-based publishing applications is to eliminate the need for cutting and pasting

to make up pages that will be printed. In addition to typesetting directly from word processors, there's also the need to incorporate graphics and images onto a page.

Already there are software programs, such as Postscript from Adobe Systems (Palo Alto, CA), which allow typesetting and formatting text for output on laser printers. Page composition programs, such as Pagemaker from Aldus Computers (Seattle, WA), provide a form of electronic paste-up so that the user can position blocks of text and graphic elements on a page, as long as the elements exist as image files. Getting text and image data into the system in the proper form to lay out a page, however, is a problem that remains unsolved.

The intelligent image scanner is one useful tool in the quest for the all-electronic paste-up. Scanners used in conjunction with desktop publishing systems are increasingly using image-processing technology developed for higher end applications. These techniques and algorithms, aided by the advent of fast, specialized silicon that has yielded the board-level products discussed above, are finding their way into chips and boards tailored to the needs of document processing and publishing.

All three basic stages of image processing are being used, in different degrees, in intelligent scanners. In the image-capture stage, the page image is scanned and stored either in the scanner or in the host computer. In the image-modifying stage, various filtering or correction algorithms are applied to clean up text, for example, or to correct the contrast of a photograph. In the image-transforming stage, data needed by the application are extracted. This includes character recognition, halftone crea-

tion, or conversion from raster to vector format.

The image-capture capabilities of a scanner must be able to produce sharp black-and-white images for text. There's also a growing need for scanners that can handle multiple levels of gray scale so that photos can be input directly. At least some of the capabilities of manipulating the scanned image and extracting data from it, such as character recognition, are beginning to be built into scanners.

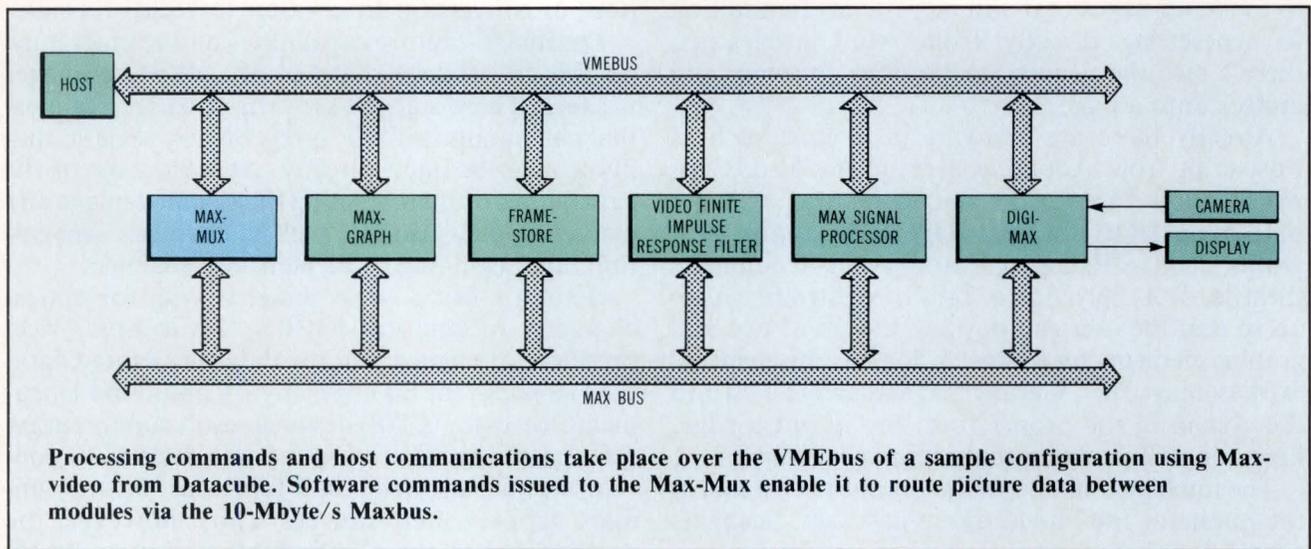
Getting a sharp, clear image is vital for optical character recognition (OCR). David Ross, vice-president of engineering for Palantir (Santa Clara, CA) stresses that his company's Compound Document Processor (CDP) design doesn't support gray-scale scanning. The company has decided to concentrate instead on the OCR functions. Bit-map images from other sources can, however, be downloaded to the CDP's 2-Mbyte image RAM, and the CDP scans line drawings like text, producing bit maps of the line drawings.

To obtain a clear 300-dot/in. image, which is the standard resolution for laser printers, the CDP scans the page at 400 dots/in. The CDP has algorithms that throw out one in every four pixels to obtain the desired 300-dot/in. image. "It cleverly throws out one in four—but it's not every fourth one," Ross says. Any time a single white pixel is bound by two black pixels, or vice versa, that isolated pixel is retained; consequently, no transition from white to black or black to white at the 400-dot/in. resolution is lost. The pixels that are most often dropped are from large areas of black.

Although OCR manufacturers jealously guard their recognition algorithms, a great deal of processing occurs before the actual recognition starts,

Possible operations using Image-Pro software from Media Cybernetics include, clockwise from upper left, graphics overlay, a histogram of pixels according to gray level, pseudo-color, and area-of-interest processing.





according to Richard Shoenhair, manager of applications development for Dest (Milpitas, CA). Filtering extraneous information and noise that might render letters ambiguous approaches the complexity of artificial intelligence problems. Palantir's CDP uses a program for image clean-up and another, based on self-contained context rules for English, that can resolve ambiguous characters. It also uses a 70-kbyte, on-line dictionary, and two supplemental dictionaries that can be downloaded.

This amount of AI-like processing is necessary for the CDP because Palantir has implemented "omnifont"—a program that recognizes any roman alphabet—OCR rather than supporting a set of downloadable fonts that its scanner will recognize. The company is expected to introduce a product that can recognize handwritten text in the near future. This may explain why the current version of CDP ROM program code occupies 1.5 Mbytes, and the document processor runs at a speed approaching 60 Mips for its specialized set of functions.

Datacopy (Mountain View, CA) is also placing more image-processing intelligence inside the scanner. Datacopy and Ricoh (Tokyo, Japan) are jointly developing an intelligent scanner that will contain processors and a firmware interpreter for the Prescript language. Prescript routines will be callable from user applications programs and will include image-processing functions such as compression, gamma (contrast) correction, thresholding and convolutions.

The two critical parameters for today's scanners are a resolution of 8 bits/pixel and 256 levels of gray, according to James McNaull, vice-president of strategic planning at Datacopy. The ability to capture an image with many levels of gray scale and to produce good halftones from that scanned image

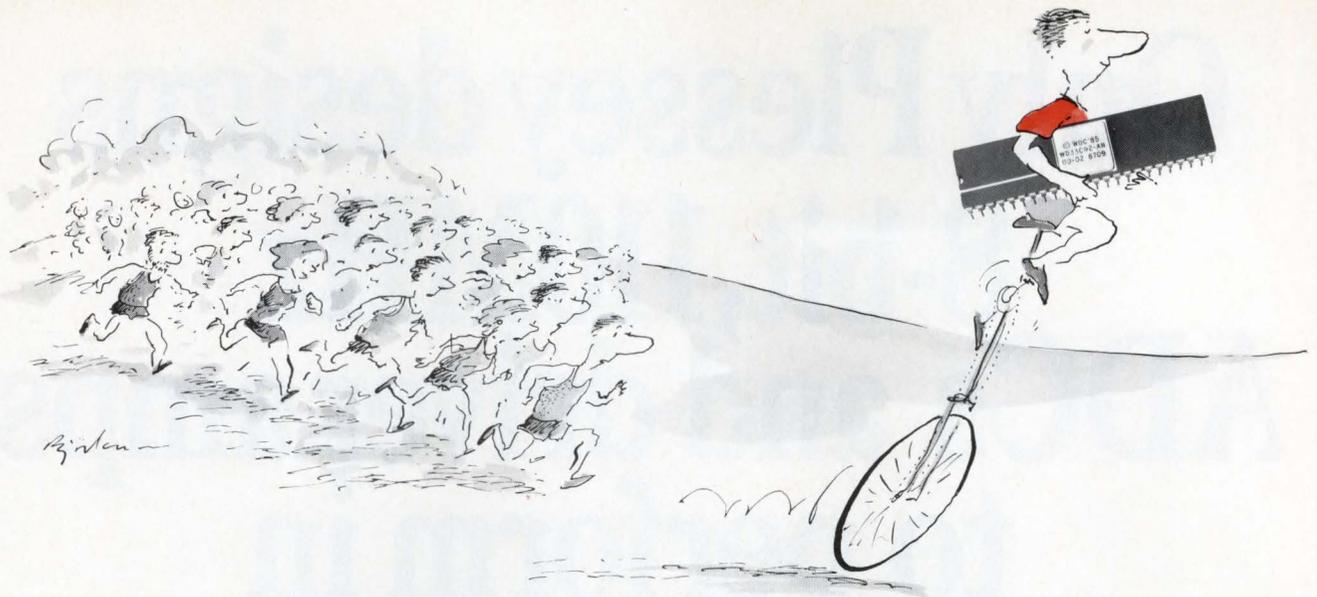
is essential for eliminating photoprocessing and cut-and-paste work from desktop publishing.

The image-processing task involved in converting a gray-scale image to a halftone requires computing an average value for pixels in a given $n \times n$ area, called the halftone cell. Sixteen 8-bit pixels in a 4×4 matrix, for example, would be converted to a value that would represent the gray value for that matrix. The matrix would be represented as a pattern of n black pixels in the 16-pixel square. The processor would then have to determine the pattern to use in placing the dots, such as spirally from the center, diagonally, and so forth.

Another set of image-processing functions vital to document processing is image scaling and gamma correction. Even before creating a halftone, the user may want to change the size or aspect ratio of an image or to crop it. If the image is scaled, the contrast will probably change and will have to be corrected. By obtaining a histogram of the gray-level distribution, the user can redistribute the brightness levels to restore or improve the contrast to bring out details. **CD**

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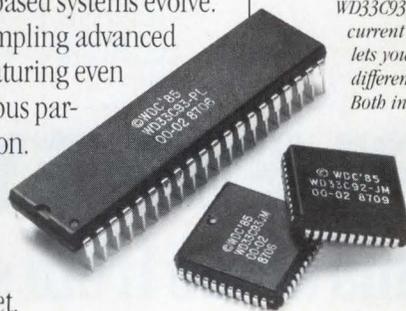
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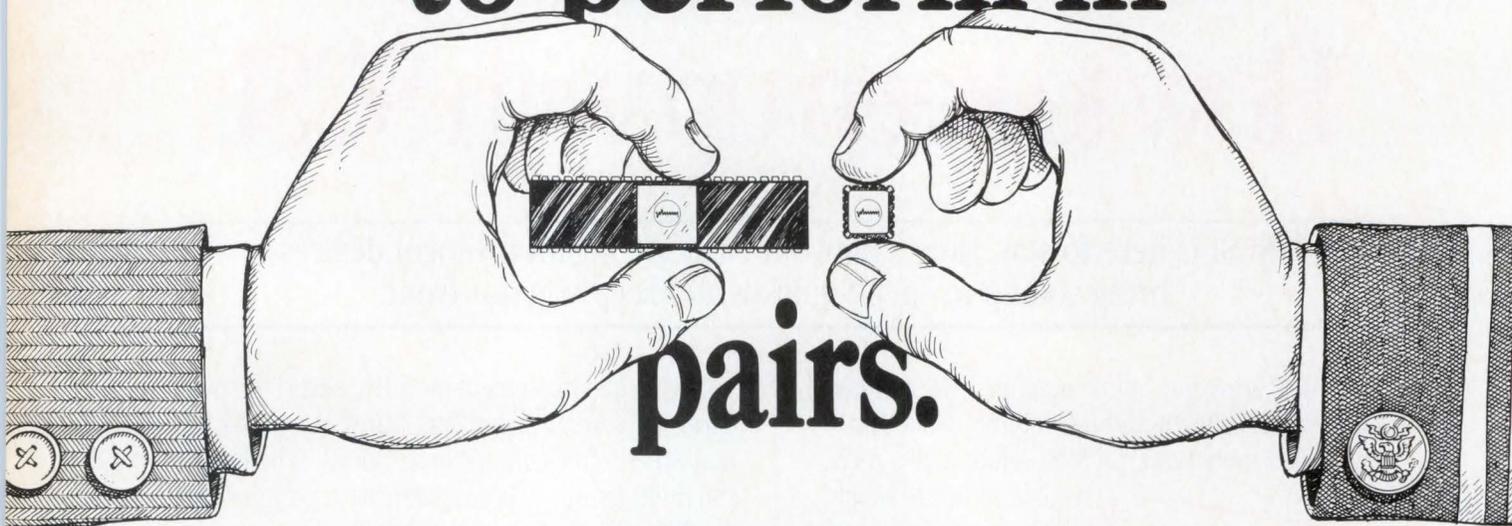
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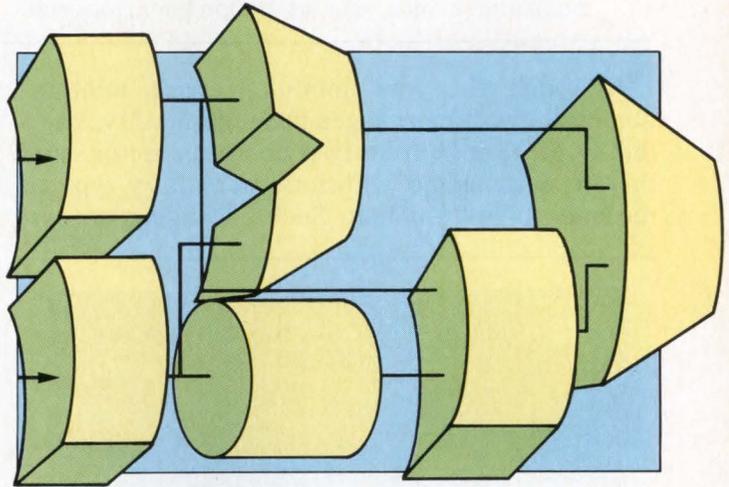
Single-chip processor runs Lisp environments

With the new dedicated Lisp chip, intelligent Lisp/AI workstations can be made much smaller, easier to use, and more affordable as either applications development tools or delivery vehicles.

A dedicated single-chip Lisp processor has been designed by Texas Instruments to replace multiple boards of MSI- and SSI-based parts. With an architecture that's optimized for Lisp/artificial intelligence applications, the new Lisp chip is one of the first of a generation of chips that will use the combination of VLSI processes and procedures that TI calls Megachip technologies.

The chip represents what can be accomplished with VLSI technology. Using 1.25-micron CMOS design rules, designers fabricated more than 553,000 transistors on a 1-cm² chip that implements 60 percent of the functionality of the original, full-size processor of the Explorer AI workstation.

Providing a powerful Lisp environment for the rapid development of AI software, the Explorer was one of the first 32-bit workstations suitable for the office environment. Explorer's genesis began with the introduction of the first Lisp machine, the CADR, developed by the Massachusetts Institute of Technology (Cambridge, MA) in 1978 under sponsorship of the Defense Advanced Research Projects Agency (DARPA). As a result of the new Lisp chip and Megachip technologies, Explorer



performance will increase by about five times and its IC count will be significantly reduced.

The Lisp chip will be the basis for a Compact Lisp Machine (CLM) that will be used in defense systems. Also DARPA-sponsored, the CLM will let the powers of Lisp and AI be put in a package small enough to fit in fighter aircraft cockpits. The CLM consists of four high-density circuit modules that can be mixed and matched. Intended for system-development applications, the modules comprise a processor, a cache, a mapper, a memory and an outside bus interface.

The four modules interconnect via the 32-bit, MIT-developed Nubus. The Explorer, the CLM and several other commercial computer products use the Nubus because of its processor independence, high speed, and ability to handle almost any combination of disparate processors in a multi-processor environment.

Gene Matthews, Robert Hewes and Steve Krueger

Matthews is director of the Symbolic Computing Laboratory of the Computer Science Center at Texas Instruments (Dallas, TX). Krueger is a senior member of that laboratory's technical staff, and Hewes is associate director of the company's VLSI Design Laboratory at the Semiconductor Process and Design Center.

CLM takes the Nubus

The Nubus, operating with a 10-MHz clock to achieve a maximum bandwidth of 37.5 Mbytes/s, is a synchronous, high-performance, processor-independent, 32-bit bus designed to support a multiprocessing environment such as the Compact Lisp Machine (CLM). It's optimized for block transfers of 2, 4, 6, 8 or 16 words, but it also supports word, halfword and byte transfers. Reading from or writing to its 4-Gbyte physical address space are the sole operations necessary and require only a simple interface protocol.

The Nubus' arbitration protocol is a combination of priority encoding and round-robin techniques. When the bus is lightly loaded, this combination provides fast access for high-priority devices. When heavily loaded, however, the combination provides equal access. Nubus also supports bus locking for indivisible operations.

The bus requires 49 signals as well as power and ground. It comprises 32 multiplexed address/data lines (with parity optional), two multiplexed mode/status lines, four arbitration lines, four slot-

identification lines and seven control lines for clock, reset and so forth.

Each bus module receives its slot identification from the backplane, identifying it by its physical location. Because the ID lines are part of the address decoding, there's no need to set switches or jumpers to identify the modules.

A fixed area in the address space of each slot defines a configuration ROM on each bus module. By reading those ROMs, the bus master can easily determine the configuration of the entire system.

In Nubus, a write operation called an event can generate an interrupt. Address-sensitive hardware detects those events. Because any event can be signaled by software or hardware, this simple protocol of events provides a flexible and powerful symmetry between hardware and software.

In addition to being used in Texas Instruments' CLM, Explorer and various business system product families, the Nubus is also used in the new Macintosh II, recently introduced by Apple Computer (Cupertino, CA).

Although the four modules aren't military-qualified, they're packaged in a high-density, size 6 (6.58 × 5.875-in.) military-style form factor, and they're designed to withstand a military type of mechanical environment. Such packaging lets sys-

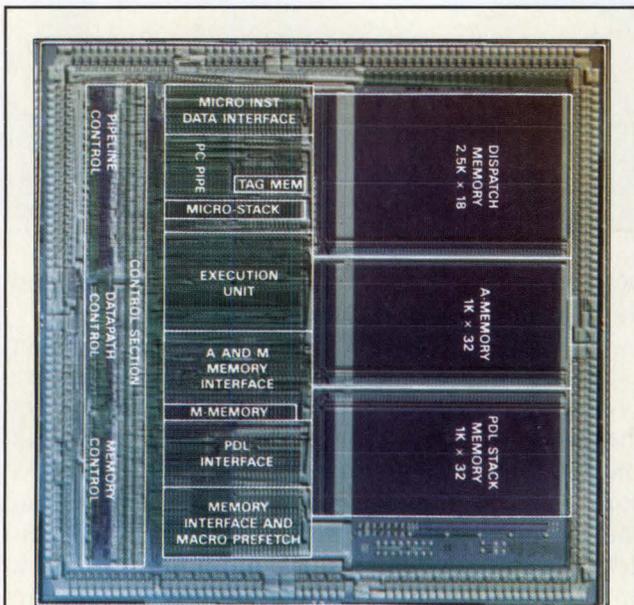
tem designers fit a CLM system into a volume as small as a shoe box. This size contrasts sharply with the several cubic feet that today's Lisp systems occupy, a fact that makes the current systems unsuitable for use as Lisp/AI applications delivery vehicles in aircraft or tanks or even for use in many commercial AI applications.

In each module, two circuit boards are bonded to a metal thermal core. The circuit boards are ceramic with copper thick-film interconnection on a cofired ceramic substrate. A surface-mounted high-density connector at one end lets the board be plugged into the bus socket. Wrap-around conductors provide connections between the boards. Optional metal covers protect the components.

The new Lisp chip is at the heart of the processor board of these four modules. Certain system designs—a plug-in board for a personal computer, for example—could use the processor board in conjunction with other boards that aren't designed for the CLM.

TI is developing system software and development tools for the CLM without government funding. The software is based on the industry-standard Common Lisp environment with extensions for Lisp machines. Object code-compatible with Explorer, the software and development tools include a set of CLM diagnostics and an Explorer-compatible interactive software development/debugging system.

Since microcode executes many of the CLM's instructions, the CLM processor module contains a write-controllable microcode-store 16k × 64-bit



On the new dedicated Lisp processor, some 553,000 transistors are implemented in 1.25-micron CMOS design rules on the new dedicated Lisp processor. These transistors implement about 60 percent of the processor-chip circuits of a high-end Lisp workstation.

static RAM for the Lisp processor itself. Packaged in a custom 264-pin grid array, the processor is memory-intensive and contains over 100 kbits of RAM. A 45-kbit dispatch memory contains multiway branch tables. One 32-kbit memory acts as a top-of-stack cache, and another 32-kbit memory provides a general-purpose scratch pad.

The processor module also contains a clock generator and an interrupt interface for the Lisp processor chip. Local software-controlled timers connect to the processor via its 32-bit virtual memory address and data buses. These buses also connect to booting and configuration ROMs and to a Nubus interface circuit. Because the Lisp chip is new, a debugging interface provides access for testing and development of the system software and microcode on existing Explorer machines and provides the system designer with a productive development environment.

Maximizing memory bandwidth

The CLM main memory is contained on one or more memory modules. Each module has a 2-Mbyte capacity and consists of an array of 72 dynamic RAMs, each configured as 256k × 1-bit. Each of the 4 bytes that make up the system's 32-bit word has a separate parity bit generated and checked by parity circuitry. The status-logic circuitry records errors detected by the parity circuitry. The control logic implements the address multiplexing, timing and control signals for accessing and refreshing the DRAMs.

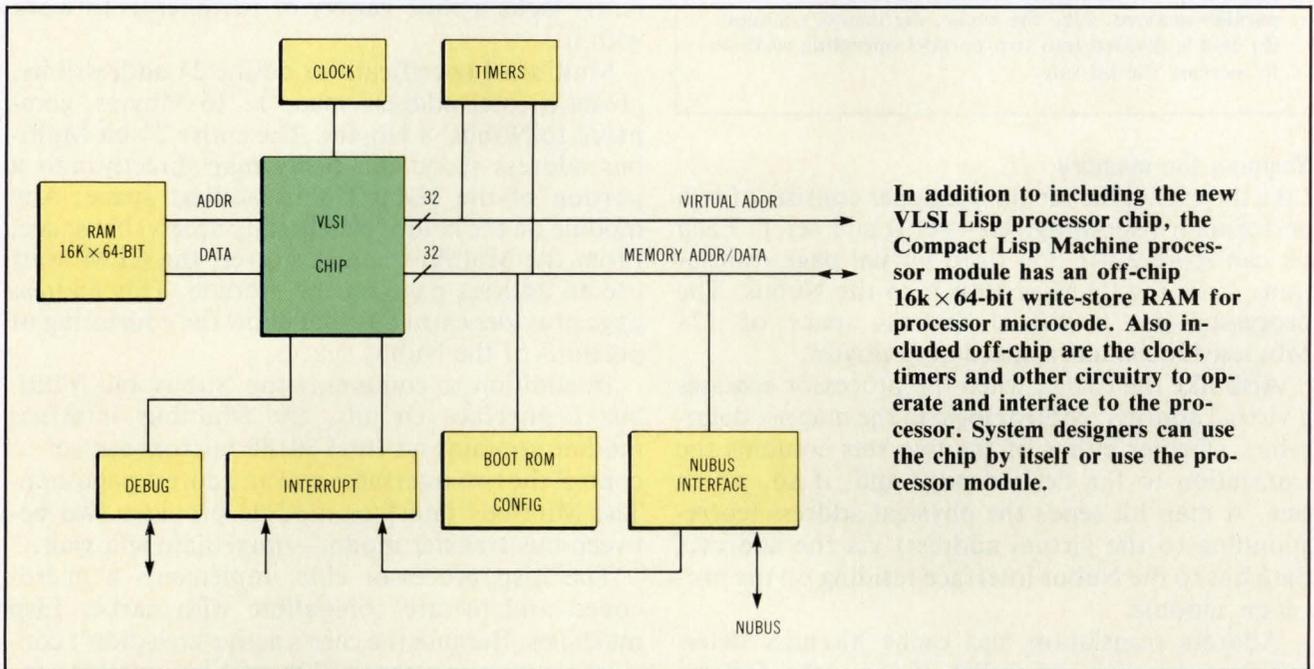
The Nubus interface of the memory module sup-

ports block as well as byte and half-word transfers. To speed updates to system cache memory, the transfers of commonly used four-word blocks are optimized.

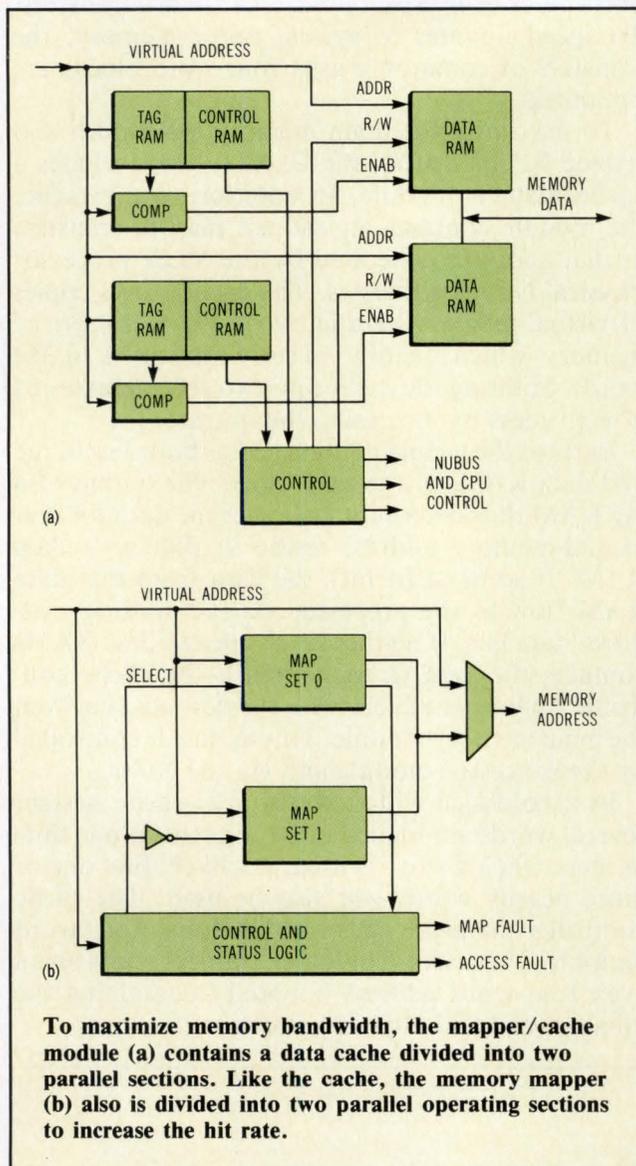
To maximize the main memory bandwidth and reduce Nubus traffic, the CLM system includes a cache/mapper module. In addition to the cache, the module contains an address map to translate virtual addresses generated by the VLSI processor physical Nubus addresses. The cache stores copies of virtual-memory data in two 8,192-word sets of memory, which means total store capacity is 16,384 words. Splitting the cache into two sets increases its effectiveness by increasing the hit rate.

Parts of the virtual address access both sets of tag and data RAMs at the same time. The output of a tag RAM thus determines whether the data for that virtual-memory address reside in that set's data RAM. If so (a cache hit), the data from that data RAM flow to the processor via the module's address/data bus. If neither set of tag and data RAMs contains the data (a cache miss), the cache controller updates the cache with the desired data from the main memory module. This update is controlled by the processor module and via the Nubus.

In accordance with conventional cache design, several words are loaded into the cache at one time because when a word is used, it's likely that one or more nearby words will also be used. The cache controller therefore calls for the Nubus four-word data-block transfer. This block transfer starts on an even four-word address boundary containing the missed word and adjacent words.



In addition to including the new VLSI Lisp processor chip, the Compact Lisp Machine processor module has an off-chip 16k × 64-bit write-store RAM for processor microcode. Also included off-chip are the clock, timers and other circuitry to operate and interface to the processor. System designers can use the chip by itself or use the processor module.



To maximize memory bandwidth, the mapper/cache module (a) contains a data cache divided into two parallel sections. Like the cache, the memory mapper (b) also is divided into two parallel operating sections to increase the hit rate.

Mapping the memory

Like the cache, the memory mapper consists of two performance-speeding sets—set 0 and set 1. Each set can store 2,048 256-word virtual page translations from the CLM processor to the Nubus. The processor has a virtual address space of 128 Mbytes; Nubus has a space of 4 Gbytes.

Also like the cache, when the processor accesses a virtual address, control logic in the mapper determines whether either of the two sets contains the translation to the desired page and, if so, which one. A map hit sends the physical address (corresponding to the virtual address) via the address/data bus to the Nubus interface residing on the processor module.

Address translation and cache hit/miss determination proceed in parallel. If the cache declares

a miss, the Nubus' physical address of the desired data in the CLM main memory could be immediately available. If the cache declares a hit, the processor doesn't need the address.

After a cache miss, it's possible that neither set of the map contains the translated address of the desired page. Such a map miss requires that the processor, under microcode control, determine the address translation and enter it into one set of the map. Addresses don't always need to be translated. The mapper can also use the physical addresses directly without translation.

The mapper contains a separate address-space status map. It divides the 128-Mbyte virtual address space capability of the processor into 4,096 regions of 32 kbytes each. Eight status bits for each region and additional status logic provide hardware support for the CLM garbage-collection function, separating some of that function from the virtual address translation.

Interfacing to the world

System designers who opt for the CLM or the Lisp chip will need to connect their designs to the outside world. Because the CLM designers expect that initial applications of the modules will be designed to widely varying requirements, there's a need for an interface—the Multibus interface module to the popular Multibus I commercial bus.

Many different types of I/O, graphics and other peripheral products are available for this bus. The Nubus, which is being considered as an IEEE standard, is ideal for supporting a Lisp system but currently lacks a wide variety of peripherals to work with it.

Multibus I specifications define 24 address bits, giving a total address space of 16 Mbytes, compared to Nubus' 4 Gbytes. The entire 24-bit Multibus address space can easily map directly into a portion of the 32-bit Nubus address space. Any module on the Nubus can directly access that space. From the Multibus end, however, the CLM must use an address page on the module. This address page provides extra bits that allow the addressing of portions of the Nubus space.

In addition to containing the Nubus and Multibus I interface circuits, the Multibus interface module contains an Intel 80188 microprocessor to control the two interfaces and an address page map. The Multibus interface module provides two between-bus transfer modes—immediate and wait.

The Lisp processor chip implements a microcoded architecture compatible with earlier Lisp machines. Because the chip's active area didn't contain enough room for the 32k × 64-bit writable con-

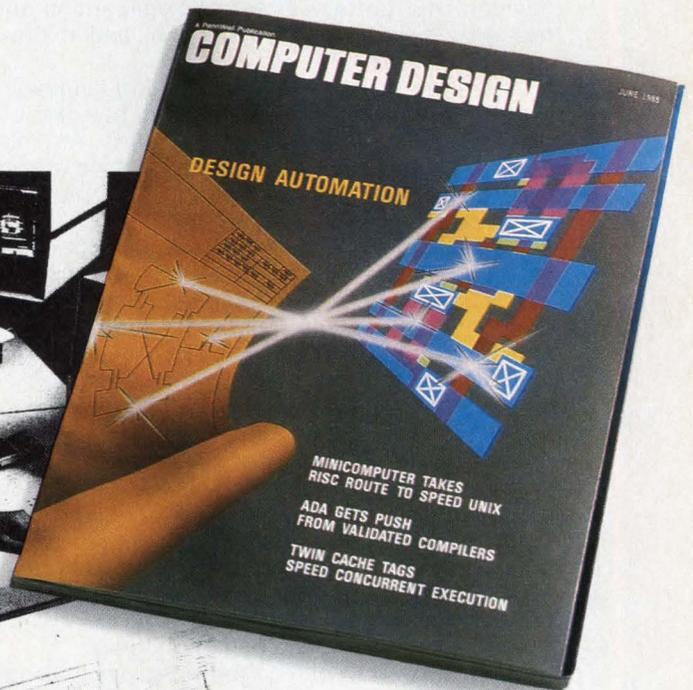
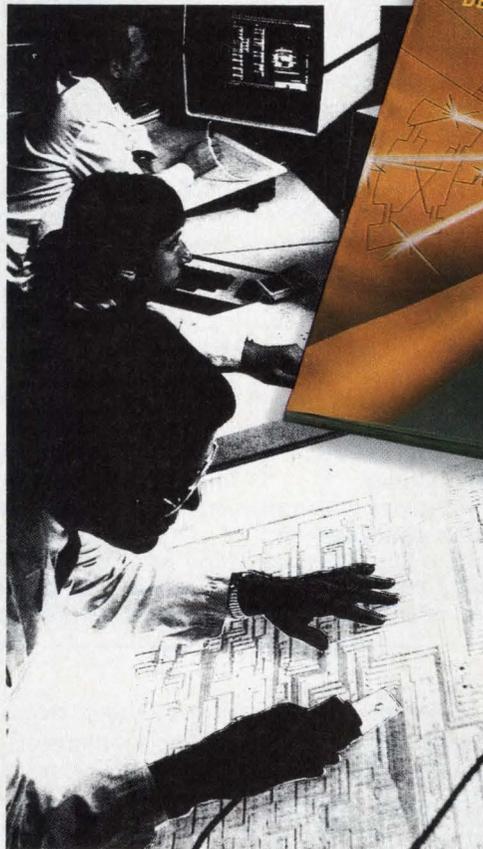
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Symbolic languages fill AI needs

Although all programming languages use symbols, conventional languages such as Basic, Pascal and C are intended primarily for numerical operations; numbers are the symbols they manipulate most readily. In contrast, artificial intelligence applications need to actually manipulate abstract, nonnumeric symbols.

To meet this need, purely symbolic languages such as Lisp and Prolog and their dialects were developed. To create a standard, a new dialect called Common Lisp has been developed and widely adopted. Incorporating the richness and power of its many predecessors, Common Lisp provides true portability for AI applications and thus has found strong commercial and military support.

Lisp differs from most programming languages in three important ways. First, Lisp has flexible data structuring in lists and structures. Any element of a list or structure may be any type of Lisp data. Lisp data may be structured naturally to match complex applications.

Second, Lisp's syntax is relatively simple. It has just two types of program elements—atoms and expressions. Atoms are variables, constants and functions; expressions consist of a function atom and its operands, which may be either kind of program element. Expressions are represented as lists, so it's easy for programs to construct or modify expressions.

Lisp functions can be interpreted from this list form or compiled into machine language, and the two types of functions can be freely intermixed. Because Lisp functions can run in an interpreted mode and because of the uniform list structure of the data, the programmer can interact closely with the code under development. This flexibility also allows extensive and speedy debugging.

The basic unit of data is the fixed-size cell containing three fields—a data type, a data value and CDR code. When data are too big to fit in the data value field or are of variable size, the cell's data type indicates that its data value is an address or

pointer to where the data are located in a block of storage located elsewhere.

The Explorer, the Compact Lisp Machine (CLM) and the Lisp chip support a wide variety of data types, including many numeric data types. In addition to these "programmer-visible" types, several internal types are used by Lisp. These internal types serve the operation of both the Explorer and the CLM.

Because the data carries its type with it, many of Lisp's basic operations are generic; they apply to multiple data types. For instance, one ADD operation works for all number representations and accepts floating-point and even complex numbers as well as integers. Attempts to operate on invalid data types, such as adding a "list" to an integer, however, cause the operation to abort with an error message. Checking for invalid data types is done both at compile and run time.

In manipulating lists, Lisp typically uses many large and small chunks of memory for short periods of time. This activity, unfortunately, can quickly fragment and exhaust the memory space. Techniques for periodically reclaiming the chunks of memory no longer used are collectively called garbage collection. Both the Explorer and the CLM have built-in garbage collection transparent to the user. This garbage collection works while the computer is used for other purposes.

The key to speedy garbage collection is the typed data concept. Typed data let the garbage collector circuitry recognize all pointers in the data. Data addressed by some nongarbage pointer aren't garbage, but data that aren't addressable are garbage.

The garbage collector rearranges the blocks of data to remove fragmentation and restore the memory to a linear, contiguous order. This automatic memory management requires overhead. For maximum system throughput, garbage collection is accomplished in hardware wherever possible. The Lisp processor enjoys the services of hardware-assisted garbage collection.

trol store, the microcode resides off-chip.

The Lisp chip supports many Lisp typed-data operations, including multiway branching for data-type checking; additional data-type checking and result tagging; and bit-field depositing or extracting for manipulating data objects internally. It also provides hardware support for garbage collection.

The reliability and quality of such a chip are major considerations. The processor is based on a 100 percent scan design, for example, and includes a signature-analyzer feature and a 16-kbit microcode ROM for self-test. But just 2.5 percent of the chip is devoted to these capabilities, which are essential to ensuring a testable Lisp system design. Further-

more, the processor was designed for zero static-power consumption. Faults involving dominance are detected by monitoring the processor power supply current.

On-chip memory dominates

Since Lisp is memory-intensive, on-chip memory dominates the chip's area. There are three larger memory units—two 1k × 32-bit and one 2.5k × 18-bit RAMs—and three smaller ones. A 256 × 64-bit microcode ROM provides the code for both booting and self-test. The chip's data paths take most of the remaining chip area, except for a small part for the control logic function.

Individual refresh counters and a master refresh timer support the RAMs. When the RAMs aren't engaged in other operations, the system refreshes them. If the refresh period expires before all RAMs can be refreshed, no more instructions are issued, so refreshing can be completed. Access time of the large memories is 17 ns; cycle time is 25 ns. This type of performance enables the processor's fast cycle time.

One of the $1k \times 32$ -bit RAMs (known as the A memory), a microcode scratch pad, acts as a single input source for the chip's arithmetic logic unit. The other $1k \times 32$ -bit RAM, a stack memory (called the PDL), and a small 64×32 -bit scratch pad (M memory) provide the other input. The PDL stores the top 1,024 words of stack on-chip. This design eliminates memory references that would be required to access or store these variables during function calls.

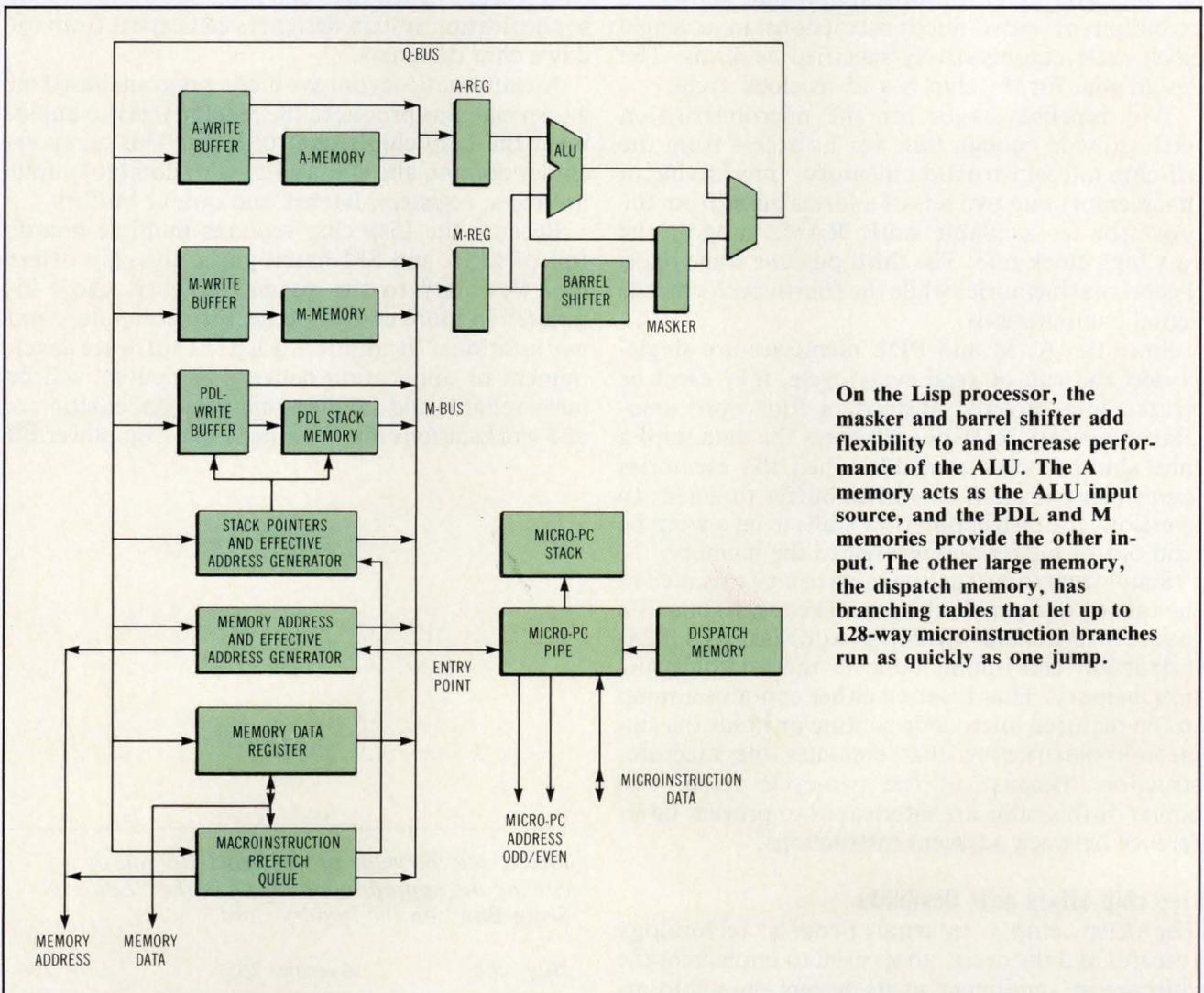
A 32-bit masker/barrel-shifter adds a great deal

of flexibility and performance to the ALU's data-processing ability. With its modified Booth's algorithm, the ALU can compute a 2×32 -bit multiply with one microinstruction. A normalization counter counts leading 0s or 1s to support floating-point calculations. A novel carry-select, lookahead circuit in the ALU lets the unit quickly compute the $ALU = 0$ state required for branching.

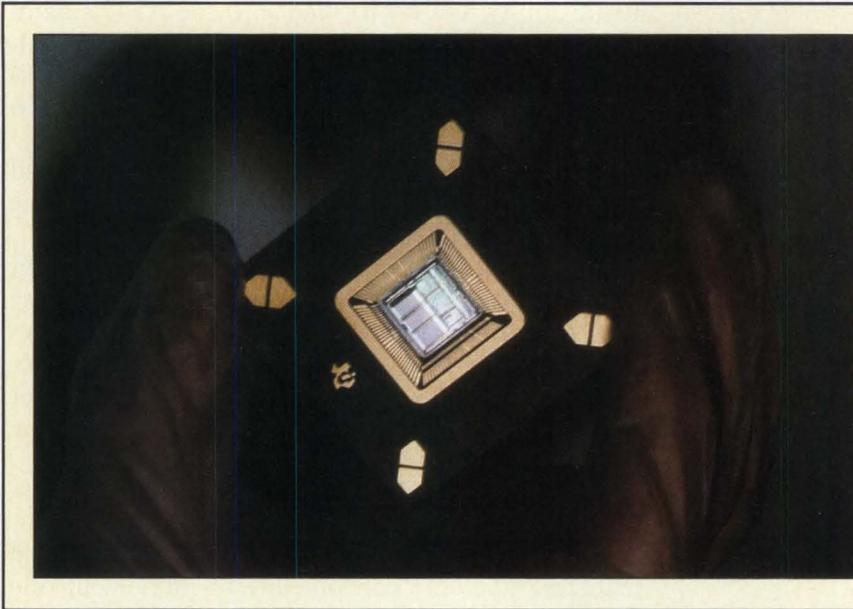
The remaining large memory, the $2.5k \times 18$ -bit dispatch memory, contains branching tables. These tables let up to 128-way microinstruction branches run as quickly as a simple jump. A macroinstruction prefetch unit prefetches up to four 16-bit macroinstructions, and statically follows the branches. This action speeds system throughput.

Other unusual features

The Lisp chip has many other unusual architectural features. The chip can pipeline to implement one microinstruction per system clock. High through-



On the Lisp processor, the masker and barrel shifter add flexibility to and increase performance of the ALU. The A memory acts as the ALU input source, and the PDL and M memories provide the other input. The other large memory, the dispatch memory, has branching tables that let up to 128-way microinstruction branches run as quickly as one jump.



A full computer system on a chip, the Lisp processor is the basis for the processor board in the Compact Lisp Machine. Occupying 1 cm², it also could form the heart of other Lisp systems, such as plug-in boards for conventional workstations and personal computers.

put is the goal here. A four-stage pipeline allows the execution of most microinstructions in a single clock cycle conservatively specified as 40 ns. The design goal for the chip is a 25-ns clock cycle.

Two pipeline stages for the microinstruction fetch provide enough time for its access from the off-chip microinstruction memory. Interleaving in that memory and two sets of address buses from the processor let available static RAMs support the very high clock rate. The third pipeline stage reads the internal memories while the fourth performs the actual computations.

Since the A, M and PDL memories are single-ported and can be read every cycle, they can't be written into directly. Instead, a four-word associative memory receives and stores the data until a time slot becomes available when the memories aren't being read. If this write buffer threatens to overflow, the instruction flow stalls to let a word be read out of buffer and written to the memory.

Simple macroinstructions also can be executed at the rate of one per clock cycle. The top 10 bits of a macroinstruction directly address a 1,024-instruction entry-point table in the microinstruction memory. That location either contains a jump to the required microcode routine or holds the single microinstruction that emulates the macroinstruction. Because of the two-cycle fetch, two copies of this table are interleaved to prevent interference between adjacent instructions.

Lisp chip offers new flexibility

The Lisp chip's internal process technology features and the design tools used to implement the chip are as significant as its system-on-a-chip ar-

chitecture. The features and tools show the level of sophistication system designers can expect from today's chip designers.

An automatic layout synthesis program based on a Lisp machine produced the regular array to implement the Lisp chip's control logic. This array includes domino and static gates with domino output inverters, registers, latches and output buffers.

Because the Lisp chip replaces multiple boards full of MSI- and SSI-based parts, the chip offers new flexibility to the system designer who's interested in more cost-effective Lisp computers and workstations. In addition, Lisp/AI software development or application delivery computers will be more reliable and smaller, and personal computers and workstations may be able to use Lisp power. **CD**

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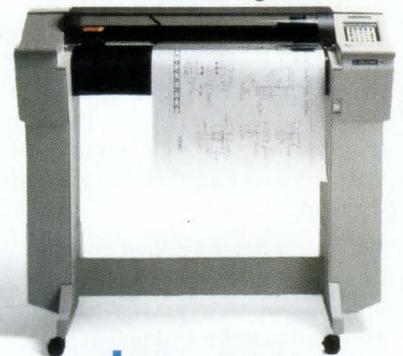
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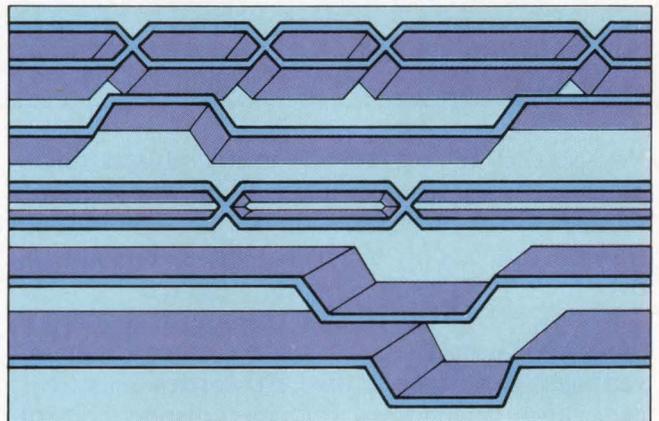
Busless graphics system boosts speed, lowers cost

No longer constrained by buses, a new graphics workstation provides a threefold performance improvement at half the cost of its predecessor without sacrificing flexibility and expandability.

Because they provide the flexibility and expandability necessary for changing or adding peripheral devices, I/O buses are usually considered essential elements of general-purpose computer systems. But whatever the CPU's natural computer power, the bus width and longer data-transfer times associated with its protocols can severely limit system performance. And the extra hardware dedicated to the bus and individual peripheral controllers increases the cost and takes more space, resulting in a larger, heavier system enclosure.

By using an identical CPU, eliminating the I/O bus and taking advantage of opportunities for additional hardware integration, designers can design a busless computer system that offers higher performance and lower cost than a system that uses a bus. Moreover, there are some types of computers, such as graphics workstations, in which these performance and cost objectives can be met without sacrificing any of the system's flexibility and expandability.

The busless VAXstation 2000 single-user workstation offers about three times the graphics performance of the Q-bus-based VAXstation II at about half its cost. Even without a general-purpose bus, this system is extensible in several important ways. It provides increased main memory (from 2 to 6 Mbytes), increased hard disk capacity, a backup



tape, a four-plane color video and an Ethernet network interconnect.

A busless system

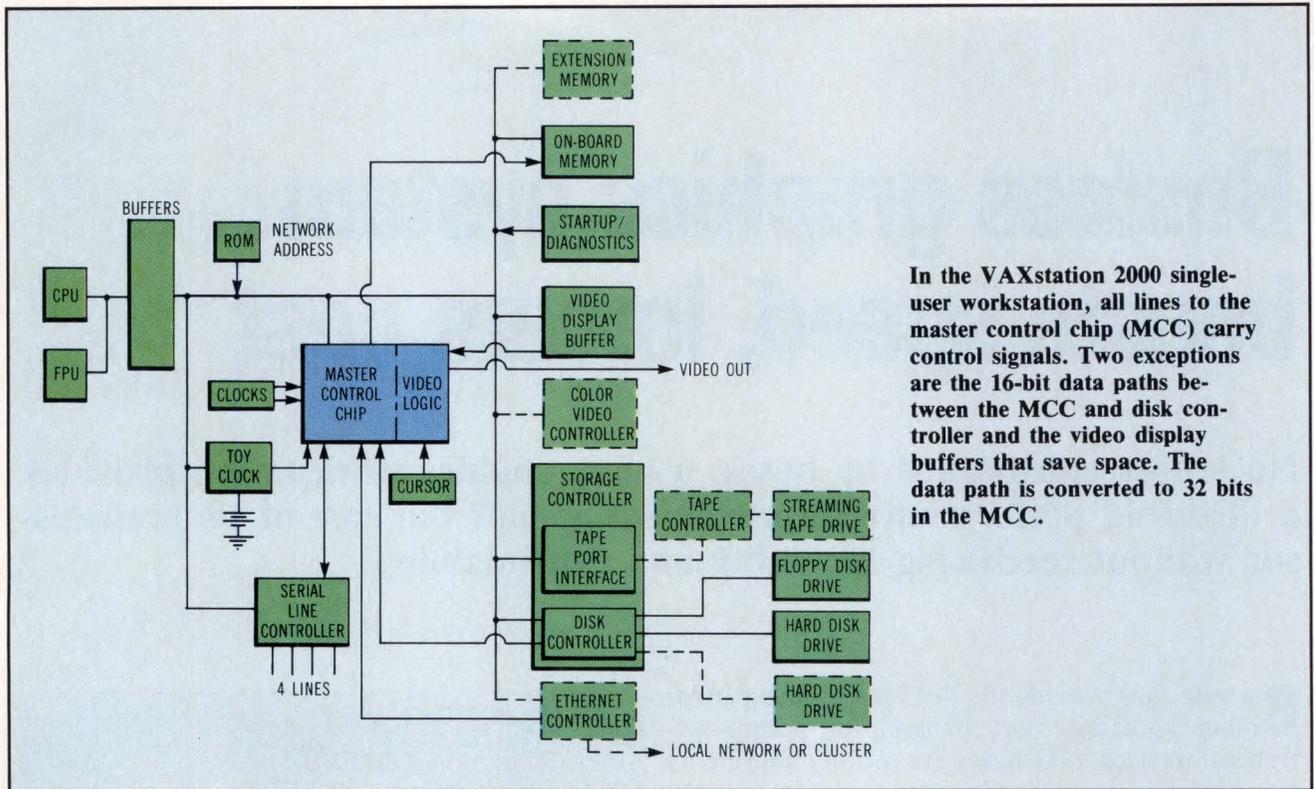
The VAXstation 2000 features components that support basic workstation operation and enhancement options. Instead of being linked by the Q-bus, all system components and peripheral devices are linked directly to the CPU through transceiver chips that buffer the CPU chip's I/O pins.

The system's designers had initially projected that the VAXstation 2000 could attain a fourfold increase in graphics performance over the VAXstation II. Half of this gain would be achieved by doubling the width of the data path between the CPU and the video display controller. The other boost would be achieved by doubling the speed of data transfer between the CPU and the video controller.

With the 16-bit data path in the Q-bus of the

John Kirk and George H. Lord

Kirk is a senior consulting engineer and Lord is a consulting engineer for Digital Equipment Corp (Maynard, MA).



In the VAXstation 2000 single-user workstation, all lines to the master control chip (MCC) carry control signals. Two exceptions are the 16-bit data paths between the MCC and disk controller and the video display buffers that save space. The data path is converted to 32 bits in the MCC.

VAXstation II, any 16 bits in a 1-Mpixel single-plane bit map—the bit map of the workstation’s monitor—can be changed in 1.2 μ s. The bit-map transfer time is only 600 ns for any 32 bits moving over the CPU’s native chip data path.

That CPU execution time remains unchanged in the VAXstation 2000. To achieve other design advantages, for example, the CPU carries out vector-generation calculations for video display control and does them no faster than it does in the VAXstation II. As a result, the architectural fourfold improvement in memory transfer performance actually results in a 2½ to 3 times improvement in graphics performance.

Eliminating hardware

Eliminating the Q-bus reduces costs because much of the system hardware associated with a general-purpose I/O bus is also eliminated. A busless system doesn’t need a card cage. Peripheral controllers can be either integrated on-board with other system functions or—for enhancement options—implemented on daughter boards.

Regardless of how many of its slots are actually occupied, a bused system must have available power for a fully populated cage at maximum possible power demand. Maximum power requirements for the VAXstation 2000’s system are lower than those required for a bus system cage, and they

can be precisely defined. The system can use a smaller power supply and a smaller, quieter cooling fan (50 dB or lower for the office environment).

Costs are also reduced by eliminating the bus drivers and receivers that are necessary on the peripheral modules for all devices connected to a general-purpose I/O bus. In addition, it’s possible to distribute and to share many peripheral control functions customarily grouped in an intelligent controller on each peripheral module. Whether integrated on-board or on daughter boards, VAXstation 2000 controller functions are implemented with significantly fewer components and in less board space.

Previous versions of the VMS operating system included device drivers designed for Q-bus devices. With the new system, new device drivers had to be written for all devices—disk, tape, video display and serial lines—and included in a new version of VMS. The fixed, predefined system configuration makes it unnecessary to include as many software tests at boot time as with a general-purpose I/O bus system, in which VMS looks for all possible devices on the bus and configures itself accordingly.

A single-board system

Because the basic VAXstation 2000 hardware configuration, which includes video display, disk, tape and serial line controllers, is implemented on one

10- \times 12-in. system board, total component count and interconnect cost is reduced. A single board is also easy to manufacture, assemble, test and service. Although the board is just 120 in.²—the largest size the enclosure would allow—it required extensive hardware integration. The principal hardware components of the VAXstation 2000 are the same as in the VAXstation II: a 32-bit MicroVAX II single-chip CPU, a floating-point unit, a 19-in. monochrome bit-mapped display monitor, a keyboard, and a mouse or a tablet.

Initial hardware-integration projections called for two gate arrays—one chip in 2-micron CMOS and one in emitter-coupled logic. ECL technology was considered necessary to handle the 70-MHz data rate required for video serialization in the display controller.

But after developing a 2-micron CMOS process with a standard-cell design library, and finding that Spice simulations indicated that CMOS standard cells were fast enough for video serialization, the designers determined that all system functions could be implemented on one large semicustom CMOS chip. A full-custom chip wasn't seriously considered because of its higher cost and longer design time, and because its greater speed offers no design advantage.

The resulting master control chip (MCC) is centrally located—functionally in the schematic and physically on the system board. The MCC is a

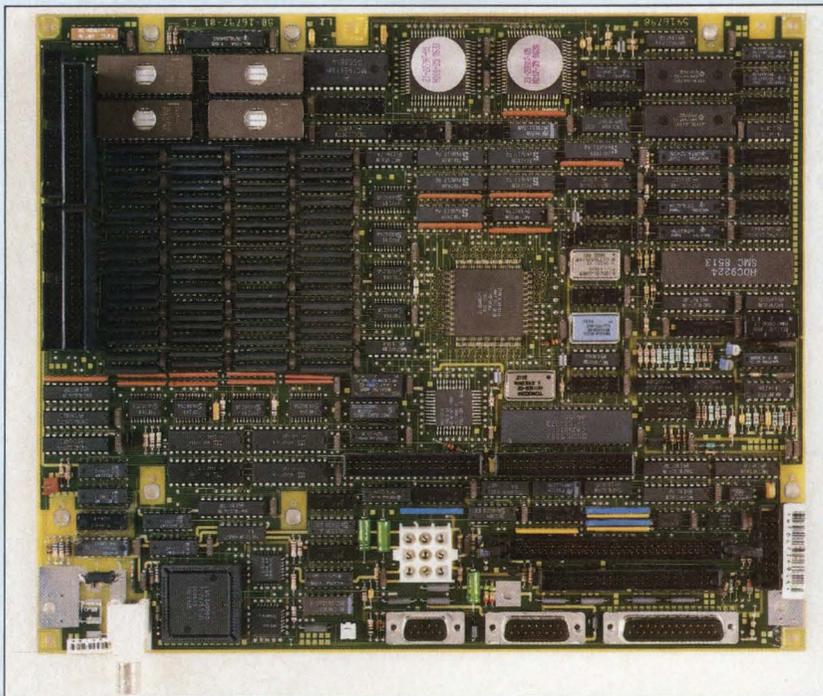
19,000-transistor, 25-mil pitch, 164-pin surface-mount device, the highest available pitch density for surface mounting.

Although in itself expensive, the 1.2- \times 1.2-in. MCC afforded a savings in hardware cost, enabling all the basic system functions to be put on a single system board. In contrast, MSI/LSI implementation of the same functions would require 70 to 80 chips, would double the system board's power consumption—from 25 W to 50 W—and would occupy about two-thirds of the total board area.

The chip contains many of the distributed peripheral control functions. Address decode, control and interrupt are common to all controllers (disk, tape, video display and serial lines), and so their MCC hardware is shared. Other MCC functions such as the disk subsystem, digital data separator and video serialization are device-specific.

Some peripheral control functions have been assigned to the CPU. Among these functions are the read head positioning for the disk controller and vector generation for the video display controller. Other peripheral control functions that specifically concern a general-purpose I/O bus have been eliminated entirely. The remaining peripheral functions are implemented in minimal space on the system board or on peripheral control modules.

The VAXstation 2000's video display controller, which uses about 15 percent of the MCC and eight ICs, occupies only 6 in.² on the system board. In



The basic hardware configuration of the VAXstation 2000 is implemented on one 10- \times 12-in. system board, the largest that can fit into the desktop enclosure. Connectors are provided for daughter boards and for storage devices in the system and expansion enclosures. Communications, monitor and printer connectors on the rear edge of the system board protrude through openings in the rear panel.

Busless system's synchronous write cycles improve timing

The VAXstation II's Q-bus specifications establish common interface protocols for address decode, control and timing, interrupt, and device-specific functions. These functions must be implemented on both the CPU and peripheral controller sides of the bus, regardless of the device's characteristics, so that any CPU and peripheral device can communicate over the bus when both meet Q-bus specifications.

In the busless VAXstation 2000, however, the characteristics of the limited number of peripheral options are known in advance and can be specifically accommodated by the system. Without the longer transfer times of the asynchronous Q-bus protocol, the system can control timing so that data transfers between devices can be matched to the device's natural speed. In contrast to a standard Q-bus write cycle of $1\mu\text{s}$, the VAXstation 2000's write cycle time can range from 400 ns—for CPU-to-memory transfers—to 800 ns—for transfers from the CPU to the time-of-year (TOY) clock.

Whatever the timing characteristics of the master or slave, the Q-bus write cycle (a) in the VAXstation II applies to asynchronous data transfers between a bus master and slave. The bus master can be the CPU or any direct memory access device on the Q-bus. The bus slave can be main memory or any peripheral device on the bus. The cycle is extended because the bus master waits for the slave to acknowledge the transfer (by asserting RPLY) and indicate that the data have been fully latched in (by negating RPLY). Only then can the master negate SYNC to end the cycle.

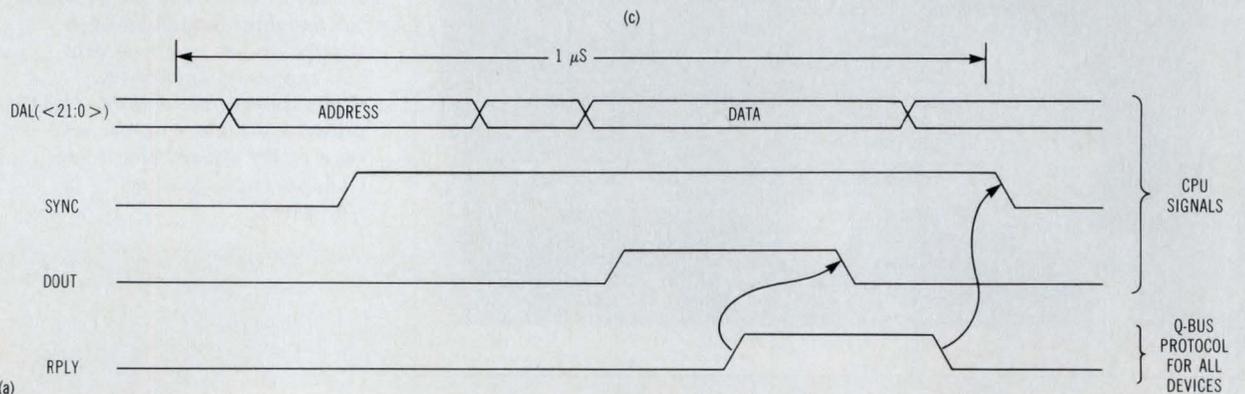
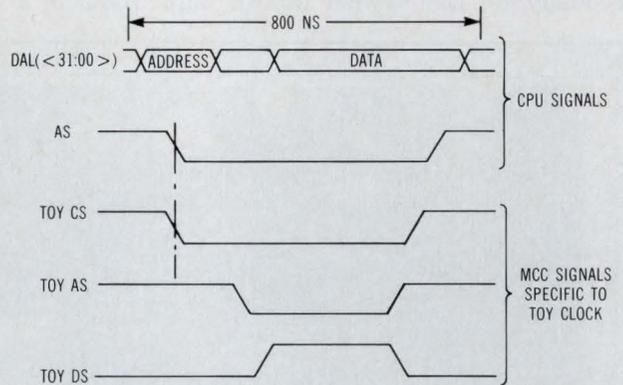
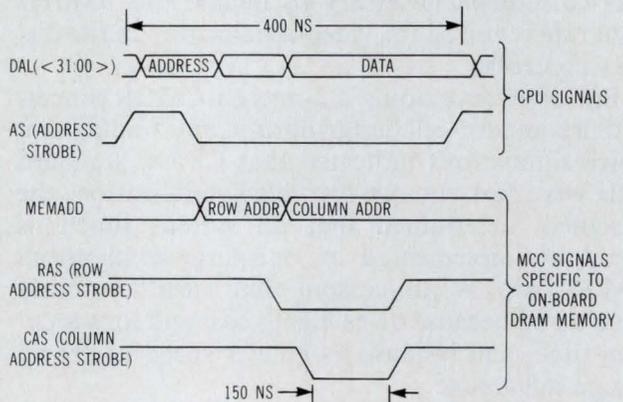
The VAXstation 2000's synchronous write cycles differ from Q-bus write cycles in two significant ways. First, the master can carry out the data transfer without waiting for a response from the slave. Second, the data transfer signals and timing are characteristic of the slave (receiving device) rather than fixed by I/O bus specifications.

In the 400-ns write cycle (b) of the VAXstation 2000, the address strobe signal tells the master control chip (MCC) that the data lines from the CPU are carrying a valid address to begin the next cycle. The MCC decodes the address and, based on the address, generates one of several sets of output signals that correspond to particular devices the

CPU can select for data exchange.

In the 400-ns case, the address is [001FFFFF:00000000]. The MCC's output signals are row address strobe and column address strobe signals, which identify row and column locations in memory. Data are written to the selected memory location, and the CPU ends the cycle by negating AS.

In the 800-ns write cycle (c) of the VAXstation 2000, the MCC generates an entirely different set of output signals for the TOY clock. Although it involves the VAXstation 2000's longest write cycle, a TOY clock write usually occurs only twice a year—when changing between standard and daylight-saving times. In frequency of execution, though, writes to memory are second only to reads.



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contrast, the VAXstation II's equivalent Q-bus video subsystem consists of nearly 100 ICs in 80 in.² of board area. In another example of distributed peripheral control, putting the digital data separator on the MCC has cut the disk controller's hardware on the system board to 29 chips from 41.

Expansion options

Three of the expansion options are daughter boards: a 4.5- \times 8-in. memory module (2 Mbytes or 4 Mbytes in 256-kbyte dynamic RAM chips); a 7.5 \times 10.5-in. four-plane color video controller module; and a 5- \times 8-in. Thinwire Ethernet controller module.

The DRAM chips on the extension memory module are double-side surface-mount to reduce the cost and to halve the volume required for memory. The extension memory and color video controller modules are mounted directly on device-specific connectors on the system board. The Ethernet controller module is fastened to the system enclosure just below the system board with short ribbon cables connecting the module to the system board.

The color video controller module is based on

five two-layer NMOS custom chips originally designed for DEC's VAXstation II/GPX color workstation. One address processor chip performs functions common to all four planes, such as bit-map address generation, raster-op computations and screen refresh. Four video processor chips provide data-transfer functions that operate in parallel in each plane. Among these operations are data first-in, first-out; refresh and scrolling buffers; and control store RAM.

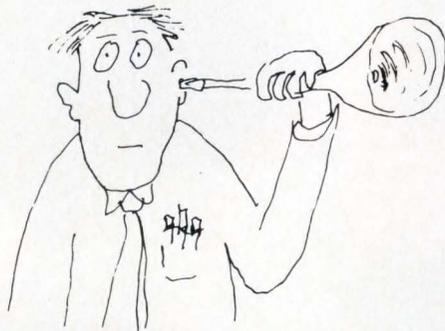
The color module also includes two semicustom chips (the second and third standard cell CMOS ICs manufactured by DEC) and one custom chip consisting of a three-channel, 4-bit digital-to-analog converter. This custom chip directly drives three 75- Ω coaxial lines to the color monitor.

To save hardware, the DEC designers made the Ethernet controller the only direct memory access device other than the CPU. Since data transfer between disks and memory is at the command of the CPU, while network data arrive at up to 10 Mbits/s with no CPU control over timing, designers chose the Ethernet controller rather than the disk controller for DMA, considering it more important to optimize memory access for Ethernet operation in workstation clusters.

By using the existing local area network controller Ethernet custom chip to perform the necessary virtual-to-physical address translation and scatter-gather mapping, a minimum of hardware and board space was consumed when DMA capability was provided for the Ethernet controller module. Providing more than this single DMA channel would have required adding a dedicated microprocessor and memory to the disk controller.

Disk access speed was increased by placing an output buffer in the disk controller and taking advantage of the VAX instruction set's block transfer move instruction (MOVC), a process that executes the necessary address translation. The CPU can transfer disk data asynchronously from buffer RAM to main memory solely by means of the MOVC instruction. Buffer/memory transfers take about the same time as DMA transfers from or to the disk controller. **CD**

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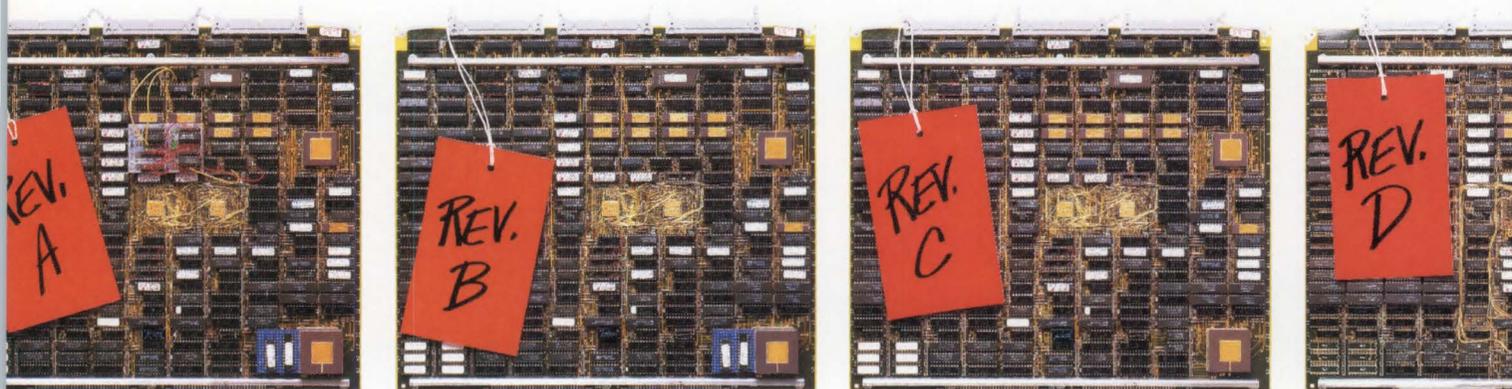
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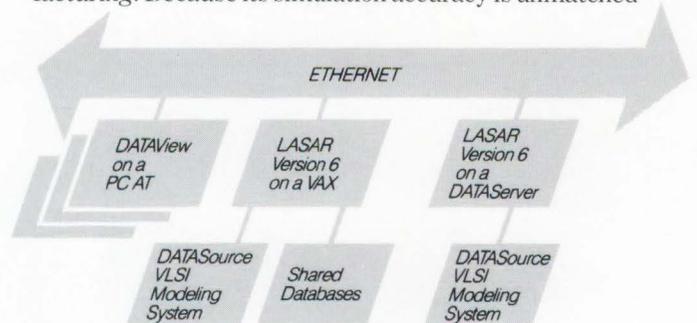
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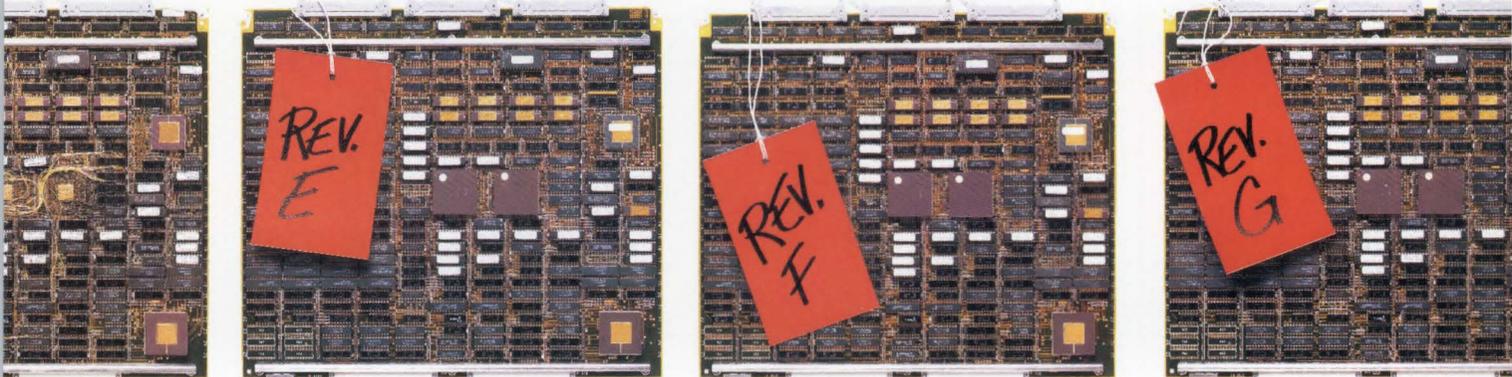
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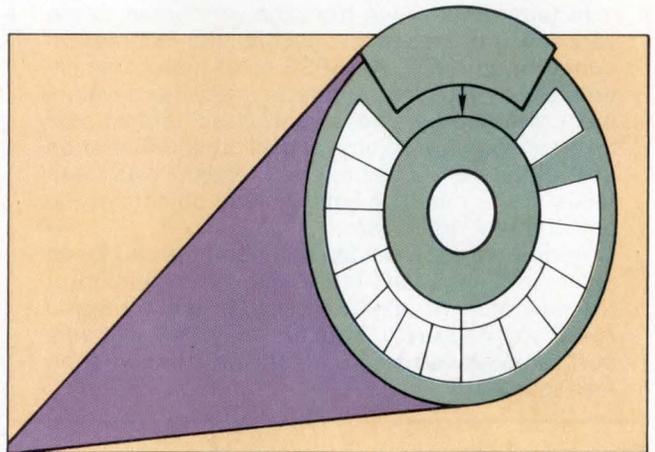
Designed to meet DOD requirements, the Ada Language System supports the entire Ada program life cycle while maximizing portability and allowing tailoring of the environment.

Ada, the standard programming language used by the Department of Defense, is a powerful, general-purpose high-level language. Adopted as a military standard in 1982, Ada directly supports such vital software engineering concepts as data abstraction, information hiding and modular design. Built-in language features promote software reliability, maintainability and reusability.

Ada can be augmented by using an Ada Programming Support Environment (APSE). Stoneman, a DOD specification for such environments, focuses on the challenges surrounding the management and control of large-scale software development projects. These issues include configuration management, version control and security.

Stoneman prescribes an architecture that maximizes portability of users, tools and projects. The standard also requires that environments be readily extensible. A Stoneman-compliant APSE allows tailoring and customization of the environment.

Softech's Ada Language System (ALS), a Stoneman-compliant APSE, is a software-development support environment for large-scale software systems written in the Ada language. A set of software tools supports Ada program generation, and an environment data base houses all programs, data and other information a site generates in using



the ALS. Built-in facilities also let the ALS be used in various hardware environments.

Currently comprising some 76 tools, the ALS provides basic support for the entire software life cycle. Text-editing and document-preparation tools assist in preparing specifications and manuals. Compilers, assemblers, linkers, debuggers and related tools support the coding and test phases. And an extensive set of configuration-control tools combine with the environment data base to organize the development and maintenance phases.

Developed for the U.S. Army by Softech, the ALS is currently hosted on Digital Equipment Corp's VAX/VMS. Rehost efforts are in progress for VAX/Unix and for the DIPS system from Nippon Telephone and Telegraph. Since its initial release in January 1985, the ALS has been installed at more than 200 sites, including university, government and commercial laboratories.

Abby Greenbaum, Evelyn M. Uzzle and David P. Wood

Greenbaum, Uzzle and Wood are senior engineers in the Ada technology department at Softech (Alexandria, VA).

Stoneman: a standard environment

To fully realize the benefits of the Ada language standard, a standard programming environment is also required. Ada represents significant progress in supporting reduced life-cycle costs. Ada alone, however, can't guarantee reliability, reusability or maintainability. The programming environment complements the language by providing the appropriate tools and facilities to support management and programmers in these goals.

Recognizing the importance of programming support environments, the Department of Defense conducted a program to determine the requirements for an Ada Programming Support Environment (APSE). The criteria established by the DOD reflect concern for supporting the entire software-development life cycle and for providing a common background for programmers as they move from one project to the next or even from one organization to another. The environment requirements eventually evolved into the DOD APSE-defining document called Stoneman.

In terms that range from the very broad to the very specific, Stoneman specifies the facilities required of an APSE. An APSE must include an extensible toolset that supports life-cycle development of Ada programs; a centralized, unified data base for software objects and all other information of a project's life cycle; and standard Ada interfaces to the primitive services and objects of the environment data base.

Additionally, Stoneman requirements call for an extensible command language; encapsulation of the environment operating system and a layered APSE architecture to support rehosting; and support for large software projects and configuration management.

Target vs. host

Applications programs developed using the ALS residing on a host computer often execute on separate target computers, which often are embedded within a larger operational environment such as an aircraft guidance system. A single ALS system can

support program generation for any number of distinct target machines.

This ability to generate software for multiple target processors within the same development environment promotes reuse of existing software. This reduces software-development and maintenance costs by eliminating duplicated efforts. The ALS environment data base tracks and organizes the reusable software.

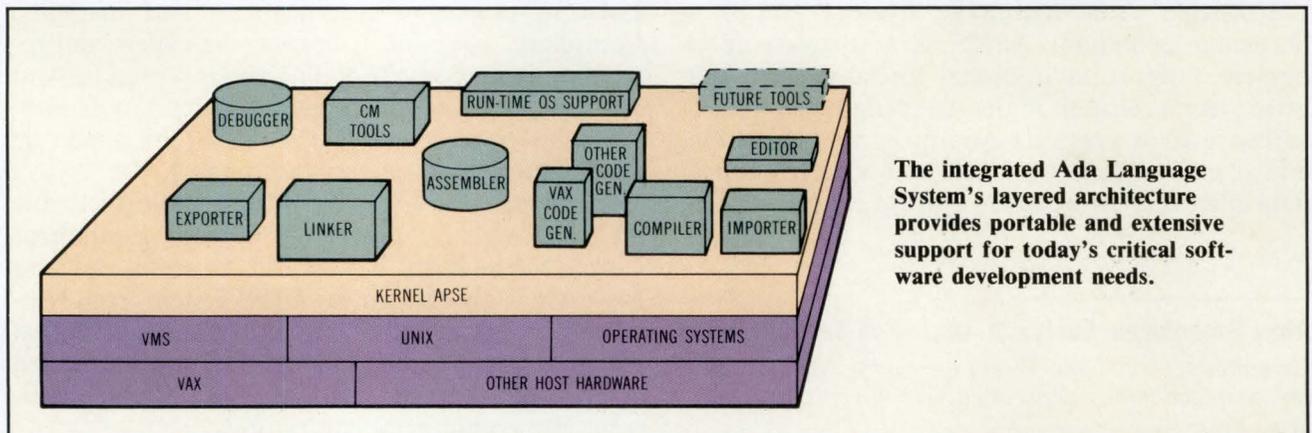
An organization might develop several different missile-control systems, for example. Using Ada, software developers can isolate and minimize software dependencies on specific target computer hardware. Using the ALS as a development environment, developers can easily share any of the target-independent missile-control software.

The relationships between shared and nonshared source-code modules are maintained and controlled in the ALS environment data base. Functions such as trajectory calculation or flight control can be implemented once and then reused in each of the separate systems.

A layered architecture

The ALS is designed to facilitate its own movement from one host system configuration to another. As required by Stoneman, the ALS has a layered architecture built on a host operating system or machine. The ALS surrounds the host system and provides a machine-independent program-development environment in which developers use the same tools and command language regardless of the actual host computer.

To its users, ALS hosted on a DEC VAX appears identical to ALS hosted on an IBM mainframe. This architectural approach is similar to that of the Unix operating system. The Kernel APSE (KAPSE) is a collection of services that provides a machine-independent interface between the ALS tools and the underlying host system. From the KAPSE, ALS



Multiple approaches to Ada support

An Ada environment can be designed in many ways. Each approach has both beneficial and detrimental characteristics. The different approaches can be summarized as piggyback, native portable, native nonportable, and specialized hardware base.

In the piggyback approach, the Ada Programming Support Environment (APSE) is built on top of the existing host operation system. Since the Kernel APSE (KAPSE) concept is supported as an agent for host portability, this approach can result in a Stoneman environment.

Because the piggyback approach provides the benefit of using the existing software base, users can realize lower development costs and shorter development time. Less beneficial aspects of this approach may include the additional performance overhead associated with a layered architecture. With proper tuning, however, this situation can be eliminated or reduced.

The native portable approach is one in which the APSE itself is the operating system. The KAPSE concept is still used, making the environment portable and hence potentially Stoneman-compliant. This approach could provide better performance than a piggyback effort but at the expense of a much longer development period and a much higher development cost. A piggyback environ-

ment could be made into a native portable environment simply by expanding the KAPSE. Attesting to the fairly high level of portability that can be achieved, Unix was developed using the native portable approach.

The native nonportable approach doesn't provide portability. An environment of this type may be either a non-KAPSE environment or a partial environment that's inserted into an existing operating system. The strategy is to insert Ada support tools into an existing environment. This method is relatively inexpensive, since none of the APSE architectural/portability goals must be met. In the case of a partial environment, much less software needs to be developed as well. Many computer manufacturers supply native nonportable operating systems. Although potentially comprehensive and easy to use, these operating systems are available only on the manufacturer's line of computers (for example, DEC VMS).

The specialized hardware base is a nonportable non-Stoneman approach that can provide a high-performance development vehicle, but at a very high cost. This approach is one in which the hardware is specially designed to suit the software, requiring ground-up design of all components of the system. The resulting system is incompatible with other systems.

software tools obtain services commonly required of a native operating system.

The KAPSE provides an insulation layer between tools and the host system. Rehosting the ALS onto a different host system requires only a reimplementing of the KAPSE. The KAPSE-tool interface is preserved while the KAPSE internals are reimplemented to interface with the new operating system. Tools are thus automatically portable from one ALS host environment to another.

Stoneman requires that an APSE be open-ended, or extensible. In an open-ended environment, any user can contribute to the toolset without needing specialized knowledge of the APSE architecture, and individual users or organizations can develop tools to support individual or site-specific needs and idiosyncrasies. For example, an organization might develop tools to check adherence to project coding standards, format progress reports or automate test submission.

In addition, the toolset can be upgraded to reflect developments in technology, protecting the environment against obsolescence. This open-endedness also eliminates functional and economic dependence on the vendor of the environment.

Adding support for a new target to the ALS represents a major upgrade to the ALS toolset. A com-

mon environment even facilitates this type of enhancement. The initial phases of the ALS Ada compiler and several other program-generation tools are common to all targets.

Promoting portability

One of the ALS design goals supporting Stoneman requirements is to promote portability for tools, users and projects. Each type of portability places distinct demands on the environment.

Tool portability refers to moving a tool from one ALS host environment to another. The ALS layered architecture and isolation of host dependencies within the KAPSE automatically make the tool set portable. Tool movement between ALS host systems increases the number of environments that can use a tool. This capability eliminates redundant tool development and saves the costs associated with new tool development.

User portability refers to whether programmers can move from one project or host environment to another. Because the ALS command language and KAPSE interface are constant across all ALS host environments, in a new host configuration the user sees an environment identical to the old environment in both function and user interface. This

(continued on page 94)

What do you ex

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Flexible environment...

(continued from page 91)

minimizes retraining when users move between projects or organizations.

Project portability refers to moving a complete project from one host to another. As software development progresses from implementation to maintenance, for example, responsibility for the software is often transferred from a development staff to a maintenance staff. When the data describing a project and its history are stored in an ALS data base, the data can be moved to a different ALS data base where they're still retrievable and intelligible to people other than the original authors.

Command language modeled after Ada

From the user's perspective, the ALS has three major components: the command language, the environment data base and the toolset. The ALS provides a powerful command language for tool invocation and control. The command language is intended for both interactive use from a terminal and for batch operation via command procedures. For consistency, the lexical format, syntax and control structures of the command language were modeled after Ada.

Command procedures can be written using Ada Loops and IF-THEN-ELSE statements. Using syntax similar to that of Ada procedure calls, including parameter passing, command procedures may invoke each other or invoke Ada programs. The command language differs from Ada in that it's string-oriented and not strongly typed. It's also smaller and simpler than Ada and is intended for interpretation rather than for compilation.

EDB serves as repository

The ALS environment data base (EDB) contains all information generated and maintained within the ALS. The EDB is a file system that serves as a repository for all the information relevant to a project. It can be used to store any type of text or binary information, such as source programs, object code, test cases, documentation, specifications, data files, management information, test sets and test results.

The EDB furnishes a standard communications medium for the ALS tools. Each object in the data base consists of information and characteristics that describe the object as well as its relationship to other objects in the data base. The structure of the data base is similar to the hierarchical, directory-

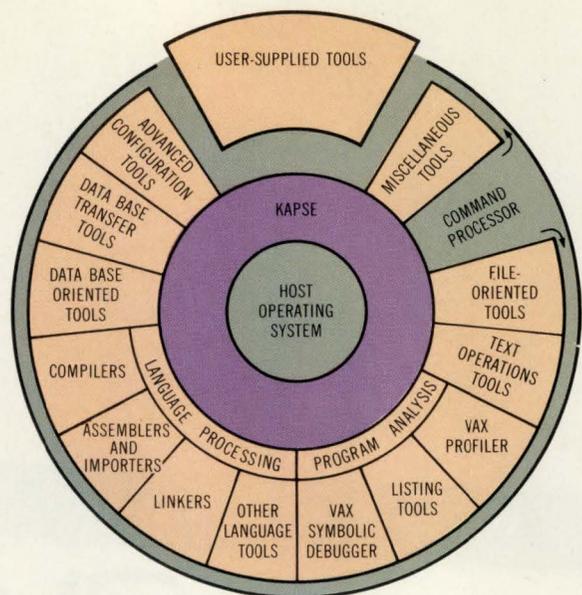
Tools can now be used outside the ALS environment

Although an all-encompassing environment such as the Ada Language System (ALS) provides the most flexible approach to software development, many applications areas may be better served with a more specific, less feature-packed environment. To meet this need while retaining the benefits of continued ALS enhancements, select program-generation tools may now be used outside the ALS environment.

The first such product to be released is called Ada-86, which features program-generation tools derived from their ALS counterparts. These new tools are targeted to 80286, 80186 and 8086 microprocessors. Program library-management tools are also provided.

Like their ALS cousins, the Ada-86 tools are hosted on VAX/VMS. Unlike their cousins, however, they use Digital Equipment Corp's command language and the VMS file system, and they operate directly under VMS in a manner similar to other VAX/VMS-hosted tools. When used in conjunction with commercially available products from DEC and Intel, Ada-86 provides users with a complete Ada software-development environment. In this environment, Ada-86 furnishes added benefits, such as faster execution speed. Ada-86 can be used, for example, to develop programs that will be used for high-performance embedded applications rather than to develop programs that will be run

under an operating system such as MS-DOS. But some benefits provided by Ada-86 require a corresponding sacrifice of some Stoneman features, such as rehostability.





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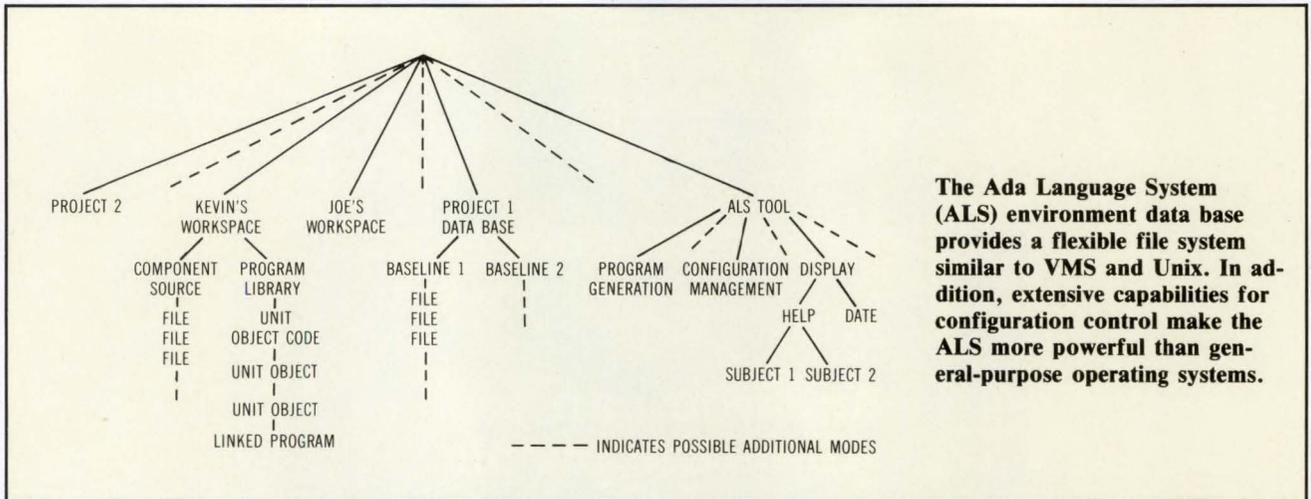
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The Ada Language System (ALS) environment data base provides a flexible file system similar to VMS and Unix. In addition, extensive capabilities for configuration control make the ALS more powerful than general-purpose operating systems.

oriented file structures of VMS, Unix and most other multiuser file systems. The primary difference is that the ALS EDB has built-in configuration management controls.

The conventions of the EDB contents and structure, coupled with the tools provided to operate on it, provide the ability to perform full life-cycle support for a project. The flexible file system structure partitions data to reflect the division of labor for a project or the organization of software.

The ALS tools support all roles within a project team, including managers and support staff as well as programmers. And they support all levels of cooperation within the team—from the individual to the subteam to the entire project team. Users can have their own private work spaces, work on different parts of the same program simultaneously or share information with one another. Access to particular information and tools can be selectively granted or restricted to specific users or groups of users.

Because of this flexibility, information can be organized and coordinated among members of a project. Multiple versions of software modules can be tracked, and files can be protected permanently from further modification and used to baseline or recreate previous baselines of a product.

Tool set operates on EDB

The ALS includes a comprehensive set of tools that operate on the environment data base and that support all phases of program development and maintenance. The tools can be categorized in terms of functionality, including program generation, data base management, configuration management, security and access control, file administration, text operations and display operations. Although the ALS provides a large number of services, users only

need to know a few of the tools to start program development, making the system easy for novice users to handle.

Program-generation tools help create Ada-executable programs for a specific target environment. The basic program-generation tools include an Ada compiler; an assembler to import externally assembled code; an exporter to produce a module that's executable on the particular target; and a linker. Additional program-generation tools include simulators or performance-analysis tools. **CD**

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

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Spot a real-time problem that's 100,000 instructions old.

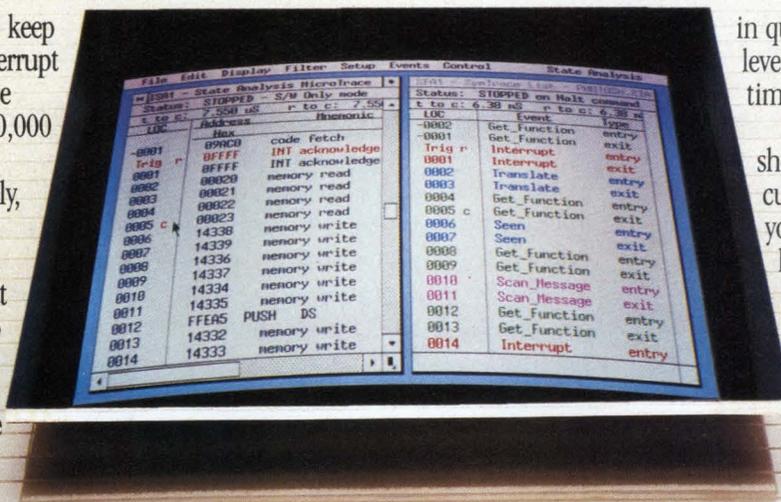
It happens all too often. You keep experiencing a real-time interrupt service problem whose source may have occurred up to 100,000 instructions ago.

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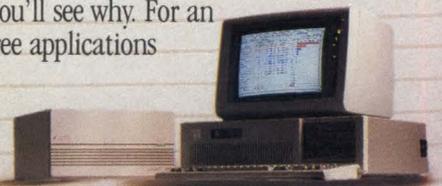
in question. Better yet, the high-level and assembly-level traces are time-aligned.

So Context Trace not only shows you how the problem occurs in real-time, but also lets you trace back through as much high-level execution as needed to find the origin of the problem.

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Plunging CAD/CAE prices drive multipen plotter advances

Though multipen plotters incorporate a 25-year-old technology, they remain the design engineer's most popular choice for color hard copy. The flexibility and ease of use of plotters, combined with a low price, makes them particularly well suited for schematic drawings in applications such as printed circuit board and IC design.

Pen plotter users have had to endure a number of problems, however. The primary problem is that pen plotters are relatively slow compared to plotters using newer technologies. Depending upon drawing size and density, a pen plotter might take hours to complete a large, highly dense drawing. In contrast, typical electrostatic devices plot an E-size drawing in a few minutes. (For media sizes, see key on page 101.) Pen plotters' maintenance re-

PRODUCT FOCUS

quirements and their lack of reliability have also been weaknesses. Pens must be constantly checked and maintained to prevent clogging or plot inconsistency.

Pen plotter manufacturers are eyeing these concerns and developing new products with improved speed and reliability. Extensive use of on-board intelligence and greater integration of VLSI technology has resulted in increased throughput. And improved motor designs and smaller, more compact products that use fewer parts have contributed to increased reliability.

Hewlett-Packard (Palo Alto, CA)

leads the pack in delivering products with increased speed and reliability. HP recently introduced the Draftmaster I and II plotters, which offer 50 percent higher throughput and 64 percent fewer parts than the company's older HP 7585 and HP 7586 models. HP has increased throughput by optimizing pen movements, thereby minimizing unnecessary pen movement. A smooth curve generator that's integrated with the plotters produces smoother curves with an uninterrupted, rather than a stepped, pen motion. A bidirectional plotting function speeds throughput by letting a plotter begin a plot at either end of a vector. Unlike the 4-MHz microprocessor used on previous models, these plotters have a 10-MHz 68000 microprocessor that processes vectors up to 250 percent faster.

One of a family of eight-pen plotters, the 1042GT from Calcomp (Anaheim, CA) offers two operating modes for use with either cut-sheet or continuous-roll media. It plots up to 60 A- to E-size drawings in a single batch run with Calcomp's Batchplot software utility. A proprietary plot-management algorithm in the company's Plot Manager firmware minimizes pen changes and movements. Pens are carried in a unique turret that reduces throughput delay by automatically changing pens over the plotting surface.

Another large-format plotter, the GP 9011 from Western Graphtec (Irvine, CA) uses a pinch-roller technique similar to the grit-drive approach. Serving A- to E-size plots, the 9011 uses an electronic sensor to automatically determine the media size and to adjust to it accordingly. A 20-character x 2-line LCD display lets users debug programs or control various manual functions. This four-pen unit operates with a variety of pen types, including liquid ink,

John H. Mayer
Associate Editor



Aimed at large design companies, the Draftmaster I and II plotters deliver high performance in a shared-resource environment. These eight-pen plotters offer a pen speed of 24 in./s and acceleration of up to 5.7 g.

Model	Type	Plot Speed (in./s)	Max. Paper Size (in.)	No. of Pens	Pen Types	Media Types	Repeatability (in.)	Addressable Resolution (in.)	Software Compatibility	Interfaces	Price (\$)
Alpha Merics 8031 Remmit Ave, Canoga Pk, CA 91304 (818) 999-5580										Circle 100	
Alphaplot II	flatbed	8	24×33	6	all	any	0.001	0.002	HP-GL	RS-232	5,900
SD3648	flatbed	24	36×48	6	all	any	0.001	0.002	HP-GL	RS-232	9,800
Customline	flatbed	24	49×97	6	all	any	0.001	0.002	HP-GL	RS-232	25,000
Bruning Computer Graphics 777 Arnold Dr, Martinez, CA 94553 (415) 372-7568										Circle 101	
Zeta 8	roll-feed	25	B	8	N, Lr, Bpt, Tr	B, V, M, Tf	0.001	0.004	HP-GL, GML, Plot 10, Calcomp 960	RS-232, IEEE-488	5,950
Zetadraf 900	—	45	37.5×49	8	N, R, Li	V, B, Tp, Pf	0.00049	0.005	HP-GL, GML, Plot 10, Calcomp 960	RS-232	7,950
Zeta 824	roll-feed	25	D	8	N, R	B, V, M, Tf	0.001	0.004	HP-GL, GML, Plot 10, Calcomp 960	RS-232, IEEE-488	8,900
Zeta 824CS	cut-sheet	25	D	8	N, R	B, V, M, Tf	0.001	0.004	HP-GL, GML, Plot 10, Calcomp 960	RS-232, IEEE-488	9,900
Zeta 836	roll-feed	25	E	8	N, Bpt, R, Li	V, B, Tr, Mpf	0.001	0.004	HP-GL, GML, Plot 10, Calcomp 960	RS-232	11,900
Zeta 836CS	cut-sheet	25	E	8	N, Bpt, R, Li	V, B, Tr, Mpf	0.001	0.004	HP-GL, GML, Plot 10, Calcomp 960	RS-232	12,900
Calcomp 2411 W La Palma Ave, Anaheim, CA 92803 (800) CAL-COMP										Circle 102	
1041GT	drum	24	D	8	Bpt, Fi, Pt, Li	Tr, B, V, G, F	0.0005	0.005	all popular CAD packages	RS-232, IEEE-488	6,495
1042GT	drum	24	D	8	Bpt, Fi, Pt, Li, T	Tr, B, V, G, F	0.0005	0.01	all popular CAD packages	RS-232, IEEE-488	9,900
1043GT	drum	24	E	8	Bpt, Fi, Pt, Li	Tr, B, V, G, F	0.0005	0.005	all popular CAD packages	RS-232, IEEE-488	8,905
1044GT	drum	24	E	8	Bpt, Fi, Pt, Li	Tr, B, V, G, F	0.0005	0.005	all popular CAD packages	RS-232, IEEE-488	13,900
Computer Talk PO Box 148, 2800 S Rooney Rd, Morrison, CO 80465 (303) 697-5485										Circle 103	
500	flatbed	20	42×60	4	Bpt, I, Fe	P, A, My	0.001	0.0005	HP-GL	RS-232	22,500
501	flatbed	20	52×60	4	Bpt, I, Fe	P, A, My	0.001	0.001	HP-GL	RS-232	30,800

Key: A = acetate; Bpt = ballpoint; B = bond; Cbrd = cardboard; Cer = ceramic; Ch = chisels; C = clay; Cr = creasing; D = drafting; Dp = double-matte polyester; Fe = felt tip; Fi = fiber tip; F = film; G = glossy; Hn = hard nib; I = ink; K = knives; Li = liquid ink; Lr = liquid roller; M = matte film; Mpf = matte polyester film; My = mylar; N = nylon; P = paper; Pen = pencil; Pl = plywood; Pf = polyester film; Pt = plastic tip; R = roller; Tf = transparent film; Tr = translucent; Tp = transparencies; Tt = tungsten tip; V = vellum; Wi = wet ink (pressurized)

Media Sizes (in.): A: 8¼ × 11; B: 11 × 17; C: 17 × 22; D: 22 × 34; E: 34 × 44

SYSTEM PRODUCTS/Peripherals

Model	Type	Plot Speed (in./s)	Max. Paper Size (in.)	No. of Pens	Pen Types	Media Types	Repeatability (in.)	Addressable Resolution (in.)	Software Compatibility	Interfaces	Price (\$)
Data Technology 4 Gill St, Woburn, MA 01801 (617) 935-8820											Circle 104
DT3454	flatbed	16	34×54	2 (4)	Pen, Bpt, Li, Fe	P, V, My	0.0025	0.0025	AutoCAD & other CAD programs	RS-232	27,390
DT4060	flatbed	16	40×60	2	Pen, Bpt, Li, Fe	P, V, My, Pl	0.0025	0.0025	AutoCAD & other CAD programs	RS-232	28,965
DT4364	flatbed	16	43×64	2	Pen, Bpt, Li, Fe	P, V, My, Pl	0.0025	0.0025	AutoCAD & other CAD programs	RS-232	33,895
DT5344	flatbed	12.8	53×44	3	Bpt, Li, K, Ch, Cr	V, My, Cbrd, Pl	0.00197	0.00197	AutoCAD & other CAD programs	RS-232	52,000
DT6444	flatbed	16	64×44	3	Bpt, Li, K, Ch, Cr	V, My, Cbrd, Pl	0.00246	0.00246	AutoCAD & other CAD programs	RS-232	58,000
Enter Computer 6867 Nancy Ridge Dr, San Diego, CA 92121 (619) 450-0601											Circle 105
SP600	paper-mover	14	B	6	Fi, Rb	B, V, Tp	0.001	0.008	HP-GL	RS-232, Centronics	995
Facit 9 Executive Park Dr, PO Box 334, Merrimack, NH 03054 (603) 424-8000											Circle 106
4550	pinch-roller	6	A	6	Bpt, Cer, F	P, G, Tp	0.001	0.008	HP-GL	RS-232, Centronics	795
4551	pinch-roller	8	B	6	Bpt, Cer, Fi	P, G, Tp	0.001	0.008	HP-GL	RS-232, Centronics	995
Gould-Recording System Div. 3631 Perkins Ave, Cleveland, OH 44114 (216) 361-3315											Circle 107
6120	pinch-wheel	8	B	7	Cer, Rb, Fi	B, Tp	0.002	0.008	HP-GL	RS-232, Centronics	995
6310	flatbed	16	A	7	Fi, Rb, Li	B, Tp, V, My	0.001	0.002	HP-GL	RS-232, IEEE-488	1,695
6320	flatbed	16	B	10	Fi, Rb, Li	B, Tp, V, My	0.001	0.002	HP-GL	RS-232, IEEE-488	1,895
GTCO 7125 Riverwood Dr, Columbia, MD 21046 (301) 381-6688											Circle 108
Autoplot	flatbed	10	D	1 (8)	—	all	0.001	—	HP-IB-compatible	RS-232	4,495
Hewlett-Packard 16399 W Bernardo Dr, San Diego, CA 92127 (619) 487-4100											Circle 109
Colorpro (7440A)	—	15.7	A	8	P, F	P, F	0.001	0.004	business graphics packages	RS-232 or HP-IB	1,295
7475A	small-format	15	B	6	P, F, Li	P, F, Dp	0.001	0.004	business & CAD packages	RS-232, HP-IB	1,895
7550A	small-format	31.5	B	8	P, F, Li, Rb	P, F, Dp, V	0.001	0.004	business & CAD packages	RS-232, HP-IB	3,900

Model	Type	Plot Speed (in./s)	Max. Paper Size (in.)	No. of Pens	Pen Types	Media Types	Repeatability (in.)	Addressable Resolution (in.)	Software Compatibility	Interfaces	Price (\$)
Hewlett-Packard 16399 W Bernardo Dr, San Diego, CA 92127 (619) 487-4100											Circle 109
Draftpro (7570)	—	15	D	8	Li, Fi	P, V, Pf	0.001	—	AutoCAD, VersaCAD, Anvil-1000, & others	RS-232, HP-IB (opt)	5,400
Draftmaster I	single-sheet	24	E	8	D, Fi, Rb	V, B, Pf, Tp, B	0.001	—	emulation mode	RS-232, RS-422, HP-IB	9,900
Draftmaster II	roll-feed	24	E	8	D, Fi, Rb	V, B, Pf, Tp	0.001	—	emulation mode	RS-232	11,900
Houston Instrument-Div. of Ametek 8500 Cameron Rd, Austin, TX 78753 (512) 835-0900											Circle 110
DMP-51/52 MP	grit-wheel	16	D	14	D, Hn, Tt	P, V, M	0.005	0.002	CAD & business graphics	RS-232	5,295
DMP-56A	grit-wheel	16	E	1 (6)	D, Tt, Hn	P, V, M	0.005	0.004	CAD & business graphics	RS-232	5,995
IBM Plotter Dept (789), PO Box 3332, Danbury, CT 06813 (800) IBM-PLOT											Circle 111
6180	tabletop	16	A	8	Fi	P, F	0.001	0.004	HP-GL command software	RS-232, IEEE-488	1,285
7372	tabletop	15	B	6	Fi	P, F	0.00098	0.004	HP-GL command software	RS-232, IEEE-488	1,900
6186-2	floor-standing	24	—	8	Fi, Rb, D	P, V, F	0.00098	0.004	HP-GL-compatible	RS-232, RS-422A, IEEE-488	11,900
6184	floor-standing	16.5	D	8	Fi, D	P, V, F	0.001	0.004	HP-GL-compatible	RS-232, IEEE-488	5,400
6186-1	floor-standing	24	E	8	Fi, Rb, D	P, V, F	0.00098	0.004	HP-GL-compatible	RS-232, RS-422A, IEEE-488	9,900
Ioline 19417 36th St W, Suite D1, Lynnwood, WA 98036 (206) 775-7861											Circle 112
LP3700	media-moving	10	37.5×81	20	Li, Rb, Fi	My, V, B, C, F	0.001	0.0025	DMPL	RS-232	4,195
LP4000	media-moving	20	37.5×81	20	Li, Rb, Fi	My, V, B, C, F	0.001	0.001	DMPL	RS-232	5,495
Kongsberg 1325 S Dairy Ashford, Ste 480, Houston, TX 77077 (713) 870-1519											Circle 113
DM1216	flatbed	27	47×63	4	Bpt, Wi	all	0.00005	0.0006	all CAD systems	RS-232	127k
GT5000	flatbed	40	47×63	4	Bpt, Wi	all	0.00005	0.0006	all CAD systems	RS-232	158k
DM1825	flatbed	27	47×63	4	Bpt, Wi	all	0.00005	0.0002	all CAD systems	RS-232	177k
Numonics 101 Commerce Dr, Montgomeryville, PA 18936 (215) 362-2766											Circle 114
5860	—	8	D	8	Fi, Bpt, Cer	P, V, My, B	0.0098	—	AutoCAD, CAD master.	RS-232	4,495

SYSTEM PRODUCTS/Peripherals

Model	Type	Plot Speed (in./s)	Max. Paper Size (in.)	No. of Pens	Pen Types	Media Types	Repeatability (in.)	Addressable Resolution (in.)	Software Compatibility	Interfaces	Price (\$)
Roland DG 7200 Dominion Cir, Los Angeles, CA 90040 (213) 685-5141 Circle 115											
DPX-3300	flatbed	16	D	8	—	—	0.0005	—	HP-GL	RS-232, Centronics	—
United Innovations Crossroads Industrial Pk, Holyoke, MA 01040 (413) 534-4400 Circle 116											
Mural	flatbed	7	27×36	1	all	to 5/16-in. thick	0.001	0.0035	HP-GL	RS-232	2,495
Western Graphtec 12 Chrysler St, Irvine, CA 92718 (714) 770-6010 Circle 117											
MP2000	flatbed	10	B	8	Fi, Bpt, Cer, I	all	0.0004	0.004	—	RS-232, Centronics, IEEE-488	1,195
MP2300	flatbed	10	B	8	Fi, Bpt, Cer, I	all	0.0004	0.004	—	RS-232, Centronics, IEEE-488	1,395
FP5301	flatbed	18	B	10	Fi, Bpt, Cer, I	all	0.004	0.004	—	RS-232, Centronics, IEEE-488	3,290
PD9311/F	pinch-roller	18	B	4	Fi, Cer, Bpt, I	all	0.004/0.002	0.008	AutoCAD, VersaCAD, CADplan & others	Centronics, IEEE-488, RS-232	3,295
PD9111	pinch-roller	18	D	4	Fi, Cer, Bpt, I	all but tissue	0.004/0.002/0.001	0.004	AutoCAD, VersaCAD, CADplan	Centronics, IEEE-488, RS-232	5,995
PD9011	pinch-roller	18	E	4	Fi, Cer, Bpt, I	all but tissue	0.004/0.002/0.001	0.004	AutoCAD, VersaCAD, CADplan	Centronics, IEEE-488, RS-232	8,950
Xynetics Products 2962 Stender Way, Santa Clara, CA 95954 (408) 980-4149 Circle 118											
1201A	flatbed	40	64×96	4	Wi, Bpt	V, F, B	0.001	0.001	—	—	—
1051A	flatbed	40	36×48	4	Wi, Bpt	V, F, B	0.001	0.001	—	—	—
1101A	flatbed	40	48×64	4	Wi, Bpt	V, F, B	0.001	0.001	—	—	—

water and oil-based fiber tips, ball-points and ceramic pens. Like most plotters in its class, the 9011 is compatible with most popular CAD software packages.

As the price of microcomputer-based CAD/CAE workstations has dropped, plotter manufacturers have tried to keep pace by packing the features of a full-scale large-format plotter into a lower cost package. The LP4000 from Ioline (Bellevue, WA) is a 20-in./s, 0.001-in. resolution plotter that plots on media sizes up to 37.5×81 in. It handles either cut-sheet or roll stock. Ioline keeps prices in the \$5,000 range by

offering options, such as its multi-pen changer. With four-pen modules, this option expands the plotter's pen capability to 20 pens. A second option, called the hyperbuffer, adds a CPU and a 512-kbyte buffer to reduce plot time and increase throughput.

At the low-performance end of the spectrum, manufacturers are offering increasingly low-cost, desktop units to complement a similarly low-cost PC-based CAD or graphics system. Products such as HP's Colopro, IBM's 6180, or Western Graphtec's MP-2300 are priced at under \$1,500.

Some models, such as the 6120 from Gould (Cleveland, OH), the 4550 and 4551 from Facit (Merrimack, NH), and the SP600 from Enter Computer (San Diego, CA) dip below \$1,000. Like many low-cost personal models, the SP600 operates from any MS-DOS- or CP/M-compatible microcomputer. The desktop rollerbed unit is restricted to A- and B-size plots, but runs at 14 in./s with 0.001-in. addressable resolution. The plotter has both serial and parallel interfaces, and it senses which interface is being used and then switches between them automatically. Prices begin at \$995. **CD**

TEXAS INSTRUMENTS REPORTS ON

GRAPHICS

IN THE ERA OF

MegaChip[□]

TECHNOLOGIES



Graphics in the Era of MegaChip Technologies:

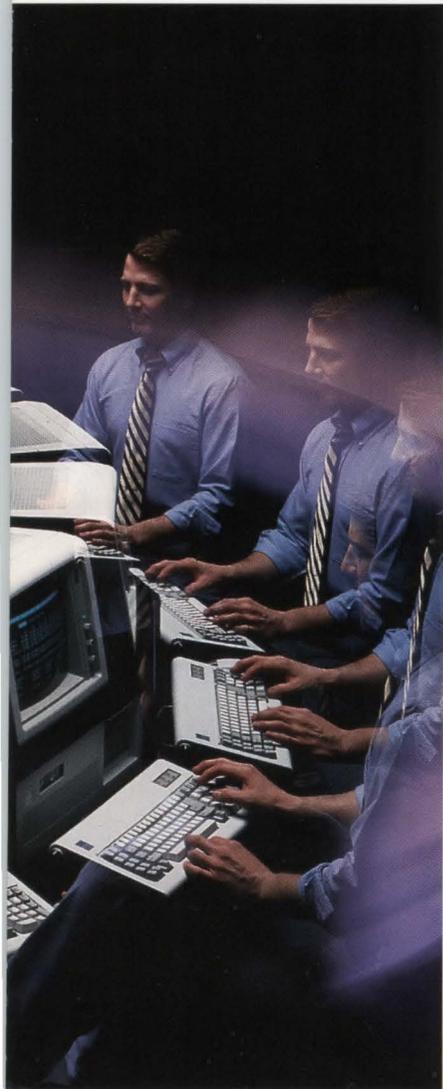
New Texas Instruments lets you program circles plus filled polygons, spline curves, antialiased lines,



From PC displays to laser printers, the flexibility of TI's TMS34010 processor delivers the leading-edge performance you need today and to stay out in front tomorrow.

In TI's TMS34010 Graphics System Processor, you have a new and better graphics-design approach: The first high-performance, 32-bit CMOS microprocessor optimized for graphics applications. The 34010 can execute all function needed by graphics operating environments; hard-wired coprocessors can only execute a small part.

32-bit graphics processor around competition... text, and more.



But there's an even more important aspect to consider. The 34010 will help keep your system ahead of competition because it is compatible with existing graphics hardware standards — CGA,[™] EGA,[™] and PGC[™] — and supports graphics software standards such as CGI, DGIS,[™] and MS-Windows.[™]

Standards like Windows and DGIS run faster on TI's TMS34010

The 34010 is also among the fastest microprocessors available. It handles six million instructions per second with a "draw" rate of up to an amazing 50 million pixels per second. Thus, it can boost total system performance.

Because of the support of MS-Windows and DGIS alone, many major applications software packages can already run on 34010-based systems.

TI's MegaChip Technologies

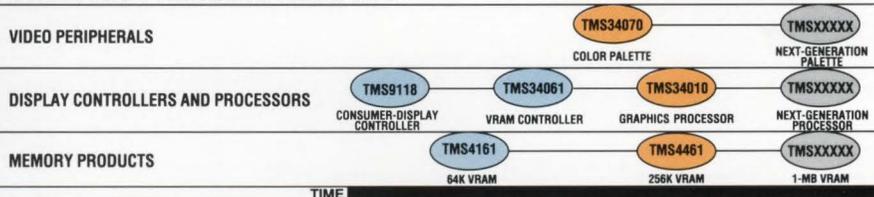
Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip[™] Technologies, and they are the means by which we can help you and your company get to market faster with better products.

workstations, terminals, plotters, FAX, image processing, digital copiers, mass storage, robot vision, and communications.

TI's total systems solution

In implementing your design, you'll want to consider other building blocks TI has developed. Included are the single-chip TMS34070 66-MHz Color Palette that supports simultaneous display of 16 out of 4,096 colors and the

GRAPHICS-PRODUCTS ROAD MAP



Road map to tomorrow's graphics systems: Next-generation additions to TI's innovative graphics-products family will allow you to build on your present designs to develop even higher-performance systems.

"You would think TI designed the 34010 with our technology in mind."

Luis Villalobos, Conographic president, refers to the power of the 34010 to process font outlines for desk-top publishing. Resolution up to 64K × 64K means no hardware limits for laser printers and other hard-copy devices.

Host independence and the flexibility of a device programmable in "C" language make TI's 34010 the cost/performance leader for PC displays, laser printers, desk-top publishing,

TMS70C42 Microcontroller that handles all serial interface duties.

Also included are high-speed video random-access memories (TMS4161 and TMS4461), plus linear small and large-area CCD image sensors.

To provide the host bus interface and any other customized functions you may require, TI offers quick design and production turnaround through its Application-Specific Integrated Circuits (ASICs) capabilities.

Development tools are available now for applying the 34010. Turn the page for details. ►



"Because the 34010 is programmable, it is in a league all its own."

Jim Richards, president of VMI, is talking graphics performance. You can program the 34010 processor to perform any graphics function you want, unlike hard-wired coprocessors. This means you can readily customize your system to outperform your competition.

"Texas Instruments had ready the full set of development tools we needed."

As William Frentz, executive vice president at Number Nine Computer, points out, TI has ready the hardware, software, and documentation you will need to make designing in the 34010 as fast and as easy as possible.

TI's 34010 software includes a full Kernighan and Ritchie "C" compiler with extensions and an assembler package for both MS-DOS™ and VAX™ operating environments.

A graphics/math library provides source code for more than 100 functions, whereas a typical controller chip offers only 15 to 20. A special font library contains more than 100 type fonts to expedite development of desktop publishing applications.

The TMS34010 XDS/22 Emulator is a flexible, realtime, in-circuit emulator. It can be used in a stand-alone mode through a standard terminal or through a host computer with a powerful debugger interface.

To see immediately what TI's new graphics processor can do for you, just plug the TMS34010 Software Development Board into an IBM® PC-compatible or TI Professional computer. The board is populated with TI's 34010 Graphics Processor, Color Palette, and VRAMs. It provides an ideal environment for developing your own high-performance graphics applications.

For more information on TI's total graphics-system solutions, including details on TI's Graphics Design Kit and design training courses, complete and return the coupon today. Or write Texas Instruments Incorporated, P.O. Box 809066, Dallas, Texas 75380-9066.

FOR FREE ON-LINE INFORMATION, dial 1-800-345-7335 with any 80-column ASCII terminal or PC and a 300 or 1200 baud modem (EVEN or IGNORE parity, 7 data bits, 1 stop bit). At "Enter Response Code," type TIGRAF. In Conn. dial (203) 852-9201.

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26-4537

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To speed the design of your graphics system, TI's range of development tools includes a comprehensive design kit (left rear), a realtime emulator, and a plug-in software development board. On floppy and magnetic disks: "C" compiler, assembler package, and function and font libraries. User's guides, development books, product bulletins and data sheets, and TI's newsletter, *Pixel Perspectives*, are all readily available.

Hundreds of designers must be right.

Hundreds of hardware and software designers are making TI's 34010 the new graphics standard. Among them are leading board-development houses and major software vendors.

In fact, the wide range of graphics standards and application software already written for TI's 34010 makes it the easiest-to-use new graphics chip ever introduced. Here's just a sampling of the software that will run on top of Graphic Software Systems DGIS* 34010:

Software Products	Company
AutoCad™	AutoDesk
GSS*CGI™†	GSS
Master Series™	Ashton-Tate
Freelance Plus™	Lotus GPG
Graphics Development Toolkit™†	IBM
Harvard Presentation Graphics™	Software Publishing Corp.
ProDesign II™	American Small Business Computers
VersaCad™	VersaCad Corp.
Windows™†	Microsoft
Symphony™, 1-2-3™	Lotus Development
PCAD™	Personal CAD Systems

†Trademarks are as noted.

†More than 100 graphics applications are currently available for these operating environments.

Texas Instruments Incorporated

SPV153OS700C

P.O. Box 809066
Dallas, Texas 75380-9066

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**TEXAS
INSTRUMENTS**

Emulation finds role in prototype board test

A new test and troubleshooting tool for microprocessor-based boards can also be used by designers for prototype verification. The 9100 series family of emulative board testers provides hardware designers with the type of support that microprocessor development systems lend to software designers.

Like an in-circuit emulator, an emulative board tester plugs directly into the microprocessor socket, letting the operator control the unit under test. As a tool for hardware designers, the emulative board tester doesn't provide software tools such as compilers and debuggers. Nor does it allow real-time emulation. The 9100 series lets engineers stimulate the board from the microprocessor socket and emulate microprocessor functions from the microprocessor interface pod. In addition, support is available for more than 50 microprocessors, including the 80286 from Intel.

In addition to containing its own microprocessor, each pod has its own RAM, ROM and I/O, making each a complete kernel. The board's bus becomes an extension of the pod's bus, letting the pod control all bus-related devices on the board. Plugging in the pod also causes the clock circuit of the board under test to channel to the pod's microprocessor, so tests can run with the board operating at its normal speed.

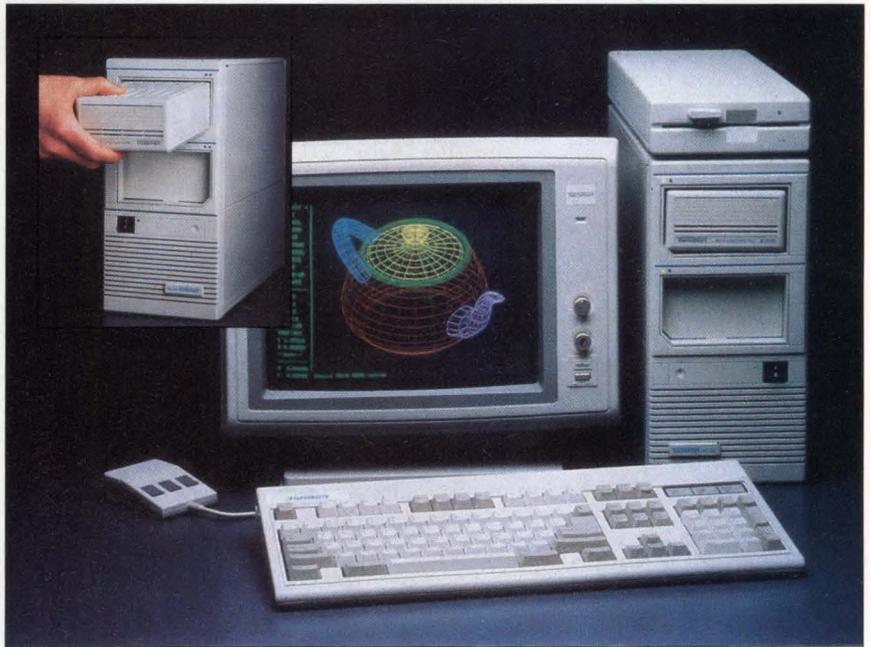
The 9100 series provides built-in bus, RAM and ROM test routines. With one keystroke, the tester can read all ROM locations or access all RAM within a given address range. Users can also write test programs at the keyboard and store them for later use. Test programs written for prototype test can be passed on to production test and field service departments.

For fault analysis and troubleshooting, the 9100 series offers a technique called signature analysis, in which the electrical "signature" of a node on the board under test is compared with that of the same node on a board that's known to be good.

Response factors such as logic levels, event counts and frequencies can also be compared. Reference data are gathered from known-good boards through an interactive process in which the user types in nodes, runs a test and stores the response factors that are most appropriate for each node.

tests, and the 9105A, which is an execute-only tester. The 9100A has 2 Mbytes of memory, a 20-Mbyte hard disk and a 3½-in. floppy. The 9015A includes an 800-kbyte floppy for executing test programs.

For \$21,500, the 9100A includes a mainframe, a programmer's station, an I/O module and a single-point



A new type of circuit interface device, the I/O module, lets users test up to 40 nodes at once at signals up to 10 MHz. Up to four I/O modules can be used to test 160 pins simultaneously. An I/O module can drive a node high or low, stimulate a node, take signatures, sense logic levels and count events or frequencies. These modules work with both synchronous and asynchronous circuitry. A single-point probe is available for signals up to 40 MHz.

The 9100 series provides three levels of automation. Guided fault isolation completely automates the troubleshooting process; unguided fault isolation lets the user identify specific nodes; and the immediate mode is used for manual operation.

Two models are available: the 9100A, which is used for both developing test software and running

probe. The \$9,000 9015A comes with a mainframe, a single-point probe and an asynchronous clock module.

John Fluke Mfg, PO Box C9090, Everett, WA 98206. **Circle 119**

—R.G.

COMPUTER DESIGN reprints

Reprints of any article or advertisement appearing in *Computer Design* may be ordered directly from June Bozarth, CSR Reprints, PennWell Publishing Co., P.O. Box 1260 Tulsa, Oklahoma 74101, 1-800-331-4463 or 918-835-3161 Ext. 379. Minimum order: 100 black and white copies, 500 four-color copies.

Self-contained 30-Mbyte hard disk is portable

In keeping with the premise that innovations in peripherals drive the personal computer industry, Tandon has introduced the concept of portable hard disks as the basis for truly personalizing personal computers. The 30-Mbyte, 2.5-lb Data Pac fits into a receiving slot of a subsystem called Ad-Pac 2 or into a Data Rac slot as part of the company's IBM PC AT-compatible Pac 286 computer. It combines the benefits of a fixed hard disk with the portability of a floppy disk.

While removable hard disks are not new, most have been built to secure data rather than transport it. In contrast, the Data Pac is an enclosed Winchester disk that's shock-mounted and whose drive is more resilient than most cameras. Able to withstand up to 250 g of force, the Data Pac can be dropped from up to 18 in. onto a concrete floor without being damaged. The Pac's airtight enclosure ensures freedom from dust, smoke and other contaminants for the self-contained Winchester disk. The disk consists of four drive heads and two platters.

The Pac is designed so that the drive itself is suspended within a hard plastic case by four individual shock mounts. The mountings are calibrated to three different shock-absorption rates to compensate for the drive's displaced center of gravity. This support gives the drive a safety margin of 7.6 mm from all six walls of the case, while providing sufficient dampening to minimize excess vibration during normal use. A proprietary head-locking mechanism that prevents the heads from ever touching the medium also ensures that a large jolt during transport won't move the heads from a safe area to a sector where data is stored—a common occurrence in today's hard disk drives.

The Personal Data Pac is inserted into a receiving slot through an auto-insertion mechanism in the same way a tape cassette is inserted into a video cassette recorder. When activated, this mechanism draws in the Pac until a proprietary 36-pin connector engages with the data bus. The Pac is removed via software control by the user or the applications program.

Applications programmers access data on the Pac using standard AT functions. In addition, the disk supplies two reserved areas: one for manufacturing and audit information and the other for a vendor-installed serial number, which can be used to control and track the recipients of copies of an application. This feature and the Pac's compact size and ruggedness is prompting the company to promote the Pac as a useful vehicle for better software distribution. True turnkey applications can be shipped in a Pac and run directly from the box. Or, application-specific Pacs could be made available through software dispensers at computer retailers.

Currently available in 30-Mbyte versions, future Pacs will have capacities in excess of 100 Mbytes. A 128-kbyte cache buffer transfers all data from one Pac to another in less than 3 min. The Pac is formatted with 26 sectors of 512 bytes each. Access time is 40 ms, while the transfer rate is 7.5 Mbits/s. The Pac is priced at \$350. The Ad-Pac 2, a subsystem that can handle two Pacs and that can be attached to any AT-compatible computer, is available for \$500. A Pac 286, configured with a floppy drive and one Data Pac, sells for less than \$3,000.

Tandon, 405 Science Dr, Moorpark, CA 93021. **Circle 120**

—N.M.



Coming May 15
Look for Howard Falk's
technology focus report
on in-circuit emulation.

3-D terminal series supports hierarchical display lists

A new series of high-end graphics terminals addresses mechanical CAE/mechanical CAD, military training and simulation, electrical engineering and general scientific applications. The 9000 family from Megatek boasts screen resolutions of $1,280 \times 1,024$ pixels. Both new terminals offer software emulation of Tektronix 40xx and 41xx as well as DEC VT-100 products. The terminals connect to host systems via Ethernet, direct memory access or RS-232 interfaces.

The series consists of two terminals. The 9100 is optimized for three-dimensional wireframe display and can process 200,000 transformed vectors/s and display 16 or 256 colors from a palette of either 4,096 or 16.7 million colors. It performs 3-D clipping, rotation and transformation as well as perspective and depth cueing on the stored display list. Both terminals support a display-list memory of 1 to 8 Mbytes. Double-frame buffers for animation and cine-loop displays and for dynamic display updating without visible redraw are standard features.

The 9300 is optimized for solids modeling and can process 20,000 fully shaded polygons/s and display



4,096 colors from a palette of 16.7 million. Shaded solids are rendered as flat or shaded surfaces using Phong or Gouraud shading algorithms. In addition, the 9300 supports rational cubic B-splines, which render curves according to their true mathematical definition, rather than as a series of vectors, and curved surfaces as true curves rather than a mosaic of polygons.

The display-list hardware is for use with hierarchical display lists, such as those that are used by the Programmers Hierarchical Interac-

tive Graphics Standard. A transform and traversal processor speeds the processing of tree-like display-list structures. Both terminals also use custom VLSI for transformation and vector processing. They have hardware support for 32-bit floating-point precision to support the interactive manipulation of complex 3-D objects.

Prices start at \$24,000 for the 9100 and at \$30,000 for the 9300. **Megatek**, 9645 Scranton Rd, San Diego, CA 92121.

Circle 121
—T.R.W.

EGA-compatible board adds high-resolution mode

Building on the custom ET2000 VLSI Graphics Engine, the Enhanced Video Adapter (EVA)/480 is a graphics board that's compatible with the IBM Enhanced Graphics Adapter (EGA). The EVA/480 features a high-resolution 640×480 -pixel mode. To take advantage of the high-resolution mode, users need an NEC Multisync monitor or the equivalent.

EVA/480 offers all of its predecessor's features, including 640×350 -pixel resolution, 16 colors from a 64-color palette and all standard EGA capabilities, such as smooth scrolling, pixel panning and split

screen. Additional features include hardware zoom, viewport/zoom window and a potential 300 percent speed improvement via a microsequencer. The board has 256 kbytes of memory and a parallel port.

Full software support for the 640×480 -pixel version is standard. Screen drivers are provided for running Windows from Microsoft (Redmond, WA), 1-2-3 from Lotus (Cambridge, MA) and Dr. Halo from Media Cybernetics (Silver Spring, MD). In addition, Media Cybernetics will distribute a free copy of the most advanced version of the Dr. Halo paint program with

complete support for the board's viewport and zoom features. The board supports many PC-based CAD programs. Also available is an optional driver, for example, which runs AutoCAD in the 640×480 -pixel mode. The board is downwardly compatible with the IBM Color Graphics Adapter, the IBM Monochrome Display Adapter and the Hercules Graphics Card.

The price of the board is \$680.

Tseng Laboratories, Newtown Industrial Commons, 10 Pheasant Run, Newtown, PA 18940.

Circle 122
—J.H.M.

Why this magazine and more than 900 others let us go over their books once a year.

Some magazines, we're sorry to say, keep their readers undercover. They steadfastly refuse to let BPA (Business Publications Audit of Circulation, Inc.) or any other independent, not-for-profit organization audit their circulation records.

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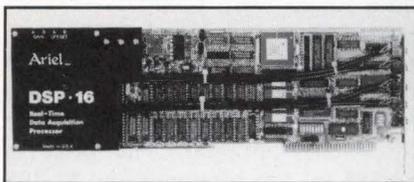
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Digital audio signal processor fits into one IBM PC slot

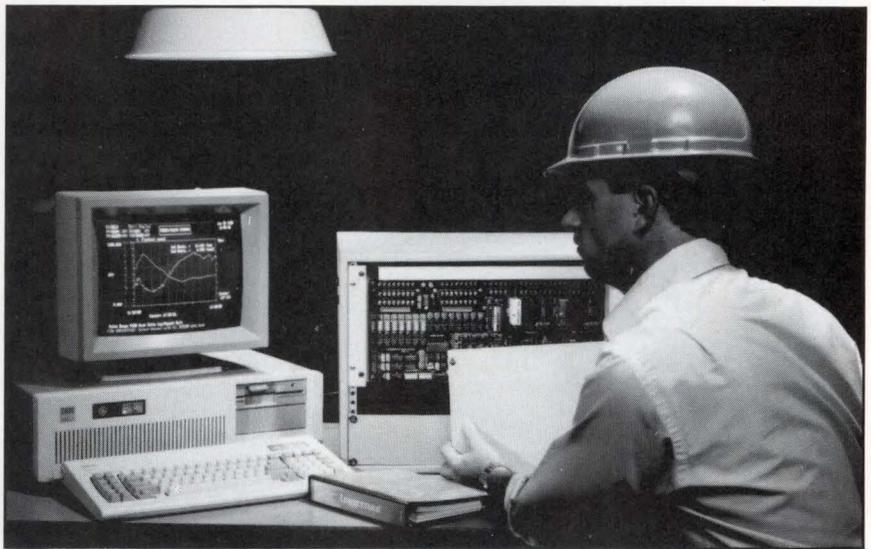
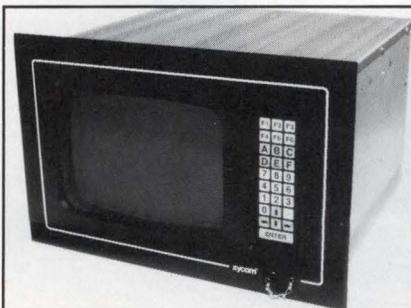
The DSP-16 data acquisition processor features two channels of I/O conversion, a large data buffer and the TMS32020 digital signal processor. The processor delivers a throughput of 5 Mips. Processor programs are uploaded from the host to 16 kwords of zero-wait-state RAM. A separate processor-to-host interface permits program modification and data transfer. The unit buf-



fers up to 256 ksamples of data (expandable to 1 Msample). It includes input buffering, antialiasing and output filters, and I/O sample/hold. A program development system and five applications programs are provided with the board. Price is \$2,495. **Ariel**, 110 Greene St, New York, NY 10012. **Circle 123**

Industrial computer based on 68000 module

The 4860-VME industrial computer has a 12-in. amber monochrome terminal, a sealed membrane keypad, a five-slot double-high VME chassis and a 120-W power supply. The 68000-based processor module has a firmware debug monitor and 32 kbytes of static RAM and supplies all VMEbus system utility functions. The computer's terminal emulates DEC VT100 and VT220 and Hazel-



Data logger targets factory environments

The Loggernaut adds a trend recorder, a data logger, alarm monitoring and automatic data collection/reduction capabilities to IBM PCs and compatibles. For use in factory or laboratory environments, the board features 500-V isolation, 14-bit analog-to-digital resolution and direct connection to sensor inputs. The Log-

gernaut offers user-defined scans of up to 64 analog input signals in addition to digital inputs and outputs. Scans can be performed at user-defined intervals or on event-driven interrupts with data automatically logged to disk. **Cyborg**, 55 Chapel St, Newton, MA 02158.

Circle 125

tine 1500 terminals. Mounted in a panel or rack, the 4860-VME features self-diagnostics, an ASCII character set and graphics control. The price is \$3,750. **Xycom**, 750 N Maple Rd, Saline, MI 48176.

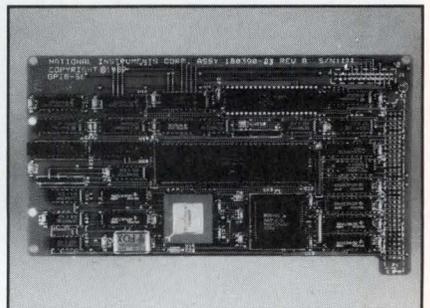
Circle 124

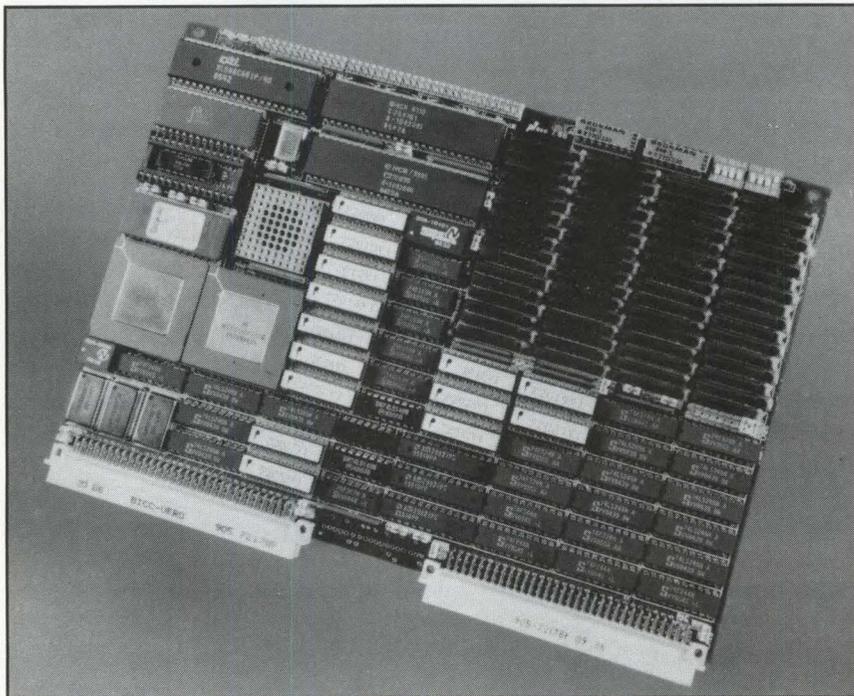
IEEE-488 interface card serves Macintosh SE

The GPIB-SE is an IEEE-488 interface card for the Apple Macintosh SE 68000 processor. The board and software let the Macintosh SE act as a data-acquisition and instrumentation-control platform for laboratory, production and general-purpose test and measurement applications. Features include IEEE-488 bus transceivers, a controller chip, and a custom gate array, which improves performance. An 8-MHz

68440 direct memory access controller with a 500-kbyte/s data transfer rate and a 12-MHz 68881 math coprocessor is optional. The card supports Labview, a graphics programming environment for data acquisition, instrument control, data display, data analysis, data management and report generation. The base price for the card is \$495. **National Instruments**, 12109 Technology Blvd, Austin, TX 78727.

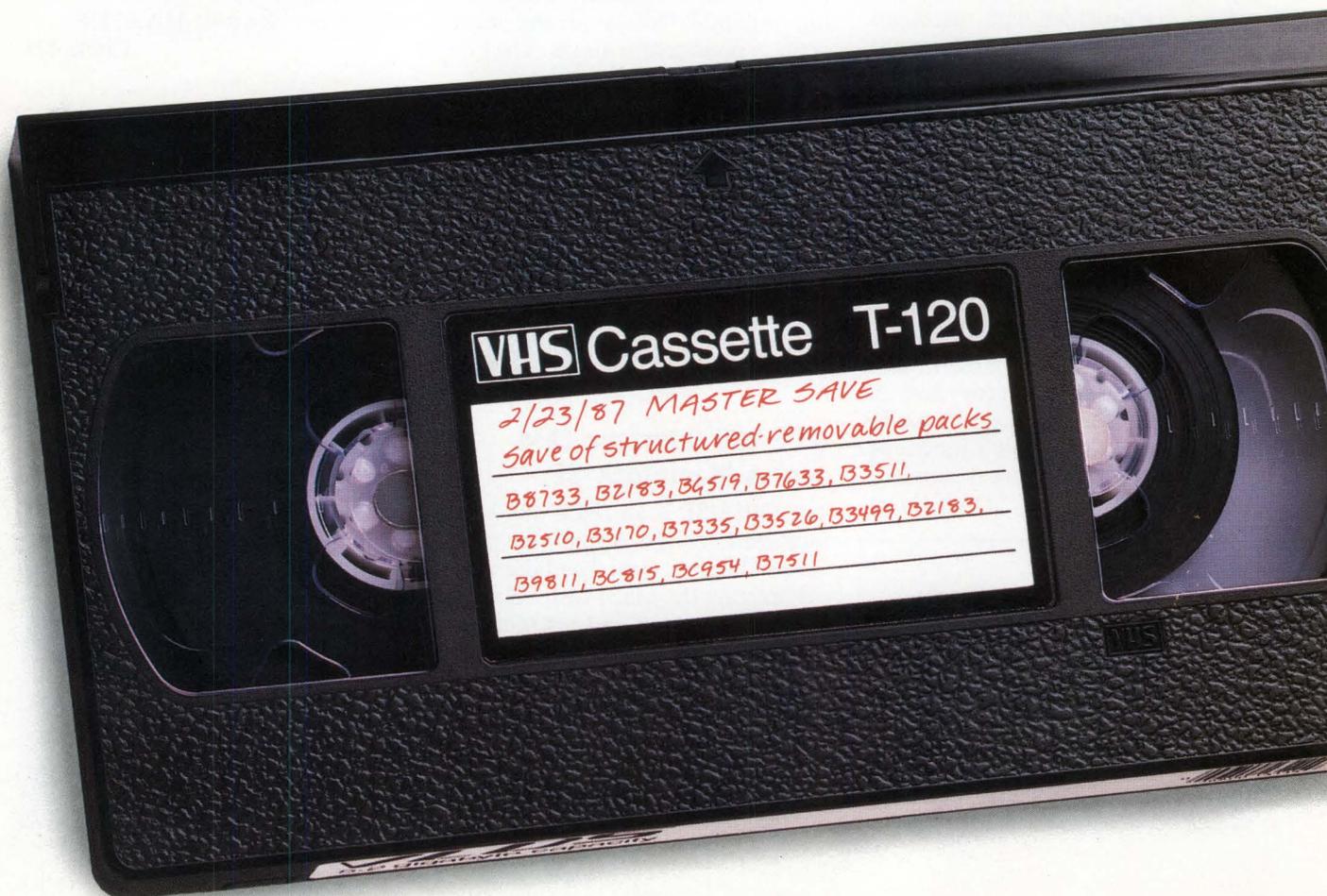
Circle 126





Single-board computer runs Unix System V.2

The TP20-V single-board VMEbus computer runs Unix System V.2. The board provides a 68020 processor, a 68851 paged memory-management unit, a 68881 coprocessor, 2 or 8 Mbytes of dynamic RAM, two serial ports, a small computer systems interface and a VME system controller interface. It operates at 12 or 16 MHz with one wait state. The TP20-V is the first CPU board to run Unix on a single VME board. The computer also furnishes a battery-backup real-time clock and up to 64 kbytes of EPROM. Eight kbytes of battery-backed static RAM are optional. The price is \$4,595 for the computer and \$1,395 for the Unix object license. **Pascot**, 17981 Skypark Cir, Irvine, CA 92714. **Circle 127**



Boards emulate 8088 and 80188 processors

Emulating either the 8088 or 80188 processors, the Y88, B88 and R188 single-board computers are IBM PC bus-compatible. The boards provide up to 256 kbytes of EPROM, a programmable serial port console with RS-422A and PC-compatible BIOS. The Y88 targets OEM applications; the B88 is for use with a PC keyboard. The R188 accommodates the 8088 and the nonprotected 80188/80286 instruction sets. **I-Bus Systems**, 5730 Chesapeake Ct, San Diego, CA 92123. **Circle 128**

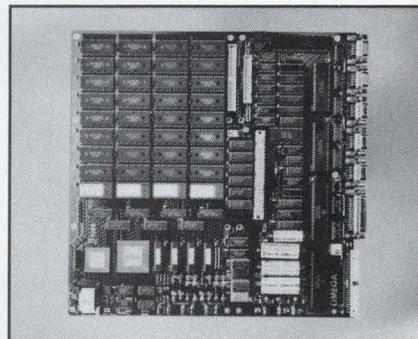
25-MHz processor features zero-wait-state on VMEbus

The CPU-21B 32-bit CPU operates at 25 MHz on the VMEbus with zero-wait-state. The CPU connects

to up to 1 Mbyte of static RAM via a local memory extension board. Based on a 68020 microprocessor, the unit includes a 68881 20-MHz coprocessor and eight Jedec-compatible sockets for up to 512 kbytes of EPROM. The board's multiprotocol communications controllers handle up to three serial ports. The board has VMEbus system control functions and handles data and address functions. **Force Computers**, 727 University Ave, Los Gatos, CA 95030. **Circle 129**

32-bit single-board computer offers five serial ports

The Omega-OEM has a 12.5-MHz 68020 processor and a 25-MHz 68881 coprocessor. The multilayer single-board computer measures 12 x 12 in. and fits into a 19-in. rack.



The board has five RS-232C ports, a Centronics port, a 16-bit bidirectional parallel printer port and a battery-backed clock/calendar. It offers 1 Mbyte (expandable to 5 Mbytes) of no-wait-state nonvolatile static RAM, a small computer systems interface initiator and a Shugart-compatible floppy controller. **Windrush Micro Systems**, Worstead Laboratories, N Walsham, Norfolk, England, NR28 9SA. **Circle 130**

In the world of information storage, this is known as a warehouse.

Imagine storing up to 5.2 gigabytes of data on a standard T-120 VHS high-energy cassette. Now you can with Honeywell's new VLDS system (Very Large Data Store).



You no longer need thirty 10-inch reels of 6250 bpi 9-track computer tape. Or 5,200 double-sided 5¼-inch floppy disks. Or fifty-two 5¼-inch WORM optical disks. Just VLDS and a single standard VHS cassette.

VLDS provides a 4-megabyte-per-second sustained transfer rate, a media cost of less than .21¢ per megabyte, and a bit error rate of 10^{-12} . And to assure easier, cost-effective system integration, optional high-performance imbedded controllers are available, including SCSI and VAX/VMS.

VLDS is the latest advancement in Honeywell's line of magnetic tape systems that have been unsurpassed in quality and support services for over 30 years.

For details on VLDS, and its OEM pricing, contact Tom Balue, Honeywell Test Instruments Division, Box 5227, Denver, CO 80217-5227. (303) 773-4491.

Together, we can find the answers.

Honeywell

CIRCLE NO. 40



68020 in-circuit emulator increases speed to 16.7 MHz

An enhanced version of Applied Microsystems' 68020 in-circuit emulator reaches 16.7 MHz. Additional new features include an expanded trace memory width from 72 to 101 bits; a trace disassembler capable of handling 8-, 16- and 32-bit wide traces; a time-stamp capability with resolution steps of 100 ns, 1 μ s or 10 μ s; and improved software that

searches raw trace for address, data, or status information. An expanded RAM overlay memory option adds up to 2 Mbytes. The emulator operates as a stand-alone or with a variety of hosts, including the IBM PC family, and Sun, Apollo and Digital Equipment Corp workstations. **Applied Microsystems**, 5020 148th Ave, Redmond, WA 98073. **Circle 131**

Package accelerates 3-D CAD

Running under the Microsoft Windows environment, Pro3D/PC is a three-dimensional solids modeling program. The package includes a 3-D cross-sectional modeling tool that lets users draw slices of an object and then turn those slices into a solid model. Two-dimensional drawing aids provide rotation in 1°

increments, eight mirrors, high-resolution curve generation and curve fitting, 12 types of scaling, linearization, zooming, and relative and absolute dimensioning. The system requires 512 kbytes of RAM and a color graphics adapter board. Price is \$595. **Enabling Technologies**, 600 S Dearborn St, Suite 1304, Chicago, IL 60605. **Circle 132**

Data Communications

Analyzer debugs StarLAN networks

The LANalyzer EX 5000E/S for Starlan networks debugs and analyzes local area network applications and protocols for system develop-

ment and monitoring applications. Components include the Exos 225 Ethernet Analyzer Controller board, a Starlan adapter board, and system software for an IBM PC XT, PC AT or compatible computer. Users can

Router handles complex board designs

The ARX20 peripheral processor configuration uses multiple dedicated algorithms to route complex, high-density printed circuit boards. Operating as a network server, the processor queues and routes numerous designs from many engineering workstations. Dynamic monitoring of electrical and mechanical design rules creates error-free multilayer routing of analog, digital or mixed boards. Spacing flexibility permits the definition of traces, clearances and vias of any size. The system uses a 32-bit 68020 microprocessor hosting the Unix V operating system. Price is \$75,000. **Scientific Calculations**, 7635 Main St, Fishers, NY 14453. **Circle 133**

Change-control tools aid documentation management

Complementing Context documentation workstations, a series of tools manages changes from product-change proposal, review and approval to the production and distribution of changed material. The tool set builds on the capabilities of DOC, the company's text editor and formatter. The system automatically maintains an audit trail of a document and various changes to it, recording when each change was created, modified or frozen and by whom. It can electronically produce change markings and change pages or produce a hard copy of them. **Context**, 8285 SW Nimbus Ave, Beaverton, OR 97005. **Circle 134**

define a range of test criteria for up to eight channels to capture specific types of information simultaneously. Price is \$9,995. **Excelan**, 2180 Fortune Dr, San Jose, CA 95131.

Circle 135

Modem uses dual error-correcting protocols

The 2400-33 is an error-correcting 2,400-bit/s modem for users of terminals and PCs. It supports both MNP and X.PC error-correcting protocols. Running at 2,400, 1,200, or 300 bits/s, the Hayes-compatible modem supports the industry-standard IBM PC AT command set. The price is \$749. **Ven-Tel**, 2342 Walsh Ave, Santa Clara, CA 95051.

Circle 136

Unix V.3 Ethernet connection runs on 80386-based PC AT

An integrated Unix V.3 Ethernet connection for an 80386-based IBM PC AT, the NP622 networking package consists of an NP600A protocol processor board, Transmission

Control Protocol/Internet Protocol (TCP/IP) software, stream drivers, and supporting network utilities. The product supports the Remote File Sharing of Unix V.3, assuring transparent file and device sharing among Unix V.3 systems on the network. Standard TCP/IP applications, such as Telenet, File Transfer Protocol and Berkeley's R-Utilities, streamline communications among Unix V.3 and other Unix and non-Unix systems. Price is \$1,390. **Micom Systems**, 4100 Los Angeles Ave, Simi Valley, CA 93063. Circle 137

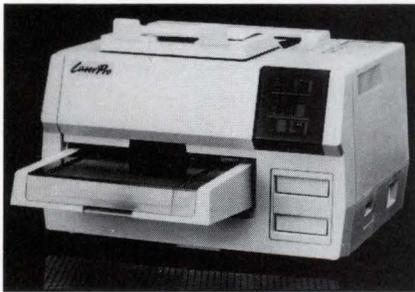
Managers control networks

The INM 400 network manager offers single-point management and control capabilities for medium-sized networks. INM supports up to 1,600 channels at speeds up to 9,600 bits/s on Infotron's 990/992NP net-



work processors, 400 Infostream 1500 T1 multiplexers or 64 Infostream NX nodes. A second product, the INM 1000, delivers network management and control features for large networks. It supports up to 4,000 channels at speeds up to 9,600 bits/s. Prices are \$38,000 and \$48,000, respectively. **Infotron Systems**, Cherry Hill Industrial Ctr-9, Cherry Hill, NJ 08003. Circle 140

Peripherals



Laser printer provides custom font generation

Printing at 8-pages/min, the Laserpro 814 graphics and text laser printer offers a custom font-generation system that lets users vary parameters such as typeface and point size. It has 1.5 Mbytes of RAM, expandable to 3 Mbytes. The printer's command language permits simple access to all printer features from a system terminal. The unit provides 300-dot/in. resolution, downloadable font capability, portrait and landscape print modes, and face-down printing. Included emula-

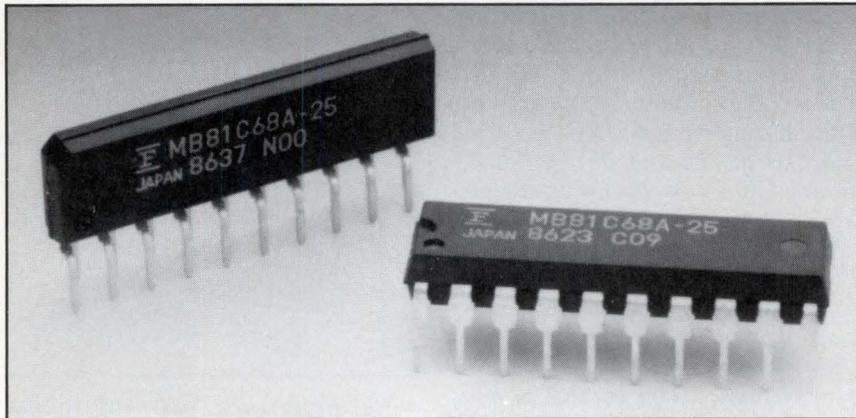
tions are Laserjet Plus, HP-GL-compatibility, Epson FX-80, Diablo 630 and ANSI 3.64. Price is \$5,650. **Office Automation Systems**, 8352 Clairmont Mesa Blvd, San Diego, CA 92111. Circle 138

Monitors adjust to horizontal frequencies

The ECM 1910, 1911 and 1912 color monitors adjust automatically to horizontal and vertical frequencies. The horizontal adjust lets the monitors interface with personal computers that use 15- to 34-kHz graphics boards and software. Vertical frequency adjusts from 50 to 85 Hz. The 19-in. monitors' resolution is 1,024 x 512 pixels noninterlaced and 1,024 x 800 pixels interlaced. The 1910 and 1911 offer short-persistence phosphor; the 1912 offers long-persistence phosphor. Price is \$3,195. **Electrohome**, 809 Wellington St N, Kitchener, Ont, Canada N2G 4J6. Circle 139

Laser printer suited to multiuser environments

The Laserjet 2000 laser printer offers a print speed of 20 pages/min. Designed for use with personal computer networks and minicomputers, the printer supports Hewlett-Packard's Printer Command Language. In addition to two 250-page paper-input bins and a 1,500-page correct-order output stacker, the printer supports letter, legal, ledger, executive, and European A3 and A4 paper sizes. Its standard 1.5-Mbyte RAM is expandable to 5.5 Mbytes. It supports 34 fonts and offers automatic font rotation. A second version features a third paper-input bin with a 2,000-page capacity, and a third version features the third paper-input bin plus automatic dual-sided printing. The price of the Laserjet 2000 printer ranges from \$19,995 to \$24,995. **Hewlett-Packard**, 1820 Embarcadero Rd, Palo Alto, CA 94303. Circle 141



SRAMs combine fast access and low power consumption

The MB81C68A and MB81C69A families of 16-kbit static RAMs have access times as low as 25 ns. Organized as 4,096 words \times 4-bits, the devices offer chip-select times of 15 ns. Fabricated with mixed-MOS technology, they provide 385 mW power

consumption. A power-down mode for the 68A reduces power consumption to 138 mW. Both families are fully static and require no clock or timing strobes. **Fujitsu Microelectronics**, 3320 Scott Blvd, Santa Clara, CA 95054. **Circle 143**

Devices feature fast multiply time

The ADSP-8018 10 kHz ECL-compatible multiplier and the ADSP-7018 TTL-compatible multiplier offer 15- and 19-ns multiply times, respectively. Each device supplies a 32-bit parallel output port. Input, instruction status and output latches are independent and can be made transparent. Operands and results are stored in individually enabled latches with separate clocks. In quantities of 100, prices are \$260 and \$205 for the ADSP-8018 and ADSP-7018, respectively. **Analog Devices**, One Technology Way, Norwood, MA 02062. **Circle 142**

Cache memory controller targets the 80386

Eliminating 80386 wait states and reducing bus accesses to main memory, the 82385 cache controller executes a posted write-through policy for writing to main memory. A bus-watching mechanism ensures cache coherency without performance penalties. Interfaces to the

80386 and system bus are hardware- and software-transparent. The device stores 32 kbytes of most frequently used code and data from the 80386's 4-Gbyte physical address range. Its bus-watching logic ensures that cache memory contains an up-to-date copy of the main memory segment. **Intel**, PO Box 58065, Santa Clara, CA 95052. **Circle 144**

1-Mbit DRAMs use buried stacked capacitor cell design

The MSM411000 1 Mbit \times 1 page, the MSM414256 256 kbit \times 4 page and the MSM411001 1 Mbit \times 1 nibble-mode dynamic RAMs are available in 100- or 120-ns versions. A proprietary buried stacked capacitor cell design permits a bonding option in which one die can be selected to produce any of the three DRAMs. The devices have a feature that refreshes column address strobe-before-row address strobe. After refresh is performed, the refresh address counter is automatically incremented. All inputs are TTL-compatible. Standby power con-

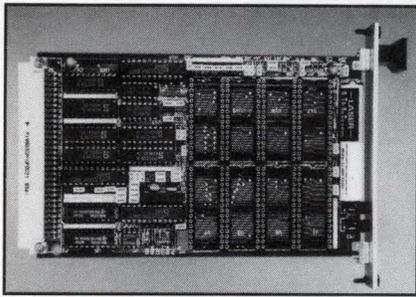
sumption is 28 mW; active mode consumption is 385 and 413 mW for the 100- and 120-ns versions, respectively. Prices start at \$50 each in quantities of 100. **Oki Semiconductor**, 650 N Mary Ave, Sunnyvale, CA 94086. **Circle 145**

Peripheral increases system I/O speed

The 82380 integrated system peripheral incorporates a direct memory access controller that uses the 80386 32-bit bus bandwidth via eight independently programmable channels. On-chip peripheral functions include a 20-level programmable interrupt controller, four 16-bit programmable interval timers, a programmable wait-state generator, a dynamic RAM refresh controller and system reset control logic. Used with 16- or 20-MHz versions of the 80386, the device is a superset of prior generation peripherals used in IBM PCs, ensuring compatibility with existing PC-DOS applications. Prices in lots of 100 are \$149 each for the 16-MHz version and \$299 each for the 20-MHz version. **Intel**, PO Box 58065, Santa Clara, CA 95052. **Circle 146**

Graphics device operates at 66 MHz

A version of the Bt453 Ramdac graphics device runs at 66 MHz. It integrates three 8-bit video digital-to-analog converters with a 256 \times 24-bit dual-ported RAM color palette. The device supports up to 259 simultaneous colors from a palette of 16.8 million. A separate 3 \times 24-bit RAM overlay palette stores colors for displaying cursors, grids, and menus. The device generates RS-343A-compatible RGB signals and drives doubly terminated 75- Ω coax. Prices in 100-piece quantities are \$45 for ceramic dual in-line packages and \$49 for 44-pin J-lead versions. **Brooktree**, 9950 Barnes Canyon Rd, San Diego, CA 92121. **Circle 147**



Module provides VME RAM/ROM

The XVME-10 single-high VME memory module accommodates a total of 1 Mbyte of RAM, EPROM and mask-programmable ROM, or 256 kbytes of EEPROM. The module provides eight 28- or 32-pin Jeduc sockets logically arranged as two banks, each with four sockets. Each bank is independently configured via jumpers for the type and speed of its memory devices, and for the address modifiers and the VMEbus addresses of those devices. The XVME-10 module provides an on-board battery backup circuit and two front-panel LEDs that indicate memory access activity to the two memory banks. The price is \$400. **Xycom**, 750 N Maple Rd, Saline, MI 48176. **Circle 148**

Test and development systems tackle SCSI

The SDS-100 offers 50 preprogrammed small computer system interface (SCSI) test functions through a menu-driven, interactive interface. The device operates at an asynchronous transfer rate of 1.8 Mbytes/s. An I/O status window automatically provides statistics on bus status, sense information and bytes written, compared and uncomparing. A second product, the SDS-210, is a specialized logic analyzer that monitors and interprets SCSI bus activity. It combines traditional logic analyzer capabilities with simple programmability and SCSI bus event results. Price for the SDS-210 is \$3,750. The SDS-100 sells for \$5,500. **Adaptec**, 580 Cottonwood Dr, Milpitas, CA 95035. **Circle 149**

Board supplies 4 Mbytes of RAM for IBM PC AT

The BocaRAM/AT offers up to 4 Mbytes of RAM per board for IBM PC AT and PC XT 80286 and compatibles using 64- or 256-kbit, 150-ns RAM chips. The board can be configured with 128 kbytes of conventional memory and/or up to 2 Mbytes of expanded memory. Its extended memory can be configured with up to 4 Mbytes per board. Packaged with a menu-driven installation program, the board uses a hardware-based Lotus-Intel-Microsoft Expanded Memory Specification. Up to four boards may be connected on the 16-bit bus for up to 8 Mbytes of expanded memory. Extended memory operates with Vdisk, Xenix and DOS. The board includes a RAM disk utility, a print buffer

and diagnostics software. Prices start at \$245. **Boca Research**, 6401 Congress Ave, Boca Raton, FL 33431. **Circle 150**

Board provides error detection

VMERAM/16 memory module offers on-board error detection and correction for the VMEbus. Using 1-Mbit zig-zag in-line package dynamic RAMs, the board offers a 16-Mbyte capacity. It uses a chip set caching feature for fast average access times. The board supports block mode transfers and unaligned transfers. Available in an 8-Mbyte version, the module allows 16-, 24- or 32-bit addressing and 8-, 16- or 32-bit word lengths. **Clearpoint**, 99 South St, Hopkinton, MA 01748. **Circle 151**



Tape subsystem stores 2,300 Mbytes

Storing up to 2,300 Mbytes of data, the EXB-8200 8-mm tape-cartridge subsystem consists of a tape drive and an integrated controller. The subsystem is the same size as a full-height, 5¼-in. disk drive. It uses helical scan technology to write data in a series of diagonal tracks across the tape surface to get more tracks/in. Read and write heads are

mounted on a 1,800-rpm drum. The subsystem features a small computer systems interface, on-board error-correction code and recovery procedures. Data transfer rate is 1.5 Mbytes/s peak, 246 kbytes/s sustained. The price of the subsystem is under \$1,000 in OEM quantities. **Exabyte**, 4876 Sterling Dr, Boulder, CO 80301. **Circle 152**

Development kit taps 80386 protected mode

The 80386 DOS Developer's Tool Kit lets developers write programs larger than the 640 kbytes that run in the 80386's protected mode under PC-DOS or MS-DOS control. The kit contains an 80386 assembly-language debugger, a compiler, an assembler, a linker and VM/RUN. VM/RUN loads the 80386 application into the protected mode. When the application requests a DOS or BIOS service, VM/RUN passes that request to DOS in virtual 80386 mode and returns control to the application once the request has been serviced. Price is \$1,995. **Softguard Systems**, 2840 San Tomas Expwy, Santa Clara, CA 95051. **Circle 153**

Assembler targets programmable processors

The mcASM structured microcode assembler is used to program micro-programmable processors, such as the Am2900 and Am29300 families, Am29100 controller family, Am 29500 signal processor family, and ADSP, 74AS888 and 74AS890 families. The assembler's constraint management catches errors at assembly time. A nonpositional keyword syntax allows field assignments in any order. Microword widths of up to 1,024 bits are supported and multiple microword formats can be defined for each assembly, consisting up to 128 fields. Price is \$4,500 for the VAX version and \$2,000 for the PC-DOS version. **Microtec Research**, PO Box 60337, Sunnyvale, CA 94088. **Circle 154**

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Fault-tolerant computer

Eight-page brochure describes XA2000 fault-tolerant computer system for on-line transaction processing and company's hardware approach to fault tolerance. **Stratus Computer**, Marlboro, MA. **Circle 155**

Data-acquisition cards

System 10 catalog provides detailed descriptions of entire family of off-the-shelf data-acquisition and control cards for DataPac mainframes. **Daytronic**, Miamisburg, OH. **Circle 156**

Multibus computer boards

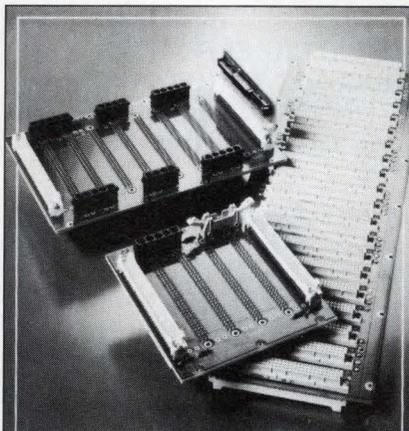
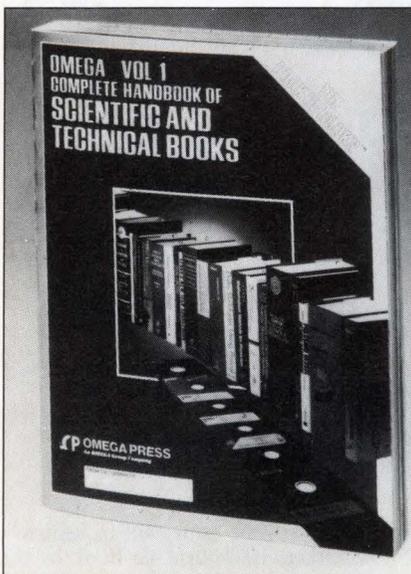
Product guide describes and illustrates series of Multibus I and II single-board computers, memory boards and software support. **Microbar Systems**, Sunnysvale, CA. **Circle 157**

IEEE 488 interfaces

Catalog contains detailed information about line of instruments, plotters, printers, I/O devices and software packages to support IEEE 488 systems. **IOtech**, Cleveland, OH. **Circle 158**

Handbook of technical texts

Encyclopedia/handbook lists more than 10,000 significant texts and scientific software from 14 science and technology publishers. Request copies on company letterhead and enclose business card. **Omega Engineering**, PO Box 4047, Stamford, CT 06907.



Multibus II hardware support

- Support for IEEE P1296 Bus Standard
- Backplanes-Extender Boards
- Microracks-Cardframes
- Power Supplies-Prototyping Boards



Multibus II hardware

Products, including backplanes, extender boards, power supplies and prototyping boards, designed to meet the IEEE P1296 bus standard are described in 16-page catalog. **Bicc-Vero Electronics**, Hamden, CT. **Circle 159**

Data communications

Direct sales catalog presents information about line of hand-held test sets, modems, multiplexers, converters, data switches and accessories for data communications. **International Data Sciences**, Lincoln, RI. **Circle 160**

Graphics subsystem

Brochure describes CGS-4600 graphics engine, a 68020-based, single-card interactive subsystem that supplies 1,280- \times 1,024-pixel color graphics when installed in DEC MicroVAX II computer. **CalComp, Display Products Div**, Hudson, NH. **Circle 161**

Programmable gate arrays

Design handbook contains 288 pages of data on family of CMOS user-programmable gate arrays and associated development systems as well as information on implementing designs. **Xilinx**, San Jose, CA. **Circle 162**

CMOS microprocessor

Vol 20-2 of Analog Dialogue contains performance data of ADSP-2100 single-

chip CMOS microprocessor for digital signal processing, plus data on a digital-to-analog converter and modular I/O industrial automation processor. **Analog Devices**, Canton, MA. **Circle 163**

Parallel processor

Four-page brochure provides applications information, technical specifications and operating diagrams for the I-bus IQ1888 parallel processor, which is based on a 10-MHz 80188 processor. **I-Bus**, San Diego, CA. **Circle 164**

Data distribution

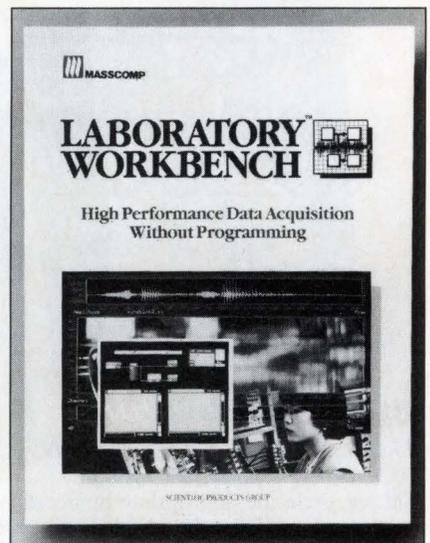
Catalog describes range of data-distribution products, including line drivers, local multiplexers, data private branch exchanges and accessories. **Equinox Systems**, Miami, FL. **Circle 165**

STD Bus products

Details on full line of hardware and software products, including CPU, memory, I/O and special-function cards, for STD Bus systems are presented in 20-page catalog. **Octagon Systems**, Westminster, CO. **Circle 166**

Data-acquisition software

Brochure describes Laboratory Workbench software that scientists use to design, test and run high-performance data-acquisition projects without writing code. **Masscomp**, Westford, MA. **Circle 167**



DESIGNER'S BOOKCASE

SOFTWARE VALIDATION, VERIFICATION, TESTING AND DOCUMENTATION

By Stephen J. Andriole

This complete sourcebook is divided into five separate "books" to enable the reader to pick and choose the information they need. The first book is called Planning for Software Validation, Verification and Testing. Book two deals with Software Validation at a much more specific level. Book three deals with structured methodology using a specific methodology. Book four describes 30 techniques and tools for software validation, etc. Book five deals with software documentation including guidelines for:

- Preparing a Management Summary Manual
- Preparing a User's Manual
- Preparing a Programmer's Manual
- Preparing an Analysts Manual

\$49.50

Circle 241

CREATING EFFECTIVE DOCUMENTATION FOR COMPUTER PROGRAMS

By G. Prentice Hastings and Kathryn J. King

With the techniques and procedures contained in this handbook, it's easy to produce the kind of clear documentation that lets end-users fully utilize even the most complex software. You get step-by-step writing guidelines...an invaluable "resource timeline" that shows who is doing what during each phase of the documentation process...model formats for different users or applications...strategies for cutting production costs to the bone—plus helpful procedures for maintaining smooth and efficient communications between the documentation writer and the programmers, project managers and everyone else involved in the process.

\$24.95

Circle 242

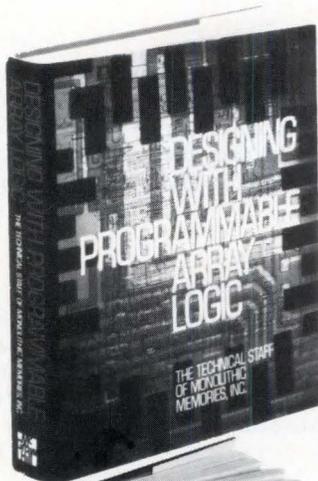
DESIGNING WITH PROGRAMMABLE ARRAY LOGIC, 2/e

by The Technical Staff of Monolithic Memories, Inc.

Programmable array logic devices save time and money by solving many of the system-participating and interface problems brought about by progress in semiconductor technology. The comprehensive book discusses the theory behind PAL, the available types of PAL chips, and their applications, with design examples. It shows how PALs can lower inventory, cut design cycles, and provide high complexity with maximum flexibility, making them a circuit designer's best friend!

\$42.50

Circle 244



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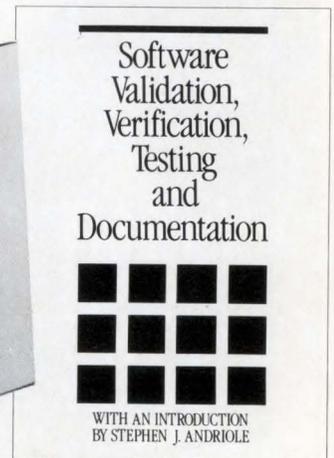
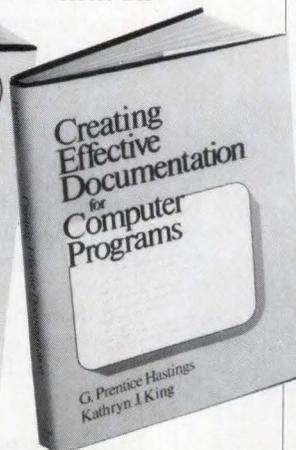
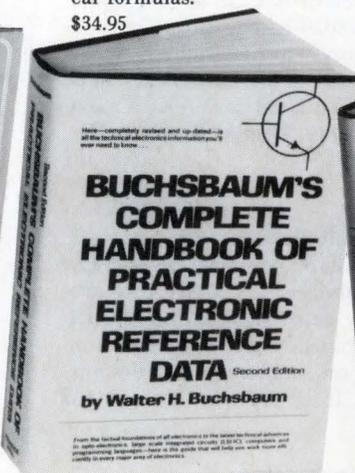
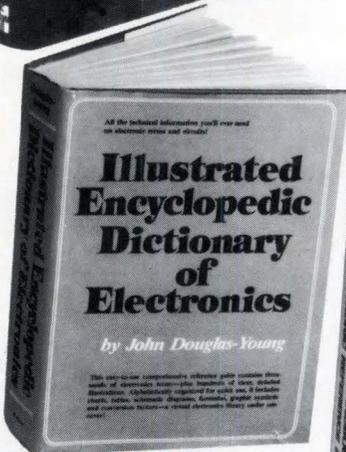
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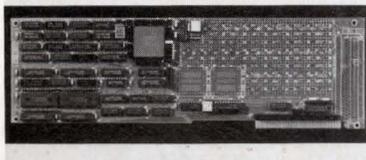
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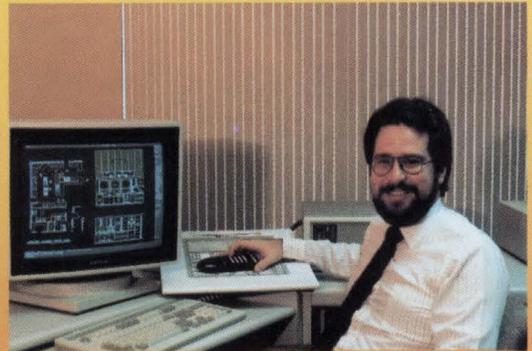
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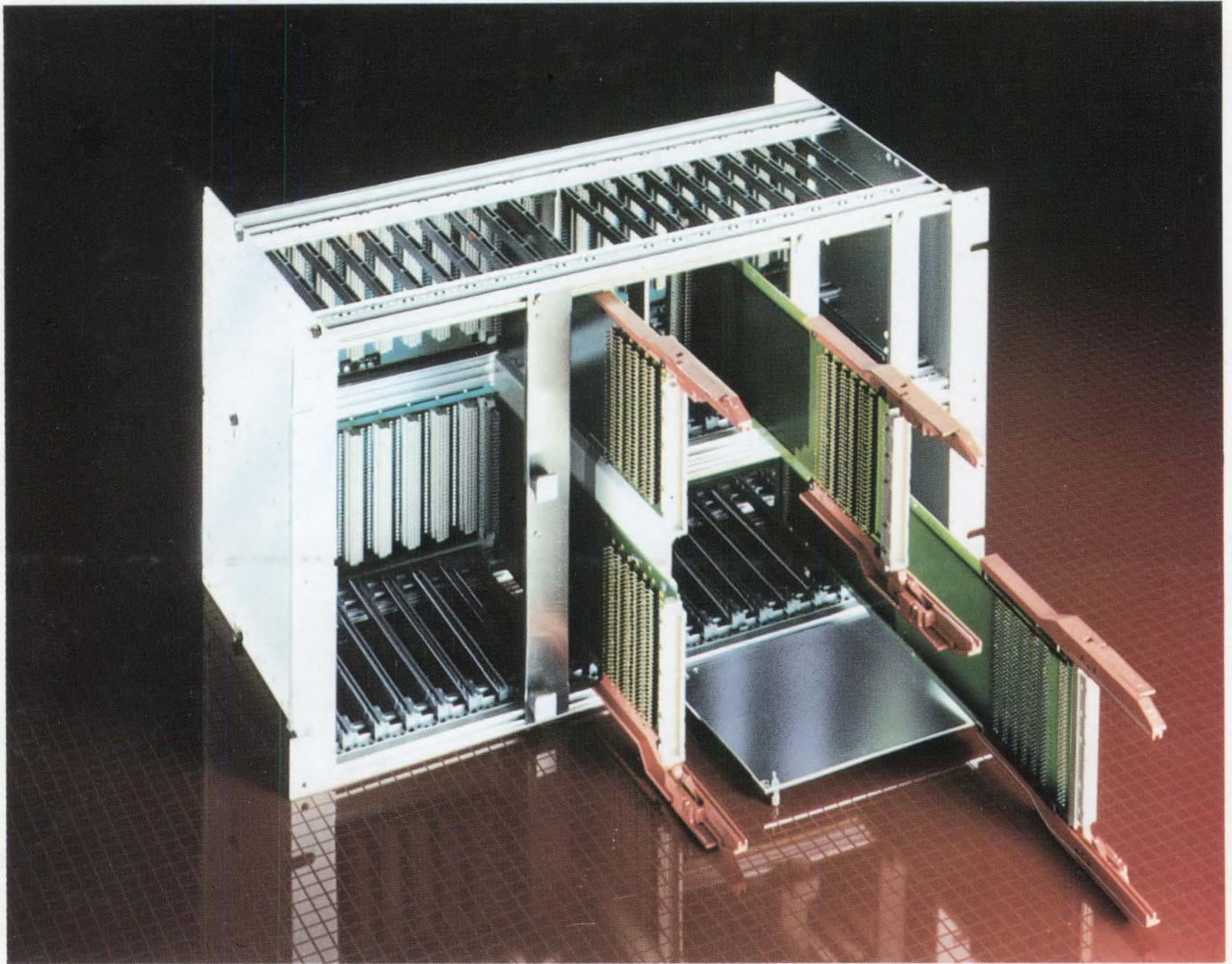
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