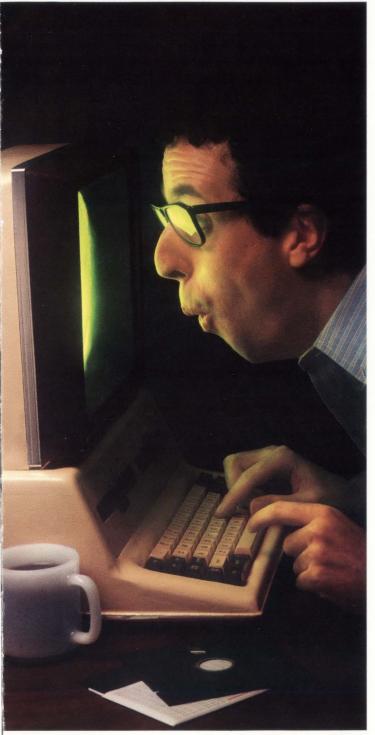


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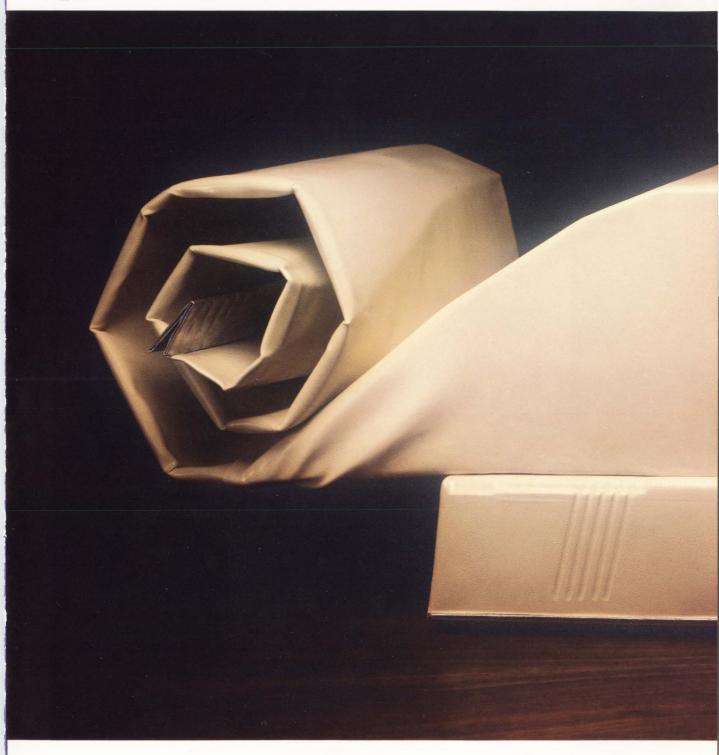
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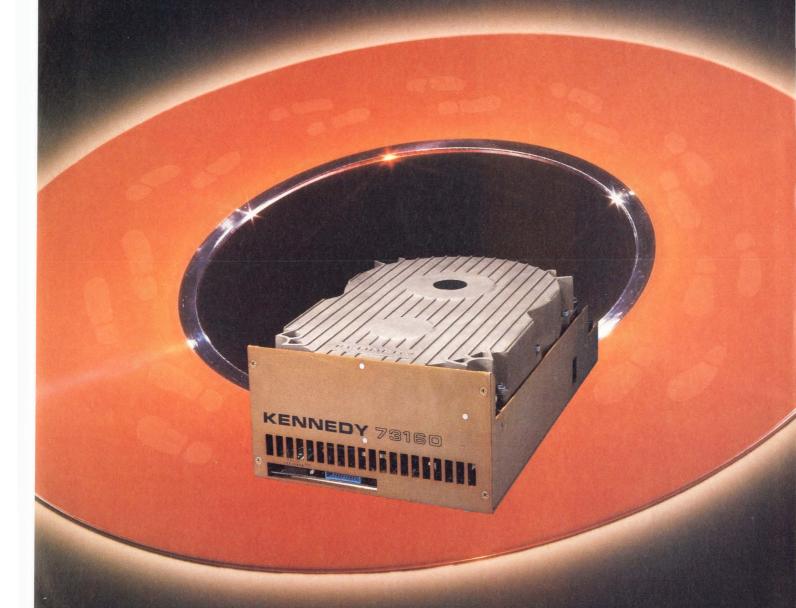
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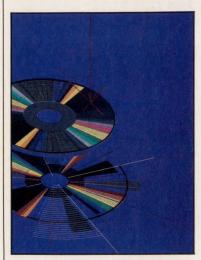
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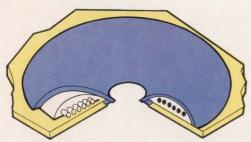
This month's cover was designed at Coddbarrett Associates, Inc, by Mary Codd and Steve Branch. It was illustrated by Mary Codd, using a DICOMED D-38 design station and D-48 high resolution film recorder.

SPECIAL REPORT ON MASS STORAGE

- Mass memory systems continue to proliferate, providing a match for every system storage need. Disks pack gigabytes of data, tapes promise compact storage for these masses of data, and optical techniques offer still untapped potential. Meanwhile, standards groups hope to gain agreement on compatibility issues to ensure that no matter what price/performance equation a system presents, a storage system will provide a plug-in solution.
- 71 Mass storage devices keep pace with system needs
 Storage peripherals stretch and shrink to serve recognized system
 demands. Renewed standards efforts open the way for technological
 advances to come and allow designers to mix or match at will.
- 85 Optical memory research pays off
 Delivering on promises to provide gigabit capacities, optical memories are coming into their own. At the same time, the pieces needed for the next generation of products are falling into place.
- 97 Secondary storage devices look to the long term
 Secondary storage is now a primary concern—and a dilemma—for designers and users of computer systems. The problem can be solved for both the short and long term with intelligent tape drives.

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- 183 Thirty-two bit micro tailored for high level languages

 A symmetrical architecture, multiple addressing modes, and slave processors support efficient high level language compilers in a 32-bit microprocessor.
- 197 Nonvolatile memory gives new life to old designs Terminals and other equipment can be made more flexible, and product life can be extended by upgrading and customizing with NOVRAMS and EEPROMS.
- 213 Simulator drives digital designs
 Designing complex circuitry requires
 sophisticated design aids at all levels. Logic
 simulation, from functional specs to fault
 analysis, manages and automates the process,
 freeing the designer for more creative tasks.

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- 113 Cartridge disk meets needs of portable systems

 Fast access, large capacity, and removability are key data storage criteria. Cartridge disks combine all these in a single low power device.
- 123 Two-chip set tackles disk control problems
 Handling data separation functions before passing data to the disk
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 while ensuring design flexibility.
- 141 Designing hard disk drives to take abuse

 The bangs and bumps of an office environment can affect the performance of hard disk drives. Some economical designs can provide the shock and vibration protection necessary to ensure reliable operation.
- 157 Efficient 1/O unleashes benefits of open bus concept
 Innate advantages of the open bus can free CPU-, bus-, and 1/O-bound
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SYSTEM COMPONENTS

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Personal computer benefits from 80286, networking, and software

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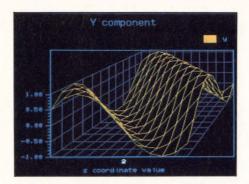
Dual-processor design soups up supermicro system

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Workstations unite 32-bit processing with graphics

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Ease of system installation highlights system clock chip

228 Data communications:

Seven ISO/OSI layers covered by powerful LAN boards

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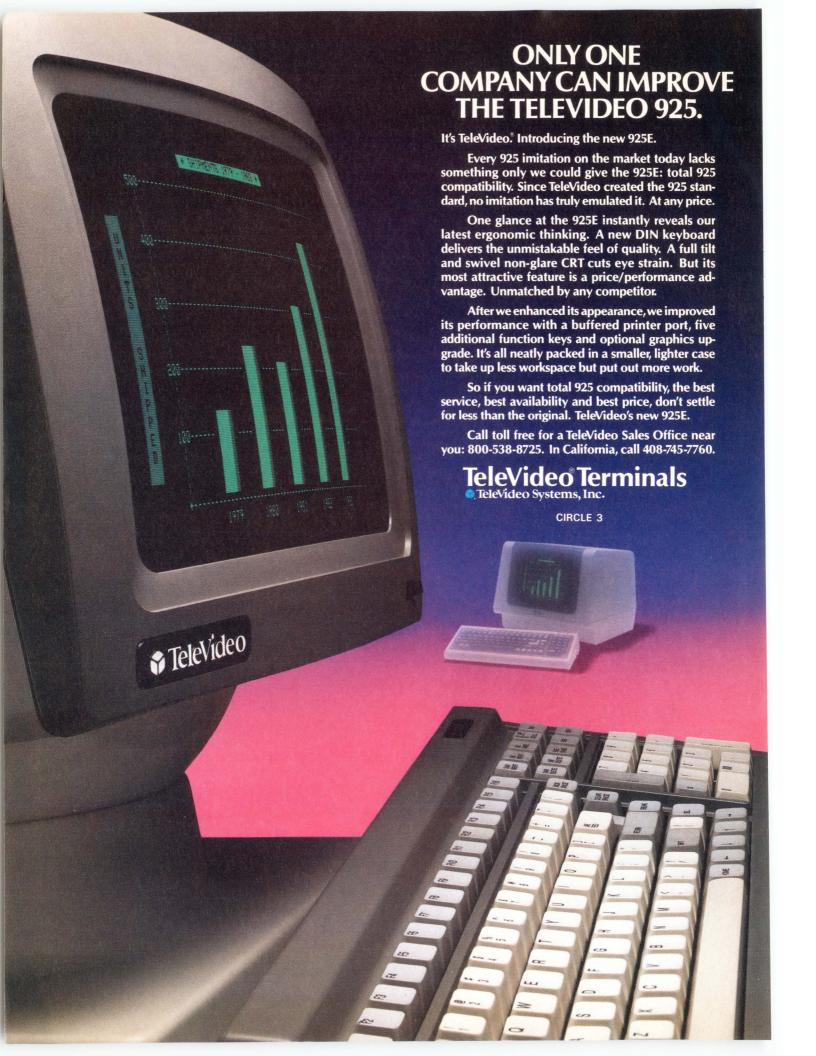
Support package allows benchmarking and debugging

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WESCON/84

51 Geopolitics of the 80s—and its effect on the entire electronics industry—will be stressed at WESCON/84, from the keynote address through the entire professional program. Special events will also be included to complete IEEE's year-long centennial celebration.



UP FRONT

Data General finally enters portable market

According to several industry sources, Data General Corp (Westborough, Mass) will announce its long-expected portable computer just after this issue of *Computer Design* goes to press. NCC scuttlebutt (see *Computer Design*, "Up front," Aug 1984, p 8) now seems to have been only minimally accurate, but the new system will have an LCD and built-in disk drives as reported. However, that display will be one of the largest yet offered with a portable computer—twenty-five 80-char lines. Software compatible with the IBM PC, the battery-powered briefcase-size Data General unit will be available with a choice of either one or two diskette drives and will weigh less than 10 lb.—*S.F.S.*

IBM blesses three graphics standards

The graphics industry took a big step toward standardization when IBM announced its PC Professional Graphics Series. IBM has thrown its weight behind three proposed standards—the Virtual Device Interface, the Graphical Kernel System, and the Virtual Device Metafile. All three are either proposed or under consideration by ANSI. The VDI standard defines a device-independent interface between application software and I/O devices; the GKS, already adopted by the ISO, provides applications programmers with a standard interface to graphics utilities and tools; and the VDM is for storage of graphics or text data. IBM's Professional Graphics Series was developed by Graphic Software Systems (Wilsonville, Ore). The latter company is actively involved in the ANSI standards committee—a good indication that IBM will be in line with ANSI standards once they are adopted.—*R*, *G*.

CAE test and verification made cost effective

Integrating test and verification into computer aided engineering could, until recently, only be achieved in automatic test equipment costing upwards of \$100,000. Now, for almost a quarter of that price, designers can have all the hardware required to simulate a prototype IC and to compare the resulting output with a known good simulator output at realtime device operating speeds. Design Master, from Integrated Measurement Systems, costs \$29,200 and fits into the design environment by interfacing with any computer system via either RS-232 or IEEE 488 interfaces, or with a terminal through VT100 terminal emulation. It will receive and execute test commands and report the results of the test procedures. The host computer system can be most mainframes, mini or microcomputers, or any of the powerful CAE workstations. By integrating Design Master into the CAE environment, the designer can reduce the time required to test the prototype IC by 45 to 80 percent, according to the Beaverton, Ore company—N.M.

UP FRONT

Full ANSI Fortran on the IBM PC

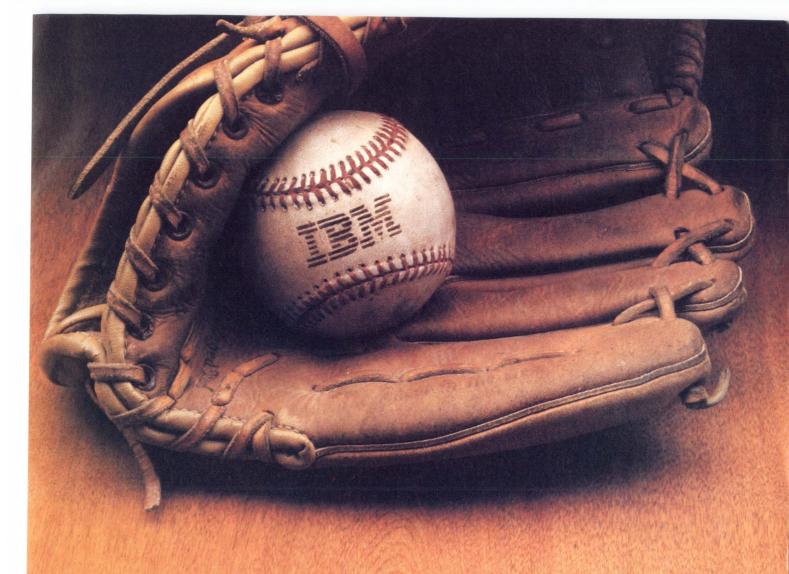
Computer system designers running their numerical computations on the IBM PC have found that many engineering programs require an IBM PC Fortran compiler that is more sophisticated than those from Microsoft, Inc and other firms. Many Fortran-based engineering programs are made to run, for example, on DEC's PDP-11/70 and VAX machines and their Fortran IV compilers. Now, Small System Services, Inc offers its Computer 2000 Fortran compiler that runs full Fortran IV (to ANSI X3.9-1966 standards, including double precision and complex variables) on the IBM PC. Fortran programs for the PDP-11/70 and VAX can run on the PC with this compiler. The compiler has features beyond those specified in the 1966 ANSI standard.—H.H.

Factory automation vendors must talk or flop

No matter how much is predicted for "the factory of the future," that facility will never exist unless its various computers and computer-controlled units function with a standard interface. They must talk to one another. General Motors still leads the movement to select standard protocols for multivendor data communications in the automated factory. Backed by the National Bureau of Standards as well as the International Organization for Standardization and the American National Standards Institute, GM began the studies in 1980 that have now resulted in its Manufacturing Automation Protocol (MAP). MAP is a seven-layer communication model that uses existing or emerging protocols. A number of major potential suppliers of system components-including IBM, DEC, Gould, HP, Motorola, and Concord Data Systems—have joined the program, making cooperation mandatory for other companies hoping to remain in the market. In addition, Intel Corp just announced its commitment to support MAP. According to Ed Gelbach, executive vice president, "Intel's support of MAP reflects its continuing commitment to meeting the needs of factory automation at the silicon, board, systems, and software levels."—S.F.S.

Professional 350 goes multi-user with new operating system

Digital Equipment Corp's Professional 350 personal computer has two limitations—it can accommodate only one user, and its operating system is not compatible with the PDP-11. S&H Computer Systems (Nashville, Tenn) wants to change all that with its new PRO/TSX-Plus operating system. This multitasking operating system allows the Professional 350 to support three users. It also provides access to applications and utilities under RT-11, DEC's most popular operating system for the PDP-11. Userdefined priority, data and directory caching, and user-friendly interface are said to be the selling points of the new operating system. PRO/TSX-Plus is a logical step for S&H Computer Systems; it is an enhancement of the company's TSX-Plus operating system, a multi-user, RT-11-compatible operating system for the PDP-11.—R.G.



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UP FRONT

Chip version of Lisp machine is on the way

Texas Instruments has been awarded a contract by the U.S. Navy to develop a Lisp VLSI chip with 2 to 10 times the processing power of available symbolic processors. The chip will operate at up to 40-MHz speeds and execute a superset of Common Lisp, recently adopted as the generic Lisp language by the Department of Defense. Worth \$6 million over 27 months, this project is part of DARPA's Strategic Computing Program, backbone of the U.S. effort to stay in the lead in computer technology. TI expects to use sub 2-micron CMOS technology while developing the chip at the company's Central Research Laboratories in Dallas, Tex. The VLSI IC will effectively replace several hundred ICs that currently execute Lisp instructions in commercial machines.—N.M.

Little things mean a lot—another step in submicron development

Motorola, Inc (Phoenix, Ariz) has announced a major milestone in its submicron CMOS development and very high speed integrated circuit program. That company has fabricated fully functional l k static RAMs with half micrometer geometries. The circuits feature fully scaled CMOS devices and have been successfully operated with both 3-V and 5-V power supplies. The SRAMs are believed to be the highest functional level of integration achieved to date with half-micron CMOS technology. Motorola has teamed with primary contractor TRW, Inc in a VHSIC Phase 1 program sponsored by the U.S. Navy's Naval Electronic Systems Command.—J.H.

Pascal environment covers DEC

A uniform Pascal-based software line, developed for all Digital Equipment Corp micro, mini and supermini computers, has been completed by Oregon Software (Portland, Ore). The recent addition of the company's Pascal-2 compiler for the VMS operating system means that a programmer can develop source code on any DEC computer and transport it to any or all other DEC machines. Also, all source-code debugging procedures are identical across all DEC computers.—T.W.

Chip and controller boost disk capacity

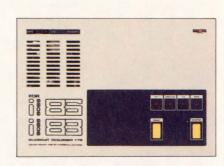
A new chip and controller board from Adaptek (Milpitas, Calif) use run-length limited encoding to increase disk capacity by 50 percent. These products, the AIC-270 encoder/decoder chip and the ACB-4070 controller board, are the first to bring RLL encoding to the microcomputer industry. The AIC-270 can be purchased separately or as part of the ACB-4070, which provides an interface between a SCSI bus and an ST506 disk. Two other new products place Adaptek in the secondary storage market for the first time. The ACB-4010 controller board supports ST506 removable disks and the ACB-3530 controller board supports QIC-36 quarter-inch streaming tape drives.—R.G.

COMPUTER DESIGN©1984 (ISSN-0010-4566) is published monthly, with a thirteenth and fourteenth issue respectively in June and October by PennWell Publishing Company, Advanced Technology Group, 119 Russell Street, Littleton, MA 01460. Second-class postage paid at Littleton, MA 01460 and additional mailing offices. COMPUTER DESIGN is distributed without charge to U.S. and W. Europe-based engineers and engineering managers responsible for computer-based equipment and systems design. Subscription rate for others is \$50 in U.S.A. and \$75 elsewhere. Single copy price is \$5.00 in U.S.A. and \$7.50 elsewhere. Microfilm copies of COMPUTER DESIGN are available and may be purchased from University Microfilms, a Xerox Company, 300 North Zeeb Road, Ann Arbor, Michigan 48106.

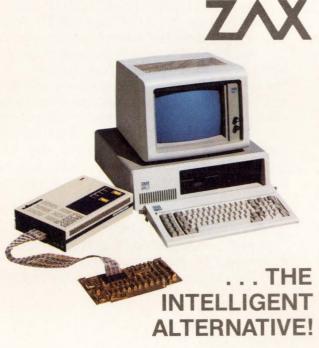
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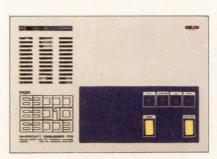
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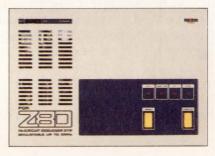


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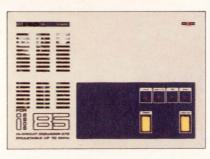




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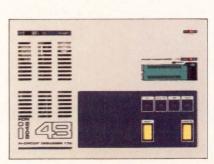
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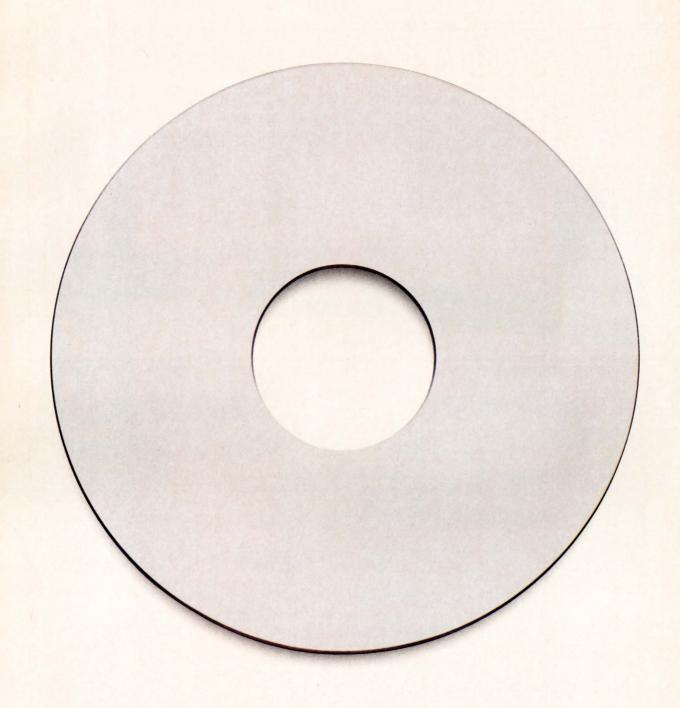
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AN AWARD WINNING TEAM

Last December, I mentioned that several of our editors had submitted entries for achievement awards in journalism and technical writing. I am proud to announce that we just about swept the board. This year, 16 of our entries received awards, compared to four last year. To place this in perspective, I should point out that none of our major competitors received any awards—unless they have been too modest to mention them.

I hesitated before writing this admittedly self-congratulatory editorial. I know how sickening it can be to watch, say, a TV news program and to hear the anchor people bragging about their Emmy awards instead of doing the job they are paid to do. Similarly, I believe that computer journalists should talk about the technology and the industry—not about themselves. But, like



the TV networks, we compete for audience preference against several formidable rivals. Although one of our major competitors lists its recent achievements on the editorial page of every issue, our editors tend to be more modest. To give our editors and artists the credit they deserve, however, I feel I should salute the editorial team that produces *Computer Design*.

The American Society of Business Press Editors honored *Computer Design* with a total of six awards—one in the National Competition, and five from the New England Chapter. Current and former *Computer Design* editors receiving ASBPE awards included: Chris Brown, Michael Elphick, Peg Killmon, Nicolas Mokhoff, and Sydney F. Shapiro.

In the International Competition of the Society for Technical Communication, two of our editors received an Award of Achievement for an article published in *Computer Design*. Editors also received awards from the Boston Chapter of the STC for nine of their entries. (The actual number of awards for these nine entries was 22 because many of the entries involved more than one editor.) Editors and artists receiving one or more awards in the STC contests were: Suki Adams, Chris Brown, Michael Elphick, Alan Green, Debra Highberger, Peg Killmon, Mark Lindquist, Jocelyn Melanson, Nicolas Mokhoff, Sydney F. Shapiro, Ken Silvia, Lauren Stickler, Leslie Ann Wheeler, and Tom Williams.

Finally, while I am praising our editors, I would like to introduce three people who recently joined our staff: John Miklosz, Bill Furlow, and Richard Goering.

John Miklosz, our new Executive Editor, came to us from *Electronic Engineering Times* where he was Technical Managing Editor. Earlier, he was an editor at *High Technology* magazine. With a PhD and MS in physics from Yale University and a BS from City College of New York, John has also worked as a researcher at GTE Laboratories.

Bill Furlow, our newest Senior Editor, joined us from *Electronic Products* magazine and will work out of our Sunnyvale, Calif office. He has also worked as an editor for *EDN* and *Electronic Business* (where he won a Jesse H. Neal Certificate of Merit from the American Business Press for a series of articles that he wrote). With a BSEE from Heald Engineering College in San Francisco, Bill has worked in industry for GTE, Ball Brothers Research, and Tektronix.

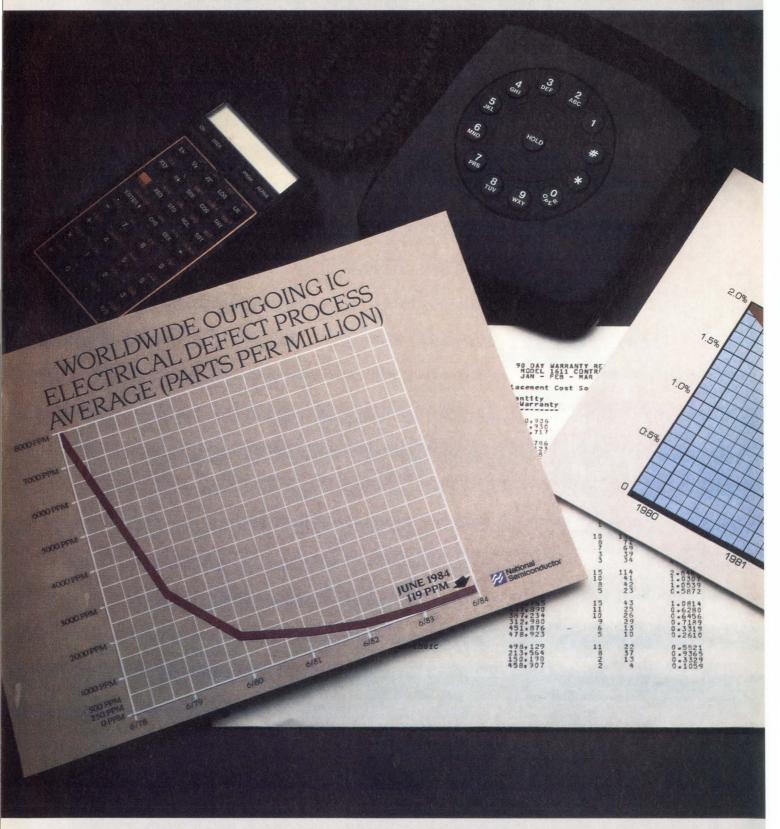
Our third new editor, Richard Goering, will also work out of our Sunnyvale office as Field Editor. He has a BA in Journalism from the University of California at Berkeley, and has studied computer programming at the University of Missouri. Before joining us, he headed a technical writing group at DIT-MCO International, a manufacturer of automatic test systems.

I am sure that these three highly qualified editors will help *Computer Design* serve you even better in providing the information you need, organized for your convenience. And, perhaps they will help us win a few more awards as well.

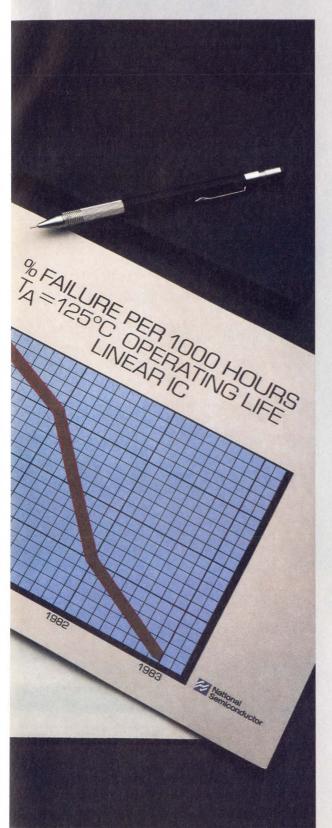
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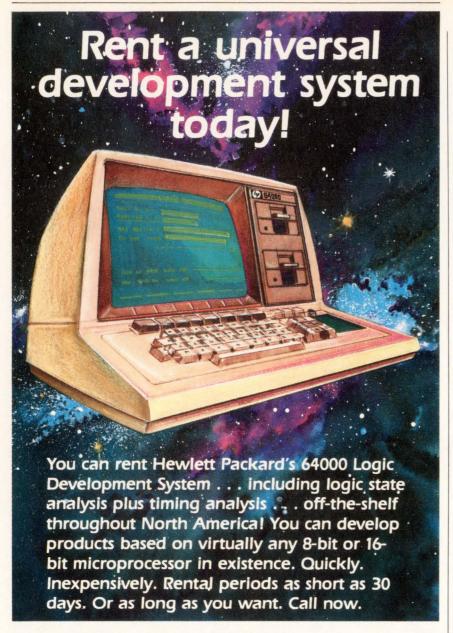
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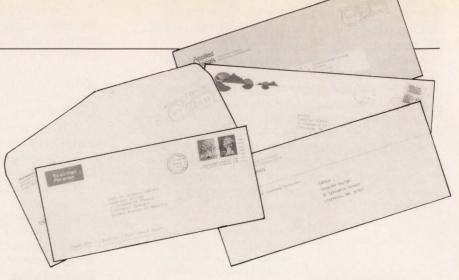
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LETTERS TO THE EDITOR

Conflicting reports and confusing data

I was puzzled by three points in "Chips Support Two Local Area Networks" by Bob Dahlberg (May 1984, p 107). First, the article refers to Intel Ethernet chips as "available," but in Up front in the same issue, availability of these chips is predicted for 1985. Second, it implies that HDLC is suitable only for short distances. Hasn't Dahlberg heard of international X.25 networking? Third, like several recent articles, it implies that the Ethernet 2.0 specification from the Digital/Intel/ Xerox consortium is compatible with the IEEE 802.3 draft standard. In reality, the first word in an Ethernet packet following the source address is a type code. In IEEE 802.3, this word is a byte count. There is no way these two protocols can interwork; the most they can do is share a cable.

Brian Carpenter CERN European Organization for Nuclear Research Geneva, Switzerland



Making it clear

Intel's 82586 LAN coprocessor is available. The 82586 went into production in December 1983. We are presently ahead of schedule and expect to ship over 300,000 82586s in 1984. The 82501 Ethernet Serial Interface is available from two sources, Intel and SEEQ.

I agree that HDLC has nothing to do with distance of transmission. The point of the article was to contrast HDLC CSMA/CD in LAN applications, not to imply that HDLC was only appropriate in LAN applications. I regret the misleading implication.

At Intel, we use the terms, Ethernet and 802.3, interchangeably. In fact, Intel is actively encouraging the standardization around the 802.3 specification; Intel products are designed to comply with 802.3. We expect that networks designed around a "Blue Book" Ethernet will not proliferate. On the issue of the type field, the 802.3 recommendation for byte count has to do with padding the frame size to ensure a minimum frame size of 64 bytes. The problem was not anticipated in the original Ethernet document.

Bob Dahlberg Intel Corp 3065 Bowers Ave Santa Clara, CA 95051

Use English, please

I enjoy Computer Design magazine and your editorials. At the same time, I deplore the manner in which engineers misuse the English language. Accordingly, I am hoping you will try and set a higher editorial standard and avoid perpetuating some of the inane jargon and some of the usage which seems to me to be destructive to the language. Some examples are: "sophisticated" applied to inanimate objects (try substituting "complicated" or "complex"); "software" for "computer program"; "model" applied to a "mathematical description"; and "algorithm" for "algorism."

Dale L. Jensen Rockwell International Corp PO Box 1183 Downey, CA 90240

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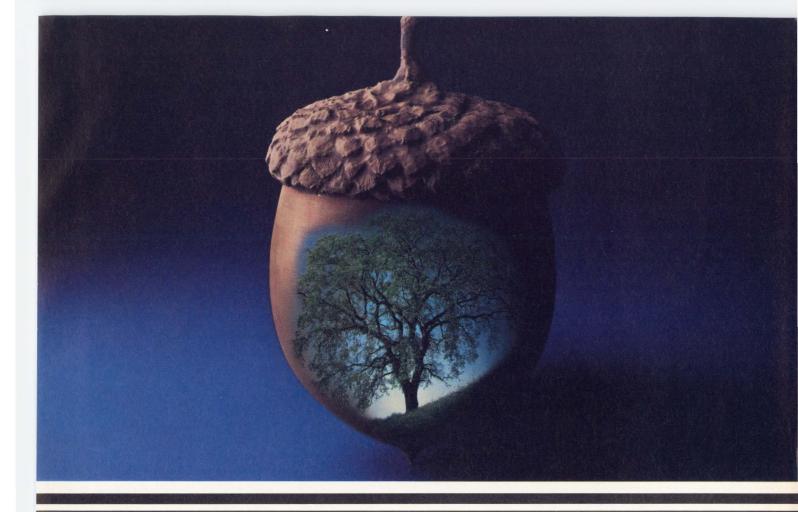
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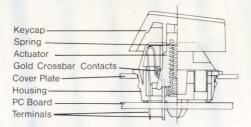
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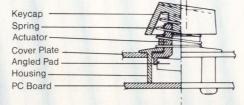
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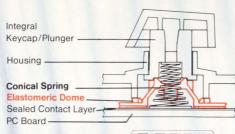
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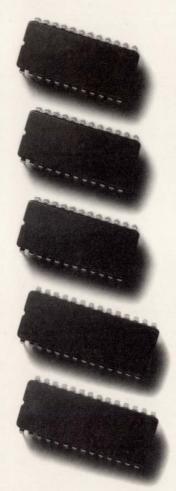
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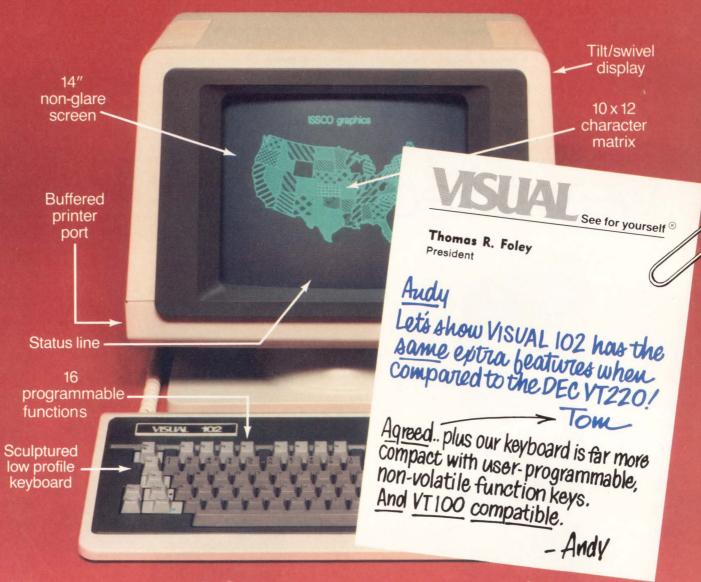
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Multi-user AT computer creates standards overnight

IBM's new "three-user" AT computer establishes several *de facto* software and hardware standards for small business computers. Like its single-user floppy disk-based PC and hard disk-based XT predecessors, the latest product (introduced in August) from the Boca Raton, Florida Entry Systems Division, will become an industry model.

The single-user floppy disk-based PC and XT are standard in the corporate environment. The AT has established the pattern for networked, multi-user, small business computers. With the AT (Model 5170), IBM has set the industry rules for what operating systems will be used, what disk sizes will be standard, how a small business network should be configured, what firms will have an early share in profits, and more.

IBM has decided that Microsoft Corp's (Bellevue, Wash) DOS-3.0 (soon to be replaced by DOS-3.1) and Xenix are the operating systems best

able to serve the one- to four-user, small business computer market in either a standalone or network mode. An Intel microprocessor will dominate this market according to IBM, just as it controls the 16-bit market for single-user machines. Moreover, IBM has indicated that broadband carrier sense multiple access/collision detection (CSMA/CD) is today's preferred local network access scheme for small business computers.

IBM has also determined what size and operating format should be standard in a megabyte range, floppy disk drive, and a 20-Mbyte hard disk. Standards for a host of lesser hardware components, including VLSI parts and memory, have also been decided (see "Personal Computer Benefits from 80286, Networking, and Software," on p 225 of this issue).

Like its predecessors, the AT (advanced technology) personal computer will be used in many capacities: as a personal productivity tool, as a

manager's desktop link to a corporate mainframe, to implement vertical business application software, and as an engineering design and development tool. It will also act as a networked file server, a software development station, and a network link to such expensive remote resources as laser printers.

Computer designers and system integrators involved in a vast variety of software or hardware projects will have to study what IBM has done with the AT and how it has done it. Engineers will have to adapt add-on printed circuit boards to the AT's backplane slots in order to increase its functions. They will also have to mold value-added packages for computer aided design, manufacturing, or engineering; backup tape drives and additional disks; and many other products to the AT. From now on, small business computer products will have to be AT-compatible and meet that machine's standards to remain competitive in the market.

Most important, IBM has continued the open architecture policy used to set up third-party software and hardware vendors for the PC and the XT. IBM offers detailed documentation to ensure proper software and hardware connections for memory or coprocessor boards. For example, a prototype adapter board comes with extensive documentation, including system interface logic diagrams. This should be of immediate interest to computer designers hoping to provide third-party AT devices.

IBM will sell a technical reference manual geared to programmers and design engineers who need to know how the AT works. It includes the functional specifications of all the AT hardware and the basic input/output system (BIOS) software so critical to interfacing AT equipment. Software developers need not be content only with the BIOS. Xenix has a set of

A peek inside

The AT is an Intel Corp (Santa Clara, Calif) 80286 microcomputer-based machine. This 130,000 transistor microprocessor, second-sourced by Advanced Micro Devices, Inc (Sunnyvale, Calif), sports a 32-bit internal architecture, a 16-bit wide external data bus. and a 24-bit address bus. The address bus allows the 6-MHz mos device to address and communicate directly with 224, or about 16 Mbytes, of RAM. In addition, the 80286 can address a 1-Gbyte virtual address space with management and protection supported by its hardware.

The 80286 runs many DOS programs in an 8086 emulation mode. This will be a major selling point for the AT in the

future, even when Xenix application programs become available. The AT's low cost and high power will encourage buyers to opt for it, even if they are not ready to run a multi-user or networked microcomputer. In fact, the AT will become the new single-user standard because of its price/performance ratio. With no other machine in its class, purchasers will use it merely as a high end personal computer.

The AT offers eight expansion slots (some occupied by such essential boards as floppy drivers), a socket for Intel's 80287 mathematics coprocessor, an 8086-compatible real address mode, as well as a protected virtual address mode.

(continued on page 28)

SYSTEM TECHNOLOGY/ MIGROPROGESSORS/MIGROGOMPUTERS

Multi-user AT

(continued from page 27)

Comparison of Xenix and Unix

Feature	Xenix	Unix
Utilities		
Bug Fixes	Microsoft and System V	System V
Shell	Microsoft and System V	System V
sccs	Microsoft and System V	System V
mm	Microsoft and some System V	System V
minor utilities	Xenix 5.0	System V
Line printer spooler	Xenix 3.0	System V
Enhanced BSD mail package	Xenix 3.x	No
Visual shell		
Communications		
VPM	No	Yes
User-configurable	Xenix 3.x	No
Machine-machine mail interconnect	(MicNet)	140
UUCP enhancements	Microsoft and System V	System V
Software development	undresert and eyetem v	System v
ANSI 77 Fortran	Optional MS-Fortran	Yes
Ratfor	No	Yes
Miscellaneous Fortran utilities	No	Yes
MS-DOS X-development libraries	Xenix 3.x	No
Software generation system	CMERGE ¹	System V
Common object format	x.out	COFF ²
C compiler extensions	Microsoft and System V	System V
Standard library improvement	Xenix 5.0	System V
Hardware independent floating point	Yes	No
Operating system improvements		
Process locking	Microsoft and System V	System V
Messages	Microsoft and System V	System V
Semaphores	Microsoft and System V	System V
Shared Memory (data)	Microsoft and System V	System V
Record and file locking	Xenix 3.0	No
IK file system	Xenix 5.0	System V
File system integrity	Xenix 3.0	System V
System administration utilities	Xenix 3.0/PC-oriented	System V/data processing-oriente
Xaction process improvement	Xenix 3.0	No
Performance improvement	Microsoft and System V	Primarily VAX-oriented
Compatibility with System III:3	PC-oriented	
Device drivers	Yes	Ne
C compiler	Yes	No
Object formats	Yes	No
Executable formats	Yes	No No
Include files	Yes	No No

¹ CMERGE refers to a C compiler developed at Microsoft. It is retargetable and generates optimized code. It is language compatible with Unix C and C Standards Committee.

² COFF, as currently defined, will not work for some processors, including the iAPX 286.

³ This refers to upward compatibility between System III, System V, Xenix 3.0, and Xenix 5.0.

software development tools that Microsoft has created.

IBM is also selling its own windowing program and associated software toolkit to allow application developers to include window facilities in their AT software. Unless it flops, the IBM Topview windows software will be the *de facto* standard—even though Microsoft and VisiCorp (San Jose, Calif) also make window software.

Multiple choices

The AT will come with two operating systems. Microsoft Corp's DOS-3.0 is geared mostly to take care of the single-user's needs in a local operating mode. It has some networking capability, however. Microsoft's DOS-3.1, scheduled for the first half of 1985, promises full networking. The firm's Unix-licensed Xenix-286 operating system, given new prestige by IBM's endorsement, accommodates the multi-user environment with AT&T (Short Hills, NJ), Berkeley, and Microsoft Unix enhancements. It is also compatible with Unix Systems III and will soon be compatible with System V.

According to Microsoft, Xenix-286 features record and file locks, semaphores to help manage multi-user/multitasking data, automatic disk recovery for better reliability, and more. It too will be available next year. For now, the AT remains a single-user machine with some network capability.

By using Xenix for its multi-user operating system, IBM has created an instant de facto operating system standard for the two- to five-user market. Even though Xenix is a licensed Unix, IBM does not consider this to be the same as an endorsement of AT&T's product. Moreover, by associating itself with Xenix, IBM retains its relationship with Microsoft. Xenix is not fundamentally limited to the three-user market. If IBM dubs it the multi-user operating system for its next 5- to 25-user personal computer, Xenix has a good chance of competing with Unix System V.

The niche IBM currently has in mind for its AT comes clear from a

look at Unix's background and the small business computer market. Unix is a minicomputer-based operating system. Typically, such machines serve 5 to 25 users and are served well by one of the many Unix derivatives. High end microcomputers will soon do the 5- to 25-user job, however. These will need a Unix version—with enhancements for commercial viability—to do the job properly. Because no one wants to write another operating system for this niche, Unix System v (or some descendant) will, however, remain dominant.

AT&T Unix will control this market segment for high end microcomputers for several reasons. The operating system is heavily promoted. It communicates with the outside world by means of AT&T private branch exchanges, digital switches, national and international voice, data and video networks (all needed by the more than five-user market). And most conclusively, there is no strong alternative. Due to these factors, IBM is gradually announcing a variety of Unixes to hook up everything—from its XT to its mainframes (Computer Design, Aug 1984, p 44). The AT already runs IBM's PC/IX singleuser Unix.

But, IBM is in no hurry to sanction the works of AT&T directly. AT offers an opportunity to avoid such an endorsement. Studies show that by far the largest share of the multi-user professional personal computer market is in the two- to five-user environment. IBM intends to offer an alterative to Unix on a machine that can accommodate Unix System v if that operating system becomes a standard.

IBM's competitors in this area, including Fortune Systems Corp (San Carlos, Calif), Durango Systems, Inc (San Jose, Calif), and Altos Computer Systems (San Jose, Calif), are nervous about the AT, even as they claim that IBM's entry will be "good for legitimizing the business." Such firms as Corvus Systems, Inc (San Jose, Calif) and 3COM Corp (Mountain View, Calif) that have been hooking personal computers to their own local networks have expressed

similar feelings since being upstaged by Big Blue.

The PC-DOS operating system software used in the PC and XT has contributed greatly to their success. Microsoft's generic MS-DOS-customized for IBM as PC-DOS—and its most recent DOS 2.1 version make it relatively easy for third-party vendors to provide a variety of software and hardware enhancements. But IBM might end its dependence on the Microsoft software. Some industry gurus believe IBM is working on its own next version of the PC's PC-DOS operating system. Moreover, IBM will introduce a version of its proprietary VM operating system for the AT. For the near and intermediate term, however, IBM will use Microsoft's own DOS-3.0 and DOS-3.1, repectively. And, as IBM itself puts it, many existing DOS programs (including DOS-2.1) will run "unchanged" on the AT with DOS-3.0.

Among its other chores, DOS-3.0 will drive the AT's 320/360-Kbyte floppy, 1.2-Mbyte floppy, and 20-Mbyte hard disk. The AT can be configured for up to 41.2 Mbytes of auxiliary memory. For full networking, however, the industry must wait for the DOS-3.1. Microsoft has said that the DOS will provide multitasking and networking capabilities; in the past, however, the firm had insisted that DOS would not handle a multi-user environment.

Doing windows

The DOS-3.0, using 36 Kbits of RAM, also allows implementation of a virtual disk. This enables the AT user to access RAM above the 640-Kbyte limit allowed by the PC or XT. Moreover, it will be able to supply data and programs to IBM's Topview that currently handles a singleuser, multitasking environment. Nevertheless, it is likely that Topview will soon allow both DOS and Xenix applications to display windows on the same screen.

That IBM has taken this route—ignoring other vendors' windows—indicates its willingness to get directly involved in the personal computer (continued on page 30)

Multi-user AT

(continued from page 29)

software business and establish standards in this domain. Topview will compete with the Apple (Cupertino, Calif) Macintosh's computer programming toolkit for the attention of third-party software developers. These third-party programmers may well opt for the IBM route to success rather than the iffy Macintosh road, given the latter's comparatively closed architecture and operating system.

As mentioned, Microsoft's DOS-3.0 or 3.1 could ultimately be upstaged by an IBM DOS. For example, the IBM 80286 is quite capable of running another DOS-like operating system in its 8086 emulation mode. It can also run the Berkeley 4.2 BSD Unix version or the Unix System v. While IBM is not likely to rush to endorse its archrival's product, another company might. For example, Digital Research, Inc. (Pacific Grove, Calif) is already

porting System V to the 80286 with AT&T and Intel. Digital is also likely to make its Concurrent DOS available for the AT. Clearly, the AT will be as important to future operating systems as it is to those it already runs.

IBM has not announced an operating system that handles single users, multiple users, and networking simultaneously. Such an operating system could combine the features of both a DOS-like and Unix-like operating system, and handle a variety of application programs. This kind of operating system is a logical next step as the market grows in sophistication, however. Obviously, an AT user cannot run two operating systems at the same time. IBM will have to solve this problem with a proprietary system, probably to appear in a machine geared to more than five users.

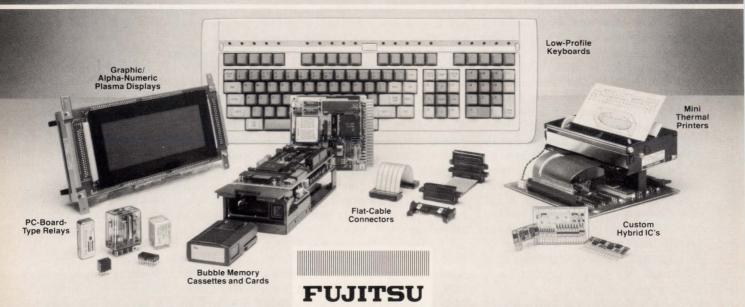
There is yet another operating system scenario. Suppose either Micro-

soft or IBM, eschewing both Unix and Xenix, develops a powerful networking version of DOS. This new DOS would have to handle multiusers, multitasking, file and print serving, multi-user file management (lots of bookkeeping), and more. Such an operating system (to be like Unix in structure, even as Microsoft says its DOS is becoming more like Unix now) would not owe any license fees to AT&T. It would be palatable to IBM's tastes for the two- to fiveuser machine's networks. Microsoft could then concentrate on Xenix as a competitor to Unix for the 5- to 25-user market, possibly with encouragement from IBM.

Disk madness

IBM has settled the question of how many megabytes a small business computer's floppy disk should have. Its choice of half-height, 1.2-Mbyte

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(1.6-Mbyte unformatted), 51/4-in. floppies establishes this size as the standard, ending a long-standing industry controversy. Both original equipment manufacturers and disk drive manufacturers will grab onto the new standard size. Adopting this standard will present few problems since they will be able to continue using a well-defined IBM-originated standard design.

IBM has settled several other dilemmas. For example, it chose 360 rpm for drive speed and 96 for the number of tracks/in. (the AT reads and writes on the PC and XT's 48-track/in. media, however). By setting up the AT to support 300 and 500 Kbit/s, it established the data transfer rate. IBM will not say who makes its drives (it has a variety of suppliers), but inside two machines are drives were "Made in Japan" labels.

A variety of other hardware standards have been set by IBM's AT. For example, it uses 128-Kbit x 1 dynamic RAMs. One opened AT showed Mostek, Inc. (Carrollton, Tex) RAMs. In the chip domain, IBM offers the Intel 80287 mathematics coprocessor, which complies with the IEEE proposed standard for floating point arithmetic. This 4-MHz clock speed chip has an 8087 mode for coprocessing with the 8086 mode of the 80286 and a coprocessing mode for the 80286. The chip will speed numeric calculations for 8086 or 80286 application programs. Finally, IBM has defined the attributes of a halfheight 20-Mbyte hard disk drive such as a transfer rate of 5-Mbit/s and a speed of 3573 rpm.

Hook them up

IBM has put Sytek, Inc (Mountain View, Calif) on the map overnight.

The small networking company offers a version of the International Standards Organization's (ISO) seven layer model for computer communications that is adaptable to such personal computer networks as IBM's. Layers one through five (from the physical through the session layer) are included in Sytek's implementation of a 2-Mbit/s (CSMA/CD) network. In effect, IBM has opted for the ISO model as a standard for personal computer networks-even though IBM is nowhere near giving up its Systems Network Architecture model for large scale computers.

The ISO model-based network hooks up all of IBM's personal computers with a 75- Ω coaxial cable that handles data other than personal computer data. For example, it will accommodate voice and video. The small capacity version of the network

(continued on page 33)

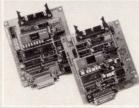
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Never has so much memory offered so many advantages in so many ways.

Fujitsu's custom bubble memories offer maintenance-free operation, card expandability to 4 megabits, access time 4 times faster than competitive bubbles and 10 times faster than floppy discs, ambient temperatures from 0°C to +50°C (case temperatures from 0°C to +70°C) and a non-volatile memory that generates without a seed bubble.

What's more, tough Fujitsu cassettes go



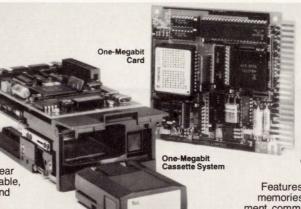
Adapter FBM-A003 (left) interfaces with GPIB; Adapter FBM-A002 with RS232C.

where discs fear to tread. Portable, detachable and magnetically shielded, they shrug off shock, vibration, dirt, oil, and chemicals.

And now, the new adapters shown in

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the inset interface the 1-megabit cassette and the 4-megabit card to both RS232C and GPIB (IEEE 488).

Also you can now order a 1-megabit, single power source (+5v) cassette system. This new unit has a built-in power-fail signal, which prevents loss of data in the memory. Its internal circuitry also provides for +12v and -12v power sources.

Finally, you can order a new 4" x 4" 1-megabit bubble memory card and card kit. The assembled card plugs into a standard card-edge connector.

Features like these make Fujitsu custom bubble memories ideal for test and measurement equipment, communication systems and data processing.

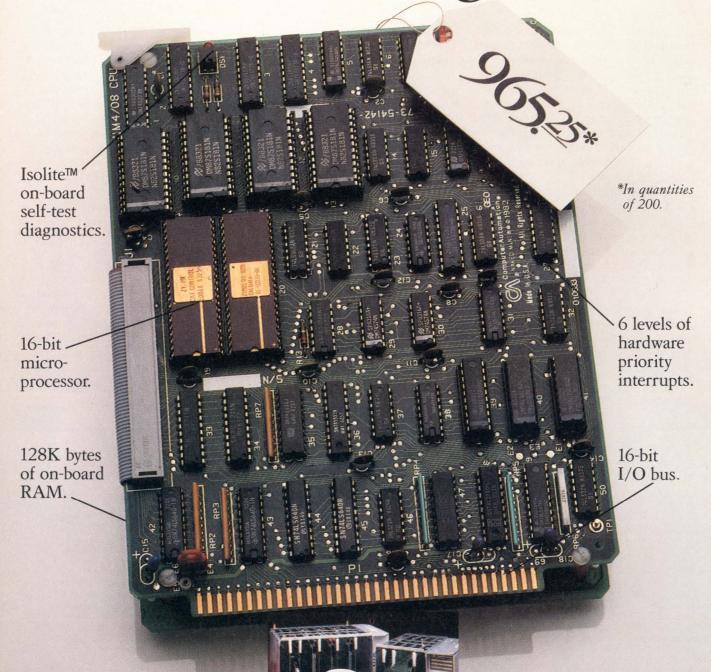
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CIRCLE 17

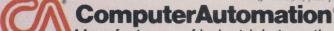
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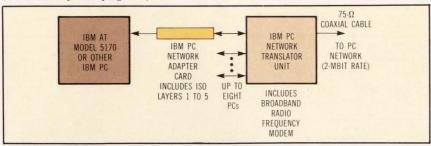
CIRCLE 18



Manufacturers of industrial strength, low cost minicomputers for 16 years.

SYSTEM TECHNOLOGY/ MIGROPROGESSORS/MIGROGOMPUTERS

Multi-user AT (continued from page 31)



Sytek, Inc's broadband local network for all IBM personal computers, except the Jr, is served by a carrier sense multiple access/collision detection access scheme. The expandable network handles a variety of signals on its 250-Kbyte/s transmissions.

can be installed by users. Large networks need professional channel tuning and installation for their frequency divison multiplexing, broadband radio frequency modems. Frequency division multiplexing and broadband are the technology standards with which designers will have to comply when interfacing with the IBM personal computer network.

A printed circuit board that connects any IBM personal computer to the network contains a ROM-based network BIOS. To keep the hookup price low, the board also has an Intel 82586 coprocessor VLSI-based CSMA/ CD interface chip. This chip implements the ISO layer two (data link) network connections. It replaces a fistful of SSI and MSI parts and establishes yet another hardware component standard. IBM did not opt for Intel's iNA 960 Transport/Network Manager software; instead it took the Sytek version of this software for layers three through five. Intel's 82501 Manchester encoder/ decoder is not used because it is geared to 10-Mbyte network operations-the personal computer network features 250-Kbyte (2-Mbit) transmissions.

IBM has said that it will make a token-passing network available for its backbone, high capacity link in the wired building, campus, and other areas. It will have subnetworks that attach to its main networks. The ISO standards token-passing factory network, shown at the recent National Computer Conference in Las Vegas, is one such subnetwork (see Computer Design, June 15, 1984, p 64). Although the Sytek network for personal computers does not perform

token-passing, it can interface with token-passing networks by means of bridges and gateways. IBM says it plans to take this approach to link disparate local networks to its network backbone (when the main network becomes available) in two to three years.

The personal computer network's broadband capabilities allow it to handle a variety of voice, video, and certain other services that baseband Ethernet CSMA/CD cannot. This is

the secret to another of IBM's clever uses of the Sytek network. It is true that in its personal computer local network IBM has given nominal support to the ISO. Now, however, IBM offers a standards-based alternative to Ethernet, backed by its office equipment competitor—Xerox (Dallas, Tex). Moreover, IBM has the potential to offer a voice alternative to AT&T's private branch exchange, as well as another option in the undeveloped market for such video conferencing services as AT&T sells.

Whether IBM will offer an alternative to the Sytek approach—one that allows other vendor's equipment to be hooked up-remains to be seen. Certainly, Sytek stands ready to do it. In any case, IBM will not come up with a direct token-passing network for personal computers since it feels the Sytek network does the job just fine.

> -Harvey J. Hindin. Special Features Editor SYSTEM TECHNOLOGY (continued on page 38)



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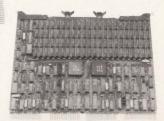


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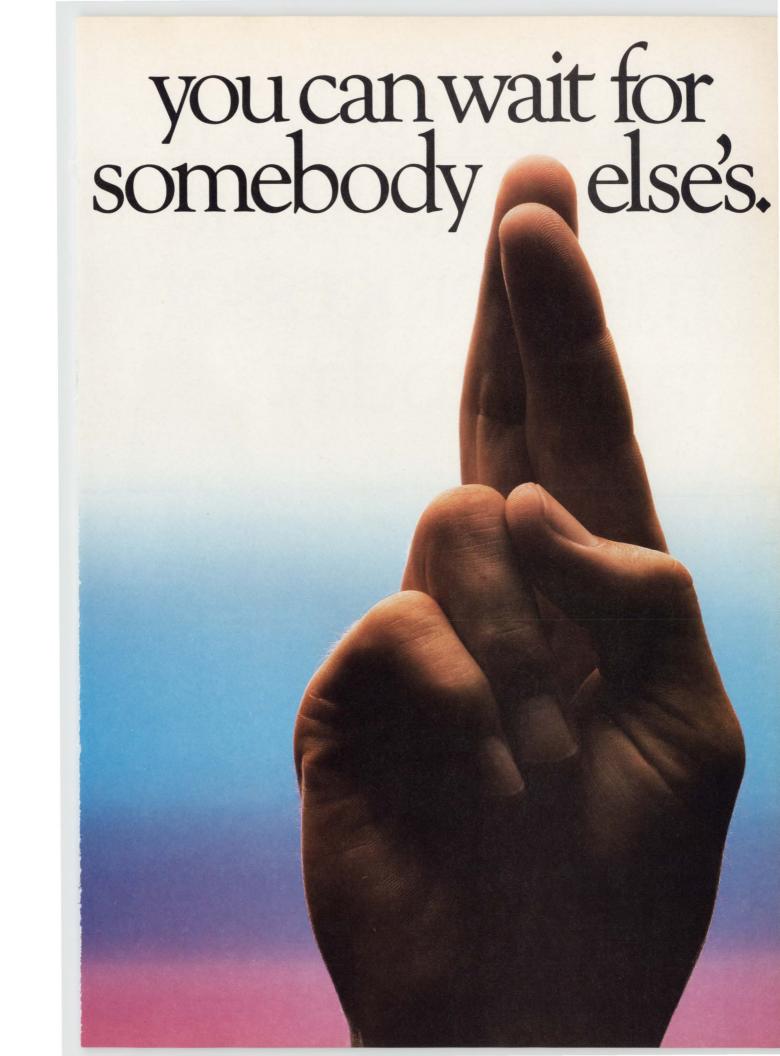
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CIRCLE 20

Silicon handles arbitration and message interrupts on Multibus II

The recently introduced Multibus II architecture incorporates a total of five bus specifications—two of them carried over from the earlier Multibus I definition. In addition to the multichannel DMA I/O bus and the iSBX I/O expansion bus from Multibus I, Multibus II includes a local bus extension for connecting multiple physical boards that appear to the system as a single "virtual" board. It also has a serial system bus for low cost interprocessor communication.

The fifth bus in Multibus II is the parallel system bus (iPSB). This bus supports four address spaces: a 32-bit memory address space, an 8-bit message address range, 16 bits of interconnect addressing, and 16 bits of memory-mapped I/O address. It is most useful for high performance systems that take advantage of its burst transfer capability, which yields a sustained bandwidth of 40 Mbytes/s.

The Multibus II specification supports a bus arbitration protocol and message passing. Message passing allows block transfers between two boards on the system having local CPUs (bus agents) without worrying about memory management. The bus arbitration protocol allows bus agents

to arbitrate among themselves for ownership of the bus without going through a central arbitrator. Intel Corp has now introduced two ICs to implement message handling and bus arbitration. Thus, the ICs reduce component count and speed development of systems using Multibus II.

The 84110 bus arbiter controller (BAC) and the 84120 message interrupt controller (MIC) work together or separately to off-load tasks from the local CPU. They monitor the address stream for messages, generate the needed interrupts, and arbitrate requests for control of the parallel bus. When initiating a message, the local CPU and the MIC both go through the BAC to get to the iPSB.

To control arbitration

The 84110 BAC has three basic interfaces. One interface is to the iPSB, the second is to the local environment on the host board. This interface consists of two ports: one to the local CPU and one to the MIC. A third interface is a register interface to three 5-bit registers: the arbitration ID register, the slot ID register, and the error status register. The slot ID tells the system what kind of board

is in a given slot, while the arbitration ID determines that board's relative priority in arbitrating for bus control

The error status register uses 1 bit to signal a bus error and 1 bit for a time-out error. Its remaining 3 bits represent various types of agent errors. The local CPU can monitor this register and decide what to do in different error conditions.

The slot ID and the arbitration ID are loaded into the registers of each BAC in the system from a backplane board known as the central services module. This is done on power-up or system reset. After that, all arbitration takes place only among those BACs that have requested the bus at the same time.

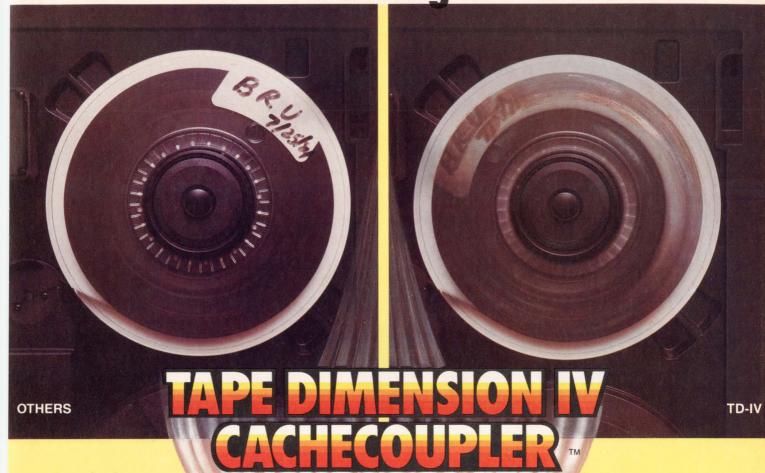
On the other side, the components on each board (CPU, MIC, memory, etc) are decoupled from the arbitration process. When the processor wants the bus, it merely toggles the BAC with a request. The BAC then either occupies the bus (if it is not currently owned by another agent) or arbitrates for it. When it has control of the bus, it signals the CPU via its GRANT line. The transfer cycle can then take place. Likewise, the bus request could have come from the MIC. In this case, the GRANT line would have signaled the CPU that the transfer cycle could begin.

The BAC supports two forms of priority-normal and high. Normal priority is based on the arbitration IDs assigned by the central services module at system initialization. High priority is asserted when a bus agent needs to override arbitration and gain immediate access to the bus. Of the six arbitration lines from the BAC to the iPSB, ARB 0 to ARB 4 represent the arbitration ID stored in the 5-bit arbitration ID register. When ARB 5 (an additional signal) is asserted, it invokes high priority.

MULTICHANNEL DMA BUS iSBX BUS In the Multibus II architecture, the 40-Mbyte/s parallel system bus (iPSB) is MEMORY I/O CONTROLLER the main system bus. The bus arbiter controller and the message interrupt controller provide standard arbitration and message iPSB BUS support. iSSB BUS

(continued on page 40)

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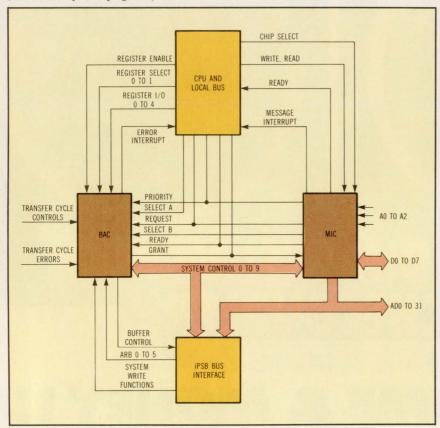
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CIRCLE 42



Silicon and Multibus II (continued from page 38)



In this typical arrangement of a bus arbiter controller (BAC) and a message interrupt controller (MIC) on a bus agent, both the CPU and the MIC share the priority and the grant line to the BAC. The arbitration lines to the iPSB (ARB 0 to 5) signal the agent's priority in the arbitration protocol. Assertion of ARB 5 almost guarantees instant bus ownership.

To gain control of the bus, new bus agents must first sense that the bus request line, BREQ*, is inactive and that other agents are not currently arbitrating for control of the bus. If they are, the requesting agent must wait until all those currently contending have had their turn before another set can vie for control. As each agent is serviced, it stops driving BREQ*, which is an OR-tied signal. When the last agent begins to be serviced, the signal becomes inactive.

When the BAC senses an inactive BREQ*, it drives its arbitration ID onto the bus. It then compares the ID on the bus with its own ID. If a higher priority ID has been driven onto the bus at the same time, the high order bit will not match and the higher priority will get control. When that is done, a new comparison is made. Assertion of ARB 5 overrides arbitration, except in rare cases where two agents have asserted priority at the same time and must then arbitrate among themselves.

Since every board can potentially signal high priority, application programs can be flexible. For the same reason, any given bus agent can potentially be used for critical functions. In addition, it is possible for software—either the application program or the operating system-to alter the arbitration IDs dynamically. Thus, it is possible to globally reconfigure the system for a different application set without resetting it. It is also possible to introduce a new board to a running system. Note that arbitration IDs can be altered dynam-

ically, but slot IDs cannot. This enables such errors as duplicate arbitration IDs to be introduced, so caution is advised.

To control interruptions

Like the BAC, the MIC has three interfaces: to the iPSB, to the local CPU, and to the 84110 BAC. Via its local CPU interface, the MIC behaves like a slave I/O port. The CPU can set its control and output message commands, as well as receive source and status information on incoming interrupts. The MIC contains both transmit and receive first in, first out registers, which contain addresses for queued message packets.

The MIC's interface to the parallel bus allows it to act as both a requesting and a replying agent on the bus. As a replying agent, it monitors the iPSB's 16-bit message space. If it finds a destination address in the space that maps to its host CPU, it replies and handshakes with the bus via the BAC. It then stores the message information and signals its CPU via an interrupt line. It may do this directly or via an interrupt controller suitable to whatever CPU is involved.

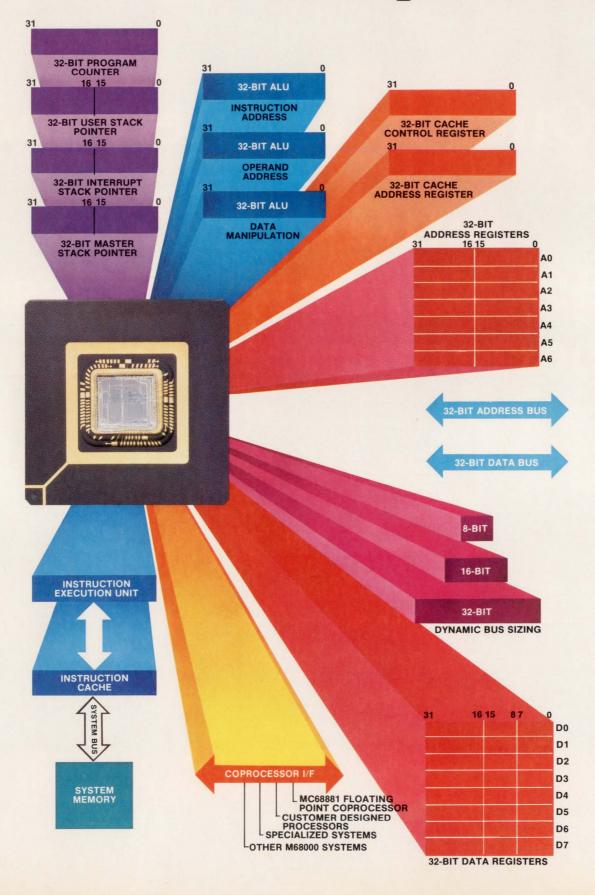
The MIC can also be a requesting agent. To transfer messages generated by the CPU, it activates its own request line to the BAC. When the BAC returns a GRANT signal, it performs the Multibus II unsolicited message protocol by driving its address onto the message address space of the iPSB. The interface to the BAC includes a priority line so the CPU can tell the MIC it has a priority message. The MIC, in turn, can request the BAC to assert high priority for immediate bus ownership. Unsolicited messages can be up to 32 bytes long. Since both the 84110 BAC and the 84120 MIC are processor independent like Multibus II itself, they interface to the normal address, data, and control lines of popular microprocessors.

> -Tom Williams, West Coast Managing Editor SYSTEM TECHNOLOGY (continued on page 44)

Once in a generation:

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new system with the MC68020: microprocessor.

The new performance standard.

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No other 32-bit MPU makes this extensive a leap in performance improvement. At 16.67 MHz the MC68020 typically runs at 2.5 MIPS for integer processing. MIPS rates several times typical are achievable in dedicated 32-bit applications.

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The MC68020 creates opportunities you've never had before--opportunities to unleash the full potential in your 32-bit MPU-based systems because it sets the standard for 32-bit microprocessors. And, because it's the first complete 32-bit microprocessor available, more than just a 16-bit design on a data bus stretched to 32 bits. A detailed look at the architecture reveals this totality.

A fully compatible M68000 Family member.

Yes, the MC68020 has features new to the M68000 Family to maximize its true 32-bit capabilities.

Yes, it's an all new design built with advanced, highly manufacturable HCMOS technology.

And, yes, it's a fully-compatible member of the M68000 Family of MPUs and peripherals. All user object code written for previous M68000 Family MPUs executes without revision. In fact, MC68020 enhancements allow it to run more than three times faster.

Family compatibility is further enhanced by dynamic bus sizing, which supports the use of 8-, 16- and 32-bit ports in 68020-based systems. In fact, the MC68020 can be used in existing 8- or 16-bit systems.

New features enhance 32-bit architecture.

The MC68020 design is new, however its architecture is based on the proven M68000 Family 32-bit register set. And, the MC68020 is highly enhanced.

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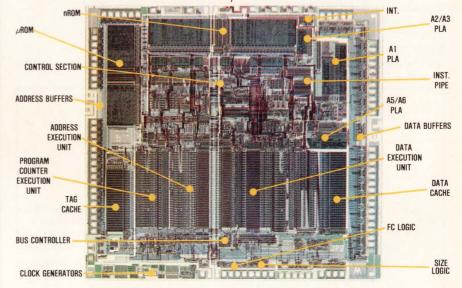
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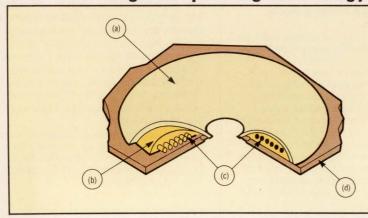
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Low cost magnetic printing technology uses thin-film heads



In a magnetic head element, the top pole structure (a) covers magnetic material (b), which surrounds the coil structure (c). The flux lines pass through the substrate (d) onto the drum instead of off the edge, as in traditional techniques.

A new magnetic printing technology uses standard copier toner, a low cost, compliant rotating drum, and thin-film magnetic heads to record latent images. Reproductions can also be made offline. The technology

centers around a newly developed thin-film magnetic head.

The head, developed by Ferix Corp (Fremont, Calif), has a 16 x 8 array of magnetic head elements. These elements produce 240 dots/in. The

elements transfer their magnetic flux through the head substrate onto an oxide-coated drum. A crucial part of the head design is that the dot elements do not interfere with one another.

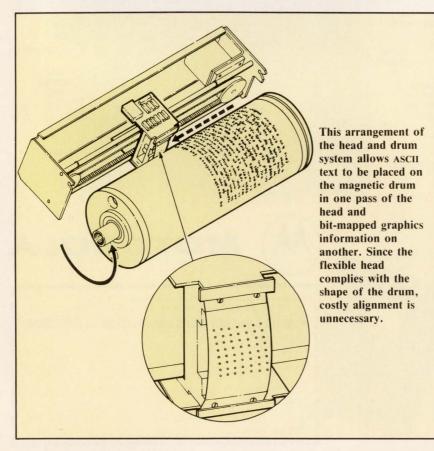
An "inside out" head architecture eliminates interference. It replaces the traditional ring core magnetic head with a design that has an internal coil structure surrounded by magnetic material. This half toroid shape has a circular gap near the center of the element. The lines of magnetic flux group around that gap and penetrate the underlying substrate. The substrate itself is in contact with the oxide coating on the surface of the rotating drum.

Lightweight and flexible

The head is a piece of flexible material and the array of dot elements is staggered for increased density. The drum is also a lightweight cardboard material with an oxide coating much like that used in floppy disks. Since both drum and head are compliant, neither needs to be as precisely machined as laser printers, for example, which require very exacting optics.

The heads are manufactured using a wet chemistry process that takes six days to complete. The design, with

(continued on page 47)



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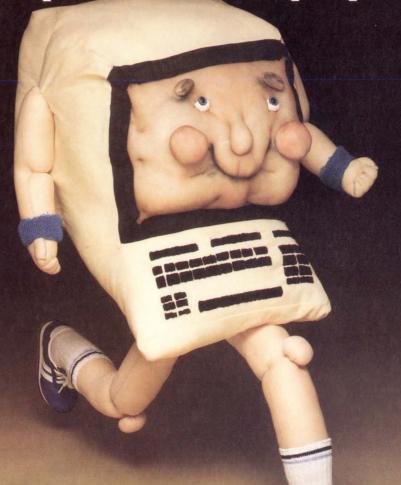
One of the best measures of the Alpha 10H's true OEM height is in the versatility it allows you to design into your system. Our highly reliable, easily transportable and absolutely interchangeable 10-megabyte cartridges mean the sky's the limit on system capacity in applications as diverse as system control and monitoring, office information and word processing, and industrial instrumentation, among others. So is convenience. Be it loading large and complex data bases, or the rapid, reliable backup of system data, the Alpha 10H simply cannot be topped. Lastly, in low cost per megabyte, no storage device, fixed or floppy, stacks up.

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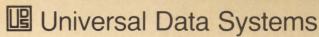


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Magnetic printing technology

(continued from page 44)

coils and circuit paths on the flexible strip, will, according to Ferix, lend itself to future integration with custom LSI circuits. Since the heads are produced using a mask process, new masks can be generated to provide different pixel density and size combinations. Another property of the head material is that the substrate is extremely hard. Thus, it can be used in contract recording without concern for the tolerance associated with flying heads.

The magnetic printing technique has another inherent property. The heads transfer a magnetic image that remains on the drum until it is erased or changed by another pass of the head. Thus, an image, once put on the head, can be used to print any number of copies of a page offline. Copies are made much faster than if actual data were transferred for each copy—even from an internal offline buffer. In addition, images can be overlayed. One pass can be used to deposit ASCII text, and another for bit-mapped graphics.

Multiple images

Ferix is introducing its new technology in the form of an office page printer that can print 10 pages/min as duplicates. In the Model 800 page printer, the head moves on a shuttle across the drum via a stepper motor. Up to three lines can be imaged on each revolution. The head array is then stepped during a built-in dead time.

When the image is complete, the drum receives dry toner. Paper is then passed against the drum and the electrostatically charged toner is transferred to the paper. The copy then passes through a fuser as in Xerography.

The page printer can store six ROM font cartridges. Each cartridge holds one to four fonts—for a total of 24 fonts online. There is also RAM area for downloading fonts from the host. Ram storage for bit-mapped graphics allows the printer to handle images and such things as signatures up to its 240- x 240-dot/in. resolution.

Cost of the page printer is expected to be \$2000 to \$3000 in original

equipment manufacturer quantities, with an end-user price of about \$5000. Ferix has also indicated that the technology will serve as a basis for a whole family of printer prod-

ucts, and that the company is prepared to license the technology for specialized areas.

> —Tom Williams, West Coast Managing Editor



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8Kx8—The cost and space saver. This newest member of the INMOS 64K DRAM family, available in a plastic package, offers access times of 120 and 150ns. The by-8 organization is a natural for microprocessor designs and other applications that require word width rather than memory depth...in process controllers, intelligent terminals, and buffer memories for example. And its pin 1 refresh makes it a very attractive alternative to 8K x 8 static RAMs. Because it combines low power and low cost with minimal support circuitry.

16K x 4 — The performance chip. With 100, 120, and 150ns access times, this organization makes a lot of sense in high-performance systems, such as high-resolution graphics, where high data rates are required. Packaged in plastic DIPs, the IMS2620 also gives you the right combination of cost, organization, and speed for microprocessor systems, terminals, and even arcade and home games. If you're upgrading from 16K x 1 chips, it provides a factor of four reduction in chip count. And its "CAS before RAS" refresh assist function minimizes required support circuitry for cost and space savings.

64K x1—The big-system choice. This DRAM also gives you a choice of 100, 120, and 150ns access times. What's more, it includes "Nibble Mode," which allows effective cycle times below 85ns. Available in a variety of packages, including plastic DIPs, ceramic DIPs, and chip carriers, it's ideal for systems requiring lots of memory depth.

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Organization	Access Time (ns)	Cycle Time (ns)	Part No.
8Kx8	120	190	IMS2630-12
	150	240	IMS2630-15
16Kx4	100	160	IMS2620-10
	120	190	IMS2620-12
	150	240	IMS2620-15
64Kx1	100	160	IMS2600-10
	120	190	IMS2600-12
	150	230	IMS2600-15

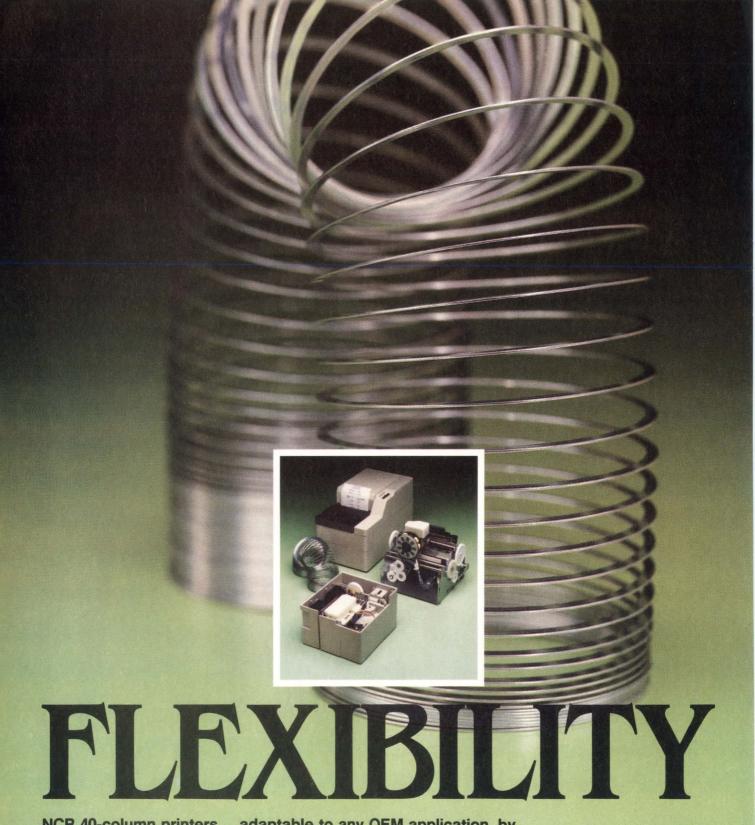
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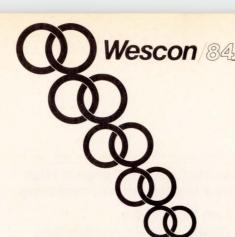




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Electronic Show and Convention

Anaheim Convention Center October 30 to November 2

The IEEE's year-long centennial celebration is about to move west. Wescon/84 will be the culmination of the year's major special events that started with Electro in Boston last May.

Since 1984 is an even year, Wescon/84 will be held in Anaheim, California, rather than in San Francisco, with which it alternates. Because of its size, this year's conference will be held in the Anaheim Convention Center. Conference dates are Tuesday, October 30 through Friday, November 2.

This also marks a separation of Wescon from Mini/Micro for the first time. In past years, Wescon and Mini/Micro West were held concurrently. Now, Mini/Micro West has been rescheduled for February of 1985. (This does not affect concurrent schedules for East, Southeast, Midwest, and Northwest Mini/Micro conferences—at least at this time.)

A particularly strong professional program has been set up for Wescon/84. Most of the 37 technical sessions are of primary interest to design engineers. Many are aimed at helping such persons solve their design problems. Subjects vary from software trends to local area networks, from microprocessor development to electronic packaging, from new concepts in VLSI design to modular automatic test equipment. Sessions of the professional program will take place from Tuesday through Friday from 10:00 am to 4:30 pm. Exhibit hours will be from 9:00 am through 5:00 pm.

As usual for major IEEE conferences, Wescon/84 will offer a series of paid tutorials. The range of subjects vary but again several offer potential value to design engineers. All are full-day in length (9:30 am to 5:00 pm), with two on each of the conference days. Some interesting titles include "Systematic Design of Microcomputer Software," on Tuesday; and "Project Management: For Small to Medium Projects and Subprojects," on Wednesday. Of equal potential are "Computer Aided Design and Computer Aided Manufacturing" plus "Introduction to Robotics," on Thursday; and "Flexible Manufacturing Systems" and

"Grounding and Shielding Electrical Instrumentation," on Friday. The fee for each tutorial is \$175.

The program for Executive Day—Thursday—contains both the keynote luncheon and a centennial banquet. Keynote luncheon speaker will be John G. Stoessinger, a Cox distinguished professor of international affairs with Trinity University's Political Science Department in San Antonio, Texas. His working title will be "Can Peace Survive the Eighties?" and the emphasis will be on geopolitics.

In a telephone discussion, Dr Stoessinger said that the details of his address will likely be modified, depending on current events at Wescon time. However, he will cover "various flash points of international affairs as they pertain to Wescon attendees and the electronics industry in general."

The keynote luncheon will be held at the Marriott Hotel, from 12:00 noon to 2:00 pm. A fee of \$25 will be charged. Advance registration is recommended.

Ray Bradbury, long known for his unique presentation of science fiction, will be the featured speaker at Thursday's centennial banquet. Actually a social event, the banquet will be held from 7:00 pm to 12:00 midnight at the Doubletree Hotel. It will be a black tie occasion, with the dinner preceded by a cocktail hour. A big band style orchestra will play during cocktails and for dancing after dinner. Tickets are priced at \$45 each and may be ordered in advance.—*S.F.S.*

Wescon/84 is sponsored by the Los Angeles and San Francisco Bay Area Councils of the IEEE. For further information, contact Wescon/84, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965.

(conference coverage continued on page 52)

(continued from page 51)

Professional Program Excerpts*

Session 1: Software Trends for CAD/CAE Workstations, or How to Prepare Software Now for the Future of Workstations

Tues Oct 30, 10 am to 12:30 pm

Chair: M. J. Ashley, American Microsystems, Inc, Santa Clara, Calif

1/1 "Layout Verification and Workstations"
W. S. Goerke, ECAD, Santa Clara, Calif

1/2 "Workstations—A Passing Fad?"
R. Kirk, American Microsystems Inc, Santa Clara, Calif

1/3 "Personal Computer Software IncreasesEngineering Access to CAD Tools"T. A. Zimmerman, Future Net Corp, Canoga Park,

Calif

1/4 "Software Trends for CAD/CAE Workstations—
A PC-based CAD/CAE Workstation"

A. K. Hung, Personal CAD Systems, Inc, Los Gatos, Calif

1/5 "User Extensible and Portable CAE Software for ic and PC Design"

S. Sapiro, CAE Systems, Sunnyvale, Calif

Session 2: Towards a Complete Fiber Optic LAN—Part 1: The System Issues

Tues Oct 30, 10 am to 12:30 pm

Chair: S. P. Joshi, Advanced Micro Devices, Sunnyvale, Calif

2/0 "Session Overview"

S. Joshi, Advanced Micro Devices, Sunnyvale, Calif

2/1 "An Overview of FDDI"

K. Moulton, Sperry Corp, Blue Bell, Pa

2/2 "Enhancing Local Workstation Capability and Performance With Mainframe Services Via High Speed LAN"

B. J. Milander, IBM, Research Div, San Jose, Calif

2/3 "High Performance LAN Applications"L. Green, Communication Machinery Corp, Santa Barbara, Calif

2/4 "Streamlining Protocol at High Data Rates"
V. Iyer and S. Joshi, Advanced Micro Devices, Sunnyvale, Calif

2/5 "Fourth-Generation PABX Applications Using FDDI"
E. O. Rigsbee III, cxc Corp, Irvine, Calif

Session 4: New Technologies Impact High Speed Digital Signal Processing

Tues Oct 30, 10 am to 12:30 pm

Chair: J. Haight, GigaBit Logic Inc, Newbury Park, Calif

4/1 "New cmos Multiplier-Accumulator Eliminates 1/0 Bottleneck"

Dr. J. Eldon, TRW, LSI Products Div, La Jolla, Calif

4/2 "Digital Gallium Arsenide: A Laboratory Technology Comes of Age"

R. M. Hickling, GigaBit Logic Inc, Newbury Park, Calif

4/3 "Bipolar & CMOS Technologies Become Partners in Digital Signal Processing"

R. M. Perlman, Advanced Micro Devices, Sunnyvale,

4/4 "CMOS DSP with Muscle"

G. Ramachandran, Fujitsu Microelectronics, Inc, Santa CLara, Calif

4/5 "смоѕ Word Slice Architectures Speed Signal Processing"

P. Toldalagi, DSP Div, Analog Devices, Inc, Norwood, Mass

4/6 "A Data Flow Architecture For Digital Image Processing"

Y. Chong, NEC, Natick, Mass

Session 5: Thirty-two-bit Microprocessor Product Development

Tues Oct 30, 10 am to 12:30 pm

Chair: S. K. Skoog, NCR Microelectronics, Colorado Springs, Colo

5/1 "Product Development for the MC68020"

B. Beims, Motorola Inc, Austin, Tex

5/2 "The Impact of External Microprogrammability on Firmware Development"

J. S. Beekley, NCR Microelectronics, Colorado Springs, Colo

5/3 "NS32032 Family Support Tools"

R. Mateosian, National Semiconductor, Santa Clara, Calif

5/4 "Hardware and Software Development System for 32-bit CPU and MMU with Internal Cache" W. A. Stubblebine and R. A. Rango, Bell Laboratories, Holmdel, NJ

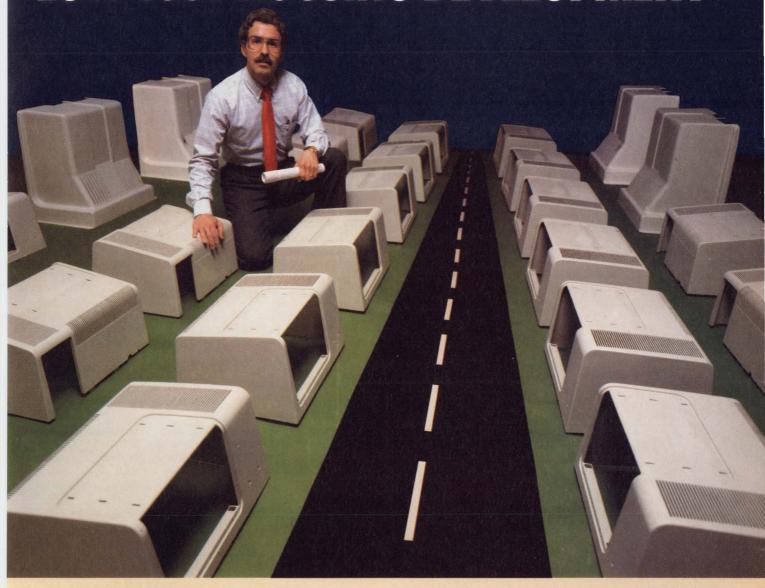
5/5 "Z80,000 Product Development Support" R. G. Andrews, Zilog, Campbell, Calif

5/6 "Thirty-two-bit Development Systems: A One-Board Approach"K. Peterson and C. Delise, Digital Equipment Corp,

Hudson, Mass

^{*}Based on information available at press time. Subject to change.

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(continued from page 52)

Session 6: Turning Personal Computers Into Professional CAE/CAD/CAM Tools

Tues Oct 30, 2 pm to 4:30 pm

Chair: D. M. Laughlin, Personal CAD Systems, Inc., Los Gatos, Calif

6/1 "The PC-Personal Computer, or Design Tool?" D. M. Laughlin, and C.-S. Horng, Electronic Design Automation Div, Personal CAD Systems, Inc, Los Gatos, Calif

6/2 "Integrating Personal Computer Tools Into a Systems Environment"

J. Willner, Hughes Aircraft, Fullerton, Calif

6/3 "Microcomputer-based Solid Modeling Systems" S. Crane, Cubicomp, Berkeley, Calif

6/4 "PC-based Instrumentation Merges With CAE" J. E. Fischer, Northwest Instrument Systems, Beaverton, Ore

Session 7: Towards a Complete Fiber Optic LAN-Part II: The Hardware Issues

Tues Oct 30, 2 pm to 4:30 pm

Chair: S. P. Joshi, Backend Networks, Advanced Micro Devices, Sunnyvale, Calif

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7/0 "Session Overview"

S. P. Joshi, Backend Networks, Advanced Micro Devices, Sunnyvale, Calif

7/1 "Fiber Optic Transceiver Design for High Speed Local Area Networks'

I. Ohel, Optical Communication Div, Hewlett-Packard, Palo Alto, Calif

7/2 "Media Trade-offs for FDDI Applications"

D. Charlton and K. Murphy, Telecommunications Products Div, Corning Glass Works, Corning, NY

7/3 "Fiber Optic Cable Design for LANS"

T. P. Huegerich, Siecor Corp, Hickory, NC

7/4 "Optical Bypass Issues in Fiber LANS" T. Odderstol, Frequency Control Products, Woodside, NY

7/5 "Power Budget Considerations for Ring Networks"

J. McDonnell, Motorola, Inc, Phoenix, Ariz

Session 9: VLSI Alternatives in Digital Signal Processing: Building Blocks to **Full Systems**

Tues Oct 30, 2 pm to 4:30 pm

Chair: F. Toth, DSP Div, Integrated Device Technology, Santa Clara, Calif

"Signal Processing Gate Array Macrofunction Yields Customizable Standard Products"

A. Tregida, International Microcircuits, Inc, Santa Clara, Calif

9/2 "Trade-offs in the Use of the TMS320 as a Digital Signal Processing Element"

J. Bradley, Texas Instruments, Inc, Houston, Tex

9/3 "CMOS Word-Slice: A Compact Solution for DSP Design"

R. M. Lopes, Synertek, Inc, Santa Clara, Calif

9/4 "High Performance CMOS DSP Building Blocks Allow Low Power System Optimization'

F. Toth, DSP Div, Integrated Device Technology, Santa Clara, Calif

9/5 "Highest Performance System Uses a New CMOS Mult/Accumulator"

F. Williams, TRW, LSI Products, La Jolla, Calif

Session 10: Using High Performance Multiprocessing and **Coprocessor Architectures**

Tues Oct 30, 2 pm to 4:30 pm

Chair: H. Look, Zilog, Campbell, Calif

10/1 "Multiprocessing with TMS 32010"

D. G. Garcia, Texas Instruments, Inc, Houston, Tex

10/2 "Implementing Multiprocessor and Coprocessor Architectures with the Z80,000 CPU"

H. Look, Zilog, Campbell, Calif

10/3 "Multiprocessing Features of the MC68020"

B. Beims, Motorola, Inc, Austin, Tex

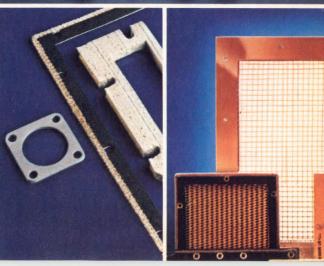
(continued on page 56)

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(continued from page 54)

10/4 "Distributed Processing with the NS32032" R. Mateosian, National Semiconductor, Santa Clara,

10/5 "Increasing System Performance Using Coprocessors"

D. Krelle, Intel Corp, Santa Clara, Calif

Session 11: Access Paths to Memory: **Processors and Peripherals**

Wed Oct 31, 10 am to 12:30 pm

Chair: C. H. Kaplinsky, Signetics Corp, Sunnyvale, Calif

11/1 "Access Paths: Memory Hierarchies and Protection"

C. H. Kaplinsky, Signetics Corp, Sunnyvale, Calif

11/2 "The Signetics Memory Access Controller" Dr. M. Freeman, Signetics Corp, Sunnyvale, Calif

11/3 "NS32032 Memory Bus Usage"

D. Gurley and M. Baron, Architecture Group, National Semiconductor, Sunnyvale, Calif

11/4 "The z80,000: Memory Management and Cache Aspects"

A. Patil, Zilog, Campbell, Calif

11/5 "A Dual-Port Memory Interface via a DRAM Controller'

J. W. Sleezer, Peripheral Components, Intel Corp, Santa Clara, Calif

Session 12: Microprocessor-based System Software

Wed Oct 31, 10 am to 12:30 pm

Chair: C. Hunter, Hunter & Ready, Inc, Palo Alto, Calif

12/1 "Microprocessor-based Software Integration" P. Zappacosta, Logitech, Inc, Redwood City, Calif

12/2 "Improving User Productivity with Database Management Systems"

M. Stonebraker, Relational Technologies, Berkeley, Calif

12/3 "Software Component Calling Conventions" L. Froisland, Hunter & Ready, Inc, Palo Alto, Calif

12/4 "Satellite Applications for Microprocessor Software"

W. Ivey, Equatorial Communications Co, Mountain View, Calif

12/5 "Transparency in Communication Software" T. R. Firman, Action Technologies, Inc, San Francisco, Calif

Session 14: Customizable Linear VLSI

Wed Oct 31, 10 am to 12:30 pm

Chair: N. J. Miller, Micro Linear Corp, San Jose, Calif 14/1 "Customization Through Programmable Digital Signal Processing"

R. Apfel, Advanced Micro Devices, Sunnyvale, Calif

14/2 "Mask Programmable Analog Array Complexity Considerations"

D. Bray, Interdesign, Inc, Scotts Valley, Calif

14/3 "Measuring the Level of Linear Integration"

P. Brown, Micro Linear Corp, San Jose, Calif

14/4 "Advanced Design Automation Techniques for Analog VLSI"

G. Kelson, Silicon Systems, Inc, Tustin, Calif.

14/5 "Analog Digital System CMOS Semi-Custom IC" A. Kadis and Dr. G. Sheu, Telmos, Sunnyvale, Calif, Dr. H. Voss, Lockheed Missile & Space, Inc. Palo Alto, Calif

Session 15: Futures in Electronic Packaging

Wed Oct 31, 10 am to 12:30 pm

Chair: C. L. Hutchins, Texas Instruments, Inc, Houston, Tex

15/1 "Tape Automated Bonding"

C. E. Huwen, International Micro Industries, Scottsdale, Ariz

15/2 "Advanced Concepts in Ceramic Packaging"

R. Sigliano, Kyocera, Irvine, Calif

15/3 "Key Issues of Surface Mounted Integrated Circuits'

H. Test and C. L. Hutchins, Texas Instruments, Inc. Dallas, Tex

15/4 "Tomorrow's Package—More 1/0s?"

A. Russo, M. Hagen and M. Cusak, United Technologies Microelectronics, Colorado Springs,

Session 16: I/O Handling Techniques in Microprocessor-based Systems

Wed Oct 31, 2 pm to 4:30 pm

Chair: J. Miller, Adaptec, Inc., Milpitas, Calif.

16/1 "Realtime 1/0: Nobody Ever Said It Was Going to be Easy"

J. Ready, Hunter & Ready, Inc, Palo Alto, Calif

16/2 "I/O Bottleneck For Microcomputers is Real and Solutions are Here'

S. Bal, Adaptec, Inc, Milpitas, Calif

16/3 . "A Standard Protocol for Host Computer/ Peripheral Interface Allows Upgrading to the Latest Mass Storage Devices"

S. DeHart, Hewlett-Packard, Greeley Div, Greeley,

Colo 16/4 "Intelligence and Disc Drives"

I. D. Allan, Priam Corp, San Jose, Calif

Session 17: Unix for Microprocessors

Wed Oct 31, 2 pm to 4:30 pm

Chair: R. Mateosian, National Semiconductor, Santa Clara, Calif

17/1 "The MC68020 and Unix System V/68"

B. Beims, Motorola, Inc, Austin, Tex

17/2 "Unix for the NS32032—The Best Unix Micro You Can Buy"

K. Wallace, National Semiconductor, Santa Clara,

(continued on page 58)



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(continued from page 56)

- 17/3 "The z8000 and z80,000 for Maximum Unix Performance"
 - B. Andrews, Zilog, Inc, Campbell, Calif
- 17/4 "Unix and Western Electric's Computer Systems"
 - P. Lu, AT&T Bell Laboratories, Holmdel, NJ

Session 19: Instant Turnaround Custom ICs—New Concepts in VLSI Design"

Wed Oct 31, 2 pm to 4:30 pm

- Chair: R. F. Hartmann, Altera Semiconductor Corp, Santa Clara, Calif
- 19/0 "Session Overview: Instant Turnaround Custom ICS—New Concepts in VLSI Design R. F. Hartmann, Altera Semiconductor Corp, Santa
 - Clara, Calif
- 19/1 "Second-Generation Programmable Logic Devices Extend Design Capabilities"
 - J. Yee, Advanced Micro Devices, Inc, Sunnyvale, Calif
- 19/2 "Programmable Logic Replaces Gate Arrays"U. F. Chan, Altera Semiconductor Corp, San Jose, Calif
- 19/3 "An Easier Way to Design with Programmable Logic"
 - R. Osann, Assisted Technology, Inc, San Jose, Calif
- 19/4 "Next-Generation Programmable Logic"V. J. Coli and J. Grenier, Monolithic Memories, Inc, Santa Clara, Calif
- 19/5 "Personal Computer-based Programmable Logic Design Support System"
 - S. M. Walters, Valley Data Sciences, Mountain View, Calif

Session 20: Advances in Automated Circuit Board Assembly

Wed Oct 31, 2 pm to 4:30 pm

- Chair: B. Kaufman, Augat/Alcoswitch, North Andover, Mass
- 20/1 "Auto-insertable Passive Devices—Integrating Circuits in Dip Switches"
 - R. Deziel, Augat/Alcoswitch, North Andover, Mass
- 20/2 "Payback on Auto-insertion—A Look at the Dollar Savings"
 - D. Brault, Northeastern Tool Company, Laguna Hills, Calif
- 20/3 "A User Reports on Auto-insertion Benefits"D. Shoquist, Hewlett-Packard Co, Santa Clara, Calif
- 20/4 "The Benefits of Surface Mount Technology"
- P. Marcoux, AWI, Santa Clara, Calif 20/5 "Using Auto-insertable Dip Switches in the
- 20/5 "Using Auto-insertable Dip Switches in the Manufacture of Computers"
 - G. Samii, MAI, Basic Four, Tustin, Calif

Session 21: Ada-Multiple Points of View

Thurs Nov 1, 10 am to 12:30 pm

- Chair: Dr. T. M. VandenHeede, Zilog, Inc, Campbell, Calif
- 21/1 "Ada From the User's Point of View"
 - Dr. T. M. VandenHeede, Zilog, Inc, Campbell, Calif
- 21/2 "Ada From the Implementor's Point of View"D. Eilers, Irvine Computer Sciences Corp, Irvine,Calif
- 21/3 "Ada From the Validator's Point of View" Dr. T. H. Probert, Institute of Defense Analysis, Alexandria, Via
- 21/4 "Ada From the DoD Point of View"

 T. A. Oberndorf, Naval Ocean Systems Center,
 San Diego Calif
- 21/5 "Ada From the Vendor's Point of View" D. Morris, SofTech, Inc, San Diego, Calif

Session 22: EMI/RFI Regulations and Compliance

Thurs Nov 1, 10 am to 12:30 pm

- Chair: R. M. Simon, Transmet Corp, Columbus, Ohio
- 22/1 "Plastics That Shield Against EMI/RFI"
 - S. R. Gerteisen, Wilson-Fiberfil International, Evansville, Ind
- 22/2 "Plastics for ESD"
 - J. Travis, LNP Corp, Malvern, Pa
- 22/3 "ASTM Testing for EMI/RFI Shielding"
 - R. M. Simon, Transmet Corp, Columbus, Ohio
- 22/4 "EMI Shielding Enclosures"
- L. Tracewell, Tracewell Enclosures, Inc, Columbus, Ohio
- 22/5 "Testing for FCC Compliance"
 - G. Dash, Dash, Straus, and Goodhue, Inc, Boxborough, Mass

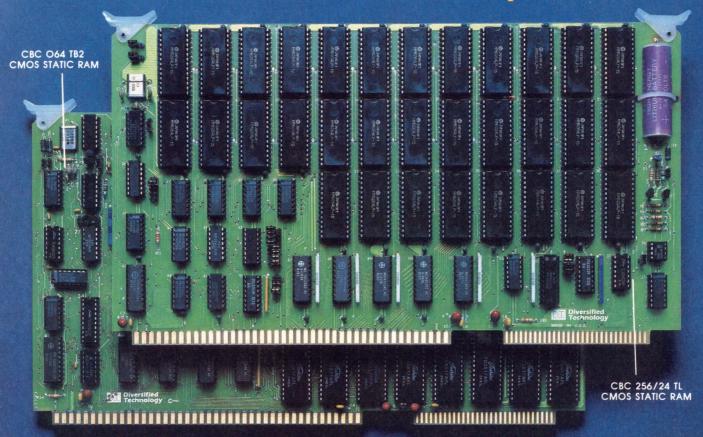
Session 23: Graphic Video Interfaces: A System Design Perspective

Thurs Nov 1, 10 am to 12:30 pm

- Chair: P. Madan, EXEL Microelectronics, Inc, San Jose, Calif
- 23/1 "The New Graphics Standards—An Overview"
 S. Stash, Precision Visuals, Boulder, Colo
- 23/2 "Design Considerations for Implementation of NAPLPS Videotex Terminals"
 - J. Lopinto, Communication Specialties, Inc, Commack, NY
- 23/3 "HCMOS Graphics Processors Provide Extensive Support for Wide Range of Bit-mapped Displays" P. Madan, EXEL Microelectronics, Inc, San Jose, Calif

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CIRCLE 31

(continued from page 58)

23/4 "Graphics Display Processor Integrates
Drawing Algorithms and Display Control in cmos"
H. Maejima, Hitachi America, San Jose, Calif and
K. Katsura, K. Minorikawa, and H. Yonezawa,
Mutashi Works

23/5 "LSI Bit-mapped Video Memory Control" R. Palm, Synertek, Santa Clara, Calif

Session 24: System Oriented VLSI for Mass Storage Control

Thurs Nov 1, 10 am to 12:30 pm

Chair: D. Horton, Advanced Micro Devices, Sunnyvale, Calif

24/1 "Advanced vlsi Disk Controller Solves System Interface Problems"

M. S. Young, Advanced Micro Devices, Sunnyvale, Calif

24/2 "System-oriented ic Chip Set to Support High Speed Bit Stream in Hard Disk Control" N. Siddique, Signetics Corp, Sunnyvale, Calif

24/3 "Two-Micron CMOS VLSI Hard Disk Controller Integrates Data Buffer and Error Correction" T. Funabashi, K. Minorikawa, H. Yonezawa, T. Cantrell, and K. Iwasaki, Hitachi American Ltd, San Jose, Calif

24/4 "VLSI Disk Controllers"

R. Chung, Western Digital Corp, Irvine, Calif

24/5 "Power Adaptec Chip Set Simplifies Disc Controller Design"

G. Venkatesh, Adaptec, Inc, Milpitas, Calif

24/6 "Programmable Winchester/Floppy Disk Controller With Dual 10 Mbyte/sDMA Channels" M. Evans, National Semiconductor Corp, Santa Clara, Calif

Session 25: Applications of Networks Using Standard Personal Computer Interfaces

Thurs Nov 1, 10 am to 12:30 pm

Chair: Dr. J. MacCalla, Advanced Systems Concepts, Inc. Pasadena, Calif

25/1 "Interface Consideration in Computer Networks"

Dr. M. Schneidewind, Naval Postgraduate School, Monterey, Calif

25/2 "Distributed Networking of Peripherals in Industry"

Dr. E. MacCalla, Advanced Systems Concepts, Inc, Pasadena, Calif

25/3 "Interconnecting Distributed Computers and Instruments"

D. J. Nadon, National Instruments, Austin, Tex

25/4 "Remote Networking Over Telco Lines"

D. Buck, Com Design, Inc, Goleta, Calif

25/5 "Methods of Merging Asynchronous and Synchronous Networks"

R. D. Guthrie, Local Data, Inc, Torrance, Calif

25/6 "Small Area Networks for Personal Computers"
A. Kingsbury, Signetics Corp, Sunnyvale, Calif

Session 26: Uses of Modula-2

Thurs Nov 1, 2 pm to 4:30 pm

Chair: A. W. Brown, Volition Systems, Del Mar, Calif

26/1 "A Unix-like Shell in Modula-2, a Systems Implementation Language"

D. R. Cohen, Jet Propulsion Laboratory, Pasadena, Calif

26/2 C. T. Helmers Jr, North American Technology, Inc, Peterborough, NH

26/3 "Low Level Machine Access in Modula-2"M. Hofkin, Journal of Pascal, Ada, and Modula-2, La Jolla, Calif

26/4 "Object-oriented Construction Systems in Modula-2"

Dr. A. Munro, Univ of Southern California, Redondo Beach, Calif

26/5 "Modula-2's Masterful Implementation of Interrupts"

J. P. Shaver, Allergan Pharmaceuticals, Irvine, Calif

Session 27: Modular Automatic Test Equipment (MATE)

Thurs Nov 1, 2 pm to 4:30 pm

Chair: S. Levine, Litton Guidance & Control, Woodland Hills. Calif

27/1 "The Impact of MATE on the Commercial Electronics Manufacturing Industry"

P. W. Shelton, Sperry Corp, Great Neck, NY

27/2 "MATE Systems Software—the Contractor's Perception"

Dr L. L. Lane, General Dynamics/Electronics, San Diego, Calif

27/3 "MATE User Group—Its Activities to Date"
J. S. Martins, John Fluke Mfg. Co, Inc, Everett, Wash

27/4 "The Effect of MATE on the Military Equipment Manufacturer"

C. Smith and S. Levine, Litton Guidance & Control, Woodland Hills, Calif

Session 28: Bit-mapped System Design— ECL Solutions

Thurs Nov 1, 2 pm to 4:30 pm

Chair: A. Sfarti, Advanced Micro Devices, Sunnyvale, Calif

28/1 "ECL-TTL Partitioning in Bit-mapped System Design"

O. Garbe and P. Reilly, Advanced Micro Devices, Sunnyvale, Calif

28/2 "Frame Buffer Memory Organization"
R. Lawrence, Digital Equipment Corp, Marlboro,

28/3 "Semicustom Gate Array Chip to Handle 60-Hz Non-interlaced Video"

R. Pineau, Lexidata, Billerica, Mass

(continued on page 62)

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(continued from page 60)

28/4 "High Performance Display Controller Operates From Single 5-V Power Supply

J. G. Torborg, Raster Technologies, North Billerica, Mass

Session 29: Leading Edge Semiconductor Memories

Thurs Nov 1, 2 pm to 4:30 pm

Chair: S. Grossman, EXEL Microelectronics, Inc, San Jose, Calif

"High Density EPROMS"

K. Pope, Advanced Micro Devices, Inc, Sunnyvale,

29/2 "EEPROM Speed and Power Breakthroughs" R. G. Huff III, EXEL Microelectronics, Inc, San Jose,

29/3 "High Speed cmos Static RAMS"

F. Jones, Inmos Corp, Colorado Springs, Colo

29/4 "High Performance 256 K DRAMS"

H. Sussman, Mostek Corp, Carrollton, Tex

29/5 "Video Memory Technology and Applications"

R. Pinkham, Texas Instruments, Inc, Houston, Tex

Session 30: Talking to 'Big Blue'— Alternatives for Data Communications With IBM **Mainframes**

Thurs Nov 1, 2 pm to 4:30 pm

Chair: A. Goldberger, EXEL Microelectronics, Inc., San Jose, Calif

30/1 "Hi, Big Blue. I Speak All Languages'-The SCN68562 DUSCC'

J. Magill, Signetics Corp, Sunnyvale, Calif

30/2 "Highly Integrated Coprocessor Simplifies SDLC Implementation'

R. Jigour, EXEL Microelectronics, Inc, San Jose,

30/3 "Micro to Mainframe Utilizing the 3270 Coaxial Connection'

R. Rawson, Forte Data Systems, San Jose, Calif

30/4 "Mainframe Interconnection Via Protocol Conversion'

R. Penn, Protocol Converters, Inc., Woodland Hills, Calif

Session 31: Semicustom Alternatives— An Overview

Fri Nov 2, 2 pm to 4:30 pm

Chair: J. Kamdar, National Semiconductor, Santa Clara, Calif

"The Low Cost, Quick Turnaround, High Performance, Semicustom Solution: Programmable

J. Vithayathil, National Semiconductor Corp, Santa Clara, Calif

31/2 "An Overview of Bipolar ECL Gate Arrays, The High Speed Alternative'

R. Allgeyer, Fairchild Camera & Instrument Corp, Milpitas, Calif

31/3 "High Speed нсмоз Logic Array Design for Systems/Board Level Engineers" P. Zaballos, LSI Logic, Milpitas, Calif

31/4 "Standard Cells—The Next Generation of Semicustom Logic"

D. G. Wick and D. W. Still, Honeywell, Colorado Springs, Colo

31/5 "Testing Semicustom Logic"

E. J. McCluskey, The Center for Reliable Computing Science, Stanford Univ, Stanford, Calif.

31/6 "Packaging Design Considerations for a New Generation of IC Devices'

J. L. Hayward, Advanced Micro Devices, Sunnyvale, Calif

Session 32: IBM PC Interfaces For Industrial Control

Fri Nov 2, 10 am to 12:30 pm

Chair: R. Born, High Tech Business Consultant, Monterey, Calif

"Extending IBM Personal Computer to Interface With Real World Plant'

D. G. Holmes, Monash Univ, Dept of Electrical Engineering, Melbourne, Australia

32/2 "I-Bus IBM PC Compatible Single-board Computers for Board Level OEM Systems"

J. P. Choisser, I-Bus Systems, San Diego, Calif

32/3 "The PC/STD Connection"

R. L. Mack, Ultra Link, Inc, Capitola, Calif

32/4 "A simple STD BUS Control System for the IBM PC'

A. Allard, ProLog Corp, Monterey, Calif

32/5 "The IBM PC as a Process Controller"

R. Floyd and R. C. Stanley, IBM-Manufacturing System Production, Boca Raton, Fla

32/6 "IBM PC Goes Multibus"

P. Vukovic, Bit 3, Minneapolis, Minn

Session 33: Speech Technology in the 80s

Fri Nov 2, 10 am to 12:30 pm

Chair: J. A. Binneboese, Motorola, Inc, Austin, Tex

33/1 "A Total Speech Synthesis System"

K. S. Padda, L. Bonet, A. A. Shaheen-Gouda, and T. Williams, Motorola Inc, Austin, Tex

33/2 "Operational Evaluation of Automatic Speaker Verification Systems"

D. E. Crabbs, Interstate Voice Products, Orange,

33/3 "Speech Recognition Using Interactive Laboratory System (ILS)" S. Davis, STI, Goleta, Calif

(continued on page 64)

BOB, CAROL, TED & ALICE



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(continued from page 62)

- 33/4 "A Single Chip cmos Speech System"
 - J. Reimer, Texas Instruments Inc, Houston Tex
- 33/5 "Voice Processing Services for Office Automation and Telecommunications: The DSC2000 Voiceserver"
 - D. Wong, Digital Sound Corp, Santa Barbara, Calif

Session 34: Software Development **Techniques**

Fri Nov 2, 2 pm to 4:30 pm

- Chair: J. Bates, Motorola Inc, Austin, Tex
- 34/1 "Assembly Language Techniques"
 - V. Wintriss, Computer System Assoc, San Diego, Calif
- 34/2 "Realtime Multitasking on a Single-Chip Microcomputer"
 - D. Weiss, Motorola Inc, Austin, Tex
- 34/3 "Cross-Support Tools for Microcomputer Product Development"
 - Dr. J. Kelley, Relational Memory Systems, San Jose, Calif
- 34/4 "Using Personal Computers for Single-Chip Software Development'
 - H. Gordan, Network Research Corp, Santa Monica, Calif
- 34/5 "Innovative Programming Techniques"
 - J. Zurkow, Avocet Corp, Rockport, Me

Session 37: Local Area Network Solutions on Silicon

Fri Nov 2, 10 am to 12:30 pm

- Chair: R. C. Brand, National Semiconductor, Santa Clara, Calif
- 37/1 "VLSI for Standard & Nonstandard Networks" V. Coleman, Advanced Micro Devices, Sunnyvale, Calif
- 37/2 "Generalized Data Engine for CSMA and Token Local Area Networks'
- G. Moseley, Seeg Technology, San Jose, Calif
- 37/3 "LAN Controller Design Approaches"
- C. Yeager, Intel Corp, Santa Clara, Calif
- 37/4 "Open System Interfaces Provided by Token Ring LAN Adaptor"
 - J. Hughes, Texas Instruments Inc, Houstin, Tex
- 37/5 "Focused Design Teamwork Produces IEEE 802.3 Chip Set"
 - R. V. Balakrishnan, National Semiconductor Corp, Santa Clara, Calif
- 37/6 "Network Concepts Simplify Microcontroller Interfacing"
 - R. Mitchell and B. Houghton, Signetics Corp, Sunnyvale, Calif



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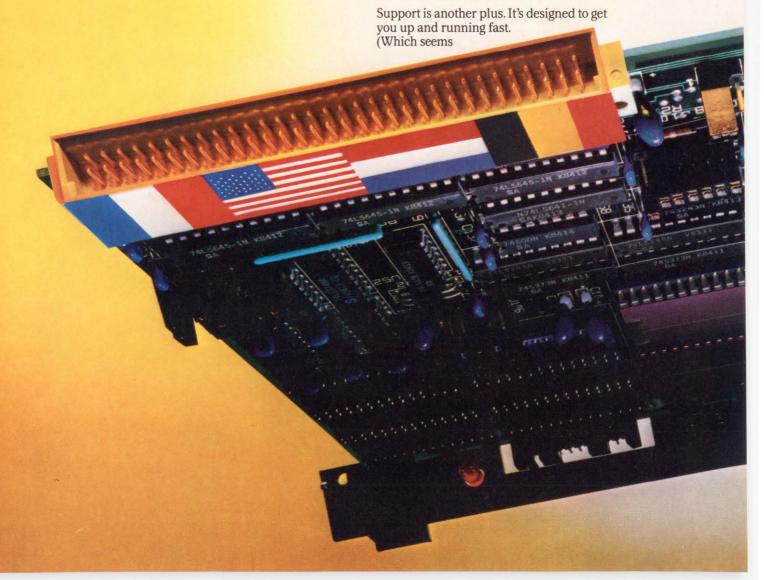
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MASS STORAGE

Bigger, better, faster, smaller, cheaper, and more flexible...these features are at the top of every system designer's wish list. CPU designers focus on smaller, faster, and cheaper, hoping to produce the next generation's supermachine.

Occupying a critical position in the systems to come are mass storage devices. Their charter is to supply both the massive amounts of data storage capacity and the rapid access to data that these systems will require. Since systems to come span the gamut from super to micro, storage systems offer size and capacity choices to match.

Data storage capacities in the gigabyte per device range are well within sight before the end of the decade. Emerging optical storage devices will serve to put multiple gigabytes online. Rigid disk drives using thin-film media and low flying thin-film heads will bring capacities up into the gigabyte range. Trickle down effects promise smaller form factors with expanded capabilities. The smallest of these, just coming into quantity production, continues to focus on shock resistance and power consumption.

The need to maintain duplicate copies of stores of information is resurfacing with a vengeance. Propelled by the increasingly realtime nature of systems and by the magnitude of damage that even momentary downtime can cause, backup devices are occupying an increasingly important position in the storage hierarchy.

These secondary stores are based on magnetic tape. Here, as in disk devices, thin-film media and heads play a part in putting more data into increasingly more compact packages. Optical and removable disk drives are also destined to play a part in serving the secondary storage needs of future systems.

In the background, standards activities continue. Standardization served as the driving force behind the widespread acceptance of 5½-in. Winchester drives and the quarter-inch tape cartridges that serve as their backup. As the product mix becomes more complex and the product life cycle grows shorter, the issue of standardization at both the system and the device level becomes even more important.

Peg Killmon Senior Editor

COMPUTER DESIGN/October 1, 1984 6

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MASS STORAGE **DEVICES KEEP PACE** WITH SYSTEM NEEDS

Storage peripherals stretch and shrink to serve recognized system demands. Renewed standards efforts open the way for technological advances to come and allow designers to mix or match at will.

by Peg Killmon, Senior Editor

Driven by rapidly expanding data bases, storage devices continue to grow in speed and capacity. With this demand for greater capacity has come a call for a smaller form factor to match the scaled down size of the most recent central processors.

Concurrently, the distributed concept of computing power and the enhanced processing speed of primary computer systems has called for faster transfer of data between storage and the processor itself. And, while storage devices work to meet these needs, they must simultaneously respond to concerns of reliability, availability, and cost of ownership.

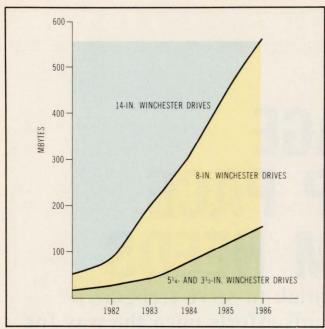
A primary consideration

Data storage devices must serve two different types of data bases. One is volatile; data resides online continuously and are subject to constant updates. These data bases require storage systems that facilitate the update process. The storage device must supply fast access to data, the ability to readily modify data, and rapid transfer of data to the processing unit. These are characteristics of rotating magnetic memories, disks and drums, and are driven by cost/ drive factors.

The other type of data base is archival; data is stored, rarely changed, and only a small fraction of



the data base is online at any one time. Archival storage demands nonvolatility as well as removability and easy storage. The removability factor makes media cost an important consideration. The nonrealtime nature of the applications as well as the cost factor, puts archival applications into the realm of magnetic tape. Here, the ability to store quantities of data on a low cost reel of tape that is compact and easy to handle has resulted in the formation of vast libraries of tape. Advances in disk technology—



Winchester disk drives serve primary online storage needs that range from 5 Mbytes to 1 Gbyte. Three basic form factors compete on two levels-between 100 and

first the floppy disk, then the storage module drive, and, more recently, the removable disk cartridge have allowed disk devices to participate as archival devices also.

Have it your way

Magnetic recording technology provides the vast information stores that led us to become the "information society" described in John Naisbitt's book, Megatrends. It supplies the computer industry with disk drives that store anywhere from 256 Kbytes to more than 1 Gbyte—more than 4000 times as much. It is also responsible for the massive amounts of data available on magnetic tape in installations across the world. Still, continued growth in pure processing



Cyber 400 Series thin-film heads are direct plug-compatible replacements for minicomposite and minimonolithic ferrite heads. Cybernex Corp designed the heads to fly at 12 μ in. with a 15-g load force.

power provided by the influx of faster CPUs has not stopped, posing the problem of satisfying future data storage needs. This dilemma has spurred researchers to make devices able to store data at higher densities and supply it to processors faster.

Contenders in this race take many forms—optical data storage technology shows increasing promise; research in vertical recording techniques shows signs of appearing in commercial devices soon; and longitudinal magnetic recording technology has not yet reached its limits.

However, storing the most bits per square inch of media remains the concern primarily of those in the research and development labs. Leading edge products are being developed that match the processing needs of supercomputers and other special applications. A far larger number of system designers can take "hand-me-down" technology pioneered by these leading edge products and adapt it to the needs of the many mini and microcomputer systems that are begging for storage. Thus, the cost/performance equation is juggled to fulfill system demands across the spectrum.

Among the state-of-the-art disk systems intended to feed the rapacious appetites of mainframe class computers. IBM's 3380 has served as a standard since its introduction. Storage systems from StorageTek (Louisville, Colo) and Control Data Corp (Minneapolis, Minn) are in the same league. These systems, which introduced the use of thin-film media and thinfilm heads, are capable of storing more than 1 Gbyte of data on a single spindle disk drive.

Those supplying the less rigorous demands of minicomputers and other high performance systems have adopted these technologies as they became more readily available. This led to the development of higher capacity disk drives of the now familiar 14-in. Winchester variety. Among these are a 1.4-Gbyte drive from Ibis Systems (Westlake Village, Calif) and an 825-Mbyte drive produced by Ampex Corp (Redwood City, Calif) that aims to supply the best price/performance ratio yet.

The 160-Mbyte Atlas series drive from Alpha Data Inc (Chatsworth, Calif) tackles the problem of sagging response times encountered when multitasking systems are heavily loaded. The 50 heads in this drive provide a virtually constant response time, no matter how heavy the load. Under a light load, the unit supplies a 20-ms access time. Response remains in the 40-ms range under strenuous conditions.

Capacities of 8-in. drives continue to grow as multi-user system requirements climb. Filling needs of both mini and microcomputer systems, these units must compete with both 14-in. and 51/4-in. drives. In this form factor, Micropolis (Chatsworth, Calif) has designed its 1450 series to store 330 Mbytes with access times of 20 ms. Using 20 heads on six platters, this unit writes data at 12,899 bits/in. on 1160



MegaVault's 8-in. parallel transfer disk MVP212 Winchester drive dedicates an amplifier to each head to minimize noise. The drive's eight data surfaces are divided into two sets of four parallel read/write channels to allow 38.6-MHz transfers.

tracks/in. Northern Telecom Inc (Ann Arbor, Mich) extended its Mercury family to 378 Mbytes. These 8300 series drives use thin-film heads to attain the density necessary to accomplish this.

NEC Information Systems (Boxborough, Mass) pushes its D2300 drive to 520 Mbytes. This drive uses 20 read/write heads to record at a density of 18,600 bits/in. Problems of spindle tilt, encountered with the stack of six platters, are dealt with by supporting the spindle on both ends.

To speed storage and retrieval, the 212-Mbyte MVP212 from MegaVault (Woodland Hills, Calif) breaks its eight data surfaces into two sets of parallel read/write channels. Allowing any read/write combination to occur on four surfaces guarantees a 38-MHz data transfer rate using four channels.

In the 5½-in. size that has caused 8-in. drives so much consternation, the pace has not slowed. Introductions continue in both full- and half-height units. Capacities continue to grow as thin-film media and thin-film heads are put to work.

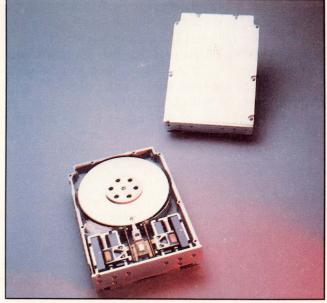
A recent introduction from startup Tulin Corp (San Jose, Calif) uses three thin-film plated disks with 3370-type ferrite heads to put 26 Mbytes in a half-height drive. The design puts the read/write preamplifier inside the head/disk assembly to guarantee a clean signal. Plans for the future include reducing the access time from its current 100 ms by supplying an encoder to the stepper motor and using a voice coil motor to increase track density.

Thin-film heads are combined with thin-film metallic media in drives from Advanced Storage Technology (San Jose, Calif). Writing 103 Mbytes on three platters at 20,880 bits/in., the AST 96203

uses a voice coil linear positioner and a closed loop dedicated servo to achieve accurate positioning.

Applied Information Memories (Milpitas, Calif) puts 250 Mbytes on five platters in its Dart 250. Using thin-film heads and sputtered media, the drives record at 700 tracks/in. Average positioning times is 18 ms and data transfers occur using a storage module drive (SMD) interface.

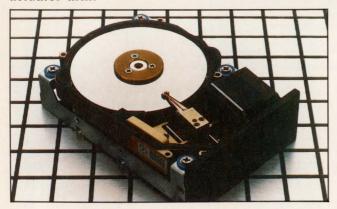
Destined to capture as much attention as 5 1/4-in. drives, the rapidly growing 3 1/2-in. Winchester world faces demands for low power, ruggedness, as well



Storing 103 Mbytes, the half-height $5\frac{1}{4}$ -in. 96203 from Advanced Storage Technology uses thin-film heads and three thin-film platters. Thin-film heads contribute aerodynamic stability to improve signal-to-noise ratio.

as reliability. These units typically store 5 Mbytes on one platter, with two platters raising capacities to 10 Mbytes. Average access times are about 90 ms.

Because these units are widely used in portable computers, shock mounting and other protection features are important. Mechanical brakes are added to prevent head movement during transit. One newcomer, LaPine Technology (Santa Clara, Calif) has designed units to withstand a 40-G shock load. Called the Ranger family, these drives use a 4-point internal suspension system. With additional external shock absorbers on two sides, they can withstand a 100-G shock load. Head and media damage are avoided using a proprietary head lifter and arm lock. Rodime PLC (Glenrothes, Fife, Scotland) protects its drives through a 30-G shock. A mechanical failsafe brake acts as a transit lock for the dc motor. A similar brake for the stepper motor locks the actuator arm.



Microscience International's half-height 31/2-in. Winchester drive, the HH-312, uses a proprietary closed-loop servo and linear actuator to achieve 70-ms access to 10 Mbytes.

With the 5-Mbyte capacities well in hand, faster, higher capacity units are beginning to appear. Microscience International (Mountain View, Calif) supplies a 10-Mbyte drive that uses two platters and has an access time of 70 ms. Plated media, in conjunction with closed-loop servo and embedded servo information, contribute to the 9680 bits/in. density achieved in this drive. Another high capacity drive, the M-125 from Microcomputer Memories, Inc (Van Nuys, Calif), can store 25 Mbytes with an average access time of 85 ms.

Seeing the light

Raising the limits of recording density, optical memory storage systems are beginning to come to light. Using lasers to read and write from optically sensitive media, these units can store gigabits of data on 14-in. disks. Once written, information can be deleted, but cannot be rewritten in the same place.

Optical disk storage units provide online storage costs comparable to those of magnetic disks. Offline storage costs are one third those of magnetic tape. Storage capacities of optical disks combine with their

access times to fit between magnetic disks and magnetic tape. Optical recording devices supply a lower cost per byte of data stored than disk, and faster access than tape devices.

Theoretical limits for optical media are 100 times greater than those of magnetic media—30 Gbits/in² versus 300 Mbits/in². Today's magnetic technology has reached 12 Mbits/in²; available optical units supply 600 Mbits/in2.

In the first high performance system, the 7600 Optical Storage System from StorageTek, 4 Gbytes of data are packed on one side of a 14-in. disk. A more recent drive from Hitachi America Ltd (San Bruno, Calif) uses a 12-in. disk to store 2.6 Gbytes. The model 301, however, uses both sides of the platter and writes at 19,500 bits/in.

Shugart Corp's Optimem Div (Sunnyvale, Calif) records 1 Gbyte on its Optimem 1000. Designed for use as a low cost storage device, this drive records at 14,500 bits/in. on 14,500 tracks/in. It supplies a 130-ms average access to data and transfers at rates between 3.8 and 8 Mbits/s. Similarly, Gigadisc, from the Alcatel Thompson Gigadisc Div of Thompson-CSF (Redondo Beach, Calif) writes 1 Gbyte on either surface of its 12-in. platter. LaserDrive 1200 from Optical Storage International (Santa Clara, Calif) also has a 1-Gbyte capacity on a single-sided 12-in. platter. In addition to matching the current storage needs of mini and microcomputers with their 1-Gbyte capacities, these units also ease integration into systems by supplying an SCSI interface.

3M Co's, Optical Recording Project (St Paul, Minn) supplies optical memories for both write-once drives such as these and for read-only devices. While write-once drives use laser beams to form reflective microfeatures in the media's surface, read-only systems use focused laser beams to access prerecorded and microreplicated data on the media's surface. The reflective microfeatures can be read using the same lower power beam focused on the laser spot.

Like video disks, read-only disks are becoming common in the digital world. An example of this is the Compact Disc Read-Only Memory (CD-ROM) from Nippon Columbia (Tokyo, Japan). This drive uses pulse code modulation digital recording techniques first applied to high quality audio recording. Hitachi's CD-ROM uses a 4.7-in. prerecorded disk with a 552-Mbyte capacity. Incorporating error correction and built-in interface, the drive supplies a 176-kbit/s transfer rate and accesses data between 0.5 and 1 s. Optical Information Systems Inc (Colorado Springs, Colo) plans to make devices similar to the CD-ROM using 4.7-in. compact disks. Current plans are to supply 550-Mbyte prerecorded systems for use by microcomputers.

Because of their write-once or read-only nature, commercial optical storage devices are limited to filling needs for archival storage. While commercial

From

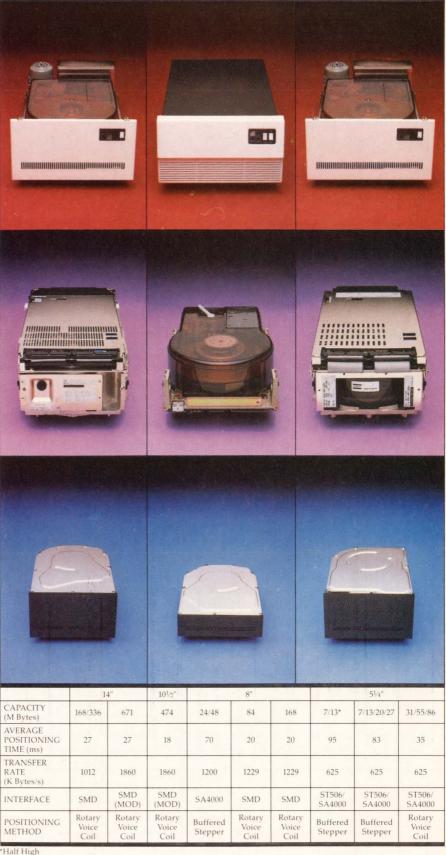
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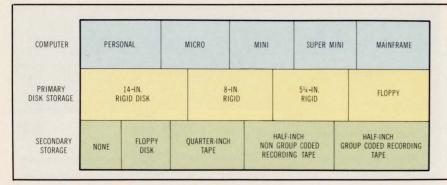
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Computers on different performance levels are served by disk and tape peripherals of varying performance and capacity. Matching storage peripherals on primary and secondary levels to attain performance balances results in the most cost-effective system.

units are not yet available, prototypes of erasable optical drives have been shown by Sony and Canon in Japan. When they become available, the benefits and potential of optical media storage will become obvious.

More interest in tape drives

Magnetic tape is enjoying a revival. The rotating magnetic recording devices of the 1960s replaced magnetic tape as the primary means of mass storage for computer systems. Now, however, interest has been spurred in tape drives by the Winchester disk drive that revolutionized disk drives. This, coupled with the move toward nonremovable media that occurred in the 1970s, has renewed interest in tape drives. While the disk drive offers fast direct access to data, there is a finite limit to how much data it can hold. Thus, any data not directly associated with the problem at hand must be stored elsewhere.

Removable disk storage modules and magnetic tape are two solutions to this dilemma. Tape is usually chosen as the secondary storage medium because it is relatively inexpensive and compact enough to make storage easy. Thus, magnetic tape drives occupy a secure position, albeit, a secondary one.

Tape systems come in two varieties—start/stop and streaming. Some provide both methods of recording. They also come in reel-to-reel or cartridge form, compliance arm, and vacuum column versions. All have specific general parameters and characteristics, and all are supported for a range of applications.

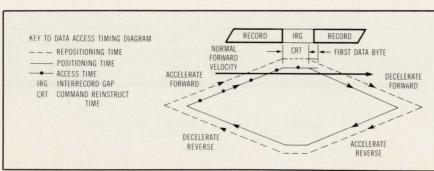
Start/stop drives record data in blocks. Each block is bounded by a gap between records. This gap acts as a reference point for starting and stopping

and is part of the American National Standards Institute (ANSI) recording format standard. Unlike start-stop drives, streaming drives write record gaps while the tape is in motion. Thus, they eliminate the electromechanical parts necessary to generate the gaps in start/stop devices and speed the recording process. However, to record efficiently, they must have a continuous data stream supplied to them. Repositioning the tape while the drives are stopped results in significant speed loss.

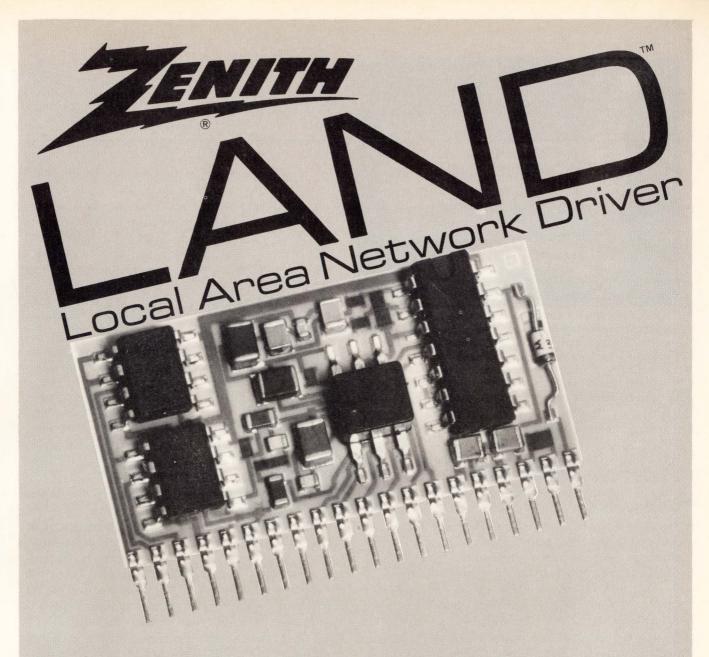
Typically, half-inch, reel-to-reel, start/stop tape drives are used in mainframes and minicomputers. Half-inch streaming drives provide low cost backup for 8- and 14-in. Winchester disk drives, handling capacities between 40 and 100 Mbytes. Units are available which span all mid to high level performance and capacity needs. Cipher Data, Control Data, Kennedy, and Pertec are the giants in halfinch, high performance tape drives.

To overcome the limitations on streaming tape drives—basic mismatch in data transfer rates that forces the tape drive to wait—a high speed buffer is used. In Cipher Data's (San Diego, Calif) Cache-Tape, for instance, the integral controller has a cache memory (more properly termed a buffer). This improves performance by compensating for variations in the system's ability to maintain a constant data rate.

The system can use the drive for transactional backup in the same way it uses vacuum column or tension arm drives. The function is software transparent—no special software is necessary to support streaming performance. A compact, IBM compatible, nine-track streamer, the PCT-1000 stores 138 Mbytes. In the unit, Ibex Computer Corp (Chatsworth, Calif)



The access time of magnetic tape drives is made up of several components. These differ depending on whether streaming or start/stop mode is involved. Some typical times are: repositioning 363 ms at 100 in./s, positioning 294 ms, and access 69 ms. Start/stop time at 50 in./s is 8 ms.



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The MT-2210 cartridge tape drive from MegaTape can backup or restore 500 Mbytes in 36 min. Data are written on 1500 ft of half-inch tape using a 24-track serpentine format at a packing density of 9600 bits/in.

uses two microprocessors and a realtime operating system to handle tape motion and tension control. Thus, they eliminate the need for traditional swing arms and capstan motors, and cut costs. Measuring 19 x 5.25 in., the unit handles 7-, 8.5-, or 10.5-in. tape reels, allowing access to archival data banks and data interchange between all types of systems.

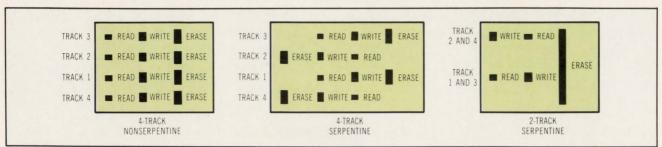
The compactness of drives based on tape cartridges virtually guarantees their success as the tape storage systems of the future. To date, however, there is no agreement on what size the cartridge will be. For example, MegaTape Corp's (Duarte, Calif) MT-2000 drives record 500 Mbytes on a book-sized (9³/₄ x 6 % in.) tape cartridge. These drives use a 24-track serpentine format and pack data encoded in a 4/5 GCR format at 9.6 kbits/in. The 24-track serpentine format is achieved by stepping a 2-track read/write head 12 times. This technique allows any record on the cartridge to be accessed in an average of 30 s.

Using an industry standard Pertec microformatter interface, the drives can read 300-Mbyte cartridges written on their predecessors. The drives sense which cartridge has been inserted and electronically adjust for it. Operation can be at 200 or 50 in./s streaming or 50 in./s start/stop, allowing use either as Winchester backup or for archival storage.

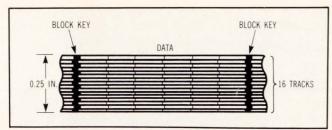
In an 8-in. form factor, Rosscomp Corp (Cerritos, Calif) offers the D160 with what is claimed to be the industry's simplest drive mechanism. Media is wound on a self-protecting reel that eliminates tension problems associated with cartridges. Tapes are kept on course by spring loaded and ball bearing guides. A single capstan motor drives both supply and take up reels with one belt. Self-threading 4-in. reels of tape are recorded using a 24-track serpentine format at 8000 bits/in., and can store 160 Mbytes in 20 min. A 5¹/₄-in. version, the D5160, supports QIC-02 and Small Computer System Interface (SCSI) standards.

Designed to fit a smaller footprint, the model 1110 from Memorex Corp, OEM Products Group (San Jose, Calif) meets the more modest needs of 51/4in. Winchester drives. This drive records 130 Mbytes in start/stop or streaming modes. The unit uses an Enhanced Standard Device Interface (ESDI) interface to transfer data at 225 kbytes/s. Tandon Corp (Chatsworth, Calif) entered the half-inch streaming tape field using a design based on technology derived from earlier tape and flexible disk efforts. The TM951 records 20 tracks on a single reel of selfthreading tape using a serpentine format. Dual recording heads similar to those used in floppy disks provide read after write for data verification. The data transfer rate matches that of the 51/4-in. floppy standard to simplify integration efforts.

IBM's (Rye Brook, NY) recent announcement of its 3480 tape subsystem confirms tape's position as a key element in the mass storage hierarchy. By stating its intention to extend tape technology into the 1990s, IBM provides a rallying point around which a standard for high performance tabe cartridge systems can be built. The 3480 replaces the 10-year-old 3420, raises the storage capacity on a reel of tape, and changes the form factor of the tape subsystem. It also reduces the size of a reel of tape from 10½ to 4 in. in diameter. The system is based on a reelto-reel servo control drive rather than the vacuum columns used in the older drive. This cuts the overall size of the subsystem. Recording density is raised to around 38,000 bits/in. by using thin-film heads and a half-inch chromium dioxide coated tape. This permits 200 Mbytes to be stored on an 18-track tape



Tape drives commonly use one of several types of recording heads. Serpentine and nonserpentine recording heads show distinct differences. A two track head is frequently used to record 16 or 32 tracks in moving head systems.



Preformatted tape in 3M's DC600HC cartridge without inter-record gaps establishes block locations with forward and reverse reading block keys. This allows data to be stored more compactly.

that is packaged in a 4- x 5- x 1-in. cartridge. The data transfer rate is raised from 1.24 to 3 Mbytes/s.

Quarter-inch tape drives better serve small microcomputer-based systems. Intended primarily to supply secondary storage to 5- and 10-Mbyte Winchesters, units from Cipher Data, Archive, Wangtek, Control Data, Data Electronics, and Tandberg provide a cost, size, and performance match for singleuser systems.

Built to supply 134 Mbytes of formatted storage to compete with half-inch cartridges, 3M's HCD-134 Data Cartridge Drive records 32 tracks in a serpentine format and transfers data at 70 kbytes/s. Address markers are prerecorded on the cartridge's tape every 1024 bytes. This contributes to fast access, allowing any file to be located within 45 s.

Most units in the 5½-in. form factor using quarter-inch tape as a media are designed to handle cartridges (eg, 3M's DC100). However, Memtec (Salem, NH) uses cassette concepts. This company's units replace mechanical components with electronics. Whereas a cartridge requires pulleys and tensioning belts, the cassette approach controls the tape with a servo. This allows Companion series drives to store 40 Mbytes on a nine-track tape; 10 or 20 Mbytes on a four-track tape.

Offering capacities of up to 32 Mbytes, Cipher Data's 525 CT FloppyTape uses standard floppy disk drive interfaces and formats. Each tape has six streams, each having 255 segments. Each segment stores 20.8 Kbytes of data. Each tape track appears to the system as a separate logical floppy disk drive. Operating at 78 in./s with a 500 kbit/s transfer rate, 26.6 Mbytes can be read or written in about 9 min.

A 64-Kbyte cache memory in the Sponge T100 from Bering Industries, Inc (Fremont, Calif) combines with disk emulation to allow the tape to run like a disk (a 20-Mbyte, quarter-inch tape cartridge subsystem). To provide backup, the tape drive temporarily becomes the active controller on the bus. In backup mode, the subsystem functions like a computer, thus eliminating the need for a software driver. In normal use, it remains connected to the bus and emulates a disk drive.

Focusing on 3½-in. Winchester drives and their backup needs, Irwin Magnetics's (Ann Arbor, Mich)

48105 puts 10 Mbytes in a minicartridge. Using closed-loop servo technology, the Irwin 210 writes eight tracks at 6400 bits/in. on 0.15-in. wide tape in a DC100A cartridge. Supporting streaming, start/stop, and random access operation, the drive uses a standard minifloppy controller.

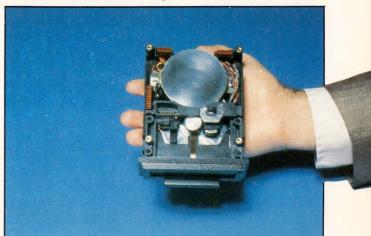
Designed to store 80 Mbytes of data on a DC300XL data cartridge, the Jetstream 16 from North Atlantic Industries, Inc's Qantex Div (Hauppauge, NY) simplifies system upgrades by reading current 4- and nine-track tapes adhering to the QIC-24 recording format. A two-channel, bidirectional tape head controlled by a microprocessor allows either 9- or 16-track tapes to be read or written. A directory block written at the logical end of tape allows any file to be located without streaming through each track.

Claiming that the single record per tape aspects of QIC-24 hinder record update functions, the TG-4060 subsystem from Tallgrass Technologies (Overland, Kan) records in the PC/T-11 format. Storing 60 Mbytes of formatted data on a DC600A cartridge, the quarter-inch tape drive writes data on 11 tracks and can transfer at 720 kbits/s. This format serves personal computer needs by allowing access to tape through DOS commands. ID records within the format serve as landmarks to aid file location and ease the update process.

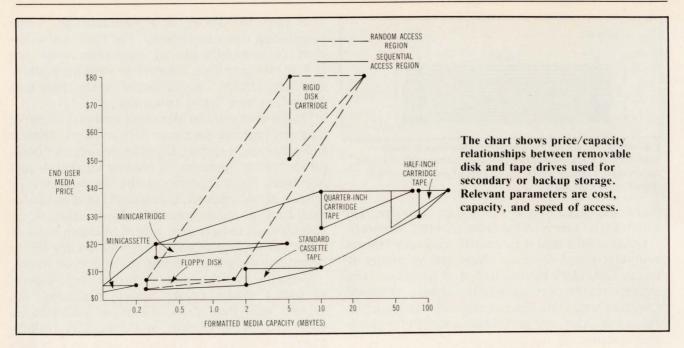
Decisions, decisions, decisions

The secondary storage backup function is also served by products based on technologies other than tape. Floppy disk drives offer removable media suitable for archiving as well as software and data interchange. Removable hard cartridge disk drives are also cost-effective in certain applications.

Floppy disks are not new but are proving hard to replace. Although there were rumors that flexible disks in the 8-in. form factor would soon become dinosaurs, Hitachi recently announced an 8-in. drive



Closed-loop servo technology allows the Irwin 210 to pack 10 Mbytes of data onto a DC100A size cartridge. In a $3\frac{1}{2}$ -in. form factor, the drive uses an industry standard minifloppy interface to ease integration.



that can store 9.6 Mbytes. The FDD-441 combines custom LSI and servo technology with an ultrahigh density media. The unit's 1.5-Mbit/s transfer rate is handled by a modified ST506 interface.

The media (Maxell FD2-HD) is coated with a coepitaxial formulation that is less than half as thick as conventional coatings. Narrow gap Mn-Zn read/ write heads produce a stronger magnetic field than conventional Ni-Zn ferrite heads. This achieves the precise high resolution recording necessary to write data at 20,560 bits/in. on 96 tracks/in.

Advances in head technology will provide 10 Mbytes on a floppy by 1985: 40 Mbytes by 1989.

In the 51/4-in. form factor, 3.3-Mbyte units from Amlyn (San Jose, Calif) and Drivetec (San Jose, Calif) rely on closed-loop servos and preformatted high density diskettes to extend their capacity. Even higher capacities should soon begin appearing. Advancements in head technology will provide the possibility of 10 Mbytes on a floppy by 1985; 40 Mbytes by 1989.

The majority of recent entries, however, show capacities of 1 Mbyte in one-third, two-third, onehalf, and full-height drives. A 1.6-Mbyte drive from Canon USA, Inc (Lake Success, NY), the MDD516A, uses high resolution media to extend its capacity. NEC Information Systems, Inc supplies the FD1155 with a 1.6-Mbyte capacity. These units cut overhead costs by dropping power requirements to 4.5 W. IBM used drives such as these in its recently announced PC AT. This virtually ensures that 1.6 Mbytes will become the standard floppy capacity.

Scaled down versions of these drives, those in the 3½-in. form factor show just as much promise. Most have capacity for 0.5 to 1 Mbyte with higher capacity units appearing. All are compatible with the larger units in logical interface, transfer rate, number of tracks, and bytes per track. Power requirements have been cut to 3.9 W to accommodate their use in portable systems.

While initial products in the 3-in. (Hitachi) form factor survive, the industry seems to be taking the 3½-in. units seriously. Major contracts between Apple and Sony, Sony and Hewlett-Packard, and Shugart and Gavilan appear to have forced the issue.

Hewlett-Packard Co (Greeley, Colo) has announced plans to build a double-sided product with 600-Mbyte capacity by late 1984. By 1988 it expects to pack 4 to 6 Mbytes into that form factor when vertical recording technology emerges.

Yet another way to save

Disk cartridge drives also serve a secondary storage function. These come in sizes that match the form factors of hard disk drives and in capacities between those of floppy disks and tape cartridges. Another bonus is that cartridge disks match the access times of Winchester disks for speed sensitive applications. Many companies feel that cartridge disks do the job better and faster. These include Century Data, Cynthia Peripherals, Amcodyne, Control Data, DMA Systems, Vermont Research, and New World Computer.

The removable cartridge, characterized by a hard disk enclosed in a sealed envelope, benefits by sharing mechanical assembly, electronics, and interface controller with the primary fixed disk drive. It can match access times and transfer rates as well. However, since the cartridge must open to admit the read/

write heads before it can operate, contamination can be a problem.

The Century Data Systems (Anaheim, Calif) 8-in. C2048 pumps double filtered air through a ventilated spindle and moves the air uniformly over each disk. Contaminants on the media are removed by the air flow and exhausted from the drive. The drive has the capacity for 34 Mbytes on three fixed disks and records another 7 Mbytes on the cartridge.

An embedded servo positioning system addresses the problem of accurate head positioning. Cartridges compound this problem by adding another set of track positioning variables. Prerecorded servo data correct tolerance differences between the cartridge and the drive.

Another company, Cynthia Peripherals (Palo Alto, Calif), uses a patented embedded servo technique to ensure cartridge interchangeability. The D140 drives supply a 12-Mbyte capacity on a removable cartridge and match that on the companion 10½-in. fixed disk. Combined with a linear voice coil actuator, the embedded servo ensures accurate head location. Ramp load heads are loaded only when the disk comes up to speed.

The Whitney head suspension used in Amcodyne's (Longmont, Colo) 8-in. Arapahoe 7110 avoids head/disk contact. A 53.2-Mbyte fixed/removable combination, this drive positively pressurizes and purges as the spindle comes up to speed. Then, the heads are loaded onto an established air bearing.

Syquest's (Fremont, Calif) 3.9-in. removable cartridge uses a graphite lubricated plated disk in a sealed cartridge to avoid contamination. These drives use a combination of embedded servo with microstepping stepper motor to achieve precise positioning. Servo information is stored in a single wedge per track. This permits servo positioning to be done within a single disk revolution. New World (Irvine, Calif) solves these problems in its 5½-in. TurboDisc by building the heads into the cartridge. TurboDisc is a 5-Mbyte fixed/5-Mbyte removable combination. The cartridge sells for \$695. The drive itself uses 12 heads mounted on a patented parallelogram-shaped slider assembly to gain 8-ms access to any of the 12 tracks under the heads.

Storing 6.5 Mbytes on an ANSI standard cartridge and 19.5 Mbytes on a fixed disk, Micro/Magnum 5/15 drives from DMA Systems (Goleta, Calif) use a closed loop tracking and positioning scheme. A half-height, removable-only drive, the model 360, stores 7.5 Mbytes and has a 98-ms access time. Onboard firmware allows cartridges to be formatted in the drive. This eliminates the need for the prewritten servo while retaining interchangeability.

A newcomer, Cardiff Technology Inc (San Diego, Calif) may soon produce a 40-Mbyte fixed/removable drive. The design may use a linear actuator with an embedded servo to achieve a 25-ms access time.

Plated media and thin-film heads should allow the unit to store 11,000 bits/in. at 980 tracks/in. on each platter.

Sporting a similar package but different media, Iomega's (Ogden, Utah) 8- and 5½-in. drives use Bernoulli technology to float the read/write head above flexible media. This media is encased in a rigid cartridge. The technique allows high density and fast transfer.

By 1986, vertical recording will be feasible in half-height, 51/4-in. drives with 330 Mbytes.

Stretched surface recording from 3M is another approach. The recording media is formed by stretching a flexible magnetic recording material over both sides of a rigid substrate made from a plastic-like material. The resulting magnetic surface retains sufficient resilience to allow contact recording at very high density. Tests have shown that the media can be used in Winchester drives with a slightly modified head design.

Commercial disk drive magnetic technology has attained 1-Gbyte levels on 14-in. platters with access times in the 16-ms range. A look to the future shows the possibility of 6 Gbytes and more than 700 Mbytes on 8-in. media with similar access times. By 1986, vertical recording is expected to appear and bring with it the possibility of half-height, 5½-in. drives recording 330 Mbytes. Optical disks in the 12-in. size range will stretch to 8 Gbytes per surface.

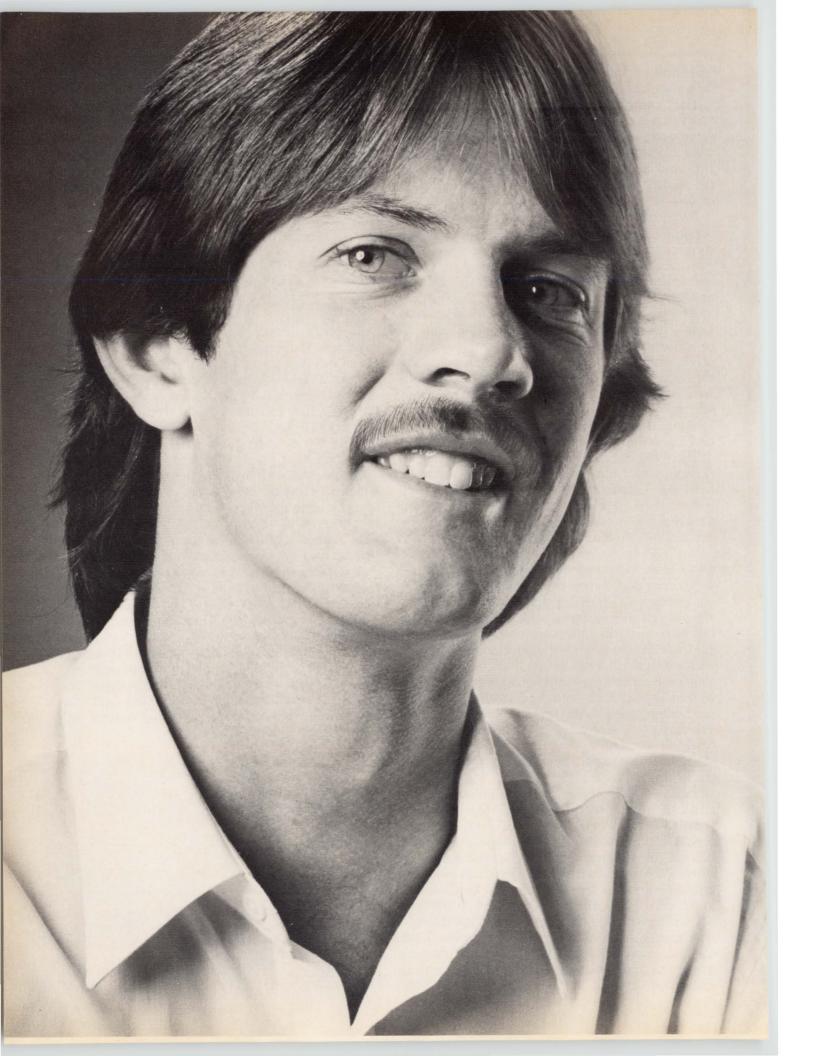
Magnetic tape also holds much potential. There, thin-film heads and vertical recording techniques should put half-inch cartridge capacities in the gigabyte range before 1990. Although we can only project the future, we do know that storage capacities will grow, speed of access will improve, and the needs of all types of future processing systems will continue to be met.

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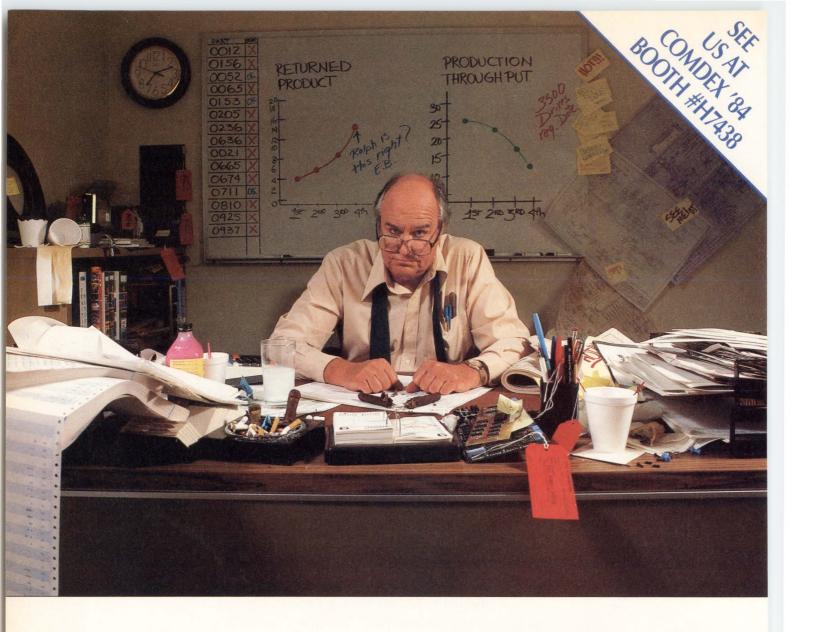
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OPTICAL MEMORY RESEARCH PAYS OFF

Delivering on promises to provide gigabit capacities, optical memories are coming into their own. At the same time, the pieces needed for the next generation of products are falling into place.

by Maarten de Haan, Chris Steenbergen, and Di Chen

Optical recording and reading techniques have been under intense development for the past 20 years. Today, data storage devices using these techniques are finally reaching maturity. For example, optical memory features are being incorporated into products developed by the video, audio, image, and digital data recording industries. The characteristics and performance of key components now in development will contribute to the optical data storage devices of the future.

Read only video disks, introduced in 1978, store 45,000 picture frames on one side of a 12-in. diameter disk. Because these frames can be randomly Maarten de Haan is director of development at Optical Storage International, 1050 S Academy Blvd, Suite 138, Colorado Springs, CO 80910. He holds a BS in mathematics, physics, and chemistry and an MS in physics, mathematics, and electronics, both from the University of Amsterdam, Amsterdam, The Netherlands.

Chris Steenbergen is manager of the media and systems evaluation group at Optical Storage International. He holds an Ms in technical physics and a PhD in technical sciences, both from the University of Technology, Delft, The Netherlands.

Di Chen was director of technology at Optical Storage International. He holds a BS from National Taiwan University, Taipei, Taiwan, an MS from the University of Minnesota, and a PhD from Stanford University. He is now executive vice president at Optotech, Inc, Colorado Springs, Colo. accessed, the disks have served as the basis for interactive video development. As a follow-up to this development, documentation storage devices have appeared. Toshiba, Philips, and Hitachi are among the first to announce such products. In this case, 10,000 pages of information can be written on one side of a 12-in. disk, and read at 0.5-s access time. Since the documents are stored as high resolution images (about 2500 x 1700 pixels), the required bit error rate (BER) is only 10^{-8} . This type of device is urgently needed in Japan since the written language includes Chinese characters that cannot be readily coded, and therefore, must be recorded as high resolution images.

Major electronics companies such as Matsushita, Sony, Sharp, and Canon have all responded to this need and joined in the development effort. Besides a single-disk write once/read only recorder, "Jukebox"-type systems containing up to 100 disks are also being developed. Documentation filing systems using this type of recorder and software with a page reader, hardcopy printer, and high resolution CRT or other display devices, are available for less than \$100,000.

Because coded digital data storage requires a BER of 10^{-11} to 10^{-12} , efficient coding and error correction schemes must be developed. A more rapid access time (about 250 ms) also calls for refinements in the servo and actuator design. After years of development, efforts in this area are finally bearing fruit. In 1983, announcements of devices by Hitachi, Optimem, Thomson CSF, STC, NEC, and OPL were made. These products fall into two categories: low end and high end.

On the low end, storage capacity is about 1 Gbyte/disk surface with 200-ms access time and a 2-Mbit/s

TABLE 1 Optical Disk Drive Systems										
Company	Disk diameter (in.)	Capacity Gbytes/ or page/ surface	Access time (ms)	Transfer rate Mbits/s	Direct-Read- After-Write	Bit-error rate 10-X	Size (in.), height, width, and depth	Revolutions/ min 480	Media Te alloy	
OSI	12						5¼ x 19 x 25			
Optimem	12	1.0	125	3	no	12	-	-	Bubble forming metal film	
STC	14	4.0	62	24	_	12	55 x 52 x 32	2000	-	
Thomson CSF	12	1.0	100	3.8	-	12	-	-	Bubble forming	
FOA*	12	0.6	350	2.4	modified	9	(28 x 18 x 25)	600	-	
Hitachi	12	1.3	250	2.3	no	11 to 12	(7 x 14 x 23)	600	Te alloy	
Matsushita	8	0.7	300	5		7	80 x 20 x 20	900	TeO _x	
Mitsubishi	12	37,400 frames	3000		no	-	-	1800	Metal film	
NEC	12	1.3 15,000 pixels	250	6.5	10.5	12	10 x 18 x 21	900	3 M media	
Sanyo	12	18,000 pixels	300	4	no	(5)	(28 x 18 x 25)	345	Te alloy	
Sony	8	9000 pixels		1 to 5.5	burst error detection			900	Sb ₂ Se ₃ +Bi ₂ Te ₃	
Toshiba	12	1.2	500	1.43	no	8	25 x 16 x 20	300 to 500	TeC	
Sharp	51/4	0.14 1000 pixels		-	no	8	5.Ta 160		magneto- optic erasable	

data rate. Most of the products announced belong in this category. On the high end (developed by STC. and demonstrated by RCA), the memory device capacity is 4 Gbytes/disk surface at a 120-ms access time, and a 3-Mbyte/s data rate. The performance characteristics of some representative systems are summarized in Table 1. Figs 1 and 2 show the capacity/access time relationship and capacity/data rate relationship, respectively, of the various optical recording drives from several companies.

The read only and write once/read only systems fall into the following categories with computer applications: archival storage, disk backup, journaling, information distribution, reference store, and online hierarchical storage. In consumer applications, the categories include video player and recorder; and compact disk sound system. Industrial and educational applications include interactive and intelligent video disk; sales, service, and cataloging video disk; and publishing business. When erasable optical memory becomes available, its applications will be the same as today's for the magnetic recording devices.

Applying optical techniques to data storage

Research and development efforts have been underway to apply the controllable energy source of lasers to data storage applications since its discovery. Early efforts concentrated on the investigation of the physical phenomena associated with the interaction between the material medium and the laser beam. These phenomena are useful for writing, reading, and erasure operations. Special attention has been focused on the development of erasable media, since researchers have believed that the laser beam addressable memory technology will replace magnetic recording technology.

Interest in inertialess electrooptic and acoustooptic beam modulation and deflection technology was directed toward addressing applications. The high areal density offered by the laser memory approach, coupled with the promise of inertialess addressing, raised worldwide interest. By the end of the 1960s, most major computer companies were engaged in optical memory work.

The realization that, technically, it is extremely difficult to make an inertialess beam deflection system that will address more than a 1000 x 1000 diffraction-limited beam locations, placed a limitation on the size of bit-oriented inertialess optical memory. A holographic recording approach based on a "one page per spot" operation was introduced to counter this limitation. This, however, required development of a block input device (or page composer), and highly sensitive media.

At the same time, the magnetic recording industry was steadily improving. Areal density of magnetic storage peripherals improved by a factor of two, every two to three years. Also, the technical problems associated with optical erasable inertialess

() = estimate

or holographic recording held back many research and development efforts in digital optical memory. Steady progress was made, however, in attempts to apply optical technique for write once/read only memory and video disk players. Laser video disk players were fully developed and produced, and an image/documentation file based on an optical direct-read-after-write (DRAW) disk was introduced in the late 1970s.

Current efforts in optical recording reflect the advantages and limitations of optical memory, and the need for mechanical motion in addressing. To-day's systems combine a rotating optical disk with an optical head that is driven by a linear motor for addressing. Media are almost exclusively made in disk form. The large head to media distance in the optical approach makes it possible to use removable media while maintaining extremely high areal density. Besides video disk, digital audio disk players have also been recently introduced. Alterable optical disks and double density DRAW disks are currently under development.

Status of optical recording media

Today, write once/read only media of various forms are well developed. The writing process used with these media is based on the laser heating effect that causes ablation, deformation, bubble forming, or melting.

The media's writing sensitivity and read out signal are enhanced by the use of multilayer structures that take the form of bilayer, trilayer, and quadrilayer media. These media use antireflective and reflective coatings. The sensitive recording material is protected by air sandwich lamination (Fig 3). In this case, the transparent substrate forms the protective barrier for the information layer. It also places the outside surface out of focus for the focusing laser beam. This barrier makes the media insensitive to dust and other contamination.

The header, tracking, and clock information must be provided by the unrecorded media to facilitate the storage operation. A pregroove technique meets this requirement. Media are pregrooved using a mastering machine that exposes a photo resistant layer on a polished glass plate. This creates a spiral or concentric groove, one-eighth of a wavelength deep over the entire disk. In the header region, header information is created by forming one-quarter wavelength deep depressions (Fig 4). In-track clock information can also be provided by varying the depth of the track in a sinusoidal manner. The resulting master disk is replicated through a galvanic process to produce a number of stampers. Pregrooved information on the stamper is replicated on a photopolymer layer coated on the substrate. Finally, the sensitive information layer is deposited on the disk, and an air sandwich is formed from two such disks.

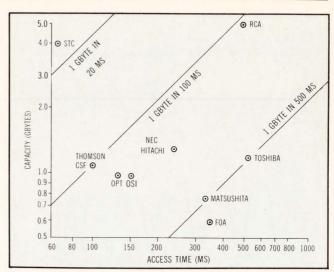


Fig 1 Optimal recording devices vary in both capacity and access time. The relationship between capacity and access time of various devices is plotted on the graph.

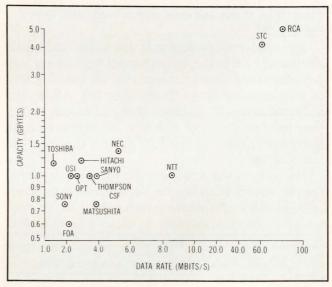


Fig 2 Announced optical storage devices exhibit various data transfer rates. The graph shows the capacity to data rate relationships of various devices.

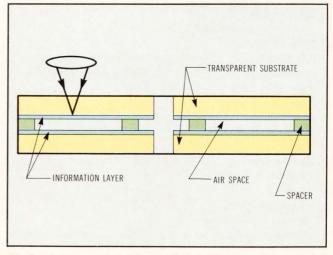


Fig 3 An air sandwich lamination technique protects the sensitive layer of recording material in optical disk media.

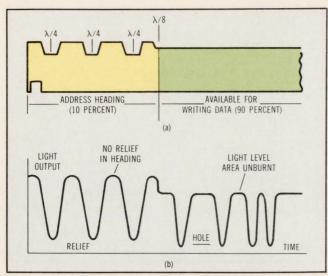


Fig 4 Cross section of pregrooved track in optical recording media cut along track direction (a) shows depth of grooves holding header and recorded data. Read-out signals from header and from recorded data dark spots are shown in (b).

The read only optical disk for video and audio applications uses the same stamper replication process described above, except that all information, as well as the grooves, is prerecorded. Aluminum is coated over the stamped disk to provide reflection for readout, and polymer substrates with an in-contact cover are used to protect the recorded information.

The most popular write once/read only material for the information layer is the ablative monolayer tellurium alloy. Phenomena such as the bilayer phase transition of materials such as antimony₂selenium₃/

TA	BLE 2							
Characteristics and Performance of Te Alloy Disk								
Capacity								
(12-in. diameter disk)	10 ⁹ bytes							
Bit-error rate								
(with error correction)	~10-12							
Bit-error rate								
(without error correction)	~10-5							
Life writing	>5 years							
Life reading	>10 years							
User band	32,000 spiral tracks							
Pitch	1.6 μm							
Track segmentation	32 or 64 sectors with							
	track ID							
Clock information	In track							
Weight	0.45-k (without cartridge)							
Birefringence	<10 nm							
Substrate transmittance								
factor	~0.85							
Refractive index	1.5							
Reflectance of sensitive								
layer	0.40							
Signal to noise ratio	= 50 dB							
Writing sensitivity								
(μm diameter pit)	10 mW/100 ns pulse/8 rps							

bismuth2tellurium3, refractive index change in tellurium oxygen_x caused by heating the bubble formation on material such as refractory metal coated polymer, and the deformation in bilayer dye polymer have subjected these materials to scrutiny. Gold island material and trilayer media using Te are also being considered for practical memory applications. Table 2 presents typical characteristics and performance of a Te alloy disk.1,2,3,4,5,6,7

Erasable media research considers the physical effects of certain materials. These include thermal effects such as Curie point or compensation point recording using magnetooptical material and amorphous-crystalline phase change recording. Also being researched are photon-induced effects such as photochromic and photo refractive effects and photon activated effects in thermoplastic and ferroelectric-photoconductive materials.

Some of the physical effects and typical materials explored for use as alterable media are summarized in Table 3.8 Currently, major efforts are underway to develop magnetooptical materials and phase transition materials, both based on thermal effects. The most favored magnetooptical materials under investigation are in the amorphous rare-earth-transitionmetal group. The use of amorphous material instead of crystalline material marks a distinct departure from the direction taken by earlier efforts. Crystalline material such as manganese/bismuth produces a high magnetooptical effect and therefore high readout signal. However, the fixed pattern medium noise associated with the grain boundary diffraction drastically reduces the signal to noise value of the material.

Amorphous material does not have as high a magnetooptical effect. However, since there is no grain boundary, the medium noise is greatly reduced, resulting in high signal to noise ratio. Development of media using the magnetooptical effect is underway at a number of companies. Table 4 summarizes the optical recording properties of some materials currently being studied. The highest signal to noise ratios are obtained by using a quadrilayer structure.

Another material that shows promise as an alterable optical memory media is the amorphouscrystalline phase transition material. The use of a short laser heating pulse causes the crystalline material to convert to amorphous, and a long, less intense heating pulse causes it to revert to the crystalline phase. Earlier material developed by Energy Conversion Devices suffers medium fatigue effect, therefore the number of erasure operations is limited. Matsushita, using germanium or arsenic doped tellurium oxide, has demonstrated over one million cycles of write and erase without degradation.9

To increase the number of tracks that can be written on the media, IBM has proposed a twowavelength approach where adjacent grooves are of

TABLE 3 Physical Effects Proposed for Alterable Optical Memory Applications Physical effects Typical materials Category GdTbFe, GdFe, ThFe, HnBi Thermally induced Curie-point thermo-magnetic GdCo magnetooptic compensation point coercivity reduction Co-P, Fe₂O₃ by heating thermoreminent CrO2 Te₈₈Ge₇As₅ TeO_x: Ge, TeO_x: Sn amorphous-crystalline phase transition VO₂ semiconductor-metal phase transition Photon induced photochromic F-center KBr F_A-center KCI with NaCl or LiCl doping M-center KaF photo dimerization Acridizimium, Toluene-Sulfonate LiNbO₃, BNN, SBN photorefractive linear nonlinear LiNbO₃, KTN YIG: Si photomagnetic TWF-PVC Photon Activated thermoplastic composite elastomer composite Ruticon single layer Bi₁₂SiO₂₀ ferroelectric-Bi₄Ti₃O₁₂-ZnS photoconductive two layer magnetooptic-Gd_{2.5}Yb_{0.5}Fe_{4.8}Al_{0.2} CdS photoconductive composite

different depths. The different depths cause each to be "seen" by only one of two laser beams of different wavelengths. Matsushita has proposed an alternative approach where adjacent tracks are tilted slightly from the norm in opposite directions. This directs the reflected beam to two detectors, while each detects the signal from only one of the adjacent tracks. Both of these approaches will allow track density to be doubled because no space is needed between neighboring tracks.

To improve the bit density along the track, a multiple bit per spot location has been proposed by IBM, using the photochemical hole burning effect in halide crystals. ¹⁰ In principle, this technique allows up to

TABLE 4										
Characteristics of Magnetooptic Materials Under Investigation										
	KDO	Sharp	Matsushita	NHK	NTT	NHK	3M	Philips	Xerox	
Recording media	TbFe	TbDyFe/	MnCuBi/		MuBi/	= = = = = = = = = = = = = = = = = = = =	DENIE STATE	-	-	
	GdTbFe	GdTbFe	GdTbFe	GdCo	MnCuBi	Cr ₂	Re to Tm	GoTbFe	TbFe	
Recording method	Tc	Tc	Tc	T _{comp}	Tc	Tc	T _{comp}	Tc	Tc	
Operating temperature (°C)	140/160	70/150	200/160	70 to -80	360/200	_		150	140	
Kerr-rotation angle										
(degree)	0.3/0.4	0.5/0.7	0.43/0.4	0.3	0.7/0.2	RIG to 1		0.5	0.3	
Disk diameter (mm)	120/200	140	120	150	135	300	300	50	76	
Substrate material	Glass/PMMA	Glass	Glass	Glass	Glass	Sheet	AI,PMMA	PMMA	Glass	
Rotation speed (rpm)	450 to 1800	720	400	1800	1000 to 2000	1800	1860	600	600	
Light source	GaAlAs	GaAlAs	GaAlAs	He to Ne	Ar	Ar	GaAlAs	GaAlAs	GaAIA	
Recording power (mW)	5 to 10	4.5	5	5.6	40 to 70	30 to 60	12	3	5	
Reproducing light source	GaAlAs	GaAlAs	GaAlAs	He to Ne	Ar	He to Ne	GaAlAs	GaAlAs	GaAlA	
Reproducing power (mW)	1 to 2.7	to 2	to 2	to 2	10 to 25	to 10	3	1	0.3	
Bit size (μm)	1	1	1	1	2	2 x 7	1 x 1.5	2 x 5	1	
Track spacing (μm)	2.5	2	5	3 to 6	5	15	1.7	10	1.8	
I/O signals	Digital	Digital	Digital	FM	Digital	FM	Digital	Digital	Digita	
Read/write speed (MHz)	0.5 to 2	2	2	1 to 5	0.5	10	10	0.25	1.1	
S/W, C/W (dB)	C/W-45	C/W-40	C/W-40	C/W-35		S/W-40	C/W-50	S/W-30	S/W-3	
Bit error rate	10-5		-	T	6.28 x 10 ⁻⁶	-	10-4,10-5	10 ⁻⁴ , 10 ⁻⁵		
Capacity/disk (Gbyte)	5.2	2.3	3.5	3.4		5.8	25	80 Mbit	1.5	
Sensitive layer thickness (µm)	0.025	0.015	0.02	0.2		5		0.05	0.035	

TABLE 5 Some Commercially Available Diode Lasers

		Power o	output	Threshold		Be	am		Polarization ratio numerical	Spatial	Axial
Laser structure	Wave-length (nm)	P _{CW} (mW)	P _{pulsed} 50ns	current I _{th} (mA)		diver	(Carrier Co.)	Astigmatism Z(μm)		mode (profile)	mode (spectral)
CSP	820 to 850	20	25	55	0.25 to 0.4	12°	30°	5	20:1	Near Gaussian	Single
1 CSP	800 to 830	7	10	30	0.36	110	40°	-	-	Near Gaussian	Single
TJS	800 to 830	15	15	25	0.4 to 0.5	9 º	32°	5	40:1 (1mW)	Near Gaussian (extra peak)	Single
TS	800 to 830	15	15	28	0.4 to 0.5	14°	40°	5	_	Near Gaussian	Single
DH (Single-M)	820 to 850	5	5	65	0.3	12°	40°	-	30:1 (2mW)	Near Gaussian	Single
SML	770	5	55	70	0.3	10°	36°	_	-	Near Gaussian	Single
LOC/CDH	800 to 830	20	40	100	0.4	10°	30°	8	60:1 (40mW) pulsed	Near Gussian	Single
DH multi-M	800 to 850	5	50	100	0.17 (cw) 0.4 (pulsed)	34°	60°	12 to 35	5:1 (1 mW)	"Rabbit ears"	Multiple
V-groove	780 to 800	20	20	100	0.20	30°	60°		-	''Rabbit ears''	Multiple

1000 bits of information to be stored in one spot location. However, the need for a cryogenic environment, and a precisely tunable laser make this approach impractical.

In an optical memory system, it is desirable to use one laser to perform both read and write operations. If the laser is not properly designed, however, the temperature and carrier density can change at the junction due to high power for write and low power for read. This can result in beam walk-off, wavefront distortion, wavelength shift, and noise generation. Low noise is required only during reading; high beam collection efficiency is needed for writing.

Status of laser sources

High efficiency, ease of modulation, and compact size make laser diodes the most practical energy sources for optical memory applications. All lasers currently in use are of gallium aluminum arsenide (GaAlAs) p-n junction type. Depending on the longitudinal mode structure, there are currently two types of lasers: single mode and multimode. Also, based on the waveguiding approaches, lasers can be divided into index-guided and gain-guided categories. Typically, index-guided lasers operate in single mode while gain-guided operate in multimode. Measured by wavefront distortion, the optical quality of indexguided lasers is typically better than that of gainguided lasers.

The optical beam emitted by a diode laser is fan shaped. The far field pattern is broader in the direction that is perpendicular to the junction than that parallel to the junction. Furthermore, the beam waists for the perpendicular and parallel directions do not coincide. The distance of these waists—the astigmatic distance—is typically tens of micrometers in a gain-guided laser, and only a few micrometers in the index-guided laser. Therefore, it is easier to collimate index-guided than gain-guided lasers.

On the other hand, single-mode lasers, although having very low noise under ideal conditions, exhibit mode hopping noise when current or temperature is changed. They also generate excessive noise when part of the beam is reflected back to the laser. Multimode lasers, although more or less immune to these noise problems, are inherently noisier.

To combine the best features of both laser types, noise suppression techniques are introduced. The noise problem in the single-mode laser can be suppressed either by high frequency modulation or by intentionally reflecting a substantial amount of light to the laser. The characteristics of some commercially available lasers are given in Table 5.

In the future, a shorter operating wavelength (<700 nm) will be needed to improve packing density. Higher power output (>100 mW) is required to improve data rate. Also, longer lifetime and immunity to electrostatic and electric transient damage are required to improve reliability.

The growth of optical memory technology will depend on technological advances in recording media, in laser diodes, and in optical transducer heads. Development of holographic optical elements will reduce the cost and weight of the transducer head as well as the access time. Improvement in transducer head design will be patterned after magnetic recording

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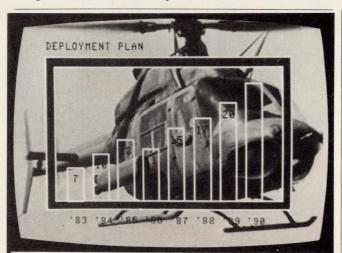
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technology. The counterpart of a plated thin-film magnetic head is an integrated optical head where the laser, optical components, and detectors are all integrated on a chip. The size and weight of the head is drastically reduced making delicate alignment procedures a thing of the past. Microelectronic techniques will be used for head fabrication, and costs will be reduced dramatically.

For strategic computing, a large transportable capacity (around 1012 bits) online memory is required. The requirement for transportability exerts volume and weight restrictions. When integrated optical heads become available, one may envision a 10¹²-bit optical memory that will have size and weight comparable to an IBM 3380 disk drive. This memory will provide a spindle with 20 optical disks read and written by 40 integrated optical heads at a 50-ms access time.

The outlook for technological improvement and optical memory device performance focuses on several areas. Erasable optical media will probably be available within two to three years. Double density media with no physical spacing between adjacent tracks will be developed over the next one or two years. A long-life laser diode with up to 100-mW peak power output and acceptable noise characteristics should appear in two to three years. Over the longer term, the developments in the next five to



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eight years may reduce the laser diode operating wavelength to the 700-nm range. Research efforts will lead to the development of holographic optical components within three to five years. Advances will result in integrated optical recording heads within 8 to 10 years.

Performance improvements that seem likely to result from these technological advances are just as significant. As media areal density approaches 109 bits/in.2, a double-sided 12-in. disk that can store 5 Gbytes of data should become possible. The improved laser diode output power and reduced wavelength will permit data rates that will reach 3 Mbytes/s. The use of holographic optical components leads to reduced weight and size of the optical carriage. This will allow access times of below 50 ms.

Erasable optical storage devices will be developed as erasable media become available. Availability of integrated optical recording heads will allow the development of an optical disk pack storage device. An optical transportable memory with 20 disks on one spindle at a 50-ms access time will be extremely attractive for fifth-generation computer applications.

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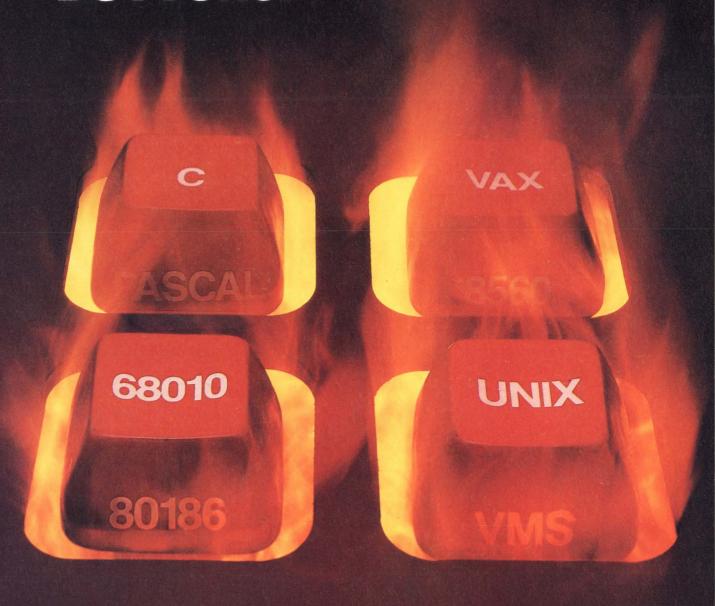
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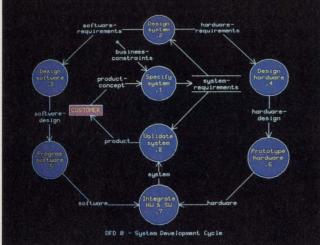
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SECONDARY STORAGE DEVICES LOOK TO THE LONG TERM

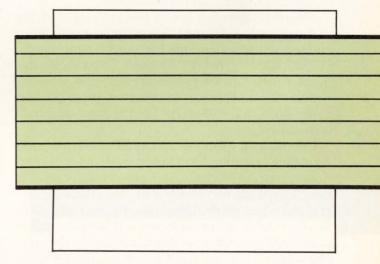
Secondary storage is now a primary concern—and a dilemma—for designers and users of computer systems. The problem can be solved for both the short and long term with intelligent tape drives.

by Larry D. Hemmerich and Peter Grohmann

How much capacity is needed and how fast it must be accessed depend on system size and application. But, the source of the dilemma remains the same choosing the right secondary storage device. The choice is becoming increasingly difficult, however. Disk storage requirements and per-spindle capacities are growing at an exponential rate. This is due to more sophisticated, complex, and user-friendly software; and the accumulation of data bases. Thus, with so many factors at stake, computer system designers and users can no longer give secondary attention to a system's secondary storage facility. Instead, they must quickly select, among many

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confusing options, the best way to protect, input, and retrieve their data.

Consider the results of the failure to take such actions, using the IBM PC/XT as an example. Hard disk storage has increased its online disk capacity by a factor of 30. This, in turn, has made it possible for PC users to join the Unix parade. But, the PC/XT's secondary storage remains unchanged. It is still a low capacity floppy disk. As a result, PC users find that in order to take advantage of IBM's Unix version, they must shuffle through 19 floppies,

Choosing the Right Secondary Storage Option

Short-range Concerns

Existing storage device form factors

System software

Applications

Product availability and price

Medium-range Concerns

Present and proposed standards

Current technology

Forecast product availability and price Long-range Concerns

Future technology

Future adopted and ad hoc standards

Future product availability and price

loading each software module in a specific sequence without error. Mainframe DP managers face a similar dilemma. Removable disk packs are a principal medium for secondary storage. But, as primary storage capacities climb over 1 Gbyte per spindle, the daily backup with bulky disk packs becomes extremely costly and chaotic.

Tape to the rescue

This puzzle calls for an across-the-board solution. Thus, not surprisingly, the answer is usually magnetic tape—an old standby coming to the rescue like an old-fashioned cavalry charge, but in new and different garb. Yet, even this solution introduces another problem: there are so many new magnetic tape devices, formats, interfaces, and controllers (see Computer Design, May 1984, p 29) that the choice is still a confusing and difficult one.

Magnetic tape devices vary from the very familiar to the recently developed. Some of the more mature and tested devices have not been significantly altered or upgraded in nearly 20 years. New half- and quarter-inch tape cartridges are just now receiving widespread acceptance. In addition, there are even newer units that will accept both quarter- and halfinch cartridges.

Choosing tape formats and interfaces is even more confusing and complex. Proven by decades of experience, tape is still the least expensive and easiest to handle medium for storing data. Yet, there are several older and many newer tape formats and interfaces available. Included in this mix are such unique innovations as tape units that are driven by disk-type controllers. The only common denominator is the tape itself.

Order can be made, however, out of this chaos. Products are not developed and brought to market unless there is a perceived or real need. These needs can be organized into three categories: short-range, medium-range, and long-range. The Table summarizes the principal concerns that narrow the options and simplify the decision-making process when this division is made.

Short-range or "quick-fix" concerns center on the existing investment in hardware, system software,

and applications. At the lower end of the computer system spectrum, fixed-disk capabilities have probably been increased without changing the form factors of the 51/4- or 8-in. drives. Chances are that the existing secondary storage is a floppy disk drive. From a hardware point of view, then, the quickest, least disruptive way to expand online secondary storage is to replace the floppy with a much higher capacity tape unit (20, 60, or even many 100 Mbytes, compared to a floppy's fraction of 1 Mbyte) with the same 51/4- or 8-in. form factor.

Computer system designers can no longer give secondary attention to the system's secondary storage facility.

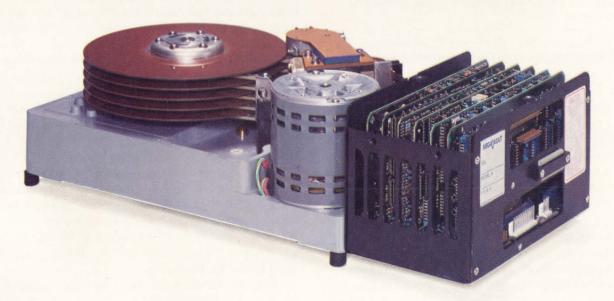
Recently announced half-inch cartridge tape units meet this criterion, but most of them are still at the introductory stage. They are, therefore, a risk when marketing considerations demand a fast, safe upgrade in the system's storage facilities. By comparison, quarter-inch cartridge units have been designed specifically for this application, and are currently mass produced. These cartridges are available from multiple suppliers, most of whom have elected to meet one or more of a set of industry-wide format and interface standards (QIC-02, QIC-24, or QIC-36).

Tape that looks like a floppy

Protecting an existing investment in software when expanding secondary storage presents its own problems, but is not impossible. Applications and system software are all based on random access floppy disk storage. File management utilities assemble records in floppy-sized sectors, track by track. The operating system includes a floppy driver, which assumes a floppy controller. In contrast, quarterinch tape is recorded serially in blocks or files. Although hardware form factors may be compatible when quarter-inch cartridge drives take the place of floppies, software for the two types of secondary storage devices is anything but compatible.

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Fig 1 A floppy tape device can greatly increase the online secondary storage capacity of floppy-based systems, without any significant changes in system software or controller hardware.

Fig 1 shows one solution to this dilemma. To the camera and the eye, the drive looks like a quarter-inch tape cartridge drive. To the host computer system, however, the device is a floppy drive. Information is stored in data structures that match the tracks and sectors of a floppy disk (Fig 2). The physical interface—control lines and handshaking procedures—are essentially the same as those dictated by the SA450 or SA850 floppy device interfaces. Thus, the same device controller chip or board can be retained and system designs can be upgraded by simply removing one device and inserting another.

In this way, software modifications that accommodate larger parameters and facilitate the streaming operation complete the conversion. A streaming tape obviously does not "step" from track to track. Instead, the tape is formatted by a cartridgeinitialization pass (similar to a floppy-initialization pass) into programmable-length sectors and "segments" (floppy tracks). There are up to 255 segments along each of six "streams" (streaming tape tracks), representing floppy disk surfaces.

Streams are chosen by interpreting the standard floppy disk drive-select and side-select interface signals (jumpers give the user a choice of seven different stream-assignment configurations). The tape drive then "steps in" or "steps out" a selected number of "tracks" by moving the tape forward or backward. Meanwhile, it counts the index marks that were recorded when the cartridge was initially formatted.

Streaming that looks like start/stop

Similar cost-effective options are available from half-inch tape units and larger systems. These systems need more secondary storage facilities to match fixed-disk units with hundreds of megabytes of capacity. Again, the objective is to obtain an immediate gain in online secondary storage without increasing the size of the system components. The additional secondary storage should have little or no impact on existing applications, system software, device drivers, or interface controllers.

Fig 3 illustrates one available option. To the eye, it is a compact half-inch streaming tape unit that can store up to 180 Mbytes on a single 10½-in. reel. To the host computer, however, it is a start/stop unit that preserves all of the system software, including all file management utilities and device drivers that are written for the start/stop format.

The high online capacity and compact size are made possible, because the tape has a streaming format. Interblock gaps are reduced to a small fraction of an inch. This increases the amount of data that can be stored on the same length of tape by 50 percent or more. In addition, this particular unit records that data at 6250 bytes/in., using a group code recording (GCR) format—nearly four times the figure for conventional recording at 1600 bytes/in., or nearly twice that of a double density 3200-bytes/in. recording.

Data transfer rates are also doubled or quadrupled (at an equivalent tape speed), helping to match the higher read/write rates of the new-generation higher capacity, higher performance disk drives. But, this benefit can only be realized if the tape continuously streams without falling behind or running too fast for the flow of data to or from the disk or host

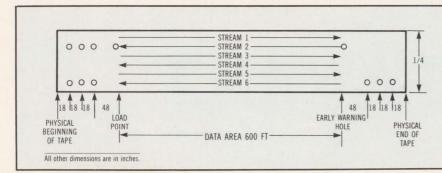


Fig 2 A streaming quarter-inch tape cartridge simulates floppy disk storage by substituting sequential tape segments for concentric disk tracks and tape streams for disk surfaces.

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computer. Several streaming tape units help keep the disk and tape transfer rates in unison by providing a large buffer space for overflows and underflows. The drive in Fig 3 carries this concept an important step further. Its "cache" electronics not only store the data, but also convert its structure from start/ stop records to streaming blocks. Thus, the interface to the host is identical to that of a conventional. start/stop drive. Consequently, no changes need to be made in any of the system software or even in the physical connection to the host.

Safety in standards

Standard interfaces and formats play a part in the evaluation process when short-range objectives are measured. In the options discussed previously, the quarter-inch tape cartridge can serve as a substitute for limited-capacity floppy disks. While the half-inch GCR tape unit can substitute for lower-capacity bulky, and expensive start/stop units by matching industry-wide start/stop standards.

The importance of standards increases as the solutions extend into medium- and long-range commitments. Although standards are not perfect forecasters (technology is too dynamic for that), they do provide a valuable guide to future trends and developments. Medium-range objectives look to currently available products, new and old, for a graceful transition to expand storage facilities. Any savings that might occur from past hardware and software investments are worth considering, but are not usually decisive factors.

Fear of product obsolescence is also minimal. It is assumed that within five years or less, the entire system, hardware and software, will be revamped. More important is the assurance that the selected storage devices will be available (ideally from multiple sources) during the next several years. This would encourage product competition and lower prices.

Naturally, the best way to be sure of device availability is to stay with well tested and top quality equipment. Most likely, no matter how large the market for half-inch tape cartridges becomes, it will



Fig 3 Cache-type GCR half-inch drive combines the capacity, economy, and size benefits of streaming tape with the simpler programming and easier implementation of start/stop tape.

never support six or more incompatible drive form factors, medium form factors, and data formats. Except for the marketing benefits that come with novelty, taking a chance on one of the new tape devices will be exactly that—a chance. On the other hand, given the current pace of change in secondary storage technology, a new device may emerge as a clear leader within a year or two and set a new de facto industry standard.

QIC standards

Quarter-inch tape products are generally adhering to one of the three standards summarized in Fig 4. As shown, QIC-36 is a basic interface that allows the user to format and record data on streaming tape, to detect and correct errors as they occur, and to retrieve data at a later time, using the same or a different drive. QIC-24, by comparison, establishes a standard format for the data. It calls for specified block lengths and a nine-track serpentine path that takes only moderate advantage of the available tape width. The QIC-02 defines a parallel data interface between a streaming cartridge controller and

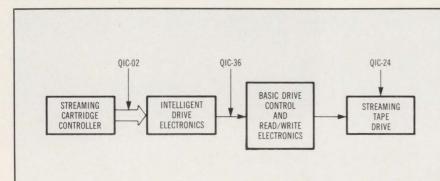


Fig 4 Format and interface standards are now bridging the gap between quarter-inch and half-inch cartridges. QIC-36 and QIC-02 define quarter-inch cartridge tape device interfaces; QIC-24 specifies a streaming-tape format that maximizes quarter-inch cartridge capacities by minimizing the distance between data blocks.

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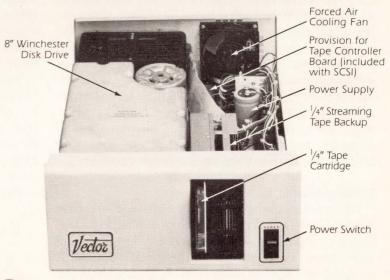
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Standards for higher capacity, quarter-inch cartridge subsystems are now being developed. The standards have also been applied to half-inch cartridge interfaces, providing an upwardly compatible growth route for systems based on the QIC standards.

New standards for half-inch tape

The same combination of established standards and soon-to-evolve standards applies to half-inch tape. If anything, existing half-inch standards have been even more firmly entrenched, and new developments on the horizon are even more revolutionary. Nine-track tape formats are almost as old as the ASCII code, and equally honored. They include the 800-char/in. nonreturn to zero inverted (NRZI) standard and the 1600-char/in. phase encoded format. Even the newer 6250-char/in. GCR has been an American National Standards Institute standard for the better part of a decade. The so-called Pertec tape drive interface, originally developed for the IBM plug-compatible market, has an equally long history. One of the few constraints in the computer industry has been standard magnetic tape on standard reels.

All of this is now subject to change. A variety of half-inch cartridges are, as mentioned, vying for a piece of the future. The likely winner is a completely new and different type of chromium-oxide coated, half-inch tape developed by IBM. This new tape cartridge can perform transfer rates up to 3 Mbytes/s at a tape speed of nearly 80 in./s. It can also record data on 18 tracks to produce a linear data density of approximately 38,000 bytes/in. (three times the linear bit density of the 6250-char/in. standard).

Of equal importance are the drives designed for the new format, which feature a very high level of intelligence and a 512-Kbyte buffer that almost guarantees continuous streaming, no matter how the data is organized by the system software. Stated another way, with this amout of local intelligence and memory, any debate over the merits of start/stop and streaming becomes an academic exercise.

Looking ahead

The amount and type of future drive intelligence become critically important when evaluating long-range concerns. In this case, system designers and users must take a gamble on the specific standard, adopted or *de facto*, that is likely to dominate the industry in 5 to 10 years. This standard will be the one able to offer the greatest chance of a variety of products from competitive suppliers.

A moderate step in the direction of increased drive capabilities is represented by the emerging Enhanced Small Disk Interface, now broadened to Enhanced Small Device Interface (ESDI). The original intent of the ESDI specification was to double the data rate of the *de facto* ST506 standard for 5½-in. Winchester disk drives and to move functions such as data separation from the controller to the drive itself. A subset of these capabilities is now being applied to tape devices.

More significant is the Small Computer System Interface (SCSI) architecture with up to eight peer level controllers or CPUs sharing a single SCSI bus, and up to eight disk or tape devices connected to each controller. SCSI streaming data rates can extend up to 4 Mbytes/s on a byte-wide bus.

Intelligent SCSI controllers can also relieve the host computer of such tasks as processing and controlling the transfer of data between primary and secondary storage devices. Both disks and tapes are connected through their controllers to a common bus. A single command—copy—can therefore initiate a disk-to-tape or tape-to-disk transfer without any further involvement by the host processor.

The proposed Intelligent Peripheral Interface (IPI) standard goes even further, with an upper limit of 10 Mbytes/s in data streaming mode on two bytewide bidirectional buses. Only eight devices can be active on the daisy chain IPI buses at the same time. But, up to 128 disk or tape drives can be addressed by the IPI protocol.

The IPI interface allows tape drives to perform multiple block operations, bursting data in increments that take only 175 μ s of bus connect/disconnect time. IPI Level 3 intelligence also reduces system costs by eliminating the need for an intermediary tape controller. The drive is attached, instead, directly to the IPI bus. Moreover, both disks and tapes can share a common I/O channel, with a single set of high-level IPI commands controlling the transfer of data to and from both types of devices.

Tape drives meeting these specifications are now available as off-the-shelf products, although it may be several years before their full potential is realized. But, if computer system designers and users need to meet enhanced secondary storage requirements for the long-range future, then one of these intelligent tape drive designs should be a viable option.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

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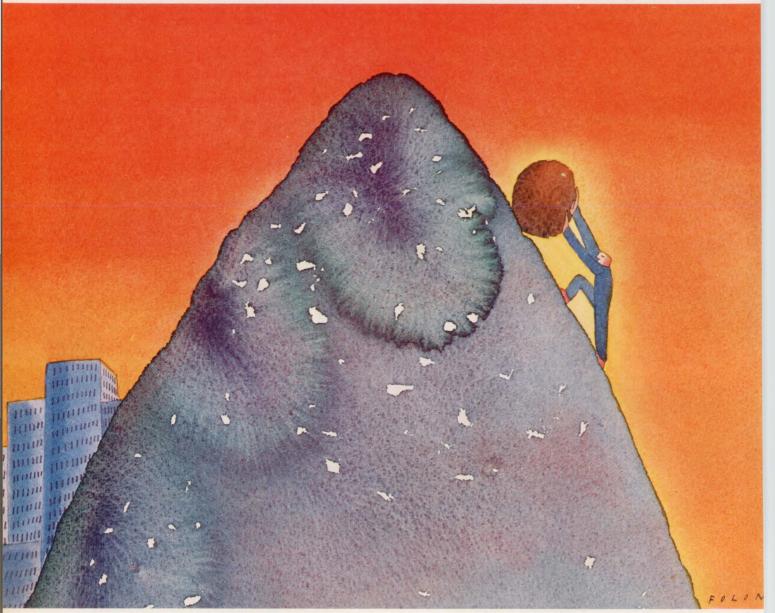
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DISPELLING THE MYTH ABOUT SINGLE CHIP MICROCOMPUTERS.

This is the first in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.



Single chip microcomputers are marvels of advanced electronic technology. Going beyond even the tiny architectures of today's general-purpose microprocessors, they combine the functions of multiple chips to form a single-device solution. Indeed, they are awesome machines.

But after their introduction, myths grew up around MCU's. Designers believed that they were difficult to design with; that there wasn't sufficient hardware and software support for them; that those who selected them would get a Sisyphus Complex. Sisyphus, you remember, is the character in ancient Greek mythology who was condemned forever to push a rock up a hill. Just as the rock reached the top, it escaped Sisyphus and rolled back to the bottom.

Some MCU's, no doubt, deserve the stigma of this myth. But one definitely does not. Zilog's Z8* MCU Family. For there is more than enough evidence to prove that the Z8 chip is not only the fastest MCU around, but it's the easiest to work with, too. In fact, it should be the chip of choice for any dedicated control applications that must get to market

on time—even if you need large quantities of them to fill your needs. Because the Z8 device is available now for off-the-shelf delivery.

But what does ease of design mean to you? What do you look for when you select a chip? What do you need to make your job easier? Whatever it is, you'll find Zilog provides everything you need, and more:

- Hardware and software development tools
- An existing software base
- Factory and field sales support
- Preproduction parts supplies

Z-SCAN™ 8 PROVIDES REAL-TIME EMULATION CAPABILITIES.

Zilog's Z-SCAN 8 is an in-circuit Emulator with a combination of hardware and sophisticated software that gives you efficient, interactive emulation of the entire family of Z8 microcomputers. By the simple exchange of target devices, the selected Z8 MCU can be emulated in a real-time mode that gives you the ability to inspect and control the tested environment. It also gives you real-time trace speed up to 12 MHz, two breakpoints, single-step capability and extensive mappable memory. All to ensure that you get an accurate simulation of your Z8 operating environment.



The Z-SCAN 8 Emulator is a combination of hardware and firmware that allows efficient, interactive emulation of the Z8 MCU. When hooked to an IBM PC software host, Z-SCAN 8 provides real-time, in-circuit development system capabilities. The Z-SCAN 8 will connect easily to other PC's making it a highly versatile unit.

The Z-SCAN 8 operates with both Zilog systems and other 8-bit development systems running CP/M* and/or other operating systems. Its standard RS-232 serial link makes it particularly useful with the IBM PC and other CRT terminals. Hardware and software debugging is fast and convenient. Two screens display the status of the Z-SCAN 8 monitor and Z8 MCU target resources. Target memory can be displayed and modified in a scrollable window. Moreover, the Z-SCAN 8 is interactive and easy to use. Commands are selected from menus and command arguments are self-prompting.

The set-up procedure and initialization for the Z-SCAN 8 is done for you—a unique feature in itself. The Z-SCAN 8 is designed to reduce design time. But it's not the only time-saving device Zilog provides for the Z8 MCU.

THE Z8 MCU DEVELOPMENT MODULE CUTS HARDWARE AND SOFTWARE DEVELOPMENT TIME.

The Z8 Development Module (DM) features two 4K Z8 devices on a single-board microcomputer. It's designed to assist you in the development and evaluation of hardware and software designs based on the Z8 MCU. With it, you can easily build a prototype using the Z8 prototyping device, and then develop code that will eventually be mask-programmed onto the Z8 on-chip ROM.



The Z8 Development Module allows you to build a prototype using the Z8 prototyping device, thereby developing code that will eventually be mask-programmed into the Z8 on-chip ROM. The Module is a single-board microcomputer system designed to develop and evaluate hardware and software designs based on the Z8 family.

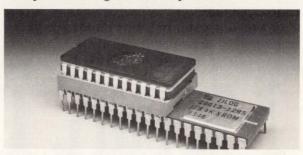
The Development Module connects to the CRT terminal and host system through two on-board RS-232 serial ports. So the DM fits between the CRT and host. A simple command makes the DM transparent in the serial path, which allows software

to be developed on the host-resident assembler without disconnecting the DM from the CRT and host.

The DM has a range of features to make Z8 designs easier than you ever thought possible: • 4096 bytes of static RAM for convenient creation and debugging of user code; • an on-board socket that tests user code in a 2716 or 2732 EPROM; • up to 4096 hardware breakpoints on address compare that can cover the entire internal ROM space; • a wire wrapped area for prototyping; and much more.

Z8 MCU DEVELOPMENT SOFTWARE SPEEDS UP DESIGN TIME.

Zilog also provides you with a growing library of sample programs and convenient assembler packages to help you get started testing your Z8 MCU designs. In our Subroutine Library, for example, there's our arithmetic subroutine, an I/O subroutine and a general control subroutine. What's more, there are several versions of the Z8 device: a 2K and 4K ROM version; a ROMless version; and a Protopak for prototyping. Each offers different memory addressing structures. Zilog is developing more all the time. Plus, there's an existing software base for all the Z8 MCU's. We can provide you with samples of designs currently in use.



The Z8613 MPE is used for prototype development and preproduction of mask-programmed applications. The Protopack is a ROMless version of the standard Z8611, housed in a pin-compatible 40-pin package.

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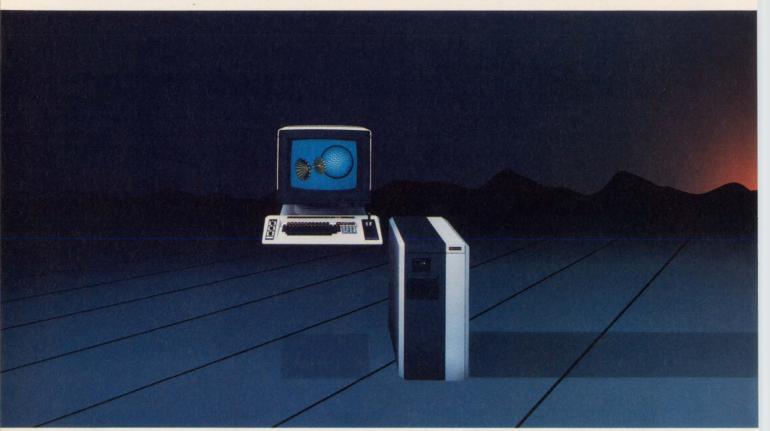
From the factory to the field, Zilog provides support at every level. A worldwide field sales network stands ready to help you with both hardware and software support. And you can get all the Z8 MCU's you need right now. Yields for the device are up 40%, and price reductions reflect our new supplies. What's more the upcoming Z8 Super 8" promises a smooth migration path for today's Z8 MCU family.

Zilog's Z8 single chip microcomputer. Believe the myths. Or get the facts. If bringing your product to market is important to your business, then design with the part that does more for success than any other. The Z8 MCU makes getting over the design hill and into production a lot easier than you might think.

For more on the Z8 MCU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call (408) 370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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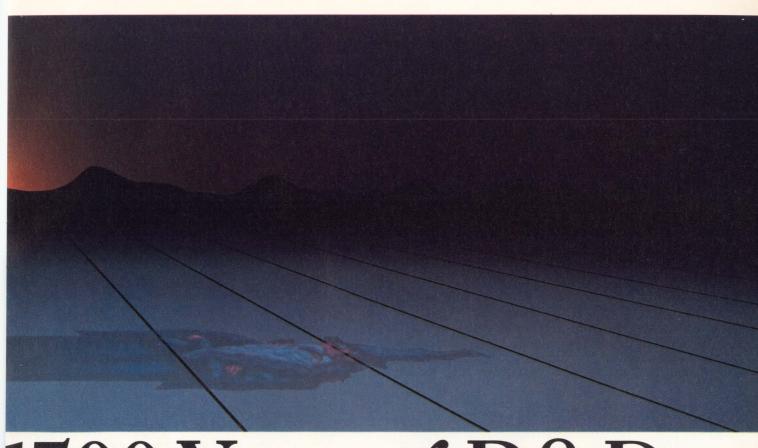
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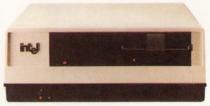
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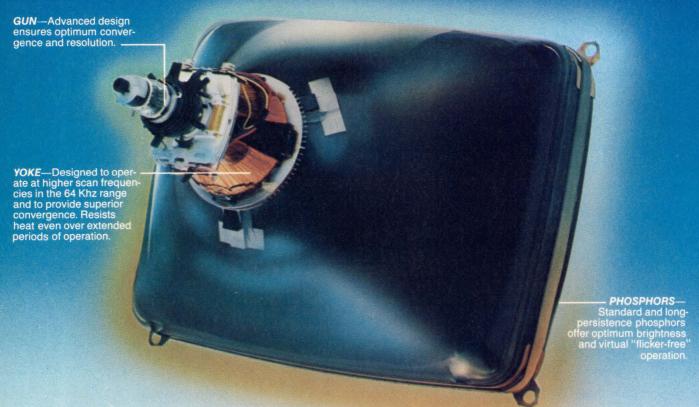
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	10" (9V)					0.31		
Availability Dot trio pitch (mm)	12" (11V)					0.31	0.37	0.47
	14" (13V)		0.2	0.31	0.25	0.31	0.4	0.4
	16" (15V)			0.31		0.31		
	20" (19V)	0.25	0.25	0.31		0.31	0.44	0.56
	26" (25V)			0.37				
Screen	Structure	Dot	Dot	Dot	Dot	Dot	Dot	Stripe



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CARTRIDGE DISK MEETS NEEDS OF PORTABLE SYSTEMS

Fast access, large capacity, and removability are key data storage criteria. Cartridge disks combine all these in a single low power device.

by Dick Troutte

Space, weight, and power are three critical factors in portable computer designs. They have kept designers away from hard disk mass storage devices. Floppy disk drives, on the other hand, lack the performance and capacity of Winchester hard disk drives. Traditionally, systems using fixed-disk Winchester storage devices needed an additional removable media unit—usually a floppy drive. Thus, additional space, weight, and power were traded for the speed and capacity gained when using this storage device combination. Today, by merging the advantages of floppies, cartridge tape, and Winchester disks in a single mass storage device, the hard disk cartridge drive eliminates these penalties.

The cartridge drive offers large capacity, high transfer rates, and removable media, without a second drive. The current standard configuration combines a Winchester drive with 10-Mbyte or more capacity and at least one floppy drive. A Winchester

cartridge drive can emulate the dual-device configuration in a single half-height unit. This smaller unit supplies the weight and power consumption ideal for portable computers.

In portable computer design, mass storage options that fit into the standard half-height, 5½-in. form factor are the floppy disk, tape cartridge, Winchester cartridge, and fixed-disk Winchester. Each of these has a standard width of 5¾ in. and behind-the-panel depth of 8 in. The parameters listed in Table 1 are for typical devices in each category.

Storage alternative to portable systems

Floppy disk drives benefit from a long history of high volume production and usage. They are the least expensive and require the least power of the four mass storage devices listed. In addition, the floppy drives can offer capacities over 1 Mbyte.

Dick Troutte is president of DMA Systems Inc, 601 Pine Ave, Goleta CA 93117. Mr Troutte holds a BS from California State University, Fullerton and has completed advanced studies at Stanford University.

TABLE 1
Storage Alternatives for Portable Computers

Height	Weight	Power
1.625 in.	3.6 lb	12 W
1.625 in.	3.0 lb	21 W
1.625 in.	3.3 lb	19 W
1.625 in.	3.0 lb	22 W
	1.625 in. 1.625 in. 1.625 in.	1.625 in. 3.6 lb 1.625 in. 3.0 lb 1.625 in. 3.3 lb

According to some designers, however, floppy technology is close to exceeding the potential data track density of its environmentally sensitive, flexible film media. In addition, the direct abrasive contact that occurs between the read/write head and the recording surface limits possible rotational speed and, thus, the rate at which data can be transferred to and from the drive.

Streaming tape cartridge drives dramatically increase the amount of data that can be stored without changing media—up to 60 Mbytes on an extra-length quarter-inch magnetic tape cartridge. However, the technology's sequential access method makes location and retrieval of a given record or file slow. Data is recorded serially, requiring repeated winds and rewinds to reach a selected track. Data transfer rates are also limited to about 90 Kbytes/s. The quarter-inch tape cartridge, therefore, serves a secondary backup role in a high performance computer system, while providing an ideal medium for low cost archival storage.

The half-height Winchester cartridge requires twice as much power as a floppy, but can store up to 10 Mbytes on a single cartridge disk. That is more than enough to provide primary storage for a single-user portable computer. In a Winchester-technology type device, with coated media and flying heads, the drive can accept and return data at the standard 5½-in. Winchester rate of up to 600 Mbytes/s. There is no reason why these figures cannot increase as the industry moves to higher performance interfaces such as the Enhanced Small Disk Interface (ESDI) now being considered by an American National Standards Institute (ANSI) committee.

The fixed disk Winchester was the only 5½-in. device capable of providing the high online capacities and throughputs required by many personal computer software packages. These half-height, fixed-disk, Winchester drives have standard ST506 interfaces and capacities up to 12 Mbytes. Again, higher capacities and transfer rates can be expected as Winchester technology evolves.

Various useful combinations of these storage devices are listed in Table 2. Assuming that the design objective is a complete storage system with

the capacity and transfer rate of a Winchester drive, plus the removable media essential for I/O functions, portable computer designers have four options. Three of these are to combine a fixed-disk drive with one of the removable-media devices. The fourth is to take advantage of the removability built into a Winchester cartridge drive.

Dual-device systems impose several design problems. There is a size penalty whether or not the two drives are placed side by side or the fixed-disk unit is buried inside the system. The size disadvantage is greater when one or both of the devices are packaged separately and connected to the computer by a plug-in cable. Floppy disks and tape cartridge drives lose their weight and power advantages when combined with a fixed-disk device. The combinations' additional controller circuits, device connectors, and cables add space, weight, and power, even when using a common set of dual-purpose, device controller chips. In addition, two device drivers must be included in system software.

Single device storage system

The single controller advantage of the Winchester cartridge drive enters into the fourth option: an all-Winchester system consisting of two drives—one fixed and one removable. This system is best for applications requiring more online storage than is available in a single cartridge. The same interface applies to both drives, allowing a multi-unit disk controller to perform the task.

TABLE 2
Alternative Fixed/Removable Storage Combinations

Storage System	Total Height	Total Weight	Total Powe
Winchester cartridge	1.625 in.	3.3 lb	19 W
Fixed-disk Winchester/ floppy disk	3.25 in.	6.6 lb	34 W
Fixed-disk Winchester/ tape cartridge	3.25 in.	6.0 lb	43 W
Fixed-disk Winchester/ Winchester cartridge	3.25 in.	6.3 lb	47 W

Winchester-level storage systems have the highest power requirements possible for a battery-operated system without needing frequent recharging. The all-Winchester combination is probably beyond the practical limit for truly portable systems. But, it is worth considering for a "transportable" computer system.

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495				16SE						1
1195	General Purpose	DT2801	12	or	13.7	12		16		
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1295	Low Level	DT2805	12		13.7			1		
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provides all the system's storage requirements, including program loading, archival storage, and backup protection for data.

The Winchester cartridge drive delivers the same device reliability and low error rate as a fixed-disk Winchester system. This is an important consideration in a computer system located far from the usual sources of technical or service support. In addition, a single Winchester cartridge can contain software and data sufficient for an effective software environment. If stored on floppies, 10, 20, or even 40 separate disks might be required to assemble the right combination of system software, application software, and source information.

The Winchester cartridge can serve both as primary storage and as a distribution medium. This eliminates the need to transfer data from one format to another. The two cartridges can efficiently distribute and store applications such as word processing or spreadsheet packages. With 10 Mbytes of storage available on each cartridge, not only the specific application, but also the appropriate operating system, utilities, device drivers, and tables can be stored on each disk.

Within the limits of the cartridge's capacity, no changes in system software are required to reflect that only one device is attached to the system. As illustrated in Fig 1(a), the disk surfaces can be divided into two or more logical or "pseudo" storage devices. For the sake of software compatibility, data or software modules can be copied from "secondary" to "primary" storage on the same disk for processing or execution.

This concept can be applied to achieve the minimum storage requirements for compatibility with the IBM Personal Computer/Interactive Executive (PC/IX) operating system [Fig 1(b)]. For compatibility with the Unix-based PC/IX, most of the cartridge's capacity is partitioned off as a logical hard disk drive. The balance is divided into one or more logical floppies with standard IBM capacities of 160 or 180 Kbytes for single-sided diskettes, 320 or 360 Kbytes for doubled-sided diskettes.

Protecting data in portable units

The same primary/secondary storage concept can be applied to data backup. Copies of the data can be recorded either as the data is entered [Fig 2(a)] or as a separate backup operation in which selected data fields can be copied from one section of the disk to another [Fig 2(b)]. Either method preserves the data integrity until the data is transmitted to a home office for conventional backup, or brought into the office for transfer to an established backup medium: tape, disk, or floppy.

The most obvious Achilles heel of Winchester technology in portable applications is the direct headto-media contact when a computer is powered down

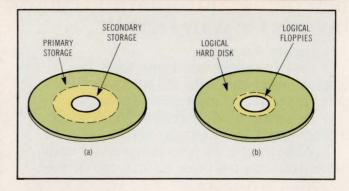


Fig 1 The 10-Mbyte capacity of the Winchester cartridge can be divided into logical or "pseudo" disks to emulate primary and secondary storage functions (a). The minimum storage requirements for the IBM Unix-based PC/IX operating system can be simulated by dividing the cartridge into a logical hard disk and one or more floppies (b).

or in transmit. The disk stops rotating and the heads rest on the recording surface. Some form of protection must be provided to prevent damage to the media or the heads. The safest solution is to lift the heads off the disk surface and to retract them completely. Only if a cartridge is fully seated in the drive is it safe to power up the drive, extend the heads, and dramatically lower them to their flying height above a disk that is already spinning at full speed.

This is achieved simply by mounting the upper and lower head assemblies on spring steel arms. Stationary wedge-shaped cams force the arms apart, lifting the heads off the spinning disk as the head carriage is retracted. Extending the carriage has the opposite

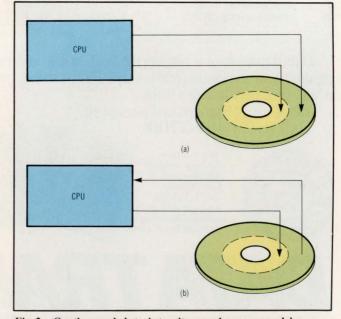


Fig 2 On-the-road data integrity can be preserved by recording data twice on different sections of the high capacity Winchester disk (a). Conventional backup functions can be emulated by copying selected records from one section of the disk to another as a separate computer operation (b).

effect; this motion lowers the heads to their read/ write positions after a protective air bearing has been formed between the heads and the revolving surfaces.

A single Winchester cartridge drive delivers the same device reliability and low error rate as a fixed-disk Winchester system.

Using this technique, Winchester cartridge drives with fully retracted heads have withstood typical baggage handling shocks up to 50 G without damage to the drive or the cartridge. The addition of a linear retraction mechanism, however, extends the length dimension of the drive beyond the 51/4-in. form factor. Part of the solution is to design the drive as a pull-out drawer, like the turntable drawer of an old phonograph console. The drawer design allows the cartridge to be top-loaded on the disk spindle, further reducing the chance of damage to cartridge or drive. The drive extends in front of the mounting panel, giving the user a handle to grasp the drawer and pull it out when loading or unloading a cartridge.

To squeeze a 3/4-in. high Winchester cartridge into a 1.625-in. high box requires the use of minia-

ture permanent magnet dc servo-drive motor with roller bearings to stabilize the spinning disk. A PC board wraps around the drive's mechanical components, and the spinning disk surface generates a flow of filtered air.

Media costs are reduced by eliminating the process of prerecording embedded-servo data on each cartridge before it leaves the factory. Instead, the drive itself is directed to record servo data the first time a cartridge is used. The recorded servo data, including a calibration track to correct out-of-round or offcenter conditions, ensures interchangeability when the cartridge is subsequently reloaded into the same or a different drive. The drive controller is like that of any 51/4-in. Winchester drive, with the addition of signal lines to direct the operator to replace the cartridge, to check that the cartridge has been inserted and is fully latched, and to instruct the drive to write servo data.

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TN 22-W1M1	3.5	5	2600	105	17	3600	40	22	13.3
TN 38-T1N1B	12	30	3800	170	225	4350	60	38	19
TN 38-T11N1B	12	30	4000	175	210	4600	60	38	17
TN 54-S1N1B	8.5	35	2500	210	220	2900	70	54	16.2

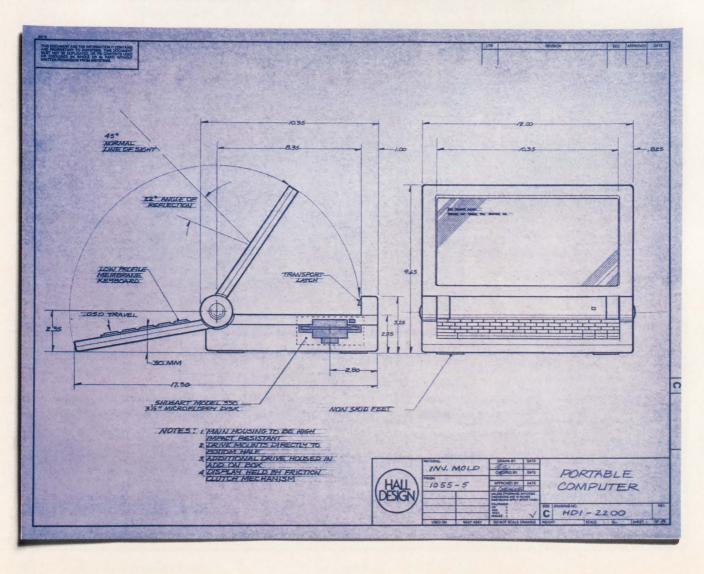
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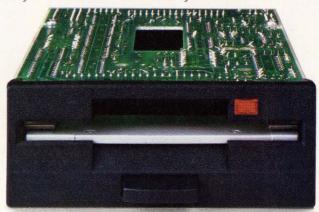
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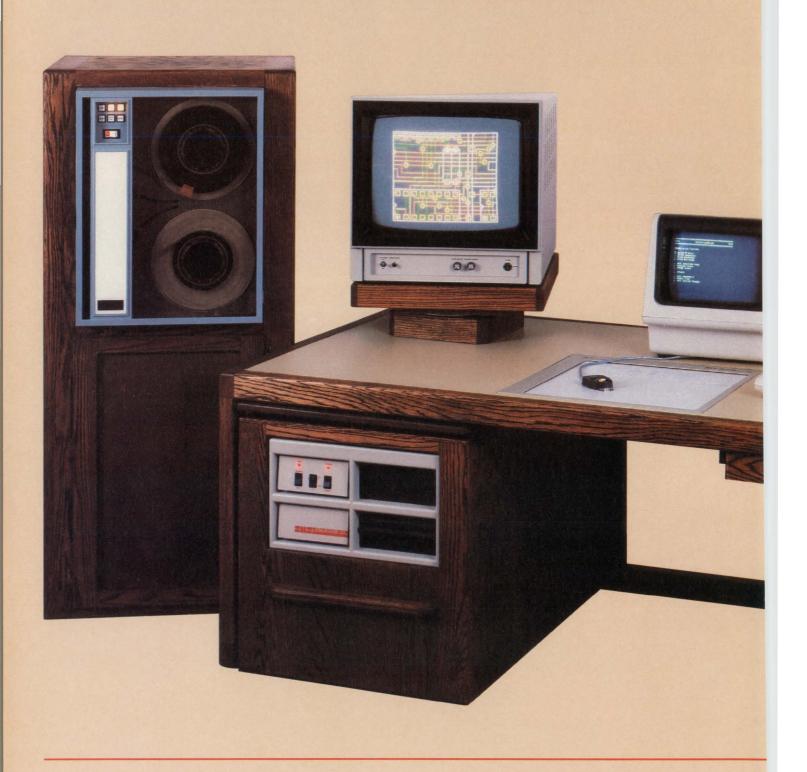


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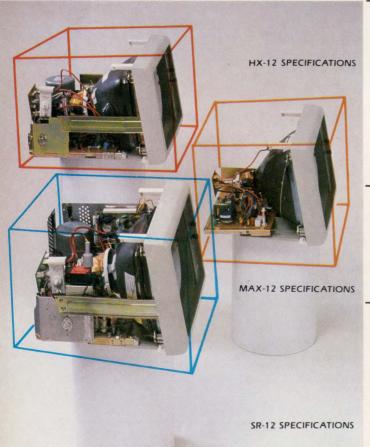
Misconvergence

Display colors

Characters Input Connector

Display size

Resolution



12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22) Input Signals R, G, B, channels, Horz Sync, Vert Sync, Intensity-Video Bandwidth 15 MHz Horizontal: 15.75 KHz Vertical: 60 Hz Scan Frequencies Display Size 215mm x 160mm Resolution Horizontal: 690 dots Vertical: 240 lines (non-interlaced) 480 lines (interlaced) Misconvergence Center: .6mm max Corner: 1.1mm max **Display Colors** 16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels 2000 characters (80 characters x 25 rows—8x8 dots) Characters 9 Pin (DB9)—cable supplied to plug directly to IBM PC Input Connector 12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor) Input Signals Video signal, Horz Sync, Intensity—positive TTL level Vertical Sync—negative TTL levels Video bandwidth Horizontal: 18.432 KHz Vertical: 50 Hz Scan frequencies Display size 204mm x 135mm Horizontal: 900 dots Vertical: 350 lines Resolution Input Connector 9 Pin (DB9)—cable supplied to plug directly to IBM PC 12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels Input Signals

> 9 Pin (DB9)—cable supplied CIRCLE 58

Horizontal: 31.5 KHz Vertical: 60 Hz

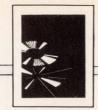
Vertical: 480 lines (non-interlaced)

Center: .5mm max Corner: 1.0mm max

16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels) 2000 characters (80 characters x 25 rows)

215mm x 160mm

Horizontal: 690 dots



TWO-CHIP SET TACKLES DISK CONTROL PROBLEMS

Handling data separation functions before passing data to the disk controller lets a two-chip disk controller supply high data transfer rates, while ensuring design flexibility.



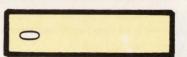
by Mark S. Young, Pradeep Padukone, and **Neil Adams**

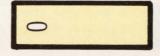
Designers attempting to integrate Winchester and floppy disk drives into systems are faced with a complicated and demanding task. To coordinate the activities of an asynchronous, analog device (the disk) with a synchronous, digital interface (the computer system), several major problems must be solved. Special analog circuitry is necessary to synchronize and decode data pulses coming from the disk during a read operation. Complex algorithms are required to improve relative read or write speeds. Attention must be paid to data recovery methods as well as to error detection and correction. In addition, software support and system interface overhead must

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Pradeep Padukone is senior product planning engineer at AMD. He holds a BE from Bangalore University and an ME in electrical communication from Indian Institute of Science, both located in Bangalore, India, and a PhD in systems engineering from Oakland University, Rochester, Michigan.

Neil Adams is a senior engineer at AMD. He holds a BS in physics and electronics from Manchester University, Manchester, England.





be carefully considered in order to ensure effective communication with the computer system.

These problems have been addressed by specialized disk interface chips. A lack of sufficient onboard intelligence, however, limited their success while higher bit densities, advanced encoding schemes, and faster data rates made the job more difficult. In a renewed attack on the problem of providing a cost-effective interface between disk and computer system, a two-chip controller set segregates the data separation function from other tasks to maximize disk I/O.

Addressing disk control issue

The Am9580/Am9581 chip set addresses issues related to controlling disk drives. The Am9580 hard disk controller (HDC) is a MOS VLSI Winchester floppy disk controller, and the Am9581 is a bipolar disk data separator (DDS). The two-chip set performs three basic functions: disk format/ control, data separation/data encoding and decoding, and data transfer to and from system memory. When used together, the chips provide a complete solution to Winchester/floppy disk control (Fig 1).

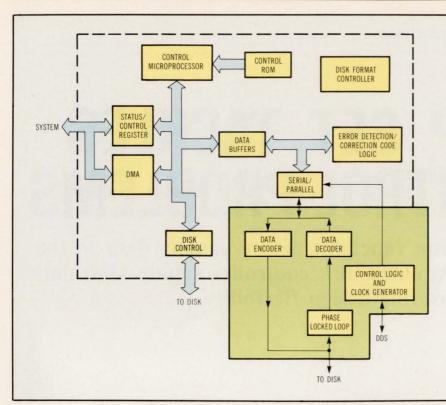


Fig 1 Typical disk controller block diagram shows the partitioning of the hard disk controller (HDC) and the disk data controller in the disk subsystem.

Alternatively, the system designer can customize the controller by adding and deleting features of the chip set with pin straps or software.

The HDC can link the system, via a DMA/CPU interface, to up to four Winchester or floppy disk drives in any combination. On the disk side, the chip's data format controller is fully programmable for disk data and format fields to be accessed. A built-in, 16-bit CPU with powerful software algorithms links the disk and system control units to handle disk control and data transfers. All basic disk controller functions are provided on the HDC: DMA for data transfers, dual-sector buffers for data buffering, Reed-Solomon error detection/correction codes (EDC/ECC), a data format controller, floppy ST506/412HP/custom disk control interfaces, and disk macro commands to assist operating systems in maximizing disk I/O. The companion DDS chip provides a total digital and analog solution to interfacing disks with serial transfer from 125 kbits/s to 15 Mbits/s.

Providing the HDC (or any disk controller logic) with a serial data stream frontend processor gives the DDS separate read write channels. (See Fig 2 for a detailed view of the chip's internal architecture.) In addition, extra control logic supports address mark functions, run-length limited (RLL) codes, and drive select and drive error functions.

The bipolar DDS chip provides stable data during read operations by using an integrated phase locked loop (PLL) to synchronize the disk data for decoding. This improves performance by allowing higher operating frequencies, supplies better noise immu-

nity than discrete implementations, and minimizes costs by eliminating external components.

An onchip, second order, low pass filter within the PLL allows the bandwidth to accurately track the data rate without the noise and cost associated with an external filter. This low pass filter determines the lockup time of the PLL to the raw disk data. Worst case lockup is 2 bytes, regardless of the data rate.

To support data transfer speeds of both floppy and hard disk drives, the PLL handles both the 125-to 500-kbit/s and the 5- to 10-Mbit/s serial transfer speeds. They use the crystal clock to determine the exact frequency. No external components are necessary to adjust the operating speed of the PLL to handle data transfer rates within either the 125-kbit to 1-Mbit/s floppy range or the 4- to 16-Mbit/s Winchester range.

Chip handles Winchesters and floppies

In addition to synchronizing the serial data pulses from the disk, the DDS chip also provides frequency modulation or modified frequency modulation (MFM) decoding. This decoding, in combination with the write channel encoded in the DDS, allows the HDC/DDS chip combination to handle both floppy and Winchester drives without additional logic.

Encoded data/clock pulses are translated into nonreturn to zero (NRZ) data in conjunction with a data reference clock. Disk data formats include special synchronization patterns (address marks) on the disk that allow byte field synchronization for the controller logic. Address mark detection/generation takes the form of a clean control handshake to the



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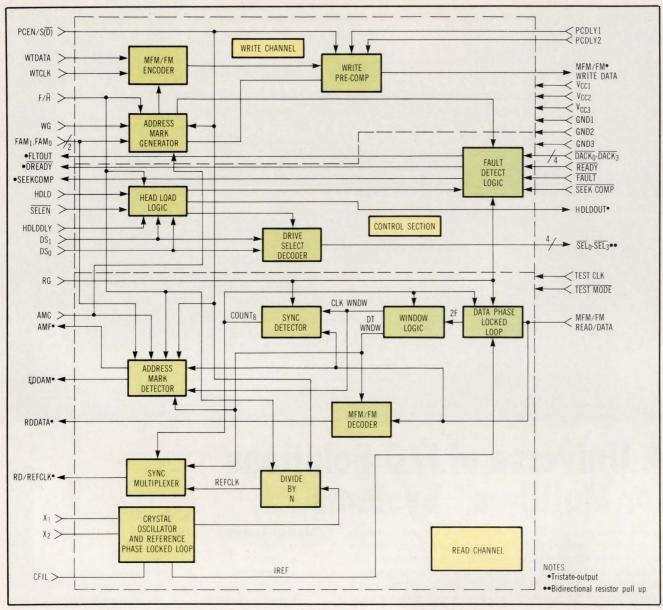


Fig 2 The disk data controller consists of three main sections—read, write, and control. The read section transforms the modified frequency modulation (MFM)/frequency modulation (FM) encoded data into nonreturn to zero (NRZ) data and an associated clock. The write section converts the NRZ data and its reference clock into MFM/FM data to store on the disk. The control section handles the drive select, floppy head load, and fault detection functions.

encode/decode logic. If the HDC is writing the address marks, the address mark control (AMC) line is raised sometime after the write (WG) line. From the next rising edge of the data clock until the address mark found (AMF) line is asserted by the DDS (or custom encoder chip), the HDC waits for an address mark to be written (Fig 3). In the read case, the read (RG) and AMC lines are asserted; assertion of the AMF line by the DDS or custom decoder circuit indicates that an address mark has been found. This signal resynchronizes the controller's internal byte clock for the data read operation. This control sequence allows flexibility in the type of address marks on the disk.

Since the data encoding and decoding function occurs offchip with a simple handshake procedure

to generate read and address marks, the HDC permits any type or size address mark. The read channel of the DDS chip provides the address mark detection logic to indicate when such a mark has been encountered. Based on control inputs to the DDS, seven different types of address marks used by Winchester and single/double density floppy disks are recognized. The write channel logic includes the ability to generate these address marks when writing to the disk. A simple handshake between the HDC and DDS indicates when an address mark is written or read.

Precompensation logic built into the DDS solves the problem of magnetic pulse interference that can occur when data bits are packed closely together.



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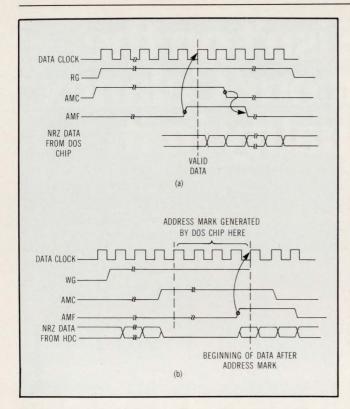


Fig 3 HDC coding is independent of the address mark generator/detector logic. When reading an address mark, the address mark found (AMF) signal indicates when an address mark has been detected (a). Signal AMF indicates that the address mark has been written on the disk, and that the DDS is ready to receive disk data (b).

When pulses are pushed too close together or pulled too far apart (pulse shift), they become more difficult to read. Precompensation methods calculate effects of pulse interaction and compensate for them by "unshifting" data pulses that will be shifted by magnetic pulse interaction before writing pulses to the disk. External delay pins on the DDS (one of the few external components required) allow a choice of shift delay. Depending on the ratio of the resistors attached to these two pins, the precompensation delay value can be selected to within 1 ns or 5 percent of the delay desired, whichever is greater.

Additional functions in the chip eliminate external SSI/MSI "glue" logic. An onchip two to four decoder selects one of four drives. Each of the four drive select pins has a 48-mA driver built into its output, eliminating the need for a separate chip to provide these drivers. Also, since each drive acknowledge input has Schmitt-trigger buffers, extra buffer chips are not required for these pins.

A clock generator within the DDS chip gives the HDC access to a clean clock at all times. Normally, a disk controller that is reading data derives the clock from the variable data/clock encoded in the disk data stream. When writing data, the controller requires a stable frequency at the nominal disk read/write speed. When performing neither of these

tasks, it needs a reference clock. The DDS chip automatically switches between these three clocks.

Partitioning disk control functions between the two chips improves the performance of both devices and provides upgrade paths. Putting data encoding/decoding functions on the DDS allows the HDC to handle twice the data rate of VLSI chips that perform the encoding function on the controller. Disk codes such as MFM and RLL require at least twice the normal raw data frequency to handle the encode/decode functions. However, since the high speed bipolar DDS performs this function, the HDC can work with unencoded data rates at up to 20 Mbits/s.

Segmented functions allow flexibility

Keeping the encode/decode function on a separate device also gives the designer flexibility and future upgrade capability. Some interfaces, such as the ST506/412 interface, require that data separation and encoding be performed by the disk controller. Other interfaces, such as the Enhanced Small Device Interface (ESDI), embed these functions in the drive. Thus, putting the encode/decode function in a separate device allows designers to easily interface with alternate standards. Such alternate encoding schemes as RLL can be accommodated by modifying the clock rate and upgrading the DDS chip. (When the DDS is configured with the HDC, the chip set directly supports the ST506/412 and the ST412HP interface, including recovery mode, without any additional logic.)

Segmented much like a board-level disk controller, the HDC uses a 16-bit microprocessor as a front end to the system interface and is coupled with a DMA controller to efficiently transfer data and commands. The format controller is linked to the twin sector buffers, the ECC unit, serial/parallel unit, and a set of user-programmable parameter RAMs. To make basic functions flexible, the HDC provides powerful hardware and software to implement critical areas of the disk controller function. But, it also allows users to selectively disable different parts of the function.

Since the disk data encoding/decoding function is implemented in the bipolar data separator chip, serial data to and from the part is NRZ. This leaves the users free to choose the encoding format. Because a data separator circuit is required, the encoding/decoding function can be put there as easily as in the controller itself. Some interface specifications such as the ESDI standard also require NRZ data to be transmitted over the interface cable. A further benefit of sending NRZ serial data to and from the controller is that higher data rates can be handled without a high speed controller.

The serial data rate is another area in which flexibility is often sacrificed for performance. Most controllers operate in a narrow range of speeds corresponding to the current requirements of the disk interfaces. As technology advances, drive manufacturers naturally want to increase the transfer rates. However, controllers typically cannot handle data rates at transfer speeds beyond those specified in the standards implemented by the board. The HDC adapts to the potential board limitations by providing a wide range of operations.

The HDC's serial channel can support data speeds from 50 kbits/s to 15 Mbits/s. The determining factor is the read/reference clock that is supplied to the HDC. Thus, to raise the data rate on a disk drive, the manufacturer need only change the data reference clock on the HDC. Because the serial format control section is essentially a static design, different speed drives can be attached to the HDC. Whenever a different speed drive is enabled, the HDC handles the drive without delays in switching or overall performance as long as the data reference clock is at the correct speed.

Choice of head positioning technique

A basic disk controller task is to provide the disk functions necessary to select and position the read/write heads over the correct head and track. The HDC supports four head positioning modes by providing implied seek capability in every disk read/write command. If this option is enabled, the difference between the current track/head (which is stored internally) and the desired track head is automatically calculated. Then the read/write heads are repositioned over the new head and track before the current disk read/write command is executed.

Seek overlap can improve disk I/O time in a typical four drive system by as much as 400 percent since all disks can be seeking at once.

A second option allows the HDC to perform simultaneous head positioning operations on different drives, in addition to the normal implied positioning option. A head positioning task (ie, a seek operation) usually requires more time than is necessary to issue the seek command to the disk drive. Once a seek command has been issued, many Winchester drives do not need to talk to the controller until the seek is complete. Thus, after issuing a seek command, the controller can disconnect from the current drive and issue a seek command to the next drive that will need I/O performed. This simultaneous seek operation, called seek overlap, is fully supported by the HDC without additional system software overhead. Seek overlap can improve disk

I/O time in a typical four drive system by as much as 400 percent since all disks can be seeking at once. This option still allows embedded seek operations.

Support is also provided for two other disk head positioning methods: restricted mode and buffered mode. In restricted mode, the normal floppy/ST506/412HP step position control is disabled. This allows a head positioning mechanism, such as the command oriented system on the ESDI interface, to be substituted. The HDC still uses the ST506/412HP drive status signals and disk serial data transfer control lines, but no longer performs the actual head positioning. Buffered mode disables all drive positioning controls and status signals, allowing the HDC to be used as a disk data serializer, buffer, ECC, and DMA unit. Additional external disk positioning control logic lets the HDC serve as the heart of customized disk data I/O controller.

Four pins on the HDC are allocated to directly select up to 16 different read/write heads. Internally, the HDC supports up to 256 heads. Additional external control logic accommodates selection of more than 16 heads. Beside head selection, the HDC provides the user with a programmable head settle delay value. A programmable 8-bit value specifies the amount of delay from read/write head selection to read/write head use. This accommodates the variance in head settling time that occurs from drive to drive.

When large amounts of data are read or written using a single command, multiple tracks and heads will be used in the data transaction. However, the specific data arrangement depends on user preference. Some store data in adjacent tracks on one surface; others store all data on the same track, but on adjacent surfaces, so that larger quantities of data can be accessed without moving the read/write heads. To accommodate either arrangement, the HDC automatically processes data over many heads and tracks without system intervention. It supports common head/track options with a user-specified multirecord policy (MRP) for each drive. Possible head/track policies are: move from track to track and change heads only when the surface overflows; move from head to head until all surfaces are used and then switch tracks; or cease operation when the current track overflows and alert the system. The MRP option requires minimum system intervention, even if the tracks overflow during a data transfer.

A reduced write current (RWC) pin on the HDC meets manufacture specifications that tracks in the inner part of the disk surface be written with reduced current in the read/write heads. The HDC allows the user to specify which tracks are affected. The RWC pin can then be properly asserted to reduce the current to the heads. Since these inner tracks are subject to magnetic bit interference, the user can also specify those tracks that require precompensation.

The HDC supports IBM formats for single- and double-density floppies as well as a standard Winchester format. All fields required are programmable in size, pattern, or, in some cases, both. Because of the vast differences between floppies and Winchesters (and between different Winchester drives), all relevant parameters are programmable. Four sets of parameters are kept in the HDC. Whenever a command specifying a particular drive is executed, relevant drive characteristics are taken from the parameter set for that particular drive.

Dealing with data errors

Although disk drives tend to be very reliable in normal use, they are susceptible to errors. Errors result from defects on the disk media, noise in the read/write recovery electronics, or even spurious noise in the data as it is transferred. Therefore, disk controllers incorporate some sort of EDC/ECC logic to protect the data. Four different EDC/ECC options, are supplied by the HDC. The first is the Comité Consultatif Internationale 16-bit cyclic redundancy check (CRC), an industry standard for floppies. This error-detection-only code makes the HDC compatible with existing floppy controllers and is used to protect ID fields on the disk.

The second and third options are two types of Reed-Solomon (RS) error detecting and correcting codes. The first is a single-burst error correcting code that can detect double-burst errors and correct singleburst errors (Table 1). (A burst is defined as a continuous inversion of the bits in the serial data stream of a given number of bits.) The second RS code is a more powerful version of the single-burst code because it can both identify and correct double-burst errors. In addition to correcting double-burst errors,

this double-burst RS code enhances single-burst error correction. More powerful than traditional burst error or fire detection/correction codes (Fig 4), double-burst RS code provides better protection, as MFM type encoding formats yield to more complex, error-prone RLL codes.

Programmable read entry allows error correction before retry, after retry, or after retry fails.

The final option is external, user-defined ECC hardware. When enabled for this option, the HDC turns several pins into status and control signals to control external ECC hardware. Thus, special or custom EDC/ECC codes can be used with the HDC. Many system designers use EDC/ECC codes only for error detection, preferring to perform a reread or simple retry operation to recover bad data. Others combine read retry operations with error correction codes to recover data. A programmable read retry option (up to 16 attempts) on the HDC is coupled with a programmable error correction option. This allows users to specify error correction before each read retry operation, after each retry, or only after all retry operations have failed. Another option halts the HDC whenever a data error is detected, thus allowing the system to intervene.

A special data field recovery command recovers the data field of a given sector regardless of whether its ID field is intact. Normally, if the address marks denoting the beginning of data sector IDs or of the actual data are damaged or destroyed, the controller cannot even try the ECC. As long as the address

TABLE 1	
Single- and Double-burst Reed-Solomon	Codes

	Sector Size (No. of bytes)	Detection Capability (No. of bits)		Correction Capability (No. of bits)		No. of Check bytes	
		Single Bursts	Double Bursts	Single Bursts	Double		
	128	33	9	9	Bursts	6	
Single Burst*	256	33	9	9	0	6	
	512	57	17	18	0	9	
	128	49	16	25	9	10	
Double Burst * *	256	49	16	25	9	10	
	512	81	24	41	17	15	

^{*}Single-burst Reed-Solomon corrects single-burst errors and detects double-burst errors.

^{* *} Double-burst Reed-Solomon is an enhanced version of Single-Burst Reed-Solomon; it can detect and correct singleand double-burst errors.

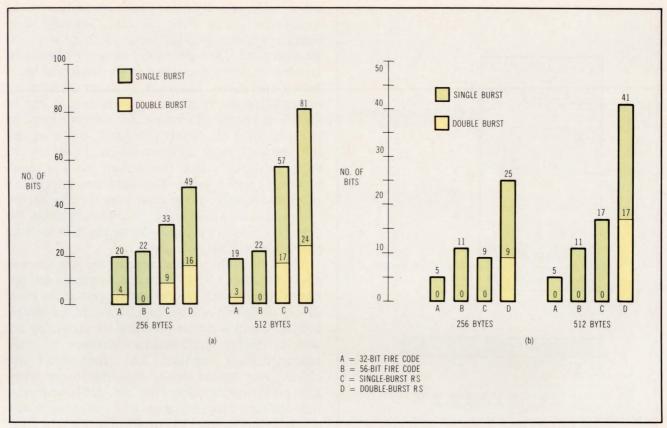


Fig 4 A comparison of the Reed-Solomon (RS) error correction codes versus the older Fire Codes illustrates why RS codes are better. In addition to having better single/double burst capabilities, the RS codes are more likely to detect an error.

mark on the data field is valid, the HDC will read the sector data and if necessary apply error correction to the recovered data.

Because they are mechanical devices, disk drives sometimes have physical defects on the disk recording surfaces. Since fixing the problem can be very expensive, systems usually map around the defect. This makes part of the disk invisible to normal disk accesses.

The HDC supports several methods of defect mapping that require minimal system intervention. The first method relocates sectors from the defective area to another area on the same track. When the system determines exactly where the defect is, the track is reformatted with the defective area mapped out. The system must remember which tracks have fewer sectors, when issuing commands.

Another method shifts format fields on the track until the defect falls into an unused field. Since field sizes are programmable, they can be altered slightly to ensure that no data or ID information lies in the defective area, once its location and size are known.

The third method of defect mapping relocates the defective track to a defect-free track. A track relocation command provided by the HDC accomplishes this by writing a special vector on the defective track; this vector contains the new location of the track (new head, new track). Then, whenever the HDC ac-

cesses the relocated track, it automatically goes to the track's new location to read or write data, if the automatic seek to relocated track option is enabled. No system intervention is required. During multitrack or multisurface read or write operations, the

	TABLE 2				
Different I/O Parameter Block Commands Available on the Hard Disk Controller					
Multisecto	r commands				
(1 to 256	sectors/command)				
	Read				
	Write				
	Verify				
Initializatio	n commands				
	Format (1 Track to entire disk)				
	Relocate track				
	Restore drive				
	Load drive parameters				
	Dump drive parameters				
Data recov	very commands				
	Load buffer				
	Dump buffer				
	Load syndromes				
	Dump syndromes				
	Correct buffer				
	Read data absolute				
General co	mmands				
	Seek				
	Read ID				

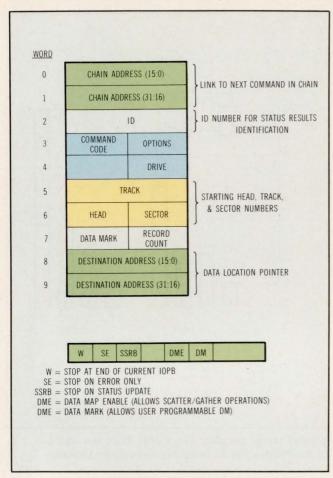


Fig 5 A typical 1/0 parameter block (10PB) command illustrates the different command options. For example, a multisector read command would require starting track number, drive, starting sector, number of sectors to be read (record count), and a printer to a block system memory where data is to be stored. Command modifiers allow user options on error response, data mapping, or even user-defined data marks.

HDC can automatically seek to the new track, process the data on the alternate track, and then return to the normal process sequence (in the multitrack/head command) to complete the data transaction.

Controller commands provide extensive options (Table 2). The basic read, write, and verify sector commands allow 1 to 256 sectors to be handled using only one I/O parameter block (IOPB). Overflows to different tracks and heads are handled automatically using programmable options. Options selected for each IOPB modify the method of data transfer to and from system memory, the number of sectors, the starting head/track, error handling, or the type of data mark to be used in the data field (Fig 5).

Embedded software in the HDC determines how the control algorithms allocate internal hardware resources. The HDC's dual sector buffer architecture enables zero-interleave data transfers to run automatically at data rates up to 15 MHz. During a multisector read operation, for example, the HDC always dumps one buffer into system memory while the

other buffer is being filled simultaneously with the next sector's data from the disk. Because zerointerleave operation is the natural state of HDC, the time necessary for read, write, or verify operations is automatically reduced two to six times over interleaved operations. However, if sector interleaving is necessary for system considerations, it can be specified. The initial track/sector map is created by the user when the disk is formatted, allowing any interleaving format to be specified. In effect, the HDC maximizes data throughput with a dualprocessor architecture. The data format/control processor is active at the same time the macro control processor is calculating information about the next data transfer or sending/receiving data to/from the system via the DMA unit.

The wide performance range of the Am9580/9581 chip set ensures a long life to disk interface designs. Major chip manufacturers have supported the trend toward utilization of advanced, backward-compatible hardware and software products by providing advanced, higher performance versions of their microprocessor families. The HDC meets this challenge by automatically adapting to oncoming high performance storage devices. A designer need only alter the data separator clock or replace it with a new one to increase the performance of the HDC.

As vertically recorded floppies start arriving on the scene next year, the HDC will be able to handle them without trouble. As RLL encoding replaces MFM encoded data, programming the HDC to use the powerful double-burst Reed-Solomon ECC will maximize data reliability or change data encoding/decoding. As add-on peripherals increase "traffic" on the system bus, the system can alter the HDC's bus characteristics to ease the congestion, or speed bus transactions by raising the system clock to a full 10 MHz. Finally, the ability to customize the HDC interface will allow adoption of proprietary designs, while retaining all the benefits of a powerful, VLSI disk controller nucleus.

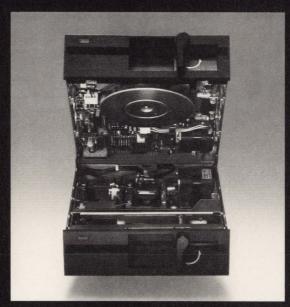
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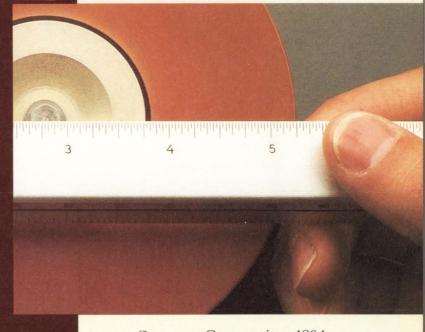
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DESIGNING HARD DISK DRIVES TO TAKE ABUSE

The bangs and bumps of an office environment can affect the performance of hard disk drives. Some economical designs can provide the shock and vibration protection necessary to ensure reliable operation.

by Alireza Rahimi

Winchester disk drives are becoming common in desktop and workstation computer systems. Because such systems are moved frequently, or are located near sources of vibration such as printers or machinery, their drives are subjected to far more shock and vibration than larger, higher capacity drives that remain in the computer room. This increased exposure is coupled with the greater vulnerability to shock and vibration that Winchesters have compared to floppy disk drives. And, while the 19- μ in. flying height of Winchester read/write heads enables them to offer higher performance than floppies, care must be taken to minimize shock and vibration effects. Design features must prevent unwanted contact between the heads and media.

Sudden, violent head/media contact could scatter particles from the media/heads throughout the drive. If these separated particles should come between the

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read write heads and media, they could cause the heads to "crash" into the media. A crash could ruin the media or heads and render the drive inoperable.

Proper data protection features, however, will make Winchesters resistant to those shock and vibration levels that might occur in work environments or during shipping. These features enable Winchesters to be used in small, easily transportable systems without undue concern over reliability. Different approaches have been taken to protect these hard disk

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drives from shock and vibration. Shock/vibration isolators (mounts), dedicated head landing/shipping zones, a low mass head/flexure design, a spindle brake, and a stiff actuator system design are protective measures that have been incorporated in Shugart's line of 51/4-in. Winchesters. Laboratory and field testing conducted prior to shipping confirms the ability of these drives to withstand shock and vibration.

Shock and vibration isolators

Shock can be defined as an impact of short duration. An example is a package falling to the ground. A shock pulse is normally measured by its peak amplitude, duration, and overall shape. Vibration, on the other hand, is of a continuous nature and can be generated by the drive's spindle motor as well as by office equipment such as typewriters and printers. Shipping is another common source of vibration. Vibration is expressed in terms of frequency and amplitude—ie, the amount of the force, displacement, or acceleration.

The term "shock mount" is commonly used to refer to both shock and vibration isolators, although the terms "shock isolator" and "vibration isolator" are not generally interchangeable. Typically, both shock and vibration isolators consist of pieces of rubber designed to reduce the dynamic motion or force transmitted from the drive's casting to the head/disk assembly. In Shugart's 700 and 700S series drives. they are placed between the mounting brackets and the head/disk assembly. As a resilient element, the isolators serve to temporarily store the incoming energy. This stored energy is released to the drive gradually, thereby reducing the magnitude or motion of the force to the head/disk assembly. In order to be most effective, these isolators must be placed at

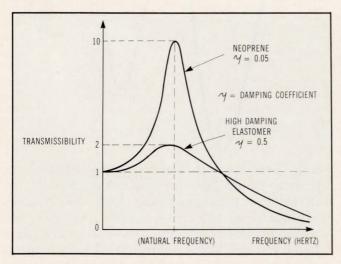


Fig 1 Typical transmissibility curves for highly and lightly damped disk drives are shown. Transmissibility is defined as the ratio of transmitted force to impressed force.

or near the drive's center of gravity. In addition, they are selected or designed for optimum drive protection.

Shock isolators are devices that instantly absorb input energy. This energy is stored within the isolator and released over a long period of time with a frequency that matches the drive's natural frequency. To absorb the energy and release it for a longer duration requires soft isolators that will yield larger dynamic displacement of the drive frame.

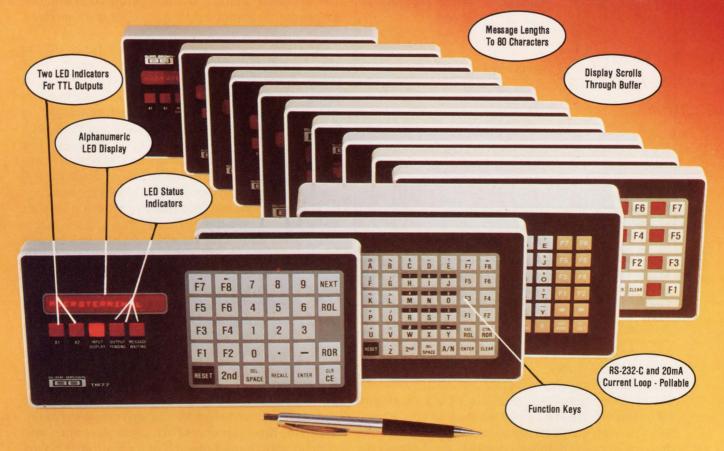
In contrast, vibration isolators must reduce the input displacement from the vibration source. Therefore, the composition of vibration isolators must be stiffer than that of shock isolators in order to limit the drive displacement. Input energy isolation is attained primarily by maintaining proper frequency relations within the drive—ie, the relationship between the input frequency and the drive's natural frequency.

Isolator damping properties play a major role in shock or vibration reduction. The input energy from a shock or vibration will be absorbed by the isolators, and a portion of that energy dissipated in the form of heat, through the internal damping of isolators. The remaining energy will be transmitted to the drive. Therefore, isolators with higher damping properties will transmit less energy to the head/disk assembly (Fig 1).

Transmissibility is defined as the ratio of transmitted energy (output) to the incoming energy (input). A rubber, or neoprene, isolator has a damping coefficient of approximately 0.05 to 0.08. The 700 and 700S series drives, however, incorporate isolators made of an energy absorbing elastomer, which has a better damping quality than natural rubber or neoprene. An isolator formed of this material transmits vibration at a resonance frequency that is at least five times lower than that of the rubber isolator. This results from the dissipation of input energy through the optimum polymer structure of the isolator.

In addition to stiffness, a key consideration in designing isolators is the maximum allowable movement of the drive in its frame. This movement is called "sway space." To achieve a specifically desired shock or vibration performance, a minimum dynamic displacement is necessary to absorb the transmitted energy and gradually release it. The amount of sway space is dictated partially by space constraints of the disk drive's design. To ensure sufficient clearance between the drive and its outer frame, designers must calculate the maximum displacement of the mounted unit under the most severe shock conditions. Isolator stiffness should be selected so that the maximum displacement does not exceed the sway space in the worst case. If the sway space is exceeded, the drive bottoms out. Then, any

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TM76	12	300 & 1200	36	Numeric	8	Larger keys	+5VDC
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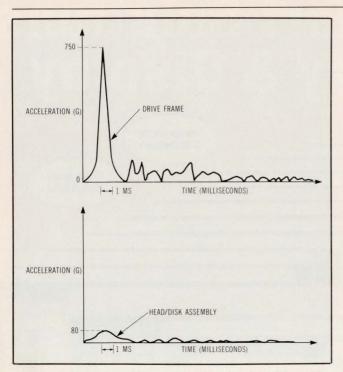


Fig 2 In these 3-in. drop test results of a disk drive with optimum shock mounting, the upper curve is the acceleration history of the drive frame. The lower curve is the transmitted acceleration to the head/disk assembly.

subsequent shocks will transmit greater energy to the head/disk assembly.

The company has designed an isolator for the 5¼-in. Winchester that minimizes both shock and vibration effects. The isolators used in the 700 and 700S series are made to reduce the input force to the drive by approximately 90 percent. Fig 2 shows the results of a drop test performed on a 10-Mbyte, 712 drive. To simulate an accident that might occur in an office, the drive was dropped from a 3-in. height onto a wooden desk. The upper trace shows acceleration history of the drive frame with a peak of 750 G. (G is a unit of acceleration.) The lower trace shows the transmitted acceleration to the head/disk assembly with a peak of 80 G, a reduction of approximately 90 percent.

Minimizing head/media contact

Effects of shock and vibration on the drives are mininized by dedicated head landing/shipping zones. The zones do not contain data tracks and are designed for parking the heads when the drive is not in use. The read/write heads can be retracted to the zones whenever the drive is powered down. Therefore, when the drives are in transit or turned off, a shock of sufficient force to cause the heads to separate from the media will not destroy data, even if the heads are jolted off the surface of the media, and then slapped down onto the disk.

The low mass head/flexure design also helps minimize the effects of shock and vibration. The

3380-type heads and flexures (named for the IBM high capacity 14-in. Winchester in which they first appeared) have about one-fourth the mass of the 3350-type heads used in an earlier generation of IBM 14-in. Winchesters. Therefore, their natural frequencies are twice as high and less prone to resonance in normal transportation and operation-induced frequencies.

The 3380-type heads exert 15 g of force on the disk, compared to 9 g for 3350-type heads. This added force, when combined with the lower head mass, allows the 3380-type head to absorb much higher acceleration during a fall, before leaving its position above the disk surface, and slapping back onto the surface and breaking particles loose. The lower mass and higher load of the 3380 design translates into approximately six times more shock protection than that provided by the 3350-type head.

The 3380 heads also provide the benefit of higher capacities. With a smaller core, they are less likely to read bits next to the ones being read. This benefit enables disk drive and media manufacturers to offer higher bit densities without increasing the risk of read/write errors.

To prevent the heads from scratching the media during transportation or normal handling, a spindle brake is incorporated into the design of Shugart's rigid disk drives. As the name implies, a spindle brake prevents the disk from rotating when the drive is powered off. The mechanism, a simple solenoid-powered brake, releases the spindle and allows the disk to spin freely whenever the drive is powered on. When the drive is powered off, the brake comes into contact with the spindle to halt its motion. This design provides further protection for the heads and data during power-down situations.

A stiff actuator system can also reduce the amount of shock and vibration transmitted to the heads. Consisting of a rotary arm, band, capstan, and stepper motor, Shugart's proprietary actuator design provides the required stiffness to prevent jittering of the heads under normal shock/vibration conditions.

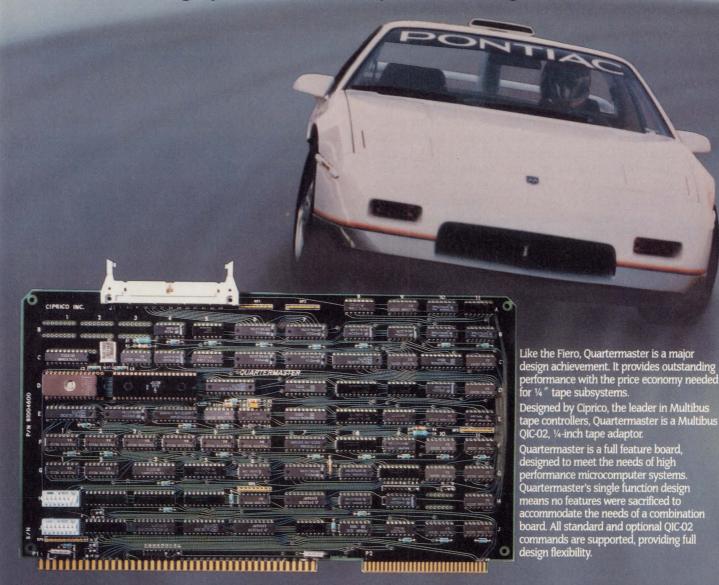
Incorporation of these shock and vibration protection features enables the drives to achieve higher resistance to shock and vibration than most low capacity (under 50 Mbytes) drives of this kind. In a nonoperating mode, they can withstand 40 G of shock and a drop from a 5-in. height onto a hard surface. In operating mode, these drives can withstand 10 G and a drop from a 2-in. height without damage to the heads or media.

Alternative protection methods

This level of shock and vibration isolation offers sufficient protection against workplace and transportation hazards. Additional methods of shock and vibration protection are not only unnecessary, but add to the cost of the drive. The higher capacity

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Winchesters, however, may require alternative shock and vibration protection features. Common approaches that have been chosen by other Winchester disk drive manufacturers include actuator locks, double shock mounting, and harder media.

The actuator is part of the assembly that positions the read/write heads over the disk. An actuator lock prevents head movement during transportation by clamping the actuator arm in place, usually when the heads are parked in the dedicated head landing/ shipping zone. Actuator locks provide additional insurance against shock and vibration, but are not necessary in low capacity products. These locks can be either automatic or manual. While automatically activated locks offer the advantages of being simpler to operate and more reliable, manually operated locks are easier to manufacture and less expensive.

If properly designed, double shock mounting provides greater force or vibration reduction. In drives with single shock mounting, the head/disk assembly and drive casting are connected to mounting brackets (inner frame) by four shock mounts. In double shock mount drives, four additional isolators connect the inner frame to the outer frame or host casing. Although a double shock mount design offers greater protection, it is more expensive than single shock mount designs and may extend the form factor of the drive.

Some disk drive and media manufacturers believe that harder media are less susceptible to damage when read/write heads and media make contact. Today's standard disk media are made with gamma ferric oxide coating on an aluminum substrate and are coated with a silicone lubricant. Plated media, now being used by some disk drive manufacturers, have a coating of a cobalt/nickel solution over an aluminum substrate. Since this plating is harder than gamma ferric oxide, the possibility of dislodging particles is reduced if the head contacts the disk. However, users of gamma ferric oxide media claim that such media are less susceptible to scratches. When particles separate from the disk, the lubricant enables them to slip between the heads and the disk, thus avoiding the possibility of a head crash. Furthermore, although contact between heads and plated

	Nonoperating	Operating
Shock	40 G, 11 ms Half-sine pulse	10 G, 11 ms Half-sine pulse
Vibration	5 to 22 Hz, 0.5 G 22 to 44 Hz, * 44 to 500 Hz, 2 G	5 to 17 Hz, 0.035 in. (Double amplitude)
		17 to 150 Hz, 0.55 G 150 to 200 Hz, **
		200 to 500 Hz, 0.25 (

media is less likely to dislodge particles, the hardness of the media can damage the head and slider assembly.

Testing protection effectiveness

Just as different approaches are taken to protect products from the effects of shock and vibration, different testing methods are applied to determine the effectiveness of such protective methods. It is recommended that both laboratory and field testing be performed to determine the effectiveness of the drive's design.

The shock and vibration testing procedure used by Shugart is designed to simulate conditions in typical operating environments. For example, the 700 and 700S series are designed to withstand levels of shock and vibration equivalent to those experienced by the drive when being transported by truck or when located near such vibration sources as printers and motors. Shock and vibration specifications for these drives are given in the Table.

In testing, the shock and vibration laboratory uses a Genrad 2506 structural dynamic analyzer and an Unholdz-Dickie Electrodynamic shaker table. The analyzer has a DEC PDP-11/34 computer with Genrad microprocessors, 64 Kbytes of RAM, a 1.6-Mbyte floppy disk drive, and a 14-Mbyte Winchester disk drive. The analyzer measures the test results conducted on the shaker table. The Table's sinusoidal and random vibration modes, and shock wave generation capabilities simulate environmental shock and vibration conditions.

Drives are first tested for their ability to withstand shock and vibration in three orthogonal axes—ie, with the drive lying on its base and on its sides. Drives are secured to the table and subjected to simulated shock and vibration for varying amounts of time. Tests are first performed in the nonoperating mode, with the heads parked at the landing/shipping zones, and the power off. After each test, the drives are examined for any damage to the read/write heads or media, and for hard (nonrecoverable) errors.

Tests are then conducted with the drive in an operating mode, while a data transfer is being performed. Errors caused by shock and vibration while the drive is operating are called soft (recoverable) errors. These errors cause no permanent damage to the heads or media.

Field testing follows laboratory testing. Dropping the drive onto a hard surface like a desk simulates a common hazard to which drives are exposed in an office environment. Drives undergo two complete series of tests, first in shipping containers, and then without shipping containers.

When tested inside a container, the drives are dropped onto a concrete floor from a 36-in. height. Inside the container, the drive is packed in several

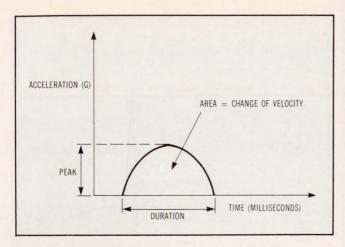


Fig 3 A typical shock pulse is defined by its peak acceleration, duration, and shape. The area under the curve is equal to the change of velocity, due to shock.

inches of foam to provide protection from rough handling during transportation. This testing phase consists of dropping the containers on different sides and at different angles several times. After each drop test, the drive undergoes both visual and functional inspection. Drives foam-packed in shipping containers have proven capable of resisting damage to the heads or media when dropped from this 36-in. height onto a concrete floor.

Drives are then dropped without the protective container onto a hard surface from varying heights. After each drop, they undergo visual and functional testing. In tests, 700 and 7008 series drives, dropped from a 5-in. height in a nonoperating mode, have come through without damage to the heads or media. Similar drop tests are then performed when the drive is transferring data. Results show that the drives can be dropped from a 2-in. height onto a hard surface without damage.

The relationship between field and laboratory testing can be explained in terms of equivalent energy, or change in velocity. Generally, shock is defined as a motion in which there is a sharp, sudden change in velocity. A shock pulse is usually characterized by a rise and decline of acceleration in a very short period of time (Fig 3). The area under the curve is

equal to the change of velocity due to shock. The acceleration peak, duration, and the curve's shape measure the shock level caused by the transmitted energy or change in velocity due to impact.

Other typical shock waves are square, triangular, and random. In field situations, the shock wave could be similar to any of these waves or any combination of waves, depending on the nature of impact. Shock pulse duration also depends upon the material properties of the contact surface, and whether it produces an elastic or inelastic impact.

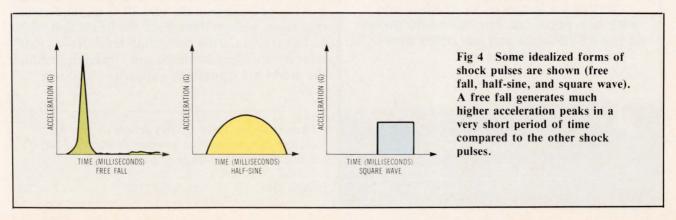
Different types of shock pulses, such as half-sine, square wave, or free fall (Fig 4) can be compared by equating the change in velocities. A free fall drop pulse generates much higher acceleration peaks in a very short period of time than do the other types of shock pulses.

For example, a 3-in. drop height creates a change in velocity of 48.1 in./s for an inelastic impact. This velocity change, when transmitted to a drive during a period of about 1 ms, will generate approximately 250 G of acceleration peak. The resulting spike type of shock pulse can be approximated by a triangular wave. For a duration of 0.2 ms, a 3-in. drop height generates a peak of 1250 G.

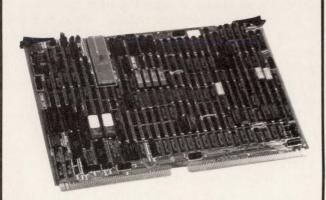
Shock pulses can be compared by equating the changes in velocities.

A half-sine pulse with an acceleration peak of 40 G and duration of 11 ms creates a change in velocity of 108 in./s. Fig 5 shows the relationship of equivalent energies of a 40-G half-sine shock with a duration of 11 ms and a 1-ms spike pulse. In practice, the longer shock duration is sensed by the disk drive in the shipping box.

Tests show that if the shipping container is dropped from 36 in., the drive receives a shock peak of 40 G with a duration of 10 ms and a shape close to that of a half-sine wave. As a result of the rubber foam pack in the shipping box, the drive receives a reduction in peak amplitude and an increase in shock duration. For an ideal inelastic impact, a 5-in.



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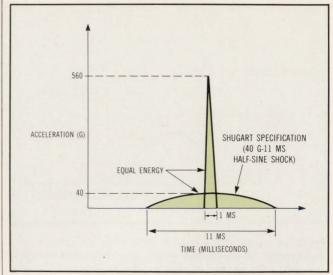


Fig 5 Two different shock excitations result in equally transmitted energies. The free fall spike pulse is reduced to the half-sine wave by rubber foam packing in the shipping box.

drop height produces a change in velocity of 62.1 in./s. The acceleration peak for a duration of 1 ms will be 322 G, while for a duration of 0.3 ms, the acceleration peak rises to 1073 G for a spike shock.

Matching protective measures to the environment

To provide the high capacity and fast access that they promise, Winchester disk drives must be designed to withstand the shock and vibration that occur during transportation and in working environments. Exposure to shock and vibration can produce catastrophic effects on the performance and reliability of rigid disk drives if protective features are improperly designed.

Half-height 51/4-in. Winchester drives can be adequately protected from shock and vibration through the use of several features. These features include four-point shock/vibration isolators with high damping characteristics, a low mass head/flexure design, dedicated head landing/shipping zones, a spindle brake, and a stiff actuator design. Laboratory and field testing prove that these protective features enable Winchesters to withstand 40 G of shock in a nonoperating mode, and 10 G of shock when operating, without damage to the heads and media or loss of data. This protection level proves sufficient for the types of shock and vibration to which the drives are commonly exposed.

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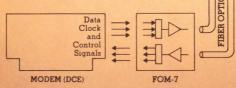
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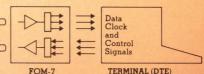
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- Provides secondary data channel

In short, you can use our new fiber optic modem between any two plug compatible units in your local area network. And it won't require any jury-rigging or looping clock and interface signals. That's because, from an operating standpoint, our fiber optic modem looks just like an EIA cable; whether you're going from a long-haul

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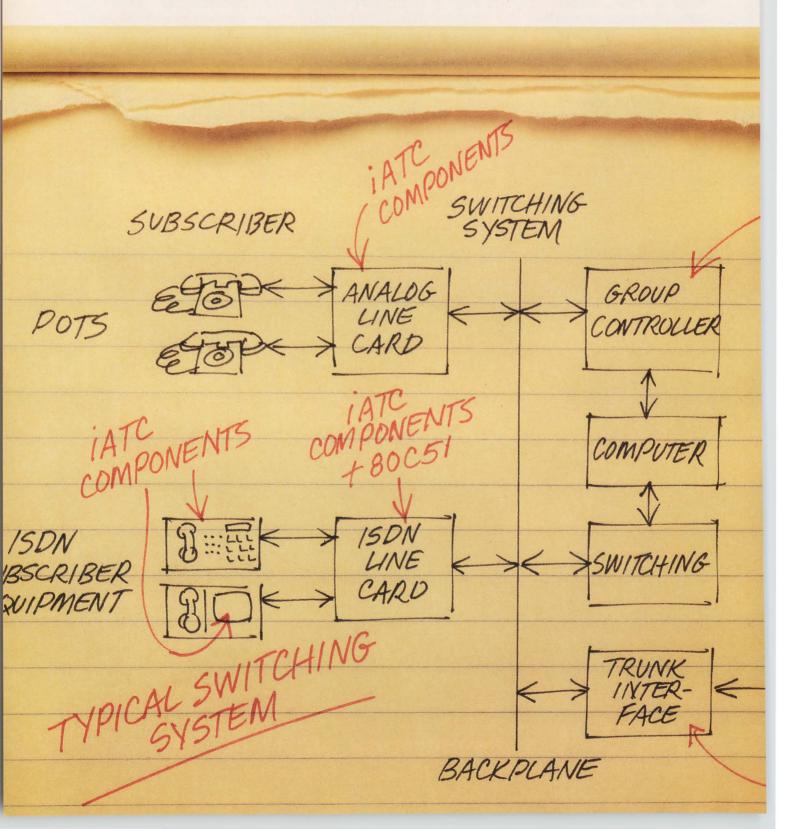


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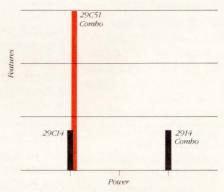
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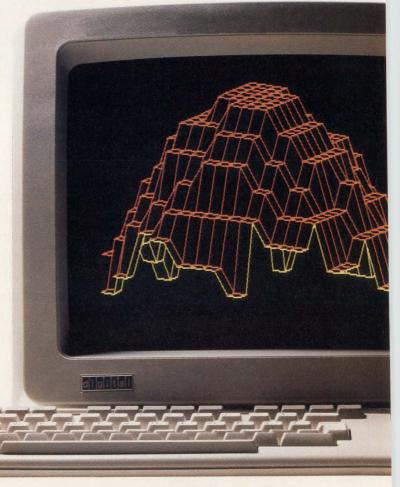
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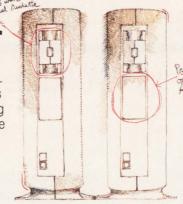
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Hitachi's new technology is capable of converting the 0 to +5V output levels of microcomputers and standard logic to a voltage great enough to drive solenoids, gas discharge displays, piezoelectric elements, and other HV loads. Hitachi high-voltage ICs, based on dielectric isolation technology, may now be used in applications up to 300 volts.

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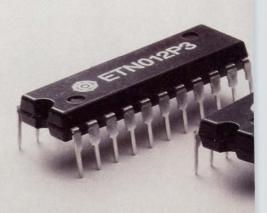
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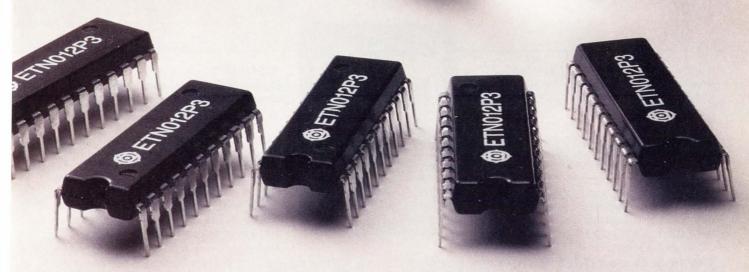
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EFFICIENT I/O UNLEASHES BENEFITS OF OPEN BUS CONCEPT

Innate advantages of the open bus can free CPU-, bus-, and I/O-bound systems. Peripheral controllers are the key to overcoming the devices' inherent limitations and lead to efficient bus use.

by Chappell Cory and George Jackson

Major minicomputer manufacturers that support closed (or proprietary) buses have imposed severe constraints on system designers during the last decade. This has led to wide use of the open bus scheme. From this scheme, the engineer can gain a powerful and flexible way to build computer systems that meet specific application needs.

One well-known open bus is the Intel Multibus. Because Multibus is well specified and because it is in the public domain, some 250 companies have developed more than 1000 products compatible with it. Yet, although Multibus appears to offer an engineer's utopia, it has not always done so. Many system designers are unable to build an integrated machine that fully uses the capabilities of present-

Chappell Cory is vice president of research and development at Xylogics, Inc, 144 Middlesex Tpke, Burlington, MA 01803. He holds a BS in mechanical engineering from Stevens Institute of Technology, Hoboken, New Jersey.

George Jackson is applications manager at Xylogics, Inc, European Headquarters, 4648 High St, Slough, Berks SL1 IES, U.K. He holds a BS in physics from City University, London, England. and next-generation processor chips in an open bus environment. This is due to inefficient data transfers between disks, tapes, and CPU memory.

An analysis of typical Multibus applications provides the key to many design benefits of this open bus. These advantages fall into two main categories. First is the simple dedicated single-task, or single-user application, such as signal measurement and word processing. Second is the performance-critical area of multitasking/multi-user applications. This latter category includes high performance file servers for the increased demands of modern local area networks, speed-critical requirements of image processing for both the medical and printing trades, computer aided design (CAD), and the immediate response requirements of commercial multi-user systems (Fig 1).

Solving CPU-, bus-, and I/O-bound problems

Typical Multibus operations have one thing in common. They all rely on passing large amounts of data at high speeds between the CPU and peripherals, which work concurrently [Fig 2(a)]. This poses a problem found in many mini and microcomputer applications: the system can become CPU-, bus-, or I/O-bound. These problems occur when the CPU runs out of power, the bus runs out of bandwidth (restricting the speed at which data can be transferred), and the time taken for I/O access becomes

excessive, respectively. The peripheral's fixed data rate leads to inefficient data transfers between the device and the CPU's memory. This causes a severe decline in system performance.

The 16- and 32-bit processors now being designed and used on the Multibus are solving the CPU's power loss problem. These processors include the 80286 and 68010, both of which have higher execution speeds and 32-bit internal data paths to allow long word calculations. Also, production yields are helping create parts that can run at ever-increasing clock speeds, thus alleviating the problem of a compute-bound processor.

Furthermore, the CPU bus bandwidth problem, which causes excessive processor wait states, has been largely relieved by the advent of 16- and 32-bit wide, separate CPU to memory data paths. Adoption of local CPU buses, such as the Intel iLBX, enables the CPU to fetch data and instructions directly from memory. This leaves the bus free for peripheral data transfers. The iLBX and other "P2" buses developed independently by various vendors use a previously undefined connector—the P2 edge connector on the backplane. The iLBX is a 16-bit data path that runs at rates of up to 19 Mbytes/s. In some cases, other P2 buses are 32 bits wide and run at speeds close to 40 Mbytes/s.

Memory technology is also keeping pace as semiconductor memories lower access times, even as capacities increase. Memories with access times of less than 350 ns are not uncommon, and several vendors are using static memories with access times of 200 ns or less. A prefetch method is sometimes used to anticipate the second of two consecutive reads on a 16-bit bus. Using a 32-bit memory array, it provides the second access in under 20 ns. Block-mode transfers can also be used to allow back-to-back word transfers, saving 20 to 30 percent of bus time.

The 16- and 32-bit processors being designed and used on the Multibus are solving the CPU's power loss problem.

An architecture that uses a CPU fetch channel results in a Multibus that has truly become an I/O bus in these higher performance machines [Fig 2(b)]. In this sense, it is fully analogous to Digital Equipment Corp's PDP-11/70 and VAX, and to other machines that have separate memory and I/O channels. Note, however, that the Multibus can attain more than twice the DMA throughput of the DEC machines.

Only design trade-offs that address the needs of the type of system planned can achieve the Multibus' potential efficiency, however. The key to efficiency seems to be a high DMA rate. Fig 3 shows the consumption of bus bandwidth, or total throughput,

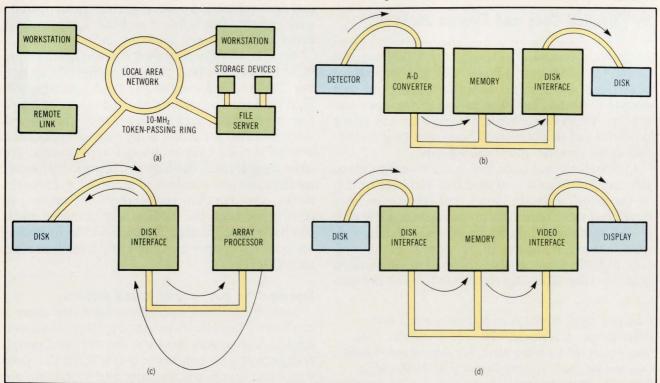


Fig 1 Many types of systems can benefit from the Multibus. Open system buses can be used in file servers for local area networks (a). Medical image systems have high throughput requirements that can be met by a combination of dedicated and open system buses (b). Image processing systems use the open system bus for connection of the system to a disk controller (c). Computer aided design systems for image processing are easily built with off-the-shelf components, based on a common open system bus (d).

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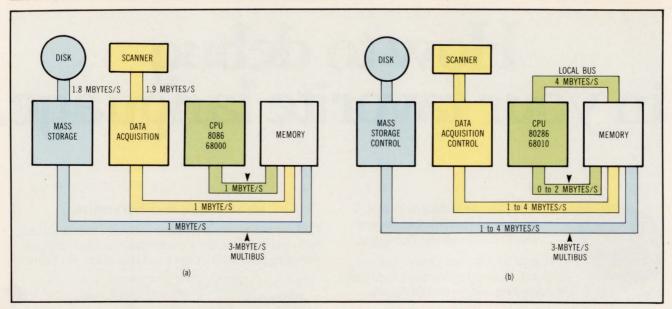


Fig 2 Multibus operations can pass large amounts of data at high speeds between the memory and peripherals while the CPU also accesses memory over the same bus (a). In very high performance systems, the Multibus becomes a dedicated I/O channel with a specialized local bus providing the path between the CPU and memory (b).

by four disk controllers with varying DMA transfer rates. All four controllers run a disk with a 1.35-Mbyte/s aggregate data rate.

Note that when running small noncontiguous block transfers of 1024 bytes (with a reasonable optimized file structure), bus usage is always low. But it is not a constraint in this case. This I/O scenario is common in multi-user systems. However, multiuser systems and many medical, CAD, and imaging systems must also handle large block transfers (for virtual paging, overlays, screen images, user swapping, and more) on the order of 10 Kbytes to

Using FIFO buffers

An interesting feature of first in, first out buffers is that their useful size is much larger than it appears to be. Since a FIFO can be filled at one other "end" while it is emptied simultaneously at the other "end," its capacity is not an absolute value. The equation for the useful capacity is dependent upon the number of relative rates of filling and emptying. In the case of a disk read, these rates are data rate and bus DMA data rate,

The equation is Kf = k + k/[(Bt/Dt) - 1], where Kf is apparent FIFO size in bytes, k is physical FIFO size in bytes, Bt is bus time for one byte transfer, and Dt is disk time for one byte transfer. Note that if the bus time is equal to the disk time or less, the apparent FIFO size is infinite.

If the transfer times are close, say 800 ns for the bus and 740 ns for the disk, the apparent size of the buffer is 109.328 bytes for a FIFO of 8192. This means that even though there is a slower bus than the disk, a large number of bytes can be transferred before a data late occurs. This is important when comparing products with different buffer schemes because Ping-Pong and staged buffers do not have this feature and will overrun much sooner.

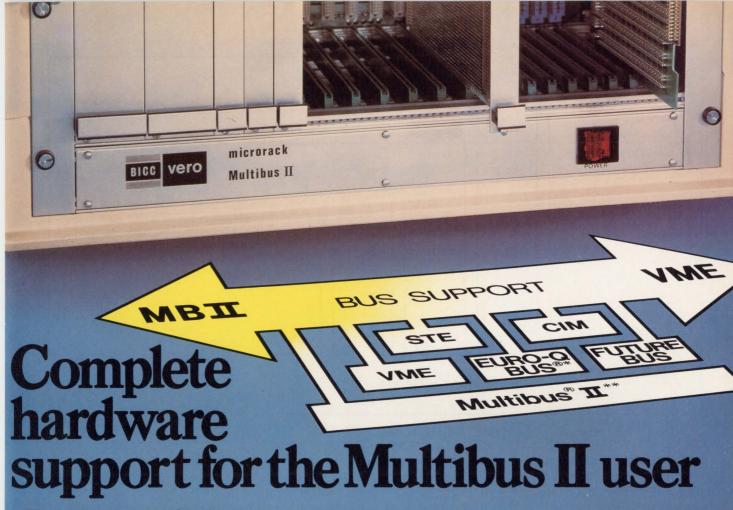
1 Mbyte. The key to avoiding total I/O bandwidth consumption is a high DMA rate. It is often important that other peripherals be allowed to access time slots on the bus continuously because of their realtime needs and small buffers.

Inefficient use of Multibus

Peripheral controllers that use small buffers often cause a mismatch between the data rate of the device and the bus. This mismatch becomes critical when many devices are vying for bus priority. In such cases, the peripheral may have to miss a turn (data late errors). In the case of a disk, a whole revolution or more may be lost, depending on the intelligence of the controllers.

Peripheral controllers exert considerable influence on the transfer rate. Fig 4 shows the effect that two parameters of a peripheral controller, buffers and block size, have on a key system performance indicator: transfers/s. The graph assumes that the I/O shell in the operating system is fairly well optimized. Because new blocks are near the current blocks on the disk, the high performance drive has a track-totrack seek of 5 ms and a 1.35-Mbyte/s average trans-

When bus availability is high, DMA rate and buffer size have little or no effect on the number of transfers/s. In this example, there are 70 disk operations/s. However, when other peripherals make demands on the bus bandwidth, an interesting event may occur. If the block size is larger than the buffer in the controller, the system can hit a "stone wall." This can cut the average number of disk operations in half. Note that a higher rate controller will hit its stone wall only at a much lower availability figure.



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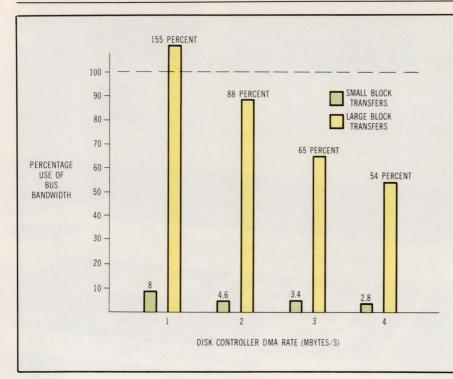


Fig 3 Each of the four disk controllers has different DMA transfer rates. The higher the DMA rate, the more efficient the use of the bus.

If the block size is smaller than the buffer in the controller, no stone wall occurs and performance degradation occurs gradually. In this case, even with only 10 percent of the bus available, 80 to 90 percent of performance is maintained. These calculations are based on a first in, first out (FIFO) buffering scheme. (See Panel, "Using FIFO buffers.")

Ping-Pong or staged buffers have more overhead and must be much larger to achieve the same apparent buffer size. Moreover, this method of matching block and buffer size can be accompanied by burst control. This will manipulate the amount of data allowed onto the bus. It lets the system designer optimize bus use and match peripheral and bus speeds.

Because the Multibus protocol does not allow concurrency between arbitration and data transfers arbitration wastes bus bandwidth. Standard DMA is controller chips are very slow in performing the arbitration required to gain bus access and data transfer rates. Specifically designed DMA sequencers, however, can yield very fast access times and achieve data transfer rates of up to 3 Mbytes/s. They also handle word- or byte-mode transfers under program control. Typical transfer sequences for single transfer (throttle = 1), large bursts (throttle = infinity), and system matched throttle (throttle = 8) are shown in Fig 5.

Inefficient use of peripherals

Inefficient use of peripherals is the second performance critical area. In trying to maximize the efficiency of disk or tape drives, the specific type of peripheral device used has a major impact on performance. An example of inefficient tape system use is when a streamer tape cannot be kept streaming. This

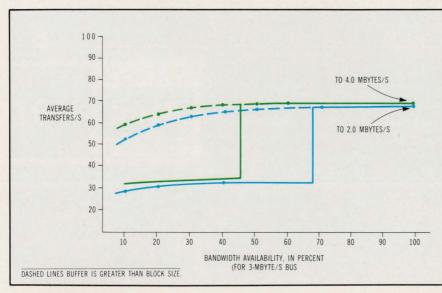
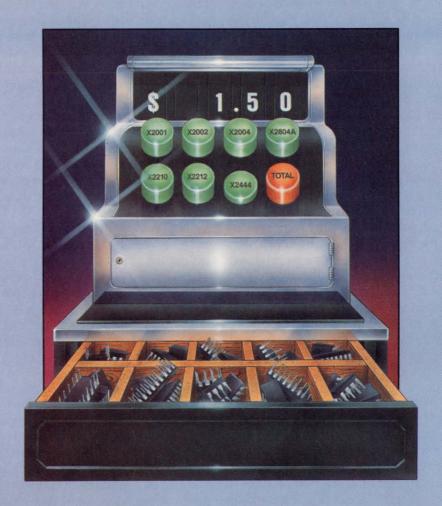


Fig 4 The buffer size and DMA rate of a controller affect the number of transfers/s. If the block size of the transfer is greater than the buffer size, and if demands on the bus bandwidth reach a critical level, the system hits a "stone wall" in transactions/s.



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may be due to the job's organization, DMA speed of the tape controllers, or buffer size of the tape controller. Likewise, inefficient use of disk peripherals results from the limitations in achieving full potential disk speed and from restricting use of total disk drive capacity.

Inefficient use of disk drive capacity is caused by three factors. First, disk sector size may not be matched to system block size. Second, the use of packing bits within the data format (to enable slow controllers to respond to different sector data fields) is inefficient. Third, media defects can reduce the space available for large, contiguous files.

Systems with long command initialization times can prevent disks from being used at full speed. These times are composed of the time required for software to load the command into the controller, and the time necessary for controllers to interpret the command and manipulate the disk address to point to the physical block on the disk. Only when these tasks are completed will the disk controller start using the disk for its main purpose: to store or retrieve data. Other reasons that disks are not used to full potential include inability to perform overlap seeks, occurrence of data late errors, time to switch from one drive head to the next, and interleaved disk data that is not matched to operating system requirements.

Controllers hold the key

These speed and capacity limitations can be overcome with a variety of carefully selected features in disk and tape controllers. The use of I/O parameter

blocks allows asynchronous operation between system software and peripheral devices. These blocks are set up in main memory by the CPU with chaining between the blocks. This method allows the peripheral device to access the next instruction from main memory. No software time is required to reload control registers, thus a much faster reinstruct time is provided.

A faster DMA channel allows concurrent disk and tape transfers, and enables data to be streamed from disk to tape. Large buffers allow software to run with multiple ring buffers in memory. Thus, interblock gaps are used fully, and the effects of disk seek times are minimized when streaming data between disk and tapes.

As previously stated, data late conditions can be avoided by using a large FIFO buffer. In a multitasking computer system, there are often peaks of DMA activity from other devices that require the slowing of the disk data rate. In order to avoid retries of the operation that waste both bus and CPU bandwidth, a revolution of the disk may be slipped. If an entire sector's worth of data is not present in a buffer ready to write onto the disk, or if there is not enough space in the buffer for the next sector to be read in, a revolution of the disk should be missed before transferring the next sequential sector to/from the system.

Disk data transfer rates can be enhanced by having a programmable sequence of logical sectors on each track. This feature allows sector skew to compensate for head switching time during spiral reads and writes. It also enables system timing to be optimized through the use of different interleave factors

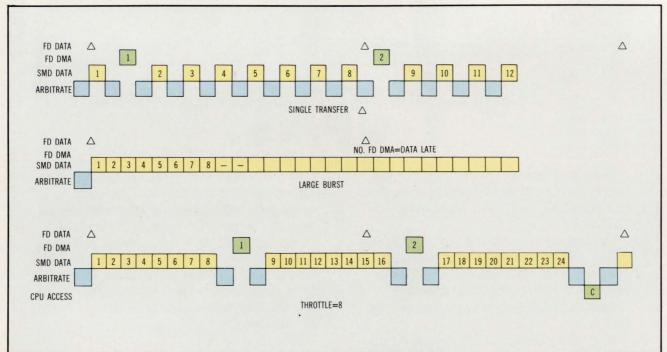


Fig 5 With a program defined DMA burst length (throttle), the system can be tuned so that high speed bursts from the disk or tape controller keep up with the peripheral's data rate, while time critical devices also get serviced.

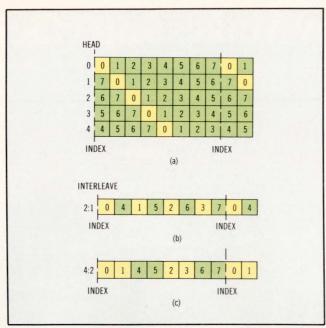


Fig 6 A programmable interleave factor for disk blocks can be used on systems with low bus bandwidth to decrease controller demands on the bus (a). When using single sector transfers, interleaving can be used to limit the effects of missing sequential sectors (b). By basing the interleave factor on groups of multiple sectors, performance improvements can be achieved where data blocks span more than one sector (c).

for data and program areas on a disk. Interleaving can also be based on multisector blocks to match software block size (Fig 6).

Inefficient use of the CPU is the third critical area affecting computer system performance. The amount of main CPU power, and time required to operate the peripheral device, is inversely proportional to the intelligence and the degree of function within the peripheral device. The better the controller capability, the less time is spent by the CPU to support the device driver, and more time is spent on application software.

Two examples of inefficient controllers include those requiring software handshaking to set up for an operation, and devices with nonstandard command structures and diverse completion information. Both of these limitations can be overcome using a unified I/O parameter block (IOPB). The IOPB allows drivers to be written in such transportable high level languages as C and PL/M. Additional overhead on the main CPU appears in systems that do not have automatic error recovery. High performance controllers can now be designed to retry an operation after an error occurs, and to correct a data error using error correction codes (ECCs). Thus, the main CPU is relieved of these tasks (Fig 7).

Peripheral controllers featuring this level of high performance are the Xylogics 400 Multibus peripheral controllers. Models 421 and 422 are combination 5½-in. disk and quarter-inch tape cartridge control-

lers. The 421 handles ST506 disk drives and is compatible with the 422, which handles Enhanced Small Device Interface (ESDI) disk drives. Model 450 is a high performance Storage Module Drive (SMD) disk controller that can handle from one to four disk drives, with a mixture of data rates up to 2 Mbytes. Model 472 is a half-inch tape controller that will handle both start/stop and streaming tape drives, with speeds from 12.5 to 125 in./s and densities of 800, 1600, 3200, and 6250 bits/in.

From software to controller

All four controllers use a simple IOPB system to pass commands from software to the controller. They can chain commands and interrupt either after each command or on completion of the final chain command. The disk controllers include automatic error detection and correction, using industry standard ECC codes.

The SMD disk controller and the half-inch tape drive controller include a high speed DMA sequencer that is integrated into a CMOS gate array on the 421 and 422 models. The DMA controllers can run at a transfer rate of 1.5 word transfers/ μ s. Thus, they allow other devices to use more than one half of the Multibus bandwidth when running a standard speed SMD or ESDI disk at 1.2 Mbytes/s. Even under these conditions, the controllers can transfer a full cylinder of data between disk and memory without wasting a disk revolution.

Large, pure FIFO buffers in these controllers permit full use of bus bandwidth in both small and large block transfer cases. A DMA data rate that is twice the disk drive rate ensures an "infinite" buffer under nearly all conditions of bus usage.

With today's high technology explosion, seemingly limitless applications, and ever-expanding need to interconnect systems and devices, open standards are not only desirable, they are becoming mandatory. The open system bus concept, such as Multibus, gives engineers flexibility to meet these needs. Available high performance disk and tape controllers for open system buses can relieve many of the bottlenecks that make IEEE 796 computer systems I/O-bound. This allows computer system designers to build integrated machines that will fully use the capabilities of present- and next-generation processor chips in an open bus environment.

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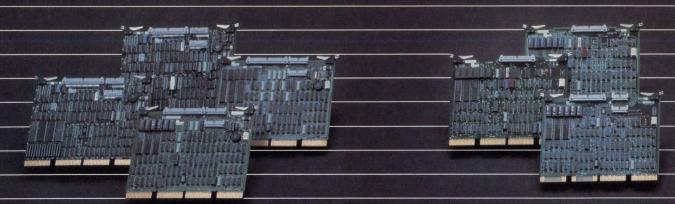
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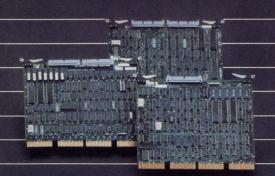


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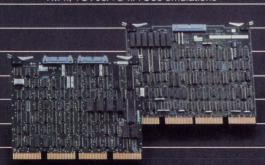
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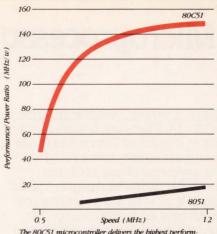
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CHOOSING THE BEST OPERATING SYSTEM

A number of trade-offs must be considered when selecting an operating system. The best choice depends on the intended use.

by Theodore F. Hatch, Jr, James B. Geyer, and Patrick E. Prange

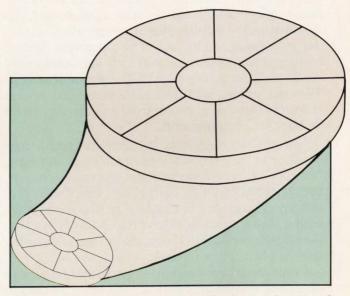
As operating systems become more complex, they tend to lose flexibility and require more and more memory space for their operations. Performance speed decreases, software maintenance requirements increase, and learning time for operators gets longer. On the plus side, unsophisticated user interface eases (eg, using automatic teller machines is easier). Because no one operating system can suit everyone, the trick lies in matching the operating system to each functional requirement in order to obtain the greatest efficiency and lowest cost for any given application.

An operating system's primary job is to make resources such as memory, processors, I/O devices, and data available to users. At the same time, the operating system should manage these resources efficiently and protect the system and its users from one another. Functionally, operating systems for multiuser processing applications share the computer's

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James B. Geyer is a principal staff engineer for operating systems at Honeywell, Inc, where he is responsible for defining and designing operating system extensions. He holds a BS in mathematics from Ursinus College, and an MS in mathematics from Syracuse University.

Patrick E. Prange is a principal staff engineer at Honeywell, Inc, where he is responsible for database development. He attended Michigan State University.



resources among users, while relieving each user of the task of reprogramming hardware for each new job. Single-user operating systems perform the same function, but their primary concern is assisting users and protecting users' data from their own mistakes.

Related developments

The first computer systems required that all instructions be entered in machine language. Early operating systems, called job-to-job monitors, were developed to perform the task of readying the machine for each successive job. Next, operating systems were developed to provide I/O operations overlapped with central processing, and to provide concurrent multiprogramming of several user programs stored in main memory. Time-sharing systems followed, allowing interactive use with the operating system managing resources to process requests as quickly as possible. Given sufficient resources, such operating systems make realtime applications possible, with the operating system providing almost instantaneous response.

As the first commercially acceptable general-purpose operating system, OS/360 (for the IBM 360 series) was capable of supporting multiprogramming, and

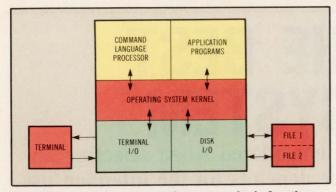


Fig 1 For a minimum operating system, basic functions include hardware resource management, command language processing, and runtime services for application programs.

batch time-sharing, and realtime applications. (Its 360 designation implies that it covers all points on the processing compass.) The operating system represents a complete software shell surrounding the hardware, and acting essentially independent of it. The user enters jobs and gains access to system resources through a job control language (JCL) with its own set of commands.

Current developments in computer technology continue to burden operating systems more and more. Networking, online transactional processing, security, user friendliness, data basing, and distributed processing all generate a demand for an operating system with a higher functional level (ie, the ability to support these new facilities more easily than when using only application software).

Commercial applications in particular require an operating system able to deal with sensitive data in almost constant use. For example, banking environments have operators and programmers not only working directly with a central system, but also customers at widespread locations operating automatic teller machines. All these users are trying to access the same data base simultaneously.

Establishing common ground

Before looking at the differences among operating systems, their common ground should be established. This requires looking at the mandatory elements that make up an operating system (Fig 1). At the very least, the operating system must hide hardware interfaces from the user and present a more generic, machine-independent face to application programs. To accomplish this, three basic functions must be provided: hardware resource management, runtime services, and command language processing. The operating system allocates and deallocates main memory, I/O devices, disk space, and CPU time, and should allow programs to run unaware of the details of the hardware used. For example, programs are not tied to a specific memory location or single disk unit. The operating system provides basic services such as program loading, intertask communication,

and timer functions. It includes a command language processor to respond to typed-in commands.

In performing these functions, the operating system is responsible for handling transient hardware errors (many in such a way that correction remains invisible to the running programs or the user). Acting as the machine's policeman, the operating system segregates users from one another, and protects itself, the rest of the machine, and other users. In this way, effects of an error are confined to the user who initiated the error. The operating system often provides logging and accounting of system activities for an administrator.

Beyond these three basic elements, most operating systems include extra or optional functionality. Many designers place operating system elements directly in the application software. These elements may not be of particular interest to all users, although they may be essential to some.

These optional features include data management, screen-format management, graphics, communication

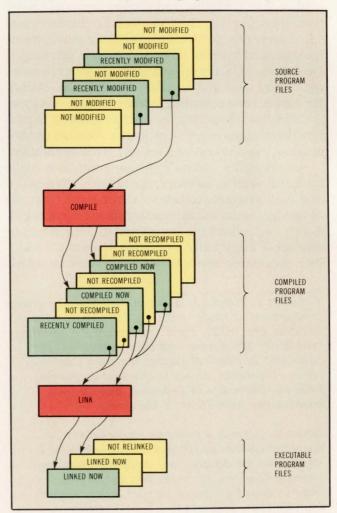
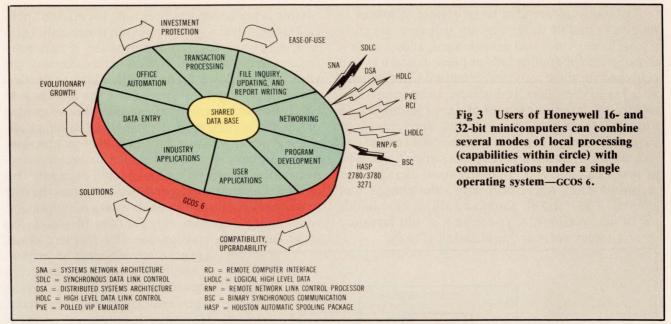


Fig 2 Under Unix, to create a consistent, up-to-date set of programs, the "make" command recognizes which files must be compiled and/or linked, and does only the necessary operations.



protocols, networking capability, language compilers, and utility programs (such as text editor and file copy/print). Nearly all multi-user operating systems include these features to some extent. The real differences come in the depth to which any given activity is supported. These include the number and types of communication protocols, file organizations, user interfaces, and language compilers offered as part of the operating system as well as how easy these facilities are to use.

In many cases, adding extra facilities to the general operating system causes a loss of execution speed (performance) in specific functions. As such, these complex operating systems actually represent a trade-off. As the system begins to offer more generalized capabilities, the operating system occupies more and more space, and individual functions may become slower. Some applications cannot be carried out as efficiently as would be possible with more specific or more flexible programming.

For example, an operating system supporting widely varying applications must present different interfaces to varied classes of users who require separate services. Among other things, the ability to handle individual interface layers, such as menu selection versus control language job sequencing, must be present. Thus, operating system capability must be extended once again to create a generalized system, as more repetitive tasks are removed from individual application programs. Conversely, a single way of doing things may be forced on all users, reducing the flexibility achieved by leaving these functions within the application software.

Two prime examples of this divergence in approach are represented by Unix and Honeywell's GCOS 6 operating system. AT&T Technologies' Unix system perhaps best reflects the "bare-bones" approach that

emphasizes performance and flexibility, while placing the burden of many optional functions onto the user application software. Meanwhile, GCOS 6 was developed to support varied commercial applications. The design approach emphasizes user orientation and internal protection versus speed of execution, while allowing easy optional configuration and expandability. Since both approaches mean trade-offs in one area or the other, neither can be said to offer the best solution for everyone. However, each offers an excellent solution for its intended market.

Reviewing the Unix story

One of the real success stories of software engineering is that of Unix. The system was developed by AT&T after its withdrawal from a joint project involving Massachusetts Institute of Technology (MIT), General Electric, and Honeywell. This project was aimed at creating a general purpose system for diverse users.

Instead, AT&T began to work on a system for programming research and development. The AT&T group's intent was to design a program development system with a powerful control language that could operate independent of specific hardware. The system they designed was subsequently rewritten in the high level C programming language, which required more space than assembly language. C language vastly increased portability, however, making this system one of the more easily understood and quickly learned operating systems available. The result has proven widely popular and, although it was originally designed for Digital Equipment Corp's PDP-11, it is also available for implementation on a wide variety of machines ranging from micro- to minicomputers and mainframes. It is available in many versions, with differing levels of complexity.

As Unix was intended to be simple, it leaves as much as possible to application software. Its great strength lies in program development, allowing users to program for applications as needed, and it is well equipped for these activities. Standard Unix includes an array of compilers, text editors, debugging tools, and traces. It permits output of one program to feed directly into another to simplify the development of large software systems. Unix source code control system stores, updates, and retrieves multiple versions of programs and text. In doing so, it changes and records "who, when, and why" the change was entered. The "make" command allows easy building of new versions, or re-creation of old versions, of a complex software application (Fig 2).

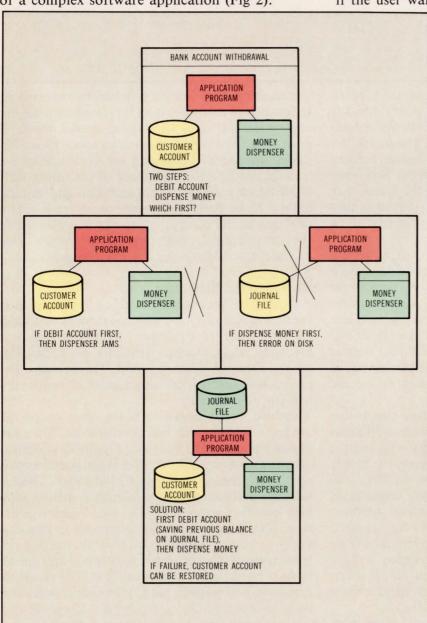


Fig 4 Data recovery mechanisms are necessary for commercial transaction processing. The two center diagrams show how errors can occur, while the proper sequence (below), ensures smooth operation without data loss.

Unix is particularly appropriate for ad hoc applications (ie, when a system does not necessarily know what may be asked of it). For instance, if an inquiry requires data manipulation in an unforeseen way, the Unix user has powerful tools with which to develop a way of getting the answer. Once the answer is in hand, the ad hoc program can be either discarded or saved, according to need, rather than automatically putting the application into everyday production.

The system's great weakness lies in data management. I/O is stream rather than record oriented. This facilitates hardware independence but forces the user to write program code to handle data management. In addition, Unix uses only random file access, so if the user wants to organize files further, again,

application code must be written.

Similarly, Unix uses a shell concept for user interface, providing a powerful command interpreter. However, to interface at other levels (such as menu selection). custom shells must be added. Also less emphasized are security safeguards, error handling, and recoverability. While Unix allows for added capabilities in these areas. their extent in the standard versions is insufficient for some commercial applications.

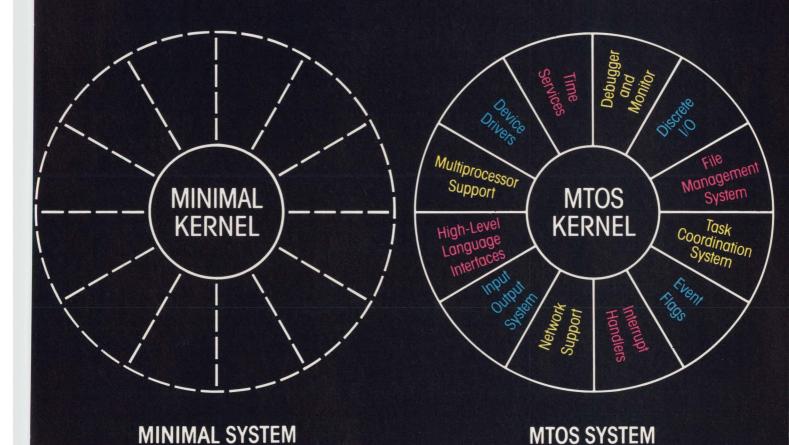
In sum then, Unix reflects its roots. It is very strong on program development but its lack of data management facilities can make Unix difficult to use in commercial data processing where the emphasis is on day-to-day production environments.

A general alternative to Unix

Honeywell's operating system for its DPS 6 mini/micro line, GCOS 6, owes its roots to the same MIT project that gave birth to the Unix development effort. Unlike AT&T, however, the goal for Honeywell remained a general purpose operating system for the commercial operations less well served by Unix.

The markets do, in fact, present different requirements, emphasizing data management over ad hoc program development activities. For example, a commercial information processing operation will usually have data that, if lost or mishandled, could result in either

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The standard-setter in operating system software

financial or time loss. Such users are more concerned with data integrity and system recovery than in a typical software development-oriented operation. In addition, when the operating system must interface with various classes of users, system applications for users of command language, transaction processing and network, and realtime applications all require different capabilities.

In designing a general purpose operating system, decisions must be made as to how well the operating system will support each class of users. The intent is to create a system that supports all functions and users at an acceptable level of performance. In its current form, GCOS 6 (Fig 3) offers a wide range of facilities including interactive multiprogramming, realtime and batch processing, as well as data communications. The operating system can be configured to process different applications concurrently. Programs or multi-user subsystems run in their own operating environment, protected from one another, sharing the resources of the hardware as allocated by the operating system.

The divergence in operating system design is a function of intended usage, not a question of better or worse.

The file system also allows programmers to work with a variety of data organizations such as indexed sequential, rather than simply random access files. Error protection and system recovery capabilities include controls for concurrency and journalization within the operating system to help maintain data integrity. For example, if two users attempt to update a single file at once, concurrency controls cause the operating system to sequence each user and start one over (if necessary) without the users being aware of the problem. Inconsistencies resulting from simultaneous access are also eliminated. Similarly, the journalization function keeps a record of all transactions, usually on disk, so that a power failure will not cause the loss of the second half of the dual transaction (as when a bank must debit one account and credit another), as shown in Fig 4.

Since it is a single operating system serving many masters, this system was designed in a modular form that allows customization or tunability to suit individual information processing operations. The system has been implemented in such a way that certain functions can be kept either on disk or in memory, depending on user preference and their importance to the particular operation. Frequently-used facilities can be kept in memory, while those needed less often can be stored on disk and loaded as required. This system also allows for easy expansion or reconfiguration. If greater capability is needed in a given area, subexecutives can be added to increase performance.

As expected, all of this added functionality brings trade-offs in system performance. For the designer, it means making a series of choices among functionality, system performance, and memory space required for the operating system.

The essential questions in operating system design center on the amount of memory required by the operating system to perform its functions and how fast it must perform those functions. On one side of the equation lie error protection, ease of use, and multifunctionality. On the other are flexibility, the speed with which functions are carried out, and the amount of memory available.

The error recovery, multifunction capability, and user friendly interfaces provided by the system, for example, consume memory space and affect operating speed. Facilities such as journalization, concurrency controls, and subexecutives provide the redundancy and ease of use required for commercial applications, but inhibit optimal performance and can prove burdensome to some users, such as those involved in ad hoc programming. In the ad hoc environment, the principal user is more likely to be a programmer than a data entry worker. Rather than entering repetitious data in a strict format, software development is the main activity, and delegating tasks to the application level increases the overall flexibility of the system.

In addition, the use of the C language in Unix not only promotes portability, but also allows easy maintenance. The assembly language used in GCOS 6 and many other multifunction operating systems helps relieve the pressure on memory resources that arise from the system's complexity. However, it makes the system more difficult to learn and maintain.

The divergence apparent in operating system design, then, is a function of intended usage, not a question of better or worse. With a system such as Unix, the programmer has a powerful tool with which to develop custom application software and meet day-to-day demands. With systems such as GCOS 6, the user trades away some flexibility and ultimate speed, but gains in data protection and avoids the necessity of reinventing the wheel in each of the varied tasks the system will be called upon to perform. Today's computer market provides ample room for both.

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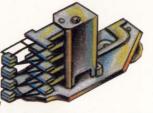
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THIRTY-TWO BIT MICRO TAILORED FOR HIGH LEVEL LANGUAGES

A symmetrical architecture, multiple addressing modes, and slave processors support efficient high level language compilers in a 32-bit microprocessor.

by Jonathan Ryshpan

Much of today's software for 16- and 32-bit microprocessors is compiled from high level programming languages. Compilers, for machines with modern architectures, can now generate code that is nearly as compact and as fast as hand-assembled code. Moreover, the large software projects done on these machines simply can no longer be accomplished using assemblers or macroassemblers. While microprocessors of the new generation appear to offer address ranges sufficiently large to accommodate most application programs, they differ in the extent to which their architectures are adapted to support high level language compilers.

The NS32000 family was developed to support high level languages, to allow architectural extensions via slave processors, and to provide the same 32-bit internal architecture with 8-, 16-, and 32-bit external data paths (Fig 1). The 32-bit internal architecture is designed to support today's high level compilers and to generate compact, flexible code. It is symmetrical in that it allows a complete choice of addressing modes and data types for almost all addresses of almost all instructions. The instruction set itself is relatively small and contains a minimum number of special cases. Floating point and memory man-

agement instructions allow direct use of the floating point unit (FPU) and/or the memory management unit (MMU) and/or custom slave processors. In addition, the NS32000 family has a uniform linear address space of 16 Mbytes, which is the preference of such programming languages as C and Pascal.

Symmetry in reference to machine architecture can also be termed regularity or orthogonality. It relieves the programmer of having to decide which data type and addressing mode to use for every instruction. Conversely, it frees the programmer from only being able to use the instructions available for a given address mode or data type.

A symmetrical architecture is a vital tool for writing a compiler that produces fast, reliable code. If architectural asymmetry creates serious difficulties for assembly programmers, it creates nearly insolvable ones for the authors of compilers. The problems of generating code for an asymmetric architecture are so great that the irregular parts are often just discarded and "fancy" features that promise to produce fast code in special cases are never generated by the compiler.

Even machines that have a large number of general-purpose registers require compiler writers to immediately dedicate a fair number of them, thus leaving a smaller number of general registers to work with. By dedicating the program counter, the static base, the frame pointer, two stack pointers, and an interrupt base, the NS32000 family has saved the compiler writer trouble and enforced a degree of consistency across a range of programming languages. Presuming that the majority of uses for the family would involve high level languages, the designers feel that more than eight general-purpose

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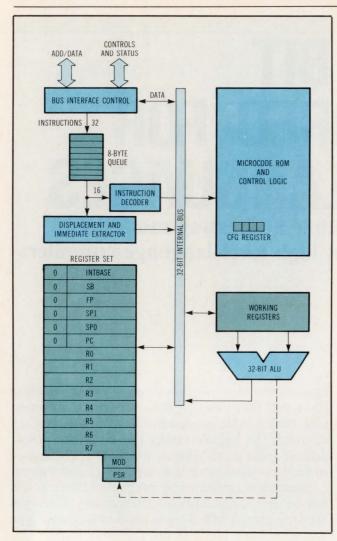


Fig 1 The only difference between NS32000 family members is in the data bus interface section (shown here for the full 32-bit NS32032). Dedicated registers aid consistency in implementing compilers, while eight general-purpose registers provide a high degree of flexibility. The configuration (CFG) register is loaded at system initialization to signal the presence of slave processors.

registers—given the dedicated registers provided—will increase the length of the addresses and be a waste of silicon. Of the NS32000's fourteen 32-bit registers, six are dedicated and eight are left as general-purpose registers. There are two 16-bit registers, the processor status register and the module register, and a 4-bit configuration register.

The only instructions that do not specify a general-purpose operand are those that jump and branch relative to the program counter, those used for saving registers in context switching and memory management, and some that allow use of displacements in addition to general operands (bit field instructions). The NS32000 family keeps its basic instruction set small by not having separate instructions for different data types and addressing modes, and allowing the programmer to specify these things in the general instruction format.

These machines implement memory as one uniform linear address space as opposed to segmented addressing. Thus, even when using memory management techniques requiring page translation, swapping of multiple users, or implementing of virtual memory by translating logical addresses to disk, any program or data structure appears to the processor as a set of addresses in the 16-Mbyte range. This is again well suited to languages such as C, which are based on the assumption of an infinitely long string of memory locations.

One group of instructions that is particularly suited to the needs of high level languages is the bit field instruction set. Specific "extract" and "insert" instructions enable the processor to pull out any bit field from 1 to 32 bits, regardless of word boundaries, and to put it back wherever desired. This eliminates the extra instructions needed to align the bit field after it has been subjected to logical operations. Because code generators often use bit field operations every four or five instructions, this is of particular importance for compilers. Having these steps in microcode not only reduces the size of the code generator, but also makes it run faster.

Addressing the data

In order to generate efficient code for high level languages, these machines provide facilities that fit the model used by modern, block-structured languages such as Pascal, C, Ada, and Modula-2. This model is tailored to support reentrancy and recursion by keeping the local variables and arguments for modules and procedures on the stack and by referencing them via CPU registers. Addressing modes that can access locations on the stack so that they are functional extensions of the processor's register set are also used as references. These addressing modes, called the memory space modes, use any of three CPU registers, the stack pointer, the frame pointer, and the static base register.

As procedures are called, the frame pointer is used as the index register from which their data elements are referenced. Thus, for any currently running procedure, the stack is where the important elements are kept, and they are referenced relative to the frame pointer. Each procedure has a private variable space and does not interfere with another procedure's area.

In Fig 2, as each procedure is called, its return address is pushed onto the stack. As other elements are pushed onto the stack, the frame pointer indicates a place in the stack that contains the next level's address—a thread back through the stack's structure. The elements of a given procedure are addressed relative to the contents of the frame pointer. At the far right, the elements of the frame for the procedure P2 are accessible relative to the frame pointer. When P2 is finished, its stack frame goes

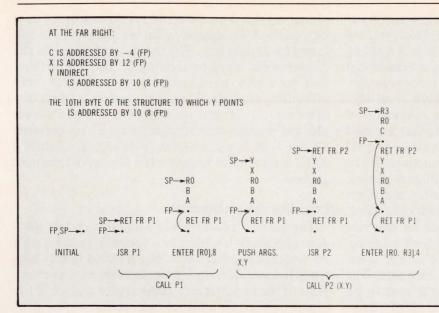


Fig 2 The stack grows through various operations. At the far right, the frame pointer contains an address that points to an address just below P2, which in turn points to a location just before P1. The program can keep the procedures it is currently running in order.

away and the frame pointer drops down one reference level, freeing space on the stack for other procedures. Just as important, the elements of the frame for the procedure P1 are again addressable relative to the frame pointer; they have not been destroyed and do not need further address recalculations.

In this example, P1 has no arguments and uses two local 32-bit variables: A and B. P2 has two arguments, a 32-bit variable and a pointer to a structure: x and y, respectively. It also uses one 32-bit variable: C. The variable is not required to be 32 bits, since the NS32000 series allows access to any variable at any byte location. The JSR P1 instruction at the lower left of the figure (executed by the caller) invokes P1 and pushes the return address onto the stack. The ENTER [R0], 8 instruction adjusts the frame pointer to the base of the working storage (ie, the frame) for this invocation of P1, and pushes its old value onto the stack. It also allocates 8 bytes for variables A and B, and saves R0 (which is needed for working storage) on the stack. When P2 is invoked, the caller, P1, starts by pushing the arguments X and Y onto the stack and continues in the same way as in the invocation of P1.

This arrangement not only helps a compiler writer produce an orderly set of calling conventions, it is also helpful for assembly programmers. The frame pointer references the beginning of a space on the stack where all the local variables are kept. Reference to them all is made simply by address relative to the frame pointer. Variables indexed from the frame pointer can be used via the memory space modes in the same manner as variables stored in CPU registers.

This use of the memory space addressing modes is an extension of a more familiar mode, register relative. But, instead of addressing to any place in memory relative to a general-purpose register (which has its own uses), the dedicated memory space reg-

isters are used to point into the stack area where all the procedure variables are kept and organized. This makes for efficient memory use and speed, and gives the programmer an easier overview of reentrance and recursion.

Scaled index mode is another addressing mode designed to help manipulate data in arrays. Using the address generated by any other addressing mode (except immediate or another scaled index) and adding the contents of a general-purpose register to it, scaled index mode finds the effective address. Before adding the contents of the general register, this mode multiplies its contents by 1, 2, 4, or 8. In this way, it conveniently accesses any element of an array whose first element is addressed by any other addressing mode.

Another addressing mode, the external mode, supports modular software, and allows modules to be linked quickly and easily. For every module, there is a link table, containing pointers to all objects referenced via external mode. A reference using this mode gives the number of the entry in the link table containing the pointer. A displacement is then added to the pointer to give the address required.

Thus, all external references for a module are gathered into a single table. With everything that the linker needs to modify in one place, it can run very quickly. This makes it practical to run at program load time or during execution. Using this, it is possible to support common runtime libraries (ie, facilities available to all programs in a system), and still not require that programs using the library be relinked when the library changes. Most other computer architectures make linking a slow process, since the references to external variables are scattered throughout the code.

The use of this mode carries a speed penalty in contrast to the generation of an absolute runtime image, but the benefit is relocatability. It allows the program to defer worrying about where an object will actually be located until run time. However, external addressing is only an option. There is nothing to prevent programmers from using a traditional linkage editor to produce an absolute runtime image.

Use of 32-bit architectures and high level languages has necessitated efficiency improvements in using displacements, or those numbers that are used to offset from a base address in a register to find data in memory. Large programs sometimes make use of large displacements. Most displacements, however, are relatively small and most machines implement displacements as large as their data word. Thus, the largest displacement in an 8-bit machine is 8 bits (256 bytes), the largest in 16-bit architectures is 16 bits (65,000 bytes), and so on. A 32-bit displacement (4 Gbytes) should be adequate. The problem now is that using 32 bits for 8- and 16-bit displacements, which make up 90 percent of all displacements, can be very wasteful.

In the NS32000 family, displacements can be 7, 14, or 30 bits, with the size of the displacement marked in the first one or two bits of the displacement itself. For example, a 7-bit displacement will be a 0 followed by seven data bits (ie, 0xxxxxx); a 14-bit dis-

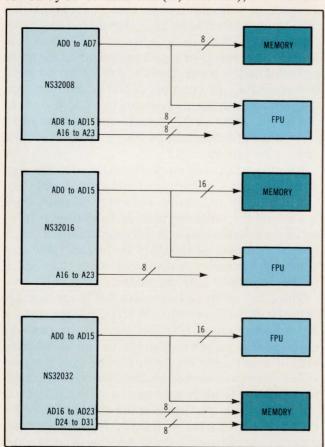


Fig 3 The floating point unit (FPU) interfaces to all three family members as a 16-bit device. The paths shown are the data/address lines as they exist as data paths during the data portion of the multiplexing. On the address side, all CPUs can address a full 24-bit range.

placement is a 2-bit field (10B) followed by 14 data bits, and a 30-bit displacement is two ones (11B) followed by 30 data bits. The processor recognizes the displacement range by looking at the first bits and does not need to use an entire double word for every offset. For example, when it recognizes a 1-byte displacement, it converts the last 7 bits to a two's complement number that represents an offset between 63 and -64 bytes: a 14-bit is ± 8 Kbytes, while a 30-bit displacement ranges ± 0.5 Gbytes off the base address.

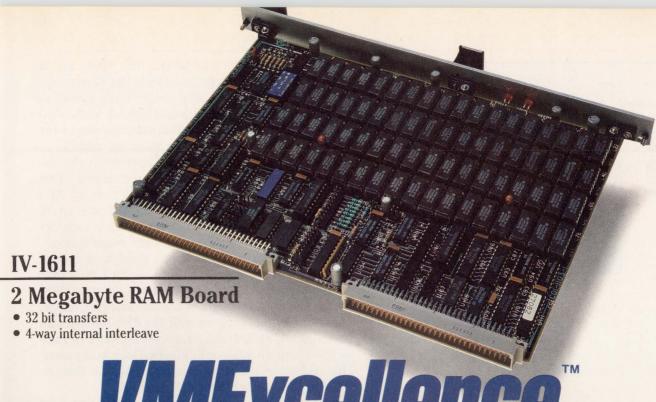
Extending the architecture

The use of coprocessors to accelerate certain standard operations has become a common practice with 16- and 32-bit processors. The NS32000 family currently has two such slave processors that act as extensions of the architecture. There is also a place in the instruction set for another, user-defined slave processor. The two standard slave processors are an MMU and an FPU. Since the only difference between the processors of this family is in the onchip data bus interface unit, it was possible to design slave processors that work with all family members. The only exception is that the 8-bit NS32008 does not support memory management and so cannot be used with the MMU. All data transfers with the slave processors are 16-bit transfers.

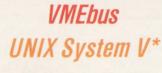
With the NS32032, the first 24 data lines are multiplexed with the 24 address lines; the 8 high order data bits are not multiplexed, and the first 16 are used for data transfers to the slave. On the NS32008 and the NS32016, data lines are also multiplexed with the corresponding address lines. When connected to an FPU, the NS32008 uses its first 16 address/data lines as a 16-bit data bus (Fig 3). A relatively simple communication protocol allows a slave processor to take advantage of all the CPU's addressing modes while devoting a relatively small portion of its own silicon to communication.

The MMU, unlike the FPU, has its own onchip bus interface unit, which enables it to access the bus on its own behalf. When the CPU sends the MMU a virtual address and the MMU cannot find the physical translation in its cache, it translates the virtual address into the physical address, then outputs it on the address bus (Fig 4) and updates its cache.

When the MMU receives a logical address from the CPU, it first goes to the address page table where it finds a pointer to one of $256 = 2^8$ pointer tables, each of which holds $128 = 2^7$ page pointers. Each of the pointer tables occupies exactly one page and can itself be paged out to disk storage. This gives it a 15-bit number that identifies the page in physical memory (which may be on disk or in RAM). To this, it appends the 9-bit offset from the logical address supplied by the CPU to find the address in physical memory.



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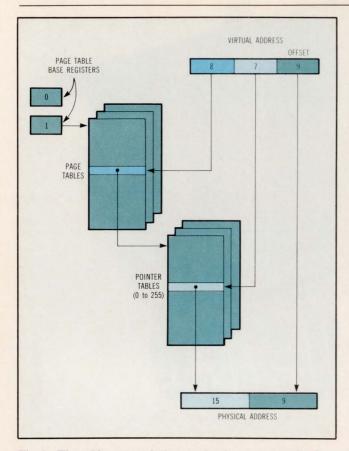


Fig 4 The address translation mechanism uses two levels of page pointer tables. By loading a different base address in page table base register 1, the system can switch between completely different 16-Mbyte memory maps at a single stroke.

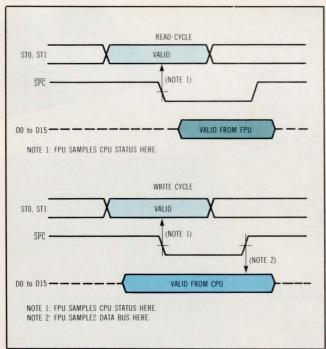


Fig 5 The slave processor protocol for both read and write transactions in both directions is controlled by the slave processor control (SPC) pulse. Status signals whether FPU is taking data, returning a result, or signaling an error.

To speed address translation, the MMU has a 32-element, onchip cache that holds the 32 most recently accessed virtual addresses (15 bits), as well as their translated physical address (16 bits). If the CPU requests a (logical) address that matches one of the entries, the MMU accesses the physical address in one memory cycle. Otherwise, it performs the address translation without CPU intervention. This takes 16 clock cycles. But, if the MMU must do a translation, it updates its cache. The MMU can check the cache on every memory cycle because it checks all 32 locations at once rather than sequentially.

In every NS32000 family CPU, there is a special 4-bit configuration register that tells the CPU's control logic whether a slave processor or support chip, such as the NS16202 interrupt control unit, is present. The 4 bits, C, M, F, and I, tell the CPU whether an MMU (bit M), an FPU (bit F), a custom slave processor (bit C), or an interrupt unit (bit I) are being used. This register is set at system initialization time to indicate the hardware actually present.

Especially in the case of the FPU, this allows chip designers to create a relatively simple part that still uses all of the powerful addressing modes needed by modern compilers. A custom slave, whether as a single chip or as a multichip design, has the same advantage of a simple interface to the full power of the CPU's addressing mechanism.

In communicating with the FPU or any other slave, the CPU prefetches all instructions and operands using any of its addressing modes. Instructions and operands as well as ID codes are exchanged with the FPU via the 16 data lines. All transactions between CPU and FPU depend on the slave processor control (SPC) signal, which is one clock wide. The status bits (ST0, ST1) are sampled on the falling edge of SPC. Data is sampled on the rising edge of SPC, either to or from the CPU, depending on whether the status bits indicate a read or a write cycle.

A slave protocol (Fig 5) starts by sending the slave ID via the data bus. The code activates the appropriate slave processor. On the next data cycle, the CPU sends the opcode, prefetched from its instruction stream, followed by the appropriate number of operands. When the FPU gets all the operands, it processes the data and signals the CPU when ready. Status is signalled first so that if the CPU sees an error code, it can execute an FPU error trap.

Slave processor errors, be they from the MMU or the FPU, cause the CPU to abort the current instruction, save its status on the stack, and trap to the operating system. The system can then check the status of the slave processor to determine the cause of the error. This does not necessarily halt the operation. A trap from the FPU usually indicates an arithmetic error such as size overflow or division by zero. Typical operating systems allow application programmers to indicate how they want such traps to be handled.

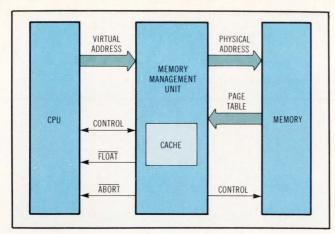


Fig 6 The MMU occupies both the address and data buses. In addition to address translation and caching 32 such translations onchip, the MMU can cause the CPU to abort an instruction on a page fault and save its status while the operating system tries to correct the fault and schedule another task.

If no FPU trap management has been supplied by the application, it is terminated.

A trap from the MMU usually indicates a page fault or protection violation. A page fault is an attempt to access a logical address that is not mapped into any physical address, but corresponds to data on the disk. The MMU responds to a page fault by activating the ABORT line (Fig 6) to the CPU, which will halt the memory cycle and store its status on the stack. The operating system then swaps the needed page from the disk to the physical memory in place of another physical page, which it writes back to disk. At this point, the aborted instruction can be retried. While this is taking place, the operating system can run other processes. A protection violation, such as an attempt to write to read only memory usually results in termination of the offending process. However, some operating systems do allow a task to manage protection violations in the same manner as FPU errors.

To efficiently serve multiple users, the NS32000 family's memory management scheme provides quick switching of large and complex memory maps. Since programs can require completely different arrangements of their 16 Mbytes of virtual memory, rapidly switching contexts among users can be cumbersome. The MMU is pointed to the memory address page table by a single number. That number is the table's base address which is stored in a page table base (PTB) register.

Various user's page tables reside concurrently in physical memory so that the CPU only needs to write one other value into the PTB register to entirely remap memory. When this is done, the MMU's 32 cache registers are invalidated to make room for addresses from the new memory map. Also, applications do not contend with the operating system

because there are two PTB registers: one for the supervisor mode—the operating system— and one for the current user. Thus, it is possible to rapidly change the entire mapping of the system. And, during those times when a task requests a service that will open a short, but not insignificant time window such as a DMA request, the operating system can easily schedule another user's task by simply changing the PTB register.

The combination of a symmetrical architecture, a wealth of addressing modes, and the existence of slave processors have made this family of CPUs well adapted for use with today's high level language compilers. In addition, the 8-, 16-, and 32-bit data bus options give the designer a range of price/performance options. The simple protocols involved with using slave processors do more than make their inclusion easy for the system designer. They also make progress towards the goal of having slave processors and CPU reside on the same piece of silicon.

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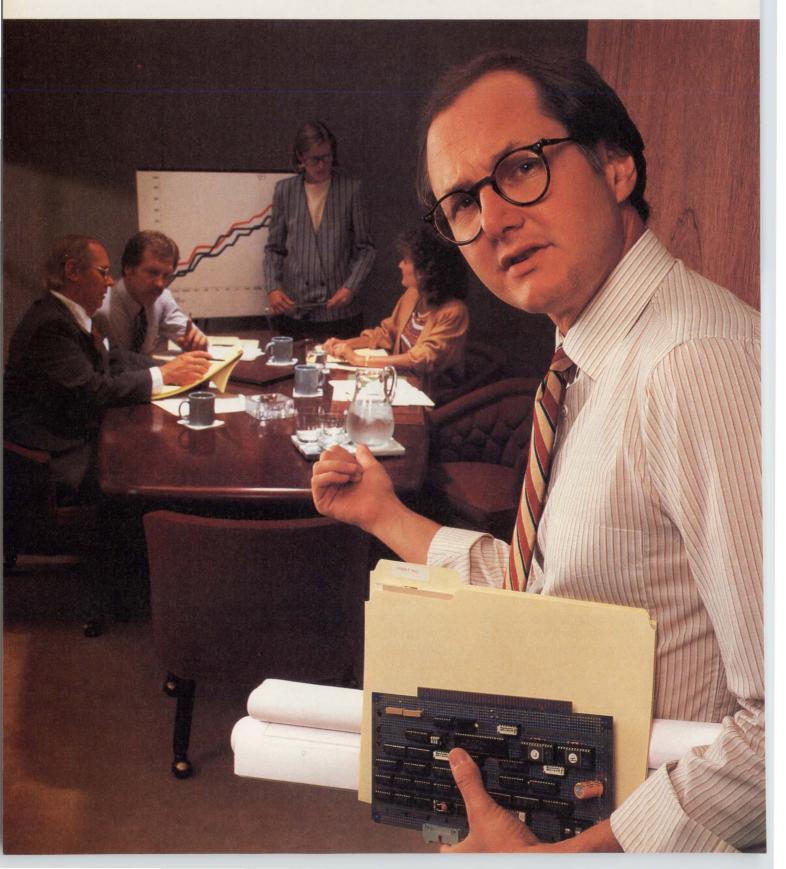
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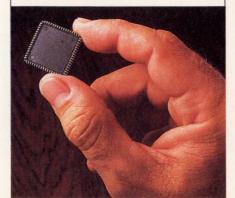
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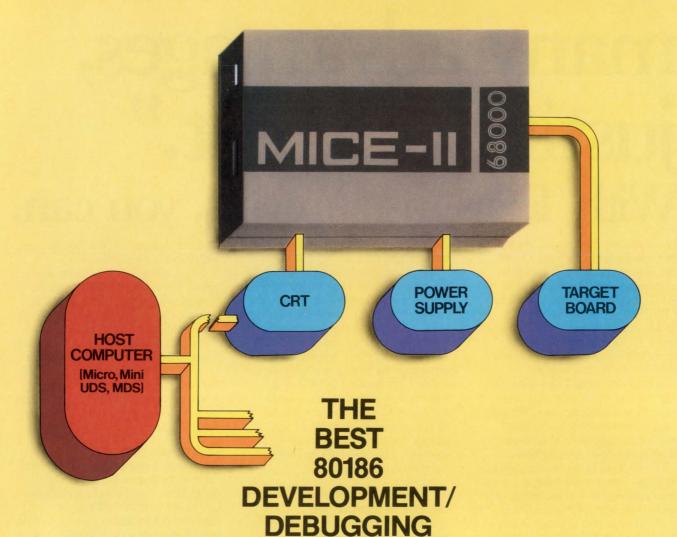
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NONVOLATILE MEMORY GIVES NEW LIFE TO OLD DESIGNS

Terminals and other equipment can be made more flexible, and product life can be extended by upgrading and customizing with NOVRAMs and EEPROMs.

by Richard Orlando

The recent appearance of low cost, 5-V nonvolatile memories has led to design applications that can be broken into two distinct classes. One class uses nonvolatile memory to store such data as configuration or calibration parameters. This information can be updated and then stored in the device for access on power-up. The second application uses nonvolatile memory for program storage. Here, the nonvolatile memory's main advantage is that content can be updated or changed remotely, rather than by device replacement.

Unfortunately, many end products completed prior to the availability of these devices are threatened by newer designs. The latter take advantage of the added flexibility and features afforded by nonvolatile memory. There are, however, ways to add nonvolatile memory to existing designs without a major redesign.

For example, consider the schematic of an intelligent terminal design, which will be used to illustrate methods that improve the flexibility of almost any microprocessor-based design (Fig 1). Here, the 6800 processor is the source of the "intelligence" in

the design. The serial communication channel is through a 6551 asynchronous communication interface adapter (ACIA), which features an onchip baud rate generator. A 2716 erasable PROM is the program store for the 6800, and the two 2114 RAMs provide 1 Kbyte each of buffer, stack, and parameter storage. The keyboard is an ASCII-encoded type whose inputs are fed through one port of a 6821 peripheral interface adapter (PIA). The other port of the 6821 receives the dual inline package (DIP) switch settings for such user-defined operational parameters as baud rate, parity, and protocol selections.

Video control is provided by a 68045 (or 6845) CRT controller. The display RAM interface is set up as a tightly coupled, shared RAM interface. The timing

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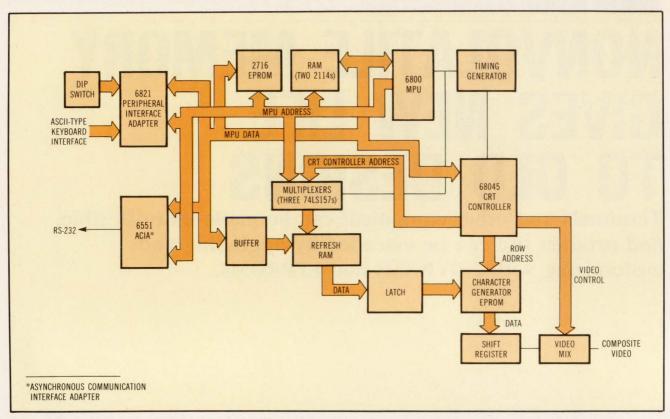


Fig 1 The original terminal design has dual inline package (DIP) switch settings that must be read by the processor. They are then parsed to determine setup parameters invoked from the terminal program contained in the EPROM.

is such that the CRT controller only accesses the data in the display RAM during the bus "dead" time of the 6800. This allows the processor to access the data in the display RAM at any time, regardless of the state of the CRT controller. The CRT controller can access the RAM transparent to the processor, and thus can relieve the processor of any access arbitration tasks.

Improving the design

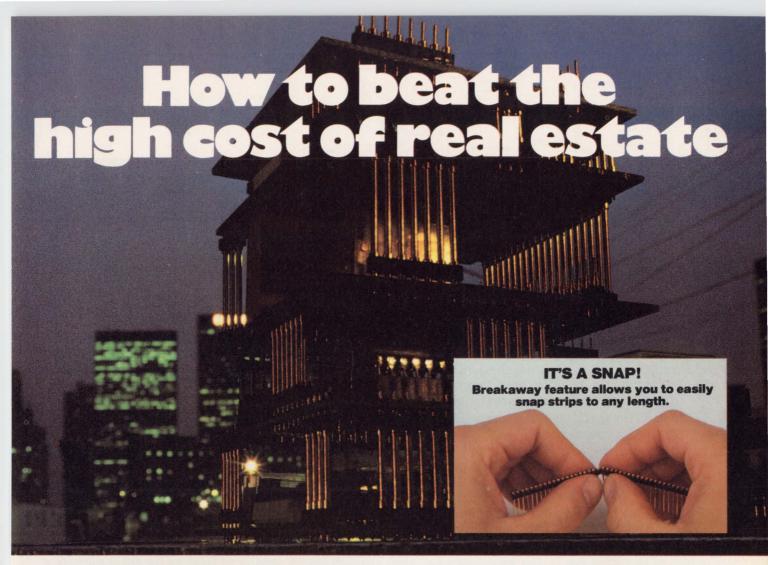
Although the design serves its initial purpose, several areas, which will make it more flexible and possibly extend the life of the product, can be improved. Intended for use in a variety of applications, the original design relies primarily on software for its characteristics and "feature set." Simple changes to the erasable PROM containing the 6800's software allow such terminal "customization." This approach is adequate when end-user needs are known prior to manufacture. However, if a user wants to upgrade an existing terminal, someone must perform a costly EPROM change in the field. The same penalty applies to the manufacturer who wishes to "upgrade" the software of the existing units in the field, in order to increase performance or to eliminate possible errors.

The second area in need of improvement is the DIP switch used for the input of user-definable parameters. It creates many manufacturing problems, since most DIP switches cannot be

handled by automated assembly equipment, such as insertion machines and wave solderers. Additionally, because someone must manually toggle the switch through a sequence of positions in order to fully test the boards, DIP switches slow down automated board testing. Also, to change parameters, a DIP switch requires the terminal user to remove an access panel and manipulate switch toggles while referring to a manual. As the range of user-definable parameters expands to include such features as emulation modes, the problem becomes even more awkward.

In the example terminal, added features and enhancements can be made in two ways. The first involves replacing the DIP switch with an X2443 serial NOVRAM, which is used to store user-defined setup and configuration parameters. The second replaces the EPROM with an electrically erasable PROM.

The NOVRAM, a 256-bit serial device, is organized as 16 words of 16 bits each. All communication between the device and the processor is done in a bit-serial fashion using the data in input, data out output, and the synchronous clock lines shown in Fig 2. All operations are controlled by the microprocessor through the serial interface. Read and write operations are executed through the transmission of a specific 8-bit instruction code with an embedded address of the word to be accessed. In the write operation, the processor follows the write command with 16 bits of data to be written. In the



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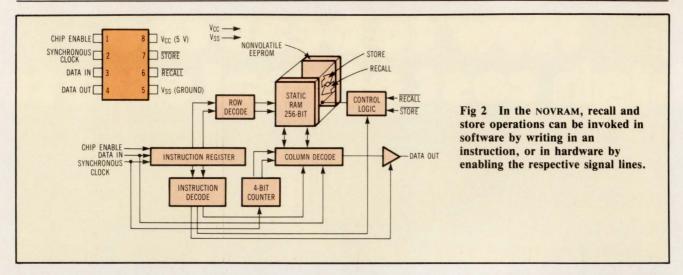




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read operation, the processor supplies the read instruction, and then gives the X2443 16 clock cycles, which the device uses to output the data to be read. The NOVRAM also includes several non-data types of instructions to control the nonvolatile operation of the part, the part's power consumption, and the write/store lockout feature.

The X2443 is designed to interface with single-chip microcomputers when the main consideration is minimizing I/O lines and software overhead. This device also works well in microprocessor-based designs requiring upgrading with minimal design changes. It consists of a serial static RAM overlaid or "shadowed" bit-for-bit with a 5-V EEPROM array, as shown in Fig 2. The execution of a store operation, either from the input STORE or by the execution of the software store instruction, transfers the current contents of the SRAM en masse into the nonvolatile EEPROM array. In a similar manner, the execution of a recall operation, via the RECALL input, transfers the contents of the nonvolatile EEPROM array into the SRAM array. On power-up, the contents of the EEPROM array are automatically loaded into the RAM array for a default configuration.

When using the X2443 to replace an existing DIP switch, it is advantageous to drop the NOVRAM into the existing switch "footprint." Fig 3 shows the simple conversion of the existing site or socket (a) to accept the X2443 (b). Four of the eight 6821 I/O lines used to read the DIP switch are already mapped into pins 1 through 4 of the NOVRAM. These lines originally input the current settings of the DIP switches, but can be configured through the 6821's data direction register to serve as the three outputs and one input needed for interfacing the NOVRAM. Since hardware STORE and RECALL signals are not needed in this application, they are simply tied to V_{CC}. All nonvolatile operations occur through software control, whose requirements are relatively

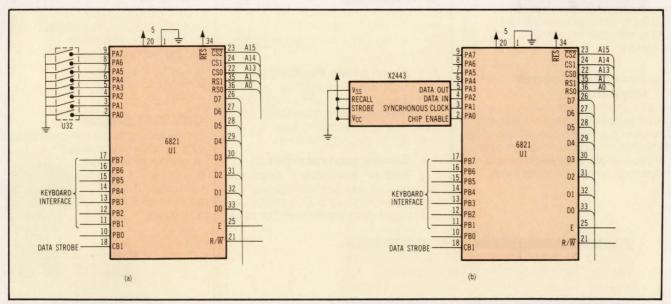


Fig 3 Within both the original DIP interface (a) and the X2443 implementation (b), the interface is serial. Therefore, only the clock, enable, data input, and data output lines need to be used.

STRAIGHT.....



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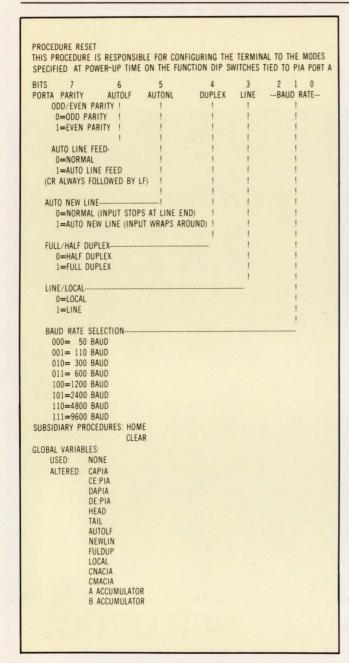


Fig 4 When using a header for a parsing program used with the DIP switch configuration, the possible parameters are limited to 8 bits, and an elaborate software routine is needed to interpret them.

straightforward (as described). With this software in place, the communication between the processor and the device simply becomes a series of reads or writes to the appropriate serial device locations.

The original design only allowed eight userdefinable inputs, since only one DIP switch is used in the terminal. The meaning of the various input conditions is shown in the DIP switch map portion of the program header in Fig 4. Since the single 8-bit input is used for so many functions, parsing the input byte into the appropriate setup parameters requires an extensive piece of code. The problem with this implementation is the extensive software required to make switch operation straightforward in the user's manual.

Replacing the DIP switch with the NOVRAM has several significant advantages. The 256-bit nonvolatile storage leaves adequate room for storing an "image" of all interface circuit registers. Thus, the parsing problem of the DIP switch implementation is eliminated. Even the control registers that do not need to be user-programmable can benefit from this imaging, since they can be changed remotely in the field for hardware or software updates. This method simplifies field upgrading when compared with the usual method of storing these register images in the program store ROM or EPROM.

New images can either be down-loaded remotely or loaded through a diagnostic mode using a directconnect RS-232 interface. Examples of where this capability is beneficial are numerous, and include changing interface protocols, data formats, or other hardware, interface, or networking options.

The use of the device for storing setup parameters also allows a more user-friendly operator interface. Software in the original design includes routines that allow random placement of the cursor or text through the use of a "go to X-Y" routine. It becomes a fairly trivial task to implement a menudriven setup mode. After entering a certain escape sequence, the user is placed in the configuration mode, which presents an English menu.

The return key increments the curse position to the next setup area where the current setting is displayed, and the spacebar key increments that setting through all possible choices. Once the user has set up the parameters for a particular session, depressing the escape key writes the current settings into the RAM section of the NOVRAM. With this operation, the user can set up a temporary configuration without changing the default parameters in the EEPROM section of the NOVRAM. Default settings are changed only when the user executes a certain control sequence (such as control X and then the escape). In some applications, it may be desirable to allow only certain users to change these default parameters before entering a special code.

Replacing the DIP switch with the NOVRAM allows increased design flexibility, as well as reduced manufacturing and testing costs.

Since the X2443 has a much larger capacity than actually needed for this application, the remainder of the nonvolatile storage can hold such data as serial number of the individual unit, revision level, and hardware configuration diagnostic parameters. Otherwise, it can be reserved for future expansion. The Table shows a sample address map for the

NOVRAM Address Map		
<u>Location</u> O	Bit map XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	Interpretation S = Stop Bit Control WW = Word Length BBBB = Baud Rate
1	XXXXXXXPPPETTRD	PPP=Parity Check Controls E=Normal/Echo Mode TT=Transmit Controls R=Receiver Interrupt Enable D=Data Terminal Ready Control
2	XXXXXXXEEEEEEE	E = Emulation Designator (1 of 256)
3	SSSSSSSSSSSSS	S = Serial Number
4	RRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRR	R = Revision Level
5	xxxxxxxxxxxxx	L=Latch data from keyboard on high-to-low or low-to-high
X = Don't Care		

device, with the associated data stored in each of the 16-bit locations. The end results of replacing the DIP switch with the NOVRAM are increased design flexibility, as well as reduced manufacturing and testing costs.

Program storage considerations

The second aspect of improving the terminal design involves the program store for the 6800 microprocessor. The original design uses a 2716 EEPROM since the software requirements for the terminal are not extensive. The feature set of the X2816A EEPROM makes the replacement easier because EEPROMs of the X2816A generation incorporate high voltage generation, address and data latching, and the write-cycle timing circuitry on the memory chip. During read operations, the device functions just like the 2716 EPROM in its use of chip enable (\overline{CE}) and output enable (\overline{OE}) signals. During a write operation, the X2816A latches the addresses on the bus during the high to low transition of the write enable (WE) signal, and then latches the data to be written on the rising edge of the WE signal.

The duration of this signal is not important, since the EEPROM only uses it to initiate the write cycle; the timing for the write operation is generated onchip. The processor needs only to ignore the EEPROM for 10 ms during the write cycle, and the device does the rest. The latched and self-timed nature of the X2816A allows it to be placed in a 16-K SRAM socket and be read and written with the same signals used for the SRAM.

The read operation of the X2816A is the same as that of the 2716 EPROM, so this part of the EEPROM operation is of no concern. The only changes required to the existing circuitry involve the write operation. The first change allows the processor to write to the EEPROM, and the second protects the EEPROM from unwanted write operations during power-up and power-down.

The memory map for the original design was not very full, so only large blocks of the address map

are decoded for each memory device and I/O chip on the bus. The 2716 logically resides at addresses F800 through FFFF since the 6800 reset vectors must be included. The physical decoding for the 2716 includes the address range of F000-FFFF since only the microprocessor's two most significant address lines A15 and A14 are used for the decoding.

Since line A14 is used to drive the \overline{OE} line of the 2716, the EPROM is selected whenever A15 is a logical one. Possible conflict with the system RAM residing at 8000-81FF is avoided by restricting the processor's access to the 2716 in the logical F800-FFFF range. Since the processor can now read and write to the logical address range of the 2716 socket, the \overline{CE} must also be derived from the A15 and A14 address lines. And, since \overline{CE} is active low and the address line is active high, a simple NAND gate will suffice (Fig 5). Luckily, an extra NAND gate in the

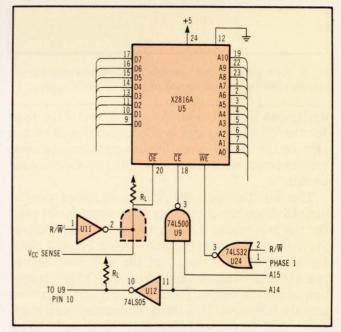


Fig 5 The EEPROM control logic uses the processor's high order address lines to map the device into the proper address range and enable it at the same time.

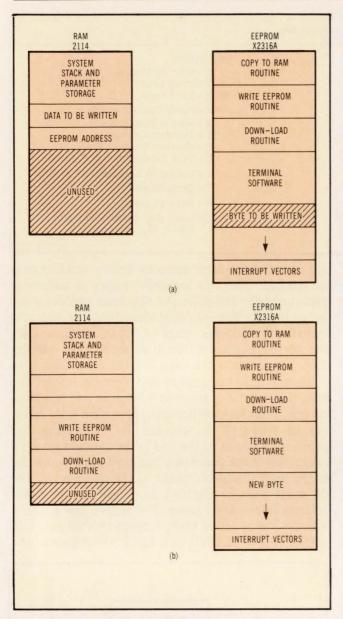


Fig 6 Address maps for updating EEPROM software are kept in EEPROM (a) and copied to RAM (b) when needed.

design can be used as an inverter. The inverter used for the \overline{CE} is no longer needed, and therefore can replace the NAND gate. The inverter on A14 must remain intact since it is used in the 2114 RAM decode circuit.

The \overline{WE} line for the X2816A EEPROM can be derived from the composite RAM write signal used for the 2114 RAMs. This signal is the logical OR or the R/ \overline{W} output from the 6800 and the Phase 1 clock signal. This qualification of the R/ \overline{W} line ensures that the addresses are valid on the high to low transition of the \overline{WE} signal. Therefore, they can be latched into the EEPROM. This ORing connection also guarantees that the data to be written is valid on the rising edge of the composite \overline{WE} signal. The \overline{OE} signal on the EEPROM can simply be driven from the complement of the R/ \overline{W} signal from the processor. This

technique requires that all accesses to the EEPROM be made in the logical address range of F800-FFFF to avoid bus contention with the system RAM.

Discussion of the circuitry needed for the \overline{OE} signal also must include another important issue: ensuring that the chip does not experience an accidental write cycle during power-up or power-down. Even though the chance of \overline{CE} and \overline{WE} going low during power-up or power-down is rather remote, the possibility must be eliminated.

The EEPROM simplifies write protection by including an onchip voltage sensor that monitors the V_{CC} input level and automatically disables writes from occurring when V_{CC} falls below 3 V. Also, a noise filter on the \overline{WE} input prevents a write from being initiated by a low spike. Functional interaction of the control inputs on the chip allows a low level on the \overline{OE} to disable any write operations regardless of the state of the \overline{CE} and \overline{WE} inputs. By holding \overline{OE} low while V_{CC} is between 3 and 4.75 V, inadvertent write cycles are inhibited.

The power supply must be modified to generate an active low signal whenever V_{CC} is below a specific level. This signal disables the write operation during both power-up and power-down. Because this signal is wire-ANDed with the control signal driving the \overline{OE} signal, all writes to the chip are disabled when V_{CC} is below the 4.75-V limit.

Software modification

Once hardware changes have been made, infactory modifications and in-field modifications must be addressed in order to take full advantage of an X2816A. In-factory modifications can be handled in many ways. If the terminal configuration is known at assembly time, the appropriate software can be loaded into the EEPROM through the use of a standard PROM programmer. However, this method does not take full advantage of the features of the in-circuit reprogrammability inherent in the X2816A. A more advanced approach also makes automated board testing easier.

For example, the EEPROM can be initially installed with a diagnostic program for testing the completed terminal board with an automated test system. Once the board has been tested, the tester controls the 6800 processor by holding it in a quiescent state such as reset or halt. The tester then assumes control over the terminal bus and writes the actual terminal software into the EEPROM. This greatly reduces the overhead required to manufacture a variety of different configurations or "models" on a single assembly line. In-line programming also allows for the verification of the EEPROM write operation and control circuitry.

The real advantages of the EEPROM surface when it comes to modifying software in the field. In this case, the terminal is placed in a down-load mode,

and the software revision is loaded through the RS-232 interface, either from a service "box" or remotely via a modem. The X2816A allows the terminals in the field to be called over phone lines for loading new operating software, thereby greatly reducing the cost and impact of a software update.

Although full-featured EEPROMs such as the X2816A simplify this task significantly, there remains one software issue to be resolved. While the EEPROM is performing its internal write cycle, it is unavailable for further writes or reads. For example, the processor, executing out of a program stored in the EEPROM, might perform a write cycle to the chip and then fetch the next instruction. Since the X2816A is occupied with its internal write cycle, the next instruction fetch will yield a high impedance bus. The processor will take this data as its next instruction and enter the "catch fire and die" mode of operation.

To avoid this situation, a very compact routine fetches the byte to be written into the EEPROM from a given location, writes the byte into the EEPROM, and then enters a timing loop to wait the 10-ms period required to complete the write. Since the RS-232 interface supports full handshaking, there is no chance of overrun from the down-loaded data. This routine is initially loaded into the EEPROM, but it is never executed from this device. Instead, another

"copy to RAM" routine copies the routine from EEPROM into RAM, from which it is executed.

Since the terminal has 1 Kbyte of RAM capacity. there is ample room for storing such a routine during the EEPROM write cycle. Fig 6 shows address maps for both the EEPROM (a) and the RAM (b) prior to and during the execution of the EEPROM write routine. This method works especially well with the 6800 since its architecture is that of a von Neumann machine, and can therefore execute program segments out of the memory space reserved for RAM

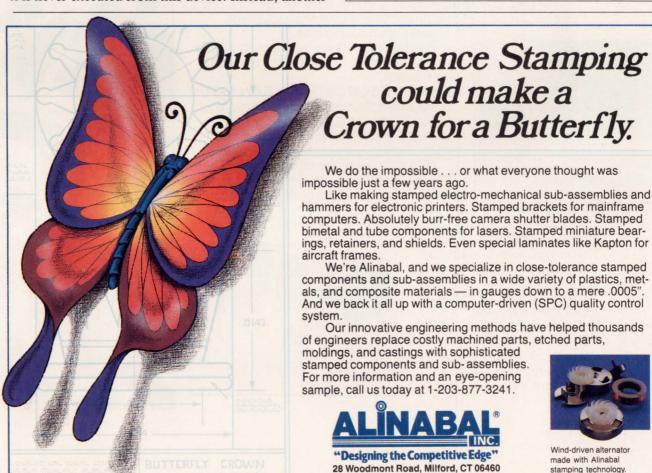
In-field terminal upgradeability has two important benefits. If the terminal software is upgraded or revised after the unit is sold, the new software can be added to the existing units in the field at minimal cost. This method also eases the addition of optional hardware in the field, since the new software supporting the hardware option can be down-loaded instead of replacing the terminal EPROM.

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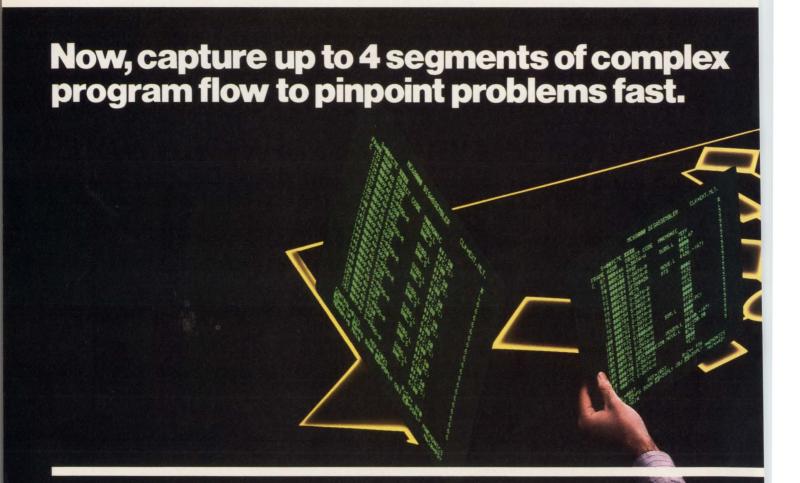
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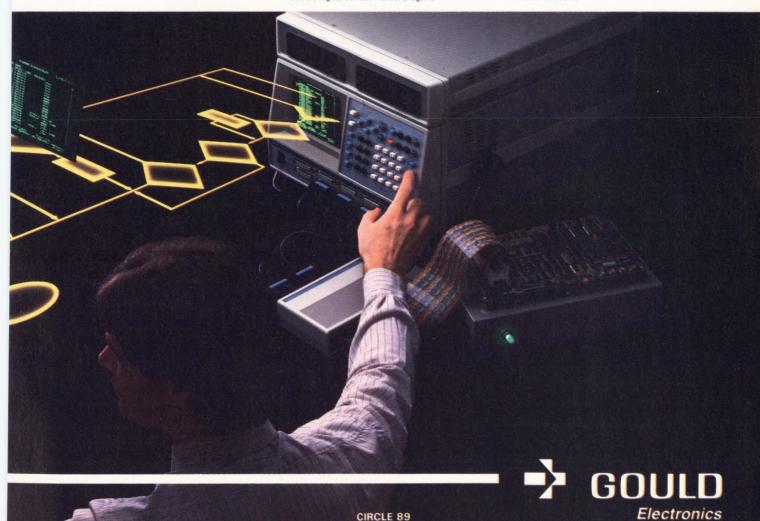
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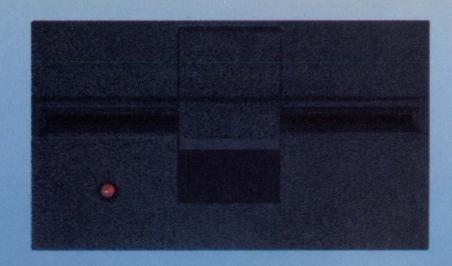




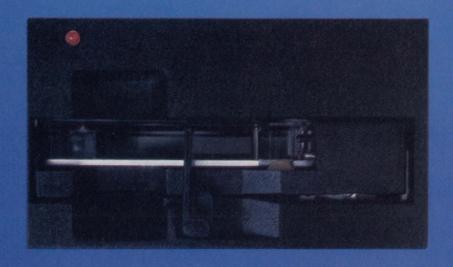
The K105-D gives you two levels of HELP at the touch of a button. First, step-by-step operating instructions that appear along the bottom of the analyzer screen. Second, a menu that allows you to select more detailed "help" should you need it.

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SIMULATOR DRIVES DIGITAL DESIGNS

Designing complex circuitry requires sophisticated design aids at all levels. Logic simulation, from functional specs to fault analysis, manages and automates the process, freeing the designer for more creative tasks.

by Mahesh Doshi, Rick Sullivan, and Donald Schuler

Both the expanding use of increasingly complex LSI and VLSI digital circuits and the addition of semicustom LSI to PC boards have put a strain on design tools and techniques. Not surprisingly, hardware engineers have turned to decomposition techniques, starting with a high level design and moving through successive stages of refinement to more detailed designs. Techniques such as these have been used for some time to handle complexity in software systems. Now, they are used more extensively in hardware design.

Logic simulation is essential to the design of LSI and VLSI circuits. It detects logic and timing errors, and evaluates test programs. The need for logic

Mahesh Doshi is manager of electrical design analysis tools at Prime Computer Inc, Old Connecticut Path, Framingham, MA, 01701, where he manages the development of electrical design analysis tools in electrical CAD. He holds an MS in electrical engineering from the University of Wisconsin-Madison.

Rick Sullivan is a principal software engineer at Prime Computer. Mr Sullivan holds a BS in electrical engineering from Tufts University and an MS in electrical engineering from the University of Illinois, Urbana-Champaign.

Donald Schuler is a senior technical consultant and manager of advance CAD development at Prime Computer. He holds a BS in electrical engineering from Clarkson College. simulation in PC board design is growing due to its increased use of faster logic circuits and semicustom LSI devices that are more difficult to breadboard accurately. The problem is that most logic simulators do not support modern design techniques.

A hierarchical, event-driven, and multilevel interactive simulator—THEMISTM Logic Simulator—performs simulation at the switch, logic, register transfer, functional, and behavioral description levels. It supports fault simulation, and works with the electronic design management system (EDMS). THEMIS handles LSI, VLSI, and PC board designs from functional specification to logic analysis; from logic analysis to timing analysis; and from timing analysis to fault analysis. It runs simulations of up to one million equivalent gates.

Unlike traditional batch simulators, this simulator provides an interactive debugging environment that allows changes in signal and storage values, test patterns, and print lists during simulation. It can establish breakpoints on a variety of circuit conditions, and provides an efficient checkpoint and restart facility. Delay models can change to unit, nominal, minimum, and/or maximum values at any time, without recompilation of the circuit description. Checking of both the functional and the timing characteristics is available.

Hierarchical design support

Many electronics companies refine a functional specification to a functional block diagram or to a register transfer level (RTL) description. The diagram or RTL description is further refined to a gate or transistor level description, and eventually, to a layout description. Error detection and correction occur early in the evaluation and verfication process. Fig 1 illustrates the simulator's support for the hardware

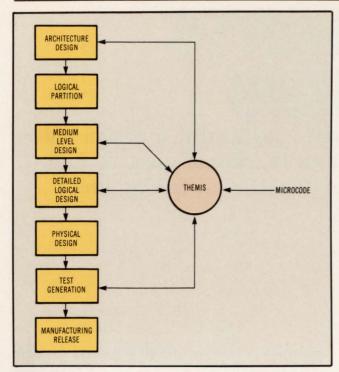


Fig 1 Simulators can be used for design verification from architectural design to detailed design, as well as for generating of test patterns to be used in automatic test equipment.

design process. As shown, the simulator verifies each refinement of the design process and compares it with the original functional specification. The functional specification, written in the register transfer language, also serves as documentation.

THEMIS can simulate a large design at any description level. It can also handle multiple levels of description simultaneously, and accurately simulate both timing and functional characteristics. Fig 2 shows three representations of the same circuit, simulated simultaneously. Each of the three circuits is a 16-bit two's complement adder. One is modeled at the RTL level, another at the gate level, and the third at the transistor level. There is no restriction on the mix of modeling techniques that can be used to describe a circuit.

Circuit models at any level interconnect to form new models within the simulator. At the lower levels, THEMIS is a 10-state simulator (driven, resistive, and capacitive for 0, 1, and X plus high impedance) with built-in models for bidirectional MOS transmission gates, pull-up/down resistors, delay lines, and timing blocks. At the higher levels, it is a four-state simulator (0, 1, X, and high impedence). In all cases, the software handles bused outputs and tri-state logic automatically.

Combined, THEMIS and EDMS present and accept design data to and from a single data base for logic design, analysis, and physical design. This not only reduces the expense of encoding a large circuit into two data bases, but reduces the potential for making

errors as well. The designer encodes the system to be simulated using one or more of the modeling techniques. Each model compiles interactively for online error correction. These models then link with the necessary component models from either a local library or from the permanent libraries. The system is ready for the simulation after the linking process sets the initial condition.

Encoding the system for simulation

Accurate models of elements and systems can be simulated at different levels of detail. Boolean equations, the THEMIS architectural design language (TAD), PL/1, Fortran, C subroutines, and special built-in primitives can all be used to create models. Any previously defined models can be wired together into a new circuit by using the network modeling language. In this way, a network can be used as a model in a network at a higher design level.

Boolean primitives can have up to eight inputs and one output. The output is either two-state (0, 1) or tri-state (0, 1, Z). If an element cannot be modeled as a single Boolean, it is modeled as a network or a function. The Boolean definition itself consists of delay variables, equations, and initialization commands. A special table lookup technique makes the Boolean primitive evaluation very efficient.

Another essential feature in hierarchical design support is TAD, a nonprocedural architectural design language. With TAD, the designer encodes the behavorial description of any element. Elements include gates, flipflops, ALU, register files, stacks,

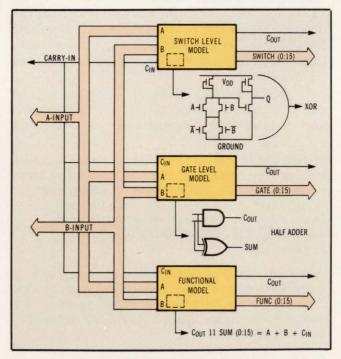
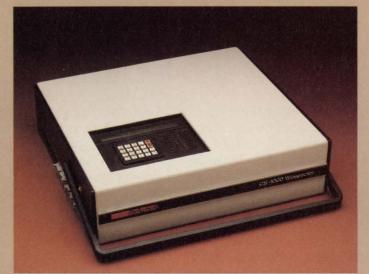


Fig 2 This example of a 16-bit adder circuit shows mixmode simulation. Three different levels of the same design are simulated in the same session.

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and microprocessors. Statements that reference and manipulate registers, RAMs, ROMs, pins, and clocks describe component behavior. The component's delay may be a function of both input and output states. Logical, arithmetic, relational, and sequencing operators are included in TAD (see the Table). Sequencing operators allow descriptions of parallel and sequential hardware.

To control the code execution, TAD supports conditional statements, such as If-Then-Else and Decode-Case. Designers can specify internal multiphase clocks with TAD, as well as define new operators. TAD supplements, but does not replace, Boolean models. While Boolean models simulate faster, TAD models include a larger class of operations and are easier to write.

Standard programming languages (eg, Fortran, C, PL/1, and Pascal) are used to create behavioral models. These models can read and modify the values of registers, RAMs, ROMs, and pins using special subroutine calls and standard features of the programming language. Registers, RAMs, ROMs, and pins are declared for language models the same way they are declared for TAD models. Communication with other models occurs through nets and pins.

Network models interconnect existing Boolean, functional, language, and network models, along

with built-in primitives, to form new models. There is no limit to the network model nesting. Moreover, any simulated circuit can automatically turn into a network model. Network models overwrite lower level delay definition and initial values.

To move from the model compiler to the model simulator, the designer issues the link command. The linker resolves undefined references by searching libraries that are in a designer-specified order. The linker generates a detailed statistical report on system usage and transfers control to the simulation routines. THEMIS allows designers to analyze and modify the simulation of a circuit while the circuit is simulating, rather than requiring all analysis to be done as a postprocessing step.

As an example, the breakpoint command allows users to stop simulation on a variety of circuit conditions. These include signal, data path, register or memory changing to a particular value, occurrences of positive and negative edges on signals, and increases and decreases in data path, register, and memory values. Multiple breakpoint commands can be specified, displayed, and edited at any time. An action list, a command set that executes automatically whenever a specified event occurs, can be associated with any breakpoint. Action lists are extremely powerful in debugging logic. Like breakpoints, they

THEMIS Architectural Design Operators				
Operator	Symbol	Precedence Level	Typical Syntax	Result, assuming A and B are of dimension N, and K is an integer
Concatenation	1	9	А∥В	All elements of A and B in a set
*Complement	~,	8	~A	Bit-by-bit complement of A
Negate	-	8	-A	Negate A
Reduction		7	о А	A1 o A2 o A3 Where o is any operator and to or below
Add	+	5	A + B	Arithmetic sum of A and B
Subtract	-	5	A - B	Arithmetic difference of A and B
Less than	<	4	A < B	A smaller than B
Greater than	>		B > A	B larger than A
Equal	=	4	A = B	A and B are same
Less than or Equal to	<=	4	A <= B	A is less than or equal to B
Greater than or Equal to	>=	4	B >= A	B is greater than or equal to A.
Not equal	~=	4	A ~= B	True is A and B are different numbers
*AND	&	3	A & B	Bit-by-bit logical product
*Exclusive—or	#	2	A # B	Bit-by-bit exclusive—or
* OR * Also available in Boolean equa	tions	1	AIB	Bit-by-bit logical sum

can be displayed and edited at any point during the process. Any command used during simulation can also be in an action list.

At any time, the interactive simulator can display and change any signal value, delay value, or test pattern. Interactive features include the ability to display signal values in waveform format and receive input either from key entry or from a file. Input from a file is especially powerful because any file can be edited from within the simulator using a standard line editor.

Providing traditional logic analyzer features for electronic circuit debugging, the simulator triggers activities, displays values, and probes the circuit. In addition, it provides debugging tools unavailable in the lab to modify delays, fault circuit elements, and stop simulation when some condition is detected.

One system integrates analyses

The simulator combines logic, timing, and fault analyses in one model. For logic analysis, it becomes a four- to nine-state simulator with languages for modeling the circuits' functional characteristics. For timing analysis, it provides flexible ways to add timing characteristics to functional models. Most outputs have two to six separate delay values: rise and fall for two-state; rise, fall, $Z \rightarrow 0$, $Z \rightarrow 1$, $0 \rightarrow Z$, and $1 \rightarrow Z$ for tri-state outputs. TAD models output delay relative to edges on clocks and as a function of input state. Additional built-in models check for stable data relative to an edge or a pulse.

All delays have minimum, nominal, and maximum values, and can be a function of the capacitive load driven by the output drivers. Races and hazards are automatically detected and reported. Concurrent fault simulation provides an accurate, efficient method for measuring fault coverage using the same models, including timing characteristics. This concurrent fault simulation works with any modeling or evaluation technique and is 10 to 30 times faster than parallel fault simulation.

Designers can either supply test patterns for the system or generate them using built-in functions. The test pattern specification can be defined for a specific time or incremental time. During the simulation, test patterns can be applied or changed. In-circuit events or external control signals can trigger the application of test patterns. A list of built-in functions and a repeat facility reduce the work necessary to generate test patterns.

Simulation can progress to a specific time, for a number of incremental time steps, until a breakpoint is encountered, or until there is no activity in the system. Events such as memory writes, signal or data path changes, and register increments can trigger breakpoints. The simulation can also be interrupted asynchronously (by pressing the break key) and continued without losing any circuit events. Users can

change test patterns and resimulate the circuit quickly. Restart points can be saved from session to session, and debugging runs can continue from day to day without recompilation.

The print command consists of options to control and tailor the output to the designer's needs. The output can be in horizontal or vertical format. Signals, pins, registers, memory elements, and data paths can be printed on octal, hex, binary, decimal, and ASCII base. In combination with breakpoint action lists, this command provides the facility to trigger output by circuit activity.

The trace command monitors all signal, register, and memory element activity. Values are printed as the changes are propagated through the monitored variables. The trace report goes to the terminal, a fixed location on the terminal screen, or to output files. Independently formatted and controlled output proceeds to the terminal or any number of output files. Hazard reporting of output spikes or busing conflicts can be enabled or disabled at any time.

Logic analyzer emulation is an important part of the user interface. The designer inserts virtual probes into the circuit and specifies the sampling clock (incircuit or external), triggering, and arming criteria. After the data is collected from the probes, it can be displayed in a state table or a graphical waveform. This simulator allows an arbitrary number of virtual logic analyzers.

Since it is impossible to foresee the needs of all potential users, the simulator includes an abbreviation facility that enables designers to tailor the user interface. The user can abbreviate commands and sequences of commands to almost any short string of characters. The same facility allows sequences of commands to be bound to terminal function keys. Also, an input facility allows the input stream to be directed from the terminal to a file. A long series of commands, such as the circuit initialization sequence, can be stored in a file to be read in interactively.

As the complexity of systems increases, so must the sophistication of the tools used to design them. A simulator must support the design process from the initial, conceptual phase through the detailed stages of implementation. It must allow devices to be modeled before their implementations are known, and it must provide a natural, interactive environment in which the logic can be debugged. A simulator, such as THEMIS, which satisfies these requirements can greatly reduce design time and cost, and lead to higher quality, more reliable products.

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CIRCLE 94



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Personal computer benefits from 80286, networking, and software

Compatible with most IBM PC hardware and software, the 80286-based PC AT is available in two versions. The base model provides 256 Kbytes of memory, flexible disk drive, fixed-disk and drive adapter, and seven 1/0 expansion slots. The enhanced version has 512 Kbytes of memory, flexible disk drive, 20-Mbyte fixed-disk drive, fixed-disk and diskette adapter, serial/parallel adapter, and six I/O expansion slots. The AT requires a video display adapter and display output device.

The system unit holds the 80286 and provides a 6.0-MHz clock speed with 24-bit address and 16-bit data path. The internal 64-Kbyte ROM has 150-ns access time and 355-ns cycle time. The keyboard has 84 keys with the thoughtful addition of caps lock, number lock, and scroll lock indicators.

The diskette drive is a half-height 5½-in. double-sided drive with 1.2 Mbytes of storage capacity. Standard in both AT models, a second drive of this type can be installed in the system unit. Both drives use the same fixed-disk and diskette drive adapter. The high capacity drive can read disks in 160/180-Kbyte, 320/360-Kbyte, and 1.2-Mbyte mode. Technical specs include 512 bytes/sector, 15 sectors/track, and 96 tracks/in. In the 96-track/in. mode, average access time is 94 ms. It supports 300- and 500-kbit/s data transfer rates.

In the base model, the 20-Mbyte fixed-disk drive can be the first or second fixed-drive; in the enhanced model it is the second drive. Customer installable, the 20 Mbytes of storage has a 40-ms average access time with 512 bytes/sector, 17 sectors/track, and turns at 3573 rpm. Transfer rate is 5 Mbits/s.

Memory options for the AT range from 256- to 512-Kbyte increment expansions. The 256-Kbyte memory module kit allows the base model user to upgrade base memory from 256 to 512 Kbytes. It consists of 18 dynamic RAM modules that plug into existing sockets on the system board. The DRAMS are organized as 128-K x 1-bit, with 16-bit data paths.

With the 128-Kbyte memory expansion option, the base memory of both models expands from 512 to 640 Kbytes. For users requiring support for the 512- to



640-Kbyte address space, the AT is compatible with PCs, XTs, and IBM portables. Performance characteristics are identical to the 256-Kbyte memory module kit.

The 512-Kbyte expansion option allows for 512-Kbyte increment additions to expand above 1 Mbyte of base memory. Expansion slots hold up to five cards for a total of 3 Mbytes of primary storage.

Available operating systems include DOS 3.0, DOS 3.1, and Xenix. The DOS 3.0 configures itself to support six international keyboard versions and provides an enhanced screen dump utility program. A virtual disk feature allows the use of extended memory (above 1 Mbyte). The operating system uses approximately 36 Kbytes of RAM. The DOS 3.1 version provides all DOS 3.0 functions, plus enhancements that support IBM PC Network hardware and software.

The company also offers Xenix (by Microsoft), which is derived from Unix. It supports single- and multi-user configurations and can run several programs at one time. It supports large memories up to 3 Mbytes via the 80286. Device support includes CPUs, three drives, CRTs, and printers. Optional features include a software development package and a text formatting system.

Topview software is also available. With Topview users can operate several different programs concurrently, switch from one task to another, or view data from several programs using windows—all on a single display screen. A Toolkit includes information on accessing functions from application programs, supporting mouse devices, and creating and using windows.

The lowcost broadband PC Network uses standard 75-Ω CATV coaxial and connection hardware. The 2-Mbit carrier sense multiple access/collision detection (CSMA/CD) network consists of an adapter, a translation unit, and cabling hardware. The network adapter is a cord that connects the PC, XT, AT, and portables to the IBM PC network. It contains the network BIOS in ROM. BIOS provides the basis for all network program controls. The translator unit provides broadband frequency translation, from the return channel to the forward channel. for a passive network. A connector assembly attaches eight PC stations within a 200-ft radius.

Price for the base model is \$3995 and the enhanced model is \$5795. Hardware options range in price from \$350 to \$1595, with network hardware from \$59 to \$695. In software, DOS 3.0 costs \$65, DOS 3.1 is \$65, Xenix is \$395, and Topview software is priced at \$149. IBM Corp, Entry Systems Div, PO Box 1328, Boca Raton, FL 33432.

—M.B. Circle 260

Dual-processor design soups up supermicro system

The MC-500DP series gives multiple job users additional computing power through dual processors. The Unix-based realtime system can connect a second CPU, with associated memory, via multiple high bandwidth buses. This design offers performance superior to that of single-processor architectures.

Incorporating single-processor features, the system includes an integrated array processor, multiple independent graphics processors, 8-MIPS data acquisition and control processors, and an Ethernet communication processor. The dual processors can support disk sizes from 50 Mbytes to 474 Mbytes, floppy disks, quarter-inch cartridges, and halfinch magnetic tapes.

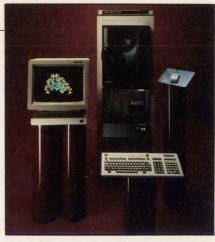
The unit uses an asymmetric (master/slave) system based on dual-processor extensions to the realtime Unix operating system. The software supports menus, window management, graphics, and

several languages—including Fortran, C, and Pascal.

The system operates in two modes. It will either automatically distribute the computing loads between CPUs or allow the user to define which tasks each CPU will run. Each CPU connects to its associated memory by separate memory interconnect (MI) buses. Communication occurs via an enhanced Multibus.

Unlike multiple CPU architectures, memory access is not uniform between the two MIs. Operating system coordination of separate cache address translation buffers minimizes the asymmetry effect for all but the most time-critical processes. For realtime maximum performance applications, the user can choose memory resource allocation options to ensure that pages of a process are on the same MI as the CPU executing the code.

Two floating point processors, one on each MI, provide a 560,000 Whetstone



benchmark performance. A CPU can access only the FPP that is on the same MI. Both master and slave CPUs can support an FPP.

The series consists of seven systems: three workstations, one tabletop, and three cabinet configurations. The lowest priced system is the tabletop version at \$36,900. It includes the two CPUs, 2 Mbytes of ECC memory, a 50-Mbyte disk, a 1-Mbyte 5½-in. floppy, a 15-slot backplane, terminal, 5 serial lines, and software. **Masscomp**, One Technology Park, Westford, MA 01886. —*M.B.* Circle 261

Workstations unite 32-bit processing with graphics



The 6000 family consists of two software compatible groups—the 6100 and 6200 workstation series. Both use National Semiconductor's NS32000 micros. These devices feature a mainframe-like architecture and an instruction set designed for efficient execution of high level language programs.

Members of the 6100 series employ the NS32016, a 32-bit processor with an external 16-bit bus. Three basic products are included in the series—the 6110 instru-

ment controller, and the 6120 and 6130 graphics workstations. The 6110 instrument controller runs a realtime operating system (RTOS) and can execute object code programs generated in Basic, C, Fortran, or Pascal. It features a GPIB port including pass control with optional DMA. Standard equipment includes 256 Kbytes of memory, dual RS-232 ports, and a 360-Kbyte flexible disk.

The 6120 workstation uses the proposed ANSI Basic

providing graphics functions, extended 1/0, and interactive editing. Standard is a keyboard and mouse, 1 Mbyte of memory, FPP, a 360-Kbyte, 51/4-in. flexible disk, and a 10-Mbyte Winchester.

Designed for data analysis, software development, and CAE applications, the 6130 is similar to the 6120, but also includes an enhanced version of Unix. A 20-Mbyte, 51/4-in. Winchester disk, a 360-Kbyte flexible disk, 1 Mbyte of memory, and an FPP are all standard.

The 6200 series is based on the NS32032 with a 32-bit data bus. It is expandable through the Global bus: a standardized, high speed (40-Mbyte/s) interface that connects the computing systems. The two basic products in this series are the 6210 and 6212 graphics workstations. The 6210 is suitable for custom VLSI and gate array design. It can also be configured as a file and a peripheral server for workstations on a LAN.

The 6212 workstation has dual 32-bit application processors, and large disk and memory. It is optimized for concurrent execution of compute- and interactive-intensive tasks such as editing designs and circuit simulation.

For configuration flexibility, the family provides industry standard interfacing options. These include RS-232, RS-422, IEEE 802.3 Ethernet, Centronics, Multibus, SCS1, and IEEE 488 interfaces. The 6110 controller is priced at \$4995. The graphics workstations range in price from \$7995 to \$35,950. **Tektronix**, **Inc**, PO Box 1000, Wilsonville, OR 97077. —*M.B.*

Circle 262

Graphics software makes dynamic data stream display possible

DataViews graphics software enables dynamic data display in real time. Users can compose, edit, and display numerical data without programming. DataViews can be used for instrumentation applications, in lieu of analog displays. It can take temperature, rpms, pressure, and oil flow in an engine, and display this data as a simulated instrument panel on a color monitor.

This system accepts data from a communication link to a physical process, from a data base or file, from programs generating information, and directly from a keyboard. Written in C, this package runs on Unix systems. It can be used on 16- and 32-bit micros, minis, and superminis. Minimum main memory of 512 Kbytes is required.

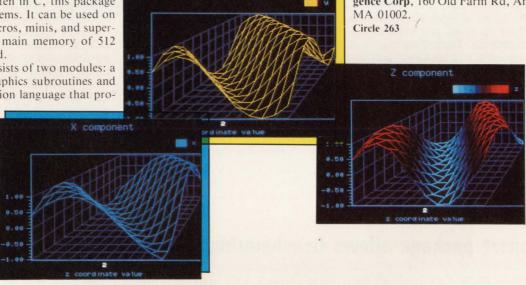
DataViews consists of two modules: a full library of graphics subroutines and a menu specification language that provides a high level interface to subroutines. System integrators can embed all or part of this general-purpose package, creating application specific display formats faster. Also, users can modify DataViews to create their own formats. The menu specification language module allows alteration of existing menus.

Subroutines offer over 40 display formats including line graphs, dials, bar charts, surface plots, and flow fields. Multiple screens can be constructed with

Y component

a variety of viewports and formats. In an aerospace application, for example, windows show each dimension of net velocity as data is generated on a display of simulated vector fields. (A network of supercomputers, minis, and color graphics workstations was used in the 3-D simulation pictured here.)

Instrumentation, automatic test equipment and process controls, as well as engineering, science, and simulation are among DataViews uses. In quantities over 25, the product is priced at \$1000 for a one- or two-user system. Visual Intelligence Corp, 160 Old Farm Rd, Amherst, -J, V



Ease of system installation highlights system clock chip

Chip suppliers, off chasing the 10-cent wristwatch IC market, seem to have ignored general-purpose timing circuits for the computer industry. But system designers will find that the IMC717OB timekeeping IC, intended specifically for operation on an 8-bit data bus, furnishes excellent accuracy (which, depending on the crystal frequency chosen, can reach 0.10 ppm), and provides a system access time of 250 ns.

This realtime clock uses the CMOS process and an onchip power-down detector. Thus, a simple battery on the clock board prevents the loss of timing data during a power failure or system downtime. Timing information in eight internal registers provides time (in 12- or 24-hour formats) to the 100th of a second, month (in numeric format), date, day of week (also in numeric format), and a two-digit year. An external crystal drives the internal oscillator, with optional crystal frequencies available. Designers can select 32.768 kHz, 1.048576 MHz, 2.097152 MHz, or 4.194304 MHz.

An address latch enable input allows interfacing to microprocessors that multiplex the address/data bus. Clock data is latched each time the 1/100ths-second

counter is accessed. This prevents rollover during the read cycle, and provides a stable time value. All output buffers are then latched until the next access of the 1/100ths-second buffer, at which time they are all updated.

The ICs use the now standard CMOS inverter (Pierce) oscillator and require two external capacitors (one can be trimmed) with the crystal. Configured as a 24-pin DIP, the ICM7170B realtime clock is priced at \$9.50 in quantities of 100 per month. GE Intersil, Inc, 10710 N Tantau, Cupertino, CA 95014. -B.F.Circle 264

Seven ISO/OSI layers covered by powerful LAN boards

Boards in the NP series are second-generation intelligent Ethernet processors that connect to established buses. These boards can support all seven layers of the ISO/OSI communication protocol model. By off-loading the host's protocol processing activity, NP units provide improved CPU performance and high throughput.

Designers working with Unibus, Q-bus, and Multibus systems can use the NP100, NP200, and NP300 processors, respectively. These allow connection to an Ethernet/IEEE 802.3 local area network (LAN). Software provides a high level interface to the host environment and cuts the time needed to develop a LAN application.

The Xerox Network Systems/Internet Transport Protocols (XNS/ITP) package is offered for Unibus hosts running





VAX/VMS or RSK-11M Plus, Q-bus hosts running RSX-11M/M Plus, and Multibus machines running Unix System v. The XNS/ITP package offers high bandwidth communications and a full set of transport level services. The Internet Protocol/ Transmission Control Protocol (IP/TCP) implementation is also available for Unibus hosts running 4.2 BDS Unix and Multibus hosts using System v. Each network processor features a dedicated

80186 microprocessor, up to 256 Kbytes of RAM, 16 Kbytes of EPROM, an intelligent DMA interface, and an 82586 Ethernet LAN interface. Data link diagnostic functions are onboard.

For system integrators working on specialized transport or application level protocols, a software development toolkit is available that includes an operating

system executive with integrated device drivers to the Ethernet and host bus. The network processors are compatible with Ethernode link level controllers. The Unibus network processor with XNS/ITP or IP/TCP is priced at \$4290. The Q-bus version (with XNS/ITP) and the Multibus net processor (with XNS/ITP or IP/TCP) are priced at \$2690. Interlan, Inc., 3 Lyberty Way, Westford, MA 01886. Circle 265

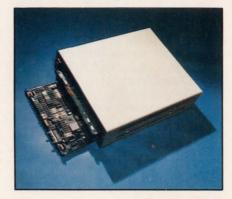
Support package allows benchmarking and debugging

First-time users of the MC68020 MPU can evaluate the chip and start code development with the Benchmark 20 system package. This 32-bit development package includes hardware and firmware for benchmark testing, debugging, and paged memory management. The Benchmark 20 is VERSAmodule-based, and can be configured with existing VERSAmodule boards to provide user target systems. A VME/IO or EXORmacs host system can assemble, compile, and down-load software for execution the Benchmark 20.

The Benchmark 20 includes two VERSAbus compatible boards: the VM04 32-bit monoboard microcomputer and the VM13 1-Mbyte memory board. Also included is a 4-slot VERSAmodule chassis with a power supply, and an EPROMresident debug monitor named 020bug. The boards and 020bug can be purchased separately.

The VM04 uses the MC68020 at a fixed clock rate of 16.67 MHz. It provides a socket for optional use of the MC68881 floating point coprocessor, which improves speed in arithmetic operations. The VM04 also has an onboard cache, memory management, dual multiprotocol serial I/O ports, and a high speed RAMbus interface.

Designed for use with VERSAbus and RAMbus, the VM13 is a dual-ported, 1-Mbyte dynamic RAM board with parity. The RAMbus interface is specifically designed to enhance VM04 performance, and it allows concurrent DMA transfers on VERSAbus, with RAMbus transfers between the VM04 and VM13. The VM13 has parity generation and error detection circuitry that works with con-

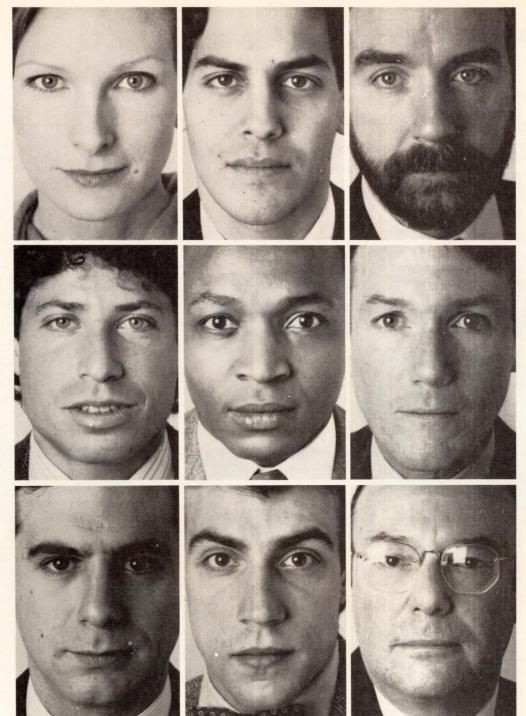


trol and status registers for error detection and memory diagnostics. The VM13 uses high density 64-K x 1-bit DRAM

In the Benchmark 20 system, 020bug is resident on the VM04. It allows the user to access any MC68020 internal register, VM04 status/control bits, timer for benchmarking applications, and any memory-mapped VERSAbus or RAMbus resource. Additional features include two types of power-up, self-test diagnostics, and software drivers to accommodate both serial ports, an operating system bootstrap command, and breakpointing and tracing capabilities.

A cross macro assembler for 020 code, a C language cross compiler, and a cross linker are now under development. An MC68020 cross macro assembler is available. As a single unit, the Benchmark 20 system is priced at \$14,995. The VM04 can be obtained separately for \$6,855 and the VM13 for \$4,200. The 020bug package can be purchased for installation on the VM04 for \$500. Motorola Microsystems, PO Box 20912, Phoenix, AZ 85036.

Circle 266 -R.G.



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Speech synthesizers incorporate complete words

Model CE 4510-2 speech units synthesize complete words, instead of phonemes, to produce natural speech. Mounted on 4.5x 6.5-in. plug-in cards, the CE 4510-2 is fully STD bus compatible. Each unit combines a standard vocabulary ROM set with 144 program selectable words and signals.

A custom ROM set with 126 selectable telecommunication words, prefixes, and suffixes is also onboard. Unit price is \$349. Conway Engineering, Inc., PO Box 6625, Oakland, CA 94603.

Circle 267

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This IBM format-compatible 9-track tape drive weighs 60% less than any equivalent system available. And occupies 25% less space. (Save up to \$200 on freight costs alone!). It's simple and reliable. Fewer moving parts. No automatic threading failures. No noisy blower. And look at all you get:

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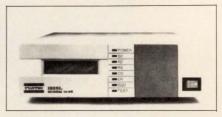
*OEM quantities, 1600 bpi PE format, domestic prices.

Phoenix: ASR-NM, (602) 949-8293 · Los Angeles: Gemini Associates, (213) 594-9618 · Rochester, NY: Ossman Group, (716) 424-4460 · San Jose: Reptek - No. Calif., (408) 947-0622 · Chicago: SEA, Inc., (317) 846-2591 · Washington, C.C.: Scott Data Corp., (703) 765-7901 · Orlando: Southeast Data Prod., (305) 788-3666 · Union, NJ: Stearns Associates, (201) 686-2980 · Boston: Sturdy Corp., (617) 235-2330 · Dayton: Swenson Associates, (513) 866-3233 · Dallas: Thorson Company, (214) 233-5744

Fiber optic link offers range of 425 ft

Data Channel is a fiber optic transmission link that achieves a useful transmission range of 425 ft without a repeater. It is field installable without additional tools, and plugs into an RS-232-C port. Using this device, electrical data is transformed into a light signal and transmitted, then reconverted into an electrical signal. Data Channel contains one LED transmitter and one detector amplifier. The light guide is a twin-light path that permits two-way, side-by-side transmission. Thomas & Betts Corp, Optoelectronic Products Div, 920 Route 202, Raritan, NJ 08869. Circle 268

High speed standalone modem transmits up to 14.4 kbits/s



The F1925L standalone modem exhibits 14.4-kbit/s synchronous transmission over unconditioned lines. It has an automatic adaptive equalizer that optimizes performance by continuously adjusting to line characteristics. In full compliance with CCITT V.29, fallback speeds of 4800, 7200, and 9600 bits/s can also be selected. This compact unit has a 32-char LCD and a built-in 6-channel time division multiplexer. The F1925L lists for \$6500. Fujitsu America, Inc, 1945 Gallows Rd, Vienna, VA 22180.

Circle 269

System links micros to mainframes and offers powerful menus

Consisting of software and a plug-in expansion board that fits IBM and IBMcompatible PCs, the PCI-Link also has a coaxial cable that connects from the PC expansion slot to an IBM cluster controller. Software features allow cursor movements to initiate 3278 functions. Macros of up to 4000 characters let the user set common sequences. Running PC-DOS, or MS-DOS version 2.0 (or later), is required, as is a 256-Kbyte main memory. Price is \$995. Protocol Computers, Inc, 6150 Canoga Ave, Woodland Hills, CA 91367. Circle 270

Local network gains X.25 interface

The Net/One LAN can connect to a public data network via the X.25 Gateway. This interface supports as many as 32 virtual circuits with an X.25 link speed of up to 64 kbits/s. Physical interface occurs via RS-232-C, V.35, or RS-449 connections. The Net/One X.25 Gateway is certified for use with the Telenet public data network, with other certifications anticipated. The X.25 Gateway is priced at \$10,090, plus \$2500 per net for X.25 software. Ungermann-Bass, Inc, 2560 Mission College Blvd, Santa Clara, CA 95050. Circle 271

Frontend Ethernet processing enhances Unix-based system

An Ethernet LAN package that features frontend processing and the transmission control protocol/internet protocol (TCP/IP) is now available for the Samson computer system. This adaptation of Ethernet version 1.0 runs at up to 10 Mbits/s and uses frontend Ethernet

processing that off-loads the system CPU for improved performance. Up to 60 Kbytes are available for packet buffering. Presentation and session layers are included in the software package. Price is set at less than \$200 per user, based on a fully implemented Samson system. SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Circle 272

Eight-line communication chip links peripherals to 16/32-bit devices

A communication chip, called the OCTART, combines eight asynchronous serial lines. It connects terminals, printers, and other serial devices to 16and 32-bit microcomputers, terminal concentrators, and multiplexers. This hybrid MOS chip is packaged in a 68-pin surfacemount, JEDEC standard carrier. It is functionally equivalent to eight UARTS. Integral, independent baud rate generators for each line support data rates from

50 to 19,200 bits/s. Character transmission/reception monitoring methods are designer selectable. The OCTART chips cost \$123 in 1000-unit quantities. Digital Equipment Corp, 10 Main St, Maynard, MA 01754.

Circle 273

Intelligent comm controller operates in Multibus systems

The TIL LPC458 supports 12 serial I/O ports and 16 lines of parallel I/O with handshaking. The board conforms to the IEEE 796 standard, operates as a slave with 24-bit addressing and a 16-bit data bus; and generates 8 nonvectored interrupts. To a Multibus system, the board appears as 64 Kbytes of memory. Hardware features include a 68B09, operating at 1.8432 MHz; 64 Kbytes of CMOS SRAM, dual-ported between the 6809 and the Multibus; and a 6522 VIA for parallel communication and internal timers. TIL Systems, Ltd, 60 Yonge St, Toronto, Ontario M5E 1H5.

Circle 274

1 BAINING

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CIRCLE 100

SYSTEM COMPONENTS/ DATA GOMMUNICATIONS

Expandable 300- and 1200-baud modem features clock/calendar

The ProModem 1200 is a Havescompatible Bell 212A, 300- and 1200-baud phone modem with built-in clock/ calendar. It can be fitted with an optional 64-Kbyte buffer memory. The buffer can be used to store messages for transmission at a preset time-by means of the internal clock/calendar-to a specified group of phone numbers from the directory. Standard features include autoanswer and auto-dial, programmable intelligent dialing, tone and pulse dialing, built-in speaker, and separate phone and data jacks. Basic unit costs \$495. Prometheus Products, Inc, 45277 Fremont Blvd, Fremont, CA 94538. Circle 275

Micro-mainframe link adds IBM 3270 support

Microseek Plus micro-mainframe communication software can link a PC or PC XT to a mainframe as both an asynchronous terminal and 3270 display. Microseek Plus includes file transfer, asynchronous and 3278 terminal emulation, a set of prepackaged log-on sequences, and the ability to automate repetitive PC/host tasks. The package

detects and corrects transmission errors. For 3270 access, the PC must be equipped with an IRMA circuit board. Microseek Plus costs \$7000 plus maintenance. Mainframe software and diskettes for five micros are included. Additional diskettes are \$200 per copy with multiple copy discounts available. **Comshare, Inc,** 3001 South State St, Ann Arbor, MI 48106. Circle 276

Communication package extends PC capabilities

The Proto.Call hardware/software communication package is designed expressly for the IBM PC and PC/XT. It provides electronic mail, automatic send, and unattended send and receive capabilities. Hardware includes a Z80 microprocessor, 64 Kbytes of RAM, 103/212A modem, and RJ11/RJ45 connector slots. Companion communication software diskettes include extensive help screens and menus. Realtime clock with battery backup permits stamping of all transmitted and received messages with the correct date and time. American Teleprocessing Corp, 10681 Haddington, Houston, TX 77043. Circle 277

MEMORY SYSTEMS

Quarter-inch tape drive capacity reaches 132 Mbytes



Designed for use on small to midrange computer systems, the HP 9144A quarter-inch cartridge tape drive backs up HP fixed-disks with capacities up to 12 Mbytes. A 60-Mbyte disk can be backed up in 30 min. The 12-Kbyte drive buffer and optimized system software minimize waits for data transfers and host commands. Read-after-write capability means that media problems are detected as they occur. The HP 9144A is priced at \$3500. Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303.

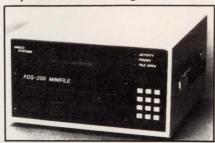
Circle 278

Nonvolatile CMOS static RAM boards attach to the O-bus

Static CMOS RAM boards in the LM1164 series feature two-month minimum data retention time. These 128-Kbyte O-bus units offer 22 address lines, and LSI-11 bus interface, and a maximum operating current of 400 mA at 5 V. Automatic memory protect logic is available onboard. The board has a jumperselectable starting address on 4000-word boundaries and a memory write protect on 8000-word boundaries. Battery backup options are two-fold: a rechargeable NiCad battery ensures 1500 h minimum data retention; and a nonrechargeable lithium battery provides minimum data retention time of 2 years with a projected battery life of up to 10 years. Price is \$1494, with discounts available. Diversified Technology, Inc, PO Box 748, Ridgeland, MS 39157.

Circle 279

Data storage system is portable and intelligent



The Minifile is a flexible high capacity system based on 51/4-in. floppy disks. The unit contains a disk drive, power supply, micro-based controller, serial and parallel interfaces, keyboard, and display. Storage capacities range from 256 Kbytes to 2.7 Mbytes on one floppy. Serial interfaces allow the device to connect to all types of computer-based systems and peripherals, while the optional parallel interface replaces existing paper tape reading and punching devices. Cost is \$2195. Greco Systems, 372 Coogan Way, El Cajon, CA 92020.

Circle 280

A 256-Kbyte RAM addition saves an expansion slot

A 256-Kbyte RAM can be added to the Compag Portable and Compag Plus personal computers. This upgrade gives users the capability for up to 640 Kbytes of RAM on the main system board. It thereby saves an expansion slot for modem, LAN, or other PC-compatible peripheral use. The chip can be installed without system modification. The chip is also standard on the Deskpro model 4 system. Compaq Computer Corp, 20333 FM 149, Houston, TX 77070.

Memory board delivers 256-Kbyte to 4-Mbyte capacity

Employing 22-bit addressing, the MM-1123D is compatible with LSI-11/12 and LSI-11/23 microcomputers and can be used as an enhancement or replacement for the DEC MSVII-LK and MSVII-P memories. With a 200-ns access and 375-ns cycle time, the quadwidth board uses a single 5-V supply. The family is available in 256- and 512-Kbyte versions, as well as in 1-, 1.5-, 2-, 3-, and 4-Mbyte versions. Price of the 1-Mbyte board is \$1795. Micro Memory, Inc, 9436 Irondale Ave. Chatsworth, CA 91311.

Circle 282

Mini floppy drives provide unformatted capacities up to 1000 Kbytes

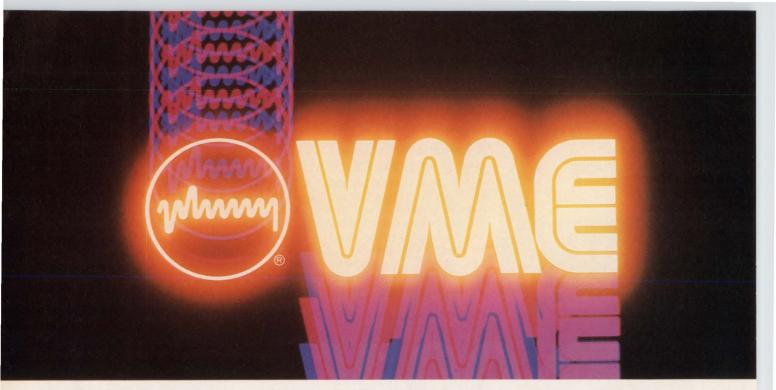
Available in 1/3- or 1/2-high versions, the GM3000 series includes a 48-track/in. version and a 96-track/in. version. The positioner/head assembly has a compact linear stepping motor that is micro driven and has only one moving part. The direct drive spindle motor is also micro driven and designed for continuous use. MTBF is 11,000 hours with no duty cycle limitations. Step times range from 3 to 6 ms with a 15-ms settling time. The drives use 7 W in typical operations. Okidata, 532 Fellowship Rd, Mt Laurel, NJ 08054. Circle 283



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CIRCLE 102

THE SHIP SHIP STORY SHIP SHIP

Floppy disk drive is Apple-compatible

A single-sided, double-density Applecompatible floppy disk drive has track density of 48 tracks/in. and 5.5-kbits/in. recording density. Using a brushless dc drive motor, this unit sports a 250-kbyte/s data transfer rate. Dubbed the FD-100, the disk drive uses a sensor that prevents disk damage by reducing friction within the mechanism. Write error protection circuits eliminate errors caused by the pulse of power on. The FD-100 sells for \$90 in 100-unit quantities. Multitech Industrial Corp, 266 Sung Chiang Rd, 9F, Taipei, Taiwan. Circle 284

Bubble memory system hooks up to LSI-11 microcomputers

Fast access time in harsh settings is the driving force behind this bubble memory system design. An RL02-compatible unit for DEC LSI-11 microcomputers, the OBL-11/02 controller has 22-bit addressing. Storage capacity ranges from 256 Kbytes to 32 Mbytes, depending on choice

of Bubbl-Board companion storage module. Bootstrap ROMs for both the RT-11 and RSX-11 operating systems are included on the OBL-11/02. The controller uses an onboard, single-chip microprocessor to control up to 16 Bubbl-Boards. The controller also contains self-diagnostics. The OBL-11/02 is priced at \$776 (quantity ten). Bubbl-Tec, 6800 Sierra Court, Dublin, CA 94568. Circle 285

Dynamic RAM board extends STD bus environments

The model 6210 is a self-contained dynamic RAM. It has an onboard DRAM controller and crystal oscillator. Several jumper-selectable refresh modes let the user optimize performance. For example, hidden refresh mode can be enabled with either Z80 or 8085 CPUs. This STD bus product features a large bank-switched RAM compatible with all 8-bit CPUs. Onboard parity circuitry generates both a visual indicator (a front card LED) and

a vectored interrupt. The vectored interrupt can be used by the CPU to determine which memory board generated the error. Memory capacity hits 128 Kbytes. Power requirement is 5 Vdc at 1.1 A maximum. Price is \$465. Systek, 1023 N Kellogg St, Kennewick, WA 99336. Circle 286

Removable Winchester provides 10 Mbytes in sub-51/4-in. format

The SQ312RD has 740 tracks/in., 612 cylinders, and 1224 read/write tracks. It is a single disk system with recording surfaces utilized. The drive uses 3.9-in. thin-film metal plated disks, which are sputtered with graphite for improved performance. The graphite acts as a lubricant for head takeoffs and landings and protects the disk surface. Quantity 1000 price is \$750, with the 10-Mbyte cartridge at \$70. SyQuest Technology, 47923 Warm Springs Blvd, Fremont, CA 94539. Circle 287

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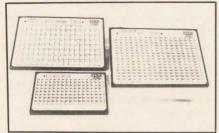
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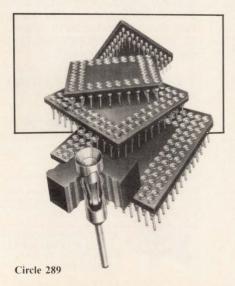
Touch-sensitive feature offers input flexibility



The Concept keyboard is available in three versions, with 128 to 256 touch cells that produce a unique output code. The code output is incrementing binary, commencing at cell 0 with hex 00 to hex ff at cell 127. The output codes are compatible with the ASCII, ISO, and EBCDIC. Standard output is 8-bit parallel, but 4 serial output options are available. Each is supplied with a switch selectable baud rate generator, covering a 50- to 9600-baud range. Power requirement is 5 V at 20 mA. Star Microterminals Ltd, 22 Hyde St, Winchester, Hampshire SO23 7DR United Kingdom. Circle 288

Pin grid array socket has high performance screw machine contacts

Series 709 PGA sockets feature high performance screw machine contacts and a four-leaf beryllium copper inner contact for secure retention. These pin grid array sockets sport a low profile 0.062-in. (1.57-mm) blue glass epoxy insulator and accept standard IC leads. Low insertion/withdrawal force (2.1/1.8 oz) allows easy insertion. Pricing is \$4.20 each for a 64-lead, gold-plated PGA socket in units of 5000. Midland-Ross Corp, 2055 Gateway Pl, San Jose, CA 95110.



Keyboards plug directly into the IBM PC

The PC-84 features the IBM keyboard configuration with return and shift keys in the customary position. The keyswitch has a passive contact system that isolates the contact force from the actuation force to optimize switch performance. The unit is IBM or ASCII compatible, meets the latest DIN standards, has a keyswitch life of 100 million cycles, and includes a 30-char buffer. Tactile or linear feel is available. NMB/Hi-Tek Corp, 7274 Lampson Ave, Garden Grove, CA 92641.



Circle 290

Power MOSFET sports low threshold

The TNO5 has a maximum threshold of 1.5 V, while the standard threshold devices are 3 to 3.5 V. The device requires only 5 V for full saturation for a significant voltage reduction, and is available in both 240- and 200-V versions. Offered in TO-92 and TO-39 packages, as well as in die form, the MOSFETS are \$0.42 in 100 piece quantities. Applications include solid state relays, telecommunications, and battery operated systems. Supertex, Inc, 1225 Bordeaux Dr, PO Box 3607, Sunnyvale, CA 94088.

Circle 291

Compact rack-mountable CRT supplies 80 cols of display

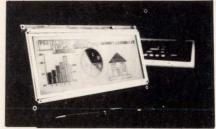
Half-rack width 2200CR and 3200CR system monitors have a full 24-line x 80-col display width. Standard features of the full RS-170 composite video output include: bold writing, double height/width characters, blinking, reverse video, and bar graphics. The units offer optional ASCII keyboards, with a Drawbar feature that permits up to 64 analog parameters to be simultaneously displayed. Also standard are an RS-232/423 serial port and provision for coaxial cabling to a larger remote screen for monitoring and annunciation. Adac Corp, 70 Tower Office Pk, Woburn, MA 01801. Circle 292

Solid state relays help reduce current surges

A Soft Start relay provides a gradual power build-up feature that reduces surges. The two module relays will last longer, produce less noise, and afford greater safety than SSRs or electromechanical relays. A proprietary control circuit provices, by phase control, a gradual application of ac power over 180 ms. Price for the relay is \$27 in 1000s. Crydom, Div of International Rectifier, 1521 Grand Ave, El Segundo, CA 90245. Circle 293

Character count on LCD matches CRTs

Using a 5 x 7 dot matrix, the F641D LDC shows 25 lines of 80 chars and features low power requirements. Power consumption of 200 mW suits the unit for portable applications. The F641D comes with CMOS drivers on a PC board. The unit does not contain a character generator. To simplify connection to other devices, the display incorporates interface circuitry that reduces data input signals to two lines. Outer dimensions of the display package measure 11.8 x 5.75 x 0.51 in. (29.9 x 14.6 x 1.29 cm) while viewing area is 10.7 x 3.9 in. (27.2 x 10 cm). The F641D costs \$410 in quantities of 100. Seiko Instruments, 2990 W Lomita Blvd, Torrance, CA 90505.



Circle 294

Edge connector IC panels come in two sizes and 1/0 areas

The 1208/09/10/11 devices accept filter capacitors and have an 1/0 area of 70 contacts (35 dual rows) or 140 contacts (two sets of rows). The series has tapered entry socket terminals, with four leaf, BeCu, closed-entry inner contact, and machined outer sleeve. Tails are suitable for 1-, 2-, or 3-level wire wrapping. Glass epoxy boards have 2 oz of copper per side, 60/40 tin-lead plated. A universal pattern accommodates DIPs on 0.300and 0.600-in. centers. Precicontact, Inc. 1150 Wheeler Way, PO Box 798, Langhorne, PA 19047. Circle 295

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MEDIA INTELLIGENCE

Product line is IEEE 696/S-100 compatible

The multi-user 816/Dd is based on an 8-MHz 8086 CPU, and features 512 Kbytes of 16-bit RAM (expandable to 1 Mbyte), two 8-in. floppy disk drives with 2.4 Mbytes of storage, four serial ports, plus one printer and one parallel port. The 10-MHz 68000 is at the heart of the 816/Ee, which features 256 Kbytes of 16-bit RAM. Designed as low cost versions of the 816/D and 816/E, the units offer the same features with less memory. The basic 816/Dd system costs \$7995. A basic 816/Ee lists for \$6495. With an 80-Mbyte hard disk subsystem configuration it costs \$12,995. CompuPro, 3506 Breakwater Ct, Hayward, CA 94545. Circle 296

Single-chip microcomputer sports Z8 family architecture

Billed as a "ROMless" version of the Z8 memory control family, the Z8691 provides 8- or 12-MHz memory control. This

single-chip microcomputer handles a system addressing up to 128 Kbytes of offchip memory, supports many memory configurations, and provides up to 24 programmable 1/0 lines. It uses a 5-V power supply and comes in a 40-pin, TTL-compatible plastic package. The Z8681 is priced at \$11.80 each in quantities of 100 or more units. SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Circle 297

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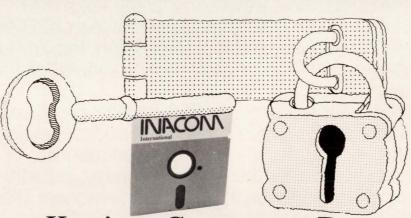
The FE 6420 series of single-board computers is IBM PC-compatible. The series uses the FE 2000 VLSI CPU controller chip and an optional FE 2100 floppy disk controller chip. Models in the series include 64 Kbytes of EPROM, two serial ports, a Centronix printer port, IBM-compatible

Single-board systems

feature PC compatibility

keyboard port, and eight IBM-compatible expansion slots. The units' onboard software supports MS-DOS, PC-DOS, CP/M 86, and Concurrent CP/M. The 4-layer board sports RAM capacities of 64, 128, or 256 Kbytes. Quantity prices start at \$285. Faraday Electronics, 743 Pastoria Ave, Sunnyvale, CA 94806. Circle 298

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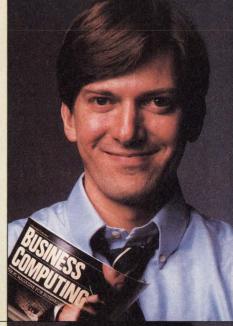


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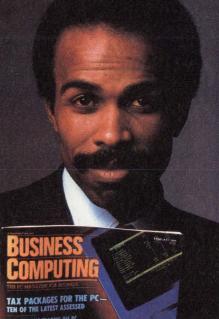


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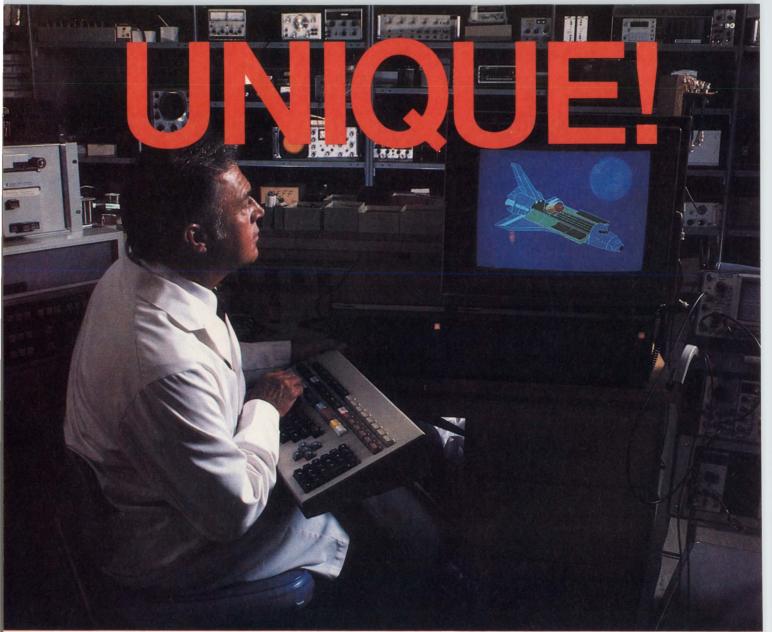


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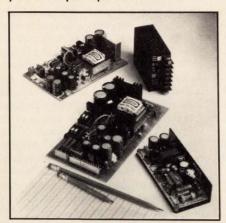
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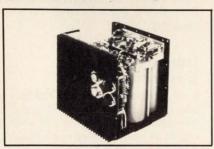
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Power supply line features low power output apt for micros



Switching power supplies offer low profile L-bracket or fully enclosed construction. These models accept a 90- to 130-Vac input voltage range. They also have built-in protection against overload and overvoltage conditions, as well as inrush current limit. The line includes 15-, 30-, and 50-W models with 5-Vdc single output. Also available are 40-, 50-, 65-, and 90-W models in triple and quad output that cover standard output combinations of -5 and 5 Vdc, and -12 and 12 Vdc. Built-in emi filtering and low output ripple are added features. Sola Electric, 1717 Busse Rd, Elk Grove Village, IL 60007. Circle 299

Rugged switching supply sports extended input range



A 165-W, triple-output military power supply, the M7958 offers extremely wide input voltage range of 45- to 350-Vac or 70- to 500-Vdc. Power supply outputs are 5 Vdc at 5 A and ±15 Vdc at 4 A. Each output is independently adjustable and protected against overvoltage and overcurrent conditions. The 0 to 71 °C operating temperature allows operation in rugged environments. CEAG Electric Corp, Power Supply Div, 1324 Motor Pkwy, Hauppauge, NY 11788.

Triple output dc-dc converters feature short-circuit protection

Model MT02812T units provide both 5 Vdc at 2 A and ±12 Vdc at 208 mA from a nominal 28-Vdc input. Rated as 15-W converters, these units are hermetically sealed in metal packages that measure 1.95 x 1.35 x 0.50 in., and provide typical efficiencies of 80 percent over the full input range of 16 to 40 Vdc. Thick-film hybrid circuitry provides small size and high reliability. MT02812Ts feature shortcircuit protection, internal ripple filter, and full 1/0 isolation through use of an optocoupler in the feedback loop. The 100-quantity price is \$267. Integrated Circuits, Inc, 10301 Willows Rd, Redmond, WA 98052.

Circle 301

Multibus-compatible rack handles five cards

The 0.750-pitch rack has a bus structure with enhanced noise immunity. All signal lines run between two parallel ground lines. A ground line also runs directly under the signal on the connector side of the backplane. User installed wire wrap sockets, ICs, pullup resistors, and appropriate wiring convert the system from serial to parallel priority. The rack complies with the IEEE 796 M20 standard. Gold-plated edge connector fingers and connector contacts are standard and power connectors are installed in the backplane. A seven-position version is also available. Prices range from \$193 to \$273, depending on version and quantity. Mupac Corp, 10 Mupac Dr, PO Box 3099, Brockton, MA 02401. Circle 302

Sealed lead acid standby power batteries require no ventilation

The Liberty series is available in 6- and 12-V units with capacities of 25 to 200 A-h at the 8-hour rate. A special model handles high rate discharge. The batteries use an oxygen recombination electrolyte system for a better power to weight ratio, more watts per volume, and better short-term discharge capability. They never need water because, by means of an electrochemical process, the oxygen at the positive plate is reduced to water at the negative plate. **C&D Power Systems**, 3043 Walton Rd, Plymouth Meeting, PA 19462. Circle 303

Conditioner and UPS tasks merge 200- and 500-VA units



Stabiline units combine uninterruptible power supply and conditioner functions in a single, compact assembly. Besides providing backup power, the units regulate voltage within ± 3 percent of nominal, and attenuate transverse and common mode noise. The units sound an alarm and provide continuous sine wave output upon power disruption. An automatically charged battery gives a minimum of 10-min backup at full load or 20-min at half load. Single-phase input ranges from 95 to 135 Vac at 60 Hz. Models are available in 200- and 500-VA ratings with prices ranging from \$800 to \$1000. Superior Electric Co, 383 Middle St, Bristol, CT 06010.

Circle 304

Compact UPS is one-third the size of standard units

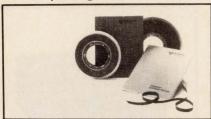
The UPSjr comes in 750-VA, and 1.25-and 2.5- kVA models. The online reserve transfer system provides complete power protection with zero delay transfer time. It suppresses transients, regulates voltage during brownouts, and maintains continuous power to the load during utility outages. Desk high, the unit runs at 55 dBa. Clary Corp. 320 W Clary Ave, San Gabriel, CA 91776.

Circle 305

Tell us what you like

Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Utility off-loads host for fast plotting



The Fastplot utility for Scicards and Schemactive software allows a random element processor to off-load sorting and rasterization. This produces fast electrostatic plotting and reduces host overhead. Fastplot supports color and monochrome plotting. It requires Versaplot Random or Color.Random plotting software on a VAX system. Written in Fortran 77, the utility is available on magnetic tape (800 or 1600 bits/in.) for \$2000. Versatec, 2710 Walsh Ave, Santa Clara, CA 95051. Circle 306

Integrated set of software tools aids design process

Midas software consists of a set of integrated applications for logic simulation, fault simulation, and layout. Distinguished by an integrated data base and engineering data library, the software allows compatibility between all data used in different applications. It also allows simulation of complete systems rather than being limited to individual components. Midas works on CYBER computers and the Cybernet data services network. Control Data Corp, PO Box O, Minneapolis, MN 55440. Circle 307

Seismic software speeds geologic interpretation

In combination with a 32-bit standalone, Landmark 3-D interpretation software can increase interpretation speed by as much as 500 percent. Softcopy interpretation tools include color seismic and contour displays, windows for across-fault correlations, manual and automatic horizon picking, interactive horizon contour mapping, isochron and isopak calculations, volume computations, and pan and scroll of enlarged sections. Other features include split-screen, inline, cross-line or time-slice section comparison; horizon flattening; and horizon attribute mapping. Landmark Graphics Corp, 1011 Hwy 6 South, Houston, TX 77077. Circle 308

Operating system is updated with development tools, faster speed

An Oasis operating system—the Oasis8 Version VI—adds application development tools and increases speed and overall system performance. Enhancements include a command-level, full-function algebraic calculator and EXEC job control language extensions. FIFO queues control disk I/O and overlay management, and improves multi-user performance. The algebraic calculator includes 26 lettered variables that can be assigned and recalled. Oasis Technologies, Inc, 201 Lafayette Cir, Lafayette, CA 94549. Circle 309

Package converts Fortran programs to C

Rapitech's Fortrix-C transforms Fortran programs and files to C code. The package includes integer character string converters, space allocators, string parsers, and other string manipulators not included in standard C libraries. It can be used as a self-instruction aid in understanding the architecture of C code. The Fortrix-C conversion process provides error validation for the input Fortran code. Fortrix-C is priced at \$2500. **Rapitech Systems, Inc**, 565 Fifth Ave, New York, NY 10017. **Circle 310**

Simulation tool brings GPSS to the PC



Aimed at large scale simulation problems, the GPSS/PC software package—an implementation of the General Purpose Simulation System used on IBM mainframes—runs on PCs and PC-compatibles. The package contains over 70 GPSs blocks and commands, and over 45 system numerical attributes. All blocks and SNAs can be accessed from within the program or entered interactively through the keyboard during a simulation. The GPSS/PC is available for a one-time license fee of \$900. Minuteman Software, PO Box 171, Stow, MA 01775. Circle 311

Development package provides cEnglish to C translation

The cEnglish language is based on dBASE II syntax and supports a complete set of standard control flow and data manipulation facilities for application development. It supports virtual memory, procedure calls, parameter passing, and multidimensional arrays. A cEnglish transcompiler is included. This program translates cEnglish into C and uses the host C compiler to translate C into machine language. The cEnglish development tool is portable across micros, minis, and mainframes; interfaces a variety of popular database management systems; and allows escape into direct C programming. The package costs \$1495. cLINE, Inc, 20 W Ontario, Chicago, IL 60610

Circle 312

Concurrent PC-DOS turns IBM PC into multitasking system

Concurrent PC-DOS can run up to four PC-DOS or CP/M application programs at one time. The system provides menus both as a user aid and to let users create their own menus or to compose special commands. Communication capability allows work on one application while the system receives information from a data base. Windows provide the ability to monitor the execution of four simultaneous applications. The windows can be anywhere onscreen and can be scrolled or sized to display certain parts of applications. Price is \$295. Digital Research, 160 Central Ave, Pacific Grove, CA 93950. Circle 313

Lattice windowing eases screen splitting

Lattice Window software simplifies the task of creating programs with multiple onscreen windows. Up to 255 windows can be defined and each can be independently written to or read from, even if the windows are offscreen. Subroutines in Lattice Window automatically open the window, write text within it, process input from the keyboard, and close the window—thus restoring the screen to its previous state. The programmer can define the window's size, shape, color, border, position, and priority, and cause it to move, shrink, or grow. The subroutine library is written in 8086 assembly language. Lifeboat Assoc, Inc, Dept C, 1651 Third Ave, New York, NY 10128. Circle 314

Two artificial intelligence languages get together

A joint implementation of Lisp and Prolog artificial intelligence languages runs on Prime computers. This package combines interpretive and compiled modes for both languages. Each language may be compiled or interpreted as required, making calls on each other without returning to operating system mode. Mapping between the two is accomplished by identical representation of atomic constants. Written in Fortran 77, the system compiler can perform its own bootstrapping. 1/O is performed directly rather than with Fortran I/O. Mitchell Assoc, PO Box 6189, San Rafael, CA 94903. Circle 315

Software controls information transfer

Different computers can communicate with one another in a strictly controlled, secure environment using L:IS. The network application is called a virtual server and resides on the host or on small computers. It acts as a staging area for information and lets users access and transfer data. This server can port information to different types of hardware while transforming the files transferred to the appropriate file format. Linkware Corp, 77 Rumford Ave, Waltham, MA 02154. Circle 316

Engineering package appears in advanced version

Integrated computer aided engineering and manufacturing (ICEM) software now features advanced design drafting and numerical control capabilities. These added functions are united via a shared data base. This gives designers and engineers access to similar versions of all generated data and drawings. The ICEM design/drafting function enables construction of 2-D and 3-D geometries. Numerical control allows generation of control tapes automatically from design geometry. Enhancements of ICEM appear in the areas of design work plane and space, entity selection, part integrity, tablet programs, Bezier curves, and online help functions. Control Data, PO Box O, Minneapolis, MN 55440.

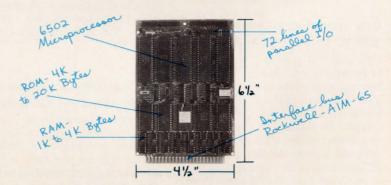
Circle 317

Logic programmer links with high level Boolean package

The ZL30 logic programmer has gained a high level, Boolean entry package. The Compiler for Universal Programmable Logic (CUPL) software package allows logic specifications to be written for any programmable logic device without exact

device definition. Written in C, CUPL is compatible with VAX Unix, CP/M-80, CP/M-86, MS-DOS, and PC-DOS. A ZL30 bundled with CUPL costs \$2850. Stag Microsystems, Inc, 528-5 Weddell Dr, Sunnyvale, CA 94086. Circle 318

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190 S. Whisman Road, Mountain View, California 94041, Telephone (415) 962-8237

Dual-bus architecture enhances Multiple controller

A self-contained processing system with RAM, PROM, and I/O—the CM-5646—controls up to eight ANSI-compatible Winchester disks, and up to four 3M HCD 75 cartridge tape systems. Dual-bus architecture allows an onboard 8089 to communicate with onboard devices over a 16-bit local bus, and with the host system over a Multibus. Communication between the CM-5646 and the host is through parameter blocks in system memory. The CM-5646 performs all disk and tape control, error correction, retries, and DMA control. It can execute user-written 8089 programs from system memory or from local RAM. It is priced at \$1755. Symbicon Assoc, Inc, 89 Route 101A, Amherst, NH 03031.

Circle 319

Data acquisition system teams with PC for powerful workstation

The IDAS 500 provides 128 channels, 14-bit resolution, 50-kHz throughput, and microprocessor control. The unit uses a versatile scan sequence that is downloaded from a computer. Up to 128 channels can be digitized in any order. The system has realtime channel monitoring, selectable display formats, programmable conversion rates, and setup through RS-232 or optional IEEE 488 ports. Price is under \$3000 in quantity. Phoenix Data, Inc, 3384 W Osborn Rd, Phoenix, AZ 85017.

Circle 320

Low cost interface controller expands Net/One LAN

A low cost network interface controller, the Personal NIC, joins the Net/One Personal Connection LAN line. The Personal NIC is compatible with other Net/One Personal Connection products and allows PCs to link with the 10-Mbit/s Ethernet. The NIC, unlike the NIU, executes its protocols within the PC and, while the NIU is placed in a disk or print server PC, the NIC is placed in PCs that function solely as workstations. The Personal NIC is \$595. When equipped with an optional onboard transceiver for use with thin coaxial baseband, the unit is \$750. The Personal NIU is \$1095. Ungermann-Bass, Inc, 2560 Mission College Blvd, Santa Clara, CA 95050. Circle 321

Analog-digital converter adapts to industrial settings



A multifunction process monitor, the model 930, permits conversion of analog to digital signals. It features a dual-slope integrator that updates the signal at a fixed rate compatible with the controller access speed. The 930 accommodates voltage and current in a range of 200 mV, 2 V, 20 V, and 200 V with 100-μV resolution. Models are available for use with 5-, 15-, or 24- Vdc input voltages. Output signals are tri-state latches rated at 5 Vdc. Housed in a rugged aluminum case, the 930 adapts to industrial settings. Cincinnati Electrosystems, Inc, 469 Wards Corner Rd, Loveland, OH 45140. Circle 322

Unit furnishing a 128-byte FIFO buffer joins Z8000 family line

The Z8038 I/O interface unit, available in 4- and 6-MHz versions, provides an asynchronous, bidirectional 128-byte FIFO buffer between two CPUs or between a CPU and a peripheral. This buffer interfaces with a 16-bit or wider data path and expands in depth to add as many Z8060 FIFOs as are needed. The 4-MHz version is priced at \$18.40 in units of 100; the 6-MHz model is \$23.50 in units of 100. SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Circle 323

Rackmounted interface analyzer features LED display

Model 9700 is an analyzer for modems, terminals, multiplexers, and computers. This rackmounted EIA RS-232 module also handles CCITT V.24 diagnostics. The 9700 sports a tri-state LED color display that shows polarity, activity, and validity of key interface signals. It can be patched in series between data terminal equipment and data communication equipment to access and monitor data, timing, and control signals. Interface pins can be individually crosspatched with the analyzer's minipatch cords to test and correct problems. The analyzer is priced at \$275. Electro Standards Lab, Inc, PO Box 9144, Providence, RI 02940. Circle 324

Board features 22-bit DMA, works without CPU intervention

Model 1622DMA is an LSI-11 half-quad board with full 16-, 18-, and 22-bit addressing. This allows high speed memory transfers of analog and digital data from external devices. The board contains all necessary housekeeping and control functions for operation with companion A-D and TTL boards. It features a 16-bit word count register and an 8-bit last channel register, plus a 16-bit control status register. The 1622DMA is compatible with the 1620TTL digital 1/O and 1023FT silo-buffered A-D board. ADAC Corp, 70 Tower Office Pk, Woburn, MA Circle 325

Interface multiplexer sports rapid data comm rates

Aimed at meeting the data communication interface needs of workstations and graphics displays, the VMZ/32HS is a 16-line asynchronous multiplexer interface. It supports rates up to 38.4 kbaud on all lines and is designed for use with DEC VAX machines. The VMZ/32HS exhibits 120,000-char throughput and hardware flow control. Based on earlier VMZ/32 technology (which emulates two DMF32 controllers), the device features rapid fault isolation, programmable DMA, and modem control. MTBF for the VMZ line is set at over 100,000 hours. The VMZ/32HS is priced at \$3750. Able Computer, 1732 Reynolds Ave, Irvine, CA 92714.

Personal computers share printer via intelligent interfaces

ShareSpool family additions allow up to three personal computers to share one printer. Known as the ESI-2016 and the ESI-2018, these devices act as intelligent printer interfaces. They automaticaly buffer and manage print output for one to three units. The ShareSpool family members require only one full-length option slot in on IBM PC/XT, and use none of that machine's processing time. Using the ESI-2016, printer output from two additional personal computers of any type is accepted via their RS-232-C interfaces. The ESI-2018 allows sharing via a parallel, Centronics-compatible interfaced printer. Basic ESI-2016 and ESI-2018 models, with 64 Kbytes of memory and splitter cable, are priced at \$595 each. Extended Systems, 6062 Morris Hill Ln, PO Box 4937, Boise, ID 83711.

Hard disk controller upgrades computer data storage facilities

The LTI-5150 allows installation of ST412 half-height Winchesters to IBM PCs and compatibles. The controller includes a ROM BIOS that is compatible with PC-DOS 2.0 without the need for software drivers. The board features error correction and handles drives with up to eight heads. The unit can be installed in any available expansion slot on the motherboard. Cost is \$395 with quantity discounts available. Logicom Technology, Inc, 560 Forbes Blvd, S San Francisco, CA 94080. Circle 328

Analog input expansion submultiplexer handles acquisition

The model EXP-16 can be used with any data acquisition system. This universal analog input expansion submultiplexer concentrates 16 differential analog input channels into one analog output channel. It also delivers signal amplification, filtering, and conditioning. A high grade instrumentation amp provides userswitch-selectable gains of 0.5, 1, 2, 10, 50, 100, 200 and 1000, and can be programmed for special applications needing specific gains. Provision is made onboard for filtering, attenuation, and measuring current. Analog input connections are made on miniature screw connector strips. Price is \$345. MetraByte Corp, 254 Tosca Dr, Stoughton, MA 02072. Circle 329

Integrated controller boards work with IBM PC

The FE 5141 reduced-size floppy disk controller cuts onboard chip count to eight. It measures 4.5 x 3.8 in. (11.43 x 9.65 cm) and controls from one to four single- or double-sided 51/4-in. floppies. The FE 5200 is an integrated monochrome display adapter with a surface mounted CMOS IC providing control logic. The FE 5200 measures 4.2 x 7.36 in. (10.66 x 18.69 cm) and supports an 80- x 25-char display at

8888 88

350 x 720 pixels. Pricing for the FE 5200 starts at \$120; the FE 5141 starts at \$50. Faraday Electronics, 743 Pastoria Ave, Sunnyvale, CA 94086. Circle 330

Intelligent laser printer controller has universal interface

Claiming compatibility with all present laser printers, the Pixel 300 offers three performance levels. It configures as an 8- to 15-page/min machine, an 18- to 60page/min machine, or as a high performance graphics printer with high resolution and a 4000-char (32 x 50) full page bit map at 0.6 s. This 68000-based system's open architecture accommodates VMEbus products and provides expandable fixed fonts, as well as text, forms, and graphics merge. It is offered at \$3000 per unit in quantities of 500 or more. Electronic Machine Corp, 417 South Hill St, Los Angeles, CA 90013. Circle 331

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247

Software/hardware enhancements increase abilities of logic analyzers

Enhancements to the uAnalysist state and timing logic analyzers include, software performance analysis histograms, context-dependent disk-based help, a 32-channel memory card, and 8088, 8086, and 68000 disassemblers. The histogram menu offers programmable address ranges, masking by symbols, and babysitting mode. The memory card allows a greater number of channels per slot, with the maximum configuration at 80 channels of state analysis and 16 channels of timing analysis.

Northwest Instrument Systems, Inc, 15201 N W Greenbriar Pkwy, Beaverton, OR 97006.

Circle 332

System integrates development and debugging

The MPDS speeds product development by combining hardware and firmware design tools. Emulation, symbolic debug, logic state analysis, and software performance analysis are some of the system's features. An EPROM programmer permits immediate implementation of firmware. Based on CP/M, the unit can run any CP/M compatible application program. The CPU is a Z80A at 4 MHz, with a 64-Kbyte DRAM and 4-Kbyte EPROM. Other hardware includes dual 5½-in. floppy drives, keyboard, and display. Price is \$8400. MicroTek International, Inc, Science Rd 1, Science-Based Industrial Pk, Hsinchu, Taiwan, 300, R.O.C. Circle 333

Machine improves memory testing capabilities

Combining the features of its predecessor J389 memory tester with improved software and added testing capabilities, the J389E is marked by horizontal and vertical manual testing functions. Among the features are clock multiplexing and single-bit complement. The machine can test a broader range of memory products, including static and dynamic RAMS, ECL and NMOS RAMS, and ROMS. A realtime

bit-mapping software enhancement allows on-the-fly modification of test programs and produces displays of bit failures in up to 100 colors. **Teradyne**, **Inc, Inquiry System Analysis**, 535 Morrissy Blvd, Boston, MA 02125.



Circle 334

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Multifunctional system tests VLSI boards and gate arrays

The VDS-8000L tests VLSI-based PC boards. gate arrays, and microprocessors. Interfacing with a device-under-test (DUT) is possible with such devices as edge connectors and flying leads/clips, or by means of remote control boxes or probes. The system offers five test modes: a go/no go mode that involves a "pass" or "fail" for each test routine; a manual mode that resolves mismatches between predicted data and actual operation, a dynamic probe mode that locates defective modes; a learn mode; and a verify mode that allows checking of test data against the DUT response. The Vanwell Corp, 83 Hanover Rd, Florham Park, NJ 07932. Circle 335

Digital sampling oscilloscope interfaces with IEEE 488 instruments

The SAS-8130 offers a 7-in., high-intensity CRT, with the brightness of waveforms and characters controlled independently. Features include digital time and voltage readouts, plus automatic waveform search and auto-ranging. Two sampling heads can be selected to match the required frequency range. Continuously variable pots allow smooth variation of the waveform display's vertical position. Ergonomically designed keyboard can operate in manual, continuous, and ASCII modes. A 3.5-GHz, dual-trace unit sells for \$23,000. Iwatsu Instruments, 120 Commerce Rd, Carlstadt, NJ 07072. Circle 336

Universal programmer comes in small and light package

A portable programmer, the Omni 64, weighs about 14 lb and measures 3 x 9.5 x 14.2 in., while featuring plug compatibility with over 300 different computers and operating systems. It uses up to 64 high speed, high current programmable pin drivers (expandable to 128). It has a large data base of test and programming algorithms to program NMOS, HMOS, CMOS, and bipolar PROMS, EPROMS, EEPROMS, PALS, and single-chip microprocessors on just two ZIF sockets. Software configured pin drivers run at up to 100 V/ μ s. Unit pricing starts at \$3250. Oliver Advanced Engineering, Inc, 676 W Wilson Ave, Glendale, CA 91203. Circle 337

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Single-board color graphics engine has display RAM of up to 2 Mbytes

Color graphics processors in the VM-8851 series are Multibus/IEEE 796-compatible. These boards use 8088 microprocessors as CPUs. Combining DMA and programmed 1/0 functions, they offer 256 simultaneous colors drawn from one of four selectable 4096-color palettes. Using 256-Kbit devices, the basic 512-Kbyte display RAM expands to 2 Mbytes. Options available for the VM-8851 include graphics printer support, light pen and touch-screen input, an iSBX connector, and a resident interact graphics command interpreter. Programmable screen format for 512 x 512 pixels or 640 x 480 pixels is offered. Pixel draw speed ranges from 40 ns to 3 μs. Vermont Microsystems Inc, One Main St, PO Box 236, Winooski, VT 05404. Circle 338

Personal supermini implements Unix, supports System V applications

The U! technical workstation is based on a 68010 virtual memory micro running at 8 MHz. It features demand-paged virtual memory, high resolution graphics, and a multiwindow extension of BSD 4.2 Unix. Standards include 1 Mbyte of memory, a 640-Kbyte diskette, a 22-Mbyte hard disk, high resolution monochrome display, and virtual memory. The system has a fast file system with eight times the performance of other Unix implementations. More than 250 utilities are available. Programming languages include C, Fortran 77, Pascal, Lisp, and assembly. Price is \$15,495 with quantity discounts available. NBI, Inc, PO Box 9001, Boulder, CO 80301. Circle 339

Minicomputer has custom VLSI with support for 32 workstations

The Astra 300 series of 32-bit minis offers a price/performance advantage over the VAX, Data General's MV series, and Prime's 2250. This advantage is a result of a custom 32-bit VLSI CPU with virtual memory segmentation that provides an execution environment free of memory constraints. The minicomputers are compatible with the Astra 200 series. Software applications transport to the larger machines. The series is priced from less than \$15,000. NEC Information Systems, Inc, 1414 Massachusetts Ave, Boxborough, MA 01719. Circle 340



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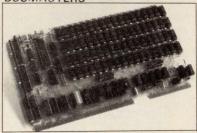
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CIRCLE 112

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SYSTEM COMPONENTS/ COMPUTERS

Micro offers color and monochrome graphics on the 8086

Based on the 8086, Stearns' desktop systems now have monochrome and color graphics capabilities. A monochrome graphics board delivers 720- x 348-pixel resolution and supports graphics programs (such as Lotus 1-2-3, Auto CAD, and PC Plot) developed for the Hercules graphics board. The monochrome graphics board also gives a full 26-row x 80-char dis-

play. Soft function keys are available for customizing programming applications and storing repetitive keystrokes. Memory of 64 Kbytes allows the board to store two pages of graphics data. **Stearns Computer Systems**, PO Box 9384, 10901 Bren Rd E, Minneapolis, MN 55440.

Circle 341

Graphics Controller VGME-512 Features and Specifications High Resolution 512 x 512 Pixels GPS Subroutine Package Dot Addressable via Cartesian Points, Lines, Circles, Arcs, Coordinates Rectangles and Polygons 4 Bits-Per-Pixel Line and Area Texturing Color/Intensity Alphanumerics—96 Characters— Eight Colors with Dual Intensity 2 Sizes Blink at 1Hz to Black or Reduced Picture Storage & Retrieval Intensity High Performance 800,000 Pixel-Per-Second Vector Graphic Generator All Planes Drawn Simultaneously Strategies, Inc. 60Hz Non-Interlaced Refresh Rate 1445 Koll Circle, Suite 107 Line by Line Vertical Scroll San Jose, CA 95112 Multiple Cursors of Arbitrary Shape (408) 294-1300

Notebook-size portable provides 8 x 80 LCD



The PX-8 portable is a 4-lb (1.8-kg) notebook-size machine. The basic unit includes three MicroPro programs (for word processing, spreadsheet analysis, and scheduling) on ROM capsules. The PX-8 offers CP/M 2.2, plus 32 Kbytes of ROM and 64 Kbytes of RAM. The PX-8 measures 8.5 x 11.5 x 1.75 in. (21.6 x 29.2 x 4.4 cm) and features an 8-line x 80-char, high resolution LCD that flips up and adjusts, a full-size ASCII keyboard, and built-in microcassette drive. Base price is \$995. **Epson America**, **Inc**, 3415 Kashiwa St, Torrance, CA 90505.

Enhanced system supports multi-user configurations

A high performance version of the Work-Force computer system provides support for up to 128 users. This version includes a 12.5-MHz 68000 or 68010 microprocessor and a memory management board that accommodates up to 16 Mbytes of memory addressing in a multi-user environment. Multibus-compatible, the CPU design features a high speed secondary bus structure supporting 32-bit data transfers at up to 36 Mbytes/s. The enhanced WorkForce can run up to eight 625-Mbyte SMD drives, eight half-inch nine-track tape drives, and a 6-Mbyte RAM. It also supports X.25, 3780, and Ethernet protocols. Tentative pricing for a 16-user system is \$24,000. Digital Datacom, Inc, 27721 La Paz Rd, Laguna Niguel, CA 92677. Circle 343

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High level language simplifies software development

Robasic is interactive at all times for easy software development and maintenance. Its speed eliminates the need for machine code programming in 90 percent of applications. This language incorporates special industrial control commands such as: TACH, which measures the rpm of a tachometer signal at any or all ports, and PERIOD, which measures the period of a periodic waveform with a 100-µs resolution. Software development tools include a text editor for writing, testing, and storing programs on a single-board computer. Octagon Systems Corp, 6501 W 91st Ave, Westminister, CO 80030. Circle 344

Waveform acquisition machine based on HP 9816S

System 1298 represents a complete multichannel waveform acquisition, measurement, and processing machine. Centered around the HP 9816S computer, the system uses the MALPAK2 supervisory program, a DL1200 programmable waveform recorder, and an HP 9121D dual 3 1/2-in. disk drive. The waveform recorder provides high resolution, 12-bit digitization, and buffer storage for up to eight simultaneous waveforms together with 32 channels of logic event recording. The MALPAK2 can sequence individual key functions and instrument commands into an automatic acquisition and measurement program routine that a user creates to suit a particular task. Transamerica Delaval Inc, CEC Instruments Div, 325 Halstead St, PO Bin 7087, Pasadena, CA 91109. Circle 345

Production system works in batch-oriented environs

The CTX4000-PC is a production control system designed for collection of inventory and ongoing work data associated with batch-oriented process manufacturing environments. Featured are bar-code reader input for error reduction and scheduling systems to manage processing priorities. The baseline CTX4000-PC includes software, an 86000-based CPU, an 80-Mbyte Winchester disk drive, four terminals, a tape drive, a modem, two floppy disk drives, and a printer. System cost, including training and one year service agreement, is \$150,000. CTX International, 575 N Pastoria Ave, Sunnyvale, CA 94086.

Circle 346

Box implements control in industrial settings

The ISB-80C Control Box represents a complete realtime industrial control system. Based on the STD bus, the ISB-80C consists of a single-board computer, a STD bus card cage, a 125-W power supply, and a cooling fan. It contains a 4-MHz Z80A CPU, 64 Kbytes or 256 Kbytes of DRAM, four counter/timer channels, floppy disk controller, DMA controller, 16 parallel 1/0 lines, and two RS-232-C channels. The system resides in a standard 19-in. rackmount enclosure. Disk storage is available. A CP/M operating system comes with the disk equipped models. Price is \$2680. ISI International, 1275 Hammerwood Ave. Sunnyvale, CA 94089. Circle 347

Industrial network software runs on IBM PC

Powr-Spec, together with Adatek's RS-422 expansion card, becomes an inexpensive master station in a factory network. The IBM master gathers data from any of the stations, displays it with color graphics, charts, and symbols; and stores it for future use. The network can include up to 128 programmable controllers. Dual twisted-pair cables make connections up to 5000 ft. Control and monitoring functions include trend analysis, alarm monitoring and sounding; and data logging. The price is \$4950. Adatek, Inc, PO Box 1339, Sandpoint, ID 83864.

Numerical control boards cover axes movement

Compatible with the Multibus, numerical control boards include the NCB-102-2B master board for two-axis control, and its slave-the NCB-102-3B, which allows control of one or two additional axes. Applications cover machine tooling, robotics, table movement, and plotting. Both linear and circular interpolations can be programmed. An onboard z80A allows high speed communication between the host CPU and the device under control. Functions provided include automatic acceleration/deceleration, emergency stop, jog/step feed command, and encoder-pulse multiplication. Sample quantity price is \$2150 for the NCB-102-2B, and \$1360 for the NCB-102-3B. Toko America, Inc, 5520 W Touhy Ave, Skokie, IL 60077.

Circle 349

Integrated hardware and software system based on IBM 5531 PC



An integrated hardware and software system centers on the IBM 5531—an industrial-strength version of the PC/XT. Software support includes full capability for data acquisition of pressure, temperature, and other process variables. Complete process control functions and Action Factory Calc (which provides real-time analog and digital data acquisition spreadsheets compatible with Lotus 1-2-3 and dBase III). Action Instruments, Inc, 8601 Aero Dr, San Diego, CA 92123.

Control Basic streamlines programming of control systems

The C4 Basic language requires minimum system RAM and ROM space for operation. Well-suited for standalone application, it includes standard Basic commands and commands for 1/0 interfacing and control applications. The companion NOVOS software allows C4 programs to be created and tested directly on the target hardware. The C4 Basic (runtime) and NOVOS (development) software are each supplied on a 4-Kbit ROM for use with the Z80 Smart Card STD bus processor board. The cost is \$150 each. VersaLogic, 87070 Dukhobar Rd, Eugene, OR 97402. Circle 351

Computer simulator tests software in industrial systems

The Real Time Simulator imitates the operation of photocells, solenoids, motors, other system components, and process machinery when debugging system control software. A color/graphics display of system activity highlights stress points and evaluates component performance. The simulator can be used as a diagnostic monitor to reduce the time required to identify and correct component failures, without halting production. HEI Corp, 290 S Main Pl, Carol Stream, IL 60118. Circle 352

Smart terminals based on ANSI X-3.64

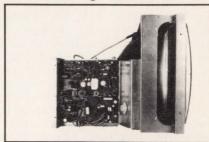
A smart terminal based on ANSI X-3.64 standards, Fame II features a 14-in. screen and multiple-mode capability for the VT-100 and VT-52. Two bidirectional RS-232-C ports permit connection to dual hosts. Nonembedded video attributes and a 256-byte input buffer are standard. Options include full page soft setup screen, smooth scrolling, split screen, and complete local editing. Fame II sells for \$795. Falco Data Products, Inc, 1286 Lawrence Station Rd. Sunnyvale, CA 94089.



3201 Latham Drive Madison, WI 53713

Telex 469532

Monitors available as 19-V models with high resolution



Two 19-V high resolution analog color monitors handle computer graphics. The CDA-203 HA and CDA-203 HLA are raster scan units with precision inline gun CRTs. The CDA-203 HA, with standard P22 phosphor, displays 1024 x 512 pixels in a noninterlaced mode. The CDA-203 HLA displays 1024 x 1024 pixels in a noninterlaced mode; long persistence phosphors are used to eliminate flicker. Both models feature horizontal scan rates of 28 to 36 kHz and video bandwidths exceeding 40 MHz. Ikegami Electronics, Inc, 37 Brook Ave, Maywood, NJ 07607. Circle 354

Video upgrade improves PC output

Designed for upgrading PC and PCcompatible displays, the RGBvision model 440 represents a high resolution RGB color monitor. Combined with the BoB board, the 440 features 720 x 500 line resolution, a 0.31 dot pitch, black face CRT, and a 4000-char display capability. It uses advanced 24.75-kHz horizontal scan frequency. The RGBvision 440 costs \$899.95. Taxan Corp, 18005 Cortney Ct, City of Industry, CA Circle 355 91748.

Thermal printer available in two unique carriage sizes

Whisper printers with standard 2048 char buffers have a 35-char/s print speed. They perform a screen dump of twentyfour 80-char lines in less than 2 s. These standalone, receive-only printers come in two sizes. A 41/2-in. carriage handles 40-col printing and supplements this with an 80-col compressed printing mode. And, an 81/2-in. carriage performs 80- and 136-col printing. Both serial and parallel interfaces are offered. The thick-film thermal printhead (which has a 50-million char life expectancy) and paper drive constitute the only moving parts. 3M, PO Box 33600, St Paul, MN 55133.

Circle 356

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preparation, and general office

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trademark of the U.S. government, Ada Joint Program Office. RM-COBOL is a trademark of Ryan-

McFarland Corp. HK68 is a trademark of Heuri-

kon Corp. Multibus is a trademark of Intel Corp.

800/356-9602 In Wisconsin

608/271-8700

Video display terminal is intended for VT-100, VT-220 operations

A code-compatible replacement terminal for the VT-100 and VT-220, the 922 sports enhanced ANSI characteristics, and has block and function keys that can be programmed in either the shifted or unshifted positions. These features simplify 922 use in software design applications and increase throughput. The 922 has a tilt-and-swivel screen and a keyboard that meets DIN standards. It sells for \$995. TeleVideo Systems, Inc, 1170 Morse Ave, Sunnyvale, CA 94086. Circle 357

Dot-matrix printer touted as low cost portable

An 80-col dot-matrix printer family—the Hush 80—features bidirectional printing at 80 chars/s, graphics at 4800 dots/in.², and weighs only 28 oz. The Hush 80 is offered in three models, each of which can be equipped with a built-in rechargeable nickel-cadmium battery pack option. The 80P is a Centronics parallel version, while the 80S provides a serial RS-232 interface. A single PC card measuring only

21/4 x 11 in. incorporates the internal power supply, print controller, and interface electronics. Complete with interface and cable, prices start at \$159.99. Ergo Systems, Inc, 1360 Willow Rd, Menlo Park, CA 94025. Circle 358

Printer utilizes double daisy wheel design

With a built-in buffer that stores up to 2048 chars at a time, the 5040 printer has a 40-char/s, letter-quality daisy wheel operation. The unit prints in both directions with adjustable character spacing of 10, 12, or 15 char/in., and can handle spreadsheets up to 16-in. wide. The 5040 double-daisy design accommodates up to 125 chars on a single wheel. Various typefaces are available. External software controls allow the 5040 to print up to 309 international Teletex characters. The unit is priced at \$1695. Amdek Corp, 2201 Lively Blvd, Elk Grove Village, IL 60007. Circle 359

Compact unit delivers dot-matrix and near letter-quality printing

The GP-550 offers both standard dotmatrix printing and near letter-quality printing in a single compact unit. In the draft mode, the printer can work at 86 chars/s with six different character sets. The GP-550 has a self-test mode for diagnosis. It has built-in interfaces to microcomputers including Apples, IBM PCs, and PC lookalikes. With built-in interfaces, units start at \$319. The PCcompatible unit costs \$299. Axiom, 1014 Griswold Ave, San Fernando, CA 91340. Circle 360

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Bipolar PROMs sport access time of 15 ns

Fast 32-bit x 8-bipolar TTL PROMS work instead of (or in conjunction with) programmable logic arrays. The devices use 125-mA maximum power supply current, with output drive capability set at 16 mA. Featuring tri-state outputs and full Schottky clamping, 63S081A applications

include random logic replacement and code converters. In quantities of 100, the plastic version costs \$2.98, and the ceramic is \$3.48. Monolithic Memories, 2175 Mission College Blvd, Santa Clara, CA 95050.

Circle 361



Here is a Multibus* based system designed for your real time applications, such as process control/monitoring and data concentration. With it you get:

- Our OB68K1ATM 10MHz 68000 single board computer with 128K bytes of zero-wait-state, dual-ported RAM (addresses 16MB).
- 6 RS232C serial ports, 4 can be RS422.
- 3 (16 bit) parallel ports (1 configured as a Centronics compatible printer port).
- 1 QIC-02 compatible tape interface.
- 20/40/80 MB 8" hard disk.
- 1.2 MB 8" floppy disk.
- 8 slot IEEE 796 card cage (5 slots user definable) with 200 Watts available.
- Calendar clock with battery back-up.
- DMA disk controller.

Software packages from Omnibyte address your real time needs. These include polyFORTH/32**, a 32-bit compact operating environment (ideal for process control) with operating system, high level language, assembler and development tools. Also available, is Idris†, a Unix††-like operating system with real-time enhancements. High level language support includes C PASCAL, BASIC compiler, FORTRAN 77, C Executive, 68000 Native Assembler, hardware floating point support and more!

For more specifics, call Peter Czuchra, Marketing Manager.

- *Multibus is a trademark of Intel Corp.
 **polyFORTH/32 is a trademark of Forth Inc.
 †Idris is a trademark of Whitesmith, Ltd.
 †Unix is a trademark of AT & T Bell Laboratories

A Look at Today. . . A Vision of Tomorrow.



High density CMOS ROMS have 75-ns access times

The 256-Kbit 23C256 ROMs are produced on a 2-micron HCMOS II process. Worstcase access times are 100 and 120 ns over the commercial temperature range, and 150 ns in industrial and military ranges. They also feature, under worst-case conditions, operating current of 25 mA, standby current of 100 µA, and LSTTLcompatible I/Os. These asynchronous and full static CMOS ROMS require no clocks or strobes. Production volume prices are below \$20 each. Solid State Scientific, Inc, 3900 Welsh Rd, Willow Grove, PA 19090. Circle 362

Microprocessor system increases memory speed

Two high performance 16-Kbyte PROMs, the 82S191A and 82S191B, feature maximum address access times of 55 and 45 ns, respectively. Current consumption hits 185 mA. Made with nickel-chromium fuse technology, these devices operate from a single 5-V power supply with a typical power dissipation of 775 mW. Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Circle 363

Gate arrays in HCMOS have 75-MHz flipflop toggle rates

Flipflop toggle rates of 75 MHz are featured on a series of HCMOS gate arrays. Designated Quad Logic arrays, these semicustom family members use a basic 4-gate equivalent cell arranged as two 2-input and two 3-input gates. This architecture limits the number of gates needed to implement macro functions. It also ensures efficient routing and interconnection. Use of double-layer metal interconnections and 3-µm processing technology allows high density circuit layout. Hughes Aircraft Co, Solid State Products Div, 500 Superior Ave, Newport Beach, CA 92663. Circle 364

Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

Onchip voltage regulation marks EEPROM processed in SNOS

An 8-pin, 256-bit serial device, the NCR 59306 expands the NCR family of n-channel silicon-nitride-oxide-silicon (SNOS) EEPROMS. This 16- x 16-bit chip uses a 5-V power supply. An onchip voltage generator allows programming without external high voltage supplies. In the standby mode, power consumption registers only 25 mW. The device is pin compatible with the NMC9306. The NCR 59306 supports four instructions—read, write, word erase, and chip erase. NCR, Microelectronics Div, 8181 Byers Rd, Miamisburg, OH 45342. Circle 365

Family of EPROMS offered in two addressing versions

With 512-Kbit capacities, the 27512 and 27513 devices use HMOS II-E technology. The 27513 features page addressing, making the EPROM compatible with systems based on 8-bit micros and 8- and 16-bit microcontrollers. Partitioning the device into four 16-Kbyte pages frees the processor's address space for additional memory. Both versions provide high density firmware storage for a broad range of applications. Typical programming time is less than 6 min. Each comes in two speeds, offering access times of 250 or 300 ns. The 300-ns version, in 1000s, is \$140. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Circle 366

Programmable logic array devices provide high speed data path

Four programmable logic array devices operate with typical propagation delays of 10 ns (15 ns maximum). Sporting maximum output register toggle frequencies of 50 MHz, these units are suitable as high speed data path logic replacements. Current requirements remain unchanged at 180 mA maximum. The series consists of a TIBPAL16L8 with six I/O ports, a TIBPAL16R4 with four I/O ports and four tri-state registered Q outputs, a TIBPAL16R6 with two I/O ports and six tristate registered Q outputs, and the TIBPAL16R8 with eight tri-state registered O outputs. Devices are available at \$5.18 each in 25,000-piece quantities. Texas Instruments, Inc, Semiconductor Group, PO Box 809066, Dallas, TX 75240.

Circle 367

Gate array circuits offer high density

The 03500 series gives 3500 equivalent gates and support ECL, TTL, or combined ECL/TTL. The Q3500S, the initial array, operates at 0.5-ns typical gate equivalent delays, with power remaining at 1 mW/ equivalent gate. Cell use averages 95 percent of the 242 internal logic cells, with

automatic placement and routing. The 120 universally programmable I/O cells permit interface to TTL, ECL 10K, ECL 100K, or 5-V referenced ECL. Applied Micro Circuits Corp, 5502 Oberlin Dr, San Diego, CA 92121.

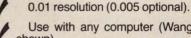
Circle 368

Digitize any standard or custom active area up to 60" x 72" for under \$2,600.00.

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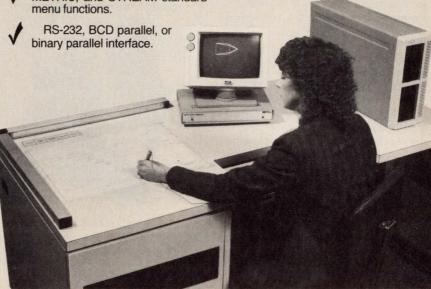


Use with any computer (Wang shown).

Data take-off with stylus or cursor.

There's a lot more to our GP-8 story than low price. We'll tell all: Write or call for our new technical bulletin. We're Science Accessories Corporation, 970 Kings Highway West, Southport, CT 06490, (203) 255-1526, Telex 964-300.

ACCESSORIES



Batteries for memory protection



Five types of sealed nickel cadmium batteries are described in an eight-page illustrated brochure. Detailed data on applications, charging, discharge rates, and temperature ranges are provided for these memory protecting devices. Varta Batteries, Inc, Elmsford, NY.

Circle 410

Industrial computers

Brochure contains information on the IMP-68000 industrial multiprocessor system. The eight-page document outlines these rugged, expandable single-board products, Indocomp Inc, Drayton Plains, Mich.

Circle 411

Protocol converters

System descriptions on a full line of protocol converters include spec outlines for ASCII to SNA/SDLC, ASCII to Bisync, 3275 to SNA/SDLC, and other conversions. Protocol Computers, Inc, Woodland Hills, Calif.

Circle 412

Transceiver connection

Installation and operation of the NT100 Ethernet/IEEE 802.3 transceiver unit is the topic of an NT100 user manual. General truths garnered from three years of local net experience make this pamphlet particularly handy. Interlan, Inc, Westford, Mass.

Circle 413

Interconnections galore

Pin-grid array, DIP, high temperature, LED, and surface-mounted sockets are among the sockets depicted in this 18-page catalog. Advanced Interconnections, Warwick, RI.

Circle 414

Programmable motion controller

Brochure highlights the P420 multiple axis programmable motion controller. Applications and system features (eg, simultaneous coordinated control up to four axes and linear and circular interpolation) are depicted. North Coast Automation, Inc. Cleveland Ohio.

Circle 415

Custom strip assemblies

The S-83 strip products catalog contains specs on a line of socket and terminal strips. These strips can be used to interconnect or stack PC boards, mount ICS, op amps, relays, or as test points. Samtec, Inc, New Albany, Ind.

Circle 416

Digital to resolver converter

An eight-page, two-color data sheet introduces the HDR2116 16-bit digital to resolver converter, which has a 2-VA output and microprocessor compatibility. Natel Engineering Co, Inc, Simi Valley, Calif.

Circle 417

Circle 418

Data acquisition for Apple II

Data acquisition, control, and laboratory analysis programs for the Apple II-based DAISI line are profiled in this directory. Algebraic functions, colorimetry, fast Fourier transforms, and robotic applications are described. Interactive Structures, Inc, Bala Cynwyd, Pa.

Optical cable termination



Procedures and techniques for terminating optical fiber cables are illustrated in a 50-page manual aimed at demystifying these processes. Optical Fiber Technologies, Inc, Nutting Lake, Mass.

Circle 419

Networking glossary

A 24-page booklet covers important terms associated with local area networking. Access methods, topologies, and media, as well as gateways and protocols, are briefly explained. Ungermann-Bass, Inc, Santa Clara, Calif.

Circle 420

Monochrome displays

An 18-page, full-color brochure covers monochrome displays in 5- to 15-in. diagonal sizes. Zenith Electronics Corp, Glenview, Ill.

Circle 421

Circuit board packaging with ZIF

Packaging technology using zero insertion force (ZIF) card guide retainers is chronicled in a comprehensive brochure that provides engineering application information. International Electronic Research Corp, Burbank, Calif.

Circle 422

Amp bulletin

A four-page bulletin presents W-series ultrabroadband rf power amps. It covers models delivering linear operation over the 100 kHz to 1000 MHz spectrum with 1, 5, 10, 50, and 80 W minimum output ratings. Amplifier Research, Souderton, Pa. Circle 423

Video instruments

Bibliography depicts the uses and applications of expansive video instrument line that includes video frame stores, peak stores, digitizers, X-Y indicators, position analyzers, pointers, and mass image storage systems. Colorado Video, Inc, Boulder, Colo.

Circle 424

Intelligent disk controllers

A four-page, four-color brochure describes Sybercache intelligent disk controllers. Charts depict performance improvements based on Sybercache user results. StorageTek, Louisville, Colo.

Circle 425

Switching power

Fifty types of standard switching power supplies are outlined in a catalog. Included are listings from 15 to 150 W, single-, triple-, and quad-outputs, in enclosed or open types. Disk drive switchers also are considered. L-Com, Inc, N Andover, Mass.

Circle 426



CONFERENCES

OCT 29-NOV 1—Comdex/Europe, RAI Congress and Exhibition Centre, Amsterdam, The Netherlands. INFORMATION: The Interface Group, Inc, Rivierstaete, Amsteldijk 166, PO Box 7000, 1007 MA, Amsterdam, The Netherlands

OCT 30-31—Flat Information Display Conf, Red Lion Inn, San Jose, Calif. INFORMATION: Murray Disman, Int'l Planning Information, Inc, 164 Pecora Way, Portola Valley, CA 94025. Tel: 415/854-7306

OCT 30-NOV 2—Wescon High Technology Electronics Exhibit and Convention, Anaheim Convention Center, Anaheim, Calif. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

NOV 2-4—Autotestcon, Sheraton Washington Hotel, Washington, DC. INFORMATION: M. D. Myles (Code Air 552), Naval Systems Command, Washington, DC 20361. Tel: 202/692-3146

NOV 4-8—Int'l Congress on Advances in Nonimpact Printing Technologies, Stouffer's Concourse Hotel, Arlington, Va. INFORMATION: Richard C. Beach, Itek Graphic Systems, 811 Jefferson Rd, Rochester, NY 14692. Tel: 716/475-9050

NOV 12-15—IEEE Int'l Conf on Computer Aided Design, Santa Clara, Calif. INFORMATION: John A. Domiter, Bell Telephone Labs, 4K523, Holmdel, NJ 07733. Tel: 201/949-6675

NOV 13-17—Elektronica, Munich Trade Fair Center, Munich, W Germany. INFORMATION: Kallman Assoc, 5 Maple Ct, Ridgewood, NJ 07450. Tel: 201/652-7070

NOV 14-18—Comdex/Fall, Las Vegas Convention Center, Las Vegas, Nev. INFORMATION: The Interface Group, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600

NOV 16-17—Forth Interest Group Convention, Hyatt Palo Alto, Palo Alto, Calif. INFORMATION: Forth Interest Group, PO Box 1105, San Carlos, CA 94070. Tel: 415/962-8653

NOV 27-30—Conf on Magnetism and Magnetic Materials, Town and Country Hotel, San Diego, Calif. INFORMATION: Alex P. Malozemoff, IBM Research Center, PO Box 218, Yorktown Heights, NY 10598. Tel: 914/945-2154 NOV 28-30—Winter Simulation Conf, Sheraton-Dallas Hotel, Dallas, Tex. INFORMATION: Udo W. Pooch, Dept of Computer Science, College of Engin, Texas A&M Univ, College Station, TX 77843. Tel: 409/845-5498

DEC 3-9—Int'l Microcomputer Conf & Display 1984, The Guangdong Scientific Hall, Guangdong, People's Republic of China. INFORMATION: Meridian Technology Exhibitions Ltd, Rm 1201 Kai Tai Commercial Bldg, 317 Des Voeux Rd C, Hong Kong

DEC 4-6—Western Design Engin Show, Moscone Center, San Francisco, Calif. INFORMATION: David J. Caplin, Clapp & Poliak, 708 Third Ave, New York, NY 10017. Tel: 212/661-8010

DEC 5-7—Conf on Artificial Intelligence Applications, Sheraton Denver Tech, Denver, Colo. INFORMATION: R. Haralick, Dept of Elec Engin, VPI & SU, Blacksburg, VA 24061. Tel: 703/961-6819

DEC 6—California Computer Show, Hyatt Hotel, Palo Alto, Calif. INFORMATION: Norm DeNardi Enterprises, 289 S San Antonio Rd, Suite 204, Los Altos, CA 94022. Tel: 415/941-8440

DEC 6-8—Realtime Systems Symposium, Hyatt Regency Hotel, Austin, Tex. INFORMATION: Miroslaw Malek, Dept of Computer Science, Univ of Texas at Austin, Austin, TX 78712. Tel: 512/471-5704

DEC 9-12—IEEE Int'l Electron Devices Meeting, San Francisco Hilton and Towers, San Francisco, Calif. INFORMATION: Melissa M. Widerker, Courtesy Associates, Inc, 665 15th St, NW, Suite 300, Washington, DC 20005

DEC 10-11—IEEE Computer Society Computer Networking Symposium, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

DEC 11-13—Fifth-Generation and Supercomputer Symposium, Rotterdam, The Netherlands. INFORMATION: Rotterdam Tourist Office, Stadhuisplein 19, 3012 AR Rotterdam, the Netherlands. Tel: 010/14 14 00

JAN 24-26—Modeling and Simulation on Microcomputers, Bahia Hotel, San Diego, Calif. INFORMATION: Ray Swartz, Berkeley Decisions/Systems Inc, 730 Park Ct, Santa Clara, CA 95050. Tel: 408/984-6397 FEB 5-7—Mini/Micro West Computer Conf and Exhibit, Anaheim Hilton Hotel, Anaheim Calif. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-1965

FEB 13-15—Int'l Solid State Circuits Conf, New York Hilton, New York, NY. INFORMATION: Lewis Winner, Almeria, Coral Gables, FL 33134. Tel: 305/446-8193/4

Feb 25-28—Compcon Spring, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SHORT COURSES

NOV 7-9—VDT Ergonomics: Man-Machine Interface, Washington, DC. INFORMATION: George Harrison, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

NOV 7-9—Los Angeles; DEC 5-7—New York—Data Communications and Networking for Personal Computers. INFORMATION: Software Institute of America, Inc, 8 Windsor St, Andover, MA 01810. Tel: 617/470-3880

NOV 12-14—Workshop in Data Communications for Microcomputers, Washington, DC. INFORMATION: George Harrison, The George Washington Univ, School of Engin and Applied Science, Washington, DC 20052. Tel: 202/676-6106

NOV 26-27—Personal Computers/ Worcester Polytechnic Institute, The Hilton, Natick, Mass. INFORMATION: Kathy Shaw, WPI, Office of Continuing Education, Worcester, MA 01609. Tel: 617/793-5517

NOV 28-30—Engineering Use of Lotus 1-2-3/Worcester Polytechnic Institute, Int'l Management Services Computer Lab, Framingham, Mass. INFORMATION: Kathy Shaw, WPI, Office of Continuing Education, Worcester, MA 01609. Tel: 617/793-5517

NOV-DEC—Miscellaneous data communications seminars at various locations. INFORMATION: Beth L. Holl, Datapro, 1805 Underwood Blvd, Delran, NJ 08075. Tel: 609/764-0100



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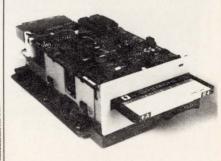
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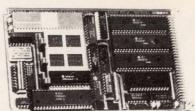
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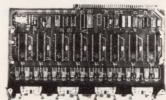
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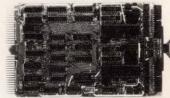


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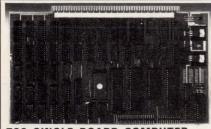
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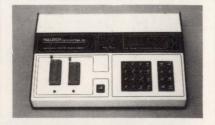
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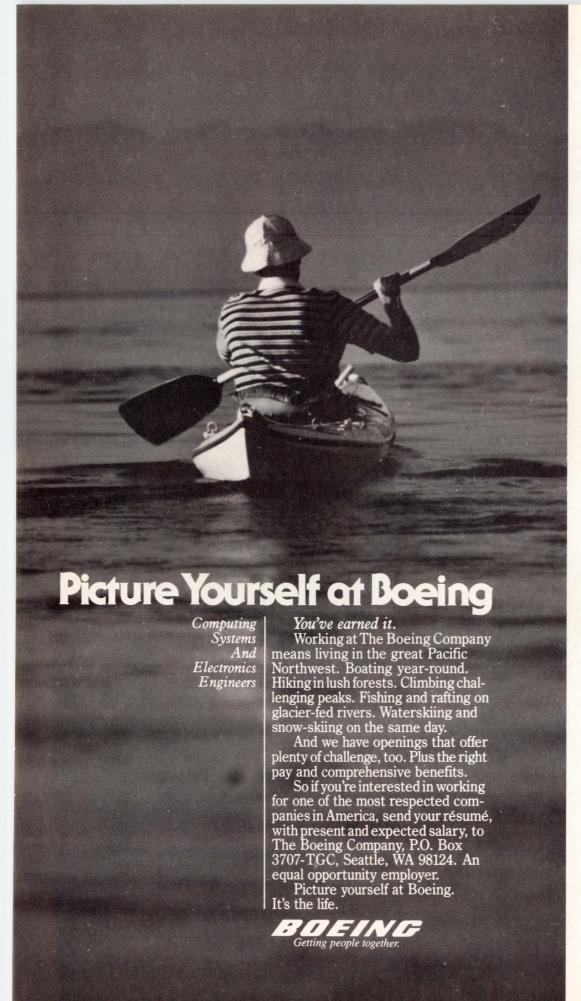
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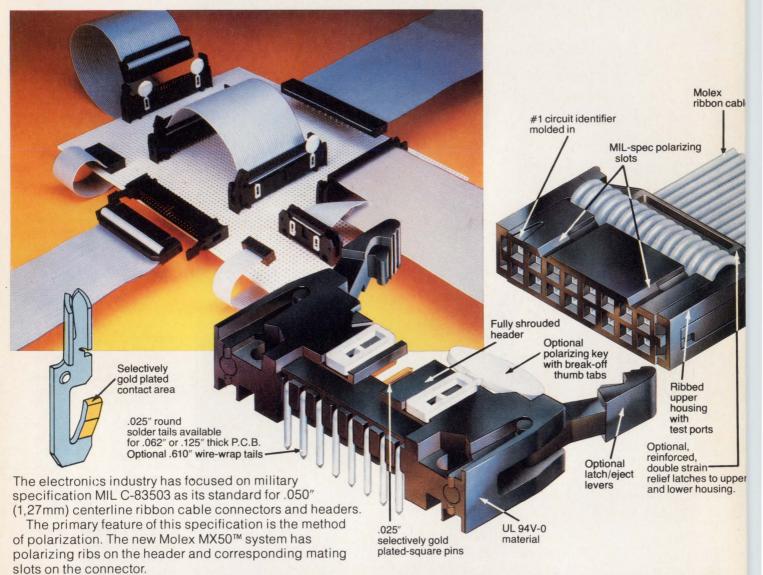
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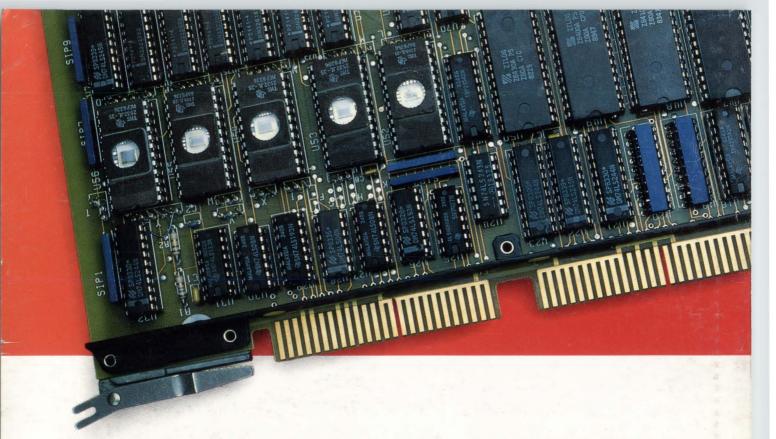
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