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COMPUTER BASED SYSTEMS

POWER SUBSYSTEMS: PROBLEMS AND SOLUTIONS A STATUS REPORT: ANSI 8" HARD DISK INTERFACE

NGG 82 PREVIEW

SPECIAL REPORT: FUTURE DIRECTIONS IN SYSTEMS DESIGN MAY 1982

Whizzard[®] 7600— Another Megatek First.



Megatek has pioneered dynamic interactive refresh graphics systems for years. Ten to be exact. Our Whizzard 5000 was the first advanced high-quality vector stroke generator. The 7000 modular, high-performance 3-D stroke system followed. Then, the 7250 dynamic, high-speed color raster system and 7290 system, which combined stroke and raster workstations powered by one Megatek Graphics Engine.[™] All industry firsts.

Local intelligence

Now, Whizzard 7600. Another first. A new color graphics system with a powerful, userprogrammable 16-bit 8086 microprocessor in a local intelligent front-end module. 7600 gives you a dramatic increase in intelligence. Four user tasks – structuring primitives, running applications subroutines or system peripherals – can be easily and simultaneously handled.

Real-time 3-D object rotation

The 7600 offers many other new innovations. Totally interactive real-time rotation of 3-D objects in 16 of 4096 available colors. Three-dimensional surfaces of up to 600 sides can be filled instantly. And, a 3-D surface processor comes with the system while a floating point processor can be added as needed. Scaling, clipping, 2-D and 3-D rotations are easy. You can choose either 4096² vector refresh or 512² or 1024² raster resolutions.

Offloading the host

What's more, this power and increased intelligence actually reduces drain on the host computer. That's because local intelligence and dedicated processors perform all calculations for complex transformations. Local intelligence also manages display lists, event queues and peripheral interaction, further freeing up your computer. Communication between the CPU and the 7600, up to 1000 feet, is by high-speed parallel data transfer. For greater distances, the 7600 is equipped with two standard RS232 interfaces.

Whizzard 7600. Latest advance in color graphics systems from Megatek where "firsts" have been a habit for years. For details, call or write Megatek Corporation, 3985 Sorrento Valley Blvd., San Diego, CA 92121 or (714) 455-5590. TWX 910-337-1270. MEGATEK, S.A., Avenue du Tribunal Federal, 34, CH-1000 Lausanne, Switzerland. Telephone: 41/21/207055. TELEX: 25037 MEGA CH.



When you ask some people about backup — they back off.

And for good reason. Ask any other supplier of peripheral products for system backup, and you'll find that some can supply a disk, some can supply a cartridge recorder, others a streaming transport. But none can supply the choice which Kennedy can offer.

Kennedy is the only company that can offer an SMD compatible, 8" 40 MByte disk drive (Model 7300) and an 80 MByte 14" Winchester disk drive (Model 5380). To back them up, Kennedy has a ¼" cartridge recorder (Model 6450), and Model 6809, ½" Data Streamer Tape Transport.

Kennedy was the first to utilize the 1/4" 3M cartridge for disk backup; Kennedy was the pioneer in Winchester disk technology, and was a leader in developing a low cost streaming tape drive.

All of these products were conceived and designed to meet the need for reliable, low cost backup — for our systems or for any other system.

Kennedy has always backed its products. That's why we're No. 1. Call or write us about your problem.

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The T-1805 is the latest evolution in the popular and proven T-1000 series of serial printers. As such, the

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JUNE 7-10 Booth #6100



UP FRONT

Computer pioneer receives Computer Society award

Jeffrey Chuan Chu, president of Sanders Technology, Inc, was named the first recipient of the IEEE Computer Society's Computer Pioneer Award at the Compcon Spring conference in recognition of his outstanding work in early electronic computer logic. The award also honors Mr Chu, who was a key member of the engineering team that built the original electronic computer, ENIAC, for "the number of computer professionals that he has inspired in his various leadership capacities in the companies for which he has worked."

Nominations sought for ACM award

The Association for Computing Machinery is requesting nominations for its Grace Murray Hopper Award, given each year to an outstanding young computer professional. Recipients are selected on the basis of a single recent major technical or service contribution to the computer industry. Candidates must be 30 years of age or less at the time the qualifying contribution is made. Emphasis will be placed on the fields of data processing and/or personal computing. The award includes \$1000 donated by the Univac Div of Sperry Rand, and will be presented at the opening of the Association's annual conference on Oct 25, 1982. Nominations, which may be made by the nominees themselves, should be sent before June 15 to David C. Wood, The Mitre Corp, 1820 Dolly Madison Blvd, McLean, VA 22102 (Tel: 703/827-6394). Include name, address, and phone number of both the nominee and the person making the nomination, as well as the date of birth of the nominee, and the date on which the qualifying work was completed. A 200- to 500-word statement, describing the contribution and why the nominee deserves the award, should accompany the nomination.

English-into-Japanese machine translator announced

Hitachi, Ltd has developed a prototype English-into-Japanese machine translation system. Machine experiments have produced passable translations of random paragraphs extracted from English readers for Japanese senior high school students. In the future, the company expects to upgrade the system's performance to enable translation of English science and technology documents. Hitachi also plans to extend this technology to a Japanese-into-English machine translation system for technical documents.

Technology exchange agreements

United Technologies' Norden Systems and Digital Equipment Corp have announced an agreement under which Norden will design, manufacture, and market to the Government militarized versions of DEC's VAX family of computers. The militarized VAX computer will be operationally identical to its commercial counterpart and will run all of the commercially available VAX software.

Rockwell International Corp and NCR Corp have signed a microelectronics exchange agreement that includes alternate sourcing arrangements for selected NMOS and CMOS devices. Details will be disclosed in future announcements.

American Microsystems, Inc (AMI) has announced a design agreement with Weitek Corp under which AMI will manufacture and market Weitek's S681XX family of high speed NMOS ROMS. Included are 16k-, 32k-, and 64k-devices in standard 24-pin packages and pinouts. First samples are expected in June.

UP FRONT

Pretriggers *Peripherals*

Microprocessors/ microcomputers

Interface

Data communications

Control & automation

Development systems

Over 400 characters can be printed from a single plastic printwheel on the Diablo Systems model 630 ECS printer terminal. A printwheel contains two rows of up to 96 characters each and as many as 250 additional characters or graphics can be constructed.

A bit-slice processor in Genisco Computer Corp's G6100 series graphics terminal relieves the load on the host computer by performing high speed raster refresh, data processing, and I/O operations. Resolution is as high as 1536 x 1024 pixels with a pixel write speed of up to $1 \ \mu s$.

Under software control, Cromemco's model DPU combines 8-MHz MC68000 and 4-MHz Z80 microprocessors on a single board with a shared bus. A pseudobank switching technique allows the Z80 to address the full 16M-byte range.

A series of bipolar LSI circuits, called a Macrocell array, can be used as digital processor building blocks. Motorola Semiconductors' MC10900 family includes an 8-bit parity ALU slice, 8- x 8-bit expandable multiplier, an 8-bit BCD/binary ALU slice, and a microcode expander slice.

With a mainframe caliber relational database management processor from Intel, system integrators can design into small systems data storage and handling functions usually found only in mainframes.

3Com Corp's 3C400 Ethernet controller meets specifications established by Digital Equipment Corp, Intel, and Xerox for interfacing MULTIBUS computers to Ethernet. The single-board device with dual-ported memory plugs into the MULTIBUS and connects to an Ethernet coaxial cable via a transceiver.

Fiber optics interface modules from Artel handle RS-170 video graphics over cable runs as long as 10,000 ' (3048 m).

A Winchester disk controller designed by Adaptec for multitasking operating systems is implemented with four ICs, two of which perform data separation. Features include 32-bit ECC, CRC, and block transfers.

A protocol communications processor from Industrial Computer Controls emulates BSC and SDLC standard protocols and provides five conversion levels.

Honeywell's Distributed Systems Architecture adds X.21, X.25 connections and improved networking products.

Cromemco has thrown its hat into the local network arena with C-NET, an economical microcomputer network using shielded twisted pair as a medium.

Key features of a low cost family of CAD/CAM systems for PCB design from Telesis are an innovative touch screen system control and an applications software package.

A portable integrated computer system, Intel's iPDS, can be used either for developing 8-bit microprocessors or as a personal machine for CP/M based applications. It supports integrated hardware and software development, product testing during manufacture, and customer support after the product is in the field.

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	22	01	9	0	10
0	22	01	8	0	18
Q	22	Q1	8	Q	18
Q	22	Q1	8	Q	18
Q	22	Q1	8	Q	18
Q	22	Q1	8	Q	18

The basic 1.0 MB W23 (occupying only eight of the 27 slots) with 80 MB RM02-emulating Winchester is under \$20K! Call us at 609-799-0071 for more details.

Dataram Corporation, Princeton Road, Cranbury, New Jersey 08512. 609-799-0071. Telex: 510-685-2542.

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COMPUTER DESIGN[®]

System technology



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- 277 Interface: A status report: ANSI 8" hard disk interface by Anthony F. Kozlowski—Progress has been swift on ANSI 1226, the rigid disk interface standard for 8" Winchester drives

NCC '82

81 Houston's Astrodomain is gearing up for the 1982 National Computer Conference, where hundreds of exhibitors will display the latest in computers, computer based systems, and peripherals. This year's Technical Program will run the gamut from computer architecture and software engineering to social implications of computers. NCC '82 sessions of particular interest to *Computer Design* readers are previewed in this issue, along with many of the products that will be exhibited.



Vol 21, No 5 May 1982

Special report on future directions in systems design 201 This month's "Design Front

This month's "Design Frontier" discussions include the use of rf network analyzers that aid digital designers; the advantage of custom integrated circuit design in VLSI applications; design automation tools that allow the development of MOS/LSI chips from standard design cell libraries; the benefits of connecting conventional SSI/MSI design to HCMOS arrays; addressing shorthand that allows a chip to address 2⁴⁰ bytes of virtual memory; and a processor architecture that provides designers with tools for effective system resource management



This month's cover, entitled "Self-Correcting Machines," was created by Mark Lindquist on the Digital Effects Video Palette III, a computer aided freehand drawing system

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Paul C. Barr Howard M. Berlin

*Appearing in Domestic issues only

COMPUTER DESIGN 7





7 reasons why the K100-D is now the world's best-selling logic analyzer.

How the general-purpose K100-D beat out H-P to become #1.

Not so long ago, Hewlett-Packard logic analyzers were the industry standard. We asked digital designers to compare the K100-D with H-P's popular 1610B and 1615A logic analyzers before making any buying decision.

In head-to-head comparison, the K100-D came out looking so good, it's now the best-selling logic analyzer in the world. Here's why:

1. It's easy to systematize.

For automated troubleshooting and production ATE, the K100-D features a fully-programmable GPIB interface.

To help you support a wide variety of bus-oriented systems, there are standard high-performance probes, specialized probing accessories and detailed application notes available on all the popular microprocessor systems currently in use.

2. It's concise.

The K100-D monitors 16 channels in time domain, 32 in data domain, so you can probe enough points to pin down problems at their source.

3. It's fast.

A 100 MHz clock rate resolves signals to 10 nanoseconds. The front end is also sensitive enough to capture glitches as narrow as 4 ns.

4. It's deep.

1024 words deep in memory—for faster, more accurate debugging. The K100-D extends the length of data you can trap from your system at any one time.

5. It's clear.

The K100-D has a large keyboard and interactive video display, a comprehensive status menu, highly useful time domain display, and data domain readout in userspecifiable hexadecimal, octal, binary or ASCII.

6. It has remote diagnostics.

A new T-12 communications interface option lets your field troubleshooters share their system observations with the best engineers back at headquarters. Remote diagnostics provide faster debugging and save a lot of time and travel for your most valuable people.

7. It's well supported.

You get full applications support from the experts in logic analysis.

For a free copy of our "Logic Analyzer Comparison Guide," request card for microprocessor system application notes, and T-12 Communicator information, just circle the appropriate reader service numbers. Or contact Gould, Inc., Instruments Division, Santa Clara Operation, 4600 Old Ironsides Drive, Santa Clara, CA 95050, phone (408) 988-6800.

Terrer -

The T-12 "top hat" for the K100-D provides logic analyzer remote diagnostic capability. Other options include the GPIB Analyzer and RS232 Serial Data Analyzer.



Circle 5 for Comparison Guide Circle 6 for App. Note request form Circle 7 for T-12 communicator data





We've doubled storage capacity <u>and</u> reduced reading time...simultaneously

Introducing the KB-32 Magnetic Card Reader/Writer. At Vertel we're always looking for ways to improve parameter loading. With our new KB-32 Card Reader/Writer, we have even outdone the KB-31 system...a system that has become an industry standard.

For example, we've doubled the storage capacity of our Kilobyte card[™], which now means you can record over 2176 8-bit bytes <u>on one</u> <u>card</u>. And our new reader/writer has an improved head that reads all 4

tracks simultaneously...providing twice the amount of information in one-half the time, thereby improving reading time by a rate of 4.

Designed for microprocessorbased systems, the new KB-32 is ideally suited as a low cost peripheral for parameter loading and/or data storage in process control systems, medical data systems and other similar applications.

Call us today to see how the Kilobyte[™] system can benefit you!



CIRCLE 9

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TRY IT, You'll like it

An interesting thing happened on the way to the 16-bit micro market: the public seems to have recognized that computers don't compute much without software. Consequently, nobody has been rushing out to buy 16-bit micros instead of 8-bit micros.

Computer companies, like oil companies, have to move more products every year to keep shareholders thinking in the manner to which they have become accustomed. There was a time when only a foolhardy or an underfinanced company would announce a new piece of hardware without a reasonable amount of software support. However, low cost of entry into the microcomputer business turned almost everyone with a soldering iron and a 'scope into a hardware manufacturer. The result, aside from numerous bank-



ruptcies, was an enormous pile of hardware that frustrated many buyers for lack of software.

Then came CP/M—already well on its way to becoming as generic as Coke or Xerox. Without a doubt, 16-bit micros are here to stay. Everybody, big or small, has either announced or is about to announce a 16-bit wunderkind that will be *the* cat's meow when the software finally arrives. Software companies, created from the 8-bit micro phenomenon, have all jumped into the fray with UNIX or UNIX-like products. This is because UNIX is highly transportable, with transportable compilers available. Of course, the battle with Ma Bell and her offspring over who really owns UNIX has yet to be fought.

Fearful that UNIX may not be the CP/M of the 16-bit world, hardware vendors are borrowing a twist used by third-party vendors for non-CP/M 6502 based machines. That is, build a second micro that runs CP/M into the 16-bit micro so CP/M can be run on (or is it in or under?) a 16-bit micro until software is available.

The big question is why would any cost-conscious OEM, dedicated to building the best performance product for the lowest price, be interested in buying two computers when one will do?

Dunnan

Saul B. Dinman Editor in Chief

Best Technical Article of the Month—December "Semiconductor Memory Update: EEPROMS" Eugene R. Hnatek, Viking Laboratories This article will now compete with other monthly winning articles for the 1981 Windjammer cruise award.

For the microcomputer design manager who wants to bring out the best in his team.

Tek introduces the 8560.

To help his people work as a team, a design manager's got to pull together every designer. But he can't do it alone.

Code volumes are heading toward the megabyte range. Soon, a single project may require designers to develop and debug hundreds of modules all against ever tightening production schedules.

As microcomputer design becomes this demanding, only a team working tightly together can be successful.

But not until now has a micro-

computer development system been dedicated specifically to the needs of a team of designers.

Not until the Tek 8560 Multi-User Software Development Unit. **The 8560 is targeted directly at the team effort.**

For openers, the 8560 sup-

ports up to eight workstations. With each station configurable as either a software development

by project, in sub-directories. So you can quickly locate any file: yours or your team-members'.

TYPICAL 8560 SYSTEM CONFIGURATION



terminal or a hardware/software integration site.

You get all the standard tools you'd expect from a highperformance development system: editors, language translators, loaders, linkers, spooling line printers and hard disc mass storage.

But that's just the start. The 8560 goes on to organize these tools specifically for use in a closely knit team effort. One that channels individual efforts into a workable, synergistic whole.

All through TNIX* TNIX ties the team together.

TNIX, an operating system derived directly from Bell Laboratories' UNIX** V.7 operating system, runs the 8560. Refined specifically for microcomputer development. TNIX includes a multitude of features that enhance the team effort.

The 8560 Supports:						
68000 Z8001 Z8002 8086 8088 8088 8080A 8085A	6800 6801 6802 6809 Z80A 8048 8039	8035 8748 8049 8021 8041A 8022				

A hierarchical filing system allows you to organize your files

*TNIX is a trademark of Tektronix **UNIX is a trademark of Bell Laboratories

Plus multi-level read/write protection that lets users' files become more accessible as they become more complete.

Text processing keeps team members well informed by facilitating timely documentation. All design specifications are easily updated working

documents.

With the number of code modules running into the hundreds, the integration of different "versions" of source modules from multiple team members can result in very bothersome program bugs. TNIX provides a powerful solution through "make", a utility which tracks dependen-

cies between source and object modules,

and insures that only up-to-date object modules are included in the final program.

TNIX extends to hardware/ software integration as well.

For hardware/software integration, the 8560 uses the Tektronix 8540 Integration Unit as an intelligent subsystem. The 8540 employs Real-Time Emulation for fast, efficient debugging. And for tracing real-time program execution, an optional Trigger Trace Analyzer allows highly selective acquisition of bus transactions and other prototype logic events.

And because the 8540's debug commands are fully integrated into TNIX, you have unprecedented power to process debug data. For instance, a few simple commands provide the capability to sift through debug trace data and produce a frequency distribution of all subroutine calls as executed by the prototype program.

Put the 8560 on your team. For more information, contact your nearest Tektronix Sales Engineer about buying or renting the 8560. Or contact us at any of the addresses listed below.

-- 8560 GUIDE --

- 1) Introduction to GUIDE 2) Select prompting level

- 3) File Manipulation Menu 4) Program Processing Menu (compilers, assemblers, etc.)
- 5) Program Debugging Menu (with 8540/8550 only)
- 6) Other System Operations Menu 7) System Maintenance Menu (must be "superuser")
- 8) Terminate GUIDE
- 9) Temporary escape to command language

Select by entering a number from 1 to 9:

GUIDE, a friendly user interface, provides a menu-driven path through system operations, while allowing a return to the con-ventional TNIX command interface at any time.

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Circle 11 for Literature **Circle 12 for Sales Contact**

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The Gould CONCEPT 32/87 minicomputer with array processing provides the unique bandwidth, memory interface and real-time demux I/O capabilities to perform seismic data reduction. The architecture, including the single 26.7 megabyte/sec. SeIBUS, is ideally suited to seismic center processing, where average bandwidth loading often exceeds 10 Mbytes/sec. per bus. Our Common Memory Interface allows the CSPI array processor to operate in parallel for maximum ease of use and processing speed, while freeing up the CPU to handle additional job streams and other applications.

Fully integrated seismic data processing systems, based on CONCEPT/32 mini's, make the most of your computational dollar. They provide enough compute power to handle multichannel trace sorting, reservoir modeling and 3-D processing in an interactive environment... and more.



That's why Denver Processing Center, Inc; Grant Geophysical Corporation, A Petrolane Company; Sefel Geophysical Ltd.; and Seiscom Delta United Inc. all recommend and use Gould CONCEPT/32-based systems. Join the seismic pacesetters.

Gould Inc., S.E.L. Computer Systems Division, 6901 West Sunrise Boulevard,

Fort Lauderdale, Florida 33313. 1-800-327-9716.



Electronics & Electrical Products

CALENDAR

CONFERENCES

JUNE 7-10—National Computer Conf, Astrodomain, Houston, Tex. INFORMATION: AFIPS, NCC, PO Box 9658, 1815 N Lynn St, Suite 800, Arlington, VA 22209

JUNE 13-17—Internat'l Conf on Communications, Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Merrill W. Buckley, Jr, RCA MSR, 108-129, Morrestown, NJ 08057. Tel: 609/778-2554

JUNE 13-17—National Computer Graphics Assoc Conf and Expo, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: NCGA, 2033 M St, NW, Suite 330, Washington, DC 20036. Tel: 202/466-5895

JUNE 13-17—IEEE Pattern Recognition and Image Processing Conf, Holiday Inn Hotel and Casino, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

JUNE 14-16—Design Automation Conf, Caesar's Palace, Las Vegas, Nev. INFORMATION: Bryan Preas, VR Information Systems, Inc, 5818 Balcones Dr, Austin, TX 78731. Tel: 512/458-8131

JUNE 21-23—Technical Conf on emi/rfi Shielding of Plastics, Sheraton O'Hare Hotel, Rosemont, III. INFORMATION: Harold Chapman, D.M.E. Co, 1975 N 17th Ave, Melrose Park, IL 60160. Tel: 312/626-2900

JUNE 28-30—Comdex/Spring '82, Atlantic City Convention Hall, Atlantic City, NJ. INFORMATION: The Interface Group, PO Box 927, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502; 800/225-4620 (outside Mass)

JULY 12-15—Powercon 9, Power Electronics Conf and Exhibit, Hyatt Regency Crystal City, Washington, DC. INFORMATION: Ronald Birdsall, General Chairman, Power Concepts, Inc, PO Box 5226, Ventura, CA 93003. Tel: 805/656-1890

JULY 19-21—Computer Simulation Conf, Marriott City Center Hotel, Denver, Colo. INFORMATION: Marlene Moller, The Aerospace Corp, PO Box 92957, Los Angeles, CA 90009. Tel: 213/648-6608

JULY 25-30—Harvard Computer Graphics Conf, Hyatt Regency Hotel, Cambridge, Mass. INFORMATION: Ann Quenin, Conf Mgr, Special Programs, Harvard Univ, Graduate School of Design, 48 Quincy St, Cambridge, MA 02138. Tel: 617/495-2578 JULY 26-30—ACM Siggraph '82, Boston, Mass. INFORMATION: Convention Services Dept, 111 E Wacker Dr, Chicago, II 60601. Tel: 312/644-6610

SEPT 14-17—Wescon, Los Angeles, Calif. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEPT 20-24—Compcon Fall '82, Capital Hilton Hotel, Washington, DC. INFORMATION: Compcon Fall '82, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

SEMINARS

MAY-SEPT—OEM Sales and Sales Management Training Seminars, various U.S. cities and dates. INFORMATION: Educational Services, Data General Corp, 4400 Computer Dr, MS F019, Westboro, MA 01581. Tel: 617/366-8911, X4030

MAY 31-JUNE 4—Personal Microcomputer Interfacing and Scientific Instrument Automation, Virginia Tech, Blacksburg, Va. INFORMATION: Linda Leffel, CEC, Virginia Polytechnic Institute and State Univ, Blacksburg, VA 24061. Tel: 703/961-4848

JUNE-OCT—Protecting Data and Information, various U.S. cities and dates. INFORMATION: Digital Equipment Corp, Educational Services, Seminar Programs, 12 Crosby Dr, BU/E58, Bedford, MA 01730. Tel: 617/276-4949

JUNE 9-11—Introduction to UNIX, Holiday Inn, Rosslyn, Va. INFORMATION: Institute for Advanced Professional Studies, 55 Wheeler St, Cambridge, MA 02138. Tel: 617/497-2075

JULY-SEPT—Forth Fundamentals, Advanced Systems, and Applications, various dates, Belmont, Calif. INFORMATION: Inner Access Corp, PO Box 888, Belmont, CA 94002. Tel: 415/591-8295

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.

SHORT COURSES

MAY-AUG – EMC, TEMPEST, and emi/rfi course studies, various U.S. cities and dates. INFORMATION: Don White Consultants, Inc, Internat'l Training Ctr, State Rte 625, PO Box D, Gainesville, VA 22065. Tel: 703/347-0030

MAY-DEC—Courses on F9445, F16000, F8, F3870, FS-1, F680X systems, and Pascal for microcomputers, Fairchild Corp, Santa Clara, Calif. INFORMATION: Education Ctr, Fairchild Camera and Instrument Corp, Microprocessor Div, 3420 Central Expressway, Santa Clara, CA 95051. Tel: 408/773-2161

JUNE 1-11—Design of VLSI; AND JUNE 21-25—Personal Computers, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: Industrial Liaison Program; and James Austin, Director, Summer Sessions Office, MIT, Cambridge, MA 02139. Tel: 617/253-2691 and 617/253-2937

JUNE 2-4—Fault Tolerant Design of Microprocessor Based Systems, Univ of Wisconsin, Madison, Wis. INFORMATION: Avinash Vaidya, Program Dir, Dept of Engineering and Applied Science, Univ of Wisconsin Extension, 432 N Lake St, Madison, WI 53706. Tel: 608/262-8592

JULY-AUG—Computer Science Courses, including computer graphics, data bases, local area networks, Ada, artificial intelligence, programming, and systems design, Univ of Calif, Santa Cruz. INFORMATION: Anne Earl, Institute in Computer Science, Dept B, Univ Extension, Carriage House, Univ of Calif, Santa Cruz, CA 95064. Brochure available. Tel: 408/429-5434

JULY 6-9—Peripheral Array Processors for Signal Processing and Simulation, UCLA, Los Angeles, Calif. INFORMATION: Marc Rosenberg, UCLA, 6266 Boelter Hall, Los Angeles, CA 90024. Tel: 213/825-1047

JULY 12-AUG 6—Technical Institutes/Courses, Union College, Schenectady, NY. INFORMATION: Union College, Office of Graduate and Continuing Studies, Wells House, 1 Union Ave, Union College, Schenectady, NY 12308. Tel: 518/370-6288

JULY 19-23—Mini- and Microcomputers: Their Structure, Characteristics, and Applications; AND AUG 16-20—Database Technology, Univ of Michigan, Continuing Engineering Ed, 300 Chrysler Ctr, North Campus, Ann Arbor, MI 48109. Tel: 313/764-8490

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For Immediate Interest Circle 15 For information Only Circle 72

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In nuclear medicine, doctors use Shugart's SA851 drive to store and playback images of the heart (shown here superimposed over x-ray). Photo courtesy of Technicare Corporation.

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Are you designing a highperformance system? Call or write AMD. We're a whole lot faster than fast.



Four microprocessors and several support ICs increase 68000 family's processing power and functionality

otorola, Mostek, and Signetics have jointly developed several circuits that expand the processing power and functionality of the 68000 family. The devices include an 8-bit processor, a true virtual machine, and a computer on a chip for industrial control; all share the 68000's architecture. In addition, several peripheral chips were developed. There is some overlap in the newly announced parts, however. As one company spokesman put it, "we have agreed on the design of a coliseum, now we are going to battle it out."

VM, 8-bit bus, and full 32-bit processor

Two microprocessors—the MC68010 virtual memory processor and the MC68008 8-bit data bus processor—are expected to be available for customer sampling late this year. From **Motorola Semiconductor Products Inc**, 3501 Ed Bluestein Blvd, Austin, TX 78721, both processors are compatible with previous 68000s.

The MC68010 virtual machine (VM) can operate either as a true virtual machine or as the processor in virtual memory systems. When a bus error signal is received, the VM is capable of complete controlled storing of the internal processor state. The internal state can be recovered once the error has been corrected. In addition, the device can be used as a virtual processor with a governing operating system that supervises a number of operating systems. This allows virtual 1/0 to be supported. Each operating system thinks it has complete control of the machine. The VM also includes an allowance for a delayed bus error signal to abort a bus cycle. This bus relaxation allows error detection and correction to be performed without slowing the execution time of instructions when no error occurs.

Execution of instructions takes place on one of two privilege levels—user or upper supervisor. Higher level language, applications, and utility programs are run at the user level. Some instructions and resources are privileged and not available to the user level operations. Operating systems, interrupt handling, and resource and system control functions should execute at the upper supervisor level.

As a virtual machine, the processor can handle virtual 1/0. One governing operating system can execute at the supervisor level and control the management of several others executing at the user level. In virtual 1/0, software drivers for 1/0 devices can be written once and executed from any user level routine throughout the automatic traps. Thus, each separate operating system or application program does not have to contain the I/O drivers, but simply has to know the parameter passing technique for the virtual drivers.

MC68010 is pin for pin compatible with the MC68000. Timing on signals such as the BERR is modified slightly. Opcodes, data, and other software written for the MC68000 will execute on the MC68010. The part will be available this year.

The MC68008 provides designers of systems with 8-bit data buses the benefits of 32-bit microprocessor architecture. The part is source and object code compatible with the 68000. Applications for the microprocessor are seen in byte wide memories and peripherals. It provides users with seventeen 32-bit registers and 56 basic instructions. Moreover, the programmer's model is identical to the MC68000. Nonmultiplexed address and data buses eliminate the need for external demultipliers. It is scheduled for availability this year.

A third microprocessor, the MC68020, is compatible with the MC68000, MC68008, and the MC68010. The device is a full 32-bit microprocessor with instruction set enhancements including floating point and coprocessor operations, improved operating system support, improved bus efficiency, and an instruction cache. Sampling of this part is planned for late 1983. In addition to the processors, two new controllers will also be available. Designed to perform memory to memory and peripheral to memory data transfers, the MC68440 dual direct memory access controller (DDMAC) moves blocks of data with minimum involvement of the host processor. Addressing range is 16M bytes, and both single- or dual-address transfers are accommodated.

The MC68452 bus arbitration module (BAM) allows multiple local buses to be multiplexed onto a common bus. This multiplexing allows the local buses to share memory and 1/0 devices, and easily communicate with each other. The device is completely asynchronous. A single BAM provides arbitration for up to eight local buses and can be expanded to support more.

Single-chip microcomputer and four ICS

A version of the 68000 and four family support circuits are being contributed by **Mostek Corp**, 1215 W Crosby Rd, Carrollton, TX 75006. The devices are the MK68200 16-bit single-chip microcomputer, the MK68564 dual-channel serial 1/O (SIO) peripheral circuit, the MK68590 local area network controller for Ethernet (LANCE), a companion part, the MK3891 serial interface adapter (SIA), and the MK68901 multifunction peripheral (MFP) chip.

Designed for high performance industrial control and instrumentation (continued on page 24)



MK68590 local area network controller and MK3891 serial interface adapter create Ethernet interface to computer system.

From the Spinwriter People: The new NEC FD 1165 diskette drive.



Half the space/twice the capacity. Boost your profit margins and add new capabilities to your system with NEC's new Model FD 1165 diskette drive.

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uses only DC voltage, and cuts power and power supply costs. These are just a few of the technical extras you get. <u>Reliability.</u> An MTBF of 24,000 hours over 5 years usage at normal duty cycles —an MTTR of 30 minutes and a 60% parts reduction, make the Model FD 1165 the most reliable product in its class. Ease of installation. Vertical or horizontal mounting. Without modification. By now you get the idea. Find out more about NEC's new Model FD 1165 diskette drive. Call your nearest NECIS sales office to order an evaluation unit today.

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> NEC's new Model FD 1165 diskette drive doubles your storage capacity–from 1.6MB to 3.2MB–witbout doubling your space.

applications, the MK68200 is not intended to run an operating system. Instead, the microcomputer which uses 16-bit addressing, was developed for optimum control performance. For example, the microcomputer performs a 16 x 16 multiply in $3.5 \ \mu s$, a 32/16 divide in $4 \ \mu s$, a 500-ns register to register move or add, and runs at a 6-MHz clock rate. Several MK68200 processors can be interconnected by either a single serial channel or a shared parallel bus where multiple processors or distributed intelligence is required.

Onchip resources such as ROM, RAM, and I/O are accessed within each microcomputer without affecting the use of the shared bus so that only external communications compete for bus bandwidth. In addition, the microcontroller can be used as a peripheral controller. Since the MK68200 includes both a serial channel and an external bus capable of performing DMA transfers, it can be programmed to act as a serial DMA controller.

Implemented in Scaled Poly-5 NMOS, the microcomputer is packaged in a 48-pin DIP with 40 pins available for I/O. The 4k bytes of onchip ROM and 256 bytes of onchip RAM are provided within a 64k-byte address space allowing expansion in future versions. The part will be available for sampling in the last quarter of 1982.

The dual-channel MK68564 SIO is capable of handling asynchronous and synchronous bit and byte oriented protocols. As a data communications device, the SIO transmits and receives serial data. As a 68000 peripheral, it interacts with the CPU and other peripheral circuits, sharing the data, address, and control buses, and is a part of the 68000 interrupt structure. It can also act as a peripheral to other microprocessors, providing nonvectored interrupts, polling, and simple handshake capability. The SIO is fabricated in N-channel silicon gate depletion load MOS technology in a 48-pin DIP. Availability is slated for sampling during the last quarter of 1982.

The SIA and LANCE chips are intended to operate in an environment with a closely coupled memory and microprocessor. The two local area network devices are shown as components of a network interface module in the Figure. MK68590 LANCE interfaces to a microprocessor bus with time multiplexed address and data lines. Local memory provides packet buffering for the chip and serves as a communication link between the chip and the processor. During initialization, the control processor loads into LANCE the starting address of the initialization block plus the operating modes of the chip via two control registers. The host processor talks directly to LANCE only during the initial phase.

MK3891 SIA interfaces the LANCE Ethernet protocol controller with a standard Ethernet transceiver cable.

The MK68901 MFP combines several microprocessor system peripheral functions onto a single chip. These functions include four timers, an interrupt controller for 16 sources, and eight parallel 1/0 lines. Control and status interface is provided by 24 directly addressable internal registers.

Five peripheral circuits

Five circuits—the SC68430 single channel DMA interface (DMAI) circuit, the SC68681 dual asynchronous receiver/transmitter (DUART), the SC68562 dual universal serial communications controller (DUSCC), the SC68454 intelligent multiple disk controller (IMDC), and the SC68459 disk phase locked loop—were announced by **Signetics Inc**, 811 E Arques Ave, Sunnyvale, CA 94086. Engineering samples of the DUART will be available this month. Samples of the DMAI will be available in the last quarter of 1982. The others will be available for sampling in the third quarter of this year.

The DMAI transfers a series of operands (data) between microprocessor memory and a peripheral device: operand sizes can be byte, word, or long word. A block is a sequence of operands: a transfer count stored within the DMAI determines the number of operands in the block. The SC68430 can be programmed to utilize signal cycle (cycle stealing) or burst data transfers. Constructed using ISL bipolar technology, it is contained in a 48-pin DIP.

SC68681 DUART provides two independent, full-duplex asynchronous receiver/ transmitter channels. The part can be used with the 68000 and other microprocessors. Operationally, it is similar to the company's SC2681 chip. The device can be used in polled or interrupt driven systems. Features of the DUART include quadruple-buffered receiver data registers, programmable data formats, baud rate and parity, and framing and overrun error detection. MOS communications device is implemented in a 40-pin package.

As well as asynchronous protocols, the S©68562 DUSCC was developed to support bit oriented and character oriented (byte count and byte control) synchronous data link controls. The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. It is well suited for dual-speed channel applications.

Each channel of the DUSCC consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase locked loop, a parity/CRC generator and checker, and associated control circuits. Each channel's operating mode and data format can be programmed independently. The transmitter and receiver each contains a 4-deep FIFO, with appended command and status bits, and a shift register. There are two DUSCC versions; the standard version is packaged in a 48-pin DIP. while a 40-pin version is limited to dualaddress transfers during DMA operation. Both are fabricated in MOS.

SC68454 IMDC is capable of simultaneously controlling up to four Winchester-type hard disk drives with SA1000 or Seagate ST500 interfaces, or floppy disk drives in any combination. A DMA controller, capable of handling data transfers between the host system memory and the drives connected to the IMDC, is included in the host interface. Data transfers on the host data bus can be programmed for either 8- or 16-bit parallel operation. The disk driver interface handles a serial data rate up to 10M bps. Circuitry is fully TTL compatible, and is in a 48-pin DIP.

A companion to the IMDC, the SC68459 disk phase locked loop interfaces to the disk and IMDC. The 22-pin digital and analog device is fabricated in bipolar technology.

—Douglas Eidsmore, Senior Editor Motorola—Circle 240 Mostek—Circle 241 Signetics—Circle 242

16-bit single-board computers run at 8 MHz

Based on the 8086, iSBC 86/30 and 86/14 are 16-bit single-board computers with 8-MHz performance. iSBC 86/30 has 128k bytes of onboard RAM; iSBC 86/14 has 32k bytes. Memory capacity of both boards can be doubled with the addition of the company's recently released RAM Multimodule memory boards. Both boards have two 16-bit iSBX interfaces to Multimodule products such as parallel I/O, serial I/O, math, A-D, D-A, and IEEE 488 and floppy disk controllers. *(continued on page 28)*

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70 megabyte CSS-800 storage system lets your micro work like a mainframe.



Multi-ported cache memory with look-ahead buffer

The CSS-800 has the first microprocessor-based controllers to use advanced data management architecture normally found only on mainframe machines. Its Model 3450 disk controller contains a 32 Kbyte multi-ported cache memory which delivers continuous full track data transfers without sector interleaving delays. Cache management logic determines which disk sectors are being used most often and keeps them in cache for immediate access. When you're doing sequential transfers, the CSS-800's look-ahead buffer will probably have the data you want in cache before you ask for it.

Emulates DEC RK07 and TU10

To DEC systems, the CSS-800 looks like DEC's RK07* cartridge disk drive and TU10* industry standard tape drive. So the CSS-800's 70 megabytes of disk storage with ¼ inch cartridge tape back-up adapts to your DEC system like part of the family.

^{*} LSI-11 , Q-bus, Unibus, RK07 and TU10 are registered trademarks of Digital Equipment Corporation. Multibus is a trademark of Intel Corporation.

Diagnostics built-in for disk, tape drive, and controllers

Status codes for controllers and drives are displayed on front panel lights. The CSS-800 can easily be commanded to run exhaustive self-diagnostic tests on its controllers and peripherals, and a fault indication is simultaneously provided to the host computer and displayed on the status lights.

RT-11, RSX, RSTS/E, TSX, and UNIX

The CSS-800 is software compatible with all three major families of DEC operating systems: RT-11, RSX, and RSTS/E. It also supports the popular TSX and Bell Laboratories' UNIX operating systems for the DEC LSI-11 hardware family.

ECC error correction and automatic error logging

The CSS-800 corrects all errors up to 8 bits in length using a 32 bit Error Correction Code (ECC). Any disk error is automatically logged. The controller automatically remaps defective disk sectors so that the process is transparent to the host computer.

Rugged desk top or rack mounted chassis

The CSS-800 is 5¼ inches high and weighs only 42 pounds, its Winchester disk is internally shock-mounted, and the system is engineered for continuous, trouble-free use.

Just plug it in

Everything you need...hardware and software...is built right in. The CSS-800 is up and running on your existing system as fast as you can get it out of the box and plug in the AC line cord and the host interface. Our Q-bus*, Unibus* or Multibus* compatible interface boards are included as standard equipment. So the CSS-800 is plug compatible with LSI-11, PDP-11, VAX, and all Multibus hardware. For any other bus structure the proprietary USDC I/O bus® is easily adapted.

If you need more than 70 megabytes of storage capacity, you can add on up to 210 megabytes more disk and 51 megabytes of tape back-up by using three economical CSS-800A expansion units. Since the CSS-800A drives are controlled by your CSS-800, they do not require their own host interfaces or controllers.



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Our CSS-800 microprocessor-based controllers are software-intensive, which gives us the flexibility to adapt our hardware to advancements in host system technologies. The CSS-800 is a flexible system, designed to pace a rapidly evolving industry.

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CIRCLE 20

SYSTEM TECHNOLOGY/MIGROPROGESSORS/MIGROGOMPUTERS



Block diagram of isBC 86/XX single 6.75" x 12" board computer. 86/30 has 128k bytes RAM, 86/14 has 32k bytes RAM. Both 8086-2 based computers perform at 8 MHz. System clock, read/write memory, ROM, I/O ports and drivers, serial communications interface, priority interrupt logic, and programmable timers are onboard.

Applications are seen in word processing machines, small business computers, instrumentation, industrial automation, and data acquisition and control systems. A functional diagram of the board is shown in the Figure.

The boards' central processor is the iAPX 86/10 (8086-2). A jumper selectable option provides a 5-MHz clock rate. CPU architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers, and two 16-bit index registers, all accessed by 24 operand addressing modes.

The 8086 instruction repertoire includes a variable length instruction format (with double-operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. For enhanced numerics processing capability, the iSBC 337 numeric data processor extends the iAPX 86/10 architecture and data set. Over 60 numeric instructions offer arithmetic, trigonometric, transcendental, logarithmic, and exponential instructions.



Prefetching of sequential instructions is provided by a 6-byte instruction queue, which can reduce the 750 ns minimum instruction cycle to 250 ns for queued instructions. The stack oriented architecture supports modular programming. Four segment registers (code, stack, data, extra) contain program loaded offset values used to map 16-bit addresses to 20-bit addresses. Each register maps 64k bytes at a time.

The single-board computers contain 24 programmable parallel I/O lines. System software is used to configure the I/O lines in several combinations of unidirectional I/O and bidirectional ports. Sockets are provided for interchangeable I/O line drivers and terminators.

A programmable communications interface using Intel's 8251A USART is contained onboard. A software selectable baud rate generator provides the USART with common communication frequencies. Mode of operation is under program control.

Three independent programmable 16-bit interval timers/event counters are provided. Each counter is capable of operating in either BCD or binary modes. Two of these timers/counters are available to the systems designer to generate accurate time intervals under software control. Routing is jumper selectable. The outputs can be independently routed to the 8259A programmable interrupt controller and to the I/O terminators associated with the 8255A. This allows external devices or an 8255A port to gate the timer or to count external events. The third interval timer in the 8253 provides the programmable baud rate generator for the RS-232-C USART serial port.

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processor based N-key-rollover and phantom key lockout system developed by Oak engineers. Without the cost and complexity of Hall Effect and capacitive technologies.

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Interactive Data Terminals.

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- RF or Video output. Designed to work with standard TV sets or monitors.
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Plus much more.

For more information write RCA MicroComputer Marketing, New Holland Avenue, Lancaster, PA 17604, or call 717-291-5848. To order, call toll-free, 800-233-0094.

*OEM quantity price, Model VP-3301 (video/audio output).



SYSTEM TECHNOLOGY/MIGROPROGESSORS/MIGROGOMPUTERS

MULTIBUS arbitration control logic allows up to three boards to share the system bus using a serial (daisy chain) priority scheme and up to 16 masters to share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations, it also provides an efficient mechanism for all forms of direct memory access transfers. Both boards are available now. In small quantities the 86/30 is priced at \$3800; the 86/14 at \$2475. The isBC 304 128k-byte RAM Multimodule expansion for the 86/30 is \$1250; the isBC 300A 32k-byte RAM Multimodule expansion for the 86/14 is \$750. Intel Corp, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.

Circle 243

DEVELOPMENT SYSTEMS

Ethernet based network uses standalone microprocessor development workstations as network nodes



Fig 1 Hierarchical file structure. Each file can be traced by path name that uniquely identifies every directory on tree.

Recently announced by Intel, NDS-II network development system allows the company's installed base of standalone Intellec systems (*Computer Design*, July 1977, p 124) to serve as nodes on a network of shared hardware and software development tools. NDS-II connects these systems to one another and to high performance peripherals and a large data base, sharing these distributed resources to increase the scope of their original functions. Modular in concept, NDS-II can be expanded by incrementally adding capabilities as needs dictate. All Intellec models, from the MDS-800 to the Series III, can become network workstations.

Physical and data link requirements of NDS-II are provided in accordance with Ethernet; movement of data packets containing files or electronic messages is managed by Intel's local network architecture iNA. The Ethernet baseband network supports 10M-bps transmission and reception of packetswitched messages over a 50- Ω coaxial cable. Cable segments are up to 500 m in length and can handle as many as 200 attached nodes. Larger networks can be effected by joining cable segments via repeaters. Network access is by hardware based, carrier sense multiple access with collision detection (CSMA/CD).

NDS-II allows a large number of stations to work simultaneously on program code creation, assembly, compilation, debugging, and program management. Sophisticated system hardware and software support complex programs and their management. However, user interface and commands are consistent with those used since 1975 when the first Intellec system, model MDS-800, was introduced.

Heart of the system is the network resource manager (NRM), an 8086 based system that attaches to the network in the same way as other stations, through an Ethernet transceiver. Acting as an intelligent file server, the NRM oversees the activity of all stations connected to the network. A powerful multitasking operating system resident in the NRM concurrently supports electronic mail, disk storage, I/O operations, and file management.

Another NRM function, distributed job control, allows a user to prepare a source code module for compilation, and export the compiling job to another available workstation while he continues to work on source code editing. NRM job control software automatically performs this transaction. This parallel processing capability can significantly reduce overall development time. A protected hierarchical (inverted tree) file system provides efficient file sharing. Each user directory represents a node in the hierarchy of directories (Fig 1). The file system is distributed and includes not only the files located in the common data base but also those in the user's own workstation disk. When logged off the network, the user can access only his own files; logging on allows access to all NRM directories. Use of these facilities is virtually transparent to the user.

Several new software tools such as project management tool suite (iPMT) for software version control and automated software generation, plus a high level language debugger, Pscope, complement the system. An iPMT program called MAKE can be resident in the NRM and shared by all users. MAKE automatically merges the latest versions of source or object modules into larger programs ready for assembly or compilation. When the modules to be combined are specified, MAKE handles modular dependency requirements and combines the modules.

The NRM is packaged in a floor standing cabinet (Fig 2) that incorporates 13 MULTIBUS slots, power supply, 8086 microprocessor board, 8088 and 8089 I/O processor board, 512k-byte memory board, NDS-II communication boards, and a 5.25" flexible disk drive.

Existing Intellec development stations may be upgraded for use as NDS-II resources with the NDS-II communication (continued on page 32)



Fig 2 NDS-II with two Intellec development systems. Up to eight such stations can be connected. NRM, left of table, oversees workstation activities; peripheral attachment houses Winchester drive. Supervisory terminal atop NRM cabinet provides access to network management software.

ASCII Encoded Keyboards.

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- Two-key rollover circuitry.
- Aural keypress feedback with adjustable volume.
- High noise immunity CMOS circuitry.
- Low power, 5V DC operation.
- Three serial output modes: RS-232C, 20 mA current loop and TTL.

For more information, write RCA MicroComputer Marketing, New Holland Avenue, Lancaster, PA 17604, or call 717-291-5848. To order, call toll-free, 800-233-0094.

*OEM quantity price, Model VP-601 (parallel output).



SYSTEM TECHNOLOGY DEVELOPMENT SYSTEMS



Fig 3 Intellink-connected mini-network. Intellink module allows up to eight workstations and NRM to be interconnected without expense of Ethernet transceivers. If required, Intellink cluster can access NDS-II Ethernet cable through single transceiver.

controller board set. The 2-board set provides the physical and data link requirements and plugs into MULTIBUS card slots on the chassis. One board contains an 8088 microprocessor with associated ROM and RAM, interval timers, and DMA channels for 10M-bps transmission and reception of data. The second board incorporates bit serial send/receive logic, Ethernet message packet address-recognition logic, and error detection logic. The two boards combine to handle message framing, link management, error detection, preamble generation and decoding, and bit encoding and decoding.

In configurations where a cluster of workstations is located within a 50-m radius, an Intellink communications module can be used in conjunction with an NRM to form a mini-network (Fig 3). Up to eight workstations can be connected to the Intellink via 10- or 50-m cables, saving the expense of full-length Ethernet cables and associated transceivers. When it is time to expand the network, the Intellink cluster can be connected to the Ethernet through a single transceiver.

NDS model iMDX-450A-035 includes the NRM, one Intellink controller, system control console, 5.25" floppy disk drive, 35M-byte Winchester drive, software, documentation, and interconnecting cables. System price is \$39,950.

Communication upgrade kit iMDX-455 for Intellec models 800, Series II/85, and Series III, is priced at \$2000. Kit iMDX-4551 is for Series II/80 and costs \$4000. Prices quoted are U.S. only. All items are currently available. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

—Jim Hughes, Senior Editor Circle 244

Interactive system enables remote users to specify, design, and verify custom LSI, VLSI circuits

ULA Designer is an interactive design system consisting of a powerful minicomputer, control console, edit terminal, digitizer, and optional plotter. When installed in a customer's premises, it provides the design engineer with all the computer aided design (CAD) facilities required to specify, design, and verify LSI and VLSI circuits. The Ferranti system is a primary extension of the company's uncommitted logic array (ULA) concept. Operation of the system does not require experience in computer systems or semiconductor technology.

Ferranti's ULA inventory, which dates from 1971, consists of more than 50 LSI chip types-each with an array of uncommitted active and passive components, and each fully processed except for the final interconnect process-entirely devoted to component interconnection for integration into a system. A single mask is required for this final process, compared to five to eleven for other techniques. This results in shortened development and production times and lowered costs. ULA chip complexity ranges from 100 to 10,000 gates, with performance characteristics from CMOS level to ECL speeds. The ULA concept permits the implementation in LSI form of digital, linear, or mixed digital and linear (DIGILIN) circuits to user specifications.

In the ULA chip organization, power rails are placed in the bulk semiconductor material. The final design stage can be dedicated to chip component interconnection and applied with a single mask. Each chip has a matrix of identical uncommitted component cells for system logic hierarchy, surrounded by peripheral cells for linear and interface functions. All ULAs are based on Ferranti advanced bipolar LSI process (FAB-2).

System hardware is based on the DEC PDP-11/23 minicomputer, supported by the RSX-11/M operating system. The minicomputer unit contains two exchangeable RL01 5M-byte hard disks. One holds the operating and communication systems; the other the ULA software and libraries. The ULA Designer uses DECnet software to communicate with the host computer over voice grade telephone lines.

Control console is an LA34 DECwriter, a microprocessor-driven desktop dot (continued on page 39)



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DO printer family.

oriented control panel customization.

GE 3000's achieve real breakthroughs in paper handling. An exclusive self-threading configuration makes paper loading a snap. Paper is held in a unique four point push-pull paper capture design featuring push tractors and pinch rollers making for real stability during printing of high resolution characters and graphics. Tension is maintained across the print line for precise first-to-last multipart paper registration and improved handling of perforation folds.

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but try talking to our competitors. In the GE 3000 series we've combined high configuration flexibility for high application flexibility with extensive design commonality for maximum profitability.

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General Electric. We're the industry leader in electronic printing. We pioneered the industry in the first place.

Barren and State State

The new GE30

NOW, ONE PRINTER SERIES CAN HANDLE VIRTUALLY ALL YOUR APPLICATION NEEDS.

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At last a highly capable OEM printer series with single-design simplicity, without the application limitations of a single-model product line.

SIX BASIC MODELS TO CHOOSE FROM.

The GE 3000 printer family includes three 136 column standard EDP matrix models (GE 3180, GE

3240, and GE 3400) with three different speed ranges starting at 180, 240, and 400 cps. Two dual mode 136 column models combine 100 to 198 cps near letter quality printing, (more than double the speed of competitive models) with 240 to 500 cps standard EDP output (GE 3244 and GE 3404). Finally, an 80 column model is available to handle smaller system data processing needs (GE 3181).

STANDARD FEATURES GEARED TO OEM NEEDS.

GE 3000 printers come with a long list of standard features to meet your output printer needs. Standard: Six-part forms capability, built-in tractors, and a close-in tear-off bar to cut forms waste. Standard: Logic-seeking bi-directional printing

Standard: Logic-seeking bi-directional printing with multiple print fonts in 10, 12, 13.1, 16.5 cpi – and expanded double width printing. All with underline and lower case descenders. Plus 72×72 dot/inch graphics capability.

Standard: A 512-character line buffer, built-in fault diagnostics, and a range of serial and parallel interfaces. Local and host selectable configuration parameters are downline loadable and non-volatile. An embedded ten-key membrane control panel for easy application-





SPECIFICATIONS

DATA TRANSMISSION

Code: USASCII/ISO 7 bits, plus optional parity

Interface: Serial RS-232, optional:

Serial RS-449, current loop, parallel

Speed: Serial: 110/300/1200/2400/4800/9600/19,200 baud

Parallel: 100K char./sec.

PRINTING

Type: Matrix Impact

Speed:	-	Characters/Sec. at:			
1		10	12	13.1	16.5
		CPI	CPI	CPI	CPI
GE 3180, 31	81 EDP	180	216	236	297
GE 3240, 32	244 EDP	240	288	314	396
GE 3244	NLQ	120	144	157	198
GE 3400, 34	04 EDP	400	480	500	500 +
GE 3404	NLQ	100	120	125	125 +
Technique: h	oi-direction	al, logic	seeking	Ş	

Head: GE 3180, 3181, 3240: 9-wire

GE 3244 :18 wire, staggered

GE 3400, 3404 :18 wire, parallel

Font: 96 graphics (ASCII/ISO) plus 10 National character sets, plus optional additional character sets.

Character Formation:

	STD	NLQ
10, 12, 13.1	5 of 9 Dots wide	9 Dots wide
ĆPI	9 Dots high	18 Dots high
16.5 CPI	4 of 7 Dots wide	7 Dots wide
	7 Dots high	14 Dots high
Character Spacing	: 5, 6, 6.55, 10, 12, 1	13.1, 16.5 per inch
Line Spacing: 3, 4	, 6, 8 per inch or by	1/144th in.
incr	rements	
Print Line: GE 31	81 8 inch (203 mm)	
All oth	er models 13.6 (345	5mm)
Buffer: 512 chara	cters	
D'11 0 1	$1 - 1/U > (\Box A - 1) ($	10 E

Ribbon: Cartridge, nylon $\frac{1}{2}'' \times 54$ yd. (12.5 mm $\times 49.4$ m) 6×10^{6} character life

Test: Local and remote test and diagnostics

PRINT CONTROL

Margins: Left & right, any position Horizontal Tabs: Absolute (22 positions) or relative Top of Form: Form lengths to 22 in. (559 mm) Vertical Tabs: Absolute (12 positions) or relative Bottom of Form: Any position provides auto-perforation skip over

Auto CR, LF: Avoids loss of received data

PAPER HANDLING

Paper Drive: Dual precision 6-pin, push tractors combined with adjustable pinch feed friction rollers

Paper Width: GE 3181, 2.95 to 10 in. (75 to 254 mm) All other models 2.95 to 15.35 in. (75 to 390 mm)

PRINTER PARAMETERS

Locally Selectable: At the printer Remotely Selectable: By escape (ESC) sequences $(ANSI \times 3.64)$

Retention: By battery-supported memory (multi-year life)

INFORMATION DISPLAY

Displays: Status of printer parameters Diagnostic results and alarms

PHYSICAL

Size: GE 3181: 20w×15.6d×5h in. (508w×396d× 127h mm)

All other models: $24w \times 15.6d \times 5h$ in. ($609w \times 396d \times 127h$ mm)

Weight: GE 3181: 18 lbs. All other models: 20 lbs.

ELECTRICAL

 $\begin{array}{c} \text{Domestic Model: 117 VAC} \ (+10\%-15\%) \ 48-65 \text{Hz} \\ \text{International Model: 110-240 VAC} \ (+10\%-15\%) \\ & 48-65 \text{Hz} \end{array}$

Power: 180 watts

OPERATING ENVIRONMENT

Temperature: $+40^{\circ}$ to $+104^{\circ}$ F ($+4^{\circ}$ to $+40^{\circ}$ C) Humidity: 5 to 95% relative

OPTIONS

Re-inker and carbon film ribbon cartridges Single Sheet Insertion Automatic Sheet Feeder 2, 4, 6, or 8K extended line buffers Dense 144× 144 dot/in graphics International models for each printer

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Fig 1 User's logic diagram. This is key reference base for layout and logic verification routines. It is digitized into ULA Designer system as complete graphical drawing.

matrix printer. It has a typewriter keyboard and a 45-cps processing rate. The interactive graphics terminal is a high resolution raster graphics workstation with a green phosphor screen. Communication is by joystick cursor control and a separate keyboard with full ASCII character set, function keys, and numeric keypad.

The digitizer is mounted on an adjustable stand equipped with an electric lift. It has a 1200- x 900-mm active area and includes a 4-button cursor with 0.1-mm resolution. An incremental drum plotter is optional. It has a 930-mm drawing width, a 0.5-mm increment, and 50-mm/s drawing speed. Connection to the PDP-11/23 is via an RS-232-C interface, with 9600-bps asynchronous operation.

System software provides all the programs necessary for ULA design and verification. These include ULA libraries, layout, logic description, test specification, and communication utilities. The software package is being developed as new ULAs are added. Automatic layout aid programs will be available later this year.

The DECnet-controlled communication link to the ULA host computer at a Ferranti CAD center accesses software programs for layout and design rule checking, logic checking and simulation, automatic layout aids, circuit simulation, high level test language, and test program and schedule verification. Since most of the design work is done by the ULA Designer, the 2400-bps link to the host computer is only required for short time periods.

Four simple steps are carried out by the design engineer at the customer's premises. Enter Logic Diagram is the key reference base for layout and

verification routines (Fig 1). The Design ULA Layout step is accomplished using standard and user-defined functions. When completed, layout data are digitized into the ULA Designer and a check plot is produced. Interactive editing of errors and modifications are performed at the graphics terminal (Fig 2). The Enter Test Schedule step is used both for logic verification and for the production of the final ATE program. It is written in the high level language used by the ULA host computer, entered into the ULA Designer, and a complete syntax check is performed. Finally, Verify Design transmits three main files to the host computer: logic, layout, and test schedule, together with command files requesting logic simulation, layout checks, and test program generation. The results are returned over the link to the ULA Designer for analysis. When the design is complete the user sends instructions to proceed with the mask and prototype manufacture.



Fig 2 ULA layout. Shown on interactive graphics terminal screen is section of ULA layout with metallization tracks superimposed on matrix of cell components. Layout editing is carried out at this terminal. Operator prompts appear at left hand side of screen.

Design timescales from first step to last vary, depending on chip complexity. As an example, verified design for a single 1000-gate ULA LSI circuit is said to take three to four weeks; operational prototypes are available after an additional four to seven weeks.

Including operating systems, ULA design utility programs, and two ULA libraries, the ULA Designer is priced at \$99,000. Full training in system management and use is also provided. Availability in the U.S. is scheduled for mid-1982. Ferranti Semiconductors, 87 Modular Ave, Commack, NY 11725.

—Jim Hughes, Senior Editor Circle 245



Here are some of Xentek's 43 varieties of Disk Drive Power Supplies

Whether you use floppy or hard disks, or a combination—or disks with tape drive backup—chances are we've already designed and built the supply that matches your requirements. There are off-the-shelf models for many popular single and multiple 51/4" and 8" floppys, and OEM supplies for 51/4", 8" and 14" Winchesters.

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32-bit superminicomputer ups performance with universal optimizing FORTRAN compiler

apitalizing on its experience in the **J** 32-bit minicomputer field, Perkin-Elmer's Computer Operations has designed the model 3250 to handle complex applications such as scientific research and computation, seismic data acquisition and processing, computer aided design and manufacturing, training simulators, and high performance commercial transaction processing. The system claims to offer unprecedented price/performance in every facet of superminicomputer measurement: system capacity and throughput, processing power, reliability, and accuracy. Prices start at \$150,000.

Using a Whetstone benchmark to measure its ability to execute scientific/

mathematical calculations in a FORTRAN environment, the model 3250 achieves ratings of 3048 single-precision instructions using universal optimization. Universal optimization is supplied by the FORTRAN VII Z compiler, introduced concurrently with the 3250. Capable of optimizing across the complete universe of a FORTRAN program, the compiler supplies increased execution speeds for FORTRAN written applications while supporting the full ANSI language definition of X3.9-1978.

A typical 3250 system includes 2M bytes of memory, terminal console, 80M-byte disk, 75-ips, dual-density tape, floating point processor, battery backup, loader storage unit, and 10 communications lines. The system features a modular central processing unit that employs a hierarchical storage scheme. Optimal system performance is derived from three levels of progressively faster storage that are transparently used by the CPU.

A high speed instruction buffer prefetches instructions from cache immediately prior to the CPU's requesting them. Incorporated in the model 3250 is an 8k-byte 4-way set-associative cache with an 85% to 95% hit ratio that interfaces the main memory to the CPU. In effect, cache simulates a faster main memory system by anticipating CPU requests for instructions and data and having that (continued on page 42)



Perkin-Elmer's 3250 features 32-bit parallel architecture with 64-bit arithmetic unit, 32-bit memory paths, and 32-bit data paths that allow parallel processing of data. Its 16M bytes of directly addressable, interleaved memory handle large program storage and realtime processing.

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SYSTEM TECHNOLOGY/GOMPUTERS



Price and performance comparison of several minicomputers based on Whetstone benchmark. Using universal optimization provided by FORTRAN VII Z compiler, 3250 achieves Whetstone ratings of 3038 single-precision instructions.

information available to the processor from its high speed storage. The third level, main storage, directly addresses up to 16M bytes of memory.

Memory size and system throughput can be tailored to the application, and allow for the easy implementation of large complex systems. The system uses state of the art 64k MOS RAM technology, implemented in 1M- and 2M-byte memory modules.

Memory is organized and divided equally into either two or four banks. A 2-bank system can be 1- or 2-way interleaved; a 4-bank system, 1-, 2-, or 4-way interleaved. The system operates whenever possible in quad-word (16-byte) mode. This improves overall throughput by reducing bus overhead.

All memory is connected to the common memory bus which consists of two unidirectional, asynchronous, 32-bit buses. One bus transfers addresses and writes data while the other is used only for reading data. All read/write operations can be performed on up to four full words at a time, using quad-word mode.

The processor has 2k words of fixed control store (ROM) available to implement the standard instruction set. These instructions include a most frequently used subset of commercial instructions, single/double-precision transfer instructions for mixed mode floating point operations, and support of decimal data formats.

Peak system bandwidth is 64M bytes/s. Up to 40M bytes/s of this bandwidth can be used for 1/0. Achieved through technological advancements such as a 64-bit memory bus and a modular approach to expanding throughput, this system capacity provides sufficient reserve bandwidth to keep the processor performing at peak efficiency even under full 1/0 loading. 1/O capacity is attained from the system's MULTIBUS architecture. The system incorporates a multiplexer bus that interfaces medium speed devices, and direct memory access buses to handle high speed devices such as disk drives.

Reliability features enhance system availability and uptime, including full memory error checking and correction and a resilient power supply designed with wide input tolerances. A memory scrubber scans memory independently of the processor to locate and correct memory errors before the location is accessed by system or application programs. Other reliability features include a self-test during which basic memory and processor functions are checked, and a multimedia diagnostics package that includes diagnostic programs for processor, memory, and peripherals with purchase of the operating system.

The system is fully compatible with models 3210 and 3230. Using the company's multitasking OS/32 operating system, the 3250 runs 32-bit software including CAL MACRO, FORTRAN VII, RPG II, BASIC II, COBOL, CORAL 66, Pascal, and the Reliance transaction processing system. Interactive program development facilities for up to 64 concurrent terminal users programming in a mix of high level languages are available under the multiterminal monitor. Also available is the Edition VII Workbench, a standard version of the UNIXTM timesharing environment, which is offered as a fully supported product.

Users gain maximum benefit from the underlying power of the computer system and also from enhanced programmer productivity when they use FORTRAN VII Z. Since inefficient programs are eliminated by the universal optimizing compiler, programmers no longer need concern themselves with that aspect of the task.

Previous optimizing compilers have been limited to optimizing individual modules within a program. Even global optimization was constrained each time there was a call to a subprogram. FORTRAN VII Z, however, applies universal optimization to look across module boundaries, eliminate call overhead, and optimize subprograms in context. This permits the maximum possible runtime performance while maintaining the source level structure of the program as written.

The package eliminates inefficient code. This contributes to programmer productivity in both the development and life cycle maintenance phases of an application system. Self-documenting code can be written in FORTRAN to a greater extent than before. For example, a number of references to SIN (X) can be written out, so system programmer and maintenance programmer can see what is really happening.

Important control structures or algorithms can be centralized in a subprogram under control of a single programmer, preventing problems that occur when such code is spread around a system. The compiler also includes a development facility that enables programs to be compiled at speeds exceeding 3000 lines/min directly into a linkable object code.

(continued on page 46)

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This unique combination of large capacity, 135 tpi, and small size lets you design equipment that's more compact, more efficient, and less expensive to run.

Of course our Micro Floppydisk comes with the kinds of features you'd expect from Sony. Like a rigid

disk shell and sliding metal guard to keep the disk free from damage. Plus fail-safe disk insertion, greater centering accuracy, and a faster rotation speed to give you higher signal quality.

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peed data systems wants to use ns you can-right now."

100K ECL is a real breakthrough for ultra high-speed digital systems. So we've put together a broad-based 100K family, including logic ICs, memories and gate arrays, to bring you all its advantages.

"They're your best bet for upgrading system performance."

Our 100K circuits really have a lot going for them. To begin with, their subnanosecond propagation delays make them faster than any other ECL family. Then, their super high density lets you put almost double the functions in the same space. And, with compensated temperature and voltage for increased stability over the entire operating range, they're much easier to design with and 11Se.

No wonder they're so popular! But impressive specs don't mean a thing if you can't be sure of getting them with every circuit. That's why we've set up a special quality control system to assure standardized specifications.



We even offer burn-in on all 100K parts. And, since the technology is already mature (we've been selling it for more than five years), you can be sure there won't be any more changes in performance characteristics.

"There are plenty of 100K circuits to go round."

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FORTRAN VII programs can run under the timesharing monitor, OS/32 MTM, directly under the OS/32 operating system, or under the Reliance transaction processing environment. The language is generally source level compatible with FORTRAN 77 and UNIX FORTRAN. This permits the program development and source code control system of the UNIX Workbench to be used for large complex programs and to switch to FORTRAN VII for production modules. Price of the package is \$24,950. Perkin-Elmer Corp, Computer Operations, 2 Crescent Pl, Oceanport, NJ 07757. Circle 246

Array processing system extends host performance into supercomputer range

Designed to serve as a tool for scientific problem solving, Sperry Univac's array processing system (APS) supplies both greatly increased arithmetic performance and sufficient bandwidth to sustain that performance over periods of time. These characteristics, demanded by the increasing volume of data and problems within the geophysical area, apply equally well to other applications areas.

The APS, an extension of existing 1100/80 systems, is a high performance scientific processing system that consists of independent functional units. Scalar units (CPUs) are general purpose; input/ output units (IOUs) directly support peripherals and communication devices; and vector/array units (APUs) supply high speed computation on arrays and vectors. Each functional unit connects to and operates directly on large real system memory in a multiprocessing, multiprogramming environment. A maximum configuration consists of four separate scalar and four 1/0 processors working simultaneously to prepare work for the vector/array units.

Each APS consists of two major components: array processor unit and array processor control unit. The APU provides four control and arithmetic pipelines, local scratchpad memory, and supporting registers. Each arithmetic pipeline has one floating point multiplier and two generalized arithmetic and logic units.

Each APU provides one multiply and one addition result every 25 ns. Each pipeline produces a result every 100 ns, for an effective sustainable performance level of up to 80M floating point opera-



APS system architecture has separate logical and physical units for scalar, 1/0 and communications, and vector/array processing. Each function unit is coupled directly to central memory through caches that transfer data to them at high speeds.

tions/s. For each APU, maximum theoretical performance is 120M flops.

The array processor control unit (APCU) functions as a fully associative cache and transparent high speed buffer memory to the central memory. It streams host data to or from the APU at rates of 40M 36-bit words/s. This high data rate between host and APU ensures high sustained performance. High data bandwidths are achieved by integrating the APU with the host by means of the cache buffer memory within the APCU. Buffer memory is 16-way interleaved and is fully associative with central memory. When data are fetched or stored from or to central memory, pages (continued on page 48)



Array processing unit within Sperry Univac's 1100/80-APS contains four parallel arithmetic pipelines, temporary vector scratchpad data memory, 8192-instruction microcode memory, and control/index processors that decode microcode instructions and dynamically configure the four pipelines in each cycle.



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SYSTEM TECHNOLOGY/ COMPUTERS

of 64 words are transferred. This minimizes impact on the host, because main storage needs to be accessed only when the APU requires data not available in the APCU cache.

Organized as 256 64-word pages, the APCU's 16k-word buffer memory supplies operands to the APU pipeline at effective rates of 25 ns/operand. By providing each APU with a transparent view into central memory, the APCU offers an 8M-word address space or real memory problem size for vector operations executing in each APU. Vector/array operations by the APU require no data migration to or from local memory by application or user. In addition, the overhead associated with data migration over 1/0 channels is eliminated, making short vector/array operations more attractive.

Users operating in the host complex can directly access each APS. Programs can execute in batch mode, from remote terminals, or from interactive terminals in timesharing environments. Migration of existing applications written in FORTRAN for execution on scalar computer systems is provided by the APS FORTRAN vector to array syntax translator (VAST).

Submitted as source code to the vector translator, the user application is analyzed, restructured to vectorize certain scalar constructs within DO loops, and translated automatically to an intermediate FORTRAN code that contains statements necessary to access APS pipelines for vector operations. Use of the translator requires no changes to the FORTRAN source code.

A fully loaded 1100/80 with 8M-byte memory and array processing system carries a purchase price of approximately \$10M. The design performance rating for this system is 250M flops. This can be compared to the CRAY-1 with 1M memory which performs 160M flops at the same approximate price, and the \$16M CDC 205 which has 4M memory and can do 200M flops in native mode. Sperry Univac, Div of Sperry Corp, 6700 W Loop S, Suite 500, Bellaire, TX 77401.

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SYSTEM TECHNOLOGY/GOMPUTERS

Updated 16-bit processor improves performance at lower cost



Model 4/11 processor from Computer Automation

To benefit from advances in design and process technology, the LSI 4/10 16-bit processor from Computer Automation has been revamped to increase its performance while reducing its cost. The improved version, the LSI 4/11, now offers such capabilities as floating point arithmetic and double-register shifts, which were previously available only with the company's more expensive processors.

Updated architecture is compatible with the company's other processors. LSI 4/11 uses a proprietary bus, and will run current operating systems, assemblers, and high level languages as well as software developed on older systems. Power supplies, chassis, memories, and 1/0 devices are also compatible; systems can be upgraded further without losing compatibility with presently used software and peripherals.

Still retaining the half-card format of its predecessor, the processor has 128k bytes of RAM, and sockets for up to 16k bytes of onboard EPROM with direct memory addressing of either 128k bytes or 64k words of data. It also retains eight registers of the original that include four general purpose accumulators (of which two can be used as index registers), two stack registers, a program counter, and a status register. Six levels of priority vectored interrupts are also supported that include; realtime clock, console and four program-selectable 1/O interrupt levels.

Also offered are 10 addressing modes to effectively manage the 128k bytes of memory capacity such as absolute, relative, and indirect, all in several combinations with indexing. Input and output modes are selectable from direct and



Model 4/10 and 4/11 performance comparison

interrupt, programmed to automatic word and byte operations as well as direct memory access. Other standard features retained from its predecessor are power fail, automatic restart and realtime clock capabilities.

Redesign of the 2-chip architecture makes possible execution in hardware of such instructions as floating point operations that were formerly emulated only in software. The basic instruction set that included 89 operations, such as register to register, bit manipulation. and conditional jumps, has now been expanded to 123 instructions that include multiple-word memory reference, single register and double register shifts, and floating point arithmetic. Such capabilities now enable the processor to handle such high performance, multitasking applications as industrial control, data communications systems, and development systems.

The processor's expanded instruction set also reduces instruction cycle time to nearly half the 750 ns now possible with a 4/10, an improvement attributed to the redesign of the ALU. With the older processor, separate instruction cycle times were needed for ALU and non-ALU operations. The new processor now has a single instruction cycle time with ALU operations executed as quickly as the others. Other improvements include reducing the length of critical paths within the processor and the use of $5-\mu$, silicon-gate NMOS with thinner oxides and smaller line width.

Memory access speeds have also been reduced up to 20% with memory now included onboard. Formerly with memory located on another board, many memory operations were transmitted over the memory bus. Locating the memory with the processor reduces bus overhead.

Although the four distributed 1/0 channels were eliminated on the newer processor to make room for the expanded memory capacity, a high performance 1/0 card is planned as an option. The option card will be microprocessor controlled to offload 1/0 functions from the host processor. An onboard microprocessor also leaves open the possibility of being able to use third-party software while protecting proprietary software, a move the company claims is necessary to take advantage of software now available for many popular 8- and 16-bit microprocessors. The model 4/11 sells for \$1600 with 128k-byte parity. Computer Automation, 18651 Von Karman, Irvine, CA 92713. Circle 248

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Propagation delay of 2000- and 1000-gate logic arrays is 1 ns

Map of TAT020 STL logic array. Array includes 121 cells organized 11 x 11, 2000 auto-routable gates, 120 buffers, 120 inputs (max) and 60 outputs (max). There are 120 signal and 8 power bond pad locations.

arger, denser, and faster than their previous logic arrays, Texas Instruments' latest Schottky transistor logic (STL) gate arrays are designated TAT020 and TAT010. TAT020 has a gross gate count of 2420, 2000 auto-routable gates, and 120 TTL input buffers (see the Figure). TAT010 specifications include a 1280 gross gate count, 1000 autoroutable gates, and 88 TTL input buffers. The arrays were introduced about a year after the introduction of the company's TAT004 and TAT008 STL arrays. Comparing the TAT020 to the TAT008 reveals notable performance improvement. For example, TAT008 with 800 routable gates is implemented in a 66k-mil² chip yielding a gate density/chip length of 1, while TAT020 is implemented in a 60k-mil² chip with a gate density/chip

length of 2.7. The interconnect delay per average stage on the TAT008 is 1.5 ns; the TAT020 delay at 0.37 ns is much faster.

TAT020 provides 60 TTL output buffers with an 8-mA sink and 36 or less with a 24-mA sink. The TAT010 provides 44 TTL output buffers with an 8-mA sink and 19 or less with a 24-mA sink. Performance specifications for both arrays are the same. Propagation delay is typically 1 ns per internal gate, 1.5 ns per TTL input buffer, and 3 ns per output buffer. Power dissipation is 350 μ W per internal gate, 4 μ W per input buffer, 4 μ W per 8-mA sink output buffer, and 8 μ W per 24-mA sink output buffer. Power dissipation for an entire array is 1.5 W static and 2.5 W dynamic for the TAT020; 1 W static and 2 W dynamic for the TAT010.

According to the company, system design in the '80s will be driven by four needs-high performance, high density, low power, and reduced costs. STL gate arrays are most suitable for high performance and high density applications. In the past, high performance arrays have been fabricated in ECL, taking advantage of that technology's high gate speed. In the future, ECL density will be limited by its power density and ECL packaging will be more expensive than STL arrays, due to cooling requirements. For example, a 40,000-gate system implemented in ECL would dissipate 220 W; in STL, power dissipation would be 24 W. The onchip logic stage delay for the ECL arrays would be 0.65 ns, and 1.3 ns for the STL arrays. Also, the STL system could be implemented in 20 packages while present ECL technology would require 40 packages.

Advanced STL arrays are designed to meet high density requirements. When compared to silicon gate CMOS, power dissipation per gate is higher with STL, but performance is expected to be faster. In speed or drive critical applications such as CPU data paths, offcard drivers, and peripheral data paths, STL arrays should be well suited. Silicon gate CMOS arrays are planned for terminals, printers, and other implementations where speed is not critical.

Interface logic for the STL arrays is highly flexible. Special drive or loading considerations are not required for 1/Obuffers. Logic can be performed within an 1/O buffer and there are few restrictions on 1/O buffer placement. Power busing structure was designed to reduce the effect of T_{pd} on interconnect capacitance. STL gate structure is also flexible, and collector ties and parallel gates are allowed. Receive capabilities in the structure allow the use of a remote drive. In addition, ECL 10k-interface translator circuits are built in the periphery of the arrays.

The STL array family is supported by the company's design automation system, including automatic layout, simulation, verification, reliability, and testability programs. Typically a customer describes an array's requirements in a hardware description language and the required input and output characteristics in a test description language. Customer design support is available in the company's Houston facility and at regional technology centers.



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SYSTEM TECHNOLOGY/INTEGRATED GIRGUITS

A host of packaging options is available. TAT020 can be packaged in 68-pin plastic and ceramic chip carriers, 84-pin plastic and ceramic chip carriers, and 84-, 108-, and 132-pin grid arrays. TAT010 can be implemented in 40-pin plastic and ceramic DIPs, a 64-pin grid array, 68-pin plastic and ceramic chip carriers, and 84-pin plastic and ceramic chip carriers. Both arrays will be available by mid-year. Texas Instruments Inc, Central Literature Response Center, PO Box 202129, Dallas, TX 75220.

—Douglas Eidsmore, Senior Editor Circle 249



Monolithic chips supply all control functions for switching regulators

Single monolithic chip contains all functions necessary for construction of regulating power supplies, inverters, or switching regulators. Each device includes onchip reference, error amplifier, programmable oscillator, pulse steering flipflop, uncommitted output transistors, high gain comparator, and current limiting and shutdown circuitry.

As its entry into the linear integrated circuits area, Unitrode has announced the UC1524A series pulse width modulators. By redesigning the industry standard 1524 circuit, output voltage increases from 40 to 60 V and output current from 100 to 200 mA.

Devices 1524A, 2524A, and 3524A incorporate on single monolithic chips all control functions necessary for constructing regulating power supply inverters or switching regulators. Each device includes an onchip reference, error amplifier, programmable oscillator, pulse steering flipflop, two uncommitted output transistors, high gain comparator, and current limiting and shutdown circuitry. They can also be used as control elements for high power output applications. Designed for switching regulators of either polarity, transformer coupled dc-dc converters, transformerless voltage doublers, and fixed frequency, PWM polarity converters, dual alternating outputs allow either single-ended or push/pull applications.

A fixed frequency PWM voltage regulator control circuit, the UC1524's regulator operates at a frequency programmed by timing resistor (R_T) and timing capacitor (C_T). The constant charging current established by R_T for C_T results in a linear voltage ramp at C_T . The device also contains an onboard 5-V regulator that serves as a reference, powers the internal control circuitry, and supplies external support functions. This reference voltage is lowered externally by a resistor divider to supply a *(continued on page 61)*



The VTM and VTC series of compact switchers offers constant efficiency to 73% over a broad input range and UL1012 recognition. Ripple regulation provides excellent line transient immunity and superior cross regulation capability. Single outputs (VTM) of 5V, 12V, and 15V priced at \$70.00 (unit quantity); dual outputs of $\pm 12V$ and $\pm 15V$ priced at \$84.00 (unit quantity) at 15W; triple outputs (VTC) of $+5V/\pm12V$, and $+5V/\pm15V$ at 50W priced at \$188.00 (unit quantity). These switchers are being marketed by Semiconductor Circuits, Inc. under an exclusive collaboration with ØETA **ETA Electric Industry** Co., Ltd, Japan.

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SYSTEM TECHNOLOGY/INTEGRATED GIRGUITS

reference within the common-mode range of the error amplifier. A second resistor divider network senses the power supply output to generate a feedback signal to the error amplifier. The amplifier output voltage is compared to the linear voltage ramp at CT, and the resulting modulated voltage out of the high gain comparator is steered to the appropriate output pass transistor by the pulse steering flipflop. Outputs may be applied in a push/pull configuration or paralleled for single-ended applications.

The UC1524 is characterized for operation over the -55 to 125 °C military temperature range. 2524A and 3524A operate from -25 to 85 °C and 0 to 70 °C, respectively. Unitrode Corp, 5 Forbes Rd, Lexington, MA 02173. Circle 250

PERPHERALS

Ergonomic multipage terminal uses parity checking to prevent data contamination



multipage display terminal designed A for user productivity, high throughput, and data integrity, Tandem's 6530 is intended to be an integral part of the company's fault tolerant systems. Terminal is designed for extended use by different operators. Therefore, several ergonomic features were incorporated in the design, allowing users to configure the terminal to meet individual needs. As part of a fault tolerant system the terminal must maintain data integrity. To prevent data contamination, parity checks of data buses, memory, and communications lines are incorporated.

Operator comfort contributes to a system's performance and productivity. The terminal can be tailored to a user's

comfort through hardware and display adjustments. For example, the monitor tilts and swivels and the detachable keyboard has a palm rest and a 2-position tilt angle. The 15" (38-cm) screen, with large green phosphor characters displayed on a dark contrasting background, also contributes to operator comfort. When combined with a refresh frequency of 60 Hz, the medium persistence phosphor results in a highly readable flicker-free display.

Stroking a CONFIG key brings up a terminal configuration menu. Through this menu the user can change the form of the cursor; set the volume of (or turn off) the bell, and specify the column in which it chimes; set the volume of (or turn off) the key click; and display a dotted line on the screen between the 24th or 25th text lines. In addition, the user can specify whether the current configuration should replace the one in nonvolatile memory, making it the new default configuration. An extended menu is used to select language, mode, full- or half-duplex transmission, and so forth. The display memory supports 300 lines in conversational mode for access to previous screen displays, and 8 pages in block mode for high data throughput.

Several methods of interacting with the host processor are provided. In conversational mode, the terminal interacts with the host on a character by character basis. Display memory is organized as 300 lines by 80 columns wide; 24 lines display at a time, and the screen can be rolled up or down to view all 300 lines. Line 25 of the screen is used by the system to display messages such as terminal status. In block mode, the 6530 transmits and receives blocks of characters, storing 8 pages of 1920 characters in terminal memory and allowing the processor to write to or read from any page of the terminal. In single-page block mode, the terminal supports AM6520 interactive terminal interface (ITI) protocol, allowing it to act as if in conversational mode while connected in a multipoint or synchronous environment.

Seven languages, including U.S ASCII English, Danish/Norwegian, French (both QWERTY and AZERTY formats), German/Austrian, Swedish, Finnish, Spanish, and U.K. English are standard. Language changing is done electronically via the configuration menu; keyboards are available to match. It can operate in many combinations of synchronous or asynchronous modes, in half- or full-duplex, and supports both RS-232-C and current loop interface. A (continued on page 66)

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series of 6530s can be configured in a multipoint environment, either by daisy chaining or through a 6810 peripheral line adapter (PLA). The terminal utilizes Tandem software subsystems, including the vs Block Mode Editor, the EXPAND Network Monitor, and the PATHWAY Transaction Processing System.

The 6530 was designed from the ground up as a component of fault tolerant systems that would maintain data integrity. For example, when it is first turned on, the terminal automatically performs a number of self-test functions to ensure that it is operating reliably. After that, data integrity is continuously monitored by parity checking. There are parity checks on the 32k bytes of RAM, on the Z80 data bus for transfers to and from option cards, on the keyboard interface and, when a character is displayed, on the row buffer display. The 32k bytes of ROM are protected by checksumming. When a parity error is detected, a nonmaskable interrupt is generated and sent to the Z80. The location of the error is then determined and a signal is sent to a beeper and a keyboard LED. If another parity error occurs during the process of executing a parity interrupt, the system freezes.

In single quantities, the terminal is priced at \$3200. Limited quantities are now available and volume shipments are expected mid-year. **Tandem Computers Inc**, 19333 Vallco Pkwy, Cupertino, CA 95014.

—Douglas Eidsmore, Senior Editor Circle 251

Circuit board/software combination lets IBM PC run CP/M software

Baby Blue CPU Plus enables the IBM Personal Computer to run virtually any software that is CP/M-80 compatible. This relieves users from translating existing CP/M programs for use on the system, and permits programs to run faster than when an emulator is used.

A combination of $11" \times 4" \times 0.5"$ (28- x 10- x 1.3-cm) circuit board and software, the device plugs into an existing slot in the IBM chassis. A full Z80B with 64k bytes of 200-ns RAM on the board, it runs the programs and passes the task of communication with external devices to the IBM computer. During normal PC DOS operations, the board acts just like a 64k-byte RAM board. However, when its special software is used, it becomes a second computer within the IBM computer, permitting the system to run programs written to run under the CP/M-80 operating system.

Hardware consists of 64k bytes of dual-ported 200-ns RAM with parity checking and a Z80B microprocessor that runs at 4.77 MHz. The software, occupying 1k of memory, consists of a translator that turns what CP/M programs want into what PC DOS needs, and an intelligent converter. The converter can read one or several files from popular 5.25" soft sectored CP/M format disks, determine which are executable, and, while converting to PC DOS format, give executable files a special header that activates the Z80B CPU.

The added header consists of two parts: instructions to be executed by the 8088 and the translator used by the Z80B. A converted CP/M program stored on disk is identical to a PC DOS file and loads into memory the same way, differing only when the 8088 starts to run the program.

Execution begins with the header's 8088 instructions, which cause the 8088 to move the translator and CP/M program from its memory into the 64k space available on the Baby Blue board. The Z80B runs the CP/M program while the 8088 handles I/O for the system peripherals. When a system call is encountered, it is passed to the translator where it is converted for use by the 8088. It is then passed to the 8088, which handles the request. Normal PC DOS operation resumes when the CP/M program is completed.

Although the \$600 device can be used with 32k or 48k systems, a minimum of 64k is recommended. Program execution times with the device compare favorably with those of native CP/M systems, since the Z80B runs at 4.77 MHz while most CP/M systems run at 4 MHz. 1/0 operations may show greater speed gains as the 8088 handles peripherals while the Z80B does the processing. **Xedex Corp**, 645 Madison Ave, New York, NY 10022. Circle 252

Task oriented CAD system supplies PCB design and production tools

PC-800 Model 3 is a task oriented CAD system that concentrates on those activity areas that benefit most from computer power. By focusing on these areas, Gerber Scientific has put together a system that covers the entire design to manufacturing cycle. The unit consists of design console with 19" (48-cm) color graphics display, 20M-byte Winchester disk drive, and onscreen design software. Configuration options include high precision photoplotters, 42" x 60" (107- x 152-cm) coordinate digitizer, and various output devices.

Designers can display on command up to eight levels of data in seven colors with the system. Layers can be differentiated simultaneously for designing multilayer boards; each layer can also be displayed separately to verify design decisions. A 16-bit minicomputer with 64k bytes of memory controls all functions and data manipulation. Designers can enter line widths, pad sizes, and other parameters through the ASCII or system keyboard. Symbols can be called from the symbol library with a function key.

Task oriented software permits manipulation of onscreen graphics. Traces can be routed from one level to another. Designers can pan the design, zoom in, and magnify elements. Selected elements can be easily removed without affecting the rest of the data base.

The disk stores utility data, such as applications programs, tables, and the symbol library. Designs are built using the Winchester drive, then transferred to a floppy disk for archival storage. From a common data base, the system can automatically generate artwork masters. solder masks, pad masters, silk screen masters, component drawings, parts lists, and bills of materials. It can also produce production tapes for NC drill machines, as well as tapes for automatic component insertion and sequencer machines. The overall effect is reduced turnaround time and increased productivity.

Software supplied with the system includes digitize/edit for data entry onto job disk, symbol librarian for storing symbols, component manager for producing support documentation, plot/ verify for transferring data to output devices, and plot at width for generating scaled plots to check spacing.

Model 390 RS-232-C communications interface provides communications between the unit and a host computer. This interface also links the graphics system to peripherals including plotters and other computer systems. Price of the system is \$45,000. Gerber Scientific Instrument Co, PO Box 305, Hartford, CT 06101. Circle 253

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See us at ELECTRO, Booth Nos. 2334/2336 See us at NCC, Booth Nos. 3439/3440 Handheld terminal contains auto-dial modem



A handheld, full ASCII terminal with built-in modem from IXO has been designed to access remote data bases. The terminal, Telecomputer, weighs 13 oz (369 gm) and comes with a modular phone cord, allowing it to be plugged into the telephone system from just about anywhere. A 16-character 5- x 7-dot matrix LCD, the display has four additional annunciators: on line, on hold, lower case, and low battery. Display memory holds 80 characters that can be scrolled back and forth.

The terminal contains a 1k x 4-bit CMOS RAM memory that uses a Polaroid Polapulse battery for backup. When the unit connects to the telephone system, it draws power from the phone line. CMOS memory stores items such as user's name, local password, telephone numbers, and log-on protocols for access to computer systems.

Use of the I/O Access Center is a service provided with the Telecomputer. The Access Center is a computer that stores user and warranty information, and downloads password and protocol data into the CMOS RAM of the terminal. Dow Jones accounts, The Source, and Compuserve are currently available protocols. For private accounts, protocols can also be stored in user files at the Access Center. Thus, once the proper protocols and telephone numbers are downloaded into the terminal's memory, log-on can be accomplished with a single keystroke. The user selects that option and the terminal auto-dials. When the remote host answers, the terminal automatically sends the proper protocols, access codes, and passwords.

In addition, the Access Center is used to download the local password lock, ensuring that unauthorized persons cannot use the individual terminal without the proper password. Each authorized user's name is stored in RAM. A machine readable ID number and an access encryption algorithm are additional security features. Depending on protocol size, the memory can generally hold from 8 to 10 access protocols.

Access options are presented to the user in sequence after password verification; dialing is initiated as soon as the YES key is pressed for the option selected. If a stored option is not selected, MANUAL ACCESS? is offered. The user can then enter a telephone number that will be auto-dialed and stored as the manual access number. Any protocols or passwords under manual access must be entered from the keyboard.

Several dialing algorithms are supported. The dialer will switch to pulse mode if there is still a dial tone present after two DTMF digits are dialed, or the unit will go online, bypassing dialing if it detects the presence of a modem carrier. The modem is Bell 103 compatible, originate only, direct connect, and at a fixed -9 dBm transmit level.

The terminal is supplied with a serial peripheral port, in the form of a mini jack that allows various peripheral devices provided by the manufacturer to be attached. These include an acoustic modem, a 20-column thermal printer, a video interface, and an RS-232 interface. The RS-232 interface allows connection of standard serial peripherals such as printers and terminals; it is asynchronous and handles ASCII data at 300 baud. The video interface is capable of displaying sixteen 32-character lines and has automatic wraparound and scrolling. IXO Industries, 6041 Bristol Pkwy, Culver City, CA 90230. Circle 254

DATA COMMUNICATIONS





E nlarging the capabilities of a company's internal telephone network to handle local data communications, the DCS-2 data carrier system by Teltone Corp provides a means to connect remote terminals and centralized data processing equipment without acoustic couplers or modems. Peripherals such as video displays, word processors, and printers can be placed wherever a telephone is located, without tying up the telephone solely for data transmission.

The single-wire pairs in many private automated branch exchange (PABX) telephone systems can double as full-

duplex asynchronous data links with simultaneous voice and data transmission. Appearing as dedicated circuits to data processing equipment, separate data channels are created by using high frequency carrier techniques. An M-821 station unit located next to a telephone connects a terminal anywhere within 5000 cable feet of a PABX wire center or computer room, and transmits RS-232 compatible data at speeds up to 9600 bps (Figure). A full-duplex data channel is established above 4 kHz by the station unit to send data between 36 and 40 kHz and receive data between 72 and 80 kHz. (continued on page 70)

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Fujitsu America Inc. Component Sales Division 910 Sherwood Drive-23, Lake Bluff, Illinois 60044 Phone: 312-295-2610 Telex: 20-6196 TWX: 910-651-2259 An M-831 termination card located at the PABX distribution center separates the derived data channel from the physical voice channel that carries telephone conversations below 4 kHz.

Due to the separation of voice and data transmission, normal telephone and PABX operations, such as ringing and dialing, operate independently of the data carrier system. Data move constantly while the telephone is ringing or in use, and voice transmissions still occur if the data carrier system is shut down. As many data links can be added as there are available wire pairs without losing the use of telephones or decreasing system traffic capacity.

To diagnose data errors, a loopback switch is included in the station unit that verifies the data paths between the terminal and station unit, as well as across the PABX wire pair. Data sent by the terminal can be sent back to its receiver section by the station unit without using the PABX wire pair. Any discrepancies between the data sent and received can then be traced to a terminal malfunction. This loopback capability is also used to echo data sent from central DP equipment, back to the termination card to check the integrity of the data path between the station unit and the termination card.

If the distance between a PABX wire center and computer room exceeds several hundred feet, a DCS-2A data carrier system with integral multiplexers can be used to extend the range and reduce channel wiring. Thirty-two asynchronous data channels are compressed to a single 4-wire circuit that extends up to 6400 ' (1951 m) on 24-gauge cable. Standard T1 span line repeaters can extend the range of private 4-wire data networks to include inter-building communications. Range of the repeaters is further increased by using a telephone company's TI digital carrier line or a microwave radio T1 link for inter-city service.

Because the M-835 time division channel multiplexers are transparent to data, different data rates and protocols can be run on each channel without manual adjustments or an external controller. No external modems or line drivers are needed because the TI driver and receiver circuits are built into the multiplexer. Maximum data rate for the DCS-2A system is 7200 bps for all ports simultaneously with a high speed composite rate of 1.544M bps.

These data carrier systems can be expanded from as few as two (16 channels for the DCS-2A) to as many as 256 data channels, and usually require only the addition of station units and termination cards. Terminal relocations are also readily handled. Terminal and station unit need only be unplugged, moved to the new location, and plugged into the existing telephone. Station unit uses a standard modular telephone cord to connect the terminal in series between the telephone and PABX wire pair, and is powered from any 117-Vac standard outlet. Relocation ends with moving four jumper wires at the PABX distribution frame. If a company moves to another location, the data carrier system can be disconnected and reinstalled at the new site.



Teltone DCS-2 mini file has integral power supply to handle up to four 2-channel termination cards. Station unit is shown at lower right.

Both data carrier systems have FCC part 68 registration that ensure plug-in connection with any leased or privately owned PABX telephone system. A complete 2-channel system costs about \$1500 for a card file, 2-channel termination card, and two station units (Photo). A complete 8-channel system is priced at \$474 per channel. For a typical 32-channel system, the DCS-2A with channel multiplexers is priced at \$573 per channel. The RJ71C jack providing the interface to the PABX system can be ordered from the vendor that provides the PABX services. Teltone Corp, 10801-120th Ave NE, Kirkland, WA 98033. Circle 255



 INNOVATIVE DATA TECHNOLOGY

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CIRCLE 44

The key to greater PCB The right test strategy



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Media translator converts flexible disks, magnetic/paper tapes without retyping



To reduce the cost of converting from 5.25" and 8" flexible disks, magnetic tapes, or paper tapes to other media formats, the TransMedia 500 media translation system from Applied Data Communications provides offline processing without the need to retype, proofread, and correct data. The system accepts media prepared on one system, and reformats data to be suitable for use on a second system. Its flexibility in handling over 35 different word and data processing media formats makes the system suitable for applications such as word processing to phototypesetting conversion, spooling of disks onto magnetic tape for input into a large scale CPU, and creating disks from magnetic tape records for remote distribution.

In order to read and write a wide variety of formats, the system is designed to handle 1- or 2-sided flexible disks, single or double density, with hard or soft sectored, single 5.25" and 8" flexible disk drives. It can also be configured to read and write to a 9-track magnetic tape or communicate over a local TTY connection.

While the company supplies complete turnkey systems with both software and

hardware, users can program the system to meet special requirements. The software is written in an extended version of BASIC with enhanced string operations that provide greater efficiency in transla-



Transmedia 500 media translation system from Applied Data Communications

tion. Device formats can be independently defined for input in one format and output in another.

Using extended file definition capabilities of the BASIC interpreter, entire disks then can be treated as a single file with the system defining such structures as the blocking factor—whether track or sector—and the relative positions to any sector within the disk. File directory structures of popular media formats are already defined in the system, with special file directories created by the user. Thus, the user need only specify the proper input and output formats, and the system converts the data so that the process is transparent to the user.

Data conversion is handled the same way. Character strings, such as typesetting codes, can be defined using BASIC commands for both input and output formats. As the file is translated, these strings will be converted as already defined. Thus, errors that can occur during manual conversion of media retyping, proofreading, and correcting can be eliminated, as well as the associated time required to perform these tasks.





Auscom, Inc. introduces a whole new array of IBM-related capabilities. If you've had problems integrating other systems to your IBM mainframe, Auscom's Model 8900 IBM Channel Interface Module and Model 8911 Programmable Channel Interface can supply the solutions. The 8900 and 8911 provide cost-effective means of interfacing in the areas of networking, exotic peripherals, telecommunications, CPU-to-CPU adaptors, and custom interfaces.

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For further information on the Auscom IBM to Anything Interfaces, contact:



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CIRCLE 46

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SYSTEM TECHNOLOGY DATA GOMMUNIGATIONS

Since media translation occurs offline, the system does not tie up word and data processing equipment during conversion. Data communication devices such as modems or dedicated phone lines are not needed, which eliminates the possibility of errors caused during transmission.

The system includes an enhanced 8080A based microcomputer system with interface support for a variety of 5.25" and 8" flexible disk drives, magnetic tapes, paper tapes, asynchronous communications, as well as printers. A single CRT (24 lines x 80 characters) is included with the system. A menu-oriented display guides an operator through the operation to reduce errors and simplify training.

Prices start at \$15,900 for a direct frontend configuration to phototypesetting equipment, to \$28,000 for a system that includes magnetic tape. **Applied Data Communications**, 14272 Chambers Rd, Tustin, CA 92680. Circle 256

INTERFACE

Parallel port connects host computer with power and analog control system

ntended for applications that require a computer to monitor power and analog interfaces, the parallel addressable multiplexer family from Opto 22 attaches to a parallel port of the host computer to control up to 512 power control devices. as well as a maximum of 48 analog input and eight analog output devices on the same bus. A single 50-conductor daisy chain cable allows up to 16 PAMUX II stations to be addressed for digitally controlled power interface, or 16 ADAM I stations to be addressed for analog control and monitoring. A common bus allows PAMUX II and ADAM I stations to be connected in any combination up to 16 stations.

Since PAMUX II and ADAM I are mounted externally to the host computer, logic functions are isolated from power fluctuations that occur in an industrial environment. High voltage input/output and control can then be handled by single-board computers because PAMUX II stations also serve as termination points for high voltage lines.

A PAMUX II mounting rack accommodates the parallel addressable logic and (continued on page 78)

C is better than ever. Whitesmiths, Ltd. is now shipping Release 2.1 of our highly acclaimed C Compilers for ten different operating system families on four architectures: LSI-11, PDP-11: 8080, 8085, Z80: **RT-11** CP/M. CDOS RSX-11M. RSTS/E. IAS ISIS-II* Idris/R11, UNIX Idris/B80 **VAX-11**: MC68000: **VERSAdos** VMS Idris/S68k **UNIX/32**

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up to eight high density power modules with a total of 32 power input/output functions. With additional PAMUX II stations also individually addressable by eight high density power modules, up to 16 stations can be multiplexed on a single PAMUX II bus for a total of 512 addressable control points.

The PAMUX II bus consists of a 6-bit address field, followed by a switchselectable 8- or 16-bit data field and a 3-bit control field. The first four bits of the address field give the individual addresses of up to 16 stations, and the remaining two bits act as steering bits for data transfer of the specified 8- or 16-bit data field. Data transfer is bidirectional for control (output) or monitoring (input). A switch on the PAMUX II mounting rack determines the size of the data field to be compatible with any 8- or 16-bit computer. Control bits direct the action to be taken such as a write output transfer or read input transfer. In addition, a watchdog timer monitors the bus for periodic activity on the read and write control lines with a switch-selectable option that either resets all output functions, or sets an external flag in case the watchdog timer malfunctions.

Each high density power module controls four power interface functions of



PAMUX II parallel address multiplexer from Opto 22



ADAM I analog-digital-analog multiplexer from Opto 22

the same type. Each individually addressable ac power input or output module can be 120 or 240 Vac, and dc power modules can be 60 Vdc on output or 10 to 32 Vdc on input. The dc power modules can also handle ac inputs and outputs from 15 to 32 Vac, and ac power modules can handle dc inputs and outputs of either 95 to 150 Vdc or 200 to 300 Vdc.

ADAM I analog-digital-analog multiplexer provides a major expansion of the parallel bus also used by PAMUX II. Analog input is available with 8, 24, or 48 channels that can be unipolar or bipolar. Voltage range is selectable from 0 to 5 V, 0 to 10 V, ± 2.5 V, ± 5.0 V, and ± 10 V. Analog input channels are read individually. Host computer establishes the specific input channel address, issues the convert command, and reads the digital representation of the analog input. Analog output is available in either 2, 4, or 8 channels and has a unipolar output of 0 to 5 V or optionally as 1 to 10 V full-scale. Analog output channels can be updated per channel, or all channels can be simultaneously updated with one transfer command. Host computer first establishes the specific output channel address, follows with one or two data transfers depending on 8- or 16-bit word size, then issues the transfer command for singlechannel update. The host computer can also establish new data for any or all channels before issuing the transfer command.

Because of compatibility with the company's analog signal conditioning products, the ADAM I can use plug-in modules to provide signal conditioning on a per channel basis. One such module provides current to voltage conversion for 0 to 20 mA or 0 to 50 mA dc, as well as voltage to voltage conversion up to ± 10 V at unity gain for input to ADAM I. Another module converts voltage to current at 0 to 20 mA or 0 to 50 mA dc, as well as voltage to voltage to voltage at unity gain with filtering for output from ADAM I.

A single PAMUX II station is priced at \$295, with the 4-input power modules priced at \$40 each in quantities up to 24 units. An ADAM I system requires an intelligent control board that ranges in price from \$500 for 8-channel A-D capability up to \$1110 for 48 A-D channels and 8 D-A channels, satellite boards that can handle 8 or 24 input prices at \$105 and \$170 each, and individual analog modules that cost \$20 each in quantities of 10 to 24 units. **Opto 22**, 15461 Springdale St, Huntington Beach, CA 92649. Circle 257

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1982 National Computer Conference

Astrodomain Houston, Texas June 7 to 10



Russell K. Brown Conference Chairman





Howard L. Morgan Program Chairman

James E. Olson Keynote Speaker

"Advancing Professionalism" is the theme of the 1982 National Computer Conference, which will take place June 7 to 10 at the Astrodomain complex, Houston, Texas. Sponsored by the American Federation of Information Processing Societies (AFIPS), Association for Computing Machinery, Data Processing Management Association, IEEE Computer Society, and Society for Computer Simulation, the convention will host over 650 exhibitors displaying the latest developments in computer hardware, software, and services. Exhibition hours will be Monday, 11 am to 7 pm; Tuesday and Wednesday, 10 am to 6 pm; and Thursday, 10 am to 5 pm.

Technical Program sessions will offer a variety of presentations in eight major program tracks. Language and database processing, hardware/ computer architecture, personal computing, social and organizational implications, software engineering, management issues/decision support systems, applications of computing, and office systems will each be introduced in a state of the art review by a leading professional. (See pp 84-86.) Sessions are scheduled on Monday, 1:45 to 3:15 pm and 3:30 to 5:30 pm; Tuesday and Wednesday, 8:30 to 10 am, 10:15 to 11:45 am, 1:45 to 3:15 pm, and 3:30 to 5:30 pm; and Thursday, 8:30 to 10 am, 10:15 to 11:45 am, and 1:45 to 3:15 pm.

Professional Development Seminars will take place concurrently at the Shamrock Hilton Hotel. The 13 full-day and 4 half-day courses will offer professional enrichment in computer graphics, communications/data security, data management, current issues in new technology, and general topics. (See p 87.) Full-day sessions will meet from 9 am to 4:30 pm; half-day sessions from 1:30 to 4:30 pm. Separate registration through AFIPS, limited to 100 attendees per session, is required; a fee of \$60 (full-day) or \$30 (half-day) also gains admittance to the exhibition floor at the Astrodomain.

Pioneer Day, Wednesday, June 9, will celebrate the 25th anniversary of the first formula translation compiler. The opening Pioneer Day topic, "The Stored Program Concept," will be examined by people who were directly involved in its development during the 1940s. Next, Jeanne Adams, chairman of the FORTRAN Standards Committee, will conduct a session about "The Early Days of FORTRAN." Panelists will highlight a review of early compiler technology with anecdotes and developments associated with the first FORTRAN compiler. The closing session, "The Institutionalization of FORTRAN," will be chaired by John Backus, leader of the team that developed the first FORTRAN compiler.

An international visitors' lounge near the registration area will provide interpreters, international currency exchange, message center, "friend-finder" minicomputer, and refreshments. Free shuttle buses will operate regularly between major Houston hotels and the Astrodomain complex.

Registration

At-conference registration on Sunday, June 6, 2 to 6 pm, will be followed by an Early Bird Reception at the Astrohall. Fee for the full conference, including Technical Program, exhibits, and hardbound *Conference Proceedings*, is \$95. One-day registration is \$25 for programs and exhibits; \$10 for exhibits only. Fee for four days at exhibits only is \$30. For more information, contact NCC Registration, AFIPS, PO Box 9658, Arlington, VA 22209. Tel: 703/558-3608.

Technical Program Sessions*

Language and Database Processing Tuesday, 8:30 to 10 am

Topics in Database Systems G. Thomas, Kent State Univ

Tuesday, 10:15 to 11:45 am Database Management Systems for Microcomputers F. Maryanski, Digital Equipment Corp

Wednesday, 8:30 to 10 am Intelligent User Assistance for Computer Based Environments T. Kehler, Texas Instruments Inc

Wednesday, 10:15 to 11:45 am What Is Different about Teaching Ada? V. Mall, Ada Joint Program Office

Thursday, 8:30 to 10 am Realtime Applications of Forth E. D. Rather, Forth, Inc

Thursday, 10:15 to 11:45 am Pascal-Easing the Maintenance Burden A. W. Brown, Data Point Corp

Monday, 1:45 to 3:15 pm Research Towards Database Standards J. Swager, Honeywell Inc

Monday, 3:30 to 5:30 pm Machine Intelligence: From the Laboratory to the Cold World A. Borgida, Rutgers Univ

Tuesday, 1:45 to 3:15 pm Database Integration D. McLeod and A. Motro, Univ of Southern California

Tuesday, 3:30 to 5:30 pm Analysis of DBMS B. Yao, Univ of Maryland

Wednesday, 1:45 to 3:15 pm When Will We Be Able to Use Ada? S. J. Lomonaco, Institute of Defense Analyses

Wednesday, 3:30 to 5:30 pm Computerized Dictionaries: Processing Machine Readable Text M. Evens, Illinois Institute of Technology

Thursday, 1:45 to 3:15 pm Distributed Computing R. Filman, Univ of Indiana

*Note: Program sessions are subject to last minute changes

Pioneer Day

Wednesday, 10:15 to 11:45 am The Stored Program Concept N. Stern, Hofstra Univ

Wednesday, 1:45 to 3:15 pm The Early Days of FORTRAN J. Backus, IBM Corp

Wednesday, 3:30 to 5:30 pm The Institutionalization of FORTRAN J. Adams, Chmn, ANSI X3J3

Hardware/Computer Architecture

Tuesday, 10:15 to 11:45 am Innovation in Commercial Architectures: What Have We Learned and Where Are We Going? D. Frailey, Texas Instruments Inc

Wednesday, 8:30 to 10:00 am Microprocessor Systems in CMOS K. Kristie, Motorola, Inc

Wednesday, 10:15 to 11:45 am Distributed 16-Bit Processing B. Patterson, Intel Corp

Thursday, 8:30 to 10 am Software for Realtime Parallel Systems C. Davis, Ballistic Missile Defense Advanced Technology Center

Thursday, 10:15 to 11:45 am Powerful Parallel Systems for Realtime Applications S. I. Kartashev, Univ of Nebraska; and S. P. Kartashev, Dynamic Computer Architecture, Inc

Monday, 1:45 to 3:15 pm Microprogramming and Firmware Engineering S. Davidson, Western Electric Co

Monday, 3:30 to 5:30 pm Commercial Fault Tolerant Computer Architectures J. F. Meyer, Univ of Michigan

Tuesday, 1:45 to 3:15 pm Data File Compatibility for Small Systems D. Minami, DMA Systems

Tuesday, 3:30 to 5:30 pm ANSI/1226-OEM Storage Interface of the '80s R. C. Layer, 3M Co

Wednesday, 1:45 to 3:15 pm Single-Chip Microcomputer Advances C. McClean, Motorola, Inc

Wednesday, 3:30 to 5:30 pm Single-Chip Microcomputer Programming J. Millar, Texas Instruments Inc

Personal Computing

Tuesday, 8:30 to 10 am Local Area Nets H. Dreifus, Univ of Pennsylvania

Tuesday, 10:15 to 11:45 am Large Volume Software Issues J. W. Brackett, Softech Microsystems Inc

Wednesday, 8:30 to 10 am The Fun and Games Business F. Thorlin, Atari, Inc

Wednesday, 10:15 to 11:45 am User Interface for Personal Workstations (Part 1) P. Heckel, Interactive Systems Consultants

Monday, 1:45 to 3:15 pm Software Environments/Operating Systems A. Irvine, Softech Microsystems Inc

Tuesday, 1:45 to 3:15 pm Personal Computer Industry: The Experts Forecast the Future P. Isaacson, Future Computing, Inc

Tuesday, 3:30 to 5:30 pm Personal Computer Industry Forum P. Isaacson, Future Computing, Inc

Wednesday, 1:45 to 3:15 pm User Interface for Personal Workstations (Part 2) L. Tessler, Apple Computer, Inc

Wednesday, 3:30 to 5:30 pm Small Computers in Large Organizations I. Nesbit, Nesbit Consulting

Social and Organizational Implications

Tuesday, 8:30 to 10 am Improving Job Satisfaction of the Computer Professional A. Hoffman, Consultant

Wednesday, 8:30 to 10 am New Laws in Computing S. Nycum, Gaston Snow & Ely Bartlett

Thursday, 8:30 to 10 am Resiliency of the Information Society R. Turn, California State Univ

Thursday, 10:15 to 11:45 am Vulnerability of the Computer Society L. Hoffman, George Washington Univ Monday, 1:45 to 3:15 pm Encryption, Science, and Secrecy D. Brandin, SRI International; and P. Denning, Purdue Univ

Monday, 3:30 to 5:30 pm Privacy and Security J. M. Nye, Marketing Consultants International, Inc

Thursday, 1:45 to 3:15 pm Small Computer Applications in Criminal Justice S. Kologney, Search Group Inc

Software Engineering

Tuesday, 8:30 to 10 am Effective Software Documentation R. G. MacAuslan, Honeywell Inc

Tuesday, 10:15 to 11:45 am Software Engineering Education D. C. Rhine, Western Illinois Univ

Wednesday, 8:30 to 10 am Software Engineering in the 1990s J. A. Rader, Hughes Aircraft Co

Wednesday, 10:15 to 11:45 am Impact of Ada on Software Engineering G. Booch, U.S. Air Force Academy

Thursday, 8:30 to 10 am Software Engineering Requirements: Definition and Analysis J. W. Winchester, Hughes Aircraft Co

Thursday, 10:15 to 11:45 am Software Quality Assurance Environments and Approaches M. A. Holthouse, The Analytic Sciences Corp

Monday, 1:45 to 3:15 pm Parallel Programming and Parallel Computing for Large Systems J. C. Browne, Univ of Texas, Austin

Monday, 3:30 to 5:30 pm Designing Systems for Performance K. M. Chandy, Univ of Texas, Austin

Tuesday, 1:45 to 3:15 pm Breadboarding/Prototyping of Software Systems J. E. Urban, Univ of Southwestern Louisiana

Tuesday, 3:30 to 5:30 pm Software Development Environments M. S. Deutsch, Hughes Aircraft Co

Wednesday, 1:45 to 3:15 pm Application Generators: Current Use and Future Prospects J. M. Grochow, American Management Systems, Inc

Thursday, 1:45 to 3:15 pm Software Life Cycle B. W. Boehm, TRW Inc

Management Issues/ Decision Support Systems

Tuesday, 8:30 to 10 am Artificial Intelligence and Decision Support Systems A. E. Robinson, SRI International

Wednesday, 8:30 to 10 am Decision Support Systems in Government P. G. W. Keen, Massachusetts Institute of Technology

Wednesday, 10:15 to 11:45 am Organizational and Behavioral Impact of Information Technology C. F. Gibson, Index Systems Inc

Thursday, 8:30 to 10 am Complex Business Systems: A Strategy for Success N. L. Bloom, American Management Systems, Inc

Thursday, 10:15 to 11:45 am Software Maintenance N. Chapin, InfoSci, Inc

Monday, 1:45 to 3:15 pm Decision Support Systems in Medicine J. S. Augenstein, Univ of Miami/Jackson Memorial Hospital Medical Center

Monday, 3:30 to 5:30 pm Programmer Productivity L. Webber, Peat, Marwick and Mitchell

Tuesday, 1:45 to 3:15 pm Tutorial for Decision Support Systems A. Napier, Univ of Houston

Wednesday, 1:45 to 3:15 pm Management of Computer Resources T. Johnson, Nolan, Norton and Co

Wednesday, 3:30 to 5:30 pm Concepts and Practice of Measurement in an MIS R. Mason, Univ of Southern California

Thursday, 1:45 to 3:15 pm Computer Assisted Decision Rooms P. Gray, Southern Methodist Univ

Applications of Computing

Tuesday, 10:15 to 11:45 am Computer Graphics Applications S. Gnanamgari, Siemens Corp

Wednesday, 8:30 to 10 am Computing Applications R. C. Gammill, North Dakota State Univ

Thursday 8:30 to 10 am CAD/CAM Applications and Development A. Smith, Atlantic Richfield Co Monday, 3:30 to 5:30 pm Direction in Library Applications D. Penniman, OCLC Inc

Tuesday, 1:45 to 3:15 pm Distributed Processing Approaches R. Billings, Billings Computer Corp

Tuesday, 3:30 to 5:30 pm Network Management Issues R. Shatzer, Sytek, Inc

Wednesday, 3:30 to 5:30 pm Interconnecting Our Automated Offices J. McQuillan, BBN Information Management Corp

Office Systems

Tuesday, 8:30 to 10 am Management and Professional Workstations E. S. Wilkes, Arthur Anderson and Co

Tuesday, 10:15 to 11:45 am Strategic Planning for Office Automation H. Morgan, Univ of Pennsylvania

Wednesday, 10:15 to 11:45 am Local Area Networks: How Broad is Broad Enough? D. Kutnick, The Yankee Group

Thursday, 8:30 to 10 am Advanced Technologies for the Office C. Mueller-Schloer, Siemens Corp

Thursday, 10:15 to 11:45 am Electronic Mail W. Ulrich, Ulrich and Assocs

Monday, 3:30 to 5:30 pm Combining Image and Data Processing Within the Office D. C. Zatyko, Zatyko Assocs

Tuesday, 1:45 to 3:15 pm Overview Session: The State of Office Automation A. Wohl, Advanced Office Concepts

Tuesday, 3:30 to 5:30 pm Office Automation and Knowledge Worker Productivity M. Kahn, Honeywell Inc

Wednesday, 1:45 to 3:15 pm User Interface: Help Facilities R. Fenchel, Xerox Corp

Wednesday, 3:30 to 5:30 pm Text Editing Advancements P. Seybold, The Seybold Group

Thursday, 1:45 to 3:15 pm User Interface D. Vaskevitch, Standard Software Ltd

Professional Development Seminars*

Monday

Data Management

Database Management in the '80s (F) J. A. Larson, Honeywell Inc

Current Issues in New Technology Creating Receptivity to Technology (H) G. J. Gery, Gery Assocs

General

The Computer Professional as Expert Witness (H) J. M. Conley and J. J. Marcellino, Gaston Snow & Ely Bartlett

Tuesday

Computer Graphics

Computer Graphics for Management Information Systems: An Overview (F) I. M. Jarett, I. M. Jarett, CPA, Ltd

Communications/Data Security

Regulatory and Legislative Developments and their Implications for Telecommunications and Data Processing (F) M. J. Manning, Hedrick & Lane; and W. Hinchman, Hinchman & Assoc

Data Management

Structured Design (F) N. Chapin, InfoSci, Inc

Current Issues in New Technology

Low Cost Word Processing (H) L. Press, Small Systems Group

*F-Full day, 9 am to 4:30 pm H-Half day, 1:30 to 4:30 pm

Wednesday

Computer Graphics

Implementing Successful Business Graphics Systems (F) A. T. Paller, AUI Data Graphics

Communications/Data Security

Overview and Directions in Local Computer Networks (F) H. A. Freeman, Architecture Technology Corp

Data Management

Data Analysis Techniques (F) R. C. Perkinson, QED Information Sciences, Inc

Current Issues in New Technology

Managing, Controlling, Auditing Minicomputer Systems (F) E. H. Murray, Management Advisory Services

General

Motivating Data Processing Personnel (H) J. D. Couger, Univ of Colorado

Thursday

Computer Graphics

Computer Graphics Design for Effective Communications (F) G. F. McCleary, Jr, Univ of Kansas

Communications/Data Security

Control and Security Issues in System Development (F) A. E. Brill, Yourdon, Inc

Current Issues in New Technology

Human Issues in Designing and Implementing Office Automation Systems (F) L. K. Williams, Consultant

General

Breakthroughs in Strategic Planning and EDP Project Management (F) A. P. Martin, Proactive Management Group, Inc or

Effective Listening (F) L. K. Steil, Communications Development, Inc

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Technical Program Excerpts*

Session M1-1: Microprogramming and Firmware Engineering

Mon 1:45 to 3:15 pm, Rm A

As they are designed into numerous computer systems, microprograms are growing in size as well as diversity; soon the same problems that hinder the efficiency of large programs will beset microprograms. Techniques for developing microcode, analyzing parallelism to increase efficiency, and ensuring firmware reliability will be evaluated in this session.

Chairman: S. Davidson, Western Electric Co

- M1-1/1 "Current Usage of High Level Microprogramming Languages" S. Davidson, Western Electric Co
- M1-1/2 "Firmware Quality Assurance" H. Berg and P. Rao, Honeywell Inc
- M1-1/3 Presentation TBA S. Dasgupt, Univ of Alberta

Session M1-2: Parallel Programming and Parallel Computing for Large Systems

Mon 1:45 to 3:15 pm, Rm C

Parallel programming and parallel processing are key features of high performance computer systems. A survey of the status of parallel structuring in database processing and the results of an experiment in large scale parallel programming will round out discussions on several aspects of this subject.

Chairman: J. C. Browne, Univ of Texas, Austin

- M1-2/1 "Exploiting Parallelism for the Performance Enhancement of Nonnumeric Applications"D. DeWitt and D. Friedland, Univ of Wisconsin
- M1-2/2 "Reconfigurable Network Architectured Computer Systems: An Environment for Parallel Computing"

J. C. Browne, Univ of Texas, Austin

- M1-2/3 "A Systolic Processor for Signal Processing" G. A. Frank, E. M. Greenawalt, and A. V. Kulkarni, ESL Inc
- M1-2/4 "Parallel Processing a Large Scientific Code" R. Hiromoto, Los Alamos National Laboratory
- M1-2/5 "Design of Software for Distributed/ Multiprocessor Systems"
- T. R. McKelvey and D. P. Agrawal, Wayne State Univ M1-2/6 "The Problems of Programming for an
- Architecture with a Large Number of Processors" A. Gottlieb
- M1-2/7 "Some Experiments in Parallel Computing on Large Scale Numeric Problems" B. Buzbee, I. Bucher, and P. Frederickson

*Program sessions are subject to last minute changes

Session M1-3: Software Environments/ Operating Systems

Mon 1:45 to 3:15 pm, Rm 311

Software engineers are calling for a more sophisticated development environment and more complex operating system support for burgeoning microcomputer applications programs. Panelists will relate what software environments can provide today and the needs of application developers, then predict what can be expected in the future.

Chairman: A. Irvine, Softech Microsystems Inc

- Panelists: E. Juliusser, Future Computing Inc; M. R. Posehn, Organic Software Inc; and
 - M. Overgaard, Softech Microsystems Inc

Session M2-1: Commercial Fault Tolerant Computer Architectures

Mon 3:30 to 5:30 pm, Rm A

Speakers will review previous approaches to fault tolerant computing systems in military and space applications, and detail selected architectures developed for fault tolerant commercial computing applications.

Chairman: J. F. Meyer, Univ of Michigan Panelists: J. Bartlett, Tandem Computers, Inc; D. Johnston, Intel Corp; D. Morgan, Digital Equipment Corp; J. Singh, Honeywell Inc; C. Walter, Bendix Advanced Technology Center; and J. H. Wensley, August Systems, Inc

Session M2-2: Designing Systems for Performance

Mon 3:30 to 5:30 pm, Rm 307

In a discussion geared toward practical applications, panelists will suggest tools and techniques for spotting and correcting performance problems early in the design cycle.

Chairman: K. M. Chandy, Univ of Texas, Austin

M2-2/1 "The Use of Performance Models in Systematic Design" K M Chandy J Misra B Berry and D Neu

K. M. Chandy, J. Misra, R. Berry, and D. Neuse, Univ of Texas, Austin

M2-2/2 "Reconfigurable Network Architectured Computer Systems: An Environment for Parallel Computing"

C. U. Smith, Duke Univ; and J. C. Browne, Univ of Texas, Austin

M2-2/3 "Performance Modeling in the Design Process"

W. Alexander and R. Brice, Los Alamos National Laboratory

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M2-2/4 "KIDAS: A Methodology for Designing and Evaluating Large Scale Realtime Systems' E. LeMar, ECA Automation

M2-2/5 "The Research Queuing Package: Past, Present, and Future" C. Sauer, E. MacNair, and R. Kurose, IBM Corp

Session T1-2: Effective Software Documentation

Tues 8:30 to 10 am, Rm C

This session will suggest ways to improve communication between users and writers of software documentation. Speakers will consider what users expect from software documentation and how they can explain their needs to writers; what information writers need to complete successful documentation; and what direction future software documentation may take.

Chairman: R. G. MacAuslan, Honeywell Inc.

- T1-2/1 "Audience Identification for End-User Documentation"
- J. G. Raymond, Michigan Wisconsin Pipe Line Co T1-2/2 "Computer Aided Documentation"
- S. Rosenberg, Riverside Research Computer Center

Session T1-3: Local Area Nets Tues 8:30 to 10 am. Rm 311

Placing the emphasis on applications, participants will explain how to use a local area network, then go on to examine problems involved in installation. Benefits derived from LANS already in operation will be described, and future uses considered.

Chairman: H. Dreifus, Univ of Pennsylvania Panelists: D. Nelson, Apollo Computer Corp:

J. Davidson, Ungermann-Bass Corp; K. Pogran, Bolt Beranek and Newman; and D. Farber, Univ of Delaware

Session T2-1: Innovation in Commercial Architectures: What Have We Learned and Where Are We Going?

Tues 10:15 to 11:45 am, Rm A

Panelists will recount what has been learned from innovative architectural designs recently used in commercial computer products, and look ahead to what may be introduced in the future.

Chairman: D. Frailey, Texas Instruments Inc Panelists: G. Henry, IBM Corp; D. Nelson, Apollo Computer Corp; J. Rattner, Intel Corp; and D. Khandarkar, Digital Equipment Corp

Session T2-3: Large Volume Software Issues Tues 10:15 to 11:45 am, Rm 307

Problems encountered with mass distribution of software will be addressed, such as quality assurance procedures during development, reproduction, and manufacture. Legal protection for software sold to the mass market must also be taken into account.

(continued on page 94)

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CIRCLE 55

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NAME:	Session T2-8: Co Ap Tues 10:15 to 11:4 Speakers will review applications and con independence
CIRCLE 56	Chairman: S. Gnana T2-8/1 "A Microcor

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ckett, Softech Microsystems Inc Irwald, IBM Corp; F. M. Gibbons, ng Corp; C. V. Ray, Jr, Peachtree N. Freed, Powers and Hall

tabase Management stems for Microcomputers

5 am, Rm D

y has changed more than other ransition from mainframe to to microcomputer. The chief mainframe and microcomputer erives from the needs and two user groups. Requirements of database user, and how existing not match them, will be analyzed.

ski, Digital Equipment Corp t. Univ of Minnesota; P. Fisher,

E. Lowenthal, Intel Corp; Database System; and J. Driscoll, orida

mputer Graphics plications

5 am, Rm 311

a range of computer graphics nsider the importance of device

mgari, Siemens Corp

- mputer System for Color Video Picture Processing'
 - Y. Okawa, Gifu Univ
- T2-8/2 "On the Importance and Futility of Device Independence in Computer Graphics" A. Vinberg, Issco

T2-8/3 "Graphic Harmony—Conversations on Color and Computer Graphics" M. Condon, Polaroid Corp

Session T3-1: Data File Compatibility for **Small Computer Systems**

Tues 1:45 to 3:15 pm, Rm A

Cost and inconvenience of file translation make universal data file compatibility especially attractive. Representatives from such fields as operating systems, local area networks, mass storage media, and semiconductor technology will gather to discuss possible solutions to the file compatibility problem.

Chairman: D. Minami, DMA Systems

T3-1 "The 5.25" Fixed/Removable Winchester Disk Drive"

D. Minami, DMS Systems

Panelists: T. Rolander, Digital Research Corp; J. Payne, National Semiconductor; J. Jaworski, Western Digital Corp; and S. Nageshwar, Hewlett-Packard Co

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CIRCLE 58

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Session T3-2: Breadboarding/Prototyping of Software Systems

Tues 1:45 to 3:15 pm, Rm C

Criteria for evaluating breadboarding/prototyping tools and methods used in industry, government, and academia will be set forth, along with suggestions for improving existing techniques.

Chairman: J. E. Urban, Univ of Southwestern Louisiana

Panelists: J. E. Urban, Univ of Southwestern Louisiana; C. G. Davis, Ballistic Missile Defense Advanced Technology Center; C. V. Ramamoorthy, Univ of California, Berkeley; C. R. Vick, Auburn Univ; and S. Zeldin, Higher Order Software Inc

Session T3-3: Personal Computer Industry: The Experts Forecast the Future

Tues 1:45 to 3:15 pm, Rm 311

System elements, peripherals, and software, as well as retailing, international markets/competition, professional workstations, and startup opportunities, will be discussed as a board of computer consultants explores the personal computer market. Other likely topics are portable computers, electronic information distribution, and consumer robots.

Chairman: P. Isaacson, Future Computing, Inc

Panelists: B. M. Rosen, Rosen Research Inc; J. Yates, Gnostic Concepts; B. Meserve, Arthur D. Little, Inc; E. Juliussen, Future Computing, Inc

Session T3-7: Database Integration Tues 1:45 to 3:15 pm, Rm B

Combining several data bases into one integrated data base, and providing complete or partial logical interconnection among a collection of data bases, will be explained. Speakers will review information sharing among users and applications, including database transactions that manipulate information from among several data bases. An open discussion will follow brief remarks from the panel.

- Cochairmen: D. McLeod and A. Motro, Univ of Southern California
- Panelists: D. Heimbigner, D. McLeod, and A. Motro, Univ of Southern California; J. Smith, Computer Corp of America; and H. Wong, Lawrence Berkeley Laboratory

Session T3-8: Distributed Processing Approaches

Tues 1:45 to 3:15 pm, Rm D

Despite their benefits, distributed data processing systems have not been fully implemented—mainly because industry has not organized to establish and manage distributed processing installations. Recent advances in the technology promise to simplify system design, and will be addressed by representatives of leading DDP suppliers.

Chairman: R. Billings, Billings Computer Corp Panelists: D. Rislove, IBM Corp; and A. Schwager, Hewlett-Packard Co

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Session T4-1: ANSI/1226—OEM Storage Interface of the '80s

Tues 3:30 to 5:30 pm, Rm A

ANSI-1226 rigid disk interface will be compared to SMD and floppy interfaces. How future intelligent disk interface standards may impact the rigid disk system and its compatible equipment will be examined.

Chairman: R. C. Layer, 3M Co

Panelists: D. Allen, Sperry Univac; J. Payne, National Semiconductor; M. Shebanow, Advanced Micro Devices; T. Thawley, Interphase Corp; B. Burr, National Bureau of Standards; D. Reiser, Priam; and D. Dennison, зм Co

Session T4-2: Software Development Environments

Tues 3:30 to 5:30 pm, Rm C

Aerospace software engineers will describe automated methods for integrating hardware and software tools into the software development environment.

Chairman: M. S. Deutsch, Hughes Aircraft Co

T4-2/1 "An Industrial Software Engineering Methodology Supported by an Automated Environment "

M. S. Deutsch, Hughes Aircraft Co

T4-2/2 "An Approach to the Definition and Implementation of a Software Development Environment"

J. Elwell, TRW Inc

T4-2/3 "A Jovial Programming Support Environment" E. McMahon, Computer Sciences Corp

Session T4-3: Personal Computer Industry Forum

Tues 3:30 to 5:30 pm, Rm 311

Industry participants will talk about the personal computer business, and share opinions concerning where it stands between computers at large and consumer electronics.

Chairman: P. Isaacson, Future Computing, Inc Panelists: J. Purtell, Jr, Sears, Roebuck and Co; P. D. Estridge, IBM Corp, M. Markkula, Apple Computer, Inc; D. S. Wagman, Softsel; and D. Bricklin, Software Arts, Inc

Session T4-8: Network Management Issues Tues 3:30 to 5:30 pm, Rm 307

This session will provide background information on network monitoring, management, and control, and explain the levels of service required for such functions as statistics gathering, performance evaluation, fault tolerance, and activity profiles.

Chairman: R. Shatzer, Sytek, Inc

Panelists: J. Sanchez, Naval Surface Weapon Center; and P. Lin, Sytek Inc

Session W1-1: Microprocessor Systems in CMOS

Wed 8:30 to 10 am, Rm A

High performance processors, peripherals, memory, and logic functions are now available for complete



CMOS fabrication of MPU systems. Authors will describe the configuration of several such systems.

Chairman: K. Kristie, Motorola, Inc

- W1-1/1 "Practical CMOS Microprocessor Systems" B. Huston, Motorola, Inc
- W1-1/2 "High Performance, Low Power Microprocessor Based Data Acquisition Design" A. Wagner-Korne, National Semiconductor
- W1-1/3 "Distributed Processing Enhances 1800 Series Performance"
- D. Block, RCA W1-1/4 Presentation TBA
 - E. Peatrowsky, Motorola, Inc

Session W1-2: Software Engineering in the 1990s

Wed 8:30 to 10 am, Rm C

Although radical changes in hardware have made predicting the evolution of software engineering risky, four experts in the field will offer their views on what they may face in the next decade.

Chairman: J. A. Rader, Hughes Aircraft Co

Panelists: B. Roehm, TRW Inc; E. Miller, Software Research Assocs; L. Belady, IBM Corp; and B. Balzer, usc Information Sciences Institute

Session W1-4: New Laws in Computing Wed 8:30 to 10 am, Rm 307

Topics in this session will bring attendees up to date on laws affecting the computer industry, and will

include developments in proprietary protection of software, international licensing, and Tax Reform Act opportunities. Discussion of recent disputes between vendors will also be reviewed.

Chairman: S. Nycum, Gaston Snow & Ely Bartlett Panelists: J. J. Marcellino and M. Keplinger

Session W2-1: Distributed 16-Bit Processing Wed 10:15 to 11:45 am, Rm A

Several microcomputer devices and techniques that facilitate distributed processing systems will be covered

Chairman: B. Patterson, Intel Corp

- W2-1/1 "The MC68000 Family and Distributed Processing"
 - J. F. Stockton, Motorola, Inc
- W2-1/2 "Using Operational Standards to Enhance System Performance"
 - L. Kohn, National Semiconductor
- W2-1/3 "Distributed Processing with the z8000 Family"
 - J. Pathakl and R. S. Mateosian, Zilog, Inc
- W2-1/4 "Distributed Processing with IAPX 186 Microprocessor Systems" T. Zingale, Intel Corp
- W2-1/5 "Applications of VLSI Intelligent Peripherals" D. S. Laffitte, Texas Instruments Inc

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Session W2-2: Impact of Ada on Software Engineering

Wed 10:15 to 11:45 am, Rm C

Because Ada comprises many software methodologies, it can improve the clarity, reliability, efficiency, and maintainability of existing software systems. In this session, speakers will address how Ada may influence system development.

Chairman: G. Booch, U.S. Air Force Academy

- W2-2/1 "The Impact of Ada on Software Engineering" K. L. Bowles, Telesoft
- W2-2/2 "The Importance of Ada Programming Support Environments"
 - T. A. Standish, Univ of California
- W2-2/3 "Introducing Ada into an Existing Environment"

R. Mathis, Old Dominion Univ

W2-2/4 "Early Experiences with Ada Tasks" M. Lomuto, Softec, Inc

Session W2-5: Local Area Networks: How Broad Is Broad Enough? Wed 10:15 to 11:45 am. Rm 300

A debate on baseband vs broadband networks will emphasize functional advantages/disadvantages and

emphasize functional advantages/disadvantages an cost considerations. Participants will represent Ethernet, Wangnet, and one other LAN system.

Chairman: D. Kutnick, The Yankee Group

Panelists: Participants, whose names were unavailable at press time, will represent Xerox Corp, Wang Labs, and one other vendor

Session W2-9:The Stored Program Concept Wed 10:15 to 11:45 am, Rm 307

Speakers at this session, each directly involved in the development of the stored program concept in the 1940s, will discuss the origins of that theory.

Chairman: N. Stern, Hofstra Univ

Panelists: P. Eckert, Jr, Sperry Univac; H. H. Goldsteine, Institute for Advanced Study; M. Wickes, Digital Equipment Corp; and R. Clippinger, Consultant

Session W3-1: Single-Chip Microcomputer Advances

Wed 1:45 to 3:15 pm, Rm A

Pivotal innovations in the single-chip microcomputer will be outlined, following the chip's advance into low cost, high performance, and complex/single-function applications.

Chairman: C. McClean, Motorola, Inc

- W3-1/1 "High Performance, High Capacity Single-Chip Microcomputers"
 - E. Peatrowsky, Motorola, Inc
- W3-1/2 "Expanded Single-Chip Principles in Practical Applications"
 - R. Dumse, Rowill
- W3-1/3 "Making the Most of VLSI in Microcomputers" J. Corbin, Texas Instruments Inc

(continued on page 102)

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incoor ris.	۷	g-cm	rpm	mA	g-cm	rpm	mA	g-cm/A	ohm	
FN38-R53N1B	6	300	5200	4750	950	7900	470	70	0.4	
FN38-T53N1B	12	300	5200	2000	1470	6600	220	167	1.3	
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Panelists: T. Harper, National Semiconductor; J. Millar, Texas Instruments Inc; and B. Huston, Motorola, Inc

Session W3-2: Application Generators: **Current Use and Future** Prospects

Wed 1:45 to 3:15 pm, Rm C

Application generators are software development tools that may improve productivity in system design, programming, and maintenance by an order of magnitude. Functions that application generators, program generators, and similar high level system development tools perform will be summarized.

Chairman: J. M. Grochow, American Management Systems, Inc

- W3-2/1 "A Survey of Application Generation Tools" A. F. Cardenas, Univ of California, Los Angeles; and W. P. Grafton, Continental Airlines
- W3-2/2 "Program Generators and Their Effect on Programmer Productivity"
- R. L. Roth, Information and Systems Research, Inc.
- W3-2/3 "Application Generators at IBM" A. M. Goodman, IBM Corp
- W3-2/4 "Application Generators: A Case Study" J. H. Waldrop, Hamilton Brothers Oil Co

Session W3-7: When Will We Be Able to Use Ada?

Wed 1:45 to 3:15 pm, Rm D

A panel of Ada experts will answer questions about when the language will be generally available, what systems will support Ada compilers, and what kinds of programming environments will be called for.

- Chairman: S. J. Lomonaco, Institute of Defense Analyses
- Panelists: K. Bowles, Telesoft and UCSD; R. F. Brender, Digital Equipment Corp; B. M. Brosgol, Intermatics, Inc; G. Fisher, New York Univ; and L. Weissman, Softech, Inc.

Session W3-9: The Early Days of FORTRAN Wed 1:45 to 3:15 pm, Rm 307

Session abstract unavailable at press time

Chairman: J. Backus, IBM Corp

- W3-9/1 "Early Computers and Computing Institutions" J. McPherson, Consultant
- W3-9/2 "Computing prior to FORTRAN" R. Bemmer, Honeywell Inc.
- W3-9/3 "Register Allocation in the FORTRAN I Compiler Development Group" R. Goldberg, IBM Corp
- W3-9/4 "Compiler Techniques Available in 1954" R. Mutt, Computer Sciences Corp
- W3-9/5 "A Technical Review of the Early FORTRAN Compilers"
 - F. Allen, IBM Corp
- W3-9/6 Presentation TBA H. Stern, Consultant

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a subsystem that can arm or trigger another for complex measurement tasks. Interaction also provides more efficient and effective software revision by allowing immediate access to the latest version of source code. And it allows symbolic tracing. This means that both software and hardware designers can interface with the system using the same language used in programming. Or with symbols and names used in diagrams.

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measurement modes. New sequencing and windowing flexibility. And the ability to interface with each other or with software development and emulation subsystems in HP's 64000 Logic Development System.

An analyzer to deal with today's complex software

HP's software analyzer gives you a new overview mode that helps you spot software operations in forbidden areas, locate system bottlenecks, and identify inefficient code. It's a macro view that can lead designers to problem areas quickly. Then, powerful windowing and sequencing let you focus on these trouble spots, virtually anywhere in code, for detailed analysis.

Label:	ADDRESS	8085 Mnemonic	time count	time count
Base:		hex	rel	abs
Map:	ADDR_MAP	ADDR_MAP		6 10
-004	abs 0BB4	37 memory write	1.52 usec	-6.48 usec
-003	MON_TABLE+000C	JMP MON_ENTRY+0000	1.48 usec	-5.00 usec
-002	MON_TABLE+000D	08 memory read	2.00 USEC	-3.00 usec
-001	MON_TABLE+000E	00 memory read	1.40 USEC	-1. JZ usec
trigger	MON_ENTRY+0000	SHLD VBD3	2 00	2 00 11000
+001	MON_ENTRY+0001	D3 memory read	1 49 usec	3 49
+002	MON_ENTRY+0002	os memory read	1 52	5 00
+003	abs OBD3	AD memory write	1 49	6 4R usec
+004	abs 0804	out 10	1.52 usec	8.00 usec
+005	MON_ENTRY+0003	001 10	2 88 usec	10.00 usec
M				HIDE MODE
	h			WIDE MODE Sns/ sample Zus/di
	h			WIDE MODE Snis/ sampli Zus/di
				HIDE MODE Sns/ sample Zus/dir
.M				HIDE MDDE 5ns≠ sampin 2us/din −102 ×*-732 o**795
				HIDE MODE Sns/ sampi, 2us/di -102 x=-732 o*+796
				HIDE HOPE Snav samp in Zus / di -102 x = -732 o = 7732 o = 7732 7.64us
e memory * US: Awast				HIDE MODE Sna/ snapi 2us/di/ x-732 o+r736 0+r736 7.64us (x1) 17:3

Directed syntax softkeys and symbolic tracing make operation fast and simple, even for inexperienced users. And inverse assembly greatly speeds analysis.

New capability in hardware analysis

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Session W4-1: Single-Chip Microcomputer Programming

Wed 3:30 to 5:30 pm, Rm A

Programming considerations are extremely important in the selection and use of a single-chip microcomputer. State of the art instruction sets, addressing modes, and other software aspects will be detailed.

Chairman: J. Millar, Texas Instruments Inc.

- W4-1/1 "Single-Chip Microcomputer Programming" B. Huston, Motorola, Inc
- W4-1/2 "Speak Software and Carry a Strip Chip" M. Shapiro, Texas Instruments Inc

W4-1/3 Presentation TBA R. Perry, Zilog, Inc

Session W4-9: The Institutionalization of FORTRAN

Wed 3:30 to 5:30 pm, Rm 307

Session abstract unavailable at press time

Chairman: J. Adams, Chmn, ANSI X3J3

- W4-9/1 "An Early FORTRAN User Experience" H. S. Bright, Consultant
- W4-9/2 "Early FORTRAN at Livermore" R. A. Hughes, Lawrence Livermore National Laboratory
- W4-9/3 "The Emergence of FORTRAN IV from FORTRAN II" W. Heising, IBM Corp
- W4-9/4 "The History of FORTRAN Standards" M. Greenfield, Honeywell Inc

- W4-9/5 "The Early History of FORTRAN Publications" D. McCracken, Consultant
- W4-9/6 "The Emergence of FORTRAN Load-and-Go Systems"
- C. Davidson, Univ of Wisconsin
- W4-9/7 "Some Nonnumeric Applications of FORTRAN (DYSTAL)"
- J. Sakoda, Brown Univ
- W4-9/8 "The Successors of FORTRAN: Why Does FORTRAN Survive?"
- B. Rosenblatt, Standard Oil of California W4-9/9 Presentation TBA
 - J. Backus, IBM Corp

Session H1-1: Software for Realtime **Parallel Systems**

Thurs 8:30 to 10 am, Rm A

Realtime software for distributed parallel systems that optimizes the reconfiguration of resources can speed computations. Speakers will discuss new functions for distributed operating systems, including fast resolution of reconfiguration conflicts and facilitation of data exchanges between reconfigurable resources.

- Chairman: C. Davis, Ballistic Missile Defense Advanced Technology Center
- H1-1/1 "Distributed Operating System for a Powerful System with Dynamic Architecture"
- S. I. Kartashev, Univ of Nebraska; and
- S. P. Kartashev, Dynamic Computer Architecture, Inc.

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- H1-1/2 "An Approach to Functional Texting of Multimicroprocessors" M. G. Sami and M. Annanatone, Milano Politechnico Instituto
- H1-1/3 "A Methodology for the Development of Special Purpose Functions Architectures" P. B. Berra and R. A. Liuzzi, Syracuse Univ
- H1-1/4 "A Superminicomputer Based on Functionally Distributed Multiprocessors"
 - T. Bandoh et al, Hitachi, Ltd
- H1-1/5 "Applications of SIMD Computers in Signal Processing"
 - D. P. Agrawai, Wayne State Univ
- H1-1/6 "A List Processing Oriented Data Flow Machine Architecture" R. Hasegawa, Musashino Electrical Communication Laboratory

H1-1/7 "Lookahead Networks"

G. J. Lipovski, Univ of Texas, Austin

Session H1-2: Software Engineering Requirements: Definition and Analysis

Thurs 8:30 to 10 am, Rm C

Integrated system requirements engineering depends on careful definition and analysis of software needs, in light of overall system requirements. This is the approach speakers will advocate for the 1980s.

Chairman: J. W. Winchester, Hughes Aircraft Co

- H1-2/1 "Requirements Definition and Its Interface to the SARA Design Methodology for Computer Based Systems"
- J. W. Winchester and G. Estrin, Hughes Aircraft Co
- H1-2/2 "The Role of Requirements Analysis in the System Life Cycle"
 - Y. Yamamoto, Jet Propulsion Laboratory
- H1-2/3 Presentation TBA M. Alford, TRW Inc

Session H1-7: Realtime Applications of Forth Thurs 8:30 to 10 am, Rm D

Forth lends itself to many realtime applications; some, exploiting the language's speed, modularity, interactiveness, and memory efficiency, will be presented in this session.

Chairman: E. D. Rather, Forth, Inc

- H1-7/1 "The Forth Philosophy" K. Harris, Forthright Enterprises
- H1-7/2 "Commercial Applications"
- A. Gravina, Hospital Data Systems H1-7/3 "Forth Realtime Graphic Application"
- R. Johnson, General Electric Co
- H1-7/4 "Forth in Robotics"
- D. Slater, Elicon, Inc
- H1-7/5 "Forth in Communications" J. Weems, Hughes Aircraft Co
- H1-7/6 "Forth Applications in Handheld Computers" D. Colburn, Creative Solutions, Inc
- H1-7/7 "Voice Generation" G. Maresca, Materials Research Corp



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Session H2-1: Powerful Parallel Systems for Realtime Applications

Thurs 10:15 to 11:45 am, Rm A

Architectures for powerful realtime parallel systems will be analyzed, including the organization of flexible and reconfigurable multicomputer networks that compute very fast realtime algorithms and a formal method for finding the best configuration in a distributed supersystem.

Cochairmen: S. I. Kartashev, Univ of Nebraska; and S. P. Kartashev, Dynamic Computer Architecture, Inc.

- Panelists: J. P. Ignizio and C. M. Murphy, Pennsylvania State Univ; and M. G. Sami and M. Annanatone, Milano Politechnico Instituto
- H2-1/1 "Reconfigurable Multicomputer Networks for Very Fast Realtime Applications"

S. I. Kartashev, Univ of Nebraska; S. P. Kartashev, Dynamic Computer Architecture, Inc; and C. Davis, Ballistic Missile Defense Advanced Technology Center

- H2-1/2 "A Supersystem for Satellite Image Processing"
- K. E. Batcher, Goodyear Aerospace Corp
- H2-1/3 "Optimal Design of a Distributed Supersystem"
- D. F. Palmer, General Research Corp
- H2-1/4 "A Modular Approach to Realtime Supersystems"
 - R. Arnold, R. Berg, and J. Thomas, Honeywell Inc

Session H2-2: Software Quality Assurance Environments and Approaches

Thurs 10:15 to 11:45 am, Rm C

Presentations regarding software quality assurance for financial, manufacturing, and computer firms will open a discussion of validation, verification, and certification, in addition to general quality assurance problems and procedures.

- Chairman: M. A. Holthouse, The Analytical Sciences Corp
- H2-2/1 "Computer System Product Quality Assurance"
- J. R. Ryan, Texas Instruments Inc
- H2-2/2 "A Quality Assurance Program for Software Maintenance"
- J. W. Center, MEDTRONICS, Inc
- H2-2/3 "The Independent Role: Verification and Validation, and Compliance Testing" B. Taute, Time Inc
- H2-2/4 "Quality Assurance in a Large Commercial Data Processing Installation"
 - C. W. Lybrook, Information Systems Inc

Session H2-6: Software Maintenance Thurs 10:15 to 11:45 am, Rm B

Methods for handling programs and software systems in the field will be reviewed, as authors compare notes on how to manage software maintenance.

Chairman: N. Chapin, InfoSci, Inc H2-6/1 "What Life? What Cycle?"

- N. Zvegintzov, Consultant
- H2-6/2 "Software Maintenance Objective" N. Chapin, InfoSci, Inc
Session H2-7: Pascal—Easing the Maintenance Burden

Thurs 10:15 to 11:45 am, Rm D

Data and program structuring capabilities, in addition to type and range checking, simplify maintenance of Pascal programs. Speakers will describe several application packages under routine maintenance, and provide statistics for comparing maintenance of similar applications coded in other languages.

- H2-7/1 "A Brief Introduction to Pascal" A. W. Brown, Data Point Corp
- H2-7/2 "Readability—The Prime Factor in Maintaining the Answer"
 - P. Kaczowka, Management Systems Software
- H2-7/3 "Micro-bss Maintenance in the UCSD p-System Environment"
 - T. H. Koteki, Ferox Microsystems, Inc
- H2-7/4 "Advanced System Editor Maintenance— An Example of Programmer Substitution" J. McCormack, Volition Systems
- H2-7/5 "Evolving Integrated Office Productivity Tools"
 - R. W. Peterson, Texas Instruments Inc

Session H3-2: Software Life Cycle Thurs 1:45 to 3:15 pm, Rm A

Panelists from government, industry, and academia will evaluate software productivity investments.

Chairman: B. W. Boehm, TRW Inc

Panelists: B. W. Boehm and R. D. Williams, TRW Inc; J. A. Munson, Systems Development Corp; R. T. Yeh, Univ of Maryland; and L. Druffel, Ada Joint Program Office/U.S. Department of Defense

Session H3-7: Distributed Computing Thurs 1:45 to 3:15 pm, Rm D

Session abstract unavailable at press time

Chairman: R. Filman, Univ of Indiana

- H3-7/1 "Models, Languages, and Heuristics for Distributed Computing"
- Profs Filman and Friedman, Univ of Indiana H3-7/2 "Weakest Environment of Communicating Processes"
 - Z. Chaochen, Academia Sincica
- H3-7/3 "Adaptive Structuring of Distributed Data Bases"
 - K. D. Levin, Univ of Pennsylvania
- H3-7/4 "Distributed Scheduling of Resources on Interconnection Networks" B. Wah and A. Hicks, Purdue Univ

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The exhibition at NCC '82 will include many products of interest to designers of computers, peripherals, and computer based systems. Those products that have not previously been exhibited or covered in our editorial departments are described in the following pages. However, many manufacturers who were unable to meet the deadline for supplying information for these pages will also have innovative products on display.

COMPUTERS

Small business computer family runs UNIX System III and VERSAdos

Series 680TM small business systems range from single-user workstations to large multi-user systems. All systems, fully packaged or board level, are based on the M68000TM 32/16-bit microprocessor and use Intel's MULTIBUS to facilitate peripheral and controller selection. They are supported for Bell Labs' UNIX System III and Motorola's VERSAdos operating system, as well as PRO-IVTM applications software processor.

The 680/10 is a powerful single-user system priced at \$5500 in quantity. Its primary enclosure contains a fully powered 6-slot MULTIBUS chassis and complete 12" (30-cm) intelligent character display system. The display controller is offloaded to a video control subsystem having its own 8085 microprocessor. The system is directly field upgradeable to the 680/20 by replacing the 128k memory board with a 256k memory board. The CPU module contains an 8-MHz M68000 and 32-segment memory management unit with initial program load. A 2k-byte ROM provides startup self-diagnostics for the microprocessor and RAM and a debug monitor that facilitates debugging. Three programmable interval timers are also on the board.

On the asynchronous communications module are 4 asynchronous RS-232-C ports and one parallel (Centronics type) printer port. These are programmable for full- or half-duplex; 5-, 6-, 7-, or 8-bit characters, with 1, $1\frac{1}{2}$, or 2 stop bits; odd, even, or no parity; and data rates from 50 to 19.2k baud.

The 680/20 is a modular integrated workstation that offers additional configuration flexibility. These systems include the same microprocessor and video facilities as the 680/10, but provide 256k bytes of RAM that expands to 512k bytes, and can support 3 additional user workstations and a wider complement of peripherals. For example, up to 20M bytes of hard disk storage can be added. OEM price is less than \$6000.

The system's expandable hardware is managed by Motorola's VERSAdos multitasking, multi-user operating system with dynamic task scheduling and file management system. The system supports up to 128 separate tasks, 32 online terminals in 3 support layers. PRO-IV applications processor software system operates as a task under VERSAdos.

The top of the line 680/40, packaged in 2 std 19" (48-cm) RETMA racks, is suitable for desk or rackmounting. The CPU chassis includes a full-powered 12-slot MULTIBUS MIB with M68000 CPU board, 256k bytes of 200-ns RAM (expandable to 768k bytes), MULTIBUS controller for 4 asynchronous RS-232-C ports and parallel printer port; an SMD Winchester disk controller, and a streaming magnetic tape controller. Also included are two 5.25" double-sided/double-density floppy disk drives with MULTIBUS controller. The mass storage chassis has a 20M-byte Winchester disk and 20M-byte streamer tape drive, and provides space for an additional disk. The system can be expanded to 32 asynchronous RS-232-C ports and 8 parallel ports on 8 MULTIBUS boards. Up to 8 Winchester drives and 2 DMA parallel printers can also be added.

The system's expandable hardware is managed by the industry standard UNIX System III multitasking, multi-user operating system with dynamic task scheduling. To ensure complete software compatiblity, the operating system and the system can support industry standard language processors such as C, CBASIC, Pascal, COBOL, and FORTRAN. Operating as a task under UNIX, PRO-IV eliminates dependence on old hardware architecture, special programming languages, or inadequate operating systems. It allows users to build and maintain applications to specific user requirements without compromise to a standard. All documentation is produced automatically. CIE Systems, 2515 McCabe Way, PO Box 16579, Irvine, CA 92713.



See at Booth A762

Circle 447

Winchester and floppy disk based computers

Series 5200 desk model and series 5300 cabinet model Winchester based computer systems have 64k-byte main memory storage that is expandable to 256k bytes. Basic system 5200 includes CPU, one 1.23M-byte flexible disk drive, CRT, and 24M-byte Winchester drive. A 32M-byte Winchester is also available. Up to 10 CRTs can operate on the system. Basic 5300 features are identical to 5200 and, in addition, offer support for up to 3 32M-byte Winchesters for total capacity of 96M bytes. A variety of matrix and line printers, and char printer for word processing, are available for both systems.

MicroPlus floppy disk minicomputer, with 64k-byte memory, CPU, two 1.23M-byte dual-sided floppy drives, and CRT, uses 2901 bit-slice technology for more comprehensive instruction set. Two additional 1.23M-byte floppy drives can be added for a total capacity of 4.92M bytes. Computer can be expanded to support 8M- or 24M-byte Winchester drives. System can support up to 256k bytes of memory, 20 CRTs, multiple printers, and multiple 64M- and 96M-byte CMD drives. MicroPlus business management system accounting/ financial software is designed specifically for the system. Word processing, and application development and reporting tool (ADART) are also available for MicroPlus.

6400 system upright cabinet model system provides 64M- or 96M-byte fixed/removable rigid disk mass storage, expandable to 768M bytes. Access time is 800 ns, with 200-ns system clock. System can support 20 terminals, and a range of dot matrix, band, and char printers. **Centurion Computer Corp**, 1780 Jay Ell Dr, Richardson, TX 75081.

See at Booth 4032

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High quality graphics doesn't have to be expensive. The new VISUAL 500 and VISUAL 550 terminals emulate the Tektronix[®] 4010 but cost only about half as much. And they have 768 x 585 resolution for sharp text and graphics display on a large 14" screen.

Both the VISUAL 500 and VISUAL 550 are compatible with standard business, laboratory, and scientific software including PLOT 10," DISSPLA," TELL-A-GRAF, SAS/GRAPH and DI3000/GRAFMAKER. Advanced graphics features include: Resident vector draw, point plot, rectangle draw, multiple linestyles and patterns with rectangle pattern fill. Raster scan technology provides fast data update and develops a bright display image.

Powerful alphanumeric operation is also provided, displaying 80 characters by 33 lines with separate display memories for alpha and graphics modes. The VISUAL 500 provides switchable emulations of the DEC VT52," Data General D200, Lear Siegler ADM-3A, and Hazeltine 1500 terminals. The VISUAL 550 is a block mode terminal which complies to the ANSI X3.64 standard. VISUAL 500 and VISUAL 550... the latest in the industry's finest line of video terminals. Call or write for details.

Service available in principal cities through Sorbus Service Division of Management Assistance Inc.

> VISUAL 550 \$2,695 LIST

Buffered Editing Terminal with ANSI X3.64 Standard

See for yourself

Visual Technology Incorporated 540 Main Street, Tewksbury, MA 01876 Telephone (617) 851-5000. Telex 951-539

VISUAL 500 **\$2,495** LIST Character Mode Terminal with Emulations



Precise answers instantly: now waveform measurements are automatic!

Now you can cut from minutes to seconds the time it takes to perform most common waveform measurements. By automatically performing all routine measurement tasks, the Tek 7854 minimizes errors and gives you more time for more productive activity.

7854 MODULAR OSCILLOSCOPE

Touch a front panel key and the 7854 digitizes repetitive signals up to 400 MHz. Stores them. Measures them. And displays the answer. For any rise time measurement, for example, you need only press two keys—AQR and RISE-to consistently obtain a precise, repeatable answer on-screen. There is no painstaking set-up, no decision-making, no mental calculation required.

Time savings and risk reduction are even more dramatic in more complex tasks, such as calculating the area under a power curve or determining instantaneous power from current and voltage waveforms... both the work of a few seconds on the 7854.



You can develop vour own measurement routines using the companion waveform calculator. You can make virtually any sequence of procedures automatic, then leave operation to lesser skilled operators and technicians. You can even connect the 7854 to host computers and mass storage via the standard IEEE-488 interface bus

More than 30 plugins let you reconfigure capabilities at will. Like all Tek 7000 Series scopes, the 7854 keeps expanding in value. Add high-sensitivity differential amplifiers. Comparators. Counters. Spectrum analyzers. Or sampling plug-ins that let you digitize repetitive signals up to 14 GHz. At any time, you can add new performance at a fraction of the cost of a monolithic instrument.

Allow yourself more time for creative problem-solving. In this era of hand-held calculators, it's about time you let the 7854 begin making your life simpler and your time more productive. Call your Tektronix Sales Engineer today!

For further information, contact:

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Europe, Africa, Middle East Tektronix Europe B.V. European Headquarters Postbox 827 1180 AV Amstelveen The Netherlands Phone: (20) 471146 Telex: 18312-18328

Canada Tektronix Canada Inc. P.O. Box 6500 Barrie, Ontario L4M 4V3 Phone: 705/737-2700

Tektronix

COMPUTERS

Desktop UNIX based minicomputer offers PDP-11/70 class processing power



A compact tabletop system that supports up to 16 users, the P/25 offers performance usually associated with mid-range minicomputers requiring 2 to 5 times more physical space. The system incorporates industry standards that provide users and OEMs with system flexibility and transportability and, is designed for the UNIX operating system from Bell.

Architecture of the system links a powerful job processor with as many as four 16-bit I/O processors and allows each I/O processor to use burst multiplexed DMA to transfer data directly to and from main memory. This removes I/O overhead from the job processor, and permits the system to achieve high throughput while running UNIX. A typical system links the job processor and 2 I/O processors. During operation, the job processor performs computation and operating system functions while I/O processors handle disk, tape, and serial I/O. This provides powerful support for multiple users with fast response time to each.

The 16-bit job processor has more than 110 distinct instructions that operate on 7 data types, including bits, 32-bit words, and strings. For easy programming, the processor has 16 general purpose registers and supports separate instruction and data spaces as well as privileged instructions. Floating point processing is performed for single-precision (32-bit) or double-precision (64-bit) addition, subtraction, multiplication, and division compatible with the proposed IEEE format.

Up to 2M bytes of memory can be configured in a system using modules based on 64k-byte RAM chips. This provides ample space for UNIX and system buffers, and allows support of multiple users running large programs. Controller module for the system's Winchester disk drive and streaming cartridge tape drive is a single module with its own 16-bit processor and 128k-byte memory. In addition to all error checking and recovery operations, the controller automatically performs diagnostics using a reserved disk track. It also ensures the completion of disk transfers in progress during power failures. The intelligent mass storage controller, programmed in C, provides the memory and processing capacity necessary to perform file system functions, system backup operations, and caching algorithms. All serial I/O tasks are handled by modular intelligent communications processors (ICPs). Each ICP contains a 16-bit processor, 32k bytes of RAM, 16k bytes of PROM, 8 full-duplex serial ports, 1 parallel port, and 9 DMA channels. Systems may have up to 2 ICPs for a total of 16 serial and 2 parallel ports. The processor and RAM in each ICP allow segments of UNIX or customized communications and terminal handling programs to be downloaded and executed locally. The disk subsystem consists of a high performance 8" Winchester disk drive with 22M-, 35M, or 72M-byte capacity and 1.2M-byte/s data transfer rate. Average access time is 28 ms for the 72M-byte drive and 38 ms for the 36M- and 22M-byte drives.

A system with 1M-byte error correcting main memory, 72M bytes of disk storage, and 2 ICPs to handle 16 user ports is priced at \$40,000, excluding terminals. An 8-user system offering 0.5M-byte main memory, 36M-byte disk, and 1 ICP is priced at \$27,000.

While the system is being announced with Version 7, UNIX System III will be available by mid-1982. Plexus Computers Inc, 2230 Martin Ave, Santa Clara, CA 95050.

See at Booth 7532

Circle 449

16-bit microprocessor based computers

Series of 16-bit microprocessor based business computers uses multiprocessor design and integrates either MULTIBUS or S-100 card cage for expansion. System processes existing CP/M or MP/M 8-bit code without modification, while supporting CP/M-86, MP/M-86, business BASIC, UNIX, and OASIS-16. System supports up to 16 users and 16 printers, 112M-byte max Winchester disk storage, 8" diskette drive (IBM compatible), and cartridge tape drive. Series domestic list price starts at \$6995.

Other 16-bit microprocessor based systems to be shown feature RAM to 1M byte, Winchester disk capacity to 80M bytes, 10 serial ports std, ECC memory, up to 16-user capability, MULTIBUS and S-100 bus adapters, and complete communications facilities. The desktop units are priced from \$6995 to \$14,995. Series 5000 business computers with S-100 bus architecture and Z80 microprocessor will also be displayed. Prices range from \$3995 to \$9995. Dynabyte Business Computers, 521 Cottonwood Dr, Milpitas, CA 95035.

See at Booth 7132

Circle 450

32-bit desktop systems

Universe systems 68/15 and 68/17 desktop models are added to the 32-bit Universe 68 line of computers. Model 68/15 incorporates a 32-bit central processor, 256k-byte main memory, and a 16M-byte disk, housed in a 14" (36-cm) package. Model 68/17 is identical to 68/15, but includes 512k-byte main memory on a single card. Model is expandable to 2M bytes. Both models are fully compatible with previously announced Universe 68 systems, and support UNOS, a UNIX-like operating system. Languages supported are FORTRAN, BASIC, C, and Pascal. Systems are built around the 32-bit VERSAbus and SASI peripheral bus. Model 68/15 base price is \$19,200; base price for 68/17 is \$21,200. Charles River Data Systems, 4 Tech Circle, Natick, MA 01760.

See at Booth 5508



HONEST ENGINE

The New IDM 200 Relational Database Machine.

Special jobs require special machines, and the new Britton-Lee IDM 200 is the special engine for complete relational database management in business computers. This latest member of the Britton-Lee family of Intelligent Database Machines scales sophisticated relational database management down to minicomputer and microcomputer systems.

Hardware Revolution

Powerful, efficient machines replaced hand labor in the Industrial Revolution. Now Britton-Lee is substituting special computer hardware for slow-running relational software in the relational database management revolution. The IDM 200 improves DBMS performance up to 10 times by relieving the system of the repetitive, time-consuming operations imposed by software database management systems. The IDM 200 also opens the door to expansion of databases

to nearly 3 billion bytes!

See the Britton-Lee IDM in action at: DEXPO 82, Atlanta, 5/10-12, NCC, Houston, 6/7-10, COMDEX (Spring), Atlantic City, 6/28-30.

Labor-Saving Device

Ad hoc query capability lets the IDM 200 take the tedium out of database management programming. And it includes powerful functions found in the best DBMS systems, including data dictionary, concurrency control, audit logging, transaction management, security, backup and crash recovery.

Low-Cost Horsepower

The unique IDM 200 brings relational database management costs down to small business system proportions. Peaked-out systems get a new lease on life without the expense of replacement. A return-oninvestment revolution.

Get the facts! Ask your system supplier about the new IDM 200. Call or write Britton-Lee for the complete IDM information package including the more powerful IDM 500 Intelligent Database Machine.



90 Albright Way, Los Gatos, CA 95030 (408) 378-7000

Princeton, NJ, (609) 921-3113/Washington, D.C. (703) 790-0440/Boston, MA (617) 273-3943/Reston, VA (703) 860-4637/Atlanta, GA (404) 452-7676 Kansas City. MO (816) 765-0985/Dallas, TX (214) 263-2214/Houston, TX (713) 266-6933/UK, TLX 27200/W. Germany, 024-0813-108/Japan, TLX 2322008

CIRCLE 73

COMPUTERS

Distributed processing family and IBM compatible systems

Family 8860 of distributed information systems uses SNA to communicate with both the company's and IBM's host mainframes. Three field upgradeable and upward compatible models are available. Model 5, for applications where processing power is initially distributed to user sites, can support up to 12 workstations, consisting of terminal display and/or printer. System utilizes 0.75M bytes max of main memory and 2 diskette drives. Two larger 8860 systems, models 10 and 40, provide users with full complement of development software, including ANSI '74 COBOL, the company's RAPID interactive program generator, and a full set of utilities. Model 10 has 1M-byte main memory and supports 2 disk drives with up to 156M-byte disk storage, of which 26M bytes are removable. System can support between 4 and 16 workstations and 2 diskette drives. Model 40 supports 24 workstations max and 2 diskette drives. It has 1M-byte main memory and a range of disk products supporting both fixed and totally removable media with 312M-byte max storage. Central administration system allows either an 8860 model 10 or 40 at the central site to develop applications programs, and downline load them to local 8860 systems.

A family of IBM compatible information processing systems, the 8890 series, will also be displayed. This field upgradeable series has central processor, system software, and full complement of peripherals. Models 30, 50, and 70 are performance equivalents to IBM 4331 group 11, 4331 group 2, and 4341 group 10, respectively. Compatible peripherals include removable disk drives providing total system capacity of 15.4G bytes of storage. Main memory is available in 1M-byte increments up to 8M bytes. Operating system NIDOS/VSE is compatible in IBM DOS/VS(E) environments. The OS incorporates features of IBM OS/VS1 and MVS operating systems.

Systems can be used in either centralized, decentralized, or dedicated processing environments. The 8890 incorporates a central processing complex consisting of CPU with 32-bit microprocessor for instruction processing and microprogram storage, main memory processing unit, 1/0 management and processing subsystem, and service processing unit. Components can function separately or concurrently overlapping activities. **Nixdorf Computer Corp**, 300 Third Ave, Waltham, MA 02154.

See at Booth 6123

Circle 452

LSI-11 based computer system supplies 4M-byte addressing/80M-byte Winchester capacity

The w23, an LSI-11/23 based computer system, supplies capacity for 4M-byte main memory along with 80M bytes of Winchester capacity. KT-24 compatible memory management, provided by the w23's Q-MAP, allows 4M-byte addressing while maintaining software compatibility with the processor. Packaged in a 10.5" (26.7-cm) chassis with 27 dual DEC slots and 45 A of 5-V power, the system operates with RSX-11-M, RSX-11-M PLUS, RSTS, UNIX, and other DEC operating systems that support KT-24 memory management. The 1M-byte DR-213 semiconductor add-in memory in the package doubles the capacity of comparable DEC memory modules.

Q-MAP, occupying a quad-height module, emulates the KT-24 UNIBUS map option to allow 18-bit address DMA peripherals to communicate with 22-bit main memory. It has the capability to support existing peripheral controllers since it maintains the 22-bit bus for 4M-byte main memory addressing while generating an 18-bit bus for support of existing peripherals. The 80M-byte disk meets the higher capacities needed to complement the larger memory. The Q-MAP module also contains 2 serial line units that supply the CPU with serial ASCII interfaces. Baud rates for each are switch-selectable from 50 to 19,200 baud. A CPU diagnostic PROM can be installed on the board, as well as various peripheral bootstrap PROMS.

An SO4/A SMD controller, in combination with the internally mounted 80M-byte Fujitsu Model 2312 Winchester disk, emulates the DEC RM02 disk system. An additional SMD disk may be connected external to the package.

Pricing for a basic unit is \$19,400. Dataram Corp, Princeton Rd, Cranbury, NJ 08512.



See at Booth 4022

Circle 453

Information system with component fail guards

FAILSOFT and remote diagnostic capabilities provide offsite troubleshooting for the F/4000 32-bit information system. FAILSOFT limits system downtime to approximately 5 min if a system component fails. In configuring the F/4000, users can designate any or all system components as FAILSOFT modules. Under normal conditions, FAILSOFT modules enhance system performance. Should a component fail, the system shuts down, diagnoses the problem, assigns a FAILSOFT module to substitute for the failed module, and then resumes operation. FAILSOFT capability, applicable to interactive, online applications, allows repairs to be scheduled when users are not on the system. Remote F/4000 diagnostics allow hardware and software monitoring through a remote support terminal. User can also power the system on and off, load software, and monitor temp and voltage through the remote terminal. F/4000 is program compatible with IBM System/370 mainframes, giving users access to library of 370 software. The complete F/4000 system, including processor, integrated controllers, peripherals, and software is priced from \$90,000. Formation Inc, 823 E Gate Dr, Mt Laurel, NJ 08054.

See at Booth 6632

Raycorder II... the intelligent connection!

Whether your application calls for an OEM tape drive or an intelligent operating system, Raycorder has the interface you can use. The Raycorder II Model 6440 offers not only maximum reliability and performance in a low-cost cassette tape drive, but also the versatility and convenience of intelligent controller interfaces.



Select from RS232, IEEE488, ANSI Parallel, or your own design, based on your needs.

Raycorder's microprocessor motion control, coupled with its simple mechanical design, provides such features as constant tape speed and uniform tape tension. Precision head alignment assures cassette interchangeability. Optional features, such as read-after-write and 1600 BPI packing density, make the Raycorder even more versatile.

1111111111

Features

Versatility Intelligent interfaces Maximum reliability and performance Low price Constant tape speed Simple mechanical configuration Uniform tape tension Precise head alignment Ease of loading/unloading cassette

Applications

...............

Process control Automated test equipment Data logging Store and forward Program loading Instrumentation

COLUMN COUNTRY

................



\$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$ \$

Raymond Engineering Inc.

217 Smith Street Middletown, Connecticut 06457 (203) 632-1000

Raycorder Products Division

A Subsidiary of Raymond Industries Inc.

COMPUTERS

User programmable standalone display computer



Although its operating parameters make it suitable for use as a terminal in a multiprocessor environment with interactive communications to a host computer, the model 1505 can also serve as a powerful standalone computer. Its 15" (38-cm) nonglare diagonal display screen is arranged in a 25-line x 80-col format, for a std 128-char or optional 256-char ASCII set. Memory consists of either 16k or 64k bytes of RAM, with 2k-, 4k-, or 8k-byte bootstrap using 2716, 2732, or 2764 type EPROM. Two 5.25" 96-tpi diskette drive units provide up to 1.2M bytes of storage. Optional Winchester drives add 5M or 80M bytes.

A detachable keyboard is arranged in 4 sections: typewriterlike alphanumeric keyboard, control pad with cursor keys, calculator style numeric pad, and 13-function key section. Communication is via an asynchronous RS-232-C interface at speeds up to 19,200 baud, and a 2-wire direct interface can be accommodated through the same port. A synchronous option is available for speeds up to 50k baud. Software support includes BASIC, Pascal, CIS-COBOL, FORTRAN, and the company's high level OPL and MDOS/80 and HDOS/80 operating systems. CP/M can be supported as an option.

Also shown will be the 1503, basically a terminal with 2 microprocessors and read/write memory that communicates up to 19,200 baud, and the 1507, which incorporates an 8085 microprocessor and operates at communications speeds of up to 50k baud using optional controllers. Both function as online remote systems to host computers. **Ontel Corp**, 250 Crossways Park Dr, Woodbury, NY 11797.

See at Booth 4738

Circle 455

Low cost distributed processing computers

Desktop system 48/DL of the MacroComputer line of distributed processing computer systems for small installations and entry level applications is priced at approximately onethird the cost of the original MacroComputer system 48. DL version includes 6M-byte Winchester disk storage, dual CPU with 128k memory, and expandability to support 8 workstations, each with separate applications processor. System 48/SL freestanding unit supports up to 16 workstations, and up to 160M bytes of Winchester storage. Unit is intended for medium sized business applications. System 48/XL, a larger freestanding system, can support 64 workstations and has provision for industry std 9-track 0.5" tape. The /XL can be utilized in a local area network with the /DL and /SL, consisting of several hundred workstations, with a mix of 8-, 16-, and 32-bit processor types. TEI Inc, 5075 S Loop East, Houston, TX 77033.

See at Booth 4345

Circle 456

SOFTWARE

Upgraded VULCAN operating system

Operating system vos combines several attributes of VULCAN os, and ensures compatibility for users upgrading from VULCAN. The new OS is designed to take advantage of the company's current processor line, including superminicomputer H80-1A and H100-1A. VOS implements a fully automated data base for RJE protocols. It incorporates auto-dial, automatic scheduling, and load control features. The RJE Executive also simplifies user interaction. HARRIS MUSE, a word processing package, is also supported by vos. It includes menu driven user interface, full screen, cursor controlled text editor, and simple keystroke editing and formatting functions. Pascal extensions available with vos support both compatible and extended (3M-byte) mode operation. Additional FORTRAN 77 support is included. User callable walkback features for debugging have been added to the FORTRAN library, with the compiler pointing out syntax errors in a statement. Compatibility for fast refresh of symbol table results in significant time savings and throughput gain. Other features of vos include additional COBOL 74 support, modifications to both BASIC compiler and the macro assembler, additional flow control for teletype devices, new text editor and documentation processor. and alternate resident system capability. Both vos and vulcan support interactive, batch, and realtime processing modes concurrently, as well as 8 language processors and 6 remote job entry protocols. vos operating system is available immediately to users of the company's computers at no charge without source code, or at \$3000 with source code. Maintenance price is \$100/month. Harris Corp, Computer Systems Div, 2101 W Cypress Creek Rd, PO Box 6200, Ft Lauderdale, FL 33310.

See at Booth 4000

Circle 457

Software packages for generation of FORTRAN in math/statistics applications

MATH/PROTRAN package contains brief, powerful PROTRAN statements that generate FORTRAN for solving mathematical problems. Software applications perform approximation and smoothing, data fitting, differentiation, FFTs, integration, and interpolation, and solve differential equations, eigenvalue problems, linear and nonlinear systems of equations, and nonlinear least squares problems. Programs operate on IBM 360/370/43XX/30XX series and compatible mainframes, Control Data 6000/7000 and Cyber 70/170 series, DEC VAX-11 series, DEC System 10/20, and Data General MV 8000/6000.

STAT/PROTRAN performs statistical analysis featuring simplified data management and organized, labeled output. Software (continued on page 122)

Here is a picture of aWINC[™]08 controller as seen from your DEC computer.

Our WINC08 controller is completely software transparent to DEC's RL02, so your PDP-11 or LSI-11 computer won't even see it! And while this



And while this For LSI-11 users. Q-Bus®/UNIBUS® compatible controller will be totally invisible to your computer, the advantages of using it will be *immediately visible* to you.

For instance, when teamed with our dual 8-inch Winchester disk drives, WINC08 offers up to 41.6 megabytes of storage capacity in a DEC "lookalike" enclosure just 5¹/₄ inches high. The result? With WINC08, you get four times the storage capacity of DEC's RL02 in one-eighth the space!

For LSI-11 users who want the flexibility of an 8-inch Winchester combined with an 8-inch dual-headed floppy disk, there's the WINC08/F controller. It provides emulation of both the RL02 and RX02 in a single 5¹/₄-inch high enclosure!

Both the WINC08 and WINC08/F controllers offer the highest throughput available. Maximum data reliability. Unique on-board self-test capability. And the best price-to-performance ratio in the industry!

Now you can add storage capacity and increase the efficiency of your DEC system in the bargain. And we'll deliver your choice of a dual Winchester, or Winchester/floppy combination in just thirty days. Either way, you'll see a big difference, even if your computer doesn't see a thing!

To order – or for additional information – call or write us today. Advanced Electronics Design, Inc., 440 Potrero Avenue, Sunnyvale, CA 94086. Phone 408-733-3555 TELEX 357-498.

Sales Offices: LA 213-907-8811/ Detroit 313-352-4290/New Jersey 201-238-6322/Boston 617-256-1700.

* Reg. trademark of Digital Equipment Corp. TM_Trademark of AED.



THE DSD 880 WINCHESTER SYSTEM.

MADE THE WAY DIGITAL WOULD MAKE IT. EXCEPT DIGITAL DOESN'T MAKE IT.



HyperDiagnostics, HyperService and Rapid Module Exchange are trademarks of Data Systems Design, Inc. PDP is a registered trademark of Digital Equipment Corp.

OEM's: Don't miss the neww 700 Series of Multibus Winchesters at NCC Booth #A 549, Astroarena, Houston The people at Digital are a pretty smart bunch. They make some of the finest small computers in the world. So we like to think that if they were to make a new storage system like our 880 Winchester/Floppy, they'd do it the same way we did.

First of all, they'd make it extremely reliable with extensive testing and by using one of the most reliable storage technologies known, the Winchester.

Next, they'd offer it in different capacities, like 7.8, 20.8, and 31.2 megabytes, with a choice of .5 or 1 Mb floppy back-up, or none at all.

These different configurations would, of course, be fully compatible with Digital's LSI-11 and PDP®-11 computers.

And the whole package would be extremely compact, just 5¹/₄ inches high, so it would save space and fit in almost anywhere.

They might even add some on-board selfdiagnostics, similar to our exclusive HyperDiagnostics,™ so you could test, exercise, and debug without a CPU. And cut down on your service costs at the same time.

Maybe they'd even institute a module swap program, something like our Rapid Module Exchange," which would be designed to get you back up and running within twenty-four hours.

Finally, since this system would be so dependable, they'd be able to offer their extended service at a much lower price—much like we do with our own HyperService,[™] which goes into effect when the 90-day warranty expires and covers everything.

And then, as if it weren't good enough already, they'd offer this remarkable storage system at a lower cost per megabyte than any comparable system.

The fact is, though, Digital doesn't make anything like this.

Which is why we make the DSD 880 Winchester system to go with your Digital computer. And, why we make it the way we do.

Corporate Headquarters: 2241 Lundy Avenue, San Jose, CA 95131. Eastern Region Sales and Service: Norwood, MA, 617 769-7620. Central Region Sales: Dallas, TX, 214 980-4884. Western Region Sales: Santa Clara, CA, 408 727-3163.

DATA SYSTEMS DESIGN

WP FLPY	READY	
		,

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EG 82 PREVIEW

SOFTWARE

reduces statistical problem solving time and covers such areas as basic statistics, frequency and cross tabulation, correlation, regression analysis, analysis of variance, and random number generation. Package is available for IBM 360/370/43XX/ 30XX series and compatible mainframes, DEC VAX-11 series and System 10/20, and Data General MV 8000/6000. IMSL, Inc, 7500 Bellaire Blvd, Houston, TX 77036.

See at Booth 3418

Circle 458

Data management software

SAS/FSP facility for data entry, editing, query search, file retrieval, and letter writing allows screens to be viewed as order entry forms or invoices. Data can be entered into SAS data sets for data management, analysis, and reporting. Letter writing facilities allow users to compose and edit letters that can be output as hard copy on the IBM 6670 or 3800, Xerox 5700 or 9700, or std line printers. Multiple users can simultaneously view the same data set. The full-screen product is designed for SAS users with IBM 3270 terminals. It runs on IBM 360/370/30xx/4300 or compatible machines, in batch mode under OS and OS/VS, and interactively under VM/CMS and TSO. An SAS facility that also runs under DOS/VSE will be displayed.

Other products to be exhibited include SAS/GRAPH, an intelligent color graphics device for business and research applications; SAS/ETS, the econometrics and time series library; and SAS/IMS-DL/1, a DL/1 interface that provides access to batch IMS/VS or CICS/OS/VS data bases. SAS Institute Inc, PO Box 8000, Cary, NC 27511.

See at Booth M106

Circle 459

BLIS/COBOL operating system

BLIS/COBOL Version 5.0 is a true multi-user online operating system for Data General, Point 4, Ampex, Bytronix, Digidyne, Ardent, and other NOVA compatible computers. Throughput is increased over 40% by expanded main memory and virtual memory capabilities. One to 30 users can each run up to 200k-byte COBOL programs without modification on CPUs using either 16-bit extended memory addressing (128k bytes) or up to 2M bytes of mapped memory. Additional throughput is achieved by overlapped disk I/O transfers. Other enhancements include 2k-byte screen records, programmable CRT function key support, CRT block mode transfers, alternate sector support, and protective capabilities to restrict applications software to a specific CPU. **Information Processing Inc**, 1850 Lee Rd, Suite 320, Winter Park, FL 32789.



Graphics software enhancements

Second generation of Retro-Graphics terminal enhancements, the GEN. II, features Tektronix 4010 and 4027 graphics terminal emulation; monochromatics, gray scale, and color display formats; standard to medium resolution; 8- and 16-bit microprocessors; and compatibility with most industry std graphics software, including the company's PLOTPAKTM. Computer terminals that can be upgraded with GEN. II include TeleVideo, Lear Siegler ADM series, ADDS Viewpoint, TI OPTI 900 model 940, and Datamedia Colorscan (Color Retro-GraphicsTM). Enhancements provide user friendly, 4027 type commands which allow operator to plot points, draw circles and polygons, fill enclosed shapes, and selectively erase. Graphics functions are resident in terminal; data do not have to be transmitted to, and processed by, the host software and CPU. For interactive applications, GEN. II upgraded terminals can be interfaced to optional input devices, such as lightpen or digitizing pad, and to various output devices, including impact and thermal printers, plotters, and cameras. Retro-Graphics can also be purchased as a field upgrade. Digital Engineering, Inc, 630 Bercut Dr, Sacramento, CA 95814.

See at Booth A513

Circle 461

INTERFACE

Software compatible graphics upgrade for LA120

DECPLOTTM plug-in module provides precision dot addressable plotting features over entire page, while maintaining features of DEC LA120 conventional text printer. DECPLOT software conforms to graphics protocol standards of DEC, and is compatible with most DEC graphic terminal products, as well as with TEXPLOTTM, the portable graphics terminal based on Texas Instruments' Silent 700^R equipment. Three commands, and no ASCII control chars, are required for plotting. Existing software can be easily modified for graphics without rewriting systems software. DECPLOT software is also compatible with ISSCO'S DISSPLA and TELL-A-GRAF, and several computer timesharing services. As an upgrade option, it provides full graphics output flexibility from existing terminals. DECPLOT LA120 dual-mode printer system represents a dollars savings of approximately 50% for most graphic applications, compared to alternative plotting output devices. Installation of module into the DEC motherboard requires approximately 5 min. DECPLOT LA120 system accommodates full variety of std DEC terminal options. Modules are single-quantity priced at \$595. Texprint, Inc, 8 Blanchard Rd, Burlington, MA 01803.

See at Booth 7906

Circle 462

High speed digital switch

Dynamic multiple access device (DMAD) resolves disk system contention and reconfiguration for large computer systems, including multiple mainframe configurations. Additional control and data paths between the controller and disk storage units make it possible to move subsystem contention from the controller level to the device level. System disks and standby devices are shared among multiple systems on a demand basis. With 150-ns logic delay, the DMAD is hardware and software (continued on page 126)



Equipment manufacturers can now integrate a powerful, new Fiber Optic Modem directly into their equipment; resulting in a device that will provide exceptional data throughput performance in any local distribution environment.

The use of fiber optics for local data distribution assures that your end product will perform as it was designed; regardless of the environment in which it is used. Unlike conventional wire cables, optic cables are totally unaffected by rfi, adjacent noisy cables, or heavy duty electrical equipment. A big plus is that it is also effectively immune to wire tapping; yet costs about the same as coaxial cable.

In addition to the inherent advantages of fiber optics, Versitron's OM series of plugin modems offers an impressive list of performance specifications. These include: operating range up to two kilometers (6500 feet), synchronous or asynchronous operation at data rates up to 38.4 KBPS, true EIA handshaking (three separate control signals in each direction are multiplexed along with the data), and an optional alarm circuit that will shut down all traffic if the cable is tampered with.

For details on how our optical modem can help you to significantly improve the marketability of your end product, give us a call at (202) 882-8464; or write Versitron, Inc., 6310 Chillum Place, N.W., Washington, D.C. 20011.



BACKED-UP



BACK-UP

Archive backs up Winchesters 10 times faster than floppies.

Today's business computer system simply can't afford

floppy Winchester back-up anymore. Not when our Archive Super Sidewinder ¼" Streaming Cartridge Tape Drive can copy 45MB in just nine minutes.

A floppy, on the other hand, takes more than an hour to do the same job. Not counting the time you spend inserting a new disk every few minutes.

Saves "handling" charges.

One Super Sidewinder cartridge is equal in capacity to 38 eight-inch disks.

That will save you over \$200, plus the cost of handling all those disks—inserting, removing, jacketing, labeling, and filing. In addition, a Sidewinder

cartridge is completely enclosed when out of the drive, virtually eliminating damage due to handling.

More than just a back-up.

Our ¼" streaming tape drives provide the complete removable media needs of any system: Software distribution, data collection and program loading. All performed at the touch of a button. System integration made simpler.

Both our 20MB and 45MB drives are specifically designed to fit an 8" floppy disk footprint. To use the same power supply. And to use the same simple 8-bit parallel interface.

We could go on. But let's get specific, contact us today. And ask for our new handbook on streaming tape drives and how to use them. Archive Corporation, 3540 Cadillac Ave., Costa Mesa, CA 92626. (714) 641-0279, Telex 4722063, TWX 183561. Distributed nationally by Hamilton/Avnet.

ARCHIVE



See Us at the Continental Rm., Westin Oaks Hotel, Houston NCC, 3:00-9:00 p.m.

INTERFACE

transparent to the host system. Separate receive/transmit logic permits controller/device separation of up to 1000 cable ft. Up to 4 peripheral controllers can attach to each peripheral device access. Scanning at 100 MHz, the DMAD provides the requesting controller with an immediate response to a read/write request and locks on the requesting controller; upon completion of the requested function, it continues to scan the next controller port to prevent lockout. DMAD interfaces up to 4 Control Data model 7155 controllers to each access of a model 885 disk storage unit. Additional models are planned for other disk storage subsystems. Single-unit price for Control Data configuration is \$15,600. Western Electronics Technology, Inc, 11281 Richmond Ave, Suite 103, Houston, TX 77082.

See at Booth A457

Circle 463

Synchronous metallic and optical bit drivers

RS-232-C type D compatible synchronous bit drivers are available in metallic (model 9340) and optical (model 222003) versions; both meet FCC 2078 type A emi requirements. Simplex and duplex synchronous communications capabilities offer data rates up to 56k baud. Transmission range of the metallic driver at 56k baud is 8000 ' (2438 m), and 15,000 ' (4572 m) at 9.6k baud. Optical unit's transmission range depends on fiber optic cable selected. Optical driver's internal clock is switchselectable to 2.4k, 4.8k, 9.6k, or 19.2k baud. Both versions are compatible with all synchronous protocols, and feature LED status indication for system diagnosis. RS-232-C molded cable assemblies are designed for inhouse data communications between computers and peripheral units. Short-haul line extenders, used in pairs, replace conventional telephone equipment, eliminating equipment leasing and line charges.

Transmission line interface for the metallic driver uses 2 twisted pair #24 AWG or larger, with shielded pairs available for use in noisy environments. Op temp range is 0 to 70 °C; input power is 105 to 130 Vac, 60 Hz, 10 W. Belden Corp, 2000 S Batavia Ave, Geneva, IL 60134.



Modem control board



MLSI-DLV11-ED asynchronous serial interface with modem control for LSI-11 based systems is compatible with DEC DLV11-E, while offering several features not present on the DEC board. Single-line RS-232-C interface provides device addressing, UART parameters, and switch-selectable interrupt vectors. Data rates from 50 to 19.2k baud are both switch- and programselectable. Jumper-selectable 4-level interrupt capability ensures complete functionability. Board allows splitting of transmit and receive baud rates. Edge mounted LEDs expedite problem evaluation and eliminate need for breakout box or other device to assess line activity. Two LEDs indicate data being transmitted or received, and 7 others indicate status of the modem control signals-data terminal ready, request to send, carrier detect, clear to send, ring, secondary received data, and secondary transmitted data. MDB Systems, Inc 1995 N Batavia St, Orange, CA 92665.

See at Booth 2015

Circle 465

Intelligent coupler gives streaming tape capability to DEC mini- and superminicomputers

Interface board DU132 tape coupler provides streaming and start/stop tape backup for DEC PDP-11/34 through PDP-11/70 minicomputers, as well as VAX-11/750, 11/780, and 11/782 superminicomputers. The TS-11 emulating board interfaces with either 0.5" start/stop formatted 9-track tape transports from all major manufacturers, or with streaming transports with embedded formatters from Cipher Data Products, Control Data Corp, Kennedy Co, and System Engineering Labs. Coupler permits data transfer rates of up to 200k bytes/s with tape speeds to 125 ips. When used in start/stop mode, it is completely software compatible with DEC VMS, RSTS/E, RSX-11M, and RT-11 operating systems. A standalone utility software package accommodates the streaming transports.

Standard high speed bipolar microprocessor forms the board nucleus. Control store memory handles data manipulations, (continued on page 128)

NOW-One Power Supply for the Whole World!

Power-One's International Series - the New World Standard in D.C. Power Supplies

Now, for the first time, there is a high reliability open-frame D.C. power supply series designed specifically for products sold throughout the world! Not only can it make your international marketing simpler, but more profitable as well.

Wide Choice of AC Input Power

Each International Series unit is rated at 100, 120, 220, 230, and 240 volts, 47 to 63 Hz. So wherever your products are headed, one standard off-the-shelf power supply will serve. No more costly stocking of different units for different destinations.

Meets International Safety Requirements, Worldwide

More and more countries are adopting tougher safety standards, but the International Series can be used anywhere, for almost any application. It meets the most important requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.



Power-One's patented International Series transformers feature separate, fully enclosed, primary and secondary coils. Meets safety requirements of VDE, UL, CSA, BPO, IEC, CEE, and ECMA.

How did we achieve this technological breakthrough? Take a close look at our power transformers. Our new patented winding process features separate, fully enclosed primary and secondary windings. This unique construction complies with the most respected safety standards, worldwide. These include:

Leakage Current,	
Line to Ground:	5.0 µa
Spacings,	
Live Parts to Dead Me	etal: 9.0 mm
Other Than Field	
Terminals:	5.25 mm
Dielectric Withstand Vo	ltage,
Input to Ground:	3750 VAC
Input to Outputs:	3750 VAC
Outputs to Ground:	500 VAC

Phone or Write for New Brochure

No way can we tell the full International Series story here, so we've prepared a new brochure for you with all the details. Send for it today, and see what it takes to set a new standard for the world!



See us at ELECTRO '82 in Boston

CIRCLE 79

INTERFACE

adhering to specified timing limits and bus loading. All data, address, and control signals are parallel transferred between coupler and host via the UNIBUS. In addition, a 1k-byte buffer virtually eliminates data late errors. Automatic selfdiagnostics are resident on the unit. Without interfering with UNIBUS or transport bus, routines check the microprocessor, sequencer, all data paths, and buffer.

Board consists of a single quad-wide card that plugs directly into any small peripheral controller slot or DD-11 series backplane of an expansion chassis. A pair of 50-conductor ribbon cables links the board with tape transports at distances up to 25' (7.6 m). Coupler supports up to 4 transports in a daisy chain interconnection, enabling units to be added without additional interface hardware. Single-unit price is \$2850, with quantity discounts available. Streaming software package is \$350. **Distributed Logic Corp**, 12800-G Garden Grove Blvd, Garden Grove, CA 92634.



See at Booth 3108

Circle 466

Streaming controller for LSI-11

Controller TC-50 mounts directly into 1 quad-slot in LSI-11 Q-bus, and connects to popular streaming tape drives from Control Data, Cipher Data Products, and Kennedy Co. The 0.5" magnetic tape streaming drive allows up to 80M bytes of backup storage to be placed on a single tape, while streaming at 100 ips. It functions as a normal stop/start drive at speeds of

PERIPHERALS PAGE 146



12.5 to 25 ips. Controller can run up to 8 streamer or std formatted stop/start drives. It emulates DEC TM11/TU10, and is completely software compatible with DEC operating systems and diagnostics. The controller draws 2.5 A of 5-V power, and has control features such as stream/no stream, normal gap/long gap, IBM byte swap, and edit. It supports full 22-bit addressing of the Q-bus. Device comes complete with cable for connection to the formatted drive. Price is \$1200 in quantities of 10. Western Peripherals, Div of Wespercorp, 14321 Myford Rd, Tustin, CA 92680.

See at Booth 4332

Circle 467

Industry compatible streamer tape adapter

Streamer tape adapter is microprocessor controlled and interfaces industry std 0.5" streaming tape drives. The half-board is compatible with Perkin-Elmer operating systems and diagnostics. Extended command and status functions enhance streaming functions. The tape subsystem generates industry compatible 1600-bpi tapes, and is also compatible with Cipher, Control Data, and Kennedy 0.5" streaming tape devices and std formatted incremental tape drives. Tape adapter comes complete with 20' (6.1-m) cables and documentation. The adapter is computer tested, burned-in, and retested before shipment. It is also backed by a full 1-year warranty. Quantity-1 price is \$1500; OEM discounts are available. **Macrolink**, 1150 E Stanford Ct, Anaheim, CA 92805.



Century Data Systems

Finally, an off-the-shelf answer to Winchester back-up.



Introducing the Intelligent Marksman Back-Up package. And the solution to the chronic problem of Winchester back-up.

And what a solution it is. Our new formatter is specially designed to control 20, 40, 80 or 160 MB Marksman Winchesters — and the Archive Sidewinder, Cipher Quarterback, or DEI Streamer ¼-inch tape drive for back-up.

A simple host adapter and software I/O drivers are all you need to tie into word and data processors utilizing interfaces such as S-100 or Multibus, and running operating system environments such as CP/M, MP/M,UNIX and others.

If that isn't enough, just one formatter will control two Marksman Winchesters, providing a system with a storage potential of 320 MB, in a minimum of space. *Continued on next page*

Century Marksman drives: Because it's a jungle out there.

In the world outside the computer room, computer data faces constant danger.

The people out there smoke cigarettes and spill coffee. They raise dust and trip over power cords and do everything else no one would do inside the computer room.

Earlier generation disk drives just can't protect data from that kind of abuse.

But Winchesters can. A Winchester's sealed design makes it the perfect choice for any outsidethe-computer-room application: Word and data processing, computer graphics, networked data storage, data entry, computerized numerical control and any other hostile environmental applications you can think of.

But ruggedness isn't the only advantage you get with a Winchester. There's also the massive storage capacities ranging up to hundreds of megabytes per drive. Which means you can build in a system's capacity to grow.



And finally, there's the Century Data Marksman Winchester. It combines all of these advantages with the lowest cost per megabyte in the industry. So before you send any system out into the world beyond the computer room, be sure it's equipped with a Century Marksman Winchester.

back-up. Continued from first page

A storage system independent of the CPU.

But back-up isn't nearly all our new formatter offers. You also get an independent data storage package that doesn't tie up valuable CPU time.



The formatter permits independent communication among all its interconnects: From disk to tape. Tape to disk. Or either drive to and from the CPU.

Which means operators can continue to use the CPU during back-up, and even interrupt the Winchester-tape intercommunication to pull out or insert data from the disk. Without specifically shutting down and restarting the back-up functions.

The advantages of streaming tape.

Compatibility with streaming tape back-up is another big plus of the new Century formatter. As a removable media, ¼-inch streaming tape is ideal for archiving data. It's also a low-cost, high-performance, no-maintenance tape option perfectly matched to the speed and capacity of a Winchester.



Available now.

Best of all, our new formatter isn't just a promise of something to come. It's available now, right along with our full line of Marksman Winchesters and full application notes.

So if you're an OEM, systems integrator or distributor, let's get together soon. And get the problem of Winchester back-up off your back once and for all.

Sidewinder is a trademark of Archive Corp.; Quarterback is a trademark of Cipher Data Products; Streamer is a trademark of Data Electronics Inc.; CP/M and MP/M are registered trademarks of Digital Research, Inc.; Unix is a trademark of Bell Laboratories; and Multibus is a trademark of Intel.

Century Winchesters don't crash, they land.

You've heard of crashed disks before. But you've probably never heard of one in a Winchester.

That's because Winchesters rarely crash. And at Century Data, we take special pains to make sure of it.

In addition to the standard protection of disk lubrication and feather-light heads, we've designed a unique braking system and special head landing zones where no data is stored.

During a power failure or reduction, the brakes automatically slow the disk in seconds rather than minutes. And the head is programmed to seek out it's special data-free landing zones.

The combination not only prevents crashes, it virtually insures the data's integrity even if the landing is a little bumpy.

We've also taken precautions against heat related soft data failures those instances when you can't find data because temperature differences cause the disks to expand or contract unevenly.

We've developed a forced-air interdisk cooling system that uses a ventilated spindle and several air circulation paths to keep temperatures uniform throughout the sealed drive.

So when the disks expand or contract, they remain in the same physical relation to each other. And simply can't cause soft data errors.

Braking systems, landing zones and ventilated interior design. Three critical innovations that are part of our continuing commitment to no-risk Winchester design for the OEM industry.

Q: Why have you chosen Trident removable-pack drives for Japan, Mr. Kato?

A: Because of Century's design and commitment to quality.

Mr. Atts Kato is U.S. Manager for NELCO, the electronics subsidiary of Nissho Iwai — one of the largest international trading companies in Japan. The following is excerpted from an interview with Mr. Kato:

Q: After reviewing other manufacturers of removable-pack drives, what has brought you to Century?

A: Frankly, I've never seen such advanced facilities as Century's.

I've been involved in the computer business for twenty years, and have visited many U.S. computer companies. Century Data facilities for engineering, manufacturing and testing all indicate a serious commitment to disk drives.

This was a very important factor for me in selecting a manufacturer — one that can make hundreds of drives like Century has done for me.

Q: How are these drives being used in Japan?

A: We often sell the Trident drives to OEMs and systems houses, but we have other large end-users that buy quite a few. For example, Tokyo Electric Power, which is the largest utilities company in the world, and many Japanese broadcasting companies.

You see, the Japanese market situation is very similar to that of the U.S. Removablepack drives are seen as hav-



ing many desirable features, particularly storage capacity and removability. Winchesters are just now seen as becoming a good product to integrate into systems.

We see our disk business changing to Winchesters over the next few years, and this was another key reason why Century capabilities were so important to us.

As our demand for Winchesters grows, we will look upon Century to fill this need—particularly with their new products becoming available now and in the near future.

NELCO covers the entire Japanese computer market, offering individual components as well as totally integrated systems with extensive technical support capabilities for both hardware and software. And NELCO has chosen Trident removabledisk drives from Century Data Systems.

Now media compatible.

Our 300 MB Trident now provides full plug and media compatibility with other SMD-interface removable-pack disk drives. Now, Tridents can be integrated into systems without losing access to existing disk libraries.

If you would like to find out more about our proven drives and these attractive features, contact us at our address below, or feel free to give us a call.

 Intelligent Marksma Marksman Winchest Trident Removable- I would like an evaluer 	n Backup Package er Disk Drives Pack Disk Drives ation unit of the above.
Name	Title
Company	9
Street	
City/State	Zip
Phone ()	
Send to: Century Data S	ystems, 1270 N. Kraemer Blvd., Anaheim, CA 92806
	CD
	CIRCLE 8 ON INQUIRY



Century Data Systems 1270 N. Kraemer Blvd. Anaheim, CA 92806

North American Headquarters (714) 632-7500

MICROPROCESSORS/ MICROCOMPUTERS

DEC compatible computer systems and controller

Super Scorpio computer systems contain 7.5M-byte 5.25" Winchester drive, and controller that is software compatible with the DEC RK05. Software emulation provides 3 logical units, each formatted to 2.5M bytes. A 5.25" floppy disk drive and controller furnish 900k bytes of backup capacity. System can be configured with a DEC LSI-11/2 and 64k bytes of RAM, or an LSI-11/23 with up to 256k bytes of memory. The BP44 backplane and card cage allow system packaging in desktop enclosure measuring 15.5" x 6.75" x 15" (39.4 x 17.15 x 38 cm). Combination backplane and card cage accommodates 8 dual-size or 4 quad-size LSI-11 modules. There are 22 address bits supported in the bus structure; unit can be used with modules supporting 4M-byte memory. BP44 is a replacement for DEC H9270. Unit can be mounted vertically or horizontally, and fits into a 5.25" RETMA chassis. Card cage construction provides significant rf shielding. Super Scorpio OEM quantity pricing begins at \$6325.

Hard disk controllers for LSI-11 based systems include model MWV11 5.25" Winchesters, model WNV11 8" and 14" Winchesters, and model SMV11 SMD type drives. The controllers employ bit-slice microprocessors for easy adaptation to various models of disk drives. Controller models are available as component modules that can be user integrated into existing LSI-11 configurations. The SMV11 can control 2 drives of up to 300M-byte capacity each. Software compatible emulations available include DEC RP02, RL02, RM05, RK06, and RK07 formats. The WNV11 controls up to 4 Priam compatible 8" or 14" Winchester disk drives. The MWV11 version interfaces up to 4 Seagate compatible 5.25" Winchesters. Pricing in OEM quantities is \$1625 for SMV11, and \$1300 for WNV11 and MWV11. General Robotics Corp, 57 N Main St, Hartford, WI 53027.



See at Booth 4542

Low cost multi-user microcomputer family



Series 5 microcomputers incorporate advanced micro-Winchester hard disk technology in a system that allows 3 users to share a common data base. Compatible with CP/M, MP/M, and OASIS operating systems, computers are housed in desktop cabinets measuring 13.5" x 16" x 6" (34 x 41 x 15 cm), and weighing 25 lb (11 kg) each. Systems feature 4-MHz Z80A CPU with 196k RAM in 3 blocks of 48k bytes, and a 4th block of 48k reserved for utility and operating system programs. Double-density, double-sided flexible disk drive (photo left), 4 RS-232-C I/O ports, and a parallel I/O port come with the system, which can be field upgraded with an additional 5M-byte micro-Winchester disk drive (photo right).

Multitasking family serves word processing, general accounting, engineering calculations, and business forecasting applications simultaneously. One serial port can be configured as an 800k-bit multidrop network port, while another can be configured for asynchronous or bisynchronous communication. Serial ports have independently selectable baud rates. The family also offers direct memory access and parity checking, which notifies users of RAM problems.

5-15D, with dual 5.25" flexible disk drives storing 1M byte each, costs \$3990; series 5-5D features 5M-byte, 5.25" micro-Winchester backup by a single floppy (1M-byte) drive, and costs \$6990. Workstations are priced at \$2000 each. Altos Computer Systems, 2360 Bering Dr, San Jose, CA 95131.

See at Booth 1114

Circle 470

Desktop timesharing processor

Based on Motorola's MC68000 chip, AM-100/L processor runs Alpha Micro's multitasking system for 1 or 2 users. The desktop unit supports a 5.25" Winchester disk; larger systems use 8" and 14" disks, with storage expandable to 2.4G bytes. Up to 8M bytes of internal RAM and 64 terminals and printers can be supported, depending on application. CPUs link to form larger network configurations. Alpha Micro Operating System (AMOS) and Alpha BASIC compiler have been converted to run the AM-100/L CPU. Software applications are immediately available to MC68000 based systems. Alpha Micro, 17881 Sky Park N, PO Box 18347, Irvine, CA 92713.

See at Booth 5512

MEMORY SYSTEMS

8 " cartridge disk drive supplies 16M-byte removable/33M-byte fixed storage

The C2048 offers high performance and capacities, plus low physical space requirements, power consumption, and cost. An embedded servo on the removable media improves signal to noise performance, which in turn allows greater data storage capacity.

To control heat generated within the drive, the ventilated spindle concept originally used in Marksman series Winchester drives has been incorporated. This ventilated spindle evenly disperses air over the drive's disks, thus reducing temperature differences from disk to disk, reducing offtrack error, and improving data integrity. Additionally, because each sector contains track positioning information, shifts in track positioning due to head nonalignment and thermal effects are virtually eliminated. A purge cycle keeps the recording environment free of contaminants, cleaning the area around the cartridge and heads with double filtered air after cartridge loading.

Failsafe mechanisms incorporated in the unit include one which allows the drive to power-up only after the cartridge is properly seated. Another automatically returns the cartridge to lock position on power-off, eliminating human error. The Winchester disks use lightly loaded heads with a small slider profile on railed air bearings in a sealed environment. The slider is formed of calcium titanate with a manganese zinc core, and is capable of handling 480 tpi. Heads are affixed via a single contact point to the flexure and land on the lubricated media prior to flying.

The unit encompasses both dedicated and embedded servos. The dedicated servo allows for coarse track positioning, clocks, velocity feedback, and sector position data. The embedded servo serves for fine track positioning. Embedded servo data is preformatted in the part of the fixed size sector that is reserved for head and gap scatter. The sector header part of each track is available to the user. The user has full format flexibility except for the number and location of sectors.



Drive electronics use a motherboard concept that acts as a centralized hub. Read, write, and microprocessor boards plug into the motherboard. The 6802 on the microprocessor board takes care of drive functions such as track crossings, spin motor control, purge cycle, fault detection, diagnostics, and operator interface.

Dual-port capability is supplied on the SMD adapter. The basic drive has a dual hub that can address two drives. Data transfer rate is 1.2M bytes/s. Seek times are 8, 30, and 55 ms, respectively, for minimum, average, and maximum. MTBF is said to be 6000 h. Century Data Systems, 1270 N Kraemer Blvd, Anaheim, CA 92806.

See at Booth 5035

Circle 472

Cache disk subsystem

Model 5070C fixed record length cache disk keeps frequently used data from the disk subsystem and high speed solid state memory, reducing data access time significantly. It attaches to any IBM 3830 or 3880 control unit, or equivalent. If disk subsystem is initialized for fixed length records, it will support all IBM operating systems governing the control units. Std cache size is 2M bytes, expandable to 16M bytes. Three modes of operation are offered: full caching, write through, and bypass. Basic system, including dual control processors, 4-channel interface, and 2M-byte cache memory, is \$139,200. Amperif Corp, 21345 Lassen St, Chatsworth, CA 91311.

See at Booth 8328

Circle 473

SMD compatible 14 " multiplatter disk drive



Large capacity, fast access disk drive, Atlas, stores 80M to 100M bytes. Multiple heads and advanced head positioning techniques permit access times under 20 ms. Data are accessed in continuous 1M-byte sections via logical cylinders organized in 1M-byte increments. Three moving head bars serve each of the 6 surfaces; there are 72 heads on device, 4 heads/bar. Platters and heads are contained in a sealed chamber and require no preventive or periodic maintenance. Modular drive design ensures short MTTR; design life is 10 years. Package is std 19" (48-cm) rackmount, 7" (18 cm) high and 24" (61 cm) deep. Integral dc power supply, chassis slides, and interface manual are included. Quantity-100 price will be under \$6000. **Alpha Data, Inc,** 20750 Marilla St, Chatsworth, CA 91311.

See at Booth 6018

Demanding Electronic Applications Demand ULTEM Resin

Design With ULTEM Resin's Unprecedented Combination Of Exceptional Properties

Exhaustively tested and field proven, ULTEM polyetherimide resin is technology years ahead of its time. A unique amorphous thermoplastic that delivers extra high performance through a range of properties never before available in a single material.

ULTEM resin is the answer for today's exacting design and engineering challenges. With 400°F heat resistance to withstand wave and vapor phase soldering. Outstanding dimensional stability for close point-to-point tolerances without warping, plus ductility for intricate, snap-fit designs. An exceptionally low dissipation factor for minimum energy loss. And, remarkably easy processing on conventional equipment.

Get the full story on ULTEM polyetherimide resin. There's never been anything like it for reliability and performance.



GENERAL ELECTRIC COMPANY PLASTICS OPERATIONS ULTEM PRODUCTS SECTION ONE PLASTICS AVENUE PITTSFIELD, MA 01201 (413) 494-6109/6130



CIRCLE 80



Now PDP-11/23 users can expand memory beyond 256KB, maintain software compatability and use existing peripherals and controllers!

Another Technically Advanced Solution From Monolithic Systems.

Our engineers have developed a practical, cost-effective way to increase PDP-11/23 memory beyond 256Kb. Our new **Buccansers** MSC 8702 extends the ad dressability of the LSI-11/23 microcomputer from 18 to 22 bits, transparently, while maintaining compatability with RSX-11M version 3.2, RSTS/E version 7.0 and the large array of existing LSI-11/23 peripheral controllers. No software drivers or patches have to be written.

In addition to allowing the user many peripheral options now available, the MSC 8702 provides additional slots to accommodate new 22-bit DMA controllers, giving the MSC 8702 a long, useful life.

Consider Your Options

Of course you can increase your system performance by other means. You could move to a PDP-11/24, but that would require new peripherals. Or you could purchase a PDP-11/23 PLUS, but that would require new peripheral controllers. Currently, only one 22-bit device is available from DEC for that system. After you consider your

DEC PDP-11/23, PDP-11/23 PLUS and PDP-11/24 are registered trademarks of Digital Equipment Corporation.

MSC 8702 Description and Capacity

MSC 8702 FEATURES	8702-01	8702-03	
LSI-11/23 CPU with memory MGT	X		
512Kb parity memory	X	X	
Peripheral bus map	X	X	
3 bus grant cards	X	X	
6 x 9 back plane	X	X	
300 watt power supply	X	X	
Dual cooling fans	X	X	
Power sequence module/line time clock	X	X	
Multifunction module with 2 serial ports	x	A start	

CAPACITIES

□ Expansion to 4 megabytes of parity memory

- □ 5-quad and 1 dual high 18-bit peripheral slots
- □ 3-dual high 22-bit DMA slots

options, you will agree that there is really only one practical and economical way to increase your PDP-11/23 performance: the MSC 8702.

The Bottom Line The MSC 8702's ability to expand

your system capabilities while maintaining complete software compatability is impressive by itself. The clincher is the fact that the MSC 8702 is much less expensive than moving to PDP-11/24 or PDP-11/23 PLUS systems.

Questions? Contact us at

84 Inverness Circle East Englewood, Colorado 80112 Phone: 1-800-525-7661 In Europe,

Justinian Str 22, AM Holzhausen Park Frankfurt, West Germany 6000 Phone: 4961 1590061

We'll give you complete details



.means technically advanced solutions.



MEMORY SYSTEMS

Combined streaming and start/stop cartridge transport

Model 6455 operates in either streaming or start/stop mode, providing high speed disk backup while allowing normal file management operations. The company claims that this is the first cartridge transport to operate in both modes. In streaming mode, 20M bytes of data are stored or restored in under 20 min. Data blocks are written on the fly along with 1.2" (3.1-cm) interrecord gaps. In start/stop mode, unit permits consolidation of files on nonadjacent disk sectors and tracks onto a cartidge using conventional data management techniques. Once taped, individual data blocks can be edited or replaced without disturbing records written previously. Cartridges recorded in streaming mode may be read in the start/stop mode, and vice versa.

Using serpentine recording, the 4-track transport handles std 3M type cartridges. Tape lengths of 300', 450', and 600' (91, 137, and 183 m) give unformatted capacities of 11.5M, 17.3M, and 21.3M bytes, respectively. Writing and reading speeds are 30 ips; rewind occurs at 90 ips. Data transfer rate is 192k baud.



Transport employs self-clocking group code recording with a 6400-bpi recording density and read after write heads. Start/stop time is 25 ms at 30 ips and 75 ms at rewind speed. Unit stops, reverses at high speed, and rewrites a 2k-byte record in 228 ms. Embedded Picobus formatter is compatible with 6450 transport and model 7300 8" 40M-byte Winchester disk drives.

Servo board contains circuits to monitor capstan motor current. Solid state infrared tape position sensor, which is immune to ambient light, ensures absolute BOT and EOT signals. Positive cartridge detent, along with center balanced spring loaded servomotor mount, allows the drive to be operated in any position.

Unit offers a 1×10^{10} soft error rate and a 1×10^{11} hard error rate. MTTF is over 5000 h, while MTTR is under 30 min. With envelope equivalent to an 8" floppy drive, the transport measures $8.5" \times 4.5" \times 14"$ (21.6 x 11.4 x 36 cm), including

embedded formatter and servo control board; weight is 5 lb (2 kg). Power requirements are 5 Vdc at 3 A and 24 Vdc at 1.5 A. Dissipation is 21 W idle, 27 W while reading or writing, and 31 W during rewind/track select. With embedded formatter, single unit costs \$1700; in OEM quantities, cost is \$950 each. Kennedy Co, 1600 Shamrock Ave, Monrovia, CA 91016.

See at Booth 1600

Circle 476

5.25 " floppy disk replacements use high performance, thin film media

Formatted capacity up to 40M bytes in the form factor of a 5.25" floppy drive, family 5xxx uses plated disk media to provide recording density of 350 tpi and 16k bpi. Family includes series 55xx, with data rate of 5M bytes/s, targeted as a 5.25" floppy disk replacement model. The 58xx series runs at 8.2M bytes/s and is aimed at an unconstrained data rate market. Formatted capacities range from 10M to 40M bytes on from 1 to 4 platters. Form factors are identical among all drives. The drives use a brushless spindle motor with fast acceleration and improved dynamic brake, to ensure that the head is in contact with media for a shorter time while the disk is rotating, thus reducing wear. Although plated media is used on disk, the drives currently employ ferrite heads. Drive actuator circuitry of the family is open loop under microprocessor control. Microprocessor controls the 5-phase stepper motor, and handles temp compensation circuitry during track shift due to temp changes. Steps are divided into microsteps, which the microprocessor can adjust dynamically for minor track alignment adjustments. Drives also contain temp sensors and algorithms for compensation. Microprocessor stepping control also allows "ramped seeking" by buffering steps needed to reach a given track. Algorithms can then perform an electronically damped arrival time by outputting the first steps rapidly, and then slowing the step rate as the head approaches the proper track. Head overshoot and settling time are reduced for faster track access. Series 5xxx also contains a preamplifier on the actuator arm which, in conjunction with other circuitry, suppresses microprocessor noise. Drives contain isolated subframe shock mounts. Attachment points and interface connectors conform to industry standard. Evotek Corp, 1220 Page Ave, Fremont, CA 94538.

See at Houstonian Hotel, Presidential suite

Circle 477



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CIRCLE 82

APPLICATION	UNIT	PRICE	OUTPUT 1	OUTPUT 2	OUTPUT 3	OUTPUT 4	ONE	CONDOR	SIERKACIN
WINCHESTER	FD384	112.00	+5V,9A	-5V or-12V, 0.8A	+24V, 0.7A/ 4.5A PK.		CP384	FNBB-118	
	FD340	39.00	+5V, 0.5A/ 0.7A PK.	+12V, 0.9A/ 1.8A PK.		<u> </u>	CP340	FAA-512	2BXFD
LOPPY DISK	FD323	61.00	+5V, 2A	+12V, 4A			CP323	FBB-512	2BBXFD
	FD205	76.00	+5V, 1.0A	-5V, 0.5A	+24V, 1.5A/ 1.7A PK.		CP205	FBAA-45W	2DFD***
FLOPPY DISK	FD206	97.00	+5V, 2.5A	—5V, 0.5A	+24V, 3.0A/ 3.4A PK.		CP206	FCBB-90W	2PFD
	FD162	89.00	+5V, 3.0A	-5V, 0.6A	+24V, 5.0A/ 6.0A PK.		CP162	FNBB-140W	2PFD***
PERSCI	FD272	69.00	+5V, 1.7 A/ 2.2A PK.	-5V, 0.15A/ 0.2A PK.	+24V, 0.2A/ 3.0A PK.	7-10V UNREG 1.2A/10A PK.	CP272	N/A	2PRD

*** Not Direct Equivalents

MEMORY SYSTEMS

Reduced height diskette drive



SA200 MinifloppyTM diskette drive, for personal computers, memory typewriters, word processors, terminals, and printers, has single-density unformatted capacity of 125k bytes/disk, and 81.7k bytes/disk of formatted capacity. Double-density/ track capacity is 6.2k-byte unformatted and 5.1k-byte formatted. Track to track access time is 26 ms. Single-density transfer rate is 125k bps, recording density is 2768 bpi. The drive is interface compatible to SA400/450 family and all dc motors to accommodate worldwide power requirements. Height of 2.05" (5.2 cm) is more than one-third lower than the std 3.25" Minifloppies, achieved through use of low profile dc drive and stepper motors. Drive motor automatically shuts off the drive when not in use to reduce media wear. Electronics are packaged on 1 PCB containing index detector circuits, head position actuator driver, write current drivers, read amplifier and transition detectors, write protect, and drive select circuits. Head positioning actuator positions the read/write head to desired diskette track. The dc drive motor rotates the spindle at 300 rpm through a belt drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange. Read/write head assembly is positioned through use of a precision spiral cam. Cam has a V-groove with ball bearing follower attached to the head carriage assembly. Track location is accomplished as the cam is rotated in discrete increments by stepping motor. Read/write head is ceramic with straddle erase elements to provide erased areas between data tracks. Drive also features removable faceplate which also increases available space. Drive is designed to fit under CRT keyboard. It can be tilted at 10° angle without affecting performance. MTBF is 8000 POH at 15% duty cycle. Op temp is 4.4 to 46.1 °C. Voltage dc requirements are 12 V $\pm 5\%$ at 0.77 A typ; and 5 V $\pm 5\%$ at 0.24 A typ. Power dissipation is 10.5 W during continuous operation; 6.3 W at power down; and 2.8 W in standby mode. Unit measures 5.75" x 2.05" x 8.0" (14.6 x 5.2 x 20.3 cm) Shugart Associates, 475 Oakmead Pkwy, Sunnyvale, CA 94086.

See at Booth 3512

Microprocessor controlled digital cassette recorder

Model 6440 Raycorder II digital cassette recorder has microprocessor based control system that continuously monitors and regulates tape speed and tension, and ensures uniform start/stop profiles. Reel drive cassette transport is designed with all major structural components molded of thermoset plastic materials for high stability and strength. Inserted cassette is constrained within a precision head guide assembly mounted in the door. When door is closed, cassette engages reel hub motors and cassette positioning guides. Sensing is provided for tape leader, load point, early warning, cassette in place, side A/B, and write protect. Constant tape speed and tension are controlled by system's incorporated optical sensors, located on each motor shaft, which provide velocity information. Tape velocity can be calculated and controlled by knowing the amount of tape in cassette and relationship between the 2 varying hub diameters as tape is transferred from hub to hub. Microprocessor monitors velocities, performs necessary calculations, and controls voltage applied to the take-up motor for uniform velocity over the length of the tape. Tape tension and start/stop profiles are also constantly adjusted depending on tape position and relative hub diameters. The system ensures constant tape tension and uniform start/stop profiles at any point of tape travel. Tape speed is 30 ips transfer, 60 ips search. Power requirements are \pm 12 Vdc, 850 mA; -12 Vdc, 100 mA; and 5 Vdc, 370 mA. Transport assembly measures 4.5" x 5.5" x 3.75" (11.4 x 14.0 x 9.53 cm). Unit weighs 2 lb (0.91 kg). Raymond Engineering Inc, Raycorder Products Div, 217 Smith St, Middletown, CT 06457.

See at Booth 7004

Circle 479

Multi-user Winchester system

System 6809 supports up to 4 terminals and features a 2-MHz CPU, 120k-byte static RAM, 19M-byte (unformatted) 5.25" Winchester hard disk, 1M-byte (unformatted) 5.25" floppy disk, and 4 serial I/O ports. Memory is expandable up to 632k bytes. Additional memory, mass storage capacity, and I/O for additional terminals and peripherals are optional. System can select between 2 operating systems, under software control, during software development. System includes 0S-9 level 2, a UNIX-like, multi-user, multitasking OS, and the OS-9 debugger, text editor, and assembler. Languages available for OS-9 include BASIC09, Pascal, CIS COBOL, and C. GMXBUG/FLEX monitor/operating system combination, a single-user 56k-byte operating system capable of running any software written for FLEX, is also included. **Gimix Inc**, 1337 W 37th Pl, Chicago, IL 60609.

See at Booth A101

Circle 478

Circle 480



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DATAROYAL

INCORPORATE

CIRCLE 83

MEMORY SYSTEMS

Removable-only 5.25" Winchester drive

Micro-Magnum 5 removable 5.25" Winchester drive uses proposed ANSI std disk cartridge and employs basic technology of the company's Micro-Magnum 5/5 fixed/removable 5.25" Winchester. The drive can be used as backup for 5.25" fixed disk Winchesters, and as an 1/0 device. Used as a multiple drive system, it provides mass storage redundancy and ability to keep a file online.

Unformatted storage capacity is 6.75M bytes; formatted capacity is 5M bytes. There are 306 tracks, plus 5 alternate tracks, with density of 454 tpi. Each of 33 sectors/track (including 1 spare) contains 256 data bytes, plus format and embedded servo data for accurate track positioning. Other drive characteristics include 40-ms average access time, 5M-bps data rate, less than 90-s copy time for 5M bytes, and recording density of 8600 bpi. Track position data are prerecorded on disk. In operation, a closed loop system directs head to target track using servo data in conjunction with voice coil motor. CushionAireTM read/write heads never contact media and are dynamically loaded and unloaded from rotating disk. Heads are retracted off media and latched into rest position when not in use.

Cartridge has door that closes head opening, and clamp that secures disk hub to cartridge housing, to prevent contamination when cartridge is outside drive. Within drive, door closes to seal heads inside clean air system after they are retracted from cartridge. Double-door system excludes contaminants from head disk interface. DMA Systems Corp, 325 Chapala St, Santa Barbara, CA 93101.



See at Booth A843

Circle 481

DEC compatible disk system with tape backup

CSS-800 mass storage subsystem contains 35M- or 70M-byte Winchester disk drive with 17M-byte cartridge tape drive for backup. System includes 2 integral controllers with multiported memory for simultaneous disk and tape operation. Compatible host interfaces for Q-bus, UNIBUS, or MULTIBUS are provided. In DEC compatible configurations, system emulates DEC RK07 disk and TE-16 tape drives. Proprietary



microprocessor controlled dual-port cache memory gains 45% increased data throughput over typ disk systems by reading complete tracks without sector interleaving. Up to 95% improved data transfer rate is achieved by cache management table that remembers most commonly used data, and stores it in cache. Lookahead buffering improves data rate by 50% in sequential disk operation. Read/write errors are detected up to 8 bits and corrected with ECC. System has selfcontained diagnostics that check peripheral devices and controller. When bad disk sectors are found, system's intelligent disk controller relocates and records location of data, all transparent to host. Diagnostics are initiated by front panel switch; test results are displayable on front panel LEDs and are accessible from host. All errors are automatically logged. Price in quantity 100 for 35M-byte system is \$9300; 70M-byte system is \$10,300. U.S. Design Corp, 5100 Philadelphia Way, Lanham, MD 20706.

See at Booth M252

Circle 482

0.25 " cartridge tape system and controller

TFS 903 0.25" tape system provides up to 21M bytes of storage for DEC LSI-11 computers, recording in GCR for high capacity and integrity. Also shown will be TFC 922, a dual-density PE/NRZI magnetic tape controller on a single quad-board. Tape system and controller are both software compatible with UNIX and all DEC operating systems. Controller interfaces any industry std 0.5" tape drive to the LSI-11 computers, and generates IBM compatible tape. Quantity-1 price for TFS 903 system is \$3900; TFC 922 controller costs \$3300, and TFS 922 tape system is \$7900. Aviv Corp, 6 Cummings Pk, Woburn, MA 01801.



See at Booth 8128

Circle 483

Would you like your minicomputer terminals to:

1. Transmit data error-free at up to 9600 bps? 2. Operate dial-up at 2400 bps or 4800 bps?

3. Automatically recover from phone line errors?

If you are a minicomputer user, chances are that your "dumb" asynchronous terminals have kept you from using your system to best advantage, simply because they were never designed to do what you'd like them to do.

For example, have you been limited to 1200 bps or slower data communications rates because faster speeds demanded synchronous modems? No more. MICOM's Micro500 performs the asynch to synch conversion you need to use those faster modems, plus error correctionall transparently.

Has fast dial-up operation been impossible because dial-up modems are half-duplex and your dumb terminals need full-duplex support? Not to worry. The Micro500 performs full- to half-duplex conversion too-again without any changes to your hardware or software.

Or have communications errors been a problem? (If they haven't at 300 bps or 1200 bps, they surely will be at the faster speeds.) The Micro500's automatic retransmission on error assures you of error-free data every time.

Consider the Micro500 to be inexpensive add-on intelligence for your dumb terminals. It does a lot for very little. Call or send today for an 8-page brochure describing the Micro500 and its applications, and forget about those "dumb" limitations.



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WHICH WOULD YOU RATHER READ ALL DAY?



Unretouched photos-identical conditions

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Our competitor on the right claims high resolution. But what about that glare? The washed-out background? And the black and white screen? It's enough to give you a headache.

The TeleVideo terminal on the other hand, with its finer character dot matrix, sharper background contrast, and a black-on-green non-glare Panasonic screen is much easier on the eyes.

Obviously.

Every TeleVideo terminal has just four basic modules. Each module is the best that can be made.

Every screen, keyboard switch, power supply and video module on every TeleVideo terminal is identical. For the same high reliability. And same ease of service. None of our competitors can say that.

If you order 200 terminals today, we can ship them tomorrow. If you order 500, we can still ship them tomorrow.

And if you order a 1,000, well, 920C maybe you'll have to wait a day or two.



We put our terminals through five bad days so you'll never have even one bad day.

Our terminals are designed to withstand heat up to

California Santa Ana 714/557-6095; Sunnyvale 408/745-7760; Georgia Atlanta 404/255-9338; Texas Dallas 214/980-9978; Illinois: Chicago Area 312/351-9350;

The 910

PLUS
THIS IS NOT A TELEVIDED TERMINAL. THE SIMILARLY-PRICED TERMINAL ON THE LEFT IS.

WHICH WOULD YOU RATHER READ ALL DAY?

rather read all day?

155°F and shocks that simulate being tossed in the back of a truck. And before any terminal reaches you, every major component goes through a five day series of thermal and power-on cycling tests.

The

925

The result?

The highest reliability rate in our industry.

TeleVideo sells 50% more terminals a month than our nearest competitor.

Three years ago, TeleVideo shipped its first terminal. Today, we're the number one

Boston 617/668-6891; New York/New Jersey 201/267-8805;

independent terminal supplier. One reason is because our advantages are clearly visible. 8 hours a day.

For more information call, toll-free, 800-538-8725. (In California, call 408-745-7760.) Or call your nearest TeleVideo sales office.



The

910

The

950



All TeleVideo terminals can be serviced by your nearest GE Instrumentation and Communication Equipment Service Center.

United Kingdom West End Surrey 44-9905-6464. CIRCLE 85

MEMORY SYSTEMS

Streaming tape handles IBM and ANSI formats, Winchester drives supply ANSI interface

StarStreamer 0.5" streaming tape transport features std IBM and ANSI formats for data interchange and processing, and provides 46M bytes of backup storage capacity. It incorporates std interface and format to accommodate existing software packages when operated at 25 ips. Streaming mode transfer rate of 160k bytes/s includes automatic gap extension to reduce demands on controller. Auto-diagnostics on powerup, and continuous monitoring of power and environmental controls, are featured. Precision tape handling and singletrack error correction ensure less than 1 hard error read in 200. With short tape path, only heads and tape cleaner contact oxide side of tape. Low frequency tape flutter is minimized. StarStreamer dual-density configuration provides 92M-byte capacity in streaming mode.

TrakStar family of 8" Winchester drives features ANSI interface and is available with 33M-, 67M-, and 84M-byte capacities. Model D-8033 records on 476 tpi; model 8066 and 8084 record on 952 tpi. Recording density is 8200 bpi; average positioning time is 45 ms, and data transfer rate is 8.5M bps. Voice coil rotary head positioner provides single cylinder move time under 10 ms, 80-ms full stroke, and average random access time of 45 ms. Closed loop servo system provides greater track accuracy over stepper motors. Heads, positioner, and disks are in sealed section. Electronics are external to this section and are field replaceable. MTBF for sealed section is 25,000 h. **Pertec Computer Corp, Peripherals Div,** 21111 Erwin St, Woodland Hills, CA 91367.



See at Booth 3504

Circle 484

MULTIBUS mass storage subsystems

Series 700 MULTIBUS mass storage subsystems are std 19" (48-cm) rackmounted units with 5.25" (13.34-cm) height. Each chassis can accommodate any 2 of the 3 storage devices supported, including 8" Winchester drive, 0.25" streaming tape drive, or 8" floppy disk drive. System also includes the DSD 7215 multifunction controller board that combines onboard data separation, MULTIBUS interface, Winchester controller and interface for 2 drives, streaming tape interface, floppy disk controller and interface for 4 single- or 2 double-sided drives, and noninterleaved operation on a single MULTIBUS board. Also included is DSD 5215 MULTIBUS compatible multifunction controller. Subsystem features single-board controller, pipelined operation for noninterleaved disk transfers, emulation of Intel iSBC 215 and iSBC 218 software compatibility with RMX86 and



onboard self-test diagnostics. The controller board is available separately or as part of the packaged series 700. **Data Systems Design**, **Inc**, 2241 Lundy Ave, San Jose, CA 95131.

See at Booth A549

Circle 485

PERIPHERALS

IBM compatible cluster controller

Model 209 cluster controller is compatible with IBM 3274-51C and 3276-2 computers. In addition to std IBM features, the 209 includes a 25th status line, choice of green or white phosphor screen, and interface capability with any ASCII printer. Model 315 computer terminal comes in data entry, inquiry, and standalone package options; all can be accommodated by a single 209 cluster controller. Standalone option is available with 9" or 12" (23- or 30-cm) screen. Controller communicates with IBM communications processors via multipoint BSC protocol through std synchronous modems at speeds up to 9600 baud. Daisy chain interface is planned, which will allow terminals to be connected in multidrop.

Through June 15, the company's IBM 3275-2 compatible D314 computer terminal will be available at a per-unit price of \$1995. Informer, Inc, PO Box 91054, Los Angeles, CA 90009.

See at Booth 5448

Circle 486

Portable terminal for hostile environments

EPIC 1647-201 environmentally sealed portable terminal is rechargeable battery operated and enables data collection in hostile remote environments. Waterproof terminal allows custom programming, with downloading of programs from host computer; input is via keyboard or bar code. Hard and soft display definable keys are provided, along with 4 calculator function keys. Transmission is via modem or std system party lines. A 2-line, 80-char LCD enables matching prompts and entries. User can recall data from 64k memory for display or editing. Data rate is 150 to 9600 baud. Op temp is -10 to 45 °C. **Epic Data**, 7280 River Rd, Richmond, V6X 1X5 British Columbia, Canada.

See at Booth A127

We're not just selling 50NB 5¼" Winchesters.

We're selling solutions to your customers' application problems.



For more information about our new 50MB drives, call Jim Lawson, (415) 490-3100.

PERIPHERALS

Printer and ergonomic standard peripherals

Model 4542 printer has full graphics and text printout capabilities. It provides proportional spacing, and prints in red and black, elongated or underlined. Variable size bar code and a range of char sets are also available. Model 4525/26 printers operate bidirectionally at 150 cps with up to 5 copies. A tractor mechanism feeds paper either from bottom or front. Upperand lowercase chars, parallel or serial interfaces, and either 80or 132-col format are provided.

Three computer terminals, the 4411, 4420, and 4430, are alphanumeric, asynchronous, ASCII terminals, that have been ergonomically designed. Model 4410, with fixed keyboard for CAD systems and communications with microcomputer systems, also operates as a console terminal. Model 4420 uses an enhanced mode that provides 70 application specific functions. The 4430, fully compatible with DEC VT100, shares features with 4420, including detached low profile keyboard, tiltable screen, and smooth scrolling. Facit, Inc, 66 Field Point Rd, Greenwich, CT 06830.

See at Booth 7500

Circle 488

IBM System 34 and 38 compatible printer

QMS7710/34 appears to IBM Systems 34 and 38 as an IBM 5256 printer. Connection to the IBM system is through workstation communication ports. Two twin-axial connectors mount the rear of the printer; one serves as the input port that attaches directly to the computer or another device on the cable; the other is the output port, which can cable-through to another terminal device. Unit features 8085 microprocessor print control, dual 68B00 microprocessor interface control, 1-piece universal power supply, high resolution digital positioning, and a full range of paper/forms handling options. Most printer functions are under program control, reducing parts count and improving reliability. Control panel displays printer status, and allows for access to manual control and override. Printing is initiated by a small solenoid hammer which strikes a spinning thimble against the paper. Normal print life for the thimble is 30M impressions. Device prints up to 55 cps, 132 cols/line, 10 cpi. Horizontal resolution is 120 positions/in, and vertical resolution is 48 positions/in. Acoustic noise levels are 67 dBa without covers; 60 dBa with covers. Quality Micro Systems, PO Box 81250, Mobile, AL 36689.

See at Booth M261

Circle 489

Personal workstation shares peripherals over local area network

Using the 8-MHz 68000 processor, the Concept personal workstation supplies 256k- to 512k-bytes of memory formed of 64k RAMS, a full-page bit-mapped screen, separate Selectric-style keyboard, built-in Omninet local network, and 4 expansion slots for peripherals. The processor provides a 32-bit architecture with 16-bit memory bus for high performance user interface. Large program capability is supplied by the large main memory. Mass storage is provided by 1M-byte floppy or 6M-, 11M-, or 20M-byte Winchester disks that may be centrally located or connected directly to the workstation.

A standardized user interface, the ISO Pascal based system software handles concurrent multiple outputs on the system display. The 15" (38-cm) 35-MHz monitor displays a full-page work area. Bit-mapped to supply 560- x 720-pixel resolution,



the screen is configurable horizontally or vertically. A separate 6801 processor handles the high performance local network. Operating at 1M-baud over distances of 4000' (1220 m), the network supports 64 users using simple twisted pair connections. Four 50-pin card sockets, located in a pullout drawer, are provided for peripheral connection. Floppies, modems, speech devices, mass storage units, plotters, printers, and graphics tablets are among the peripherals that may be attached.

Other standard features on the machine include 2 RS-232-C connectors, calendar clock with battery backup, 2 interval timers, and flexible sound generator and speaker. Built-in diagnostics and automatic power-on boot are also provided. Operating system software is all native code for efficiency and has no memory limitations. Both Pascal and FORTRAN compilers are provided as well as EDWORD word processor, CP/M emulation, and Constellation II network software.

Users are provided a growth path from a single-user workstation sharing central peripherals to an expanded standalone unit having 5.25" floppy and Winchester, and printer, to a complete network system having up to 63 workstations with shared mass storage, printers, and modems. A network workstation with 256k-byte memory sells in the \$5000 to \$6000 range. A standalone unit with Winchester drives ranges from \$7000 to \$8000. Corvus Systems, Inc, 2029 O'Toole Ave, San Jose, CA 95131.

See at Booth 5916

Circle 490

High performance CRT terminals

Ambassador terminals are compatible with ANSI X3/64 std coding. Touch 2000, with capacitance sensing touch input on CRT menu display, is suited to high traffic applications for noncomputer personnel. Another terminal is a 1024 x 1024 graphics system with 8 bit planes for gray scale; a larger memory plane is available. Window controller draws vectors at 800 ns/pixel. Unit has default alphanumeric character set and programmable keyboard, and is compatible with Tektronix 4012 coding. High end Guru terminal is ANSI X3.64 compatible, with selectable display formats ranging from 18 to 60 lines, 40 to 160 chars/line. Horizontal and vertical zoom and scroll display controls, as well as full editing, formatting, block or char transmission, printer output, and programmable keyboard, are std. **Ann Arbor Terminals, Inc**, 6175 Jackson Rd, Ann Arbor, MI 48103.

See at Booth 2028





LSI-11[®] compatible controller for 80-300MB CDC, Ampex and Fujitsu CMD/SMD

Dataram Corporation offers the industry's widest range of DEC-compatible peripheral controllers — from comparatively simple NRZI tape controllers to complex 300 MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11, PDP®-11, or VAX® minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and, more importantly, space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

The chart shows our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.



Princeton Road Cranbury, New Jersey 08512 Tel: 609-799-0071 TWX: 510-685-2542

CONTROLLER	DESCRIPTION	COMPATIBILITY
C03	Cartridge disk controller	RK05
C33	Cartridge disk controller	RK05
Т03	NRZI mag tape controller	TM11/TU10
T04/C	Mag tape streamer coupler	TM11/TU10
T04/N	NRZI mag tape controller	TM11/TU10
T04/D	Dual density mag tape controller	TM11/TU10
T34/C	Mag tape streamer coupler	TM11/TU10
T34/N	NRZI mag tape controller	TM11/TU10
T34/D	Dual density mag tape controller	TM11/TU10
Т36	Dual density mag tape controller	TM11/TU10
T34/T	GCR mag tape controller	TM11/TU10
S03/A, S04/A	80 MB/300 MB SMD controller	RM02/RM05
S03/A1, S04/A1	80 MB/160 MB SMD controller	R M02
S03/B	80 MB/300 MB SMD controller	RK07
S03/C	200 MB/300 MB SMD controller	R P06
S03/D, S04/D	96 MB CMD controller	RK06
S33/A	80 MB/300 MB SMD controller	RM02/RM05
S33/A1	80 MB/160 MB SMD controller	RM02
S33/B	80 MB/300 MB SMD controller	RK07
S33/C	200 MB/300 MB SMD controller	RP06
S33/D	96 MB CMD controller	RK06
Products printed	in red are LSI-11 Bus compatible.	

Products printed in red are UNIBUS® compatible for PDP-11 and/or VAX minicomputers.

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PERIPHERALS

Bidirectional impact matrix printer offers choice of speed and print quality

Varityper printer model \$700 uses the patented infinite matrix principle to provide various speeds and print qualities on demand. The unit is designed to switch easily from fast draft quality print to slower, higher quality correspondence quality output. Using a 7-pin printhead, the bidirectional impact printer produces a 4-pass letter quality font at 32 to 58 cps, 2-pass correspondence quality at 65 to 195 cps, and single-pass draft quality at 220 to 390 cps. In letter mode, the printhead passes over the same line of print 4 times at 13 ips, making a minute paper advance between each pass. In draft mode, it makes 1 pass over the line at 26 ips. To produce quality equal to that of dot matrix units featuring dot overlap, intermediate mode causes the printhead to make 2 passes over the line at either 26 or 13 ips with a minute paper advance between passes.

The operator has complete control over the page format through commands inserted in the text to be printed and executed by the printer rather than the host computer. Commands control top, bottom, left and right margins, line lengths and spacing, indentation, tabulation, and justification. They also control centering, boldface, underlining, and switching between character sets and typestyles, print speeds, and quality levels.

The mechanism can print up to 960 horizontal increments/ in, including character densities of 6, 10, 12, and 15/in. It can handle up to 288 vertical increments/in including line increments of 6, 8, and 12/in. Type faces include all standard alphabets as well as major languages; proportional spacing; graphics; machine readable, scientific and math, and special applications such as dental and APL. Paper can be cut sheet, fanfold, or continuous rolls in widths up to 14.875" (37.78 cm). A bidirectional forms tractor and single- or dualsheet bin feeder can be attached for forms handling.

Models are available for most interfaces. The RS-232-C serial interface accepts characters at speeds to 9600 baud and has a 2048-char input buffer. Available parallel interfaces are compatible with most commonly used matrix and daisywheel printers. In quantities of 10 to 24, the printer sells for \$3100/unit. Font packs are priced at \$125 each in 1 to 5 quantities. Sanders Technology, 9 Columbia Dr, Amherst, NH 03061.



Add on intelligence for dumb terminals, inverse multiplexers



Microson model 596 error controller operates dumb terminals error-free at speeds to 9600 bps on dial-up or leased lines. Extended functions include automatic retransmission on error, asynch to synch conversion, full- to half-duplex conversion, and data compression. With the peripheral, users of asynchronous TTY compatible terminals can transmit data synchronously at up to 9600 baud; convert to half-duplex mode to access the dial-up network; access Viewdata and Teletex networks with asymmetrical data rates, and automatically recover from phone line errors. Switch settings control options such as full- or half-duplex, local echoplex, data compression, and 2 types of buffer overflow control. Data rates are also switchselectable, including 600, 1200, 2400, 4800, and 9600 baud, and receive/send combinations of 1200/75 and 600/75 bps. The peripheral is typically priced at \$795.

Additions to the Micro100 line multiplexer series can support data rates to 64k bps. Units split a single high speed data stream onto as many as 6 slower communications lines, using modem speeds of 4800 or 9600 baud, or up to 4 lines operating at 14.4k or 16k baud. Higher data rates make it possible to back up 56k-baud DDs facilities using only four 14.4k-baud analog lines, instead of six 9600-baud lines, as previously required. The multiplexers provide an economical alternative to wideband circuits by allowing for expansion in increments as small as 4800 baud. Special capabilities allow continuation of full-duplex operation at reduced speed without interruption, even when 1 telephone line is cut. When the failed line is returned to service, device automatically returns to higher speed transmission. Typical price for 2-channel unit is \$4300. High speed operation at 14.4k or 16k baud is a no-cost option. Micom Systems, Inc, 20151 Nordhoff Ave, Chatsworth, CA 91311.

See at Booth M103

Circle 493

Computer peripherals and 16-bit micro introduced to U.S. market

Over a dozen computer products established in Japan will be introduced to the U.S., including line, serial, and terminal printers; display monitors; disk drives; and a 16-bit microcomputer based on Intel's 8086 CPU. Line printers are available in 1250-, 600-, 300-, and 200-line/min versions. The 1250-line/min band printer has a 64-char set, OCR scannable print quality, and 132-col format. Other line printers generate compressed and enlarged chars, special symbols, graphics, and bar codes in both ASCII and international char sets, and are available with 7 x 9 dot matrix at rates of 300 and 600 lines/min. *(continued on page 155)*

150

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Model	Size (Inches)	Voltage	Ampere Hour	
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5PMP	1.2 x 1.5 x .33	3	1.000	
5PMS	1.2 x 1.5 x .33	6	.500	



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PERIPHERALS

Two band printers operating at 200 and 300 lines/min offer 64-char set and 80-col format. Generating near letter quality alphanumerics, symbols, and graphics, a serial matrix printer runs up to 110 cps in a 21-x 16-dot pattern. A thermal matrix printer for char and graphics applications produces an 80-col format at 25 dot lines/s, and comes with a Centronics compatible interface.

Also exhibited will be a high resolution page display monochrome monitor for word processing and graphics applications, along with a 19" (48-cm) color monitor that is capable of 714 x 416 resolution for graphics applications. Three disk drive systems offer storage capacities of 120M, 10M, and 6.66M bytes. The 8" rigid disk storage module holds 120M bytes on 6 fixed disks. Offering 75-ms avg access time, the two 5.25" Winchester drives maintain 10M and 6.66M bytes, respectively.

Intended for small business applications, the 16-bit KDS-7860 microcomputer system accepts MULTIBUS compatible peripherals, and runs CP/M and MS-DOS operating systems. Memory, storage, interface, display, and peripheral options include color graphics and voice synthesis. **Nissei Sangyo America**, Ltd, 40 Washington St, Wellesley Hills, MA 02181.

See at Booth 1629

Circle 494 Corp, PO Box 3444, Englewood, CO 80155.

Circle 496

OCR, bar code distributed demand printer



LTP printer produces OCR and bar code print on labels, tickets, or tags. It receives ASCII code over RS-232 interface and translates code into various sizes of chars, or sizes and densities of 8 types of bar codes. System imprints on label in any orientation or location. Std features include 2.3" (5.8-cm) wide print line max, with 250-cps printhead speed. System can print through up to 6 layers of multiple part forms, and uses a 7" (18-cm) diameter label/ticket supply roll. Dot placement is optically controlled. Chars are printed in OCR-A size 1, UPC and EAN bar codes, 2 interleaved bar codes, MSI/Plessey bar code, and code 39 bar code. Printer operates from 115 Vac, $\pm 10\%$, 60 Hz, ± 2 Hz. Other power requirements are optional. **Data Specialties, Inc,** 3455 Commercial Ave, Northbrook, IL 60062.

See at Booth 4522

Circle 495

Smart video display terminals and expanded tape storage

Ergonomic workstation

See at Booth A725

64k bytes of RAM give the Intelligent I terminal local processing capability for specialized data and word processing tasks. User friendly display guides operators step by step. Compatible with a broad range of computer systems, the terminal sells for \$1695. Also shown will be model 970, an extension of the company's model 950 smart terminal, which offers expanded memory and additional operating and printing functions.

MB531 workstation is organized to afford the data entry or

word processing operator a comfortable work space. Stand

positions terminal hardware for minimum operator strain. Keyboard is fixed at 26" to 27" (66 to 69 cm), a comfortable

typing height. Input copy sits directly in front of the operator

to eliminate neck and back twisting. Video screen is raised to

eye level, at optimum viewing distance. Desk height work sur-

faces on both sides of terminal allow sufficient space for

unfolded printouts, telephone, and other items. Station is

available in 60" or 72" (152- or 183-cm) widths. Storage pede-

stals, organizer, and modesty shelf are optional. Input-Ez

Two storage devices, TC806C and TS806H, will be introduced to expand memory and increase the versatility of the company's TS806 computer system. The multi-user, CPU based TS806 is configured with 64k bytes of RAM, a 10M-byte, 5.25" Winchester disk drive, and a 500k-byte floppy disk. Adding the TS806H expands the computer system with a 10M-byte, 5.25" Winchester disk drive. TS806C tape cartridge backup for the TS806 provides further storage of 17.2M bytes. **TeleVideo Systems, Inc**, 1170 Morse Ave, Sunnyvale, CA 94086.

See at Booth 7128

Circle 497

Receive-only and enhanced design printers

Receive-only printer DP-9620A, and enhanced design printers DP-9000A and DP-9500A, maintain acoustic noise levels below 55 dBa, making them suitable for office use. Standalone DP-9620A offers both alphanumeric and graphics capabilities. Alphanumeric print speeds range from 200 cps at 10 cpi for a 7 x 9 dot matrix to 100 cps for a 13 x 9 dot matrix that produces characters of draft correspondence quality. Other densities are 12, 15, and 16.4 cpi. Character repertoire includes 96-char ASCII set with lowercase descenders. Horizontal and vertical graphics resolutions are each 72 dots/in. Horizontal and vertical tabulation, 6- or 8-line/in vertical print resolution, and 3-ips nom vertical slew rate are std. Centronics bit parallel and serial RS-232-C interfaces are provided; serial TTY interface

IGG 32 PREVIEW

PERIPHERALS

is optional. Eight serial communications protocols are available, including 3 x-ON/X-OFF, 4 STX/ETX, and ETX/ACK.

DP-9000A and DP-9500A have heavy duty stepper motor, enhanced forms capacity, and 2.7k FIFO buffer. Both provide graphics capability and the 96-char ASCII set. Graphics resolution for the DP-9000A is 72 dots/in vertical and 60 dots/in horizontal. For the DP-9500A, it is 72 dots/in vertical and 75 dots/in horizontal. DP-9000A and DP-9500A have 3 print densities: 10 cpi at 150 cps with a 9 x 9 dot matrix; 12 cpi at 180 cps with a 7 x 9 matrix; and 13.3 cpi at 200 cps with a 7 x 9 matrix. The two series differ in the number of columns that can be printed: DP-9000A prints 80 to 132 col, whereas DP-9500A prints 132 to 220 col.

In OEM quantities (1000), DP-9620A costs under \$1100 each, DP-9000A under \$900 each, and DP-9500A under \$1000 each. Anadex, Inc, 9825 De Soto Ave, Chatsworth, CA 91311.



See at Booth 4335

Circle 498

3-mode serial matrix printers

Family of 6 serial matrix printers, the GE 3000 series has 3 operating modes for handling small systems data processing, word processing, and graphics applications. The microprocessor based printers perform data processing tasks at print speeds up to 600 cps. For word processing, 2 models provide high resolution print mode with overlapping dots for near letter quality printing at 120 to 198 cps, depending on char pitch.



Dot addressable graphics capability is std on each model. The $_{3181}$ printer, an 80-col model, measures $5'' \times 20'' \times 15.6''$ (13 x 51×40 cm). Models $_{3180}$, $_{3240}$, $_{3244}$, $_{3400}$, and $_{3404}$ are 136-col printers that measure $5'' \times 24'' \times 15.6''$ (13 x 61×40 cm). Print speeds, line spacing, paper slew rate, and other performance

parameters vary among models. Each model employs a logic seeking printhead that bidirectionally prints up to 6 copies. Print density is selectable at 10, 12, 13.1, or 16.5 cpi on all models except 3080 and 3181, which provide 10- and 16.5-cpi operation. Ribbons are contained in stationary cartridges and are driven by a dedicated motor. Paper handling systems can accommodate roll and pin feed paper, along with specialized forms. Push tractors below and behind the print line and a paper puller above, are combined to ensure reliable paper handling as well as accurate dot and char placement. All models print 3, 4, 6, or 8 lines/vertical in. Paper slew rates are 15 ips for models 3400 and 3404, and 10 ips for the other units. Standard features include 512-char buffer, nonvolatile memory, self-test and diagnostics, and ASCII 94-char type set. Prices range from \$1000 to \$2000, depending on model. General Electric Co, Data Communications Products Dept, Waynesboro, VA 22980.

See at Booth 1614

Circle 499

Terminal with built-in phone and TV interfaces

Videotex terminal VP-3501 includes built-in, 300-baud direct connect modem for phone communications, and modulated rf output for std TV information display. Terminal features color graphics capability, resident ASCII or dynamically redefinable char set, reverse video, optional acoustic coupler for subcarrier TV audio output, software selectable char format, and an expansion interface for peripheral devices. Compatible with most timesharing and database computer networks, the terminal gives user access to commercially available reports and programs. With some timesharing systems, programs in BASIC, Pascal, FORTRAN, and COBOL can be written and stored.



Terminal includes 58-key alphanumeric keypad with 2 user keys and 16-key calculator format keypad. Unitized keyboard surface, combined with high noise immunity CMOS circuitry, allows operation in hostile environments.

Color graphics capability allows individual chars and background to each be displayed in 1 of 8 software selectable colors. Chars are displayed in either 40-char x 24-line, or 20-char x 12-line formats that are switch, keyboard, or software selectable. Cursor control includes direct addressing to any screen location for fast display formatting. RCA MicroComputer Products, New Holland Ave, Lancaster, PA 17604.

See at Booth 4735

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PERIPHERALS

Intelligent terminal for CP/M and UNIX OS

CDX-268 series intelligent terminals are capable of running CP/M or UNIX operating system applications. Single enclosure contains CRT display and keyboard, multiple microprocessors, up to 128k memory, more than 1M-byte diskette storage, and interfaces to IBM host compatible network communications. Entry level system is upgradeable to full multi-user environment. System is fully compatible with existing CDX-268 product capabilities, including industry std COBOL and BASIC programming, FORMS screen format design facility, ASK record management system, Stylograph word processor, and compatible 2780/3780 and TTY communications protocols. Terminal also features integral modem, allowing it to be remotely located from systems' shared resources. 3270 SNA terminal control unit, supporting multiple CDX-268 units, is also being shown. **Codex Corp**, 20 Cabot Blvd, Mansfield, MA 02048.



See at Booth 6105

Circle 501

Low noise, letter quality daisy wheel printer operates at 55 cps

DP-55, first of a generation of letter quality daisy wheel printers features quiet operation, superior print quality, digital status display, and printing with metal or plastic printwheels. The printer is less complex, has fewer moving parts, and requires fewer adjustments than std daisy wheel printers. MTBF is conservatively estimated at 3000 h at 25% duty cycle. Separate electronic circuit board modules are employed for analog,



digital, and interface functions. Boards snap in or out of designated slots in tilt-out board cage designed for easy access and board replacement. Single-action hammer contributes to printer's rated 62-dBa operation. An acoustic cabinet, rated at 55 dBa, will be available as an option at year end. More consistent striking, less hammer friction, greater accuracy, and improved print quality results from hammer's design.

Operator can access functional parameter panel, manually selecting more than 20 print operating parameters. These functions can also be controlled by host computer downloading instructions to printer. More than 100 std plastic and metal printwheels can be used with the DP-55. Char sets can be 88, 92 or 96 chars/wheel. Printhead pivots a full 90° away from platen for printwheel changes. Interface is RS-232-C; Qume, Diablo, and Centronics protocol personality characteristics are optional. Expandable PROM up to 12k bytes and from 1k to 3k bytes of RAM provide capability for customized operating parameters. Firmware package provides common word processing functions. Price for the DP-55 begins at \$1790 for quantity 1 OEM orders. **Dataproducts Corp**, 6200 Canoga Ave, Woodland Hills, CA 91365.

See at Booth 7510

Circle 502

Low cost terminal

Viewpoint/60 buffered terminal, is claimed to provide more features than any other midrange terminal, including movable keyboard and tilt mechanism. It has 8 discrete programmed function keys, fine line business graphics, visual highlighting, editing functions, and local, conversational, page, message, and forms operating modes. Terminal provides an upward system from the Regent 60 and 40. Price is approximately \$800. **Applied Digital Data Systems Inc**, 100 Marcus Blvd, Hauppauge, NY 11787.



See at Booth 1127

Circle 505

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CIRCLE 92

10

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Need Higher Speed?

The companion IMS1421 delivers even more performance where higher speed is a must. With a chip select access time as fast as 30ns, the IMS1421 sets a new speed record for 16K memories.

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Static RAM Family	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	Max. Access Time		Max. Power Dissipation			
	Organization	Chip Enable/Select	Address	Active	Standby		
IMS1420-45	4K x 4	45ns	40ns	600mW	165mW		
IMS1420-55	4K x 4	55ns	50ns	600mW	165mW		
IMS1421-40	4K x 4	30ns	40ns	600mW	NA		
IMS1421-50	4K x 4	40ns	50ns	600mW	NA		
IMS1400-45	16K x 1	45ns	40ns	660mW	110mW		
IMS1400-55	16K x 1	55ns	50ns	660mW	110mW		



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PERIPHERALS

Multiple-font printer operates in 5 modes

Operating in 1 of 5 modes, model 7030 MultiMode printer combines high speed data processing, letter quality word processing, and graphics printing capabilities. All modes are switch-selectable and programmable, allowing the 9 x 9 serial dot matrix printer to be used as an offline print station or as a data processing component. Onboard ROM stores the printer's font library, with chars in U.S. ASCII, as well as 7 European versions. Each char print mode (180, 150, 75, and 37 cps) has a different horizontal resolution that affects the quality of print. At 37 cps, vertical resolution is doubled to 144 dots/in. Unit produces a draft copy at 180 cps and composes print quality at 150 cps. At the 2 lower speeds, the printer operates in multiple passes to generate letter quality (max resolution) print. Near letter quality mode features a 24 x 9 matrix, while letter quality uses a matrix of 48 x 18. The z80 microprocessor based printer also operates in graphics mode, and contains a 2.7k-byte input buffer. It has full graphic capability with max resolution of 144 x 144 bit-mapped dots/in at a repetition rate of 900 dots/s per needle activated.



In data processing systems, a host computer can download all printer parameters to onboard EAROM via escape code sequences. Using front panel controls, an operator can command printout of all operating parameters, including horizontal/vertical tabbing values, margin justification, font selection, proportional spacing, and selection of compressed print. In addition to stored parameter printout, a diagnostic routine printout of internal functions can be generated, including results of onboard RAM and ROM tests, status of EAROM, baud rate, parity bits, stop bits, and communications protocol selected. A Centronics compatible parallel interface and RS-232 serial interface with current loop reside in each printer. Interface selection is via DIP switch. Serial interface supports STX/ETX, X-ON/X-OFF, BUSY + and BUSY -, with baud rates from 110 to 19,200. Printer is escape code compatible with DEC LA20, LA180, and LA34. Operator controlled variable spacing between printhead and platen permits print quality to be optimized over a range of paper thicknesses. Single-quantity price is \$1995, with quantity discounts available. Qantex, Div of North Atlantic Industries, Inc, 60 Plant Ave, Hauppauge, NY 11788.

See at Booth 4516

Circle 506

Color ink jet printer

Dot addressable, color ink jet printer GP1024 operates on a pixel by pixel basis with plotting surface of up to 1440 points horizontally, and as many points vertically as printing surface allows. Printer has 2 host selectable, horizontal dot densities,



and 9 pixel types. The high resolution printer, with Centronics compatible 1/0 port, can interface with a variety of hosts and terminals. It responds to 6 control codes. Special fill chars are available to allow data transmission in compressed form. With logic seeking function, only active picture information need be transmitted. A 1024 x 1024 image with 120 dots/in is printed in approximately 4.30 min.

Drop on demand ink jet technology minimizes ink waste. Printhead contains 12 jets that deposit cyan, magenta, and yellow colors. By over-printing and half-toning the basic colors, a full color spectrum can be created. With device driver, printer can interface with most graphics devices having 120 dots/in or less resolution. The desktop unit is priced at \$5495. **PrintaColor Corp**, PO Box 52, Norcross, GA 30071.

See at Booth 2025

Circle 507

120-cps graphics dot matrix printer

Model 122, a heavy duty desktop printer intended for use in small business, communications, and personal computer systems, provides all the std features expected of an industrial grade, 132-col data processing printer, plus std pin addressable graphics for business processing or graphics design. The user can choose between std alphanumeric printing and pin addressable graphics, as well as between 6- and 8-pin graphics. Software compatibility with the company's model 739 provides a base of software applications packages, including trend analysis, business graphics, pie charts, bar codes, CAD/CAM draft plots, and data processing printing.

Standard features on the \$1195 model 122 include 120-cps bidirectional/logic seeking printing in monospaced alphanumeric mode, unidirectional/logic seeking printing in graphics mode, selectable forms length [from 3.5" (8.9-cm) to 15.5" (39.4-cm) in 0.5" (1.3-cm) increments], selectable 6, 9, or 18 lines/in, and 7 resident international char sets.

Other products exhibited will include 200-cps Printstation 350 series industrial grade matrix printers; heavy duty 150-cps 132-col desktop model 152 printer; model 739 small business printer; model 792 serial dot matrix printer; model 150 desktop printer; and LP series 600-line/min baud printers. **Centronics Data Computer Corp**, Hudson, NH 03051.



PERIPHERALS

User definable CRT

Model 16 multipage smart CRT terminal features 4-page display memory that is expandable to 8 (either volatile or nonvolatile). and transfer capability of excess display memory into function memory; user or computer definable logical line and page length; and redefinable keys. Standard function memory is 512 bytes, programmable up to 32 functions. As many as 64 keys can be redefined with ESC sequences to represent alternate chars, codes, or sequences, for a user personalized terminal in regard to keyboard location of frequently used keys and functions. Display format is 80-char lines. Horizontal scrolling is employed to display data in columns 81 and beyond. Vertical scrolling similarly is used to display data below the 24th line. Char set includes 96 ASCII and 32 control chars, 64 mosaic graphics, and 64 line drawing and special symbol chars. Alpha only and numeric only modes are std on model 16, as is protect mode. It is ANSI X3.64 compatible, operates either half- or fullduplex (with or without local echo), transmits in block and character modes, and has full-performance I/O auxiliary port. Teleray, Div of Research Inc, PO Box 24064, Minneapolis, MN 55424.



See at Booth 5706

Circle 509

16-bit based terminal with high level, user programmable software

General purpose, standalone user programmable intelligent terminal system, series 8000, is based on the 16-bit, 8-MHz MC68000 central processor chip and features high level user programmable software. Software includes an operating system, BASIC, assembler, and word processing packages. Communications options include SNA/SDLC. Hardware includes an integral controller with 128k RAM, expandable onboard to 256k, and 16k PROM; a 15" (38-cm) CRT with character density of 1920 with 128 ASCII chars; special function keys, with up to 96

TEST & MEASUREMENT PAGE 176

function/control keys and optional keyboards; 2 I/O ports for connection to optional serial printers and/or communications; and dual 5.25" floppy disks with dual-track, dual-density, dual-sided capacity of 1.4G chars. Designed to meet current ergonomic standards, terminal features detached, low profile keyboards, antiglare CRT, tiltable screen, and noiseless operation. Communications are via RS-232-C link, half- or fullduplex, asynchronous or synchronous. Data rate is 50 to 76,800 baud selectable. Basic system, including disk storage, is priced at \$4500. Megadata Corp, 35 Orville Dr, Bohemia, NY 11716.



See at Booth 3405

Circle 510

Desktop terminal emulator and CP/M based communicating intelligent terminal

DM83 emulates Burroughs' TD830/MT983. Std features include totally compatible detached keyboard with 16 user definable function keys, numeric keypad, upper/lowercase chars, printer interface, scrolling, background print operations, line drawing capability, and extensive self-test diagnostics. Operating in asynchronous/isochronous/synchronous communication modes, unit supports poll/select, fast select, group poll, and multipoint contention protocols. Memory can be optionally expanded to 36k. Emulator occupies less than 400 in² (2581 cm²) desk space. List price is \$1995.

Topper, a communicating desktop intelligent terminal initially targeted for use in IBM 3276/3278 networks, provides local workstation capabilities plus full communications protocol compatibility with mainframe computer systems. List price will be under \$5000 for std model having 64k RAM, 1M-byte mass storage, asynchronous printer interface, and full CP/M operating system. With communications compatibility to the host mainframe, unit can be used both online and offline to access either a remote or local data base. **Beehive International**, 4910 Amelia Earhart Dr, PO Box 25668, Salt Lake City, UT 84125.

See at Booth 7105

Grab the next plane, train, bus or cab to see our high performance graphics display and we'll pay your way.

At Digital, we think the best way to get a feel for a graphics display is to get your hands on one. So here's our offer.

If you're a qualified* buyer for our VS11/VSV11 high performance raster graphics display, you're invited for a free, hands-on demonstration. And transportation costs are on us.

Digital's VS11/VSV11 was designed for the most demanding requirements in CAD, CAM, process monitoring and control, imaging and simulation. The VS11/VSV11 is fast enough to give you rapid updates of even the most complex images in full color.

The software is just as impressive. RSX-11M or VAX/VMS driver software. A FORTRAN graphics subroutine library. All standard. With options including VIGL[™] Digital's advanced graphics tools package developed by Boeing Computer Services Company and PATRAN[™]-G^{*}, a structural modeling program from PDA Engineering.

So if you're looking for a high performance graphics display, we'll make it easy to see the VS11/VSV11 at your convenience. We'll even pay your way. For more information, call (603) 884-4662. Digital Equipment Corporation,

5 Flagstone Drive, Hudson, NH 03051.



*Send us an authorized RFQ for 5 or more VS11/VSV11 to be delivered by December 31, 1982. At our option, we'll arrange for , demonstration at your facility, or reimburse one person for transportation to the nearest VS11/VSV11 demonstration center within the continental U.S. If you can't take advantage of our special offer, we'd be glad to arrange a demonstration at our center. **PATRANTM-G is a registered trademark of PDA Engineering.



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All from a top name in electric motors for just about everything—Gould. These Brutes feature Gould's open frame design and patented Recirk™ bearing lubrication system for extended life.

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brute

An Electrical/Electronics Company

PERIPHERALS German ergonomic standard terminals

Line of ergonomically designed smart terminals, the TDV 2200 series is offered in models that emulate virtually any terminal, including VT-100 and IBM 3101. To meet ergonomic requirements for correct relationship between CRT light output and other elements at the workstation, a light colored background surrounds text on screen. Intensity control affects both text and background light, providing optimal contrast under all lighting conditions. An antireflex tube, and tilt and swivel mechanism eliminate reflections from the tube; matte finish of keytops and other surfaces also minimizes reflection. The 15" (38-cm) CRT displays 0.175" (0.445-cm) readable char caps. Equilite video systems displays both vertical and horizontal lines with same intensity. Char definition is consistent across entire screen.

Nonvolatile EAROM stores operational mode commands generated from keyboard or host computer. Commands are prompted from call-up menus that list alternatives for control of cursor and keyboard, screen and terminal, and communications modes. EAROM can also be used to store often used words and phrases, or code sequences. Security lock to bar unauthorized access to terminal, and magnetic card reader to limit access to host computer, are options. Series prices start at \$2300. Tandberg Data, Inc, PO Box 99, Labriola Ct, Armon, NY 10504.



See at Booth A537

Ergonomic terminal with long life CRT



An ergonomically designed, programmable video display terminal, AVANT 300 combines intelligence and 10k-byte RAM storage that can be downline loaded from host computer. An internal socket for adding initialized EPROM automatically loads RAM and function keys on power-up. Eight user or host programmable function keys, with 48-char capacity/function, are provided. Bidirectional printer port interfaces to virtually all printer models. ETX/ACK, X-ON/X-OFF, and DTR drop protocols are provided; chars for X-ON/X-OFF can be user defined. Moveable keyboard has editing keys and separate 14-key numeric pad.

Additional features include 11 international char sets, 16 baud rates independently settable on printer and main interface ports, and changeable voltage capabilities for 100, 120, 220, and 240 V. Terminal can display and transmit 31 video attribute combinations. Screen saver feature maximizes CRT life, and can be set to any turn-off time or deactivated by user or host. General Terminal Corp, 14831 Franklin Ave, Tustin, CA 92680.

See at Booth A419

Circle 513

SYSTEM ELEMENTS

83-station detachable keyboard

Off-the-shelf enclosed keyboard model P2492 includes an 83-station microprocessor encoded capacitance keyboard with serial ASCII output. Detachable keyboard design complies with ergonomic standards. In addition, keyboard features IBM Personal Computer keyboard layout that complies with ANSI and ISO standards. It features CAPS lock, and a separate numeric/cursor control pad. Keyboard termination is std 6-pin modular phone connector that can be interfaced with flexible phone type cable to the system. Other features include full N-key rollover, auto-repeat, plus 5-V only operation, rigid frame mounting, and asynchronous 300-baud serial TTL level ASCII output (9600-baud or RS-422 output are optional). Keyboard station is \$149.63 without enclosure, and \$212.63 with enclosure for 1 to 9 units. Key Tronic Corp, PO Box 14687, Spokane, WA 99214.

See at Booth 5505

Circle 512

SYSTEM ELEMENTS

Membrane switch keyboard has 81 positions

An 81-position version of the Full Travel Membrane (FTM^R) keyboard utilizes membrane switches that have 1 flexible surface membrane made conductive, usually by application of a conductive ink. This surface is slightly separated from a rigid substrate bearing a conductive circuit. Open-switch gaps are closed when the membrane is pressed down to contact the substrate. A PCB substrate, either single- or double-sided with plated-through holes, is used, depending on required switch density and mounting components, such as LEDS, connectors, and output pins. A single-sided circuit can also be produced by screening a conductive ink or paint onto a rigid support or onto a flexible membrane for later application to a rigid backing. Spacing between membrane and substrate is maintained by an insulating spacer, such as a polyester film. Holes cut into the spacer allow contact at desired switch positions.

Membrane keyboard is not directly actuated by the user's finger, but by a full-travel key. Keycap fits on a plunger mounted in a housing and supported by a return spring. An actuator spring is located at the bottom of the housing. Depressing the plunger brings it into contact with the actuator spring. The spring then presses on the membrane, forcing it into contact with the substrate. When the key is released, the return spring travels it to its original up position. Key touch and feel are virtually indistinguishable from a std typewriter keyboard. Keys with alternate action, such as shift lock, are provided with a series of small ramps in the plunger and a cam follower hook. When key is depressed, the hook engages ramps and the key stays latched down. Repressing the key disengages the hook. Smooth action of the spacer bar is maintained by a torsion wire attached to 2 housings and to rectangular inserts in either end of the bar to prevent the bar from binding when it is operated at either end.

company's Entry Error Elimination (E^3) , a microprocessor based N-key rollover function with phantom key lockout provided for all data keys. **Oak Switch Systems, Inc**, PO Box 517, Crystal Lake, IL 60014.

See at Booth M235

Circle 515

Ceiling mounted micro/mini air conditioner

Hilander, a 1.5-ton capacity air or water cooled environment controller for micro- and minicomputer systems, installs in place of a std 2' x 4' (61- x 122-cm) ceiling tile. Unit runs at 208/230 or 277 V single phase. Made from epoxy coated galvanized steel, 1-piece construction can be installed flush with suspended ceiling, semi-recessed, or fully exposed. Temperature and humidity controls are independent of the building's air conditioning system, outside temperature, or humidity. Reliability has been improved through replacement of the expansion valve that usually controls refrigerant flow with a static capillary tube. Multiple-redundancy water collection and drainage system is std. Finned electrical resistance heater and 3-lb/h humidifier, centrifugal blower, automatic condensate pump, wall mounted stop/run control, and installation rig for positioning unit 10' (3 m) above ground level are optional.

Also displayed will be 3- or 5-ton capacity Spacemaker II, which is available for mid-size systems in air, water, glycol, or chilled water models, upflow or downflow. Unit operates at 208/230 or 460 V triple phase, and can be used in master/slave or multiple-independent configuration. The Energy Conservation System (ECOS) provides 10- to 20-ton capacity for large data centers. **Hiross Inc**, PO Box 290, 2107 Liberty Dr, Niagara Falls, NY 14304.

See at Booth 3110

Circle 516



The FTM keyboard is available with optional encoder that mounts directly on the back of the keyboard and converts the row/col matrix to a choice of industry std codes. Standard encoder provides TTL ASCII coded 8-line parallel output with strobe. With add-on options, it can be converted to 3-state, open collector ASCII or to RS-232-C serial output. Encoder provides debouncing for all keys, and selectable auto-repeat for all noncontrol keys. It is specifically designed for microprocessor interface. Coding is 4-level, with unshift, shift, capslock, and control. Included is a choice of 2-key rollover or the Wafer thin card reader



Magnetic stripe card reader, the Eaglet, measures $3.5" \times 0.285" \times 1.1"$ ($8.9 \times 0.724 \times 2.8$ cm), with magnetic head protruding an additional 0.3" (0.8 cm). Decoding electronic board, measuring $3.4" \times 0.51" \times 1.05"$ ($8.6 \times 1.3 \times 2.67$ cm), is connected to head by flexible cable. Separation of reader and decoding board allows max flexibility and simplicity in reader utilization. Reader features spatial decoding technology that requires no compensation for speed or acceleration as the card is passed through the reader. It features a special spring and mounting arrangement for reliability in reading warped and contaminated cards. Reader is virtually maintenance free. OEM quantity price is \$29.30. American Magnetics Corp, 740 Watsoncenter Rd, Carson, CA 90754.

See at Booth 1928

Now you can choose from the broadest step motor line



T\$RMAX®

Tormax® Variable Reluctance Step Motor

Utilized extensively in high speed applications. Highest torque to inertia ratio of any type step motor. Step angles range from 7.5° /step to 30° /step.

Tormax[®] Salient Pole Rotor Permanent Magnet Step Motor

Where variable torques and intermediate speed responses are required to interface with large gear drives, primarily for military and space applications. Step angles range from 22.5° /step to 120° /step.

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For those difficult computer applications where accelerating torque is needed for high speed and fast response in both printers and disc drives.

The Tormax[®] Hybrid Step Motor with step angles from 0.9° /step to 5.0° /step combines high torque and small step angles for excellent positional accuracy and high reliability. A wide range of torques from 10 oz. in. to 450 oz. in. and DC voltages from 3 volts to 100 volts are available.

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The Synchron[®] Step Motor is being utilized in those computer peripheral applications where the combination of performance and low price are major requirements. Typical step angles range from 3.75°/step to 22.5°/step.

When precise positioning is needed, the Synchron[®] Step Motor combined with a lead screw gives the desired location for the various motion profiles in a floppy disc head positioner.

The Synchron[®] Step Motor is popular in paper feed, ribbon applications in the lower performance matrix, and daisy wheel serial printers. Torques of 3 oz. in. to 50 oz. in. and voltages from 3 volts to 40 volts are available for your applications.

HANSEN MANUFACTURING COMPANY, INC. • P.O. Box 23 • Princeton, IN 47670 • 812/385-3415 Subsidiary of IMC Magnetics Corp.



SYSTEM ELEMENTS

CRT modules

OptiMiser series features 12" (30-cm) and 15" (38-cm) 110° high end CRT modules that operate on 24-Vdc supply voltage. Center resolution of 1200 lines, frequency response to 35 MHz, and std horizontal scan rate to 21.7 kHz are provided, with higher frequencies optional. In addition to kit versions, series is also available in chassis form with tilts of 0° , 5° , 7.5° , 10° , and 15° . Price is under \$150 in OEM quantities.

Gardian display series protects true direct drive systems against failure, should lower than normal operating frequencies occur when CRT controller is initialized. Gard-Well circuit removes horizontal drive when frequency nears a point that normally damages horizontal deflection circuitry in comparable units. The 90° Gardian series is available in screen sizes of 7", 9", and 12" (18, 23, and 31 cm). Horizontal scan rates to 20.7 kHz are std. Higher frequencies are optional. Choice of power inputs include 12- or 15-Vdc (customer supplied), or linear power supply with 115/230-Vac operation. Series is priced under \$100 in OEM quantities. Wells-Gardner Electronics Corp, 2701 N Kildare Ave, Chicago, IL 60639.



See at Booth A227

Circle 518

Circle 519

Magnetic heads for 5.25" and 8" drives

Series of magnetic head products include the Winchester monolithic head, Winchester composite head, and microcomposite head. Heads allow 8" and 5.25" disk drive designs to withstand repeated load/unload cycles without deteriorating the integrity of the recording element. Composite head provides selected materials for thermal compatibility between the ferrite recording element, bonding glass, and main ceramic body. Micro-composite head prototypes are available with a 3370 type slider, allowing lower flying height, and achieving higher recording densities with the ferrite element. **Data Magnetics Co**, 445 Laurelwood Rd, Santa Clara, CA 95050.

See at Booth 6929

Mini printer stands

WSPS-1 and WSPS-2 solid steel stands elevate mini printers for $9.5'' \ge 15'' (24.1 - \ge 38 - \text{cm})$ paper. Two paper glides hold stacks of paper in place, ensuring precise feed into the printer. Contact clip provides simple cable glide control and direction. WSPS-1 measures $14.25'' \ge 4.25'' \ge 13'' (36.2 \ge 10.8 \ge 33 \text{ cm})$, and weighs 8 lbs (3.6 kg); WSPS-2 measures $21'' \ge 5'' \ge 13'' (53 \ge 13 \ge 33 \text{ cm})$, weighing 11 lbs (5 kg). **Bretford Manufacturing**, 9715 Soreng Ave, Schiller Park, IL 60176.

See at Booth A858

Circle 520

Compact medium resolution monitor

A mid-resolution monitor, available in both chassis and kit form, features a main PCB that measures $3.5" \ge 6"$ (8.9 x 15 cm) and includes flyback transformer. Compact size allows for improved packaging within the terminal. Horizontal frequencies of 15.75, 19.0, and 21.5 kHz are currently available. A slightly larger PCB is also available for frequencies of 23 to 30 kHz. In addition, the company will show a complete line of high resolution color monitors. **Panasonic Industrial Co**, One Panasonic Way, Secaucus, NJ 07094.

See at Booth 3510

Circle 521

Portable laser scanner

Portable handheld laser for scanning bar code labels and packages is compatible with the company's portable data entry model 787 tele-transaction terminals. The laser wand bar code reader has misread rate of 1/1G. It reads bar code on virtually any surface regardless of color or color contrast: crinkled packages, metallics, and bar codes that are dirt covered or smeared can be read. Laser shoots a low power beam of environmentally safe light. It can be held 2" to 9" (5 to 23 cm) away from the bar code surface. Laser reads all current popular bar codes, including Code 39, UPC, Plessey, and Codabar. Scanner weighs 14 oz (0.4 kg) and consists of a compact handheld head, and a miniature, fully integrated decode module power pack. **Telxon Corp**, 3330 W Market St, Akron, OH 44313.





TI just cut the modem down to size.

Introducing the TMS99532 FSK modem from Texas Instruments.

Add just a few inexpensive parts to the TMS99532, and you get a complete 300bps modem, meeting Bell 103J Data Set Spec. The chip includes modulation, demodulation, and even on-chip filtering. So, it's easy to design with. Easy to assemble.

One-chip reliability

TI's new "single-chip" modem drastically reduces the number of parts, compared to

standard, discrete modem design. Result: reliability is increased. And system cost is also decreased. In addition, the TMS99532 comes in a space-saving 18-pin package.

The TMS99532 has a TTL compatible digital interface. It can be connected electronically through a Data Access Arrangement (DAA), or acoustically via a microphone and speaker. Interface to a handset requires only a few op amps.

New dialer

And coming soon from TI: a companion dual tone/pulse dialer. The TMS99531 is

the only single-chip dialer that has both Dual Tone Multiple Frequency (DTMF) and pulse dialing capability. On-chip diagnostic mode provides for quick verification of all digits. The TMS99531 is compatible with Bell 103J specifications.

Write or call for more information on the latest leadership devices from TI's extensive family of general purpose peripherals. Call your local TI field sales office, or write Texas Instruments, P.O. Box 202129,

Dallas, Texas 75220.

Texas Instruments invented the integrated circuit, microprocessor and microcomputer. Being first is our tradition.

TEXAS INSTRUMENTS

CIRCLE 98

The new HP you'd think you were



1000 Model 65: sitting at a mainframe.

Now you can tackle your large applications without breaking your budget. That's because our new HP 1000 Model 65—with a powerful real-time operating system and advanced memory management scheme—can handle jobs that previously required a mainframe computer. And do it at a minicomputer price.

Extended code space for programs. Virtual memory for data.

The key to the Model 65's new power is our enhanced RTE-6/VM operating system. Using an Extended Code Space segmentation scheme, RTE-6/VM lets you compile, load and execute large programs (approaching 25,000 lines of FORTRAN code), or convert them from other computers. And because RTE-6/VM uses a virtual memory design, these programs can access a huge 128 megabytes of data—transparently. So your programs can virtually be as large as the application requires.

Getting a head start on development.

A Model 65 development system gives you maximum HP 1000 power in one fully-configured package. You start with RTE-6/VM, floating point

hardware and one megabyte of high-performance main memory. You also get our award-winning IMAGE data base management system; FORTRAN 77, Pascal and Macroassembler; a 16 Mb fixed disc with integrated tape cartridge; and a powerful graphics terminal to use with our Graphics/1000-II software. All for less than \$65,000.

Third parties play a part.

ATTON

RESULTS

If you're a software supplier, just picture *your* big applications on the Model 65. The cost of the "total solution" to your customer will be significantly lower. Which means more systems can be sold. And that's just the idea behind our new HP PLUS program, where selected software suppliers team up with HP to bring competitively priced, quality solutions to the market-

A one magabute Model 65

A one megabyte Model 65 development system is priced at under \$65,000.

place. And if you're an OEM, our volume discount schedules make these systems even more attractive.

For more information, call your local HP sales office. Or write Hewlett-Packard, Attn: Joe Schoendorf, Dept. 12128, 11000 Wolfe Rd., Cupertino, CA 95014.

You can see the HP 1000 working on factory applications at Productivity '82. Watch your newspaper for more details.



Price U.S.A. list; subject to change without notice.

CONRAC SERIES 2400 The benchmark in high-resolution monochrome

The new benchmark in monochrome CRT displays comes from Conrac – our 2400 high-resolution monitor. Advanced electronics and tube technology combine to give you a fine spot size, wide video bandwidth, and high horizontal scanning frequency. The result: a bright and crisp 1280 x 960 pixel rasterscan display.

information on the screen while providing the rapid rise and fall times needed for crisp pixel definition. You get all the performance you built into your system, while users appreciate the sharp, clear image.

Selectable scan frequencies.

This convenient option can cut your inventory while



Ultimate clarity and illumination.

No matter where you measure on the screen, the 2400 offers a .35 mm spot size, and the light intensity of each spot has been increased by nearly 50%.

Dynamic focusing circuitry and special beam focusing construction enable this exceptional spot performance.

Wide video bandwidth. Video bandwidth of the 2400 is a broad 40 MHz (-3dB), allowing more



giving you a new range of flexibility. Now, you can buy and stock one monitor for horizontal scanning frequencies from 15 kHz to 37 kHz, enabling compatibility with a range of systems.

And the system user gets a monitor that can be upgraded by the simple change of a switch, instead of replacing the monitor.

New versatility in applications. The high-resolution 2400 is available in cabinet.

rack-slide or chassis-only configurations – either 13" or 19" CRT. The 19" offers 1280 horizontal x 960 vertical pixel resolution at a 1225-line rate, and the 13" offers

1024 x 768 pixel resolution. Every graphics system

will look better, and offer less user fatigue, whether the system is for industrial CAD/CAM or tight VLSI circuit design. And medical electronics displays have a clarity and crispness not seen before, especially if a wide gray scale is desired.

Find out more:

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See us at the National Computer Graphics Association (NCGA) Show in Anaheim, California, June 15-18. Also see us at Siggraph in Boston, July 26-30.





Screen data courtesy of Megatek Corporation.



POWER SOURCES & PROTECTION

Motor generator power conditioner for minicomputer installations

Atlas MPC supplies computer grade electrical power for medium to large minicomputers with power requirements of 10 to 18.75 kVA. Combining up to 250-ms ridethrough with motor generator power conditioning guarantees 100% clean computer power and uninterruptible rotational energy storage to bridge momentary power outages—eliminating the need for std UPS equipment, batteries, and air conditioning. Unit requires 30" x 34" (76- x 86-cm) floor space. Optional computer room soundproof cabinet reduces noise to below 70 dBa.

MPC is directly compatible with DEC, Wang, IBM, Prime, Data General, Hewlett-Packard, Sperry Univac, Texas Instruments, Harris, Burroughs, Honeywell, and other minicomputer systems in the 10- to 18.75-kVA power range. Prices start below \$12,000. Atlas Energy Systems, 9457 Rush St, South El Monte, CA 91733.

See at Booth 3958

Circle 523

Laminated ferro based voltage regulators

Series of transformer based voltage regulation equipment provides substantially improved operating efficiencies and a 20% weight savings. Core lamination material lowers overall power consumption and operating costs and reduces cooling requirements. Lamination design is incorporated into all ferroresonant transformer products rated at 1.5 kVA and larger. Laminated products include 2000-VA portable micro/minicomputer regulator, all hardwired micro/minicomputer regulators above 1000 VA, and all constant voltage sinusoidal (Cvs) units above 1000 VA. Operating efficiencies are increased from an average of 85% to over 90% in all units. The 3000-VA cvs functions at nearly 94% efficiency, representing a 54% decrease in the amount of energy wasted in heat dissipation by the unit. The hardwired 1500-VA micro/minicomputer regulator provides a 34% decrease in heat dissipation over previous models. A 50% reduction in dissipated heat allows cooling capacity to be reduced by the same margin. Regulator power consumption is also reduced to lower overall operating cost. Improved regulator performance through use of lighter weight lamination material provides a thinner air gap between lamination layers, lowering resistance in the core, and thereby increasing efficiency. Lamination gives the ferro based regulators operating efficiencies in the range of electronic designs. Sola Electric, a unit of General Signal, 1717 Busse Rd, Elk Grove Village, IL 60007.

See at Booth 6917

Circle 524

Frequency/phase converter power supply

New Generation UPS provides smooth electrical power for critical applications. Machine isolates load completely from the power line through mechanical shafting. If utility power is interrupted, rotating unit continues to supply power from energy stored internally. Input power can be accepted from any existing utility line because the system operates either as a frequency converter or as a phase converter. Crystal controlled output can optionally produce conventional power requirements. Continuous voltage regulation protects power from brownout conditions. Critical load is supplied by the power

interruption. All models produce 60 ± 0.02 Hz continuously and operate with common 60-Hz utility powers. Energy storage time ranges from a few seconds via inherent system inertia to several minutes with supplementary flywheel action. Unlimited storage is powered by a gas engine. MRL-Precise Power Corp, PO Box 2006, Bradenton, FL 33508.

See at Booth 8709

Circle 525

Uninterruptible ac power for microcomputers



Lifeline provides UPS protection for microcomputers, isolating critical computer power circuits from power line glitches and outages. No-break feature regulates voltage and filters lines at all times. Inverter supplies power during outages, without interrupting critical load. Maintenance-free internal battery handles full system power for 5 to 10 min. Recharge to 95% of full charge is under 40 min. Optional bank of batteries extends operation for several hours. Unit plugs into 120-Vac wall outlet; critical load plugs into dual-convenience outlet on UPS. Output power for model M95-200 is 200 VA; for model M95-600, 600 VA; and for model M95-1000, 1 kVA. Instrumentation and Control Systems, Inc, Electro-Pac Div, 520 Interstate Rd, Addison, IL 60101.

See at Booth A821

Circle 526

Uninterruptible power supplies

Line of uninterruptible power systems, series 2000 is targeted for mini-mainframes, minicomputers, and communications equipment. Series features significant size and weight reductions, and contemporary cabinet design. Batteries and electronics are housed side by side in 3 cabinets to reduce implementation costs associated with std UPS systems. Series is available in 10 ratings, from 5 to 30 kW, and 30 ratings from 15 to 45 kW.

Also being shown is the 4080 UPS, an 80-kW module that supports CPUs requiring 415-Hz power. Std system includes module containing rectifier/charger and inverter, internally sealed control power battery, I/O, motor operated battery breakers, and solid state diagnostic panel. Entire module logic can be replaced with 3 PCBs to enhance maintainability. Exide Electronics, 2 Penn Center Plaza, Philadelphia, PA 19102.

See at Booth 1907

Circle 527

TEST & MEASUREMENT

Combined simulator and analyzer for PCM lines

Combined simulator and analyzer, TE 820 can simultaneously and independently monitor pulse code modulation (PCM) lines while the simulator generates multiframe data at rates up to 2.048M baud. Data are looped or responded to by PCM equipment at the other end of the link. The tester comprises 2 independent sections which operate with different clock signals. The first section, a generator/simulator, delivers both frame and multiframe signals conforming to CCITT recommendation G732, when not affected by simulated perturbations. The receiver/analyzer section accepts a digital signal and detects frame and multiframe alignment. IEEE bus interface allows the 820 to be integrated into an automatic test system with processor controlled test sequence. All functions are pushbutton selectable, with LED incorporated to indicate that a function is in operation. TE 820 is priced at \$9750.

Data communications simulator TE 9001, also being shown, is a user definable simulator of high speed data communications protocols. It simulates, under scenario control, X.25 SDLC/SNA, I PARS, HDLC, and other protocols with densities up to 1 flag between frames, and speeds over 128k baud. The simulator is the first in a second generation of data communications testers that handle high speed links and higher level protocols. Simulator is priced at \$18,000. Tekelec Inc, 2932 Wilshire Blvd, Santa Monica, CA 90403.

See at Booth A554

Circle 528

Removable disk inspector

Model 750 disk pack inspector, a 30k cd, motorized inspector for removable disk packs, has tolerance measurement gauges with precision to 0.0002" (0.0051 mm). It illuminates full height and width of pack. Prices range from \$2700 to \$3750, dependent on accessories. Inspector has clutched, power driven spindle; packs rotate at 6 rpm. Precision comb gauges provide radial and axial tolerance check with 1 rotation. Towers combine comb gauges and mirrors on single post. Tester weighs 28 lb (13 kg), measures $14" \times 17" \times 8"$ (36 x 43 x 20 cm), and is enclosed in high impact ABS case.

Also exhibited will be the company's "Data Recovery" service, with recovered disk packs from flood or fire impacted systems. Graphics provide information concerning degree of damage from which 98% of data was recovered. Randomex Inc, 1100 E Willow St, Signal Hill, CA 90806.

See at Booth 3429

Circle 529

Computer environment analysis system

Plug-in modules for series 626 universal disturbance analyzer computer room monitoring system monitor temperature and humidity; 400-Hz, 3-phase power sources; detection and duration of impulses; and mass storage and communications. Temp and humidity module is plugged into 1 of 5 input positions to provide a printed record of any out-of-tolerance conditions. Solid state sensors are included and can be located up to 100' (30 m) from the mainframe. With 3-phase, 400-Hz module, ac power from 350 to 450 Hz can be monitored. Module is designed for IBM 370/165, 370/168, 3032, and 3033 systems; Amdahl 470 series V5, V6, and V7; and other large mainframe units. Ac measurements are accurate to $\pm 1\%$ of reading ± 1 V and ± 1 Hz. Impulse measurements are possible up to 4000-V peak, with durations up to 100 μ s. Impulse analysis



option allows analyzer to determine the origin of impulse disturbances, such as from switching power supplies, motors cycling on and off, failed components, and noisy ac inverters in UPS systems. Module can also be used to determine whether impulses are likely to affect computer operation.

For remote operation, mass storage and communications module provides added capabilities to RS-232-C interface already built into the analyzer. Module will store disturbances, which can be accessed through the self-contained autoanswer/auto-dial modem. When equipped with this module, series 626 behaves as an automatic remote data collection system. A remote operator can command several units via any voice grade telephone line. **Dranetz Engineering Laboratories Inc**, 1000 New Durham Rd, Edison, NJ 08818.

See at Booth 8015

Circle 530

Miniature 100-MHz and X-Y display oscilloscopes

Model 4100 field service oscilloscope is portable, weighing only 14.75 lb (6.69 kg), with dimensions of $4.25" \ge 8.75" \ge 15.1"$ (10.80 $\ge 22.23 \ge 38.4$ cm). The 100-MHz instrument is designed specifically for harsh environments. CRT floats within a full μ -metal shield, which is cushioned by layers of sponge rubber pads acting as shock absorbers. Dome mesh post deflection acceleration provides bright trace and small spot size. Modular construction uses std off-the-shelf components. Battery pack option operates the scope for 2.5 h on a single charge. Quantity-1 price is \$2495.

Model 2010 high performance X-Y display oscilloscope also uses dome mesh, post deflection acceleration, with a 0.32-mm spot size. High frequency capability is provided by 10-MHz vertical and 5-MHz horizontal bandwidths, complemented by 1-MHz TTL Z-axis blanking. Deflection factor is 1 V pk-pk up to 100 V pk-pk full scale. Unit measures $3.5'' \times 5.5'' \times 15''$ (8.9 x 14.1 x 38 cm), and weighs 7 lb (3 kg). Quantity-1 price is \$995. Vu-Data Corp, 7170 Convoy Ct, San Diego, CA 92111.





THE ONLY 14" WINCHESTER WITH BUILT-IN BACKUP.



The Ampex Superwinchester solves your backup problems. How? With its removable media cartridge. This is unique; Winchester reliability with built-in backup for archives and transactions.

It's two drives in one — fixed media Winchester and removable media SMD technologies. And six totally compatible drives to choose from. Each drive weighs, looks and fits the same. Each is built with 95 percent common parts. This family concept reduces your drive and parts investment. Any drive in the series is compatible with existing controllers. Your routine maintenance requirements are restricted to the removable media. A field testing exerciser combined with low MTTR and high MTBF assures these requirements are met quickly and easily.

You can upgrade your system without impacting data base, software investment, field support or system operations. The family offers 16, 48, and 80 megabytes of Winchester storage and all use the same 16 MB cartridges.

Our Superwinchester gives you the capability to quickly off-load for storage without resorting to tape drives and additional peripherals or software.

It's the disk drive that allows you to design cost-effectiveness into your system. Economic advantages you cannot overlook.

Look into it by contacting Gary Owen at Ampex, Memory Products Division, 200 N. Nash St., El Segundo, CA 90245. (213) 640-0150.

AMPEX[®] The Designer's Choice.

TEST & MEASUREMENT

Tape cleaning systems

Microprocessor based DETECTOR II cleans 0.5" tape on reels to 10.5". Reel full cycle at 300 ips nom is 3.3 min; half-cycle is 1.65 min. Two sapphire blade cleaning stations and 4 proprietary vacuum-grid stations remove particles from tape surface and reduce possibility of recontamination. Grounded to chassis, vacuum-grids inhibit static and attraction of magnetized microscopic debris. Programmable optical defect detector scans tape and displays total defects; it can also position each defect for inspection. Standard features are self-seating hubs, bidirectional footage counter, leader length indicator, and programmable footage search. Keylocked dual-tension control switch adjusts to low speed, high speed, or archival requirements. Unit measures 28.75" x 12" x 18.75" (73 x 30 x 48 cm), and weighs 90 lb (41 kg). Operation is powered by 115 Vac, 60 Hz or 230 Vac, 50 Hz, 150 W.

Patented PROTECTOR cleaning system for self-loading cartridges Easy Load I, II, and III is built with only 15 moving parts. Replaceable snap-in cleaning heads have vacuum port and multilayered cleaning pads. Cartridges are aligned by automatic metal roller chain, in conjunction with 2 unported and 1 ported centering clamp mechanisms. Drive gear motor produces 90 oz-in power; unit operates at 115 V, 60 Hz, 8 A or 220/240 V, 50 Hz, 4 A. System measures 18.5" x 11.75" x 15.75" (47.1 x 29.84 x 40 cm), and weighs 23.5 lb (11 kg). Graham Magnetics Inc, 6625 Industrial Park Blvd, North Richland Hills, TX 76118.

See at Booth A705

Circle 532

Infield isolated grounds tester

Model 7106 Accu-Test, a second generation ground impedance tester for 120/208-Vac circuits, is a pocket-sized instrument for infield detection of ac power and grounding problems. Instrument features ability to detect neutral ground shorts and/or reversals on 120-Vac systems. Additional testing capabilities include undervoltage detection, wiring error analysis, and determination of green-wire ground or neutral conductor impedance. With addition of test probe, all tests can also be conducted on hardwired equipment. Voltage and wiring tests are conducted automatically after plugging the tester into a receptacle. Pushbuttons permit operator to conduct a series of active tests of ground path quality. Included are tests for low ground path impedance, for ground loops (neutral to ground shorts), and, with use of additional probes, tests for neutral ground reversals and for isolated (green-wire) ground integrity. Tester is housed in high impact plastic case and is terminated with a 3-conductor plug. ECOS Electronics Corp, 205 W Harrison St, Oak Park, IL 60304.





Radiometer for calculating EPROM erase time

DS-254E EPROMETERTM measures the shortwave ultraviolet irradiance of EPROM erasers and recommends the proper erasing time. This takes the guesswork out of determining UV intensity and eliminates the time-consuming, error producing procedure of calculating erase time. When the user presses the selector switch corresponding to the nominal erasing energy value of the EPROM chip, the digital display immediately shows the recommended erasing time in minutes with an overall accuracy of $\pm 5\%$. The instrument features $4\frac{1}{2}$ -digit LED readout and a measuring range of 0 to 19,990 μ W/cm².

The meter is calibrated to NBS standards by pyroelectric methods to ensure maximum accuracy. It has excellent linearity and cosine response, as well as exceptional ruggedness. High quality interference filters are used that combine unparalleled accuracy, controlled spectral coverage, and elimination of sensitivity to infrared and other unwanted radiations. A special diffuser sensor window minimizes the solarization (degradation) effects on the response of the meter. Solid state electronic circuitry ensures long and trouble-free operation. **Spectronics Corp**, 956 Brush Hollow Rd, PO Box 483, Westbury, NY 11590.

See at Booth 1904

Circle 534

Self-loading computer tape tester

SLT-800 self-loading tape maintenance system cleans, retensions, and electronically evaluates the condition of a 2400 ' (732-m) reel of computer tape in 3.45 min. It also tests for proper loading characteristics on self-loading drives. The fully automatic system features interlocked safety door for operator protection. A 4-way cleaning technique, tape handling that emulates high speed, high density drives, and AGC circuitry ensure accurate test results. Price is from 17,995.

Other magnetic media products being shown include preformatted flexible disks for use on AM, CPT, MICOM, Lanier, Wordplex, Canon, and other systems; and line of color coded magnetic cards for use on all IBM compatible magnetic card equipment. Line of critically certified 5.25" mini-flexible disks, tested error-free at clipping levels above 40%, with reinforced hub rings std, will be demonstrated, along with doublesided, 96-tpi mini-flexible disks. **Dennison KYBE Corp**, 82 Calvary St, Waltham, MA 02254.

cle 533 See at Booth 5518

CYBERNEX



Take a real close look. Here's why.

ver the last 8 years Cybernex video terminals have evolved around the needs of our broad base of repeat customers.

Our early exposure to the rigorous demands of the Canadian and European marketplaces has two important results. A high quality product and a strong commitment to customer support.

Add to this, our designed-in ergonomics and a compact attractive enclosure and you get the best of both worlds. User acceptance and long term reliability.

We now offer a wide range of standard products and enhanced emulations for compatibility with most systems available today. We also specialize in adapting our terminals to meet the unique needs of our customers.

The XL-87 shown is an example of the functionality of our standard XL Series.

Line and graph drawing capabilities plus screen formatting for data entry applications are all naturals for the XL-87.

And there's more! Various models in our high resolution MDL series offer touch screen capability, windowing, multi paging, programmable function keys and local processing.

OEMs take note. Cybernex provides a reliable product available only to value added

resellers. This allows OEMs to profitably resell Cybernex terminals and to maintain a unique visual identity for their systems. If this sounds like the kind of product and supplier you have been looking for, see us at

NCC. Take a closer look. Then let's do business.



International Sales Department: 2457 Dunwin Drive, Mississauga, Ontario, Canada L5L 1T1 Telephone: (416) 828-2810 Telex: 065-22093 U.S. Sales Department: 1257 Algoma Road, Ottawa, Ontario, Canada K1B 3W7 Telephone (613) 741-1540 Telex: 053-4419

Why other ribbon cable connectors are about to lose their grip.

The reason is AMP has the system. Latch-type connectors, precision cable and tooling that give you everything the others can. And many things the others can't. Like our one-step tooling for preassembled receptacle connectors, that gives you the benefit of up to 30 percent faster termination rates. Or contacts that latch into our covers (not just onto the ends) for the best cable and cover retention. Or a unique fluted cover design that assures perfect cable alignment—automatically.

You can even pick your polarization, including military qualified types, from our complete connector and assemblies line. Match them with our universal ejector header that lets you disconnect an assembly with one hand, without any trouble.

Get a better grip on product performance with AMP.


MIL-C-83503 QUALIFIED VERSIONS

For more information, call the AMP-LATCH Connector Desk at (717) 780-8400.

mini

AMP Incorporated, Harrisburg, PA 17105.

AMP and AMP-LATCH are trademarks of AMP Incorporated.

CIRCLE NUMBER

MP means productivity.

Getting the jump on DEC^{*}compatible Winchesters

You've got to keep hopping to be a winner in the DEC-compatible world, and Charles River Data Systems has been out front with innovative technology for eight years. Now we've taken a big jump ahead with our new RLX3010 disk, featuring removable Winchester backup, RL02 software compatibility, and 22-bit addressing.

RLX 3010

Removable

Winchester drive

RLX.3010

TV	O DISK SUBSYS	STEMS
Model	Main Storage	Backup
RLX3010	31.2MB fixed Winchester (=3RL02)	10.4MB removable Winchester (=1RL02)
RLX3001	31.2MB fixed Winchester (=3RL02)	1.0MB double-sided floppy
TWO SING	LE-BOX COMPUT	TER SYSTEMS
Model	Description	
RLX3010B	Same as RLX3010, plus built-in Q-bus backplane	
RLX3001B	Same as RLX3001, plus built-in Q-bus backplane	
-	• Q-bus compatibi RSX-11M, RT-11 • LSI-11 processor	lity under

interface cards available

Complete system in 7-inch

0000

Fixed

drive

Front-panel

console

Winchester

enclosure

 Substantial quantity discounts available

Optional Q-bus backplane and floppy backup, too

To build a potent yet remarkably compact, economical single-box system, choose the RLX3010B with built-in backplane. Just plug in LSI-11 processor, memory, and interface boards, and cut cost, space, cabling, and power requirements significantly. And for even greater economy, there's the RLX3001 with RX02-compatible

floppy backup (see chart). For more information, contact Charles River Data Systems, 4 Tech Circle, Natick MA 01760, (617) 655-1800; Western Region (602) 863-7739; Europe (44) 4955-56545.

RLX 3010



CHARLES RIVER DATA SYSTEMS

Removable Winchester backup

Introducing a uniquely sensible approach to Winchester backup: a second Winchester. The RLX3010 combines a 31.2-megabyte, 8-inch, fixed Winchester with a 10.4-megabyte, 8-inch, removablecartridge Winchester. Each on a separate spindle. Use all 41.6-megabytes for data and programs. Then use the 10.4-megabyte cartridge for program swapping or highspeed, file-oriented backup. With the fixed disk running. A front panel diagnostic console permits off-line testing.

Optional Q-bus backplane

10000

Removable

Winchester

cartridae

* DEC is a registered trademark of Digital Equipment Corporation

The RLX3010 fits in a 7-inch-high

table-top or rack-mount enclosure.

(at 40 inches tall and 300 pounds).

Yet it's equivalent to four DEC RL02s

TEST & MEASUREMENT

3-level monitor/line tester



Line tester 232LT provides inline status display and true 3-level monitoring for RS-232 communication lines. Thirteen dualcolor (red and green) LEDs indicate red for ≤ -3 V (marking), and green for \geq 3 V (spacing). LEDs remain off for signal levels between 3 and -3 V (undefined per RS-232). Line tester is powered from signal line, reducing size and weight and eliminating need for batteries. Line power ensures that dead batteries will not cause malfunctions or render unit inoperative. Current requirements of less than 3 mA for each LED allows continuous monitoring of marginal lines. Each signal line, except protective ground, contains DIP switch, which allows any signal line to be opened. Pins located on both sides of the switch are used as test points for meters and oscilloscopes. Patch cords provided with unit permit cross patching of signal lines. Tester measures 3.3" x 5.1" x 0.81" (8.4 x 13.0 x 2.10 cm) and weighs approximately 7.25 oz (0.21 kg). Price is \$159/unit. Carroll Touch Technology, 1212 Hagan St, Champaign, IL 61820.

See at Booth M164

Circle 536

DATA COMMUNICATIONS

Statistical multiplexer and network processors

System 110 microprocessor based, statistical multiplexer can be used in point to point configuration, or as a slave unit in a full function network. It can service both terminals and host computers at either end of the network. System provides improved performance in single phone line networks, connecting several terminal clusters to host computer site over 1 telephone line. Two models are available—system 110/4, which supports from 2 to 4 ports over a single line, and system 110/8, which supports from 2 to 8 ports over a single line. The stat mux can share a single, multidrop trunk link modem. System 110 starts at \$1495 for 4-port capacity. System 120 network processor provides identical features as System 110, but can support up to 32 ports. Basic system is \$2450 for 16-port capacity.

Both systems can drive a 19,200-baud trunk link, and can simultaneously accept input from up to six 9600-baud asynchronous block mode devices. Systems have internal buffer of

MAY 1982

20,000 chars. Multidrop station number is switch-selectable from the multiplexer. With reconfiguration option (RCO), user can reconfigure port parameters via switches, and also guarantee that controller module, with nonvolatile memory, does not loose online configuration during power outages. Systems 110/120 have bidirectional flow control to expand the number of different hosts and block mode terminals the system can support. They can optionally reinitialize auto-baud detection upon detection of a long space, to facilitate autobaud with direct-wired terminals. Stat muxes have configurable X-OFF/X-ON delay timer.

System 125 is a 32-port max multidrop master network processor that acts as a master to 2 or more polled slave processors. System can be configured to control up to 15 slave stations. Any number of ports can be assigned to each slave station for up to 32 slaves. Slaves can be DCA system 105, 110, 115, or 120 units. In addition to providing identical features as systems 110/120, system 125 has built-in reconfiguration feature which allows network operator to reconfigure port parameters with/without a console; a built-in console port which allows operator to obtain measurements of traffic to/from each slave, errors on trunk, and per port traffic; and multidrop multiplexing for up to 15 remote locations to share a single phone line. Basic System 125 starts at \$3250 for 16-port capacity. **Digital Communications Associates, Inc,** 303 Technology Park, Norcross, GA 30092.

See at Booth 5242

Circle 537

Medium distance modem

Metromodem transmits synchronously with total reliability at speeds of 2400 or 4800 baud over distances up to 50 mi (80 km). Self-test and analysis features include analog loopback, digital loopback, and a control for placing the remote modem in digital loopback from the local Metromodem. Device is compatible with any combination of Western Electric 3002 load wire pairs and the T1 carrier network, and is available in a standalone model or rackmounted card with 8-modem nest. Other std options include 2- or 4-wire operation, external or internal timing, and carrier control or constant carrier. **Astrocom Corp**, 120 W Plato Blvd, St Paul, MN 55107.

See at Booth M221

Circle 538

4800-baud microprocessor modems and desktop network control computer

Three synchronous microprocessor driven 4800-baud data modems for use on dial lines, and point to point or multipoint leased or private lines feature signal processing functions and fast train of 27 ms. Built-in diagnostics with error rate display, BER, alternate dial interface, echo protect, data/voice mode, auto/manual answer, front panel interface indicators, and optional secondary channels are included.

Model 4800/FP provides fast polling operation in multipoint network. It uses CCITT compatible 8-phase DPSK modulation and a proprietary fast train algorithm. Unconditioned 3002 leased line (2- or 4-wire) or switched (2-wire) line, selectable with front panel switch, can be used. Modem 4800/27 is compatible with CCITT recommendation V.27. Modem is also compatible with the echo suppressor and auto-answer signaling in U.S. switched network. Unconditioned 3002 leased line or switched line can be used. Model 4800/208 AB modem is an

DATA COMMUNICATIONS



alternative to Bell models 208A (leased) and 208B (switched) modems in dial-up and leased line networks. It utilizes an 8-phase DPSK modulation.

A desktop microcomputer with diskette storage allows the company's network supervisory system to control local and remote sites from a single point. Console provides an active interface to remote alarming, protocol monitoring, and switching capabilities. Unit can detect and display local and remote network problems automatically. Unit can also gather, report, and log data to generate network statistics. To isolate faults, console can analyze remote site protocol data. **Digilog Inc, Network Control Div**, 1370 Welsh Rd, Montgomeryville, PA 18936.

See at Booth 5525

Circle 539

Network diagnostic/measurement facility

Network Performance Facility (NPF), an addition to the company's Communications Management Series diagnostic and control systems, provides main channel data measurements in large scale communications networks. The NPF measures line protocol performance in 3270 BISYNC, 3270 SDLC, 2780/3780, 2260/2848, ASCI II asynchronous, Univac Uniscope, and Burroughs and Honeywell VIP 7700. It permits up to 22 realtime measurements to be collected simultaneously and continuously for every line, control unit, and device in a network. Facility provides information on network and line availabilities, response time categorized into network and host delays, retransmission measurements for line error and analysis, and message statistics/polling data, and other general communications measurements. Coupled with network information data base of the user's line names, applications, line groups, and network configurations, the NPF provides realtime color graphics displays, alarms based on user selected threshold values, and realtime hardcopy reports for use in trouble ticketing and archival storage applications. Basic menu and function keys allow viewing of global network status or zooming in on specific problem areas. System price begins at \$41,000. Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166.

See at Booth 4010

Circle 540

Distributed data processing system commands multiple functions from single terminal

MIND series distributed data processing products allow multiple function levels from a single, intelligent display. A system can support up to 60 displays; 3-level architecture allows processing functions to be directed at display. Source and format data entry, local and remote interactive operations, and word processing can be performed concurrently.

Architecture levels include a distributed processing unit for file handling and system resource allocation, as well as data and remote job entries. Interactive processing unit functions on the front end to handle 3270 and other interactive communications with both mainframe and locally resident data bases. Intelligent displays allow use of all available series resources from any 1 display. System also provides full SNA type II operation with simultaneous accommodation of 4 mainframes for remote batch operations. Series communicates with host to retrieve or update files by emulating a 3270 BSC or SNA display. Bisync mode is also supported. Series supports printers, consoles, card readers, floppy and hard disks, and magnetic tape storage devices. 280 based displays with 64k-byte memory are available with 960-, 1920-, 2560-, and 3440-char capacities. Series is priced domestically in \$80,000 range for a typ 5-workstation application.

Low profile terminal 9279-2A, also being shown, can produce base red, white, blue, and green colors from existing application programs. Screen size is 1920 chars. Status line provides operator with system data and diagnostics. The 9279 model 2A is part of the 9200 microprocessor based, interactive computer system family. Base model 9210 is compatible with IBM 3270 product line. 9200 supports up to 32 devices/processor, with both local and remote processor communications at speeds up to 9600 baud. Local attachment is via byte, block, or selector channel in 3272 or SNA modes. Remote attachment is via BSC or SNA/SDLC protocol modems. **Harris Corp, Data Communications Div**, 16001 Dallas Pkwy, PO Box 400010, Dallas, TX 75240.

See at Booth 4000

Circle 541

Reduced size intelligent Bell 212A modems

Custom designed intelligent Bell 212A, 1200- and 300-baud fullduplex modems are configured on a single PCB that occupies 50 in² (322 cm²). All essential modem circuitry is packaged on LSI chips, including modulator, demodulator, transmit/receive filters, carrier detector, AGC, and answer tone generation/ detection. Using 212A chips as the nucleus, the company adds telephone lines, user and control interfaces, and provides FCC and UL approval. The package also contains microprocessor and custom software for optional automatic dialing with stored numbers, redial, interactive conversation with terminal operator, error control, and network diagnostics. Modem pricing begins at \$325, depending on configuration. **Racal-Vadic**, 222 Caspian Dr, Sunnyvale, CA 94086.



See at Booth 5322

Circle 542





Many companies at NCC will be showing products that have either been displayed previously or described in recent issues of *Computer Design*. Some exhibitors were unable to supply adequate information on their products in time for processing as "first time shown." These brief summaries are a sampling of additional equipment that NCC '82 attendees can expect to see.

Able Computer, Irvine, Calif—34 and 44 MagnumTM and other DEC compatible computer systems, as well as UNIBUS system enhancement products, including the DH/DM 16-line, single-board modem control DMA multiplexer— **Booth 4042**

AGT Computer Products Inc, Torrance, Calif—96-char Qume and Diablo compatible extended life dual plastic printwheels, and 88- and 96-char metalized and plastic printwheels for other printers— Booth A347



Amperex Electronic Corp, Hicksville, NY—GP300 letter quality dot matrix printer can reproduce logos, charts, fixed graphics, optical wand readable bar codes, and OCR-A and -B characters. An 18-needle (9 x 9) interlaced dot matrix head permits 18 x n character generation in one pass— Booth 8009

Anderson Jacobson, Inc, San Jose, Calif—AJ 1233 originate only, full-duplex, acoustic coupler/modem communicates with Bell 212A, VA 3400, and AJ 1200 series modems, as well as Bell 103/113 low speed modem— Booth 4322

Applied Magnetics Corp, Goleta, Calif-"Tri-Pliant" design floppy disk heads, composite Winchester type disk heads, and high density tape heads-Booth 2100



Atlantic Research Corp, Alexandria, Va—Lightweight Interview 29A/30A/40A series data analyzers are suited for field service and other applications. Each data communications test unit displays 512 characters of data and protocol sequences from an 8k buffer— Booth 4525

Audiotronics, North Hollywood, Calif-General purpose, model 9VM967 9" (23-cm) monochrome monitor features silicon transistorized circuitry, 700-line horizontal resolution, and heavy duty single-chassis construction-Booth 4535

Ball Electronic Display Div, St Paul, Minn—CRT data display monitors for data terminal, word processing, and graphics applications, including 15" (38-cm) monitor for data terminals— Booth 4018

Benson Inc, Mountain View, Calif-Electrostatic printers/plotters, pen plotters, and vector to raster converters-Booth 4745

Boschert Inc, Sunnyvale, Calif—Custom switching power supplies designed for major customers and produced in high volume— Booth 3434

Bytronix Corp, Irvine, Calif—Series 4000 and 5000 NOVA compatible computer systems feature up to 128k bytes of memory on single-board CPU, instruction set, std or high speed data channel, battery backup, and separate power supply— Booth A642

California Computer Group, Costa Mesa, Calif—C-RGM80, a 160M-byte Winchester disk/controller combination that emulates Digital Equipment Corp's RM80 VAX750 160M-byte Winchester drive, uses an Emulex SC750 VAX750 disk controller and Fujitsu M2284 160M-byte Winchester disk— Booth M142 Canford Manufacturing Corp., Cortland, NY—Custom molded injection and structural foam thermoplastic parts and enclosures— Booth A156

Central Data Corp, Champaign, Ill— Z8000 microprocessor based board and systems, plus full MULTIBUS compatible product line— **Booth A518**

Cincom Systems, Inc, Cincinnati, Ohio —Series 80 Total independent database management system supports multilevel hierarchies, inverted lists, and partially inverted files on minicomputers, as well as on most non-IBM mainframes— Booth 3010

Clary Corp, San Gabriel, Calif—30-kVA uninterruptible power system eliminates power outages and disturbances. Specs include 2.5% harmonic sine wave distortion, 60 ± 0.5 Hz output frequency, and $\pm 2\%$ voltage to critical load— **Booth M127**



Computer Transceiver Systems, Inc, Paramus, NJ—Execuport 4120 1200-baud, 120-cps portable terminal system produces high resolution characters 5, 10, and 17 to the inch, and prints up to 233 chars/line on 8.75" (22.23-cm) or 14.875" (37.783-cm) wide paper. Execuport 400 portable impact printer weighs 12 lb (5 kg)— Booth 3410

ConTel Information Systems, Inc, Great Neck, NY—Demonstrations of RTFILE interactive relational DBMs for Digital Equipment Corp mini- and microcomputers on applications suggested in advance by attendees— Booth 7922

Custom Systems Inc, Eden Prairie, Minn —Peripheral controllers, 2 compatible with Data General NOVA and Eclipse minicomputers, and 2 with Texas Instruments 990 series minicomputers— Booth 5016

Microcomputer Emerges From Logic Analysis. The NPC-764.



The NPC-764 is not just another logic analyzer—it's an experience.

It's not just a way to analyze logic—it's a way to save time.

There are no knobs and switches on the front panel, and that's as much a philosophy as a reality.

In fact, there's no front panel at all—just a familiar ASCII keyboard, a 5¼" floppy disc, and a CP/M[®] Operating System.

For the first time, you can have multiple analysis functions—plus

general-purpose computing capabilities—in a single package. All analysis functions are ROM-based and ready to go when power is turned on.

- Use a 48-channel, 1000-word Logic State Analyzer to trace your software. Dedicated probes and disassembled mnemonics make microprocessor analysis a snap.
- Call up an independent 16-channel Logic Timing Analyzer to debug your hardware. Sampling rates to 100 MHz and a 5 ns glitch memory give you the analysis power you need for debugging high-speed logic.
- Capture and display your system's analog signals with a 50 MHz Waveform Analyzer. Digital oscilloscope functions have never been so cost-effective and easy to use.
- Receive, transmit, and edit RS-232 data with a Serial Analyzer. Now you'll know whether an I/O problem is in your computer or peripheral.
- Use a 100 MHz Counter-Timer to measure hardware and software execution times. A built-in Signature Analyzer

Leading The Way In Analysis Technology



helps you fault-isolate to the component level. Store over 50 tests on

disc for later recall and execution. RS-232 and video printer interfaces make record-keeping easy.

 Add IEEE-488 test functions using a built-in Computer-Controller. With the NPC-764, you'll never need another GPIB instrument controller. Apply these features independently, link them together,

automate them. They're

always at your fingertips through easy-to-use, self-prompting menus.

And when the testing is all done, don't put your NPC-764 away. Since the CP/M Operating System makes it a desktop computer, you can generate engineering documents using TEXT EDITOR; or program it in BASIC, PASCAL, FORTRAN and other popular languages; or choose from among numerous, commercially-available programs to suit your application.

Never before has a single test instrument been so all encompassing, so productive, so reasonably priced.

Experience this new concept in test and measurement. To get additional information, prompt applications assistance, or a demonstration, contact one of our technical specialists at: Nicolet Paratronics Corporation, 2140 Bering Drive, San Jose, CA 95131. (800) 538-9713 (Outside California), (408) 263-2252 (California), TWX: 910-338-0201.

CP/M is a registered trademark of Digital Research.





Cyberex, Inc, Cleveland, Ohio—CATDTM computer aided telephone diagnostics system, a service concept for UPS and other power conditioning equipment, links customer's equipment with the Cyberserve service organization—**Booth 2030**

Cynthia Peripheral Corp. Palo Alto, Calif—D120/140 removable and fixed/ removable formatted disk drives with optional SASI interface, plus D160 high capacity compact Winchester fixed disk drive with 120M bytes formatted— **Booth 3402** Data Communications Corp/Cylix Communications Network, Memphis, Tenn— Data communications network service provides diagnostics for modems and local loops through use of high speed satellite channels— Booth 1333

Data General Corp. Westboro, Mass -16-bit EclipseTM S/20 and S/120 minicomputers with MP/AOS realtime operating system, plus office automation products— **Booth 4508**

Data Motion, Torrington, Conn—Dualfeeding tractor moves individual sheets or perforated folded paper; plus other tractor feed and sheet feed mechanisms for printers— Booth 3546

Data Peripherals, Sunnyvale, Calif— Completely compatible 42.4M-byte Puma Winchester disk drive and 10.6M-byte 8" removable cartridge Winchester disk system— Booth 1631

Data Printer Corp., Malden, Mass— Series 3001 high speed band line printers and series 1200 microprocessor controlled line printers— Booth 4716

Datec, Inc, Chapel Hill, NC—Model 212 dual-speed modems with optional CPU, model 30 and 32 acoustic couplers, and multiple-modem rack— Booth A834

Digi-Data Corp, Jessup, Md—100- and 125-ips 0.5" streaming tape drives for 1600 bpi, with 3200 bpi optional at 50 and 62.5 ips, series 40 start/stop tape drives, and series 6400 0.25" cartridge tape drives—**Booth A337**

Digital Research, Pacific Grove, Calif— Demonstration of CP/M-68KTM operating system on a 68000 based system— Booth A507

Dolch Logic Instruments, Inc, San Jose, Calif—Model 4850A 48-channel logic analyzer with model 8086 trace module— Booth M100



Critical picture definition. Does your application require high resolution color graphics? PrintaColor's GP1024 ink jet printer lets you be critical – with dot addressable color control of each pixel in a 1024x1024 display.

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Electronic Processors, Inc, Englewood, Colo—STR^R-Stream compact 0.25" cartridge incremented recorder backup for Winchester disk stores up to 17M bytes in space of 8" floppy—



Booth A729

Emcor Products, Rochester, Minn— Series 10 cabinetry features 1.75" (1.76-cm) wide frame channels, fully welded frame corner members, and multiformed zinc plated mounting angles— Booth A826



Ex-Cell-O Corp. Remex Div. Irvine, Calif —RFD 960, a 5.25" flexible disk drive with 96-tpi data storage, and RFD 480, a 48-tpi version, are 2.25" (5.7 cm) high, ANSI compatible, and equipped with direct drive brushless motors— Booth 5032

Everest Electronic Equipment, Anaheim, Calif—DEC compatible cabinets, including front and rear doors, filler panels, retractable stabilizer feet, and power supply and controller— Booth A750

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Gould Inc, Electric Power Conversion Div, San Diego, Calif—6000 series 45-kVA UPS offers high efficiency and superior output performance in 78" x 60" x 30" (198- x 152- x 76-cm), 3200-lb (1451-kg) unit— Booth 4518



Integral Data Systems, Inc, Milford, NH —Prism 80 and 132, 200-cps, 24 x 9 or 18 x 9 dot matrix printers have microprocessor controlled Centronics and RS-232-C interfaces— Booth 4749

Intel Corp, Santa Clara, Calif—Database processor, 86/330 integrated OEM microcomputer system, and NDS-II Ethernet development system using Intellec microprocessor development workstations as nodes— Booth 6610

Intelligent Systems, Norcross, Ga— IS/2048 fully integrated, intelligent terminal combines color and full-screen graphics and includes a 13 " (33-cm) CRT, CPU, std level 4 ASCII 72-key keyboard, and graphics package— Booth A500

Interdyne Co, Van Nuys, Calif—Unireel 650 0.5" tape package with 250M-byte capacity and model IU 1650 tape drive, as well as IC 2500 digital cassette tape drive— **Booth 6904**

Interstate Electronics Corp, Anaheim, Calif—VRT101 and VRT200 intelligent voice terminals, VRQ400 Q-bus and VRM102 MULTIBUS microcomputer compatible boards, and other voice recognition modules— Booth 6923

Isoreg Corp (formerly Frequency Technology, Inc), Littleton, Mass—Modules protect computers from voltage spikes and brownout voltage drops, as well as from voltages that remain excessively high on a near-permanent basis—**Booth 2032**

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La Marche Manufacturing Co, Des Plaines, Ill—Uninterruptible power systems— Booth 2737

Liebert Corp, Columbus, Ohio-SitemasterTM microprocessor based monitoring system for company's power conditioning products and external computer support functions, plus the Accommodate2TM, a combined environmental control and power conditioning system for smaller data processing center— Booth 7909



3M, St Paul, Minn—Model 723 high speed computer output micrographic printer, full line of magnetic media, data cartridge drives, and compact disk drives— Booth 4528

M/A-COM DCC, Inc, Germantown, Md— Data communications products including statistical multiplexers, switch multiplexers, and error controller, all with optional built-in modems, and CP9000 communications processor—

Booth 1133

Matrox Electronic Systems Ltd, Montreal, Quebec, Canada—GF-18 modular color graphics CRT terminal system emulates Tektronix 4010/4114 terminals, features 512 x 512 x 8 resolution, color overlay alphanumerics, 700-ns/pixel vector generator, 16 x 10⁶ color lookup table, and 8- or 16-bit CPUS— Booth M239



Microcomputer Systems Corp, Sunnyvale, Calif—UP-1697 disk controller operates up to 4 SMD type drives and permits HP-IB systems to use all attached drives as Hewlett-Packard drives; also HP compatible drives and mass storage systems— Booth 4038

Microdata Corp, Irvine, Calif— SovereignTM multifunction computer system for distributed data processing, SequelTM large business system with 32-bit CPU, Reality^R small business system, and ALLTM software generator— **Booth 5006**



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Micromation, Inc, San Francisco, Calif-Mariner and M/System computer systems, and M/Link intelligent communications controller-Booth 5707



Micro Peripherals, Inc, Salt Lake City, Utah-Model MP150 wide carriage printer features heavy duty printhead rated for over 100 x 10⁶ chars continuous duty, 7 x 9 matrix font for high speed data printing, 11 x 9 serif style matrix font for correspondence quality printout, and graphics capability-Booth 4755

Minicomputer Technology, Palo Alto, Calif-Single-board emulating and compatible controllers to interface DEC. Data General, and Perkin-Elmer computers to various SMD compatible disk drives-Booth 2924



Multitech Electronics, Inc., Sunnyvale, Calif-Micro-Professor Z80 based microcomputer system can serve as educational and prototyping tool as well as a production OEM microcomputer board. and includes EPROM programming and speech capability-Booth A300

National Semiconductor, Santa Clara, Calif-NS44F 256k- x 26-bit dynamic NMOS random access single-card memory system replacement/enhancement module for the PDP-11 extended, modified, or standard UNIBUS; plus NURAMTM high speed bulk RAM and HEX 3000TM controller for all UNIBUS systems-**Booth A734**

On-Line Software International, River Edge, NJ-Data VantageTM software database management removes the complexities of IMS program testing while making the IMS environment easier to control-Booth 8019

Orange Micro, Inc, Anaheim, Calif-Centronics compatible parallel interface for the Apple II and II Plus microcomputers-Booth A545

OSM Computer Corp, Santa Clara, Calif-ZEµSTM combines a Z80A based microcomputer module with minicomputer performance and capacity. including hard disk storage of 34M to 600M bytes-Booth 4722

Point 4 Data Corp, Irvine, Calif-Mark 3, 5, and 8 minicomputers, FORCE automatic programming system, Lotus cache memory, rev 8 of IRIS operating system, and 4SITE realtime turnkey project control system-Booth 3412



Printek, Inc, Benton Harbor, Mich-200-cps model 910 and 340-cps model 920 multifunction printers-Booth A664

Sanyo Seiki (America) Inc, Lyndhurst, NJ-"Total involvement" approach to sophisticated control systems and electronic components-Booth A800

Seagate Technology, Scotts Valley, Calif -6.38M-byte ST506 and 12.76M-byte ST412 5.25 " micro-Winchester disk drives feature 5M-bps transfer rate, 3-ms track to track access time, 8.33-ms avg latency, soft error rate of 1 per 1010 bits read, and hard error rate of 1 per 10¹² bits read-Booth A218

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CIRCLE 113

Sharp Electronics Corp, Paramus, NJ-



Model PC-1500 handheld personal computer features 7 x 156 programmable dot matrix LCD and Extended BASIC language operating system, capable of handling 2-dimensional arrays, variable string lengths, program chaining, and full graphic commands— Booth 1622

Software AG of North America, Reston, Va—Adabas, Natural, Com-Plete, and Adabas M software— Booth 3104



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Spectra Logic Corp., Santa Clara, Calif— Single-board emulating disk controller for Perkin-Elmer minicomputers permits attaching up to four 80M- or 300M-byte drives, UNIBUS compatible controller for DEC minicomputers to attach up to 4 SMD drives in up to 16 different drive types, and "streaming" software for DEC minicomputers— Booth 8702

SSM Microcomputer Products Inc, San Jose, Calif—AIO-IITM serial/parallel interface board for the Apple II combines 2 boards into 1 unit and permits microcomputer to be connected to a wide variety of peripherals; it performs 4 independent functions: serial modem, serial terminal printer, parallel Centronics compatible printer, and general purpose parallel port—**Booth 8600**

Summagraphics Corp, Fairfield, Conn— Bit Pad One and Ten tabletop digitizers for CRT cursor control, data entry, menu input, or graphics input; ID series singleand dual-tablet configurations; Supergrid, which uses direct magnetostrictive technology; and Summagrid electromagnetic digitizers— Booth 7915

The Superior Electric Co, Bristol, Conn —Stabiline^R ac voltage monitor and voltage conditioning equipment— Booth 3111

Syncom, Mitchell, SD—0.5" magnetic computer tape, 8" and 5.25" flexible diskettes, digital cassettes, MC/ST magnetic cards, top loading and front loading disk cartridges, disk packs, data modules, and 0.25" data cartridges— Booth 5510

Systems Group, Orange, Calif—Business ExpressTM software system generates user application solutions directly from menu driven prompts, bypassing the use of high level languages— Booth A162

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Tec, Inc, Tucson, Ariz-Series 80 Data Screen^R CRT video display terminal meets international ergonomic requirements; and 630C combines smart CRT terminal with magnetic stripe card reader-Booth 7011

Telegenix, Inc, Cherry Hill, NJ-Remote controlled TDS2000 flat panel video data display, 10 times standard size, is visible from 100 ' (30 m) in bright light-Booth 7006

Telex Computer Products, Inc. Peripheral Products Div, Tulsa, Okla-6200 series OEM line of 19" (48-cm) rackmountable tape drives for use with minicomputers and 8020 series end-user tape drives feature 6250-bpi density and 125-ips speeds-Booth 2013

Termiflex Corp, Nashua, NH-Handheld control/display devices for OEM applications display up to 80 alphanumeric characters; send and receive all 128 ASCII codes; include RS-232-C or current loop signal interface; have 10- to 240-cps speed, bit-serial asynchronous; offer odd, even, mark, and space parity; and weigh 12 to 19 oz (340 to 539 g)-Booth 2001

Testor, Inc, Huntington Beach, Calif-Sapphire family of 14" Winchester disk drives with 83M-, 165M-, and 200Mbyte capacities unformatted-Booth A741



Texas Instruments Inc. Houston, Tex-Business System 200 small business computers based on TMS9900 16-bit microprocessor and compatible with DS990 family and TMS99000 high performance microprocessor offer 64k bytes of memory and use 64k-bit dynamic RAM chips-Booth 4504

Three Rivers Computer Corp. Pittsburgh. Pa-PERQ^R single-user workstation features a minimum of 256k bytes of main memory, integral Winchester disk, 10M-bps Ethernet local network, high resolution raster scanned graphics display, floppy disk option, and IEEE 488 and RS-232 interfaces-Booth M129

Topaz, Inc, San Diego, Calif-Powercenter, a self-contained mobile power distribution system with complete power conditioning for protecting computers from power disturbances-Booth 5534

TSK Electronics Corp, Duarte, Calif-KT5 5" (13-cm) green CRT monitor has with glare or nonglare tube, P31 phosphor, and a display format of 64 x 16 lines (5 x 7 dot matrix). Video band is greater than 12 MHz; active display area is 92 x 70 mm. 9" (23-cm) and 12" (30-cm) models are also available. Model KG-12N green phosphor monitor has detachable filter for choice of color density; 12" (30-cm) screen displays 25 lines x 80 chars in 5 x 7 matrix, or 16 lines x 64 chars in 7 x 9 matrix-**Booth A453**

Universal Data Inc, Clarkston, Mich-Handheld input display terminal weighs 21 oz (595 g), functions at 300 and 1200 baud standard or optionally up to 9600 baud, is fully RS-232 compatible, uses an 8-bit ASCII data code as standard but other disciplines are optional, and has a 2-line, 16-char LCD display-Booth M255

Visual Technology Inc, Tewksbury, Mass -Model 500 and 550 microprocessor based video display terminals with 768- x 585-line resolution on 14" (36-cm) screen emulate the Tektronix 4010; model 300 provides 192 lines of display memory-Booth 1633

Volker-Craig Inc, Rochester, NY-CRT terminals including "dumb" conversational, editing, Hazeltine emulating, APL, and DEC VT-52 and -100 emulating-Booth 1019

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CIRCLE 116

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249 The *iAPX* 432 processor's instruction set was chosen with the compiler writer in mind rather than the assembly language programmer

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TEST & MEASUREMENT

BORROWING RF TECHNIQUES FOR DIGITAL DESIGN

Using an rf network analyzer as a design aid may seem strange to digital designers, but the insight gained from looking at the frequency domain can be vital

by David Montgomery

s computer clock rates increase, logic circuits that have gate delays comparable to the time delays between circuit elements have become commonplace. At today's high clock rates and fast rise times, these interconnections can no longer be ignored as they take on the appearance of transmission lines. Unless connections are designed properly, reflections can occur that will distort the incoming pulses enough to produce ringing and glitches that are difficult to troubleshoot. A transmission line approach to high speed digital circuits is necessary because fast rise times involve significant frequency components in the radio frequency and low microwave range. The faster the rise time, the more important it is to consider the pulses as traveling on a radio frequency "cable," rather than a conductor designed for direct current or low frequency voltages.

An analog radio frequency (rf) network analyzer is currently being used to analyze high speed circuits. To follow this rf approach, the first step is to estimate the approximate bandwidth required for distortionless pulse transmission. Fig 1 plots an approximate relation between rise time and bandwidth, and notes the range of some common logic families.¹

The need to minimize pulse reflections off interconnections and terminations—eg, sockets, edge connectors, and device input/output ports—is just as important as supplying adequate pulse path bandwidth. In a high performance logic circuit, the time required for reflections to travel between gates approaches the pulse rise time. As a result, the reflection becomes a significant cause of bit errors (Fig 2).

Efforts must be directed toward the design of connectors and printed circuit (PC) boards to reduce these pulse reflections. It is necessary to minimize the size of the reflected signal, whether it is being fed into a device or onto a transmission line. Comparing the size of the reflected signal with that of the incident signal is one way to characterize the quality of the connection. This can be stated in terms of a measurement in which the reflected voltage (V_{ref}) to incident voltage (V_{inc}); ρ takes on values from 0 to 1, which represent no reflection and complete reflection, respectively. For a connection between two transmission lines of impedances Z_0 and Z_1 , ρ can be calculated²

$$Q = \frac{V_{ref}}{V_{inc}} = \frac{Z_1 - Z_0}{Z_1 + Z_0}$$
(1)

In this case, the reflection coefficient looks into a line with impedance Z_1 from a transmission line with impedance Z_0 . If the two impedances are equal, then $\rho = 0$, which means that no portion of the signal is

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Fig 1 Pulse rise time/bandwidth relationship. Bandwidths for any family can range from typical clock rates to highest frequency components of significance within pulse.

reflected. Intuitively it can be seen that if the two impedances are equal, any discontinuity will be invisible. In addition, if one of the impedances is unknown, it can be easily calculated once the reflection coefficient is measured.

Phase angle, ϕ , can be calculated in degrees between the reflected and incident signals, yielding the complex reflection coefficient, Γ .

$$\Gamma = \frac{V_{ref}}{V_{inc}} \qquad \left[\phi_{ref} - \phi_{inc}\right] \tag{2}$$

This phase change occurs when at least one of the impedances (either Z_0 of the transmission line or Z_d or Z_1 of the discontinuity) has a capacitive or inductive component. Comparing Eq (1) and Eq (2), it can be seen that ρ = magnitude Γ .

Pulse reflections

As a starting point, examine the pulse transmission between a line driver and a receiver connected by a length



Fig 2 Pulse distortion due to reflections. False detection of logic 0 state results.

of PC board or cable (Fig 3). This emitter-coupled logic (ECL) driver has an output impedance of 75 Ω and is driving a trace with a characteristic impedance (Z₀) of 120 Ω ; the line receiver presents an approximate load impedance of 7.5 k Ω . Logic state 0 has a nominal value of 0 V while 1 has a value of 1.0 V. For calculating the reflected signals, the driver, line, and receiver need only be represented by their impedances.

When the positive voltage pulse traveling down the line hits the receiver, part of the signal is reflected back on the line due to the mismatch in line and receiver impedances. Amplitude and sign of the reflected signal depend on the difference in impedances. In this case the receiver is the load, so the reflected signal has amplitude

$$V_{ref} = \rho V_{inc}$$

where

$$p = \frac{Z_{\text{receiver}} - Z_{\text{line}}}{Z_{\text{receiver}} + Z_{\text{line}}}$$
$$= \frac{7500 - 120}{7500 + 120} = 0.97$$

Thus the amplitude of the reflected signal is $V_{ref} = \rho (V_{inc}) = (0.97) (1.0) = 0.97 V.$

The reflected pulse, amplitude V_{ref} , travels back toward the source where it encounters the driver output. Once again, part of the pulse is reflected due to the mismatch in driver and line impedances; it is assumed that any pulse amplitude attenuation from traveling the line is negligible. The driver output impedance is the load so the amplitude of this re-reflected pulse is

$$V_{\text{rref}} = \rho_{\text{d}} V_{\text{ref}} = \frac{(Z_{\text{d}} - Z_{\text{o}}) (V_{\text{ref}})}{Z_{\text{d}} + Z_{\text{o}}}$$
$$= \frac{(75 - 120) (0.97)}{(75 + 120)}$$
$$= (-0.23) (0.23) (0.97) = -0.22 \text{ V}$$

This negative signal is again traveling toward the receiver, but is delayed in time by T_d (the time it takes the signal to travel down the line and back), and will subtract from the signal present at the receiver input.

$$\tau_{\rm d} = (t_{\rm d}) 2 \, {\rm x} \, {\rm l}$$

where

$$t_d = (1.017) (0.475 \epsilon_r + 0.67) \text{ ns/ft}$$

and l is the line length. If the dielectric constant, ϵ_r , is 5 for the PC board, then

$t_d = 1.78 \text{ ns/ft} = 0.06 \text{ ns/cm}$

If the driver and receiver are spaced 1 ' (30 cm) apart, $\tau_d = (1.78 \text{ ns/ft}) (2') = 3.56 \text{ ns.}$ This pulse keeps bouncing between the driver and receiver, and is reduced in amplitude by each successive reflection from either ϱ_d or ϱ_R , the reflection coefficients of the driver and receiver, respectively. (See Fig 4.)

Depending on the timing of the -0.22-V re-reflection (with respect to pulse rise time position), it will cause the false detection of a low state. If the driver, line, or receiver impedance were different, resulting in a positive ρ_d or negative ρ_R , the re-reflected pulse would have been

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Fig 3 Equivalent circuit of ECL driver, line, and receiver. Pulse reflections can be calculated by viewing components as impedances.

positive in amplitude and might cause the false detection of a high state (or false clocking on latch of a flipflop) (Fig 2).

Crosstalk and line matching

Crosstalk, the amount of noise present due to nearby line activity, must be quantified before board layouts and design can be compared. A simple example of crosstalk is shown in Fig 5.

Line spacing, routing, and ground locations-points. paths, or planes-all affect the amount of crosstalk in a circuit or along a signal path. Acceptable crosstalk levels are usually set at a fraction, or percent, of the active line signal's maximum amplitude. By measuring the signal induced on the quiet line and comparing it to the active line signal, this fraction can be calculated. This quiet line signal is measured at different points in relation to the active line driver, giving rise to the terms "forward" and "backward" crosstalk. Crosstalk becomes a problem when the voltage induced on a quiet line by adjacent lines is high enough to produce a false logic reading at the receiver. Once a system is up and running, bit errors arising from crosstalk are difficult to troubleshoot and will occur intermittently (historically during crucial steps or processes). While proper positioning of ground lines or planes helps, this will be hit or miss unless improvements can be characterized. This calls for a direct test of crosstalk and line length to determine exactly where, and in what designs, problems arise.

Line length matching, more often a problem in parallel data transmission schemes, is a measure of the difference in delays that pulses encounter when traveling parallel paths. Pulses sent to the same point down parallel paths, in practice, rarely arrive at the same instant. Until recently, the difference in delays was so small, relative to the time of the high or low state, it could be ignored. In high performance logic circuits, especially when data are sent across or between boards, these differences in delays will skew the bit stream and cause an error. In long distance digital transmission, such as digital telephony, data can be encoded or framed in packets to detect when this slippage occurs. Obviously, within central processing units or other hardware internal to a computer, such framing is impossible. When this occurs, the byte or bytes will be lost. By measuring the lengths of the signal paths, it is easy to



Fig 4 Pulse bouncing caused by receiver/driver induced reflections







Fig 6 Effect of electrical length on delay in logic circuits. Unequal lengths cause bit slippage and errors in parallel transmission schemes.

see when these delay differences will reach an unacceptable level (Fig 6).

PC trace impedances

Regardless of whether an analysis is being done in terms of frequency or time (ie, looking at the pulse shape), it is necessary to calculate and measure the impedance of traces on a PC board. These impedances depend on the geometry of the layout and are sensitive to the dimensions of the board and conductor. Consequently, they fall prey to manufacturing tolerances. Dependence on

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Fig 7 Variables affecting PC board trace impedances. Conductor (trace) thickness, line geometry, and board dielectric constant all play role in trace impedance, Z. Equation has been checked empirically and found to be accurate over range of practical interconnection geometries. All measurements are in mils.

geometry for a stripline PC board is shown in Fig 7, which represents a single-sided PC board with a ground plane; recall that a power supply plane is an effective ground for rf signals. While this board is an oversimplified version of the multilayer boards used today, it illustrates impedance effects due to line width, conductor, and dielectric thickness.

Fourier transform of a square wave

Any time-varying waveform has an equivalent representation in the frequency domain, ie, in amplitude vs frequency terms.³ By examining both the frequency components of a pulse waveform and the frequency response of a connector, the type and size of pulse distortion can be calculated. Time domain analysis for a 33-MHz clock waveform is in Fig 8(a). Rise and fall



Fig 8 33-MHz square wave represented in both time and frequency domains

times, t_r and t_f , each equals 2 ns; high state time, τ , is 13 ns. Solid line represents the actual waveform, while the dashed segments indicate an idealized pulse with zero rise/fall times.

Equivalent frequency domain representation for both the idealized and actual pulse waveforms is shown in Fig 8(b). The solid line, the Fourier transform of the idealized waveform, follows the familiar sinc (x) function sinc (x) = $\sin(x)/x$. Zero rise time causes frequency components extending to infinity to be present, decreasing in amplitude by the factor

sinc (B) = $\sin (B)/B$

where

$$B = \pi t_n/2$$

 $n = 1, 3, 5, \dots$

The Fourier transform of actual waveform, shown by the dashed line, also contains frequency components to infinity but these are now scaled by the factor sinc² (B), again where

$$\mathbf{B} = (\pi) \, \mathbf{t}_{\mathrm{n}} / \tau$$

Because the magnitude of higher order frequency components falls off as sinc² (B), bandwidth needed for high fidelity pulse transmission is less than that needed for the ideal (zero rise time) pulse. This is simply another way of explaining the empirically derived practice of deliberately slowing a pulse rise time to reduce ringing. The larger ac component equals the pulse repetition frequency—33 MHz in this example. Intuitively, this follows from the crude approximation of a 33-MHz square wave with a sine wave of the same frequency. Negative frequency components simply represent sine waves that are shifted 180° (one-half of a cycle) from the 33-MHz fundamental sine wave.

To preserve the pulse shape, it is necessary that both amplitude and phase relationships of the frequency components not be distorted. When phase or amplitude is altered, component sine waves no longer add up to produce the original pulse. Distortion of the lower frequency components affects the general pulse shape more dramatically than distortion of higher frequency components. However, overshoot, undershoot, and slowing of rise time all result from distortion of the higher frequency signals. As used here, distortion includes the partial reflection of a signal off a connector or socket.

Because a voltage pulse is made up of several distinct sine waves, the reflection coefficient must be measured over a range of frequencies that encompass the sine wave components of the pulse. Thus, the design goal becomes one of minimizing the reflection coefficient over the range of frequencies.

What to measure and how

In a discussion of general sources of pulse distortion and diagnostic type measurements, the primary parameter of interest is Γ , the complex reflection coefficient.

$$\Gamma = \frac{V_{ref}}{V_{inc}} < [\phi_{ref} - \phi_{inc}]$$

For those readers familiar with scattering, or S parameters, Γ is the equivalent of S₁₁. The reflection



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coefficient, ρ , is simply the ratio of the voltages with no phase angle information, and can be obtained from Γ .

$$\varrho = mag(\Gamma) = \frac{V_{ref}}{V_{inc}}$$

Attention should be directed toward the equipment that makes these measurements; the amplitude and relative phase angle of the incident and reflected signals must be separated, detected, then measured.

Traditionally, the primary analytical tool for impedance measurements has been the use of a time domain reflectometer (TDR) for reflection measurement and fault location. TDR operation is analogous to closed loop radar in that a very sharp pulse is sent down a line (PC board trace or cable), then an oscilloscope waits for a reflected signal to return. The shape of the reflected pulse contains information about the inductance, capacitance, and resistance of the line and its termination, as well as the physical location of any discontinuities. Information supplied by TDR, while nominally quantitative, requires a good deal of interpretation. Finite sharpness of the stimulating pulse limits the information, relative to today's fast logic speeds. In addition, no information about the relative phase angle of the incident and reflected waves is supplied by TDR. While designs using TDR techniques, along with empirically derived know-how, have proved successful for present logic speeds, they are unsuitable for higher speed logic circuits.

Basics of a network analyzer

A network analyzer has three elements: signal source, test fixture or signal separation device, and receiver system (Fig 9). The source provides the analog (sine wave) stimulus for the test circuit, continuously sweeping upward in frequency at a uniform rate with constant power between designated start/stop frequencies. Sweeping up rather than stepping up over a sequence of discrete continuous wave frequencies enables glitches, such as narrowband resonances, to be observed. The frequency range selected for the measurement depends on the pulse rise time and repetition rate. Approximate bandwidth (BW) can be calculated

$$BW = \frac{0.35 N}{t_r}$$
(3)

Here t_r is the pulse rise time and N is the highest harmonic to be passed. In addition, Fig 1, shown earlier, plots the approximate bandwidth needed vs system rise time for N = 1 and N = 10.

The test fixture holds the PC board connector, or socket to be tested, and routes the analog signal from the source to the test device input. It also routes the reflected and transmitted signals to the appropriate receiver inputs for detection and measurement. Since the test fixture routes the analog signal to and from the test device, it is necessary that its frequency response be easily measured and repeatable over time, so that its effects may be subtracted and separated from that of the unit under test. Measurement accuracy can be further improved via mathematical error correction techniques, which require the addition of a microcomputer to handle the computations.⁴



fig 9 Network analyzer elements: signal source, fixture, and signal receiver

The receiver downconverts the rf signals to a lower intermediate frequency, while preserving all amplitude and phase relationships. With rf loosely defined as the 1- to 1500-MHz range, this conversion is necessary to accurately measure the magnitude and phase of rf signals. Amplitude and phase of the test signal are measured and recorded or displayed. Phase measurements compare the difference between the test signal and a reference signal. Typically, the receiver has three channels to measure incident, reflected, and transmitted signals simultaneously. After this, V_{ref}/V_{inc} (or V_{tran}/V_{inc}) is calculated and displayed by the receiver.

Reflection and transmission measurements can be made using a Hewlett-Packard 8505A network analyzer. The 8505A contains the source and receiver, while the test fixture described in this discussion is a Hewlett-Packard 8503A S parameter test set. This system is capable of amplitude and phase measurements from 500 kHz to 1300 MHz, or over any portion of this range. The company's 9845B desktop computer can record data and improve the measurement accuracy by error correction techniques mentioned earlier.⁴

Edge connector reflection measurement

Suppose a pulse with a 5-ns rise time is transmitted off a PC board through an edge connector. Since pulses can be reshaped by buffer circuits after the connector, the harmonic N = 7 will reduce the interconnection bandwidth required. From Eq (3), the necessary bandwidth can be calculated

BW =
$$\frac{(0.35)(7)}{(5 \times 10^{-9})}$$
 = 490 MHz

This will be the upper limit for the network analyzer's sweep frequency testing. The lower frequency limit need only be below the repetition or clock rate of the pulse that is to be passed. This ensures that the connector's response to the fundamental frequency can be observed.

Fig 10 shows the test setup. The network analyzer was configured to measure reflections off one pin of the edge connector, which is appropriate and adequate in view of the uniformity between pins.

Figure 11(a) is a plot of $-20 \log \rho$ vs frequency. A logarithmic plot allows a wider range of reflection coefficient values to be displayed than would a linear display of ρ . It can be seen that the return loss varies

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between 2 and 7 dB; equivalently, ρ varies between 0.79 and 0.45 in linear terms. Some overshoot or undershoot will occur if the 2-dB point (ie, where $\rho = 0.79$, at 165 MHz) corresponds to a harmonic of the fundamental pulse repetition rate. Actually, the least amount of reflection off the edge connector results in $\rho = 0.45$, which contributes additional overshoot and undershoot.

A polar plot of Γ , the complex reflection coefficient, is shown in Fig 11(b). The center of the circle represents $\Gamma = 0$, increasing linearly to the outside edge, which is $\Gamma = 11$. Phase angle values between 0° and 360° are read from the outside edge of the circle. Frequency information must be inferred from the start and stop points, or read directly from frequency markers on the trace (such as the one shown at 165 MHz). Previously, with the return loss $[-20 \log (\rho)]$ vs frequency rectangular plot, the larger the decibel value of return loss, the smaller the reflection coefficient. With this rectangular plot, the goal to minimize reflections is a direction to lower the entire trace; that is, to minimize ρ over the sweep range. Now, with the polar plot of Γ (which, unlike the rectangular trace, contains phase angle information but no frequency axis), the design goal is to collapse the trace about the origin; that is, attempt to reduce Γ to zero over the entire sweep. One advantage of the polar plot is that an overlay may be used to read resistive and reactive components of the connector impedance directly off the graph.⁵

Crosstalk measurement

Crosstalk measurement can be directly performed with a network analyzer. The rf source drives the active line while the receiver is connected to the quiet line to measure the induced signal. Quiet line signal can be measured at various points to more accurately determine the crosstalk effects of line geometry. A network analyzer provides more accurate and quantitative measurement of crosstalk levels than does a pulse generator and scope or logic analyzer.

Line length matching

In parallel data transmission schemes it is necessary that all signal paths—either parallel traces on a PC board or wires in a ribbon cable—have equal electrical length to ensure that pulses sent out together arrive at the same time. Electrical length is used since it may differ from the physical length of the line. To determine line lengths, the amount of phase shift a sine wave incurs when it travels each line under test must be compared. A sine wave undergoes a phase shift of 2π radians or 360° every time it travels a distance equal to its own wavelength, λ . Thus, if a line has electrical length d, then the total phase shift, $\Delta\phi$, of the sine wave is

$$\Delta \phi = \frac{a}{2} 360^{\circ}$$

This testing is at a fixed, continuous wave frequency because only with constant frequency does a uniform phase change over distance occur. In Fig 12, 32 lines were measured, all having 30-cm nominal electrical length. Wavelength λ was 200 cm, which corresponds to a continuous wave frequency of 150 MHz, so the expected phase shift would be

$$\Delta \phi = \frac{(30)}{(200)} \quad 360^{\circ} = 54^{\circ}$$

The 32 dots on the plot indicate the phase of the transmitted signal; they range from 52.5° to 59° , indicating



Fig 11 Result of edge connector reflection measurements. Return loss of between 2 and 7 dB is plotted against frequency (a). In (b) is polar plot of complex reflection coefficient measured in (a). Frequency markers can be placed directly on trace for convenience.


Fig 12 Results of line length test measurements. Plot of dots indicates a phase shift of 52.5° to 59° . These traces are unsatisfactory for use in a high speed digital application due to unequal delays they create.

electrical lengths of 29.2 and 32.8 cm, respectively. An application requiring high speed data to be transmitted in parallel lines like these would prove unsatisfactory because unequal delays in parallel bit transmission would be created.

Summary

With today's fast logic speeds, digital circuits can no longer be designed to handle only dc or low frequency voltages. These circuits have to be considered as wideband signal paths and the associated problems of impedance matching and bandwidth must be solved to provide distortion-free pulse transmission. Problems of pulse reflection and bandwidth give rise to bit errors that are difficult to troubleshoot using conventional digital test equipment. An analog rf network analyzer is ideally suited for making this type of measurement. Originally developed for communications equipment design and testing, where reflections and bandwidth have long been a concern, the network analyzer has become extremely valuable for high speed digital circuit design.

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SPECIAL REPORT ON FUTURE DIRECTION IN SYSTEMS DESIGN

DEVELOPMENT SYSTEMS

MEAD-CONWAY: A METHOD FOR SYSTEMS IN SILICON

The Mead-Conway approach to small quantity, custom integrated circuit design is fueling the VLSI revolution as a new breed of designers takes advantage of services and techniques previously unavailable

by Robert P. Smith

ncreasing use of custom very large scale integrated circuits is rapidly changing the electronics marketplace. Custom circuits accounted for 20% of the total world semiconductor market in 1981. By the end of this decade, custom circuits will make up 60% of a total market that will approach \$50 billion. Custom circuits offer several well-known advantages over equivalent designs implemented with standard circuits: lower power consumption, greater reliability, space savings, lower product assembly and test costs, and design security.

Traditional custom circuit burdens

Chip complexity and the resulting design costs have been the foremost problems associated with implementation of custom very large scale integrated (VLSI) circuits. Moore's Law, devised by Gordon Moore at Intel Corporation, formulates technological advances in semiconductor processing. This theory defines growth in chip complexity—ie, the number of devices per chip—

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Moore's Law dramatically illustrates the effect



that chip complexity has on design costs. In 1970 the most complex integrated circuits (ICs) contained fewer than 4000 devices. Total design time for implementing such circuits was two to three man-years. Moore's Law predicts that circuits containing millions of devices will be possible by the mid-1980s. Obviously, the use of traditional design methods will not suffice for designing such large and complex circuits. A new approach to the definition and design of large systems is clearly needed.

Growth of custom circuits has been hindered by the economics of semiconductor manufacturing. Design time is expensive. Traditionally, custom circuits have been justified only when large volumes were involved. In the traditional custom IC market, high volumes have been required to provide the semiconductor manufacturer with the necessary financial return for expensive



Fig 1 Moore's Law. Components per chip have doubled each year since 1960.

capital equipment investment costs. Commitments to high volumes can easily translate into multiyear, multimillion dollar contracts for the customer. Prototyping and small volume production of custom circuits have been discouraged and/or are unavailable due to these volume requirements. As a consequence, many innovative product ideas have remained untried.

Slow growth of custom circuit implementations can also be attributed to the lack of industry wide conventions for standards in design, layout, and processing. Semiconductor vendors typically develop a set of rules regarding the layout and fabrication of ICs for each of their processes. This has minimized compatibility among the various vendors and made second sourcing of custom ICs a sticky issue.

Revolutionary events in the last four years are providing solutions to problems that previously afflicted the custom IC market. The Mead-Conway design methodology, emergence of the silicon foundry and silicon broker, and the availability of a technique for low cost prototyping of custom VLSI circuits are key contributors to these solutions.

Mead-Conway approach

The Mead-Conway design methodology evolved out of work done in the late 1970s by Carver Mead at the California Institute of Technology, and Lynn Conway at Xerox's Palo Alto Research Center. Development of the methodology was geared towards providing a workable solution to the design complexity problem and making custom IC design accessible to a wider spectrum of users, including logic designers, systems designers, and computer scientists.

Acceptance of the new methodology has been widespread. In 1977, one university in the United States taught such a VLSI course. By 1981, 60 universities were teaching the course. Rapid growth in the number of courses being taught will result in a rapidly growing number of potential VLSI designers. In 1978 there were an estimated 2000 IC designers in the United States. In 1981 alone, an estimated 1800 students participated in university Mead-Conway VLSI design courses. Thus, in one year, the number of students participating in at least one experience in IC design outnumbered the total United States IC design workforce of 1978. This trend will need to continue in order to support the growing demand for custom ICs.

The Mead-Conway methodology simplifies the design task by using a structural approach to the design problem analogous to the structured programming techniques now widely used in software development. (See Panel, "Elements of Mead-Conway Approach.") The custom circuit is created via a top-down design, bottomup implementation approach. The first step is to define the function of the complete system and partition it into the major functional blocks that will accomplish the desired task. The next step is to arrange a floor plan of the overall system composed of the functional blocks. placed to maximize signal flow. Efficiency is attained between the blocks by minimizing delays and area lost due to long interconnects. Once this top-down design has been completed, the bottom-up design begins for the implementation of each functional block.

Implementing the blocks with as few cell types as possible, and making use of highly regular structures wherever possible, is called for by Mead-Conway methodology. Simple circuit primitives, such as switching transistor logic (pass transistors) and programmable logic array cells, are used for these higher level functional structures. Stick diagrams that map directly into the final layout topology are normally used to define the layout and interconnect needs for each functional structure. The goal is to minimize the number of devices that must be individually designed; it is much easier for a computer aided design tool to replicate a small number of cells into a large design than it is for a designer to individually lay out all of the devices in an equivalent sized design. Use of simple circuit primitives and attention to the interplay between chip architecture and interconnect are key elements during the design cycle. Regularity is one measure of the success of these efforts.

Regularity is a term increasingly applied to VLSI designs; regularity of a particular circuit is defined as the ratio of the total number of devices to the number of individually drawn devices. In the past, extensive use of random logic resulted in low regularity. Intel's 8080, for

Elements of the N	lead-Conway Approach
Floor plans	
Use of regular structur	es
Wiring by cell abutmer	nt.
Scalable design rules ()	N
Simplified timing mode	ls (τ)
Simple circuit primitive	S
Architecture and interc design cycle	connect emphasis in the

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example, has a ratio of approximately 1:1. With the Mead-Conway methodology, ratios of 50:1 and even higher are now being achieved.

A scalable set of design rules is used to implement layouts. One variable, lambda, specifies all of the design rules-the design can be scaled up or down simply by changing the value of lambda. Lambda based design rules, more forgiving than the specific design rules published by the various processing houses, may be applied to a wide variety of similar processes and are less sensitive to violations. One minor drawback since the rules are looser, is a small area penalty (10% to 15%). However, this is not usually objectionable during prototyping and only affects high volume production where cost is tightly tied to die area. The value of lambda at any given time represents the resolution of the process being used. The most widely used process to date has been the N-channel metal oxide semiconductor (NMOS) process, with lambda values of 2.5 and 2.0 μm the most common feature sizes.

The Mead-Conway approach simplifies the design task by using a structured approach to the design problem...a custom circuit is created by a top-down design.

A simplified timing model that expresses delays in terms of tau, where tau is determined by the product of the channel resistance per square and gate capacitance per square, is used in the methodology. Timing effects due to different size transistors and different loads can be expressed in terms of the one variable, tau, and relatively accurate predictions of circuit performance can be quickly made.

The Mead-Conway methodology is changing the philosophy of IC implementation. A primary goal of the methodology is to take the mysticism out of custom design and make it accessible to the logic designer, system designer, and computer scientist. This implies the need for a separation between the design and processing functions that did not exist previously. In the past, custom circuit designers were well versed in both device performance and processing. The new philosophy maintains that the designer should concentrate on the design and be concerned only with the most basic aspects of processing such as the lambda based design rules and basic process parameters (eg, nominal threshold voltages and sheet resistances).

Foundries, brokers, and multiproject prototyping

In response to the new methodology and philosophies promoted by the Mead-Conway approach and the demand for product innovation through the increased use of custom VLSI, several new services have emerged. The silicon foundry, the silicon broker, and the existence of a multiproject wafer prototyping service all offer valuable assistance and services to the VLSI designer that were not previously available.

As the name implies, the silicon foundry is a semiconductor fabrication vendor who will accept and process independent designs. The ideal foundry offers fast turnaround processing with little or no production volume requirement. Foundry processing should be as transparent as possible, with only major items such as design rules and target process parameters supplied to the designer. Standardization of both processing and interface details is key to the success of the foundry concept. At present, most of the foundries are in the customer-owned tooling business. There is little standardization of design rules and no easy access for prototyping and low volume production.

An independent party, the silicon broker interfaces between the VLSI designer and the vendors needed to take a custom design through to a working chip. The broker handles all details involving the mask making shop, silicon foundry, and packaging shop, relieving the designer of that time-consuming task. The broker is in an excellent position to evaluate, qualify, and recommend vendors, as well as establish standards that facilitate compatibility between the processes and services available.

Other services the broker offers support the potential custom VLSI user. The broker offers training in Mead-Conway VLSI design, provides design and production services for implementing custom VLSI designs, and may even distribute computer aided design tools for use in the design and layout of custom VLSI circuits.

An extremely important service that SynMos provides is the multiproject wafer prototyping service, which allows low cost prototyping of VLSI designs and is based in principle on the multiproject chip (MPC) concept that was born in the university community about five years ago. The MPC approach was developed so universities could afford to fabricate student projects designed in the Mead-Conway VLSI courses. In the MPC concept, a number (one to ten, typically) of individual VLSI designs are merged into larger, uniformly sized chips that are then arranged on a common mask set and submitted for wafer fabrication. The obvious benefit of this approach is that the relatively fixed costs of generating masks and wafers can be spread over a number of participants, making the cost per design quite low if the number of



Fig 2 Multiproject wafer approach preserves proprietary nature of each circuit.

participants is large. A drawback to the MPC approach is that there is usually more than one design placed on a chip. Thus, the recipient of a prototype circuit receives a die with several designs on it besides his own. This has not been a problem in the university community, but would be unworkable in the highly competitive commercial electronics industry.

The multiproject wafer (MPW) approach capitalizes on the cost sharing benefits of the MPC but preserves the proprietary nature of individual circuits. As the name suggests, each circuit on an MPW is delimited by its own scribe lines rather than occupying a larger chip with several larger designs. The result is, typically, an asymmetrical wafer layout with variable pitch scribe lines which, when the wafer is sawed, will yield totally separate parts (Fig 2). The MPW provides a low cost, fast turnaround vehicle for prototyping and small volume production of custom VLSI designs without commitments to high volume production.

Summary

Acceptance of the Mead-Conway design methodology and emergence of the silicon foundry, silicon broker, and MPW prototyping service are providing custom VLSI designers with tremendous leverage. Mead-Conway is dramatically increasing the number of potential custom circuit designers, and is extending the range of disciplines in which custom designs will be available. Additionally, the hierarchical aspect of the methodology provides a viable means for handling VLSI circuit design.

The silicon foundry and silicon broker are beginning to develop and provide standards for designer interface and processing that will facilitate wider use of custom circuits. MPW prototyping is especially valuable in that it provides for small volume production of custom VLSI designs.

Viability of the methodology has already been demonstrated in such products as the Motorola 68000 and the Intel iAPX-432. Silicon foundries and silicon brokers, and the related services they offer to the VLSI designer, will serve to greatly increase the number of systems implemented in silicon in the next few years.

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SPECIAL REPORT ON FUTURE DIRECTION IN SYSTEMS DESIGN

DEVELOPMENT SYSTEMS

CUSTOM ICS FROM STANDARD CELLS: A DESIGN APPROACH

The shortage of skilled designers of custom ICs is being eased by design automation tools that allow the development of MOS/LSI chips from standard design cell libraries

by William Loesch

ystem designers have come to realize that the microprocessor fulfills only a fraction of overall U system requirements. Additional "glue" logic, special input/output, and high performance hardwired circuitry are all necessary to complete a complex system. The proliferation of microprocessor designs and architectures confirms that as complexity increases, system designers require more specialized integrated circuits. Advances in technology are altering both the way semiconductor firms design and manufacture integrated circuits, and their relationship with end users. Apparently, semiconductor manufacturers are destined to become service companies as well as manufacturing operations. However, the greatest obstacle to this development is the tremendous strain it will place on available integrated circuit design resources.

It is estimated that there are fewer than 3000 integrated circuit (IC) designers working today, and that the IC industry is critically short of skilled designers. As a result of this shortage, the industry has attempted to create new approaches to increase productivity.

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increasing engineering productivity. Unfortunately, these CAD tools have fallen short of their original promise.

Design automation-the next step

To meet the increasing demand for IC design resources, a way must be found to increase the number of design engineers available to develop complex ICs. An integrated CAD approach, which can be described as design automation, is the best way to accomplish this. The goal of design automation is to provide a sophisticated design tool that will allow engineers to develop complex ICs with a minimal amount of training. True automation will allow design in terms of functions rather than physical devices. The computer translates combinations of functions into the physical layout, generates test parameters, and, ultimately, produces the physical masks.

Key to developing a design automation tool is a comprehensive applications library of standard building blocks or cells. Standard cells provide a link between the expertise of both the IC designer and the system designer. The IC designer has the knowledge of silicon device physics, topological logic, and semiconductor



Fig 1 Five development steps of an integrated circuit

processing to create and characterize in detail each standard cell. The system designer uses his expertise in logic design and system architecture to interconnect the standard cells to perform the desired function. Standard cell libraries. together with a sophisticated design automation software tool, allow a synergy between IC designers and system designers that has been previously unattainable.

A system that uses a library of standard cells, carefully designed and laid out by IC engineers, can provide a very high

level of design automation. The ZyP* system by ZyMOS Corporation uses standard cells in a manner analogous to a mathematical transform that maps parameters from one coordinate system to another: a description of logical functions is transformed into photolithographic masks. Available to subscribing designers, ZyP is a combination

of existing CAD tools, original ZyMOS software, and applications libraries linked together to form a custom circuit design tool. The system can either be accessed through an international timesharing communications network or installed on a computer at the customer's facility.

For every IC, there are five distinct development steps. Although these steps can vary in specific definition, they must be completed regardless of the method used in developing the circuit (see Fig 1). The first step in developing any custom circuit is the logic/circuit design. Designing a custom circuit with a standard cell design automation system begins with a definition of the system logic. The designer first selects standard cells from the applications library based on information contained in the data sheets for each cell (Fig 2). Once the choices have been made, the designer enters an alphanumeric listing that specifies the desired interconnections of the standard cells.

In the second step, the designer must verify that the interconnection of standard cells he has selected meets the required circuit timing and logic specifications. The ZyP design system utilizes an eventdriven logic simulator, ZyPSIM, to give the system designer the capability to model the silicon level performance of any standard cell interconnection.

The simulator uses detailed circuit timing models for each standard cell to accurately predict silicon level performance. Net delay of each cell is modeled by ZyPSIM as the sum of an intrinsic delay component and a loaddependent delay component. Delay components for each standard cell are derived from the results of detailed circuit simulations. Independent of the interconnection of the cell in the overall network, the intrinsic delay component depends on the cell design, as well as the cell's operating temperature and voltage. The load-dependent delay component is determined by the capacitive loading of the cell, in addition to cell design, temperature, and voltage. Cell delays are nominally modeled under conditions of worst-case processing parameters, 5-V power and 27 °C ambient temperature. Derating curves have been developed to translate predicted performance under nominal operating conditions to operation with different power supply voltages and/or different ambient temperatures.

Initial timing will not be exact. Since it is unknown at this time, the capacitive load due to cell interconnect is not included. However, the artwork generation software will create additional capacitive load information in ZyPSIM format that can be fed back into the logic simulator once the routing has been completed for a

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Fig 2 Typical data sheet of standard design cell. Cells are selected from library on basis of design requirements.

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Fig 3 Cell network listing. If logic tests correct, network listing is incorporated into artwork generation module.

final checkout. Unlike most full timing simulators, these simulations are relatively inexpensive—simulating a typical 2000-gate equivalent circuit (8000 transistors) for 1 ms takes less than five minutes of computer time on a minicomputer of the Prime 750 class. This means that dozens of iterations can be made per day in the verification stage.

Since the development of metal oxide semiconductor (MOS) circuits, gates of different sizes can be wired-OR together. Each gate will have a different strength electrically. ZyPSIM models gates of different strengths, resulting in the strongest gate dominating in a wired-OR situation, overriding all others. In the ZyPSIM hierarchy, clocks, power, and ground are the strongest, followed by normal gates (strong), by weak gates (eg, resistors), then by gates in the high impedence state.

Spike conditions that occur whenever the input to a gate changes faster than the propagation delay through the gate are also modeled. For example, if an inverter has a 10-ns delay and its input changes state every 5 ns, a spike condition will be flagged.

In order to check for common error conditions in driving flipflops, ZyPSIM will automatically check for the minimum setup and hold times. The clock, set, and reset signals will also be checked to ensure that they do not violate the minimum signal width requirements. If an error occurs, an appropriate error message will appear in the output file, indicating the gate and signal in error.

In the third step, the cell network listing (Fig 3) is input to the artwork generation software module after functional and performance requirements have been verified. The module then produces an initial cell placement and routing diagram (Fig 4). If changes in the cell placement are required at this point, they can be relocated (eg, to fix pinout). When placement and routing are approved, the artwork generation software prepares a graphics database tape. Changes can be accommodated throughout this completely automated cycle. The entire process, from completion of simulation to composite artwork, can take less than two days (Fig 5).

The test program generation software module, in the fourth step, processes the output from the logic simulator to generate a functional test pattern compatible with the Fairchild Sentry VII tester. A node toggle analysis can be performed to ensure that the circuit is completely tested. By the time the prototype circuits have been fabricated, the test program is complete.

The final step is production. When the design is satisfactorily completed, photomasks are fabricated from the graphics database tape and a prototype run of wafers is produced. Following wafer processing, the prototypes are tested and several are delivered to the customer. Upon customer approval, the device can go into volume production.

Extensive library of standard functions

Key to a standard cell design system is the cell library. The ZyP system can access three libraries: one with cells designed in silicon gate N-channel MOS (NMOS), one with cells in silicon gate complementary MOS (CMOS), and one with cells in metal gate CMOS. Each library currently has over 150 elements, with others continually being added. The cells differ from those used in gate array designs in that each is hand designed and laid out in allmask layers for its specific function.

Library elements range in complexity from primitive transistors, transmission gates, logic gates, latches, and flipflops, to functions such as counters, shift registers, digital comparators, adders, and multiplexers. Even very complex elements such as random access memories (RAMs), read only memories (ROMs), programmable logic arrays (PLAs), and microprocessors are included. In addition, several analog building blocks have been incorporated into the libraries, including op amps, comparators, and voltage references.

Success of a standard cell design approach depends upon the availability of a large, technologically

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Fig 4 Initial placement and routing diagram. Diagram is generated from artwork software module.

advanced library of standard functions (Fig 6). Such a large library gives the system designer the flexibility to meet all of the system integration objectives. In fact, a large library of standard cells offers vastly greater flexibility than is possible with any gate array design.

Extensive characterization of each standard cell is undertaken before a cell is entered into the library. Initially, the desired logic function is converted into a transistor schematic; a preliminary circuit simulation is performed to get a rough estimate of the final cell performance. A topological layout is then created and a detailed circuit network, including parasitic components, is extracted from the topological design. This comprehensive circuit network is simulated over a wide range of process parameters to determine worst-case conditions. The worst-case circuit simulation model is entered into the library data base together with the final digitized artwork.

Output of the detailed circuit simulation is processed by a ZyMOS developed logic simulation model extraction program. This computer program essentially "linearizes" the circuit simulation data to provide a simple but highly accurate timing model for the logic simulator. Delay of each cell is modeled as the sum of a load-dependent delay and load-independent or intrinsic delay. Value of the delays is extracted from the circuit simulation output and entered into the logic simulation model data base. Finally, a data sheet for each cell is prepared that includes a logic diagram, information about how to call the cell model, and logic simulation timing data.

With a standard cell approach, the systems company is guaranteed at least one production source for the custom circuit it designs. Also, the systems company need not invest in expensive graphic design aids and wafer test equipment to design and build ICs. Most important, semiconductor vendors are in the best position to update libraries with the latest process technologies.

Reduced development costs

Design cost of a custom IC can be divided into development and production costs. Direct development costs for custom circuits using a standard cell design system are considerably less than for conventional full-custom design, and only slightly more than for gate array design.

But the indirect cost of development time—the greatest expense and risk in custom circuit development —is much lower using standard cells than using any other approach. Since the system designer controls the schedule, he is not at the mercy of a semiconductor vendor's changing priorities. Because the circuit is built up from well-characterized cells routed together by the computer exactly as specified, the risk of design iteration is low. When the

system algorithmically generates a test program from the logic simulation output, the risk of delays in production startup are also low.



Fig 5 Composite artwork resulting from graphics data base



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Design system tradeoffs

When selecting a design approach that will yield the minimum overall cost, two factors are important. First, of course, is expected production volume. However, second, circuit complexity is critical in determining the lowest cost design method. Measured in thousands of transistors per chip, circuit complexity affects the development cost, the ratio of package cost to silicon die cost, and the density or silicon area per transistor.

A hand drawn full-custom circuit offers the maximum density, or equivalently, the minimum area per transistor for a given set of design rules. Depending upon the specific network, standard cell layout typically requires from 10% to 20% more area per transistor than a hand drawn, full-custom design. A gate array usually requires from 50% to 100% more area per transistor than a full-custom design.

The economic tradeoffs between full-custom gate array, and devices designed with standard cells can best be summarized in the graph in Fig 7, which illustrates two points. First, as circuit complexity increases, standard cell designs become more cost-effective than gate array designs because of greater silicon area efficiency and, therefore, lower production costs. Second, as circuit



Fig 7 Complexity/production volume relationship of three IC design methods. As chip complexity increases, designing with standard cells becomes cost-effective for moderate size production runs.

complexity increases, standard cell designs become more economical than conventional full-custom design. The cost of design for a full-custom circuit increases exponentially, whereas the cost with the standard cell system goes up linearly.

Conclusion

The standard cell design approach is just the beginning of the technology evolution cycle. While the concept of standard cells dates back to the mid-1960s, the software to address their application is still in its infancy. Future enhancements and evolution will address the user interface and growing chip complexity.

In the future, the user can look forward to standalone turnkey design systems. Circuit description will evolve from a rigid syntax logic file to a functional description with schematic entry and automatic cell selection. PLAS, RAMS, ROMS, registers, and similar functions will be input in a hierarchical format. Cells will continue to evolve from primitive logic functions to complex subsystems such as core microprocessors, digital phase locked loops, and analog to digital converters.

Circuit analysis will undergo major enhancement. Processing of circuit simulation output data will allow improved data presentation (ie, timing diagrams) and removal of redundant information. Automatic test vector generation from general test strategies will be implemented.

Eventually, software will evolve to routinely accommodate cells of arbitrary aspect ratios and routing constraints. Newer processes will remove routing constraints and reduce area penalties. Direct hardware/ software links to E-beam mask fabrication systems will improve development turnaround times. Standard cells, coupled with tools that guarantee virtually error-free design, will permit complex custom ICs to become elements of nearly every electronic system.

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SPECIAL REPORT ON FUTURE DIRECTION IN SYSTEMS DESIGN

INTEGRATED CIRCUITS

CMOS LOGIC ARRAYS: A DESIGN DIRECTION

Logic dictates the benefits of converting conventional SSI/MSI design to modern HCMOS arrays; speed, power, efficiency, and compactness result

by Rob Walker, Richard Derickson, and Keith Lobo

ogic arrays provide significant speed, density, power savings, and cost advantages over conventional small scale integration/medium scale integration. The new generation of complementary metal oxide semiconductor arrays provide transistor-transistor logic speeds at lower power and cost than other logic array technologies. Using equivalent gate tables, logic complexity can be measured, and array data sheet information provides input/output pin requirements and operating speed parameters. Once feasibility of a particular array is known, the designer is in a position to begin conversion of the logic design into a gate array using modern design automation tools.

A number of important benefits are derived from conversion of a conventional small scale integration/

Rob Walker is vice president of engineering at LSI Logic Corp, 1601 McCarthy Blvd, Milpitas, CA 95035, where he is responsible for design of CMOS and ECL arrays, as well as computer aided design. Mr Walker holds an MSEE from San Jose State University and a BSEE from the University of California at Berkeley.

Richard Derickson is an LSI Logic Corp application design engineer. His former projects include the design of a digital audio tape recorder for Ampex Corp, as well as video games and music synthesizer for Atari. Mr Derickson holds a BS in naval science from the U.S. Naval Academy. medium scale integration (SSI/MSI) design to a logic array. Complementary metal oxide semiconductor (CMOS) arrays, once relegated to low speed, low complexity applications, can replace hundreds of low power Schottky transistortransistor logic (TTL) packages.

Modern CMOS arrays have a number of advantages. High performance CMOS arrays cut onchip delays down to 2 ns substantially better performance than is available with standard TTL and CMOS families. All logic arrays exhibit superior speed/power



performance over SSI/MSI designs because of lower interconnection capacitance and high inherent noise immunity. Larger high performance CMOS arrays can replace a board of standard logic, and materially reduce the size and complexity of the final product. This results in fewer components, simplified maintenance, and reduced spares and inventory. Replacement of tens to hundreds of SSI/MSI integrated circuits (ICs) and their

Keith Lobo is manager of strategic marketing at LSI Logic Corp. Before joining the company, he held marketing and engineering positions at Advanced Micro Devices and Fairchild Camera & Instrument Corp. Mr Lobo holds an MEE from Stevens Institute of Technology and an MBA from the University of Wisconsin. attendant printed circuit board interconnection, solder joints, power supplies, and decoupling capacitors substantially increases system reliability. These advantages add up to lower system cost when production requirements are sufficient to amortize design changes.

Estimating equivalent gate complexity

One of the first tasks in converting a logic function into an array is to estimate logic complexity. While no industry wide standard exists, logic complexity is usually measured in terms of equivalent gates. Elements, typically 2-input gates in CMOS arrays, may be configured into more complex gates, flipflops, complex counters, shift registers, and multiplexers. Table 1 lists the approximate equivalent CMOS gate count for logic





elements. Most offerings from other CMOS manufacturers will be similar.

A simpler technique converts 7400 TTL parts directly to equivalent gates. Table 2 lists the approximate logic complexity of most 7400 packages. Unused portions of these functions may be deleted with commensurate gate savings; offchip buffers are not included. Table 3 lists the same information for the 4000B series CMOS logic ICs.

The toughest part of estimating array applicability...is ensuring that circuit speed is sufficient.

Converting PLA/FPLA designs to gate arrays

When discussing the conversion of various logic devices to gate arrays, it is wise to clarify the use of the rather similar acronyms encountered. For simplicity sake both programmable array logic (PAL^R) devices and field programmable logic arrays (FPLAS) will be referred to as PLAS from this point on. Field programmable logic achieves higher levels of integration than is possible with standard 7400 series SSI/MSI functions. The PLA was originally intended to solve high fan in decode problems. However, PLA and FPLA have been used extensively for discrete logic compaction. A PLA block diagram is shown in Fig 1. Typically, 5 to 12 standard SSI/MSI functions can be implemented on a single programmable logic circuit.

PLA functions can be implemented in portions of a gate array with corresponding cost savings. Conversion should take into account several factors. If the original PLA program was generated from Boolean expressions, they can also be used to implement a gate solution. For higher speeds, the designer may wish to implement in

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Part No.	Gate Equiv	Part No	Gate Equiv	Part No	Gate Equiv	Part No	Gate Equiv
7400	4	7470	16	74152	24	74253	40
7401	4	7471	15	74153	27	74257	36
7402	4	7472	14	74154	33	74258	34
7403	4	7473	20	74155	21	74259	48
7404	4	7474	15	74156	21	74260	6
7405	3	7475	14	74157	22	74261	58
7406	3	7476	20	74158	23	74265	7
7407	6	7477	14	74159	18	74266	10
7408	6	7478	20	74160	68	74273	24
7409	6	7480	17	74161	68	74274	70
7410	6	7481	80	74162	68	74275	70
7411	7.5	7482	27	74163	68	74276	40
7412	6	7483	57	74164	43	74278	34
7413	14	7484	80	74165	85	74279	10
7414	30	7485	73	74166	62	74280	24
7415	7.5	7486	12	74167	52	74281	170
7416	3	7487	19	74168	80	74283	59
7417	6	7489	320	74169	80	74284	58
7420	6	7490	40	74170	116	74285	58
7421	5	7491	43	74172	205	74200	280
7422	4	7492	41	74172	56	74200	18
7422	6	7492	41	74170	37	74290	40
7425	6	7493	42	74174	25	74295	57
7426	4	7404	42	74175	23	74233	22
7420	6	7495	42	74170	42	74290	100
7429	4	7490	120	74177	56	74299	100
7420	6	7400	22	74170	50	74323	64
7430	1	7490	35	74179	20	74340	124
7432	4	7433	19	74180	100	74351	26
7433	4	74100	10	74101	100	74352	20
7437	4	74102	14	74102	30	74353	39
7430	4	74103	20	74103	100	74302	44
7440	20	74100	20	74104	100	74303	20
7443	29	74108	20	74100	80	74304	40
7440	29	74100	21	74190	76	74305	40
7445	20	74110	14	74102	62	74300	27
7446	45	74110	20	74192	58	74307	40
7440	45	74116	20	74193	70	74300	28
7448	45	74120	15	74194	16	74373	20
7440	45	74120	24	74195	40	74374	16
7450	40	74135	12	74190	42	74375	10
7451	5	74130	22	74109	41	74370	40
7451	0	74130	23	74190	92	74377	40
7452	0	74139	20	74199	05	74370	34
7455	7	74141	10	74225	450	74379	24
7454	6	74142	90	74220	110	74381	150
7400	0	74143	45	74245	83	74386	12
7400	C C	74144	98	74240	51	74390	86
7401	0	74145	24	14241	51	74393	80
7462	9	/414/	35	74248	51	74395	50
7464	8	/4148	35	/4249	51	74398	22
/465	8	/4150	60	/4251	37	74399	22
		/4151	24			74670	144

the prime implicant form and optimize propagation delays. Theoretically, a PLA requires only the necessary product terms to be programmed to make the outputs of the Boolean equations valid. However, in many applications, designers may minimize the Boolean equations only to the point where they fit in a PLA of a given size. Further, when converting such designs to gate arrays it is helpful to minimize a set of min-terms to a set of prime implicant factors. This reduces the size of the AND/NOR elements in the Boolean equations which, in turn, results in a higher speed implementation due to reduced gate count, fan in, and capacitance.

In many PLA designs all eight or ten outputs are used, simply because they are available. Some outputs may be implemented more economically by minimizing or further encoding. Most PLA designs use only about 50% of available product terms because of input/output (I/O) pin count limitations. Average PLA design complexity is about 200 gates, though many designs use less. Details of the logic used in a specific application are required for a final equivalent gate count. In Fig 2, the theoretical gate count of this block of logic can be as high as 38 equivalent gates. Actual logic can be implemented in as little as 26 equivalent gates with 3-state feature. Without 3-state outputs, gate count is reduced to 18—less than 50% of the total block of logic. Table 4 summarizes logic complexity of popular PLAs.

Wireability

In a logic array it is neither possible nor desirable to use every gate. Limitations of interconnections, I/O pins, and required function mean that the array will use from

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4000 B Series Equivalent Gate Counts for CMOS Logic Arrays

Part No	Gate Equiv								
4000	5	4030	12	4098	84	4375	14	4554	40
4001	4	4032	68	4093	32	4386	12	4555	22
4002	4	4034	110	4094	86	4501	6	4556	22
4006	108	4035	48	4099	64	4504	33	4558	65
4007	2	4038	74	4106	30	4505	271	4560	78
4008	32	4040	74	4107	18	4506	19	4580	187
4009	5	4041	4	4138	20	4508	24	4581	100
4010	5	4042	12	4139	10	4510	94	4582	31
4011	4	4043	20	4153	32	4511	136	4583	23
4012	4	4044	20	4155	22	4512	31	4584	30
4013	10	4051	6	4157	24	4514	69	4585	35
4014	43	4068	4	4158	24	4515	69	4597	103
4015	62	4069	3	4160	64	4516	66	4598	74
4017	45	4070	12	4162	54	4518	26	4599	42
4018	52	4071	6	4163	64	4519	28		12
4019	12	4072	4	4164	51	4520	44		
4020	40	4073	8	4166	84	4521	123		
4021	43	4074	14	4174	38	4522	44		
4022	35	4075	8	4175	25	4526	47		
4024	44	4076	41	4192	60	4530	16		
4026	65	4077	12	4193	56	4531	36		
4027	20	4078	4	4273	50	4532	39		
4028	22	4031	4	4373	58	4534	190		
4029	68	4082	4	4374	74	4539	24		

60% to 95% of available cells. Typically, arrays of under 1000 gates are capable of up to 90% utilization and beyond, while the utilization may drop to 65% at 5000 gates because of greater wiring congestion.

It is also advisable to hold gates and wiring channels in reserve for changes. A small change on an array that is 95% utilized may not be possible, and could necessitate a total redesign on a larger array. Provision should be made for changes, particularly in control logic, by using the next larger size array than that required.

Package selection and pin count reduction

The number of I/O pins required has an important bearing on the feasibility of an array design. First, there is a maximum number of I/O pads specified for each array. Second, packaging cost is a strong function of pin count. Package selection must be a tradeoff between system cost savings and increased array cost. A 40-pin package will be significantly lower in cost than an 80- or 100-pin package, but system considerations requiring more parallelism, fewer buried states, and more I/O may dictate packages with a higher pin count. The data sheet of an individual array family should be referenced to determine maximum potential pins.

A number of techniques may be used to reduce I/O pin count. Partitioning a system by bits rather than by function, called bit slicing, will usually reduce both pin count and the number of unique part types (see Fig 3). Additionally, where time constraints permit, data can be transmitted serially rather than in parallel. Test modes can be initialized by forcing array inputs to combinations and/or sequences that do not occur in the normal operating modes. For example, assume two control inputs, read and write. Clearly, the simultaneous activation of both inputs is illegal under normal operating

			TABLE 4				
PLA to Gate Equivalent Conversion							
Part Type	Array Inputs	Outputs	Product Terms	Output Registers/ 3-State Buffers	Best-Case Gate Equiv	Typical Gate Equiv*	
PAL 16L8	16	8	58	8	368	184	
PAL 16R4	16	8	60	4	400	200	
PAL 16R6	16	8	62	6	410	205	
PAL 16R8	16	8	64	8	424	212	
PAL 20LR	20	8	56	8	376	188	
PAL 20R4	20	8	60	4	400	200	
PAL 20R6	20	8	62	6	410	205	
PAL 20R8	20	8	64	8	424	212	
FPLA 16X48X8	16	8	48	8	380	190	
FPLS 16X48X8	16	8	48	8	540	270	
FPLA 18X32X10	18	10	32	10	318	159	
FPLS 16X32X12	16	12	32	12	456	228	

*Typical gate equivalents are based on I/O pin count limitations of these devices which limit the use of product terms

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Fig 2 Logic block from field programmable logic array. Thirty-eight equivalent gates comprising this block can actually be reduced to less than half that number in gate array implementation.



rig 3 Bit sucing. Partitioning complex function on bit-slice, rather than functional, basis often reduces 1/0 requirements.

conditions. This combination could, therefore, be used to force the array into a test mode without adding more pins. Other techniques include

- Single-rail transfer—Transfer only one polarity of signal between arrays, invert locally on the receiver array
- Local decoding—Use decoding networks on each array when there are many decoded signals required on several arrays
- Local counters—Rather than transferring counter data between several arrays, use local counters in each array and synchronize
- Signal busing—A single line may carry information from a variety of sources and local storage may be used to hold signal values
- External MSI—When a large number of parallel outputs are required, external MSI decoders may be used to save array pins (Fig 4)

Circuit speed

Probably the most difficult part of estimating array applicability to a particular function is ensuring that circuit speed is sufficient. Unfortunately, CMOS gate delays vary widely with technology, configuration, and loading. In addition, on single metal arrays, polysilicon is used for some interconnection segments, thus adding RC delays.

Once the actual array is laid out, circuit speeds are quite accurately known. The challenge is to estimate worst-case speeds and determine feasibility before detail logic design and layout. For instance, oxide isolated silicon gate CMOS arrays with 5- or $6-\mu$ gate lengths, such as LSI Logic Corporation's LC series, California Devices' HC series, or American Microsystems' UA series, exhibit gate delays from 3 ns (inverter, typical) to 32 ns (4-input NOR, average worst-case). In general, an assumption of 20 ns/gate average is a good general guideline. This corresponds to counter/prescaler operation of up to 20 MHz, or system clocks of up to 5 MHz. Oxide isolated, silicon gate double-layer metal high performance CMOS arrays with gate lengths of approximately 3 μ , such as supplied by LSI Logic Corporation and Toshiba, provide performance previously possible using only bipolar technology. Delays range from a best-case 0.8 ns to 10 ns average worst-case. In general,

Logic arrays using $2-\mu$ high performance CMOS will move that technology into the very high speed arena.

an assumption of 5-ns gate delays (Schottky TTL speeds) is appropriate. In typical systems, this corresponds to counter/prescaler speeds of 50 MHz, and system clocks of 15 MHz. Two- μ high performance CMOS is in research and development. Logic arrays using this technology will move into the very high speed arena. Gate delays of 500 ps are observable, while the worst-case delays seldom exceed 5 ns. In general, an average gate delay of 2 or 3 ns, about that of 10k emitter coupled logic, will be a useful guideline. In a prescaler application this will allow counting speeds in the 100-MHz range, while typical system clocks will operate to 30 MHz and beyond.

Computer aided design

Some modern computer aided design systems designed for logic array development accept 7400 inputs directly. The Texas Instruments HDL array design system and the LSI Logic Corporation LDS1 automatically convert from standard 7400 functions to array macro cells.

Imagine a typical small system operating on a 5-MHz clock. The present implementation uses the standard and low power Schottky TTL circuits shown in Table 5. From Table 2, it can be calculated that 482 equivalent



Fig 4 External MSI decoder or shift register may be used to reduce array pin count requirements.

TABLE 5

Existing System	Equiv Gates per IC	Total Equiv Gates
2 (ea) 74LS91	43	86
2 (ea) 74LS100	18	36
4 (ea) 74155	21	84
2 (ea) 74174	37	74
10 (ea) 7402	4	40
2 (ea) 74LS10	6	12
5 (ea) 7430	6	30
1 (ea) 74163	68	68
10 (ea) noninverting output buffers 2X drive	4	40
2 (ea) noninverting 3-state output buffers	6	12
Total Equiv Gates		482

gates will be required to implement the function in an array. Analysis of the system showed that a total of 37 I/O pins (25 inputs, 12 outputs) and two power pins would be required. Therefore, a 40-pin dual-inline package would be the most economical solution. A review of the gate delays required to meet the 5-MHz clock rate showed that 25-ns average worst-case delays would be sufficient. After considering all design requirements, it can be concluded that the 540-gate LC 5400 or the 770-gate LC 7700 CMOS arrays packed in a

40-pin plastic DIP would be the optimal solution. The 540-gate LC 5400 will require 482/540 to equal 89% utilization. Although reasonably practical, this wiring percentage at such a high level of complexity would leave little or no margin for changes. The 770-gate LC 7700 will require 482/770 to equal 63% utilization, an easy layout with plenty of room for logic additions. Notice that the required noninverting and 3-state output buffers, with the required drive capability, have been included to give the final accurate gate count of the logic array implementation.

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SPECIAL REPORT ON FUTURE DIRECTION IN SYSTEMS DESIGN

SOFTWARE

COMPACT CODEiapx 432 addressing techniques

With the ability to address 2⁴⁰ bytes of virtual memory space, it is no wonder that the 432 chip employs some ingenious addressing shorthand

by Stan Mazor and Sandy Wharton

since the introduction of the iAPX 432 in 1981, little has been reported about the processor's instruction set, which was chosen with the compiler writer in mind rather than the assembly language programmer. An introduction to 432 instruction representation and techniques that compact object code will be presented in this article.

Unlike early microcomputers, which were usually programmed in assembly language, the 432 is programmed in a high level language such as Ada, similar to Pascal. Table 1 shows a short procedure in both languages for clearing an array to zeros. Although there are some syntactic differences, most programmers can

Stan Mazor is with Intel Corp, 2625 Walsh Ave, SV3-1, Santa Clara, CA 95051, where he has participated in the design of the MCS-4, MCS-8, 8080, and several other microcomputers. Prior to joining Intel, he was a principal designer of the Symbol computer at Fairchild. Mr Mazor has published over 30 articles and papers on microcomputers and shares patents on the 8080 and MCS-4. He is a senior member of the IEEE.

Sandy Wharton is in charge of curriculum development for high level languages in the Customer Training Dept at Intel Corp. She has a BA in mathematics from Ripon College, Ripon, Wis, and an MS in computer science from the University of Santa Clara, Calif. probably read both. Therefore, it is instructive to compare the object code of the 432 with that of the 8086 for the programs in Table 1.

An 8086 central processing unit (CPU) can address 1M byte (2²⁰ bytes) of memory. The chip uses a minimum amount of storage for frequently used operations such as register increment [instruction (6)] and compare immediate [instruction (7)]. For the program in Table 1, the Pascal-86 compiler generated 20 bytes of code for the eight 8086 instructions. It uses the AX register for data values and the SI register for subscripted references to the array A. The 432 can address 240 bytes of virtual memory, and every user can access 232 bytes of addressing space. Because the 432 has a much larger addressing space than the 8086, as well as more opcodes and richer data types, one might expect its object program to be larger than the corresponding 8086 program. However, coding compaction techniques have kept the object code small. Table 1 shows that the 432 object code is approximately the same size as the 8086 program. The six instructions occupy 20.5 bytes, averaging 3.4 bytes/ instruction. One important difference is that no registers are available to the programmer or compiler on the 432—all references are to either the memory or the stack.

Individual 432 instructions vary in bit length, depending on both the addressing mode used and the number of addresses present in the instruction. Although there are no immediate data mode instructions, there are two opcodes (ZERO, ONE) that set the variable to constants (0, 1). These instructions need just one data operand. Instructions (1) and (3) in Table 1 require 22 bits of program memory. Other constants, such as TEN in instruction (5), are kept in a data segment in memory, which is created by the compiler.

Both the increment and decrement instructions require two operands. Instructions (2) and (4) require 28

TABLE 1								
	Comparative	o Cod	ing Ex	amples				
Pasca	<u>al</u>		Ada					
PROGRAM CLEARS	;		Р	ROCED	URE CLEAR	RS		
TYPE INTEGERS = 0	255;	15	IS J: INTEGER;					
VARA: ARRAY (09) OF INTEGER;A: ARRAY [09] OF INTEGERS;BEGINJ: 0MAXINT;FOR J IN 110 LOOP								
BEGIN A(J - 1) := 0; FOR J:= 1 TO 10 DO END LOOP; A [J - 1] := 0 END CLEARS;								
END.								
	Gener	rated	Code					
	Number of Bytes	dicu	0000		Nu	mber of Bits *		
(1) MOV AX,	,1H 3	(1)		ONE	J	22		
(2) L: MOV J, A	4X 3	(2)	L:	DEC	$J \rightarrow $$	28		
(3) MOV SI,	AX 2	(3)		ZERO	A [\$]	22		
(4) DEC SI	2	(4)		INC	J⇒J	28		
(5) MOV A[S	I],OH 5	(5)		GT	J, TEN, \$	47		
(6) INC AX	1	(6)		BF	\$→L	<u>17</u>		
(7) CMP AX,	OAH 3					20.5 BYTES		
(8) JLE L	2							
	20 BYTES							
*Comments for the 432 cc variable J and push onto s index and pop TOS; (4) inc	ode are the following: (stack (\$); (3) zero contr rement variable J by 1, place Boolean (true (fels	1) Set ents of place re	memor memor esult in .	y variable y element J; (5) com	J to 1; (2) de t A(J - 1) usin pare variable J	crement value of ng TOS (\$) as an to constant value		

bits. The comparison operation (5) requires three operands and, at 47 bits, is the largest in this short program segment. Obviously, the operands within the instructions are not full 32-bit addresses.

Boolean off stack, and branch if false to instruction labeled L

Instruction format

One, two, or three address references are contained in a 432 instruction, for up to 2^{32} bytes of memory variables. While this large addressing space might require each memory reference to occupy 32 address bits in the instruction memory, the designers have found ways of

reducing the number of required bits, especially for duplicate addresses. Consider the instruction

 $A + B \rightarrow A$

If this instruction were coded in a 3-address format, the instruction would contain two 32-bit address references for A. In 432 instructions, a 4-bit code is used to tell the processor to use an address twice, saving 28 bits in this common type of instruction.

This technique, known as the format code, also tells the processor when to use the stack instead of a memory variable for an operand. Table 2 shows the format code used for instructions that need three operands. Similar tables exist for 1and 2-operand instructions; their encoding. In one case, the stack is used for all three operands (1011). This instruction coding technique permits the compiler to generate pure stack machine code, or memory oriented code, as is best suited for a particular high level language statement. In this system, the compiler minimizes the amount of code generated, and executes references to the top of stack (TOS) faster because the TOS is a CPU register. This reduces the number of main memory reference cycles used.

codes require fewer than 4 bits for

Address reference fields

Memory addresses in the 432 are of the base/displacement variety. However, unlike the 8086 where the base register is implied, and the IBM 360 where the base register number is explicitly encoded, the 432 instruction contains a base segment number. A user's segment number is converted to a physical base address via an associative table inside the CPU, as shown in Fig 1. To save instruction bits, there are both short and long forms for the segment number in an instruction. A 6-bit code represents the first 64 segment

numbers, but up to 64k segments can be accessed with a 16-bit code.

The displacement field in the instruction comes in two sizes, depending on whether the accessed variable lies in the first 128 bytes of the segment. Fig 2 illustrates the four choices for addressing a scalar variable in data memory; the C-bit (CNTRL field) indicates whether the field is short or long. Many programs have 25 to 50 scalar variables. A clever compiler can allocate them in the first part of a data segment. Their address displacement can usually be represented in the short 7-bit format.

Т	A	B	L	Ε	2	
---	---	---	---	---	---	--

Format Field Locates Each Operand—The Stack or Which Reference

Opcode	Forma	ıt	Re	f 1	Ref	2	Ref 3	3		
Comment	A	So Ope	ource rand 1	So Ope	urce rand 2	Des Ope	tination erand 3	Ex Refe	plicit prences	Format Encoding
Normal 3 ad	dress	r	ef1	r	ef2	I	ref3		3	0000
		r	ef1	r	ef2	i i	ref2		2	1000
$A + B \rightarrow A$	example	r	ef1	r	ef2	1	ref1		2	0100
		r	ef1	r	ef2	1	stk		2	1100
		r	ef1	S	tk	r	ref2		2	0010
		S	stk	r	ef1	r	ref2		2	1110
	- 1. D 1	r	ef1	S	tk	r	ref1		1	1010
		S	stk	r	ef1	r	ref1		1	0001
	1.1	r	ef1	S	tk	5	stk		1	0110
	New Color	S	stk	r,	ef1	5	stk		1	1001
	1990 - 19	S	stk1	S	tk2	r	ref1		1	0111
a state and	(S	stk2	S	tk1	r	ref1		1	0101
Pure stack		S	stk1	S	tk2	5	stk		0	1011
		S	tk2	S	tk1	5	stk		0	1101
		r,	ef2	r	ef1	r	ref3		3	0011
		r	ef2	re	ef1	s	stk		2	1111
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Fig 1 Address generation on chip cache. In this system user's segment number is converted to physical base address.



Fig 2 Addressing scalar data elements. Both segment address element and displacement element can vary in length, depending on address.

Hence, the minimum reference to a scalar variable uses 13 bits,



which is less than half of the worst-case, 32-bit address



Addressing vectors

High level languages are required to address subscripted vectors, eg, V[I]. The 432 provides an efficient representation for this mode. A vector can be a separate segment (Fig 3) where the index that selects a particular element comes from the TOS. In this case, the minimum size address reference for a vector element is the same size as the short segment reference (ie, 6 bits).

	BA	SE VECTOR SEGM	ENT
OP	CTRL	6 BITS	

Because the TOS is a CPU register, using the TOS as the index is about as fast as having an index register. Furthermore, if the index is the result of a computation (eg, J + 1 or J + K), it is convenient for the compiler to leave the calculated result on the TOS, since the format

code selecting the TOS for the result uses few bits. As the segment table in the CPU (Fig 3) also contains the length of the segment, the hardware can automatically validate the index value. An exception does occur, though, if the user tries to address outside the valid range of the vector.

The subscript of the array is fetched from memory when it is a variable that is not on the stack. This may require accessing two different data segments as shown in Fig 4. Usually, the subscript I will be in an index data segment as a scalar variable; a segment number and displacement are needed to locate the index I. The processor fetches the data value for I, using it as an index displacement to locate the vector element in the base segment V. Although this mode requires more bits, the instruction is smaller than that of conventional 32-bit machines that require separate instructions for fetching both the index value and the vector element.

	-	BASE VECTOR SEG	BASE INDEX SEG	INDEX DISPLACEMENT	
OP	CTRL	6	6	5 7	
MIN	IMUM VECT	OR REFERENCE	,	/	

In Table 1, the length of the program exemplifies the storage compaction benefits that result from eliminating redundant addresses and using shorter addressing forms in the iAPX 432. The longest instruction (GT) requires



Fig 3 Addressing subscripted vectors



Fig 4 Addressing vector element V[I], I in different segment
three operands. Two of the operands are addressed with short addresses; the third is on the stack as encoded by the format code. Only 47 bits are required in this case. It is obvious that individual instructions vary in size and that they are neither byte nor digit aligned. Although the shortest instruction is 17 bits in length, the longest instruction could contain three subscripted variables and could occupy more than 300 bits.

The iAPX 432 contains many protection features to improve the program's safety during runtime. Implementation of the protection features depends on capability tables and other information descriptors that increase the amount of main memory used. For the majority of coding situations encountered, the code compaction techniques discussed here help to compensate for some of the safety overhead, making the typical instruction much shorter, and the life of a programmer slightly longer.

In 432 instructions a 4-bit code tells the processor to use an address twice, saving 28 bits in this common type of instruction.

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OPERATING SYSTEM SUPPORT--THE Z8000 WAY

All processor architectures are not created equal when it comes to providing designers with the tools they need for effective system resource management

by Richard Mateosian

D perating systems are responsible for allocation, deallocation, and protection of processing and storage elements, external interfaces, programs, and program status. They manage communication and sharing, and define, facilitate, and enforce protocols, conventions, and policy. Several kinds of architectural support facilitate the operating system's task in a wide range of applications: restriction of central processing unit and memory use, memory mapping, sharing of programs and data, program relocation, stacks, context switching, input/output system and interrupts, distributed control, and support for conventions.

Operating system support is an important feature of Z8000* architecture. Special consideration was given to that function during design of the Z8000 central processing unit (CPU), the Z-BUS* component interconnect, and their support chips. In this discussion, "operating system" will comprise the portion of the computer application—both hardware and software—that is devoted to managing hardware and software resources.

Richard Mateosian, Z8000 specialist at Zilog, Inc, 1315 Dell Ave, Campbell, CA 95008, is the author of Programming the Z8000 (Sybex 1980) and Inside BASIC Games (Sybex 1981). Formerly employed in the development of minicomputer based turnkey systems, he has a BS in mathematics from Rensselaer Polytechnic Institute and a PhD from the University of California at Berkeley.



Fig 1 Hardware block diagram of arcade game system. Essential elements include CPU, memory, input and display devices, and clock circuits.

To show how the Z8000 provides operating system support, an application of the hardware and software similar to that used in a popular arcade game will be described. Fig 1 shows the game's hardware configuration; the system elements are pieces of hardware including CPU, memory, realtime clock, input and display units, and integrated circuits for interface to the CPU. Arrows represent electrical connections through which data and control signals are passed among the elements. Configuration of the hardware elements alone, however, provides little insight into the game's operation.

In the game's software architecture (Fig 2), system elements are pieces of software "in action" on the data defining the state of play at any time. Connecting

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Fig 2 Software block diagram of arcade game application. Essential elements are processes, or tasks, that provide for graphics generation, horizontal and vertical synchronization, and realtime scorekeeping.

arrows represent the paths and directions of interprocess communications (messages). The software configuration gives a good idea of how the game works. Fig 3 lists system elements supporting the hardware and software function outlined in Fig 1 and Fig 2. These software components allow manipulation of hardware and applications software, and represent system services that all operating systems must supply.



Fig 3 Underlying operating system elements required by arcade game application. All elements support software functions. Hardware support is provided by interrupt/trap handler, clock manager, and utility elements.

Restriction of CPU access

The operating system must allocate the CPU to a process while protecting itself and other processes. In other words, the operating system must be able to turn the CPU over to a process that will not perform potentially destructive actions. To this end, the Z8000 incorporates a system/normal (S/N) bit in its flag/ control word (FCW) register, which corresponds to the program status word (PSW) in other machines. (See Fig 4.) The S/N bit determines whether the CPU executes in system or normal mode. In normal mode, the portion of the FCW containing S/N is inaccessible; the only way to enter system mode is through execution of a system call (SC) instruction.

The refresh and program status area pointer (PSAP) control registers and the system mode stack register are all inaccessible from normal mode. The normal mode stack register is accessible from system mode under the alias normal stack pointer (NSP), so that normal mode programs can pass arguments to system mode programs on the normal mode stack. When the S/N bit is

in the normal state, privileged instructions—ie, 1/0, interrupt return, nonmemory synchronization, control register manipulation, and halt—cannot be executed; operating system tasks are executed in the system mode.

Another protective feature is associated with the S/N bit. There are two copies of the implied stack register, one for interrupt and one for subroutine returns. One is used when the CPU is executing in system mode, the other when it is in normal mode. Programs executing in normal mode have no access to the system mode stack register.

Passing between system and normal modes requires a change to the FCW, which is accomplished through a privileged instruction or automatically in response to an interrupt or trap. Privileged instructions are load from control register (LDCTL), interrupt return (IRET), and load program status (LDPS). A system call trap, which is a 1-word instruction with eight programmable bits, allows a normal mode program to call one of 256 system mode programs.

The arcade game illustrates how system and normal modes can be used. All of the application software processes seen in Fig 2 can run in normal mode, while the operating system elements in Fig 3 can run in system mode. Calls to the operating system elements from the applications software processes are made using the 256 system calls. For example, the defender guns process can execute the instruction SC #createprocess in order to fire a rocket. The constant, createprocess, is a number from 0 to 255 encoding one of the system functions namely, the one that creates processes. Programs and data that constitute the initial state of the new process can be passed to the process creation program in registers or on a stack.

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Fig 4 Z8000 system/normal operation. s/N bit of flag/control word determines execution mode, system or normal, of CPU.

Memory management

Existence of a user mode and privileged instructions does not solve the entire protection problem; the other half of the solution involves restriction of memory use. Most CPU designs call for a comprehensive memory management facility to unify the approach to restriction of memory use, memory mapping, program relocation, sharing of programs and data, and stack use.

The Z8000 uses an external memory management unit (MMU) that is integrated with a segmented addressing scheme in the CPU. The MMU translates addresses, checks attributes, and interrupts the CPU if an invalid access occurs. Sets of attributes are checked against access rights implicitly or explicitly associated with each process. Then, for example, if a program in user mode attempts to access a memory address whose attributes do not match the program's access rights, the CPU will trap to a system routine designed to deal with such invalid accesses. CPU addressing scheme and the MMU determine which sets of attributes can be associated with portions of the memory address range. Typically, attributes are associated with a segment in a machine that uses 2-dimensional, or segmented, addressing. In a machine with linear addressing, attributes are usually associated with fixed size blocks of addresses called pages.

The arcade game probably does not need memory mapping or virtual memory, since the total memory space of such an application is small. Access restriction, relocation, and sharing of programs and data can be useful in any application, however. On the other hand, UNIX and UNIX-like operating systems, in which there are many small processes, are well suited to the Z8000's segmented addressing and memory management.

Use of stacks

Stacks are important tools for meeting the operating system's responsibilities. A stack is a last in, first out memory associated with two operations: pushing (adding an item) and popping (removing an item). Stacks are explicitly or implicitly used by the operating system to allocate memory in a flexible way, which, in connection with based addressing, allows programs needing nonregister storage to be reentrant and position independent. A special case of this is storage of return addresses for subroutine calls and machine state for interrupt processing. In the arcade game, the use of stacks to allow reentry of programs plays an important role. Rocket processes, for example, can all share a common processing routine while each uses a different set of data.

Z8000 architecture calls for the placement of stacks as arrays in memory with an address register marking the top of the stack and providing, through based addressing, access to items at locations relative to the top of the stack. The stack register is a dedicated (special purpose) register in some architectures. In the Z8000, any of the registers R1 to R15 can be used as a stack register, although the architecture determines which stack register is to be used for saving returns from a subroutine or the machine state on interrupts.

The implementation of stacks as arrays in memory and the use of general purpose address registers for stack registers make provision for overflow and underflow protection difficult. The Z8000 provides stack limit protection through use of the attribute specification associated with memory protection. Other architectural features are desirable for the support of stacks, including the ability to designate one or more stacks for program use, single- and multiple-argument push and pop instructions, and automatic warning (traps) of impending stack overflow or underflow.

Context switching

One difficulty that arises when several processes run concurrently is the overhead associated with context switching. The context of a process is that portion of its state which occupies shared resources. For example, since all processes must share the program counter (PC), each process's PC value is part of its context. The Z8000 has a single set of general purpose registers, control registers, CPU status registers, and so forth. Thus, when the same processing element (CPU) is allocated to more than one process, the process contexts must include the contents of any register that is used. Context switching saves the context of one process and recalls the stored context of another process.

Automatic context switching is provided for interrupts and traps. When an interrupt occurs, the current CPU status (FCW and PC) is saved on the system mode stack, along with a "reason" read from the address data lines AD15 to AD0 during the interrupt acknowledge cycle. Then new values for the FCW and PC are taken from the program status area (PSA). The IRET instruction restores PC and FCW to the preinterrupt state and discards the reason, leaving the stack as it was before the interrupt. Architectural features that expedite context switching include automatic saving of CPU state on interrupts, single-instruction block register saving and restoring, and access to all necessary control registers.

The Z8000 interrupt and trap handling facility provides an automatic, rapid context switch from the executing program to the interrupt processing routine using interrupt vectors stored in a memory table (the PSA). The FCW, PC values, and a reason are saved on the

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United Kingdom Representative: Scicon Computer Services, Brick Close, Kiln Farm, Milton Keynes, Bucks MK11 3EJ. Phone (0908) 565656. Telex 826693. For European Representative, contact: DACI, Roskildevej 398, DK-2610 Rødovre, Denmark. Phone (01) 41 51 33. Telex 15080. system mode stack, and new FCW and PC values are set from the PSA entry (vector) corresponding to the interrupt type. The IRET instruction restores the CPU to the preinterrupt state, while at the same time removing the saved information from the stack.

Context switching involving general purpose registers is facilitated in the architecture by block register saving and restoring instructions. These can be used to simulate pushing or popping a block of registers to or from any stack. For example, the eight registers R0 to R7 can be saved on the stack controlled by register RR14 by executing

DEC R15,#16	!Make room on stack!
LDM @RR14,R0,#8	Save the registers!

These two instructions require 39 clock cycles of execution time, or less than 4 μ s at 10 MHz.

Stacks are an important tool for meeting the operating system's responsibilities.

In some cases, the values of control registers are essential to the context of a process; the normal mode stack register and the flags register, which contains the bits that define condition codes such as "less than or equal to," are obvious examples. A load control register instruction allows the transfer of any of these registers to or from a general purpose register, permitting them to be saved and restored.

I/O system and interrupts

Operating system responsibilities in the I/O system and interrupts vary greatly with the type of application. Architecture of a general purpose CPU must provide the flexibility necessary to accommodate the I/O requirements of a wide range of applications.

One of the operating system's most difficult tasks is control of access to I/O resources. Unlike memory, which can be divided into large, relatively homogeneous blocks, the elements of the I/O space require special purpose management, protection, and access techniques. In addition, device timing requirements and externally set policies for conflict resolution make hardware support of I/O mechanisms mandatory.

Architectural features that support the I/O system and interrupts are a vectored interrupt scheme; specification under program control of the CPU state to be established for each type of interrupt; and a rapid, automatic context switching mechanism in response to interrupts. Also desirable are a means of defining conflict resolution policies and interruptibility of interrupt processing; a coherently designed family of components, compatible interconnection bus, and established set of bus protocols to allow future family growth; block I/O instructions and direct memory access; and restricted access to I/O facilities.

A vectored interrupt scheme allows the CPU state to be switched immediately to an appropriate processing routine without the need for software to ascertain the interrupt type and call the appropriate routine. This is done on the basis of either the port of connection or the contents of a vector supplied by the interrupting device. The PSA block of memory stores interrupt vectors (ie, the new CPU status) for each type of interrupt and trap. In addition to separate lines for nonvectored and vectored interrupts, as well as a nonmaskable interrupt for situations that cannot wait, there is a table of PC values to be indexed by an 8-bit vector placed on the AD bus by the interrupting device. The block of memory used for the PSA is not fixed, as it is in some CPUs; it can be anywhere in memory, and a pointer to it (the PSAP register) can be set using the privileged LDCTL instruction.

Conflict resolution is achieved through a simple scheme. The three levels of interrupt-nonmaskable, nonvectored, and vectored-are assigned three levels of priority by the CPU. Using the privileged disable/enable interrupt (DI/EI) instruction, the vectored and nonvectored interrupt lines can be masked so that interrupts wait until the unmasking of the associated line. When interrupts arrive simultaneously on more than one line, priority determines which will be processed first. The processing routine for one interrupt type can be interrupted by the routine for another if the corresponding line has not been masked. Whether other lines are to be masked or not can be determined automatically by specifying the appropriate mask bit in the FCW portion of the PSA entry. Otherwise, the determination can be made by the program, which can bracket interrupt sensitive code between DI and EI instructions.

A priority scheme is daisy chained through devices attached to the CPU on the same interrupt line. In this way devices closer to the CPU can interrupt the processing of more remote device interrupts unless the given line is masked during all or part of the processing. This approach allows any priority resolution scheme to be implemented externally.

Block I/O instructions and direct memory access are important and straightforward performance improvement features. Block I/O instructions require careful implementation; they must use general purpose registers continuously to save their current state so that they can be interrupted. Direct memory access functions require the development of bus control protocols and a means of protecting partially loaded or saved memory blocks from access by concurrently executing programs. A key aspect of the Z8000 I/O system is the protection privileged instructions provide, allowing an operating system to manage the I/O interfaces without interference from normal mode programs.

Distributed control

When processes to which separate processing units may have been allocated share a common memory, guarded commands and semaphores are used. Basic architectural support for these techniques is atomic test and set (TSET), a CPU instruction that tests a memory location for the value "available" and simultaneously sets the value to "not available." "Atomic" refers to the fact that there can be no other access to the given memory location between the test and set portions of the instruction. This prevents two concurrently running processes from finding the location set to "available" simultaneously.

Architecture provides synchronizing procedures, both for processes that share memory and for those that do not. In the case of shared memory, the TSET instruction provides the basis for synchronization. In the case of nonmemory synchronization, the Z-BUS specification includes a set of lines and a protocol for resolving simultaneous requests for shared resources while the CPU provides instructions to support the bus connection and protocol.

Support for conventions

In the design of a CPU, consideration must be given to whether architecture should support all conventions equally or encourage specific conventions through special features. For instance, should a CPU be designed with general support for high level languages, or should it be designed to optimize Pascal at the expense of FORTRAN programming efficiency? Should it provide special features that make a subroutine argument passing convention using the stack especially efficient at the expense of the efficiency of other argument passing conventions? Z8000 design supports many conventions, including a segmented addressing scheme, message passing for interprocess communication, component and backplane bus protocols, and interrupt protocols for all components.

A message is a set of characters (or words) emitted by one process and received, asynchronously, by another. The processes do not need to know whether they have been allocated the same or different processing elements. Message passing support includes block 1/O instructions in the Z8000 CPU; asynchronous interprocessor connection in the Z-FIO (first in, first out) buffer chip; acceptance of commands from and delivery of messages to the master CPU in designated message registers by the universal peripheral controller (Z-UPC); and allowance for high speed direct access to memory from external devices (eg, a Z-FIO chip) through the direct memory access chip.

Summary

Several kinds of architectural support are available to system designers for meeting the requirements of the modern operating system. Restriction of access to CPU facilities, restriction of memory use, memory mapping, sharing of programs and data, program relocation, stacks, context switching, an I/O system and interrupts, and distributed control and support for conventions are all tools that can expedite effective system resource management.

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POWER SUBSYSTEMS: PROBLEMS AND SOLUTIONS

Power system designers must expect the unexpected when engineering for reliability. Knowing the vendor doesn't hurt either

by Thiagarajan Natarajan, Ermand B. Centofanti, Allen B. Hansel, and Philip N. Lioio

While designing a modular power subsystem for a minicomputer, a number of exceptional component-related problems were encountered. Problem areas included turn on current surge protection, solid state relays, bridge rectifiers, protective fusing, battery backup manufacturability and reliability, electromechanical power switch selection, capacitors and resistors, output Schottky diodes, fans, busbars, voltage sensing, signal connectors, and standards associations' specifications. The simplified power subsystem block diagram in Fig 1 illustrates component locations relevant to the discussion.

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Turn on surge protection circuit problems

In offline converter design, a solid state relay (SSR) is frequently used to reduce the inrush current to protect the neighboring equipment and the offline converter. A scheme that is presently being used in Perkin-Elmer equipment is shown in Fig 2. Initially, capacitor C is charged through resistor R. After it is charged to a specified voltage (250 Vdc in approximately 750 ms), a control signal turns on the SSR.

Solid state relay problems

When using SSRs, care must be exercised both in the specification of the dv/dt rating and in the circuit design in order to meet the constraints imposed by this rating. False triggering of the SSR must be avoided and attention given to the potential for high pot problems in the SSR.

Specification of dv/dt rating. Care must be taken to specify the dv/dt for the condition of very low source impedance and operating temperature range, and also to make sure that the vendor tests for it accordingly. For example, one of the SSR vendors was performing the dv/dt test per Electronics Industries Association/National Association of Relay Manufacturers

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Fig 1 Component block diagram for power subsystem. Modular component placement is illustrated.







Fig 3 SSR dv/dt reduction circuit



Fig 4 SSR dv/dt reduction equivalent circuit. Network values in line filter can be substituted for calculated value of L.

(EIA/NARM) standard RS-443 with the prescribed $50-\Omega$ source impedance as opposed to almost zero source impedance in offline converter applications.

Design for the required dv/dt rating. A simple circuit to reduce the dv/dt across the solid state relay is shown in Fig 3. Initial turn on approximate equivalent circuit is shown in Fig 4. The voltage Vo and dVo/dt across the SSR can be shown to be

Vo = Vin
$$(I - e^{-Rt}/L)$$

dVo/dt = Vin $(L/R) e^{-Rt}/I$
dVo/dt (max) = Vin (L/R)

With a given R, and Vin (max) known, the required value of L for a given dVo/dt (max) can be calculated. Again, allowance for the inductance value with current and temperature has to be considered to arrive at a value of L to guarantee dVo/dt (max). The network values in the line filter can be used to replace the calculated inductance (L) value.

False triggering of the solid state relay. High common mode voltage between the ac line side and the control side can occur intermittently when the circuit breaker is closed. This can be a major cause of false turn on of the SSR. False triggering is definitely a problem for the application shown in Fig 2. False triggering will cause large inrush current peaks of the order of 250 A through the bridge rectifier and the inrush current may vary from location to location, depending on ac line source impedance. This inrush current will wipe out the bridge rectifier if the bridge rectifier peak current specification does not meet the inrush current peak. Failure of the bridge rectifier might, in turn, wipe out the SSR. Potential for these failures is critical in aerospace and medical applications.

A request to the vendor to application test his SSR will solve the problem of false triggering. By testing the relay in the application test setup with the photocoupler removed, the vendor can isolate the problem of false triggering from high dv/dt. The relay should pass the turn on test without any false outputs. One way to prevent false triggering is to reduce the coupling from the ac side to the control side, through the photocoupler itself. One vendor who had this problem used a different type of photocoupler with an increased gap between the light emitting diode (LED) and the phototransistor. Increasing this gap can reduce the direct coupling into the base of the phototransistor. The vendor can also make circuit adjustments to avoid false triggering.

High pot failures. Depending on the requirements [such as meeting Underwriters' Laboratories (UL), Canadian Standards Association (CSA) or Verband Deutscher Elektrotechniker (VDE) specifications], dielectric strength between the ac side and the control side can be specified. High pot failures of one Perkin-Elmer vendor were attributed to the photocouplers used within the relays. There is also a delayed action nature of the breakdown that sometimes occurs several seconds after initial application of voltage. The vendor can be requested to increase his vigilance at his receiving inspection of photocouplers with longer duration high pot checks (say one minute), and change his photocoupler, if necessary.

There may be other types of failures in the solid state relays. One vendor's power silicon controlled rectifier (SCR) chip was damaged in assembly, subsequently resulting in shorted output when put in service. Vendors can be requested to do stabilization bake, temperature cycling, and post conditioning electrical tests before shipment, and to closely monitor the testing of relays.

Bridge rectifier problems

As explained before, the diode surge rating shall be specified for the case of false triggering of SSR. The construction details of the bridges must be analyzed to make sure that the surge rating is, indeed, what is specified. Perkin-Elmer used a 50-A, 600-V bridge rectifier in one of the power subsystems. Design problems encountered can be seen in the results obtained from four different vendors.

Two of the vendors had a similar assembly design: diode elements within the bridge consist of parallel axial lead rectifiers soldered between massive heat dissipator plates. These plates, part of the individual terminal stampings, have their major surface area located parallel to the base of the device.

The third vendor's device featured three parallel axial lead rectifiers that were simply wired, in almost random fashion, to 0.25" (0.64-cm) terminals. These terminals had no massive heat dissipator sections.

The fourth vendor's design was the only one that used a single large rectifier per diode element. In this case, the chips in the bridge were soldered parallel to the base. Lead frames for bridge interconnections and terminals, and better thermal transfer, were also included.

Although the first two vendors' parts had slightly better thermal properties when operated at either 25 or 30 A, the overall limitations of paralleled design really became evident in overload situations. Even for the current levels within the 50-A bridge's ratings, there was evidence of the normalized thermal resistance value changing by 20% from 25- to 30-A level. The number of diodes in parallel is also a performance factor.

There is no guarantee of perfect current sharing in the parallel diode design. When operated at high surge current levels, overstress of one or more of the paralleled diodes can result in failure. This is important for the application shown in Fig 2.

The third vendor was a disaster for Perkin-Elmer. His diodes were not matched for voltage drops. Even the outer surface was not flat, causing heat sinking problems. The surge, due to premature turn on of the SSR in the start sequence, caused hard failures of his 50-A bridge almost immediately. This, in turn, caused hard failures of the solid state relay.

Race conditions in the control logic

Another condition that caused premature turn on of the SSR was a race condition in the controlling logic. During startup, the internal bias supply for the control logic came up very slowly, resulting in a false SSR turn on signal. One volt was sufficient for the control signal to activate the SSR. Adequate precautions must be taken in the initial design to prevent this problem.

Selection of protective fusing

Selection of fuse F (Fig 2) is an important consideration to protect the surge resistor R across the SSR. The heat sink type (25-W) resistors that are used tend to explode, if not protected. If someone happens to apply the input voltage with shorted switching transistors in the offline converters loading the bridge rectifier, without a properly sized fuse (F3), the resistors will fail catastrophically. Since the capacitor is about 10,000 µF, resistor R must have the proper energy rating to survive during turn on. In order to prevent circuit failure, the fuse F has to meet two requirements: it must now blow during normal operation, and it must protect the surge resistors when the power subsystem is turned on with shorted switching transistors under worst-case low- and highline conditions. A worst-case analysis can be done by having the input voltage as dc and equal to the peak value of the input ac sinusoidal waveform. Worst-case capacitance, maximum value, should be assumed for this analysis. The circuit is shown in Fig 5.



Fig 5 Surge resistor protection circuit. Each resistor must be capable of withstanding peak plus steady state power dissipation levels.

It can be shown that

 $i(t) = (V/R) e^{-t/RC}$

Energy in total resistance, in joules

$$\int_{0}^{\infty} i^{2}(t) dt R = \frac{1}{2} CV^{2}$$
(2)

Energy, in resistors R1, R2, and R3, (expressed in joules) may be broken down as the sum of the following

 $R1 = \frac{1}{2} CV^2 R1/R$ (3)

 $R2 = \frac{1}{2} CV^2 R2/R$

 $R3 = \frac{1}{2} CV^2 R3/R$ (5)

Each resistor must be able to withstand the peak energy in addition to the steady state power dissipation. Peak energy is calculated up to the time the SSR is turned on, and should be within the energy rating of the resistor. The calculation of root mean square (rms) current through the resistor for period T is

$$I rms (T) = \sqrt{[1/T \int_{o}^{T} i^{2} (t) dt]}$$

= (V/R) \sqrt{[RC/2T (1 - e^{-2T/RC})]} (6)

Energy in R1 for time T

1² rms (T) R1 T

Eq (6) also provides the rms current through the fuse. From Eq (6) and published fusing current-time characteristics, a proper fuse can be selected.

After selecting the fuse rating for normal operating conditions, energy in the resistors must be checked at high- and lowline inputs, and under conditions of shorted switching transistors. The equivalent circuit is shown in Fig 6.

Highline I (h), the rms current through the fuse, is 264/R. The time for the fuse to open, T1, is obtained for F1 from the available fusing time characteristics and the energy in resistor R, which equals I^2 (h) R T1. This calculated energy should be checked against the manufacturer's energy ratings for R1, R2, and R3.

Lowline is the worst case for the resistors since it takes longer for the fuse to open under a fault condition. Lowline rms current through the fuse, I (1), is 180/R. Again, the time for the fuse to open, T2, is obtained for F1 from the available fusing time characteristics and the energy in resistor R, which equals I² (1) R T2.

It should be noted that it is difficult to meet the requirements under all conditions of the ac line and for both normal and abnormal (ie, shorted transistor) operation. If the system is turned on at, say, 100 Vrms, an unlikely but not impossible circumstance, the fuse will not open at all and the surge resistors are not protected under shorted transistor conditions.



Fig 6 Equivalent circuit for resistor surge protection.

Reliability of battery backup system

(1)

(4)

A 180-Vdc battery (ten 18-Vdc subassemblies in series) module is used to support the high voltage dc bus that is derived from the rectified ac to provide metal oxide semiconductor (MOS) memory battery backup operation during power outages. The use of the series connected batteries posed a reliability problem. It was thought that such a large number of series connected cells might exhibit an excessive failure rate. The low level of failure reports from inhouse testing, as well as from the field, have shown this not to be a problem.

Use of a 180-Vdc battery posed a shock hazard during assembly and handling. Implementation of an interlocked connecting system, whereby the full battery stack circuit is not connected until the module cover is secured, is responsible for eliminating this safety question.

An unforeseen battery handling problem was encountered during the initial phases of production. If one of the 18-Vdc battery subassemblies was accidentally shorted during module assembly, the internal interconnecting links between the cells would raise the temperature of the module package to a point that constituted a burn hazard to anyone handling the module. In one instance, this high temperature condition resulted in a fire within the module.

In response to these problems, the battery vendor redesigned the battery shell to meet the requirements of UL flame retardency specification 94-V-2. In addition to more insulation around the interconnecting links, the links were redesigned to fail to open if they sustained a short circuit current for more than 1 s. Also, the battery design was changed to incorporate a recessed positive terminal, reducing the chances of an accidental short circuit across the battery terminals.

Close attention was given to the effects of battery shelf life. The shelf life of an unfloated battery (ie, not maintained on trickle charge) depends on ambient temperature during storage and initial charge level prior to storage. To ensure that batteries drawn from stock would always be good, it was necessary to set up quality control (QC) procedures to monitor the storage periods of the batteries in stock. Battery specifications included requirements for vendor supplied parts to be delivered with a minimum charge level. To monitor parts, the QC department developed test procedures for checking the battery charge level at incoming material inspection.

Circuit breaker or on/off switch

An on/off switch is not recommended if operation of the switch may result in a high current surge through its contacts during a power-on operation. False firing of the SSR, even once, could cause the contacts of the switch to weld. Apart from the SSR, a 60-Hz transformer for battery charging, bias supplies, and other low current outputs, connected ahead of the SSR, may draw a surge current of 60 to 90 A during a poweron switch operation. This could also result in welding of the switch contacts after repeated turn on sequences.

To get around the problems of using a conventional on/off switch, a circuit breaker should be used in place of the switch. A properly sized circuit breaker, rated at 150% of the maximum power subsystem run current, will tolerate several hundred amperes of surge current experienced during a false triggering of the SSR turn on

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sequence. In addition to the run current criteria, the circuit breaker timing curve must be carefully looked at to avoid nuisance tripping of the breaker due to the surge current characteristics of any transformer loads applied ahead of the SSR.

Capacitor and resistor problems

A number of problems encountered with capacitors and resistors were due to poor vendor QC practices.

High voltage dc input capacitor problems. The high voltage dc filter capacitors, large aluminum electrolytic devices that filter the rectified ac voltage, accounted for several unexpected problems, mainly due to poor vendor practices. One vendor submitted parts (1300 μ F at 450 Vdc) that exhibited high leakage current at 300 Vdc. Another vendor delivered parts that did not meet the shelf life specification. Perkin-Elmer's QC department was required to provide strict incoming inspection testing to ensure receipt of quality parts. One hundred percent testing of input leakage current and a 1% acceptable quality level (AQL) lot test for shelf life is recommended to yield an acceptable product for use in manufacturing. Experience shows that lack of adequate incoming testing on these parts results in catastrophic failures, both in manufacturing and at the customer site after installation.

In addition to vendor quality problems, high pot problems appeared during the initial production phase. Since these capacitors were mounted directly on the chassis, it became necessary to add a piece of insulation under each to reduce the high pot leakage current between the capacitor element within the case and the chassis.

Output capacitor problems. Some output capacitors received from one vendor contained no electrolyte. The vendor was advised to improve his internal QC practice. Offline converters implemented high ripple current stacked foil capacitors. Although the vendor had produced these devices for several years, he had not fully solved the electrolyte leakage problems. The eventual solution was an epoxy seal around the electrical terminations. Once the vendor installed this fix there were no further problems with this part.

Other capacitor problems. More high pot problems were experienced in the mounting of small axial leaded capacitors that use only their leads for mechanical attachment to the printed circuit (PC) board. Depending upon the position of the capacitor, the distance between high voltage PC track and the capacitor leads would vary, and high pot failures resulted. By exercising care in the PC board layout, and realizing that handling can force the parts to deviate from their initial mounting position, this problem can be eliminated.

Resistor problems. Some integral heat sink resistors used across the solid state relay could not meet the high pot test requirements. Even 0.25-W resistors, if not evaluated, could give rise to serious problems. One of the approved vendors supplied resistors to a 0.25-W purchase specification that turned out to be less than 0.1-W rated parts. Unfortunately, there was no power testing applied to these parts at incoming test and they filtered into the manufacturing system. A small number of these devices failed during system test, and an additional small number made it out into the field before QC collected the data identifying these parts as deficient.

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The parts were assembled into a critical circuit which resulted in a large installation being nonoperating due to the failure of a 30 cent resistor. The moral of this story may very well be "test everything at incoming inspection."

Output Schottky diode problems

Schottky diodes are used in the offline switching converters where they provide high efficiency rectification with a 20-kHz input waveform. When these devices are used, peak reverse voltage, under all case temperatures, must be specified. Peak reverse voltage should be checked during steady state operation and also during transient conditions, especially during converter turn on. Because of a dv/dt limitation across the device, good circuit design dictates the use of properly designed resistive-capacitive (RC) snubber circuits. If a snubber is not used, the ring-out voltage across the diode results in peak reverse voltage exceeding the rating of the parts. Again, close attention should be paid to minimizing this reverse voltage, including high frequency ring-out, during all possible operating conditions.

A good deal of thought should be given to the assembly of the Schottky diodes onto the heat sink. The connections from the inverter transformer to the diodes have to carry high currents, on the order of 150 A.

The moral of this story may well be "test everything at incoming inspection."

Though connecting wires were selected to be multistranded [eg, 84 strands of #27 American wire gauge (AWG)] for flexibility and ease of mechanical assembly, diodes were mechanically stressed due to improper torquing of the screw connection between the diode's anode flag and the cable termination. In some instances, the diode's glass-to-metal seal at the anode fractured and the anode termination was free to rotate inside the case. Some of the stressed diodes survived the initial subassembly testing but, luckily, failed before leaving system test. In order to overcome these problems, mechanical assembly procedures require special fixturing to support the diode's anode during tightening of the screw termination. An allen head screw, used in conjunction with a torque measuring drive, provides control over the tightening torque applied to the connection. The tightening torque is critical since too low a torque could result in a loose connection that would overheat during converter operation.

Fan problems

Fans must be specified to operate at the extremes of high- and lowline voltage overlayed on high and low ambient temperatures. Cases have occurred where fans, used to cool the power subsystem, have stopped or refused to start due to bearing related problems. Some fans that did start were slow to accelerate or did not maintain design speed. These problems, isolated to a single vendor, were caused by loss of lubricant through physical leakage, accelerated by high temperature stress experienced during continuous operation. The escaping lubricant oxidized and combined with residual graphite

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NCR OEM Marketing Division to form a coating on the bearings. This increased the load on the fan motor causing it to slow down, stop, or not to start at all. To eliminate this problem, the vendor changed his design to a sealed bearing. A ball bearing fan may be required in an environment that exceeds 50 $^{\circ}$ C.

It is wise to provide overtemperature protection in the power subsystem to avoid the possibility of switching transistor failure due to a faulty fan. Thermal testing of the power subsystem with and without fans determines the optimal location of the thermal sensor. In Perkin-Elmer's case, the output diode heat sink containing the Schottky diodes turned out to be the best location, since it experienced the fastest rise in temperature due to a faulty fan condition. To preclude field problems, field service engineering should periodically check the condition of all fans.

Busbar selection and voltage sensing

Busbars were selected to carry 5 V at 300 A to the processor, memory, and I/O subsystems. Initially, phosphor bronze busbars were used because of machinability and low cost. However, due to poor electrical conductivity, this material was quickly discarded in favor of electrolytic tough pitch copper.

Worst-case analysis of the power distribution system led to the optimum location of voltage sense points on the middle of the busbars. In production, an unexpected problem occurred. One of the links interconnecting two elements of a single busbar, ahead of the voltage sense points, became loose. Although the voltage sense point was being regulated to 5 Vdc, the logic boards located above the loose connection registered more than 7 Vdc. Consequently, it is important to have overvoltage protection at remote voltage sense points and also at the output of the power subsystem.

Connection of the sense leads to the busbar assembly posed additional problems. Unless the positive and negative lead attachments were different, it would be possible to reverse them, either in manufacturing or in the field during servicing. To eliminate this problem, the two sense wires were color coded and different types of terminations were used to complete each connection.

Signal connector problems

It is important that signal connectors not become loose after repeated insertion and removal. If the signal cable acts as a lever, any small disturbance on the cable will force the connector to rotate, opening some of the signal connections. This is critical if the signal connector carries synchronization signals between the regulators of the offline switching converters. When the connectors become loose, two paralleled converters fight for synchronization control and eventually switching transistor failures occur. To overcome these problems, connectors that employ some means of mechanical captivation—screws or locks—should be used.

UL, CSA, and VDE considerations

The designer must have adequate knowledge of the agency regulations at the outset of a design to take care of potential problems. Following are detailed considerations: the minimum distance between the edges of high and low voltage tracks should be kept to 0.15'' (0.38 cm); high voltage capacitors should have appro-

priate bleed (discharge) resistors across them. Upon disconnection of the voltage source, the voltage across these capacitors should discharge to less than 50 Vdc within 5 min; appropriate name/instruction/warning plates should be affixed to the product in easily visible locations; close attention should be paid to safety grounding of the equipment. High pot leakage requirements on individual components must be adequately specified; ac distribution boxes with convenience outlets

A major concern is...the need to exercise extreme care in choosing vendors.

for other attached equipment should meet the fusing and selection criteria specified for branch circuit applications; wiring devices, such as plugs and receptacles, must be derated by 20%. For example, if 30-A hardware is used, the ac line current for equipment operation must not exceed 24 A under worst-case line voltage conditions; adequate protection should be provided against the possibility of high current short circuit faults appearing at critical points in the system; in primary (high voltage) circuits, use of UL/CSA listed or recognized components are recommended wherever possible to avoid approval delays.

Summary

In addition to the specific technical solutions to problems described in this article, major concerns are the need to exercise extreme care in choosing vendors and to follow up with continuous interaction to ensure complete conformity to requirements.

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A STATUS REPORT: ANSI 8 " HARD DISK INTERFACE

Progress has been swift on ANSI 1226, the rigid disk interface standard for 8" Winchester drives

by Anthony F. Kozlowski

n mid-1979, at the urging of several drive manufacturers, American National Standards Institute subcommittee X3T9.3 started work on what eventually became the 1226 rigid disk interface for 8" Winchester drives. A year after work began, hardware aspects of the interface had been defined. Within 18 months, 99% of the interface had been completed. It has been approved by the X3 parent committee, and sent out for public review. It will also be submitted to the International Standards Organization as a proposed standard.

The fact that there are over 200 people on the X3T9.3 subcommittee mailing list indicates how well this proposed standard is being accepted in the United States.* Also, there have been requests from all over the world for copies of the standard.

Overview

Achieving an interface that is relatively low cost in construction and capable of a high degree of configuration flexibility is the general intent of the standard. A fundamental goal in developing the standard was to use a standard 50-pin, flat ribbon cable and standard driver/receiver hardware (Fig 1). Hardware constraints tended to limit the upper bandwidth to a data rate of 10M bps. Also, to keep costs low, a bit serial data transfer scheme was employed; data are transferred between the host and drive in a bit by bit serial stream. Commands are transmitted in a byte serial mode. The actual disk encoding method is not defined by the standard, leaving it up to the drive manufacturer. Generally, modified frequency modulation has been the preferred coding method.

The standard provides an interface of medium level intelligence in which command transfers are on a byte level across an 8-bit bidirectional command bus. All communication is structured as a 2-byte transfer sequence—the first byte is a command byte, the second byte a parameter byte. Definition of the interface makes it amenable for use with current microprocessor technology in the command and control areas.

Interface general description

Eight lines of the flat cable are designated for carrying parameter, command, status, and sense byte information in a parallel mode, as well as selecting a specific drive (up to eight), prior to data or status/sense transmission. Other lines carry bus handshake and control signals along with four differential signal pairs for data clock communications.

Multiple-function lines. The eight control bus lines (Fig 2) are used for information transferred in the parallel mode, as well as individual selection and attention recognition of up to eight drive modules in the string. Parallel mode transmissions consist of 8-bit command and parameter bytes, including a general

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^{*}Requests for a copy of the currently available standard should be addressed to Gary Robinson, Mail Station ML12-3/E51 Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Tel: 617/493-4094







status byte and two sense butes The

status byte, and two sense bytes. The repertoire of command codes (in hexadecimal) is shown in Tables 1 and 2, while the status byte and sense bytes are detailed in Tables 3, 4 and 5.

The American National Standards Institute (ANSI) specification defines four command categories: *Mandatory*—must be implemented by all drives; *Optional*—may be implemented by specific manufacturers; *Unique*—allowing manufacturers to make use of features in their own drives not covered in the standard; and *Reserved*—for future implementation by ANSI as desired. By defining these commands, the committee tried to provide for many of the important features found in the rigid disk drives. Radial mode transmissions consist of using the same eight control bus lines on a one/drive basis, providing a clean and unambiguous method of selecting and deselecting, and for reporting the status of the attention condition of each one of these drives on a string.

Single-function lines. Pins 10 through 50 of the interface cable operate in pairs to carry clock, data, and specific functional handshake and control signals.

	Command I	Repertoire -	Command Out
	Function	Command	Parameter Out
	Attention control	40	Bit 7 0 = enable attentior 1 = disable attention
	Write control	41	Bit 7 1 = write enable 0 = write disable
	Set upper cylinder address	42	MSB of cylinder addres
	Set lower cylinder address	43	I SB of cylinder address
	Select moving head	44	Head number
	Load attribute number	50	Address byte
	Load device attribute	51	Information byte
	Select fixed head	52	Head address
	Read control	53	Bits 7, 6
			OX = nominal strobe 10 = strobe early 11 = strobe late
	Offset control*	54	Bits 7, 6 OX = no offset 10 = offset forward 11 = offset reverse
	Spin control*	55	Bit 7 1 = spin up 0 = spin down
ļ	_oad bytes/sector high	56	MSB of bytes/sector
1	_oad bytes/sector med	57	Med SB of bytes/sector
	oad bytes/sector low	58	LSB of bytes/sector
ļ	_oad sector pulses/		MSB of sector
	track high	59	pulses/track
l	Load sector pulses/	F A	Med SB of sector
1	and sector pulses/	5A	pulses/track
	track low	5B	LSB of sector
ι	oad read permit high	6B	MSB of cylinder address
1	oad read permit low	6C	LSB of cylinder address read enabled only on cylinder equal to or greater than the above
L	.oad write		greater than the above
	permit high	6D	MSB of cylinder address
L	oad write permit low	6E	LSB of cylinder address write enabled only on cylinder equal to or greater than the share
ı	oad test byte	6F	Test byte

*Time dependent commands, generating attention condition at completion

TABLE 2

Command Repertoire - Command In

Function	Command	Parameter In
Report "illegal command"	00	General status
Clear fault	01	General status
Clear attention	02	General status
Seek*	03	General status
Rezero*	04	General status
Report sense byte 2**	OD	Sense byte 2
Report sense byte 1 * *	OE	Sense byte 1
Report general status**	OF	General status
Report device attribute	10	Device attribute byte
Set attention*	11	General status
Reserve device	12	General status
Release device	13	General status
Selective reset*	14	General status
Seek to landing zone*	15	General status
Partition track*	16	General status
Report cylinder high	29	MSB of cylinder address
Report cylinder low	2A	LSB of cylinder address
Report read permit high	2B	MSB of cylinder address
Report read permit low	2C	LSB of cylinder address
Report write permit high	2D	MSB of cylinder address
Report write permit low	2E	LSB of cylinder address
Report test byte	2F	Echo byte

Mandatory commands-codes 00 through 0F

Optional commands-codes 10 through 2F Vendor unique commands-codes 30 through 3F

All unused bits in parameters are zero

*Time dependent commands, setting attention condition at completion

* Events reported can set attention condition without preceding command

TABLE 3

Status Byte Characteristics

Bit	Multiport (common/specific)	Meaning	Mandatory optional
0	С	Not ready * * *	M
1	S	Control bus error*	M
2	S	Illegal command*	M
3	S	Illegal parameter*	M
4	C/S	Sense byte 1 * *	M
5	C/S	Sense byte 2**	M
6	С	Busy executing	M
7	С	Normal complete*	М

TABLE 4

Sense Byte 1 Characteristics

Bit	Multiport (common/specific)	Meaning	Mandatory/ optional
0	S	Seek error*	м
1	S	Read/write fault*	M
2	С	Power fault*	0
3	S	Read/write permit* violation	0
4	С	Speed error*	0
5	S	Command reject*	M
6	C/S	Other errors*	0
7	C/S	Vendor unique errors*	0

Communication sequences

Two modes of communication exist: parallel and radial. With the controller's select out/attention in strobe at 1, radial mode selection is a specific drive, as indicated by a 1 on a specific line on the control bus (Fig 2, lines 2 through 9). If select out/attention in is 0, communication is in the parallel mode.

To use the radial mode, each drive must be previously set up to recognize only the specific control bus bit that refers to that drive. Setting the control bus line is done in conjunction with setting the bus direction out line. Selection acknowledgment to the controller is via the bus acknowledge line.

The radial mode permits the controller to communicate with drives in a multiplexing manner, allowing one drive on a string to seek while another is reading or writing. Fig 3 shows the actual selection sequence after the controller asserts port enable to put all drives into their initial state. At this point, the drive is selected and the controller can communicate in the parallel mode. Bus control lines are loaded with the 8-bit coding of the command. The sequences are shown in Figs 4 and 5.

TABLE 5

Sense Byte 2 Characteristics

Multiport (common/specific)	Meaning	Mandatory/ optional
С	Initial state*	м
С	Ready transition*	M
S	Device reserved to this port	0
S	Forced release*	0
S	Device reserved to alternate port	0
C	Device attribute table modified*	0
С	Positioned within write protected	
	area	M
C/S	Vendor unique attentions*	0
	Multiport (common/specific) C C S S S S C C C C/S	Multiport Meaning (common/specific) C Initial state* C Ready transition* S Device reserved to this port S Forced release* S Device reserved to alternate port C Device attribute table modified* C Positioned within write protected area C/S Vendor unique attentions*

*Zero to one transition sets attention condition

**See sense byte 1 and sense byte 2

***Ready to not ready, and not ready to ready transition sets attention condition



Fig 3 Drive selection sequence diagram. Port enable signal places drive in initial state. Controller then asserts bus direction out, sets bit line to select drive, asserts select out/attention in, reacts to bus acknowledge, drops select out/acknowledge in, and drops bus out.

Command communication up to this point has registered the command in the drive control circuitry. That fact has been acknowledged by both controller and drive. The remainder of the parameter in/parameter out protocol sequence varies, however, depending upon whether the command is one with parameter in (information from drive to controller) or with parameter out (information from controller to drive). The complete parameter in sequence (Fig 4) is

- Controller asserts bus direction out, indicating that communiction is from controller to drive
- Controller asserts command request, identifying that signals on control bus lines represent a command
- Drive reads control bus, stores command byte, and asserts bus acknowledge
- Controller senses bus acknowledge, drops command request
- Drive senses drop of command request, drops bus acknowledge
- · Controller drops bus direction out
- Controller asserts parameter request
- · Drive loads control bus with requested information
- Drive asserts bus acknowledge
- Controller reacts to bus acknowledge, reads control bus, stores information and drops parameter request
- Drive reacts to dropping of parameter request, drops bus acknowledge

The parameter complete out sequence (Fig 5) is

- · Controller asserts bus direction out
- Controller loads control bus lines with data and asserts parameter request
- · Drive reacts to parameter request and receives data
- Drive acts on information. (For example, if command had been set upper cylinder address, drive stores information to be used later with seek command. If command had been select moving head, drive selects new head immediately.)
- Drive asserts bus acknowledge
- Controller reacts to dropping of bus acknowledge, drops parameter request
- Drive reacts to dropping of parameter request, drops bus acknowledge, ending the sequence

Time dependent commands

The previous sequences concern immediate commands—the drive acts as soon as the command is registered and the controller remains in communication. Time dependent commands take time to execute and consist of seek, rezero, selective reset, seek to landing zone, partition track, offset control, or spin control. In Figs 4 and 5, the drive asserts the busy line when parameter information is on the control bus, prior to asserting bus acknowledge. With time dependent commands, the drive accepts the command, asserts the busy line, completes the handshake protocol, then begins to execute the command.

The busy line can be set while the drive is executing the command (depending upon the architecture of the drive), indicating to the controller that the particular drive cannot communicate with it. Meanwhile, the controller can issue commands to another drive on the string or be otherwise occupied.

When the busy drive completes execution, an additional sequence occurs.

- Drive drops busy and asserts attention
- Drive puts normal complete bit in general status byte on bus control
- Controller goes into radial mode to determine which drive is involved, by dropping bus direction out and asserting select out/attention in. (This signal tells all drives to put attention information on control bus line associated with each drive.)
- Selected drive asserts bus acknowledge, indicating receipt of select out/attention in
- Controller reacts to bus acknowledge, reading control bus lines to determine which drives need attention
- Controller drops select out/attention in, taking the interface out of radial mode

With this information, the controller services each drive that requires it, by putting the interface into radial mode, selecting the drive that requires attention, shifting to parallel mode to obtain that drive's status byte, then acting on that information in the appropriate manner.

Control-line characteristics

General observations concerning communication lines will aid in understanding the interface operation. The attention signal is a party line common to all drives in

One unique feature is the attribute table, by which a controller can record and react to the specifics of each drive to which it is connected.

the string, indicating to the controller that at least one drive requires attention. Typical reasons for this signal are that drive is in initial state; there is a normal completion of a time dependent command; an error or fault exists in the drive, such as speed or power fault; there is a violation of read permit or write permit restrictions; there is an inadvertent modification of the attribute table by the controller; or, the drive has been forced to release itself from a port in a dual-port system. In some cases, the attention signal calls for immediate action by the controller; in other cases, passing information of varying urgency is the purpose.

The control of information flow always resides in the controller, through the use of the bus direction out

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Fig 4 Command parameter in handshake protocol. Busy signal is asserted prior to bus acknowledge for a time dependent command. Attention signal is asserted at completion of a time dependent command.



Fig 5 Command parameter out handshake protocol. Time dependent command is handled in same way as in command in situation.

signal. Additionally, the interface is put into the radial mode through assertion of the select out/attention in signal. This step is necessary either to select a drive or to request the current status of attention information from the drive.

Since the busy signal always indicates that a drive generating it cannot communicate with the controller, the controller sequence must always check the drive before originating a command sequence. Finally, the bus acknowledge signal is the drive's reaction to information on the control bus. In the parallel mode, the signal tells the controller that the drive is responding to a command or parameter request; in the radial mode it tells the controller that there is a selected drive on the string. See Fig 6.

Command and status byte characteristics

The four categories of commands are: mandatory, optional, vendor unique, and those reserved by the Committee for future expansion. (See Tables 1 and 2.) Mandatory commands allow for very basic drive operations such as seek, rezero, set cylinder addressing for seeking, select head, enable or disable writing, enable or disable the attention signal, and the reporting of status information.

However, the full versatility of the ANSI interface is usually not realized unless the optional commands are used. Some capabilities these commands provide include testing the integrity of the communication line

between the controller and the drive; dividing the disk surface into two regions, one on which reading is allowed, the other on which it is not; dividing the disk surface into two regions, one on which writing is allowed, the other on which it is not; and changing the sector configuration of the disk drive to make the drive configurable for different applications. Additional capabilites include recovering marginal data through judicious use of early or late read strobe, and/or forward or reverse track offset; protecting written data during a spin down cycle by moving the heads away from data areas (seek to landing zone); and tailoring controller operating parameters on the basis of a specific manufacturer's drive, using the attribute table (guaranteeing availability of alternate sources of drives where necessary).

Status and sense byte characteristics

Principally, the general status byte indicates to the controller why a specific attention condition exists (See Table 1). Its bits detail whether or not a time dependent command was completed normally; if a time dependent command completed abnormally due to an error or fault situation; if a bus protocol error has occurred; if the controller has sent

commands invalid in this implementation of the ANSI interface, or not implemented by the ANSI committee; and whether or not the drive is able to reliably perform a seek or read/write operation.

Sense byte 1 (Table 4) indicates information such as power faults, read/write fault, speed error, or other aberrations that may have caused an attention signal. Also, it specifically contains a bit that indicates seek error, telling the controller that it must command a rezero operation before doing other head movement. Sense byte 2 (Table 5) contains general information rather than just error indications. Included are status indications that show if the drive is in the initial state; if the not ready line in the general status byte has been toggled from one state to the other; if the attribute table has been inadvertently modified by the controller; and if the drive is positioned at an area defined as write protected (by a write permit command, write control command, or an external write protect switch).



Fig 6 Attention in sequence. Selected drive will assert bus acknowledge line.

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TABLE 6

Device Attribute Table*

Attribute	Number	Parameter	8431/32 Default	8533 Default
User ID	00	User defined	00	00
Model ID high	01	Vendor defined	84	85
Model ID low	02	Vendor defined	31, 32	33
Revision ID	03	Vendor defined		
Device type ID	OD	Device dependent	01	01
Table modification	OE	Action dependent	40	40
Table ID	OF	Vendor defined	01	01
Bytes/track high	10	MSB of number of bytes	00	00
Bytes/track med	11	Med SB of number of bytes	46	46
Bytes/track low	12	LSB of number of bytes	00	00
Bytes/sector high	13	MSB of number of bytes	00	00
Bytes/sector med	14	Med SB of number of bytes	02	02
Bytes/sector low	15	LSB of number of bytes	56	2E
Sector pulses/track high	16	MSB of number of sector pulses	00	00
Sector pulses/track med	17	Med SB of number of sector pulses	00	00
Sector pulses/track low	18	LSB of number of sector pulses	10	1F
Sectoring method	19	Sectoring method	01	01
Number of cylinder high	20	MSB of number of cylinders	01	03
Number of cylinder low	21	LSB of number of cylinders	18	46
Number of moving heads	22	Number of heads	02 04	04
Number of fixed heads	23	Number of heads	-	-
Encoding method 1	30	Encoding method		
Preamble 1 length	31	Number of bytes		
Preamble 1 pattern	32	Preamble pattern	1.11.2.5	
Sync 1 pattern	33	Sync pattern		
Postamble 1 length	34	Number of bytes		2.1
Postamble 1 pattern	35	Postamble pattern		
Gap 1 length	36	Number of bytes		
Gap 1 pattern	37	Gap pattern		-
Encoding method 2	40	Encoding method		
Preamble 2 length	41	Number of bytes		-
Preamble 2 pattern	42	Preamble pattern		-
Sync 2 pattern	43	Sync pattern		-
Postamble 2 length	44	Number of bytes		-
Postamble 2 pattern	45	Postamble pattern		-
Gap 2 length	46	Number of bytes		
Sap 2 pattern	47	Gap pattern	No. of Control of Cont	
Range of numbers EO through FF (in All other unused numbers reserved f	hexadecimal) re for future standa	served for vendor unique applications rdization		

Advantages

Original equipment manufacturer engineers should be aware of the ANSI interface advantages to consider choosing it over several other existing alternative interfaces. One unique feature is the attribute table, by which a controller can record and react to the specifics of each drive to which it connects. For example, the 3M 8400- and 8500-series drives are defined by the attributes list in Table 6. Contained in drive firmware, these values establish parameters and limits for use of the drive as dictated by the drive's physical attributes (number of heads and cylinders, number of heads, device type, make and model, sectoring method, sector format, etc). In addition, the attribute table allows the controller to be self-structuring (ie, drives need not be strapped in, cutting installation costs and permitting easier second sourcing). Most troubleshooting involves determining that the drive is correctly strapped, requiring considerable effort with prints and instruments.

With the storage module drive (SMD) interface, it is necessary to know the configuration at setup time, address space limitations (which ANSI does not have), and limited diagnostic indications. Finally, the use of microprocessors in both the controller and drive allows ANSI interface users to easily talk across the interface; this would require considerably more hardware if the SMD interface were used.

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Fig 7 Intelligent peripheral interface signal summary (as defined to date)

eliminating pulse position sensitivity. Moreover, the timing system in the ANSI interface is well defined; in the floppy system it is embedded in the data, making it more susceptible to noise pickup, possibly resulting in data error.

What next from ANSI?

ANSI subcommittee X3T9.3 has started work on the next interface level for rigid disks and other types of peripheral storage devices. This intelligent peripheral interface is defined as high level. The intent is to achieve a much higher level of relative intelligence in the disk



electronics; it will contain both primitive level commands and symbolic or logical level commands. Structured to handle not only rigid disk memory devices, the interface will also handle certain tape devices, typically used for backup. Printers are likely to be incorporated, also.

This high level interface will continue to use a 50-conductor transport system in either flat ribbon or coaxial cable form. Anticipated data rate is the reason for including coaxial cable. An upper data transfer rate of 5M bytes/s or 40M bps, with data transferred as 8-bit bytes or 16-bit words (2 bytes/transfer), is the present goal. As with the ANSI rigid disk interface, the intelligent peripheral interface will also be designed to use standard line drivers and receivers to keep costs low.

Further, the high level interface is being structured to work with current microprocessor technology in such a way that it can be used with or without data buffering. A set of mandatory commands, a set of defined optional commands and, finally, a set of user defined commands will be the general command structure. Fig 7 shows the intelligent peripheral interface defined to date.

Summary

Advantages of the rigid disk interface include a logical and straightforward design that uses current microprocessor technology. Compared to other interfaces currently on the market, it has good data rate capabilities up to 1.25M bytes/s. In addition, the interface uses standard hardware, including a 50-pin flat ribbon cable and standard connectors. The fact that it is rapidly gaining acceptance in the industry means that the user can easily obtain second and third sources for drives. Finally, the standard lends itself to use with a tape backup system.

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For further information, contact Siemens Corporation, OEM Data Products Division, 240 E. Palais Road, Anaheim, California 92805, (714) 991-9700 or call Atlanta, GA (404) 441-0882; Boston, MA (617) 444-6554; Dallas, TX (817) 461-1673; Iselin, NJ (201) 494-5311; Sunnyvale, CA (408) 735-7770.

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A system that programs itself

An integrated business management computer system, Dimension One allows applications program development to be achieved 8 to 20 times faster than with conventional programming. The "programmerless software," from Capro, Inc, comes as an answer to the industry shortage of programmers for sophisticated advanced systems coding, compiling, debugging, and testing. The design objective was to create a system that could program itself, thereby eliminating the need for highly technical programmers.

Dimension One is driven by a single, all-purpose, multi-application program that resides in 32k bytes of main memory. Up to 32 terminals can be accommodated with up to 1M-byte max main memory and 300M bytes of disk storage. A data streamer is incorporated for file backup. Optional printers have speeds of 150, 300, and 600 lines/min.

A group of precoded assembly language functions, claimed to execute all known business applications, makes up the program system. Users need not translate codes or symbols, since the system communicates in nontechnical terms. System features built-in user prompts as a replacement for instruction manual guidance for command construction.

The software was designed specifically to speed up productivity by simplifying program development. To execute a function, a user fills out a series of specifications forms. Sixteen forms encompass the range of Dimension One capabilities; generally 5 to 10 forms are required for any application. Forms specifications are entered into the system using a CRT, and are stored as a "link table" in a designated terminal work area or partition on disk. The link table is generated by a special PRO algorithm that selects and links in proper sequence all necessary routines from the Dimension One library within seconds to minutes after entry of specifications. A complete applications program, with documentation, results. Data quality assurance is established as an application is implemented to prevent user omissions or entry of errors.

Multi-application program instructions are in assembly language and are used directly. No assemblies, compiles, or interpretive routines are needed. Based on a totally structured, standard application format, the system is selfmaintaining. System maintenance or enhancement are not dependent on programming personnel continuityrestructuring of programs and updates are automatic.

The system has been under testing and debugging for three years prior to its recent release. The company estimates modifications/enhancements to be completed 200 to 300 times faster than on conventional systems. In addition, cost savings for startup applications programming are estimated at 90%. Over a typical 60-month period, savings could exceed \$150,000 in programming time. **Capro, Inc,** 12781 Pala Dr, Garden Grove, CA 92641.

Alternative to Apple II Pascal problems

The first commercial release of Modula-2 is aimed at offsetting Pascal programming limitations inherent in the Apple II. Modula-2, supplied by Volition Systems, is a high level programming language designed by Niklaus Wirth, creator of Pascal. It provides an alternative to assembly language, Pascal, C, and Ada for systems programming. Features of the language include modular structure, processes, separate compilation, dynamic array parameters, and low level machine access. In contrast to Pascal, which requires nonstandard extensions to handle tasks such as realtime programming, Modula-2 is a small language supplemented by library modules. Modules handle 1/0, strings, storage allocation, program loader, process scheduler, and math functions.

The language comprises a p-code interpreter this is upwardly compatible with the Apple Pascal interpreter, a fast, 1-pass compiler: a library management utility; and a standard module library. System requires a 64k-byte Apple II under Apple Pascal operating system. With minor implementation restrictions. the compiler accepts the entire language. Programs are compiled into p-code; separate compilation for up to 50 individually compiled modules per program is fully supported. Linking is not required; module binding is performed at runtime. Loader module enables programs to invoke other programs as procedures, with data sharing through imported modules.

Initial release provides access to the Apple Pascal file system and UCSD Pascal intrinsics via library modules. Releases planned for the future will include access to Pascal and assembly routines, facilities for creating interrupt driven device processes, and user definable execution error handling.

The company has targeted the language for the Apple II system to

transform it into a tool for larger industrial applications. Modula-2 is priced at \$550, quantity one. Updates and user supports via electronic mail are optional. Several Modula-2 configurations are planned for program development and turnkey applications. The company will assist in adapting the language to other hardware and operating systems. **Volition Systems**, PO Box 1236, Del Mar, CA 92014.

Low cost electronic mail system for HP/3000

ZAP/3000 electronic communications package for HP/3000 computers, from Infomedia Corp, is claimed to be the lowest priced mail system offered in the minicomputer marketplace. Messages to send, file, and transmit text are keyboard entered, processed by the computer, and sent to remote offices. The system has no distance limitations for remote sites. Communiques are automatically filed and can be retrieved according to sender, date, or subject.

Priced at \$2000, the software is approximately one-quarter the cost of the alternate HP/3000 compatible electronic mail system, the Jenny/3000. Single- or multiple-copies of messages are sent by ZAP/3000 in 3 postal style delivery classes. Registered delivery notifies recipient of pending messages and also confirms receipt to sender. Express messages are delivered automatically to the remote terminal, while normal messages alert the recipient without confirming receipt at point of origin. Five single-key commands are used for system operation. An adhesive strip, placed on the keyboard, converts any standard terminal into a ZAP/3000 terminal. The software runs on any HP/3000 CPU with 128k-byte memory and KSAM files, plus standard disk and asynchronous peripherals. Because ZAP/3000 is entirely software based, it allows immediate implementation of electronic mail service with existing HP/3000 and any ASCII terminals.

Jenny/3000, the company's upgraded electronic mail system for the HP/3000, is compatible with ZAP/3000. Any ZAP/3000 file can be transferred to Jenny/3000. Purchasers of ZAP/3000 who upgrade to Jenny/3000 are given \$2000 credit toward the upgrade. **Infomedia Corp**, 801 Traeger Ave, Suite 275, San Bruno, CA 94066.

Capro, Inc	Circle 265
Volition Systems	Circle 266
nfomedia Corp	Circle 267



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Sure, they both make terminals that work with computers from Digital Equipment Corporation. But you won't believe the differences between those terminals.

One has just a 12" display. The other has that plus a big, easy-toread 15" optional display (a must for 132 column operation).

One comes with only white phosphor screen. The other comes with your choice of white or green phosphor screens.

They both come with 80x24 displays. However, one offers 132x24 display format as an option, the other as a standard feature.

One offers bit map set-up legend. The other offers set-up legend in English.

One offers standard non-embedded attributes plus reverse video. The other offers that plus blink, bold, underline, reduced intensity, and protected fields.

One gives you line/character insert/ delete only as an option with printer port. The other gives you full editing and a printer port as standard features.

One has only USASCII and UKASCII character sets. The other

has six additional built-in, selectable international character sets.

One is the DEC VT 100 terminal. The other is the Lear Siegler ADM 36 terminal.

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IBM Personal Computer interface

Software support for the IBM Personal Computer enables access to std application programs running on IBM System/34 or /38, and allows the Personal Computer to become an intelligent terminal connected to these systems. Software allows users to access centralized data bases and applications, while maintaining local data and applications software on the Personal Computer. Software is an addition to the company's Gateway 34/38 communications system, a front end that runs on IBM series/1 minicom-



O Five paper drive combinations including top or bottom tractor drive and individual forms handler. O 200 cps. O 9-pin ballistic print head, 650 million character life. O Near letter-quality print at 100 cps. O Heavy-duty industrial design. O Five-input interfaces available.

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Cardinal's new 2170 is a rugged performer, tough enough to take anything a factory environment can dish out... yet sophisticated to the point of engineering genius.

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flipping a switch. Cardinal COMPUTER DIVISION

Another of the Cardinal Industries P. O. Box 151 Webb City, Missouri 64870 U.S.A. Phone: (417) 673-4631 puter. Gateway connects terminals to System/34 or /38, using any combination of local attachments, dial-up or leased lines, and public packet networks. Company's X.25 packet network interface is certified for operation with Datapac, GTE-Telenet, Tymnet, and Uninet networks.

Intelligent terminal support for the Personal Computer requires min storage configuration of 64k diskette, monochrome display, and asynchronous communications adapter. Gateway performs protocol conversion between IBM SNA and x.25 protocols, and between 5251 and 3101 display formatting commands. Multiple System/34 and /38 computers can be connected to a single Gateway front end, and accessed by any terminal connected to the Gateway. **Systar Corp**, 1762 Technology Dr, Suite 208, San Jose, CA 95110. Circle 268

Graphics software for Apple II

GRAPH functions either as standalone or direct interface with the company's personal filing system (PFS) data bases or VisiCalc to produce presentation quality bar, line, or pie charts. Up to 4 line and/or bar graphs can be displayed on a single set of axes; bar graphs can be stacked or comparative. Other features include automatic formatting, scaling, legend labeling, and pattern fill. **Software Publishing Corp**, 1901 Landings Dr, Mountain View, CA 94043. Circle 269

Forth based language for TRS-80

OmniFORTH language, based on fig-FORTH and 79 Standards, runs on TRS-80 model III and combines structured programming, 31-char names, virtual memory, stack organization, compiler, assembler, and file system into an extensible macro-like language. Organized as a word dictionary to reduce memory requirements, language allows user defined words to extend vocabulary of specific applications. Words are compiled on entry into code ready for immediate test and execute almost 20 times faster than BASIC. It supports coding time critical routines in assembler for fast response. Language can also produce programs smaller in size than assembler. System contains interactive OmniFORTH compiler, Z80 assembler, file system, and full-screen video editor. Package requires 32k memory and 1 disk drive. Interactive Computer Systems, Inc, 6403 DiMarco Rd, Tampa, FL 33614. Circle 270



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3-D software

SOFTWARE

SYSTEM COMPONENTS/

Technical information processing system TIPS-1 geometric software is CAD/CAM designed and serves as geometric modeler of mechanical parts. Software uses an APT-like shape description language for defining solid objects. Applications routines include graphics, design analysis, and manufacturing. System consists of 9 basic geometric elements; various regenerated solid objects are also offered. Program is written primarily in std FORTRAN. Hardware requirements include IBM 370/168 or its equivalent, and Tektronix 4014 or similar graphics terminal. System includes 9-track, 1600-bpi magnetic tape and documentation. Computer Aided Manufacturing-International, Inc, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Circle 271

Portable graphics development software

GSS-CORE portable graphics application development software runs on most major microcomputer/minicomputer operating systems, including CP/M, UCSD-p, UNIX, and RT11. Software is a 2-D graphics subroutine library, compatible with Level 1 of SIGGRAPH Core Standard. It is both computer and device independent, guaranteeing portability across a variety of computers, CRTS, printers/plotters, and film recorders. Programmer can use software to draw lines, create objects, add text and color, create graphs and charts, and analyze data. Prices range from \$300 for singleuser to \$1500 for multiple-user systems. Graphic Software Systems, Inc, PO Box 673, Wilsonville, OR 97070. Circle 272

DEC compatible communications package

Version 16 of DIALUP, an asynchronous communications package running under RSTS/E on PDP-11 and under ROSS/V RSTS/E simulator on VAX, uses std asynchronous terminal line to link host to remote computer via telephone or null modem connection. Package supports user directed dialing through automatic calling units, and transmission of ASCII text files to and from remote system. Under remote system RSTS/E or VMS with (continued on page 301)



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612/02

ROSS/V, block mode transmission of binary files with CRC16 block checking, block level retries, and preservation of attributes are supported. Binary file transfer module, written in machine language and supporting command language, is bootstrappable to remote system. Machine language reduces user mode time by a factor of 6 and overall CPU time by a factor of 2.5. Support is added for VADIC multiline auto-dialers, both DN11 and RS-232 controlled. Rudimentary command language allows branching on errors, chaining to/from other programs, waiting with retries, and definition/execution of macros that specify complex sequences of DIALUP commands. Evans Griffiths & Hart, Inc. 55 Waltham St, Lexington, MA 02173. Circle 273

Pascal/cross compilers

Pascal development system, built upon C compiler and libraries, provides complete and portable software for Pascal programming on VAX-11, PDP-11, LSI-11, MC68000, 8080, and Z80 computers. Both native compilers and cross compilers are available, running under VMS; UNIX V6, V7, and 32V; Idris-R11, -S68K, and -B80; RSX-11M; RT-11; IAS; RSTS-E; VERSAdos, CP/M, and CDOS. Cross compiler packages include native mode code generator. Pascal, C, and assembly language modules can be intermixed with std calling sequences. Language libraries provide approximately 100 functions for controlled storage allocation, formatted 1/0, data conversions, and string manipulation. Supporting portable libraries are os specific interface library and machine library called by compiler to perform 16- and 32-bit arithmetic, and 64-bit floating point arithmetic. Whitesmiths, Ltd, PO Box 1132 Ansonia Station, New York, NY 10023. Circle 274

Test package software

Advanced Test Package ATP software OS enhancement for the 1731 linear IC test system features op amp test software subsystem for testing of high volume, single supply op amps. Software also enhances test flexibility for split supply device, and provides greater programming flexibility in defining common mode voltage (VCM) conditions. Programmable dc loop settling delay feature allows full software control over hardware settling of dc test loop in op amp testing. Enhanced voltage regulator test capability coupled with modifications to 1731 hardware allows users to program 1/0 differentials of greater than 10 V while testing at load currents greater than 60 mA. Streamlined test algorithms and IEEE communications package provides increased communications capabilities in remote test station/host processor configurations. Software package is fully retrofittable on all installed 1731 test systems. **GenRad, Inc,** 170 Tracer Lane, Waltham, MA 02254. Circle 275

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of Intel Corp.

Intellec compatible cross assembler for NSC 800

SYSTEM COMPONENTS/ DEVELOPMENT SYSTEMS



SPICE, an in-circuit emulator for National Semiconductor's 800, is fully compatible with Intel's Intellec development system. Intellec compatibility makes available a powerful command set with PL/M, FORTRAN, BASIC, and Pascal, as well as easy hardware/software debugging and efficient high level programming in a stable environment. RELMS NSC 800 SPICE pod, measuring 11" x 6.75" x 2" (28 x 17.15 x 5 cm), combines the ability to perform symbolic debug with a relocation register in memory that supports modular coding and a patented relational Break Region. Unit does not require additional software packages, links, or time delays to communicate with Intellec. Relational Memory Systems, Inc, PO Box 6719. San Jose, CA 95150. Circle 276

Universal EPROM/E²PROM programmer



System 90 programs all popular 24-, 28-, and 40-pin, 5-V MOS EPROMS and E^2 PROMS, and will support future MOS devices through 64k x 8 bits via user installed field updates. Basic system includes M980 control unit with 8k-byte buffer memory, PM9080 personality module, PA28-80 pinout adapter, M304 interface adapter, and 9202A carrying case. All 24- and 28-pin devices are supported by basic system; other package configurations such as 40-pin chips are accommodated using optional pinout



64 Kbytes

Unit Qty.

\$1275 each

SYSTEM COMPONENTS/ DEVIELOPMENT SYSTEMS

adapters. Selection of PROM type is via 2 rotary switches. An 8-digit alphanumeric display shows manufacturer's part number for PROM selection. Programmer features separate master and copy sockets to allow 1-step duplicating and to prevent data in master PROM from being accidently altered. Prior to PROM programming or duplication, system automatically tests PROMs in copy and master sockets to detect shorted lines, excessive current, and incorrectly inserted PROMs. Following address programming, PROM is read at its high and low V_{CC} limits and data are compared to source. Programmer with 8k-byte buffer memory is priced at \$4450; system with 16k-byte buffer memory is \$5050. Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940. Circle 277

Prototyping system for 68000

MICRO 68000TM self-contained trainer/ prototyping system for the 68000 microprocessor comes with 6-A switching power supply, Versabus 68000 computer board, hexadecimal keyboard, and LED display. The 16k-byte memory can be any combination of ROM or RAM, and includes keyboard monitor. Monitor allows 68000 machine code instructions to be entered into memory, and programs to be debugged and run. Expanded display board shows entries in hexadecimal and binary format. Computer board contains two RS-232 ports and 32 bits of parallel 1/0. All Versabus connections are available externally for test and measurement. Price is \$985. Computer System Associates, 7562 Trade St, San Diego, CA 92121.

Circle 278

In-circuit emulation package

10-MHz in-circuit emulation support package for the 8086 microprocessor also implements map, break, and trace functions for 8087 and 8089 coprocessors. Designed for ECL-3211 development systems, package provides all hardware/ software necessary for software development and simulation, and full-speed, no-wait-state in-circuit emulation for all 8086 modes and models. Included are target interface pod, chip driver software and disassembler, macro crossassembler, linker, and universal PROM programmer utility. Queue management (continued on page 304)



- 18-bit Addressing
- Compatible with 11/2 and 11/23



board, supplied separately, can also be used with chips (such as 8088) with queues to a max depth of 16. Board allows individual breakpoints to be activated at top or bottom of queue.

System is functionally transparent to the target and does not steal any user interrupts, stack, or address space. Fullspeed 8086 emulation is handled in both max and min operation modes; breakpoint, trace displays, and pin designations are automatically altered when changed from one mode to another. For 8086 target systems that also include coprocessors, package provides byte resolution map/offset functions over full 32-bit mapping range for all coprocessors implemented; realtime trace functions are performed for coprocessors and all DMA operations. Software options permit examination and display of internal 8087/8089 registers. Eight 78-channel tri-condition prioritized hardware breakpoints are std, breakpoint recognition is performed in 60 ns. Four software controlled logical switches permit concatenation of multiple breakpoints. Emulogic, Inc, 3 Technology Way, Norwood, MA 02062. Circle 279

GOMPUTERS

Array processor with twin arithmetic processing units

MAP-400 array processor system for high throughput and realtime signal processing applications provides arithmetic processing at 24M floating point operations/s. 1024-point complex FFTs can be executed on continuous basis at rate of 2.7 ms/FFT. All arithmetic is performed in 32-bit floating point format, providing wide dynamic range and eliminating scaling problems encountered with fixed point or block floating point formats. System is upward compatible with MAP-200/300 product line, incorporating all operational, utility, and diagnostic software.

Array processor contains internal CPU, multiple independent memory buses that accommodate memory speeds of 170, 300, and 500 ns MOS, and selection of peripheral I/O interfaces for digital devices, A-D, D-A, and remote storage devices such as disk and bulk memory. Twin APUS operate in parallel without cross-interference, providing 2 to 1 improvement in processing speed over the MAP-300. System interfaces to most popular 16-and 32-bit minicomputers and superminicomputers. Basic configuration includes 16-slot chassis with selfcontained power supply, 128k-byte program memory, and operational software package with array function library. CSP Inc, 40 Linnell Circle, Billerica, MA 01821. Circle 280

Floating point processor and cache memory

Performance enhancement board PEB contains cache memory and floating point processor on single 16" x 16" (41- x 41-cm) PCB. Board is software and hardware compatible with the company's distributing operating multi-access interactive network (DOMAIN) computational nodes, and is available as field or factory installed. Performance improvements range from 50% to 400% over currently running user application programs, depending on instruction mix. Cache memory acts as high speed buffer between main memory and central processor. Buffer reduces average memory cycle time, allowing processor to spend less time waiting for instruction and data fetches from memory. The 4k-byte write-through cache uses 2-way setassociative structure and retains least recently used information to achieve cache "hit-rate" of approximately 90%.

Floating point processor uses 2900 bitslice technology and conforms to proposed IEEE floating point standard. Processor implements single- and double-precision floating point arithmetic functions, register-state save/ restore, and polynomial evaluation primitive. Typ execution time is 2.8-ms single-precision addition to 15.5-ms double-precision division. Apollo Computer Inc, 19 Alpha Rd, Chelmsford, MA 01824. Circle 281

Fault tolerant process control system

PCS-300 Can't-Fail process control system operates continuously through tripleredundant microprocessor based logic modules, triplex process interfaces, and peripherals that can be triplicated depending on application needs. Control computer modules provide memory expandable from 64k to 1M bytes in any mix of RAM, ROM, and EPROM.

Disk and CRT terminal interface are provided. Compatibility with Intel's MULTIBUS gives access to a variety of *(continued on page 306)*

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Our Media Is Our Message 5201 Patrick Henry Drive Santa Clara, CA 95050 * \$4.00 represents Dysan's suggested retail price for a one-sided, single density 8" diskette, packaged ten to a box. Minimum total cost of ownership = \$186.50 * \$182.50 represents the cost of data loading (approximately 22 hours at 11,106 keystrokes/hour at a labor cost of \$8.23/hour), based on 1981 Data Entry Management Association (DEMA) National Averages. communications/controller boards. Analog and digital 1/0 eliminate need for external thresholding and capture of pretrip histories for later analysis. System is fully software supported.

System technology uses a hardware and software approach to fault tolerance. It detects failure, corrects or masks errors, and reports failure to operator. System elements are isolated via read only communication links to prevent malfunctions from propagating to unaffected parts of the system.

At video programmer's graphics display, users visually construct ladder logic diagrams of control algorithms; special keyboard contains a set of ladder management keys. Video programmer can be used as both offline programming system and online system control console. Keyswitch and password prevent unauthorized access to system. **August Systems, Inc,** 2757 19th St SE, Salem, OR 97302. Circle 282

Array processor for MULTIBUS systems

Micro number cruncher SKYMNK-M for MULTIBUS microcomputers is the latest model in the SKYMNK family of programmable, high speed, 32-bit floating point array processors. The array processor is packaged on 2 SBC modules that plug directly into MULTIBUS backplane. System features 1M floating point operations/s; 32-bit floating point arithmetic with IEEE std format: 48-bit extended internal precision; and real, complex, and integer arithmetic instructions. Processor shares memory with host and is directly addressable up to 16M bytes. Vector subroutine library of FORTRAN callable math routines includes processing functions such as FFT, convolution/correlation, and thresholding. Software support under MP/M-86 operating system is included. For application program development, SKYMNK-M simulator is optionally provided. Sky Computers, Inc, John St, Lowell, MA 01852. Circle 283

Dual-system computer

System 83/computer system employs UNIX version 7 operating system, delivers multitasking minicomputer capability, and is configured around the MC68000 microprocessor. Computer is IEEE 696/S-100 compatible. System executes approximately 1M instructions/s. CPU

provides 16-bit data paths and 32-bit internal architecture. It supports up to 16M bytes of directly addressable memory. With memory boards, up to 4M bytes can be resident in enclosure. OS enhancements include c-shell, visual editor, and c compiler, allowing combined object code modules. Western Electric System III UNIX will be ported to the system during first half of 1982. Optional languages will include full FORTRAN 77 compiler and ISO std Pascal compiler with most UCSD enhancements. Also planned for 1982 are GSA certified COBOL compiler, Ada compiler using full DOD certified Ada subset, and DEC BASIC+. Main memory is provided by dynamic 256k-byte RAM board with parity. Both single- and double-density and 1- and 2-sided, 8" disk drives, and 8" Winchester drives are available. ADCs and DACs, and output current controller boards, can be added. Dual Systems Control Corp, 720 Channing Way, Berkeley, CA 94710. Circle 284

INTEGRATED GIRGUITS

Low cost, full-featured alphanumeric terminal controller in 4 LSI chips

When combined with standard CPUs, memory chips, and TTL, a 4-chip set can implement many CRT terminal functions with as few as 15 IC packages-half the number normally required to complete a full-featured microprocessor based terminal. Mask programmable 2670 display character and graphics generator provides up to 256 graphics chars, converting char and line address data into dot patterns for raster scan displays. Programmable keyboard and communications controller, 2671, is an MOS LSI circuit. Mask programmable ROM provides 4 levels of key encoding; the communications section is a UART with baud rate generator. Programmable video timing controller, 2672, generates operating modes, display formats, and timing profiles for use in raster scan display systems. High speed timing functions are handled by 2673 video attributes controller, a bipolar LSI circuit also designed for raster techniques.

Typ configuration incorporating nonencoded electromechanical or capacitive keyboard and raster scan CRT monitor will furnish a low cost monochrome terminal with features often found only on high cost designs. In 100-quantities, the 2670 28-pin plastic DIP is \$7.30, \$9.30 ceramic; other chips are available in 40-pin versions. 2671 is \$13.65 (plastic)/\$16.65 (ceramic); 2672 is \$16 (plastic)/\$19 (ceramic); and 2673 is \$20.40 (plastic)/\$23.40 (ceramic). **Signetics Corp**, 811 E Arques Ave, Sunnyvale, CA 94086.

Circle 285

High performance bus interface

Am29800 family of 8-, 9-, and 10-bit bus interface devices follows common pinout pattern-left inputs, right outputssaving layout time and board space. Ground pins and Vcc are standardized within family. The 24-pin, 300-mil members are fabricated using propietary IMOXTM ion implanted oxide isolated process, resulting in smaller die sizes and greater speed. Devices' tpp of 7.5 ns typ matches speed of multiple IC register configurations. Features include 48-mA commercial IOL and 32-mA MIL-IOL for optimum bus driving capability; high capacitance load capability; and low capacitance I/Os. ICs are screened to MIL-STD-883, and meet requirements of INT-STD-123, 0.2%.

Am29821 and Am29822 are buffered, 10-bit wide versions for use in 20-bit wide bus structure applications. The 9-bit wide Am29823 and Am29824 buffered registers feature clock enable (\overline{CE}) and clear (CLR) functions for parity bus interface in high performance microcomputers. Am29825 and Am29826 are std 8-bit buffered registers with all Am29823/Am29824 controls, plus multiple enables for multi-user control of interfaces. Devices can also be used as output port requiring high IOL/IOH. Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. Circle 286

Octal bus transceiver with ISO CMOS integrated circuits

G74SC245 octal bus transceiver is pin for pin compatible with std 74LS245 packages. Unit has 3-state outputs and uses noninverting buffers. Circuit provides asynchronous 2-way communication between data buses, and offers high speed performance I/O clamping. Propagation delay of 22 ns is typ for low to high outputs, and 25 ns is typ for high to low inputs. Transceiver comes in 20-pin cerDIP package. Device requires 5-V power supply and operates over 0 to 70 °C. GTE Microcircuits Div, 2000 W 14th St, Tempe, AZ 85281. Circle 287

LSI-11 System Boxes and Box Systems Functionality Versatility Reliability Cost Effective MDB makes the difference!

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MDB Orange, California 92665 714-998-6900 SYSTEMS INC. TWX: 910-593-1339

Circle 208 for more information.

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AYDIN CONTROLS offers a complete line of color and monochrome CRT display products, ranging from monitors to desktop terminals to standalone display computers and related software products for high resolution graphic and image processing applications.

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Low power Schottky components

Octal bus transceiver 74ALS245 is a 20-pin advanced low power Schottky (ALS) pin for pin functional equivalent of a std 74LS245 device. The 2 ALS parts have max low to high and high to low propagation delays of 9 ns. Max power dissipation is 315 mW. Parts operate in temp range of 0 to 70 °C, with a V_{CC} that can vary $\pm 10\%$ into a load of 50 pF.

74ALS568/569 synchronous 4-bit up/down counters with 3-state outputs have low to high propagation delay time of 12 ns into a 50-pF load. Parts require a typ I_{CC} of 20 mA. 74ALS568 is a decade counter, while 74ALS569 is a binary counter. Both devices feature asynchronous or synchronous clear, and buffer type outputs that directly drive the bus lines.

74LS18/19/24 Schmitt trigger, positive NAND gates and inverters with totem pole outputs feature different threshold voltages and low input currents. Units can be driven from the same line without excessive loading. Devices are temp compensated and can be triggered from the slowest input ramps and give clean, jitter-free output signals.

74LS169B synchronous 4-bit up/down counter features isolation for decode feedback, and additional drive capability. High to low propagation delay is 25 ns. Texas Instruments, Inc, PO Box 202129, Dallas, TX 75220. Circle 288

Monolithic 16-bit DAC

HI-DAC16, a 16-bit monolithic current output DAC is offered as HI-DAC16B and HI-DAC16C versions, with 2 accuracy grades for commercial temp range of 0 to 75 °C. Both versions provide 16-bit resolution and CMOS and TTL compatibility via advanced dielectric isolation (DI) technology. DI advantages include low leakage currents, elimination of parasitic SCRs to free latch up, and low internal parasitic capacitances for fast rise and fall times. HI-DAC16B meets specs for 16-bit monotonicity at room temp and 15-bit monotonicity over temp. Integral nonlinearity specs provide a limit of $\pm 0.0045\%$ FSR max relative accuracy over temp (14.5 bits of

relative accuracy). HI-DAC16C provides 15-bit monotonicity at room temp and 14-bit monotonicity over temp. Integral nonlinearity specs are $\pm 0.009\%$ FSR max relative accuracy over temp (13.5 bits of relative accuracy). Units are available in 40-pin cerDIP. Harris Corp, Semiconductor Group, PO Box 883, Melbourne, FL 32901. Circle 289

8- x 8-bit multiplier

Our \$109 LPB* looks and works like the other

Industry std multiplier 54/74S558 performs double-length 8- x 8-bit operations with 16-bit results in 60 ns, worst case. The Schottky multiplier also has die size of 18,720 mil². Device is a high speed modified Cray multiplier that multiplies two 8-bit signed 2's complement or unsigned numbers, and generates 16-bit signed or unsigned products. It can be used in serial or parallel configurations and can be expanded in any direction in 8-bit increments. A 56 x 56 fully parallel multiplication can be performed using 34 multipliers. Product outputs are 3-state and are controlled by (continued on page 310

EUROPEAN MARKET FOR COMMUNICATING TEXT TERMINALS

Frost & Sullivan has completed a 289-page report of the Communicating Text Terminal market in Western Europe. Market forecasts are developed for the 1981-1986 timeframe, in terms of device shipments and dollar value, within the major European country blocs for these main product types: telex terminals, communicating typewriters, teletex terminals and communicating word processors. Annual shipments of text capable (data terminals and microcomputers) terminals are also forecast through 1986 by country. The demand in the different market sectors for the classes of service that communicating text can provide are examined. Communications and terminal component technologies are assessed. Company profiles are provided for the leading suppliers. The experience of the users of communicating text terminals, and the ways in which their successes and disappointments have caused them to change their plans for exploiting these devices are described. The major environmental factors in terms of national economic and regulatory constraints, the plans of the PTTs and the attitudes of prospective users are considered.

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assertive low output enable, allowing several multipliers to be connected to parallel bus, or to be used in pipelined system. Packaged in std 40-pin cerDIP and requiring a single 5-V supply, multiplier is available as 60-ns commercial device 74S558, and as 70-ns MIL version 54S558. **Monolithic Memories**, 1165 E Arques Ave, Sunnyvale, CA 94086. Circle 290

Configurable gate array

CGA 300 Schottky TTL configurable 300-gate array features dual-layer metalization, 6-ns typ gate propagation delays, and 56 max I/O buffers. Device is available in cerDIP packages or leadless chip carriers. Screening and MIL-STD-883 classes B and s specified devices are also available. Flexible development interfaces are offered. Users can input logic diagram, critical timing path definitions, and truth table. Users can optionally choose to perform placement, routing, and digitizing from furnished array design specification. The company implements circuit design, generates necessary tooling, and supplies 25 assembled and tested prototypes as part of the development phase. **Raytheon Semiconductor**, 350 Ellis St, Mountain View, CA 94040. Circle 291

TEST & MEASUREMENT

Data transmission test set

Model 3000E of the Range Rider line of bit error rate test sets for data communications channels operating up to 10M bps features built-in EIA RS-232, RS-422/423, CCITT V.35, current Bell 301/303, MIL-188, and TTL interfaces. Portable unit provides individual displays of errored and total seconds, errored and total bits, and total bits with autoranging on all counters, and 65,535-bit pseudorandom test pattern. Operating in half- or full-duplex modes, test set has 10 LED monitor key interface signals. Proprietary technique allows fast loss of sync detection within 20 bits and does not affect error count. Unit has internal clocks of 40.8k, 48k, 50k, and 56k bps for external timing. Model 3000E operates with IDS model 2910D printer to provide permanent record of test results. **International Data Sciences, Inc**, 7 Wellington Rd, Lincoln, RI 02865. Circle 292

Apple compatible digital memory oscilloscope

Dual-channel, dc to 50-MHz digital memory oscilloscope model 85 fits as a module into Apple II and Apple II Plus microcomputers, and is compatible with Apple peripherals, added memory, and printers. Device uses display and keyboard as oscilloscope screen and control panel, the computer for waveform processing, and disk memory for waveform storage. Oscilloscope performs std laboratory functions such as signal averaging and DVM readout. Program development in BASIC or machine languages uses 8k of Apple memory. Unit is user programmable for FFT. auto- and cross-correlation, power density spectra, and integration and differentiation. Instructions can be inserted in hardware controlled software. Program development subroutines are available.

Unit acquires data through probes or cables connected to module at back of computer. Fastest sweep speed is 10 ns/div; at 1 ms/div and slower, scope operates as realtime A-D conversion system. Waveforms are displayed on software generated 8 x 10 division graticule. Graticule is erasable for easy to read display, and introduces no parallax or distortion errors. Cursor provides DVM readout for any specified point on displayed waveform.

User selects waveforms to store on disk and directs control functions through single-keystroke commands. Control settings can be saved on disk: keyboard is also reprogrammable. Waveforms are saved in text or binary format, along with 8 associated parameters. Computer software supports hardcopy output of waveform display. Unit requires Apple Disk II and display, 48k memory, and DOS 3.3. Operating software resides on 5.25" floppy disk. Northwest Instrument Systems, Inc, PO Box 1309, Beaverton, OR 97075. Circle 293

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CIRCLE 178



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COLLA DEDITE

Apple II compatible computer



Franklin ACETM 100 personal computer features 64k of RAM with 350-ns access time and hardware/software compatibility with the Apple II system. Computer has full upper/lowercase keyboard and char generator. Keyboard includes 12-key numeric pad, alpha shift lock key, and keys with VisiCalc designations. Normal, inverse, and flashing chars can be displayed. Full cursor control is provided with protected screen feature. Unit is plug compatible with the Apple system; all peripherals designed for Apple II will also operate without changes on ACE 100. All Apple II programs run on the computer without modification. The 6502 microprocessor based system operates at 1.022-MHz clock rate. Power requirement is 115 V, 60 Hz, 65 W. Fully compatible 5.25" disk drive is also available. Unit measures 19" x 5.5" x 21" (48 x 14 x 53 cm). Computer is retail priced at \$1595. Franklin Computer Corp, 7030 Colonial Hwy, Pennsauken, NJ 08109. Circle 294

Z80A based microcomputer

Datavue 80 desktop and portable Z80A based computers are available in 9 configurations, combining floppy disk and Winchester drives. System has 64k bytes of RAM, along with 4k bytes of EPROM. Two RS-232-C serial ports and two 8-bit parallel I/O ports are provided. Each model utilizes CP/M OS and microprocessor operating at 4 MHz. The 100 series models have single 5.25" floppy disk with portable enclosure. 200 series models operate as full-function desktop microcomputers with dual-floppy 5.25" drives, available in 0.25M-, 0.5M-, and 1M-byte capacities. 300 series models have one 5.25" floppy drive and one 5.25" Winchester drive. Floppies are available in 0.5M- or 1M-byte densities; Winchesters are either 6M or 10M bytes. **Datavue Corp**, 1911 22nd Ave S, Seattle, WA 98144.



Circle 295

U.L. CLASSIFIED Data Processing Plenum Cables

HITEMP WIRES manufactures the complete spectrum of Plenum Cables for the Electronic and Data Processing field. In the design of Office Network, Word Processing, Data Communications, Energy Management Systems, etc. the N.E.C. allows for the installation of U.L. classified cables in air handling plenums without conduit. When specifying or installing Data and Audio/Video cables think of HITEMP WIRES, the source for all your Plenum Cable requirements.



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CIRCLE 181

Severe environment data acquisition system

Microprocessor based remote process system for "fault proof" data acquisition and control between process sensors and host computer, Model 600 Process MasterTM provides continuous data acquisition and control operation in hostile applications. System combines distributed processing, built-in redundancy, and user friendly software. The intelligent subsystem is installable near process sensors to eliminate extensive cabling and test equipment. System interconnects with process sensors and contact points utilizing features such as

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AC 39



signal conditioning, sensor checking/ compensation, continuous data validity testing, limit checking and alarm, data integrity tagging, multilevel sequence of events processing, automatic cable/ interconnect fault verification, high voltage protection, high noise rejection, and data fault analysis. Continuous nonstop processing confirms that a min of data and controls are transmitted to and from host computer and ensures that data and controls are correct and fault proof.

AIDE software, resident in both user's host computer and model 600, allows conversational setup and operation. Software permits system operation from host workstation by setup prompts based on process 1/0 configuration. Scan, log, alarm, and direct digital control operations are automatically compared to preset restriction and verifications before system is initiated and during all online changes or upgrades. AUTECH Corp, 1301 W Copans Rd, Pompano Beach, FL 33064. Circle 296

PERIPHERALS

Filmless CCD array camera



C322 filmless CCD array camera resolves visual field with 4.5M pixels (1720 x 2592 x 8), sensitivity of 0.4 μ J/cm² at saturation, and dynamic contrast range of 500:1. Eliminating blooming, burning, gain, and offset drift problems associated with vidicon tubes, CCD array sensing provides 2.5 times more sensitivity than previously used photodiodes. Camera head is 7.13" x 5.36" x 4" (18.11 x 13.61 x 10 cm). Camera accepts most bayonet or screwmount 35-mm camera lenses. High resolution provides quality imaging for teleconferencing, photocopying, facsimile, electronic mail, micrographics, OCR, CAD/CAM, computer graphics, and other applications requiring image recognition, (continued on page 317)

CIRCLE 182

WHICH TWIN HAS THE TANDBERG? The only true ergonomic terminal in the world.

If your terminal operators are getting eyestrain, headaches, stiff necks and bad backs, chances are you haven't yet heard of the Tandberg Data Terminal. Tandberg Data manufactures the only terminal in the world which meets the stringent requirements of the German ergonomic standard. This means Tandberg terminals don't just tilt-they tilt, swivel, raise and lower to fit all size people, in any room light at any angle. Our keyboard doesn't simply detach-it's a low profile work of art so slim it can be used in complete comfort on a standard desk. And the non-glare keys are shaped for fingertip efficiency.

The luminance from our 15 inch "green" screen is adjusted to the 1:4 ratio with surrounding light which is needed to assure human comfort and health. The screen is treated to reduce glare and a unique feature, Equilite, displays both horizontal and vertical lines with equal intensity assuring readability.

The Tandberg terminal is designed for the office of the future with a beautiful, compact housing and a finished back with no unsightly cables. When you see the Tandberg you'll realize why no other terminal deserves to be called ergonomic.

And Tandberg's operating features are just as complete. The Tandberg terminal is equipped with "soft-switches" which allow operation modes to be stored in non-volatile memory (EAROM) and changed from keyboard or line. PUSH-keys let strings of commands be implemented at the touch of one button reducing time and errors. It's an operator's dream.

TANDBERG DATA Tandberg Data, Inc.

The Tandberg TDV 2200 family is offered in different models emulating the DEC VT100 and VT52. Honeywell-Bull Questar and VIP 7255, Datapoint 3600 and 8200, Computer Automation CRT II, IBM 3101, Data General 6053 and D200 and others. An advanced performance model is also available for the development of application-tailored OEM terminals. So don't put up with a pain in the neck. You can increase efficiency, productivity and operator morale with a true ergonomic terminal-the only true ergonomic terminal in the world from Tandberg Data. Call or write today to: TANDBERG DATA, INC., P.O. Box 99, Labriola Court, Armonk, New York 10504. Telephone: (914) 273-6400 Telex: #137357 Tandberg Armk.



Introducing the first 50 nsec 12x12-bit multiplier.

TRW's OMICRON-B[™]* makes the MPY112K the fastest (20 MHz – video rate) 12x12-bit multiplier available.

The 48 pin DIP VLSI multiplier gives you a combination of more usable board space and higher speed multiplication than you've ever had before.

You can multiply in two's complement or unsigned magnitude format, and you get a 16-bit product, perfect for video systems where real time digital signal processing is required at very high data rates.

All inputs/outputs are registered and TTL compatible, of course. (After all, TRW invented TTL.) Threestate output drivers, single + 5V supply, and the price is right: just \$105 in 100s.



Now in stock at Arrow Electronics and Hamilton/Avnet. For immediate information about the new MPY112K 12x12-bit parallel multiplier, call us at (714) 457-1000 or return the coupon.

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State	Zip	CD-5

* OMICRON-B[™] is TRW's advanced 1 micron VLSI bipolar process, and is the first 1 micron process commercially available.



storage, or reproduction. Greater sensitivity permits camera use with lower illumination. Greater dynamic range allows wider choice of aperture settings without loss in contrast.

Camera functions as fronted electrooptical imaging subsystem that scans text, visuals, or objects to supply corrected digitized video. Camera can be used with the company's camera control unit to form a standalone electronic camera system. Cabling carries dc power to camera and multiplexed picture data/control signals between camera and host.

When picture cycle is initiated, motor drive carries solid state array of charge coupled devices (CCDs) across image field. During picture scan, captured picture elements are transmitted as 8-bit parallel multiplexed picture data (with synchronization clocking) to host at up to 2M bps. Optical lens characteristics and focus setting selected determine viewable copy size and camera to subject distance. Using 35-mm camera lens, an imaged 8.5" x 11" (21.6- x 28-cm) page has effective resolution in object plane of 200 points/in. Options include illuminator, illumination compensator, hardcopy unit, and power supply. Camera head, without illuminator or power supply, is \$7850 quantity 1. Complete standalone camera systems are priced from \$13,700. **Datacopy Corp**, 1070 Meadow Circle, Palo Alto, CA 94303. Circle 297

Cursor control pad

E232 cursor control pad has controller that outputs stream of high resolution finger position coordinates compatible with highest resolution graphics displays. Host processor interprets coordinates to provide specific cursor control, allowing more natural cursor control than with joysticks, trackballs, or motion keys. Pad response can also be made to emulate joystick or trackball, or provide special control techniques unique to application. Uniform resistive substrate to which low voltage is alternately applied along orthogonal axes when pad is touched is primary pad element. Finger pressure causes deformable cover sheet with conductive layer to contact resistive substrate, and voltages picked off at point of contact are digitized to provide coordinates of centroid area depressed. Output is analog and continuous over entire surface; pad provides infinite resolution, with actual resolution determined by ADC in controller. Low voltages and low frequencies used ensure low emi emittance. **Elographics, Inc**, 1976 Oak Ridge Turnpike, Oak Ridge, TN 37830.



Circle 298



Intelligent desktop digitizer



Image Data Tablet System provides direct computer digitizing access through handwritten entries, sketches, and alphanumeric touch table. Resembling 0.25'' (0.64-cm) thick desktop blotter, tablet accepts documents onto $11.5'' \times 11.7''$ (29.2- x 29.7-cm) writing area and enters data into host computer or system's optional microprocessor. Any layout, including NCR and multiple copies, can be entered, with hardcopy original identical to computer entry produced. Optional hardware/software package document manager allows con-

tinual offline activity. Built-in document manager concentrator enables other peripherals to be channeled into host computer. With optional tablet concentrator, 11 tablets can be clustered to 1 system, or 11 RS-232-C/V.24 interface peripherals accepted. With associated video screen, tablet combines handprint recognition and digitizing functions to accept and display fine line and block graphics inputs. Teletype compatible touch table expands simultaneous functions to include keyboard operations, simple calculations, and user selectable programming keys. All inputs are converted to ASCII code for transmission via RS-232-C/V.24 interface at switchselectable rates of 110 to 9600 baud. Character recognition is through software program in associated microprocessor. Eleven tablets can be clustered to 1 microcomputer having disk storage. Tablet can be put online to micro, mini, or mainframe systems directly or via telephone lines. System with tablet, CRT, and microprocessor controller is approximately \$4000; availability is 40 days. Total Technical Services, Inc., 341 Cobalt Way, Suite 208, Sunnyvale, CA 94086. Circle 299



Multiport terminal



Multiport communications terminal 7700 is designed to concurrently prepare, transmit, and receive messages via TWX, TLX, DDD, and PTL protocols. Terminal has operator friendly message editor that incorporates complete set of text manipulation facilities, reducing time involved in message preparation. Message editor includes automatic word wrap, paragraph formatting, screen scroll, text insertion/deletion, and search forward/backward. Dialing, answerback verification, and transmission are automatically performed in background while new messages are prepared on CRT screen. Screen displays chars in 7- x 9-dot matrix using 25-line x 64-col format. Terminal is configured with up to 80k of memory and integrated diskette for additional storage. Also included is dot matrix impact printer with 30-cps min print speed. Carterfone Communications Corp. 1111 Mockingbird Lane, Suite 1400, Dallas, TX 75247. Circle 300

Graphics video generator

VMD-05 graphics video generator for DEC LSI-11, 11/2, and 11/23 microcomputers has 3 selectable resolution: 1 or 2 channels of 256 x 256 or 512 x 256, or 1 channel of 512 x 512. Output is composite video for either U.S. (60-Hz) or European (50-Hz) TV sync. Each channel has 2 outputs, allowing dual-channel version to drive up to 4 video displays or hardcopy devices. Full graphics display capability is provided, with each display stored in onboard MOS RAM and each point independently addressable. Single instruction software commands and x-y addressing save CPU time and increase system efficiency. PICPAC software package is available for RT-11 and RSX-11 operating systems with full set of char/ graphics routines. Generator requires 1 dual-slot in an LSI-11 systems. Mennen Medical Inc, 10123 Main St, Clarence, NY 14031. Circle 301



Emulex introduces the SC750 disk controller. And suddenly your VAX-11/750 disk drive options are wide open. It's the only DEC alternative.

You can mix brands. Mix storage capacities. Mix media types. All working off a single controller.

Better yet, the SC750 gives you all of this flexibility along with maximum system performance and media compatibility.

Our new controller is fully embedded and designed expressly for the VAX-11/750 CMI bus structure. Yet it costs thousands less than DEC and other "boat anchor" designs. This software transparent controller emulates the DEC RH750 Massbus adapter with attached RM03, RM05, RM80 or RP06 drives.

And all of the great features of the new SC750, like all Emulex controllers, are available as complete disk subsystems, pretested and installed by Emulex.

Read the facts below, then get the whole story on our total commitment to the VAX marketplace by writing or calling Emulex Corp., 2001 Deere Ave., Santa Ana, CA 92705. (714) 557-7580. TWX 910-595-2521. Outside California, call toll-free, (800) 854-7112.

For immediate off-the-shelf delivery, call our distributor: First Computer Corporation, 645 Blackhawk Dr., Westmont, IL 60559; (312) 920-1050. In Europe: Emulex Corp., 10th floor, Cory House, The Ring, Bracknell, Berkshire, England. Telephone: 0344-84234; Telex 851-849781.

SC750. THE ONLY ALTERNATIVE.

A single-board, embedded disk controller that interfaces directly to the VAX CMI bus. Functionally identical to the DEC RH750 with its disk adapters. Mix and match drive capacities from 80 to 675 MBytes. Serial data rates to 15 MHz to accommodate the new class of high-density drives. Features automatic self-test, intelligent buffer management, media compatibility, software transparency, low cost and single-board reliability. Available now.





Hardcopy printer/plotter for solid state cameras



Versatec v-80 printer/plotter, an option to the company's solid state camera systems, produces high resolution. 200-point/in, 11" x 8.5" (28- x 22-cm) hard copy in 9 s directly from camera system or data storage. The printer/ plotter gives a 1:1 camera resolution match; camera has effective resolution in object plane. System can also be used for computer directed printing/plotting. The nonimpact, electrostatic printer/

plotter has dual-array writing head that produces overlapping dot pattern for high contrast blacks and continuous lines. Max vertical dot deviation is 2 mils (0.05 mm); horizontal deviation is within 1.5 mils (0.04 mm). System includes camera control unit for camera/printer and system/host interface, dc power, and camera control. Illumination compensation operates on camera's array compensated video data to reduce effects from fixed variations in light intensity caused by lens aberrations and differences in illumination paths between light sources and subject. Versatec, a Xerox Co, 2805 Bowers Ave, Santa Clara, CA 95051. Circle 302

Personal computer terminals

ScansetTM personal terminals have 1-button information access, cursor control keys, and forms and bar/line graphics capabilities. Included are model 410 with automatic computer log-in and model 415 with built-in modem, automatic telephone dialer, and automatic

Electronics Division)

computer log-in. Both models have 6 multifunction keys programmable from keyboard or computer. Up to 12 user defined tasks can be assigned, giving access to host computers or data bases. Auto-dialer feature can dial up to 36 phone numbers (screen displayable) stored in terminal memory, automatically connecting terminal to computer or data base. Feature can also be used as auto-dialer for std telephone. Full 24 lines of displayable text with 40- or 80-char line lengths are featured, with automatic scrolling after 24th line is filled. Phosphor screen features flickerfree display. Printer can be connected through intelligent peripheral port. Buffer management system prevents data loss. Enclosure measures 10.25" x 9.5" x 14.5" (26.03 x 24.1 x 36.8 cm). Tymshare, Inc, 20705 Valley Green Dr, Cupertino, CA 95014. Circle 303

Low noise line printer

Model 40 Whisper Printer features 300-line/min operation at less than 20-dBA noise. Model 40-80 is an 80-col tabletop unit. Model 80-132 is a 132-col version, enclosed in a full-length console. Print chain mechanism produces high quality copies of up to 6-part forms. Paper guide feature provides easy forms loading and trouble-free feeding. Internal setup switches control left- and righthand margins, forms length, print lines/in, diagnostic printout, and communications protocol. Interfaces are ASCII serial RS-232-C or 20-mA current loop selectable between 150 and 9600 baud. An optional TTY compatible SSI interface is also available. HMW Enterprises, Inc, 604 Salem Rd, Etters, PA 17319. Circle 304

Intelligent graphics plotter

Intelligent graphics plotter model 1100 is microprocessor based and provides graphics output for any computer system with RS-232-C port. Std features include x-y and stripchart plotting modes, ASCII char generator with size and rotation control, and internal vector generator. Plotter uses x and y stepping motors, has resolution of 0.005" (0.127 mm), repeatability of 0.002" (0.051 mm), and plotting speed of 2.5 ips. It uses continuous Z-fold paper, disposable fiber tip pens, and is available in 115 and 230 Vac, 50 to 60 Hz. Bascom-Turner Instruments, 111 Chapel St, Newton, MA 02158. Circle 305



Hermetically sealed, 100% leak tested to MIL-STD 883A and solvent resistant.

CIRCLE 188



Belts and Brushes Murder on Life Span

The bad news for mini floppy disk drive buyers is that $5\frac{1}{4}$ inch drives are designed with belt and brush type AC motors

... and they suffer the consequences. The good news according to high level authorities is that there is an excep-tion. The Remex PICO[™] 48/96 tpi, 51/4 inch flexible disk drive has no belts or brushes because it is the first mini-sized floppy with a direct drive DC motor. Direct drive means that improper belt seating is nonexistent so variations in speed and friction-producing side loading are eliminated. Motor life is also extended. A reliable industry source indicates that the MTBF of the PICO motor is 5 years – typically ten times that of most brush type motors. The President of the United States, in his comments, stated (continued on Page 5).

Trouble Maker Eliminated

"Tap-tap wear is a thing of the past" according to design engineers evaluating the Remex PICO 5¹/₄ inch flexible disk drive. This major cause of media damage and wear on mini floppy drives, the loading and unloading of the head on the media, has been eliminated with the Remex PICO because the PICO has no head load solenoid. This design innovation also reduces magnetic leakage which may result in data errors. Rumors that PICO will receive an award from the Association for the Preservation of the Sanity of Systems Designers were not confirmed by Remex.



Direct drive DC motor saves life of 51/4 inch floppy.

Designers Spellbound by Interchange

Reliable interchange of media between Remex PICO drives is enhanced by the precise speed control of the motor's closed loop servo. Speed is regulated to 1% on Remex PICO versus typically 2¹/₄% on other small drives, therefore read/write errors caused by speed variation are not a major factor with PICO. The drive's speed control may also simplify controller design because phase lock loop requirements are less demanding. Vast crowds of cheering engineers stood outside the office of (continued on Page 11).

Drives Embezeled!

A choice of bezel sizes on the Remex PICO 48/96 tpi, 5¼ inch floppy makes this drive the appropriate choice for a wide variety of system configurations according to sources. Among the sizes available is a 2¼ inch low bezel which is ideal for space limited micro-systems. An "industry standard" bezel is optional.

Proud Parent Praises PICO

Remex is a Division of Ex-Cell-O Corporation, a Fortune 500 company with manufacturing and marketing arms in such industries as machine tool, aerospace and automotive as well as electronics. Ex-Cell-O Corporation through its Remex Division is committed to advanced technology development and quality manufacture of both 51/4 inch and 8 inch flexible disk drives.



Ex-Cell-O Corporation

REMEX DIVISION

1733 Alton Street Post Office Box C19533 Irvine, California 92713 (714) 957-0039 TWX: 910/595-1715

Remote batch printer

Remote batch printer (RBP) 1200 series ChainTrain multi-protocol high speed printer connects to most large scale host computers in native mode, and is available in 2 printing technologies. Printer has range of 600 to 1500 lines/min and employs printing technology of IBM 1403. Compressed pitch is optional. Microprocessor based hardware emulation handles the 15 protocols supplied. Clocks for synchronous operation up to 9600 baud are built into protocol converter. In asynchronous mode, protocol converter is strappable to 19.2k baud and supports virtually all signal com-



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TRANSMISSION LINE SPECIALISTS

binations. In single-protocol configuration, printer can be used on dialup or dedicated lines. In multi-protocol configurations, printer is switch-selectable from host to host, protocol to protocol, and synchronous to asynchronous modes. Unit comes with std 1k buffer, upgradeable to 2k or 4k. **Digital Associates Corp**, 1039 E Main St, Stamford, CT 06902. Circle 306

Video data terminal for TRS-80

Video data terminal DT-1 can emulate protocols of 4 std terminals, with configurations selected from the keyboard. Terminal is designed for TRS-80^R traditional and multi-user applications, and for remote communications with timesharing information networks using off the shelf direct connect modems. Terminal contains a custom programmed high speed 8-bit microprocessor that can be configured to emulate the Televideo 910, Lear Siegler ADM-5, ADDS 25, or Hazeltine 1410. Selected protocol is maintained independent of power through use of EEPROM. 12" (30.5-cm) CRT provides a full 80-char x 24-line video display. Upper- and lowercase chars are available. Terminal is equipped with built-in RS-232-C serial interface and a parallel interface; either interface can be used as a printer port for hardcopy output. Tandy Corp/Radio Shack, 1800 One Tandy Center, Fort Worth, TX 76102. Circle 307

EMI PROTEGTION

EMI/RFI shielding windows



Transparent emi/rfi shielding windows for use with all optoelectronic, CRT, incandescent, and analog displays have clear or neutral gray window substrates, or substrates colored to match spectral (continued on page 325)

Columbia Data's New Multi-Personal Computer Is Now Ready For Business

With IBM Personal Computer Software And Hardware Compatibility ... For Starters.

Columbia Data Products' Multi-Personal Computer can use software and hardware originally intended for the IBM® Personal Computer ... while enjoying the flexibility and expandability of all of Columbia Data's computer systems.

Available operating system software includes either single-user MS-DOS® (also called IBM-PC-DOS or 86-DOS) or CP/M 86®, or multi-user, multi-tasking MP/M 86®, providing users with a host of compatible software packages for both personal and business applications. OASIS-16® and XENIX® operating systems will also be available soon.

Our standard 16-bit 8088 hardware configuration provides 128K RAM with parity, two RS-232 serial ports, Centronics parallel printer port, DMA controller, eight levels of interrupt, dual floppy disk system with 1 Megabyte storage, Winchester disk interface, and eight IBM-PC compatible expansion slots , and lists for only \$2,995.

COLUMBIA DATA PRODUCTS, INC. Columbia Data optionally provides 256K RAM boards, 8087 Arithmetic co-processor for high speed math functions, dual RS-232/ RS-422 boards, networking capability, and Winchester disk based system . . . our expansion capability can easily accommodate just about any imaginable hardware configuration, including a 1 Megabyte RAM 8-user system. Call us for more information.



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Cartridge Tape Drive Myth No.2:

ALL ¼ INCH STREAMING CARTRIDGE TAPE DRIVES ARE BUILT ALIKE

Streaming ¹/₄ inch cartridge tape drives may look alike at first glance ...but look again. In interchangeability, data and mechanical reliability, some designs soar above the others.

At DEI, the world leader in ¹/₄ inch cartridge tape drives, we build the Streamer, a ¹/₄ inch cartridge tape drive with design benefits you can see. The rigid metal frame of the Streamer provides a solid base for referencing the magnetic head, cartridge, motor and sensors. In moving head models, the head is precisely held against a reference surface so positioning is repeatable "with zero tolerance." Mechanical tolerances are closely controlled through a major investment in production tooling which assures perfect placement of the cartridge time after time in every drive. The result is outstanding drive to drive interchangeability-even when data is written on one drive at one environmental extreme and read on another drive at the opposite extreme.

All DEI drives — streaming and stop/start — are built with quality. And over 100,000 units in the field are proving it. So get beyond the myth. Write for our article "The Evolution of the High Density ¼ Inch Cartridge Tape Drive" and then call DEI. Like Pegasus, we'll fly to your aid. Data Electronics, Inc., 10150 Sorrento Valley Road, San Diego, California 92121, Telephone (714) 452-7840, Telex #69-7118.



DATA ELECTRONICS, INC.

CIRCLE 192 See Us at NCC Booth #3408

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Computer Terminal Systems, Inc. 65 South Service Road, Plainview, NY 11803/516-752-1965

Honeywell

CIRCLE 193

SYSTEM COMPONENTS/EMI PROTECTION

display output for contrast enhancement. Front surface of the acrylic or polycarbonate windows is anti-glare treated, and imparts steel wool abrasion and chemical resistance. Front surface printed graphics, as well as opaque rear surface background masks, are optional. Layer of transparent gold, vacuum deposited on rear surface of window, provides emi/rfi shielding. Gold film is protected from finger marking by transparent overcoat. All windows are produced with peripheral silver bus bar to accept emi gasketing. Panelgraphic Corp., 10 Henderson Dr., West Caldwell, NJ 07006. Circle 308

EMI enclosures

EMI shielded KDS modular cabinet and console system conforms to FCC emission control regulations and has passed prototype and pre-production testing of rf shielding. System provides attenuation values through varied frequencies up to 66 dB. Interior and components are plated with protective and conductive finish to maintain positive ground with cabinet. Interior is not painted, allowing continuous ground for all equipment mounted in cabinet. Exterior and/or outside exposed surfaces not involved in grounding are painted. Panel heights range from 21" to 78" (53 to 198 cm); panel widths are 19" or 24" (48 or 61 cm). Frame depth ranges from 22" to 36" (56 to 91 cm). All sizes conform to E1A mounting standards. AMCO Engineering Co, 3801 N Rose St, Schiller Park, IL 60176. Circle 309 while inhibit command is on. Logic supply and 15 V are required. Using Monobrid^R technique, the single custom LSI chip performs most converter functions. SEM-JWP features transformer isolated synchro and reference inputs, operation at 60 or 400 Hz, 3-state digital outputs, high digital drive, and BITE. A 1A-format A increment replaces 5 existing key codes. MTBF at 60 °C naval sheltered environment condition is min 200,000 h. ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716.

DATA CONVERSION

Synchro conversion SEM

Synchro converter in standard electronic module (SEM) format, key coded JWP is designed for Navy systems and approved by U.S. Naval Weapons Support Center Qualified Products List. Module incorporates complete 14-bit synchro converter with internal transformers for improved performance. It is a type II tracking converter with transparent latch that allows continuous tracking



Circle 310

Ethernet controller for MULTIBUS



Intelligent single-board Ethernet controller NI3010 contains all data communications logic required for interfacing MULTIBUS based systems to Ethernet local area network. Targeted for 68000, Z8000, and 8086 based systems requiring high throughput over Ethernet, controller fully implements Xerox/Intel/ DEC Ethernet VI.0 specification. Board performs data link and physical channel functions that permit up to 1024 stations to communicate at 10M bps over distances to 2500 m on shared coaxial cables. On transmission, controller formats frames and performs CSMA/CD transmit link management, such as collision detection, backoff timing, and retransmission required to deliver frames onto network. When not transmitting, device continuously listens to network for frame traffic. Only frames with matching address are accepted by controller for subsequent transfer to host MULTIBUS system. Controller performs physical, multicast group, and broadcast address recognition. CRC generation on transmission and CRC validation on reception are performed on all frame traffic.

Physical channel functions implemented on transmission include generating 64-bit preamble sequence for all network receivers to synchronize onto; creating 10M-bps bit stream through parallel to serial frame conversion; generating self-synchronizing serial bit stream through Manchester data encoding; and providing proper channel access. On reception, physical channel functions include Manchester decoding of incoming bit stream into data and clock streams; synchronizing to, and removal of, preamble sequence; and im-

Designed to meet your ongoing information needs, this service offers you a vital window on the fast-paced microcomputer market, with continuous, detailed coverage and forecasts of important trends, developments, and markets. Subscribers to the service also have the opportunity to attend an exclusive annual seminar which provides advance and immediate focus on market movement. strategic indicators, and major impending innovations. **MICROCOMPUTERS:** Markets, Strategies & Opportunities Encompasses the full spectrum of this fiercely Competitive competitive market: from software to peripherals; analyses, infrom microcomputer graphics to networks; cluding in-depth from pricing trends to distribution profiles of all key competitors Focused analyses Quarterly to help you releases of project market new or updated performance forecasts and and develop or strategic refine your analyses of market critical industry strategies issues One-year Detailed, continually up-dated forecasts for subscription, US \$6000 the U.S. home, educational, large and small (Initial release only, business, government and nonprofit markets, US \$2500) as well as the international market. **Creative Strategies International** 4340 Stevens Creek Blvd. Suite 275 • San Jose, CA 95129 USA • (408) 249-7550 • Telex 278537

plementing serial to parallel frame conversion.

Board has 16k-byte receive FIFO which buffers MULTIBUS system from interarrival times of network traffic. For transmit buffering, controller has 2k-byte transmit FIFO for frame retransmissions. All data transfers between controller and host MULTIBUS system are via onboard DMA controller. DMA controller performs byte wide transfers on MULTIBUS in excess of 1M bps, and supports full 24-bit addressing range that allows direct addressing of over 16M bytes of MULTIBUS memory. Board executes power-up self-tests, has pass/fail LED indicator, and provides 3 levels of data loopback operation. Controller also collects network operational statistics. Interlan, Inc, 160 Turnpike Rd, Chelmsford, MA 01824. Circle 311

Realtime clock, communications controller, and software guard

RTC 2200 I/O board combines several Wang I/O boards into a single package for clock functions, calendar management, and 2 levels of software protection on Wang 2200 systems. Two serial ports and parallel printer port are available on RTC 2200P enhanced version. Clock section reports time in 24-h format, and provides stopwatch, countdown timer. and alarm clock. Calendar section retains system date and user date. System date represents current day, date, month, and year, and is automatically changed at midnight. User date represents day, date, month, and year retained for utility purposes by application software. Time and date information is reported in BCD or ASCII. System date/user date can be reported in any of 7 formats. Time and system calendar functions are continuously maintained by onboard rechargeable battery.

RTC 2200P provides identical time/ calendar functions as RTC 2200, but also combines functions of two Wang 2207s and one 22C02 to conserve I/O slots. Format, speed, and addresses of bidirectional serial ports become software selectable. Ports are buffered and can operate at 16 baud rates, ranging from 110 to 19,200 baud.

For software protection, board retains 8-digit license date in nonvolatile memory. Flag is set when current date exceeds license date, allowing applications software to lock out users who fail to renew license. Date is permanently retained even when power is off or when *(continued on page 329)*

CIRCLE 194


New Intelligent Graphics System[®] provides high-function programming. Easily. Quickly.

Powerful, Interpretive Graphics

- Language Most advanced graphics language available for a micro; patterned after Siggraph Core Standard
- Device-independent output; same image can be displayed on color CRT, Plotter, printer or camera
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- and keyboard Simplified implementation of graphics:
- Powerful commands mean enhanced productivity
- Professional Graphs with IGS™ 7 selectable type styles can be displayed in any size, color or orientation
- Over 150 commands, all Englishlanguage, like: PIE, PIE SLICE, BAR, LINE, GRID, AXIS, POLYGON FILLS, ROTATE, PAN, SCAN CONVERTER
- Automatic labeling and scaling of grids and axes
- Introductory Prices Include IGS Software. Terminal \$3940*
 Model 8301-R: 13" 8-color CRT, 117-key keyboard, dot addressable with readable bit map (as shown)
- Desktop \$5700* Model 8063-R: 19"8-color CRT in Industrial Cabinet, 117-key keyboard, dot addressable with readable bit map, 64K user RAM, CP/M,[®] MBASIC and dual 8" double density disk drive with 960K storage

Graphics Workstation \$11,880*

 Desktop as described above, plus Hewlett-Packard's HP 7220C 8-pen color plotter and Summagraphics' Bit Pad 1 digitizer, all program-supported by IGS

Terms/Ordering Information Prices good for the first 100 orders received, cash with order. Use it for 30 days. If you are not pleased, your only cost would be transportation charges to and from Norcross, Georgia. For further information, contact Marketing Services. Call 404/449-5295.

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225 Technology Park/Atlanta Norcross, GA 30092 404/449-5295 TWX 810-766-1581

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Design Tomorrow into your system. The Sapphire 160 is a 160 megabyte, high density 14-inch Winchester drive, with SMD compatible interface. Simplicity of design and advanced technology give you much more for less than any comparable unit.

Less weight. Rare earth magnets are used in the positioner instead of larger ceramic magnets. This permits a major reduction in positioner size, and helps cut overall weight from a typical 140 to only 88 pounds, including integral power supply.

Less downtime. Simple 5-module design and selfchecking electronics cut MTTR to less than ½ hour, and reliable construction techniques push MTBF well over 8000 hours. Less danger of head damage during transport. Because manual locks are so frequently neglected, a unique positioner solenoid lock automatically locks heads and disks in position whenever the power is off. Smaller size and weight make handling less cumbersome.

More data security. Critical data security is assured through MFM recording with PLO clock, and the use of peak shift compensation.

Maximum data storage. To achieve 160 megabytes, Sapphire 160 uses four fixed disks having 600 tracks per inch and 6400 bits per inch density. It is designed to operate in non-air conditioned environments.



Immediate availability. The Sapphire 160 is in quantity production and is available to meet your delivery requirements. Call or write today for complete information and OEM prices.

"We have the experience" 16161 Gothard Street, Huntington Beach, CA 92647 (714) 842-0077

SYSTEM COMPONENTS/INTERFAGE

battery is removed. Special key program, unique to each system house user, allows date to be changed. Serial number, which is compared to that licensed to the software, is similarly retained. Applications software cannot operate if serial numbers do not match, or if 1/0 boards are removed. RTC BASIC operating system is used to implement the software protection. **Computer Concepts Corp**, 8001 W 63rd St, Shawnee Mission, KA 66202. Circle 312

Multiplex bus terminal



MBT microprogrammable bus terminal provides general purpose interface between MIL-STD-1553 data bus systems and commercial minicomputer for MIL-STD-1533 hardware development support and test system integration. Microprogrammed control unit allows the bus terminal to stimulate responses of all 3 generic terminals defined by MIL-STD-1533 (bus controller, remote terminal, and bus monitor). In bus controller mode, terminal is also capable of simulating any subset of all remote terminals with no degradation of performance. Utilizing a comprehensive package of FORTRAN callable drivers and handlers, user can program terminal as standalone system, hot bench test station, or as key element in a full-scale, computer modeled, 1553 avionic system. Digital Technology, Inc, 4130 Linden Ave, Dayton, OH 45432. Circle 313

Multiple interface serial communications controller

General purpose serial communications controller model 1847 + allows host to host, host to 4 targets, or host to 4 terminals communications. The Z80 based intelligent module has 4 channels of either asynchronous or bit synchronous communications. Module is built to withstand electrical noise, airborne contaminants, and vibration. Each channel can be independently configured in bit synchronous record mode (SDLC), asynchronous record mode, or asynchronous character mode. All channels have onboard variable size buffering, onboard or external baud rate generation, and simultaneous operation. In SDLC mode, controller transmits and receives records or SDLC frames. In asynchronous record mode, records are separated by user defined record terminators. In character I/O mode, chars are sent and received 1 char at a time through char buffer located in system memory. To achieve industrial grade quality gold contacts, teflon coated spring clips on each nonsoldered chip, anticorrosive board coating, and corrosion protection and lubricant on all contacts are used. **Xycom, Inc**, 750 N Maple Rd, Saline, MI 48176. Circle 314



WESTREX 800 Series of 150 character per second, alphanumeric bi-directional printers include split platen, flat bed slip/document and 51 to 96 column journal printers in a variety of standard models to suit many OEM applications. All utilize the same simple, reliable drive system, head position sensors, ribbon transport mechanism and other quality tested components for maximum cost effectiveness.

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Box 3503, S-17203 Sundbyberg, Sweden 46/8+981100

MULTIBUS compatible analog I/O board

RMB-741 MULTIBUS compatible 1/0 board has 12 independent analog outputs and 16 differential or 32 single-ended inputs. All I/Os have 12-bit resolution. Bus I/O is 1M-byte memory mapped and selectable to any 16-byte boundary. Board contains onboard microprocessor that controls onboard operations and simplifies program control by host CPU. Six different modes are host programmable. Analog inputs can be jumpered for either differential or single-ended operation. A-D conversion section contains sample hold amplifier and variable gain amplifier that is software programmable for gains of 1, 2, 4, and 8. A-D sample rate is 23 kHz. Each D-A output is separately configurable for voltage or current loop output. Several jumper selectable voltage ranges are available. The 4-mA current offset for current loop mode can be directly generated by hardware, by onboard microprocessor, or by host CPU. Prices start at \$645. Robotrol Corp, 1250 Oakmead Pkwy, Suite 210, Sunnyvale, CA 94086. Circle 315

A D interface card with 8k nonvolatile RAM

Option NVM-8K for A-D interface card IB-902-AB allows data retention during power failures on 6502/6800 systems. Option allows data logger card to store up to 8k of collected data on 4 CMOS RAM chips for up to 3 months. Card features calendar/clock with interrupts and 10 years of battery backup, and 16-channel, 12-bit A-D voltage converter. Card directly interfaces to computer via main bus expansion connector. Nonvolatile RAM converts systems into 16-channel 12-bit data loggers. System can be expanded to 32- and 48-channels with corresponding 16k and 24k increase in nonvolatile memory by parallel use of 2 or 3 identical cards. Mini-motherboard allows direct connection of up to 3 boards on the system. Each IB-902-AB/NVM-8k board has 4 byte-wide configured sockets that can be populated with CMOS RAMS in 2k block configurations. Sockets can also be used for 2k, 4k, or 8k EPROMS. Programs are provided in BASIC to address memory, set and read clock, and read the 16 converter channels. Columbus Instruments. 950 N Hague Ave, Columbus, OH 43204. Circle 316

POWER SOURCES & PROTECTION

200-W battery backup power supply



Standby power system model SPS0200 provides 200-W power at 120 V for 20 minutes under max load, automatically within 1 cycle of power failure. Device contains continuous line filter to trap and eliminate current spikes during normal usage. System is plugged into power outlet, and mainframe, terminal, and other computer peripherals are plugged into the standby supply. As long as power remains constant into the supply, current passes through to the computer. If power drops below 102 V, sensing device immediately switches to output from internal battery. Output frequency is 60 Hz with rectangular waveform. Other models are available with voltage ranging from 100 to 250 V and power output of 50 or 60 Hz. Entire device is protected with line and battery fuses and low battery cutout. During brief outage or brownout conditions, device will automatically transfer back to line power and integral regulated recharger restores battery to full power. Gould Inc, Portable Battery Div, PO Box 43140, St Paul, MN 55164. Circle 317

200-W backup power supply

DATASAVERTM line of ac power backup units includes 200-W model for high end microcomputers. Model protects larger capacity microcomputers utilizing Winchester hard disk drives, personal computers, industrial grade controlling and processing equipment, most minicomputers, and multiple-unit applications needing single backup source. Unit provides continuously filtered ac power from single U.S. std (NEMA 5-15R) output recepticle. At full power, unit provides 2- to 5-min support, with 15- to 30-min support at half-power during blackout or brownout. Supply can power units with switching, linear, or ferroresonant power sources. Precision 0.1% crystal frequency standard allows realtime power sensing and prevents video jitter. Unit includes rechargeable sealed battery and automatic charger, solid state power inverter, ac line voltage monitor and cutout switch, front panel power status LED, and line power loss alarm. **Cuesta Systems, Inc**, 3440 Roberto Court, San Luis Obispo, CA 93401. Circle 318

1000-W MIL-STD switcher

Modular 28-V, 36-A switching power supply SP4008 provides 1000 W and operates from 115- or 220-V, 47- to 440-Hz input power. Supply functions at full load over temp range of 0 to 71 °C without derating; efficiency is at least 80%; line/load regulation is 0.2%. Supplies conform to MIL-T-21200, MIL-E-4158, MIL-E-16400, and MIL-E-5400 requirements. Max output ripple is 70 mV pk-pk, and max tempco is 0.03%/°C. Features include remote sensing, overcurrent/ overvoltage protection, and ability to provide 2000-W output power when paralleled. Automatic shutdown provides overtemp protection; bit circuit indicates low output. Optional remote switch shuts down supply on receipt of positive logic level signal. Devices meet or exceed vibration, shock, and humidity provisions of MIL-STD-810C. Circuit design includes soft start and half-bridge inverter circuit. Single transformer base drive eliminates possible switching transistor failure due to cross conduction. An MS3452 connector receives input power; output dc is derived from brass studs. Output voltage is variable $\pm 10\%$ with panel mounted adjustment potentiometer. CEAG Electric Corp, Power Supply Div, 1324 Motor Pkwy, Hauppauge, NY 11788.



Circle 319

SYSTEM COMPONENTS/ POWER SOURCES

& PROTECTION

Line protector

Model 232DLP data line protector provides protection for computers, CRTS, and remote equipment using EIA RS-232 data lines. Device protects lines from static discharge (ESD) and induced static buildup. Unit also provides protection from overvoltages (long duration) caused by isolation circuit failures, insulation breakdown, and misapplied test voltages including 120 Vac. Unit measures 5" x 7" x 2" (12.7 x 17.8 x 5.1 cm) and weighs 1.5 lb (0.68 kg). It requires no power and is easily installed. Connections are made with std 25-pin connector. Indata Co, 17 Birch St, Lake Grove, NY 11755. Circle 320

Standby power systems

Standby power supply RAMLOK for microcomputer and desktop systems is available in 250-, 500-, and 1000-W sizes. Under normal line voltage operation, supply filters commercial power, removing noise or voltage spikes. It continually monitors line voltage for out-oflimits conditions. Device automatically switches to standby inverter during voltage deviations and operator is alerted to failure condition, while computer system continues to operate. Standby operation from battery backup is 30 min max. When ac power is restored, unit switches computer back to line power and recharges battery. 250-W model is priced at \$325 and includes controller, inverter, and battery. Larger supply models can be purchased with/without inverter or battery. Ladco Development Co, Inc, PO Box 464, Olean, NY 14760. Circle 321

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Plug-in MULTIBUS power supply

MP 530 4-output power supply is plug compatible with std MULTIBUS card cages. Outputs are 5 V at 30 A, -5 V at 1.75 A, 12 V at 4.5 A, and -12 V at 1.75 A. An ac power fail indication is provided 3.0 ms min before dc output voltage drops below 95% of rated value, for power-down operation. All 4 outputs have foldback current limiting, plus short circuit and overvoltage protection. Remote sensing is provided for 5-V supply. Line/load regulation is $\pm 1.0\%$; output line regulation is $\pm 0.1\%$. Op temp is 0 to 55 °C. Electronic Solutions, 5780 Chesapeake Court, San Diego, CA 92123.

Circle 322

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Sunnyvale

40-W switching power supply

AC 8151 40-W switching power supply for small microprocessor based and disk drive systems, and terminal and mixed logic applications, is produced on an open PCB, is jumper selectable for either 115 or 230 Vac. Supply features fully protected voltage/current, built-in emi filter, and low output ripple. Device is UL and CSA approved, and designed to meet European safety standards. Using vacuum impregnated transformers, supply is fully protected from overvoltage and short circuits, and tested with 100% thermal cycle and burn-in. Outputs are 5 Vdc at 2.5 A, 12 Vdc at 2.0 A, and -12 Vdc at 0.1 A. Dimensions are 6.3" x 3.9" x 2.0" (16 x 10 x 5.1 cm). Astec Electronics, 1101 Space Park Dr. Santa Clara, CA 95050. Circle 323

3-way ac line surge suppressors

Line of ac line surge suppressors provides continuous protection against lightning, transient, and switching surges without "crowbar" effect. Surge suppressors can be used on any electrical service between 110 and 120 V, 208 and 240 V, or 380 and 460 V. Units for larger installations or special requirements are provided for 4160 to 13,800 V. Suppressors are installed as close as possible to, and connected on the load side of, main circuit breakers or fuses, protecting all loads connected to distribution panel. Surge overvoltage is dissipated as heat without damaging suppressor: remaining overvoltage is dissipated into ground circuit resistance. Devices are provided for main service and portable protection. Primary service models range from \$995 to \$2495. Plugin portable models range from \$700 to \$995. Eagle Hill Electronics, Inc, 41 Linden Ave, Rutledge, PA 19070. Circle 324

Plug-in ac line monitor

Plugging into std 120-Vac outlet, ac monitor checks line power for transients and surges. Any surge or transient of at least 200-V magnitude and 0.5-ms duration lights 1 of 4 monitor LEDs. Other LEDs indicate when line voltage has reached 400, 600, or 800 V or greater. Memory retains transient data for 24 h. Monitor can be pushbutton reset. Device is priced at \$159. MCG Electronics Corp, 160 Brook Ave, Deer Park, NY 11729. Circle 325

Open frame supply for 5.25 " floppies



Model CP 640 open frame power supply for all popular 5.25'' floppy disk memories features input of 115/230 $\pm 10\%$ Vac, 47 to 440 Hz. Output is 5 Vdc at 0.7 A peak, 12 Vdc at 0.9/1.8 A peak. Line regulation is $\pm 0.05\%$ for 10% load change. Load regulation is $\pm 0.05\%$ for 50% load change. Transient response is 50 μ s for 50% load change. Output ripple is 3. 0 mV peak to peak max. Op temp is 0 to 50 °C. Case measures 5.5" x 4" x 1.62" (14.0 x 10 x 4.11 cm). **Condor, Inc,** 4880 Adohr Lane, Camarillo, CA 93010. Circle 326

Unregulated power supplies

Black Line/B series unregulated power supplies power any circuitry that accepts unregulated dc power as basic drive source. Supplies range from 15 to 750 W; voltages range from 6- to 250-Vdc output. Universal input voltage is 115/230 Vac at 50/60 Hz. Specs include max ripple of 3% rms, temp rating of 0 to 50 °C (to 70 °C with derating), and overcurrent protection. Open frame construction, transformers, and floating output with computer grade capacitors are provided. Built-in input taps provide $\pm 10\%$ output voltage adjustment to compensate for line/load variations. Prices for the 38 model series range from \$29 to \$245. Supplies operate at \$0.35/W. Standard Power, Inc, 1400 South Village Way, Santa Ana, CA 92705.



Circle 327

MEMORY SYSTEMS

Add-in Winchester disk for IBM Personal Computer



Add-in Winchester disk system for IBM Personal Computer requires no external chassis, and can be installed directly in floppy disk area of the IBM system. Storage capacities are 6M, 12M, or 18M bytes/drive, with higher capacities planned. System's single-board Winchester disk controller supports up to four Winchester drives and is fully buffered with automatic error correction. System includes software, controller, disk drive, and documentation, and is priced at \$2995 (6M-byte version), \$3495 (12M bytes), and \$4195 (18M bytes). Disk controller is priced at \$1950. Datamac Computer Systems, 680 Almanor Ave, Sunnyvale, CA 94086. Circle 328

High throughput drive

Model 6064 disk drive features 16 moving heads controlled by dedicated servo positioning system and memory storage of up to 10.2M-byte formatted data (131k bytes/cylinder). Track switch time within cylinder is 10 ms. No reseek or additional settling time is required. Data throughput approaches that of a fixed head drive. Disk can replace 8 floppy drives in program store applications. Drive can be used in adverse environments where particulate contamination and wide temp variations are encountered. Actuator, heads, and media are protected from contamination within dustproof enclosure. Integral blower provides forced air cooling directed around the outside enclosure and across electronics. Op temp range is 0 to 50 °C. Vermont Research Corp, Dept P1, Precision Park, North Springfield, VT 05150. Circle 329



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CIRCLE 200

SYSTEM COMPONENTS/

DEC compatible 3-density tape and disk systems

Tape subsystems IPS 7016 are DEC PDP 11/70 compatible and provide 800-, 1600-, and 6250-bpi operation. Subsystems support TWE 16 emulation by replacing RH 70 and plugging directly into 11/70 cache bus. System supports reading and writing of data at 125-ips and 500-ips rewind speed. With hardware error recovery, system offers 2-track data correction and 3 times increased error recovery capability. In GCR mode, system reduces backup media recovery costs and guarantees end-user data recovery during disk dump and restore. Tape mount and operator intervention errors are virtually eliminated. System is compatible with all PDP 11/70 operating systems. Unit price is \$37,000. IPS BIG BYTE 160M-byte Winchester disk subsystem is compatible with DEC UNIBUS and Q-bus. Disk supports RP/RK emulations. Unit price is \$8350, and includes cables and terminators. Information Products Systems. Inc, 6567 Rookin, Houston, TX 77074. Circle 330

10M-byte Winchester for MDOS



A 10M-byte Winchester hard disk for Motorola EXORcisor system runs Motorola disk operating system (MDOS). Drive interface requires no modifications to MDOS, MDOS based software, or user software. Firmware residing in existing EXORcisor disk controller board makes MDOS appear to have 16 virtual, doublesided, single-density, 8" floppy disk drives online at any time. Installation involves changing 1 chip in EXORcisor controller and inserting hard disk interface board into EXORcisor backplane. Existing EXORcisor disk is retained for floppy disk backup. Drive is available for 6800 and 6809 systems and single- or double-sided diskette drives. Price is \$6875. Computer System Associates, Inc, 7562 Trade St, San Diego, CA 92121. Circle 331



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Call or write today for complete specs on the 9000 Series.



California Computer Products, Inc. 2411 West La Palma Avenue Anaheim, California 92801 Telephone (714) 821-2011

9600-bps synchronous modem with analyzer

SuperModem II 9600-bps modem with built-in line analyzer increases link efficiency and has noise tolerance of up to 6 dB greater than conventional designs. Modem transmits full-duplex, synchronous binary serial data over dedicated or dial-up voice grade channels, over any distance. Single-channel units operate in continuous or simulated controlled carrier mode. Four-channel units feature integral 4-channel multiplexer.

Line diagnostics include bit error rates, telephone line loss and delay distortion, S/N ratio, rms power of received signal, frequency translation measurements, call progress status, and LED status indicator tests. Thumbwheel dials, switches, display indicators and test points located behind semi-transparent front panel provide access for system status checks and routine testing. If line deteriorates, modem can be reconfigured for fallback operation at 4800 bps; a SuperModem II at other end will automatically revert to fallback mode. Four-wire connection at 9600 bps can be reestablished with pair of telephones at each path end using 2-call dial backup feature.

Device uses unique data encoding, signal generation, and data recovery technique that eliminates need for complex equalization, and is based on low baud rates. Modem transmitter simultaneously generates discrete carriers, modulating each to represent a portion of total data stream composite signal. At receiver, each carrier is independently demodulated and its data are combined with data from the other to reconstruct original data stream. Digital interfaces include RS-232-C and CCITT V.24/V.28. Units function in temp range of 0 to 50 °C and are available as standalone or rackmount equivalents. Gandalf Data Inc, 1019 S Noel, Wheeling, IL 60090. Circle 332

Broadband communications network

An expanded Net/One local area network product line includes broadband system operating at 5M-bps data rate on any 1 of 5 commonly used CATV channel pairs. System is fully interconnectable to Net/One baseband. Broadband system can be used on midsplit or dual-cable configurations. Carrier sense multiple access technique is employed to improve system throughput. System meets pro-

posed EIA guidelines for broadband local networks and employs vestigial sideband amplitude modulation for increased compatibility with video transmissions on other channels. Network interface units (NIUS) and associated software are virtually identical to baseband and

broadband versions. In hardware, a small modem interface board is substituted in each NIU, and rf modems replace network transceivers. Ungermann-Bass, Inc, 2560 Mission College Blvd, Santa Clara, CA 95050. Circle 333



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4-C



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CIRCLE 221

SYSTEM COMPONENTS/

Asynchronous quad-channel module

Four-channel module for MICROPLEXER family of statistical multiplexers/data concentrators, M-IAD supports asynchronous traffic only, and is interchangeable with existing synchronous/ asynchronous modules. It fully supports all MICROPLEXER supervisory and network management features, including network configurator and extended diagnostics options. Versions are available for RS-232, MIL-STD-188-C, and MIL-STD-118 -114 operation. User selectable std features include data speeds from 50 to 9600 bps; operation with any 5-, 6-, 7-, or 8-bit asynchronous codes including 9-bit graphics terminals; odd, even, or no parity; dynamically allocated buffers with user selected priority; inband or out of band traffic control; flyback buffering; and automatic, noninterfering downline loading of channel parameter changes. Unit price is \$750 with quantity discounts available. Timeplex, Inc, One Communications Plaza, Rochelle Park, NJ 07662. Circle 334

Stat mux with 240-channel error-free transmission

DCX840 intelligent networking statistical multiplexer provides error-free transmission of up to 240 asynchronous channels over 15 composite links max. Basic card modules include low speed channel module (LSC), automatic repeat request module (ARQ), buffer module (BUF), systems test and configuration module (STC), and bus extension module (BEM). Modules are housed in a 17-card slot enclosure frame with power supply. Each LSC module occupies 1 card slot and accepts up to 4 asynchronous inputs. Input data rates can range from 50 to 9600 bps in 5-, 6-, 7-, or 8-bit code. Max aggregate input to LSC module is 9600 bps. The stat mux accommodates up to 60 LSC modules.

ARQ module occupies 1 card slot and performs composite link interface, passing data up to 19,200 bps. Data frames are transmitted by ARQ module and simultaneously put into memory. Memory holds data until acknowledge receipt is received from distant ARQ module. If retransmission request is received, frame received in error and all subsequent frames are retransmitted. Multiplexer can have up to 15 high speed composite links at 1 location, with 1 ARQ module/composite link.

Each BUF module occupies 1 card slot, performs data buffering, and provides



CIRCLE 205

16k-char storage. Up to 6 BUF modules can be used for 256k-char buffer. Single stat mux STC module has mapping and test panel (MTC) to enable network testing and configuration control. BEM is used when extension frames are required in conjunction with master frame. Up to 4 extension frames can be added, with 1 BEM/frame needed. BEM, occupying 1 card slot in master frame, is cable connected to bus termination module (BTM). Up to 4 BEMS can be inserted in master frame to feed 4 BTMs in their own extension frames.

DCX840 is compatible with other DCX family members. Available as standalone or rack unit, with optional user switch (USO) card module, DCX840 can be field upgraded to DCX850 switching multiplexer. **Rixon Inc**, 2120 Industrial Pkwy, Silver Spring, MD 20904. Circle 335

Asynchronous data transmission modems

Family 1180 series of asynchronous transmission modems is available in originate (model 1180 A) or receive (model 1180 B) configurations, functions up to 300-bps full-duplex on switched telephone networks, and meets CCITT recommendation v.21. For transmission at 75 bps and reception at 1200 bps, modem 1182 A is available for use in fullduplex split speed operation on switched telephone facilities. Modem 1182 B provides transmission at 1200 bps and reception at 75 bps. Both 1180 B and 1182 B are provided with automatic connect/disconnect feature. For 1800-bps asynchronous requirements, series includes 1182 T modem which meets Bell 202 specs for operation over 2 or 4 leased lines in point to point or multidrop systems.

Data terminal interface meets EIA RS-232 and CCITT V.24/V.28 recommendations. Units are optionally available with TTL/CMOS compatible interface. Alternative power can be supplied from modems' associated DTEs at ± 12 Vdc or 5 Vdc, or from external ac mains transformer. Modems can be built directly into terminal, mounted in std 19" (48-cm) rack for multiple configurations, or encased in plastic desktop housing. ITT, Data Equipment and Systems Div, Suite 8927, One World Trade Center, New York, NY 10048.



Circle 336

TEMPEST statistical multiplexer

TD-1344/FYC microprocessor controlled 8-channel statistical multiplexer is designed to NACSEM 5100 (TEMPEST) standards, and conforms to MIL-STD-188-114 for electrical interface. System is functionally similar to industry std Supermux 480. Intelligent units use 1 transmission line to carry data, previously transmitted by up to 8 lines. Statistical techniques transmit only active data inputs, conserving bandwidth to allow more than double throughput of conventional multiplexers. Inputs can be mixed asynchronous or isochronous speeds to 9600 bps. Data are buffered, checked, and, if necessary, retransmitted, all completely transparent to existing terminals and software. Sufficient buffer storage is provided so that no data are lost with outages lasting 10 s or more on fully loaded 9600-bps line. Downline loading and built-in diagnostics are featured. Users can initiate tests and reconfigure remote, unattended units from central site. Unit occupies 5.25" (13.34 cm) in std 19" (48-cm) rack. Multiplexer is assigned to Federal Supply Class 5811; Federal Stock number is 01-112-3489; provisioning is in accordance with MIL-STD-1552; manuals supplied are in accordance with MIL-M-38784A. Infotron Systems Corp. Cherry Hill Industrial Center, Cherry Hill, NJ 08003. Circle 337

Broadband modem



M500 broadband cable modem shares common circuitry with M500C, allowing transmission of high speed digital data over CATV systems. Individual data rates of 56k to 7M bps are available. Aggregate data rates of 500M bps can be obtained on a single cable. Modem implements up to 3 full-duplex circuits/ 8.5" (21.6-cm) chassis for locations having more than 1 data communications usage. Features include infield expandability, and capability to add a second, redundant power supply for increased availability in critical applications. Comtech Data Corp, 350 N Hayden Rd, Scottsdale, AZ 85257. Circle 338

SYSTEM ELEMENTS

European rfi std magnetic dc systems



Permanent magnet dc motor and control systems PM/DC line meet European std for rfi. The 220/240-V, 50/60-Hz input systems meet VDE 0875 level N suppression specs, and carry VDE Marks License label, certifying that they have passed VDE radio protection test program. Line consists of 34 motors and gearmotors, plus 9 speed/torque controls. The electronic controls are available in chassis or encased configurations. Dual-rated motors and gearmotors, when operated with level N suppression circuitry controls, provide continuous duty ratings of 53 to 112 W with 1.8 current form factor. Without level N controls, continuous duty horsepower range is 95 to 190 W with 1.0 form factor dc current.

Motors have electrical efficiency of 10% to 15% higher than shunt wound motors, high starting torques, and higher torques at low speeds. In portable equipment installations, motors operate with lower current drain for more efficient battery operation and have self-braking or reduced shaft coast. By changing line connection polarity, motor can be reversed. Dynamic braking can be via shunting 2 motor leads.

Gearmotors are offered in right angle or parallel shaft versions. The controls allow for infinite speed adjustment over entire speed range. An adjustable torque control, available on 3 models, provides soft starts and controlled acceleration of inertial loads. Other features include closed loop feedback, line voltage and temp compensation, and line transient protection. Each SCR (thyristor) control carries faceplate information in 3 languages and is designed for European fusing. Optional kit to convert system to U.S. fusing is available. Bodine Electric Co, 2500 W Bradley Pl, Chicago, IL 60618 Circle 339

20-col printhead

KH128 20-column thermal printhead features 13-ms dot line print speed. Thick film technology is combined with l^2L shift registers and drive circuits mounted directly on the substrate in integrated form. Print elements, totaling 100, with dimensions of 0.01" x 0.0138" (0.025 x 0.035 cm) each are arranged in 20, 5-element char groups. Total print width is 1.86" (4.72 cm). Printing surface is located 0.14" (0.36 cm) from module edge. **ROHM Corp**, PO Box 19515, Irvine, CA 92713. Circle 340

Hybrid stepper motor

Line of 0.8°, 4SH stepper motors have fine angle bidirectional operation for head positioning in disk and tape memories, paper feeds and char drives in printers, pen drives in chart and X-Y recorders, and similar high resolution devices. Motors are less than 2.25" (5.72 cm) in diameter, and use hybrid permanent magnet construction. Holding torques range from 41 to 80 ozin. Two case lengths are available, 1.8" (4.6 cm) and 2.2" (5.6 cm), weighing 16 and 21.5 oz (0.45 and 0.6 kg), respectively. Std models include 6-, 12-, or 24-Vdc operation, double-shielded ball bearings, and 6-lead bifilar coils. Rear shaft is optional. AIRPAX/North American Philips Controls Corp, Cheshire Industrial Park, Cheshire, CT 06410.

Circle 341

Low cost screen monitors

Line of high resolution green phosphor screen monitors includes 9" (23-cm) Pi-1 and 12" (30-cm) Pi-2 models. Both monitors have 1000-line resolution at screen center. Pi-1 unit has min 64-char x 16-line text display; Pi-2 has 80-char x 24-line text display. Units feature display brightness control, anti-reflective screen, and LED power indicator. Pi-1 measures 8.63 " x 8.88 " x 9.88 " (21.92 x 22.55 x 25.10 cm); and Pi-2 measures 12" x 11.88" x 12" (30 x 30.18 x 30 cm). Connection to both is via std SO-239 connector or RCA phone jack. Units come with cable adapter. Bandwidth is 20 MHz and horizontal rate is 15.6 kHz. Monitors are priced at \$249 (Pi-1) and \$275 (Pi-2); quantity discounts are available. USI International, 71 Park Lane, Brisbane, CA 94005. Circle 342

LEGEND has it that the Phoenix will rise again, not from the flaming ashes but from out of the depths of the bayous ...



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THE LEGENDLIVES!

The Phoenix 1024 High Resolution Color Graphics



Phoenix Computer Graphics Inc.

Lafayette, Louisiana 70508 318-234-0063

'SEE US AT SIGGRAPH 82'

Press fit/discrete headers

Series 45000 headers feature 5 press fit contact sizes and 5 discrete contact sizes for fast disconnect/reconnect of PCBs to flat cable connectors. Both discrete and PCB headers offer 20, 26, 34, 40, or 50 contacts, along with protective lip. Discrete headers are offered with 3 straight and 3 right angle configurations. Both designs are available with square wrap, square solder, and round solder tails. **Dynatech Corp**, 1225 E Wakeham Ave, Santa Ana, CA 92702. Circle 343

Resistor/capacitor network line

Resistor/capacitor line in DIP and singleinline package (SIP) configurations provides high density packaging within common network body. RC networks can be supplied with thick film circuit materials specified for MIL-R-83401 qualified resistor network. Capacitors in this circuitry can be made to meet EIA RS-198 or MIL-C-55681 specs. Molded DIP networks are supplied in 14- and 16-pin styles; coated SIP models are supplied with from 4 through 12 pins. Both DIP and SIP models can be ordered with combinations of NPO, BX or X7R dielectric capacitor characteristics within the same package and over a range of resistance values. Std resistance range is 10 to 3.3 M Ω . Capacitance range is from 500 pF to 0.1 µF. Dale Electronics, Inc, PO Box 609, Columbus, NE 68601. Circle 344

ZIF production sockets

"PRO-ZIF" family series 630 of ZIF production sockets includes 24- and 28-lead versions, in addition to existing 40-lead sockets. Sockets stand less than 0.25" (0.64-cm) off the PCB and are 0.75" (1.91-cm) wide. Lever at 1 end of socket body, rotating 90°, controls opening and closing of contacts. The IC device is dropped into socket and held in place by moving lever to lock position. Sockets feature single-face wipe contacts on 0.6" (1.5-cm) centers. Made of phosphor bronze, contacts are plated with 50 μ in of tin or 30 μ in of select gold. Op temp is - 40 to 105 °C for tin-plated contacts

and -40 to 125 °C for gold-plated contacts. Body is molded of glass reinforced polyester. Sockets meet MIL-STD-83734. Wells Electronics, Inc, 1701 S Main St, South Bend, IN 46613. Circle 345

Color data display



Series 4300 high resolution color data displays have scanning capacity of 1065 lines/50 Hz (27 kHz) or 1065 lines/60 Hz (32 kHz). Typ video bandwidth is 50 MHz. Systems have Delta 90° shadow mask picture tube for accurate video reproduction. All monitors accept red, green, and blue with external sync, or red and blue with sync on green. All inputs are looped through and EIA RS-343 compatible. Screen sizes are 14" (36 cm), 19" (48 cm), and 26" (66 cm). The 37and 51-cm CRTs are black matrix type with 0.31-mm pitch. Phosphors for both screen sizes include normal persistence red, green, blue phosphors (NP); long persistence red, green, blue phosphors (RGW); and long persistence red and green combined with norma! persistence blue phosphors (LP/SB). Nonblack matrix type 66-cm CRT has pitch of 0.37 cm. Options include rackmount and polarized contrast enhancing optical filter. Barco Video Systems n.v., Th. Sevenslaan 106, B-8500 Kortrijk, Belgium. Circle 346

15 ° VR stepping motors

Size 15, 4-phase, 15° vR stepping motors measure $1.5'' \times 1.437''$ (3.8 x 3.650 cm) and are furnished in 2 models—15M34S1 for 12-Vdc operation, and 15M34S2 for 24-Vdc operation. Both offer std servomotor mounting diameter and groove. Plain output shafts are std, lead screw output shafts are optional. Electrical/mechanical specs can be tailored to custom requirements. **Novatronics of Canada Ltd**, PO Box 610, Stratford, Ontario, Canada, N5A 6V6. Circle 347

D-subminiature jumpers

D-subminiature jumpers are terminated in 9-, 15-, 25-, and 37-contact male and female styles with low overall front to back connector profile. Use of std ribbon cable facilitates D to non-D hybrid jumpers as well as custom daisy chain applications. Jumpers feature connectors that are injection molded around cable and contacts to form complete unit with integral strain relief. Connectors virtually cannot come apart. Connector body is black thermoplastic polyester with flammability classification UL 94 v-o. Contacts are nickel silver CDA C77000 alloy with 30-µin gold surface finish option. Cable is 28 AWG gray, UL style 2651, or rainbow, UL style 2884. Mounting hardware is available. The 25-position male D connector with nickel silver contacts in 1000 quantities is \$3.50; similar female D is \$3.88. Selective gold contact 25-position male D in 1000 quantities is \$4.38: similar female D is \$4.85. Symbex, 72 Corwin Dr, PO Box 938, Painesville, OH 44077.



Circle 348

Incandescent, LED switches

Lighted MPS series of pushbutton switches includes incandescent and LED models with soft and high intensities. and spot- and full-button indicator styles. Available as single- or gangedswitch assemblies, switches have bifurcated silver or gold contact system and brackets to ensure module to module alignment. Built-in standoffs are provided for cleaning and PC mounting. Spot indicator actuator accommodates snap-on, snap-off buttons. Indicator circuit independent of switch allows design flexibility. Soft intensity modules are logic circuit compatible. Bezels are optional. Hot stamping or relegendable inserts with several keycap covers are available. Centralab, Inc, 5855 N Glen Park Rd, PO Box 2032, Milwaukee, WI 53201 Circle 349

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LITERATURE

Data communications products

Black Box^R 1982 catalog describes over 200 data communications devices, including IBM compatible protocol converters, programmable communications adapter, interface converters, data switches, EIA test sets, and terminal and port sharing devices. Black Box Catalog, Pittsburgh, Pa.

Circle 355

1/0 modules

"Pitfalls to Avoid in Selecting I/O Modules" application note details current rating vs junction temp, emi induced pilot circuit false operation, and series operation compatibility. AMF Inc, Potter & Brumfield Div, Princeton, Ind. Circle 356

Cylindrical connectors

Thirty metal shell cylindrical connectors, over 130 circular plastic connectors, and 550 compatible contacts are detailed in 56-p brochure. AMP Inc, Harrisburg, Pa. Circle 357

Data conversion overview

Fourth edition handbook and circuit applications guide of A-D conversion systems compiles formulas, test methods, definitions, and specs/selection criteria for ADCs and DACs, sample and hold circuits, and ancillary devices. Analogic Corp, Wakefield, Mass.

Circle 358

PROM technology and programming

Guide describes programmable bipolar PROMS, EPROMS, FPLAS, PLAS, and covers data handling and storage, interface, and device handling. Data 1/0, Redmond, Wash. Circle 359

Data communications testers

Brochure profiles Interview 29/30/40 series of data communications testers, available as models 29A data analyzer with HEX keyboard; 30A data analyzer with fully code converted ASCII keyboard; and 40A interactive data analyzer. Atlantic Research Corp, Alexandria, Va.

Circle 360

Data processing system

CEOTM comprehensive electronic office system for automated/distributed operations is featured in brochure 021-1448. Data General Corp, Westboro, Mass. Circle 361

Power supplies for industry std floppies

Fifteen models of multiple output power supplies for 5.25" and 8" floppy disk media are outlined in catalog 3-81, with I/O voltage specs, peak surge ratings and current, and line and load regulation. Deltron Inc. North Wales, Pa. Circle 362

Open frame linear power supplies

Illustrated bulletin introduces DK series open frame linear power supplies, with dimensional drawings and specs covering 64 models. NJE, Dayton, NJ. Circle 363

Switching and linear power supplies

Brochure describes line of open frame switching and linear single- and multipleoutput power supplies, with power requirements for computers and peripheral products specified. Sierracin/ Power Systems, Chatsworth, Calif. Circle 364

Data acquisition

Data acquisition components and subsystems are profiled in 2-vol 1982 data book that features 60 new products, selection guides, and product prices. Analog Devices, Inc, Norwood, Mass. Circle 365

Decoupling capacitor chip

Technical paper describes the BitGuard^R decoupling capacitor chip, a multilayered ceramic capacitor enclosed within IC package prior to bonding and encapsulation. Avx Ceramics, Myrtle Beach, SC. Circle 366

Portable/desktop terminals

Data sheet describes Miniterm models 2300 portable and 2200 desktop terminals that are based on bidirectional printer with 1 x 11 printhead and multiple communications options. Computer Devices Inc, Burlington, Mass. Circle 367

Logic analyzers

Application note 112 overviews logic analyzers, defining digital system design/development problems that can be solved with model K100-D; note 113 describes K101-D microprocessor oriented logic analyzer that carries out selective trace on 8085A systems. Gould Inc, Santa Clara, Calif. Circle 368

Packet switching and local networks

Two manuals outline Multi-Plex.25 statistical time division multiplexer, and Multi-Switch.25 routing device for X.25 trunks. Dynatech Packet Technology, Alexandria, Va. Circle 369

Incandescent lamps

Lamp catalog 250 provides 12 pages of specs on all subminiature and miniature 1.5- to 48-V incandescent lamps, with std bases, including wire terminals, profiled. Gilway Technical Lamp, Woburn, Circle 370 Mass

Software catalog

Software Desk ReferenceTM catalog, with information on 200 microcomputer programs, includes listing of 26 new products, minicomputer systems section, and listing of 16-bit software programs. Lifeboat Associates, New York, Circle 371 NY.

Uninterruptible power systems

Illustrated product bulletin describes line of 3-phase UPS, detailing isolation of critical loads from blackouts, brownouts, line transients, and commercial ac line fluctuations. Lortec Power Systems, Inc, North Ridgeville, Oh. Circle 372

Microprocessor add-in memories

Catalog features add-in memory boards for MULTIBUS, EXORciser, and LSI-11 systems, with cycle and access times. storage capacities, power monitoring, and write protocol control profiled. Micro Memory Inc, Chatsworth, Calif. Circle 373

Software development system

Product bulletin outlines the 9520 software development system that can work independently or in conjunction with 9508 MicroSystem emulator for developing 8-bit microprocessor systems, or with 9516 MicroSystem integration station for developing 8- and 16-bit systems. Millennium Systems, Cupertino, Calif.

Circle 374

Software catalog for personal computers

NECIS PC-8000 personal computer software catalog includes programs for 10 applications areas developed by Lifeboat Associates. NEC Information Systems, Inc, Lexington, Mass. Circle 375

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The S-100 Bus Handbook by David Bursky

Exclusively discusses S-100 bus computer systems and how they are organized. Covers computer fundamentals, basic electronics and the parts of the computer. Explains all operating details of commonly available S-100 systems. Each major system board detailed as to its operation and how it connects to the rest of the system.

0897-X, 272 pages; Hayden Book Co., Inc. \$15.75

Circle 557

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The S-100 BUS Handbook WE BURSKY

Computer-Assisted Data Base Design by George U. Hubbard.

This book not only thoroughly explains the theoretical aspects, but also provides explicit directions on all data base design procedures. In addition to a practical design methodology it discusses the ways to automate the major portions of this methodology. However, all of the techniques can be utilized without computer assistance.

320 pages; 123 illustrations; 6 x 9; Van Nostrand Reinhold Data Processing Series; \$24.95. August, 1981. Circle 558

DATA COMMUNICATIONS a user's guide by Kenneth Sherman.

A BRAND NEW quick and effective source for pinpointing and eliminating system malfunctions, discovering new, more efficient data movement, learning effective trouble-shooting, ensuring strong, clear signal transmission and achieving maximum performance and value. Put these *all new* ideas and many others to work for you!

348 pages; 95 illustrations; Reston Publishing Company Inc; \$21.95. 1981. Circle 559

Android Design: Practical Approaches for Robot Builders by Martin Weinstein.

A comprehensive look at the tools, materials and techniques necessary for designing an android. Examines what an android is, what you can expect it to do, and how this will translate into the design requirements. Also looks at both usual and unusual hardware and software, and mechanics and mechanisms.

Hayden Book Company, Inc., 256 pages, 6 x 9, 5192-1, \$11.95 Circle 560

An Introduction to Microprocessors: Experiments in Digital Technology by Noel T. Smith

A "learn-by-doing" guide to the use of integrated circuits provides a foundation for the understanding of the underlying hardware actions of programming statements. Emphasis is placed on how digital circuitry compares with analog circuitry. Experiments provide clear understanding and encourages the reader to construct electronic projects using integrated circuits.

Hayden Book Company, Inc., 184 pages, 8½ x 11, 0867-8, \$10.95 Circle 561

Data Base Architecture by Ivan Flores, Ph.D.

This is the definitive guide to data base organization, giving the answers to the why's and how's. It describes the structure and use of information organized into a data base, and how application programs, data structures, data base management systems (DBMS), the operating system, and hardware relate to each data base organization.

408 pages; 295 illustrations; 6 x 9; Van Nostrand Reinhold; \$26.50. July, 1981. Circle 562

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