A PENNWELL PUBLICATION

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

JUNE 1981

BUBBLE MEMORY CIRCUITS PROMOTE 3-DIMENSIONAL STACKING

IEEE 488 ERROR HANDLING TECHNIQUES: PROS AND CONS

FPLA ARBITER CONCEPT ADAPTS TO APPLICATION NEEDS

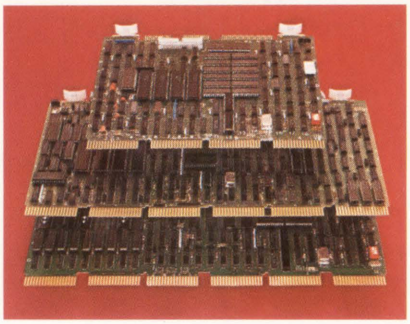
Family pride.

Now there's an advanced technology family of single board controllers for DEC* computers from Western Peripherals—the number one name in controllers.

The TC-131 (for PDP-11s*) is the first TM-11 emulating controller to combine PE and NRZ on one standard hex board. It lets you mix 9-track, PE, NRZ or dual density tape units in any combination up to 125 ips. A 64 byte data buffer allows installation at any point on the unibus without consideration of NPR priority.

The TC-151 single board NRZI tape controller interfaces any industry-standard drive to the LSI-11.* Add a dual width Phase Encode Board for the same performance as the TC-131.

The DC-231 accommodates up to four SMD disc drives of 40 to 600 mb each with RMO2 emulation. Its four sector (2048 bytes) data buffer makes "data-late" errors a thing of the past. The advanced technology "micro-engine" allows a complete track to be written on a single drive revolution. A measurable performance advantage for your PDP-11.



All three controllers are software compatible. All have self test. All are backed by one of the best factory service organizations in the business. And all can be delivered in 30 days.

For more information, call or write today: Western Peripherals Division, Wespercorp, 14321 Myford Road, Tustin, CA 92680, U.S.A. (714) 730-6250. TWX: 910 595-1775. CABLE: WESPER

Number 1 in controllers for DEC and Data General computers.

western peripherals™
Division of WESPERCORP
CIRCLE 1 ON INQUIRY CARD

*Trade name of
Digital Equipment Corporation.

We've got your number in 1981. It's 6450.

Model 6450...

The ¼″ cartridge recorder that thinks it's a ½″ tape deck.

Kenndey's Model 6450—it's a start/stop drive which is faster than streaming in almost all applications; a drive that has a data reliability rate for soft errors of not less than 1 x 10^{10} and a hard error rate of 1 x 10^{11}. The reason? Model 6450's GCR recording technique.

Need Capacity? Model 6450, with a DC 600A cartridge, will store up to 23 MBytes of unformatted data, and over 20 MBytes formatted.

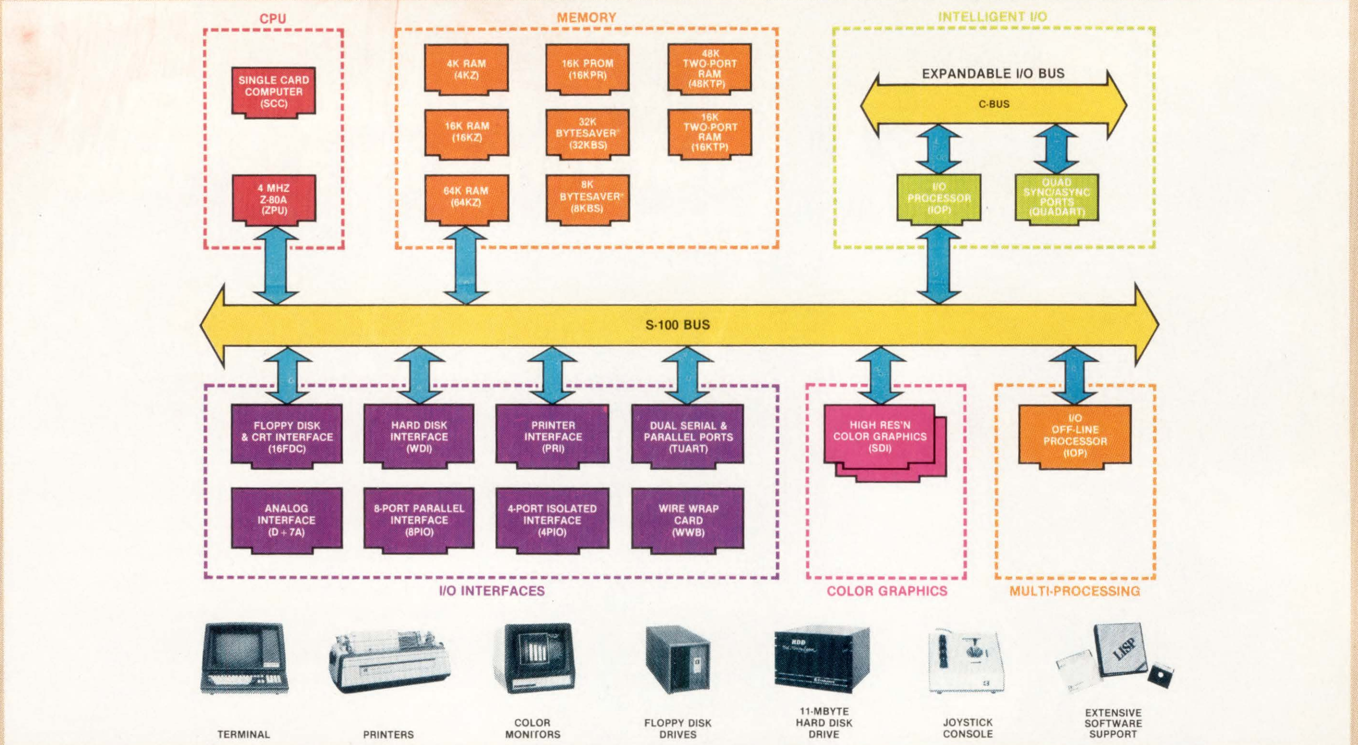
In a hurry? A serpentine head is standard on Model 6450, eliminating time consuming rewinds. **Need simple interface?** Model 6450's intelligent Pico bus interface is not only easy to interface—it's been proposed as an industry standard. If you need a controller, there are a variety for all standard mini-computers.

The bottom line! Model 6450 is the answer to Winchester back up. Reliable, low in cost and available off-the-shelf. And built with Kennedy quality.

KENNEDY
Subsidiary, Magnetics & Electronics Inc.
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TWX 910-585-3249
CIRCLE 2 ON INQUIRY CARD

Model 6450 shown in service position.

KENNEDY · QUALITY · COUNT ON IT



What Cromemco computer card capability can do for you

The above diagram shows in a functional way one of the most complete lines of computer cards in the industry.

Look it over carefully. It could be well worth your while.

These are all cards that plug into our S-100 bus microcomputers.

You can also assemble them into a custom system in convenient Cromemco card cages.

MULTI-PROCESSING AND INTELLIGENT I/O

The range of capabilities and versatility you can draw upon is enormous.

In processors, for example, you have a choice of CPU's including our extremely useful new I/O Processor. This can be used as a satellite processor to do off-line processing, multi-processing, and to form intelligent I/O. It opens the door to a whole new group of applications and tasks. Ask us about it.

HIGH RESOLUTION COLOR GRAPHICS

Again, you can have beautiful high-resolution color graphics with our color graphics interface. You can select from over 4000 colors and have a picture with a resolution at least equal to quality broadcast-TV pictures.

You have an unprecedented selection of memory including our unusual 48K and 16K **two-port** RAMs which allow high-speed color graphics.

LOTS OF STORAGE

These days you often want lots of disk storage. So you can select from our disk controller card which will operate our 5″ and 8″ floppy disk drives (up to 1.2 megabytes). Or select our WDI interface to operate our 11-megabyte hard disk drives.

POWERFUL SOFTWARE AND PERIPHERAL SUPPORT

There's much more yet you can do with our cards. And, of course, there's an easy way to put them to work in our 8-, 12-, and 21-slot card cages. Our PS8 power supply makes it simple to get the system into operation.

Finally, Cromemco offers you the strongest software support in the industry with languages like FORTRAN, C, COBOL, ASSEMBLER, LISP, BASIC and others. There is also a wide choice from independent vendors.

To top it all off, you can draw from a substantial array of peripherals: terminals, printers, color monitors and disk drives.

CONTACT YOUR CROMEMCO REP

There is even more capability than we're able to describe here.

Contact your Cromemco rep now and get this capability working for you.

CROMEMCO COMPUTER CARDS

- **PROCESSORS** — 4 MHz Z-80 A CPU, single card computer, I/O processor • **MEMORY** — up to 64K including special 48K and 16K two-port RAMS and our very well known BYTESAVERS® with PROM programming capability • **HIGH RESOLUTION COLOR GRAPHICS** — our SDI offers up to 754 x 482 pixel resolution. • **GENERAL PURPOSE INTERFACES** —QUADART four-channel serial communications, TU-ART two-channel parallel and two-channel serial, 8PIO 8-port parallel, 4PIO 4-port isolated parallel, D+7A 7-channel D/A and A/D converter, printer interface, floppy disk controller with RS-232 interface and system diagnostics, wire-wrap and extender cards for your development work.

Cromemco™
incorporated
280 BERNARDO AVE., MOUNTAIN VIEW, CA 94040 • (415) 964-7400
Tomorrow's computers today

CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN®

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

JUNE 1981

VOLUME 20, NUMBER 6

DEPARTMENTS

9 **EDITORIAL**

14 **CALENDAR**

20 **LETTERS TO THE EDITOR**

25 **COMMUNICATION CHANNEL**

Statistical multiplexers have brought considerable sophistication to data communications and have added a number of features that enhance data network design. There are a few constraints that must be observed, however, before they are applied to a system

50 **TECHNOLOGY REVIEW**

76 **DIGITAL CONTROL AND AUTOMATION SYSTEMS**

Microprocessor based user programmable plant management system employs intelligent remote controllers to reduce energy consumption throughout half million square foot complex

156 **MICRO DATA STACK**

A 2-wire interlocked handshake procedure synchronizes data transfer between talker and listener 8080A based microcomputers in a double-buffered, conditional I/O system

174 **AROUND THE IC LOOP**

Peripheral to the central processor, universal interrupt controllers improve system throughput and response time by allowing external devices to asynchronously modify the instruction sequence

190 **PRODUCTS**

226 **LITERATURE**

229 **SYSTEMS SHOWCASE**

230 **ADVERTISERS' INDEX**

Reader Service Cards
pages 233-236

Cover Artist: Darcy Gerbarg
Cromemco
Time Arts Synthesis, Mountain View, Calif.
John Dunn, Director

Number of copies printed this issue—87,900

SPECIAL REPORT ON SYSTEMS SOFTWARE

87

FEATURES

BUBBLE MEMORY CIRCUITS PROMOTE 3-DIMENSIONAL STACKING 135

by Russell MacDonald

Interface circuit flexibility of high performance bubble memories gives designers a competitive edge in customizing transfer rate, storage capacity, and access technique for a variety of host processors and storage applications

IEEE 488 ERROR HANDLING TECHNIQUES: PROS AND CONS 143

by Louis F. Santora, Jr

Comparison of several methods to detect and report errors enables designers of IEEE 488 based instruments to reduce controller overhead without adding system integration constraints

FPLA ARBITER CONCEPT ADAPTS TO APPLICATION NEEDS 149

by Alan W. Bentley

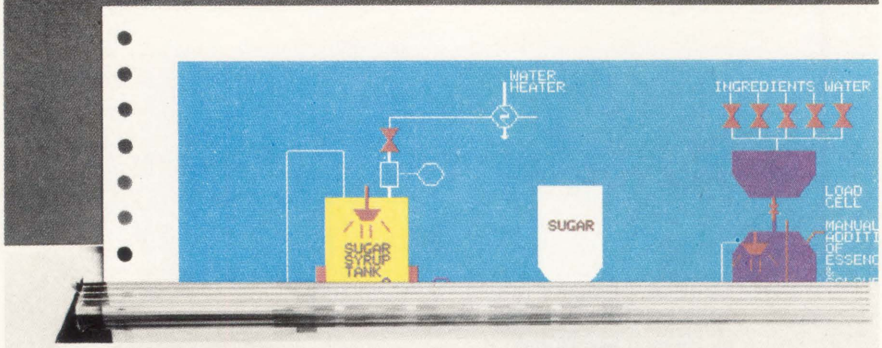
Customizable arbiter concept uses versatile Boolean statement format to implement control protocol and grant algorithms in field programmable logic

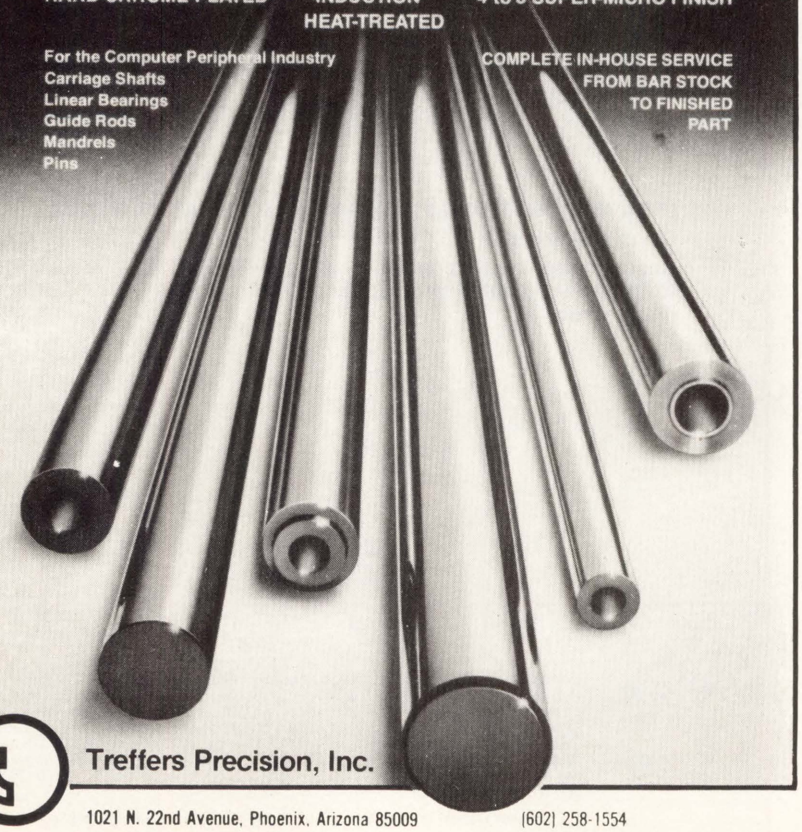
BPA

ABP

Computer Design® is published monthly. Copyright 1981 by Computer Design Publishing Co, a division of PennWell Publishing Co. Controlled circulation postage paid at Tulsa, Okla. No material may be reprinted without permission. Postmaster: CHANGE OF ADDRESS—FORM 3579 to be sent to Computer Design, Circulation Dept, PO Box A, Winchester, MA 01890. Subscription rate is $30.00 in U.S.A., Canada, and Mexico, and $50.00 elsewhere. Microfilm copies of Computer Design are available and may be purchased from University Microfilms, a Xerox Company, 300 N Zeeb Rd, Ann Arbor, MI 48106 (USPS 127-340)

® Computer Design is a registered trademark of Computer Design Publishing Company





CD* STAFF

Publisher
Ronald W. Evans
President & Founder
Robert Brotherston

Editorial
Editor
Saul B. Dinman
Managing Editor
Sydney F. Shapiro
Technical Editor
Shawn Spilman
Senior Editor
Peg Killmon
Field Editor S. Calif & SW
(213) 824-5438
Michael Chester
Field Editor N. Calif & NW
(408) 371-8901
Douglas Eidsmore
Associate Editors
James W. Hughes **Colleen G. da Silva**
Copy Editors
Sue Paxman **Debra M. Highberger**
Jun U. Smith
Editorial Advisory Board
Brian W. Pollard **Ralph J. Preiss**
Rex Rice

Circulation
Circulation Director
Robert P. Dromgoole
Data Control Manager
Wanda Holt
Circulation Manager
Alma Brotherston

Production
Production Manager
Linda M. Wright
Production Assistant
Lou Ann Sawyer
Advertising Coordinators
Sally H. Bowers **Cherie Crosby**
Technical Art
Concepts Unlimited

Marketing
Director of Marketing
Gene Pritchard
Marketing Services Manager
Linda G. Clark
Promotion Manager
Tom Hodges

Financial
Administrative Director
John O. McGillivray
Controller
David C. Ciommo

Computer System
Research Director
Wayne Newman

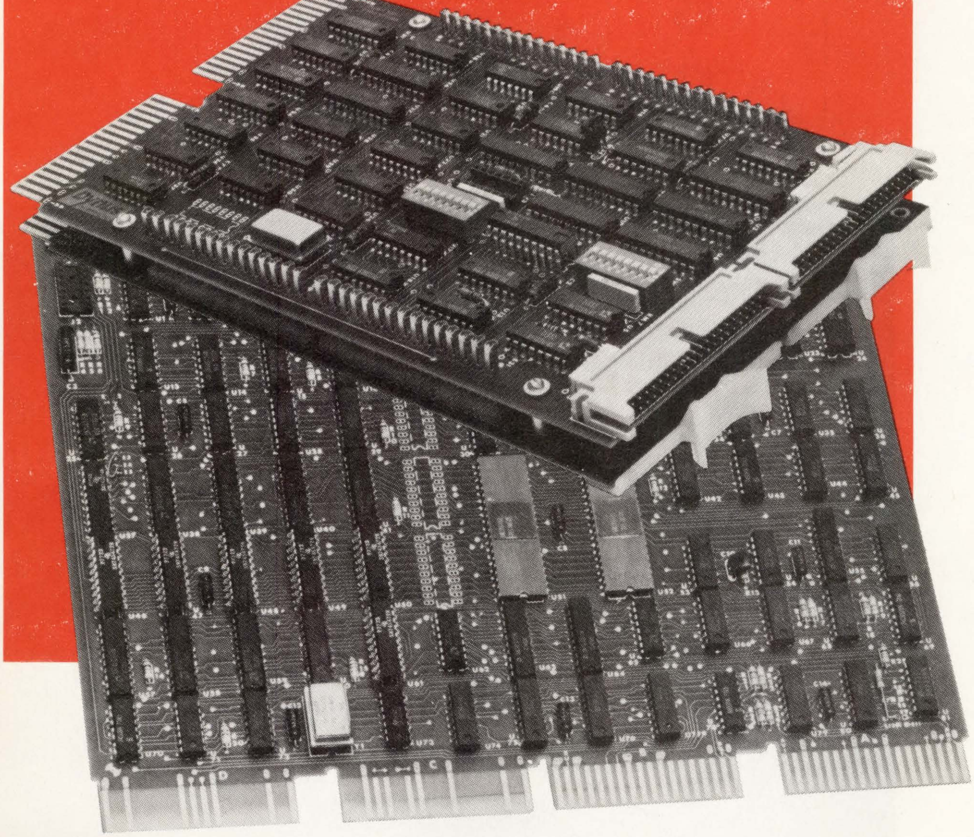
Editorial & Executive Offices
11 Goldsmith St, Littleton, MA 01460
Tel. (617) 486-8944/(617) 646-7872

Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

*(TM)

DEC®-COMPATIBLE PERIPHERAL CONTROLLERS

ALSO FROM DATARAM
JUST ANNOUNCED
PDP 11/44
MEMORY



Now, from the company that delivers the industry's widest range of DEC-compatible memory products, a family of peripheral controllers that's second to none. From comparatively simple cartridge disk controllers to complex 300MB storage module drive (SMD) controllers.

An impressive array of state-of-the-art controllers, all built around high-speed bipolar microprocessors. All software compatible with the host LSI-11® or PDP®-11 minicomputer...and all available now.

And Dataram's controllers are designed to save you money, and a lot more. Like space — our controllers typically occupy half the space required for the comparable controller from DEC. Doing it with a level of performance that makes any member of this family worth looking at.

Look at the chart of our current family of peripheral controllers, growing every day. If you don't see the controller you need, we're probably working on it right now. Call us and discuss your requirements.

DEC, LSI-11 and PDP are registered trademarks of Digital Equipment Corporation.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

DATARAM CONTROLLER	Magnetic Tape Controller			Cartridge Disk Controller		SMD Controller					
	T03	T04	T34	C03	C33	S03/A	S03/B	S03/C	S33/A	S33/B	S33/C
MINI	LSI-11	LSI-11	PDP-11	LSI-11	PDP-11	LSI-11	LSI-11	LSI-11	PDP-11	PDP-11	PDP-11
COMPATIBILITY	TM11/TU10			RK05		RM02	RK07	RP06	RM02	RK07	RP06

CIRCLE 6 ON INQUIRY CARD

TEK 7D02 LOGIC ANALYZER

The logic analyzer for

The solution to your problems.

Now. A logic analyzer made expressly for microprocessor-based design.

The Tektronix 7D02.

An instrument that provides solutions instead of compounding problems. That cuts design time and improves cost-effectiveness.

Look at just a few examples:

Design Problem: Adapting your logic analyzer to work with a specific processor.

7D02 Solution: Just plug the µP-specific 7D02 probe directly into the prototype microprocessor socket and press START. Acquired data is immediately disassembled and displayed in your processor's own mnemonics.

Design Problem: Sorting error-related data from other program flow.

7D02 Solution: Programmable data and clock qualification filters the data and stores only information pertinent to the problem.

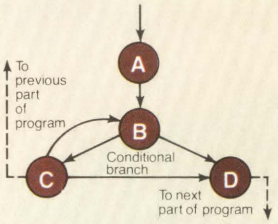
Design Problem: Relating hardware activity to program flow.

7D02 Solution: State and timing sections are included in a single logic analyzer, with each section able to trigger or qualify data acquisition by the other.

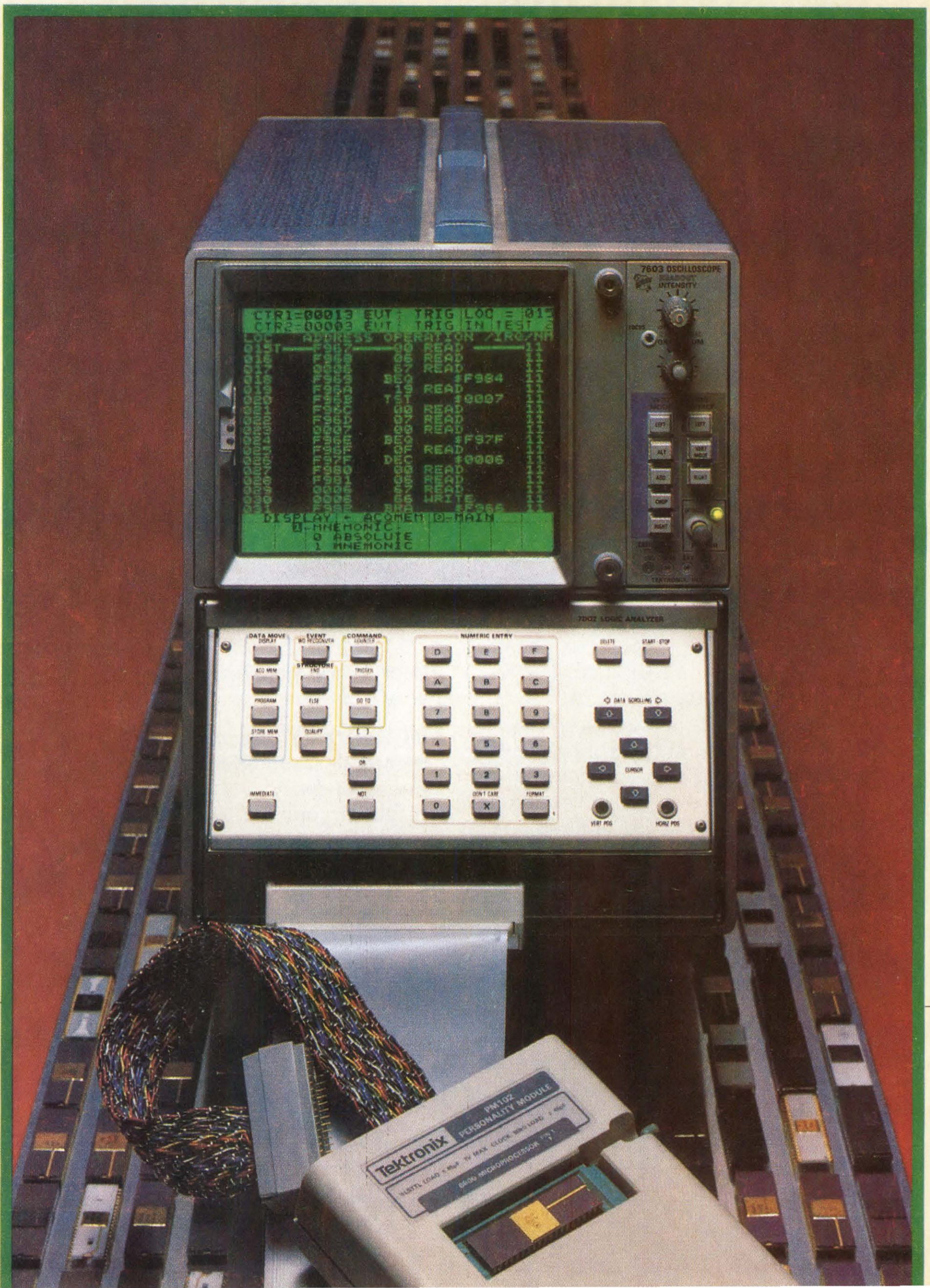
Design Problem: Monitoring I/O activity on the system bus.

7D02 Solution: Acquire both synchronous and asynchronous data through interactive triggering to examine both slides of an I/O transaction.

Design Problem: Tracking program flow through non-sequential algorithms with conditional branches to pinpoint an error.



7D02 Solution: The 7D02 can monitor multiple events and conditionally branch as part of its trigger or data qualification sequence. As a result, it can detect an error condition anywhere in your program flow.



microprocessor–based design.

7D02. The solution.
No matter how you look at it, the 7D02 has what you need for faster, more efficient microprocessor-based design.

A series of probe modules adapt the 7D02 to major 8-bit and 16-bit processors, both now and in the future. There's also a general purpose probe for use with microprocessors not specifically supported today. It may also be used like a conventional logic analyzer for troubleshooting the peripheral elements of the system you're designing.

You can have up to 52 channels of synchronous data acquisition, of which 8 channels can be used to acquire asynchronous data at speeds to 50 MHz for timing analysis.

Data acquisition resources include four word recognizers and two interactive counters that can be reset on the fly. Also several modes of both data and clock qualification.

You get two levels of glitch triggering with a resolution of 5 ns, and a separate glitch memory. Plus separate acquisition and reference memories for quick data comparisons.

And all the 7D02's resources are quickly and clearly configurable through a simple user language. One that lets you trigger right on a problem instead of around it. Minimum programming input yields maximum insight into your prototype's software and hardware activity.

For more information on the 7D02, contact your Tek Sales Engineer or call us toll-free. 1-800-547-6711.

You'll wonder how you ever designed without it.

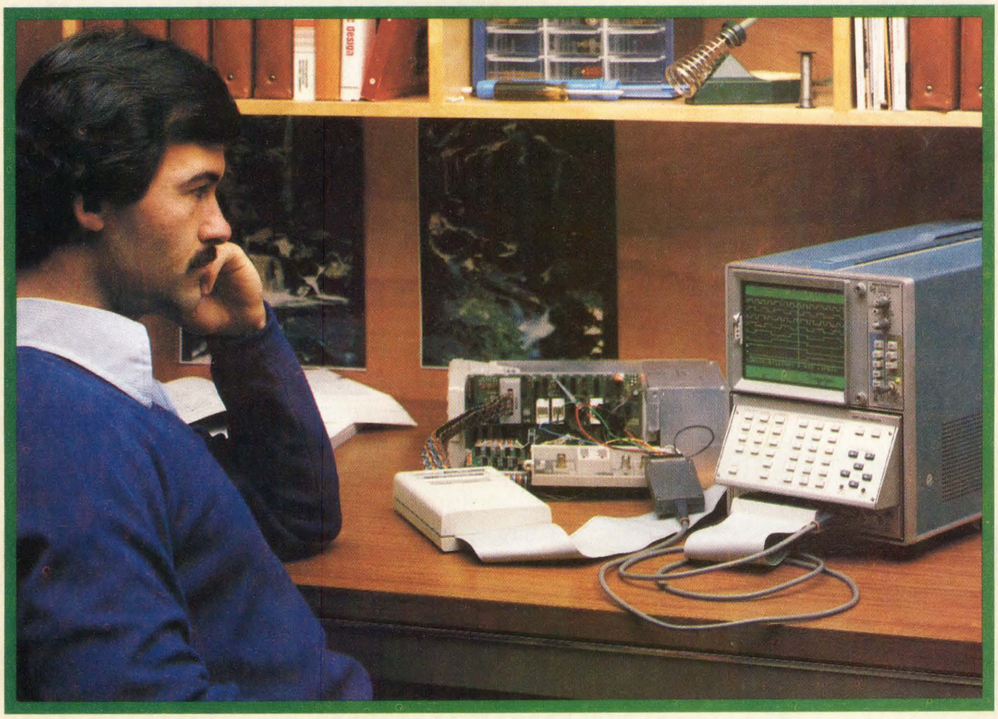
For further information, contact:

U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc.
P.O. Box 4828
Portland, OR 97208
Phone: 800/547-6711
Oregon only 800/452-6773
Telex: 910-467-8708
Cable: TEKTRONIX

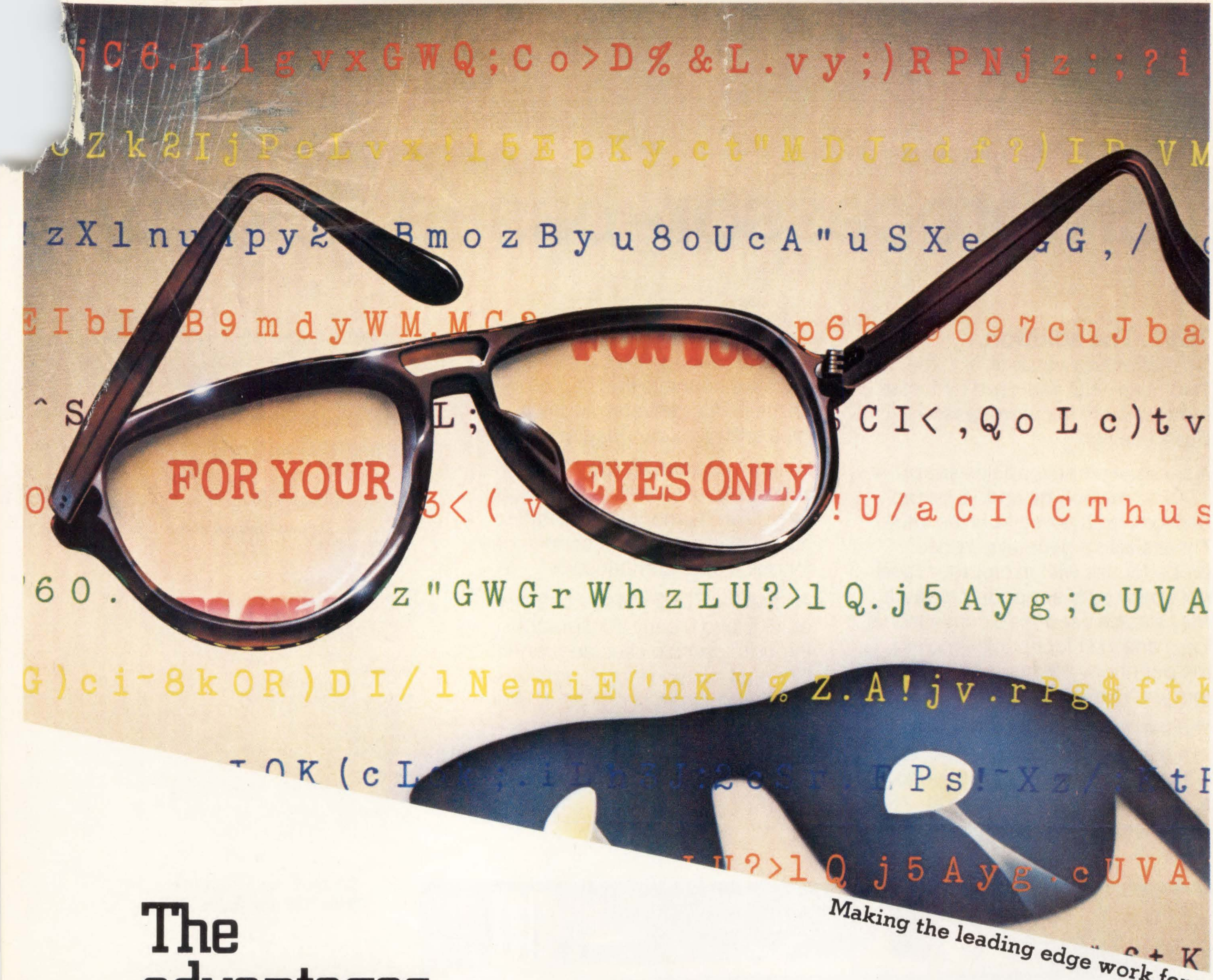
Europe, Africa, Middle East
Tektronix International, Inc.
European Marketing Centre
Postbox 827
1180 AV Amstelveen
The Netherlands
Telex: 18312

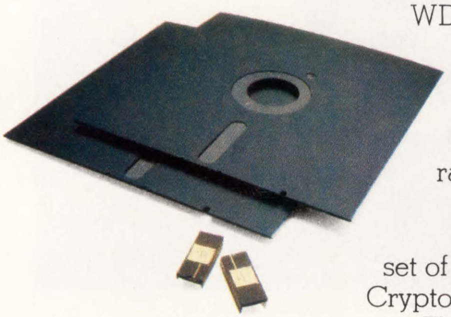
Canada
Tektronix Canada Inc.
P.O. Box 6500
Barrie, Ontario L4M 4V3
Phone: 705/737-2700

Circle 7 for Literature
Circle 147 for Sales Call

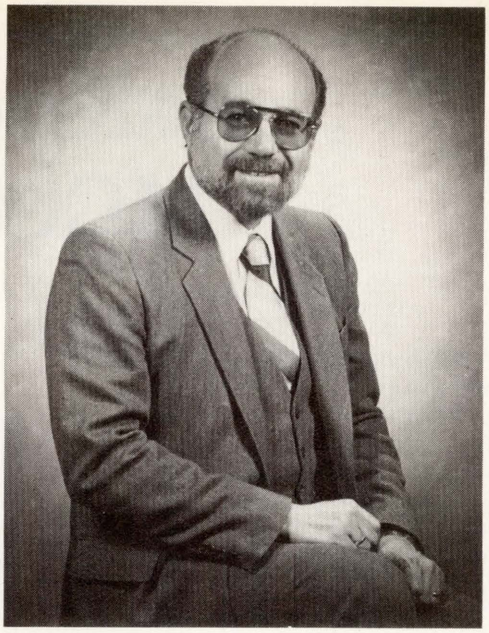


Tektronix®
COMMITTED TO EXCELLENCE


FOR YOUR EYES ONLY



WARNING: emi radiation could be hazardous to your company's health



My attention was recently redirected to FCC Rules and Regulations parts 2 and 15 as amended to encompass digital equipment. While attending NCC, I thought it might be interesting to take a quick straw poll on the floor of the show to see what, if any, is the level of awareness of the FCC emi (electromagnetic interference) regulations. The variety of answers received was interesting, and a casual check of the backs of various pieces of equipments that are already subject to parts of the new regulations showed that just a few manufacturers are in compliance with the FCC labeling requirements that have been in effect since January 1, 1981.

Briefly, those amendments to parts 2 and 15 set forth restrictions on the level of permissable emi that a piece of digital equipment may generate. The law comes in two flavors: one for commercial equipment and a more stringent version for equipment used in the home.

If you have any doubts whether or not digital devices radiate rf energy, try this simple test (probably invented by an old IBM 704 operator). Take one of the currently popular calculators (the more complex, the better), turn it on, and hold a small pocket radio near it. Tune the dial on the radio and listen to the assortment of squawks and squeaks—that's emi. Chances are that the only activities going on are a keyboard scan loop and the display multiplexing—think what happens when one of those plastic-encased desktop micro wizards is doing an ISAM update!

These FCC regulations could have the same earmarks of a potential disaster for our industry as did the early EPA automobile emission standards for the automobile industry. It is also a pretty safe bet that they are not going to disappear into a haze of deregulation.

We'd like to take a quickie editorial poll of you, our readers, while there is still time before the commercial equipment (class A) deadline of October 1, 1981. We will tabulate the results on our own noise generating system and promise to lose everyone's identity. We will keep you informed on the results as we compile them and use them to guide us in the selection of future articles on the subject.

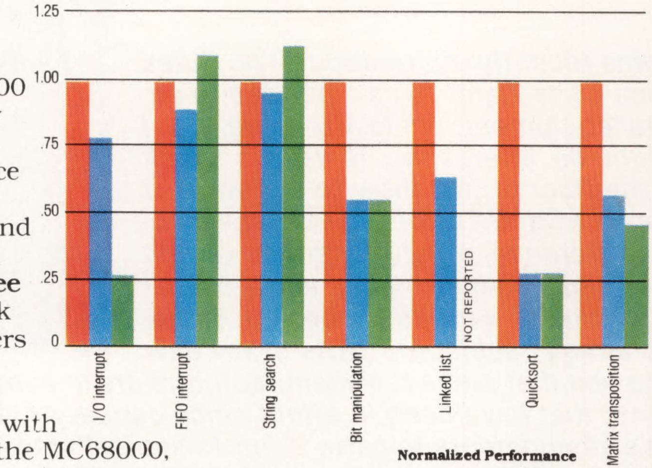
Please indicate your answers by circling the appropriate numbers in the score box of the reader service card.

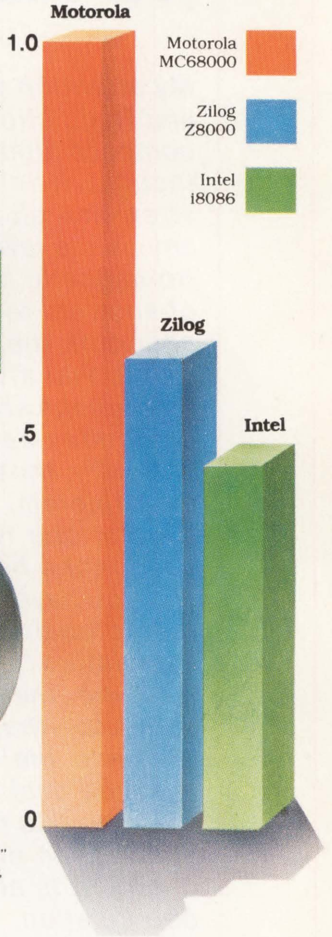
Saul B. Dinman

Saul B. Dinman
Editor

Circle 426	Yes, I am aware of the new FCC emi regulations.
Circle 427	We are in the process of complying.
Circle 428	No, I am not aware of them.
Circle 429	I would like to see more information on the subject in print.

Independent benchmarks MC68000 is first choice





Motorola's advanced MC68000 microprocessor is demonstrably superior for a broad range of 16-bit applications. The evidence is in, and it's conclusive.

The MC68000 consistently and significantly outperformed both the Z8000 and the i8086 in **three** current independent benchmark studies. Evaluations by engineers not associated with any microprocessor supplier demonstrate that the microprocessor system with the best overall performance is the MC68000, making it the clear choice for new designs.

And it's clear that the MC68000 is now recognized as the competitive edge for end-use systems. Design engineers recently confirmed that it is the first choice among 16-bit microprocessors in two independent product preference polls.*

Benchmarks measure MC68000 performance advantages.

Results of a performance comparison for a digital filter application by V.P. Nelson and H. T. Nagle, published in *IEEE Micro*, find the MC68000 nearly twice as fast as the Z8000 and almost three times as fast as the i8086.

A variety of benchmarks from the Carnegie-Mellon series as reported in *EDN* magazine by Grappel and Hemenway show that the MC68000 is significantly faster than each of these devices in handling routines for Bit Test/Set/Reset, Linked Lists,† Quicksort, and Boolean Matrix. In the same study, it also compares favorably for I/O interrupts. Overall, it outperforms the i8086 by 2.16 to 1.0 and the Z8000 by 1.71 to 1.0, even with the MC68000 addressing its full 16-Megabyte address space and the other two MPUs addressing only 64K.

Benchmarks from the Blacksburg Group, being published by Howard W. Sams and Co., indicate that the MC68000 is two times to three times as fast in four‡ out of five routines compared, including Sorts, Square Root, and Sine Look-up.

Still other benchmarks give the edge to the MC68000 for execution of multiprecision binary and BCD arithmetic operations, 32-bit array scans and string translations. Floating Point arithmetic operations can be carried out almost as fast as hardware implementations.

Results reported in "A Tale of Four MPUs: Benchmarks Quantify Performance," Robert D. Grappel and Jack E. Hemenway, April 1, 1981 EDN Magazine, *a Cahners Publication*

Memory address, 32-bit features enhance performance.

The performance advantages of the MC68000 demonstrated in the studies are impressive. And the MC68000 has still other capabilities of equal importance in helping keep you ahead of your competition.

The MC68000 has seventeen 32-bit multipurpose registers, with data and address registers separated for parallel operation. All registers can be used as index registers, and all address registers can be used as stack pointers.

No other 16-bit MPU can match the 16-Megabyte direct memory addressing, and programmers need not worry about segmentation and the overhead associated with it.

The simple, efficient instruction set includes 56 powerful types designed to minimize the number of mnemonics a programmer must know. Software development costs are minimized because addressing modes are usable with all applicable instructions.

One other thing. The MC68000 provides, in one high-quality device, what is often found in multi-

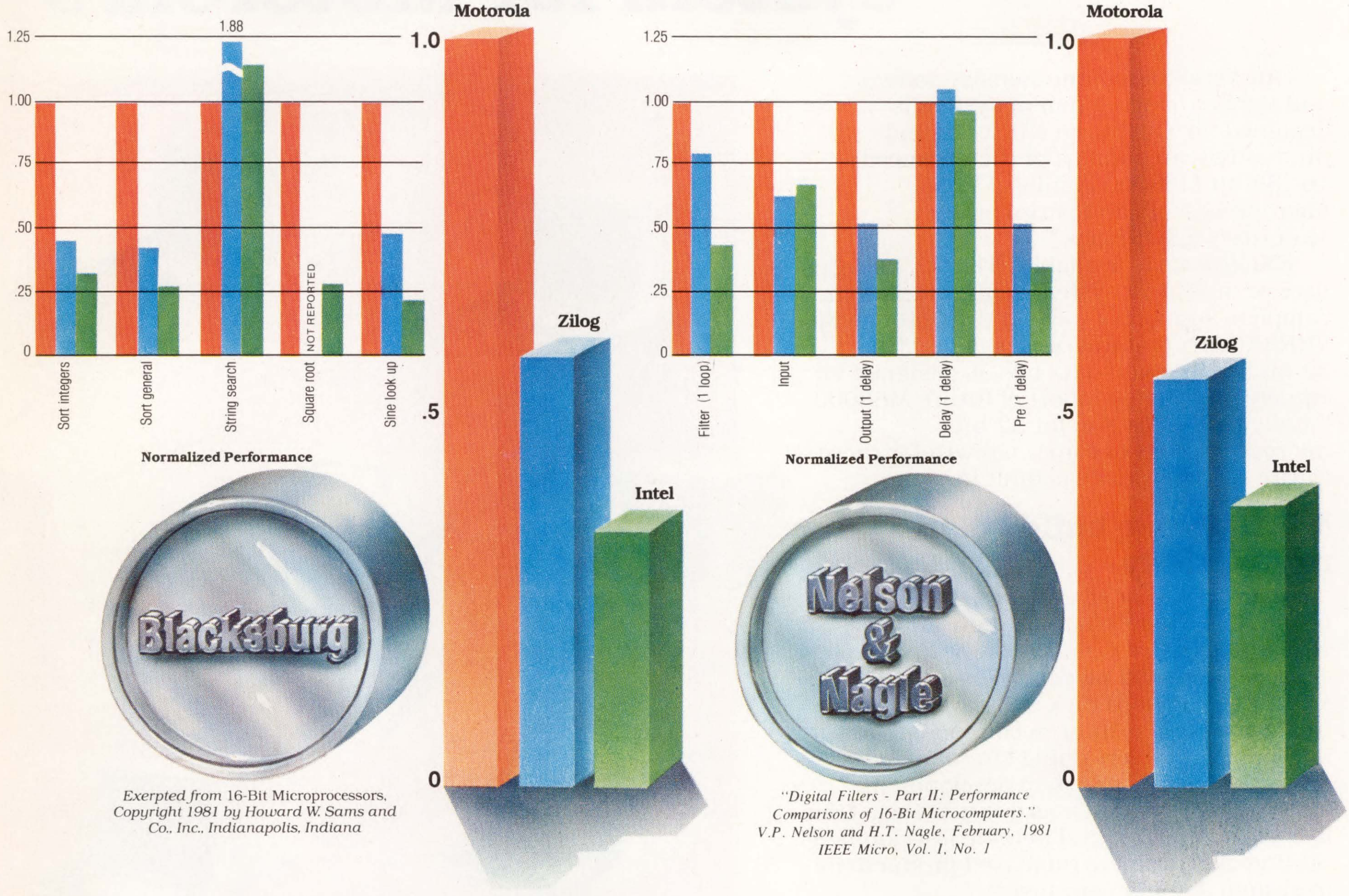
**Annual Minicomputer Survey, November 1980,* with permission of DATAMATION MAGAZINE, G.S. Grumman/Cowen & Co.

**Electronics 1980 Product Preference Poll,* with permission of ELECTRONICS MAGAZINE, McGraw-Hill, Inc.

†Not reported for i8086, but Motorola data indicates the MC68000 is more than 20% faster.

‡No report for Z8000 on Linked List.

demonstrate why the for 16-bit MPU applications.



Exerpted from 16-Bit Microprocessors, Copyright 1981 by Howard W. Sams and Co., Inc., Indianapolis, Indiana

"Digital Filters - Part II: Performance Comparisons of 16-Bit Microcomputers." V.P. Nelson and H.T. Nagle, February, 1981 IEEE Micro, Vol. 1, No. 1

chip arrangements requiring more interconnects, bus coordination, space and cost.

Keep your systems state-of-the-art.

In addition to the MC68000 microprocessor, Motorola's well-rounded family of existing and future VLSI peripherals is designed so that you can keep your M68000-based systems state-of-the-art for years. And, the 8-bit M6800 Family peripherals interface directly with the MC68000, broadening support with an attractive low-cost, medium-performance option.

Future, extra-performance versions of the MC68000 will be completely bus- and object code-compatible with the present MPU. Upgrading or expanding your system is achieved without making your software obsolete, regardless of the language in which it is written.

The M68000 Family is supported by EXORmacs™, the multiuser development system created for the 16-bit and 32-bit M68000 Family designs, and beyond.

For more information on the MC68000 and the M68000 Family, complete and mail the coupon or send your written request to Motorola Semiconductor Products, Inc., P.O. Box 29012, Phoenix, AZ 85036.

Use the MPU that can make your 16-/32-bit system a winner. Commit yourself to leadership with the M68000 Family in

Innovative systems
through silicon.

MOTOROLA INC.

TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.
92CD6/81

Please send me information on MC68000.

Name __________

Title __________ Tel.: (___)

Company __________

Address/Mail Drop __________

City __________

State __________ ZIP __________

Technological leadership.

EXORmacs.™ The one advanced system for Motorola's

One versatile, comprehensive software and hardware development system is designed for maximum efficiency and productivity in support of the advanced 16-/32-bit M68000 Family of VLSI microprocessors and peripherals. Motorola's EXORmacs™.

EXORmacs is available in either a single-user or multiuser system configuration for complete support of today's M68000 Family. VERSAbus™, Motorola's new-generation 32-bit address and data bus, is designed for equally thorough support of future M68000 Family variations and for 32-bit microprocessors to come. Growth for these future 32-bit systems is built in.

Multiple use builds high productivity.

Maximum cost effectiveness is achieved in the multiuser system configuration. A single package, consisting of the EXORmacs chassis, up to 192 megabytes of mass storage in the hard disk subsystem, and a high-speed line printer, accommodates as many as eight users doing simultaneous hardware/software system development. Optional add-ons such as our new Real-Time Bus State Analyzer and Remote Development Station also promote increased productivity in system development tasks.

The result is highly efficient project management in one system. Multiple users are simultaneously updated with each software revision and get all the benefits of timesharing.

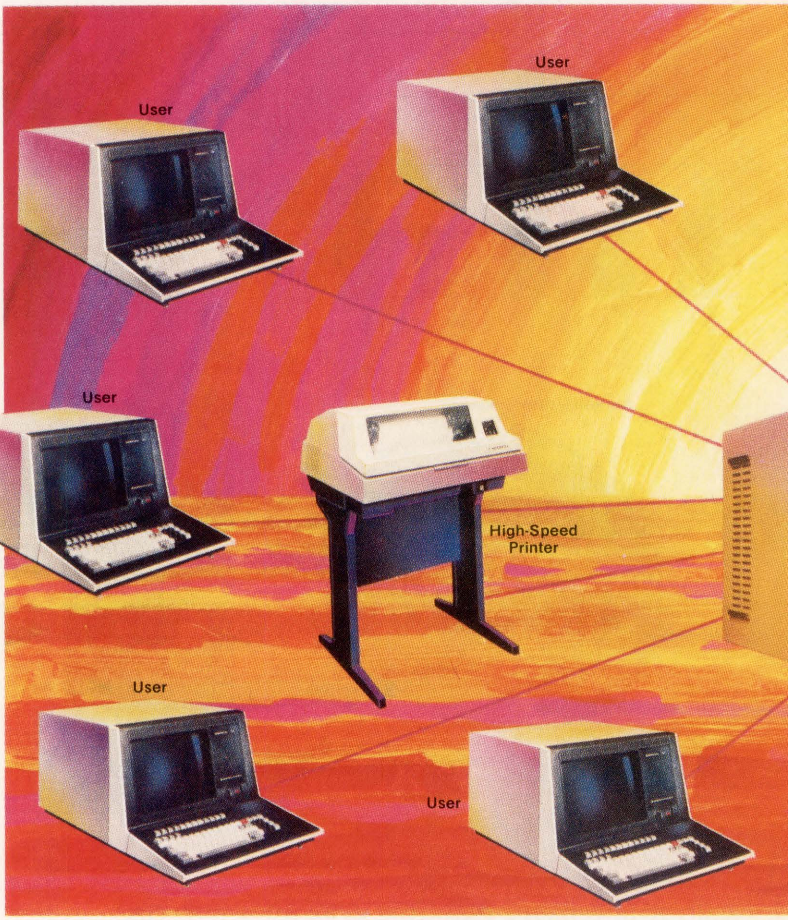
Advanced Real-Time Operating System — VERSAdos™.

EXORmacs uses a real-time multitasking, multiuser operating system called VERSAdos, in which a real-time executive provides essential task services and supports hardware memory management for memory allocation and protection. The input/output structure of the operating system supports device independence, logical as well as physical I/O, and overlapped I/O and computation.

The combination of bus arbitration logic and a sophisticated multilevel priority interrupt structure supports flexible multiprocessing capability.

System bus meets high-performance requirements.

VERSAbus is Motorola's advanced computer bus designed to meet requirements of a new generation of microprocessor-based systems. It supports a wide variety of 8-bit to 32-bit MPU architectures with high data transfer rates, and provides a flexible, economical architecture for serving industrial control, communications or general business applications.

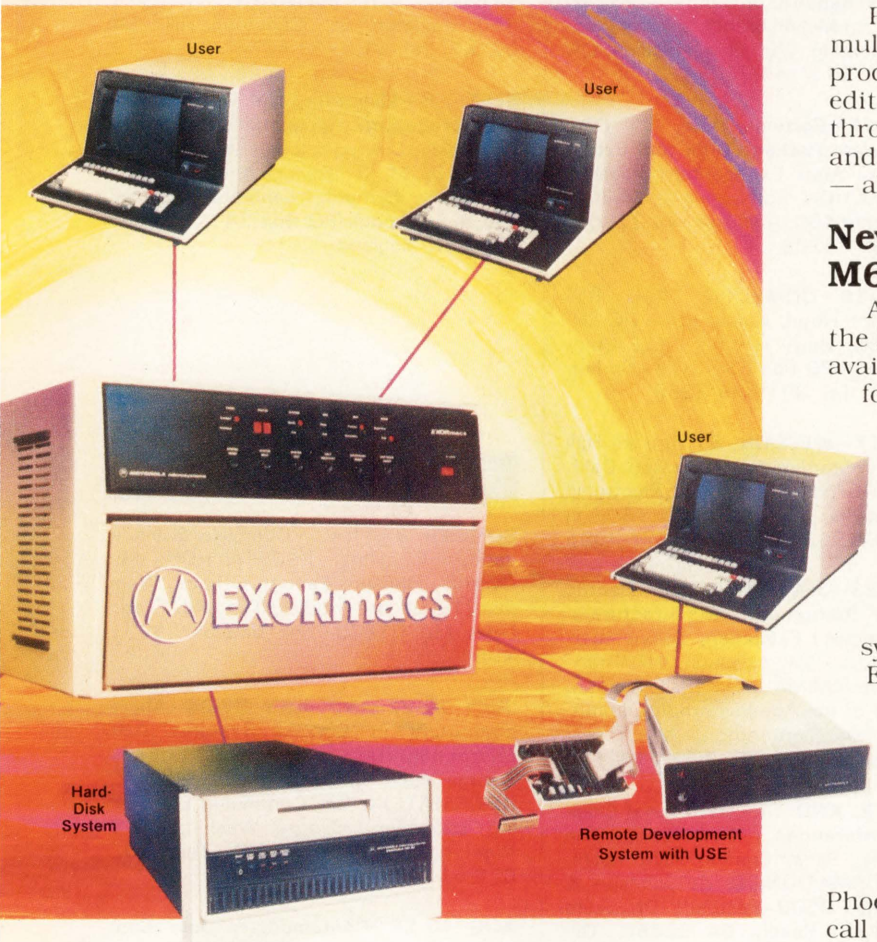


And VERSAbus easily accommodates multiple-user terminals interfaced via the EXORmacs system's MC6801-based multichannel serial communications modules. All EXORmacs peripheral device controllers are based on Motorola's Intelligent Peripheral Controller (IPC) architecture. This relieves the main MC68000 processor of I/O processing details and increases the raw computer power available.

High-efficiency software tools.

EXORmacs software is as advanced and practical as the hardware. The Pascal compiler is self documenting and promotes efficient programming technique, simplifying program maintenance. Motorola extensions of the

multiuser development M68000 Family... and more.



user-oriented Pascal high-level language include string operations, runtime error checking, long/short integers, runtime file assignment and separate compilaton and linking. A structured macro-assembler, a CRT-oriented text editor and a linkage editor for combining modularly-written procedures also are included.

The M68000 User System Emulator (USE), enables the user to extend the EXORmacs development system resources into his target system. It supports system software debug in real time and provides convenient circuit isolation for fault detection.

System debug activities also are streamlined by the new optional Remote Development Station (RDS), a separate chassis with USE capability which is interconnected to the main EXORmacs chassis through a serial link. Hardware and software development activities can proceed independently at one or more RDS units without conflict with ongoing software development at other user terminals.

Possibly the greatest impact of the multiuser EXORmacs system is in the productivity of its software resources. Faster editing, compilation and assembly, the high throughput of the hard disk, the efficiency and power of the VERSAdos operating system — all help curb spiraling software costs.

New EXORmacs software for M6800 family support.

A Macro assembler and linkage editor for the MC6809 are scheduled for mid-1981 availability, with similar development support for the MC6800, MC6801, and MC6805 to be offered by year end.

In short, multiuser EXORmacs is an all-round effective system which reduces equipment and space requirements, reduces the average cost per user and maximizes software productivity. EXORmacs also supports VERSAmodule™ 16-bit board-level system design.

EXORmacs has one final advantage. No other development system can match it in supporting M68000 Family microprocessors and VLSI peripherals. Only EXORmacs is from Motorola.

For additional information, write to Motorola Semiconductor Products Inc., Microsystems, P.O. Box 20912, Phoenix, AZ 85036, use the coupon below or call (602) 244-5714.

The EXORmacs advanced development system is designed to make it easy for you to apply MPUs from 8 bits to 32 bits in

Innovative systems
through silicon.

MOTOROLA INC.

TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

Please send me information on EXORmacs™

88 CD 6/81

Name ______________________

Title ______________ Tel.: (   ) ______________

Company ______________________

Address ______________________

City ______________________

State ______________ ZIP ______________

CALENDAR

CONFERENCES

JULY 21-22—Sym on Reliability in Distributed Software and Database Systems, Pittsburgh, Pa. INFORMATION: Marie S. Hreha, LRDC Bldg, U of Pittsburgh, Pittsburgh, PA 15260. Tel: 412/624-4908

AUG 3-5—Pattern Recognition and Image Processing, Sheraton Hotel, Dallas, Tex. INFORMATION: PRIP, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

AUG 3-7—ACM (Assoc for Computing Machinery) Siggraph '81, Dallas, Tex. INFORMATION: Dr Anthony Lucido, Intercomp, 1201 Dairy Ashford, Houston, TX 77079. Tel: 713/497-8400

AUG 5-7—SYMSAC '81 (Assoc for Computing Machinery), Snowbird Ski Resort, Salt Lake City, Ut. INFORMATION: Prof B. F. Caviness, Dept of Mathematical Sciences, Rensselaer Polytechnic Inst, Troy, NY 12181. Tel: 518/270-6731

AUG 11-14—Electronics '81, Mexico City, Mexico. INFORMATION: Franc D. Manzolillo, Proj Mgr, Rm 6015, U.S. Department of Commerce, Washington, DC 20230. Tel: 202/377-2991

AUG 12-15—NYCE (New York Computer Expo), Sheraton Centre, New York, NY. INFORMATION: NYCE, 110 Charlotte Pl, Englewood Cliffs, NJ 07632. Tel: 201/569-8542

AUG 18-21—VLSI (Very Large Scale Integration) '81 Internat'l Conf, University of Edinburgh, Edinburgh, Scotland. INFORMATION: Secretariat, VLSI '81 Internat'l Conf, 26 Albany St, Edinburgh EH1 3QH, Scotland

AUG 24-28—IFAC (Internat'l Federation for Automatic Control) World Congress, Kyoto, Japan. INFORMATION: IFAC '81 Secretariat, Kinki Hatsumei Ctr, 14 Kawahara-cho, Yoshida, Sakyo-ku, Kyoto 606, Japan

AUG 24-28—Internat'l Joint Conf on Artificial Intelligence, Vancouver, British Columbia, Canada. INFORMATION: Richard Rosenberg, Computer Science Dept, U of British Columbia, Vancouver, BC V6T 1W5, Canada. Tel: 604/228-3061

AUG 25-28—1981 Internat'l Conf on Parallel Processing, Shanty Creek Lodge, Bellaire, Mich. INFORMATION: Dr M. T. Liu, Dept of Computer and Information Science, Ohio State U, Columbus, OH 43210. Tel: 614/422-1837

AUG 26-29—Nat'l Small Computer Show, New York Coliseum, New York, NY. INFORMATION: Nat'l Small Computer Show, 110 Charlotte Pl, Englewood Cliffs, NJ 07632. Tel: 201/569-8542

SEPT 8-9—Internat'l Conf on Computer Hardware Description Languages and Their Applications, Kaiserslautern University, Federal Republic of Germany. INFORMATION: Prof Melvin Breuer, Dept of Electrical Engineering, USC, Los Angeles, CA 90007. Tel: 213/743-2308

SEPT 14-17—Software Info '81 (The Nat'l Software Package Conf and Expo), Merchandise Mart Expocenter, Chicago, Ill. INFORMATION: Software Info, 1730 N Lynn St, Suite 400, Arlington, VA 22209. Tel: 703/521-6209

SEPT 14-18—COMPCON FALL '81, Capital Hilton Hotel, Washington, DC. INFORMATION: Harry Hayman, IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

SEPT 15-17—WESCON '81, Brooks Hall and Civic Auditorium, San Francisco, Calif. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

OCT 19-23—JEMIMA (Japan Electric Measuring Instruments Manufacturers' Assoc) Internat'l Exhibition, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: 19th JEMIMA Internat'l Exhibition, Secretariat of the Administration Committee, 1-9-10, Toranomon, Minato-ku, Tokyo 105, Japan. Tel: 03/502-0601, X4

NOV 5, 12, AND 17—Invitational Computer Conferences, Amsterdam, The Netherlands; Paris, France; AND Milan, Italy. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

NOV 9-13—IECI '81 (Internat'l Conf and Exhibit on Industrial Control and Instrumentation—Applications of Mini- and Microcomputers), Hyatt Regency Hotel, San Francisco, Calif. INFORMATION: J. D. Irwin, Electrical Engineering Dept, Auburn U, Auburn, AL 36830. Tel: 205/826-4330

SPRING-SUMMER '81—Data Communications and Computer Graphics Series, various locations. INFORMATION: Karen Smolens, Ctr for Management Research, 850 Boylston St, Chestnut Hill, MA 02167. Tel: 617/738-5020

SEPT 7-8—Microprocessor Workshop on Microprocessor Applications, Liverpool University, Liverpool, England. INFORMATION: Dr M. J. Taylor, Microprocessor Workshop, Computer Laboratory, University of Liverpool, PO Box 147, Liverpool L69 3BX, England

SEMINARS

SUMMER-FALL '81—Introductory, 8080/8085 and 8086/8088 Systems Design, Single-Chip Microcomputer, Peripheral Chip Design, and Development Systems Workshops, various locations. INFORMATION: Intel Training Ctr, San Francisco, Calif, tel: 408/734-8102; Chicago, Ill, tel: 312/981-7250; or Boston, Mass, tel: 617/256-1374

SHORT COURSES

SUMMER '81—Inst in Computer Science, various locations. INFORMATION: Mrs Cynthia Johnson, Faculty Offices, Wang Inst of Graduate Studies, Tyng Rd, Tyngsboro, MA 01879. Tel: 617/649-9731, X355

JULY 20-22 AND JULY 23-24—Microcomputers in Control Systems AND Microcomputer Interfacing Methods, George Washington U, Washington, DC. INFORMATION: Dir, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

AUG 10-14—Contemporary Data Communication Networks: Planning Analysis and Design, U of Michigan, Ann Arbor, Mich. INFORMATION: Dixon R. Doll, Continuing Engineering Education, 300 Chrysler Ctr, N Campus, Ann Arbor, MI 48109. Tel: 313/764-8490

Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance.

The DSD 880 can integrate with a VT103 Intelligent Terminal containing an LSI-11/23 to form a complete, powerful table-top microcomputer.

You deserve better data storage than you get from DEC.

For your LSI-11 or PDP®-11, bigger isn't better when it comes to data storage.

DEC® builds great computers. But if you want 7.8 megabytes of data storage, they give it to you in two ungainly boxes 21 inches high. Data Systems Design gives you one compact package 5¼ inches high, with an ultra-reliable 7.8 megabyte Winchester drive *and* a 0.5 megabyte single-sided floppy (or 1 megabyte double-sided) for I/O and integral backup, plus on-board diagnostics and lots of extras.

A superb buy—the DSD 880 DEC-compatible Winchester/Floppy Disk System.

Offering far better value than RX02 and RL01 combos or dual-RL01 or -RL02 disk drives, the DSD 880 provides more bytes per buck than any DEC alternative. And you save in other ways.

Less rack space means lower cabinetry costs. The 880 backplane interfaces require 70% less backplane space than a similar DEC configuration.

The comprehensive Hyper-Diagnostics™ panel and library of microprogrammed routines, in conjunction with Data Systems Design's Rapid Module Exchange™ program and HyperService™ service contracts, deliver more uptime for less than half the cost of a DEC service contract.

Fully compatible three ways.

DSD 880 is hardware compatible. It's the *only* high-capacity storage system that integrates with a VT103. And it integrates with any DEC LSI-11 or PDP-11 computer, or any DEC-computer-based system.

It's software compatible. You can use RT-11 or RSX-11 operating systems with RL01 (Winchester) and RX02 (floppy) handlers without modification. The DSD 880 runs all applicable DEC diagnostics and utilities.

And it's media compatible. Its floppies utilize DEC double-density or IBM single-density formats.

Want to know more? For full technical details, contact your regional sales office: Western (408) 727-3163; Eastern (617) 769-7620.

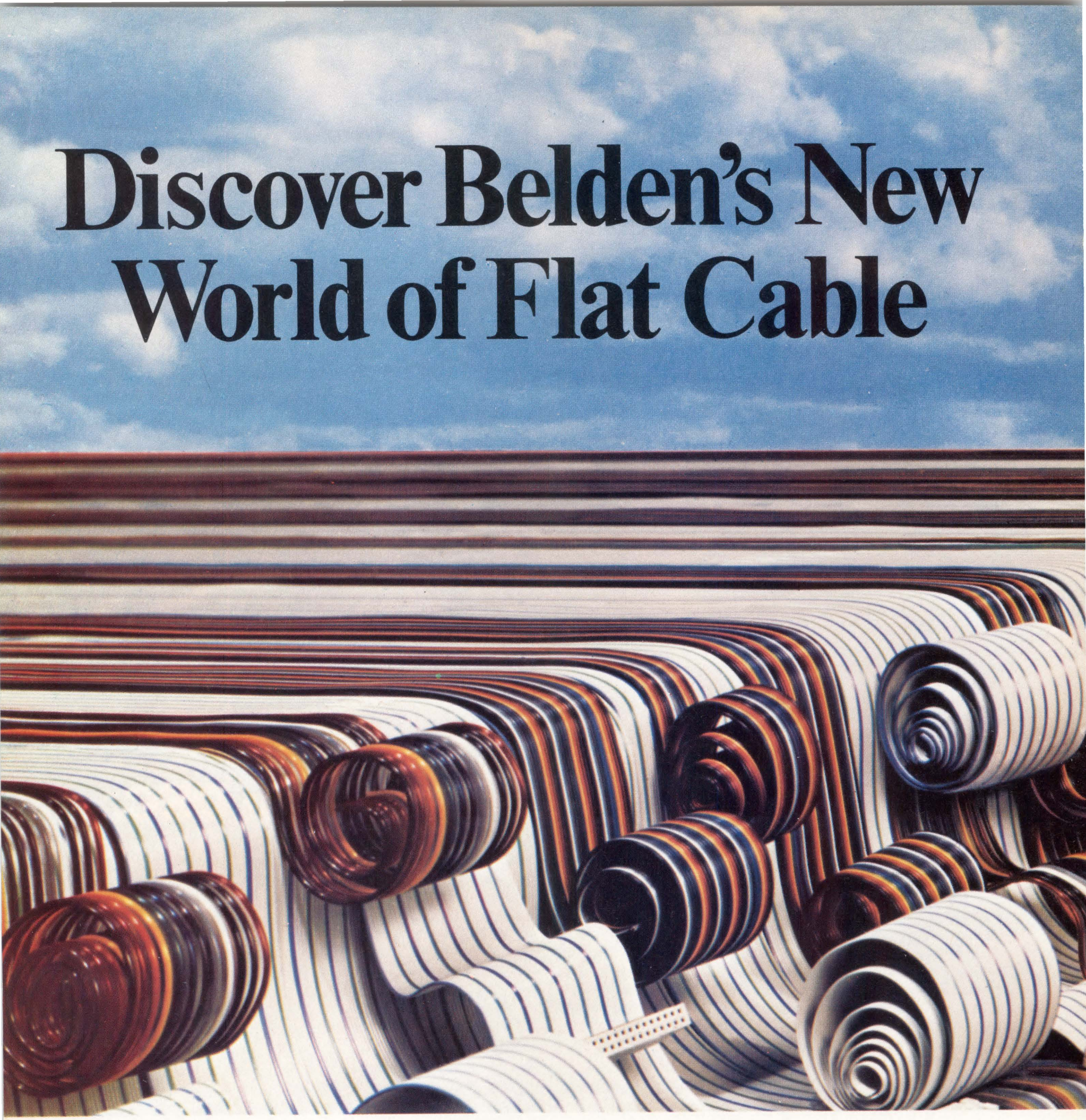
Data Systems

The Intelligent Alternative to DEC Disk Systems

International Sales: Australia: Melbourne (03) 543-2077, Sydney (02) 848-8533; Canada (416) 625-1907; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/95681 42; Israel 03/298783; Italy 02/4047648; Japan: Osaka (06) 323-1707, Tokyo (03) 345-1411; Netherlands 020/45 87 55; New Zealand 4/693-008; Norway 02/78 9460; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 01/207-1717; West Germany and Austria (089) 1204-0.

™HyperDiagnostics, HyperService and Rapid Module Exchange are trademarks of Data Systems Design. ®DEC and PDP are registered trademarks of Digital Equipment Corp.

CIRCLE 9 ON INQUIRY CARD



You can search far and wide, but you won't find a better line of flat cable and connector systems than Belden. You won't find more responsive distributors, either.

Belden cable and connectors are designed for total compatibility—that's why we call them "systems." And that's also why you can count on them for fast, easy, dependable mass terminations.

Every cable, connector and assembly tool is built to Belden's exacting quality standards. It's the kind of quality that keeps your total costs down to earth.

And, of course, all these quality products are backed by Belden's value-added flat cable distributors. Whether filling an order or providing custom and value-added flat cable products, our distributors go the extra mile to serve you better.

Discover Belden's great New World of Flat Cable and Connector Systems. Belden Corporation, P.O. Box 1980, Richmond, IN 47374. Phone: (317) 983-5200.

BELDEN

Coming through...

with new ideas for moving electrical energy

KSM Electronics, Inc.
2207 Northwest 29th St.
Ft. Lauderdale, FL 33311
(305) 739-5880

L-Comp
1115 W. National Ave.
Addison, IL 60101
(312) 628-1400

QPL Electronic Dist. Inc.
47 Calvary Street
Waltham, MA 02154
(617) 891-0460

Starks Electronic Supply
401 Royalston Ave. North
Minneapolis, MN 55405
(612) 332-1325

Federated Purchaser
155 US Route 22
Springfield, NJ 07081
(201) 376-8900

Vertex Electronics, Inc.
150 Schmitt Boulevard
Farmingdale, NY 11735
(516) 293-9880

Simcona Electronics
275 Mt. Read Blvd.
Rochester, NY 14611
(716) 328-3230

Philadelphia Electronics
112 North 12th Street
Philadelphia, PA 19107
(215) 568-7400

Sterling Electronics
11090 Stemmons Freeway
Dallas, TX 75229
(214) 243-1600

8-6-0B

© 1980 Belden Corporation

CIRCLE 11 ON INQUIRY CARD

Can your application use

a $653* 16-bit micro?

If your system design is stretching the capabilities of 8-bit performance, take the step into 16-bit micros without sacrificing cost efficiency.

And at the same time, get all the advantages of a more powerful and proven instruction set. Faster processing. Larger addressing capability. Expandability which allows your system to grow as your needs grow, without changing system architecture. And without appreciably changing your software requirements.

Chances are, you *can* use Digital's $653 16-bit micro in your application.

For full information, fill out the coupon or call toll free (800) 225-9220. In MA, HI, AK and Canada call (617) 467-7000. Or simply contact the Hamilton/Avnet or Harvey Electronics office near you.

*In quantities of 50. Single unit price is $990. Domestic U.S. prices only.

Please rush your 16-bit Micros Application Information Package to me at once. My application is:

☐ Laboratory/Scientific
☐ Data Communications
☐ Industrial Controls (please specify) __________

☐ Other (please specify) __________

Name __________
Title __________
Company __________
Street __________
City __________
State _____ Zip _____ Tel. (   ) _____

Digital Equipment Corporation
Microcomputer Products Group, MR2-2/M65,
One Iron Way, Marlboro, MA 01752

0-6-1

digital
We change the way the world thinks.

CIRCLE 12 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

The article "Making PL/M Programs More Understandable" (*Computer Design,* Nov 1980, pp 169-176) recommends replacing PL/M keywords with personal mnemonics. Allowing this practice means de-standardization. As stated on p 176, at the top of the last column, "it may come down to a matter of personal taste." It may come down, indeed, to everyone having his own PL/M dialect! Adopting dialects, instead of a standard language, decreases readability for experienced PL/M programmers and hence decreases maintainability of any software written in such a dialect. Replacement of keywords should therefore be forbidden, except perhaps for such widely used abbreviations as DCL for DECLARE and LIT for LITERALLY.

Replacing a call to a subroutine by another symbol, which is defined in a LITERALLY declaration, may improve the readability for people not familiar with PL/M. But for experienced PL/M programmers, the improvement will be marginal. Keeping maintainability in mind, we will not recommend the burden such a practice will impose. Replacing commas in an argument list with pseudo-keywords looks very nice to nonprogrammers, but a good-sounding sentence can give the argument sequence a false appearance of correctness. Besides, what is the ultimate program text the compiler has to deal with? A comma too many? A comma too few? This practice may introduce errors difficult to detect, and for reasons of maintainability, we do not recommend it.

The only instance in which LITERALLY declarations should be used, and in our opinion must be used, is in the definition of constants, as in the following example:

```
DECLARE READ$ACCESS LITERALLY '1';
DECLARE MAX$REC$NO
  LITERALLY '1234';
DECLARE LF LITERALLY
  '0AH'/* LINE FEED */;
```

Rienk S. Doetjes and Jan Duits
SKF Engineering
& Research Center B.V.
Nieuwegein, Netherlands

The Author Replies:

I do not advocate *replacing* PL/M keywords except in the case of substituting WORD for ADDRESS, which I consider to be poorly chosen. Besides, if the substitution of keywords is to be forbidden, why make an exception for abbreviations like DCL or LIT, which themselves may be contrary to the spirit of readability?

I propose simply to introduce *new* keywords that may make a program easier to understand. Clearly, if an experienced PL/M programmer is more comfortable with the basic syntax, that's his prerogative. In any given environment, the number of additional keywords should be relatively small so that the effort of learning them is not too great. Of course, the new keywords must be properly documented, like any good software. Furthermore, portability requires that the keyword declaration files be transported along with the programs.

As for maintainability, I fail to see how making a program easier to understand can make it harder to maintain. The problem, of course, is to be sure that the program writer and maintainer agree on what is understandable. Nor can I get too upset over the notion of "de-standardization," since PL/M is not a standard and, to my knowledge, no one is working to make it one. Even within Intel there are syntactic differences between the 8080/85 and 8086 versions of PL/M.

Also, I would like to comment on John M. Pantone's letter in the February issue. The notion that a DO UNTIL block always executes at least once derives from Pascal syntax. In Pascal, one writes

```
REPEAT
sequence of statements
UNTIL condition.
```

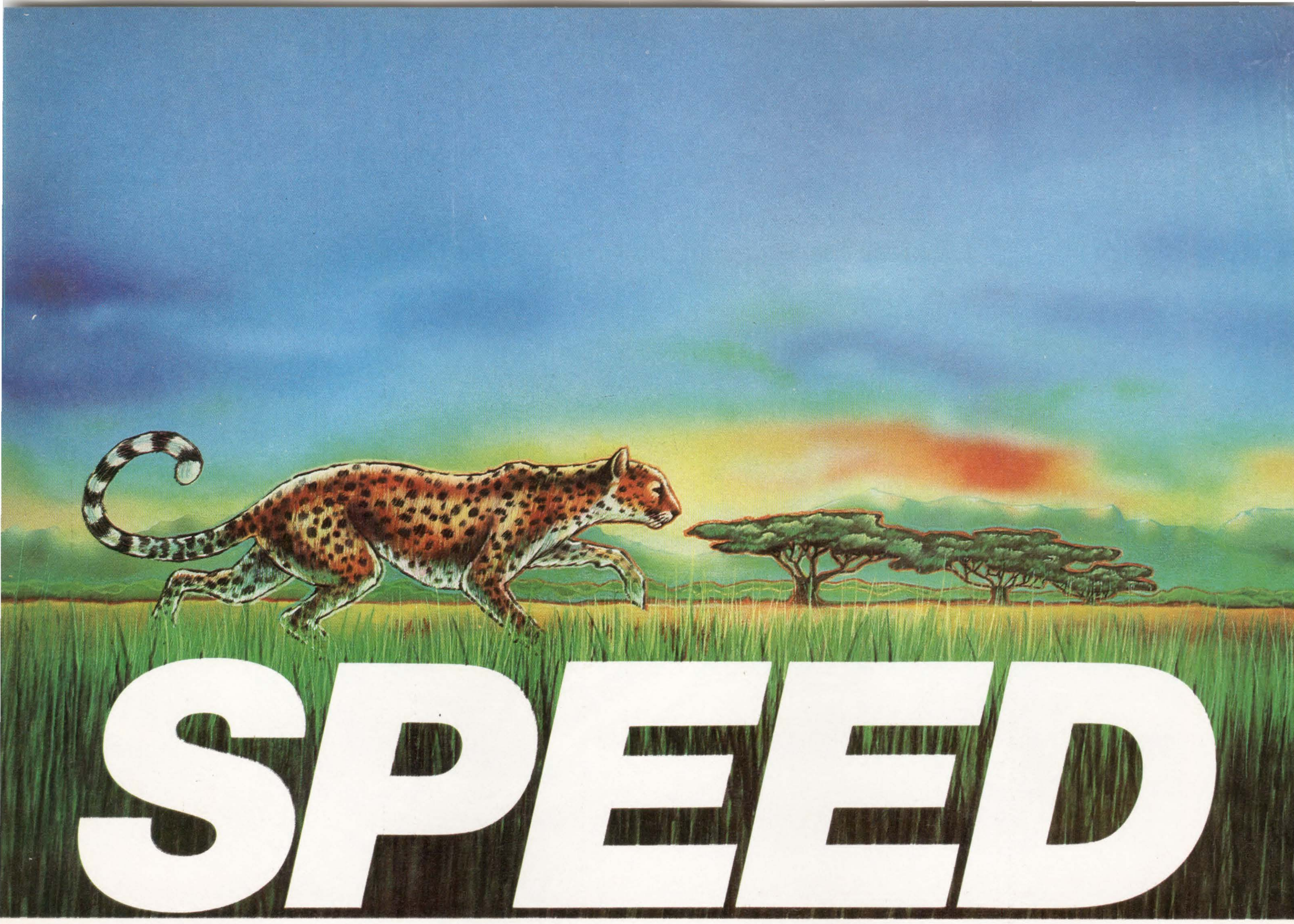
and the statements execute *before* the condition is tested; therefore, they always execute at least once. In PL/M, one must write

```
DO UNTIL condition;
sequence of statements;
END;
```

Here the condition is tested before the statements execute and, therefore, they may not execute if the condition is true on entry. In other words, it is not the keyword UNTIL that guarantees that the block will be executed once, but rather the placement of the block relative to the condition test.

Douglas L. Abbott
Zentrallabor für Electronik
Jülich, Federal Republic of
Germany

Letters to the Editor should be addressed:
Editor, *Computer Design*
11 Goldsmith St
Littleton, MA 01460


SPEED

Intel's Series 90/iQX. The memory

Intel's new Series 90/iQX is the first standard Intelligent Memory System to offer continuous operation and high maintainability at low cost.

Now, for the first time, OEMs can design systems with built-in protection against errors, downtime, and excessive maintenance costs. How? With Intel's new Series 90/iQX.

Series 90/iQX Intelligent Memory System

The iQX controller adds the intelligence of an iAPX 86 microcomputer to the standard Series 90 Memory System. Intelligence that monitors memory operation directly, detects and corrects errors, runs local or remote diagnostics, and reallocates memory space as required. All without burdening the host system.

Fault-tolerant operation

Hard errors or soft, Series 90's iQX controller uncovers them. Soft errors are simply "scrubbed" and corrected. In case of hard errors or device failure, the controller routes data around the problem, allocating spare memory as needed. It then logs the error for future reference.

With protection like this, the Series 90 system will continue operating uninterrupted until all spare memory is filled. And thanks to the iQX's memory status reporting, your customer will know well in advance of memory resource problems. Which not only improves data integrity, but increases reliability and reduces maintenance dramatically.

Instant diagnostics

To keep users continually apprised of conditions within their memory system, the iQX controller provides easy access to its complete diagnostic file. Information can be accessed by the host system either automatically via a simple message-driven software interface, or manually, using the iQX's Service Communicator. This detachable terminal allows technicians to instantly retrieve diagnostic data in plain English through a compact, alphanumeric keyboard/display. With no interruption of the host computer's operation.

For fast, simple maintenance, system diagnostics inform the user of any

machine with non-stop intelligence.

errors it has tracked—soft or hard, correctable or avoidable—and their precise location by row and column.

Many problems can also be solved using the iQX's memory tasking capability to move data blocks as required. Then too, the iQX monitors the system's power supply and signals a warning if voltages drop critically. As a final, double protection, the iQX controller even diagnoses its own operation continuously.

Diagnosing from a distance

To reduce maintenance costs for remote systems and networks, iQX diagnostics can be accessed over phone lines through a single diagnostic station. By being able to analyze problems from afar, you'll eliminate unnecessary service visits and shorten those that are required. And since one diagnostic station can easily serve up to 150 installations, the set-up and ongoing diagnostic costs are contained as well.

Consider the economics

The iQX's protection features offer important economic advantages for systems OEMs. Because of the increased demand for fault tolerance in today's marketplace, systems equipped with iQX capability add significant value to your products. In fact, many applications simply could not be justified economically *without* such self-healing and remote maintenance. Now, through Intel's leadership in 16-bit microprocessing, the Series 90/iQX brings you this capability at an incremental price only nominally above that of ECC alone.

In sum, iQX gives your systems state-of-the art fault protection, reduced maintenance costs, and therefore increased value. Best of all, Intel is delivering Series 90 systems with iQX right now. For detailed information, return the coupon to Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080. For hot line service, call (800) 538-1876.

☐ My needs are immediate; have a Sales Engineer call.

☐ Please rush me—by first-class mail—Series 90/iQX technical literature.

Name ____________________

Title ____________________

Organization ____________________

Address ____________________

City/State/Zip ____________________

Telephone ( ) ____________________

CD6

Mail to:
Intel Corporation
3065 Bowers Avenue
Santa Clara, CA 95051
(408) 987-8080

Europe: Intel International, Brussels, Belgium.
Japan: Intel Japan, Tokyo. United States and Canadian

intel® delivers solutions

CIRCLE 15 ON INQUIRY CARD

New Spinwriter 3500 Series.

Birth of a new concept in letter-quality output.

NEC's new Spinwriter™ 3500 series is the first comprehensive printing system in the letter-quality office printer/terminal market. The Spinwriter 3500 series includes eight new models.

Starting with a new medium-speed 35 CPS print mechanism, the Spinwriter 3500 printer family adds five pioneering dimensions to letter-quality printers.

One: simple, elegant design. Each new Spinwriter 3500 is 30% smaller and lighter, uses 60% fewer parts, single-board electronics, a one-piece universal power supply and digital controls that replace many mechanical functions. It's the size of an office typewriter.

Two: integral forms handlers. Ten of them, designed with the mechanism. All are user changeable. Some are user upgradeable: like a single-bin sheet feeder that can add a second bin or envelope feeder. There's also a cut-sheet guide, bi-directional tractor, push tractor with tear bar and copy separator, manual inserter and bottom feed.

Three: new uptime standards. The Spinwriter 3500 has a 3,000-hour MTBF, which means about two years between failures. And no preventive maintenance or routine lubrication. Ever. With only three major spares, MTTR is reduced to 15 minutes!

Four: word processing assist. Lets the terminal perform WP systems tasks like automatic bi-directional printing, auto PS printing, auto underlining, shadowing and bold printing. Using all the Spinwriter type styles of up to 128-character thimble print elements.

Five: immediate attachability. The Spinwriter 3500 comes in eight printer or terminal models with Qume, Diablo, Centronics, RS-232C interfaces, and is functionally compatible with Spinwriter 7700 and 5500 Series.

Find out more about the light, quiet, compact, reliable Spinwriter 3500 series. Superior in every way.

NEC

NEC Information Systems, Inc.

Home Office: 5 Militia Drive,
Lexington, MA 02173, (617) 862-3120
Eastern Office: 36 Washington Street,
Wellesley, MA 02181, (617) 431-1140
Central Office: 551C Tollgate Road,
Elgin, IL 60120, (312) 931-1850
West Coast Office: 8939 S. Sepulveda Blvd.,
Los Angeles, CA 90045, (213) 670-7346

NEC. Going after the perfect printer.

CIRCLE 16 ON INQUIRY CARD

Contemporary Multiplexing Techniques—Part 2: Statistical Multiplexers, Criteria and Constraints

James F. Kearney

Timeplex, Incorporated
One Communications Plaza, Rochelle Park, NJ 07662

The first part of this series dealt with multiplexer theory and design concepts and discussed basic types of multiplexers and how they differ. In this concluding part, a number of network design problems is shown in the context of some typical, real world network situations.

Equipment in remote locations often differs from that at the host site—eg, an IBM host and a Data 100 or other look-alike in the field. The vendor of the look-alike equipment will have an emulation program, and these programs handle data somewhat differently. Therefore it is important to know the particulars of an emulation program before putting a statistical multiplexer into the system.

Protocol Problems

If, for example, an IBM host sends traffic to an emulated IBM 3780 terminal, embedded sync characters could cause a problem. Under the IBM system these characters are normally stripped out, but with many emulated systems this is not the case. Such embedded characters can lengthen a data block considerably. Since emulated terminals usually have limited buffer space, at times the user runs the risk of overflowing the end buffer. In most look-alikes, there is a version of the emulation package that does strip away the embedded sync characters.

It is also necessary to examine operation on the host side of the system. When first configured, many systems grew out of a local environment, where a very high speed line came from a local cluster controller or terminal directly into the high speed bus of the mainframe. Poor file structure or system partitioning may not have caused any apparent deficiencies because of the high speed data transfer between local cluster controller and mainframe. However, these inefficiencies become quite evident when a communications facility is involved, especially if the number of associated lines increases to the point at which a statistical multiplexer (stat mux) is used.

For example, consider eight 2400-bit/s 3270 terminals in a local environment involving one or two local cluster controllers. The eight lines are connected to eight channels of a stat mux. Long delays can result if provision has not been made for balancing out the partitions so that online software gets a high priority, and if the associated files have not been structured to accommodate the number of tasks being performed by the system.

Buffering

Buffering concepts have changed over the past few years. Until recently, multiplexers employed static random access memory (RAM) that allocated a specific amount of buffering to each channel. When this amount was exceeded, traffic control was activated to stop the channel, provided the multiplexer had this control; if it didn't, data were lost. To insure against the loss of data, larger amounts of buffer were assigned to each channel. In the same way that time division multiplexer (TDM techniques waste bandwidth, this arrangement wasted buffer; the large storage capacities were not often needed.

Dynamic buffering was the next step. This assigns common buffer in each module to whichever of the channels associated with the module needs it. However, under the error condition known as "streaming," when a steady stream of erroneous characters is induced into the line with no pauses such as are encountered with live transmission, the stream quickly fills the buffer for the whole module. This can trigger traffic control prematurely and knock out all channels associated with the module.

The most recent variation provides an override to dynamic buffering. This assigns a buffer access priority to each channel within the module. The modular construction limits the ability of one channel in a streaming mode to interrupt other channels. The priority system further limits this effect only to the channel causing it. The rule of thumb generally used in assigning priorities is to give lowest priority, with access to 256 bytes of buffer space, to the low speed asynchronous channels operating on character by character or very small block mode; next giving access to one-fourth of the buffer pool to the 2400-bit/s interactive terminals that may have blocks of 400 to 1000 characters; and top priority, with access to all buffers in the pool, to remote job entry (RJE) terminals having a larger number of blocks to be transmitted.

(continued on page 26)

These are recommended guidelines, not requirements. The point to remember is that there will be problems in a communications network. The fundamental question facing the network designer is how to minimize the exposure generated by a particular problem. Buffer allocation should be regarded as a way of preventing one user from tying up an entire system.

Clocking

Some front ends and terminals require a clocking function. Synchronous systems require clocking; therefore, multiplexers used in such systems will have a capability to supply or receive clocking. Clocking has not been a factor in asynchronous systems until recently. However, the higher speed terminals that are emerging for asynchronous systems depend on clocking. In a normal IBM environment, for example, with any asynchronous port of more than 1200 bits/s, the front end must receive clock. This requirement is often ignored when systems are being upgraded. A system that cannot supply clocking is mistakenly acquired, and without a clock the front end and/or terminal will not operate.

On some stat muxes clocks can be changed on a channel basis. On others they can only be changed on a module basis, which means not only that each clock setting must apply to all terminals connected on the module, but that there will be a limitation in the way that channels can be associated within an individual module. This could present a problem when trying to assign channels to modules on a traffic basis.

Flexibility in clocking might also be needed on a nodal basis. If the clocks are set for internal timing on the multiplexer at the host end, which means that a clock is being generated there for the front end, must clock also be generated to the remote hardware? There may be cases in which this is not desirable, when an external clock is called for. For example, clock may or may not be wanted from a tail circuit modem.

These are all examples of how the current generation of stat muxes is closing a large gap that has troubled those trying to put together a communications network. The stat mux can make it possible to combine within the same network dissimilar equipment that could not previously have been interconnected. The user can now tie a terminal that does not use clocking at all to an IBM front end at 4800 bits/s, supplying clock to the front end through the multiplexer that is inputting data from a variety of pieces of equipment.

Data Speeds

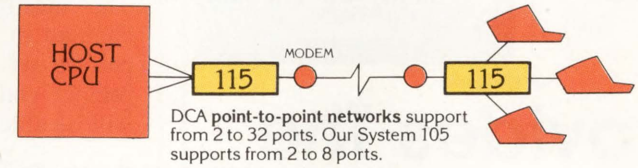
Usually programmed on a per channel basis, data speeds are not varied in a synchronous environment. However, auto speed or adaptive speed may be required in an asynchronous environment. With this

(continued on page 28)

FROM STATISTICAL MULTIPLEXORS TO COMPLETE DATACOMM NETWORKS, EVERY DCA COMPONENT IS

ENGINEERED TO EXPAND

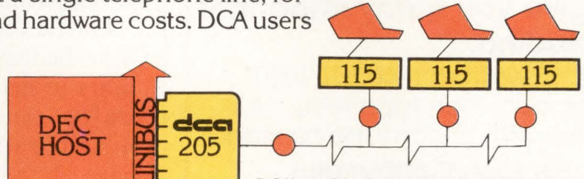
DCA protects your initial investment in statistical multiplexors with the lowest-cost network growth in the industry. So you can start with a small datacomm network today, and expand or modify it to meet your needs tomorrow.



DCA **point-to-point networks** support from 2 to 32 ports. Our System 105 supports from 2 to 8 ports.

Our System 115 statistical multiplexor can be used in point-to-point networks to support from 2 to 32 asynchronous terminals at a remote site. DCA's statistical multiplexing assures excellent response time, character transparency and error-free transmission.

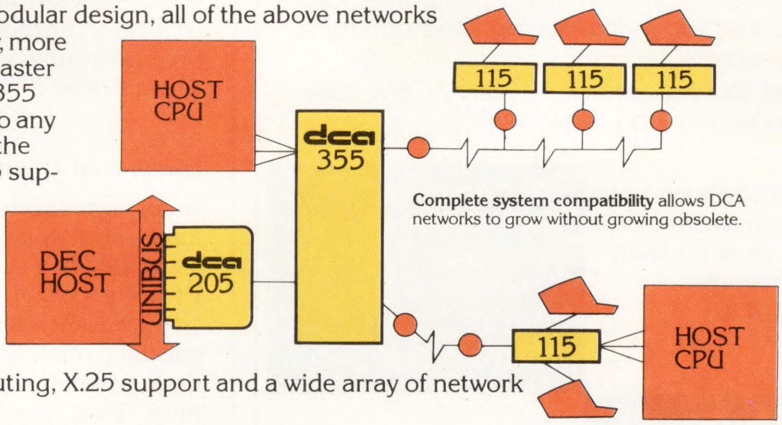
DCA's multipoint multiplexing configuration serves a number of remote terminal locations with just a single telephone line, for substantial savings in phone-line and hardware costs. DCA users have benefited from multipoint multiplexing since January 1979.



DCA's **multipoint multiplexing** permits several remote locations to share a single phone line.

DCA's System 205 is a statistical multiplexor designed for DEC UNIBUS*-based computers. The 205 requires only one UNIBUS slot to emulate up to 16 DEC DZ11 modules and a 128-port stat mux. This greatly lowers hardware costs and improves response time as well.

Because of DCA's unique modular design, all of the above networks could easily expand into larger, more powerful networks. As the master network processor, System 355 gives terminal users access to any host computer anywhere in the network. In addition, the 355 supports up to 126 ports, 62 of which can be high-speed synchronous trunk links. Several 355's can be combined to greatly expand this support. Features include port contention, switching, unlimited routing, X.25 support and a wide array of network management tools.



Complete system compatibility allows DCA networks to grow without growing obsolete.

Total system access and unlimited network growth at very low cost—that's the DCA advantage. For complete information, call or write for our 16-page brochure.

*TM Digital Equipment Corporation

dca
ENGINEERED
TO EXPAND

Digital Communications Associates, Inc. Dept. CD 1,135 Technology Park/Atlanta, Norcross, GA 30092 404/448-1400

CIRCLE 18 ON INQUIRY CARD

option the channel speed is shifted from 150 to 1200 bits/s. The remote multiplexer initiates the changes when it samples the first incoming character (usually a carriage return) and detects the speed to which to shift the channel. Once that shift is made, a character or status word is signaled to the remote unit to indicate that a change should be made. The word is also passed on to the host unit, telling it that it is getting 1200 bits/s rather than 150 bits/s. An optional adaptive speed attachment available on some multiplexers uses the large buffer capacity at the remote end to hold data so that the host can remain in a constant speed mode. In this way much of the firmware that would be associated with the mainframe is avoided. In cases of crisis in large systems with different types of front ends that recognize different characters, when one mainframe is down, a shift over to another system, with no exposures, is facilitated. The multiplexer is compensating for the speed changes in the system. All ports on the mainframe can be set for 1200 bits/s; the multiplexer on the remote end, making the necessary compensations, will be able to accept from 150 to 1200 bits/s.

Traffic Control

When a channel buffer is filled, traffic control automatically stops a sender in order to avoid losing data. It is generally available on stat muxes. (See the Table, "Traffic Control Options.") The user should be sure that the traffic control allows him to retain the flexibility in network configuration that he needs. Many traffic control arrangements are programmed per module rather than per channel. Where this is the case, if the user wants to program a clear to send (CTS) function to go low when traffic control is enabled, it is necessary to program all of the channels in the module, both local and remote, in the same way. When the multiplexer can be programmed independently for each channel end, the user has a means of establishing a functional communications link, where before it was impossible.

Number of Channels on the Line

In an asynchronous environment, limitations on the kinds of channels and traffic volumes that can be associated in a single stat mux are seldom a problem. Problems begin when bisynchronous data are introduced. Because of the polling overhead and the constant reference to each channel of some sort of data, whether live or polled, the processors are kept busy. Thus, more 4800-bit/s asynchronous channels than 4800-bit/s synchronous channels can be run on the same line.

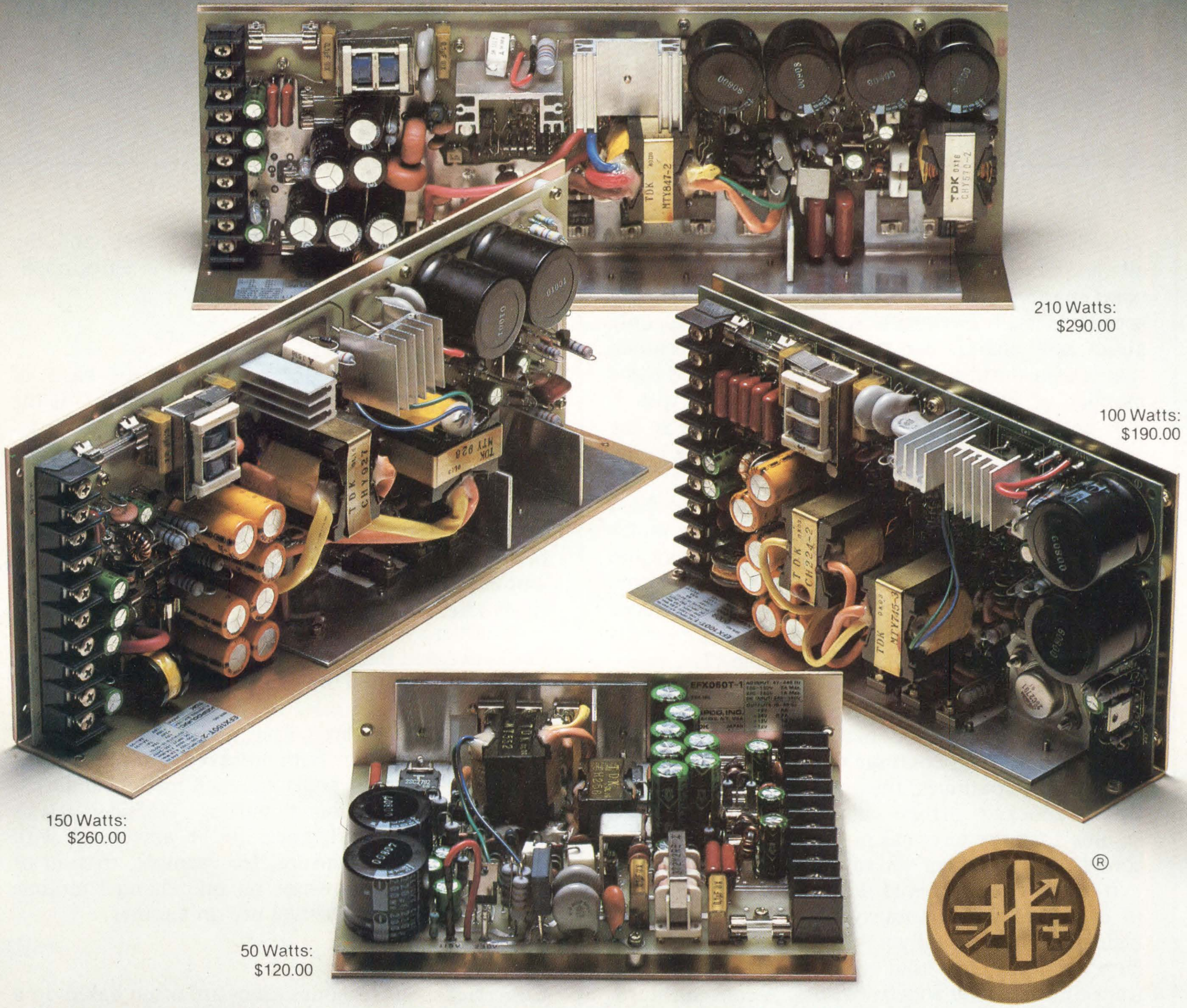
The problem is not encountered in the medium speed ranges, but appears when the user tries to run 7200 and 9600 bits/s over one 9600-bit/s line.

(continued on page 30)

HIGH QUALITY

open frame SWITCHING POWER SUPPLIES

... at a very attractive price



210 Watts: $290.00

100 Watts: $190.00

150 Watts: $260.00

50 Watts: $120.00

Single board, multiple-output, open frame switch-mode power supplies offer you high efficiency, well regulated power at a very attractive price.

The listed prices are for single unit quantities. Please contact us for quantity pricing and a demonstration.

KEPCO® For complete specifications, write Dept. DBF-79

KEPCO, INC. • 131-38 SANFORD AVENUE • FLUSHING, N.Y., 11352 U.S.A • (212) 461-7000 • TWX -710-582-2631 • CABLE: KEPCOPOWER NEWYORK

CIRCLE 20 ON INQUIRY CARD

TRAFFIC CONTROL OPTIONS

Stat Mux Controls External Equipment

Type	Character/Function	Operation
Inband	X-OFF/X-ON	Transmits X-ON/X-OFF sequence
Inband	Programmable	Transmits user selected sequence
EIA	Clear to send	Transmits high or low CTS level
EIA	F3 (connector pin 22)*	Transmits high or low level on pin 22

External Equipment Controls Stat Mux

Type	Character/Function	Operation
Inband	X-OFF/X-ON	Responds to X-OFF/X-ON sequence
Inband	Programmable	Responds to user selected sequence
EIA	Clear to send	Responds to high or low CTS level
EIA	F3 (connector pin 25)*	Responds to high or low level on pin 25

---

*Control function on F3, pin 22 or 25 of EIA RS-232-C connector; polarity of start/stop signals is user selectable

Trouble starts with the sampling of data, and even if all the data do get in, the volume will continue to upset matters because of the limitations of the high speed line itself. Even with two high speed links, only about 2400 chars/s can be sent. If an RJE terminal that is transmitting a 1000-character block and has a number of interactive terminals associated with it that possibly present 3000 to 4000 characters at any given time, the system will go into a queuing cycle. The result is that users are waiting.

In that situation the timeout factors associated with the host system must be very high. The multiplexing environment adds overhead to the system and in any case expands the timeout parameters within the mainframe. When too much data are introduced in addition to all this, chances of timeouts are greatly increased. This condition is cumulative. The mainframe sends out a block of data and gets neither acknowledgment (ACK) or negative acknowledgment (NAK). This causes the mainframe to go into a timeout and it will continue to try to retransmit the data. If this continues, the terminal will be, in many cases, knocked offline and the mainframe will assume that the terminal no longer exists. When it comes up, the system will no longer recognize it.

It must be remembered that a stat mux is a means to collect and continuously multiplex data over a high speed link, usually a 9600-bit/s line. It is not a large concentrator that collects, assembles, and transmits data over wideband lines. A concentrator is primarily used to collect very large blocks of data and send them over a number of 9600-bit/s lines or over a 56k-bit/s link. Concentrators have the memory capacity to accomplish this and, in some cases, will also do local ACKs and NAKs. However, they are more expensive—in the order of $70,000 instead of the $2500 or so for a stat mux. On the other hand, the stat mux is designed primarily for interactive application.

Network Configuration

Distributing channels to modules on the basis of utilization is the key to configuring networks. If the type of data that are coming over a particular channel is known, it should be assigned to modules according to their efficiencies; that is, what other channels it will be associated with. The effect is to make sure that one module and its channels are not tied up with scanning, buffering, and handling large amounts of data while others are sitting comparatively idle.

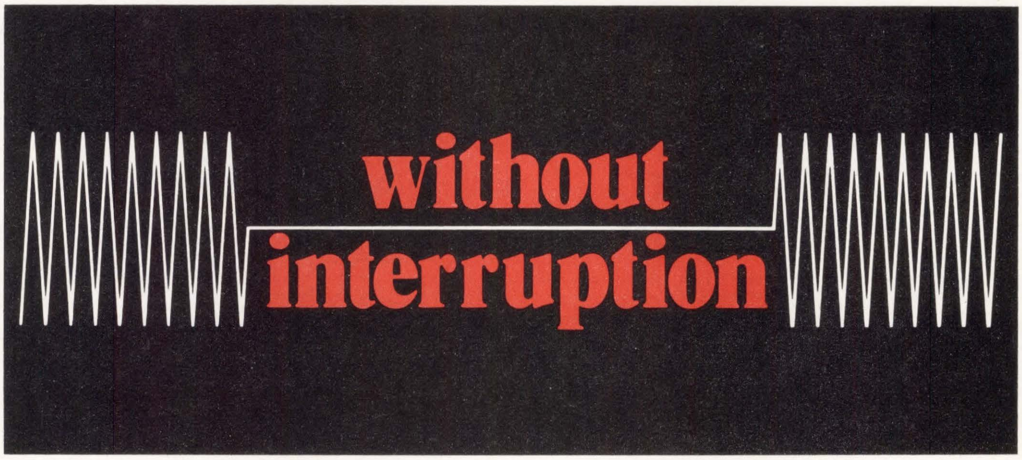
In earlier systems where one master controller (the CPU) governed the scan going out to particular channels, it was common practice to give the highest speed channel to channel one, where the scan starts, and the others to two, three, four, and so on in the order of decreasing traffic. With more recent modular concepts, there is one scanner for each module and each has its own associated buffer. Traffic analysis enables particular channels to be associated with given modules and ensure, for example, that all of the RJE terminals are not on one channel module while all of the interactives are on another.

Response Time

Concerns about response times are often based on a combination of poor understanding of what the user's own needs are and a lack of understanding of the real world. Even on a one-to-one connection the overhead in a stat muxing environment will introduce delays, although these will probably not be

(continued on page 36)

POWER TO YOUR COMPUTER



Continental Power Systems presents a unique new design in uninterruptible power sources for all mini, small business and small/medium computers.

The PoweRotor™ UPS System keeps your computer on-line through common power problems such as momentary interruptions, erratic voltages and transient spikes. Yet the PoweRotor generator maintains absolutely constant output frequency essential to computer operation. During a utility outage, the system provides 10 to 30 seconds ride-through for orderly downsequencing or switching to back-up power.

- Installation is easy, with only small footprint area required.
- Lower installed cost than static inverter/battery systems.
- Superior ride-through over motor generator sets.
- Only UPS with 3 year warranty.

Get the complete story on the better UPS from Continental Power Systems, Inc., One Landmark Square, Stamford, CT 06901. 800-243-9145.

Continental Power Systems, Inc.

A member of The Continental Group, Inc.

An international packaging, forest products, insurance and energy company.

CIRCLE 31 ON INQUIRY CARD

SHUGART
A REVOLUT

Choice.

If you've been looking at disk drives for desktop systems, you may have thought you had only one choice: take it or leave it.

Not any more. Now you can get everything you need from a single source. And get the added convenience of doing business with one company.

Say you want a reliable, entry-level drive, but cost is critical. The ideal choice? Our SA400, the original Minifloppy.™

Or maybe you need more capacity, but you don't want to give up low cost. Try our double-sided Minifloppy, the SA450.

Then too, you may want to move up to even higher speeds and capacities — up to a megabyte — in a Minifloppy-size package. For that, choose our 96-TPI SA410 single-sided or SA460 double-sided drives.

But what if your desktop system demands the high performance and reliability of a

INTRODUCES IONARY IDEA.

Winchester? Then specify our new 5.25-inch fixed disk drive, the SA600. It's got ten times the throughput of a floppy, and capacities from 3.33 to 10 megabytes. And by teaming it with a Minifloppy, you get duplicate file backup too.

Now *that's* choice. Which means you get just the right combination of cost and capacity for your application. And in the desktop market, that's a revolutionary idea.

To find out more about your desktop alternatives, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, CA 94086. Telephone (408) 733-0100. Or Hamilton/Avnet, authorized distributor.

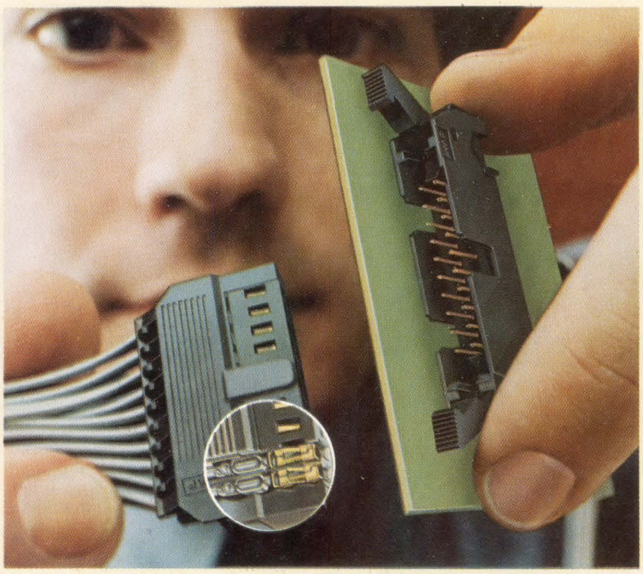
Shugart

Right from the very start.

Sales and Service: Sunnyvale CA, Costa Mesa CA, Minneapolis MN, Richardson TX, Framingham MA, Landing NJ, Atlanta GA, Toronto Ontario, Paris France, Munich Germany.

CIRCLE 22 ON INQUIRY CARD

Mass termination comes to the world's most popular interconnection system.



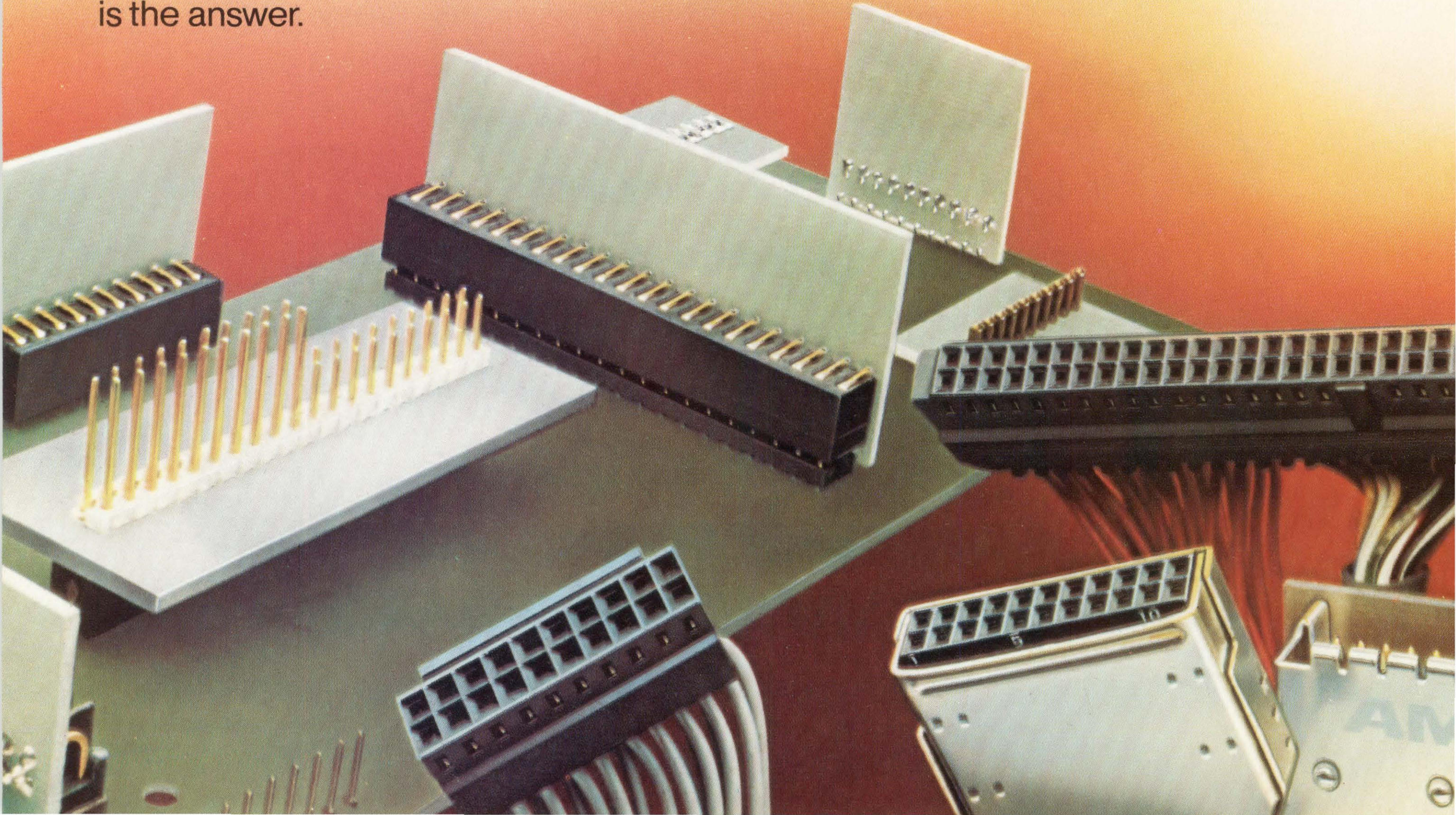
Now you can have the money-saving benefits of mass termination with the design advantages of our universal board-to-board, wire-to-board and wire-to-wire AMPMODU interconnection system.

The AMPMODU MT connector.

Its insulation displacing contact works with discrete wire, or jacketed and ribbon cable. And housings gang together with one low-profile cover assembly for multiple cable style applications. If you need EMI shielding, our inexpensive hardware kit is the answer.

We've advanced mother/daughter board packaging, too. Our newly-designed two-piece connector gives you higher density and greater performance than one-piece designs. At comparable cost.

These are just two of the latest innovations in our AMPMODU receptacle design—proved reliable for fifteen years, and even more cost-effective now with Accu-plate precision plating. So keep updating your product for the better with the AMPMODU system.

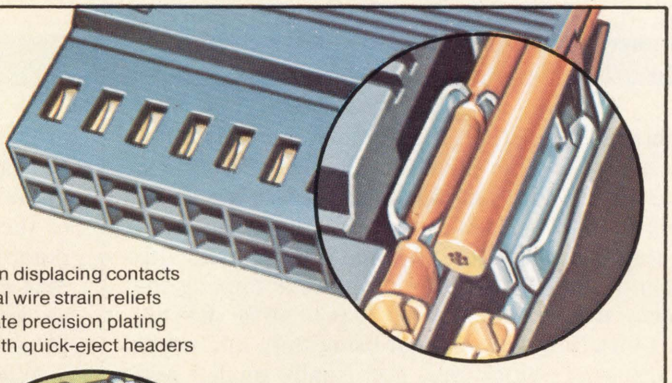


AMP Facts

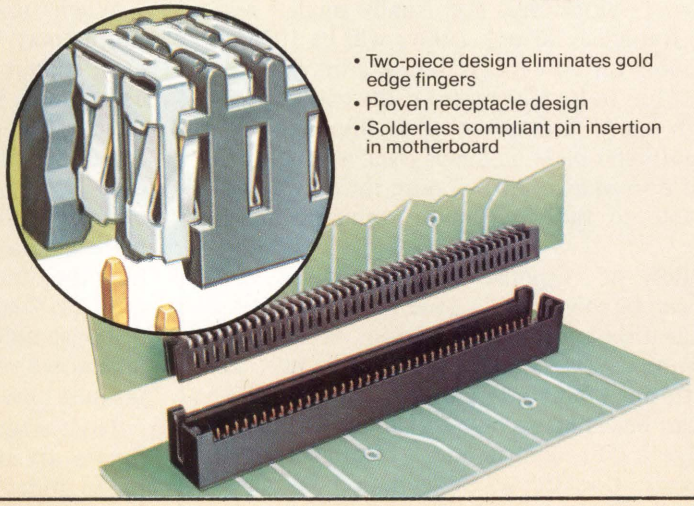
General classifications of AMPMODU posts and mating receptacles:
.031" x .062" and .025" x .025" incorporating standard, intermediate, and high-pressure design.

Housings:
A wide variety of sizes, styles and centerlines, including .100", .125" and .150". Single or double row.

AMPMODU MT Connectors:
Range from 6 through 72 positions and can be terminated to discrete wire, jacketed cable, twisted pair cable, and ribbon cable.



- Insulation displacing contacts
- Individual wire strain reliefs
- Accu-plate precision plating
- Mates with quick-eject headers

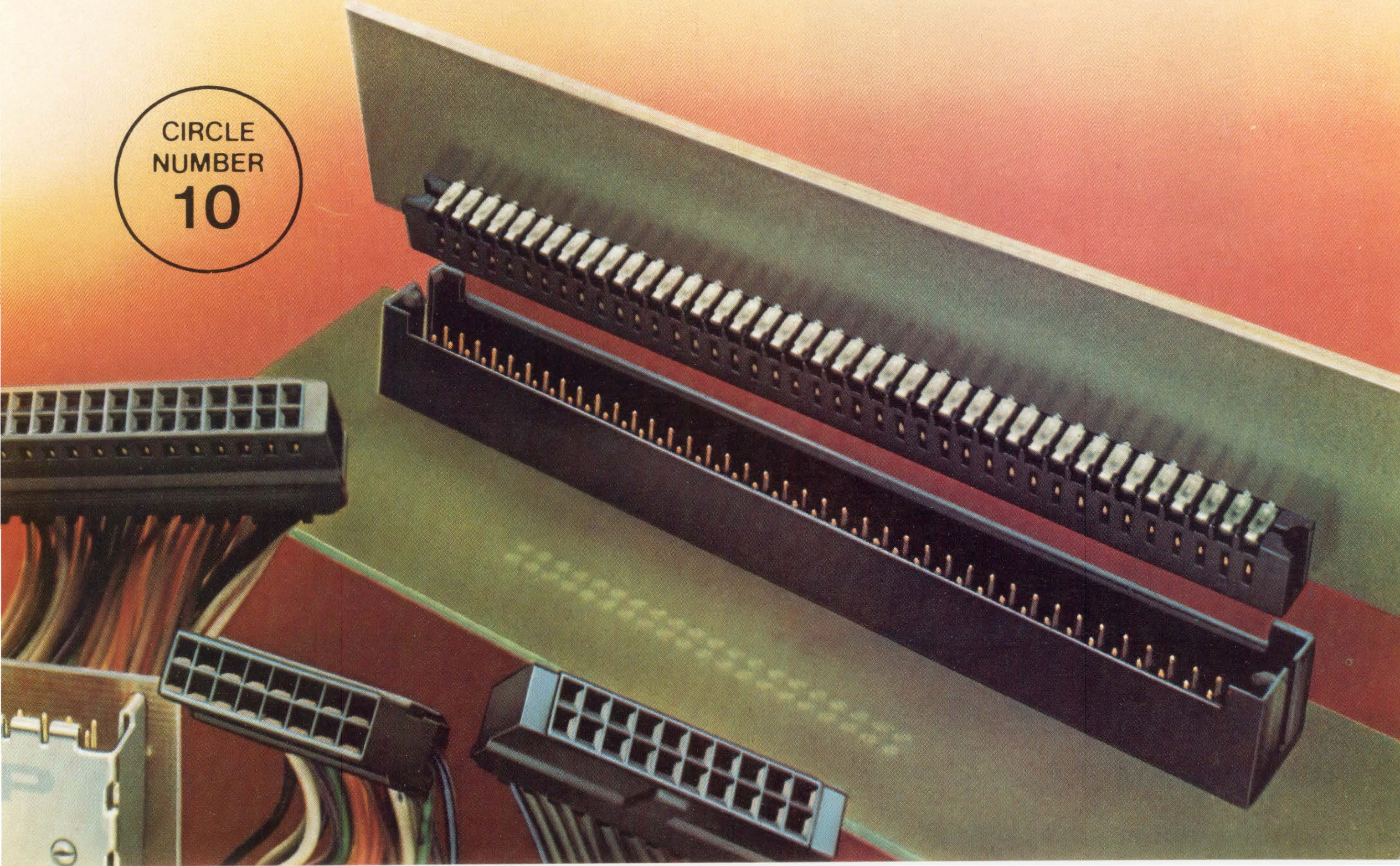


- Two-piece design eliminates gold edge fingers
- Proven receptacle design
- Solderless compliant pin insertion in motherboard

For more information, call the AMPMODU System Desk at (717) 780-8400.
AMP Incorporated, Harrisburg, PA 17105.

AMP and AMPMODU are trademarks of AMP Incorporated.

AMP means productivity.



CIRCLE NUMBER 10

noticeable on the CRT; an RJE terminal pumping out a large data block will produce a delay that is noticeable by comparison. With stat muxing, an RJE terminal encounters a 10% to 20% delay while unimpeded by other terminals. If the RJE terminal is associated with a number of interactive terminals in a stat muxing environment, delay could grow to 20% to 40%, depending on utilization. In a system using only interactive terminals, where block sizes are usually smaller and there is less frequency of use, delays will be 10% to 20%, depending on how much data are introduced. This tradeoff has to be recognized if the user expects to save high speed line costs. It is impossible to transmit eight 4800-bit/s channels over a 9600-bit/s line with no degradation of response time. If this is not acceptable to the application, multiplexing is ruled out.

Optimization of response time, assuming that some delay can be tolerated, is done by manipulating channel utilization on a modular basis as outlined above. Stat muxes that have a supervisory port arrangement through which data on traffic and buffer utilization can be called up on a CRT make it possible to obtain live traffic reports and a clear picture of loading factors. Looking at these, it is possible to determine immediately which channels are heavily utilized and to change channel assignments to avoid having too many heavily used channels on the same module. For example, on an 8-channel system, two of the channels may be 4800-bit/s computer to computer utilization and the other six 4800-bit/s channels may be interactive systems, each has a host port assigned to an adjacent controller for terminal interfaces.

When the system has been in service for a month or two it may become apparent that the applications have changed. One computer to computer channel has become intensely occupied with data and two of the associated CRT channels have become heavily occupied. If all three of these channels are on the same module, the supervisory port will indicate that that module with its associated channels has been experiencing a higher queuing rate or buffer utilization than the others. One of the channels could be moved to a less frequently used module. This will enhance response time and ensure that module failure will not take down what apparently are three of the most important lines.

High error rates also increase response time. Stat muxes are designed to provide error free data between nodes by the ACK-NAK sequence and automatic request for retransmission (ARQ) mechanism. If a high speed line begins to encounter problems where it is retransmitting much of that data, delay will be introduced. On the other hand, the stat mux is taking care of the ACK-NAK function, relieving the host system of considerable retransmission work and buying back some of the lost time.

Summary

Multiplexing has moved through three stages: frequency division, time division, and statistical. Design considerations have changed from an emphasis on the common control to an emphasis on the capabilities of microprocessors and distributed processing. Stat muxing with microcomputers not only permits loading a single high speed line with channels aggregating a speed exceeding that of the line, but also affords a number of features added to the multiplexer to enhance the whole network. Most important among these are automatic error correction, programming ease including downline loading of channel parameters, and system diagnostics that can ferret out trouble down to the individual component level with greater flexibility. A successful data communications system designer should know his people and their needs and learn which features will best serve them.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 719 **Average 720** **Low 721**

Executive 80™ knows what you're up against.

The Executive 80™ terminal is highly flexible. OEMs can customize it to their system designs, giving each system a unique, highly marketable terminal. And, their customers can switch the terminal from job to job, redefining its operating routines for each task.

This built-in flexibility of architecture is one result of the true high-speed processing and communications capability of the Executive 80's **8088** microprocessor. It permits six key-selectable operating modes, each one best suited for a particular type of application. And it allows up to 16 user programmable function keys, each capable of being programmed for a frequently used operating routine.

Would you believe–a flexible data processing machine?

Until now, you've been up against the problem of fitting your system design into the limits of a limited terminal. Now, with Executive 80, the terminal has enough smarts to fit in with your system.

Hazeltine Executive 80

Answers for the Eighties

Hazeltine Corporation, Computer Terminal Equipment,
Greenlawn, NY 11740, National Sales: (516)549-8800
Telex: 96-1435
Hazeltine and the Pursuit of Excellence

New York (212) 752-3377 • San Francisco (415) 342-6070
Orlando (305) 628-0132 • Los Angeles (213) 553-1811
England 01-568-1851 • Telex: (851) 928572

For additional sales office locations, please call our toll-free number: (800) 645-5300.

CIRCLE 24 ON INQUIRY CARD

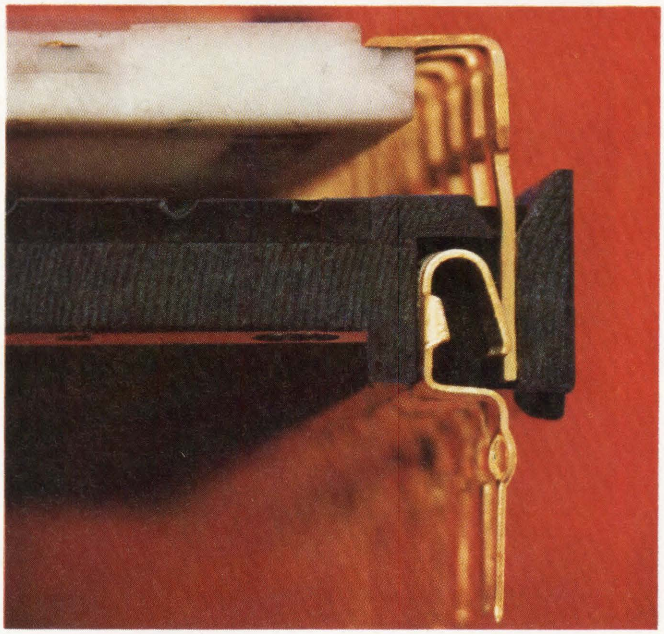

It takes a
strong, steady squeeze....

...to achieve GAS TIGHT RELIABILITY in a low profile socket

You know the secret of gas tight reliability in a low profile DIP socket. It is the "squeeze" or force the contact exerts on your IC lead. RN single leaf high compression contacts exert a "normal force"* that is 4 to 5 times greater than conventional dual leaf contacts. Result? RN low profile ICL series sockets are MIL-SPEC qualified (MIL-S-83734) to meet the toughest gas tight performance standards in the world.

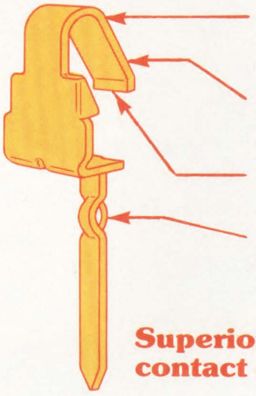
You can't buy a more gas tight low profile socket—anywhere! And, our prices compare very favorably with any comparable socket.

*NORMAL FORCE means force at right angles to the IC lead.


RN single leaf high compression contact provides maximum pressure against your IC lead.

MIL-S-83734 Environmental Test Data for ICL Series DIP Sockets

Test	Procedure	Results
Initial Contact Resistance	MIL-S-83734 Paragraph 4.7.15	R_C=7.0mΩ average
Corrosive Atmosphere	MIL-S-83734 Paragraph 4.7.16 10-25 ppm $(NH_4)_2S$, 4 hours	R_C=8.5mΩ average
Moisture Resistance	MIL-S-83734 Paragraph 4.7.14	$R_i \geq 10^{12}\Omega$
Thermal Shock	MIL-S-83734 Paragraph 4.7.13	No Damage
Mechanical Shock	MIL-S-83734 Paragraph 4.7.11	No Discontinuity
Vibration	MIL-S-83734 Paragraph 4.7.1	No Failures R_C=7.0mΩ average (final)
Socket Durability	MIL-S-83734 Paragraph 4.7.12 After 50 Cycles	R_C=7.8mΩ average


Contact available in phosphor bronze, beryllium copper, with tin or selective gold plating.

High compression contact design provides longer spring length for maximum pressure against IC lead.

"Side-wipe" design meets flat, smooth side of IC lead for perfect contact.

Self-lock lead holds socket firmly during wave soldering and prevents solder wicking.

Superior contact design

WRITE FOR COMPLETE DETAILS and latest RN catalog with full specs, dimensions and material data.

MAIL THIS COUPON NOW

Send me full details on your gas tight low profile ICL series sockets right away.

RN
800 E. Eighth St.
New Albany, IN. 47150

Name____________ Title____________

Company____________ Phone____________

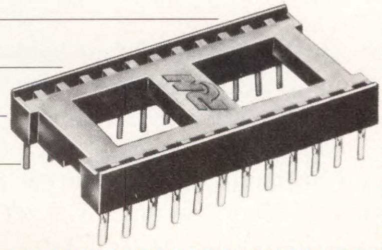
Address____________

City____________ State______ Zip______

My possible application is____________

☐ Please send MIL-S-83734 Test Results

CD681



CIRCLE 25 ON INQUIRY CARD

TM990 Series 16-bit microcomputers: Shortcut to industrial control solutions. The wide choice from Texas Instruments.

Solve a majority of your industrial control design problems rapidly. Economically. Efficiently. TI's broad TM990 Series of microcomputer modules can match your needs down the line. And off the shelf. Saving design time and money because they are preassembled, pretested. Giving you all the performance of TI's 16-bit 9900 microprocessors.

Super fast CPU

If you need a high-performance general purpose 16-bit CPU, then the new TM990/1481 two-board CPU is your answer. With 95 distinct instructions, it has the processing power of a minicomputer.

While the TM990/1481 is 3½ times faster than other TM990

CPUs when executing non-floating point instructions, it shines at floating point arithmetic. *It is 40 times faster.* In fact, the TM990/1481 performs double precision floating point in the same time as it takes competitive products to perform single precision.

Memories: Broader range

Your choice in TM990 memories includes a variety of directly addressable semiconductor memory modules, and bulk storage memories like a nonvolatile bubble memory module. With capacities up to 1024K bytes.

There's also provision to handle floppy disks drives. The TM990/303A controls up to four standard drives or three mini diskette drives.

Exceptional I/O capability

Interfacing with the outside world is relatively easy. The TM990 Series contains a comprehensive selection of I/O modules: Digital. Analog. Industrial AC and DC. And, *a readily available speech module*, the TM990/306. It can speak 179 words and is ideal for situations where the spoken word is the most effective means of communication.

Recently added to the TM990 line are two new communication modules. The TM990/308 Industrial Communication Module permits communication with as many as 31 other compatible TM990 systems. Over distances up to 10,000 feet, using twisted-pair lines. The optically isolated interfacing built into the 308 simplifies interconnects and lowers installation costs even in electrically noisy environments.

The TM990/307 allows communication with up to four RS232 devices such as terminals or modems.

Functional integration: Slashes your software costs

Functional integration. Hardware and software units developed together. To work together. TI is first with this system concept of the 80's that can substantially cut software development time and costs.

Key element is a set of software interconnect standards that ties the system together.

Broad and growing series: TI's TM990

Microcomputer Modules:
TM990/100MA
TM990/101M
TM990/180M
TM990/1481

Memory Modules:
TM990/201 EPROM/RAM
TM990/203 Dynamic RAM
TM990/206 Static RAM

Mass Storage Modules:
TM990/210 Bubble Memory
TM990/211 Bubble Memory
TM990/303A Floppy Disk Controller

Digital I/O Modules:
TM990/305
TM990/310

Analog I/O Modules:
TM990/1240
TM990/1241
TM990/1243

Communication Modules:
TM990/307
TM990/308

Speech Module:
TM990/306

Card Cages & Enclosures:
TM990/510
TM990/520
TM990/522
TM990/530

Industrial AC and DC I/O Modules:
TM990/5MT Series

Data Entry and Display Microterminal:
TM990/301

University Module:
TM990/189M

Software Development Module:
TM990/302

The Realtime Executive implementation allows you to interface TI's Component Software with the system easily and quickly. These Component Software packages provide a library of statements common to many programs. You choose what you need and combine it with the specific software required by your application. Savings can be more than two-thirds the cost of writing a typical program.

Available now: the File Manager. Coming soon: Software Data Communication packages.

The File Manager package performs such functions as library level management of diskette storage. Including install formatted volume, open/close/read/write files, random access to files.

TI's powerful AMPL hardware and software development system includes full speed emulation of 9900 microprocessors, and provides for program development in assembly language, TI Microprocessor Pascal (complete with concurrency), and Power Basic.

Complete accessories

The TM990 Series is supported by a broad selection of accessories — card cages, connectors, cables, and power supplies. Just added: the TM990/522 Enclosure containing a four-slot OEM chassis, power supply, and cooling fan in a neat, attractive, table-top unit.

For faster, simpler solutions to industrial control problems, take the shortcut. The TM990 Series of microcomputers. For more details about these time and money saving modules, see your local TI distributor, or fill out and return the coupon.

Texas Instruments Incorporated
P.O. Box 1443, M/S 6404
Houston, Texas 77001

☐ **Please send Brochure CL-377C.**
☐ **Please have a salesman call.**

NAME ____________________
TITLE ____________________
FIRM ____________________
ADDRESS ____________________
CITY ____________________
STATE ____________ ZIP ________
TELEPHONE ____________________

TEXAS INSTRUMENTS
INCORPORATED

Protocol converter supports binary synchronous and systems network architecture 3270 protocols

Protocol converter. It supports Bisync and SNA and allows mixed device multivendor networks by communicating with peripherals in one protocol and hosts in another

Said to be the first microprocessor based protocol converter that fully supports IBM's binary synchronous (Bisync) and systems network architecture (SNA) 3270 protocols, the CA12-TCP from Industrial Computer Controls, Inc, 196 Broadway, Cambridge, MA 02139, interfaces up to eight asynchronous terminals to IBM-compatible host processors. The converter emultates the Bisync 3271 and SNA 3276 cluster controllers to make asynchronous terminals appear as 3277-type and 3278-type devices, respectively.

Five different levels of conversion are provided. An industry standard interface generally ensures link level connection. Communications code conversion enables one device to recognize the intended character sent by another. At the protocol level, the converter maps data from one protocol to another. Device emulation reformats data to the specifications of an emulated device. At the device characteristics level, the command and control codes of one device are changed to those required by the other.

The converter supports either ASCII or EBCDIC communications on the synchronous links to the hosts; terminals communicate in ASCII on asynchronous links to the converter. Both half-duplex synchronous and full-duplex asynchronous communications are accommodated at speeds up to 9600 bits/s over EIA RS-232-C links. The converter can be connected directly to the host, or remotely via synchronous modems and dedicated lines. The asynchronous terminals can be local or remote over dial-up or dedicated lines.

A multitasking operating system executed on a Z80 microprocessor performs protocol conversion. A series of system function modules and links interprets commands from the host and formats the screen of the asynchronous CRT terminal so that it appears as a 3270 device. As data are transmitted from the host they enter a write module in the converter that updates an internal screen buffer called the virtual screen. The screen manager interprets the virtual screen to be in accord with the characteristics of the asynchronous terminal and transmits data to that terminal.

The software also interprets asynchronous terminal keystrokes to provide standard 3270 keyboard functions. As the terminal transmits to the host, data first enter the keyboard parser. This examines data typed on terminal keyboard, updates the virtual screen, and causes the screen manager to update the terminal. Data from the virtual screen enter the read module, which responds to read commands from the host. The keyboard parser can also bypass the virtual screen and cause the read module to transmit to the host.

The converter consists of three circuit cards: processor, memory, and serial interface. The entire unit measures 16.875 x 5.25 x 16.75" (42.86 x 13.3 x 42.55 cm) and weighs about 30 lb (13.5 kg). It will support 3270 emulation of such terminals as DEC VT-52 and VT-100, IBM 3101, Lear Siegler ADM-3, HP2621, Televideo 912 and 920, and Informer 304.

Circle 321 on Inquiry Card

Terminal series accesses two mainframes via dual protocol capability

Dual-protocol information terminals ECS 4000 series allow a single terminal to directly access two mainframes under the same protocol where two user addresses are involved, or under two different protocols for different types of mainframes. Introduced by ECS Microsystems, Inc, 215 Devcon Dr, San Jose, CA 95112, the series' currently available dual-protocol capabilities handle Burroughs TD 830, NCR 796-501, Honeywell VIP 7700 and 7801, and VT 52-compatible TTY emulations.

The dual-protocol capability is provided by universal protocol cards. Each card, which also contains firmware and I/O facilities, is configured to the required protocol. An executive P/ROM enables instant keyboard protocol selection. Each terminal is supplied with dual legend keys to handle protocol unique functions.

In local network applications multiple dual-protocol terminals can be concatenated from each line or modem. An auxiliary serial or parallel printer can also be supported with all original protocol printer functions.

Protocols can be selected in any combination, and kits are available for upgrading ECS 4000 terminals already in the field. IBM 3270 and UNIVAC U 200 emulations are scheduled for release in the near future.

Circle 322 on Inquiry Card

Local data distribution modem engineered for wire line systems

Synchronous local data distribution modem LOCALYNX^{R} GSU-1 is designed to operate on three of the most common wire line systems: telephone company local area data channels (LADCs), customer owned point to point wire line networks, or as a data service unit (DSU) replacement for remote termination in the Bell System's digital data service (DDS). The modem is offered by General DataComm Industries, Inc, 1 Kennedy Ave, Danbury, CT 06810, who say it is the first such unit to fill these applications.

The modem accommodates switch selectable 2400-, 4800-, or 9600-bit/s data rates, full duplex. Operating range is 7 miles (11.2 km) at 9600 bits/s over #26 AWG lines. Operating format is synchronous serial binary data without restriction as to data content. Bipolar return to zero modulation is used. Fully automatic line equalization handles changes in cable routing, bridge taps, or climatic conditions.

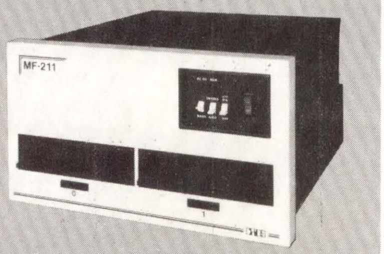
The modem can provide system timing from its crystal source, be timed externally by a terminal or CPU, or provide timing from the received line signal. Complete performance monitoring, fault isolation, and self-test capabilities are provided. The unit requires a 4-wire unloaded line facility.

Circle 323 on Inquiry Card

Build your own DEC system with CRDS...

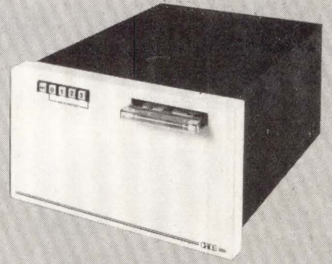
MF-211

10½" Enclosure for LSI 11/23 System with built-in RX02 equivalent floppy disk system. Available with or without processor and memory.



HD-11/T

20.8 Megabyte Winchester disk software equivalent to 4 RL01 units. Optional cartridge tape backup.

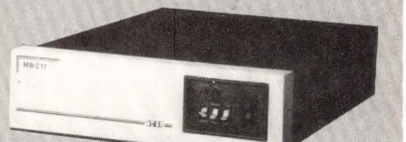


FD-311

RX02 equivalent dual floppy system, single or double sided. Includes bootstrap loader, self-tester, formatter and diagnostic diskette.

MB-211

5¼" enclosure with 8 quad slot backplane. Front panel console with switches for Enable/Halt, Boot/Init and Line Time Clock.



Complete software compatibility at a savings!

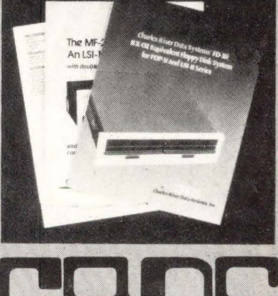
With CRDS, you can configure your own DEC system and be assured of complete software compatibility. Each of the above systems is provided with slides for rack mounting or can be used in desk top applications. All DEC LSI 11 based modules and associated software packages are available through CRDS, if desired.

Attractive Packaging
Careful attention is given the CRDS repertoire of enclosures in assuring you an attractive yet comfortable blending of product in the DEC environment.

Significant Savings
Flexibility of procurement plus attractive OEM schedules allows you to optimize dollar savings in configuring your CRDS system. Use the time tested technique. Compare.

Warranty and Maintenance
A 90 day warranty is offered with your CRDS system. In the event of malfunction, by use of provided diagnostic routines, the defective submodule is normally found within minutes. After verification with the CRDS Maintenance Department, a replacement for your defective module will be promptly forwarded.

Call or write for a comprehensive literature package and prices.

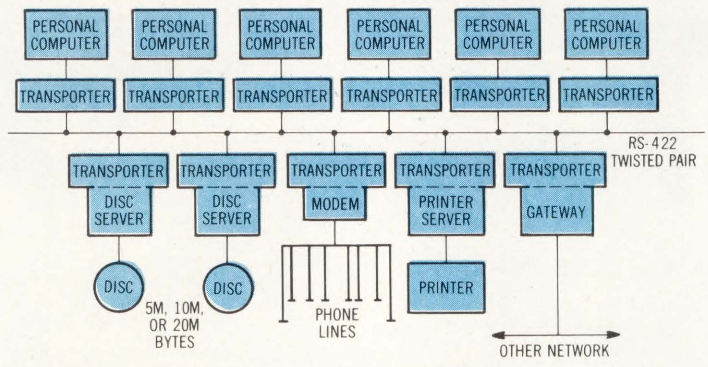


CRDS

Charles River Data Systems, Inc. 4 Tech Circle, Natick, MA 01760 Tel. (617) 655-1800 TWX (710) 386-0523

CIRCLE 27 ON INQUIRY CARD

High performance local net links up to 64 microcomputers, peripherals



OMNINET microcomputer network. Mass storage and printers are shared among 2 to 64 computers from different vendors. Gateways are planned to interconnect with other networks such as Ethernet and SNA

Highly efficient 1M-baud local data network OMNINET can interconnect up to 64 microcomputers and share mass storage and printers over a 4000-ft (1219-m) serial link. Corvus Systems, Inc, 2029 O'Toole Ave, San Jose, CA 95131, developers of the network, say it is the first such system to provide cost efficiencies in microcomputer local networks while offering the power and versatility of mainframe network systems.

The network uses RS-422 shielded twisted pair as the transmission medium; access is via carrier sense multiple access (CSMA). Heart of the system is the intelligent OMNINET transporter. This interface consists of a Motorola 6801 microprocessor, a custom gate array, and associated support components. Interfacing directly to the microcomputer or peripheral at any network node, the transporter provides error free transfer of variable length (up to 2k-byte) messages. No software intervention is required of the sending or receiving microcomputer. The system has no need for a network control processor, and the twisted pair data link does not need isolation circuits required by other networks. The network will operate with the company's CONSTELLATION software to provide up to 80M bytes of shared storage with multilevel file and user security, and spooled peripherals.

Initial product release of the network is available for Apple II, Onyx C8000, and DEC LSI-11. Future transporters will accommodate Apple III, Tandy TRS-80, any S-100 bus computer, Atari, Commodore, Altos, and others.

Circle 324 on Inquiry Card

Fiber optic multiplexer has hot standby for data flow protection

Sixteen-port fiber optic data multiplexer LDM-9500 is configured with a redundant hot standby transmission system to protect the entire electro-optical transmission path including the fiber optic cable. In the event of component failure or cable breakage the backup system automatically switches into operation to ensure the continuation of data transmission. A 4-fiber cable is required for a fully protected system. The multiplexer is a product of Valtec Corp, 99 Hartwell St, West Boylston, MA 01853.

Each of the unit's 16 ports can operate in asynchronous or synchronous mode. Data rate ranges are dc to 19.2k bits/s asynchronous and dc to 64k bits/s synchronous. The unit has full RS-232-C handshaking capability and accepts the standard EIA 25-pin plug as electrical input and converts directly to optical digital transmission. CCITT and MIL-STD-188 interfaces are available as options. Channel and system status are monitored by standard diagnostic and visual indicators.

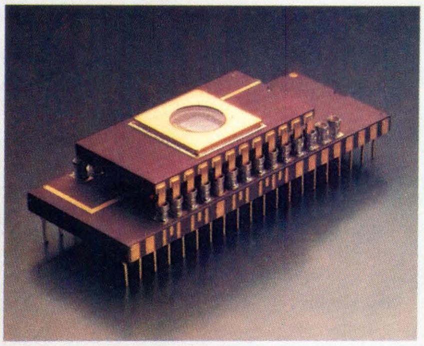
The multiplexer is also offered in 16-and 8-port unprotected versions. It is powered from a wall outlet and comes in either desktop or rackmount configurations.

Circle 325 on Inquiry Card

8 MICROS IN ONE.

For emulation or production, put the MK38P70 to work for you.

MOSTEK.



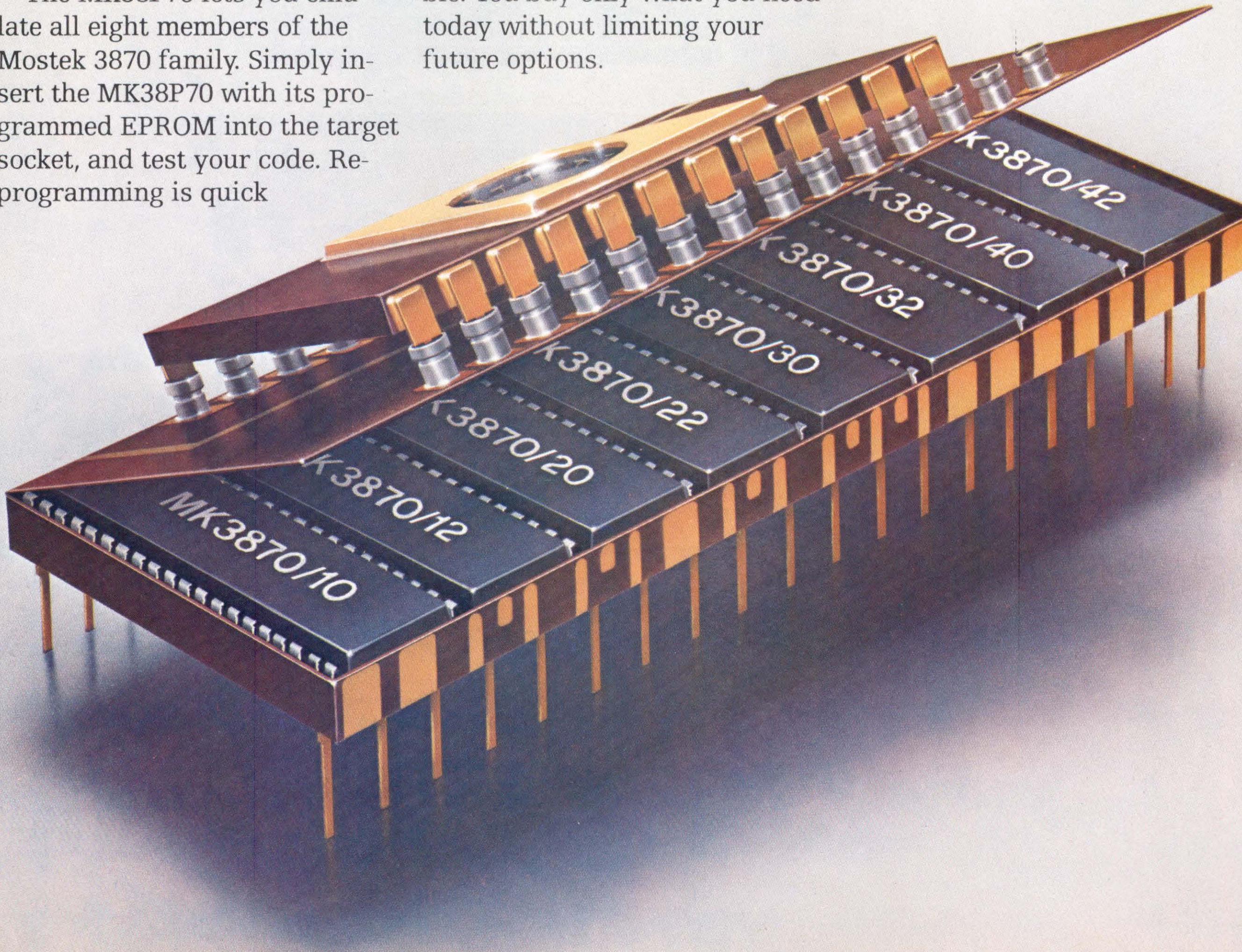
For 8-bit microcomputer applications, no other single-chip family gives you more design momentum than the Mostek 3870. Our piggyback EPROM MK38P70 is one reason why.

The MK38P70 lets you emulate all eight members of the Mostek 3870 family. Simply insert the MK38P70 with its programmed EPROM into the target socket, and test your code. Reprogramming is quick and efficient on any standard EPROM programmer.

A recent price cut makes the MK38P70 a very practical production circuit as well. In some cases, an MK38P70 is more economical than its masked-ROM counterparts. Plus it's available at your local Mostek distributor, and can be quickly put into production.

This single-chip family has been proven in hundreds of designs and millions of circuits. And all eight 3870 versions are hardware and software compatible. You buy only what you need today without limiting your future options.

Look at it another way: the MK38P70 gives you eight different custom chips in one standard package available at all Mostek distributors. That's design momentum. Put it to work for you. Call or write Mostek Corporation, 1215 West Crosby Road, Carrollton, Texas 75006; phone (214) 323-1801. In Europe, contact Mostek Brussels; phone 762.18.80.



CIRCLE 29 ON INQUIRY CARD


ALTOS
BRAND
QUALITY
RELIABILITY
DELIVERY
PROVEN VALUE
COMPUTER · SYSTEMS
PRODUCED IN THE HEART OF SILICON VALLEY, CALIFORNIA U.S.A.
ALTOS
ALTOS

BUMPER CROP

8-inch Winchester Multi-User Systems. Now In Volume-$8,500.

Altos is delivering the cream of the crop with their new 8-inch multi-user Winchester disk systems. They're freshly packed with the quality features you expect from Altos, and at a price you expect from Altos, too—just $8,500.

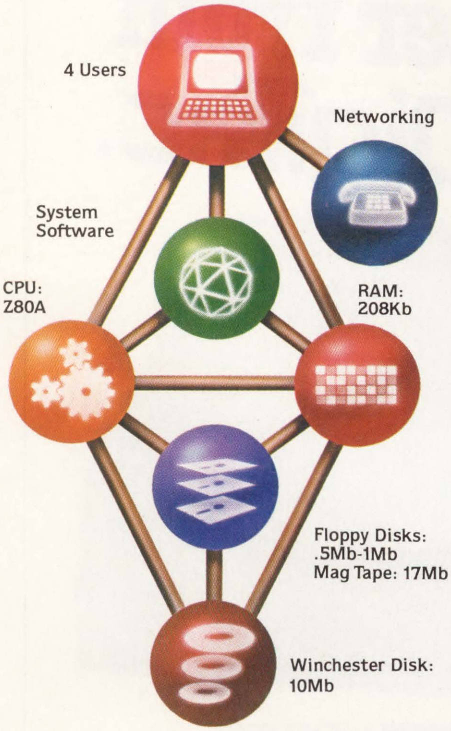
Pick from two fully integrated systems, each packaged in our new compact, stylish cabinet suitable for either rack mount or table top applications. You get 10 MBytes of reliable on-line storage in our 8-inch Winchester drives. Then for system back-up storage, you can select from either 8-inch, single or double-sided floppy drives (ACS8000-10 and -10D) or a ¼-inch magnetic tape drive (ACS8000-10/MTU). And for powerful performance, all of these Z80A*based systems come complete with 208K of RAM and 6 programmable serial ports, ready to support four users.

Here's the most bountiful selection of systems and capacities in the field from the company that knows how to deliver quality systems in the volumes that OEMs need to stay competitive.

And Altos supports these systems with a broad software selection including the three industry standard operating systems—CP/M, multi-user MP/M** and OASIS†. These operating systems support seven high level programming languages: BASIC, FORTRAN, COBOL, PASCAL, APL, PL/1 and C. Also available are comprehensive communications packages: ASYNC—Altos-to-Altos, BISYNC—Altos-to-mainframe and full networking with CP/NET. All are designed to run on a high speed 800 Kilobaud networking channel—standard with every system.

The ACS8000-10 Winchester systems join our growing family of field-proven products. In just three years, more than 8,000 systems have been shipped to an OEM customer-base.

Get to market fast. Harvest your 8-inch Winchester system direct from the heart of Silicon Valley. Call or write today for specific product information and OEM pricing. Altos Computer Systems. 2360 Bering Drive, San Jose, CA 95131, (408) 946-6700, Telex 171562 ALTOS SNJ.



SYSTEMS PICTURED:

ACS8000-10 (10Mb HD + 1 floppy)	$ 8,500
ACS8000-10/MTU (10Mb HD + DEI Mag Tape)	$10,990

Packed with Fresh Ideas

ALTOS
COMPUTER SYSTEMS

---

*Z80A is a registered trademark of Zilog, Inc.
**CP/M and MP/M are registered trademarks of Digital Research, Inc.
†OASIS is a registered trademark of Phase One Systems, Inc.
‡datapro is a registered trademark of Datapro Research Corp.

BRIEFS

Statistical multiplexer has user switching option—Latest in its DCX line of statistical multiplexers, the DCX850 from Rixon Inc, 2120 Industrial Pkwy, Silver Spring, MD 20904, offers compacted error free transmission of up to 240 channels over as many as 12 composite links. A user switching option (USO) module provides selectable switching and port contention, network monitoring, and statistics reporting. It allows users at designated ports to connect their terminals to any other compatible port anywhere in the network. Several users can contend for a limited number of computer ports. Automatic hardcopy reports of important network events as well as network statistics are provided. The multiplexer holds two network maps in memory to facilitate reconfiguration of networks.

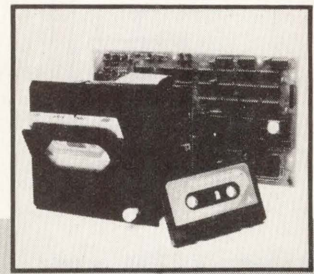
Circle 326 on Inquiry Card

Bisync option available on multiplexer line—Binary synchronous (Bisync) option is now available on the CM9100 statistical and SM9200 switching multiplexers from Digital Communications Corp, 11717 Exploration Ln, Germantown, MD 20767. The option supports point to point and polled terminals, transparent and nontransparent modes, external and internal clock options to 9600 bits/s, and EBCDIC and ASCII codes. Data channels can be independently set to handle either IBM-compatible Bisync or asynchronous data. When Bisync is chosen, the data channels support terminals using 2780, 3780, or 3270 Bisync protocol, or any similar protocol conforming to IBM Specification GA27-3004. The units statistically multiplex actual Bisync protocol sequences on the data link with asynchronous data from other channels.

Circle 327 on Inquiry Card

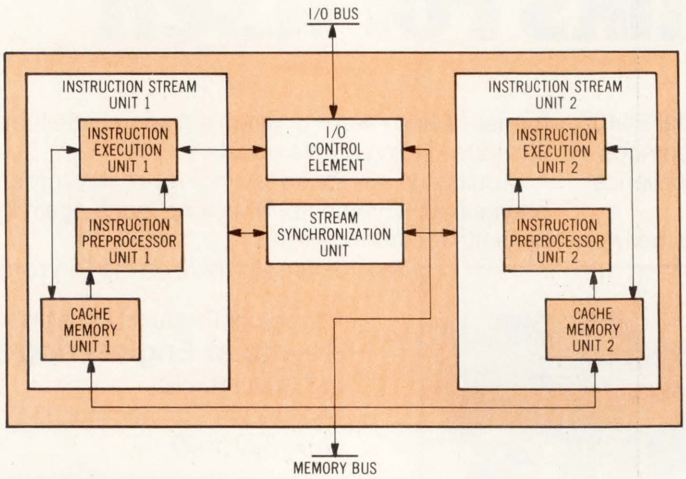
Statistical multiplexer/concentrator uses X.25 level III protocol—Intelligent multiplexer/concentrator TC 5000 allows transmission of up to 24 channels of asynchronous data over a single data link using X.25 level III protocol. The device, from DCD Telecommunications Inc, 160-162 N Main St, Mansfield, MA 02048, incorporates user command language and intelligent echoplex. Data channels are individually programmable for throughput delay, priority, data rates to 19.2k bits/s, 5 to 8 level codes, flow control, and parity. Dial-in, autobaud, and DCE/DTE channel format are standard. The system has 32k buffer overflow, internal/external clock to 19.2k bits/s, choice of packetizing timeouts, and dual-backup links with autodial. Buffer expansion, data encryption, and tandem configuration are available as options. ☐

Circle 328 on Inquiry Card




Raymond Engineerin
Data Cassette

32-bit multi-user virtual memory minicomputer implemented with multistreaming architecture



Major functional elements of Prime's multistreaming 32-bit virtual memory minicomputer are two instruction stream units and stream synchronization unit. System architecture allows two streams of instructions to be processed simultaneously, providing higher throughput than comparable systems

Multistreaming architecture of the series 50 model 850 provides 50% more throughput than current multi-user virtual memory superminicomputers. Central to the multifunctional high end system introduced by Prime Computer, Inc, Prime Pk, Natick, MA 01760, are its 2M- to 8M-byte, 2-way interleaved main memory composed of 1M-byte memory boards built using 64k-bit MOS RAM chips, and support for 128 directly connected terminals. Burst mode I/O transfers 64 bits of data per burst request at a rate of 8M bits/s.

The 32-bit internal architecture allows operating efficiency and large program support. Full 32-bit word length allows more information to be processed during each machine cycle than is possible with 16-bit architecture. In addition, 32-bit word length allows for specification of a very large number of memory address locations. The PRIMOS operating system uses efficient virtual memory management to provide each user with 512M bytes of virtual address space, of which 32M is reserved for user program space. System software functions are embedded in the virtual address space of each process, making all functions available on demand.

Multistream architecture allows two instruction streams to be processed in parallel, significantly increasing system throughput. Parallel stream processing is managed by the operating system for maximum system efficiency. Main memory, ranging from 2M- to 8M-byte capacity, is shared by both streams to dynamically fulfill demands on memory requirements.

Two parallel instruction stream units (ISUs) within the system access the same main memory through a common memory bus. Each ISU is made up of an instruction preprocessor unit, instruction execution unit, and 16k-bit cache memory unit. The instruction preprocessor improves CPU performance by prefetching and decoding four instructions ahead of the program counter from cache memory. It accesses cache independently, so that the next four instructions are prefetched, decoded, and the effective address formed in parallel with instruction execution. Central logic in the instruction preprocessor continuously prefetches data from cache to keep the four instruction buffers full. In addition, the preprocessor can resolve most indirect addresses, further increasing instruction execution speed.

The instruction execution unit consists of floating point arithmetic logic unit (ALU), decimal ALU, integer ALU, and execution control unit. The cache memory unit stores frequently used data and instructions for rapid access and greatly reduces memory overhead. A stream synchronization unit protects both ISUs from invalid cache references and manages internal system messages between ISUs. It also maintains memory access synchronization and performs internal diagnostics to ensure integrity of the data flow.

The execution control unit (ECU) uses a comprehensive set of firmware instructions to implement processor control mechanisms. Microinstructions reside in ROM that has a 52-bit word length that expands to 64 bits. The process exchange facility within the ECU automatically transfers the attention of either instruction execution unit from any of the 128 different user processes to any other. Context switching mechanisms are implemented in both hardware and firmware for rapid process exchange and minimal system overhead.

Instructions for single- and double-precision floating point arithmetic are implemented in hardware. With a 32-bit path between the unit and CPU, data are accepted at a fast rate. Parallel logic used within the unit permits exponential and fractional calculations to be done simultaneously. Separate parallel logic performs binary multiplication 4 bits at a time, division 3 bits at a time, and addition 48 bits at a time. Decimal arithmetic instructions are also implemented in hardware.

System integrity is maintained through microverification routines automatically invoked to test validity of CPU logic. Parity checking ensures data integrity throughout the system's internal buses, registers, and other data paths. A virtual control panel provides for local and remote system diagnostic capability.

The PRIMOS operating system supports both interactive and batch processes. It supports reentrant procedures as well as the database management system and DBMS query report writer. PRIMENET software supports networking and distributed processing, allowing interface to a range of terminals with multiple protocols and remote job entry options.

Circle 350 on Inquiry Card

FROM MONOCHROME TO MULTICOLOR. THE AED 512 DESK-TOP TERMINAL.

Since Chinese calligraphy originated over 2,000 years ago, familiarity with more than 10,000 individual characters is required to read and appreciate classical Chinese literature. With 256 simultaneous colors at your disposal, producing more than 16 million hues, each of these characters can be given a different shade on the AED 512 desktop terminal.

The AED 512 offers programmable symbols, plus powerful imaging and graphics capability for use in business, medical applications, scientific study and CAD—and is easily attached to your computer. It emulates Tektronix 4010-15 software, and DMA interfaces for most mini- and microcomputers are available.

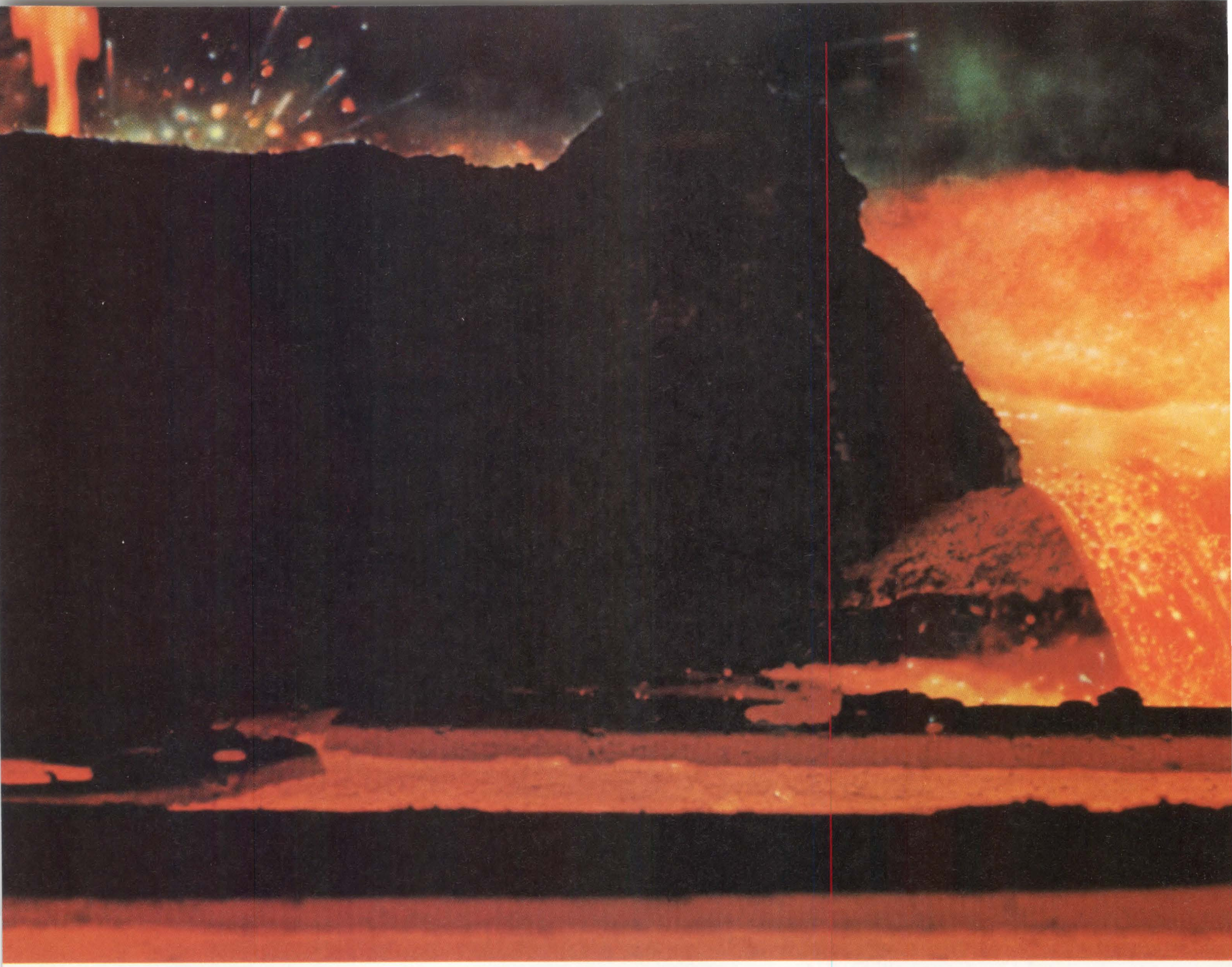
Features like 512^2 (512 x 483) pixel screen, Superoam™, 1-16 integer zoom, continuous panning, down-loadable microcode and half-second image transfer make the AED 512 the performance leader in intelligent graphics terminals. Write or telex our marketing department for complete technical details today. We'll show you why 1981 is THE YEAR OF AED!

™Superoam is a trademark of AED

Advanced Electronics Design
440 Potrero Avenue
Sunnyvale, CA 94086
408-733-3555
Telex 357-498

Boston: (617) 256-1700
LA: (213) 705-0379

CIRCLE 34 ON INQUIRY CARD



Some environments for bubbles.

Intel introduces the iSBC 254™ Bubble Memory Board. The non-volatile Multibus™ memory system that goes where disks and tapes can't go. All in time for today's designs.

Bubbles store data in environments that bewitch storage devices such as disk and tape drives. That's because as solid-state devices, bubbles are unaffected by the heat of a factory floor, the roll of a ship or the dust of the desert wind. Since all that moves is information, bubbles aren't plagued with the wear and tear and related maintenance problems of electromechanical devices.

They're non-volatile, so you don't have to worry about battery back-up. And because bubbles pack 1 million bits of data in an area less than 100 square centimeters, they can boost the performance of a portable data logger, as well as an in-house numerical control system.

Kindle your product development

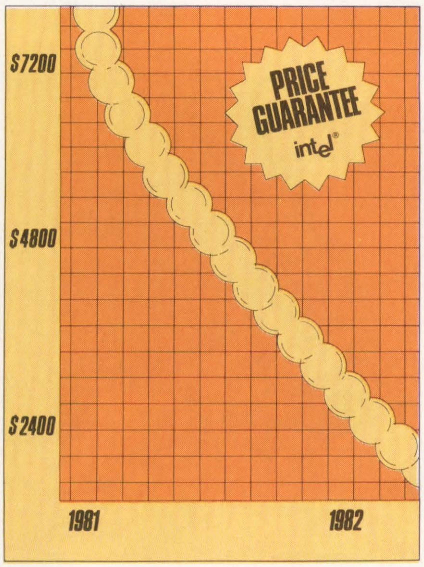
Now there's a fast, easy way for you to capture these advantages in your products: the iSBC 254 Bubble Memory Board. It puts from 128K to 512K bytes of Intel's 7110 bubble memory—complete with controller and support circuitry—on a 12 x 6.75-inch Multibus board. That's the same bubble memory and controller that's already storing data onboard ships and on factory floors. All pretested. And ready to run in your system today.

When you slip the iSBC 254 board into your Multibus-compatible chassis, it operates like any other microcomputer mass storage system. You choose from several I/O modes, including Direct Memory Access. You access data in a flash—several times faster than you can with a floppy. And move it at rates up to 50K bytes per second.

Add fuel to the fire

What's more, you can complement the performance of the iSBC 254 board in your system with any of a wide variety of Intel® Multibus boards

are a natural



Pricing for the iSBC 254™ board tracks the downward price curve of bubble memory components.

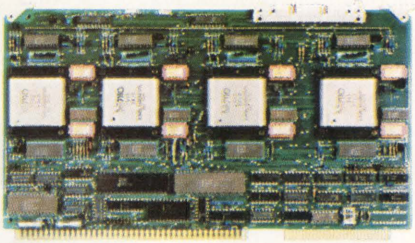
and software products available today. From 8- and 16-bit single-board computers, to analog and digital I/O, to real-time operating systems, complete with software drivers for bubble memory. Or if you want to configure your own board, you can start with Intel's Bubble Memory Prototype Kit (BPK72). It has everything you need to tailor Intel's 1-megabit bubble memory to your product.

Get the benefit of the continuous price reduction process

Like all of Intel's bubble memory products, the iSBC 254 board benefits from Intel's bubble memory price guarantee. By the end of 1981, the price of the 512K-byte board will be 34 percent lower than today's price on 100-quantity orders. After that, price reductions will continue tracking the downward spiral of bubble memory component pricing.

Put your competition on the back burner

The iSBC 254 bubble memory system is available off the shelf today. So you can start now to build the bubble's advantages into your systems. Reduced service and repair costs. Less preventive maintenance. Data integrity in hostile environments. And, as you do, you can open new frontiers. Ahead of your competition.



Find out more about how Intel bubble memory systems can help put you ahead. Contact your local Intel sales office/distributor. Or fill out the coupon below and send it to: Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call our toll-free hot line (800) 538-1876.

CD6

- ☐ I want to kindle my product development for bubbles. Have a sales representative call me with quantity price information on the iSBC 254 Bubble Memory Board.
- ☐ I want to find out more about bubble components and boards. Rush me a copy of the *Bubble Storage Data Catalog* by first class mail.
- ☐ I want to tailor bubble memory to my unique system configuration. Rush me information on the BPK72 Prototype Kit and the BPK70 Production Kit by first class mail.

Name ______________________

Title/Organization ______________________

Address ______________________

City/State/Zip ______________________

Telephone (   ) ______________________

Application ______________________

____

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

intel® delivers solutions

CIRCLE 35 ON INQUIRY CARD


LEXIDATA

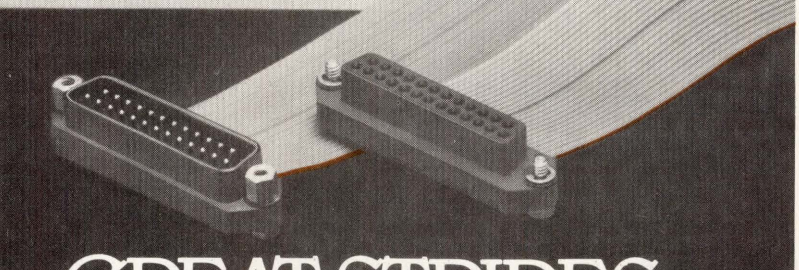
600-line/min printer features operator activated self-test capability

"LP Series" 600-line/min band printer subsystems are available in two versions that are plug-compatible with many DEC, Data General, and IBM systems. One is a standard pedestal mounted unit with open paper path (LPS); the other a totally enclosed "office quiet" version (LPQ) that keeps the noise level to less than 60 dBA.

Introduced by Centronics Data Computer Corp, Hudson, NH 03051, both models feature a printer mounted, operator activated self-test capability, built-in microprocessor electronics, and 600-line/min speed. Interfaces for DEC's PDP-11, LSI-11 and VAX-11/780, Data General's Eclipse and NOVA (programmed I/O and data channel), and IBM's Series/1 systems are available.

Self-test capability is switch actuated at the printer, enabling the operator to generate a test pattern which originates in the controller and loops through the entire subsystem. This verifies the condition of the printer, and the controller and interconnector cables as well. Choice of 48-, 64-, 96-, and 128-char print bands is provided. Paper jam and paper-out sensors, and a long life ribbon cassette are other features. Printout specifications include a 132-col print line with 10-char/in (3.9/cm) horizontal spacing and 6-, or 8-line/in (2.4 or 3.1/cm) vertical spacing.

Circle 351 on Inquiry Card



Small programmable controller designed for operation on plant floor

A compact controller with Intel 8049 based CPU, power supply, I/O track, and portable programmer, EPTAK^R 200 provides capabilities for up to 128 I/O points, capacity for 420 programming statements, a total of 32 timers or counters in any combination, two 32-stage bit shift registers, 128 control relay functions, up to 8 data registers, 6 comparisons, and an arithmetic capability. In designing the controller, Eagle Signal Industrial Controls, a division of Gulf + Western Manufacturing Co, 736 Federal St, Davenport, IA 52803, provided digital programmable logic control for thousands of small industrial applications currently using hardwired relay control systems or card logic systems, to replace other less capable small programmable controllers.

The processor in the controller has 1k CMOS RAM battery protected user memory and a 420 program statement capacity. It has a scan time between 2 and 35 ms with 20 ms typical. Program data retention is 90 days without external power. Mounted with the processor is the I/O track containing up to 16 dual-point modules for a maximum of 32 I/O points per track. The system can be expanded to 128 I/O points using a total of 4 tracks.

Color-coded plastic I/O modules allow the operator to easily distinguish inputs both from outputs and from other track mounted modules. Simulator modules that plug directly into the I/O track enable fast reliable system checkout and debugging without the need for a separate simulator. A watchdog timer module, also track mounted, monitors processor memory scanning and activates in 0.25 s if a failure occurs.

The system features a compact, portable programmer measuring 7.75 x 8 x 2.75" (19.7 x 20 x 6.9 cm) with power cord and battery protected memory that allow it to be programmed independent of the processor. Programming is bidirectional, so that a program stored in the processor memory can be transferred to the programmer for editing. Conventional relay ladder logic is used for easy programming. Function keys are labeled with both relay symbols and mnemonic characters. A separate keypad provides diagnostic and editing functions.

Peripherals include timer/counter access module that enables setpoints, actual values, and/or changing timer/counter setpoints to be monitored at remote locations up to 500' (152 m) from the processor. A compact impact printer provides hard copy of program statements; a magnetic card recorder/loader stores up to 1k of data; and an auxiliary interface enables users to utilize remote BCD or binary inputs and outputs such as thumbwheel switches and displays.

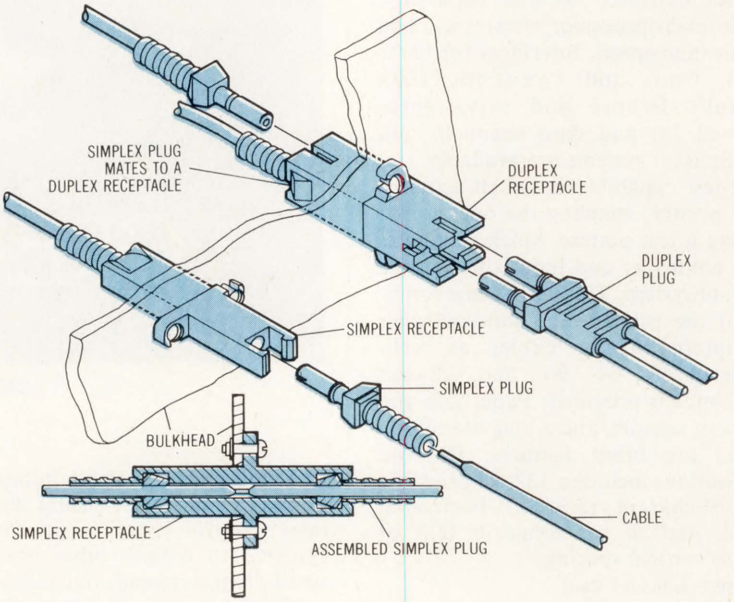
Circle 352 on Inquiry Card

Fiber optic components break price barrier in short range transmission

A fiber optic interconnection system targeted at low cost data transmission, Commercial Optimate connectors are priced at around 25¢ each. These components from Amp Inc, Harrisburg, PA 17105, operate with 1000-μm plastic fiber and TO92 packaged emitters and detectors to produce an 88% reduction in the cost of a fiber optic link, and provide a cost-effective solution for applications in the 10- to 30-m range with data rates up to 10M baud.

A significant part of this reduction is in labor required to apply the devices in the system. Glass fiber requires 15 min to prepare the cable, apply the adhesive, and grind and polish the fiber; previously available connectors used with plastic fiber also required a polishing step. The low cost connectors require no epoxy, polishing, or special tools for application.

To attach a plug, the fiber's protective jacket is stripped and the cable is inserted from the rear of the plug body until the jacket bottoms inside the plug cavity and the protruding fiber is cut off flush with the tip of the plug. The whole process takes about 12 s. A brass retention clip inside the body of the plug anchors the cable in place to withstand an 8-lb (3.6-kg) axial pull. Application of the quick-fix splice is equally simple; retention clips are positioned on the ends of the cable, excess cable is trimmed flush with the leading end of each clip, and clip/cable assemblies are inserted into opposite ends of the splice housing until they bottom.



Commercial Optimate interconnection system developed by Amp simplifies installation and cuts cost of short range fiber optic transmission systems

While low cost, all-plastic fiber emitters and detectors suitable for use in limited distance applications have become available recently, total systems cost has been kept high by the expense of the connectors necessary to complete the link. Estimates demonstrate that the cost of a system can be reduced 56% by choosing all-plastic instead of glass cables, and 19% further by use of recently introduced low end emitters and detectors; however, these costs can be reduced 74% more by use of low cost connectors.

When mating the plug to a receptacle or active device mount (with 3-lb or 1.4-kg insertion force) an audible and

(continued on page 60)

Price breakthrough: $499.

For a CMOS microprocessor development system.

Our new CDP18S693 costs less than any other 1802 microprocessor development system on the market. And the development system can even become your final target system.

The incredibly low $499* price includes:

- CDP18S601 computer Microboard.
- ROM/audio cassette controller Microboard.
- Five-card chassis and case.
- Detachable 5-volt power supply.
- Audio cassette tape I/O drive for mass storage.

You get these capabilities:

- Extended BASIC resident in ROM with full floating-point arithmetic.
- 2K-byte monitor program with extensive memory manipulation.
- RS232C or 20 mA terminal interface, up to 1200 baud.

Or, for $799,* you can get the CDP18S694. It has all the capability of the 693, plus:

- ROM-based 1802 Assembler/Editor.
- PROM Programmer board.
- A second cassette tape I/O drive.

System expansion:

- Expand your Microboard system capability, choosing from over 40 expansion boards and hardware accessories.
- Memory expandable to full 65K bytes.
- Virtually unlimited I/O expansion capability using any combination of analog and digital I/O boards.
- Run-time BASIC 3 firmware for final system configuration.

Develop software for any 1802-based component design, or for any Microboard system in BASIC or assembly language.

At these prices you can't afford not to get into CMOS.

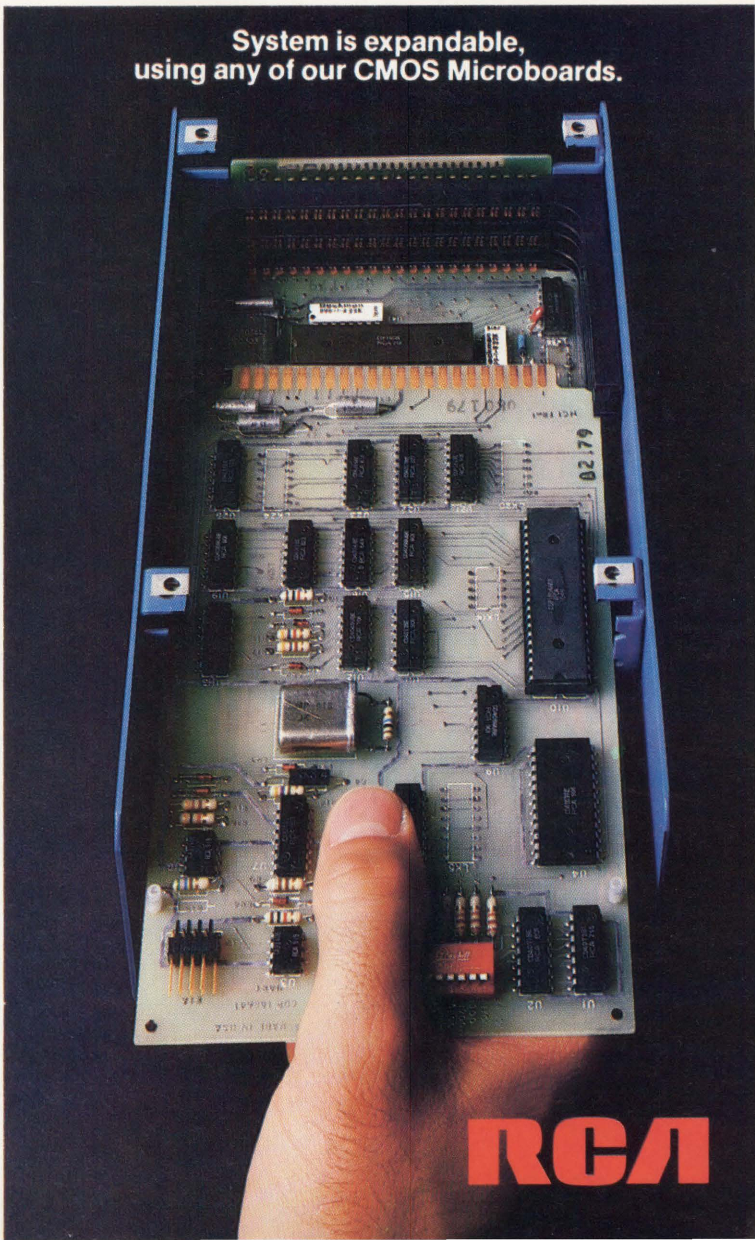
For more information, contact any RCA Solid State sales office, sales representative or distributor.

Or contact RCA Solid State headquarters in Somerville, N.J. Brussels, Belgium. Sao Paulo, Brazil. Hong Kong.

Or call Microsystems Marketing toll-free (800) 526-3862.

* U.S. optional distributor resale, single unit price.

CIRCLE 39 ON INQUIRY CARD



Bread & Bu

Count on a full selection of low-density PROMs from Signetics, your leading bipolar memory supplier.

As you inspect our menu of tempting PROM selections, don't overlook the bread-and-butter PROMs. Signetics' 256-bit, 1K, 2K, and 4K PROMs have long been and will continue to be the staple of the industry.

You'll find the PROM organization and specs you need from a wide selection of low-density parts. Both Schottky TTL and high-speed ECL, with your choice of three-state or open-collector outputs for maximum design flexibility. In memory or logic applications.

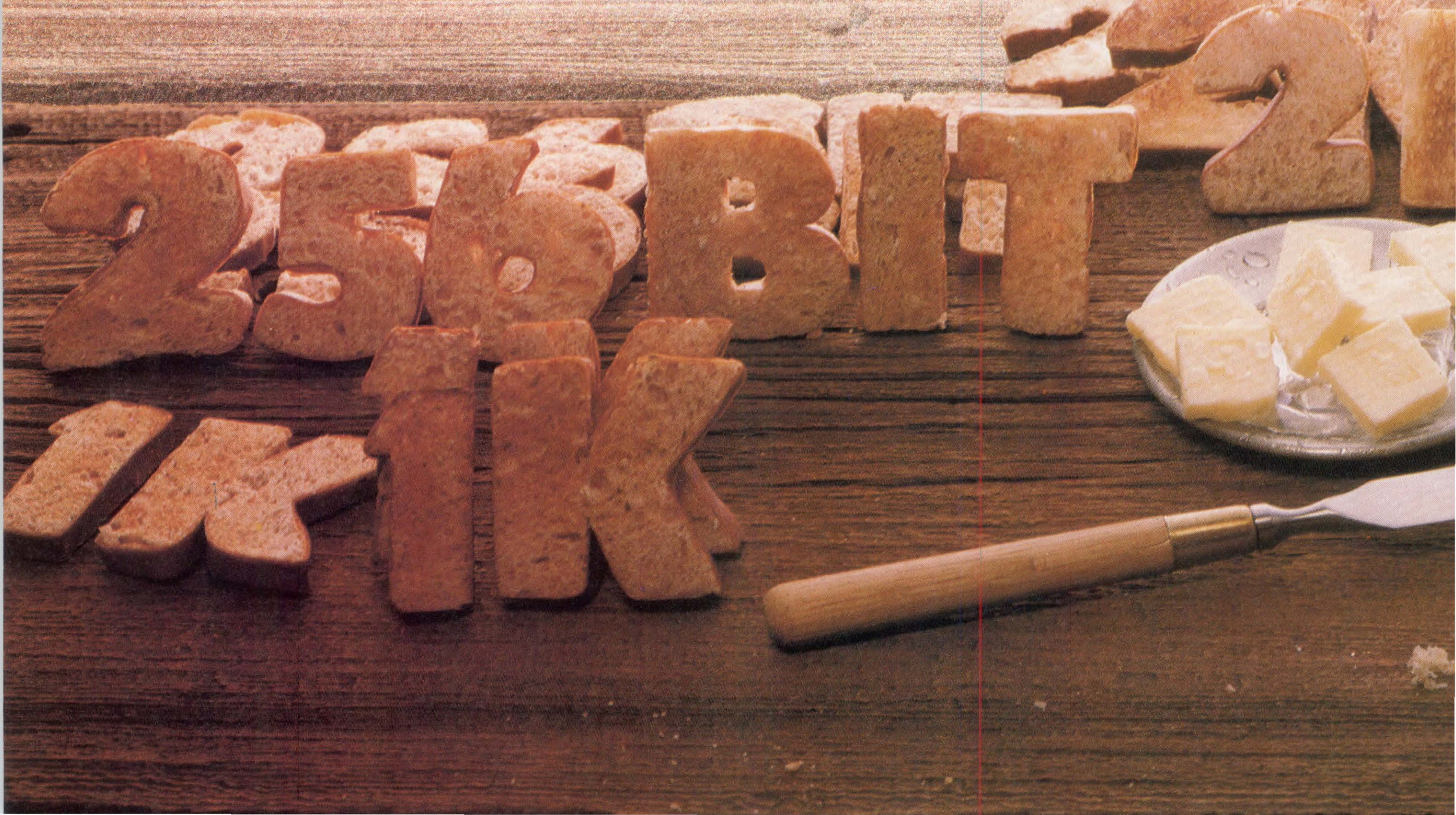
They're packaged and tested to commercial and military temperature ranges. And they offer a cost-effective programming yield that's the envy of the industry.

Once you've sampled our low-density, high-quality parts, you're sure to come back for more.

You'll also want to feast on other Signetics high-performance PROMs. Like our 8K power strobe device that cuts your power supply requirements by a factor of 10.

For dessert, high-speed 4K and 8K PROMs are the icing on the cake. Their access times are 45ns and 55ns, respectively—with even faster speeds in the oven.

Service is prompt and efficient. With new PROM production capacities for anything from a snack to a banquet we're ready to take reservations for your high-volume requirements.



tter PROMs.

BIPOLAR MEMORY SELECTION GUIDE

DENSITY	DEVICE TYPE	ORGANIZATION	OUTPUT CIRCUIT	ACCESS TIME (ns)	I_{CC}MAX. (mA)
256-Bit	82S23	32X8	OC	50	77
256-Bit	82S123	32X8	TS	50	77
256-Bit	10139	32X8	OC	20	145
1K	82S126	256X4	OC	50	120
1K	82S129	256X4	TS	50	120
1K	10149	256X4	OC	20	150
2K	82S130	512X4	OC	50	140
2K	82S131	512X4	TS	50	140
4K	82S115	512X8	TS	60	175
4K	82S141	512X8	TS	60	175
4K	82HS147	512X8	TS	45	155
4K	82S137	1024X4	TS	60	140
4K	82HS137	1024X4	TS	45	140
8K	82S180	1024X8	OC	70	175
8K	82S181	1024X8	TS	70	175
8K	82LS181	1024X8	TS	150	80
8K	82PS181	1024X8	TS	70	185
8K	82HS181	1024X8	TS	55	175
8K	82S2708	1024X8	TS	70	175
8K	82S183	1024X8	TS	60	175
8K	82S185	2048X4	TS	100	120
8K	82HS185	2048X4	TS	60	155
16K	82S191	2048X8	TS	80	175
16K	82HS191	2048X8	TS	60	175
16K	82S195	4096X4	TS	70	155
32K	82S321	4096X8	TS	90	175

To find out more about Signetics' broad PROM line, send the coupon below. Or contact your nearby Signetics sales office or authorized distributor. *Signetics Corporation, 811 E. Arques Ave., P.O. Box 409, Sunnyvale, CA 94086. (408) 739-7700.*

signetics

a subsidiary of U.S. Philips Corporation

Multiple Technologies from 8 Divisions:
Analog, Bipolar Memory, Bipolar LSI, MOS Memory, MOS Microprocessor, Logic, Military, Automotive/Telecom

To: Signetics Publication Services, 811 E. Arques Ave.,
P.O. Box 409, MS 27, Sunnyvale CA 94086 CD 6-81

☐ Please send me technical data on low-density PROMs.
☐ I'd like additional data on the new high speed PROMs.
☐ Send me general product reference material on all PROMs.
☐ I have an urgent requirement. Please have a PROM specialist phone me at once at:

( ) ________________ ext. ______

Name ________________ Title ____________

Company ______________ Division __________

Address ________________________ MS ______

City _______________ State _______ Zip _______ tactile snap indicates when the plug is bottomed and latched into place. A 6-lb (2.7-kg) extraction force is required to disconnect a plug from its mating receptacle.

Performance depends largely on the end surface finish of the end of the all-plastic fiber. Cutting the fiber with a razor blade results in insertion losses under 4 dB. Cutting it with a host knife produces a surface finish that yields insertion losses of less than 2 dB. Application of an index matching liquid reduces insertion losses more than 50%.

Currently available components of the connector system are single- and dual-position plugs, single- and dual-position bulkhead receptacles, splice housing, and single-position active device mounts for TO92 and TO46 type packages. The system is compatible with 1000-μm all-plastic fibers with 2.2-mm OD jacket manufactured by Mitsubishi and with emitter and detector packages of the TO46 type such as Honeywell Spectronics' Sweet Spot devices, as well as TO92 devices. LEDs include Motorola MFOE500 and Spectronics SE 4352; and detectors include Motorola MFOD550 TTL receiver and Spectronics SD4478 pin diode, SD4323 phototransistor, and SD4324 200k-bit/s receiver.

Circle 353 on Inquiry Card

Multitasking system expands to handle multi-user batch, online, or distributed tasks

TFC 8500 starts with an entry level single workstation and expands to 80 local and remote workstations. The system, developed by the TRW-Fujitsu Co, 9841 Airport Blvd, #620, Los Angeles, CA 90045, operates as a standalone unit, online to a central computer, or in a TFC 8500 network. It can perform batch, online, or distributed processing applications. Advanced computer design concepts and the use of LSI circuits endow the system with its range of capabilities, including complete software compatibility throughout all configurations. Main storage unit uses 64k MOS LSI devices and has 256k bytes capacity. Add-on storage units permit expansion up to a maximum of 2M bytes. Storage cycle time is 400 ns/2 bytes. The central processing unit contains a single-chip, 10,000-gate microprocessor and 700-gate/chip high speed bipolar LSI circuits and features virtual memory capabilities.

The small number of high density IC circuits use considerably less power than conventional 16k and 1,000-gate devices. As a result of this and other design features, the system does not need a special cooling system. The LSI chips and microprogram controlled circuits also permit a reduction in the number of hardware components, making possible a board/function design, which contributes to enhanced reliability and price-performance ratio.

The system is delivered with FORTRAN, COBOL, and RPG languages. Peripherals include disc storage, display, and printer workstations, magnetic tape units, and line printers. Up to eight disc storage devices in any combination of fixed and removable cartridge units may be connected up to a maximum storage size of 800M bytes. An error checking and correction code for main and disc storage, as well as a retry function for processor and peripheral units, allows automatic error recovery. A variety of diagnostic functions and programs automatically check the system and provide input for effective preventive maintenance.

In a multiple workstation configuration, local workstations can be as far as 1500 m (almost 1 mi) away from the CPU. When operated as part of a computer network, the 8500 can communicate over telephone lines with a host computer interactively or in batch mode through remote job entry.

Circle 354 on Inquiry Card

Entry level computers provide 1M-byte memory and midrange performance

With megabyte memory capacity and midrange capabilities, the entry level PDP-11/24 has 90% of the integer performance of the -11/34A and complements the upper-midrange -11/44. Features of the machine, introduced by Digital Equipment Corp, Maynard, MA 01754, include custom MOS/LSI technology, UNIBUS™ architecture, and full PDP-11 family hardware and software. Options include floating point instruction set, 22-bit extended addressing, and battery backup.

A general purpose minicomputer suited for both end user and OEM applications, the machine has four times the memory expansion of the -11/34A at a 25% to 30% lower cost. The basic unit has twice the memory and twice the performance of the older -11/04 while costing only 30% more. High packaging density makes it attractive as an alternative to the -11/34A, particularly for build-in applications where smaller size is critical. Standard packaged system includes three hardware configurations that run under the RT-11, RSX-11, and RSTE/E operating systems, and four commercially oriented, PDP-11/24 based Datasystems that run under CTS-300 and CTS-500 operating systems.

The machine employs a single hex-height central processor module with custom MOS/LSI technology, the extended PDP-11 instruction set, and the memory addressing extension previously available only on the -11/44 and -11/70. The central processor is available in 5.25 and 10.5" (13.34 and 26.7-cm) high chassis. The smaller unit provides a maximum 768k-byte memory using the 22-bit extended addressing option; the larger accepts a full megabyte of memory. The central processor has on-board provisions for the floating point instruction set as well as for a commercial instruction set to be announced later. Extended addressing option enables memory capacity to expand to a full megabyte.

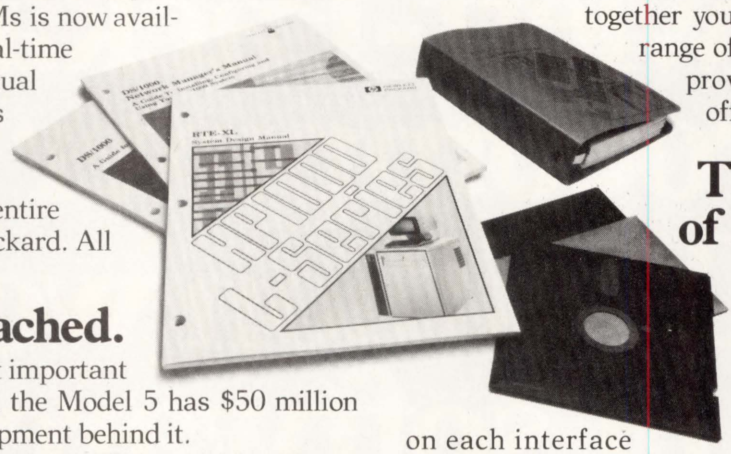
The machine supports the range of PDP-11 software, and has networking and communications capabilities enabling it to be linked to other DEC computers with DECnet software, and other manufacturers' computers via Internet software. Packaged system configurations consist of one with 128k bytes of memory, dual RX02 floppy disc drives, and choice of DECwriter IV hardcopy or VT100 video terminal; one with 256k bytes of memory, dual 10.4M-byte RL02 discs, and choice of VT100 or DECwriter III terminal; and one with 256k bytes of memory, dual 28M-byte RK07 disc drives, and a DECwriter III terminal. Datasystems based on the -11/24 are 346 and 348 using CTS 300 operating system and the 522 and 528 using CTS 500. Datasystem 346 supplies 128k bytes of memory, dual RL02 storage discs, and VT100 terminal; 348 has 256k-bytes memory, dual RK07 discs, and VT100. Datasystem 522 offers 256k-bytes memory, DECwriter II terminal, and dual RL02 discs; 528A provides 256k-byte memory, dual RK07 disc, and DECwriter III. Datasystem 528E has the hardware of the 528A with the extended addressing option and 512k bytes of memory plus the COBOL programming language.

Circle 355 on Inquiry Card

Full system support.

Announcing the new HP 1000 L-Series Model 5 microsystem.

The same two-board microcomputer that's becoming so popular with OEMs is now available as an integrated, real-time system—complete with dual minifloppies, 128K bytes of memory, your choice of interactive terminals *and* full support for the entire system from Hewlett-Packard. All for under $10,000.



All strings attached.

Software is the most important part of any system, and the Model 5 has $50 million worth of software development behind it.

You can start with either RTE-L or RTE-XL, our powerful multi-programming, multi-user operating systems. Their modular construction lets you build the real-time computing environment your applications programs demand—programs you can develop in Assembler, FORTRAN 4X and BASIC. And our HP DSN networking software makes it simple to put low-cost computing wherever you need it.

Data base management on a microcomputer? With our IMAGE DBMS, you've got a powerful tool for simple and efficient data management. And you can easily picture the possibilities offered by our GRAPHICS/1000 software. Like our other software packages, these are all upwardly compatible throughout the entire HP 1000 line, giving you an easy growth path to even higher performance.

Configure it out for yourself.

The Model 5 is completely modular, so you can virtually design a system yourself. Hard disks and other peripherals can be plugged in directly. And thanks to a 60% reduction in memory costs, you can go all the way to 1/2 megabyte of memory for an additional $2000.

Whether you buy a packaged system, or put one together yourself, you can get HP's full range of customer support services, provided from more than 170 offices worldwide.

The ins and outs of high-speed I/O.

In designing the Model 5, we used an advanced distributed intelligence architecture that puts a separate LSI I/O processor on each interface board. This means each processor has its own direct channel to the entire 1/2-megabyte memory. (We used state-of-the-art 64K RAMs to put the 512K bytes of memory onto just one board.) With the CPU free to concentrate on computation, you get significantly increased throughput and exceptional performance.

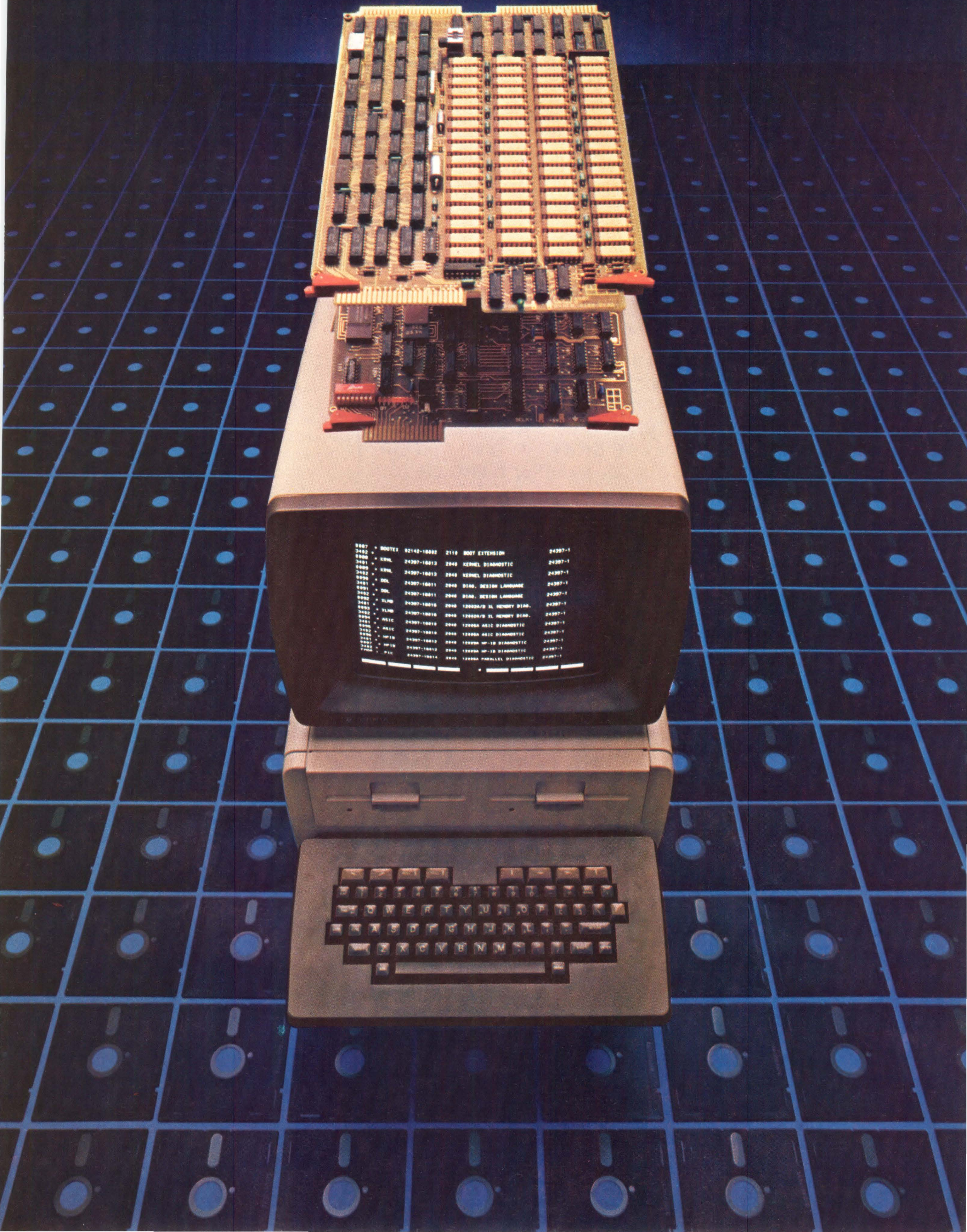
If you'd like a hands-on demonstration, just contact your local HP sales office listed in the White Pages. Or for more information, and our new OEM catalog, write to Joe Schoendorf, Hewlett-Packard, Dept. 12107, 11000 Wolfe Road, Cupertino, CA 95014.

HEWLETT PACKARD

Prices U.S.A. OEM quantities of 100 units. Prices subject to change without notice.

CIRCLE 40 ON INQUIRY CARD

22102
HPDS70



```
0087  * BOOTEX
3402 *        02142-16002  2110  BOOT EXTENSION              24397-1
0088  * KRNL
3401 *        24397-16013  2040  KERNEL DIAGNOSTIC           24397-1
0089  * KRNL
3402 *        24397-16013  2040  KERNEL DIAGNOSTIC           24397-1
0090  * DDL
3401 *        24397-16011  2040  DIAG. DESIGN LANGUAGE       24397-1
0091  * DDL
3402 *        24397-16011  2040  DIAG. DESIGN LANGUAGE       24397-1
0092  * XLMD
3401 *        24397-16016  2040  12002A/B XL MEMORY DIAG.    24397-1
0093  * XLMD
3402 *        24397-16016  2040  12002A/B XL MEMORY DIAG.    24397-1
0094  * ASIC
3401 *        24397-16010  2040  12005A ASIC DIAGNOSTIC      24397-1
0095  * ASIC
3402 *        24397-16010  2040  12005A ASIC DIAGNOSTIC      24397-1
0096  * HPIB
3401 *        24397-16012  2040  12009A HP-IB DIAGNOSTIC     24397-1
0097  * HPIB
3402 *        24397-16012  2040  12009A HP-IB DIAGNOSTIC     24397-1
       * PIC   24397-16014  2040  12006A PARALLEL DIAGNOSTIC  24397-1
```

Voice output terminal offers high quality speech at low bit rates

Machine speech is brought into the realm of the general purpose computer by a voice output terminal that provides high quality digital speech and unlimited vocabulary at low bit rates. Introduced by Centigram Corp, 155A Moffett Park Dr, Suite 108, Sunnyvale, CA 94086, LISA (logically integrated speech annunciator) uses digital speech processing at a rate of 4800 bits/s to reduce the cost of storage and transmission lines. Unlike the speech produced using other low bit rate methods, the output is almost indistinguishable from voice that has been recorded by conventional analog methods.

The unit can be used with any type of computer via an RS-232 interface in standalone mode. An additional RS-232 interface allows it to be interposed between computer and CRT with no CRT disruption. Vocabulary is stored on discs loaded into the host computer, giving the vocabulary virtually no limits (1M byte of disc storage equals 1 hour of speech). The vocabulary can be output in any form desired: single words, phrases, sentences, or lengthy statements. In contrast to the machinelike, choppy phrasing of many technologies, the pitch, tone, and cadence are natural; three out of four people will not realize they are listening to synthesized speech.

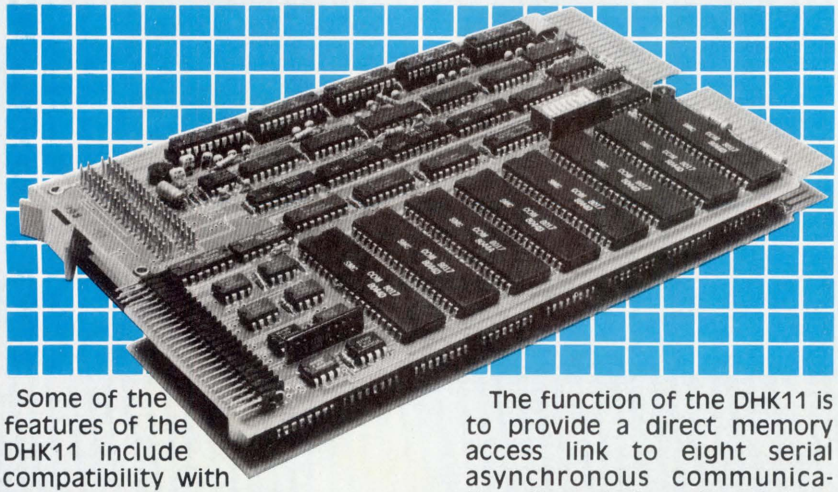
Vocabulary for the terminal is processed using the voice library generator. This unit is based on a digital voice technology called parametric waveform coding (PWC). Developed by the company, this technique derives from two earlier digital voice technologies: parametric methods like linear predictive coding and waveform analysis.

Using PWC, the original speech waveform is broken up into events. An event is the waveform that results from one opening and closing of the vocal cord, and has a duration in the range of 2 to 15 ms, depending on the pitch of the speaker. Each event is modeled by a complex parametric mathematical description. Approximately two dozen parameters are involved in this description; these numbers themselves represent a digital description of the voice waveform, and can accurately reconstruct the waveform.

A mathematical model called the autoregressive moving average is used to generate parameters for digitizing voice. When voice is input, the voice library generator uses PWC to generate parameters. The digital code is then converted back to an analog waveform, and waveform analysis is used to compare the synthesized waveform with the original. If they don't match, the generator continues to correct and compare until they do match. Result of the analysis is then stored on disc in the form of ASCII character test strings.

The resulting vocabulary disc is loaded into the user's computer system where the annunciator terminal can access it. Since digitized voice is made up of standard text characters, the computer can manipulate and transmit the bit stream without modification to the operating system. The unit also contains the autoregressive moving average model, which converts the digitized codes back into an analog waveform that drives a speaker.

Circle 356 on Inquiry Card



High Density Power I/O

Opto 22 Quad Pak™ Cuts System Cost

Opto 22 proudly announces a new generation of power I/O modules. Twenty four high power I/O inputs and/or outputs in a mounting rack that is only eight inches long, saves expensive cabinets, floor space and wiring. Four photo-isolated outputs or inputs in a one inch wide module with all the features and reliability of the industry standard I/O module that we introduced in 1977. In stock for immediate delivery. Isn't this what you expect from Opto 22?

Opto 22 Solid State of the Art

DISTRIBUTED BY:

Hamilton/Avnet
throughout the U.S. and Canada

CALIFORNIA	
VSI Electronics	714-557-7131
VSI Electronics	408-734-5470
FLORIDA	
Power Components	305-565-1614
ILLINOIS	
GBL Goold Electronics	312-593-3220
MICHIGAN	
George Instruments	313-280-1111
MINNESOTA	
Cassidy Electronics	612-835-7746
NEW YORK	
LIVERA-Polk Associates	516-484-1276
OHIO	
IPD, Inc.	513-435-2086
OKLAHOMA	
Quality Components	918-664-8812
TEXAS	
Quality Components	214-387-4949
Quality Components	713-772-7100
Quality Components	512-835-0220
WASHINGTON	
Shannon, Ltd.	206-763-0545
WISCONSIN	
Taylor Electric	414-241-4321
CANADA	
Intek Electronics	604-324-6831
Intek Electronics	403-437-2755
Multilek	613-226-2365

Opto 22
Huntington Beach, CA 92649
714-891-5876

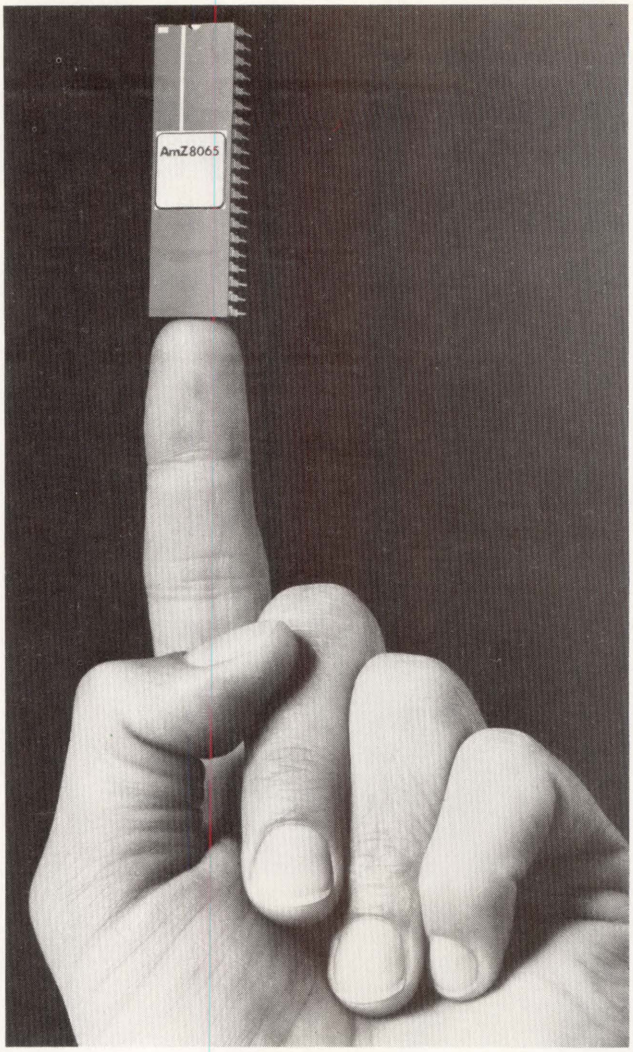
CIRCLE 42 ON INQUIRY CARD

Only the AmZ8000* family has a one-chip error detection and correction unit.

It's the AmZ8065. Remember the name, it's going to save you a whole lot of time, money and board space.

The AmZ8065 lets you say goodbye to 50-70 MSI devices. That's right, 50-70! And it's perfect for high volume applications with both hard and floppy disks.

It's so flexible it manipulates all the math necessary for burst serial-bit error detection and correction in real time. And the AmZ8065 corrects with all the



*Z8000 is a trademark of Zilog, Inc.

THE FIND IT/ FIX IT MACHINE.

commonly used 32, 35, 48 and 56-bit Fire Codes.

The AmZ8065 is just one more reason the AmZ8000 should be the power behind your system.

Here's some more:

We've got universal interrupt controllers, a data ciphering processor, timers, arithmetic processors, direct memory access controllers, and a bunch of bipolar peripherals for the AmZ8000 on the shelf and ready to go.

And AMD is the only IC company that guarantees quality. Everything we make meets or exceeds INT•STD•123, the International Standard of Quality.

The International Standard of Quality guarantees these electrical AQLs on all parameters over the operating temperature range: 0.1% on MOS RAMs & ROMs; 0.2% on Bipolar Logic & Interface; 0.3% on Linear, LSI Logic & other memories.

INT•STD•123

The AmZ8000 has it all: the architecture, the peripherals, the software, a development system, and customer education programs.

Whatever your problem, AMD can fix it.

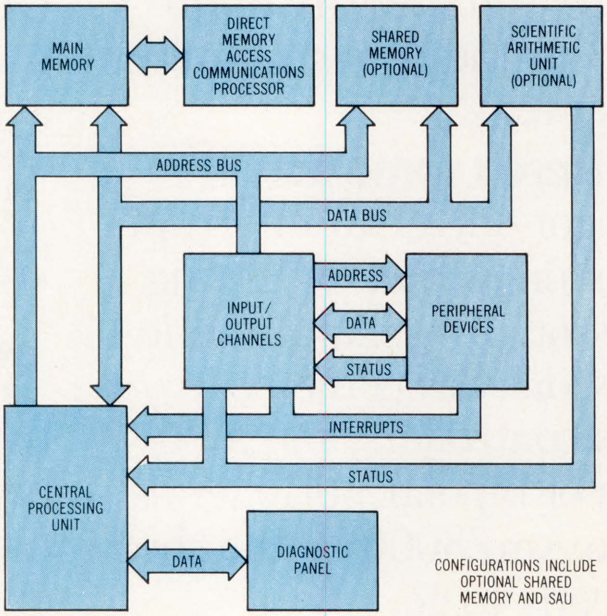
Advanced Micro Devices

901 Thompson Place, Sunnyvale, CA 94086 · (408) 732-2400

CIRCLE 43 ON INQUIRY CARD

48-bit supermini outperforms 32-bit machines at competitive price

The 48-bit model 300 superminicomputer offers benchmark performance in multiprogramming environments through its fast central system bus. Other attributes of the machine, developed by Harris Corp, Computer Systems Div, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309, include a hardware supported 12M-byte virtual memory system and 2M-byte real memory.



CONFIGURATIONS INCLUDE OPTIONAL SHARED MEMORY AND SAU

Central system bus in Harris's 48-bit superminicomputer provides high throughput in multiprogramming environments. Bus uses 48 lines for data transfer and 20 lines for addressing, allowing entire 1.9M-byte memory to be accessed

Supporting concurrent users doing interactive program development, timesharing, multistream batch, multiple remote job entry, and realtime processing, the system design centers on a very fast system bus that has 48 lines for data transfers and 20 lines for addressing. Address bits allow the full 1.96M bytes of main memory to be accessed by any subsystem using the bus. During writes to main memory, the bus transfers the memory address together with 24 or 48 data bits in one bus cycle. Typically, I/O operations transfer 48 data bits at one time between main memory and discs or tapes on the universal block channel via the system bus.

The central processor overlaps instruction fetch with execution. While one instruction is being executed, the next sequential instruction is fetched from main memory. The instruction set is compatible with the company's other computer systems.

System memory consists of high performance MOS RAM managed by demand paging hardware and software, and monitored by error correcting logic. Transfers between the main memory and the processors take place over the system bus. Main memory of the system is expandable to nearly 2M bytes. Each memory module reads or writes 48 bits plus error correcting bits in one memory cycle. Each module transfers 48 bits on the system bus to the CPU and selected I/O channels. Virtual memory makes over 12M bytes of logical address space available for running application programs regardless of the physical memory available.

The system supports up to 24 logical block mode I/O channels. The universal block channel is intended for use by high performance peripheral controllers; the integral block channel interfaces to a card reader. The programmed I/O channel interfaces to slow speed devices. It supports up to four plug-in controllers for printers and terminals. The buffered block channel interfaces disc and tape controllers to the system. Its dual-bus priority and 96-byte in-channel buffer improve transfer rate.

An optional hardware floating point processor, the scientific arithmetic unit (SAU), provides concurrent floating point operations independent of the CPU. The SAU interface transfers 48 bits to or from main memory on the system bus. Double-precision (48-bit) floating point employs an 8-bit signed exponent and 39-bit signed mantissa to achieve more than 11 decimal points of precision.

The VULCAN virtual memory management operating system is supported by a variety of registers to decrease the burden of housekeeping requirements. In addition to the VULCAN operating system, the system supports nine computer languages, five support programs, a programmable job control language, various remote job entry packages, and data management systems and utilities.

Circle 357 on Inquiry Card

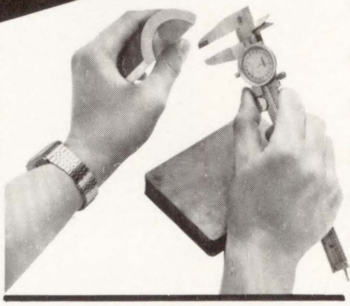
1200-line/min band printer switches to 600 lines/min for draft quality output

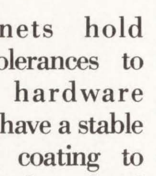
Model 3121, a high performance 1200-line/min band printer, is priced as much as 40% below competitive band or drum models. In the unit, Data Printer Corp, 99 Middlesex St, Malden, MA 02148, has provided an optional switch selectable speed feature that allows the printer to produce draft-quality word processing output at 600 lines/min.

The 132-column unit also incorporates features that make it easy to use and flexible. For example, in standard configuration, it includes more than 40 digital display symbols, a low cost spool ribbon system that lowers ribbon replacement costs over other methods by as much as 25%, a full line buffer, noise level under 65 dBA, operator interchangeable 48-, 64-, 94-, and 128-char bands with a rated life of 100M impacts/char, a gravity activated paper stacking system, fine vertical and horizontal paper adjustment features, and exceptional quality print definition.

(continued on page 70)


benson
Computer Graphics Hardcopy
for Every Application . . .
Worldwide





Optionally, it may be configured to provide 136-col printing, a cassette ribbon and ribbon re-inking system, a forms length selector switch or direct access vertical format unit (VFU), an 8- or 12-channel electronic vertical format unit tape reader, 6/8-lines/in (2.3/3.1/cm) direct access vertical line spacing, font options, a rear control panel, an elapsed time indicator, and a digital line counter.

Achieving a top print speed of 1350 lines/min with a 48-char font and 1200 lines/min with a 64-char set, the printer uses electromagnetically actuated print hammers. Hammers impact from behind, pushing a small area of the form against a ribbon and a raised typeface on the band. Printing is performed by scanning stored data in synchronism with the moving band and actuating the print hammers as the designated characters move into their respective print positions.

The band consists of repeating character sets in an endless loop. Characters are arranged according to high and low character usage to optimize print speed, and are presented in every print position as the motor-driven band laterally revolves at a constant speed in front of the hammers.

The spool to spool ribbon system uses 100 yds (91 m) of 1″ (2.54-cm) wide ribbon on two throwaway spools. The ribbon is expected to provide more than 60M character impacts on 15 lb, single-part paper, assuming a 50% print density on the page and either 132- or 136-col width. Paper stacker is an operator adjustable system that can stack forms ranging from 6 to 12″ (15 to 30 cm) in length. Unit consists of adjustable paper platform, front and rear gates that are adjusted for forms length, paper puller to direct paper into the stacking area, and hanging chain paper deflector to assist in fanfolding the forms.

Interchangeable bands, made of stainless steel alloy, contain 420 etched characters each and are available with repeating 48-, 64-, 94-, and 128-char sets offering throughput of 1350, 1200, 900 and 690 lines/min, respectively. Each band is rated for in excess of 100M impacts/char. The printer accepts from 1- to 6-part forms, multipart bond with a single carbon, and special papers such as envelopes, labels with pressure sensitive backings, and some plastic cards.

Circle 358 on Inquiry Card

16-bit military computers offer software capability, high performance

MSE/14 offers the highest performance/price ratio obtainable for midrange military computers, while the MSE/25 supplies the strongest software capability of any 16-bit military computer on the market. These processors, developed by Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050, are completely compatible with Data General Corp's Eclipse software and meet the stringent operating requirements of MIL-E-5400, MIL-E-16400, and MIL-3-4158.

The MSE/14 complements the powerful 32-bit MSE/800 (see *Computer Design,* May 1981, p 641). Its compact packaging provides a complete processing system in a single ATR chassis (0.87 ft^3 (0.024 m^3). This chassis accommodates eight I/O interfaces and either 128k bytes of core or 512k bytes of semiconductor memory. Nonvolatile core system performance is rated at 400k operations/s; 4-way interleaved semiconductor memory system performance exceeds 800k operations/s. Use of an optional expansion chassis supports core memory growth to 2048k bytes and additional I/O capability.

Configuration flexibility allows users to select the most cost effective solution to the performance needs of their application. Floating point capability is available in either firmware or hardware implementations.

MSE/25 achieves high performance with cache memory that exceeds 600k operations/s for a fixed point measure and 300k Whetstone operations/s as a single-precision floating point measure. The minimum system is packaged in a single ATR chassis and includes either 64k or 128k bytes of core memory. Main memory, which includes a parity checking capability, can be expanded to 2M bytes.

Microprogrammed architecture of the processor includes a versatile instruction set, hardware stack operations, fast vectored interrupt handling that maximizes data handling capability, and BITE (Built-In Test Equipment) for improved maintainability. Users can expand processing capability by selecting an extended arithmetic processor, memory allocation and protection, high speed cache memory, writable control store, and a commercial instruction set.

Circle 359 on Inquiry Card

Silent partner.

In the business world of today, just about everybody could use a silent partner. After all, they give your operation a real shot in the arm and hardly ever make a sound.

Now Lear Siegler can fill the bill. Because our 310 Ballistic™ Printer is one silent partner that knows when to HUSH up.

The 310 is the quietest dot-matrix printer in its class. In fact, the 310 Ballistic Printer with HUSH checks in at a soothing 56 dBA. That's quieter than most typewriters. And when you stop to think of the accumulated noise beating on your eardrums all day, the 310 emerges as a valued colleague indeed.

And what price do you have to pay for such an asset? Only $2170. (Quantity 1).

As if that weren't enough, the 310 also features an expandable print buffer with up to 2048 characters. It gives you complete horizontal and vertical forms control. And it's compatible with all LSI terminals.

Other outstanding features include the 310's printing characteristics. And a 9 high by 7 wide dot-matrix provides true underlining and lower case descenders.

In addition, the sophisticated 310 is multilingual. Because character sets are available in a variety of languages. At 180 cps, the 310 Ballistic Printer with HUSH gives you high throughput. It's rugged and durable but stylish in design and fits right into any office decor.

The 310 Ballistic Printer with HUSH is a real business secret. Why not make one your silent partner today and see what a difference it makes.

LEAR SIEGLER 310 BALLISTIC PRINTER WITH HUSH.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

Lear Siegler, Inc. Data Products Division, 714 North Brookhurst Street, Anaheim, CA 92803 800/854-3805. In California 714/774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: San Francisco 408/263-0506 • Los Angeles 213/454-9941 • Chicago 312/279-5250 • Houston 713/780-2585 • Philadelphia 215/245-1520 • New York 212/594-6762 • Boston 617/423-1510 • Washington, D.C. 301/459-1826 • Orlando 305/869-1826 • England (04867) 80666.

Ballistic™ Printer is a trademark of Lear Siegler, Inc.

CIRCLE 46 ON INQUIRY CARD


JAPAN 0G1
HM6116LP-3
JAPAN 0H1
HM6116P-3

IN STOCK NOW!

New 2K x 8 Static CMOS RAM...

The HM 6116 From HITACHI!!!

Pin Compatible With Byte-Wide Industry Standard EPROMS

The Hitachi HM6116 CMOS RAM is Available Now for Immediate Delivery! Now that you're ready to design your next system, why not use the best: the Hitachi HM6116 2K x 8 static RAM. The HM6116 incorporates Hitachi "HI-CMOS" technology and a cost-effective plastic package that bring you the best of three technologies: **HMOS** speed; **NMOS** high-bit densities; and **CMOS** low power dissipation. Like all Hitachi "HI-CMOS" RAMs, the HM6116 lets you enjoy state-of-the-art performance at competitive prices. In addition, the HM6116 2K x 8 has an address access time of 120ns; its low power dissipation during operation is 180mW, and a mere 100μW, during complete standby (compare this to the typical 700mW required by ordinary 16K NMOS cerdip RAMs). And, the HM6116 has another big plus: it's ready now for immediate delivery!

For more information about the Hitachi HM6116 CMOS RAM, return coupon or call your local Hitachi Representative or distributor sales office.

HITACHI

Hitachi America, Ltd., Electronic Devices Sales and Service Division
1800 Bering Drive, San Jose, CA 95112 (408) 292-6404

Symbol of Semiconductor Quality, Worldwide

Regional Headquarters

Western
1800 Bering Drive
San Jose, CA 95112
(408) 292-6404
TWX 910-338-2103

Central
6200 Savoy Drive, Suite 704
Houston, TX 77036
(713) 974-0534
TWX 910-881-7043

Eastern
594 Marrett Road, Suite 22
Lexington, MA 02173
(617) 861-1642
TWX 710-326-1413

Stocking Distributors

Active Component Technology • Anthem • Bell • CAM/RPC • Diplomat • Future • Jaco • Marshall • Milgray • RC Components • Resco • RM Electronics • Sterling • Time • Western Micro Technology

Yes, I want to know more about the Hitachi HM6116 CMOS RAM.

☐ Send detailed product literature.
☐ Have my Hitachi Representative call.

Name ______________________________

Title ______________________________

Company ______________________________

Address ______________________________

City ______________________________

State ______________________ Zip ________

Phone (   ) ______________________________

Send to: Hitachi America, Ltd.
1800 Bering Drive, San Jose, CA 95112

CD681-280

Low end minicomputer and operating system added to DS990 family

A low cost multiuser COBOL system, DS990 model 3 uses the multitasking DX7 operating system to provide high performance in the diskette/cartridge disc environment. Developed by Texas Instruments Inc, PO Box 202146 H-573, Dallas, TX 75220, the operating system provides comprehensive management capabilities for programs, memory, and files; an interactive user interface; and upward compatibility with the DX10 Operating System.

Incorporating a 990/10 central processor with 96k bytes of error-correcting memory, model 911 video display terminal, and a dual terminal controller in its standard configuration, the minicomputer offers mass storage in either of two forms: dual double-sided, double-density diskettes at 1.15M bytes each, or cartridge disc with 4.7M bytes of removable storage and 4.7M bytes of fixed storage. System configurations using cartridge disc are equipped with a tabletop cabinet that houses a 6-slot chassis and the CPU. Systems using diskette storage can be equipped with the tabletop cabinet or with a 30″ (76-cm) pedestal unit that provides a 13-slot chassis. Tabletop configurations requiring additional memory, three or four workstations, or a second printer can be upgraded with a chassis expansion and the addition of a pedestal cabinet.

The DX7 operating system provides COBOL program development and execution, Sort/Merge, IBM 3780/2780 communications emulation, and system generation capabilities. Operator's interface to the operating system is the System Command Interpreter (SCI). Resource management capabilities include roll-in, roll-out, dynamic memory allocation of overlays, and priority scheduling, plus procedure- and replicated-task sharing. The file management package includes sequential, relative-record, and multikey-indexed files; it provides delete and write protect, record locking, blocked files, deferred or immediate-write operation, temporary files, and blank compression. Multikey indexing, with self-maintenance capability, eliminates much of the necessity for periodic file rebuilding and reorganization. In a memory environment of 96k bytes, DX7 provides a minimum of 30k bytes of user memory space.

Circle 360 on Inquiry Card

Large scale computers handle online processing in multi-user environment

Four large scale host computers expand the growth path for current users of CP-V and CP-6 operating systems and provide an efficient operating system specifically designed for high production multi-user environment. Accommodating up to 120 simultaneous users, the DPS 8/62C, the DPS 8/44C in single- and dual-processor configurations, and the DPS 8/20C, announced by Honeywell, Inc, PO Box 6000, Phoenix, AZ 85005, serve as hosts for the Central Program 6 (CP-6) operating system. Online processing capabilities of the package include concurrent combinations of interactive timesharing transaction processing, while simultaneously accommodating multiprogrammed local and remote batch processing. The software library of the system consists of reentrant language processors that include COBOL 74, ANS FORTRAN, APL, Text, and BASIC, and the IDS-II database systems.

DPS 8/62C is a 120-user, single-processor system based on DPS 8/70C technology. It offers approximately 30% more power than a comparably configured Level 66/DPS-C system. The freestanding central system consists of CPU, system control unit (SCU), and an input/output multiplexer (IOM) with 35-channel function slots, expandable to 54 slots. In a typical configuration containing Datanet 8C (DN8C) frontend network processor (FNP), with 120 communications lines, 1200- and 1600-line/min printers, 1050-card/min card reader, four 200-in/s tape drives, and two 200M and two 1.2G disc drives, the system will sell for $1,681,287.

The single-processor DPS 8/44C is a 40-user, midrange system that offers approximately 75% of the power of a Level 66/DPS/B and about 50% more than the DPS 8/20C. In a dual-processor version, the DPS 8/44C will have up to 76% more power than its single-processor configuration, and will accommodate 80 users. The central system of this machine consists of one or two CPUs, one SCU, and one IOM with 19-channel function slots, all within one cabinet. A typical single-processor configuration includes one DN8C FNP with 40 lines, one 1200-line/min printer, one 500-card/min card reader, two 200-in/s tape drives, and 1.2G disc drive. The central system is field upgradable to a dual-processor system. In the dual-processor configuration, a typical unit consists of DN8C FNP with 80 lines, a 1600-line/min printer, a 500-card/min reader, three 200-in/s tape drives, and one 200M and one 1.2G disc unit. Purchase price of this dual processor system is $1,003,038.

A 20-user system, the DPS 8/20C is based on the technology of the DPS 8/44C and is field upgradable to it. Designed for use either as an entry level freestanding CP-6 system or as a remote satellite in conjunction with larger host systems, it is similar to the DPS 8/44C in system design, packaging, and memory options. In a typical configuration, it includes a DN8C FNP with 20 lines, a 1200-line/min printer, a 500-card/min reader, a 200-in/s tape drive, and two 200M disc units.

Central systems of all units include user storage, integrated communications processor based on Datanet 8 hardware, remote diagnostic processor, cache memory, and operator console. The hosts will use the company's large systems unit record, disc, and tape peripheral subsystems. ☐

Circle 361 on Inquiry Card

POWER-ONE D.C. POWER SUPPLIES

Our customers select their favorite models

The choice wasn't easy. Not with 105 open frame linears and a full switcher line to choose from. Still, the top models of the past year — proudly pictured below — have been named.

Actually, this is a statement of Power-One's most popular D.C. power supplies — as determined by our customers. Obviously, applications vary widely, from small floppies and micro-computers to large mainframe systems.

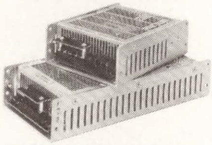
But one thing they all have in common. They're built by Power-One. Which means the most reliable power supplies available, at the lowest cost possible.

So take a look at our entire line. Send for our new 1981 Catalog and Facilities Brochure for details.

Switchers

- Hi-Tech Design
- High Efficiency - 75% min.
- Compact/Light Weight
- 115/230 VAC Input
- 20 msec Hold-up
- Totally Enclosed Packaging
- Two Year Warrantee
- 24 Hour Burn-in

SINGLE OUTPUT

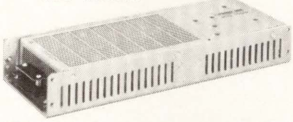


5V to 24V Models

SD, 60W : $115.00
SF, 100W : $170.00
SK, 200W : $250.00

MULTIPLE OUTPUT

150 Watts



5V @ 20A
12V @ 5A
-12V @ 3A
5V to 24V @ 3.5A User Selectable

SHQ-150W : $295.00

QUME PRINTER SUPPLY

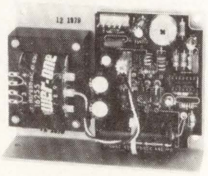
5V @ 10A
± 15V @ 4.5A/16A Peak

SP305 : $345.00

Disk-Drive

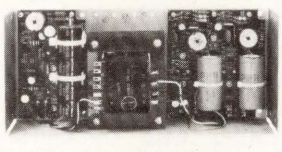
- Powers Most Popular Drives
- 7 "Off the Shelf" Models
- Powers Drives & Controller
- UL & CSA Recognized
- 115/230 VAC Input

5¼″ FLOPPY SUPPLIES



CP340, 1 Drive : $44.95
CP323, Up to 4 Drivers : $74.95

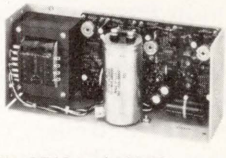
8.0″ FLOPPY SUPPLIES



CP205, 1 Drive : $69.95
CP206, 2 Drives : $91.95
CP162, Up to 4 Drives : $120.00

WINCHESTER SUPPLIES

2 Models to Power any Manufacturer's Drive

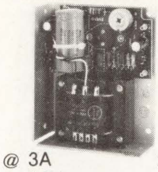


CP379, CP384 : $120.00

Open-Frame Linear

- Industry Standard Packages
- 115/230 VAC Input
- ±.05% Regulation
- Two Year Warrantee
- UL & CSA Recognized
- Industry's Best Power/Cost Ratio

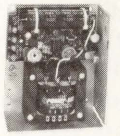
SINGLE OUTPUT



5V @ 3A
12V @ 1.7A
15V @ 1.5A
24V @ 1.2A
28V @ 1.0A
250V @ 0.1A

HB Series : $24.95

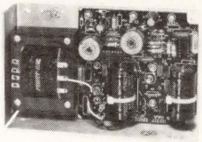
SINGLE OUTPUT



5V @ 6A
12V @ 3.4A
15V @ 3.0A
24V @ 2.4A
28V @ 2.0A
48V @ 1.0A

HC Series : $44.95 to $49.95

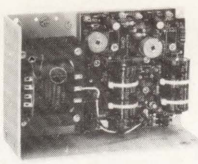
DUAL OUTPUT



± 12V @ 1.0A or
± 15V @ 0.8A

HAA15-0.8 : $39.95

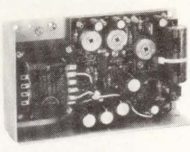
DUAL OUTPUT



± 12V @ 1.7A or
± 15V @ 1.5A

HBB15-1.5 : $49.95

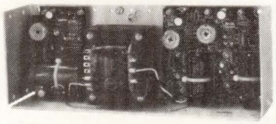
TRIPLE OUTPUT



5V @ 2A
± 9V to ± 15V @ 0.4A

HTAA-16W : $49.95

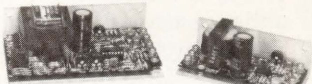
TRIPLE OUTPUT



5V @ 3A
± 12V @ 1A or
± 15V @ 0.8A

HBAA-40W : $69.95

POWER FAIL MONITORS



- Indicates pending system power loss.
- Monitors AC line and DC outputs.
- Allows for orderly data-save procedures

PFM-1 : $24.95 PFM-2 : $39.95

NEW '81 CATALOG & FACILITIES BROCHURE

Get your free copies now!

Phone or write us direct, or circle the reader service number

power-one
D.C. POWER SUPPLIES

Power One Drive • Camarillo, CA 93010 • (805) 484-2806 • (805) 987-3891 • TWX 910-336-1297

CIRCLE 49 ON INQUIRY CARD

Distributed Energy Management System Maximizes User Choices

Often, a company facing an internal requirement in terms of operating its plant or production line will develop, for its own use, a system that eventually becomes a product offered to outside users. An example of such an evolution is found in a turnkey microprocessor based energy and facility management computer system, the DCS 5000, developed by Litton Energy Control Systems (9655 Irondale Ave, Chatsworth, CA 91311) for use in a severe industrial environment. This system utilizes a central supervisory processor communicating with intelligent remote controllers (IRCs) distributed throughout a plant. Readily expandable through modular buildup, it provides as many as 8 communication lines, each capable of addressing up to 128 IRCs.

One user of the system is another division of Litton Industries, Litton Guidance and Control Systems Div, 5500 Canoga Ave, Woodland Hills, CA 91365, where 11 IRCs are employed and another is about to be added. The system extends sensors and actuators to 376 points in a 4-building, 500,000 ft^2 (46,450 m^2) complex. Functions supervised by the system include temperature monitoring, temperature-regulated duty cycling, energizing and de-energizing of systems, and power-demand limiting. Among the equipment under control are air handling units, chillers, boilers, hot water pumps, and cooling towers. Use of the energy control system has reduced the plant's annual power consumption from 2.80 million kWh to 1.75 million kWh—a 37.5% reduction.

This user-programmable system is characterized by its adaptability. The software enables users to extend monitor/control functions to a newly added sensor or piece of equipment in a matter of minutes. Users define the parameters relating to any point in the system through the use of lightpen and keyboard entries, in an interactive process at a display terminal, responding to a series of menus.

System Description

The central supervisory processor (Fig 1) utilizes a single-board microcomputer, the 86/12 from Intel Corp, OMS Div, 5200 NE Elam Young Pkwy, Hillsborough, OR 97123. This industrial board, based on the 16-bit NMOS 8086 microprocessor, is RAM-intensive, containing 64k bytes of random access memory. It also incorporates 24 programmable parallel I/O lines, 9 levels of interrupt, and 2 programmable timer/event counters. An SBC-202 floppy disc controller from the same semiconductor

(continued on page 78)

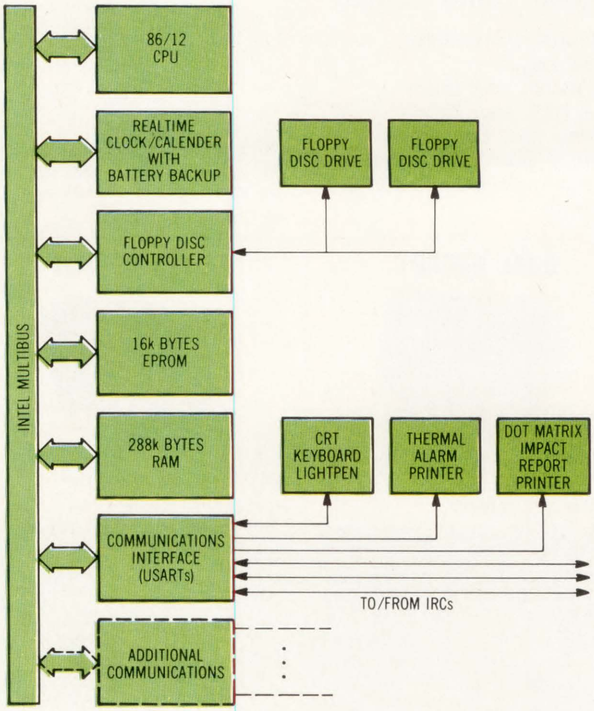
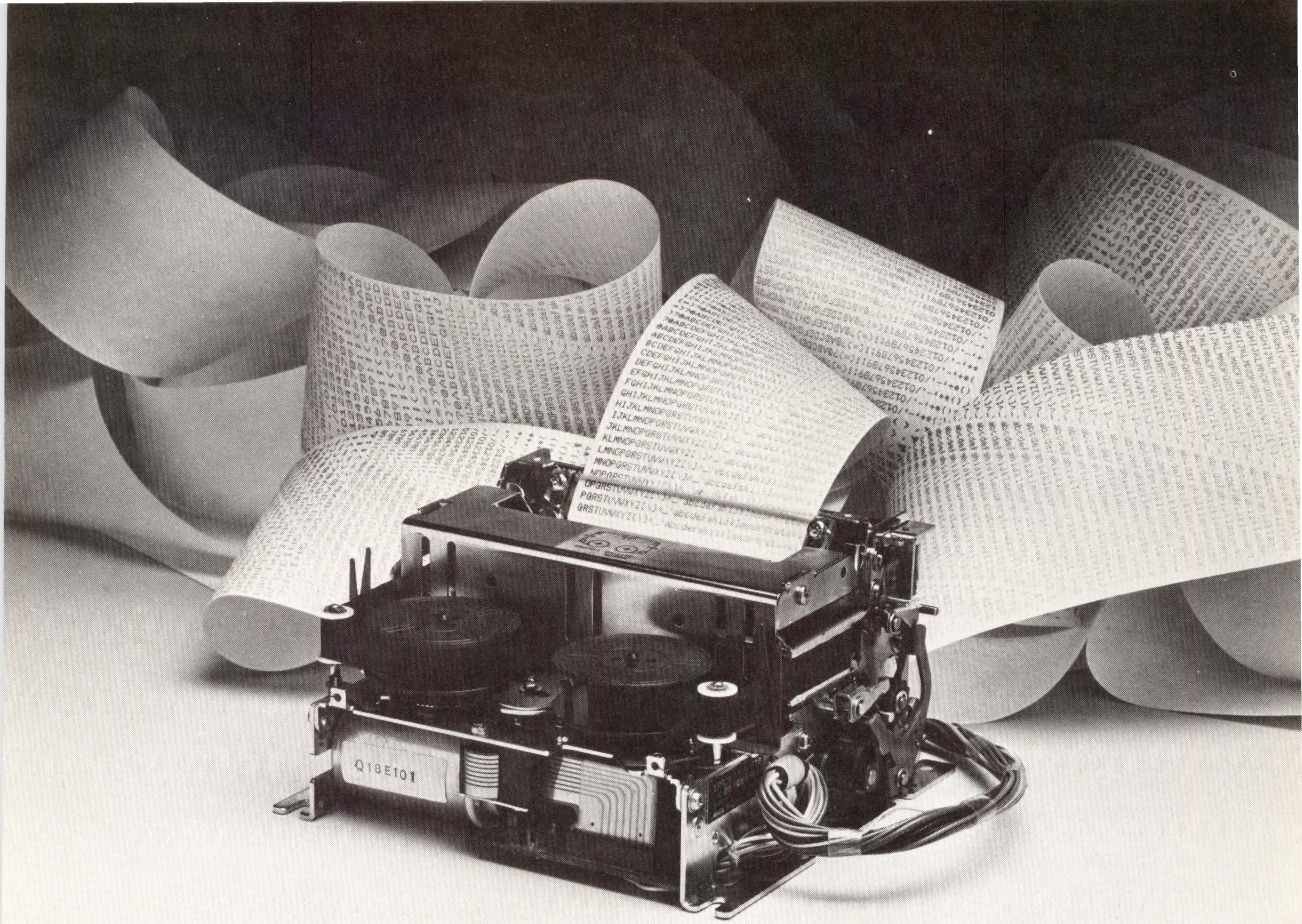


Fig 1 Central supervisory processor. Design of DCS-5000 utilizes RAM-intensive CPU board and additional memory to address distributed network of intelligent remote controllers



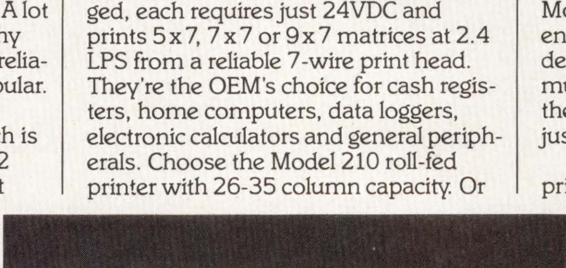
OUTRUNS THE COMPETITION.

The print head on a C. Itoh 500 series dot matrix printer prints out over 100,000,000 characters in its lifetime. That's a lot of cash register receipts. A lot of journal entries. It's one reason why C. Itoh printers are among the most reliable in the industry. And the most popular.

Of course, every series 500 printer is also long on features. Each is bi-directional. Each prints a fast 152 CPS. But best of all, there's one just right for your application. Our Model 512, for example, is the perfect journal printer with 40-column printout for a variety of applications. The Model 522, on the other hand, gives you two-stage 18-column journal/18-column receipt printing complete with logo stamp and automatic paper cutter for cash register applications. For efficient flat bed ticket or slip printing, the Model 542 40-column unit is the one to buy.

C. Itoh Series 200 printers are equally impressive. Compact and rugged, each requires just 24VDC and prints 5x7, 7x7 or 9x7 matrices at 2.4 LPS from a reliable 7-wire print head. They're the OEM's choice for cash registers, home computers, data loggers, electronic calculators and general peripherals. Choose the Model 210 roll-fed printer with 26-35 column capacity. Or the sprocket-fed Model 210S with 22-30 columns. You get 2-color printing either way. For dual-roll applications, the Model 220 records receipt and journal entries and features auto-stamp and independent high-speed line feed. And for multi-ply slip document applications, there's the Model 240 featuring an adjustable document stop gate.

So if you're looking for a little printer with a lasting impression, contact C. Itoh Electronics, Inc., 5301 Beethoven St., Los Angeles, CA 90066; Tel. (213) 306-6700. New York office: 666 Third Ave., New York, NY 10017; Tel. (212) 682-0420.



C. ITOH ELECTRONICS, INC.

One World of Quality

CIRCLE 50 ON INQUIRY CARD

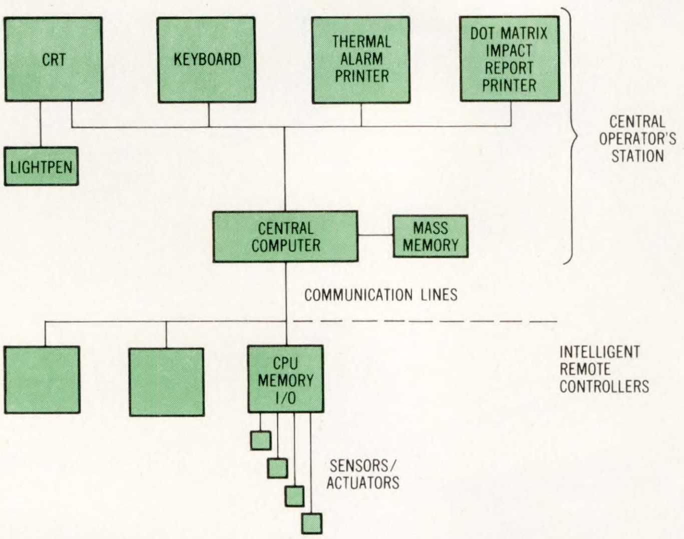


Fig 2 Block diagram shows energy management system. Each of 8 communication lines can address as many as 128 IRCs

manufacturer controls two 8″ single-sided double-density floppy disc drives, model 801 from Shugart Associates, 435 Oakmead Pkwy, Sunnyvale, CA 94086, providing a capacity of 512k bytes each, (out of the 800 available) for storage of applications software, diagnostics, and user operational instructions and data. Also included in the system are 16k bytes of EPROM, 288k bytes of RAM, a realtime clock/calendar with battery backup, and an interface card equipped with USARTs for communications to IRCs and peripheral I/O devices. (See Fig 2.) Control and data signals traveling among all of these elements utilize an Intel MULTIBUS™.

System operation is conducted by means of keyboard and lightpen entries made on a CRT terminal. The terminal is a modified Micro-B1 from Beehive International (4910 Amelia Earhart Dr, Salt Lake City, UT 84116), having an 80-column x 24-line display, and the lightpen is model LP-660-P-LH-AH-R from Information Control Corp (9610 Bellanca St, Los Angeles, CA 90045).

Two printers are in the system. One, an 80-char/s thermal dot matrix printer, the T-80 from Dataproducts, 6200 Canoga Ave, Woodland Hills, CA 91365, operates as an alarm printer, providing automatic printouts of all alarm conditions, with the time and order in which they occur. The other, a 150-char/s dot matrix impact printer, is model 810 from Texas Instruments Inc, PO Box 1444, Houston, TX 77001. This device, an add-on option to the system, operates as a report printer.

Each IRC in the system is a standalone microcomputer, connected to sensors and the central console by simple pairs of twisted wires. Three twisted pairs constitute a communications line, with one pair for remote-to-central, a second for central-to-remote, and a third pair for optional voice communication between personnel at the central console and at remote locations.

An IRC accepts up to five I/O boards, interfacing to an 8-bit bus (Fig 3). These boards can be any mix of three basic types. Digital boards are available with 8 solid state relays for output and 8 optically coupled inputs. An alternative is a digital I/O board with 6 solid state relays, a serial I/O port, a serial channel to a subremote controller, and 8 optically coupled inputs. The third type provides 16 analog inputs with 8-bit analog to digital conversion. Logic within each IRC is provided by a CPU card containing an 8-bit 8085 microprocessor and 32k bytes of EPROM, while a memory card provides 16k bytes of RAM.

Normally, an IRC accommodates two I/O cards, providing 32 control points. However, this number can be increased to 80 control points through the use of an add-on slave expander unit that makes it possible to use a total of five I/O cards. This add-on unit obtains power from the host IRC by drawing on its memory, and has separate power supplies for sensors.

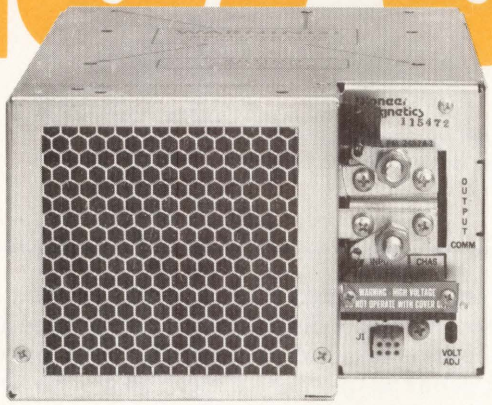
Attached to the IRC by serial communications lines, subremote controllers further extend the localized distributed control concept. One example of a subremote is the control relay panel (CRP), used to control lighting or other contact/closure points, such as turning a bank of motors on or off. Each CRP can handle up to 32 separate loads. Placement of CRPs close to the points being controlled makes it possible to take status readings and make manual overrides on a local as well as a centralized basis.

Although the system is compatible with any standard industrial sensor, the manufacturer has developed a line of instruments expressly for use with this system. This line includes space temperature sensors for room temperature measurment from 32 to 122 °F (0 to 50 °C), equipment temperature sensors covering a 50 to 338 °F (10 to 170 °C), and current/power sensors with power ranges of 0 to 11, 0 to

(continued on page 80)

Dependable Switchers...

1973 1981



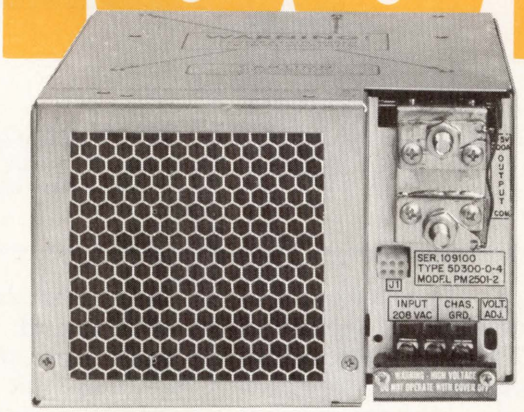
The PM2497
5V@100A/5″x8″x11″

In 1973 Pioneer Magnetics started building a 5VDC @ 100A switching power supply for applications requiring compact and efficient DC power. At the time, commercial switchers were considered state-of-the-art. We solved reliability and delivery problems for our customers that our contemporaries couldn't. As a result, our customers referred to the power supplies as the DEPENDABLES. In fact we're still delivering that same power supply to those same valued customers. We're proud to say that they've depended on us and we've responded by shipping over 100,000 high power switchers. After 8 years our supplies are still out there and running. A continuation of a tradition started in 1958.

STANDARD DC OUTPUT RATINGS.

MODEL	2V	3V	5V	12V	15V	18V	24V	28V	48V	60V	CASE SIZE
PM2496A	100A	60A	50A	30A	25A	22A	16A	13A	8A	6A	5″X8″X11″
PM2497A	200A	100A	100A 120A 150A	60A	50A	45A	33A	27A	16A	12A	5″X8″X11″
PM2500A		200A	200A	85A	70A	60A	45A	40A	24A	19A	5″X8″X11″
PM2498B	400A	300A	200A 300A	120A	100A	90A	66A	54A	32A	25A	5″X16″X11″
PM2501	400A	300A	300A	120A	100A	90A	66A	54A	32A	25A	5″X8″X11″
PM2502	500A	450A	450A	180A	150A	125A	90A	80A	47A	35A	5″X16″X11″

NOTES: 92-138VAC or 184-250VAC single phase, 47 to 63Hz.
DC input available.



The New PM2501
5V@300A/5″x8″x11″

Since 1973, we've been accepting new challenges. Within the same outline as the PM2497, we've developed output ratings of 5V @ 120A, 150A, 200A and now a new 5V @ 300, with full delivered power at 50°C.

The new PM2501 exhibits excellent dynamic response. Proven design concepts enable close control over those parameters that insure reliability. For instance, our unique heat transfer technology results in low component thermal stress, even lower than the PM2497. At three times the power level the PM2501 features an exceptionally high power density package.

Our product line includes switchers that deliver up to 2250 watts in single output and from 375 to 1500 watts in dual through quad output channels. AC or DC input.

Over 100,000 PMI switchers are in the field providing dependable, service free operation. After all, that's why customers have continuously come back to us since 1958.

Pioneer Magnetics

THE SWITCHING POWER SUPPLY PEOPLE SINCE 1958

1745 Berkeley Avenue, Santa Monica, CA 90404 (213) 829-6751

CIRCLE 51 ON INQUIRY CARD

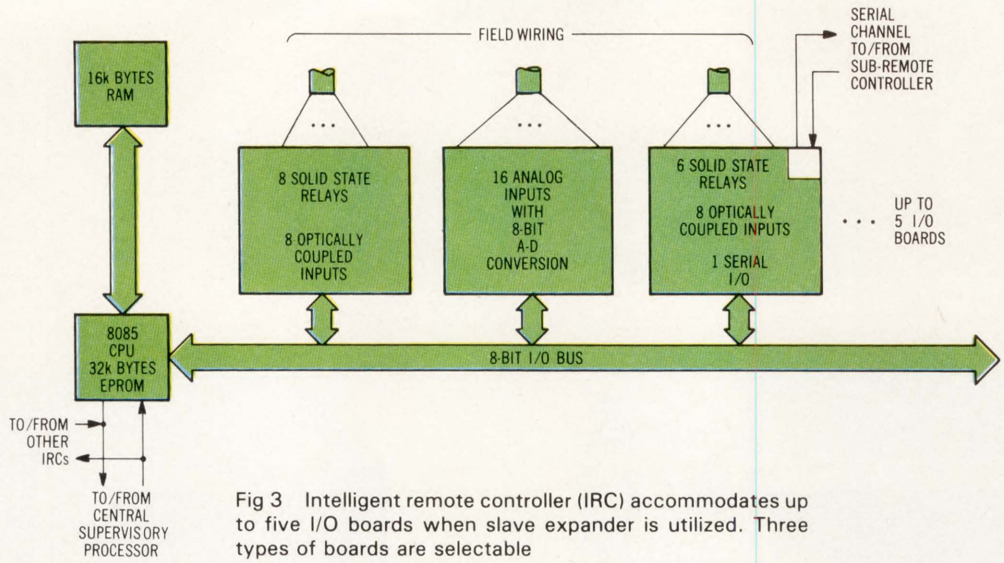


Fig 3 Intelligent remote controller (IRC) accommodates up to five I/O boards when slave expander is utilized. Three types of boards are selectable

22, 0 to 55, and 0 to 110 kW or current range dependent on the external current transformer used.

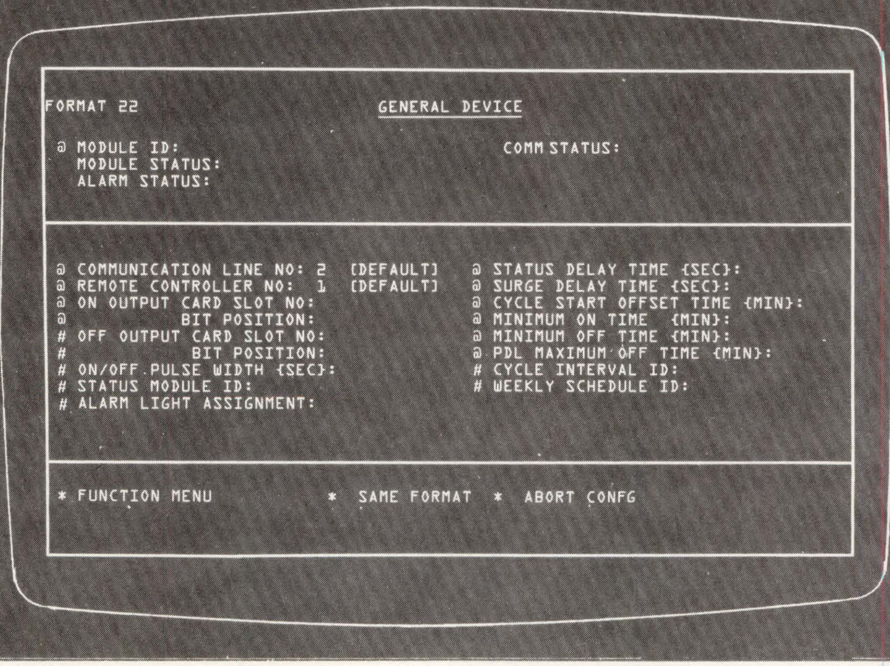
The system exhibits several useful kinds of independence. It continually runs diagnostic self checks. After power failure and restoration, it comes up automatically without manual intervention. Furthermore, all of the IRCs contain their own programs and data, ensuring continued uptime even if cut off from the central supervisor.

System Operation

A functional point is a sensor or control device that is accessed by a twisted pair via a single bit position on an I/O card of an IRC. The term "point" also signifies the set of parameters that define the location of that sensor or control device (in terms of the specific IRC bit-position assigned to it) and the set of parameters that define its operation cycle. The process by which a user establishes the parameters of such a point is referred to as "setting up a point."

Corresponding to any defined point, there is a section of program called a "function module," whose key elements are visible and accessible to the user as a specific CRT display. Blank function modules, with parameters still unspecified, are provided in the system software in a number of general formats, and it is the entry of parameters into such a format that results in the creation of a point.

(continued on page 82)



```
FORMAT 22                         GENERAL DEVICE

 @ MODULE ID:                                        COMM STATUS:
   MODULE STATUS:
   ALARM STATUS:

 @ COMMUNICATION LINE NO: 2  [DEFAULT]   @ STATUS DELAY TIME {SEC}:
 @ REMOTE CONTROLLER NO:  1  [DEFAULT]   @ SURGE DELAY TIME {SEC}:
 @ ON OUTPUT CARD SLOT NO:               @ CYCLE START OFFSET TIME {MIN}:
 @          BIT POSITION:                @ MINIMUM ON TIME  {MIN}:
 # OFF OUTPUT CARD SLOT NO:              @ MINIMUM OFF TIME {MIN}:
 #           BIT POSITION:               @ PDL MAXIMUM OFF TIME {MIN}:
 # ON/OFF PULSE WIDTH {SEC}:             # CYCLE INTERVAL ID:
 # STATUS MODULE ID:                     # WEEKLY SCHEDULE ID:
 # ALARM LIGHT ASSIGNMENT:

 * FUNCTION MENU           *  SAME FORMAT  *  ABORT CONFG
```

Fig 4 Blank function module allows user to assign parameters following colons on display screen. Items preceded by **@** require mandatory parameter entry; those preceded by **#** are optional

New for micro, mini and PC users

The first easy-to-apply A/A signal conditioning system for real world analog inputs.

Our new Series 1800 A/A (analog-to-analog) conditioners offer you a compact, easy-to-apply signal conversion package for front-ending micros, minis and programmable controllers.

Series 1800 conditioners accept low level analog signals such as mv, thermocouple, RTD and process current inputs...and output clean, high level, single-ended signals to any A/D subsystem.


Hundreds of signal conditioning modules to choose from for 28 different analog signal sources. Priced from $150 to $220.

Linearization is standard for RTD inputs, optional for thermocouple inputs. Good system protection, too: RFI immunity, plus 1500v breakdown isolation to eliminate ground loops and to save other system components from signal line noise.

Four card cage models to choose from: 4, 8, or 16-channel with industrial screw terminals, and a 16-channel cage with ribbon connection to any micro.

The 1800 system can be powered by any ± 15 v power supply and operates over a wide (0° to 70°C) ambient temperature range. Wide bandpass options available.

Call your Acromag representative for technical details on this new, low cost, computer-compatible system. Or write for Bulletin 8-180.0.

acromag

Acromag, 30765 Wixom Rd., Wixom, MI 48096, (313) 624-1541. Telex 23/0505.

ACROMAG

CIRCLE 52 ON INQUIRY CARD

Fig 4 provides an example of a specific type of function module designated as "format 22," or "general device." Fig 5 shows this function module after a user has entered parameters next to the colons. In this state, the function module defines a point. Any item of the display that is preceded by @ requires a mandatory parameter entry, whereas entry is optional after an item preceded by #.

The left-hand column of this function module relates to the system location of the configured point. Thus, in Fig 5, we see that this point is accessed via communication line number 1, via IRC number 1, utilizing the 4th bit position on the output card located in slot 0 of that remote controller. In the right-hand column, parameters have been entered that relate to the operation of the device. In most cases, these are numerical entries. However, near the lower right-hand corner of the display are symbolic entries CYC1 and WS1. Each of these is the designation of another type of module, a shared module.

Shared modules are software segments containing standard, often-used information such as weekly schedule and cycling intervals. A shared module is typically referenced by numerous function modules through the use of its code name as a parameter in the function module, and its parameters are automatically assigned to the function module that calls it. The use of shared modules by function modules is analogous to the use of subroutines by different parts of a computer program and, in fact, is implemented in that way in the software.

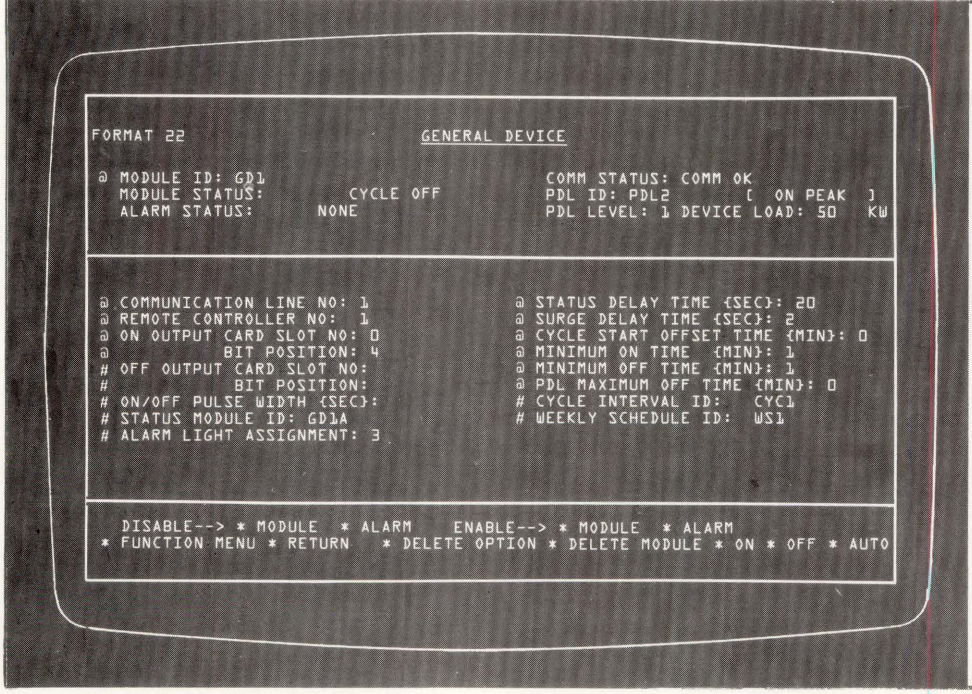
Fig 6 shows the configuration menu, a key program location from which to access various menus, summaries, and modules. Function key "f2" on the terminal keyboard brings up this menu, and then touching the lightpen to one of the asterisks leads the user to the corresponding display. The shared and function module asterisks lead to summaries of existing modules of each of these two types. Similarly, the installation summary asterisk leads to a listing and status of all remote controllers attached to any specified communication line. All remaining items in the configuration menu, with one exception, provide access to specific, frequently used functions.

The exception is the entry designated as "user defined summary configuration." This asterisk leads to a blank format in which the user can summarize any subset of existing function modules. One of the most flexible aspects of the system is that it enables the user to define such summaries, allowing him to organize the modules according to his requirements. Furthermore, the lightpen provides immediate transition from a summary display to any module listed there, as well as transition from individual modules to summaries where they are included.

In addition to all of the displays just discussed, the system provides a variety of menus. A master menu, directly accessible by keyboard function key "f1", lists all summaries that the user has defined to date. Shared module menus and function module menus list the categories of those modules. Using the lightpen, the user can then proceed from a menu to a blank configuration module of a selected category in order to define specific parameters in that format.

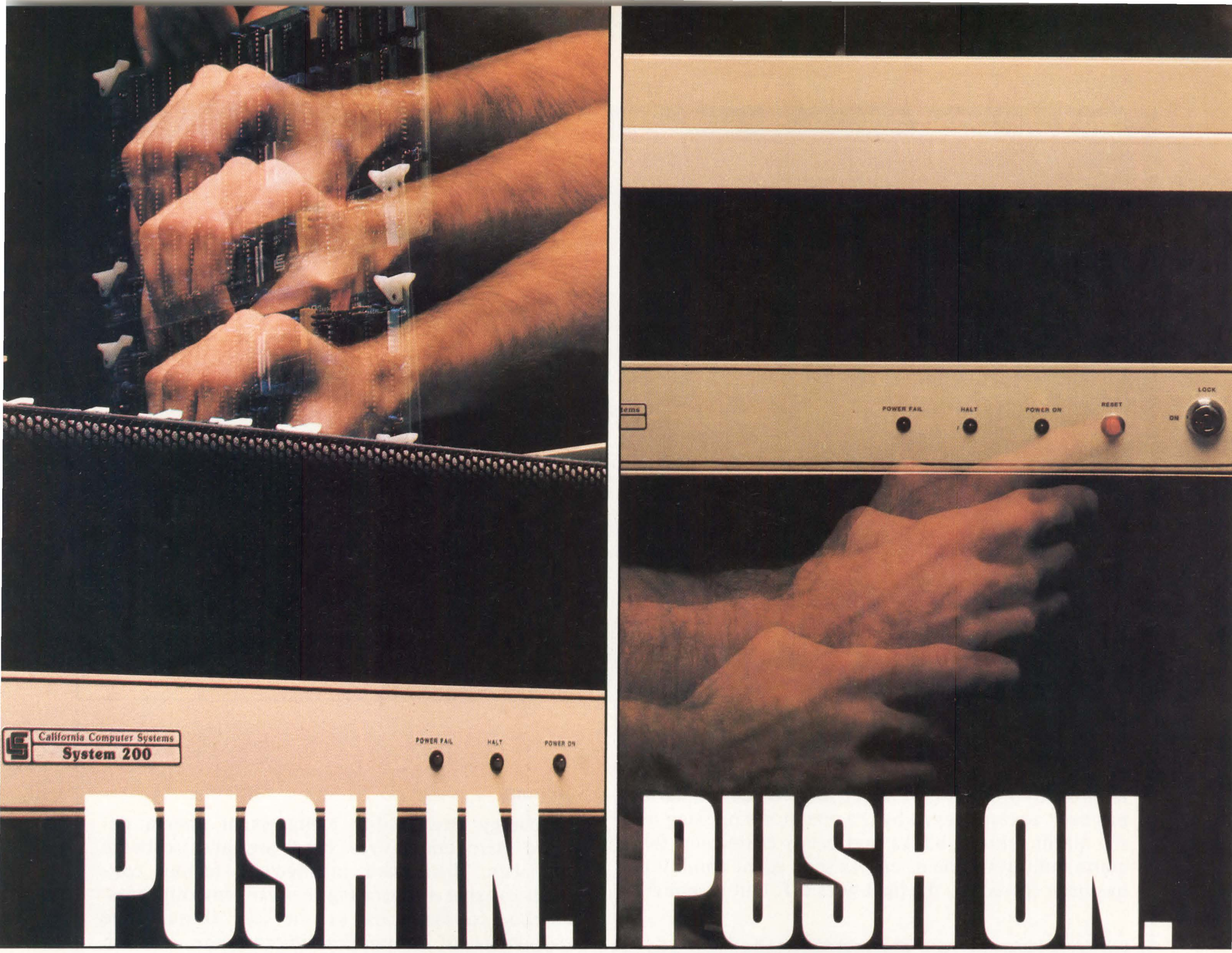
Four levels of alarms can be programmed. An out-of-bounds condition anywhere in the system will activate one of the four back-lighted alarm push buttons to the right of the CRT (Fig 7). This alarm indicator blinks, and an intermittent beep is sounded,

(continued on page 84)



```
FORMAT 22                              GENERAL DEVICE

@ MODULE ID: GD1                                  COMM STATUS: COMM OK
  MODULE STATUS:          CYCLE OFF               PDL ID: PDL2         [  ON PEAK  ]
  ALARM STATUS:         NONE                      PDL LEVEL: 1 DEVICE LOAD: 50    KW

@ COMMUNICATION LINE NO: 1                   @ STATUS DELAY TIME {SEC}: 20
@ REMOTE CONTROLLER NO:  1                   @ SURGE DELAY TIME {SEC}: 2
@ ON OUTPUT CARD SLOT NO: 0                  @ CYCLE START OFFSET TIME {MIN}: 0
@             BIT POSITION: 4                @ MINIMUM ON TIME  {MIN}: 1
# OFF OUTPUT CARD SLOT NO:                   @ MINIMUM OFF TIME {MIN}: 1
#             BIT POSITION:                  @ PDL MAXIMUM OFF TIME {MIN}: 0
# ON/OFF PULSE WIDTH {SEC}:                  # CYCLE INTERVAL ID:   CYC1
# STATUS MODULE ID: GD1A                     # WEEKLY SCHEDULE ID:  WS1
# ALARM LIGHT ASSIGNMENT: 3

  DISABLE--> * MODULE  * ALARM    ENABLE--> * MODULE  * ALARM
* FUNCTION MENU * RETURN   * DELETE OPTION * DELETE MODULE * ON * OFF * AUTO
```

Fig 5 Configured function module, after user has entered parameters. Parameters CYC1 and WS1 indicate shared modules called as subroutines



PUSH IN. PUSH ON.

CCS. MAKING MINIS OUT OF MICROS.

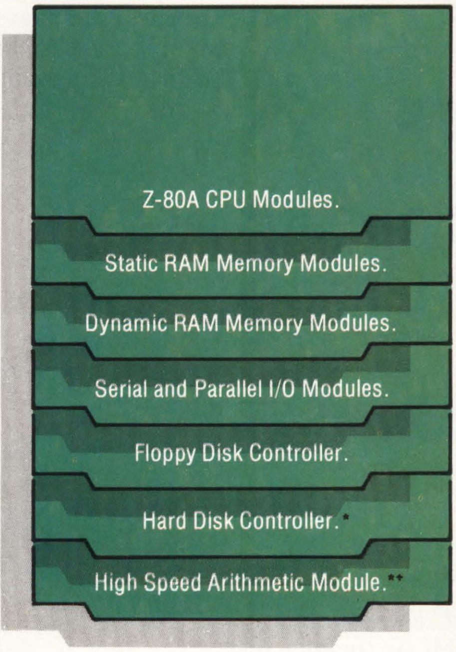
Here's the CCS line of board-level computers for system builders on the move. **Push in** the CCS board. And **push on** with your application. CCS board-level systems go together easily, come up quickly, and run reliably, with a proven return rate of less than 1%.

CCS board-level computers offer systems builders the optimal combination of low development cost, low manufacturing cost, and high reliability from proven, tested modules.

A headstart on reliability. CCS modules are designed to industrial performance standards, manufactured to industrial quality standards, fully burned in and tested. You spend more time and energy on your application when you rely on CCS modules instead of reinventing (and rebuilding) standard computer functions.

A full selection of S-100 board-level computers. Whether you want to add capability to another S-100 based system, or build a system from scratch, chances are you'll find solutions for all your system needs in the CCS product line. CCS manufactures a comprehensive selection, so you can tailor a system to your needs with a minimum of components. You buy exactly what you need. But you can easily expand later.

We'd like to tell you more about the CCS line of board-level computers, OEM systems, and computer systems. There's a lot more to tell. Send in the coupon for more information, contact your local computer dealer, or call.



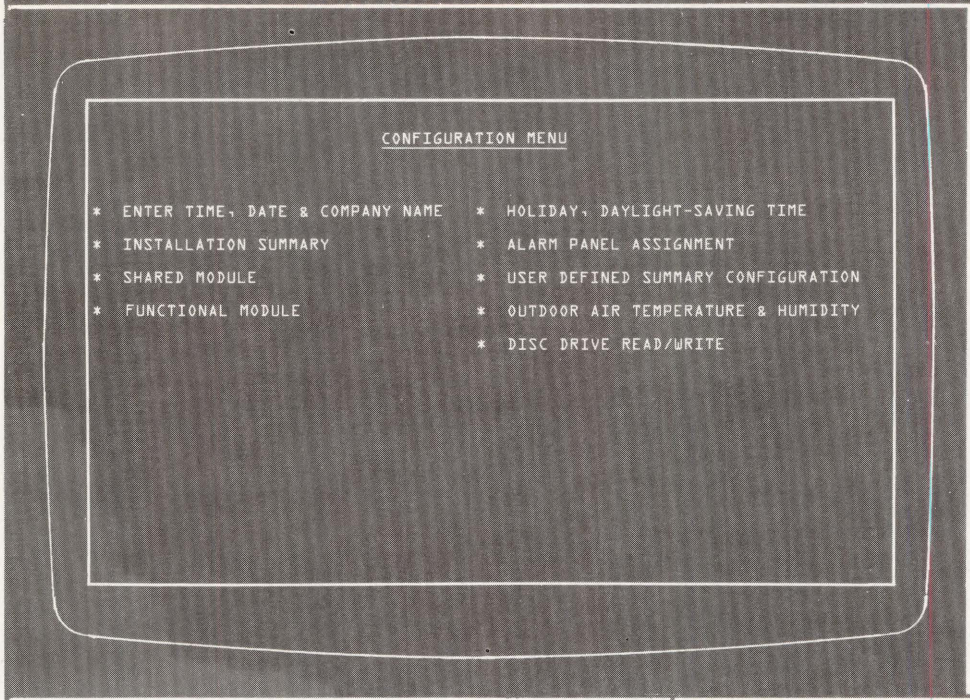
* Available Quarter 2, 1981.
\+ For use with CCS System Models 200, 300, 400.

○ Please have a sales representative call me.
○ Please send more information on CCS Board-Level Computer Modules.

Name ____________
Company ____________
Address ____________
City/State/Zip ____________
Phone (   ) ____________

California Computer Systems
250 Caribbean Drive
Sunnyvale, California 94086
(408) 734-5811

CIRCLE 53 ON INQUIRY CARD



```
                         CONFIGURATION MENU

*  ENTER TIME, DATE & COMPANY NAME   *  HOLIDAY, DAYLIGHT-SAVING TIME
*  INSTALLATION SUMMARY              *  ALARM PANEL ASSIGNMENT
*  SHARED MODULE                     *  USER DEFINED SUMMARY CONFIGURATION
*  FUNCTIONAL MODULE                 *  OUTDOOR AIR TEMPERATURE & HUMIDITY
                                     *  DISC DRIVE READ/WRITE
```

Fig 6 Configuration menu provides useful starting point. From this display, user can employ lightpen to access summaries, blank summary formats, and special functions

in intervals programmed by the user. When the alarm has been acknowledged by the operator's pressing of the alarm button, blinks and beeps cease, and the alarm indicator remains on. As soon as the condition has been corrected, the light goes off. Out-of-bound conditions not assigned priority levels act as "information-only" alarms, do not activate the alarm indicators, and are indicated only on the output of the alarm printer.

Fig 7 System console. Lightpen initiates display changes, function selections, and commands. Button indicators to right provide four levels of alarm

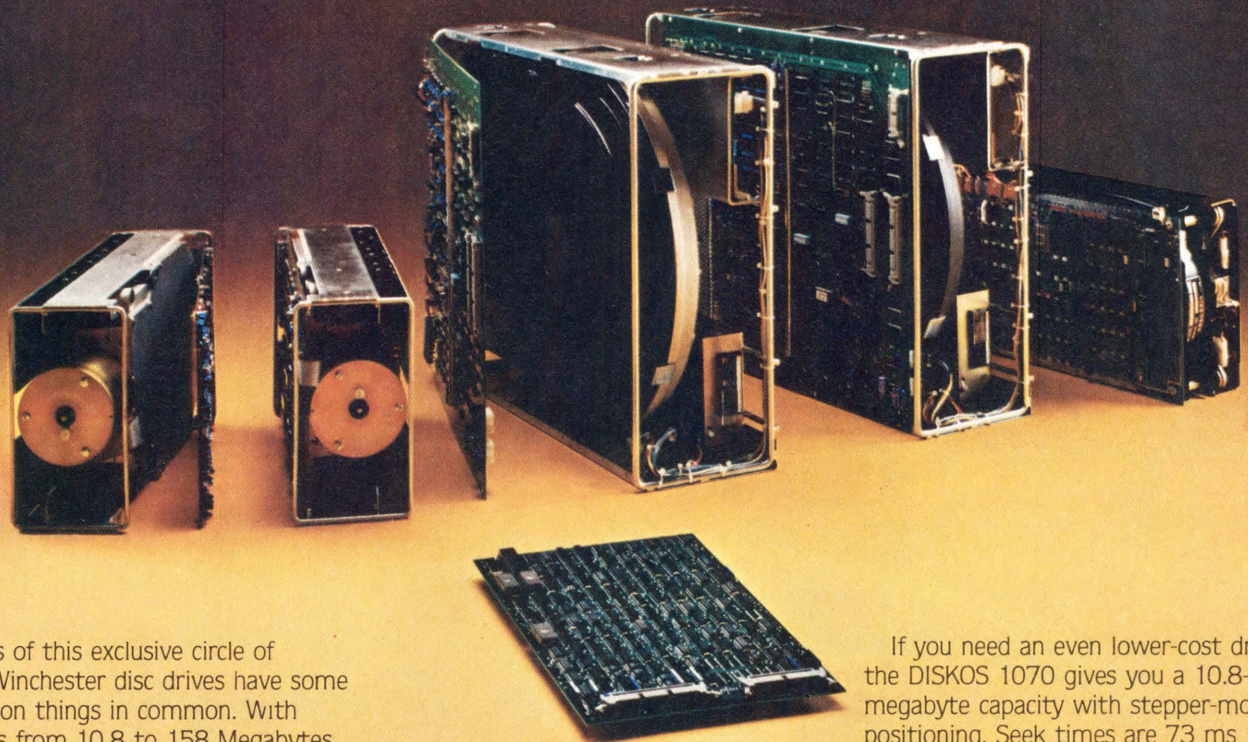
Summary

The energy and facility management system described here emphasizes hardware and software modularity, distributed intelligence, remote controllers capable of operating in severe environments, and easy configuration by the user through the development of summaries indexing the function modules that he creates. In a climate of rising petroleum costs, systems of this kind are likely to play an increasingly important role in industrial societies and may be a determining factor in the ability of such societies to continue industrial growth within existing limits of energy availability.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 710 **Average 711** **Low 712**

THE SMART SET



Members of this exclusive circle of PRIAM Winchester disc drives have some uncommon things in common. With capacities from 10.8 to 158 Megabytes, they have the same interface. And they all connect quickly and easily to microprocessor I/O busses through PRIAM's SMART or SMART-E Interface.

With a simple adapter your system can have the remarkable reliability of Winchester disc drives. And PRIAM's DISKOS drives give you the lowest cost-per-megabyte for your system database.

SMART Gets Smarter!

With its own sophisticated pre-programmed microprocessor, PRIAM's SMART Interface gives you comprehensive disc subsystem functions, including:

Control of any combination of one to four PRIAM Winchester disc drives.

Automatic alternate sector assignment for disc-defect transparency to the host processor.

In addition to all SMART functions, PRIAM's new SMART-E Interface provides ECC, streamlined software, sector interleaving, a 2048-byte buffer, and logical-sector addressing. Both the SMART and SMART-E come to you on a single 8" × 14" printed circuit board that is powered from the drive. And it piggybacks on the drive or mounts separately.

Meet The Elite! PRIAM's High-Capacity, Low-Cost 14-Inch Drives

PRIAM's high-technology 14-inch disc drives have capacities of 34, 68, or 158 megabytes, and they all fit in the same 7" × 17" × 20" package, including optional power supply. Fully servoed linear-voice-coil head positioning is reliable and fast — 45 ms average for the 34 and 68 megabyte drives and 40 ms for the 158 megabyte version. Track to track is 8 ms.

Brushless DC spindle motors in all PRIAM drives assure mechanical simplicity, precise disc speed control, and operation anywhere in the world without change. No relays, mechanical brakes, brushes, belts, or pulleys. Pure, reliable electronic control. Elegantly simple.

The Talk Of The Town: PRIAM Eight-Inch-Disc Drives!

Debut a Winchester disc drive in place of a floppy disc with PRIAM's DISKOS 3450 and 7050, expanding your database to 35 or 70 megabytes. Thoroughbred performance goes with their linear voice-coil positioners; seek times are only 40 ms average and 8 ms track-to-track.

If you need an even lower-cost drive, the DISKOS 1070 gives you a 10.8-megabyte capacity with stepper-motor positioning. Seek times are 73 ms average and 23 ms track-to-track. And they're just as SMART as other PRIAM drives when used with PRIAM's SMART or SMART-E Interface.

More Basic Interface Options!

To those who have their own controller plans, PRIAM offers lower-cost drive-level interfaces. PRIAM's bit-serial NRZ data interface, similar to the evolving ANSI standard, has an 8-bit bidirectional control bus for easy connection to popular 8 and 16-bit microprocessors. Data separation is included in all PRIAM drives.

And if you have a Storage Module controller, you can use it and your software with PRIAM's SMD Interface to update your system with Winchester drives quickly and inexpensively.

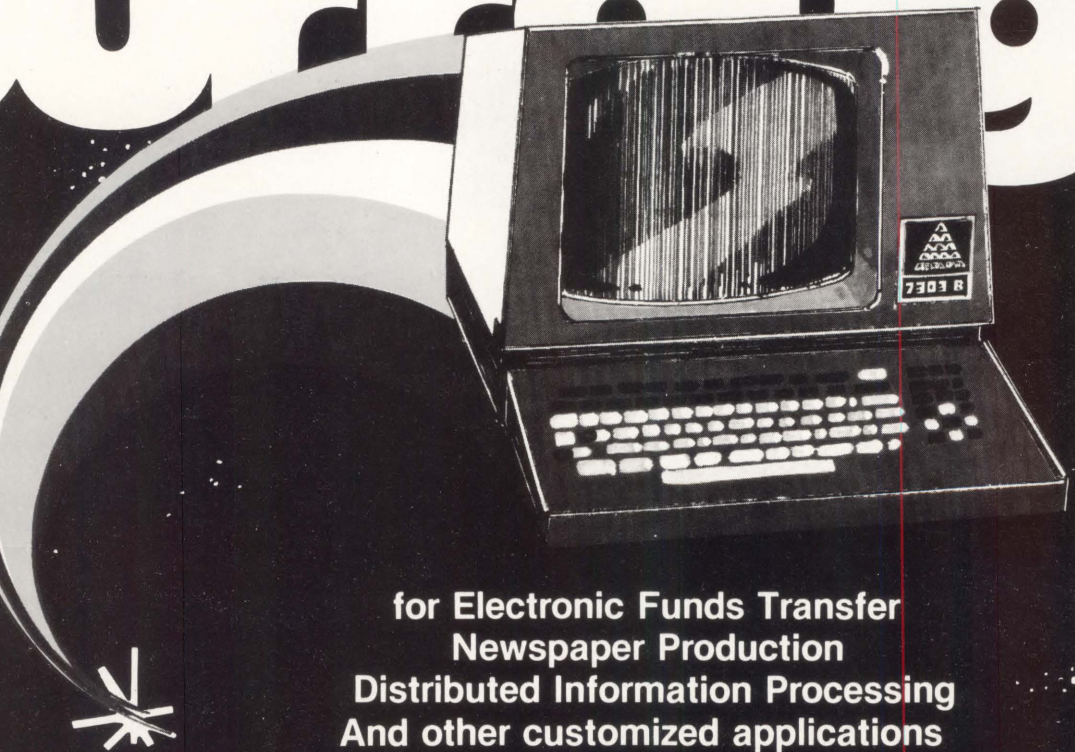
For complete information about the SMART and SMART-E Interfaces and PRIAM's SMART SET of Winchester disc drives, RSVP by telephone or write to:

PRIAM

3096 Orchard Drive San Jose, CA 95134
Telephone (408) 946-4600 TWX 910-338-0293

CIRCLE 100 ON INQUIRY CARD

we've gone beyond Burroughs



for Electronic Funds Transfer
Newspaper Production
Distributed Information Processing
And other customized applications

We've gone beyond Burroughs for you. With a full feature display terminal that offers *out of this world power, flexibility, speed and cost-effectiveness.* And that's just the beginning. These and many more advantages are available in the new DELTA 7303B text processing terminal, designed exclusively for Burroughs-based multidrop communications networks. It's the advanced Burroughs-compatible version of our popular DELTA 7303 display terminal, ready for your Burroughs network now. And we're ready to tell you all about it, with full technical literature, applications assistance and a demonstration. Come beyond Burroughs with us. Call or write today.

DELTA DATA
DELTA DATA SYSTEMS CORPORATION
Woodhaven Industrial Park
Cornwells Heights, PA 19020
(215) 639-9400

CIRCLE 54 ON INQUIRY CARD

A PENNWELL PUBLICATION

COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

JUNE 1981

SPECIAL REPORT ON SYSTEMS SOFTWARE

DILOG NUMBER 1 FOR DEC 11*

With LSI 11/PDP 11 Software Compatible Disc/Tape Controllers Offering Single Board Low Power μP Based Design and Low Cost...
Plus Many Other Good Reasons!

The reasons start with DILOG'S (Distributed Logic Corp's.) full time engineering and design staff. *Not outside suppliers.* That means when you contact DILOG for product selection or after sale service, you'll get "first hand" assistance...along with years of experience manufacturing μP based controllers that interface with DEC 11 CPUs.

The intelligent products you'll discuss all utilize common proprietary architecture and DILOG automated design techniques—products with exceptional reliability and cost efficiency...mostly available from stock. And when you plug a DILOG controller into your DEC CPU it's ready-to-run because it's *fully operating system software compatible.*

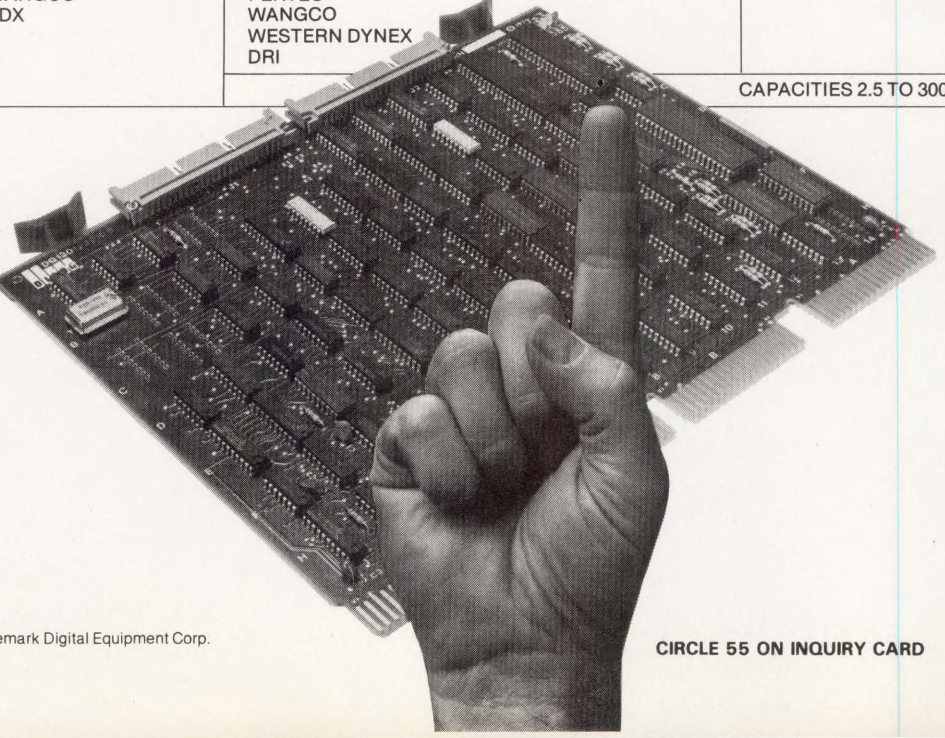
These high performance data storage interface products also feature • minimum bus/space requirements • up to 60% less power • 10 to 50% lower cost • automatic self-test...and numerous other features for easy system integration.

Consult the DILOG/disc-tape compatibility table for your needs. Then ask for detailed data on existing, or future products from DILOG...#1 in single board DEC 11 compatible disc/tape controllers.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643, Phone: (714) 534-8950 • TELEX: 681 399 DILOG GGVE

DISC/TAPE DRIVE MANUFACTURER COMPATIBILITY CHART

MAGNETIC TAPE	DISC			
½" REEL-TO-REEL STD. & STREAMER	**2315/5440/RK05 CARTRIDGE CLASS**	**CMD CARTRIDGE MODULE**	**SMD STORAGE MODULE**	**WINCHESTER 5¼", 8" OR 14"**
AMPEX	AMPEX	AMPEX	AMPEX	BASF
CIPHER	CAELUS	CONTROL DATA	CENTURY DATA	CONTROL DATA
CONTROL DATA	CENTURY DATA		CONTROL DATA	FUJITSU
DIGI-DATA	CONTROL DATA		BALL COMPUTER	KENNEDY
KENNEDY	DEC		MITSUBISHI	MEMOREX
MICRODATA	DIABLO			PRIAM
PERTEC	IOMEC			SHUGART
TANDBERG DATA (IDT)	MICRODATA			SEAGATE
WANGCO	PERTEC			QUANTUM
TDX	WANGCO			IMI
	WESTERN DYNEX			
	DRI			
	CAPACITIES 2.5 TO 300 MB			



DISTRIBUTED
LOGIC CORP.
DILOG

CIRCLE 55 ON INQUIRY CARD

---

*Trademark Digital Equipment Corp.

SYSTEMS SOFTWARE

EDITORIAL 91

BASIC EXTENSIONS HANDLE SIGNAL PROCESSING FUNCTIONS 93
by Robert W. Ramirez

Modifying BASIC extends and enhances software to fulfill evolving requirements of measurement control and waveform analysis

COBOL AS A HIGH LEVEL LANGUAGE FOR MICROCOMPUTERS 99
by Peter Hewitt

Performance comparisons between high level languages indicate COBOL's potential in microcomputer system applications

CREATING TEST EQUIPMENT FEATURES VIA SOFTWARE STRATEGY 103
by Paul Austgen and Bill Watry

Under software control, a fully automatic test measurement system provides powerful, extensible features that need virtually no added hardware

THE IMPACT OF 16-BIT MICROPROCESSORS ON SOFTWARE DEVELOPMENT TOOLS 111
by Mary Jane Elmore, David Miller, and Jim Schwabe

Development system selection criteria should demand specialized tools tailored to each step of the cycle

FORTH—THE LANGUAGE OF MACHINE INDEPENDENCE 117
by Gary Feierbach

Indirect threaded code implements a highly efficient and extremely transportable programming language with a history of success in digital control applications

SOFTWARE PRODUCTS 122

MTOS FROM IPI

THE ONLY THING COMPARABLE TO ONE IPI MTOS...

ANOTHER IPI MTOS

MTOS products are written in assembly language, with run-time support for some higher-level languages. All versions of MTOS are distributed in source language form, under a licensing policy which permits the customer to embed object versions in products without further charge.

MTOS-86 **MTOS-80** **MTOS-68**
MTOS-86MP **MTOS-80MP** **MTOS-68K**

Belgium: BETEA S.A., Chaussee de Louvain, 775, B-1140 Brussels, Phone: (02) 736 80 50, Tlx 846-23188
France: CELDIS SA, 53 Rue Charles Frerot, 94250 Gentilly, Phone: 546.13.13, Tlx 842-200485
Germany: ALFRED NEYE-ENATECHNIK, Schillerstrasse 14, 2085 Quickborn (Hamburg), Phone: 041 06 / 612-240, Tlx 841-213590
Israel: CONTAHAL LTD., 54 Ibn Gvirol St., Tel Aviv, 64364, Phone: (03) 269 379, Tlx 922-33654
Japan: TOKYO ELECTRON LIMITED, Shinjuku Nomura Bldg. 1-26-2 Nishi-Shinjuku, Shinjuku-Ku, Tokyo 160,
Phone: 03-344-5893, Tlx 781-2322240
Netherlands: C.N. ROOD B.V., Cort v.d. Lindenstraat 11-13, Postbus 42, 2280 AA Rijswijk, Nederland, Phone: 070-996360, Tlx 844-31238
Scandinavia: FRONTEC MICRODATORCENTRUM AB, Box 204, Malmvagen 28, Sollentuna, Sweden, Phone: 08-359360, Tlx 854-15130
Switzerland: XMIT AG, Bellikonerstrasse 218, CH-8967 Widen, Phone: 057-54656, Tlx 845-59955
UK: HAWKER SIDDELEY DYNAMICS ENGINEERING LTD., Manor Road, Hatfield, Herts. AL10 9LP, Phone: (7072) 73439, Tlx 851-24835

ipi Industrial Programming Inc.
Software specialists since 1963

100 Jericho Quadrangle, Jericho, N.Y. 11753 • (516) 938-6600 • Telex 429808

CIRCLE 56 ON INQUIRY CARD

EDITORIAL

This month's special issue is a double milestone for **Computer Design**, *and we trust that you will find it interesting. It represents the beginning of increased editorial coverage of system level software topics in* **Computer Design,** *and it is the first special issue on software that we have ever done. It's no secret that the advent of the microprocessor has placed the computer system designer in direct confrontation with system level software. It's also no secret that good operating level software combined with good hardware is the "stuff" of which good systems are made.*

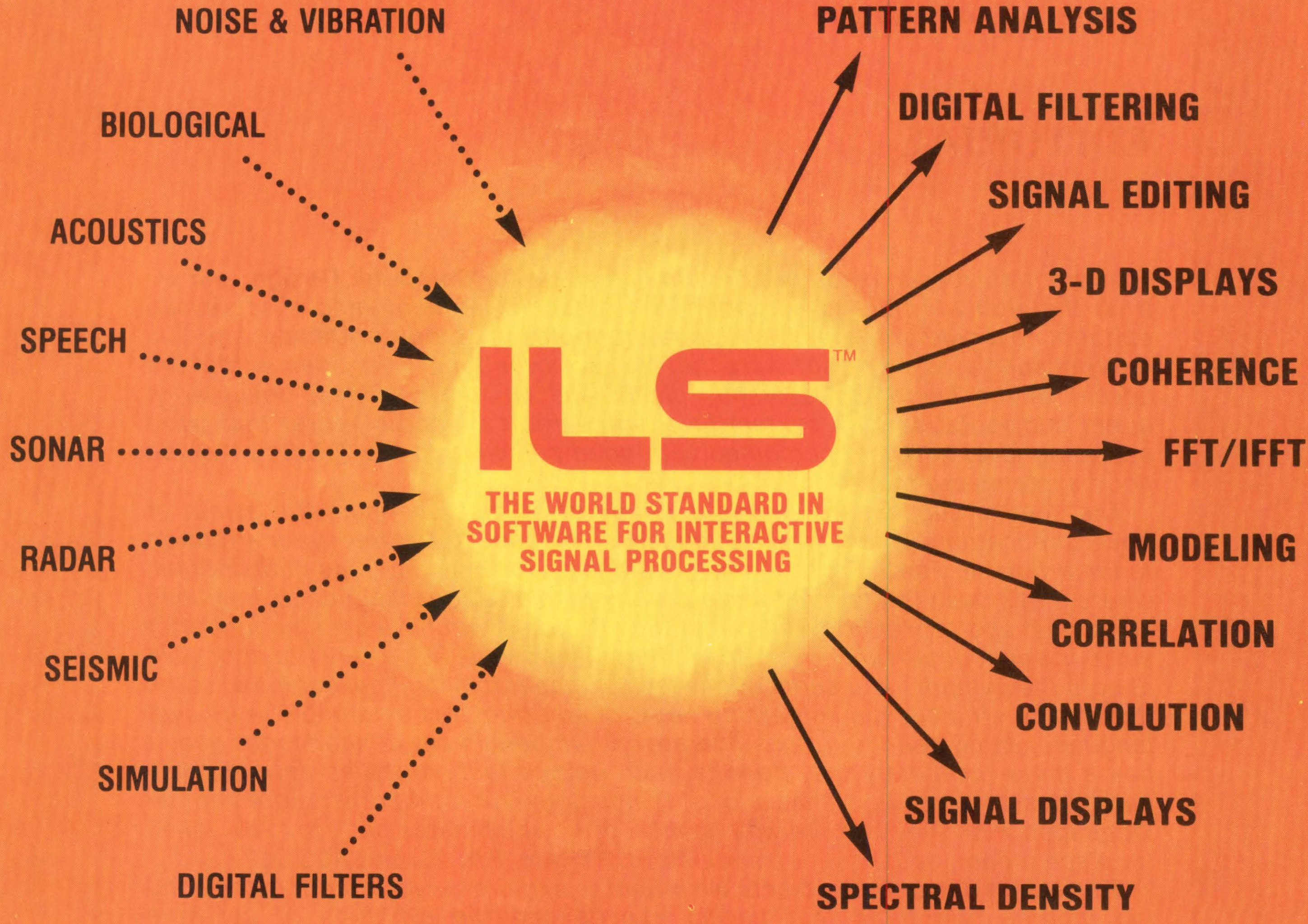
The special supplement carries a variety of articles spanning the gamut of novel applications of software to languages. We especially direct your attention to the article on Forth. Professional coverage of Forth by the trade publications, where it has been treated more as a novelty than a serious langugage, has been somewhat spotty. Yet Forth has all of the attributes that have been sought after since the cost of software outstripped that of hardware. It is easily transportable at both the compiler and applications level; it generates minimal compiled code; its runtime efficiency is something short of amazing; it is extensible in its own language; its numeric functions operate on numbers in any desired radix; and, it has a meta-vocabulary that permits such unique techniques as defining new data types. In short, Forth has a lot of things going for it that other more popular languages wish they had. So why hasn't Forth, which dates back to 1969, taken its place alongside languages such as FORTRAN, BASIC, and ALGOL?

This is just one of the subjects we intend to explore in more depth in the coming months. We think that having experienced the evolution of software sophistication that has occurred over the past 30 years, the computer industry deserves something better than a return to primitive machine language just because hardware designers have suddenly discovered software as a replacement for hardwired logic.

Saul B. Dinman

Saul B. Dinman
Editor

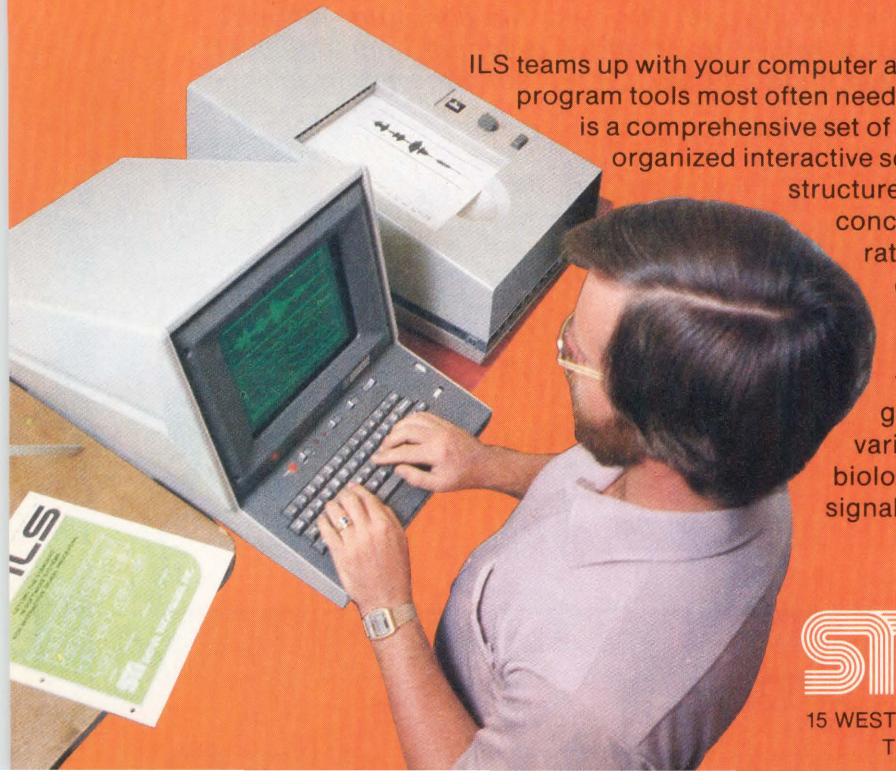
Give ILS a signal... then watch ILS give you results.



NOISE & VIBRATION
BIOLOGICAL
ACOUSTICS
SPEECH
SONAR
RADAR
SEISMIC
SIMULATION
DIGITAL FILTERS

ILS™
THE WORLD STANDARD IN SOFTWARE FOR INTERACTIVE SIGNAL PROCESSING

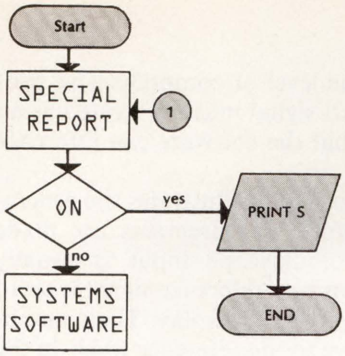
PATTERN ANALYSIS
DIGITAL FILTERING
SIGNAL EDITING
3-D DISPLAYS
COHERENCE
FFT/IFFT
MODELING
CORRELATION
CONVOLUTION
SIGNAL DISPLAYS
SPECTRAL DENSITY



ILS teams up with your computer and graphics terminal to provide a set of program tools most often needed to support signal processing activities. ILS is a comprehensive set of FORTRAN programs which makes up an organized interactive software system that has standard file structures, documentation, and support. ILS lets you concentrate on your specialized applications rather than system design and routine program development, thereby saving valuable time, and at a fraction of the cost of writing your own software. ILS has been installed worldwide in numerous industrial, university, government, and research organizations for varied applications ranging from low frequency biological signal analysis to high frequency radar signal processing.

Call Toll Free (800) 235-5787
(Except California, Hawaii, Alaska)

SIGNAL TECHNOLOGY, INC.
15 WEST DE LA GUERRA • SANTA BARBARA, CA 93101 • USA
TELEPHONE (805) 963-1552 • TWX 910-334-3471



Signal processing software package strikes a balance between capabilities and ease of use

BASIC extensions handle signal processing functions

High quality digitizers, microprocessors, and the IEEE 488 general purpose interface bus have brought measurement technology to the brink of a new era. Soon a wide variety of instruments will be linked to computers for measurement control and complete waveform analysis. Today's software, however, must be enhanced to control the broad range of instruments that will operate in this expanded measurement and analysis environment. Waveform storage, array processing, extended command sets for signal processing, graphics, and modular organization together represent a large portion of this development effort.

To be truly viable, however, a software package must meet user needs first. Since the final package will be used by someone who, at best, is only secondarily interested in programming, a familiar language that is both easy to learn and easy to use should be chosen. BASIC, which is configured as a natural extension of the user's thinking and is similar to the English language, meets these user needs. It also allows mathematical and scientific formulations to be expressed in a straightforward algebraic manner familiar to most people. Instrument control and signal processing software examples throughout this article are set forth in a Tektronix designed extension of this language, SPS BASIC.

Robert W. Ramirez
Tektronix, Incorporated
PO Box 500, Beaverton, OR 97077

Instrument control

Standard software language packages must be augmented by drivers for instrument control and signal processing. The interfacing scheme determines the form of any instrument driver. (See Fig 1.) Although high level drivers and custom interfaces can be tailored to support each instrument model, custom systems may require extensive modification when new instruments are added to expand measurement capabilities. It was for this reason that the computer automated measurement and control (CAMAC) system was developed several years ago—to establish a framework for system compatibility. CAMAC's scope and precision avoid many ambiguities that would lead to individual designer interpretations.

Because the CAMAC standard is too rigid for many applications, however, instrument manufacturers and users often prefer compatibility with the newer, more flexible general purpose interface bus (GPIB). Without dictating instrument selection or applications, the GPIB ensures compatibility by establishing electrical, mechanical, and functional requirements for a wide range of measurement instruments. One drawback of the GPIB standard is that this flexibility permits designer interpretations that can introduce operational inconsistencies. The best way to rule out these inconsistencies is to design a GPIB driver with a primitive command set encompassing all of the functions allowed by the instrument specification. This will produce line-level control of an instrument's interface over the bus, as well as the capability to cope with varying hardware interpretations of the GPIB standard. The price paid for a device of this flexibility is that it must be programmed extensively to

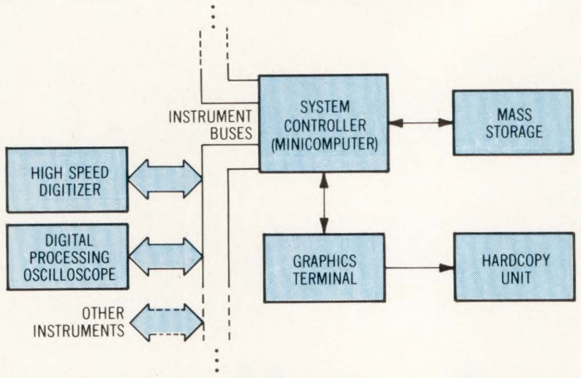


Fig 1 Typical instrument control architecture. New technologies have simplified configuration of measurement systems. Software and firmware communicate easily with any of wide choice of GPIB compatible instruments, processing and displaying data from them, including complete arrays of digitized waveforms

accomplish even simple control tasks with primitive commands. In cases in which instrument manufacturers follow widely accepted interpretations of the GPIB standard, this problem can be solved by a high level GPIB command set that will combine many primitive operations into a single command.

After instrument control has been established, the next step is usually to transfer data over the bus to a minicomputer. Unfortunately, data transmission problems often arise when large numbers of instruments are operated on several buses. Since instrument failure can result in a condition that causes malfunctions in the measurement program, user options for processing error conditions are necessary to avert such malfunctions. In SPS BASIC, for example, error processing is accomplished by the ONERR command

```
ONERR IA GOTO 750
```

where IA specifies a particular error condition and GOTO provides branching to a contingency routine if the error occurs. These error processing routines can simply provide notification of the error, or they can reconfigure the system to avoid the offending condition.

Array processing software

After instrument control has been established and data can flow over the bus to the system controller, the next step is to convert data into a standard format for easy processing. Data sometimes represent a single value, such as a voltage. In other cases, data represent a digitized signal. Once appropriate software is available, interfacing a variety of meters and analyzers that measure individual parameters becomes much less economical than accepting one digitized signal and computing such parameters as mean, root mean square, maximum, minimum, energy, and frequency spectrum. However, for this extreme level of comprehensive processing, the entire digitized signal must be treated as an entity (ie, a waveform) that the software can reference as a single piece of data.

A standard oscilloscope display illustrates the general approach [Fig 2(a)]. Before measurements are made from the display, the oscilloscope input is usually grounded and the resulting zero-reference signal is set to a convenient reference level on the display. Then, amplitudes are measured relative to the reference level. In the same way, when processing a digitized signal, a zero-reference signal is first digitized and stored. The signal to be analyzed is next digitized and stored as a set of integers ranging from 0 to 256, 512, or whatever bit resolution the digitizer permits. Multiplication by the vertical scale factor, and division by the digital increments allowed for that scale factor, convert the digitized signal data to amplitude data, usually expressed in floating point format. Subtracting the zero-reference level from each point then injects the zero-reference information.

Any waveform display exhibits the basic descriptive components of zero-reference level, vertical scale factor, horizontal scale factor, and waveform values. A digital signal processing system must incorporate all of the descriptive components into an integrated waveform data structure. Fig 2(b) shows 512 equally spaced vertical samples with a zero-reference value subtracted from each. Together with vertical units (eg, volts or amps), a horizontal scale factor, and horizontal units (eg, seconds), these form an array of waveform values, similar to the values that could have been read off the Fig 2(a) display. Scale factor and units data are separate variables, loosely attached to the array of amplitude values. Collectively, all of this data constitute the waveform data structure.

With two or more waveforms stored in waveform data structures, a standard FOR loop can perform mathematical combinations. For example,

```
FOR I=0 TO 511
LET WC{I}=WA{I}+WB{I}
NEXT I
LET HC$=HA$
LET VC$=VA$
LET HC=HA
```

where the last three lines process horizontal units, vertical units, and the vertical scale factor, respectively. The FOR loop approach is clumsy during extensive processing, however. A better approach extends the software to handle entire arrays automatically, in an element by element manner, resulting in simpler programs with faster execution times. SPS BASIC, for instance, performs the same waveform processing operations as the preceding FOR loop with only one instruction,

```
LET WC=WA+WB
```

and this instruction processes horizontal units, vertical units, and the horizontal scale factor.

Extended software routines can process all of the standard BASIC functions element by element, handling arrays automatically, The sine function (SIN), for

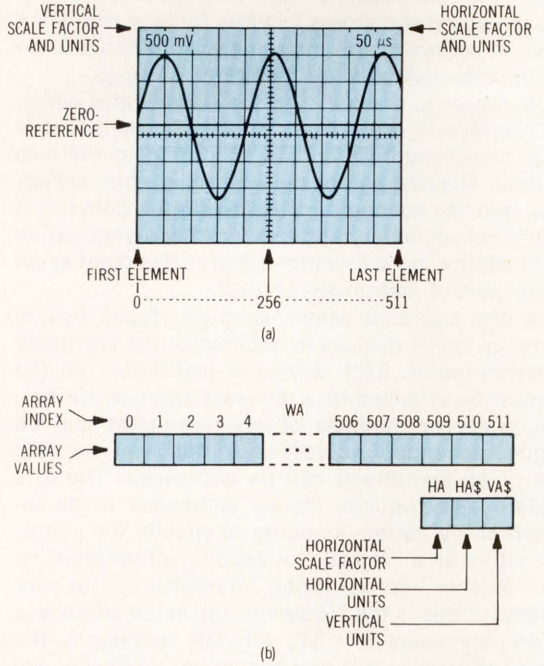


Fig 2 Expansion adds array processing capability. In this example, zero-reference value is subtracted from each of 512 equally spaced vertical samples, resulting in array of waveform values. Waveform display (a) graphs descriptive components. Waveform data structure (b) consists of zero-referenced array of waveform values, vertical units, horizontal units, and horizontal scale factor

example, can be set up to operate either on a single-valued variable in the usual manner, or element by element on an array. Given the array WD, which contains elements running linearly in value from 0 at element 0 to 2 π at element 511, when the statement

```
LET WD=SIN{WD}
```

is executed, WD will be converted to an array of values following a sinusoidal pattern.

One way to verify the results of this program is to print out the array values and compare them to a sine table. When expanded to handle arrays, the print statement

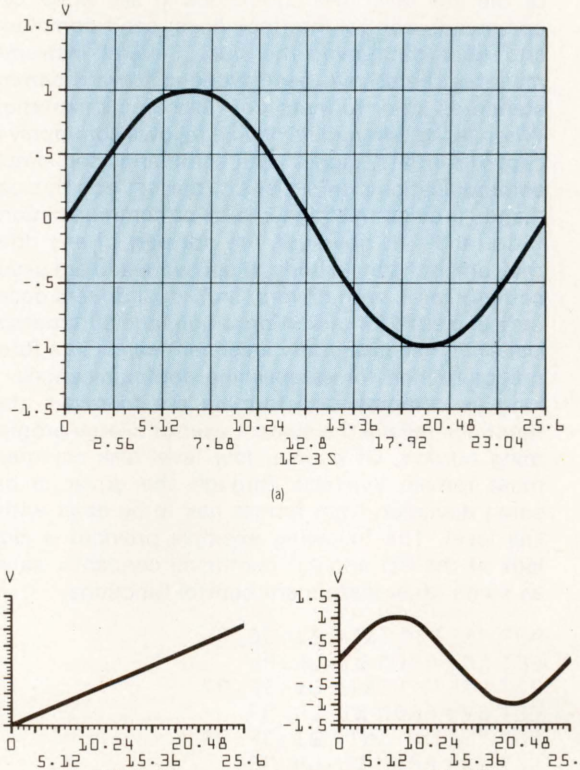
```
PRINT WD
```

produces a long string of numbers—all the values in WD. An easier way to check the results, however, is to augment the standard BASIC package with a graphics terminal driver and a graphics package so that the actual form of the contents is made visible. Fig 3 demonstrates this graphics display.

Command sets for signal processing

With added instrument control and array handling capabilities, a standard software package can become a powerful tool. A standard BASIC command set alone, however, is inadequate for this task; several common waveform measurement operations are not included as single commands in most standard packages. Integration; differentiation; and finding the maximum, minimum, mean, and root mean square values of a waveform all can be processed by FOR loop routines. In signal analysis, however, these operations are common enough to warrant their own commands. Signal processing software should have commands allowing operations like

```
INT WA,WB
LET X=MEA{A}
LET Y=RMS{WB}
LET Z=MAX{A}
```



```
VIEWPORT 100,450,150,350
SETGR GRAT 2,2,VIEW
GRAPH WD
LET D=SIN{D}
VIEWPORT 550,900,150,350
SETGR GRAT 2,2,VIEW
GRAPH WD
SMOVE 0,0
END
```

(b)

Fig 3 Command set extension handles signal processing tasks. GRAPH command of SPS BASIC illustrates simplicity and flexibility combined in signal processing package. Standard operations are performed by single commands (a) such as GRAPH WD, but can be modified by optional commands or statements (b)

Examples of Instrument Control At Various Levels

Beginning with the low level GPIB driver, a short program segment can demonstrate the potential complexities of line-level GPIB programming. The program reads ten bytes of data from a device on the bus and stores the data in an integer array. This is one possible task of the many that normally constitute a complete communications sequence. Line-level commands use programs such as

```
INTEGER B{9}
SIFCOM @N,"UNT","UNL"
SIFLIN @N,"LENB"
SIFCOM @N,TA,SA
FOR I=0 TO 9
RBYTE @N,B{I}
NEXT I
SIFLIN @N,"ATNT","NRFDF","LDIS"
SIFCOM @N,"UNT"
```

in which SIFLIN (Set InterFace LINes), SIFCOM (Send InterFace COMmand), and RBYTE (Read BYTE) are three of the low level GPIB commands in SPS BASIC. Such commands control interface lines, send commands, and read data over the bus. Several instrument manufacturers have been working toward common standards and formats for GPIB implementations. When a GPIB compatible device follows commonly accepted formats, higher level commands can simplify communications. In SPS BASIC, the GET and PUT commands provide this higher level of communications.

GET and PUT, however, are not part of any driver; they are in the main body of software and are used to communicate with drivers. Individual drivers decode GETs and PUTs for task information, and automatically issue the necessary low level commands in a format predetermined for establishing communications. As long as common GPIB formats are followed, these functions relieve the system user of a large programming burden. Of course, low level GPIB commands must remain available through the driver in case some deviation from format has to be dealt with at line level. The following example provides a closer look at the GET and PUT command concepts, as well as some other instrument control functions.

```
PUT "SET?" INTO @1,32,96
GET SM$ FROM @1,64,96
PUT "SET?" INTO @1,32,97
GET SV$ FROM @1,64,97
PUT "SET?" INTO @1,32,98
GET SH$ FROM @1,64,98
```

This program segment goes through the low level driver to get data from a 7912AD programmable digitizer and its programmable plug-ins. Essentially, it PUTs the question, "What are your control SETtings?" to the 7912AD and GETs those settings, storing them in SM$ for the instrument mainframe, SV$ for the vertical amplifier, and SH$ for the horizontal time base.

Looking at the first line for more details of the operation, the low level driver decodes the PUT command arguments for what is to be sent and where it is to be sent. In this case, a device dependent query is the command to be sent ("SET?"), and it is to be sent to address @1,32,96. The driver then sends the necessary GPIB commands (RENS, UNTS, UNLS, etc) in sequence to accomplish the task. Here, "SET?" is sent to the 7912AD programmable digitizer, to which the instrument responds by preparing a string of messages that indicate the current status of its programmable settings. Under the direction of the driver, the subsequent GET command gets the message string and stores it in SM$ for later reference or use in returning the instrument automatically to the condition indicated by the stored settings.

With regard to the @1,32,96, the @1 indicates which GPIB interface is to be used, and the 32,96 is a particular device address set up according to the GPIB standard. The first part of the address is a primary address, and the second part (following the comma) is an optional secondary address. Further investigation of this addressing is recommended at this point as an integral part of instrument control.

The GPIB standard allows each interfaced bus to control up to 14 devices in addition to the controller or minicomputer. Each device or instrument on the bus must be strapped for a different address; furthermore, parts or modules of an instrument can be assigned secondary addresses. In this way, specific parts of an instrument can be addressed. The GPIB standard also requires device addresses to be incremented by certain amounts to specify the instrument either as a "talker" for sending information, or as a "listener" for receiving information. The convention for this is the following: the listen address is the primary address +32; the talk address is the primary address +64; and secondary addresses are incremented by 96 for both talk and listen.

In the preceding PUT-GET example, communication was strapped with a 7912AD programmable digitizer for a primary address of 0 and a secondary address, also 0, for its mainframe. The 7912AD also contained a vertical amplifier with a secondary address of 1 and a time base with a secondary address of 2. Thus, following GPIB addressing, @1,32,96 addressed the mainframe as a listener and @1,64,96 addressed the mainframe as a talker. The same was done in subsequent lines for the vertical amplifier and horizontal time base.

Fourteen instruments on a bus, each with several secondary addresses, can lead to confusion; a high level driver can help bring order to such a situation. Besides reducing the number of program statements required for some tasks, a high level GPIB driver can take care of many basic details; this is illustrated when the preceding example is rewritten by the SPS BASIC high level GPIB driver,

```
ATTACH #17 AS INS 0,0:WITH 1,2 @1

 .
 .
 .

GET SM$ FROM #17,"SET?"
GET SV$ FROM #17;1,"SET?"
GET SH$ FROM #17;2,"SET?"
```

where the instrument is programmed to ATTACH to a single name, #17. (Other instruments on the same or on another bus will have different names attached.) From that point, the instrument is referred to as #17, and the high level driver keeps track of interface numbers as well as talk and listen addresses. The send and receive operations also have been combined into single commands. Other simplifications typically provided by high level drivers include automatic conversion between common data formats and specialized interrupt handling such as automatic polling.

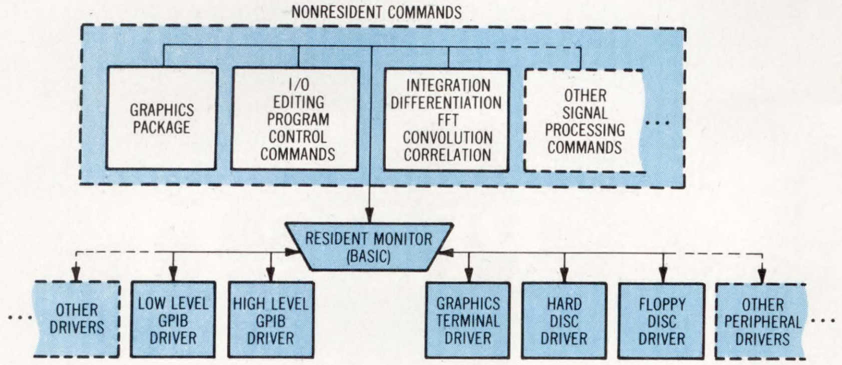


Fig 4 Modular organization promotes flexibility. Instrument drivers, peripheral drivers, and nonresident commands are loaded into main memory only as needed, and can be released or overwritten when their jobs are completed. Additionally, software is structured so that new modules can be added as they are developed

and so forth, where A and B are simple arrays, and WA and WB are waveforms. Several other operations, including the fast Fourier transformation (FFT), convolution, and correlation, are not as common as the preceding calculations but are indispensable when needed; they can also be added as single-command operations.

Modular organization

GPIB driver, peripheral drivers, graphics, array processing, and a variety of additional commands for signal processing will not fit into a minicomputer memory at the same time. Since most packages and commands are not needed in memory simultaneously, they can be organized into modules, to be held on floppy or hard discs and not loaded into memory until needed.

Modular software consists of a resident monitor (in memory all of the time), nonresident commands (loaded into memory automatically when called for), and drivers (loaded as packages when needed). Modular organization, shown in Fig 4, offers efficient memory use and the capability to add or replace modules whenever necessary. Of course, loading nonresident functions from a peripheral takes time. But this time tradeoff can be reduced significantly by programming the four or five most frequently used commands or functions to remain in memory after their first usage.

Conclusion

Measurement control and waveform analysis capabilities can be enhanced greatly by software that is designed to control a broad range of instruments and process any type of signal. In modular form, signal processing software offers flexibility as well as the potential for powerful analysis. Before comprehensive instrument control and signal processing software can be developed, however, certain fundamental needs must be met. Measurement needs include instrument control, waveform storage, array processing, an expanded command set, graphics, special analysis packages, and clear, comprehensive documentation. Human needs also must be taken into account. To be truly successful, the software must strike a proper balance between capability and usability, and for that purpose a user friendly language that is consistent and predictable must be employed.

Acknowledgments

The author wishes to thank Don Williams, Paula Ochs, Roberta Taussig, and Joyce Ferriss, all of Tektronix, Inc, for their many valuable suggestions during the preparation of this article.

Bibliography

IEEE Standard Digital Interface for Programmable Instrumentation, IEEE Std 488-1975, The Institute of Electrical and Electronics Engineers, Inc, 1975

J. Kimball, "The IEEE 488 Bus—Going Your Way?" *Handshake,* Winter 1977-78, Tektronix, Inc, Beaverton, Ore, pp 2-6

7912AD Programmable Digitizer Operator's Instruction Manual, Tektronix, Inc, Beaverton, Ore, 1978

TEK SPS BASIC V02 System Software Instruction Manual, Tektronix, Inc, Beaverton, Ore, 1979

About the Author:

Robert Ramirez is an applications engineer at Tektronix, Inc, Instrument Division. His primary responsibilities are investigation and documentation of digital signal processing techniques and applications. Mr Ramirez also edits and contributes to Handshake, *the Tektronix newsletter for signal processing and instrument control.*

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 728 **Average 729** **Low 730**

Cherry dependability... in an alphanumeric display that's readable in sunlight, any light ... and installs in seconds

Excellent brightness, full half-inch characters, 7-bit ASCII input and simple plug-in installation make the Cherry gas discharge display the right choice for you. Surprising versatility in a small package—adjustable brightness, flashing display and blank panel modes, fully addressable cursor, custom designs, too. Call or write today for complete technical literature or a full demonstration.

Take a closer look:

2 simple plugs are the only hook-up required.

Only one voltage (12VDC) required.

Selectable baud rate with RS232C or TTY standard.

5 adjustable brightness levels.

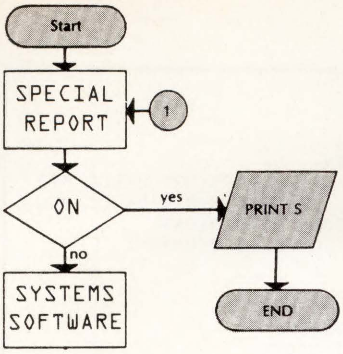
16 or 20 characters long.

CHERRY® GAS DISCHARGE DISPLAYS

CHERRY ELECTRICAL PRODUCTS CORP. 3614 Sunset Avenue, Waukegan, IL 60085—312/689-7700—TWX 912/235-1572

Worldwide affiliates and phone numbers: Cherry Semiconductor Corp., East Greenwich, RI, U.S.A., 401-885-3600 • Cherry Mikroschalter GmbH, Auerbach, Germany, 09 643 181 • Cherry Electrical Products Ltd., Harpenden (Herts) England, (05827) 63100 • Cherco Brasil Industria E. Comercio Ltda., Sao Paulo, Brazil, 55 (011) 246-4343 • Hirose Cherry Precision Co., Ltd., Kawasaki, Japan, 044 933 3511

CIRCLE 58 ON INQUIRY CARD



Once far too large to be useful in a microcomputer environment, COBOL today can be the best choice for certain microcomputer applications

COBOL as a high level language for microcomputers

The advantages of COBOL for data processing software development are unmatched by any other language used in microcomputer systems. Like FORTRAN, BASIC, and Pascal, COBOL is a high level language that has become viable in microcomputer systems, which are now able to support sufficient memory. It helps software designers in ways that other languages cannot. For example, Pascal offers flexibility but at the expense of standardization, severely limiting portability of application programs between processors. APL and Forth are extremely compact and efficient, but can be so cryptic that they are difficult to read and even harder to maintain over the life of a commercial application program. Other languages, notably BASIC, are easy to learn but lack sufficient file handling capability for many commercial applications. Further, experienced programmers are in short supply for many of the newer languages now popular on microcomputer systems.

COBOL benefits from being an established language in use for more than two decades. Mature application packages and qualified programmers abound in the industry, and its natural language format makes COBOL programs easy to read and maintain. The language facilitates modular programming, as well as provides powerful file handling, sorting, and data structuring. Because COBOL's standard is firmly maintained, the programs have excellent portability between processors.

Not a dinosaur anymore

Advocating COBOL for microcomputer systems may raise questions among some software designers who remember its reputation for huge memory requirements. They are likely to ask if it is not just a dinosaur of a language, far too large to be useful in the microcomputer environment. Indeed, this reputation is rooted in its history: over the years, it has not been uncommon for large, third-generation mainframes to have COBOL compilers with memory requirements ranging from 120k to 190k bytes. COBOL's batch application programs also typically required large amounts of memory to support input/output (I/O) buffers. However well deserved the comparison to a dinosaur may have been in the past, this is no longer the case. Software technology has responded to the needs of the microcomputer environment to produce a new generation of concise, efficient COBOL packages that are uniquely suited to microcomputers. The CIS COBOL™ (Compact, Interactive, Standard COBOL) system exemplifies this new generation available for microcomputer systems. Examining this system will illustrate how the microcomputer implementation of COBOL meets the requirements of microcomputer software development.

CIS COBOL is the first COBOL compiler designed specifically for microcomputer systems. It is also the first to be certified by the U.S. General Services Administration for government use on microcomputers, following tests administered by the Federal Compiler Testing Center. Its name underscores the distinctive features of the language implementation. The CIS compiler is compact. It makes large amounts of memory unnecessary by employing design trade-offs to make memory more efficient. A specific element in design is the use of an interpretive coding technique. Further, the system's orientation toward interactive transaction processing applications allows the software to process a single record at a time, eliminating the need for large file buffers. The resulting reduction in memory requirements is dramatic. The American National Standards Institute (ANSI) standard CIS COBOL can be used

Peter Hewitt
Micro Focus, Incorporated
1601 Civic Center Dr, Santa Clara, CA 95050

comfortably in machines with as little as 48k bytes of main memory. A second, more compact version implements a subset of ANSI standard COBOL and can be used in machines with as little as 32k bytes of main memory.

COBOL implementations for microcomputers have made a valuable contribution to the commercial data processing community. They give microcomputer system users a compiler equivalent in power to one that would fit on a medium sized minicomputer, as well as provide special interactive features like simpler screen handling, which makes software development easier and reduces software bugs in screen I/O. Interactive COBOL for microcomputers also enhances the human factor in data processing. Because users have direct "hands-on" control of the microcomputer system, they do not depend on operations personnel to mount tapes and discs. As a result, fewer devices are likely to be mounted incorrectly through operator error, as often happens in large batch processing environments where storage media are changed constantly.

```
DATA DIVISION.
WORKING-STORAGE SECTION.
01 FIRST-ADD-VALUE            PIC 9{03} VALUE 972.
01 SECOND-ADD-VALUE           PIC 9{03} VALUE 396.
01 TEMPORARY-RESULT-STORE     PIC 9{04}.
01 RESULT-FIELD               PIC 9{04}.
PROCEDURE DIVISION.
BEGIN-ADD.
  ADD FIRST-ADD-VALUE TO
    SECOND-ADD-VALUE GIVING
      TEMPORARY-RESULT-STORE.
PREPARE-RESULT.
  MOVE TEMPORARY-RESULT-STORE TO RESULT-FIELD.
```

Fig 1 Natural language readability. COBOL variable labels clearly identify nature and role of each item of data. Their greater legibility can eliminate maintenance problems and cut support costs

Language created for industry

More than 20 years ago, the U.S. Department of Defense recognized the need for a standard language for general commercial use and convened the industry-wide Conference on Data Systems Languages (CODASYL) to specify the design requirements for such a language. COBOL was created as a result, and the conference is still held about once a month to ensure that the language develops in the best interest of the entire data processing community. The standard for COBOL is published by ANSI on the basis of CODASYL's work and is enforced by the Federal Compiler Testing Center.

Today COBOL is the only nonproprietary industry-wide standard language specifically designed for commercial use. The investment in its applications programs is estimated to be approximately 10 times the total value of installed IBM mainframes. Many of the benefits of the language come from its standardization. COBOL application software is virtually processor independent because of the strict enforcement of COBOL's standard, an important consideration for companies wishing to avoid major software conversion costs when upgrading system hardware. Portability between processors is also a major concern, especially for software houses that are developing applications packages for use on a variety of processors. An increasing number of software houses that have been developing applications packages for both BASIC and COBOL are dropping their work with BASIC in favor of the more standardized COBOL. Standardization and long use have created many applications packages and qualified programmers. The result should be reduced software development costs, since applications packages can be purchased or created by personnel with expertise in both COBOL and the application involved. This, in turn, can affect new system acquisitions. As the trend toward reduced hardware costs continues, software is becoming the major cost in many system purchases; therefore, the major savings to be realized by using COBOL for software development should often outweigh all other financial factors when considering a system acquisition.

Readability and ease of maintenance are also important in commercial software systems. Unlike many short-lived scientific programs, commercial routines have a typical life of about 5 to 15 years. Consequently, several different programmers are likely to work on a commercial application program, including those who were not involved in the code's creation. This can become costly if the code is poorly documented or hard to follow. In those instances where the code is too cryptic to decipher and its originator has left the company, the program must be scrapped. COBOL helps to minimize problems related to code readability and maintenance. It allows long data names, which enable programmers to clearly identify the nature and role of each variable (Fig 1). Since it reads much like English, programmers find it easy to follow the logic of the programs. In addition, the language is designed to handle

```
DATA DIVISION.
FILE SECTION.
FD REGISTER-FILE.
01 REGISTER-RECORD.
   03 REGISTER-KEY.
      05 REGISTER-KEY-DISTRIBUTOR       PIC X{02}.
      05 REGISTER-KEY-SERIAL-NUMBER     PIC 9{04}.
      05 REGISTER-KEY-CHECK             PIC X{02}.
   03 REGISTER-DATA.
      05 CUSTOMER-ID                    PIC X{34}.
      05 STREET-ID                      PIC X{34}.
      05 CITY-ID                        PIC X{34}.
      05 STATE-ID                       PIC X{02}.
      05 ZIP-ID                         PIC 9{05}.
      05 PHONE-AREA-CODE                PIC 9{03}.
      05 PHONE-EXCHANGE                 PIC 9{03}.
      05 PHONE-NUMBER                   PIC 9{04}.
      05 TELEX-NUMBER                   PIC X{10}.
      05 DEALER-FLAG                    PIC X{01}.
```

Fig 2 Appropriate data structures. Designed expressly for business applications, COBOL data structures help simplify programming of financial statements, management reports, and common business tasks the data common to business. Its data structures facilitate the manipulation of data for financial statements and management reports. Data organized in files and records are easily defined, and the user can clearly see what data items are required (Fig 2).

One of COBOL's most useful features is its powerful file handling capability, which enables it to accept three different types of files: sequential, random access, and index-sequential. Sequential files are serially accessed. Random access files can be entered at any point according to a record number. The index-sequential file is particularly useful, as it can be treated and accessed in both of the preceding ways, and any item of data in the record can act as a key. CIS COBOL adds a fourth type, the line-sequential file. In the microcomputer environment, this file facilitates software development for applications combining data processing with text processing by reading lines of text from the text editor.

Many of the high level languages for microcomputer systems incorporate some of the features of COBOL, but none has all of them. Other languages were introduced over the years to replace COBOL as the industry standard for commercial applications. However, in each instance, the replacement did not occur, usually because the others failed to match one or more of COBOL's important features. This was the case with PL/1, which failed to gain acceptance as a replacement for COBOL and FORTRAN in the mid-1960s. Although PL/1 had all the capabilities of both languages, it was so complex and difficult to learn that it never achieved COBOL's popularity and widespread use. (See the Table.)

RELATIVE STRENGTHS OF LANGUAGES*

		ADA	APL	ASSEMBLER	BASIC	C	COBOL	FORTH	FORTRAN	PASCAL	PL/1
WRITABILITY		2	3	2	4	2	3	3	4	3	2
READABILITY		3	1	1	2	2	4	2	2	4	3
MAINTAINABILITY		3	1	1	2	2	4	2	2	3	3
CONCISENESS		2	4	1	2	2	2	4	2	3	2
EASE OF LEARNING		2	1	1	4	1	3	2	3	3	2
POWER FOR	COMPUTATION	3	4	1	1	1	1	3	3	2	3
	DATA STRUCTURING	3	3	1	1	2	4	3	2	3	3
	FILE HANDLING	1	1	1	2	1	4	2	2	2	3
	CONTROL STRUCTURES	4	1	1	2	3	3	2	3	4	4
STANDARDIZATION		4	3	1	1	4	3	4	3	2	3
PROGRAMMER AVAILABILITY		1	1	1	3	1	4	1	4	2	1
APPLICATION PACKAGE AVAILABILITY		1	1	2	4	1	4	1	4	1	1
AVAILABILITY FOR MICROCOMPUTER SYSTEMS		1	2	4	4	1	3	2	4	4	1
TOTAL		30	26	18	32	23	42	31	38	36	31

1 — Low
4 — High

*Comparison matrix tabulates relative strengths of microcomputer programming languages, showing that some adapt to a microcomputer environment better than others. Rating is subjective; however, COBOL achieves high marks by any standard

Effectiveness of microcomputer COBOL

When used on microcomputers, COBOL benefits both small businesses and programmers in training. Companies whose data processing budgets do not justify expensive hardware systems now have a powerful software systems capability within their reach. Programmers learning the language today enjoy the near-immediate turnaround of the microcomputer system—something not offered by the traditional batch processing environment. Besides making the learning process faster and more rewarding, the low cost of microcomputer hardware allows training installations to have multiple systems, rather than one expensive batch processor. The CIS COBOL package even comes equipped with an interactive debugger that allows programmers to watch code execute line by line.

How effective are today's COBOL implementations for microcomputers? Can the language handle big jobs on microcomputers? When standard CIS COBOL is installed on a microcomputer with 64k bytes of memory, the system can process COBOL source programs of several thousand lines. Using dynamic loading—another CIS COBOL feature—much larger programs can be loaded and run in segments. One user of the system already has just such a configuration and the dynamic loading feature to run a fully integrated accounting package whose overall size is about 750k bytes.

Conclusion

There is no doubt that COBOL is well suited to microcomputers and will be used at least as widely as BASIC and Pascal, while remaining the dominant language for business applications. Furthermore, as future microcomputer hardware technology adopts an entire generation of more powerful 16-bit processors, Winchester disc technology, and multi-user capability, COBOL should play an ever-increasing role in microcomputer software development.

About the Author:

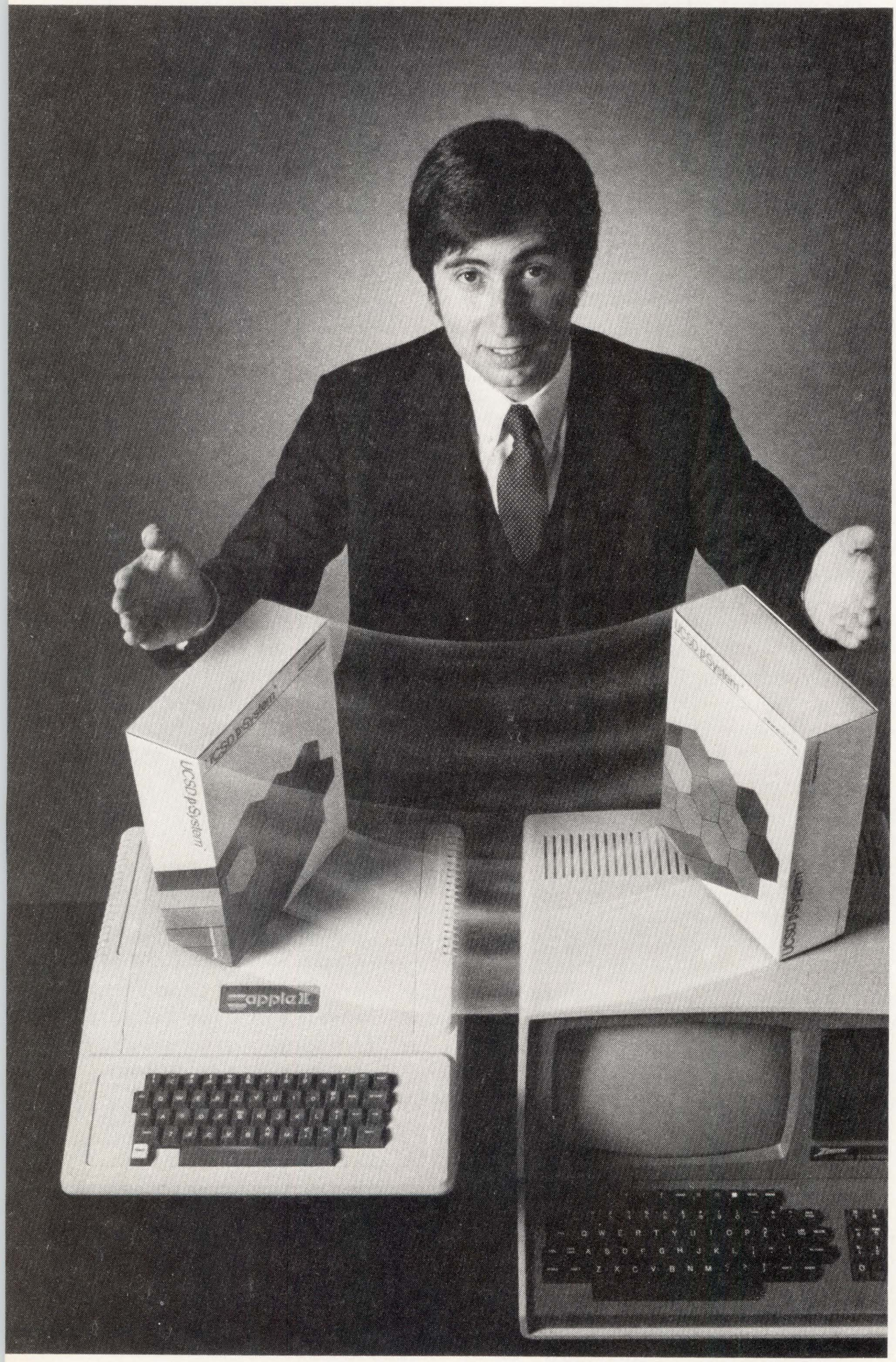
Peter Hewitt has been a marketing executive at Micro Focus since 1979. Before joining Micro Focus, he was engaged for many years in software design, development, and consultancy—using COBOL and other languages. His current interest is the improvement of software productivity through enhanced user interfaces and program generator technology. He is an honors graduate of Cambridge University in England.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 731 **Average 732** **Low 733**

"WITH THE UCSD p-SYSTEM,™ WE CAN WRITE ONE APPLICATION THAT GOES FROM APPLE TO ZENITH."

HARRY BLAKESLEE, President, Denver Software



Our business is bigger and better than ever.

A lot of the credit for that goes to the UCSD p-System software from SofTech Microsystems. It's given us ten times the market we used to have.

We can write a single, sophisticated applications program with the UCSD p-System—like our financial management package—and it just keeps on running. On Apple, Commodore, Ohio Scientific, Texas Instruments, Zenith, and more. That's the real beauty of the UCSD p-System. Any program you write for one microcomputer runs on others, both today and tomorrow. You protect your software investment, without restricting your hardware options.

And with the UCSD p-System, you can use the language of your choice—UCSD Pascal,™ FORTRAN-77, BASIC, or assembly language. All are backed by SofTech Microsystems, a leading system software company who's been around for over a decade, who knows how to develop professional quality software, and who's committed to delivering it.

Get a head start on tomorrow. With the microcomputer software that goes from "A" to "Z." Distribution licensing and single copies available. Write or call for details, so you can start going places, too.

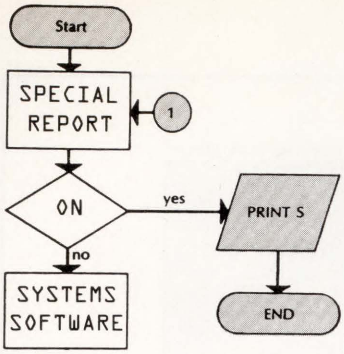
SOFTECH
MICROSYSTEMS
A SUBSIDIARY OF SOFTECH

For the software that's going places.

9494 Black Mountain Road, San Diego,
CA 92126. (714) 578-6105
TWX: 910-335-1594

UCSD p-System and UCSD Pascal are trademarks of the Regents of the University of California.

CIRCLE 59 ON INQUIRY CARD



Software improves overall performance of microprocessor based equipment within fixed hardware architecture

Creating test equipment features via software strategy

Prior to the advent of the microprocessor, designing new measurement capability into test equipment was primarily the task of the hardware designer. But measurement capability is no longer just a function of hardware performance. Software designers are making significant contributions. Software's added dimension allows the user to get more out of a hardware investment because total system performance can be greater than the sum of the individual parts.

An understanding of the software contribution to measurement systems requires a basic knowledge of the system and its operation. Fig 1 shows an HP 1980A/B oscilloscope measurement system consisting of an analog measurement and display section, a digital control and interface section, and a 16-channel digital to analog converter (DAC) to interface the digital to analog sections. The microcomputer is read only memory (ROM) based with 64k of memory space either allocated to basic system functions or reserved for enhancements such as special feature ROMs, front panel expansion modules, or an additional circuit board for repetitive waveform storage.

The key to system intelligence is the trigger flag feedback line from the sweep hybrid to the horizontal hybrid interface on the microcomputer board. It is this feedback line that provides a flag from the trigger circuit to the microprocessor, makes it possible for the microprocessor to interactively control the oscilloscope, and take the 1980A/B out of the realm of a microprocessor controlled oscilloscope into that of a truly automated oscilloscope that detects signal conditions and makes proper adjustments.

In addition to its digital computer architecture, the 1980A/B has a digital operator interface. All functions are selected by pressing "touch keys." For nonvariable functions, such as input impedance and trigger slope, touching the appropriate key results in an audible click and an indicator light showing the condition. For variable functions, such as horizontal and vertical deflection and position, the function is selected by pressing the appropriate key. The variable is then adjusted by turning the rotary control which drives a rotary pulse generator (RPG) that is slaved to whichever key has been selected.

The significance of this design, in addition to simplified operation, is that all keys are "cold switched." That is, the front panel controls are not a part of the oscilloscope circuits. Further, all functions, including variable functions, are controlled by digital signals—generated either internally or externally by a controller. Each of the front panel functions, including the rotary control, has a set of variables associated with it that occupies a dedicated location in nonvolatile memory. The value placed in that location (established as specific keys are pressed) determines the latch and DAC patterns that control operation.

Storing calibration factors

Traditionally, oscilloscopes have been calibrated by applying a known stimulus and adjusting numerous circuit

Paul Austgen
Bill Watry
Hewlett-Packard, Incorporated
1900 Garden of the Gods Rd
Colorado Springs, CO 80907

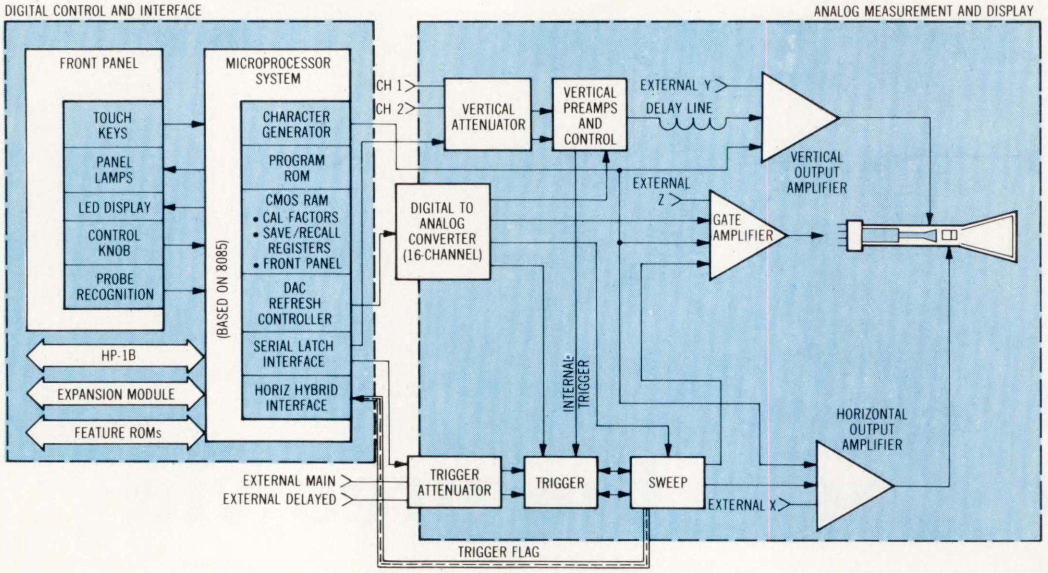


Fig 1 Oscilloscope block diagram. Hybrid design combines analog measurement and display section with microcomputer and "cold switched" front panel. 16-channel DAC interfaces digital section to analog section. Trigger flag feedback line gives microprocessor interactive control over analog circuits

components to provide the desired output at predefined nodes. In other words, circuit parameters were adjusted to provide the desired ranges and sensitivities.

Because of its architecture, a completely different technique is possible in the 1980A/B. Aside from initial setup adjustments, made at the time of manufacture or when circuit components have been replaced, calibration is accomplished entirely by computing calibration factors and storing them in memory for use by the processor in subsequent measurements.

ROM on the processor board contains the routines for calculating and storing calibration factors as well as instructions for performing the calibration routines These instructions are displayed step by step by a character generator on the cathode ray tube (CRT). During calibration, parameters establish a direct correspondence between the number on the light emitting diode (LED) display and the actual binary coded decimal (BCD) number presented to the DAC. The transfer function is assumed to be linear (Fig 2).

Major subsystems of the 1980s, such as the vertical preamplifier and horizontal ramp, are controlled by both digital voltage (latches) and analog voltages (DACs). The DAC channels require BCD numbers between 0 and 2999, with the actual voltage output of each channel dependent upon the specific circuit's design and adjustment. The front panel settings and DAC number relationship may be generally expressed as the slope-intercept form of the linear equation

DAC # = (front panel setting) · A + B

where A and B are the slope and intercept calibration factors, respectively. With a few exceptions, each of these calibration factors is an 8-bit number in the range of 0 to 377_8. Calibration factors reside in a nonvolatile memory that is write-protected except during calibration.

The slope intercept equation can be solved explicitly for A and B; therefore, these values can be calculated if a number of data points equal to the number of unknowns is available. The procedure is manual in the sense that the operator slews the DAC number, using the front panel rotary control, until the trace occupies a predetermined location on the CRT. The software is then

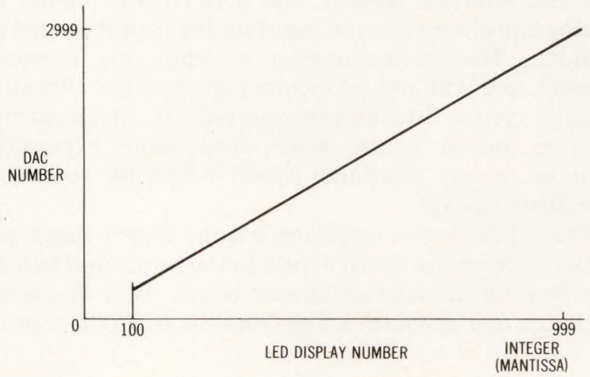


Fig 2 DAC input number versus display settings. Front panel settings (100 to 999) and DAC input number (0 to 2999) have linear relationship expressed in slope-intercept form. Software computes slope and intercept calibration factors when operator slews DAC number until trace occupies predetermined location on CRT

informed, and the number becomes a data point. When a sufficient number of these data points is indicated, the processor calculates and stores the calibration factors for that particular sequence.

Calculations are buffered in the sense that all data points must have been gathered before a calculation, and subsequent storage of a new calibration factor, takes place. This essentially eliminates the possibility of bad calibration factors, due to incomplete sequences, being written.

If a calibration factor calculation results in a number outside the range of 0 to 377_8 (an error), then an error number indicating a failure in that calibration factor is reported to the operator via the CRT. The processor then places the closest allowable value into the calibration factor so that the oscilloscope is operable even though it is out of calibration.

When the calibration routine is completed and a normal exit from the calibration mode occurs, a checksum is computed and its value is stored in write-protected memory. At power-up, the calibration factors are summed and the result is compared with the stored checksum value. During power outages, a backup battery maintains power on the memory circuits to retain calibration factors, as well as other vital data such as the last front panel setting and all stored panel settings. The random access memory (RAM) containing calibration factors is write-protected with a switch on the instrument rear panel. If the switch is in the disabled position, the calibration routine cannot be entered. The calibration factors can be protected by a calibration sticker.

The advantages provided by software based calibration are fourfold: (1) the directions contained in the calibration manual are largely duplicated with firmware and the character generator; (2) all routine calibration is done from the front panel with a single rotary control and a few touch keys; (3) calibration is much easier and can generally be done in less than 35 minutes; and (4) because calibration can be done in a rack without removing its covers, the instrument is calibrated in the same thermal environment in which it operates. (In fact, calibration can be accomplished in several different environments; each set of calibration factors can be stored by a controller, and then recalled as needed over the HP-IB interface.)

Automatic setup and range adjustments

The 1980A/B oscilloscope measurement system is most interestingly demonstrated by pressing the AUTOSCOPE key and watching the instrument find a trace (or traces) and automatically display it (or them) on the screen. When the AUTOSCOPE key is pressed, a number of functions is set to predetermined conditions—those that will most likely be required for typical measurements or that will provide the greatest safety as a starting point. For example, ac coupling is selected; trigger slopes are positive; deflection factors are set at 1 V/div; trigger levels, position controls, and delay are all set at a nominal level. This is simply a matter of accessing the state memory and sending the appropriate latch and DAC patterns.

After the presets are accomplished, the microprocessor uses the trigger flag to begin making decisions. First, it searches for proper vertical sensitivity. A typical signal search is a 4-step procedure.

1. The microprocessor searches each vertical range (1 V, 100 mV, 10 mV, 2 mV) until a signal of 1.5 or more divisions is found.

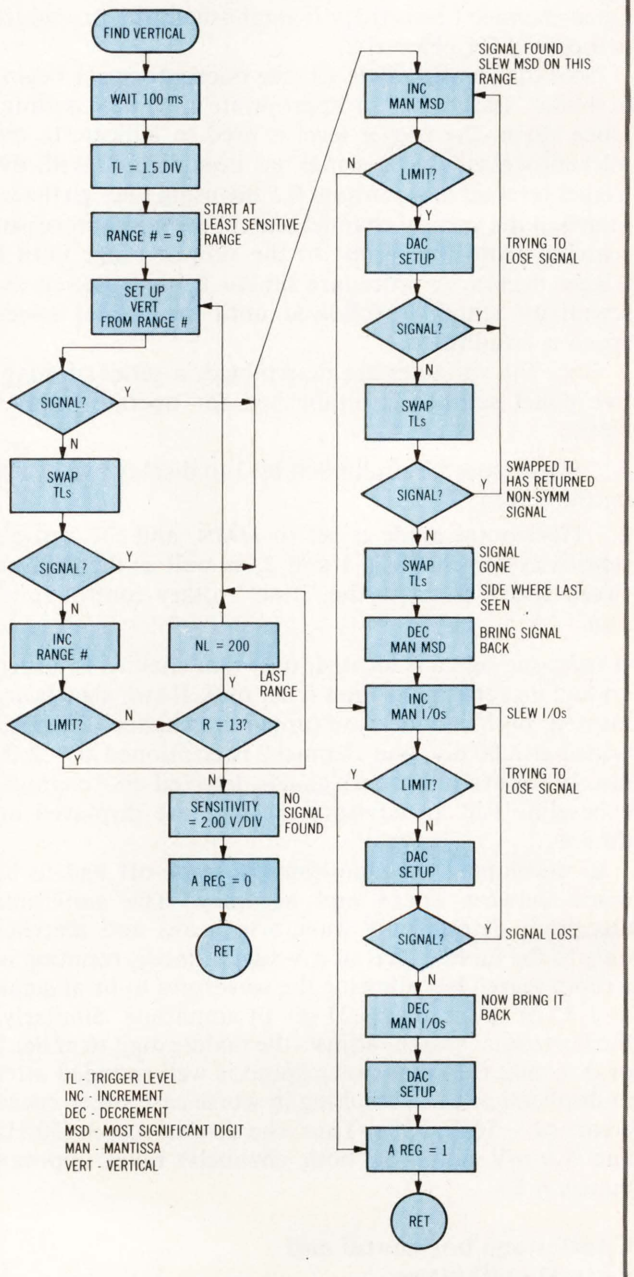


Fig 3 Flowchart for AUTOSCOPE mode. Microprocessor increases sensitivity until trigger flag indicates that trigger is found. Then, it decreases gain until trigger is lost and adjusts gain to restore trigger flag. Trigger sign change during search detects signal with dc component

2. Once a trigger is found, the microprocessor adjusts the most significant digit of the sensitivity value (DAC channel) until the trigger is lost. It readjusts that digit to bring the trigger back.

3. The microprocessor then adjusts the middle digit of the sensitivity value by 1 until the trigger is lost, then readjusts to bring it back.

4. When the trigger is lost in steps 2 and 3, the sign of that trigger is changed and the search continues so that signals with a nonzero dc component can be found.

Fig 3 is a flowchart of the vertical sensitivity search. Once channel 1 sensitivity is established, the procedure is repeated for channel 2.

Now that sensitivity is set, the microprocessor begins a similar search for an appropriate time-base setting. Once again, the trigger level is used to indicate to the microprocessor that a signal has been found. With the trigger level set at a constant 0.5 div using the sign determined in the vertical channel search, the microprocessor searches from the fastest to the slowest range until a trigger occurs. A procedure similar to that used in the sensitivity search is followed until the proper sweep speed is established.

Once the variables are determined, a series of adaptive panel settings is established for operator convenience.

1. Sweep speed is multiplied by 2 to display two cycles on the screen.

2. Horizontal mode is set to MAIN, and the vertical sensitivity for channels 1 and 2, as well as the delayed sweep speed, is set to the "fine" rotary control function.

If only one signal is located, only that channel is turned on and its vertical position is set to 0. If two signals are located, both channels are turned on, channel 1 is positioned at 2.00 div, and channel 2 is positioned at −2.00 div. In the event that no signal is detected on a channel, a baseline and an advisory message are displayed on the CRT.

In developing the algorithms, a trade-off had to be made between speed and accuracy. The amplitude algorithm detects only waveform peaks and searches only to the middle digit of a 3-digit number, resulting in a rapid search but allowing the waveform to be as small as 1.35 or as large as 3.27 div in amplitude. Similarly, the horizontal search, adjusts the middle digit to either 5 or 0 so that the final sweep speed is well rounded after multiplication by 2, resulting in worse case sweep speed errors of −50%, 33%. Thus, the slowest search (50-Hz and 9.9-mV input on both channels) takes approximately 4.5 s.

Continuous horizontal and vertical calibration

An historical limitation of the oscilloscope has been its loss of calibration when making fine adjustments to vertical sensitivity and horizontal sweep speed. Software makes a major contribution in the 1980A/B by providing a practical, cost-effective solution to this problem. This means that vertical deflection can be changed from 2 mV/div to 10 V/div with calibrated measurements at any point along the way, and sweep speeds can be changed from 5 ns/div to 1 s/div. It is by this minimizing of operator error that software contributes not only to measurement convenience but also to measurement confidence.

Using the procedure for maintaining continuous calibration of channel 1 deflection factors as an example, note that the process is a combination of hardware switching, via latches, to set input attenuators for gain to the correct range and to set analog voltage

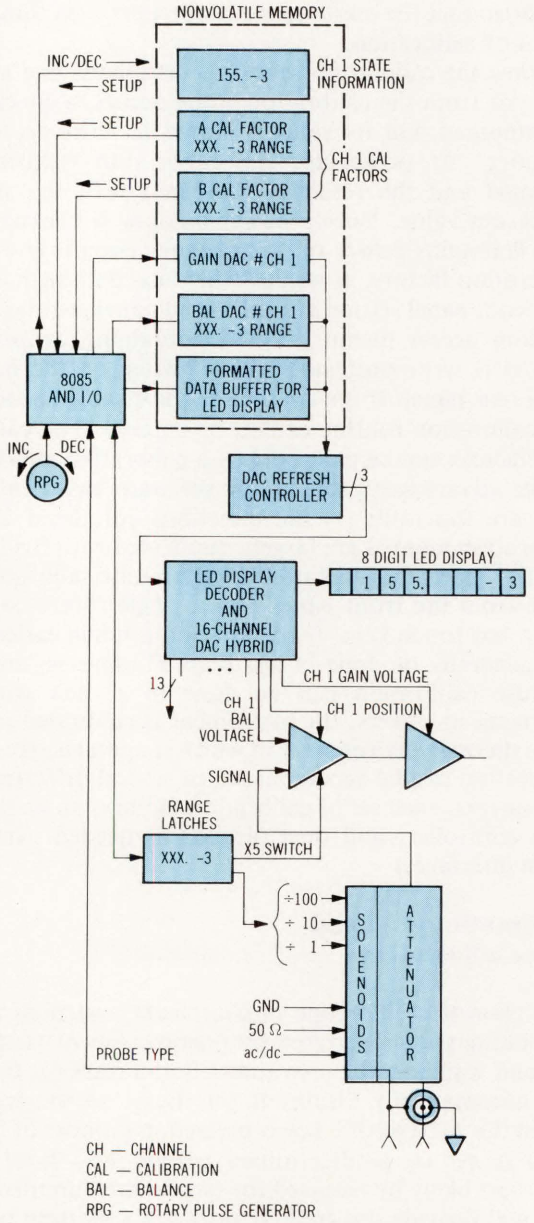


Fig 4 Continuous calibration feature. Combination of logic switching and number changes determines appropriate analog levels for fine gain setting. Once sensitivity is combined with calibration factors and stored, DAC refresh controller takes over and updates DAC channel continuously

outputs of the DAC for vernier gain control. (See Fig 4.) When the rotary control is turned, it increments or decrements channel 1 sensitivity state information in nonvolatile memory. A DAC setup is immediately executed so that the displayed trace amplitude changes in relation to the new state information. The setup program uses the sensitivity value along with two previously determined calibration factors for that particular range. It then combines them in a linear slope-intercept equation and outputs that gain DAC number to memory. The correct balance DAC for channel 1 is also selected and placed in memory. From there, the DAC refresh control circuit automatically applies these numbers to the DAC input, relieving the processor of time consuming fetch and calculation routines. These numbers are the patterns that result in the analog output voltage required to provide the gain and balance control for the channel 1 amplifier.

During the setup routine, the microprocessor also formats and transfers channel 1 state information to the formatted data buffer. The DAC refresh controller then transfers data, from the formatted data buffer, to the LED decoder, which updates the LED display on the front panel. The exponent of the channel 1 state information and probe type also determines the settings of the attenuator latches and the times 5 switchable gain of the channel 1 amplifier.

Because of this continuous calibration, there is now a choice of either setting the sensitivity and sweep speed to a specific value per division or aligning the signal with the CRT graticules and reading voltage or time directly.

Calibrating a hybrid voltage controlled oscillator

Another interesting aspect of its contribution is software's ability to compensate for hardware limitations. For example, oscilloscopes need an accurate time base for delay time interval measurements. The system crystal reference clock provides the necessary overall accuracy (0.003%), but it can't deliver that accuracy directly to the horizontal hybrid (less than ± 1 ns error). Software allows the use of a 10-MHz, restartable, voltage controlled oscillator (VCO) contained on the horizontal hybrid circuit as an accurate delay time base—even though it is subject to some minor drift and instability.

Fig 5 is a block diagram of the delay time circuit, a hybrid scheme that combines counter and ramp techniques. Using the rotary control to select a delay time (from 0 to 9.9999999999 s) places an 11-digit BCD number in nonvolatile memory. The upper 8 digits of delay are loaded into a down counter, while the low 3 digits control a fine delay ramp. The upper 8 digits of the delay count are transmitted serially to the horizontal hybrid over the BCD line; the delay count is buffered on the horizontal hybrid and updated only when a delay count change is made; and the upper 7 digits are transmitted to the BCD counter chip, while the 100-ns digit is transmitted to the horizontal control chip. The last 3 BCD digits of the 11-digit delay time number are translated by firmware to a fine delay DAC number. DAC voltage generated by the 3 fine delay digits is used to control the fine delay ramp on the horizontal hybrid, and fine delay ramp calibration is achieved through a front panel manual calibration routine, similar to the one previously described.

When the main sweep starts, a Horizontal Main Sweep Start (HMST) command is sent to the 10-MHz oscillator on the horizontal control chip. The startable 10-MHz oscillator is used to count down 8 BCD digits on the horizontal hybrid. After the count has been

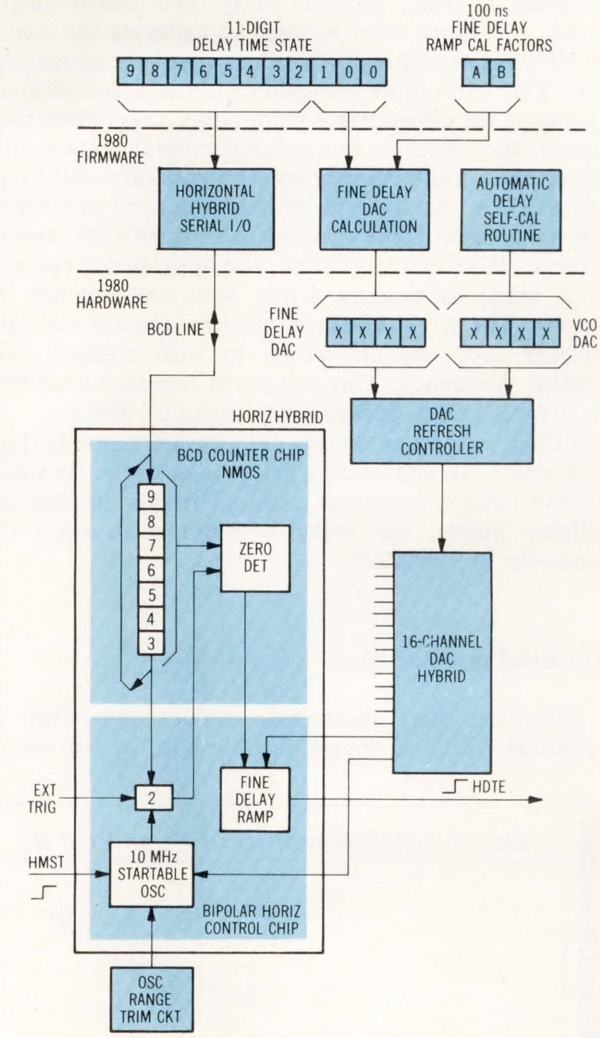


Fig 5 Counter and ramp circuits set delay time. Restartable 10-MHz oscillator provides counter time base. Software calibrates time base to system clock. One DAC channel controls fine delay ramp (0 to 100 ns), with front panel time setting and calibration factors determining DAC number

decremented to 0, the fine delay ramp is started. On completion of the fine delay ramp, a signal is generated to indicate the lapse of delay time (HDTE), arming the delay trigger.

In order to make accurate delay time measurement possible, firmware must be used to calibrate the startable 10-MHz oscillator to the accuracy of the processor clock. This delay time self-calibration is accomplished by pressing the appropriate front panel keys; when this happens, the processor executes a routine that starts the counter and simultaneously enters a software wait loop of 0.199978 s. At the end of that time, the processor reads the counter value and compares it with the crystal reference. If an error is found, the appropriate correction is made by sending a new VCO DAC number to memory. The DAC refresh controller updates the appropriate DAC channel which in turn changes the oscillator frequency. This process is repeated until the VCO is forced to an accuracy of 1 ns in 0.199978 s.

Another advantage of this counter technique is that digital delay, as well as time delay, is possible. By stepping the counter using an external trigger instead of oscillator pulses, the delay becomes a function of events—up to 9,999,999.

Unlimited possibilities

A microcomputer controlled oscilloscope with a 16-channel DAC and trigger feedback to the processor provides abundant possibilities for improved measurement features. Routines that have been developed include automatic preamp balance which, on command, automatically determines the DAC number required to provide the offset, resulting in 0 trace shift with gain change. To the operator, it means elimination of trace shift as sensitivity is varied. Also, front panel interlocks that turn off lamps and lock out keys have no effect on the trace being viewed, thus reducing operator confusion.

The list of possibilities also includes change in time (Δt) and change in voltage (ΔV) measurements provided by previous microprocessor controlled oscilloscopes such as the HP 1722A, as well as measurement capability and user convenience. For example, the bank of keys to the left of the 1980A/B's CRT is defined by firmware. Called "soft keys," their functions change depending upon the operation being performed (self-test, calibration, installed options, and more), and are identified by characters on the CRT. In addition, eight complete front panel setups can be saved and recalled by two keystrokes or a single computer command. A full-screen character generator permits user instruction under computer control, advisory messages, and instrument status information.

Even though the 1980A/B has a large number of built-in features that are the result of software, there is room for the imaginative software designer to create additional features. Because of the availability of ROM plug-in sockets and computer control via HP-IB, programmers can develop software to custom tailor instrument operation to particular measurement needs.

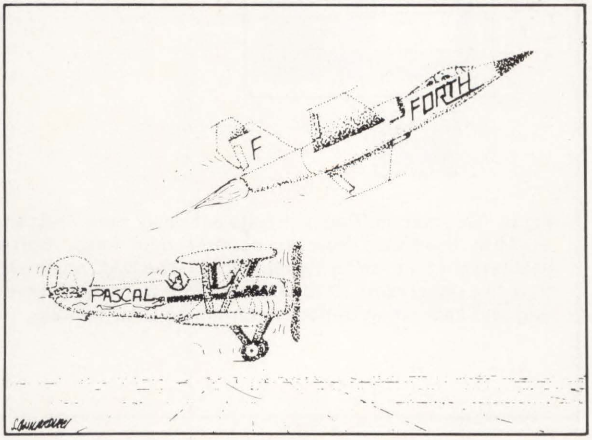
About the Authors:

Paul Austgen has worked at Hewlett-Packard as a production and a systems engineer. Upon joining the Research and Development Laboratory, he wrote one-third of the 1980 software, including AUTOSCOPE and the calibration systems. In 1979, he became project manager of all 1980 software and system enhancements. He has a BSEE in communications and an MSEE in automatic control theory from the University of Colorado at Boulder.

Bill Watry, a project engineer with the Research and Development Laboratory, has written one-third of the 1980 software, including the system expansion capabilities and the routines that interface the keyboard and rotary control, and has recently assumed the technical supervision of a laboratory group that will develop 1980 applications software. He received a BSEE in computer science from the University of Colorado at Colorado Springs.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" box on the Inquiry Card.

High 734 **Average 735** **Low 736**



THE STD BUS PEOPLE.

INTERSIL'S SYSTEMS DIVISION ANNOUNCES A SPECTRUM OF STD BUS CARDS — OFF THE SHELF.

From the people whose total systems shipments to date have exceeded seven *billion* bytes of memory. The same people who've made a reputation in ultra-reliable cards and systems over the last ten years: Intersil's Systems Division.

Now introducing a broad new spectrum of STD BUS products. All available right now. And all *truly* STD BUS compatible. So you can mix and match cards with no surprises.

Plus, you can have your choice of microprocessors: 8085 or Z80. Either way, you get total compatibility throughout the family.

Z80 CPU Card (ISB-3100)
8085 CPU Card (ISB-3110)
16K x 8 CMOS Memory Card (ISB-3216)
Parallel Input Card (ISB-3310)
Parallel Output Card (ISB-3320)
Floppy Disk Control Card (ISB-3400)
Triac Output Card (ISB-3500)
Opto-isolated Input Card (ISB-3510)
Reed Relay Output Card (ISB-3520)
Hardware Arithmetic Card (ISB-3600)
Sync/Async Communications Card (ISB-3700)

AND A SPECTRUM OF SOFTWARE PRODUCTS — OFF THE SHELF.

No, we didn't forget software. And we didn't forget that you need it *now.* Everything from DOS to PASCAL — off the shelf.

CP/M® Disk Operating System (ICP/M)
  including text editor, assembler, debug, and disk and terminal I/O handlers
Macro Assembler (IMAC)
FORTRAN Compiler and Library (IFORT)
BASIC Compiler (IBASC)
BASIC Interpreter (IBASI)
PASCAL Compiler (IPASC)
Firmware Monitor (IFMON)

® Trademark of Digital Research, Inc.

CIRCLE 61 ON INQUIRY CARD

DEVELOPMENT SYSTEMS AND MUCH MORE — VERY SOON.

We're not stopping now. Because we're committed to having the biggest and best line of STD BUS cards in the business.

So in the very near future we'll be announcing a number of major additions to the family. Including parallel I/O, A/D and D/A cards. A PROM-burner card. A bit-oriented dual-channel synchronous communications card. A remote data acquisition controller card. Three new memory cards and more.

On the software side, we'll be introducing a firmware development system, including monitor, assembler and editor, PROM-burning software and multitasking control monitor.

And tying it all together there'll be a start-up designer's kit — plus a full-fledged STD BUS development system. So stay close and watch for more good news.

AVAILABILITY: NOW. PRICING: GREAT!

Like we said, our stock is on the shelf. You can call and check that out.

And our pricing? Competitive. Very competitive.

CALL OUR HOT LINE: (408) 743-4442.

That's the number to call. To place an order or to get a full packet of our STD BUS literature super fast. Or call any one of our distributors directly: Anthem, Arrow, R.A.E. Industrial Electronics Ltd., or Zentronics.

Or simply send in the coupon — to the STD BUS People: Intersil Systems Division.

INTERSIL
SYSTEMS DIVISION
Marketing Department, 1275 Hammerwood Ave., Sunnyvale, CA 94086
Tel: (408) 743-4300 or Hot Line: (408) 743-4442.

Please tell me more!

___ISB-3100
___ISB-3110
___ISB-3216
___ISB-3310
___ISB-3320
___ISB-3400
___ISB-3500
___ISB-3510
___ISB-3520
___ISB-3600
___ISB-3700

Name/Title ________________

Company ________________

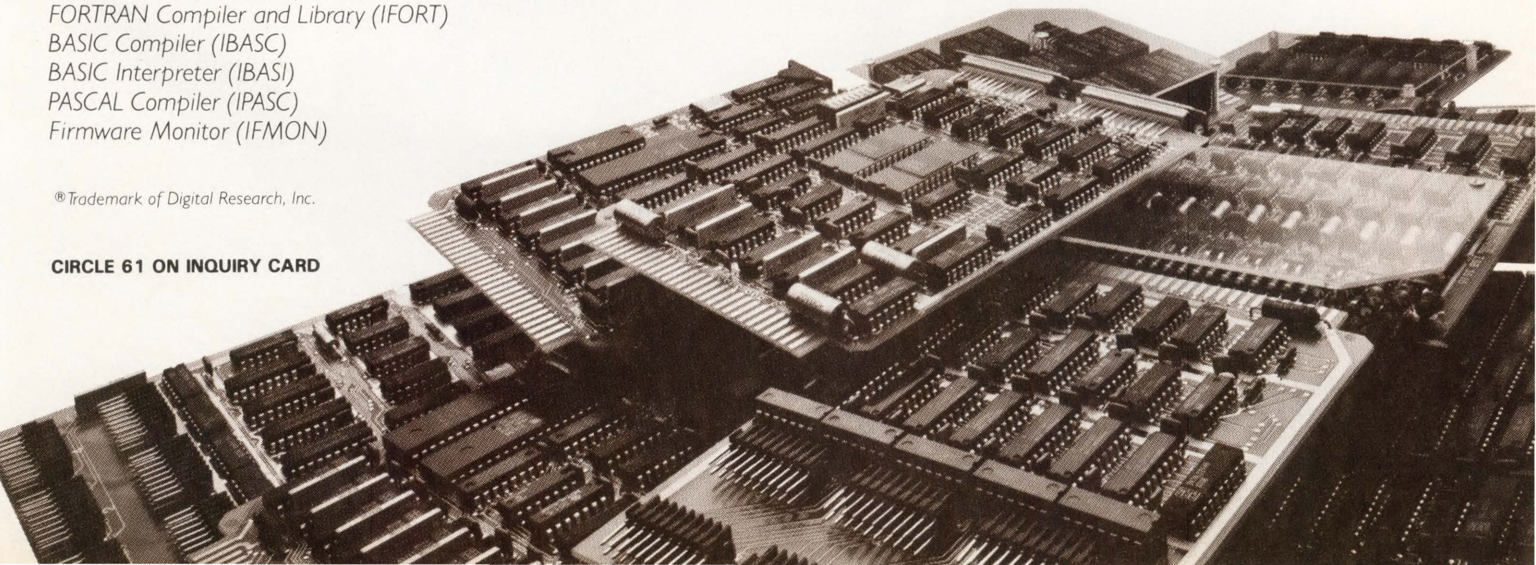
Address ________________

City/State/Zip ________________

Phone ________________

My program started/will start ________________
I anticipate an annual usage of __________ cards.

CD681



Valedictorian of the Smart Editing Class of Terminals.

Compare the new VISUAL 400 with the other smart terminals. Then compare it to your own specification. And if that doesn't do it, we have "Room for RAM" for custom modifications in large quantities.

For a pleasant surprise on pricing, call or write us today.

FEATURE COMPARISON CHART

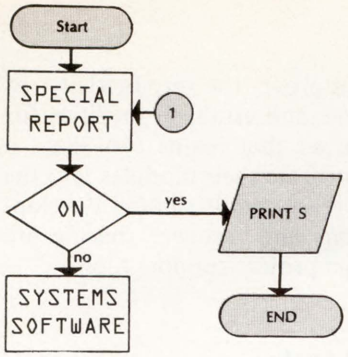
FEATURE	Visual 400	Lear Seigler ADM-42	Perkin Elmer 1251	ADDS Regent 60	Hazeltine Executive 80, Model 30	Beehive DM30
ANSI X3.64 Specified	STD	**NO**	**NO**	**NO**	STD	**NO**
Set-up Modes Eliminate External Switches	STD	**NO**	STD	**NO**	**NO**	**NO**
Typomatic Solid State Keyboard	STD	**NO**	**NO**	**NO**	STD	**NO**
Detached Keyboard	STD	STD	**OPT**	**NO**	STD	STD
CRT Saver	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Block or Underline Cursor	STD	**NO**	STD	STD	STD	**NO**
80 and 132 Columns	STD	**NO**	**NO**	**NO**	**OPT**	**NO**
Double Size Characters	STD	**NO**	**NO**	**NO**	**OPT**	**NO**
Smooth Scrolling	STD	**NO**	**NO**	**NO**	**OPT**	**NO**
Horizontal Split Screen	STD	**NO**	**NO**	**NO**	STD	**NO**
Video Attributes Require No Display Space	STD	**NO**	**NO**	**NO**	STD	STD
8 Area Qualifications	STD	**NO**	**NO**	**NO**	**NO**	**NO**
8 Resident Nat'l Char. Sets Including Line Drawing	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Programmable Non-volatile Function Keys	STD	**OPT**	STD	**NO**	**NO**	**NO**
Display of ALL Control Codes	STD	STD	STD	STD	**NO**	STD
Insert Delete Line with Push Up or Down	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Insert Delete Character with Push Right or Left	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Select Editing Extent to Field, Area, Line, Page	STD	**NO**	**NO**	**NO**	**NO**	**NO**
20 mA Current Loop	STD	STD	**OPT**	**OPT**	**OPT**	STD
Programmable Message Framing (non-volatile)	STD	**NO**	STD	**NO**	**NO**	**NO**
Programmable Answerback	STD	**NO**	STD	**NO**	**NO**	**NO**
Baud Rates to 19200 BPS	STD	**NO**	**NO**	**NO**	STD	STD
Independent Xmit/Receive Rates	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Printer Port Independent of Communication Interface	**OPT**	**OPT**	STD	STD	**OPT**	STD
Paging	**OPT**	STD	**NO**	**NO**	STD	STD

VISUAL 400

VISUAL See for yourself

Visual Technology Incorporated
540 Main Street, Tewksbury, MA 01876
Telephone (617) 851-5000, Telex 951-539

CIRCLE 62 ON INQUIRY CARD



Modern, software intensive 16-bit product development places added demands on development tools to improve programmer productivity

The impact of 16-bit microprocessors on software development tools

High performance 8- and 16-bit microprocessors are sparking developments in the design of microprocessor based products. Increased function, performance, and flexibility of these new processors have changed the nature of microprocessor applications from small, controller type designs to more complex multitasking systems. Average program size in microprocessor applications has grown from 10k to 20k bytes in the 8-bit environment to more than 64k bytes using 16-bit processors. With this increase in program size has come a change in the development process. Not only has overall development time increased, but the relative proportion of time spent on hardware and software designs has shifted. In the past, about 50% of the design effort was devoted to software development, 35% to hardware design, and 15% to hardware/software integration. This ratio has shifted dramatically toward software in the 16-bit environment. Today, 16-bit designers devote up to 90% of their effort to software development.

Modern 16-bit development is software intensive, and has created demands for development tools that improve software productivity. Availability of high level programming languages establishes one key criterion for designers to evaluate potential microprocessors and their development support systems. Efficient and easy to use text editors assume greater importance as the quantity of software increases. Off the shelf, reconfigurable operating systems also are important tools for increasing programmer productivity. In addition, greater emphasis is now placed on software debugging aids.

Because new microprocessor technology is being introduced rapidly, another important consideration is the ease of migrating from previous 8-bit designs to designs based on new 16-bit processors. The ability to upgrade any portion of an existing 8-bit program to run on a 16-bit processor can yield significant cost savings. Moreover, the ability to use or upgrade an existing development system for use with a new processor can protect a sizable investment in software development tools.

Increased size and complexity of 16-bit applications lead to a corresponding increase in the number of programmers working together on a project. The task of managing the output of a large programming team poses challenges in many 16-bit design efforts. When the programming task is subdivided among team members—as is often the case—consistent interfaces must be defined and closely coordinated. Various schedules must be coordinated also. By some estimates, up to 20% of the software development effort in large projects is spent on software project management. Development

Mary Jane Elmore, David Miller, and Jim Schwabe
Intel Corporation
3200 Lakeside Dr, Santa Clara, CA 95051

tools, therefore, must improve the productivity of multiple-programmer teams and establish facilities for programmer coordination so that teams can share a software data base and integrate their modules into the final product. For these reasons, distributed development system configurations and resource sharing are important features of large project support tools.

Selecting development tools

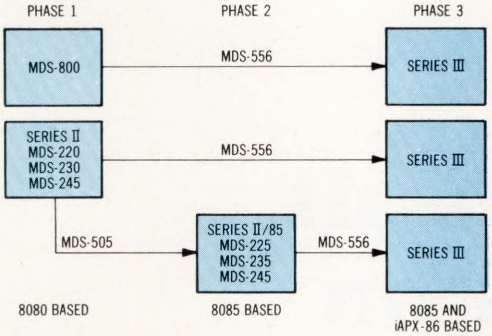
When choosing development tools to meet the changing needs of microprocessor system designers, selection criteria can be confusing. In the final analysis, the best development tools are those that provide the shortest route to a finished product at the lowest cost. The program development cycle typically includes source code preparation, translation of source to object code, software debugging, and integration of hardware with software. An effective development system will support specialized tools tailored to each step of this development cycle.

Source program text can be viewed as a programmer's primary output; a powerful and sophisticated text editor is the basic tool for creating, manipulating, and refining this output. Advanced, cathode ray tube (CRT) based text editors speed source program preparation and revision. The most efficient text editors provide two distinct modes of operation: text mode and command mode. Text mode makes full use of the CRT display with its movable cursor, insertion or overstrike capability, and versatile deletion modes. Text appears on the screen exactly as it has been stored in memory. Modifications are made by positioning the cursor on characters to be changed and using delete, insert, and overstrike capabilities to accomplish the change.

Command mode implements powerful text editing primitives—basic utility operations such as character string search, change or replacement, and formatting. Whereas text mode commands are at most single keystrokes, command mode functions accept text strings as command arguments, performing useful operations that involve these arguments and their relationship to the surrounding text. Although any editing function can be performed using only text mode, command mode operations are much more convenient for entering complicated iterative changes.

Complex, software intensive 8- and 16-bit microprocessor applications underscore the demand for a repertoire of compatible programming languages that will allow programmers to select the language whose characteristics best fit a specific application. When program size or execution speed is more important than software development efficiency, assembly language is required. On the other hand, when programmer productivity in writing, debugging, and maintaining software is the primary concern, high level languages are preferred—even though they tend to be less efficient in execution speed and use of program storage than assembly language. The best approach to this critical tradeoff combines an assembler and one or more high level language compilers that produce compatible object code. Then, assembly language modules and modules

Development System Offers Easy Upgrade Path



Convenient upgrade path. Series III preserves development system investment by providing upgrade path from any previous Intellec development system

The series III is a complete, standalone development system based on Intel's 16-bit iAPX-86 processor. It can provide overall productivity gains over previous systems, especially for designers of iAPX-86 and -88 based applications. Use of the iAPX-86 increases throughput and also provides a resident execution environment for iAPX-86 and -88 programs. Its maximum 1M-byte address range extends potential storage for symbol tables and user programs, and allows high level language compilers to run faster than in 64k memory systems. Built around two host processors—the iAPX-86 and the 8085A—the series III is not confined to iAPX-86 and -88 applications. Its 8085A host provides a resident execution environment for 8-bit applications and language translators. In series III 8-bit compatibility mode, all software written on or for 8-bit series II and model 800 development systems will run without modification.

One upgrade package converts any existing Intellec development system—whether model 800, series II, or series II/85—into a series III system. (See the Figure.) The upgrade package consists of an iAPX-86 processor board, 64k additional memory, and the Intellec software required for an iAPX environment. Insertion of boards into available slots and loading of software complete the upgrade; development software that is executed on the series II, series II/85, or model 800 still runs on the 8-bit processor board, and software developed under these systems is now upward compatible with programs developed on the series III.

compiled from one or more high level languages can be linked together in the final program. Different program modules can be implemented, each in the language best suited to the task performed.

Modern 8- and 16-bit microprocessor system designs often require operating system software. Operating system design and development can consume many years of effort and tie up considerable inhouse expertise. By offering customizable operating systems, suppliers help to free designers from the tasks of writing and debugging their own system software. Productive development efforts can then be focused on actual applications.

Microprocessor based applications often require specialized tools for software debugging and system integration; a well-planned development system should support a variety of debugging tools. For example, in-circuit emulators allow hardware and software development to proceed concurrently and interactively, thereby making the traditional system integration method of independent hardware and software development obsolete. With in-circuit emulators, prototype hardware can be added to the system as it is designed. Then, software and hardware testing begins at an especially early stage and continues throughout the product development cycle.

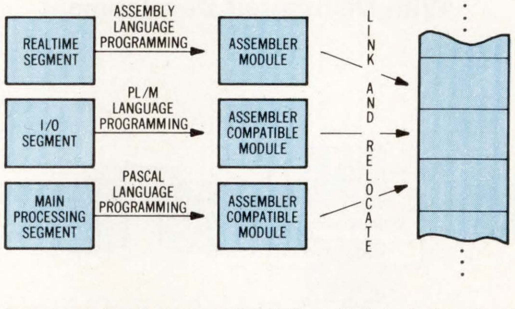
A software debugging program allows controlled execution of prototype software by implementing such features as single-step execution, setting and removing breakpoints, and examination of registers or memory locations. For maximum utility, a debugging program should be tightly integrated into the total software development package. The close working relationship among text editor, language processors, and debugging program reflects the intimate relationship among source code generation, conversion of source code to object code, and object code debugging.

Upgrading to next generation processors

To provide maximum flexibility, a development system should support a spectrum of microprocessors and single-board computers with a wide range of functional capabilities. These features reduce start-up costs for each new design and facilitate moving to the next generation product in a microprocessor family. Many microprocessor applications today are based on mid-range 8-bit processors, such as the 8080 and 8085. As these products approach the limit of 8-bit processor performance, designers may want to move up to the higher performance 16-bit processors. On the other hand, designers seeking cost optimization may want to move down to single-chip processors such as the 8051.

A development system that supports a complete spectrum of microprocessors makes it easy to migrate in either direction. Using a modular approach, migration is achieved simply by selecting the languages and in-circuit emulator that are appropriate for the chosen processor. As processor needs change, the same development system can be used with new languages and different debugging program modules. Of course, complete high level language support for a broad range of processors guarantees that preexisting program code can be moved onto the next generation processor with minimum modification.

High Level Language Produces Assembler Compatible Code



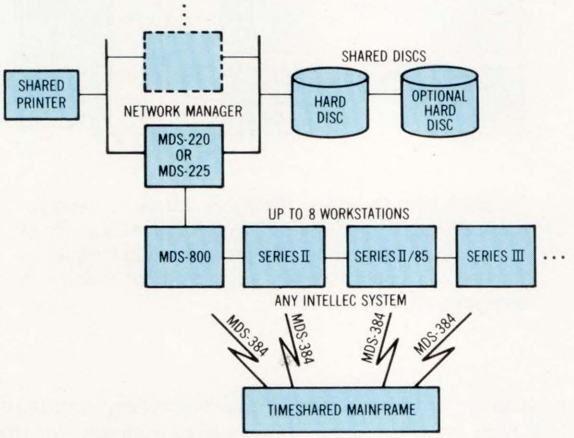
Programming language flexibility. Efficient development of microcomputer software requires variety of compatible and combinable programming languages that allows users to code each program module in best language for its task

PL/M-86/88, Intel's system implementation language, is a high level language designed specifically for the special requirements of microcomputers. Providing high level access to the microprocessor hardware—and, thus, control over the processor and its peripheral components—it also offers such high level language advantages as the ability to write programs using statements very similar to English language statements; structured programming constructs that can lead to more efficient software design; and the potential for easier debugging and maintenance.

PL/M supports machine features such as absolute addressing, interrupt handling, and direct port input/output (I/O). Its built-in procedures allow access to stack pointer and central processor status register values. Use of pointer variables and "based" variables provides a flexible means of manipulating data and addresses stored as data. In combination, these features allow programmers to interface directly with system hardware, without requiring run-time support modules. New for the series III is a high speed syntax checking option that flags source program syntax errors without incurring the added delay of object code generation.

Pascal has generated considerable interest because it is a high level language that enforces good programming techniques and produces uncommonly portable programs. The series III was the first development system to support a 16-bit Pascal compiler. Pascal 86/88 conforms to proposed standards and also incorporates extensions tailored to a microprocessor environment such as interrupt handling, direct I/O, and separate compilation capabilities. All extensions can be flagged at compile time to help maintain portability. As with PL/M-86/88, the Pascal compiler produces object code that is fully compatible with assembly language. (See the Figure.)

System Combines Resource Sharing With Distributed Development



Network development system. Up to 8 workstations share hard disc and printer resources. Any Intellec development system can be converted into workstation by adding interconnection board, cable, and software. Distributed development environment significantly increases programmer productivity and system performance over standalone development systems

Designed to address the problems of managing large software development projects, the network development system (NDS-I) connects as many as eight Intellec development systems, each as a separate workstation, in a multi-user environment. (See the Figure.) At the center of NDS-I, a network manager coordinates workstation activity by managing file access, handling the shared disc data base, and controlling requests for the shared printer. The common disc storage pool consists of one or two hard disc subsystems, each with 7.5M bytes of storage on two discs—one fixed and one removable—to allow simple and efficient disc backup.

A particularly effective development environment can be established by distributing the development cycle over several different types of workstations. For example, source file editing and program module debugging can be performed on workstations consisting of series II development systems or model 800s. Then, series III workstations with their high performance iAPX host processors can be used for all program compilations.

Simplifying management tasks

All software development projects, large and small, require traditional, specialized, microcomputer development tools that are usually available only on standalone development systems. Specialized tools include assemblers, compilers, relocation and linkage facilities, and in-circuit emulators. Additionally, large undertakings require project management facilities such as file handling and shared file access, documentation facilities, and program source control. Tools of this type are available on most mainframe computers.

One way to bring project management facilities to microcomputer software development projects is to integrate microcomputer development systems with mainframes. By combining these two resources, a project can benefit from specialized workstations that are custom tailored to the range of activities involved. For instance, a mainframe could be used both for source entry, to capitalize on the availability of multiple CRTs, and for project management, to profit from specialized management tools available on the mainframe. Development system workstations that take full advantage of their range of specialized compilers and in-circuit emulators result in low cost, highly effective, hybrid systems for all phases of development from system design through product verification and test.

Programmers typically begin by entering a source file through a CRT terminal, using the mainframe text editor and file system. The file is stored on the mainframe, allowing full use of mainframe file sharing, protection, and backup facilities. For compilation, assembly, and linking, the file is sent down the mainframe link to a development system workstation. After performing these operations, the development system sends listing and object code files back to the mainframe for backup storage. High speed line printers attached to the mainframe produce the hardcopy listing.

If source modifications are required at this stage, they can be entered at a CRT terminal; otherwise, the linked and relocated object file can be downloaded to another development system for debugging in conjunction with an in-circuit emulator. This configuration distributes the development cycle over several specialized systems and, therefore, combines in-depth support for a wide range of processors of a microprocessor development system with the sophisticated project management facilities of a mainframe computer. Such mainframe assisted development configurations, however, are not without their drawbacks: mainframe equipment is costly; effective communication between mainframe and development system for maximum system performance is a significant problem; and timeshared access to the common mainframe resource can create throughput bottlenecks.

Network development system

Spurred by the rapid decrease in microprocessor cost, distributed data processing has begun to supplant conventional timesharing in many application areas, and software development is no exception. As currently provided by development system suppliers, the network development system provides project management functions pertinent to microcomputer development without the added cost and system complexity of mainframe computers.

At the center of a development system network, a "network manager" coordinates activities of the development systems that are tied in as workstations, manages file access to a pool of shared disc units, and handles requests for the shared hardcopy printer. Ideally, shared disc storage at the central node consists of at least two hard disc subsystems, allowing simple and effective disc backup. Data should be transferred between workstations and the network manager at a rate high enough to minimize degradation when compared to a dedicated disc environment. With this configuration, the increased performance and storage capacity of the hard disc, as well as the increased flexibility of a hardcopy printer, can be shared by all of the workstations—along with their increased cost.

Network development system users must be able to declare their files as either public or private. Through a log-on procedure, each user is identified to the network manager and allowed access to the common disc storage pool. Identification codes give exclusive access to private files and shared access to public files; public files should be write-protected to ensure file integrity. Utility programs can be provided to convert between public and private file status. Individual programmers can create and revise program modules in a private workspace with guaranteed file protection. After modules are written, debugged, and tested, they can be converted to public status for integration and testing with other software modules developed by other programmers.

In some cases, software development projects are not growing larger, but more numerous. By assigning each project one or more private workspaces and performing all project development within these dedicated workspaces, many small development projects can be managed in much the same way as one very large effort. Commonly used utilities and shared software libraries can be made accessible to all projects as public files to eliminate the need for redundant files in each project workspace.

In developing a large software project—or a large number of software projects—communication among programmers is the key to productivity. Development system networks facilitate communication by allowing many programmers at individual workstations to access shared files maintained by the central file manager. Typically, a large software task must be broken up and allocated among programmers whose biggest challenge lies in interfacing individual modules to form the final program. Development system networks ease this task by allowing programmers to access one another's files in a controlled environment. Small software tasks can be handled by an individual programmer, but many such small projects present the challenge of maintaining separate software data bases. Development system networks address this problem by segmenting the software data base into separate, individual regions and allowing all programmers to access one shared, common region.

Conclusion

Designing with the latest microprocessor technology requires development systems that will give designers the opportunity to best use the microprocessor. The increased software orientation of today's applications demands development systems that provide a repertoire of compatible programming languages as well as off the shelf configurable operating systems. Development system configurations that support large project design and facilitate multiprogrammer communication must be exploited. Finally, development systems should provide an easy upgrade path that will allow both today's and tomorrow's processors to take advantage of past efforts.

About the Authors:

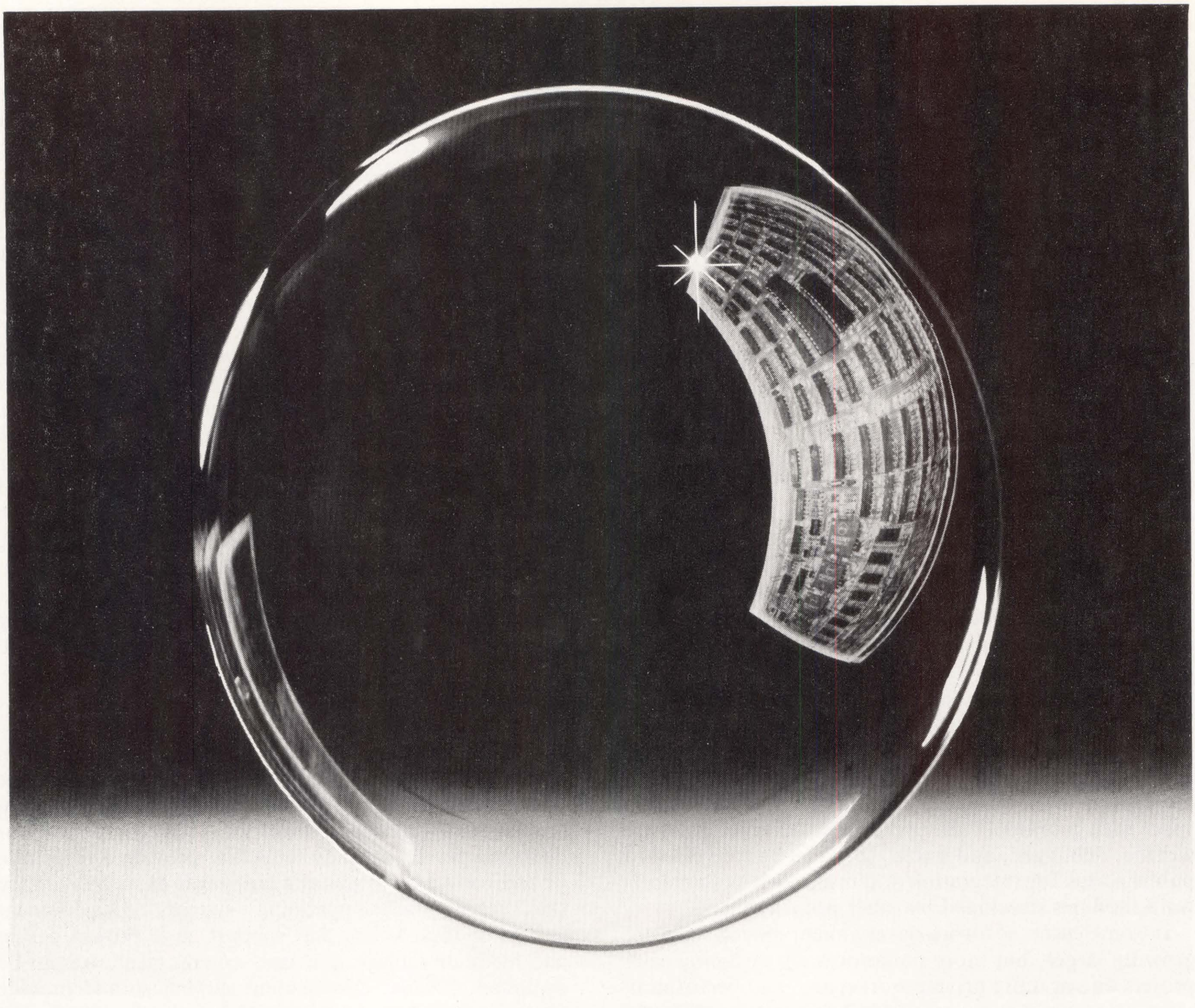
A software product manager at Intel Corporation, Mary Jane Elmore has spent the last three years at the company in technical marketing and software product management. The author has a BS in mathematics from Purdue University and is interested in microcomputer languages, utilities, and operating systems.

For the past five years, David Miller has worked on Intellec development systems as a product manager at Intel Corporation. He is a graduate of the EPFL in Lausanne, Switzerland, with a BS in electrical engineering.

Jim Schwabe holds a BS degree in mathematics from Dickinson College and an MBA from the University of Chicago. He has spent the last two years at Intel Corporation as a product manager for the NDS-I project.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 737 **Average 738** **Low 739**



Plessey customized bubble systems for commercial or military nonvolatile storage.

When it comes to field-proven, economic magnetic-bubble memory systems, Plessey Microsystems has the capability and marketplace experience that you need.

If you are looking for high performance compact memory, for industrial, commercial and warfare conditions, you need to speak with Plessey.

Multisourced, faster and more reliable than disk or cassette—and using less power—the Plessey solution could be just the one to give your memory a jog.

Possibly one of our industry standard 256-kilobyte off-the-shelf systems will just as perfectly suit your needs, so let's talk specs.

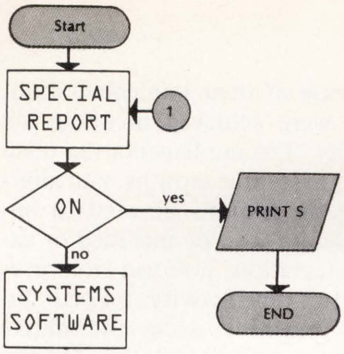
Wherever rugged maintenance-free nonvolatile storage is required, whether it's for computerized numerical control, data logging, or program loading, call Plessey Microsystems. First.

PLESSEY
MICROSYSTEMS

Plessey Microsystems Inc,
19546 Clubhouse Road,
Gaithersburg, Maryland 20760.
Telephone: (301) 948 2791. TWX: 710 828 9708
and at 1641 Kaiser Avenue, Irvine, California 92714.
TWX: 910 595 1930.

Plessey Microsystems Limited,
Water Lane, Towcester, Northants, England, NN12 7JN.
Telephone: Towcester (0327) 50312. Telex: 31628.

CIRCLE 63 ON INQUIRY CARD



Extreme efficiency and transportability to new hardware make this language a natural choice for general purpose microprocessor programming

Forth – the language of machine independence

The most conservative statement that can be made about the current, rapid evolution in the electronics industry is that the evolution will continue unabated into the foreseeable future. This is particularly true in the microprocessor field, with quantum jumps in processing power occurring every three or four years. What does this mean to the maker of intelligent instruments or the manufacturer of small business or word processing systems? Does it indicate that the redesign of a device and the production of new models must be done with the same rapidity as the development of microprocessors? A manufacturer who takes a technological back seat risks being outflanked by competitors' entries. The question answered here is: How can the impact of microprocessor introductions be mitigated without risking technological obsolescence? The most obvious answer is to design instruments and systems to be processor independent.

Processor independence has many facets, such as the use of high level languages, standardized bus architectures, and standardized protocols for communication with peripheral controllers. High level languages were originally intended to increase programmer productivity by freeing them from the bookkeeping tasks associated with assembly language programming. It was soon learned that FORTRAN programs for one machine could run on other machines with only moderate modification. Naturally the new machine had to have a FORTRAN environment. Later, this compatibility between machines was enhanced by the development of the ANSI standard for FORTRAN IV.

More recently, Pascal and Ada have been touted for their machine independence. Pascal currently suffers from a proliferation of dialects problem, although one dialect, UCSD Pascal, dominates. A standardization effort had commenced to resolve this proliferation problem. If efficiency is not a major consideration, a P-code interpretive version of Pascal can be brought up on new hardware in a matter of a few months. Ada, developed for the Department of Defense, has aroused a great deal of interest outside that agency. So far, Ada seems too large a language to be suitable for current microprocessors other than the iAPX-432. Until an officially sanctioned subset is defined, Ada is not likely to sweep the field with implementations on a large variety of microprocessors.

Other forms of machine independence, such as the use of a standard bus (eg, IEEE-696), afford the user the opportunity to change processors without changing the rest of the system circuitry. However, the added features or the maximum speed of the new processor may not be available if the selected bus architecture does not handle them. To further complicate matters, there is no guarantee that a peripheral controller manufactured by company X will communicate with a processor card made by company Y, even though they both meet the

Gary Feierbach
Inner Access Corporation
3206 E Laurel Creek Rd, Belmont, CA 94002

same bus specifications. Currently, either a driver must be written for the company X product, which is then incorporated into the operating system for the company Y processor, or company X emulates a product already incorporated into company Y's operating system. If peripheral protocols were standardized, a third aspect of machine independence would be achieved.

Who will benefit?

There is a tendency to think of a more advanced processor as one that executes more instructions per second or one that has a larger instruction set or address space. A new breed of microprocessors with very reasonable amounts of integral read only memory (ROM) and random access memory (RAM) is now emerging, eg, the Zilog Z8. These processors are large enough to support a high level language and will allow more compact instruments or systems. This means that the evolution of microprocessors, as well as those devices that use microprocessors, is likely to develop into families of devices of varying capability and cost. A high level language can provide a common base for these families by allowing the same development tools, the same programming staff, and even perhaps identical versions of the same programs to be used with a family of products.

Beneficiaries of machine independence include more than the manufacturer who is able to introduce a new or improved product sooner. They also include system houses that can transfer their value added software to new hardware with relative ease. Many instrument manufacturers and commercial system vendors have vast libraries of application software for their machines, representing a considerable investment of time and money that should be machine independent. More often than not it is written in native machine code for efficiency considerations. This establishes the need for a language that is not only easy to bring up on new hardware but is efficient in terms of execution speed and memory utilization. Forth is such a language.

Forth and machine independence

Forth was invented by Charles Moore about eleven years ago to fill a need, as he saw it, for a programmer amplifier. In short, he wanted to be a more productive programmer,[1,2] and felt he could be if a language were developed that, by the natural act of programming, would *extend* itself *toward* the application. In this way, at the highest level, a programmer could write statements like `TURN LIGHT ON` or `ROTATE RIGHT 20.05 DEGREES`, and these events would occur. In its first three years, Forth was used almost exclusively in the field of radio astronomy. Later Charles Moore started his own company to support a growing community of users. Widespread use did not begin, however, until 1978 when the Forth Interest Group (FIG) published a number of implementations on mini- and microcomputers. The language is now in the public domain and an international standard was developed in 1979 with nearly unanimous consensus from all segments of the Forth community.[3]

As a testimony to the ease of their implementation, the FIG implementations were achieved in about six months of part-time activity. The implementation team met every Saturday for the first three months, and alternate Saturdays thereafter, in sessions devoted to implementation details and features to be included or excluded to make the implementations uniform from processor to processor. As a full-time activity, a Forth implementation on a new machine using the native assembler generally takes at most two months. The use of a meta-compiler can cut this to one month or less with the side benefit of a native code assembler written in Forth.

Forth's virtues

The virtues of Forth as a machine independent language surpass its ease of implementation and standardization. Most versions of Forth are both memory and execution speed efficient, using about 4k bytes of storage and 20% to 50% of the execution overhead for the inner interpreter. The language is structured, ie, there is no GO TO statement, and enforces top-down design and modularization as does no other; therefore, it is difficult to program in Forth in an undisciplined manner.

Extensibility is the language's most compelling virtue. Every compiled statement in Forth defines a new word that may be used in the statement's stead. This is the key reason for its compactness and accounts for its chameleon-like ability to *become* the language of the application. Unlike subroutine calls in other languages, the Forth word is evoked by only one word in the calling program, and parameters are passed on a stack. No other syntactic or semantic overhead is involved.

Forth's drawbacks

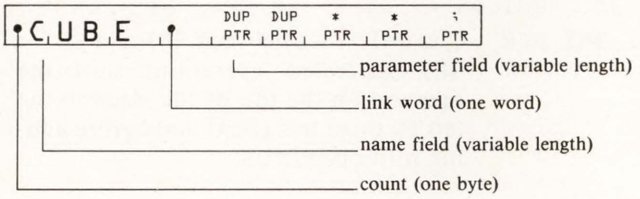
In some ways Forth's most notable virtue is also its Achilles' heel since it allows programmers to be as cryptic as they wish. This spells a need for rigidly enforced documentation standards and a dedication to clarity. On this same note, Forth lacks standardized data structures, so each programmer ends up implementing his own. This is not a problem from the point of view of machine independence, since the data structures are generally implemented in high level Forth; it is a problem in intelligibility. Standardized ways for implementing commonly used data structures will emerge with time.

Another important aspect of Forth is the institutionalization of change in the form of a group called the Forth Modification Laboratory (FORML). This group ensures that the language will continue to evolve with new extensions, which, after extensive testing in the user community, may eventually become standard. The Forth 79 standard has no floating point operations although several floating point implementations are in the public domain. There is general agreement that the floating point implementations should eventually be in compliance with the IEEE-754 floating point standard.[4] None currently are.

It has been argued that Forth is a difficult language to learn. To a certain extent, this is true. It is not a language amenable to the stream of consciousness coding that some programmers do in BASIC. Other programmers have learned not to be modular in FORTRAN because of the subroutine linkage overhead on a particular vendor's hardware. Still other programmers are entrenched in infix notation, ie, ordinary arithmetic expressions using parentheses, and find it difficult to learn to use postfix notation (reverse Polish). Nonprogrammers, however, find Forth not much more difficult to learn than BASIC, up to a point. Beyond that point there are some advanced concepts that are difficult to understand, including the meta-defining words that add a powerful dimension to the language but are not necessary in ordinary applications. As the teaching of Forth is still in the developmental stages, only a few good texts and manuals have emerged.[5]

The dictionary, inner interpreter, and outer interpreter

Internally, a compiled Forth program looks much like a dictionary. Each entry contains a header that represents the defined word and is followed by its definition, either in machine code or as pointers to other Forth words. Additional information, such as the length of the defined word and link pointers to other definitions, is necessary for the mechanics of dictionary lookup.



An inner interpreter, the threaded list interpreter, threads its way through the hierarchy of Forth words after an outer interpreter, the dictionary lookup, finds the high level word to be executed. The outer interpreter is, in general, not very fast. This is less important than one might think as it affects the user in only two ways. It adds an unnoticeable amount of overhead when keying in words to be directly interpreted, and it slows down compiling from disc to some extent. The important consideration is the execution speed of compiled words, a function of the efficiency of the inner interpreter.

The inner interpreter follows pointers from high level Forth words to lower and lower level words until at the lowest level machine code is executed. On some processors, eg, DEC PDP-11 and Motorola 68000, the inner interpreter may take only two instructions, while on other microprocessors, eg, Intel 8080, it may take eleven or more. It is the time spent in the inner interpreter compared with the time spent in machine code words that determines a microprocessor's Forth implementation efficiency.

Programming in Forth

Programming in Forth means defining new words in the Forth dictionary. These new words are fully equivalent to the words already in the dictionary and may actually supersede them if that is desired. In this way the Forth user is writing a personal language as a natural result of programming. The usual way of defining a new word is through the use of the : (colon) defining word. (The following statement defines the word `CUBE`.)

```
: CUBE DUP DUP * * ;
```

The word `CUBE` duplicates the top stack item twice then `*` multiplies the top two items, replacing them with the product. Applying `*` again leaves the cube of the initial stack item on the top of the stack. The `;` (semicolon) terminates the definition. When compiled, `CUBE` consists of a dictionary header containing the word `CUBE` and a parameter field containing pointers to the words `DUP` and `*`. In all subsequent definitions, the word `CUBE` can be used instead of the more wordy `DUP DUP * *` adding clarity to the program. Because in the Forth language there is no GO TO type statement, a variety of other control structures is available instead of this potentially "harmful" construct.

Meta-defining words

Perhaps the most elegant and powerful Forth words are `<BUILDS DOES>`. These meta-defining words allow the user to define new defining words like : (colon). Suppose we wish to define a case defining word, that is, a word that creates a case statement for a specific entity or attribute. This can be done with the `<BUILDS DOES>` word combination. The general form of the `<BUILDS DOES>` definition is

```
: XXX <BUILDS (compile-time words) DOES>
  (execution-time words) ;
```

`XXX` becomes a new defining word. Each time `XXX` is used the compile-time words are executed creating a new Forth word. This new Forth word, when executed, performs the execution-time words. Using the case example alluded to above,

```
: :CASE <BUILDS ] DOES> SWAP 2 * + @ EXECUTE ;
```

`:CASE` becomes a new defining word. `<BUILDS` sets up a dictionary header for the `:CASE` defined word, `]` begins compilation, and `SWAP 2 *` converts a case number to a byte index which is added by `+` to become the address of the indexed case word. `@` fetches the case word address, and `EXECUTE` executes it. `:CASE` can now be used to define a case statement. Suppose the numbers 0, 1, and 2 represent the colors red, yellow, and blue. To represent that, create words `RED`, `YELLOW`, and `BLUE` that display the text 'red', 'yellow' and 'blue'.

```
: RED ."red"; : YELLOW ."yellow";
  : BLUE ."blue";
```

Then, create the case `COLOR`:

```
:CASE COLOR RED YELLOW BLUE ;
  (Defines COLOR as a case word)
```

The statements, `0 COLOR` will then display 'red', `1 COLOR` will display 'yellow', and `2 COLOR` will display 'blue'. The `<BUILDS DOES>` meta-defining words can be used to create data structures with built-in intelligence, like strings and arrays with self-incrementing pointers or automatic range checking on values or indexes. One particularly interesting use of the `<BUILDS DOES>` words is found in writing a Forth assembler.

A powerful one-page assembler

The Figure shows an 8080 assembler written in Forth on less than one page. To those not familiar with Forth, this comes as quite a surprise. Using assembly language, an 8080 assembler could easily occupy 50 or more pages of code. There is one explanation for this compact code (compact object code as well as source code) over and above the usual Forth reasons for compactness—the extreme modularity of the language and each word reference occupying only one word.

```
FEIR 1 {OCR FONT}

{ FIGFORTH 8080 ASSEMBLER                               JJC 80MAR04  )
HEX VOCABULARY ASSEMBLER IMMEDIATE
' ASSEMBLER CFA ' ;CODE 0A + !            ( PATCH ;CODE IN NUCLEUS )
: CODE ?EXEC CREATE [COMPILE] ASSEMBLER !CSP ; IMMEDIATE
: C; CURRENT @ CONTEXT ! ?EXEC ?CSP SMUDGE ; IMMEDIATE
: LABEL ?EXEC 0 VARIABLE SMUDGE -2 ALLOT [COMPILE] ASSEMBLER
    !CSP ; IMMEDIATE
: 8* DUP + DUP + DUP + ; ASSEMBLER DEFINITIONS
4 CONSTANT H    5 CONSTANT L    7 CONSTANT A    6 CONSTANT PSW
2 CONSTANT D    3 CONSTANT E    0 CONSTANT B    1 CONSTANT C
6 CONSTANT M    6 CONSTANT SP                2A28 CONSTANT NEXT
: 1MI <BUILDS  C,  DOES> C@ C, ;
: 2MI <BUILDS  C,  DOES> C@ + C, ;
: 3MI <BUILDS  C,  DOES> C@ SWAP 8* + C, ;
: 4MI <BUILDS  C,  DOES> C@ C, C, ;
: 5MI <BUILDS  C,  DOES> C@ C, , ;

00 1MI NOP      76 1MI HLT      F3 1MI DI       FB 1MI EI
07 1MI RLC      0F 1MI RRC      17 1MI RAL      1F 1MI RAR
E9 1MI PCHL     F9 1MI SPHL     E3 1MI XTHL     EB 1MI XCHG
27 1MI DAA      2F 1MI CMA      37 1MI STC      3F 1MI CMC
80 2MI ADD      88 2MI ADC      90 2MI SUB      98 2MI SBB
A0 2MI ANA      A8 2MI XRA      B0 2MI ORA      B8 2MI CMP
09 3MI DAD      C1 3MI POP      C5 3MI PUSH     02 3MI STAX
0A 3MI LDAX     04 3MI INR      05 3MI DCR      03 3MI INX
0B 3MI DCX      C7 3MI RST      D3 4MI OUT      DB 4MI IN
C6 4MI ADI      CE 4MI ACI      D6 4MI SUI      DE 4MI SBI
E6 4MI ANI      EE 4MI XRI      F6 4MI ORI      FE 4MI CPI
22 5MI SHLD     2A 5MI LHLD     32 5MI STA      3A 5MI LDA
C4 5MI CNZ      CC 5MI CZ       D4 5MI CNC      DC 5MI CC
E4 5MI CPO      EC 5MI CPE      F4 5MI CP       FC 5MI CM
CD 5MI CALL

C0 1MI RNZ      C8 1MI RZ       D0 1MI RNC      D8 1MI RC
E0 1MI RPO      E8 1MI RPE      F0 1MI RP       F8 1MI RM
C9 1MI RET      C3 5MI JMP      C2 CONSTANT 0=  D2 CONSTANT CS
E2 CONSTANT PE  F2 CONSTANT 0<     : NOT 8 + ;
: MOV 8* 40 + + C, ;  : MVI 8* 6 + C, C, ;  : LXI 8* 1+ C, , ;
: ENDIF 2 ?PAIRS HERE SWAP ! ;       : THEN [COMPILE] ENDIF ;
: IF C, HERE 0 , 2 ;
: ELSE 2 ?PAIRS C3 IF ROT SWAP ENDIF 2 ;
: BEGIN HERE 1 ;
: UNTIL SWAP 1 ?PAIRS C, , ;  : AGAIN 1 ?PAIRS C3 C, , ;
: WHILE 1F 2+ ;
: REPEAT >R >R AGAIN R> R> 2 - ENDIF ;



( EXAMPLES USING FORTH 8080 ASSEMBLER                  JJC 80MAR12 )
FORTH DEFINITIONS
CODE CSWAP ( WORD-1--- SWAPS HI AND LOW BYTE OF WORD ON STACK )
    H POP  L A MOV  H L MOV  A H MOV  NEXT 1 - JMP  C;
CODE LCFOLD    ( FROM-2 QTY-1--- CONVERTS LOWER CASE TO UPPER )
    D POP  H POP
    BEGIN  D A MOV  E ORA  0=  NOT
    WHILE  M A MOV  60 CPI  CS  NOT
        IF  20 SUI  A M MOV
        ENDIF  D DCX  H INX
    REPEAT  NEXT JMP  C;
```

This further compaction is achieved by using the meta-defining words `<BUILDS DOES>`. First, `<BUILDS DOES>` is used to set up instruction class defining words which, in turn, are used to define the individual instructions. The instruction class defining words `1MI` through `5MI` cover five 8080 instruction formats from 1-byte instructions with no operands to 3-byte instructions with one operand. How these class operators work is shown by applying each one to define a particular instruction belonging to its class.

```
: 1MI <BUILDS C, DOES> C@ C, ;
```

`07 1MI RLC` — `1MI` defines `RLC` to implant the hexadecimal code `07` in the dictionary each time it is used. The `<BUILDS` part of `1MI` puts away the code `07` with `C,` . On the execution of the `RLC` word the `DOES>` part of the `1MI` definition is evoked picking up the previously stored code (with `C@`) and placing it in the dictionary (with `C,`).

```
: 2MI <BUILDS C, DOES> .C@ + C, ;
```

`A0 2MI ANA` — In this case `2MI` defines `ANA` to implant the sum of the code `A0` and the top of the stack into the dictionary. The difference between this definition and the prior one is the `+` applied after `C@` fetches the code and adds it to the prior top of the stack.

```
: 3MI <BUILDS C, DOES> C@ SWAP 8* + C, ;
```

`05 3MI DCR` — The difference between `3MI` and `2MI` is `3MI` generated operations shift the operand on the top of the stack to the left by three bits (`SWAP 8*`) before adding it to opcode `05`.

```
: 4MI <BUILDS C, DOES> C@ C, C, ;
```

`F6 4MI ORI` — Here the opcode is sent to the dictionary unaltered as with `1MI`, and the operand is sent as a separate following byte.

```
: 5MI <BUILDS C, DOES> C@ C, , :
```

`F4 5MI CP` — This category is nearly the same as `4MI` except that the operand is sent to the dictionary as a 16-bit word.

Three instructions, `MOV`, `MVI`, and `LXI`, do not fit into the above five categories. Since they are the only instructions of their respective classes (formats), they are explicitly defined using `:` (colon) definitions. There is no space saving benefit or added convenience provided by using a `<BUILDS DOES>` defined class word and then applying it to only one instruction.

Certain instructions like `JP`, `JM`, `JPO`, `JPE`, and `JMP` can be compiled directly from higher level words analogous to Forth control words, eg, `BEGIN`, `WHILE`, and `REPEAT`. This allows the user to directly govern the creation of object code while taking advantage of the clarity afforded by the use of such control words. The fact that these control words are defined with the same names as Forth control words is not a problem since these exist only in the assembler vocabulary. When vocabularies are switched, the words of the new vocabulary are turned on while the words of the old vocabulary are turned off. (A common root vocabulary remains on, and redefined words may be reactivated when vocabularies are switched.)

The Forth word `CODE` evokes the assembler vocabulary and starts a machine code definition in the dictionary. The assembler syntax uses Polish notation with the operands before the operations just as they would be in Forth. This is relatively easy to get used to, particularly because the complete power of Forth is available for operand address calculations.

Future of Forth

There are several ongoing efforts and activities that ensure that Forth will evolve to become the most dynamic computer language available. The foremost of these is FIG, with 2400 members and a dozen chapters in the United States, Canada and Japan, and the European Forth Users' Group (EFUG). FIG's bimonthly newsletter, *Forth Dimensions*, is a first-rate publication containing proposals for extensions, standards proposals, applications programs, Forth-related ideas, suggestions, and announcements.

Another ongoing effort, perhaps unique for any language, is FORML. This group, under the auspices of FIG, investigates such subjects as standards, programming methodology, concurrency, meta-compilers, other languages implemented in Forth, and Forth implementation questions. FORML can be thought of as FIG's research and development arm. Each year a FORML conference is held where papers are presented and discussed in a workshop atmosphere. Last year 65 people attended the conference in Pacific Grove, California. It is noteworthy that so far several simple operating systems and three higher level languages have been implemented in Forth with reduced size and fast execution. The EFUG has implemented UCSD Pascal, Extended Basic, and LISP, while another version of LISP has been implemented in the U.S.

In addition to monthly meetings, FIG has an annual event, a national convention with exhibits, workshops, presentations, and a dinner. At last year's convention about 250 Forth users, dealers, programmers, and enthusiasts attended a full day of sessions in San Mateo, California.

There are several FIG special interest subgroups. Although they are separate, it is difficult to segregate them from FORML since many of the same people and topics are involved. Results are usually presented at a FORML group after a gestation period in a special interest group. Currently, the special interest groups are concerned with virtual machines, graphics, numeric extensions, teaching Forth, text processing, and file systems. One of the most active groups is FIGGRAPH, a graphics group.

The development that may prove to be most interesting is the emergence of Forth machines. First of all, Forth to most Forth users *is* a machine. A user is generally not concerned with the real hardware under the machine unless it is either too slow or it provides insufficient storage capacity. Since Forth is easily ROMable, implementations are now showing up as ROM versions on such machines as the NSC-800 from EiComp and the 8100FMP from Inner Access Corporation. A FIG interest group is currently designing a bit-slice machine to carry this another step by directly executing primitive Forth instructions, an effort that should lead to fast and efficient implementation of Forth.

Perhaps the most important and unique thing about Forth was pointed out by Alan Taylor ("Taylor Report") of *Computerworld* at the Forth convention. "A crucial strength of Forth is in its collection of bright people it has attracted. Their enthusiasm and tireless efforts are sure to make an indelible mark on the evolution of computer languages and perhaps computers themselves."

References*

1. E. Rather and C. Moore, "The Forth Approach to Operating Systems," *Proceedings of the Annual Conference ACM '76*, pp 233-240
2. C. Moore, "The Evolution of Forth, an Unusual Language," *Byte, The Small System Journal*, Aug 1980, pp 76-90, and other articles in this issue that focus on Forth
3. *Forth-79, A Publication of the Forth Standards Team,* Oct 1980 (available through FIG)
4. "Proposed 754 Floating-Point Arithmetic Standard," *Computer Magazine,* Mar 1981
5. L. Brodie, "Starting Forth," to be published, Autumn 1981, by Prentice Hall Pub Co, Englewood Cliffs, NJ

*A number of publications and Forth implementation listings are available through FIG, PO Box 1105, San Carlos, CA 94070.

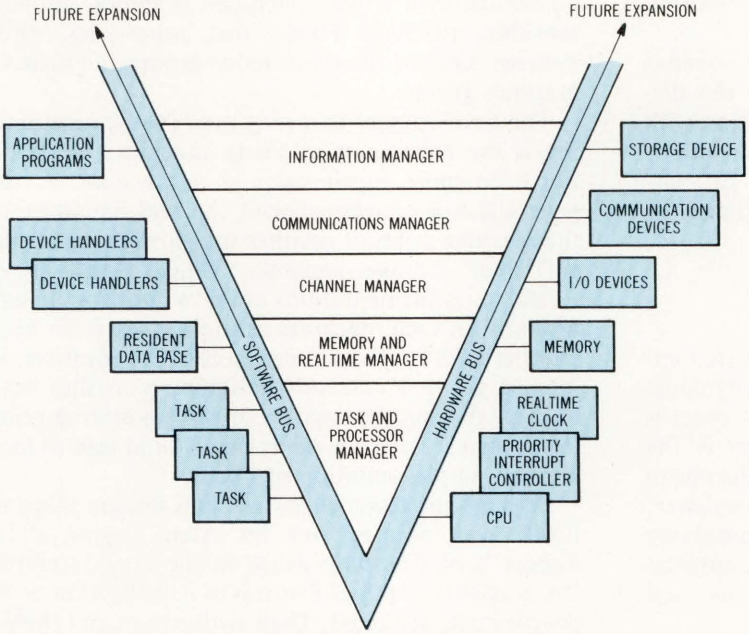
About the Author:

Gary Feierbach is president of Inner Access Corp in Belmont, Calif, a firm involved in the manufacture of Forth based systems and software, and responsible for implementations of Forth on Zilog's Z8000, Burroughs' Illiac IV, and Computer Automation's LSI-2. He earned a BA and an MSEE at the University of California at Berkeley.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 740 **Average 741** **Low 742**

16-bit modular realtime executive extends bare hardware architecture



REX-80 SYSTEM BUS HIERARCHY

REX-80/86 is a modular realtime executive for the iAPX-86/88 family of microprocessors that addresses the growing complexity of software by establishing a foundation that, in effect, extends bare hardware architecture. Its architectural extension provides better software through standardization, along with facilities for multitasking and multiprocessing. Designed to be compatible with high level languages such as PL/M and C, it ensures open ended growth of system designs, promotes modularity, and adapts to a variety of application environments.

Systems & Software, Inc, 2801 Finley Rd, Downers Grove, IL 60515, has introduced the REX-80/86 executive as an architectural extension of the basic iAPX-86/88 hardware, to incorporate programming facilities that manage memory, handle device interrupts, coordinate asynchronous events, perform time based synchronization, and effect co-processor synchronization. (See the Figure.) For example, one significant advancement of the iAPX-86/88 family is the addition of an I/O processor and a numeric co-processor. Architectural extension of the hardware is easily incorporated into a REX-80/86 structure through use of a channel manager and co-processor manager called the special processor executive (SPX). Tasks can invoke SPX facilities to extend their co-processing capability by increasing usage of special co-processor instructions and internal registers. While properly managing each task's co-processing capability, the SPX also coordinates the task's extended instruction execution sequence with that of the co-processor, providing both synchronization and exception handling capabilities.

Supplied as a set of library program modules that can be maintained through use of the object program librarian in the development system, basic REX-80/86 requires less than 4k bytes of ROM and 512 bytes of RAM to implement the core functions of intertask synchronization, interrupt handling, and memory management. Additional facilities such as time based synchronization and co-processor synchronization can be added from the library, as needed, to custom tailor a target system configuration.

Circle 401 on Inquiry Card

Screen formatter automates terminal I/O programming

Screen Formatter System (SFS) runs on Sperry Univac V77 minicomputers to generate and modify terminal display screen formats and thereby eliminate much of the programming overhead usually associated with tasks that create and access terminal displays. Most types of business forms, property registration documents, bills of lading, and purchase orders, for example, can be formatted for screen display in either transaction or batch mode. With COBOL as its target language, SFS generates statements in disc files that ease the application program's task of accessing data fields. It offers field presentation control with protected, unprotected, and blinking field options.

Screen formats in the software package from Sperry Univac, PO Box 500, Blue Bell, PA 19424, can be prepared interactively at a UTS-400 terminal, or in batch mode using a card image format. Format changes and edits are easy to enter. A supplementary format documenter lists the source language statements that were used to create a screen format. Input subroutines supplied with SFS serve as the data interface between the screen and the driver program, and special symbols can be defined through use of the control character manager. The one-time licensing charge is $500.

Circle 402 on Inquiry Card

Forth language adapts EXORset 30 to digital control tasks

EXORFORTH™, developed by FORTH, Inc, 2309 Pacific Coast Hwy, Hermosa Beach, CA 90254, is a multiprogrammed operating system, a full-feature Forth compiler, an assembler, and a fast graphics package, all occupying only 8k bytes of memory in the Motorola EXORset 30. Use of EXORFORTH typically reduces software development time by up to half, and cuts memory requirements substantially, while simultaneously increasing program performance. It is intended to make the full power of the EXORset 30 available to high level language programs, especially programs for process control applications. Purchase price includes a computer aided instruction course.

Circle 403 on Inquiry Card

DIGI-DATA VALUE MEANS:

COMPUTER COMPATIBLE TAPE SYSTEMS THAT START AT $4550*

Digi-Data's complete line of reel-to-reel magnetic tape systems includes a version for your need. Reel size from 7" to 10.5"...tape speed from 12.5 ips to 75 ips... imbedded NRZI, PE or dual density formatter...all the controls you need for computer operation. And any one of those drives can be interfaced to your computer...be it LSI-11, PDP-11, NOVA, Eclipse, HP 2100 or HP 21MX.

But the real clincher for Digi-Data value is cost. You pay up to 65% less for Digi-Data tape systems than you would the equivalent system from DEC, Data General or HP. And there are over 15,000 drives with satisfied users in the field to prove our units are just as good.

Don't forget that Digi-Data makes the value leader in RS-232 compatible printers, too. So take advantage of Digi-Data value. Contact us at

DIGI-DATA
CORPORATION
8580 Dorsey Run Rd.
Jessup, MD 20794
(301) 498-0200
TWX 710-867-9254
®... **First In Value**

*Single unit price. Attractive OEM discounts available.

CIRCLE 64 ON INQUIRY CARD

Daisywheel plotting makes typewriter a graphics device

Written in FORTRAN for use under CP/M, Daisywheel Plotting System is a graphics package designed specifically for daisywheel printers. Sixty user callable FORTRAN subroutines implement many of the features normally associated only with graphics software. Line, bar, and circle graphics can be produced with minimal programming effort. Other routines provide basic plotting functions needed to develop customized applications and to merge graphs with surrounding text when producing a complete document.

Features of the graphics package, released by Escape, Ltd, PO Box 18797, Atlanta, GA 30326, include automatic data scaling, tic marks and grid lines, legends, full use of 2-color ribbon, and complete error diagnostics. A set of upper- and lowercase characters can be produced in any size. Tabbing and vector drawing are supported at any resolution, using any designated plot character. Area shading, cross-hatching, printhead positioning, and line segment output routines can be adapted to specialized daisywheel applications that do not need the full graph generation capability. Purchase price of $600 includes source for various FORTRAN compilers and extensive documentation.

Circle 404 on Inquiry Card

High speed sort utility runs under RT-11

ZORT, an RT-11 record sort utility, places virtually no restrictions on the number of records, their size, or the number of sort keys. Invoked from the keyboard as a standard RT-11 utility or from another program by means of a subroutine call, ZORT resequences file records in ascending or descending order by sort key data. It recognizes a variety of data types including various number (radix) systems, character strings, and system date formats.

ZORT, announced by Logicaid Ltd, 97 Craig Henry Dr, Nepean, Ontario K2G 3S8, Canada, is written in MACRO-11 and optimized for speed. It uses a sophisticated swapping technique to overlay itself and its callers during execution, making almost all system memory available to perform the sort and reducing the overhead required to swap records in and out from disc. It restores all preempted memory upon completing the sort, to make its swapping mechanism completely transparent. ZORT also supports the XCALL statement under DBL (a DIBOL derivative with greater power and more facilities). Purchase price includes object file and documentation.

Circle 405 on Inquiry Card

Nonlinear analysis no problem on Prime computers

TWODEPEP stands for 2-dimensional elliptic, parabolic, and Eigenvalue problems, only some of the applications for this small, easy to use, finite element modeling program designed for Prime computers. TWODEPEP solves a broad range of 2-dimensional partial differential equations, including highly nonlinear problems and systems of several simultaneous equations. It offers such features as nonresident memory; a graphics output package to plot scalar, vector, and stress fields; variable time step, and direct handling of time domain Dirichlet boundary conditions. A special bandwidth reduction algorithm also improves on the standard Cuthill-McKee bandwidth. The software, furnished and supported by IMSL, Inc, 7500 Bellaire Blvd, Houston, TX 77036, gives Prime users valuable and cost-effective solutions to problems involving elasticity, diffusion, head conduction, potential energy, the Schrodinger equations, Navier-Stokes fluid flow analysis, and surface minimization.

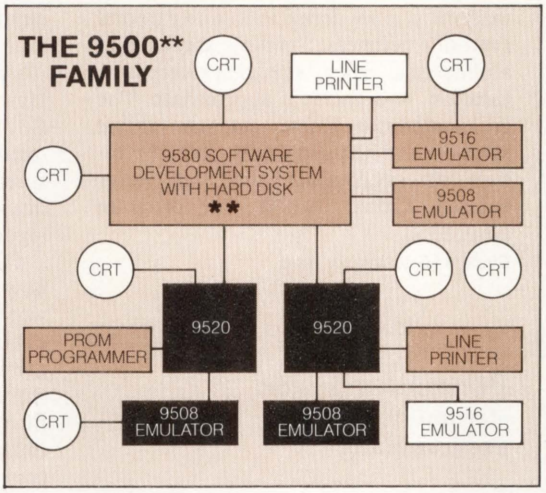
Circle 406 on Inquiry Card

Software retrofit enhances MT-80S printers

Existing MT-80S printers can be converted in the field by a software package, supplied by Microtek, Inc, 9514 Chesapeake Dr, San Diego, CA 92123, that prints full ASCII or APL characters in two operating modes at 70 lines/min. APL character software can print at 10 chars/in (4 chars/cm) in APL mode and at 5, 10, or 15 chars/in (2, 4, or 6 chars/cm) in the 96-char ASCII mode. With APL printing selected, internal logic detects and validates all overstrikes defined by a character-backspace-character sequence, then prints valid overstrike pairs as legible, preformed, composite character. MT-80S-APL is fully compatible with the Volker-Craig 415APL terminal.

Circle 407 on Inquiry Card

Now, multi-tasking productivity in a modular development system



The price/performance equation. You can either add engineers or you can make the engineers you have more productive. Simple as that. That's where the 9500 family of development systems comes in. It attacks the productivity issue head-on.

The 9520 Software Development station. Generate software for your µP-based system on our multi-tasking 9520 Software Development System. It's capable of handling three development tasks at once. Edit one program at the same time that you compile another, and print a listing of another. Three tasks performed simultaneously under control of a single programmer. That's productivity.

The 9508 ICE* station. Separating software generation from both software debug and hardware development is a key element of the 9500 family. The 9508 MicroSystem Emulator is a stand-alone ICE station that works in harmony with the 9520 Software Development System. Download your object files from the 9520 to the 9508. Then break the link. The 9508 can handle all your software debugging functions, with such tools as real-time trace, in-line assemblers and disassemblers, complex hardware breakpoints, and mappable emulation memory. Unbundled software debug. Greater productivity.

Separate hardware debug. Plug the 9508's emulation cable into the µP socket of your prototype system, and you have a stand-alone hardware ICE station. It supports most popular 8-bit µP's and µC's with the most powerful and transparent ICE available anywhere. It doesn't intrude on your µP's memory or I/O addressing space. It supports all of the operating modes of your µP. And, it operates at the full speed of the microprocessor. That means that you can design your product around your µP's capabilities rather than an instrument's limitations.

Upgrade to a dual-user system. The 9520 Software Development System starts off as a multi-tasking, single user system. Just add some memory and a second CRT terminal (it has plenty of ports for expansion), and you have a dual user system that can support two programmers simultaneously. Double productivity from a single software development system.

Total support for the most popular 8-bit µP's. Now. The 9520 has cross assemblers for the most popular 8-bit µP's. Today. And a C compiler and Pascal compiler that generates direct object code for the Z80, 8080 and 8085. The 9508 supports those same 8-bit µP's with transparent ICE. Here's a full list.
8080, 8085, Z80, 8048 family (including 8049, 8041, 8021 and variations) 6800/02, 6801 family (including variations), and more coming.

Next, compatible 16-bit support. 9520 cross assemblers and cross compilers for 16-bit µP's will be available with a totally new stand-alone emulator.

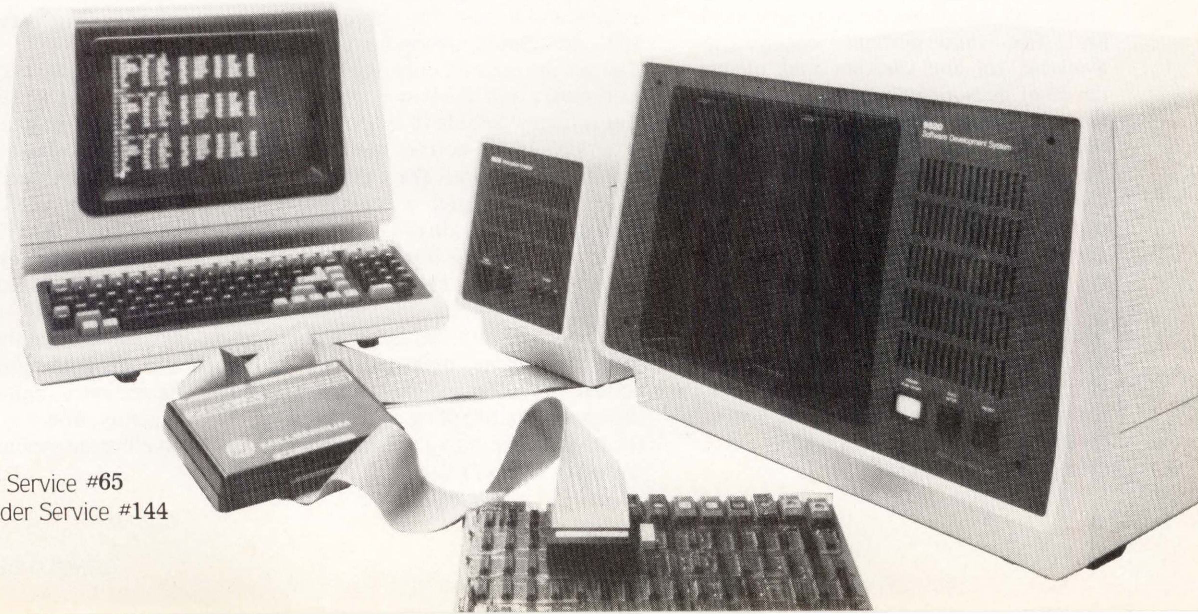
Want more information? Call us (our toll-free numbers are listed below). Or circle one of the Reader Service numbers. We'll respond in real-time.

MILLENNIUM

(800) 538-9320 Toll Free
(800) 662-9231 in California

Millennium Systems,
19050 Pruneridge Ave.
Cupertino, CA 95014
A subsidiary of
American Microsystems, Inc.

*ICE is a trademark of Intel Corporation
**Products shaded in black immediately available.



Information: Circle Reader Service #65
Demonstration: Circle Reader Service #144

Optimizing FORTRAN 77 compiler migrates easily to new environments

Portable compiler brings full ANSI standard X3.9-1978 FORTRAN IV (with optional MIL-STD 1753 extensions) to virtually any combination of host and target machines. Optimization techniques include moving invariant code out of loops, strength reduction (eg, X**2 becomes X*X), constant folding (eg, X = X + 1 compiles to INC X, not ADD 1,X), and common expression elimination. Compiler also performs "peephole" and other machine dependent optimizations.

Generic code generation routines make the Pascal based compiler, released by ACT Corp, 437 Madison Ave, New York, NY 10022, especially easy to modify for new target architectures. Pascal declarative structures create a "skeleton" for each object code sequence within the appropriate procedure. To generate a new set of relocatable object codes, only the skeletons in the various procedures need be changed. In this way, the entire back end of the compiler can be replaced with minimum effort. Purchase price of $155,000 includes distribution rights, documentation, source, and support, with customization services and other options available separately.

Circle 408 on Inquiry Card

PDP-11 environment speeds development of Intel microprocessor systems

Offered by Programming Concepts, Inc, 1 Village Ct, Coram, NY 11727, ASAR software makes the power and convenience of RSX-11/M development tools and file management capabilities available for the creation and maintenance of microprocessor based software. Using a command language nearly identical to that of ISIS-II, it transfers files between ISIS formatted single-density diskettes and PDP-11 minicomputer systems, in either direction, with all required format conversions. A FORTRAN IV subroutine library, included with ASAR, allows direct access to ISIS diskette files. ASAR neither eliminates nor restricts the MDS in-circuit emulation environment. It can be purchased in object format ($795) or in source format ($1850).

Circle 409 on Inquiry Card

Utility program cross-references symbols

Cross-reference utility determines where a symbol is publicly defined and in which object files it is referenced as an external variable. ISIS-II utility program, released by Xener Corp, 6641 Backlick Rd, Springfield, VA 22150, reads object files and produces a cross-reference listing of all public symbol definitions, external symbol definitions, and external symbol references. Symbols are listed in alphabetical order, with their references, location, and value, if appropriate. The cross-reference listing catalogs global symbols and helps to locate unused symbols or subroutines that are never entered. Called OBJXRF, the program costs $350.

Circle 410 on Inquiry Card

Development system streamlines IDMS programming

Totally integrated application development system, ADS/Batch, is said to increase programmer productivity by up to 90% over conventional programming languages in IDMS based systems. Released by Cullinane Database Systems, Inc, 400 Blue Hill Dr, Westwood, MA 02090, ADS/Batch eliminates repetitive coding of numerous routines and definitions, and standardizes error checking. It also reduces maintenance programming because changes need be defined to the system only once, and it reduces programming cost by lowering the time and effort needed both for training and for actual implementation.

For example, in many other IDMS systems, any change to transaction file formats will make it necessary to revise many different application programs at a substantial cost for reprogramming. With ADS/Batch, in contrast, file format changes are entered only once in the data dictionary, and the newly modified format is then available to every application program. Input definitions and editing specifications are also defined only once, and ADS/Batch automatically performs error checking using these centrally defined specifications to ensure consistent error checking across all applications. With the addition of ADS/Batch to an IDMS environment, application routines need contain only the code required for special processing, and this exception handling code can be written in a simple high level language.

Circle 411 on Inquiry Card

HP 3000 operating system now 50% more responsive

Sites running heavy application loads, relative to their configuration, will experience a significant performance gain with version IV of the multiprogramming executive (MPE) operating system for HP 3000 business computers. Improvements to memory and file management, task scheduling, spooling, and I/O handling augment an entirely new intertask communications facility. Other enhancements to this operating system, from Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, increase main memory capacity (up to 4M bytes), spread virtual memory across multiple discs, and improve resource handling algorithms.

Dispatcher and scheduler algorithms now extend control over the system workload. For example, disc accesses are queued by priority, giving higher priority processes better access to bulk storage resources. A TUNE command filters out lengthy transactions, such as those typically found in a batch processing environment, to improve online performance during periods of peak interactive loading.

In a typical, large system with 24 or more online terminals, MPE IV should provide up to 50% more transactions per hour and, consequently, up to 50% better response time than version III. In lightly loaded applications, MPE IV leaves more excess capacity for future growth before a field installed upgrade becomes necessary. MPE IV is available at no charge to series II, III, 30, and 33 installations that are under support contract.

Circle 412 on Inquiry Card

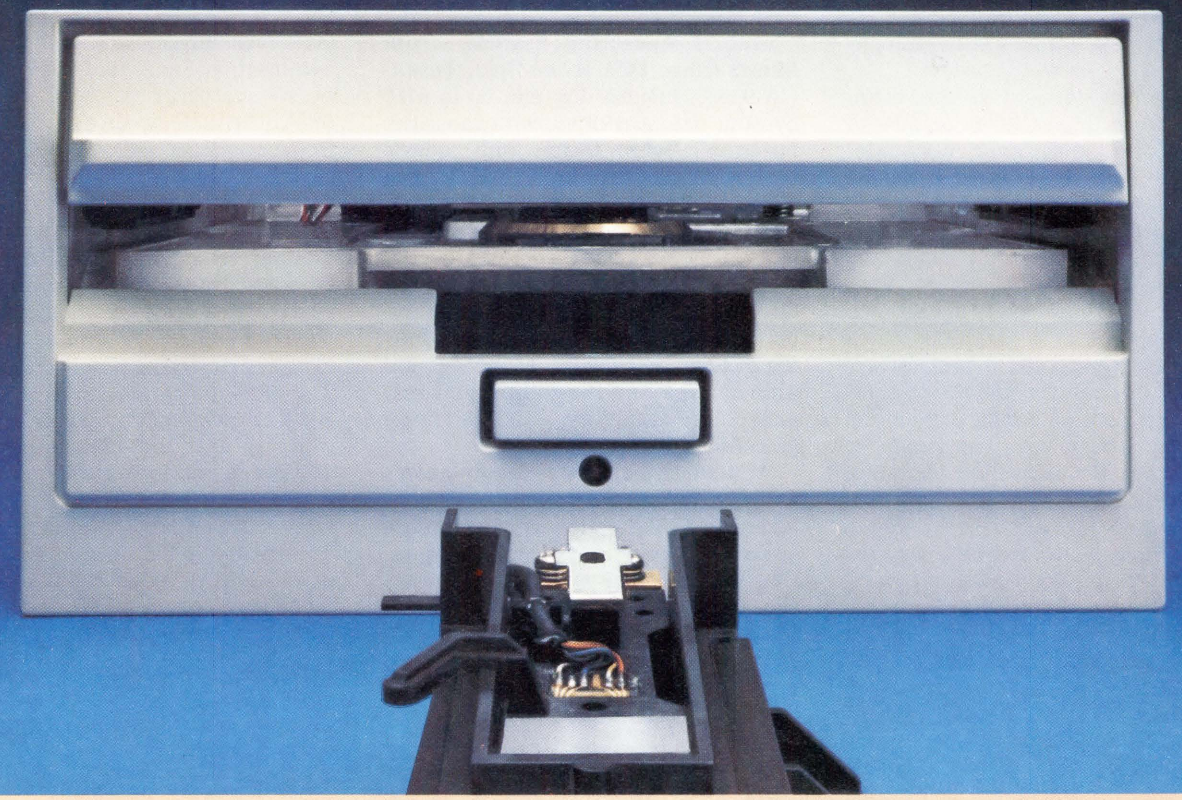
Data entry package enhances distributed processing environment

Raytheon 3270 system users can optimize their online system resources with two software packages, introduced by Raytheon Data Systems Co, 1415 Boston-Providence Tpk, Norwood, MA 02062, that perform full-function data entry in a distributed processing environment. RayKey/1 for the PTS-100 (3270 emulation) system and RayKey/2 for the larger PTS/1200 distributed processing system can reduce communication line and programming costs, decrease host dependency, handle peak loads more efficiently, and increase throughput. Both give instantaneous access to local stored

(continued on page 128)

THE MITSUBISHI FLEXIBLE DISK DRIVE:

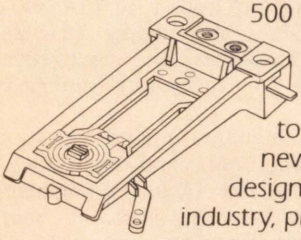
The first of three new models is heads above the competition.



Introducing the MITSUBISHI M2894. Compatible. Interchangeable. Superior.

That's saying a lot, but be sure to examine the realities before you look casually at this Double-Sided, Double Density unit, because it is unique, yet affordable.

Externally, the M2894 is fully compatible and interchangeable with units like Shugart's SA850R, and media interchangeability is assured (IBM media and format compatible–Diskette 1,2,2D or equivalent).



On top of 1.6 MByte capacity per 8 inch diskette, 500 Kbits/second data transfer rate, and 3 ms access time, the M2894 illustrates that unique designs are common to MITSUBISHI: MITSUBISHI's new SOFTOUCH™ Gimbal Head design, unique to the flexible disk industry, provides program seeking accuracy and constant, continuous soft contact for a new experience in lower media cost. Dual magnetic heads load softly (even Tap-Tap), creating excellent read/write characteristics. And, even the location of the stepper motor was critical to MITSUBISHI engineers, minimizing adverse damage or wear due to temperature fluctuations.

You realize the benefits.

Ask your MITSUBISHI Sales Representative or write for complete details.

The M2894. Heads above the competition. Available now. And there's more to come.

Computer Peripherals Division

MITSUBISHI ELECTRONICS AMERICA, INC.
2200 West Artesia Blvd.
Compton, CA 90220
(213) 979-6055 Telex 69-8246.

MITSUBISHI ELECTRONICS
Advanced and Ever Advancing

CIRCLE 66 ON INQUIRY CARD

formats. Discs provide intermediate storage for data that will be transmitted to the host. These features combine to insulate online data entry from external problems such as line, modem, or host failure that would otherwise halt production. When the host is unavailable, data entry continues without interruption.

Local format storage frees host memory and processing capacity, leading to more efficient mainframe operation. Combined with local error checking capability, this reduces line traffic substantially by eliminating the overhead due to format transmission and retransmission following errors. Host communication uses either conventional inquiry/response or a simultated batch mode. Inquiry/response is best for applications that require immediate entry of time-critical or perishable data. Batch transmission eliminates any need for separate 2780 ports and handles data files that were created while the host was offline.

Both packages have format generators designed for use by novice programmers. They allow supervisors to produce screen images with associated validation checks to ensure that only verified data are transmitted to the host. Extensive validation checks, established by supervisory personnel during format generation, range from simple alphanumeric validation to arithmetic calculations. Formats can be retrieved locally or remotely, a feature that simplifies installation and lets users change over at their own pace.

Circle 413 on Inquiry Card

CP/M compatible OS improves throughput, reliability, convenience

MuDOS™ multi-user operating system can be customized to any Z80 hardware configuration and used in place of CP/M™, MP/M™, or CP/NET™. It is ideal for use with the MuSYS NET/80™ and EXP/80™ network slave processors. MuDOS offers many features that are either optional, at extra cost, or simply not available under CP/M, such as a buffer manager, a totally reentrant file manager, and an optional print queuing capability for multiple printers. A sophisticated buffer manager can reduce physical disc accesses substantially; the MuDOS unit accepts buffer capacity as a user parameter that can be changed dynamically under program control. A reentrant file manager allows simultaneous accesses on different DMA controllers and permits high priority tasks to interrupt long file access operations. Concurrent spooling supports multiple-print queues, forms types, fonts, and hand-fed operation for single-sheet devices.

MuDOS operating system, from MuSYS Corp, 1451 Irvine Blvd, Tustin, CA 92680, handles disc files up to 67M bytes in size, and drives with capacities up to 2G bytes. Usable with today's most advanced hardware, it makes warm start and disc log-on displays unnecessary, while allowing disc exchange at any time a transfer is not in progress. Read-after-write verification of each disc update is performed with little or no performance degradation. Error reporting includes meaningful diagnostics and alternative handling instructions, enhancing reliability, and allowing graceful error recovery.

A modular software design adapts easily to various environments. The relocating, linking loader determines system memory size, selects configuration specified in a symbolic parameter file, and loads necessary modules. Hardware dependent elements reside in up to 30 separate modules that can be changed or replaced without massive reassembly or system generation. Extensive utility software is said to equal the support available under CP/M.

As a CP/NET replacement in the MuSYS NET/80 network slave processor, NET/80 performs as a Z80 slave loosely coupled to an S-100 bus and includes 64k of RAM, a single-level interrupt, a console serial port, and a parallel port for communication with the bus master CPU. A MuSYS EXP/80 expansion board adds a second serial port, a Centronics printer port or bidirectional parallel port, priority interrupt control, realtime clock, and similar networking features. Software price is $300 to $700, depending on hardware configuration.

Circle 414 on Inquiry Card

Multitasking executive offers prepackaged approach to M6809 realtime applications

Realtime multitasking executive for the Motorola M6809, called RMS09, controls up to 255 concurrent tasks through supervisor calls that handle task synchronization, resource management, and time dependent operations. Scheduling is based on a fixed task priority level. Fast interrupt response of 150 µs complements a variety of timing options. Other features include ENQUEUE and DEQUEUE functions for resource sharing, logical I/O for true device independence, and a SYSGEN capability that configures customized systems.

Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, also includes standard asynchronous communications interface adapter (ACIA) and peripheral interface adapter (PIA) provision, as well as a customizable I/O environment and customizable interrupt handling scheme that can replace standard interrupt handlers with specialized program code. Optional system monitor can be configured into prototype systems, to control the realtime environment during prototype test and debug. RMS09 can be used as a development system or as an application system. The development environment requires M6809 development system hardware with 32k RAM, EXORdisk II, and MDOS. The minimum application environment includes a timer, 8k ROM, 2k RAM, serial interface, and 20-line parallel port. The Monoboard Microcomputer 19 (M68MM19/19A) provides this hardware. Single unit price is $2700.

Circle 415 on Inquiry Card

User-friendly program generator aids novice on PDP computers

Compatible family of program generators can produce high level language programs to create or maintain data files, generate terminal input displays, sort data elements within files, merge fine data, and create final reports. Designed to help novice programmers prepare complete application software packages, the program generators, developed by Information and Systems Research, Inc, 410 Rouser Rd, Coraopolis, PA 15108, also supply business graphics capabilities and interactive design aids for formatting summary reports.

Output languages include ANSI-74 COBOL, DIBOL, DBL, and BASIC-Plus, spanning the full Digital Equipment Corporation language spectrum from high end RSTS/E applications to the low end RT-11 environment. Because all program generators are compatible, users are not aware of the particular output language—a definite advantage when moving from RT-11 to RSTS/E and back. Typical single-CPU license fees are $11,250 for OEM and $7500 for end user.

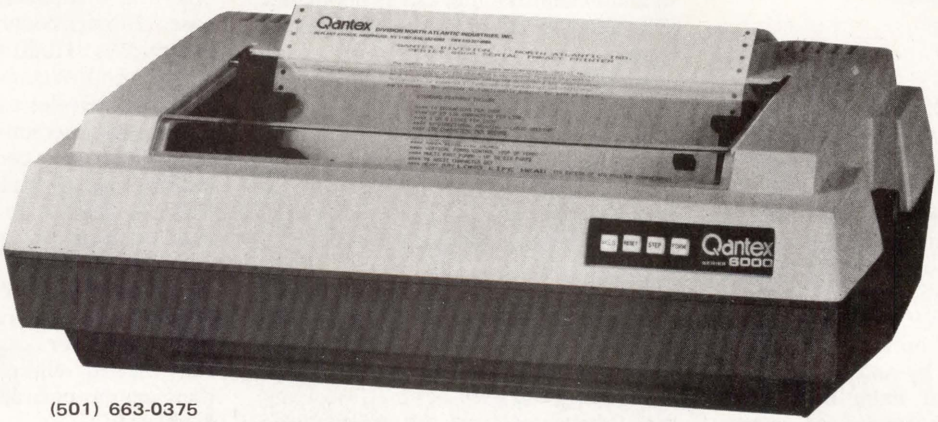
Circle 416 on Inquiry Card

MORE BANG

Qantex Impact Printers
150 Characters Per Second
136 Columns Per Line

The microprocessor controlled **Series 6000** is packed with standard features. True lower case descenders and underlining. Bidirectional logic seeking. Built-in test capability. Rugged 400 million character print head. Beautiful 96 character set in a 9 x 9 matrix. Parallel, or up to 19,200 baud serial interfaces supporting RS-232, X-ON, X-OFF or Current Loop. Full operator controls. Quietized, sleek enclosure to enhance your system. Delivery from stock.

Qantex Division of
North Atlantic Industries
60 Plant Avenue, Hauppauge, N.Y. 11787
(516) 582-6060 TWX 510-227-9660
(800) 645-5292



For more information call your local distributor:

ARKANSAS	
Hemco Electronics	(501) 663-0375
ARIZONA	
Qualtech	(602) 967-4655
The Phoenix Group Inc.	(602) 967-1421
CALIFORNIA	
Basic Systems Corp.	(213) 673-4300
Basic Systems Corp.	(714) 268-8000
Basic Systems Corp.	(408) 727-1800
ILLINOIS	
Engineered Sales	(312) 832-8425
INDIANA	
Audio Specialists	(219) 234-5001
Compusoft, Inc.	(317) 642-8081
LOUISIANA	
Micro Computer of New Orleans	(504)885-5883
MARYLAND	
Source Associates	(301) 431-0587
Systems International Inc.	(301) 977-0100
MASSACHUSETTS	
S & S Electronics, Inc.	(617) 458-4100
MINNESOTA	
Integrated Peripherals	(612) 831-0349
Vikeland Sales	(612) 645-4647
MISSOURI	
ESC Sales & Leasing	(314) 997-1515
NEW MEXICO	
Qualtech	(505) 255-6100
NEW YORK	
Washington Electric Co.	(212) 226-2121/(800) 221-5416
Daily Business Products,Inc.	(516) 543-6100 (800) 645-5556/(212) 594-8065
Synchro Sound Enterprises	(516) 484-1852
PENNSYLVANIA	
QED Electronics	(215) 674-9600
TENNESSEE	
Southland Video Distributors	(800) 238-3274
TEXAS	
Data Trend, Inc.	(512) 496-1111
Datanet, Inc.	(214) 669-1758
Qualtech	(915) 592-2415
VIRGINIA	
Nine Associates, Inc.	(703) 273-1803
AUSTRALIA	
Mitsui Computer Systems	02-9299921
CANADA	
Computer Markets	416-445-1978
DENMARK	
T.M.S. Dataudstyr	(45) 2-911122
ENGLAND	
Philbrand Associates Ltd.	(44) 372-67646
FRANCE	
Gepsi	(33) 1-554-9742
GERMANY	
Technitron	49 (89) 692-4141
HONG KONG	
Hong Kong Equipment	5-453870
NETHERLANDS	
Compudata Benelux B.V.	31-73-215700
SPAIN	
Data Bus De Gabriel Sarasola 2i Ingenieria Informatica	204-2099

Distributor inquiries welcome!

CIRCLE 67 ON INQUIRY CARD

Energy management system specializes in small physical plants

MICROWATT^{R} monitors and controls up to 150 electrical loads at up to 35 remote locations. Its PDP-11 based software assigns each load a power rating, attaches the load to one of up to 5 meters, and switches power on a scheduled, cycled, or demand basis. Scheduled loads (eg, floodlights) are handled fully automatically. Cycled loads (eg, refrigeration equipment) can be shed for part of their scheduled runtime. Demand loads (eg, elevators) can be shed and restored on a priority basis to avoid costly demand peaks. Quantum Technology Corp, 652 Papworth Ave, Metairie, LA 70005, claims that this easily configured system needs virtually no conventional programming, yet bridges the gap between mechanical timeclock and shedders and expensive facility management products. First software license requires pilot system hardware purchase for about $25,000.

Circle 417 on Inquiry Card

VAX archive software features selective save and restore

Incremental file backup and restore system copies only selected VAX-11 files from VMS based disc storage to magnetic tape, and restores designated files individually from tape archives. RABBIT-5 selects files for archiving on the basis of file name or extension, version number, length, date of creation, or date of last access. It also allows "wild card" and "greater/less than" options.

RABBIT-5, offered by AAXCO Inc, 3336 N Flagler Dr, West Palm Beach, FL 33407, operates in novice or expert mode. Expert mode is most useful for system maintenance personnel who can request partial or complete disc backup either interactively or automatically, at predetermined intervals. Novice mode includes a prompter that helps operators fill in blanks to request individual archiving and restore functions such as checkpointing to guard against fatal errors during very long computation runs. Available for purchase ($3750) or rent ($149/mo), this FORTRAN IV and MACRO language program is one of a family of VAX application routines.

Circle 418 on Inquiry Card

ADABAS brings powerful DBMS capabilities to VAX

Assembly language implementation of well-known database management system gives VAX-11/780 and /750 systems under VMS complete transparency of migration from RSX-11/M. Comprehensive, dictionary driven package, from Software AG of North America, Inc, 11800 Sunrise Valley Dr, Reston, VA 22091, blends inverted/relational data structures with full data and index compression technology. Its reentrant, multithreaded nucleus supports relational (ie, value based) access to multiple files, random access via search under mask, sequential access on any key, and optional phonetic retrieval.

Both native and compatibility mode languages can access the data base directly, if required. A terminal based query and report language and a set of interactive utilities for database maintenance are also supplied. Of special importance, data integrity is secured at several distinct levels: automatic restart after system software or hardware failure, record level lockout to avoid interlock during competitive update operations, logging of database update transactions to a recycling disc journal, and reapplication of journaled updates to "roll forward" the database content. Per-CPU license, which includes installation and training, can be purchased ($40,000), rented on a monthly basis, or leased.

Circle 419 on Inquiry Card

Nested arrays extend APL power, versatility

Viewed by many as the next major evolutionary step for APL, nested arrays are multidimensional arrays in which any element can itself be an array of any rank, shape, or type. APL manipulates entire arrays the way other languages handle individual numbers. The first commercial version of APL to support the Nested Arrays System, from STSC, Inc, 7316 Wisconsin Ave, Bethesda, MD 20014, includes new APL functions and operators that work directly on the more natural, nonrectangular, nested array data structures. An experimental version of the enriched language, which should allow much more natural representation of data for common business applications, is available to APL•PLUS^{R} users until January 1982 at no charge.

Circle 420 on Inquiry Card

PL/1 language serves all desktop computer applications

PL/1 language system for 8080, Z80, and 8085 microcomputers, including PL/1 compiler, relocatable macro assembler, linkage editor, and runtime support library, has been announced by Westico, Inc, 25 Van Zant St, Norwalk, CT 06855. Compiler generates industry standard (Microsoft) relocatable code that permits linking subroutines programmed in other high level languages into a PL/1 language program. Disc to disc linker can handle load modules up to the maximum size of the machine. Runtime support library contains more than 300 individual subroutines; however, linker includes only those routines actually used by a program. Minimal runtime package occupies less than 600 bytes. Three comprehensive manuals and a quick reference guide, included with $500 package, serve as a hands-on introduction to the PL/1 language.

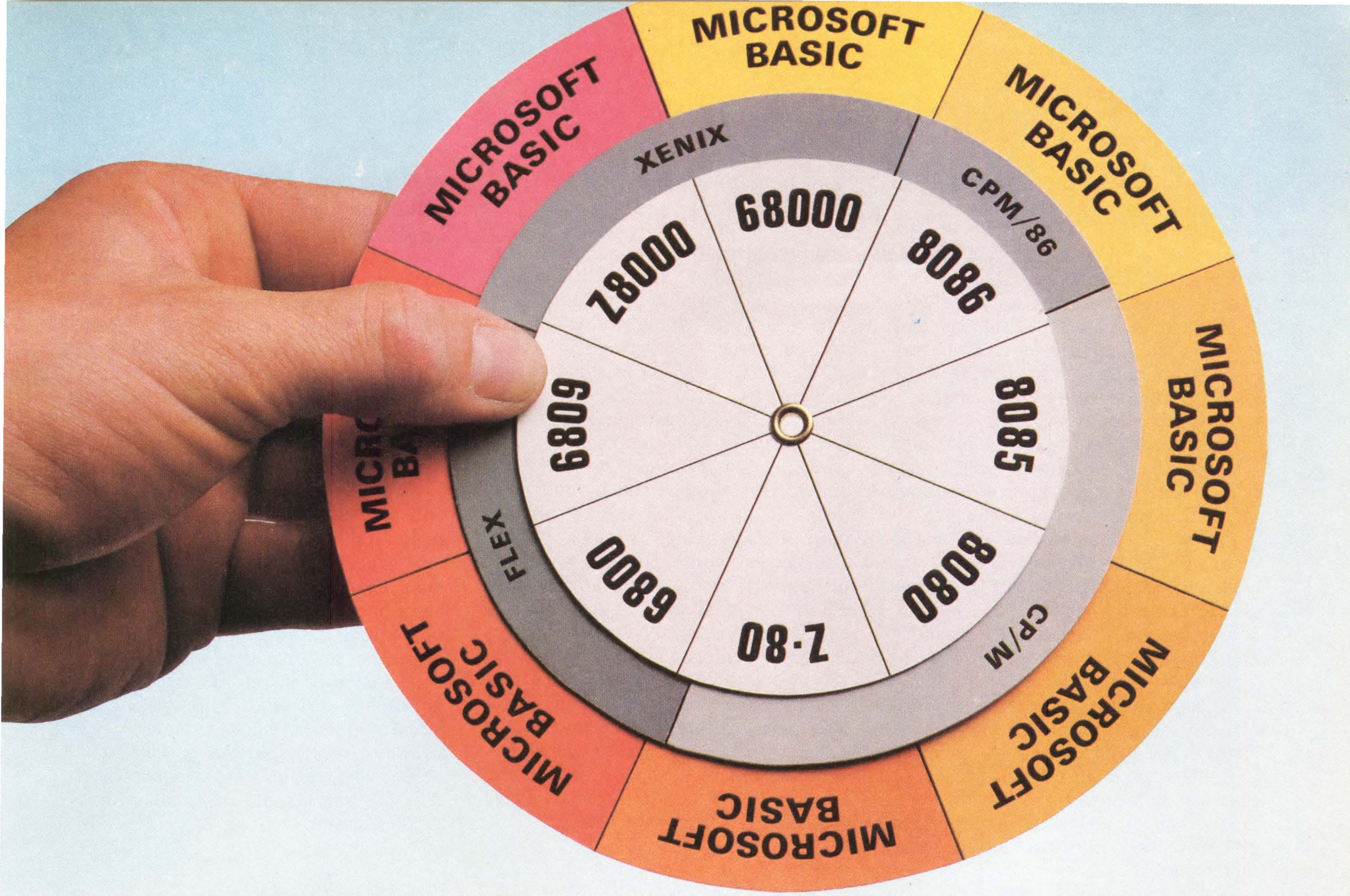
Circle 421 on Inquiry Card

Hardcopy graphics package drives popular, low cost plotters

CURVE is a sophisticated, general purpose, 2-dimensional graphics package that drives Houston Instruments HI PLOT^{TM} and Watanabe Digi-Plot plotters. First developed in 1969 as one of the premier interactive graphics routines on a mainframe computer, CURVE has evolved through numerous implementations on mainframes and minis, and is now available on 8080 and Z80 based microcomputers. It handles Cartesian, parametric, and polar equations; individual data points; shaded bar graphs; either linear or logarithmic axes; and fully scaled alphanumeric characters that can be entered directly from the keyboard.

The BASIC language software features interactive program entry that guides a novice step-by-step through its operation using animated CRT graphics and messages. Built-in diagnostics trap unreasonable input quantities. Generally, only the most elementary knowledge of graphics is needed for successful operation. Sixteen CURVE subroutines can be used to integrate graphics into specialized programs. The complete package, from West Coast Consultants, 1775 Lincoln Blvd, Tracy, CA 95376, costs about $200.

Circle 422 on Inquiry Card



If they write it in Microsoft BASIC they'll only write it once.

Transparent BASICs. Microsoft BASIC implementations are user-transparent from system to system. That's what makes them the defacto standard of the industry. Applications programs written in Microsoft BASIC are transportable across systems with little or no modification. That's a powerful selling tool for an OEM. When a customer is ready to move up to a new system, applications software written in Microsoft BASIC is ready to move, too. That's why more OEMs build systems with Microsoft BASIC than with any other implementation of the language.

More BASICs. There are Microsoft BASICs for Z80, 8080, 6800, 6809 and 6502 microprocessors. Off the shelf BASICs for CP/M® and FLEX. There are Microsoft BASICs for the 8086 and Z8000 under such operating systems as CP/M-86® or the XENIX® OS. All of which means that when you're ready to migrate, you or your customers won't have to start developing applications programs from scratch.

Interpreter and compiler. Write and debug programs with the Microsoft BASIC interpreter. Save, execute and distribute programs with our ultra-efficient BASIC compiler. Microsoft BASIC compiled code is highly optimized, fast, and compact.

CP/M is a trademark of Digital Research, Inc.
UNIX is a trademark of Bell Laboratories, Inc.

Better BASICs. Microsoft BASICs have been in use for over six years and now have more than 700,000 installations. What's more, more applications software has been written in Microsoft BASIC than any other BASIC. Here's why: Microsoft BASIC provides powerful features such as WHILE/WEND, PRINT USING, CHAIN and COMMON, error trapping, protected files, EDIT command, trace facilities, PEEK and POKE, and dynamic string space allocation. Plus, we're adding features all the time—updates are free to most customers.

OEMing hardware? Why not OEM software? Microsoft's aggressive new royalty program makes it easy. Your initial investment is low and you pay us royalties only as you sell systems. Start with the BASICs. But don't forget Microsoft FORTRAN, COBOL, Pascal and the XENIX operating system (UNIX® for 16-bit microcomputers). If you'd like all the details about Microsoft's OEM royalty program, call our OEM Accounts Manager, (206) 455-8080. We'll show you how you can OEM software.

MICROSOFT

WE SET THE STANDARD

10800 N.E. 8th St., Suite 819
Bellevue, Washington 98004
(206) 455-8080 • TLX: 328945

CIRCLE 68 ON INQUIRY CARD

SYSTEMS SOFTWARE

Low cost Z8000 cross assembler runs under RSX-11/M

Fast, efficient Z8000 cross assembler announced by Cambridge Micro Computers Ltd, Milton Rd, Cambridge CB4 4BN, England, can be used for Z8001 and Z8002, in both segmented and nonsegmented modes. It is compatible with the standard Zilog Z8000 assembler language, but includes significant enhancements. Written in BCPL for use as a training aid, the PDP-11 based software is easily transported and has had extensive use in an interactive, multi-user environment.

Extended features embrace added directives for full-listing control, "included" source files, and named program sections that can be either relocatable or absolute. Nested macro facilities and conditional assembly are possible, along with the ability to test macro string arguments. Errors are displayed interactively, at the terminal, and on the listing. Following assembly, a cross linker produces absolute object code that can be downloaded directly to a Z8000. A special downline loader handles all Z8000 development module requirements.

Circle 423 on Inquiry Card

Simulator predicts data link performance

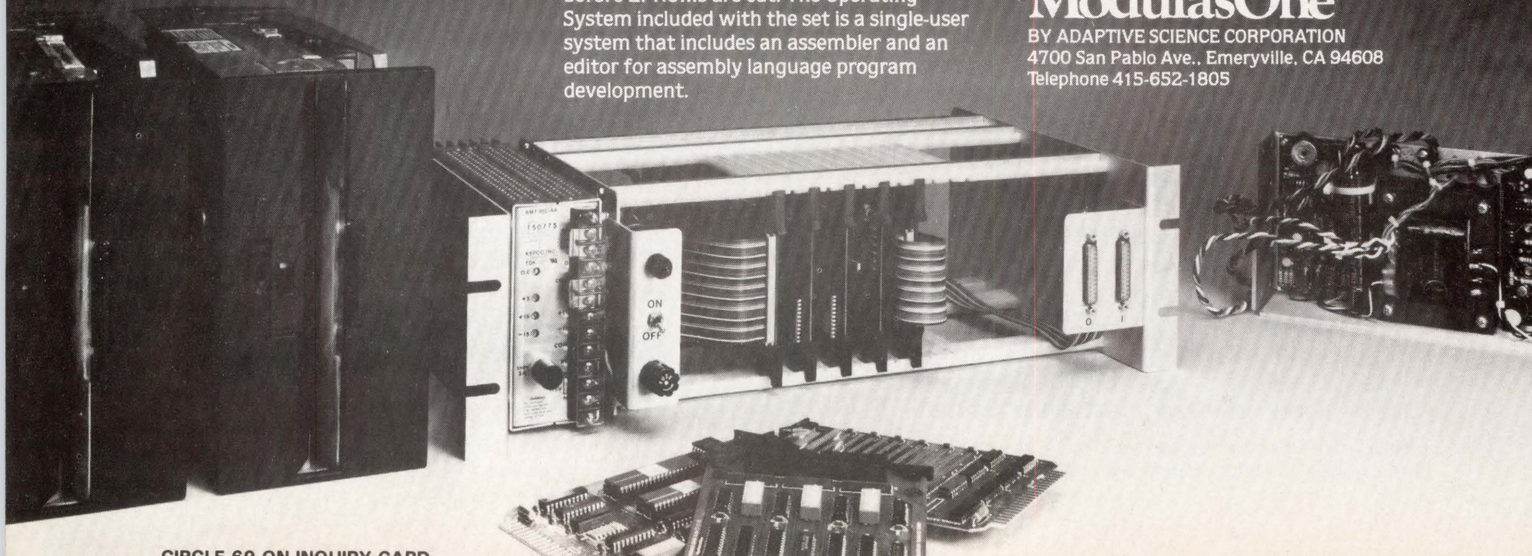
Link Evaluation Model computes network performance data, such as link capacity and response time, that can be used to evaluate various protocols, optimize efficiency, and identify performance factors. Announced by NCR Comten, Inc, 2700 Snelling Ave N, St Paul, MN 55113, the program simulates link activity by representing the predefined characteristics of link speed and length, message traffic load, protocol, etc, using specified values or standard defaults. It formats polling statistics, response time components, utilization data, and throughput parameters in concise summary reports. One basic core module combines with a choice of protocol modules to run on IBM 360/370, 303X, 43XX, or equivalent processors under OS/VS or DOS, in about 200k bytes. Currently available protocol modules, which are licensed separately from basic module, support bisynch and SDLC protocols. Licensing fees range from $2400 to $3000 for first year.

Circle 424 on Inquiry Card

CAD software performs circuit analysis on desktop computer

Ac circuit analysis and waveform analysis of general purpose linear circuits are only two of a series of comprehensive circuit modeling and synthesis aids that COMTRAN, a program developed by Compact Engineering, 1070 E Meadow Circle, Palo Alto, CA 94303, offers on HP-9845T desktop computers. It combines and improves upon two Hewlett-Packard programs, AC-CAP and S-WAVE. Calculated frequency domain results include voltage gain, modal impedance, time delay, and tolerance effects. The transient analysis routine accepts impulse, step, or square wave inputs. Either the HP-9845T CRT, its internal printer, or an auxiliary plotter can produce computed waveform results. Optimization is performed by modifying selected component values to achieve a desired response. COMTRAN is fully compatible with existing AC-CAP and S-WAVE data file formats and is available for a $2500 licensing fee.

Circle 425 on Inquiry Card



Sam Thompson, VP/Marketing, DEI, left, and Doug Broyles, President, Onyx Systems, Inc.

After all, isn't this one available right off the shelf like all the others?

And like the others, isn't this one of the Funnel Series?

And after 6 years, it is the one that's the industry standard for Winchester save and restore isn't it?

And just like the others, it loads 17.5 MBytes in less than 4 minutes doesn't it?

Doesn't it also have a 4-track serial recording format which conforms to the proposed ANSI Standard?

And to Onyx Systems, Incorporated, who has already purchased over 3,500 of them, it's just another one too.

So why make a ceremony about presenting this one to Doug Broyles?

Because this is the 35,000th one and no one else has ever done that before.

After you've made 34,999 high density cartridge tape drives why celebrate one more?

DEI®

DATA ELECTRONICS INC.

10150 SORRENTO VALLEY ROAD, SAN DIEGO, CALIFORNIA 92121 (714) 452-7840 TELEX 69-7118

DEI is a registered trademark of Data Electronics, Inc.

CIRCLE 70 ON INQUIRY CARD

HERE'S WHY MONOLITHIC SYSTEMS IS WINNING THE SINGLE BOARD 8 BIT COMPUTER RACE

We make you more productive...

The MSC 8009* is a "REAL" Single Board Computer. Based on the Z80A® processor, with enough memory - 64K bytes of dual ported RAM and up to 32K bytes of EPROM - to handle most processing tasks on the internal bus. It contains a floppy disk formatter/controller, a choice of powerful APU's, prioritized vectored interrupts and extensive I/O. This total system solution is provided within a single MULTIBUS® card slot...reducing board count, increasing reliability and leaving the MULTIBUS free for system functions. And the MSC 8009 is supported by our extensive and growing line of system modules (ask for our catalog).

And, we put you on the right track for the future...

Monolithic Systems has combined industry standard elements to achieve an elegant computer system architecture...a Z80A processor, IBM floppy disk data format, a 9511/12 APU...all performing under the amazing CP/M®. This is the key to a universe of software that you can select from our catalog or from standard industry offerings. For multiuser or networking capability, MPM® and CP/NET® extends your system performance.

We respond to your needs...

We have a record of consistantly meeting the needs of our computer OEM's for over 10 years. And, when you have a special system requirement, we utilize that extensive experience to deliver a special solution. For applications assistance contact us at 84 Inverness Circle East, Englewood, Colorado 80112 or phone (800) 525-7661.

Monolithic Systems means......
Technically advanced solutions

Monolithic
Systems corp.

MSC Regional Sales Offices: Eastern Region
1101-B9 State Road, Princeton, NJ 08540, (609) 921-2240
Southwestern Region 7505 Lakeshore Drive,
Parker, CO 80134, (303) 841-0888
Western Region 49 South Baldwin, Suite D,
Sierra Madre, CA 91024, (213) 351-8717

*Single Unit Price $1895.00
MP/M, CP/NET and CP/M are trademarks of Digital Research Inc.
Z80A is a trademark of Zilog Corp.
MULTIBUS is a trademark of Intel Corp.

CIRCLE 71 ON INQUIRY CARD

BUBBLE MEMORY CIRCUITS PROMOTE 3-DIMENSIONAL STACKING

Mix or match expansion potential and high speed I/O techniques of interface circuit family enhance bubble memories as disc replacements

Russell MacDonald Texas Instruments, Incorporated
PO Box 225012, Dallas, TX 75265

For a long time bulk storage memories have included two basically different types of components. At one end of the speed/cost spectrum has been the disc, tape, or drum memories, and at the other end has been the semiconductor random access memory, with very little between them. Now magnetic bubble memories are being used more and more to fill the gap between these two extremes in cost and performance. The larger capacity of medium sized hard disc systems enables them to achieve a low cost per bit. However, many applications do not require such a large capacity, and the total system cost may be prohibitive. Floppy disc systems are also nonvolatile and have a lower user-entry cost than other disc systems, but they have a long access time of approximately 300 to 500 ms.

Bubble memories share the advantages of nonvolatility, a low user-entry cost and a potentially low cost per bit. In addition, they have a fast access time of less than 12 ms (as low as 4 ms in some cases), plus the higher reliability of solid state technology as well as being lightweight for portable applications. These characteristics enable them to provide fast auxiliary storage for mainframe computers and to replace fixed head disc or floppy disc memories, especially in harsh environments. As the speed and capacity of bubble memories continue to increase and the costs continue to decrease, they will be increasingly competitive with disc memories.

A magnetic bubble memory product, Texas Instruments' TIB1000 1M-bit bubble memory, is organized as two sections of 512k bits, each with features such as the block swap/replication of data and an onchip map loop for transparent handling of redundant loops. This device is supported by a high performance family of interface circuits that contains all the circuits needed for a complete bubble memory system. (See Fig 1.) The emphasis here is on the hardware interfacing for the magnetic bubble memory (MBM) system, particularly two of the interfacing circuits—the bubble memory controller (BMC) and the data corrector/formatter (DCF). Interfacing for simple systems and high speed systems with direct memory access (DMA), interrupt, and polled input/output (I/O) illustrate MBM interface flexibility, as do the various ways a bubble memory system can be expanded to achieve either greater capacity, higher speed, or both.

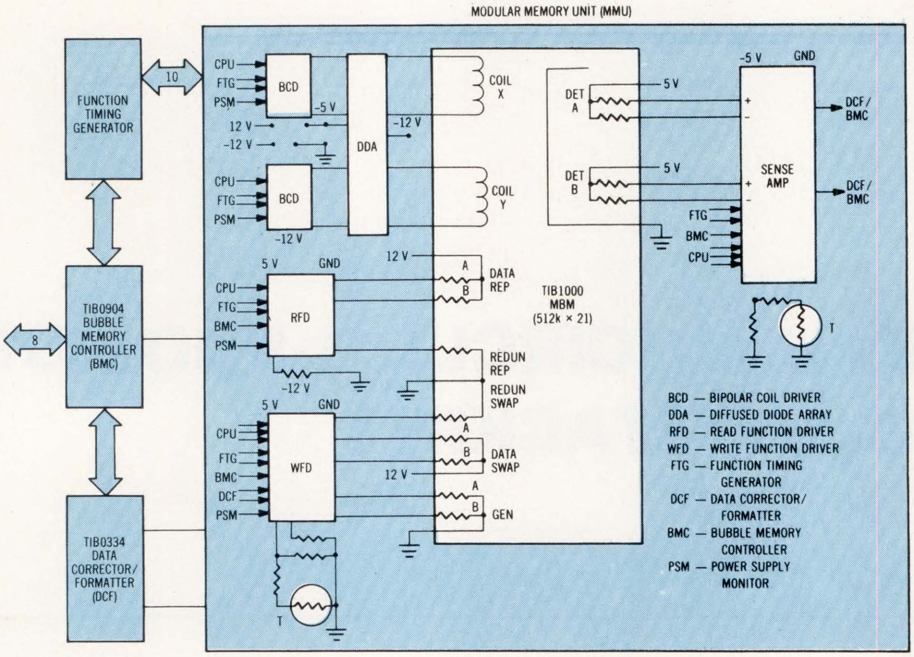


Fig 1 Basic bubble memory system. High performance interface circuit family provides all required support capabilities

BMC Provides High Level Interface

Basic functions of the TIB0904 BMC are to start and stop bubble movement, maintain page position information, control bubble generation and block swap/replication, and initialize redundancy information. It maintains detailed information regarding system status and error correction, and has internal data accumulators for operation with up to four DCF circuits in parallel. With proper buffering, it can control an unlimited number of these devices in parallel when the outputs of the DCF circuits are connected directly to the system data bus.

This BMC is an N-channel, silicon gate, metal oxide semiconductor (MOS) device that operates from a single 5-V supply and is housed in a 40-pin, 600 mil 1.5-cm package (Fig 2), and has several software selectable functions. Certain registers, shown in Fig 3, are accessible to the host so the operation of the controller can be set to meet the requirements of different systems. One of these registers is the bubble parameter register, which is actually a collection of separate registers. It contains all the bubble count distances, from one point to another on the MBM chip, needed to specify a particular type of bubble memory, and is mask programmable. During initialization, the host has the option of selecting certain predefined values for the bubble loop length and the interpage gap. Since all the bubble memory's count distances can be mask programmed, the controller will be able to operate with future products as long as the number of minor loops does not exceed 300. Two other registers, the DMA block size and the DMA dead time, are used to program DMA operation. By loading these registers, the host can select either single-cycle or burst operation for DMA data transfers and can determine the burst length and dead time between bursts.

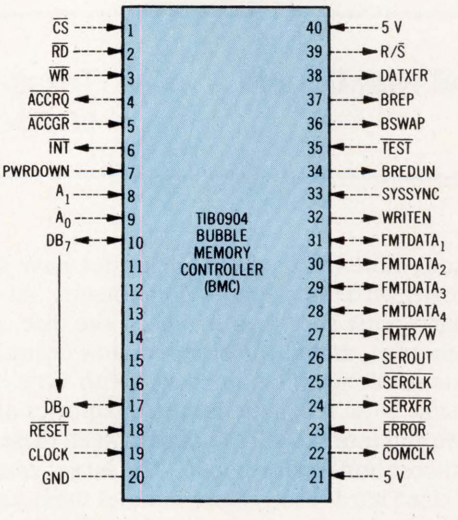


Fig 2 BMC pinout. A_0 and A_1 select BMC registers. DB_0 to DB_7 carry data between BMC and host under RD and WR control. ACCRQ requests DMA transfer, ACCGR indicates DMA in progress, and INT signals interrupt request

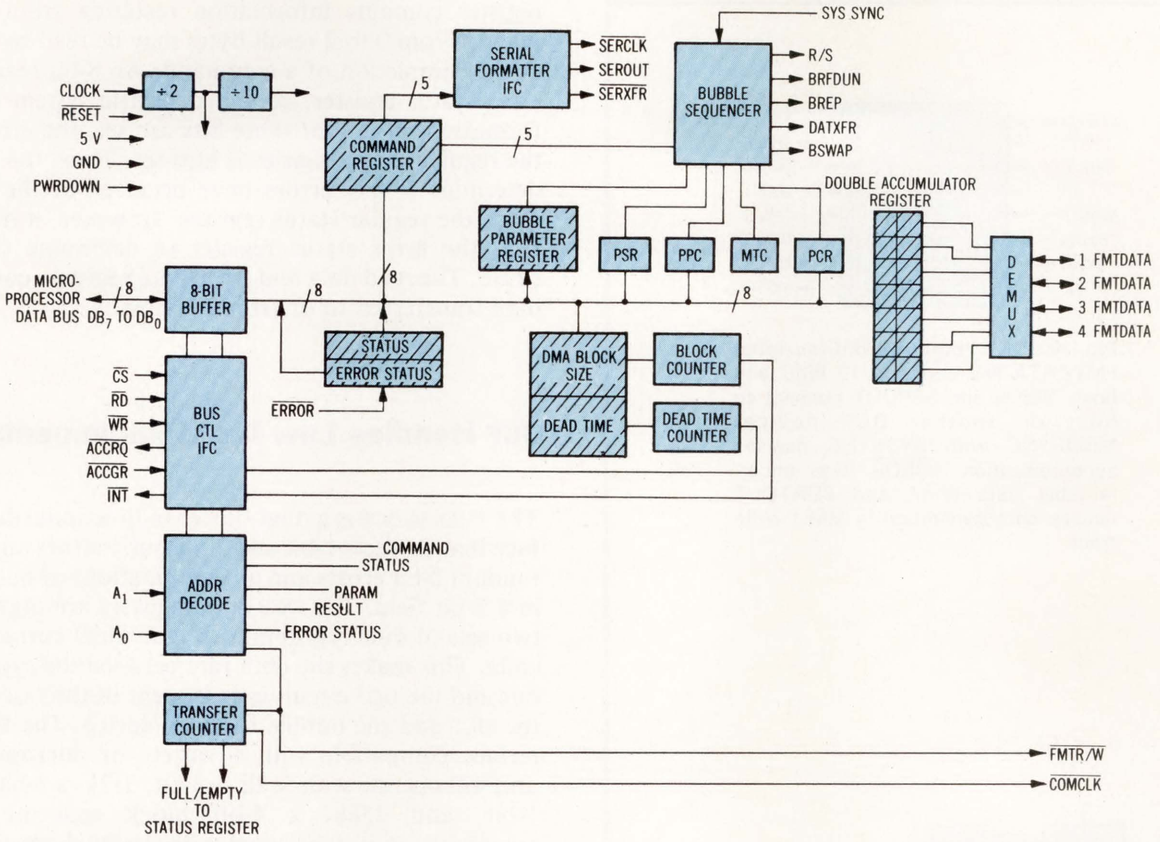


Fig 3 BMC block diagram. BMC appears to host as seven registers (shaded). $\overline{CS}$, A_0, A_1, $\overline{RD}$, and $\overline{WR}$ select particular register under software control. Host can choose loop length, interpage gap, and count distances, as well as single-cycle or burst operation under DMA option

The controller has a general purpose interface that connects easily to most systems. Data can be transferred either with or without DMA. Commands are sent to the bubble memory subsystem via the host controller interface, and results are read through this interface. One of the ways the controller communicates with the host is through the interrupt interface. The interrupt section of the controller activates the interrupt line when the DCF data buffer is full during a read operation, when the DCF buffer is empty during a write operation, when the current operation is completed, or if an error condition occurs.

Another part of the microprocessor interface is the data interface, which may have one of two configurations depending on how data are to be transferred. DMA is generally required if eight or more bubble devices are operated in parallel because the data rate is more than 600k bits/s. Either DMA or program controlled I/O may be used when four or fewer MBMs are running in parallel. If DMA is not used, the host must either wait for interrupts or poll the status register to determine when data are ready to be transferred to or from the data buffer. The host then accesses each data byte and transfers it to or from the system memory.

The BMC's interface to the DCF circuits is a serial link on which commands are sent out by the controller. In the operation of the circuits, the serial stream of data representing commands is clocked through each DCF and then a transfer pulse latches the command into all DCF circuits. Every serial operation transfers four command bits from the controller to the DCF.

The controller appears as seven registers to the microprocessor or host. The first of these is the command register which stores the commands received from the processor. When any bubble operation is in progress, a BUSY signal tells the host not to send any further READ or WRITE commands. The 8-bit status register contains sufficient information to tell the host when operations are in progress or are completed, and whether any errors have occurred. This register can be read to determine the reason for an interrupt or it can be polled if interrupts are not used. The parameter register is used to transfer information to the controller that is required to execute a particular command. Controller initialization information, page count, the page selected, etc, are transferred to the controller through the parameter register. Up to four parameter bytes may be transferred following the command byte. The results

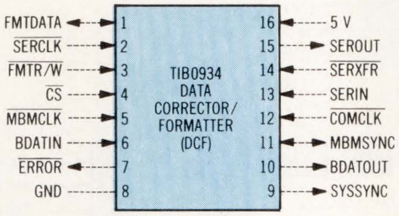


Fig 4 DCF pinout. Bidirectional FMTDATA line connects to BMC and host. SERIN and SEROUT connect to host or another DCF device. MBMSYNC with SYSSYNC handles synchronization, ERROR flags uncorrectable data error, and BDATOUT causes data generation in MMU write track

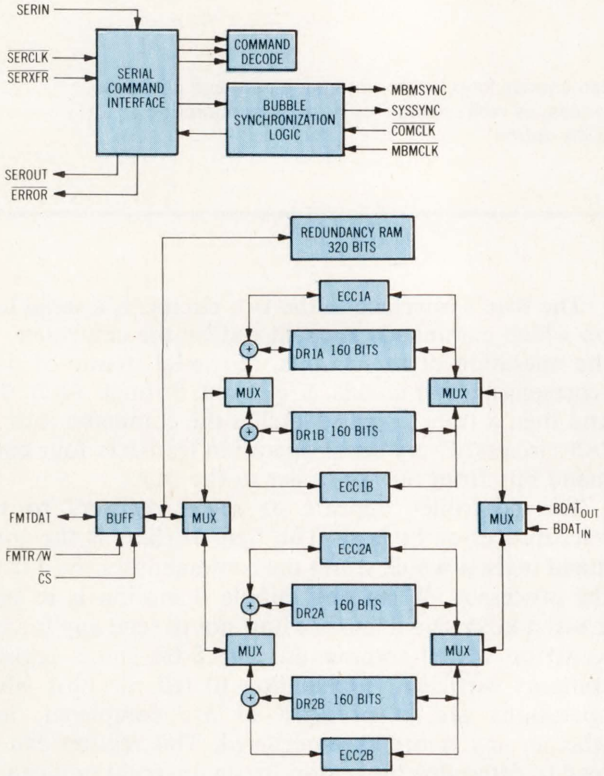


Fig 5 DCF block diagram. DCF register pair holds one full page of data in any operating mode. DCF actually contains two such register pairs, as shown, with dual architecture allowing higher burst rate

register contains information resulting from a command. From 0 to 2 result bytes may be read by the host at the completion of a command. An 8-bit register, the error status register, contains specific system error information. If any of these bits are set, the error bit in the regular status register is also set. Thus, the host can determine if any errors have occurred at the times it reads the regular status register. However, it must then read the error status register to determine the exact cause. The read data and write data registers contain the data transferred to or from the host.

DCF Handles Low Level Implementation

The TIB0934 DCF is a dual-buffer bidirectional data interface that corrects 1-bit and 2-bit burst errors and detects random 2-bit errors and all combinations of burst errors in a 5-bit field. The DCF data registers are organized as two sets of dual registers with individual correction circuits. This makes the data rate between the system data bus and the DCF circuit independent of the rate between the DCF and the bubble memory device. The DCF is interface compatible with a variety of microprocessors and will operate with 512k- x 2-bit, 512k- x 1-bit, 256k- x 1-bit, and 256k- x 4-bit block replicate bubble memories. It is fabricated with an N-channel, silicon gate MOS process; housed in a 16-pin, 300-mil package; and operated with a single 5-V supply (Fig 4).

The DCF handles data using a dual-register pair, shown in Fig 5, each pair containing up to a page of data in any operating mode. This dual-buffer architecture allows data transfers to a host system at burst rates of up to 3 MHz. In the operation of the circuit, one register pair receives data while the other pair transmits and corrects data. When both pairs have completed their operations, a signal from the controller swaps the buffers so that the full register can transmit and the empty register can receive.

The DCF maintains information to show which of the minor loops in the bubble memory device is defective. Redundancy information is stored in a 320-bit random access memory (RAM) in the DCF that can be read from or written to by the host system. The redundancy RAM data are initialized from the redundancy map data contained in a dedicated redundancy loop on the bubble memory device. The redundancy RAM can handle up to 320 bits of data, one bit to describe each of 318 possible loops plus two extra bits to indicate which half of the bubble memory the map describes and to identify which of two copies the map is. During data transfers, the redundancy RAM is synchronized with the serial bit stream that is shifted to or from the bubble memory. Those loops or bit positions, considered redundant, are represented by 0s in the redundancy RAM, while the loops selected for data storage are represented by 1s. Redundancy mapping is totally transparent to the host.

No memory system works perfectly; errors do occur. In a bubble memory system, transient errors usually

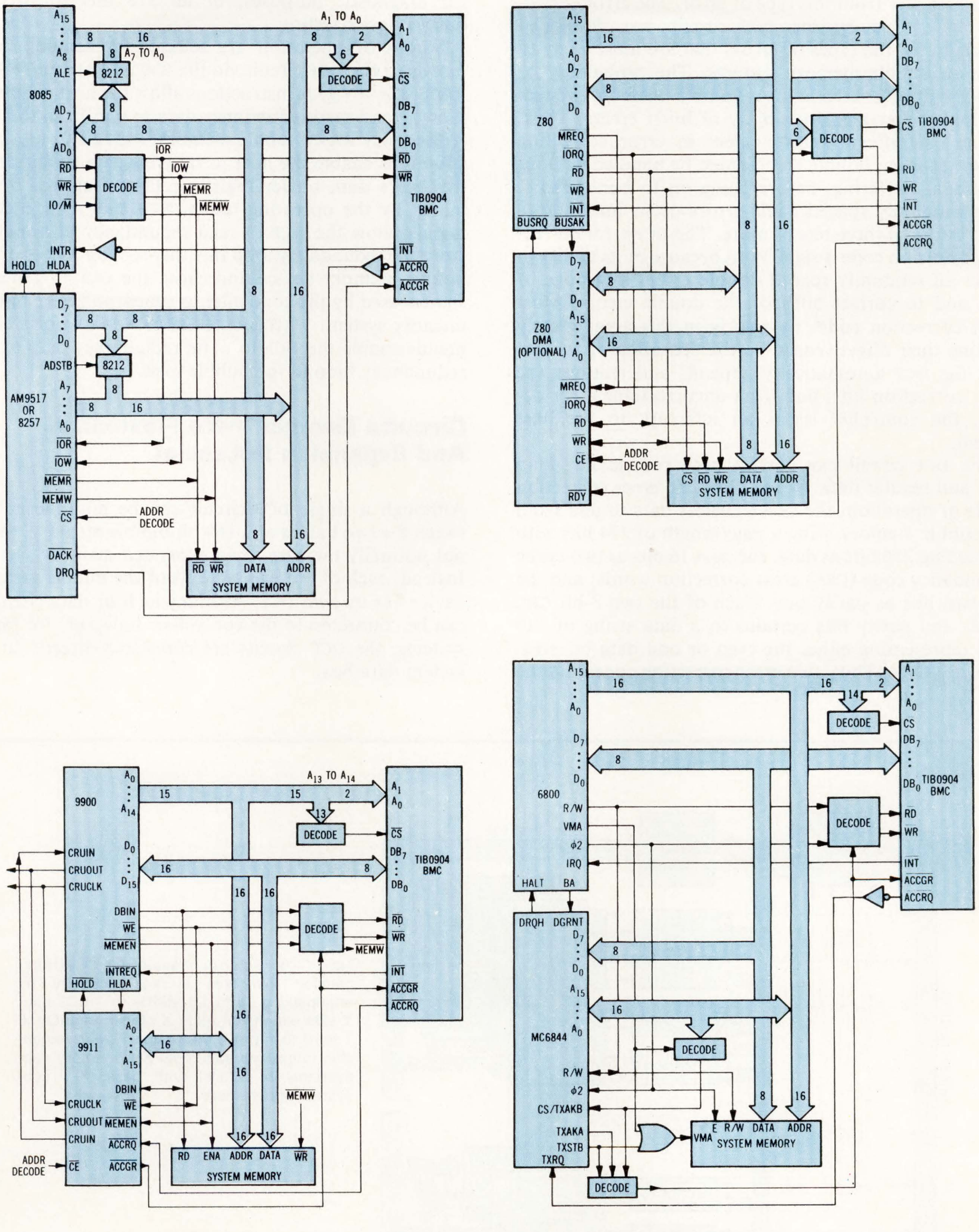


Fig 6 Typical microprocessor and BMC interface arrangements

occur during the bubble detection process, but these can be recovered by rereading the page of data. A memory resident error, on the other hand, involves erroneous data within the minor loops and is repeated each time the page is read. Rewriting with correct data is the only way to recover from this type of error. The error correction code used by the DCF circuit was developed especially for the types of errors that are most likely to occur in bubble memory systems. The probability of random double errors in a bubble memory system dominates over any probability of burst errors. Thus, for any significant improvement in error correcting ability, random double errors must be handled without additional buffering, before going on to burst errors. Even randomly spaced triple errors occur long before burst errors of three bits or more. The DCF error correction/detection code is significant because of its ability to detect all randomly spaced double errors in a page of data and to correct 50% of the double errors. Most burst correction codes do poorly in this area, greatly limiting their effectiveness. In the operation of the circuit, the DCF automatically appends and removes the error correction bits; and if an uncorrectable error occurs, the controller issues an interrupt to the host system.

The DCF circuit can correct both redundancy map data and regular data. When using the error correction mode of operation, the DCF transfers data to and from the bubble memory using a page length of 274 bits with the leading 256 bits as data, the next 16 bits as two cyclic redundancy code (CRC) error correction words, and the last two bits as parity bits. Each of the two 8-bit CRC words and parity bits pertains to a data string of 128 bits, representing either the even or odd data bit positions in a page. Thus, two error correction codes and the data they represent are interleaved throughout the bubble memory page as alternate bits. In addition to the normal error correction mode, there are three other modes of operation that allow the user to read or write 272 bits with transparent parity detection, or 274 bits for diagnostic purposes, or all 318 bits for offline bubble device testing.

Modes of operation are selected by sending commands to the DCF circuit via the BMC. READ and WRITE REDUNDANCY RAM instructions allow the host processor to write and read redundancy data to and from the DCF redundancy RAM. Bubble memory WRITE and READ instructions enable the host to transfer data to and from the DCF's data buffer registers. Page length is determined by the operating mode. RESTORE A or B commands allow the DCF to read redundancy information from the redundancy loop in either section A or B of the bubble memory device and cause the DCF to generate signals used by the controller to synchronize the bubble memory system. WRITE REDUNDANCY MAP A or B commands enable the DCF to write redundancy data to the redundancy loop in the bubble memory.

Circuits Demonstrate Flexibility And Expansion Potential

Although a single DCF circuit can be multiplexed between the two halves of a 1M-bit bubble memory, this is not normally the case in an expanded memory system. Instead, each of the two sections of the bubble memory device has its own DCF. As many as four data channels can be connected to the controller; however, for larger systems, the DCF circuits are connected directly to the system data bus.

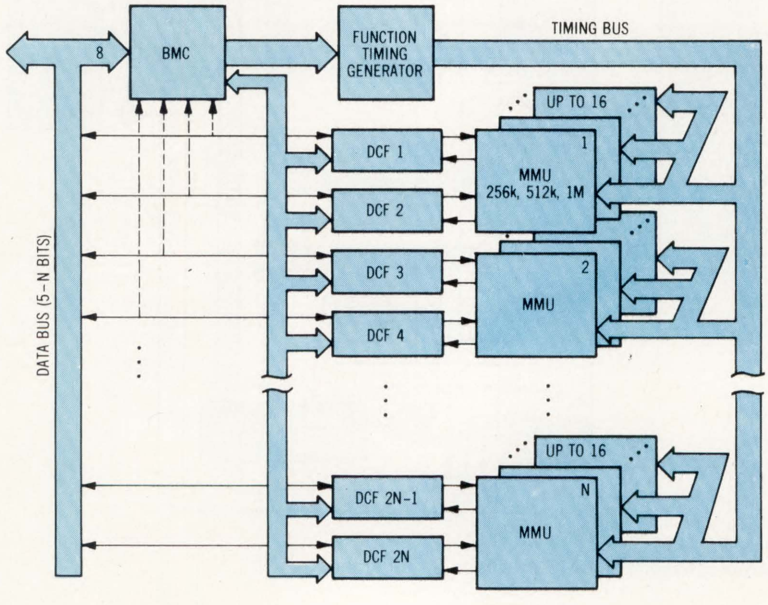


Fig 7 Three planes of expansion. X-axis expansion increases storage capacity by multiplexing up to 16 MMUs to 1 DCF pair. Y-axis expansion adds X planes (numbered 1 to N) to improve throughput. Z-axis expansion interfaces additional X-Y memory subsystems in parallel with basic X-Y subsystem shown here

TIB0934 BMC is compatible with a variety of hosts. DMA may be used when the data rate is high, as when eight or more bubble memory devices are operated in parallel. The timing and sequential addressing for DMA transfers is provided by an external DMA controller. In order to provide maximum system flexibility, the BMC can be programmed for different DMA burst lengths and different intervals between bursts. Communication with the DMA controller is through the usual DMA request and DMA grant signals, while the READ and WRITE signals clock the actual byte transfers. Fig 6 illustrates connection of the BMC to various hosts with DMA capability.

Whether a bubble memory system consists of one bubble memory device or a large array, the controller provides the interfacing to the host system and, as discussed above, can handle data transfers as well. When several modular memory units (MMUs) are multiplexed for operation with the DCF circuit, the system is said to be expanded in the X axis. Multiplexing is accomplished via chip select lines common to all interface circuits within the MMU. Without additional buffering, the DCF can be timeshared among as many as 8 MMUs. If the system is expanded in the X dimension only, data are normally transferred through the BMC where an 8-bit accumulator provides an interface to an 8-bit system data bus.

The primary reason for expansion in the X axis is to increase the storage capacity. If increased data rate is also desired, several data channels are operated in parallel (Fig 7). This means expansion in the Y axis. For larger configurations, the data lines connect directly to the data bus. The overall transfer rate is equal to the maximum data rate of the DCF, 3M-bits/s, times the number of data channels operated in parallel. A typical system with 32 channels yields a data rate of 96M bits/s or 12M bytes/s. With proper buffering, there is no limit to the number of DCFs that can be operated in parallel; thus, the maximum system speed is unlimited. If both increased capacity and increased speed are desired, the system can be expanded in both the X and the Y dimensions.

When expansion in the X and Y dimension does not meet the requirements of the user's application, the system can be expanded in the Z axis as well. Expansion in the Z axis multiplexes two or more memory planes where each plane consists of the basic system shown in Fig 7. When 16 or more of these memory planes share a common address and data bus, the number of DCFs involved allows continuous operation to and from the host system. With 16 planes, the total system capacity is 4096M bits or 512M bytes, and the system can read or write 2048 bytes of data before the DCFs in one memory plane are emptied.

Summary

The TIB0904 BMC and TIB0934 DCF interfacing circuits provide a high performance bubble memory system with error correction that enables bubble memories to compete in the disc replacement market. These circuits handle the details of a bubble memory system such as status, data manipulations, page addressing, redundancy, and error correction, thus freeing the host processor to perform other system tasks to a degree never achieved before. At the same time, these circuits meet the needs of the lower performance but cost sensitive applications as well as the higher performance fixed-head disc market. Although many bubble memory systems are somewhat limited in their ability to expand and to transfer data, the BMC and DCF are extremely flexible in this area since they enable the system to be expanded to quite a large capacity with a high data rate and a low access time.

About the Author:

Russell MacDonald is manager of the Systems Development Section of Magnetic Bubble Memories at Texas Instruments Inc. In this capacity he is responsible for today's as well as future advanced bubble memory systems and has written and presented several papers on the subject. Prior to this, he was lead engineer of a design team developing special purpose high speed CPU test equipment for the military. Mr MacDonald holds BS and MS degrees in electrical engineering from the University of South Florida.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 701 **Average 702** **Low 703**

Ask Ramtek.

(Nobody knows more about Colorgraphics.)

How can a graphics display system save software development time?

By giving you everything you need to start applications programming.

The Ramtek 9400 puts you in the picture fast. We've already solved your graphics problems in the 9400 so you can get your application on line without waiting for—or spending money on—needless systems software development.

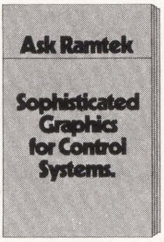
The 9400 puts you in total control. Monitor the situation in real time. Reduce an extremely large or complex picture for a quick look or enlarge portions of it for a closer one without distorting line thickness, texture or character size. At the same time, the 9400 automatically displays the appropriate detail so the picture is always clearly understood.

Need to interact with the picture? Our exclusive entity detection feature lets you identify objects that are pointed out on the screen. Whether a single line or a complex object, let the 9400 find and identify them to the host computer.

Need high resolution or fast response? The 9400 offers a wide range of resolutions up to 1280 X 1024 picture elements in full color. System throughput of over 16,000 vectors per second permits multi-channel operation without sacrificing response time. The bright TV-like picture makes it easy to use in normal room lighting.

For more information on the 9400 and Ramtek monitors and accessories, write: Ramtek, 2211 Lawson Lane, Santa Clara, CA 95050. Or call your nearest Ramtek office.

How much can graphics do?
To find out more about the power of full color interactive graphics, request the booklet "Sophisticated Graphics for Control Systems." It's Issue Number 3 of Ramtek's "USE OUR EXPERIENCE" Series.



Ramtek
Our Experience Shows.

REGIONAL OFFICES: Santa Clara, CA (408) 988-2211, Newport Beach, CA (714) 979-5351, Seattle, WA (206) 838-5196, Albuquerque, NM (505) 884-3557, Dallas, TX (214) 422-2200, Maitland, FL (305) 645-0780, Huntsville, AL (205) 837-7000, Chicago, IL (312) 397-2279, Cleveland, OH (216) 464-4053, Washington, DC (301) 656-0350, Metropolitan NY (201) 238-2090, Boston, MA (617) 273-4590, The Netherlands 31 2968 5056.

CIRCLE 72 ON INQUIRY CARD

IEEE 488 ERROR HANDLING TECHNIQUES: PROS AND CONS

Standardization of error reporting procedures for IEEE 488 based systems reduces controller overhead

Louis F. Santora, Jr

Bell Laboratories
11900 N Pecos St, Denver, CO 80234

To provide a method of centrally controlling sophisticated multimeasurement test procedures on a given device, in 1975 the Institute of Electrical and Electronics Engineers established the IEEE 488 standard for a general purpose interface bus. This standard defines a strict protocol for the transmission of data messages between instruments and a bus controller. Individual instruments can be controlled remotely through the transmission of device dependent messages that a particular instrument will recognize. Within the instruments, device dependent instruction sets allow remote operation. As with any programming language, methods were required to ensure the validity of program code and to aid the programmer in locating and debugging faulty program strings.

When the general purpose interface bus (GPIB) became popular, many diverse functions were designed into instruments. Some instruments use the bus solely for returning measurement data, while others allow full front panel operation via the remote bus controller. Diversity of implementations in the IEEE 488 functions also results in instruction sets that are generally unique to a specific instrument.

A major difference between the instrument environment and a minicomputer environment is the relative lack of compilers that help programmers debug instrument programs. However, efficient writing and program debugging within the integrated instrument system is still necessary. To solve this problem, most designers have added error detection and reporting processes to their instruments.

Error detection and indication were not incorporated into the 1975 standard. Several instruments use similar basic schemes for error detection and reporting; however, sufficient differences warrant special software consideration for each instrument. Thus, further standardization of error reporting procedures and error code syntax can reduce programming time and system software complexity.

Error Detection

Error handling schemes must first consider what errors the instrument should detect. Erroneous data messages that may cause damage either to the device under test or to the instrument performing the test must be detected and aborted, as must errors in data messages that result in inaccurate or inconsistent measurements. Several instruments now available can handle this task. Message syntax must be understood, however, before error detection in data messages received on the GPIB can be adequately considered. This section will deal with two common types of message format: key-code and command-argument. Which of the two data message formats is the better represents a design problem that depends on the functional complexity of a specific instrument.

The *key-code* scheme encodes the stimulus of a function key on the instrument front panel so that a command received on the IEEE bus can be considered in the same way as a stimulus received from the front panel. Key-coded data messages are generally processed by the instrument as they are received. *Command-argument* data messages have the general form

<command> <argument> <command> <argument>...
<terminator>

The <command> <argument> string may be of variable or constant length, depending on the specific instrument. Generally, if the instrument allows only a single <command> <argument> pair, the <terminator> is not used; a specified argument length is detected instead. In variable length data messages of this form, the message string is typically buffered, and execution of the complete string is initiated either when the data message buffer is filled or when the string terminator is detected.

Another method[1] establishes interim registers as commands are received, and transfers these data to an associated set of working registers when the termination character is detected. The <terminator> may be a line feed (LF); a carriage return/line feed (CR/LF); or a special character, such as 'X' or 'S', that is defined by the instrument to trigger execution of the command string.

Key-Code Messages

Each message unit transferred to the instrument on the GPIB usually corresponds to a front panel keystroke. Since a message unit may consist of a variable number of bytes, preliminary information must be stored—usually on an interrupt basis—until a complete message unit is received. For example, the HP5342A microwave frequency counter is interrupted when the first character is received. If the character does not represent a complete message unit, the processor then awaits the remaining characters in the key-code. After all the characters in the complete message unit have been received, the key-code is processed as if the equivalent front panel keystroke had occurred.

One obvious error that must be accounted for during the reception of key-coded messages is the entry of an invalid (ie, inaccurate) key-code. Although this type of error is detected by both the HP3585A spectrum analyzer and the HP8901A modulation analyzer, the HP5342A operating and service manual[2] does not consider the possibility of invalid key-coding. A simple example immediately indicates the importance of this error check. Suppose that the string 'SRAU' is inadvertently keyed for the intended string 'SR5AU'. After the 'S' is received, the microprocessor is interrupted until a complete key-code is received. Because the '5' is missing, the processor does not acknowledge reception of a complete key-code. Consequently, the string is not executed and the microprocessor may be interrupted indefinitely.

The order in which the various key-code commands are given is important because device dependent bus commands are handled as if they were keystrokes. Generally, the key-code string transmitted on the GPIB must emulate keystroke operation in the same order as would be performed by front panel function key operation. Failure to follow the same order may result in erroneous measurements. Particular attention must be given to key-codes that rearm a sweep or retrigger a measurement because they can abort the cycle currently in progress.

> *"One way to solve the problem of improper key-code ordering would be to set up a parsing tree structure similar to that in a compiler."*

Since the three instruments just mentioned, HP5342A, HP3585A, and HP8901A, do not address the key-code ordering problem, the programmer must be familiar with local operation of specific instruments in order to ensure reliable remote control. Detecting errors in key-code ordering requires a complex error detector. Since key-codes are executed as they are received, isolation of improper key-code ordering requires the provision either for storing previous key-codes or for prescribing the allowable sequence of the key-code path. One way to solve such a problem would be to set up a parsing tree structure similar to that in a compiler, wherein the point in a given path is marked as each key-code is received. Every node of the tree has a fixed number of branches associated with it. If one of these branches corresponds to the next key-code received, execution is permitted; otherwise an error is indicated.

For instance, a parsing tree structure could be used to detect errors in key-code ordering for a hypothetical instrument with 100 key-codes, and in which each key-code could be followed by only three possible key-codes. The parsing tree would be a linked structure that contained three addresses, and each address would point to a possible next key-code. Storing such a parsing tree would add 300 words of memory (each word link of 9 bits). Besides the memory that the parsing tree would add to the instrument, the time required to search the three linked key-codes to determine whether a valid path has been pursued must also be considered. This searching process, if performed in software, can add microseconds to the response time of each key-code sent, thereby slowing the entire integrated system.

The preceding example is much less complex than the parsing tree that would be required by an instrument like the HP3585A. Solving the key-code ordering problem on such an instrument would add both hardware and software complexity to the system, as well as increase the processing time of any given key-code. If the additional hardware complexity in the instrument is of little concern, then an alternative could be to provide a GPIB test mode. In the test mode, the hardware and software routines of the instrument's instruction parser could be switched into the system to test the validity of a given instrument program offline. The instrument could then be returned to normal mode for integrated instrument operation, thereby eliminating additional processing time during normal execution. However, the additional expense and hardware complexity must justify the detection of this error.

Command-Argument Messages

Command-argument format, today the most common type of device dependent data message, includes any message that requires header information followed by a specific argument. Since this is the most common bus implementation, it offers a worthwhile analysis of error handling on the bus. Before the development of intelligent large scale integration (LSI), error detection in GPIB implementations was hindered by medium and small scale integration (MSI and SSI) technology. This was a limitation in both the HP6002A extended range power supply and the HP59501A power supply programmer, which expect a message of the form RDDD, where 'R' specifies range and 'DDD' specifies desired voltage or current output within the range 'R'. 'R' can be either 1 or 2, and 'D' can be any digit 0 through 9. However, the hardware for 'R' consists of a single J-K flipflop that is set or reset by the state of lines DI01 and DI02. Also, the 'D' characters are stored in 4-bit registers that look only at lines DI01 through DI04 and perform no comparison to ensure that these lines are within the desired limits. Since the four high order data lines are not considered, any characters presented on the bus will result in a definite state at the output of the R flipflop and the D registers. Lack of error detection in these instruments can be critical because the power supplies can damage devices under test when faulty information is provided.

"Although padding a program string with blanks or other special characters can enhance readability, it may also hinder the programmer from recognizing erroneous operation and subsequently from debugging his program."

Microprocessor technology provides increased error detection capability for command-argument data messages. Two common methods of handling program string errors are demonstrated by the Nicolet series 2090 Explorer oscilloscope, the Tektronix 7912AD programmable digitizer, and the HP3325A synthesizer/function generator. The first method ignores extraneous characters, and the second method issues a service request whenever an unrecognized character is detected.

The Nicolet oscilloscope uses the first method. Any unrecognized characters are ignored without indication to the programmer. Although the status byte (bit 3) indicates the existence of a GPIB error, the type of error is not indicated. Therefore, it is assumed that 'ignore' means that no action is taken to set the status byte. Although padding a program string with blanks or other special characters can enhance readability, it may also hinder the programmer from recognizing erroneous operation and, subsequently, from debugging his program. The HP3325A avoids confusion by ignoring only spaces, carriage return characters, and commas. Other instruments, such as the HP8901A modulation analyzer, ignore a larger set of special characters that could not be confused with a program code.

The Kepco SN488D digital programming system uses a method of ignoring characters in a different fashion; in this device, the entire command string is ignored. The SN488D expects a message with the format X=YAAABBB, where 'X' defines the card address, 'Y' is a control byte, and 'A' and 'B' represent information for channels A and B, respectively. This card has an elementary parser that scans for an '=' character. When detected, the character preceding it is assumed to be a card address. If 'X' agrees with the present address of this card, seven more digits are collected and the program begins executing. If seven digits are not available before the next '=' is detected, the <command> <argument> string is ignored. No indication other than the lack of an expected response is given to the programmer.

At first glance, the method of ignoring characters or strings may seem to be no different from the lack of error handling displayed by the HP power supplies discussed earlier. This is not the case, however, since no instrument action based on the ignored characters is initiated. The HP power supplies, on the other hand, do not prevent erroneous operation that may be caused by the extraneous characters. If this method is to be used effectively, special consideration should be given to the set of characters to be ignored. Only characters that cannot be confused with normal program codes should be ignored (eg, those that can be selected easily from a program code as obvious mistypes). The HP8901A enhances this method by detecting a normally ignored character if it falls within a possible program code.

Ignoring extraneous characters can complement another approach to error handling. To increase readability of program codes, the HP3325A ignores a small set of characters. All other extraneous characters not in the ignored set raise the service request line (SRQ). Thus, the second method of error handling provides a technique for notifying the programmer of an error. The Tektronix 7912AD uses the service request method only, so that inadvertent errors cannot slip through ignored.

One further aspect of the program code string that must be considered in error handling is the termination character. As mentioned earlier, the termination character may be the standard CR/LF or any special symbol defined by the instrument instruction set. The termination symbol is important because it generally initiates execution of the program code string preceding it.

Most bus controllers available today are based on high level languages similar to BASIC. Although the WRITE statements automatically generate CR/LF after each output, constructs are available for suppressing these characters. For example, the HP9825A allows for suppression of the CR/LF in a WRT statement by including a 'Z' in the associated FMT statement. This controller feature is necessary for all instruments that require a special symbol terminator or an argument count terminator. In such cases, no CR/LF characters are expected; if they are sent, the controller will initiate the handshake sequence. But if the instrument has received all of the message it expects, unless it is designed to ignore CR/LF these characters may affect the measurement taking place or cause the SRQ to be activated inadvertently.

Error Reporting

Once errors have been detected, they must be communicated to the controller so that corrective action can be taken. Such communication may be needed for a device dependent message error or for an operational error; the latter is of concern to the programmer because it may have resulted from an ill-defined program string. Two functions that report program code errors are provided by the GPIB definition: the service request cycle and the serial poll function. Devices discussed here initiate error reporting by setting the SRQ line and a bit in the status byte. This action notifies the controller that an error has occurred and allows the controller to determine what type of error has been detected.

> *"Since status bits are designated different functions in different instruments, software error routines are much longer than they need to be."*

Even though the error reporting just described is standard in several instruments, not all instruments use the same bit to indicate a program code error, even within a single manufacturer's line. For example, the HP3325A uses bit 0, but the HP8901A uses bit 1. Consequently, since status bits are designated different functions in different instruments, software error routines are much longer than they need to be.

To further enhance error reporting, several instruments provide an extra "error" byte that can be accessed through the instrument instruction set. For example, the Tektronix 7912AD allows the instrument error status to be queried by the 'ERR?' instruction. The instrument then returns a 3-digit error code that refers to the last status byte reported. Codes of specific interest that may be returned are 102 and 103—invalid command header and invalid command argument.

The HP3325A allows a similar function with its IER (interrogate error) instruction. When this instruction is received, the instrument will return the message ERDATA the next time it is addressed to talk. The 'DATA' in the above message correspond to an ASCII parameter that specifies the error (first error if more than one occurred before IER was issued) that activated the SRQ line. The HP3325A encodes several errors of interest to the programmer: entry parameter out of bounds, invalid delimiter, unrecognizable mnemonic received, and unrecognizable data character received.

No matter how many errors are checked for in a program code string, errors will still be passed over inadvertently. For example, a program code parser cannot determine whether a mistype allows an instrument to be set to the wrong range for the given input signal. Such an error may result in an overload condition or cause some other execution error detectable by the instrument hardware. Indication of this type of error is provided either by a status bit setting or by the output data returned from the instrument.

All instruments that return measurement data have a defined output format. For example, the HP2804A quartz thermometer formats its output data as SDDD.DDD, the HP8901A modulation analyzer formats its outputs as DDDDDDDDESNN, and the HP3438A digital multimeter uses the output format SD.DDDESN. In the preceding formats, 'D' indicates a numeric digit, 'S' indicates the sign, and 'N' indicates the exponent digits. If an overload or execution error condition is detected, each of these instruments returns a specified value or range of values to notify the controller.

The HP3438A returns a data value of +1.DDDE+9, and the HP2804A returns a value of S999.000. The controller must sense these error values and respond accordingly. In the HP8901A, the error code is supplied in the error output data value it returns. Specifically, the value +900000CCE+02 is returned whenever an operational error is detected. In this case, 'CC' is the error code that can be extracted by subtracting 9.E+9 and dividing this result by 100.

Again, we see that several instruments use the same basic approach to communicating an error condition to the GPIB controller. How each instrument implements its error reporting scheme varies just enough to require a different software routine for each specific instrument on the bus.

Conclusion

Major error detection practices today are based on an 'ignored character set' and the detection of extraneous characters. Although each instrument has a unique instruction set, a program could be debugged more easily if all instruments ignored the same set of characters. For example, a simple set of characters to ignore is {space, comma, semicolon}; this set allows sufficient padding of program code strings to enhance readability. Two standard termination characters, CR and LF, should be added to the 'ignored set' of some instruments. In instruments not using these termination characters, provision should be made for accepting and ignoring them, thereby emulating equivalent termination response within all instruments and eliminating the need for special controller functions.

The process of reporting errors presents the greatest difference among instruments. Although all instruments reviewed use the status byte to indicate a GPIB program code error, different bits are assigned similar tasks in the various instruments. Also, several instruments provide special instructions for further interrogation of the error condition. Once again, diversity marks the output data error reporting scheme. Although these levels of error reporting are useful, the diversity encountered increases the software requirement of the integrated instrument system.

"Although each instrument has a unique instruction set, a program could be debugged more easily if all instruments ignored the same set of characters."

Perhaps software is one area of GPIB communications that could develop more stringent restrictions. For example, the extra status information could be included in an extended status byte common to all instruments. Now that instrument designers are focusing in on the set of errors they would like to detect, specific error assignments could be given to each bit. This would make a single error handling routine possible for all instruments on the bus.

Although the preceding suggestions further restrict GPIB device design, they in no way affect the device dependent part of the instrument. Furthermore, since each instrument has a unique instruction set, a large quantity of redundant software already resides in the controller. For these reasons, possible software savings will outweigh recommended design restrictions.

References

1. *Model M107 Precision D.C. Voltage Source Instruction Manual,* Systron Donner Corp, 1980
2. *Microwave Frequency Counter 5342A Operating and Service Manual,* Hewlett-Packard Co, February 1980

Bibliography

Digital Multimeter 3438A Operating and Service Manual, Hewlett-Packard Co, February 1978

Extended Range Power Supply Model 6002A Operating and Service Manual, Hewlett-Packard Co, September 1976

HP-IB Isolated D/A Power Supply Programmer Model 59501A Operating and Service Manual, Hewlett-Packard Co, January 1977

Instruction Manual for Series 2090 Explorer Digital Oscilloscope, Nicolet Instrument Corp, December 1979

Modulation Analyzer 8901A Operating Manual, Hewlett-Packard Co, January 1980

9825A Desktop Computer Extended I/O Programming, Hewlett-Packard Co, 1976

Quartz Thermometer 2804A Preliminary Operating and Service Manual, Hewlett-Packard Co, February 1978

7912AD Programmable Digitizer Service, vol 1, Tektronix, Inc, April 1979

SN488 Digital Programming System Instruction Manual, Kepco Inc, 1977

Spectrum Analyzer 3585A Operating Manual, Hewlett-Packard Co, October 1978

Synthesizer/Generator 3325A Operating and Service Manual, Hewlett-Packard Co, July 1978

About the Author:

Louis F. Santora, Jr is a member of Technical Staff in the Circuit Design Department of Bell Laboratories, where he is responsible for designing circuits for private branch exchange (PBX) systems. Currently interested in computer architecture and digital systems design, Mr Santora holds a BSE in computer engineering from the University of Michigan and a MSEE from Georgia Institute of Technology.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 704 **Average 705** **Low 706**

OUR CONTACTS GIVE YOU MORE RELIABLE INFORMATION.

In the world of electronic data processing, a bad contact is often the same as no contact. And that means information is lost. So when you're connecting a PC board to a backplane or assembling I/O connections, check into the ITT Cannon Electric ADAPTA-CON connector series.

The ADAPTA-CON line is our most versatile packaging concept. Whenever you need a large number of contacts in a specific connector length, ADAPTA-CON gives you high density, high reliability two-piece connectors in a wide variety of crimp or solder type, high or low insertion force, all-plastic designs. Which means you can handle increased capacities with greater reliability. Plus you get Cannon quality with fast delivery at very competitive prices.

For immediate information refer to our pages in EEM. For literature, the name of your local ITT Cannon distributor or other information contact Rectangular Division Marketing Manager, ITT Cannon Electric, a Division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. (714) 964-7400. In Europe, contact ITT Cannon Electric, Avenue Louise 250, B-1050 Brussels, Belgium. Phone: 02/640.36.00.

CANNON ITT
You can always connect with Cannon.

CIRCLE 73 ON INQUIRY CARD

FPLA ARBITER CONCEPT ADAPTS TO APPLICATION NEEDS

Field programmable logic implements efficient, easily customized arbiter whose versatile Boolean statement format meets numerous system requirements

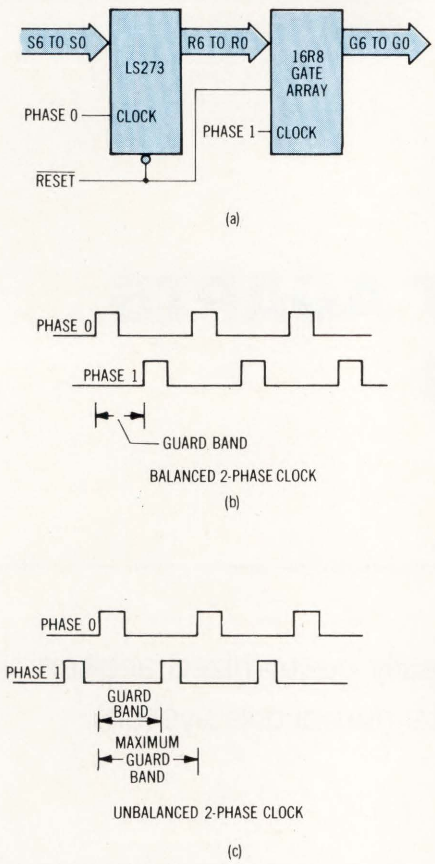
Alan W. Bentley
Cubic Corporation
9333 Balboa Ave, San Diego, CA 92123

Today's trends toward shared resources, multiprocessing, and decentralized, bus oriented system organization underscore the demand for arbiters that work independently and issue grants according to predetermined algorithms. Functionally, a requirement for stable processing of system requests is created when several processors use a common device and each requests service asynchronously. It is the arbiter's task to issue grants for sequential access in accordance with a preestablished algorithm. By using a versatile Boolean statement format to express its algorithms, an arbiter can be customized to interface with single-array, multiple-array, and hybrid logic configurations. Designing arbiters to be flexible in implementing algorithms can help to meet the demand for cost-effective data processing systems and bring heretofore expensive, hence scarce, devices into wider use.

Arbiter Interface

From the system's perspective of the interface, when a system is ready for service from the device, it raises a request line. The arbiter responds by issuing a grant to the system that clears it to conduct transactions with the device. Upon completion of service, the system drops its request line. The arbiter, in turn, cancels the grant and is then free to issue a grant to the next pending request.

Stable system requests are necessary because all requests and grants are evaluated each clock period. These requests are generated asynchronously and are synchronized through a set of input latches. If a 2-phase balanced clock is used, with requests synchronized on phase 0 and grants issued or released on phase 1, the maximum time from a system request for service until synchronization of that request is one clock period. Minimum time from completion of the transaction to release of the synchronized request is the system's internal delay, as it drops the request line, plus the setup time of the synchronizing latches. At the completion of a transaction, there is a half-clock period, the time from phase 0 to phase 1, when a unique signal combination exists—a grant issued to a system that does not have a synchronized request. During this half-period, all other synchronized requests are examined and, according to the servicing algorithm, the recipient of the next sequential grant is determined. Then, on phase 1, the existing (unsolicited) grant is canceled and the next grant issued.



(a)

BALANCED 2-PHASE CLOCK

(b)

UNBALANCED 2-PHASE CLOCK

(c)

$$G_W = \underbrace{\underbrace{\overline{RESET} \cdot R_W}_{\text{EXTERNAL}}\ [\underbrace{\overline{R}_X \cdot \ \ldots \ \cdot \overline{R}_Y}_{\text{INTERNAL}}}_{\text{MODIFIER}} \underbrace{(G_X + \ \ldots \ + G_Y}_{\text{TRANSFER}} \underbrace{+ G_X \cdot \ \ldots \ \cdot G_Z)}_{\text{IDLE}} \underbrace{+ G_W]}_{\text{MAINTENANCE}}$$

(d)

Fig 1 Arbiter circuitry, timing, and grant expression format. In (a), S6 to S0 are system requests. Latch outputs R6 to R0 are synchronized requests that arbiter algorithm converts to system grants, G6 to G0. Unbalanced clock phases increase guard band (b and c), with maximum guard band needing only one phase. Logic equation for algorithm (d) combines four subexpressions

The sum of the requesting system's internal delay in dropping its request line, the synchronizing latch setup time, and one-half the clock period, act as a guard band to ensure separation of systems interacting with the device. Arbiter clock frequency, therefore, is a major factor in determining guard band time. For a given arbiter clock frequency, the guard band can be increased by unbalancing the clock, increasing the time between phase 0 and phase 1 to more than half the clock period. The limiting case occurs when the time between phase 0 and phase 1 is increased until it equals the clock period. This makes phase 0 and phase 1 coincident, requires only a single-phase clock, and maximizes the guard band for a given clock frequency. The limiting case relies on the propagation delay of the latch flipflops and the setup time of the array logic grant flipflops to ensure a delay of one clock period between release of the synchronized request and the associated grant. Start of the guard band signifies completion of the current transaction, and guard band time is used to determine the next grant recipient; then, at the start of the next clock period, the current grant will be canceled, and, if one or more requests are pending, the next grant issued.

Octal D flipflops (LS273) are used to synchronize the input requests, and a programmable gate array (16R8) is used to evaluate the requests and issue grants. In the 2-phase clock, phase 0 synchronizes requests and phase 1 issues grants (Fig 1). Both the octal flipflops and the logic array are 20-pin packages. In addition to the clock and 3-state control inputs, the logic array has 8 data inputs and 8 D flipflop outputs. The Q output of each flipflop is inverted and buffered, and is a 3-state output; the $\overline{Q}$ output is returned to the array internally, where the 8 flipflop settings and the 8 data inputs are complemented and are available in both original and complement form at 8-input OR gates. There are eight OR gates, each forming the D input for one of the eight flipflops.

By programming through fusable links, the set condition of each flipflop is established from the eight data inputs, the current state of the eight flipflops, and the complements of both. Each flipflop's set condition can be represented as a Boolean expression of up to eight ORed statements. Each statement is created by ANDing terms drawn from the data inputs, the flipflop status, and their complements. Limiting parameters of this configuration are the 8 data inputs and the fixed 8-term OR gate at the D input of each flipflop. Boolean expressions implemented through the programmable fuses must be true when the flipflop is to be set or maintained in the set state, and false when the flipflop is to be reset or to remain reset.

Single-Array Configuration

Any of several servicing algorithms, expressed as Boolean statements, can be implemented with a single logic array that will process service requests for up to seven systems. The first two algorithms represent the organizational extremes. "Priority service" algorithm has a strict priority ranking from R6 to R0: a grant will be issued only if no higher priority system has a pending request. The other extreme is the "polled service" algorithm; here, all systems place equal demand on the device and are serviced through a rotating, or "round-robin," method. In this case, when one transaction has been completed, the following grant is issued in response to the next ranking request (eg, next lower number). Circular continuity is maintained by having R6 follow R0 in the granting sequence. Between the extremes, algorithms 3 and 4 represent hybrid organizations. The "executive and polled service" algorithm allows a single, high priority executive system (R6), with the remaining systems (R5 to R0) equal and polled in a

ALGORITHM 1: PRIORITY SERVICE

$$G6 = \overline{RESET} \cdot R6\,[G5 \cdot \overline{R5} + G4 \cdot \overline{R4} + G3 \cdot \overline{R3} + G2 \cdot \overline{R2} + G1 \cdot \overline{R1} + G0 \cdot \overline{R0} + \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0} + G6]$$

$$G5 = \overline{RESET} \cdot R5\,[\overline{R6}\,(G6 + G4 \cdot \overline{R4} + G3 \cdot \overline{R3} + G2 \cdot \overline{R2} + G1 \cdot \overline{R1} + G0 \cdot \overline{R0} + \overline{G6} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G5]$$

$$G4 = \overline{RESET} \cdot R4\,[\overline{R6} \cdot \overline{R5}\,(G6 + G5 + G3 \cdot \overline{R3} + G2 \cdot \overline{R2} + G1 \cdot \overline{R1} + G0 \cdot \overline{R0} + \overline{G6} \cdot \overline{G5} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G4]$$

$$G3 = \overline{RESET} \cdot R3\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4}\,(G6 + G5 + G4 + G2 \cdot \overline{R2} + G1 \cdot \overline{R1} + G0 \cdot \overline{R0} + \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G3]$$

$$G2 = \overline{RESET} \cdot R2\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3}\,(G6 + G5 + G4 + G3 + G1 \cdot \overline{R1} + G0 \cdot \overline{R0} + \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G1} \cdot \overline{G0}) + G2]$$

$$G1 = \overline{RESET} \cdot R1\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2}\,(G6 + G5 + G4 + G3 + G2 + G0 \cdot \overline{R0} + \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G0}) + G1]$$

$$G0 = \overline{RESET} \cdot R0\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1}\,(G6 + G5 + G4 + G3 + G2 + G1 + \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1}) + G0]$$

ALGORITHM 2: POLLED SERVICE

$$\begin{aligned} G6 = \overline{RESET} \cdot R6\,[\overline{R0}\,(&G0 + G1 \cdot \overline{R1} + G2 \cdot \overline{R2} \cdot \overline{R1} + G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} + G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1}) \\ &+ \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0} + G6] \end{aligned}$$

$$\begin{aligned} G5 = \overline{RESET} \cdot R5\,[\overline{R6}\,(&G6 + G0 \cdot \overline{R0} + G1 \cdot \overline{R1} \cdot \overline{R0} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \\ &+ \overline{G6} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G5] \end{aligned}$$

$$\begin{aligned} G4 = \overline{RESET} \cdot R4\,[\overline{R5}\,(&G5 + G6 \cdot \overline{R6} + G0 \cdot \overline{R0} \cdot \overline{R6} + G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R6} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R6} + G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R6} \\ &+ \overline{R6} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G4] \end{aligned}$$

$$\begin{aligned} G3 = \overline{RESET} \cdot R3\,[\overline{R4}\,(&G4 + G5 \cdot \overline{R5} + G6 \cdot \overline{R6} \cdot \overline{R5} + G0 \cdot \overline{R0} \cdot \overline{R6} \cdot \overline{R5} + G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R6} \cdot \overline{R5} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R6} \cdot \overline{R5} \\ &+ \overline{R6} \cdot \overline{R5} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G3] \end{aligned}$$

$$\begin{aligned} G2 = \overline{RESET} \cdot R2\,[\overline{R3}\,(&G3 + G4 \cdot \overline{R4} + G5 \cdot \overline{R5} \cdot \overline{R4} + G6 \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} + G0 \cdot \overline{R0} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} + G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \\ &+ \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G1} \cdot \overline{G0}) + G2] \end{aligned}$$

$$\begin{aligned} G1 = \overline{RESET} \cdot R1\,[\overline{R2}\,(&G2 + G3 \cdot \overline{R3} + G4 \cdot \overline{R4} \cdot \overline{R3} + G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} + G6 \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} + G0 \cdot \overline{R0} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \\ &+ \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G0}) + G1] \end{aligned}$$

$$\begin{aligned} G0 = \overline{RESET} \cdot R0\,[\overline{R1}\,(&G1 + G2 \cdot \overline{R2} + G3 \cdot \overline{R3} \cdot \overline{R2} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + G6 \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \\ &+ \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1}) + G0] \end{aligned}$$

ALGORITHM 3: EXECUTIVE AND POLLED SERVICE

G6 = SAME AS G6 EQUATION, ALGORITHM 1

$$\begin{aligned} G5 = \overline{RESET} \cdot R5\,[\overline{R6}\,(&G6 + G0 \cdot \overline{R0} + G1 \cdot \overline{R1} \cdot \overline{R0} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \\ &+ \overline{G6} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G5] \end{aligned}$$

$$\begin{aligned} G4 = \overline{RESET} \cdot R4\,[\overline{R6} \cdot \overline{R5}\,(&G6 + G5 + G0 \cdot \overline{R0} + G1 \cdot \overline{R1} \cdot \overline{R0} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \\ &+ \overline{G6} \cdot \overline{G5} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G4] \end{aligned}$$

$$\begin{aligned} G3 = \overline{RESET} \cdot R3\,[\overline{R6} \cdot \overline{R4}\,(&G6 \cdot \overline{R5} + G4 + G5 \cdot \overline{R5} + G0 \cdot \overline{R0} \cdot \overline{R5} + G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R5} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R5} \\ &+ \overline{R5} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G3] \end{aligned}$$

$$\begin{aligned} G2 = \overline{RESET} \cdot R2\,[\overline{R6} \cdot \overline{R3}\,(&G6 \cdot \overline{R5} \cdot \overline{R4} + G3 + G4 \cdot \overline{R4} + G5 \cdot \overline{R5} \cdot \overline{R4} + G0 \cdot \overline{R0} \cdot \overline{R5} \cdot \overline{R4} + G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R5} \cdot \overline{R4} \\ &+ \overline{R5} \cdot \overline{R4} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G1} \cdot \overline{G0}) + G2] \end{aligned}$$

$$\begin{aligned} G1 = \overline{RESET} \cdot R1\,[\overline{R6} \cdot \overline{R2}\,(&G6 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} + G2 + G3 \cdot \overline{R3} + G4 \cdot \overline{R4} \cdot \overline{R3} + G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} + G0 \cdot \overline{R0} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \\ &+ \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G0}) + G1] \end{aligned}$$

$$\begin{aligned} G0 = \overline{RESET} \cdot R0\,[\overline{R6} \cdot \overline{R1}\,(&G6 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + G1 + G2 \cdot \overline{R2} + G3 \cdot \overline{R3} \cdot \overline{R2} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \\ &+ \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1}) + G0] \end{aligned}$$

ALGORITHM 4: DECLINING PRIORITY AND POLLED SERVICE

G6 = SAME AS G6 EQUATION, ALGORITHM 1

G5 = SAME AS G5 EQUATION, ALGORITHM 1

G4 = SAME AS G4 EQUATION, ALGORITHM 1

$$\begin{aligned} G3 = \overline{RESET} \cdot R3\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4}\,(&G6 + G5 + G4 + G0 \cdot \overline{R0} + G1 \cdot \overline{R1} \cdot \overline{R0} \\ &+ G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G3] \end{aligned}$$

$$\begin{aligned} G2 = \overline{RESET} \cdot R2\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3}\,(&G6 + G5 + G4 + G3 + G0 \cdot \overline{R0} \\ &+ G1 \cdot \overline{R1} \cdot \overline{R0} + \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G1} \cdot \overline{G0}) + G2] \end{aligned}$$

$$\begin{aligned} G1 = \overline{RESET} \cdot R1\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R2}\,(&G6 \cdot \overline{R3} + G5 \cdot \overline{R3} + G4 \cdot \overline{R3} + G3 \cdot \overline{R3} + G2 \\ &+ G0 \cdot \overline{R0} \cdot \overline{R3} + \overline{R3} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G0}) + G1] \end{aligned}$$

$$\begin{aligned} G0 = \overline{RESET} \cdot R0\,[\overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R1}\,(&G6 \cdot \overline{R3} \cdot \overline{R2} + G5 \cdot \overline{R3} \cdot \overline{R2} + G4 \cdot \overline{R3} \cdot \overline{R2} \\ &+ G3 \cdot \overline{R3} \cdot \overline{R2} + G2 \cdot \overline{R2} + G1 + \overline{R3} \cdot \overline{R2} \cdot \overline{G6} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1}) + G0] \end{aligned}$$

circular pattern by decreasing number (R5 follows R0). The other hybrid algorithm, "declining priority and polled service," services three systems in declining priority (R6 to R4), and allocates four systems the lowest priority; R3 to R0 have equal priority and are polled in a circular pattern by decreasing number (R3 follows R0).

In each configuration, the eight inputs consist of a RESET command and seven synchronized requests. Outputs are the seven corresponding grants, each the set output of a flipflop, buffered and inverted. When activated, the RESET command negates all expressions, resetting all grant flipflops. After a synchronized request is received, the appropriate expression becomes true, and the grant flipflop is set at the following clock edge. Upon completion of the transaction, the grant is released one clock period following the clock edge that terminates its synchronized request. This interval, when the grant is true and its synchronized request is false, denotes the completion of the service cycle. If one or more synchronized requests are pending, all expressions are evaluated, and, based on the servicing sequence expressed by the Boolean statements, the next grant is issued. If at the completion of a grant there are no pending requests, then all grant flipflops are reset and the device reverts to the idle state.

When the device is idle, all synchronized requests are scanned each clock period. Detection of a single synchronized request causes a grant to be issued at the following clock edge. If two or more requests are synchronized simultaneously, the expressions must provide a hierarchical method for issuing the initial grant. If the systems are organized from highest to lowest priority, the issuing of an initial grant follows the same seniority pattern. However, if all systems polled are of equal priority, the initial grant hierarchy must be established arbitrarily; in these examples, the grant hierarchy is based on highest to lowest sequence, systems R6 to R0. All these factors are apparent in the Boolean statements that implement the various grant algorithms. Each statement is the D input of a flipflop, and when a statement is true, the corresponding flipflop becomes (or remains) set at the following clock edge, issuing (or maintaining) a grant. As grants must be issued sequentially, the statements must be interlocked to prevent multiple flipflop settings.

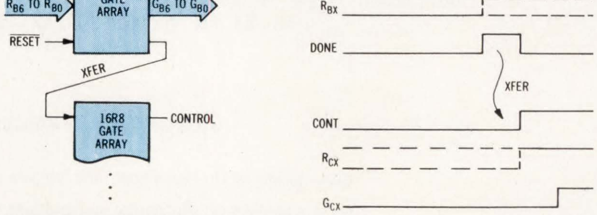
The format set forth in the Boolean expressions of algorithms 1 through 4 [compare Fig 1(d)] is used when writing all statements. It consists of four sections: a modifier divided into an external and an internal portion, a transfer expression, an idle expression, and a maintenance expression. The external modifier, which operates on the entire contents of each statement, is the $\overline{\text{RESET}}$ term ANDed with the appropriate synchronized request. This establishes the basic requirement that RESET not be issued—and that the synchronized request be present—to consider whether to issue or to maintain a grant. The internal modifier operates on the transfer and idle expressions, and is the AND of synchronized requests that must be false for a specific grant to be issued. Since in a complete or partial priority structure, the highest numbered system (R6) always takes precedence, the internal modifier for the G6 expression is nonexistent.

The transfer expression identifies the completion of a transaction through the combination of a grant with no corresponding request. In conjunction with the modifiers, the transfer expression evaluates the pending requests to determine the next sequential grant. If one or several simultaneous requests are synchronized when grants are not active, the idle expression, in conjunction with the modifiers, determines which grant will be issued according to the established priority. The maintenance expression, the set output of the grant flipflop, maintains an established grant until its external modifier becomes false.

There are at least two other practical hybrid combinations: two prioritized systems with the remaining five polled, and four prioritized systems with the remaining three polled. Expressions for these two configurations can be derived from the four examples just discussed.

Multiple-Array Configuration

The single-array configuration handles up to seven systems with a broad selection of operation modes and is suitable for a configuration that has a limited number of systems with high rates of interaction with the device. When there is a large number of systems that have low rates of interaction individually, it is necessary to scan blocks of synchronized requests rapidly in order to minimize response time, thereby maximizing device



FOR ELEMENT GIVEN CONTROL BY RESET
CONTROL = RESET + XFER + CONTROL$\cdot\overline{\text{DONE}}$

FOR ALL OTHER ELEMENTS
CONTROL = $\overline{\text{RESET}}$ (XFER + CONTROL$\cdot\overline{\text{DONE}}$)

Fig 2 Multiple-array configuration. Each of n elements can service six systems arranged in circular (ie, polled or "round-robin") configuration. RESET issues control to one element. Then, as systems are serviced, DONE and CONTROL commands pass control function among elements as shown utilization. This is accomplished by using the same 8-register programmable array device, with 6 of the registers issuing grants and the remaining 2 used to transfer the control and done commands. Devices thus organized become elements in a daisy chain configuration that is, in theory, infinitely expandable. Within the daisy chain, the element whose control flipflop is set is empowered to issue grants. Each element, while completing its last transaction, clears the grant flipflop, and, on the same clock edge, sets the done flipflop for one clock cycle. (See Fig 2.) Output of the done flipflop serves as an inhibit command within the element, and externally as a transfer (XFER) command to set the control flipflop of the next element.

Upon receipt of control, if one or more requests are pending, they are evaluated and a grant is issued at the next clock edge; if there are no requests, the clock edge instead sets the done flipflop to again transfer the control capability. Within an element, the same clock edge releases a completed grant and initiates a new grant, as was the case in the single-array configuration; among elements, there is a 2-period delay between succesive grants for sequencing of the done and control flipflops. Therefore, if the device is idle, an element that monitors six system requests is scanned each two clock cycles as the control function is sequenced through the elements.

Since this configuration can be expanded to accommodate servicing of numerous inputs, the elements are polled and equally weighted. However, within each element a protocol for responding to requests must be established; in these examples, priority is from the highest to the lowest number (R5 to R0). Algorithms 5 and 6 are variations of this configuration. In the "multiple-array polling" algorithm, the element retains control and services all requests in a declining polling sequence; control is relinquished only when there are no remaining requests. In the "multiple-array priority" algorithm, requests are serviced in a strict order of declining priority (ie, decreasing request numbers), and control is released in the absence of requests or upon completion of a device service period when no lower numbered systems have pending requests. In an application, these two configurations can be intermixed because the element interfaces are identical. The

ALGORITHM 5: MULTIPLE-ARRAY POLLING

$$\begin{aligned}\mathrm{G5} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R5\, [\overline{R0}\, (G0 + G1 \cdot \overline{R1} + G2 \cdot \overline{R2} \cdot \overline{R1} + G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1}} \\ & \mathrm{+ G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1}) + \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0} + G5]}\end{aligned}$$

$$\begin{aligned}\mathrm{G4} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R4\, [\overline{R5}\, (G5 + G0 \cdot \overline{R0} + G1 \cdot \overline{R1} \cdot \overline{R0} + G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}} \\ & \mathrm{+ G3 \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} + \overline{G5} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G4]}\end{aligned}$$

$$\begin{aligned}\mathrm{G3} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R3\, [\overline{R4}\, (G4 + G5 \cdot \overline{R5} + G0 \cdot \overline{R0} \cdot \overline{R5} + G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R5}} \\ & \mathrm{+ G2 \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R5} + \overline{R5} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0}) + G3]}\end{aligned}$$

$$\begin{aligned}\mathrm{G2} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R2\, [\overline{R3}\, (G3 + G4 \cdot \overline{R4} + G5 \cdot \overline{R5} \cdot \overline{R4} + G0 \cdot \overline{R0} \cdot \overline{R5} \cdot \overline{R4}} \\ & \mathrm{+ G1 \cdot \overline{R1} \cdot \overline{R0} \cdot \overline{R5} \cdot \overline{R4} + \overline{R5} \cdot \overline{R4} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G1} \cdot \overline{G0}) + G2]}\end{aligned}$$

$$\begin{aligned}\mathrm{G1} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R1\, [\overline{R2}\, (G2 + G3 \cdot \overline{R3} + G4 \cdot \overline{R4} \cdot \overline{R3} + G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3}} \\ & \mathrm{+ G0 \cdot \overline{R0} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} + \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G0}) + G1]}\end{aligned}$$

$$\begin{aligned}\mathrm{G0} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R0\, [\overline{R1}\, (G1 + G2 \cdot \overline{R2} + G3 \cdot \overline{R3} \cdot \overline{R2} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2}} \\ & \mathrm{+ G5 \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{G5} \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1}) + G0]}\end{aligned}$$

$$\mathrm{DONE = \overline{RESET} \cdot CONT \cdot \overline{DONE} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}}$$

CONT = CONTROL (SEE FIG 2)

ALGORITHM 6: MULTIPLE-ARRAY PRIORITY

$$\mathrm{G5 = \overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot \overline{G4} \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0} \cdot R5}$$

$$\mathrm{G4 = \overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot \overline{G3} \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0} \cdot R4\, [\overline{R5} + G4]}$$

$$\mathrm{G3 = \overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot \overline{G2} \cdot \overline{G1} \cdot \overline{G0} \cdot R3\, [\overline{R4}\, (\overline{R5} + G4) + G3]}$$

$$\mathrm{G2 = \overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot \overline{G1} \cdot \overline{G0} \cdot R2\, [\overline{R3}\, (\overline{R5} \cdot \overline{R4} + G4 \cdot \overline{R4} + G3) + G2]}$$

$$\begin{aligned}\mathrm{G1} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot \overline{G0} \cdot R1\, [\overline{R2}\, (\overline{R5} \cdot \overline{R4} \cdot \overline{R3} + G4 \cdot \overline{R4} \cdot \overline{R3}} \\ & \mathrm{+ G3 \cdot \overline{R3} + G2) + G1]}\end{aligned}$$

$$\begin{aligned}\mathrm{G0} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot R0\, [\overline{R1}\, (\overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2}} \\ & \mathrm{+ G3 \cdot \overline{R3} \cdot \overline{R2} + G2 \cdot \overline{R2} + G1) + G0]}\end{aligned}$$

$$\begin{aligned}\mathrm{DONE} = {} & \mathrm{\overline{RESET} \cdot \overline{DONE} \cdot CONT \cdot \overline{R0}\, [\overline{R1}\, (\overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} + G4 \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2}} \\ & \mathrm{+ G3 \cdot \overline{R3} \cdot \overline{R2} + G2 \cdot \overline{R2} + G1) + G0]}\end{aligned}$$

CONT = CONTROL (SEE FIG 2)

differences are within the elements—ie, the methods used when evaluating requests to issue grants and when generating the transfer command. Since only one element can have a set control flipflop and the associated authority to issue grants, one control flipflop must be set, and all others reset, during initialization. During implementation, the system start of poll (established by RESET) must be selected, and each element's control equation implemented accordingly. (See Fig 2.)

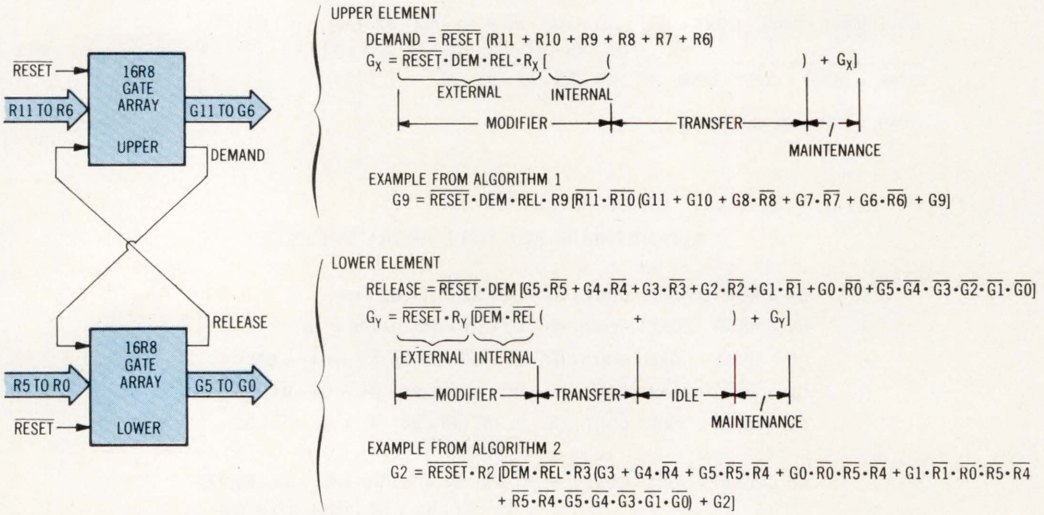
The Boolean statements in algorithms 5 and 6 are configured in the format shown in Fig 1(d). In algorithm 5, the external modifier has two additional terms, CONT and DONE, both establishing that the element has control. The remainder of the terms is similar in content to the terms in algorithm 2, and, with the exception of the idle expression, also similar in concept. Since an element does not retain control in the idle state, this term instead establishes the initial grant upon receipt of the control function. Subsequent grants are issued through the transfer expression, and when all requests are satisfied, the done flipflop is set for one period, initiating a transfer of control to the next element.

Hybrid Configuration

Single- and multiple-array configurations have limitations. The single-array concept services only seven systems, but offers flexibility in configuring the response patterns. Conversely, the multiple-array configuration can handle a large (theoretically unlimited) number of systems, but is not flexible in configuring response patterns because the control function must cycle through elements in a prescribed sequence. By restructuring the control lines, designers can interconnect elements in a hierarchical fashion, both increasing the number of systems serviced and providing service flexibility. An example that consists of two elements, each servicing six systems, is shown in Fig 3. The two elements are labeled "upper" and "lower" to denote their relative priorities. Each element has a control flipflop whose output is an input to the other element.

The control flipflop of the upper element is set whenever it has a synchronized request, and is a DEMAND for control. The control flipflop of the lower element is set when it receives a demand and does not have an active grant; it is a RELEASE of control. Thus, the upper element DEMANDs and receives control when it has a request. When all upper element requests are satisfied, the demand flipflop is reset and control shifts to the lower element by default. The control equations for the upper and lower elements are shown in Fig 3, along with the format for the grant equations and one sample grant equation for each element. Because the equations for the hybrid configuration are similar to those for the single-array configuration, the grant equations are modifications of those shown in algorithms 1 through 4. When in the idle state, the default location for control is in the lower element; therefore, the equation for the upper element does not require an idle section.

Efficient transfer of control and prevention of inadvertent simultaneous grant issuance during the transition sequence are primary considerations in arbiter



UPPER ELEMENT

$$\mathrm{DEMAND} = \overline{\mathrm{RESET}}\,(R11 + R10 + R9 + R8 + R7 + R6)$$

$$G_X = \underbrace{\overline{\mathrm{RESET}}\cdot \mathrm{DEM}\cdot \mathrm{REL}\cdot R_X}_{\text{EXTERNAL}}\,[\underbrace{\qquad\qquad}_{\text{INTERNAL}}(\qquad\qquad\qquad) + G_X]$$

EXAMPLE FROM ALGORITHM 1

$$G9 = \overline{\mathrm{RESET}}\cdot \mathrm{DEM}\cdot \mathrm{REL}\cdot R9\,[\overline{R11}\cdot\overline{R10}\,(G11 + G10 + G8\cdot\overline{R8} + G7\cdot\overline{R7} + G6\cdot\overline{R6}) + G9]$$

LOWER ELEMENT

$$\mathrm{RELEASE} = \overline{\mathrm{RESET}}\cdot \mathrm{DEM}\,[G5\cdot\overline{R5} + G4\cdot\overline{R4} + G3\cdot\overline{R3} + G2\cdot\overline{R2} + G1\cdot\overline{R1} + G0\cdot\overline{R0} + \overline{G5}\cdot\overline{G4}\cdot\overline{G3}\cdot\overline{G2}\cdot\overline{G1}\cdot\overline{G0}]$$

$$G_Y = \underbrace{\overline{\mathrm{RESET}}\cdot R_Y}_{\text{EXTERNAL}}\,[\underbrace{\overline{\mathrm{DEM}}\cdot\overline{\mathrm{REL}}}_{\text{INTERNAL}}\,(\qquad\qquad + \qquad\qquad) + G_Y]$$

EXAMPLE FROM ALGORITHM 2

$$G2 = \overline{\mathrm{RESET}}\cdot R2\,[\overline{\mathrm{DEM}}\cdot\overline{\mathrm{REL}}\cdot\overline{R3}\,(G3 + G4\cdot\overline{R4} + G5\cdot\overline{R5}\cdot\overline{R4} + G0\cdot\overline{R0}\cdot\overline{R5}\cdot\overline{R4} + G1\cdot\overline{R1}\cdot\overline{R0}\cdot\overline{R5}\cdot\overline{R4} + \overline{R5}\cdot\overline{R4}\cdot\overline{G5}\cdot\overline{G4}\cdot\overline{G3}\cdot\overline{G1}\cdot\overline{G0}) + G2]$$

Fig 3 Hybrid configuration. Two elements have hierarchical structure. Upper element demands control when request is pending, thereby preventing lower element from issuing grants and gaining control when lower element becomes idle. Modified grant expression format and typical grant expression appear for each element. Release expression is also shown. Each element offers full flexibility shown in algorithms 1 to 4

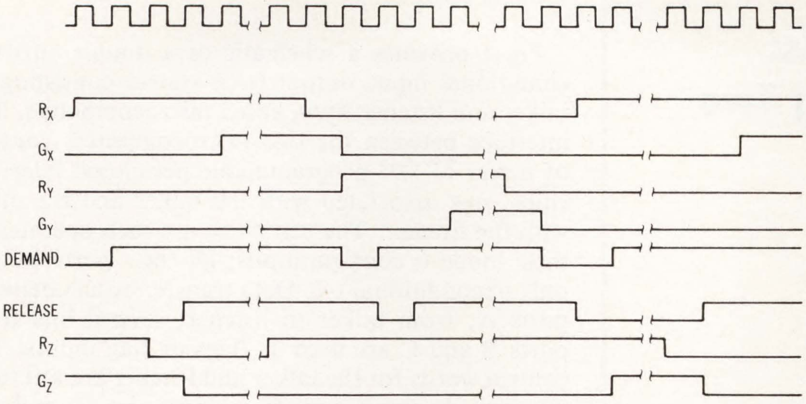


Fig 4 Hybrid configuration timing. Diagram shows timing relationship as control function passes between upper and lower elements. At left, control passes from lower element to upper element upon completion of G_Z. In second sector, upper element releases control and reestablishes demand during same clock period (adverse situation). Lower element with pending request must reinitiate release, causing 3-period delay between grants. In two right sectors, upper element releases control and reestablishes demand one clock period later. Lower element issues grant for its pending request and releases control upon completion of service

design. Control equations and modifier sections of the grant equations, respectively, fulfill these design requirements. Three transitional sequences for hybrid configuration are shown in the timing diagram. (See Fig 4.)

Summary

The increased desirability of sharing resources among several systems has increased the requirements for arbiters that can function independently. Such arbiters enhance the profitability of shared resource data processing systems. A versatile Boolean statement format can implement efficient control protocol and grant algorithms in field programmable logic. The flexibility and logic density of register arrays can facilitate efficient custom arbiter implementation.

Bibliography

K. Søe Højberg, "Queue Handling Arbiter Solves Shared Resource Conflicts," *Computer Design,* Nov 1979, pp 129-135

James Nadir and Bruce McCormick, "Bus Arbiter Streamlines Multiprocessor Design," *Computer Design,* June 1980, pp 103-109

Emil Petriu, "N-Channel Asynchronous Arbiter Resolves Resource Allocation Conflicts," *Computer Design,* Aug 1980, pp 126-132

About the Author:

Alan W. Bentley is a design specialist, responsible for the technical development of a high speed data processing and display system at Cubic Corporation. He is also an instructor in the Engineering Department of San Diego Community College. He has a BS degree in electrical engineering from Tufts University, an MBA from United States International University, and an MA from San Diego State University.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 707 **Average 708** **Low 709**

Interfacing Fundamentals: 2-Wire Handshake Using Two Microcomputers

Peter R. Rony
Department of Chemical Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

Though the IEEE 488 bus standard employs a 3-wire handshake procedure to synchronize data transfer between a talker (source, transmitter) and a listener (acceptor, receiver), it is instructive to examine experimentally the behavior of a 2-microcomputer system that uses a simpler *2-wire interlocked handshake* procedure. The 3-wire handshake is for applications in which one output port is transferring the same data simultaneously to many input ports, whereas the 2-wire handshake is useful for transferring data between a microcomputer and a single input/output (I/O) device.[1]

Fig 1 provides a schematic of a double-buffered conditional input/output (I/O) system consisting of talker and listener 8080A based microcomputers. The interface between the two microcomputers consists of a pair of 8255 programmable peripheral interface chips, one associated with the talker and the other with the listener. The 8255 chips are each operated in their mode 0 configurations; all their ports exhibit only unconditional I/O. Data transfer occurs between ports A, from talker to listener; several bits from ports B and C are used as flags or flag inputs. The control words for the talker and listener are 82H (output port A, input port B, output port C) and 92H (input port A, input port B, output port C), respectively.

Fig 2 provides versions of the talker and listener flow charts that are simplified representations of the familiar IEEE 488 handshake flowchart.[2-4] The NRFD signal is omitted because we are concerned only with a 2-wire (or 2-signal) handshake procedure. The basic characteristics of the flowchart can be discussed with the aid of the timing diagrams for the signals DAV and NDAC, shown in Fig 3. DAV is the mnemonic for the data available signal, and NDAC is the mnemonic for the not data accepted signal. The four edges, shown as 1 through 4 in Fig 3, are the basis for understanding the 2-wire handshake procedure. Each edge is tested by a software test loop either in the talker or listener software (two loops are associated

(continued on page 158)

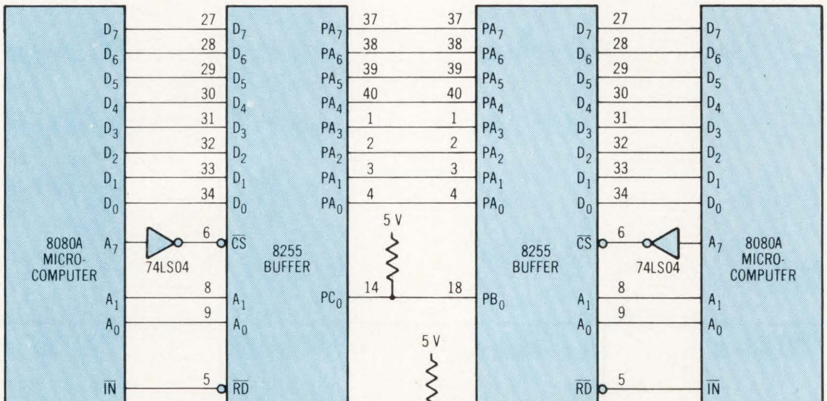
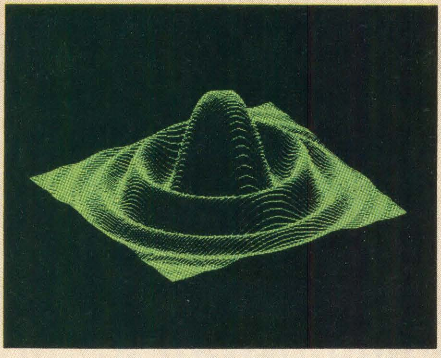


Fig 1 2-microcomputer double-buffered conditional I/O circuit. Depending upon control words chosen for two 8255 chips, data flow can be either from left to right, or right to left. In Fig 4, which depicts left to right data transmission, PB0/PC0 pair of bits is for DAV signal; PB2/PC2 pair is for NDAC. 1k Ω pull-up resistors are used for flag outputs PC0 and PC2

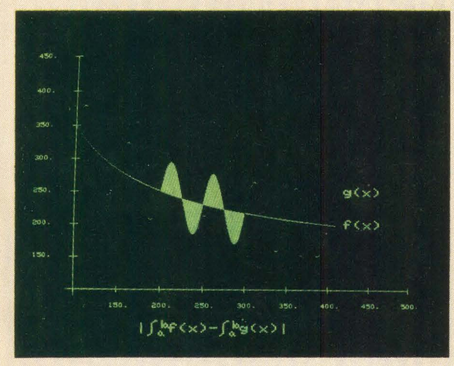


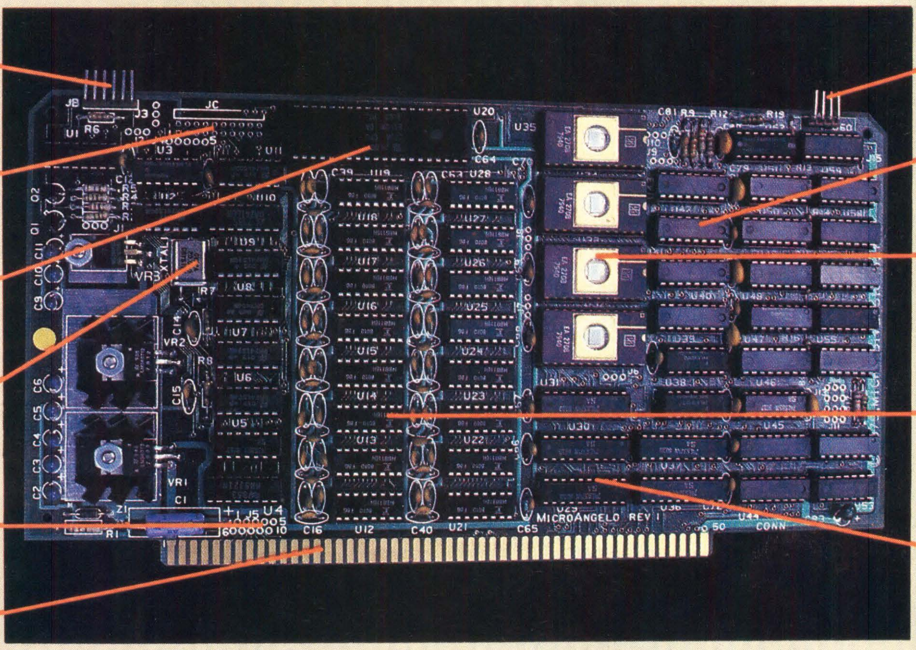
MICROANGELO™

HIGH RESOLUTION GRAPHICS SINGLE BOARD COMPUTER
512 x 480 RESOLUTION MONOCHROME DISPLAY

by

SCION
CORPORATION





RS-170 composite or direct drive output

Local or external sync generation

4 or 5 Mhz Z80 microprocessor

60 hertz real-time clock

8 level interrupt tie-in

IEEE S100 bus compatible

Light pen interface

Time multiplexed refresh

4K resident Screenware™ Pak I operating system

32K RAM isolated from host address space

High speed communications over parallel bus ports

Screenware™ Pak I

A 4K byte operating system resident in PROM on MicroAngelo.™ Pak I emulates an 85 character by 40 line graphics terminal and provides over 40 graphics commands. Provisions exist for user-defined character sets and directly callable user extensions to Screenware Pak I.

TEKEM™

A Tektronix 4010/4014 graphics terminal emulator which is fully PLOT-10 and CP/M* compatible.

Screenware™ Pak II

An optional software superset of Pak I which adds circle generation, polygon flood, programmable split screen for separate graphics and terminal I/O, relative coordinates, faster vector and character plotting, a macro facility, full UCSD Pascal compatibility, and more.

SCION CORPORATION
8455-D Tyco Road • Vienna, Va. 22180
(703)827-0888 • TWX: 710-831-9087

CIRCLE 74 ON INQUIRY CARD

---

*CP/M is a registered trademark of Digital Research Corp.

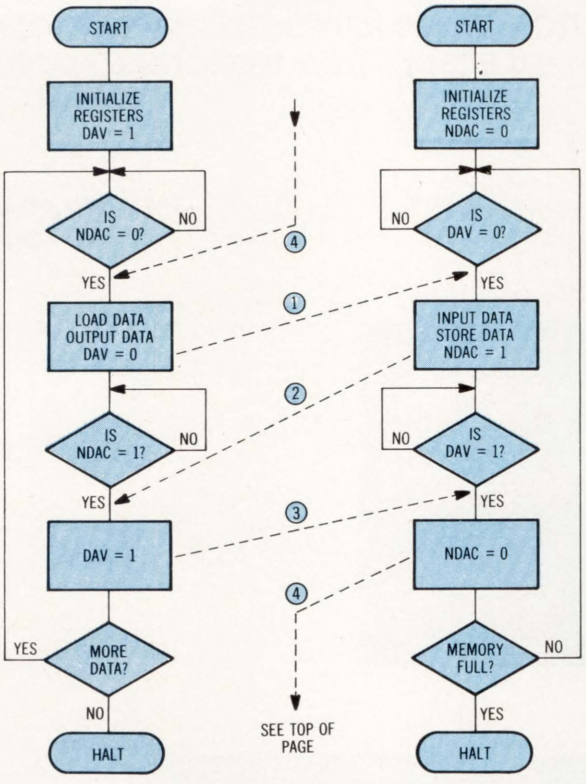


Fig 2 Flowcharts for 2-wire handshake procedure. Talker is on left, and listener is on right. Flowcharts do not include setting, clearing, and testing of NRFD signal, which is employed in 3-wire handshake procedure

with the talker, and two with the listener). The information that these edges convey can be summarized as

① talker informs listener that data are available;
② listener acknowledges that is has accepted the data;
③ talker informs listener that data no longer are valid; and,
④ listener acknowledges that it will not accept data again until DAV = 0.

The talker tests for edges②and④,while the listener tests for edges①and③.This sequence of tests, along with the associated signal lines, comprise the 2-wire handshake.

The dotted arrows in Fig 2 match the edges shown in Fig 3. As shown in Fig 2, the talker cannot load or output data until NDAC = 0, and the listener cannot input or store data until DAV = 0. After data is transferred from talker to listener, the two devices inform and acknowledge, respectively, that valid data is no longer present between ports A. Observe the symmetry in the talker and listener flowcharts.

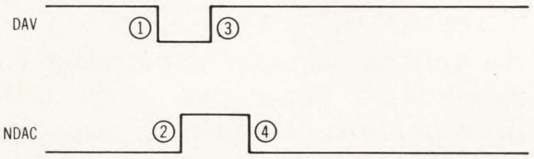


Fig 3 Timing diagrams for 2-wire handshake procedure. To understand the basis for 2-wire handshake, focus on four edges, shown as ① through ④. DAV flag is set and reset by talker software, and NDAC flag by set and reset listener software

Detailed listings for a pair of 8080A based microcomputers exchanging a block of data from one memory to the other are provided in Fig 4. A 2-wire handshake protocol is used. (Compare Fig 4 with Fig 2.) Sixty-four data bytes, starting at memory location 0380H, are transferred byte by byte from the talker to the same set of memory locations in the listener. The instruction sequences at the end of the programs—MOV A,L/XRI COH/JNZ 03XXH—test for the completion of the memory to memory block transfer process. For both the talker and listener, the initialization of the stack pointer, memory address pointer, 8255 control register, and output port C occurs in the first fourteen program bytes.

The various input, output, and mask bytes that appear in the software in Fig 4 are summarized in Fig 5. For the talker, the 8255 control register configures the ports as output port A, input port B, and output port C; for the listener, the port configuration is input port A, input port B, and output port C. The talker

(continued on page 160)

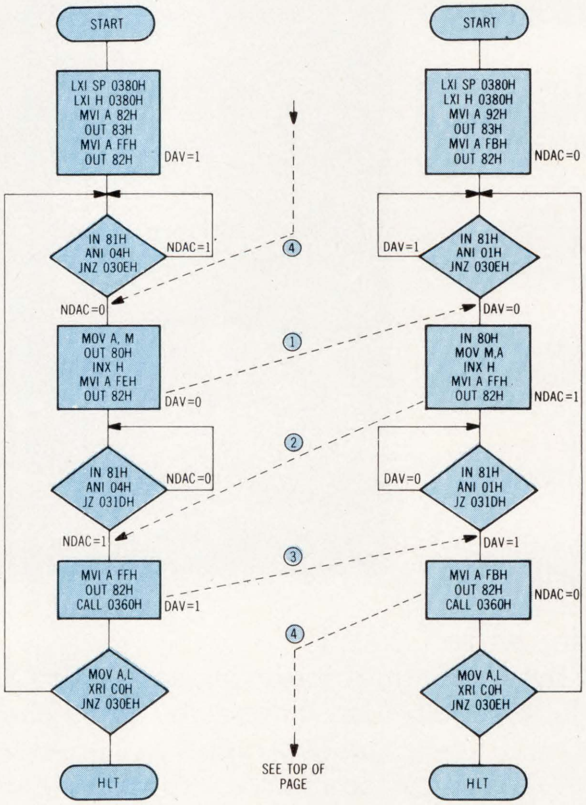
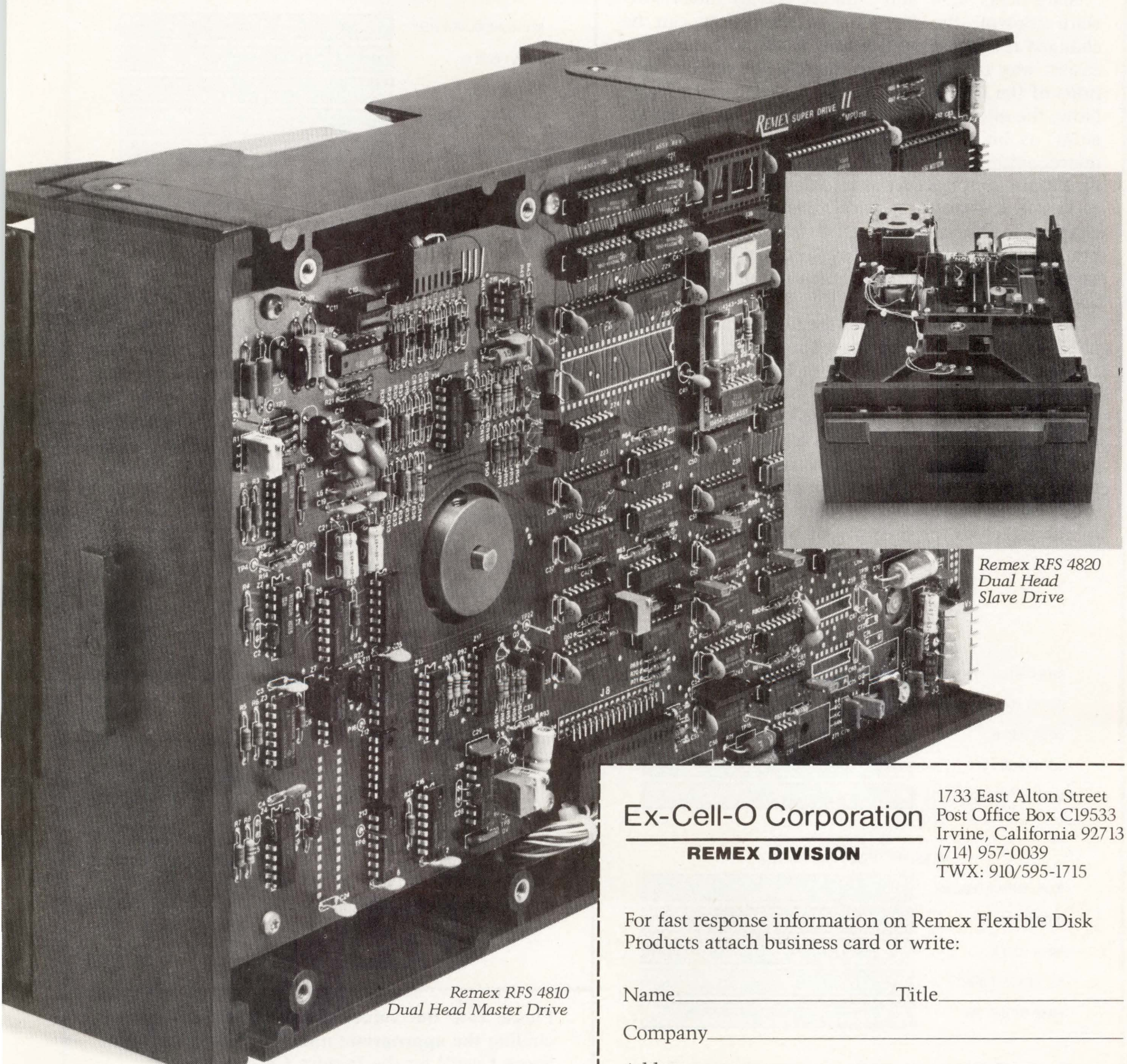


Fig 4 Flowcharts and assembly language programs. Talker is on left, and listener is on right. Programs correspond to data flow from left to right in Fig 1. Definitions of registers, ports, and mask bytes are given in Fig 5

Remex Intelligent Flexible Disk Drives.

On-Board Controller. Non-Stop Economy.



Remex RFS 4820
Dual Head
Slave Drive

Remex RFS 4810
Dual Head Master Drive

Write or Call for Specifications and Delivery.

Ex-Cell-O Corporation
REMEX DIVISION

1733 East Alton Street
Post Office Box C19533
Irvine, California 92713
(714) 957-0039
TWX: 910/595-1715

For fast response information on Remex Flexible Disk Products attach business card or write:

Name________________ Title________________

Company________________________________

Address________________________________

City________________ State________ Zip________

Phone________________________________

outputs the DAV flag (bit PO$_0$) and inputs the NDAC flag (bit PB$_2$). For the listener, it is just the opposite: the NDAC flag (bit PC$_2$) is output, and the DAV flag (bit PB$_0$) is input. In the test loops in Fig 4, the mask bytes are 04H for the talker and 01H for the listener. The device codes for the 8255 ports or registers are 80H (port A), 81H (input port B), 82H (output port C), and 83H (control register). The OUT 80H and IN 80H instructions output and input the data byte that is being transferred from the talker to the listener.

Since ports A, B, and C on the 8255 are under software control, the direction of data flow can be changed through modifications in the software. The easiest way to do this is to interchange the bit positions of the DAV and NDAC flags, as shown in Fig 6. Now, the microcomputer on the left in Fig 1 outputs NDAC as bit PC$_0$, and inputs DAV as bit PB$_2$. The microcomputer on the right in Fig 1 inputs NDAC as bit PB$_0$ and outputs DAV as bit PC$_2$. The MOV A,M/OUT 80H and IN 80H/MOV M,A pairs of instructions are interchanged in the software of the two microcomputers, but the mask bytes in the four test loops remain the same. The control words for the 8255 control registers and interchanged as well.

As in previous columns,[5,6] the rate of data transfer has been measured, in this case for the circuit given in Fig 1 plus the software given in Fig 4. For a talker operating at 0.75 MHz and a listener operating at 0.75 MHz, 20.37 ms were required to transfer a block of 64 bytes of data. This figure corresponds to 318.3 μs/data byte. The CALL 0360H instruction in each program permits the testing of the effect of time delay loops on the rate of data transfer from the memory of the talker to the memory of the listener. With a 9.53 ms delay in the listener, 617.2 ms, or 9.64 ms/byte, were required to accomplish the same data transfer. A 9.50 ms delay in the talker, but no delay in the listener, resulted in an overall time of 629.6 ms, or 9.84 ms/byte. Finally, when 9.50 ms and 9.53 ms delays were present in the talker and listener, respectively, the rate of data transfer was 9.79 ms/byte.

TALKER
(MICROCOMPUTER ON LEFT IN FIG 1)

8255 CONTROL REGISTER:	1	0	0	0	0	0	1	0
OUTPUT PORT C:	X	X	X	X	X	X	X	DAV
INPUT PORT B:	X	X	X	X	X	NDAC	X	X
SET OR RESET DAV:	1	1	1	1	1	1	1	0/1
MASK ALL BUT NDAC:	0	0	0	0	0	1	0	0

LISTENER
(MICROCOMPUTER ON RIGHT IN FIG 1)

8255 CONTROL REGISTER:	1	0	0	1	0	0	1	0
OUTPUT PORT C:	X	X	X	X	X	NDAC	X	X
INPUT PORT B:	X	X	X	X	X	X	X	DAV
SET OR RESET NDAC:	1	1	1	1	1	0/1	1	1
MASK ALL BUT DAV:	0	0	0	0	0	0	0	1

Fig 5 Definitions of registers, ports, and mask bytes. Data flow is from left to right in Fig 1. Corresponding software listings are given in Fig 4

TALKER
(MICROCOMPUTER ON RIGHT IN FIG 1)

8255 CONTROL REGISTER:	1	0	0	0	0	0	1	0
OUTPUT PORT C:	X	X	X	X	X	DAV	X	X
INPUT PORT B:	X	X	X	X	X	X	X	NDAC
SET OR RESET DAV:	1	1	1	1	1	0/1	1	1
MASK ALL BUT NDAC:	0	0	0	0	0	0	0	1

LISTENER
(MICROCOMPUTER ON LEFT IN FIG 1)

8255 CONTROL REGISTER:	1	0	0	1	0	0	1	0
OUTPUT PORT C:	X	X	X	X	X	X	X	NDAC
INPUT PORT B:	X	X	X	X	X	DAV	X	X
SET OR RESET NDAC:	1	1	1	1	1	1	1	0/1
MASK ALL BUT DAV:	0	0	0	0	0	1	0	0

Fig 6 Definitions of registers, ports, and mask bytes. Data flow is from right to left in Fig 1 (talker and listener have been interchanged)

References

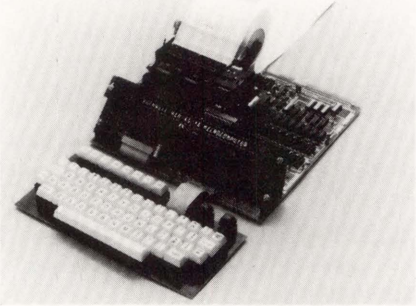
1. D. L. Hillman, "Intelligent Buffer Reconciles Fast Processors and Slow Peripherals," *Electronics,* Sept 11, 1980, pp 131-135
2. G. R. Samsen and R. D. Hudson, "Bus Adapter Simplifies Interprocessor Communication," *Computer Design,* Dec 1980, pp 119-124
3. R. M. Williams, "LSI Chips Ease Standard 488 Bus Interfacing," *Computer Design,* Oct 1979, pp 123-131
4. J. Pieper and R. J. Grossi, "LSI Streamlines Instrument Interface with Standard IEEE-488 Bus," *Electronics,* Apr 26, 1979, pp 145-150
5. P. R. Rony, "Interfacing Fundamentals: Conditional I/O Using Two Microcomputers," *Computer Design,* Aug 1980, pp 136-138
6. P. R. Rony, "Interfacing Fundamentals: Bidirectional I/O Using Two Semaphores," *Computer Design,* April 1981, pp 184-188

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Card" on the Inquiry Card.

High 722 **Average 723** **Low 724**


CONTROL 1
SHIFT
CONTROL 2

Modular system combines μcomputer, printer, display, and keyboard



Modular board level microcomputer system. AIM 65/40, advanced version of AIM 65 microcomputer, is available from Rockwell International as complete system or as individual computer and intelligent peripheral modules

A modular board level microcomputer system for industrial and scientific applications, AIM 65/40 is available as a complete system or as individual computer and intelligent peripheral modules from Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803. The system, an advanced version of the company's AIM 65 microcomputer (see *Computer Design,* Dec 1978, p 136), is composed of four modules: an R6502 based single-board computer with onboard expansion to 65k bytes of memory, a printer with full graphic 280 x N-dot matrix and 40-column alphanumeric display, and a full ASCII keyboard with user assignable function keys.

The Series 1000 single-board computer module features system address expansion up to 131k bytes, with 65k bytes of onboard memory, up to 48k bytes of RAM, and up to 32k bytes of ROM or EPROM. Extensive I/O capability provides an RS-232-C asynchronous communications interface channel with programmable data rates of up to 19,200 baud for terminals or modems, plus a 20-mA current loop TTY interface, dual audio cassette interfaces, two user definable 8-bit parallel ports with handshake control, and an 8-bit serial shift register. Three additional directly programmable 8-bit parallel ports are provided by the module interface to keyboards, displays, and printer modules. The printer connector is compatible with the Centronics parallel interface. Six-level priority interrupt logic and six 16-bit multimode timers are also included. ROM resident software provides I/O drivers for the intelligent peripherals.

A buffered system bus accommodates offboard expansion using the company's RM65 microcomputer modules that include intelligent peripheral controllers of 5.25 or 8" (13.34- or 20-cm) floppy discs, CRT monitors, and the IEEE-488 instrumentation bus. Serial and parallel communications interfaces and a selection of RAM, ROM, and P/ROM memory options providing up to 128k bytes of memory expansion are also offered.

Model 0600 graphics printer module, consisting of an intelligent microprocessor controller integrated with the printer mechanism, operates in two modes. Character mode operation prints upper- and lowercase ASCII characters, mathematical symbols, and a semigraphic character font formatted as 40 char/line at 240 lines/min. Full graphics mode outputs any data pattern desired as a 280 x N-dot matrix. This freestanding peripheral includes microprocessor controller, user changeable character generator ROM, thermal head drivers, motor control, and parallel handshake ASCII interface.

A standalone alphanumeric display module, model 0400 features a vacuum fluorescent 40-character alphanumeric display, and operates from a single 5-V power source. It includes a microprocessor controller for display of alphanumeric, special, and limited graphic characters, parallel handshake ASCII interface, and support circuitry. Special control commands permit variable display timing, cursor control, auto-scroll, and character blinking.

The keyboard module, model 0200, provides a terminal style alphanumeric and special character keyboard matrix with 64 keys, including locking ALL CAPS, control, and eight user definable function keys. ATTN, RESET, and PAPER FEED keys have dedicated lines to the interface connector.

All four modules are integrated into a complete microcomputer system in the series 5000. It incorporates ROM resident monitor software that controls the system with single keystroke, self-prompting commands, and supports software development with assembler, debug, and control commands. A multifile text editor supports both line and screen editing functions. Optional languages include a fully symbolic R6500 assembler and BASIC. Forth, Pascal, and PL/65 software packages are in development.

Circle 461 on Inquiry Card

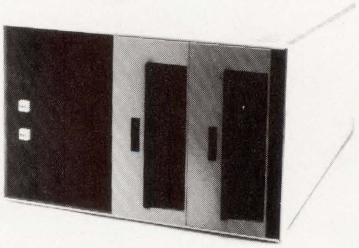
Alternate source pact for M68000 family is arranged

Signetics/Philips, 811 E Arques Ave, Sunnyvale, CA 94086, has elected to alternate source the M68000 microprocessor family of Motorola Semiconductor Produts, Inc, Phoenix, Ariz; the agreement covers circuits, hardware, software, and support tools. Signetics/Philips will produce pin for pin compatible M68000 family products as well as develop new products that will be manufactured by the participants.

At least three Signetics peripheral data communication chip designs will be added to the line. Both companies will produce software including operating systems, language processors, and application packages, as well as development system tools. During the next two years, 12 or more additions to the line are anticipated.

Circle 462 on Inquiry Card

Modular STD BUS μcomputer runs CP/M operating system



Designed for the Mostek/Prolog STD BUS, the modular XM800 computer runs CP/M and combines a 16-slot card cage plus terminated motherboard, power supply, and dual 8" (20-cm) floppy disc drives in a single metal enclosure. The system, manufactured by Xitex Corp, 9861 Chartwell Dr, Dallas, TX 75243, can be configured to specific applications using a wide range of peripheral and I/O cards from over 35 manufacturers.

The system is normally supplied with a 5-output linear power supply, but is also available with a switching power supply, including VDE0875 approved rf filtering. For worldwide use, the computer is capable of both 120/240-Vac, 50/60-Hz operation. Double Eurocard and Multibus versions will be offered this year.

Circle 463 on Inquiry Card

"Quantum fully intends to be the leader in 8-inch Winchester drives by 1982."

—Jim Patterson, President Quantum Corporation

We have the very best people.
People whose impressive credentials inspired a level of financial backing seldom seen in a company so young. A management team with 110 years' experience and 20 patents in computer peripherals. The same people who developed the first generation of low-cost Winchester drives. And the second. People who have demonstrated the ability not only to design a superior drive, but to produce it. In high volume. At low-cost. So you can count on reliable delivery of high-quality drives . . . always at a competitive price!

The very best drives.
Our Q2000 series of 10, 20, 30 and 40-megabyte drives gives you up to four times the capacity of the current industry-standard Shugart SA1000, at a lower cost-per-megabyte. And all four are compatible with the SA1000 and with standard 8-inch floppy disk drives.

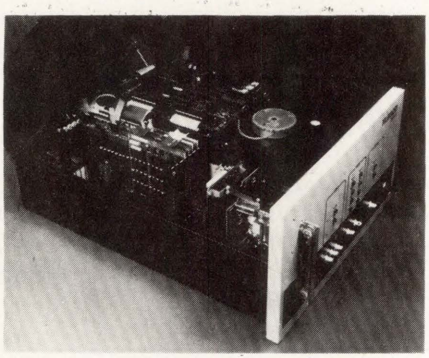
Major OEMs have already given the Q2000 series their highest vote of confidence: orders. To stay competitive in today's exploding market for low-cost computer systems, you need to know about Quantum 8-inch Winchester drives now.

For details, call Bob Teal, Quantum Corporation, 2150 Bering Drive, San Jose, CA 95131, phone (408) 262-1100.

QUANTUM ***Driving down the cost of quality.***

CIRCLE 77 ON INQUIRY CARD

LSI-11 packaged system runs DEC software without modification



LSI-11/23 packaged system. XL2300, from Xylogics, Inc, emulates Digital Equipment Corp hardware, allowing standard DEC operating systems and application packages for DEC to run without modification

An LSI-11/23 based system from Xylogics, Inc, 42 Third Ave, Burlington, MA 01803, XL2300 integrates Digital Equipment Corp's microprocessor, memory, and communications ports with the company's Winchester disc and tape cartridge subsystems into a compact tabletop or rackmount cabinet. The OEM package provides high performance and reliability, and emulates DEC hardware; standard DEC operating systems and application packages for DEC run without modification.

Included in the system are a 96k- to 256k-byte DEC RAM; a 24M-byte, 8″ (20-cm) Winchester disc subsystem with full RL02 emulation; and a 17M-byte 3M DC 300XL tape cartridge subsystem with full TU-10 emulation and full error checking for high speed file structured storage and backup. Up to eight DL-11 RS-232 communications ports, a 12-slot backplane that is structurally identical to DEC's Q-bus, power supply, ventilation, diagnostics, and all cables required for operation are also provided.

The system runs all DEC operating systems, including RT-11, RSX-11M, and RSTS/E; DEC compatible applications software and diagnostics will run without modification. The system also supports third party software not previously available on LSI-11, including TAPS, WORD-11, UNIX, and others. A built-in operator-initiated reliability test is executed when the system is powered on or booted.

A high performance 8″ (20-cm) Winchester disc drive offers 20.8M bytes of storage. The disc subsystem provides for full emulation of a DEC RLV11 with four RL01 disc drives or an RLV21 with two RL02 disc drives.

The tape subsystem uses a 3M DC 300 compatible tape cartridge drive with full emulation of a DEC TM11/TU10. The start-stop tape drive allows either file or volume copies, with full data error checking, using read-after-write and CRC techniques. Cartridge capacity is 17M bytes.

Up to eight RS-232 asynchronous communication ports that can be strapped to run at 110 to 9600 baud are available. Any DEC or equivalent communications peripheral supported by the operating system can be attached.

Circle 464 on Inquiry Card

Add-in memory allows μcomputers to produce graphic images on CRT

Packaged in a dual-height module that plugs directly into the Q-bus, model VCG-Q, from Peritek Corp, Computer Technology Div, 3014 Lakeshore Ave, Oakland, CA 94610, is a direct access color graphics add-in memory for Digital Equipment Corp's LSI-11/2 and /23 16-bit microcomputers. The module contains all the hardware necessary to connect these computers to a standard color or monochrome CRT monitor and produce a color or gray-scale graphic image.

Image format can be 512 x 512 x 4 or 512 x 640 x 3. Up to 16 of 4096 different colors or gray-scale levels can be displayed concurrently. Scan is interlaced, and vertical frame rate is programmable for 50- or 60-Hz operation. The graphic image can be initialized or cleared without processor attention.

Frame buffer memory is accessed by the CPU in two different ways. The image can be accessed, one raster line at a time, through data registers located in the I/O page. A control register determines which of the 512 lines is currently being accessed. Alternately, the extended addressing capability of the LSI-11/23 can be utilized to address the entire frame buffer directly as 64k words of memory. This method allows for rapid transfer of image data between the add-in memory and disc. Both methods allow multiple pixels to be read or written with a single memory reference, for efficient pattern filling, character generation, and other operations that require accessing adjacent pixels.

Incorporated in the design of the unit, 22-bit addressing allows the user to take advantage of the LSI-11/23's capabilities, while maintaining compatibility with other LSI-11 processors. The board's memory section can be set to any 64k-word boundary within the 22-bit space. A "unit select" feature allows access to multiple frame buffers sharing the same address space.

For first time users, a package of maintenance and utility software is included. Applications software available separately includes CSP-I, an entry-level color graphics subroutine package that provides joint and vector plotting, software generated graphics cursor and character output, erase capability, and readback of image data. A more advanced package, CSP-II includes CSP-I functions, plus circle, arc, and rectangle generation, pattern fill, selective erase, and other advanced graphic functions.

Circle 465 on Inquiry Card

Memory mapped board provides video display system for S-100 computers

VB3 memory mapped board provides a flexible video display system for S-100 bus computers. The 48-line x 80-character display features upper- and lowercase characters with true descenders. The board is available from SSM Microcomputer Products, Inc, 2190 Paragon Dr, San Jose, CA 95131.

In addition to the video RAM, the board features a second RAM block that contains attribute bytes allowing any character to appear as a standard alphanumeric upper/lowercase font or user-programmed font, in low intensity, reverse video, as well as added print functions such as underscore, strikethrough, thin line, or dot graphics. Since the board is memory mapped, its banked switching occupies memory only when activated. The board generates both U.S. and European TV rates and includes a keyboard input.

Software for the board includes a CP/M compatible driver routine and a terminal simulator routine. Software controlled options include timing, top and bottom margins, horizontal position, inverted video, (2 x 4) graphic character, one level of gray, blinking character, underline, blank out, and cursor. A 24-line x 80-character version of the board is also available.

Circle 466 on Inquiry Card

Multi-user system offers complete hardware/software development facilities

Multi-AMPL systems for microprocessor prototyping and development allow a team of designers to utilize a single computer for hardware and software development, eliminating the need for a CPU and software for each user. Three versions, TMAM9010, TMAM9020, and TMAM9040, available from Texas Instruments Inc, PO Box 202129, Dallas, TX 75220, provide a full set of hardware and software development facilities for the company's 9900 family 16-bit microprocessors and TM990 series microcomputer modules.

Each standard system provides complete concurrent multitask operation, including compile, assemble, debug, and edit and print, plus multiple processor emulation, and contains CPU; a dual hard disc drive unit; one to four 1920-character, 12" (30-cm) diagonal video display terminals (VDTs) with keyboard; and software. Users can be remote from the host computer and from each other. Added to the standard system, one to four AMPL stations accommodate simultaneous processor emulation and logic state trace analyzers. A high level debug and test procedure language, using integer and Boolean mathematics, speeds prototyping and debugging.

TMAM9010, a basic system, includes a 256k-byte CPU; 9.4M-byte dual disc drive (4.7M-byte removable); video display with keyboard; multi-AMPLUS interactive disc system software; AMPL debug high level language; interactive screen editor; 9900 family macroassembler; link editor and P/ROM programming utilities; diagnostic software; and an enclosure for CPU, disc drive, power supply chassis, and cables. It allows two users to assemble, edit, and compile optional high level languages, or run one AMPL debug without performance degradation. Since the system supports disc overlays into dynamic memory regions, more tasks can be running, with the system controlling the most favorable turnaround. Optional expansion is built into the hardware for adding another 9.4M-byte drive, AMPL station, and VDT.

A basic system enhanced with a second 9.4M-byte disc storage unit on a pedestal cabinet, TMAM9020 provides two VDTs and two keyboards, and accepts two to four users. It handles two compiler tasks or two AMPL station debug sessions in parallel with two assembly, editor, or other system utilities.

With four VDTs and four keyboards, TMAM9040 accommodates four to eight users. Its main memory contains 320k bytes; two 44.7M-byte formatted disc units meet mass storage requirements. In addition to emulation and high level language options, the system has expansion options for a variety of needs, including Pascal and FORTRAN high level language, one or two line printers, and up to four AMPL stations.

The AMPL language controls the emulation of target applications, setting breakpoints, defining data or address comparison events, data and address trace, direct target system I/O, and memory manipulation. Constructs included are capable of repetitive sequences and decision making. The AMPL emulator exercises the target application without programming the code into ROM. Emulation kits contain emulator memory that is separate from the main memory, allowing the code to execute, without target system memory, at full specified frequency.

Options for the totally interactive system include Pascal or FORTRAN, a logic analyzer kit, emulator expansion memory, a P/ROM programmer kit, line printers, and the company's component software. The systems will also handle additional options to provide speech synthesis verification and perform advanced emulation techniques.

Circle 467 on Inquiry Card

8-bit STD BUS μcomputer offered on a 4.5 x 7" card

A STD BUS compatible microcomputer, MCPU-800 combines a 4-MHz Z80A CPU, 32k bytes of ROM, 64k bytes of RAM, memory mapping, 24 parallel I/O lines, a fully programmable serial port, and I/O port expansion on a single 4.5 x 7.0" (11.4- x 17.8-cm) board. Offered by Miller Technology, 16930 Sheldon Rd, Los Gatos, CA 95030, the microcomputer is supported by a number of software packages for various applications.

Four sockets are provided for 8k to 32k bytes of EPROM or ROM. 24-pin 2k, 4k, and 8k ROMs and EPROMs are accommodated with onboard jumpers. Up to 64k bytes of dynamic RAM can be used on the board. Sockets available will accept triple-supply 4116, or single-supply 4516, 4132, and 4164 type RAMs. A memory map port allows use of both ROM and RAM in the same address space. The standard bipolar P/ROM provides 32 memory map modes. Other modes can be used by inserting alternate bipolar P/ROMs. Offboard memory can be extended to more than 2.5M bytes.

Serial interface ports provide complete software control of the serial interface characteristics. 5- to 8-bit characters; even, odd, or no parity bit generation and detection; 1, 1.5, or 2 stop bit generation; and bit rates from 30 to 56k baud are software programmable. Eight I/O bits are associated with the serial interface to fully control either terminals or modems. The serial I/O interface signals are available on a 14-pin connector compatible with ribbon cable.

An 8255A parallel interface provides 24 I/O lines. Three basic modes of operation are software selectable: the first mode allows data to be written to or read from one of the three 8-bit ports, the second allows the transfer of data through two 8-bit ports using handshaking signals, and the third supports a bidirectional 8-bit bus port with handshaking. All I/O bits are available on a 26-pin connector compatible with ribbon cable.

Boards with 4116 type RAM require 5, −5, and 12 V. When populated with 4516, 4132, or 4164 type RAMs, the board requires only 5 V. The card edge connector is the STD bus compatible 56 pins on 0.125" (0.318-cm) centers. Operating temperature range is 0 to 55 °C.

Several software packages on ROM are available for software support. A monitor allows the user to dump or enter data into memory, set breakpoints, change the contents of the CPU registers, download programs from another computer, control I/O lines, and begin execution at any address. The user can also search memory for any 1- to 3-byte occurrence, perform memory tests, and change memory map modes.

An integer-only BASIC is available for control oriented applications. In addition to standard BASIC functions, memory locations can be examined or modified, I/O ports written to or read from, and calls to machine languages are also supported. Up to 24k bytes of BASIC statements can be placed in ROM. A high level 8k-byte BASIC is also available, that adds floating point arithmetic, string manipulation, matrices, and DATA statements.

Circle 468 on Inquiry Card

Compare the ROLM® MSE/800

The First General Purpose 32-Bit Military Computer

Processors	Mil-Spec Compliance	Max. Program Size	Word Size (Bits)	Maximum Physical Memory	Package Size (1 MB Memory)	I/O Bandwidth	Performance FORTRAN Whetstone Mix	Cache Size
MSE/800	MIL-E-5400 MIL-E-16400 MIL-E-4158	4.3 Billion Bytes	32	8 MB	11.8 ft.^{3}	18.2 MB/Sec.	1200 KOPS	16 KB System 1 KB Instruction
VAX* 11/780	None	4.3 Billion Bytes	32	8 MB	50.0 ft.^{3}	13.3 MB/Sec.	1120 KOPS	8 KB System
11/70M	MIL-E-5400 MIL-E-16400 MIL-E-4158	128 KB	16	4 MB	3.5 ft.^{3}	5.8 MB/Sec.	600 KOPS	2 KB System
AN/UYK 7	MIL-E-16400	1 MB	32	1 MB	27.9 ft.^{3}	4 MB/Sec. per IOC 3 IOC's Max.	250 KOPS (Est.)	None

It's #1

#1 in Price/Performance based on advanced architectural concepts like 3 cache memories, pipelining, and instruction look ahead.

#1 in software support for real-time applications and program development. Higher order languages include FORTRAN 77, PL/1, BASIC and COBOL ... with advanced packages like X.25, Data Base Management, File Management System and Transaction Processing Monitor.

#1 in software compatibility. The MSE/800 is fully software compatible with ROLM's 16-bit Mil-Spec ECLIPSE systems and Data General's 16 and 32-bit ECLIPSE® computers.

#1 in system support with a full line of interfaces and peripherals including ROLM's new Model 4051 Subsystem—a full militarized 36 MB, 8-inch Winchester disk.

ROLM is a registered trademark of ROLM Corporation.
ECLIPSE is a registered trademark of Data General Corporation.
* VAX is a trademark of Digital Equipment Corporation.

#1 in reliability and maintainability with a built-in SNIFFER that checks and corrects random memory errors, sophisticated BITE capability, self diagnostics, and a minimum of LRU's.

The MSE/800 brings the next generation of computer technology to the military market today ... not years from now. Give us a call if you have a severe environment application, or would like to do some more comparing.

We're #1 in Mil-Spec Computer Systems

ROLM
MIL-SPEC
Computer Systems

4900 Old Ironsides Drive, Santa Clara, CA 95050.
(408) 988-2900, Ext. 2643, TWX 910-338-7350.
In Europe: Muehlheimer Str. 54, 6052 Muehlheim/Main, West Germany,
6108-60935, TWX: 4-189-063.

CIRCLE 79 ON INQUIRY CARD

I/O board provides separate serial channels and parallel ports

An I/O board for S-100 bus systems, Multi I/O features four separate serial channels and five parallel ports. The board, available from Micromation, Inc, 1620 Montgomery St, San Francisco, CA 94111, is used in the company's single- and multi-user M/NET multi-CPU system.

Each of the four serial ports contains an 8251 USART with individually selectable baud rates of 600, 1200, 2400, 4800, or 9600. Other rates can be acquired under software control. For interrupt driven I/O, each port can be jumpered to any of the eight vectored interrupt signals. The five parallel ports consist of two 8-bit, high current 67S374 output drivers and one 8255 with three 8-bit ports. The five ports attach to a 50-pin connector to accommodate a variety of peripherals.

Features include a large wire wrap area for custom applications, jumper selectable addressing to prevent address conflicts with other boards in the system, and an 8253 programmable timer with two unallocated outputs for special functions. Complete documentation includes installation guide, theory of operation, and programming examples.

Circle 469 on Inquiry Card

Video display controller card offered for LSI-11/Q-bus systems

VDC11 video display controller from Andromeda Systems, Inc, 9000 Eton Ave, Canoga Park, CA 91304, for use with LSI-11/Q-Bus systems, provides the functions of a 2-channel interface card, a standard video display terminal, and a graphics display controller. When plugged into a standard Q-bus backplane, the card appears as two serial ports: one port drives the video controller logic; the other is an independent interface that can be used with any RS-232 serial device.

Standard features include 80H x 24V character display, full upper- and lowercase 96-character ASCII set with descenders, three scrolling speeds, hardware scrolling of the graphics set, and serial or parallel keyboard input. The microprocessor based card can be programmed by the company to emulate a variety of video display terminals.

The card is compatible with existing serial channel software, including the DEC console terminal handlers, and will run standard terminal control software. It connects to a direct drive video monitor and a parallel keyboard; with minimal external logic, it will drive an RS170 composite video monitor and listen to a serial keyboard.

A graphics display feature allows the card to function like the Tektronix 4010 vector display terminal. Functions provided include vector generation on an apparent 1024H x 780V grid and generation of alphanumeric characters anywhere on the screen. The card extends the functionality of the 4010 by allowing single point plotting; selective erasure of points, vectors, and characters; and readback of the graphics screen for output to a hardcopy device. Single-line scrolling and screen synchronization commands are also included to allow the generation of strip chart recorder type displays.

The card's second channel is a standard RS-232-C serial interface. Transmit and receive baud rates are selectable from 50 to 19,200 baud. Logic to interface an external "busy" line is included to allow the serial output port to drive a line printer.

VDC11-A is configured to emulate the Lear Siegler ADM-3A video terminal; VDC11-B emulates the DEC VT-52. All versions include the smooth scrolling and graphics features. The card can also be used as a controller in a standalone video terminal. The second serial channel is then used as the interface to other systems, and the Q-Bus interface is deleted.

Circle 470 on Inquiry Card

Timing and counting controller offered for STD BUS systems

System timing and counting controller, model SB8355 from Micro/sys, Inc, 1353 Foothill Blvd, La Canada, CA 91011, solves timing and counting problems with extensive programmability. The controller can be configured for uses with most STD BUS based timing of counting systems, including event counters, high resolution programmable duty cycle waveform generators, waveform analyzers, FSK modulators, and time of day clocks with alarm.

Five independent 16-bit counter groups, each with four to six registers, are included in the controller. The main register of each group can be configured to count up or down, in binary or BCD, once or repeatedly. Inputs can be external signals, internal timebases based upon CPU clock or optional crystal, or adjacent counter group outputs. Each group allows programmable input selection, gating selection, register usage, output configuration, and mode selection. A flexible interrupt structure includes mask and status registers, and a priority interrupt controller interface connector.

Two of the counter groups can be configured to operate in a time of day mode, providing hours, minutes, seconds, and tenths of seconds. These groups have 16-bit alarm and comparator registers, allowing interrupts on absolute count or absolute time of day. A zero crossing detector allows connection of an external line frequency ac signal for timekeeping.

Circle 471 on Inquiry Card

Products offered for STD and S-100 buses

Two motherboards, a processor board, and two static RAM boards are offered by CompuPro Div of Godbout Electronics, PO Box 2355, Oakland Airport, CA 94614. STD MBD-8 and -16 are motherboards for the STD bus, STD CPU-Z is a Z80 based processor, STD RAM-16 is a 16k x 8-byte static RAM board for the STD bus, and RAM-17 is a 64k-byte static RAM board for S-100/IEEE 696 computers.

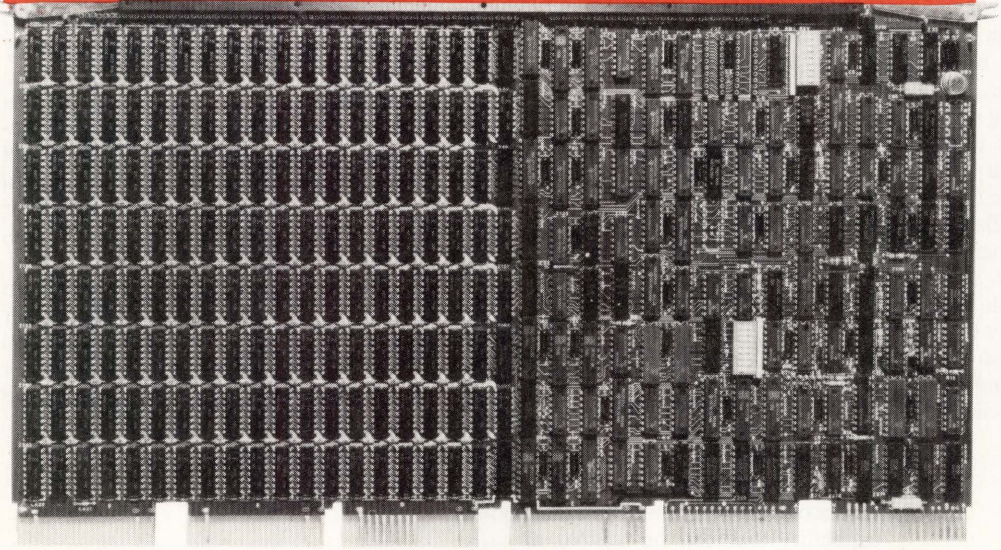
STD MBD-8 and -16 motherboards have 8 and 16 slots, respectively, allowing system designers to choose the exact size desired for their system. Faraday ground shielding around signal lines ensures noise free signals and minimizes crosstalk; heavy power buses have thorough capacitor bypassing to suppress noise. A power connector applies all power to the bus, and a reset connector allows connection for a pushbutton reset. Edge connectors are spaced on 0.75" (1.91-cm) centers to facilitate cooling and allow the accommodation of nonstandard component heights. Both motherboards mount in a Vector Electronics card cage or operate in a standalone configuration.

The STD CPU-Z processor card has provisions for up to 8k bytes of P/ROM or RAM, and features an RS-232 serial channel, a power-on-jump circuit to any 256-byte boundary, wait states for all machine states, and a 4-MHz processor. ICs are socketed for ease of maintenance, and the board has a complete solder mask and component legend along with a comprehensive user's manual. A 6-MHz processor and an EPROM assembler/editor/monitor are optional.

(continued on page 170)

ADD-ON ADD-IN

MEMORY... FROM THE LEADER



PDP®-11/44-compatible
1.0 MB ADD-IN

There's lots of good reasons to buy your ADD-ON/ADD-IN memory from the leader.

For starters, there's the wide range of core and semi mini-memories we offer. The industry's widest. In fact, Dataram is the only company in the world supplying minicomputer-compatible core and semiconductor main memory and disk emulation systems. The *only* company.

And Dataram ADD-ON/ADD-IN products do more. Like save money...as well as valuable space in your minicomputer. And they increase throughput and improve overall performance.

Just some of the reasons why Dataram is the leading supplier of ADD-ON/ADD-IN memory for the minicomputer industry...and shipping at an annual rate of $25 million.

Want more reasons? If you're using a minicomputer, and want to get more for your memory dollar, talk to us. We're very reason-able. Dataram.

DEC, PDP and VAX are registered trademarks of Digital Equipment Corporation.

DATARAM CORPORATION

Princeton Road
Cranbury, New Jersey 08512
Tel: 609-799-0071 TWX: 510-685-2542

	CORE	SEMI
DEC®	✓	✓
DATA GENERAL	✓	✓
PERKIN-ELMER	✓	✓
VARIAN	✓	✓
INTEL	✓	✓

I'd like more answers about mini-memories for my

____________________ minicomputer.

☐ Please send information.

☐ Please have a salesman contact me.

Name ____________________

Title ____________ Phone ____________

Company ____________________

Address ____________________

City ____________ State ______ Zip ______

Canada: Ahearn & Soper Ltd., 416-245-4848 • **Finland:** Systek OY, (80) 73 72 33 • **France:** YREL, (01) 956 81 42 •
Hungary/Poland/Rumania: Unitronex Corporation, WARSAW 39 6218 • **Italy:** ESE s.r.l., 02/607 3626 • **Netherlands:** Technitron b.v., (020) 45 87 55 •
Sweden: M. Stenhardt AB, (08) 739 00 50 • **Switzerland:** ADCOMP AG, 01/730 48 48 • **United Kingdom:** Sintrom Ellinor Ltd., (0734) 85464 •
West Germany: O.E.M.-Elektronik GmbH, 07 11-79 80 47 • **Yugoslavia:** Institut "Jozef Stefan", 263-261 • **Australia/New Zealand:** Anderson Digital Equipment, (03) 543-2077 •
India: Infosystems Private Limited, 79281 • **Israel:** Minix Computers & Systems Ltd., 03-298783 • **Japan:** Matsushita Electric Trading Co., Ltd., 06 (282) 5111

CIRCLE 80 ON INQUIRY CARD

Configured as two 8k x 8-byte blocks that are addressable on any 8k-byte boundary, STD RAM-16 uses 2114 static RAM chips and runs with 4-MHz processors. It can also be populated with Xicor 2214 shadow RAM/ROM memory chips, allowing the system to have 1k to 16k bytes of nonvolatile memory. The board responds to the memory expansion signal if more than 64k bytes of system memory are desired.

Offered on a 5" (13-cm) high board, RAM 17 runs with 6-MHz Z80 and 10-MHz 8086/88 processors. The board meets all IEEE 696 specifications, including 24-bit addressing, allowing up to 16M-bytes of system memory. It is addressable on any 64k page boundary and can be disabled in 16k-byte blocks. The upper 8k-byte blocks can have 2k-byte windows disabled to allow for memory mapped peripherals; 2k x 8-bit static RAM chips that are pin compatible with 2716 EPROMs allow up to 32k bytes of EPROM to intermix with the RAM. The board features DMA operation and low power dissipation, and is also available in a 48k-byte configuration.

Circle 472 on Inquiry Card

Personality module supports emulation of 8048 μprocessor

Support for Intel 8048 based microprocessor development is offered by a personality module for the MicroSystem Designer. The basic system, available from Millennium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014 (see *Computer Design,* Nov 1979, p 164), serves simultaneously as a universal prototyping instrument and a training aid for 8- and 16-bit microprocessor based systems.

The personality module offers users all the emulation capability of the MicroSystem Designer; 8048 software can be downloaded over the integral RS-232-C port, executed, and debugged without the construction of prototype circuits.

When necessary, the MicroCable allows integration to prototype hardware. A solderless prototype area built into the development system eases circuit testing.

Standard operations include ability to examine and modify register, memory, and I/O port contents. Program and circuit debug are facilitated by operation at full speed with a hardware breakpoint or single- or auto-step operation with data monitoring.

Processor-specific capabilities include the ability to manually control the T_O and T_I inputs to the microprocessor via a special keyboard. The module also allows the user to exercise the interrupt capabilities of the microprocessor asynchronously, permitting the program logic of interrupt handling routines to be debugged prior to full hardware availability.

Circle 473 on Inquiry Card

In-circuit emulator provides development and debugging tools

ICE-51, an in-circuit emulator for the 8051 8-bit, single-chip microprocessor, combines with the Intellec microcomputer development system and 8051 software development package to provide full capability for developing and debugging application hardware and software. Developed by Intel Corp, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123, the emulator provides testing and debugging capability that can be utilized at each stage of system development, from initial software development to realtime testing of the final package.

Included in the module are 8k bytes of emulator resident RAM that can be mapped into either onchip or offchip program memory for realtime emulation of the user's program. The module can conditionally halt emulation and record execution history, while emulating the microprocessor at its full 12-MHz clock rate, without distorting offchip timing. Advanced emulation software such as symbolic debugging, HELP files, and conditional command constructs are included to speed learning and automate debugging. Assembly and disassembly commands that change individual program lines in assembly language mnemonics ease program alteration.

Emulator hardware links the microcomputer development system with the user's system through a buffer box and a cable that replaces the CPU during debugging and testing. The interface between the emulator module and the application system is a 64-pin configuration, or bond-out, of the 8051 microcomputer, located directly on the system's 8051 socket. The bondout chip provides "back door" access to the 8051's onchip features while it emulates the microcomputer.

Circle 474 on Inquiry Card

Hard disc system offered for S-100 bus μcomputers

Discus M20, a fixed disc system for S-100 bus microcomputers, features a Fujitsu 2302 8" (20-cm) Winchester disc drive with a data transfer rate of up to 600k bytes/s. The system, offered by Morrow Designs, 5221 Central Ave, Richmond, CA 94804, delivers 20M bytes of formatted storage (23.4M bytes unformatted) and is expandable to 80M bytes by daisy chaining up to four drives.

A single-board S-100 intelligent controller supervises all data transfers between the host and the disc system via four I/O ports. For database security, a 512-byte sector buffer, with each sector individually write protectable, is provided onboard.

The complete system consists of hard disc drive, metal cabinet with fan, power supply, cables, S-100 controller, and CP/M 2.2 operating system. A dc motor is provided for ease of conversion from 110 to 220 Vac.

Circle 475 on Inquiry Card

System acts as personal data management tool

A Series 80 personal computer, a mass memory ROM, an HP 82901M dual-drive flexible disc, and Information Management Pac software make up the Personal Information Management System from Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304. The system acts as a data management tool, creating, accessing, modifying, searching, and sorting data; it handles up to 1000 records of information, and performs numerous complex analyses.

For the non-computer user, Information Management Pac (IMPac) software features a querying system with easily followed prompts. It also provides a report writer for organizing and formatting products; a sorting and statistics capability for comparison analyses, and a graphics capability to create line, curve, bar, and pie charts for reports or presentations.

The system's 5.25" (13.34-cm) dual-drive flexible disc provides 270k bytes of random access storage per drive, for a total of 540k bytes of memory. Programs can be stored on one disc and data on the other, allowing different programs and data to be used interchangeably.

Circle 476 on Inquiry Card

Cortron announces a solid state keyboard at "bare bones" prices.

Solid state intelligent keyboard for only $45

If you are considering a low cost type keyboard, have we got an offer for you. The Cortron® CP-4550 Keyboard is a high quality, solid state, intelligent keyboard with full microprocessor capabilities.

Compare all the features of the Cortron Capacitance Keyboard—serial output, N-Key rollover, automatic repeat, custom codes—with "bare bones" type offerings. You be the judge of just how much more the $45 starting price can buy volume keyboard users at Cortron.

Long-life, highly reliable keyswitch

We've designed a keyswitch with an exceptional, true linear feel. It's also environmentally superior to foam pad design approaches. The keyswitch uses the full line of impressive Cortron keytops. All of this with a life test rating in excess of 100 million cycles.

Ferrite Core and Capacitance . . . the best of both worlds

Cortron pioneered and built a reputation on the advanced ferrite core switching technology. Today, there are millions of ferrite core keyswitches in Cortron Keyboards around the world. We've applied this known expertise to further reduce keyboard costs. Cortron broadens the line with the introduction of the new capacitance keyboard. Now, you can choose the technology to fit your application needs from the best of both worlds. At Cortron, our people work hard at being responsive to your needs for advanced technology, cost efficiency, broad line and lower prices.

For full details and *free literature* on the Cortron CP-4550—$45 Solid State Keyboard, call or write Cortron, A Division of Illinois Tool Works Inc., 400 West Grand Avenue, Elmhurst, IL 60126. Phone: (312) 279-9110. TWX: 910-254-0154.

CORTRON
A DIVISION OF ILLINOIS TOOL WORKS INC
THE KEYBOARD PROFESSIONALS AROUND THE WORLD

CIRCLE 81 ON INQUIRY CARD

Single-board memory provides 256k-byte RAM storage

From 64k to 250k bytes of dynamic RAM on a single 9.75 x 6.0″ (24.76 x 15.2-cm) card are offered by the Pachyderm memory board from Novex, Inc, 19717 Meredith Dr, Derwood, Md 20855. The board is compatible with Motorola's EXORciser bus and Micromodule series, and offers 5- or 12-V battery backup capability.

High memory density is achieved by "piggybacking" 16k-byte dynamic RAM chips; stacks of four chips each will provide 256k x 9 bits of memory. Power consumption of a 4-chip stack is approximately that of a single 64k-byte dynamic RAM chip. A switch-selectable interleaved mode exchanges high and low address bits to uniformly distribute power dissipation. Fixed memory mapping in 2k-byte increments is provided by a P/ROM for the lower 64k bytes of memory. Write protection is strappable in 2k-byte increments on a greater than/less than basis, and uses an external protect-enable signal.

A proprietary Cycle Salvaging^{TM} circuit is employed by the transparent refresh system; the circuit takes advantage of unused memory cycles, including non-RAM memory references and non-VMA cycles, to implement its refresh operations. As a result, time critical I/O operations will not be interrupted by refresh requests. A refresh request is transmitted when necessary, and the resulting 3-cycle process permits three refresh cycles to be performed. This procedure reduces by two-thirds the time required by refresh in a conventional cycle stealing memory.

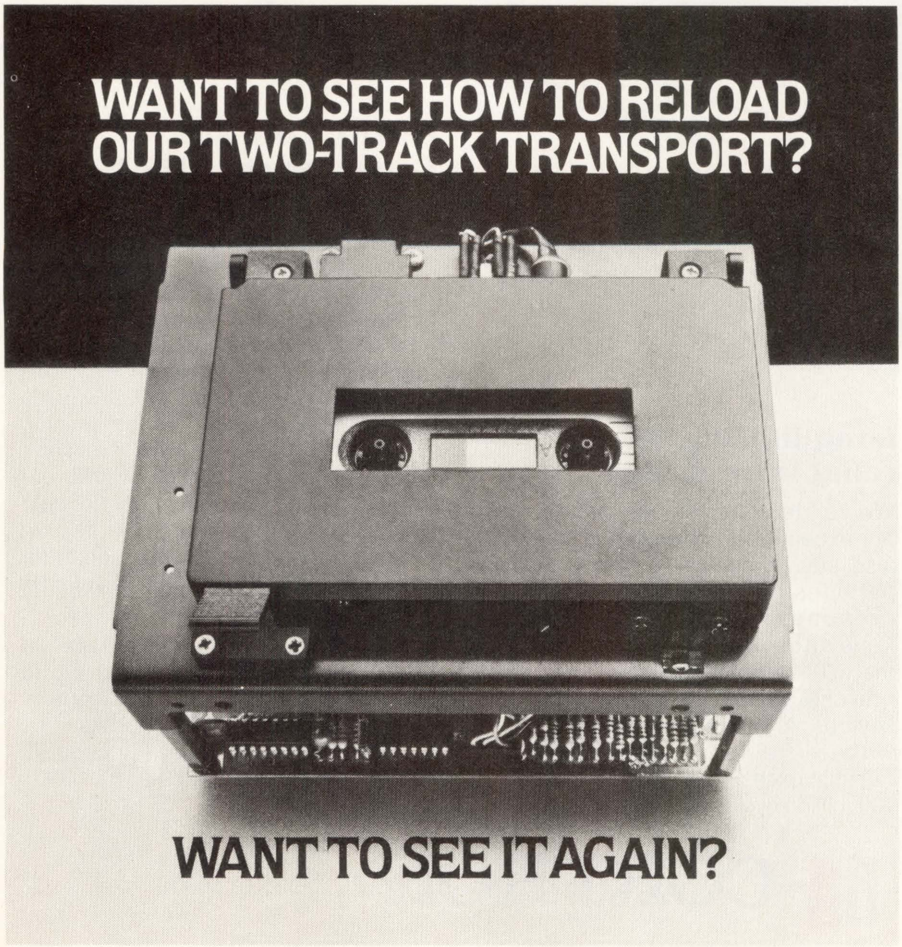
A switching regulator provides the necessary voltage to operate the memory from a 5- or 12-V backup battery. In this case, internal refresh controls take over memory cycling. In the standby mode, the fully populated 256k-byte system draws only 8 W.

Circle 477 on Inquiry Card

Rackmounted μcomputer system offered for OEMs and industry

MSC-6600, a general purpose, rackmounted microcomputer system for OEM and industrial applications, allows users to implement their microprocessor based systems without designing computer hardware. The Multibus compatible system is a product of National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Available in 4- or 8-slot card packages, the system provides software and hardware support for a standard RS-232 CRT keyboard and a parallel printer interface. Built with existing boards available from the company, it features an 8080A microprocessor, 64k bytes of RAM, and dual 8″ (20-cm) double-density single-sided floppy diskette drives. CP/M version 2.2 operating system software, included in the basic system configuration, provides users with a variety of languages and utilities for software development.



ONTEL

A CWI SUBSIDIARY

Ontel Display Computers—designed for the 80's

Thoughtfully designed to be operator friendly, the OP-1/15's advanced ergonomic styling includes a modern low-profile keyboard, tiltable CRT display, and many sophisticated video enhancements. Handling a multitude of applications, this unique low-cost Display Computer is truly designed for the 80's.

A comprehensive selection of software packages. Superior customer support. Very attractive pricing.

Those are just a few of the reasons why we've installed 20,000 systems worldwide.

We can assemble and deliver complete OEM systems in less than 90 days. Be informed. Contact us today.

Ontel Corporation
250 Crossways Park Drive
Woodbury, NY 11797 (516) 364-2121

CIRCLE 83 ON INQUIRY CARD

Interrupt Priority Controller Increases Microprocessor Efficiency and Versatility

Alex R. Shevekov

Advanced Micro Devices
901 Thompson Pl, Sunnyvale, CA 94086

Microprocessor based systems include a powerful state machine as the central unit for decision making and transfer of information. The microprocessor's intelligence is derived through a logical sequence of instructions while information is being gathered by a variety of specialized peripheral devices. Although data processing activity almost always occurs at a predictable rate, peripheral activity occurs at random periods and dwell time varies according to each type of peripheral. For example, a disc drive has significantly different service requirements than does a parallel port monitoring a valve or keyboard activity. The basic parameters that influence the design of peripheral servicing algorithms are the frequency of service required, the allowed service latency, and the service duty cycle of the devices.

Two general methods are utilized to initiate and coordinate peripherals: program controlled service and interrupt driven service. When varied and multiple peripherals are mixed, it is less likely that program controlled peripheral service will be successful. In a program controlled system, a peripheral service request controller can unburden the overhead required for polling and soften the impact of software service routine complexity.

Universal Interrupt Controller

A universal interrupt controller is a peripheral device to the central processor that is used to improve system throughput and response time by allowing external devices to asynchronously modify the instruction sequence of a program being executed. The controller monitors simultaneous service requests from various peripherals, prioritizes them according to a predetermined sequence, and informs the central processor with a hardware interrupt request. Upon acknowledgment of the interrupt by the central processor, the universal interrupt controller places an instruction on the data bus, generally a call subroutine instruction, with the vector routine's address. Because a direct identification of the highest priority peripheral and its service routine has been provided, the pertinent service subroutine for the peripheral is then immediately executed by the central processor.

The Am9519A universal interrupt controller (Fig 1) manages the masking, priority resolution, and vectoring of up to eight interrupts. Several Am9519As can be cascaded to expand the number of serviceable interrupts. A mix of 1-, 2-, 3-, or 4-byte responses to an interrupt acknowledge from the microprocessor can be programmed for any of the eight levels of priority. Contention among multiple interrupts is managed by a fixed or rotating priority resolution. Fixed priority is hardware dependent and is fixed by the interrupt level input pin (IREQ 0 to 7) to which the interrupting device is connected. IREQ 0 is the highest priority and IREQ 7 is the lowest. Normally, high speed peripherals with more demanding service requirements are designated as having the higher priority. Rotating priority, on the other hand, treats the eight interrupts with the same priority. This technique is useful for devices with similar duty cycle and service latency requirements. The rotating priority mode can be visualized as a circular chain with the lowest priority assigned to the most recently

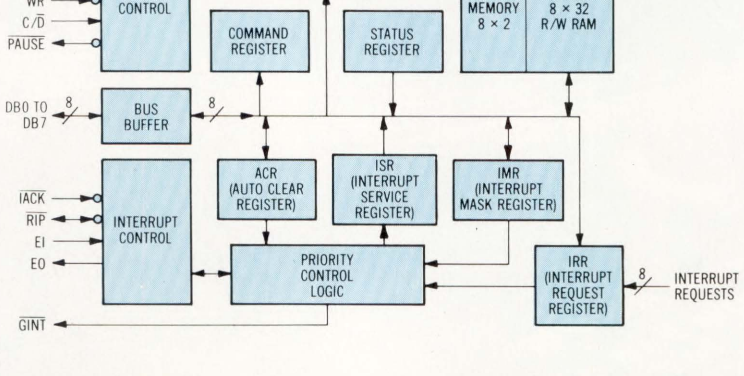


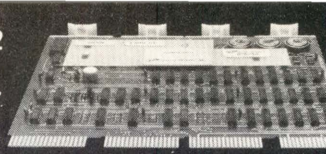
Fig 1 Block diagram of Am9519A universal interrupt controller. Eight interrupt requests are accommodated

OUR TIMING CONTROL UNIT HELPS YOUR COMPUTER KEEP SCORE OF TIME AND DATE.

Power-up or power-down, your computer always knows the time, *exactly*, with Digital Pathway's Timing Control Unit (TCU). Even during extended power interruptions. Rechargeable battery support makes our TCU immune from power failure of any kind. For as long as three months. And an on-board crystal-controlled oscillator ensures supreme accuracy.

No matter what model computer you have, you'll find our TCUs offer many features that make living with computer timeouts less complicated. And some models can even be set to initiate an interrupt at a chosen date and time. Or at specified intervals.

Find out how we can help make your time more productive. Call or write Digital Pathways today for more information at 1260 L'Avenida, Mountain View, CA 94043. Telephone (415) 969-7600.
TWX: 910-379-5034.



*PDP-11 and LSI-11/2 are registered trademarks of Digital Equipment Corp. Others listed are trademarks, respectively, of Intel Corp., Motorola Inc., Hewlett-Packard, Lockheed Corp. and Computer Automation Inc.

*PDP-11	TCU-100	$495
	TCU-150	$460
*LSI-11/2	TCU-50D	$325
*Multi-Bus	TCU-410	$325
*EXORcisor	TCU-68	$325
*HP 2100	TCU-2100	$395
*Lockheed SUE	TCU-200	$550
*Naked Mini	TCU-310	$385
Any Model Computer (RS-232/20mA)	SLC-1	$640

DIGITAL PATHWAYS

NOW YOU'RE SAFE FROM COMPUTER TIMEOUTS EVEN AFTER THE POWER GOES.

Circle **84** on inquiry card.

Canada: (403) 286-2744 • England: 403 813 813
Germany: (089) 60 60 71-72 Telex: 5216290 isic d • Switzerland: 022/310587 Telex: 289191

serviced device. A polled mode of priority resolution can also be utilized. This mode is useful where processor interrupts are undesirable; however, hardware prioritization of devices enhances the software.

For hardware and software checkout, the Am9519A also permits software generated interrupts. A mask register allows selective masking of undesired interrupting devices on a bit by bit basis. In addition, an auto clear feature can be programmed to allow or disallow further interrupts from a peripheral device. This feature is useful in preventing interrupts from the device until the end of the service routine.

Interrupt inputs use "pulse-catching" circuitry so that an external interrupting level need not be maintained until peripheral service is begun. The interrupt polarity may be selected as either active high or active low. Interrupt pulses of less than 40 ns are ignored by the pulse-catching feature of the Am9519A.

Interrupt Expansion

Several universal interrupt controller chips may be cascaded to increase the number of interrupts that can be handled by the system. In general, expansion will require an added chip select signal for each additional chip. The $\overline{\text{GINT}}$ (gate interrupt), $\overline{\text{PAUSE}}$, and $\overline{\text{RIP}}$ (response in process) signals are all designed to be wire-ORed in expanded systems.

The 5-chip expanded system in Fig 2 illustrates the expansion of the number of interrupts to forty. Any one of the interrupt controllers may initiate a $\overline{\text{GINT}}$ to the processor. Interrupt prioritization will not begin until an active interrupt acknowledge ($\overline{\text{IACK}}$) is output by the processor. Upon $\overline{\text{IACK}}$ active, all chips will activate their $\overline{\text{PAUSE}}$ and $\overline{\text{EO}}$ (enable out) outputs and begin prioritizing any pending interrupt requests (as latched in their interrupt request registers). If the highest priority controller does not have any pending interrupt, then it will raise its EO output allowing the next device in the daisy chain to respond to the $\overline{\text{IACK}}$ signal. In other words, the EI (enable in) level (high) ripples through the daisy chain until the device holding the highest priority interrupt request is discovered.

A second interrupt occurrence must have a setup time of at least 200 ns before $\overline{\text{IACK}}$ goes active in order to be serviced in this sequence. The higher priority Am9519A in the daisy chain link will then force its EO output to stay low through the length of the interrupt acknowledge sequence in order to disable lower priority devices; if the RIP signal is high, the higher priority device will force RIP active low. This action has a dual purpose: it prevents the other connected chips from responding to the IACK signals, and causes the $\overline{\text{PAUSE}}$ signal in all the Am9519As in the daisy chain link to go inactive. $\overline{\text{RIP}}$ will stay low until all response bytes have been transferred.

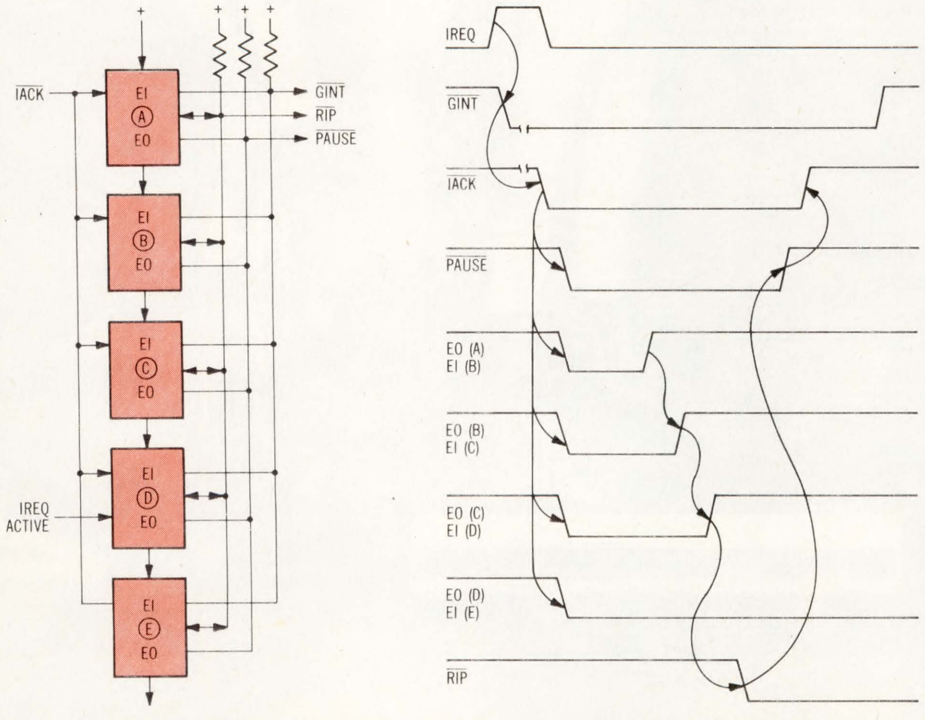
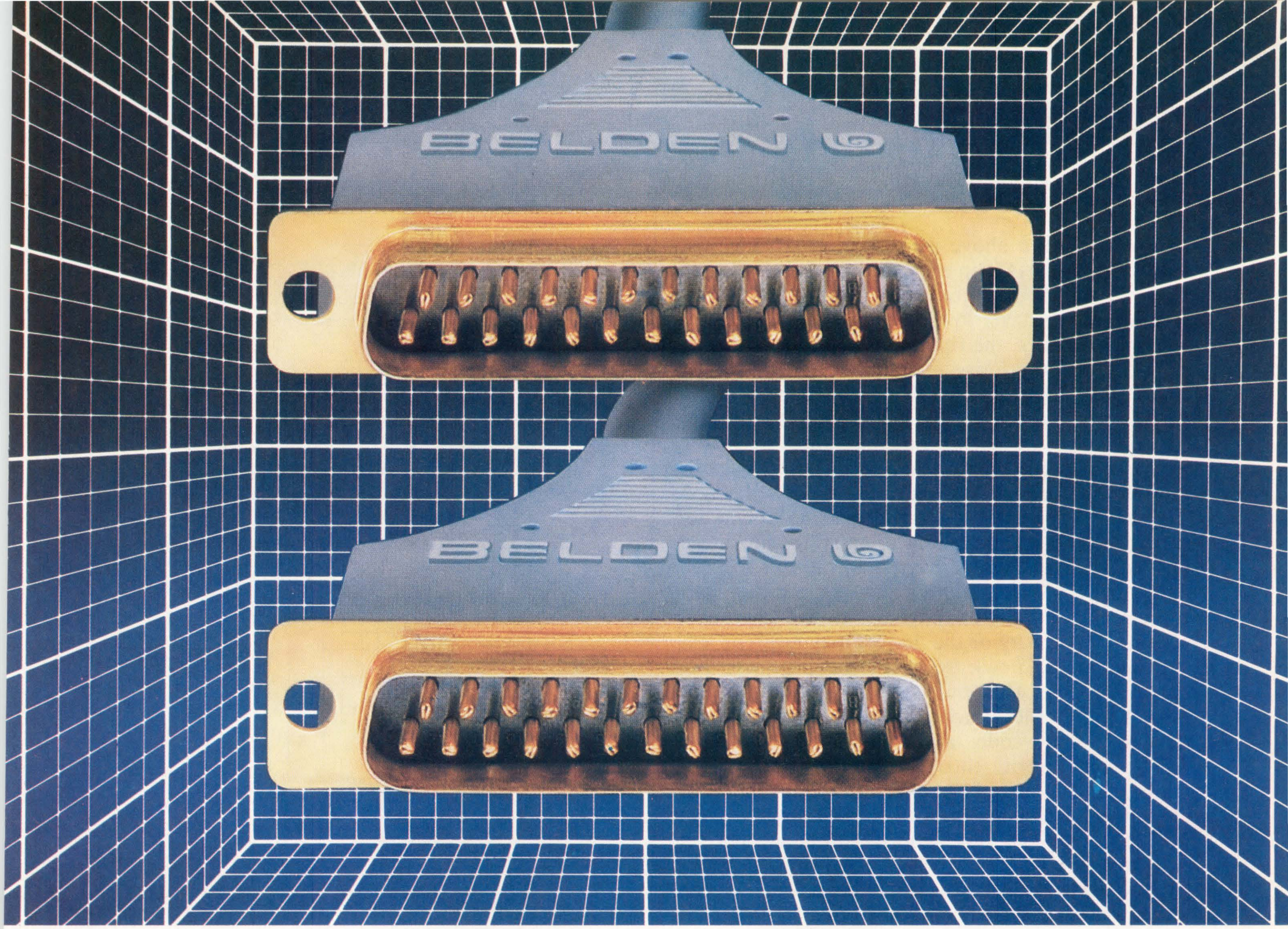


Fig 2 Am9519A universal interrupt controllers are cascadable without additional logic and allow any number of interrupts. Interrupt request to device D prevents other devices from responding to interrupt acknowledges



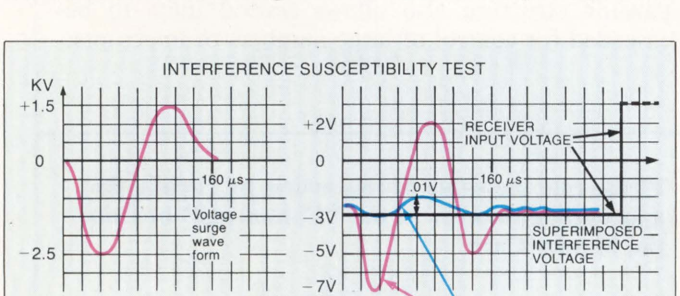
One of these cable assemblies can cut your interference levels 59db.

Both meet RS-232-C specifications. Both are made by Belden using rugged materials and proven designs.

But one is shielded. One is not. And that can make a big difference in critical data communications applications.

Although RS-232-C standards do not specifically call for shielded interconnect devices, our research indicates that cable *and* connector shielding is required to insure the signal integrity of the assembly. In fact, transfer impedance, leakage current power spectrum, electrostatic discharge and interference susceptibility tests at Belden all demonstrate the value of Belden totally shielded connector-cable assemblies over nonshielded assemblies.

With a complete line of rugged and highly reliable standard molded connector designs including GPIB, and complete custom design capabilities, we can make exactly what you need, when you need it. And show you ways to increase performance without increasing costs. Whenever you have a shielding need or a question involving interconnect devices, contact Belden. We'll share our experience. For a free catalog, write Belden Corporation, Interconnect Systems Operation, 105 Wolfpack Rd., Gastonia, NC 28052. Phone: (704) 865-4513.



BELDEN

Coming through...

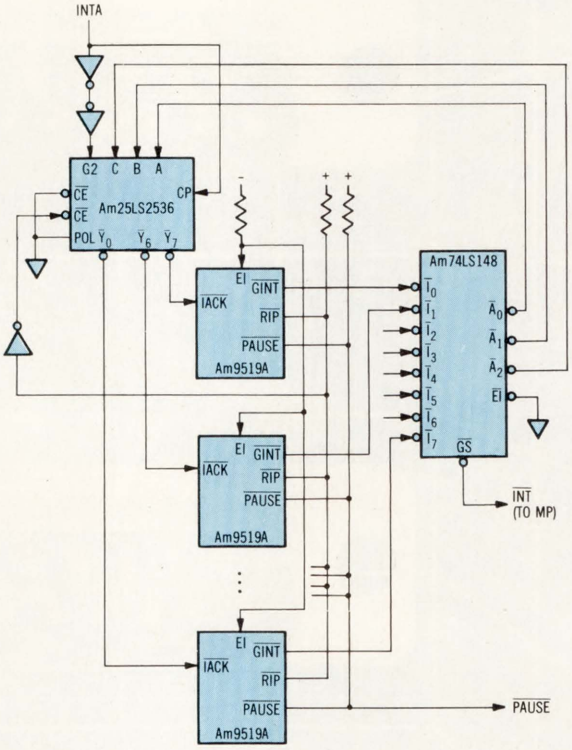
with new ideas for moving electrical energy

CIRCLE 85 ON INQUIRY CARD

As seen in the above prioritization scheme, the number of Am9519As in a system can be very large. However, the ripple through time from EI to EO will accumulate whenever lower priority devices request service. Normally, the ripple through time is 300 ns for the highest priority interrupt controller in the chain and 150 ns for a subsequent chip. The accumulated ripple time may have significant impact on the total system throughput rate since the microprocessor must remain in a WAIT state condition until all the priorities have been resolved. Fig 3 shows a daisy chainless priority expansion scheme accomplished by adding two medium scale integration (MSI) devices and three inverters to the system. The LS148 priority encoder prioritizes the various controllers and outputs an interrupt to the microprocessor. The priority of the devices may move up until interrupt acknowledge from the processor becomes active. The processor's INTA (interrupt acknowledge) then latches in the highest priority device's 3-bit code and ripples through the Am74 LS148 priority encoder prioritizes the various controllers and outputs an interrupt to the microprocase in which a higher priority Am9519A generates an interrupt while the lower priority device has not yet activated its RIP output, the RIP signal from the interrupt controller under service will be active low until all response bytes have been transferred. The signal is used to lock out further INTA signals from changing the destination of the $\overline{\text{IACK}}$ signal by disabling further storage updates by the Am25LS2536.

As an example of an interrupt controller to microprocessor interface, consider a 1-MHz 6800 microprocessor implemented with two sets of address decoders and the insertion of WAIT states during both phase 1 and phase 0 of the clock. Two 25LS2521 8-bit comparators provide the means of memory mapping the controller in order to access its internal registers. Since only two addresses are required for access, the least significant bit of the address bus (A_0) drives the command data input directly. In such a configuration, the Am9519A decodes its interrupt acknowledge from the vector interrupt memory addresses FFF8(H) and stretches the phase 1 and phase 2 clock to the 6800 microprocessor.

The interrupt controller begins resolving its highest priority interrupt following the active edge of the $\overline{\text{IACK}}$, which is the address FFF8(H) in a 6800 system, and requires a 500 to 1000 ns delay before the first vector address appears on the data bus. The delay is accomplished by stretching the phase 2 clock high via the $\overline{\text{PAUSE}}$ active signal to the $\overline{\text{MEM READY}}$ input of the clock device. The only constraint is for the PAUSE signal to be active before the rising edge of the phase 2 clock.



CP — CLOCK INPUT
INTA — INTERRUPT ACKNOWLEDGE
POL — POLARITY
Y_0 TO Y_7 — OUTPUT 0 TO 7

Fig 3 Eight-chip daisy chainless priority expansion scheme eliminates device priority ripple through time. System includes two MSI devices and three inverters

Summary

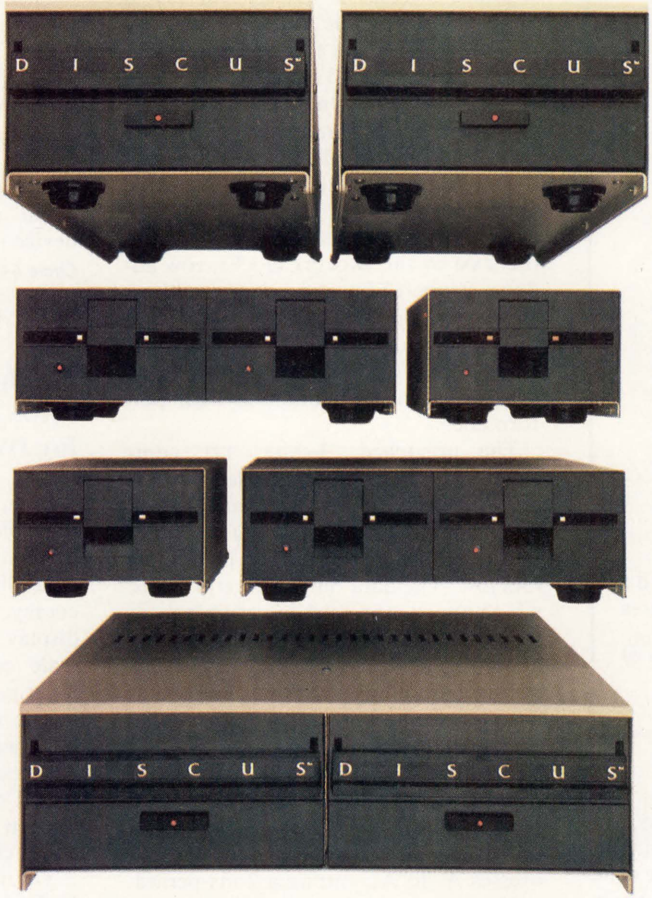
Interrupt controllers provide an interrupt structure to increase the efficiency and versatility of microcomputer based systems. The analogous interrupt request and acknowledge request mechanism of the variety of general microprocessors, and the ability of one device, the Am9519A, to output up to four bytes of user selected information, facilitates interface to a variety of 8- and 16-bit microprocessors. A simple expansion structure also allows several units to be cascaded for control of large numbers of interrupts.

Please rate the value of this article by circling the appropriate number in the "Comments" box on the Inquiry Card.

High 725 **Average 726** **Low 727**

MORROW DESIGNS

Cost effective answers to floppy disk problems.



DMA answers. Standard, accumulator transfer floppy disk controllers can stall your microcomputer system's CPU for as long as 160 milliseconds. Just to access and transfer a sector of data to main memory. If CPU processing speed and system performance are critical, you need something better. That's where Morrow Designs' new intelligent Disk Jockey DMA™ controller comes in. This new breed of perpherial handles both 5¼" and 8" drives and can read almost any format in existence. Speed? Your CPU runs at full tilt while the DMA controller seeks and gathers a sector of data. How? Information transfers to and from main memory occur as "cycle steals" from the system bus. And the missing memory cycles are transparent to the CPU totalling only two milliseconds instead of the usual 80.

Build a buffer. Give the Disk Jockey DMA a little extra memory and your system's performance gets even better. The extra storage is used as a track buffer. So, whenever a sector on a new track is read, the track buffer is automatically filled with the other sectors on the track. The result? Additional data on the track is immediately available. Without the 80 millisecond rotational latency normally encountered. And similar efficiencies occur with disk writes. Sectors in the track buffer are conditionally written on the disk only if a new track is accessed. And only one revolution of the disk is required.

Now, prices:* All systems listed are supplied with a floppy disk drive, Disk Jockey Direct Memory Access Controller, CP/M** 2.2 operating system, power supply, fan, cables, cabinet and Microsoft 5.2 BASIC.

Even lower prices. Morrow Designs' floppy disk systems with Disk Jockey™ 2D controllers offer the same high quality at even lower prices. Now without memory mapping!

Fast answers. See Morrow Designs' family of cost effective floppy disk systems at your computer dealer. For a somewhat more leisurely answer, circle the reader service number below. For immediate answers, phone us at (415) 524-2101.

LOOK TO MORROW FOR ANSWERS.

5¼ Inch Systems (formatted data)	
400,000 Bytes (1) Dual Sided 48 TPI Drive	$1110
800,000 Bytes (2) Dual Sided 48 TPI Drive	$1899
800,000 Bytes (1) Dual Sided 96 TPI Drive	$1499
1,600,000 Bytes (2) Dual Sided 96 TPI Drive	$2599

OEM pricing available

8 Inch Systems (formatted data)	
500,000 Bytes (2) Single Sided Drive	$1199
1,000,000 Bytes (2) Single Sided Drive	$1975
1,000,000 Bytes (2) Dual Sided Drive	$1595
2,200,000 Bytes (2) Dual Sided Drive	$2675

OEM pricing available

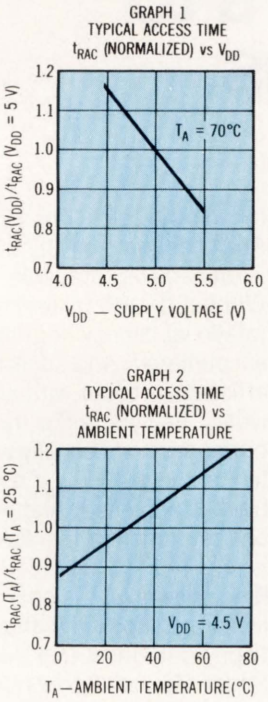
MORROW DESIGNS

5221 Central Avenue, Richmond, CA 94804
(415) 524-2101

*Prices subject to change without notice.
Disk Jockey DMA and Disk Jockey 2D are trademarks of Morrow Designs
**CP/M is a trademark of Digital Research.

CIRCLE 86 ON INQUIRY CARD

64k N-channel MOS dynamic RAM includes redundant circuitry



Typical access time of Intel's 2164 dynamic RAM. Graph 1 compares t_{RAC} (access time from $\overline{RAS}$) to V_{DD}. Graph 2 shows t_{RAC} as function of ambient temperature

Recently announced by Intel Corp, 3585 SW 198th Ave, Aloha, OR 97005, the 2164 is a 65,536 word by 1-bit N-channel MOS dynamic RAM fabricated in the company's HMOS process. The 2164 is packaged in the industry standard 16-pin DIP and is designed to operate with a single 5-V supply. A single transistor cell and advanced dynamic circuitry enable the 2164 to achieve high speed at low power dissipation.

Three 64k devices are available in the 2164 series. The -15 is accessible in 150 ns (maximum) with a 60-mA (maximum) active power dissipation. Maximum specifications for the -20 are 200-ns access time and 55-mA active power dissipation. A 250-ns maximum access time and 50-mA active power device is designated -25.

The 2164 chip contains four extra memory rows and four extra memory columns not needed for basic functions. If a defect is discovered when a chip is tested, a faulty column or row is replaced with a redundant one. The result should be increased yield of error free devices.

The 2164 dynamic RAM and the 2167 16k x 1 static RAM are the first of the company's products to be manufactured using redundant designs. Because of its fourfold increase in density, the 2164 is an available upgrade device for markets presently served by the company's 2118 16k dynamic RAM. To ensure upgrading with future 256k dynamic RAM designs, pin 1 of the RAM is not connected.

Multiplexing the 16 address bits into the 8 address input pins allows high packaging density. The two 8-bit TTL level address segments are latched into the RAM by the two TTL clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$). Non-critical timing requirements for the $\overline{RAS}$ and $\overline{CAS}$ clocks allow the use of the address multiplexing technique while maintaining high performance.

The unlatched, 3-state, TTL compatible data output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read/modify/write cycle, data are maintained on the data output pin by holding $\overline{CAS}$ low. The data output is returned to a high impedence state, by returning $\overline{CAS}$ to a high state. Hidden refresh capability allows the device to maintain data at the output by holding $\overline{CAS}$ low while $\overline{RAS}$ is used to execute $\overline{RAS}$ only refresh cycles.

Refresh is required for data retention. Refreshing is accomplished by performing $\overline{RAS}$ only cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of addresses A_0 to A_6, during a 2-ms period. Address input A_7 is a DON'T CARE during these refresh cycles. A write cycle will refresh stored data on all bits of the selected row except the bit that is addressed.

Circle 441 on Inquiry Card

High speed sample/hold built for military applications

Specially built for military applications in the −55 to 125 °C temperature range, a high speed sample/hold amplifier features precision laser trimmed thin film resistors and is available with MIL-STD-883 processing. HS346, from Hybrid Systems Corp, 22 Linnell Cir, Suburban Industrial Park, Billerica, MA 01821, is pretrimmed to a maximum of 0.02% gain error with a low sample to hold offset of less than 4 mV. The company claims that the gain will stay within ±0.05% over the temperature range.

Other key performance specifications include an aperture uncertainty of 6 μs, 0.01% linearity, and a 0.5-mV/μs droop rate. A small internal holding capacitor is combined with a high slew rate output amplifier for a fast signal acquisition time of 2 μs maximum. Pin and function equivalent to the MN346 and MN347 with equal or superior performance, the device is packaged in a 14-pin DIP.

Circle 442 on Inquiry Card

Single-chip 4½-digit CMOS A-D converter for DVM/DPM applications

ICL7135, a precision A-D converter with multiplexed BCD output and digital drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy. The ADC is suited for the visual display DVM/DPM market. 2.0000-V full-scale capability, auto-zero, and auto-polarity are combined with true ratiometric operation, exceptional differential linearity, and true differential input. All necessary active devices are contained on a single CMOS IC, with the exception of display drivers, reference, and a clock.

The device, from Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95104, combines high accuracy, versatility, and economy. Performance specifications include auto-zero to less than 10 μV, zero drift of less than 1 μV/°C, input bias current of 10 pA maximum, and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins that allow it to operate in more sophisticated systems. These include $\overline{\text{STROBE}}$, OVERRANGE, UNDERRANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART. All outputs are TTL compatible. Devices are available in the 0 to 70 °C temperature range, and are packaged in 28-pin plastic or cerDIP packages.

Circle 443 on Inquiry Card

MORE OF THEM.
MORE TO THEM.

The 1981 line-up of Memorex® OEM peripherals is bigger—*and smaller*—than ever before. Our 14-inch rigid disc drives, for instance, include mid-range units such as our under-100-mb Models 601 and 612, the 200-and 300-mb 677, as well as our latest, the Model 659, with 680 megabytes of capacity. Our eight-inch family features the Models 550 and 651 floppy disc drives, the 11.7-mb Model 101 and 23.4-mb Model 102 Winchester-type rigid disc drives and the new 25-mb Model 201, with 12.5 megabytes of fixed storage and 12.5 on a removable cartridge.

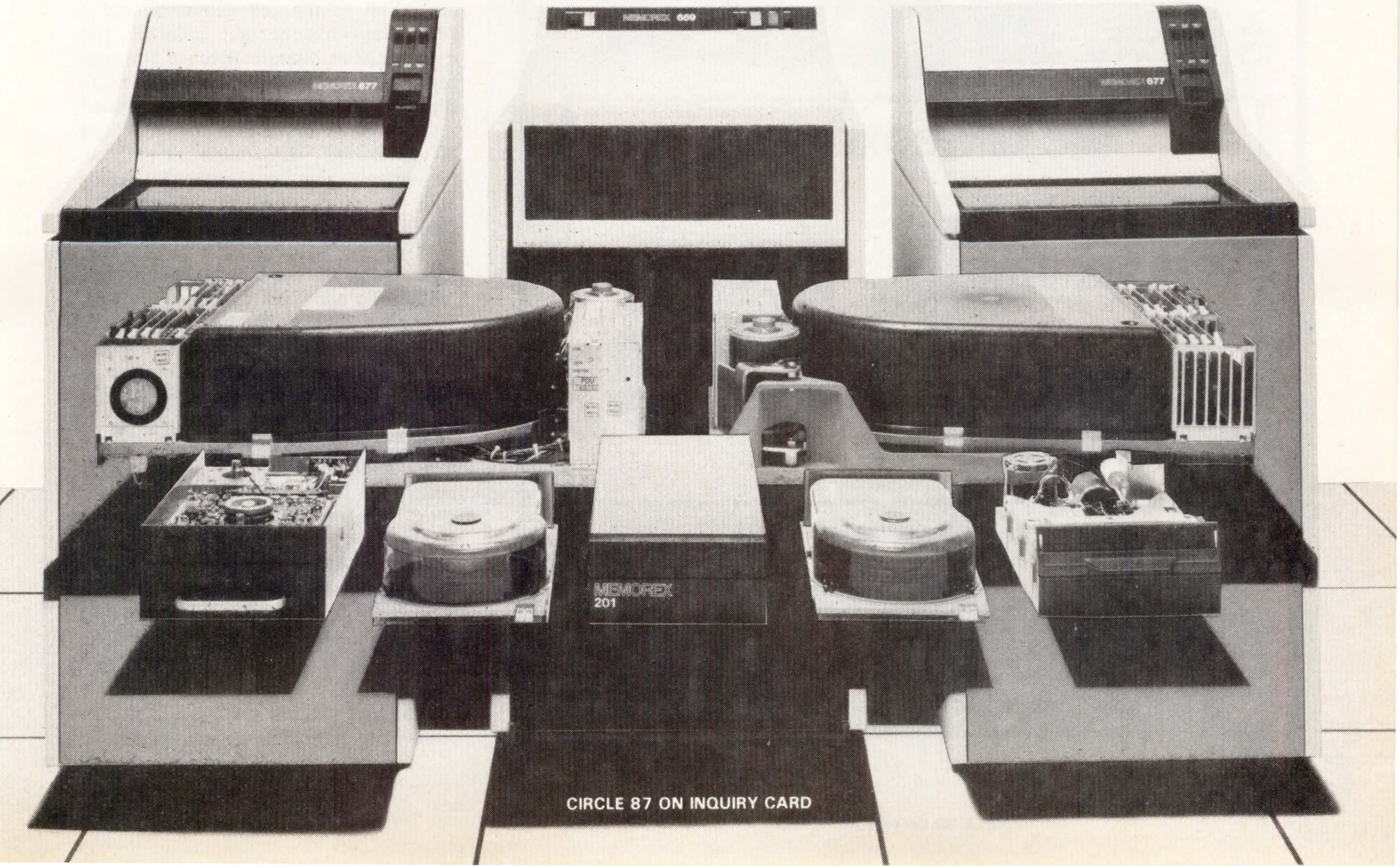
Together, these products represent a continuum of capacity and compatibility matched only by the continuum of quality that has always distinguished Memorex offerings. A continuum that reaches back through six generations of disc drive manufacturing experience and seven in disc packs and cartridges. And a continuum secured by Memorex's edge in technology, the investment in research and development and the fact that we create and control the key elements of our drives—the media, heads, PCBs.

The bottom line is more products—and, of course, better products. Products that mean more to our customers because—be it in engineering, manufacturing, test, service and support—they are products that mean more to us. Products that mean that, more than ever before, Memorex is in the OEM business. Call your Memorex representative for *more*.

MEMOREX

There's **MORE** in Memorex **OEM** products.

San Francisco Area (408) 987-1373; Los Angeles Area (714) 891-2541;
Boston Area (617) 890-0700; Dallas Area (214) 258-3510;
Denver Area (303) 837-0205; New Jersey Area (201) 325-0164;
Memorex International Headquarters: London, U.K. 01-572 7391.



CIRCLE 87 ON INQUIRY CARD

High soft error immunity is claimed for 64k dynamic RAM

Offered in versions with access times of 200, 150, and 120 ns, a 64k dynamic RAM is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage, and applications requiring low power dissipation and compactness. MSM3764, from OKI Semiconductor Inc, 1333 Lawrence Expy, Suite 401, Santa Clara, CA 95051, is a fully decoded RAM organized as 65,536 1-bit words. The device is fabricated using silicon gate NMOS technology and the company's double-layer polysilicon process. This manufacturing process, in conjunction with a single-transistor memory storage cell structure, allows maximum circuit density with minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

A high level of soft error immunity is claimed for the device (500 x 10^3 device hours with no alpha failures at 70 °C). High resistance to alpha particle errors is attributed to the cell geometry and a proprietary silicone chip coating. The dynamic RAM operates from a 5-V supply and draws 248 mW when active. On standby, the 120-ns device, designated -12, draws 28 mW, and the 150- and 200-ns devices, designated -15 and -20, respectively, require 23 mW. All inputs and the output are TTL compatible. Multiplexed row and column address inputs permit housing in a 16-pin DIP. Pinouts conform to the JEDEC approved pinout. To allow pin compatibility with upcoming 256k RAMs, pin 1 is uncommitted.

The RAM architecture is shown in Fig 1. A total of 16 binary input address bits is required to decode any one of the 65,536 storage cells within the RAM. All input addresses must be stable on or before the falling edge of $\overline{\text{RAS}}$ (row address strobe). $\overline{\text{CAS}}$ (column address strobe) is inhibited (or "gated") internally by $\overline{\text{RAS}}$ to permit triggering of $\overline{\text{CAS}}$ as soon as the row address hold time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Data are written during a write or read/write cycle. The last falling edge of

(continued on page 184)

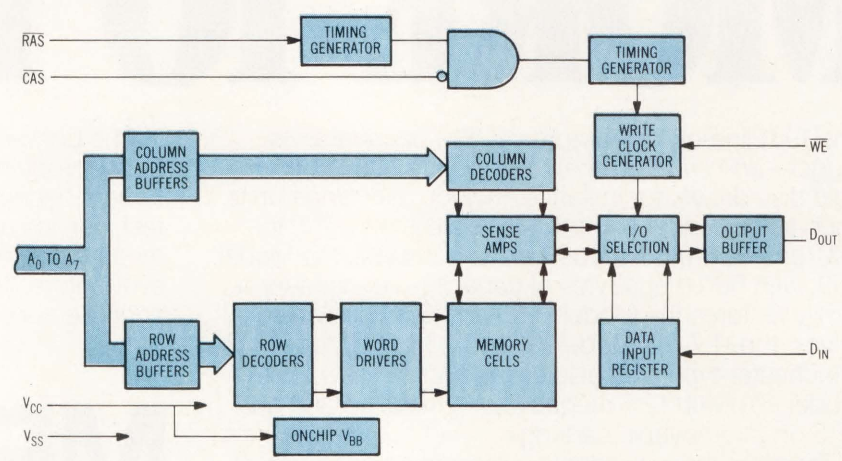


Fig 1 Block diagram of OKI Semiconductor's MSM3764 64k dynamic RAM. Eight row address bits are established on input pins (A_0 to A_7) and latched with row address strobe ($\overline{RAS}$). Eight column address bits are established on input pins and latched with column address strobe ($\overline{CAS}$)

NEW BIOMATION **K500-D**

Introducing the world's fastest logic analyzer. Incomparable.

500 MHz for debugging mainframes and super-minis.

Now you can dramatically shorten the debug cycle in high-speed random and stored program logic design with our powerful new 500 MHz, 8-channel K500-D. With state-of-the-art 16-bit microprocessor control, 2K static RAM memory and GPIB interface for fully-automated operation, the K500-D is the industry's most advanced integrated test tool for the digital designer.

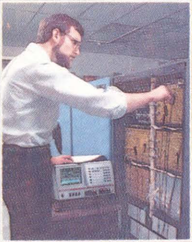
Resolution to 2ns.

Clocking via internal time base, or with your superfast system clock, the K500-D gives you the best timing resolution available in a logic analyzer today. Glitches, transitions and other critical events can be captured and sampled every two nanoseconds. You can even track a channel of analog activity at the same time for troubleshooting analog/digital interface, or for high speed cause-and-effect relationships. Two trigger levels gives you precise data trapping.

Advanced probe design.

Our probes were designed for high performance to cope with the speed and complexity of large systems, as well as complement the super high speed of the K500-D. Now, with 6-foot probes and hybrid buffering circuits in each probe tip, you can conveniently debug even the largest systems with minimum disturbance. With our unique scroll mode, you can probe hard-to-reach test points individually and build your timing diagram one channel at a time.

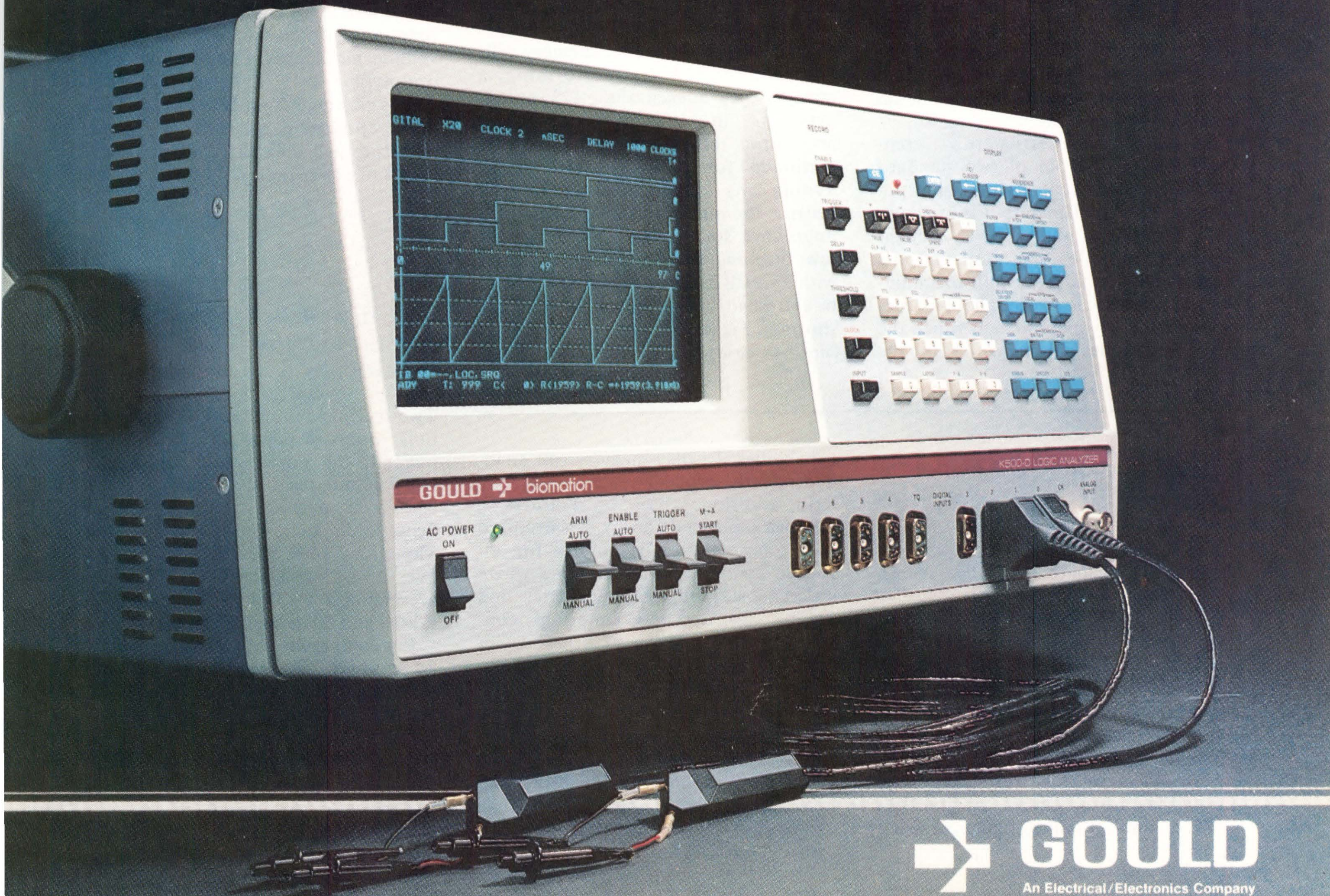
Legendary ease-of-use.



Our new K500-D is even easier to use than our best-selling K100-D . . . and that's saying something. Its status and data displays permit easy, flexible programming and data analysis. You can expand horizontally X10, X20, or X50, and specify the display format in binary, octal and/or ASCII.

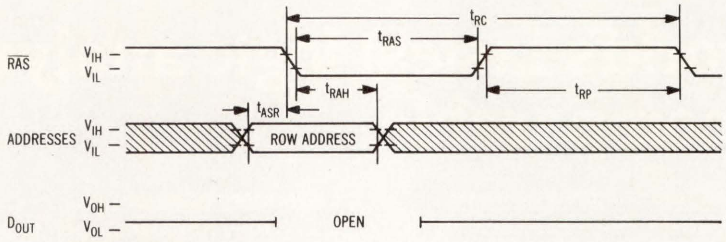
You owe it to yourself.

Any designer debugging mainframes or super-minis deserves full details on this revolutionary new logic analyzer. Write Gould, Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. Or call (408) 988-6800.



GOULD
An Electrical/Electronics Company

CIRCLE 89 ON INQUIRY CARD



t_{RAS} — $\overline{\text{RAS}}$ PULSE WIDTH
t_{RC} — RANDOM READ OR WRITE CYCLE TIME
t_{RP} — $\overline{\text{RAS}}$ PRECHARGE TIME
t_{RAH} — ROW ADDRESS HOLD TIME
t_{ASR} — ROW ADDRESS SETUP TIME

V_{IH} AND V_{IL} ARE REFERENCE LEVELS FOR MEASURING TIMING OF INPUT SIGNALS. V_{OH} IS OUTPUT HIGH VOLTAGE AND V_{OL} IS OUTPUT LOW VOLTAGE.

Fig 2 Refresh timing of MSM3764 dynamic RAM. Each of 128 row addresses must be refreshed every 2 ms. Further $\overline{\text{RAS}}$ only refresh results in substantial power dissipation

$\overline{\text{WE}}$ or $\overline{\text{CAS}}$ is a strobe for the data in (D_{IN}) register. In a write cycle, if $\overline{\text{WE}}$ is brought low (write mode) before $\overline{\text{CAS}}$, D_{IN} is strobed by $\overline{\text{CAS}}$, and the setup and hold times are referenced to $\overline{\text{CAS}}$. In a read/write cycle, $\overline{\text{WE}}$ will be delayed until $\overline{\text{CAS}}$ has made its negative transition. Thus, D_{IN} is strobed by $\overline{\text{WE}}$, and setup and hold times are referenced to $\overline{\text{WE}}$.

The output buffer is 3-state TTL compatible with a fanout of two standard TTL loads. Data out has the same polarity as data in. The output is in a high impedance state until $\overline{\text{CAS}}$ is brought low. Page mode operation permits strobing the row address while maintaining $\overline{\text{RAS}}$ at a logic low throughout all successive memory operations in which the row address does not change. Thus, the power dissipated by the negative going edge of $\overline{\text{RAS}}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row addresses (A_0 to A_6) at least once every 2 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{\text{RAS}}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{\text{CAS}}$ is brought low. Strobing each of 128 row addresses with $\overline{\text{RAS}}$ will cause all bits in each row to be refreshed. $\overline{\text{RAS}}$ only refresh timing is shown in Fig 2.

Circle 444 on Inquiry Card

Graphics display controller speeds display and manages display memory

A graphics display controller (GDC), when placed between a video display memory and a microprocessor bus, performs tasks required to generate faster displays and manages display memory. The intelligent microprocessor peripheral is compatible with the 8080/85/86, Z80, 6800, and other microprocessors. Designated μPD7220, the GDC minimizes host processor software overhead through its instruction set, integral DMA control, and graphics figure drawing capabilities. Display memory can be independently scrolled.

In addition, the GDC features a lightpen input and can by synchronized with other GDCs. It is suitable for advanced computer color graphics where space, cost, and both character and graphic displays are important considerations. The device is fabricated with 3.0-μ N-channel technology. Operating in excess of a 5-MHz clock rate and packaged in a 40-pin DIP, it requires a single 5-V supply. It is available from NEC Microcomputers, Inc, 173 Worcester St, Wellesley, MA 02181, and is second-sourced by Intel Corp.

Circle 445 on Inquiry Card

8192 x 8 static ROM with automatic power-down

Organized as 8192 words by 8 bits, a 64k ROM series has address access times of 200, 300, and 450 ns. SY2365A, from Synertek, 3001 Stender Way, Santa Clara, CA 95051, is designed to be compatible with all microprocessors. Applications are seen where high performance, large bit storage, and simple interfacing are important. The ROM conforms to the JEDEC approved pinout for 28-pin 64k ROMs.

The ROM includes an automatic power-down. Power-down is controlled by the chip enable ($\overline{\text{CE}}$) input. When $\overline{\text{CE}}$ goes high, the device will automatically power-down and remain in a low power standby mode as long as $\overline{\text{CE}}$ remains high. This feature provides system level power savings as high as 90%. An output enable function eliminates bus contention in multiple-bus microprocessor systems. Two programmable chip selects allow up to four 64k ROMs to be OR-tied without external decoding.

The device is pin compatible with the 2764 EPROM, thus eliminating the need to redesign printed circuit boards for volume mask programmed ROMs after prototyping with EPROMs. The company's existing 24-pin 16k, 32k, and 64k ROMs operate in the SY2365A's 28-pin socket, as will 128k and 256k parts.

Circle 446 on Inquiry Card

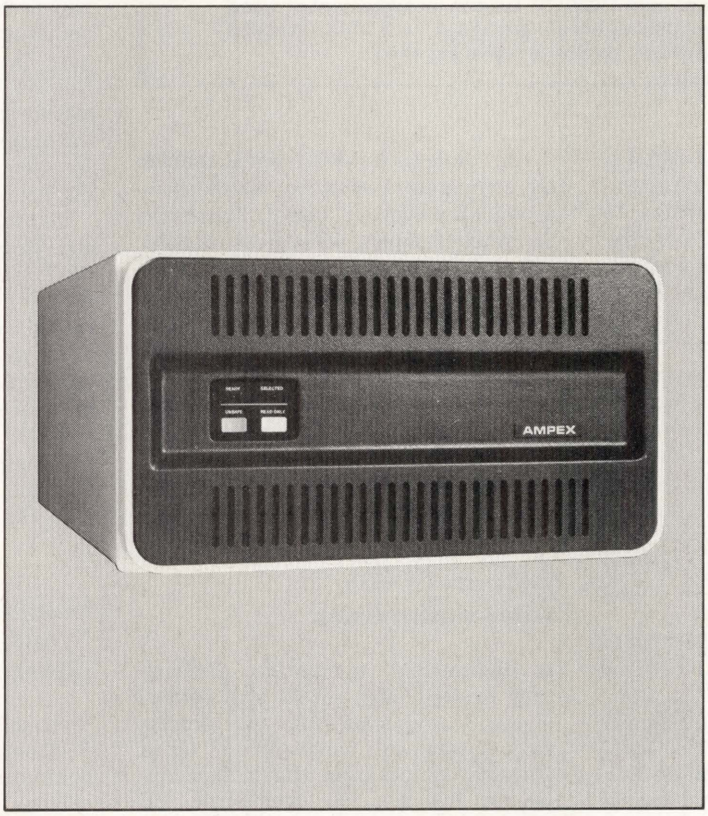
Fast 1k and 2k P/ROMs with titanium-tungsten fuses require low power

Two recently announced P/ROMs require only 70 mA of power or approximately one-half the power required by their NiCr counterparts that draw 130 mA. The latest members of the low power Schottky bipolar P/ROM family, from Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, have access times of 55 ns for the 1k TiW P/ROM and 60 ns for the 2k device.

Pin compatible with standard Schottky P/ROMs, these titanium-tungsten P/ROMs are organized as 256 x 4-bit (1k) and 512 x 4-bit (2k) configurations. Commercial parts are identified as 63LS140/1 (1k) and 63LS240/1 (2k). Military parts are designated 53LS140/1 and 53LS240/1.

Circle 447 on Inquiry Card

THE EXPANDING AMPEX WINCHESTER FAMILY.



Discover two new cost-effective members of the Capricorn family of Winchester 3350 rack-mounted disk drives. One has a capacity of 165 megabytes, the other 330 megabytes.

You get low cost of ownership. For several reasons. First, a reduced component count and self-test diagnostics performed by the built-in microprocessor, combined with the recognized advantages of Winchester assure less down time and few service calls. Second, there's the additional benefit of an attractive purchase price.

There are more pluses! For example, no preventive maintenance! And seven functionally partitioned modules that are easily replaced for fast and efficient service. This provides you with reduced spares inventory; another cost savings benefit.

There's more! Standard SMD/CMD compatibility, and simplicity of design that offers fewer interconnections, for higher reliability.

When you add it up, the sum total is that the Capricorn family of Winchester drives is designed and configured to meet your needs with maximum efficiency and low cost. A product line for the 80's.

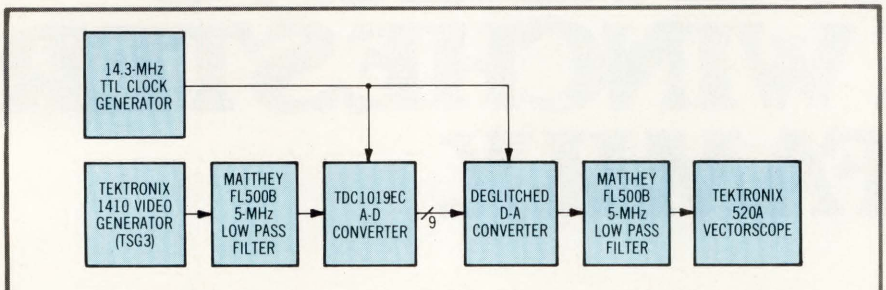
For the whole incredible story of the Capricorns call Gary Owen at (213) 640-0150, or write him at Ampex Corporation, Memory Products Division, 200 N. Nash Street, El Segundo, CA 90245.

AMPEX

MAKES THE DIFFERENCE

CIRCLE 90 ON INQUIRY CARD

ADC capable of 20M-sample/s operation



TDC1019J A-D converter from TRW/LSI. Used in measurement of video test signals, A-D and D-A converters are strobed at 14.3 MHz, unlocked from color subcarrier, and full composite signal encoded

Capable of digitizing an analog signal at rates up to 20M-samples/s, a high resolution, monolithic "flash" analog to digital converter utilizes 9-bit A-D converters. Using 9-bit, rather than 8-bit, converters doubles the number of usable, undistorted conversions. Applications for the device include video data conversion, radar data conversion, high speed multiplexed data acquisition, microprocessor based instrumentation systems, digital oscilloscopes, satellite communications, and fiber optic transmission systems. Designated TDC1019J, from TRW/LSI Products, PO Box 2472, La Jolla, CA 92038, the 64-pin ceramic DIP device operates from a single −5.2-V supply.

To help ensure that internal noise does not affect performance, ECL interfaces are used. Because ECL is a nonsaturating logic family, ECL circuits generate less noise than do TTL circuits. The differential configuration of ECL presents a nearly constant power supply load avoiding the relatively large current swings that are characteristic of TTL.

To convert an analog signal, the ADC accepts a 2-V input, compares it with an internal reference voltage, and activates a specific number of its 511 differential comparators in accordance with the magnitude of the applied voltage. For example, at 0 V no comparators are turned on, at 1 V 255 are turned on, and at 2 V all 511 are activated. A 511:9 encoder then supplies a digital input to a 9-bit latch, that, in turn, provides complementary ECL outputs. The ac characteristics of all comparators are matched. Parasitic capacitance, resistance, and inductance are held within tight tolerances by making all 511 comparators topologically identical.

An ECL level CONVERT signal enables the comparators, encoder, and latch to produce the digitized output. The device accurately samples, without an external sample/hold circuit, input signals with large signal frequency components up to 7 MHz. Input offset voltages are held to less than 1 mV to yield less than ½ LSB linearity error. The ADC also features a differential phase of 0.5%, differential gain of 1.0%, and an aperture jitter of 25 ps.

Circle 448 on Inquiry Card

4-channel CMOS video multiplexer

A single-ended, monolithic, dielectrically isolated, high speed, high performance analog multiplexer can process video signals with bandwidths of up to 10 MHz. HI-524, from Harris Semiconductor, PO Box 883, Melbourne, FL 32901, is designed to operate into a wideband buffer amplifier, such as the HA-5190 fast settling op amp. The device also provides two ON switches in series for use as a feedback element in conjunction with the amplifier.

High channel to channel and OFF isolation of 60 dB at 10 MHz makes the device well-suited for applications in which high isolation is required, such as telemetry and radar systems applications. HI-524 is packaged in an 18-pin ceramic DIP and is now available in HI-524-5 (0 to 75 °C), HI-524-2 (−55 to 125 °C), and HI-524-8 (MIL-STD-883 Class B) configurations, as well as HI-524-6 dice and HI4-524 LCC packages, both available for hybrid applications.

Circle 449 on Inquiry Card

CMOS chips drive LCD dot matrix displays

PE 7901 and PE 7902 metal gas CMOS LSI chips are versatile LCD 5 x 8 dot matrix display drivers. PE 7901 generates the multiplexing backplane-row driving signals for 8 scan lines and PE 7902 drives 40 columns or 8 alphanumeric, graphic 5 x 8 dot matrix displays. An 80-character display system requires one PE 7901 and ten PE 7902 chips. Both are available from Polycore Electronics, 1107 Tourmaline Dr, Newbury Park, CA 91320.

Five voltage level LCD multiplexing schemes are employed for optimum display performance. The voltage levels can be adjusted through voltage level input pins. During the display mode, an onchip clock generator on PE 7901 generates all the clock and timing information for the display system. A direct access input for the selection of the annunciation display is also provided.

PE 7902 contains an onchip 8-row x 40-column bit map RAM for storage of display information. Reading and writing of the display RAM are fully controlled by the onchip microprocessor interfacing circuits. Graphic display can be implemented through the programmable bit map storage and display. Power dissipation is less than 20 μA/character. For simplicity of use and better display contrast, a single 9-V battery is required.

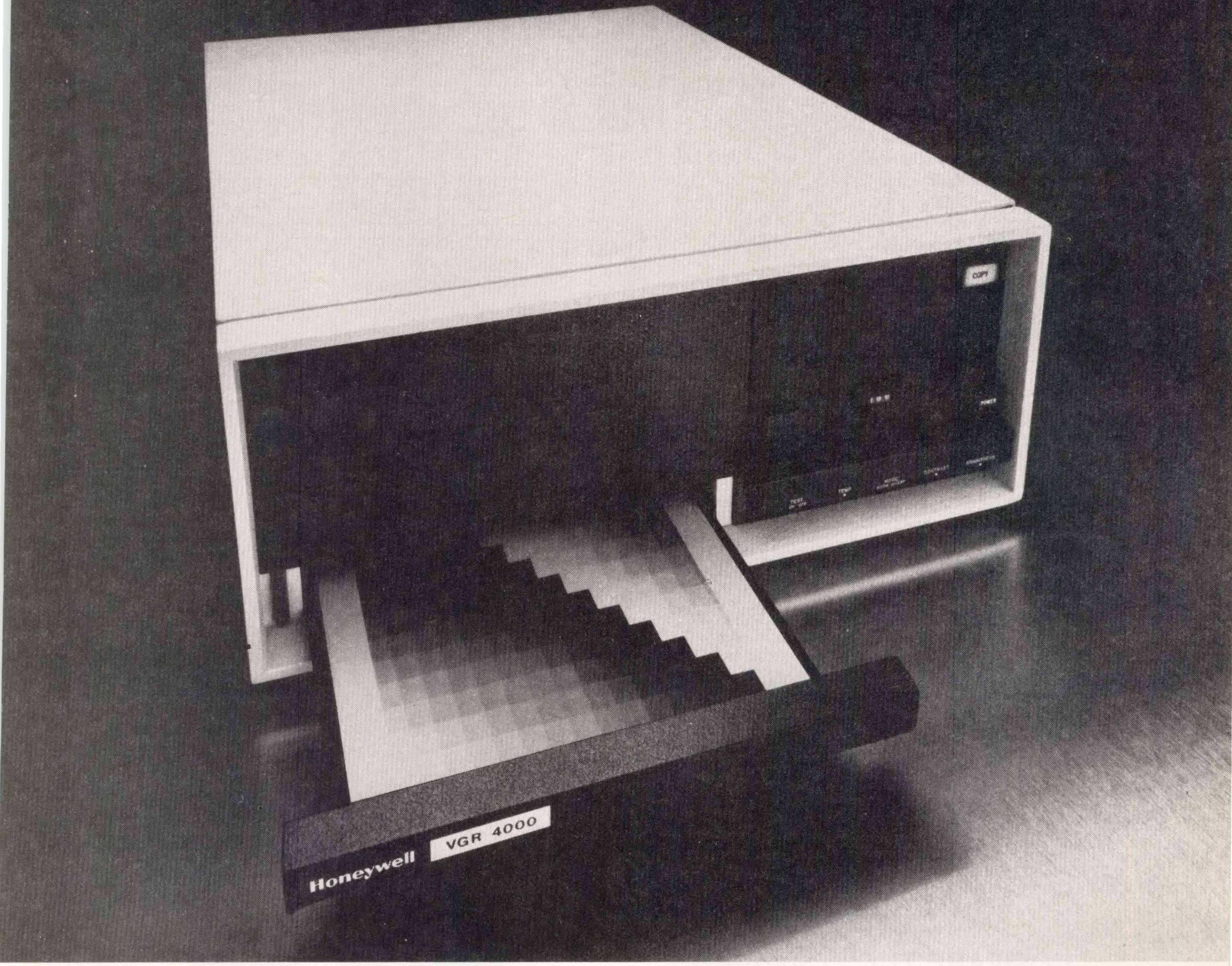
Circle 450 on Inquiry Card

Complementary N- and P-channel power MOSFETs

Two series of complementary N- and P-channel power MOSFETs are designed for microprocessor and IC logic interface driving, motor control, sensing and timing circuits, power supplies, and frequency amplification applications. Utilizing a vertical DMOS structure with compact interdigitized geometries, ZVN01 and ZVP01, from Ferranti Electric Inc, Semiconductor Products, 87 Modular Ave, Commack, NY 11725, offer low input capacitance and fast switching speeds. They can be paralleled without base current sharing resistors, and do not exhibit thermal runaway and thermally induced secondary breakdown. Both series consist of 10 devices, with voltages ranging from 20 to 200 V and drain current ratings up to 3 A. Each is available in TO-39, TO-92, or TO-220 packages, either as arrays in 14-pin DIL packages or in chip form.

Circle 451 on Inquiry Card

THE LATEST ADVANCE IN VIDEO GRAPHIC HARD COPY RECORDING FROM HONEYWELL



VGR 4000, Honeywell's new and advanced video graphic recorder, provides fast, crisp, 8½ x 11″ hard copies on dry silver paper from most CRT's and other video sources.

White-on-black or black-on-white images are as simple as flipping a switch. With options, images can be produced having up to 16 shades of grey or even more.

An innovative processing technique eliminates the need for large heated platens. This allows the recorder to run cool, consuming very little energy.

The VGR 4000 is the only recorder on the market available with a self-contained test-pattern generator providing a choice of formats for proper copy verification.

Rugged, yet cleanly designed for easy operation, the compact VGR 4000 can be used on a desk top or rack-mounted, taking up only 7″ of front panel space.

Honeywell's VGR 4000 is the latest advance in video-input hard-copy reproduction systems, built by the people with the most fiber-optic CRT recorder experience in the field.

To get the whole story on the VGR 4000 and how it can meet your needs, call Durke Johnson at 303/773-4700. Or write Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

WE'LL SHOW YOU A BETTER WAY.

Honeywell

HON-6-631

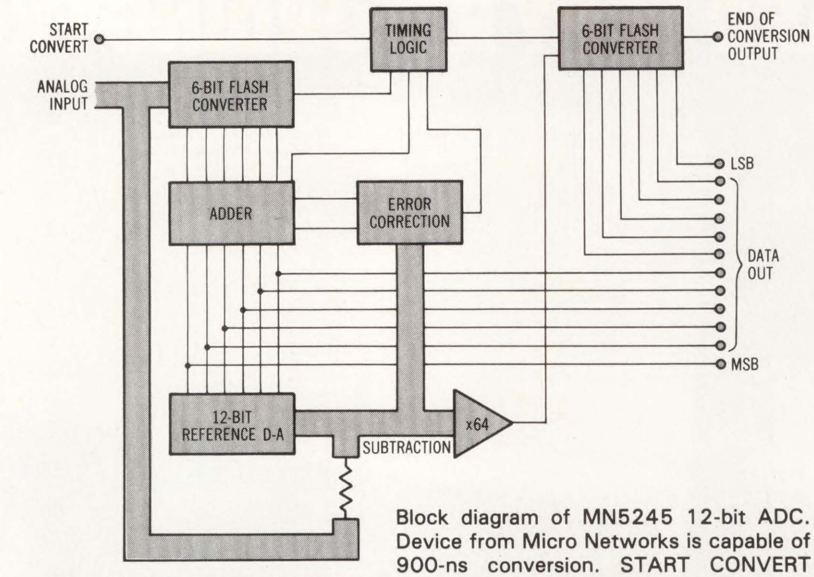
CIRCLE 91 ON INQUIRY CARD

12-bit A-D converter has 1-μs max conversion time

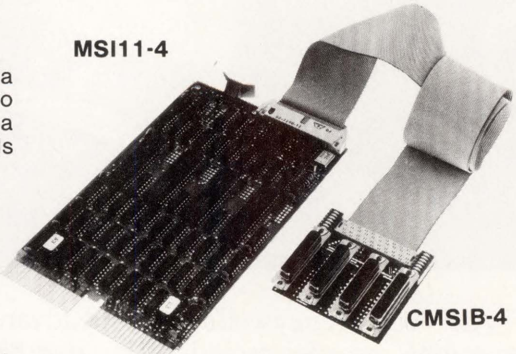
MN5245 is claimed to be the first complete 12-bit ADC in a dual-inline package to offer a maximum conversion time of less than 1 μs. Linearity is better than ±1 LSB, and no missing codes are guaranteed over the full operating temperature range. Absolute accuracy is a maximum of 0.3% FSR over temperature without the need for external adjustment or calibration. The recently announced device is available from Micro Networks Co, 324 Clark St, Worcester, MA 01606.

Capable of 1-MHz word rates, the ADC is suited for high speed data acquisition where reliability, accuracy, and size are important considerations. The high speed of the device allows the replacement of up to twenty 25-μs converters at a savings in cost and system complexity. Typical applications are spectrum analyzers, fast Fourier transforms, radar, video digitizing, and high speed digital data processing systems. The standard operating temperature range is 0 to 70 °C. For military/aerospace and demanding industrial applications, the MN5245 is available with an extended temperature range of −25 to 85 °C and high reliability screening to the requirements of MIL-STD-883 Method 5008.

Circle 452 on Inquiry Card



Block diagram of MN5245 12-bit ADC. Device from Micro Networks is capable of 900-ns conversion. START CONVERT signal must be positive pulse with a minimum pulse width of 40 ns. If pulse is more than 60 ns, additional time will be added to conversion



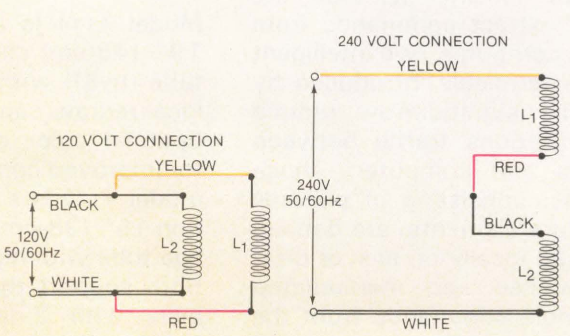
Dual voltage. For wherever in the world you connect!

Here's 60Hz and 50Hz, 120- and 240-volt versatility in one fine axial cooling fan for domestic and foreign applications. CFM ranges from 20 to 120. With or without venturi. And a choice of three designs for mounting on $4\frac{1}{8}$" or $2\frac{13}{16}$" centers.

All from a top name in electric motors for just about everything—Gould. These Brutes feature Gould's open frame design and patented Recirk™ bearing lubrication system for extended life.

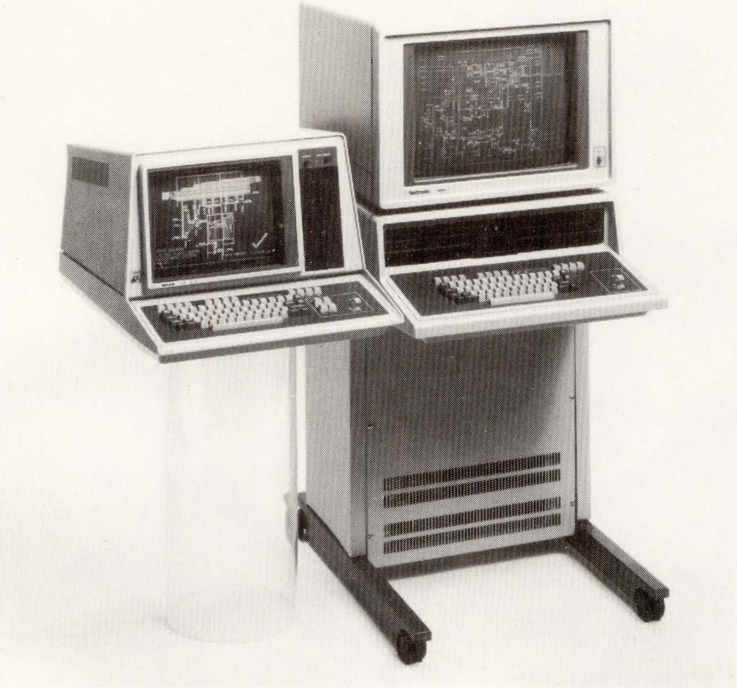
Metal parts are coated with a corrosion inhibitor and only flame-retardent plastics are used. U.L. recognized and CSA certified. Special modifications can be designed in.

For more details or to order these inventory-reducing fans, call (315) 788-5530. Gould Inc., Electric Motor Division, 6393 Coffeen Street, Watertown, NY 13601.



GOULD
An Electrical/Electronics Company

CIRCLE 93 ON INQUIRY CARD



Standalone capabilities of intelligent graphics terminals reduce dependency on host computer

Because they retain picture segments locally, without the need to extract commands from the host computer, two intelligent graphics terminals introduced by Tektronix significantly reduce communications traffic between terminals and computer. Those segments, consisting of pictures and picture elements, are defined and stored locally on RAM or disc, then recalled and manipulated with simple commands from the host computer. There is no need to retransmit all vectors or for the host to act each time a segment is used.

Characteristics and capabilities

Model 4114 is a high resolution 19" (48-cm) direct view storage tube (DVST) with refresh and fast local redraw capabilities and with optional color enhanced refresh for improved contrast (Option 31); model 4112 is a moderate resolution 15" (38-cm) raster scan storage tube with high addressability. Both support the segment capability with 2-dimensional transforms that translate, rotate, and scale the picture segments. The necessary refresh is inherent in the raster terminal, while the DVST has been augmented with the capacity for 3000 short vectors in refresh, and a fast redraw feature that additionally updates the screen. (An IC mask containing 26,000 short vectors stored in RAM can be erased and redrawn on the screen in less than 0.5 s.) On the Option 31 DVST the refreshed information appears in orange-red rather than in the normal green of the stored image.

Data communications speeds—up to 19.2k baud on the 4114 and continual transmission of 9.6k baud on the 4112—are considered more than adequate for most current user requirements, but provide capability for future needs. Block mode asynchronous transmission and half-duplex communication are available as an option.

In block mode communications, a means of ensuring integrity of data transferred, checksum is appended to each block for error detection. Using block mode, any host computer can use the compact instruction formats, even if those hosts cannot normally send or receive such information as control or lowercase characters. Full 8-bit binary files can be sent over any link and/or host operating system. Error checking is ensured, and long strings of data, such as graphic input strokes, can be entered without regard for overrunning the host input buffer.

To support the expanded local capability, RAM capacity is expandable up to a total of 800k bytes, and optional single or dual flexible disc mass storage provides 512k bytes/disc.

Standard RS-232-C data communications interface includes flagging and independently specified transmitting and receiving rates. An optional RS-232-C 3-port peripheral interface enables plug-to-plug connection of peripheral devices such as the 4642 printer, 4662 or 4663 interactive digital plotters, and other RS-232-C devices such as graphics tablets and hardcopy units. Offline plotting and background spooling, in which results may be output to disc and plotted while the user continues with other tasks, can be accomplished via the peripheral interface.

Storage tube resolution of the 4114 serves applications where high density of line graphics and text is required. A user-definable, scrollable dialog area adds to the available workspace on the screen.

The model 4112 may be preferred for applications where selective erase or shaded area fills are important or where the terminal must be used in an area with high ambient lighting. An optional multiple bit plane feature adds two memory planes to the terminal's single standard plane to provide three separately addressable display surfaces or overlays and up to eight shades of gray. Addressable resolution consists of 4096 x 4096 addressable points behind a 640 x 480 viewable point screen. Local zoom and pan capability lets the user magnify and move the addressable area around to bring selected portions into view.

Up to 16 viewports on the 4112 can be individually defined, with separate zoom and pan for each. Several displays, or several perspectives of the same display, can be displayed at once. A user-definable, scrollable dialog area keeps commands from cluttering the workspace. Optional block mode communications and an RS-232-C peripheral interface, similar to those for the 4114, are also available for the 4112.

Both terminals, as well as other future models in the 4110 series, will be supported by Tektronix PLOT 10 IGL software, with added features such as locally retained picture segments, supported by IGL modules. Existing programs that use the PLOT 10 terminal control system will run on 4110 series terminals in 4010 series emulation mode. Existing 4010 series application programs will run on the 4110 series terminals with modification required only to implement the terminals' advanced features.

Specifications

Standard memory on both terminals is 32k bytes of RAM; however, the 4114 can be expanded to a total of 1M bytes of RAM/ROM, and the 4112 can be expanded to 672k bytes. Optional flexible disc mass storage, at 512k bytes/disc, is available in single- or dual-configuration for the 4114 and single for the 4112.

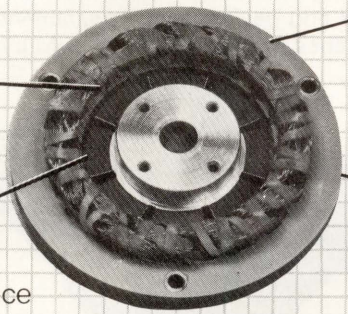
The standard alphanumeric character set on both models is a full 94 displayable characters. Optional foreign and APL character sets are available.

Power requirements are 90 to 132 Vac, 11 A max or 180 to 250 Vac, 5.5 A max, 48 to 62 Hz for the 4114, and 6.25 A and 3 A max at the same respective voltages and frequency range for the 4112. The 4112 is 51" (129.5 cm) high, 23.5" (59.7 cm) wide, and 32" (81.3 cm) deep and weighs 237 lb (107.5 kg); the 4114 is 21.5" (54.6 cm) high, 15.9" (40.4 cm) wide, and 32" (81.2 cm) deep and weighs 102 lb (46.3 kg).

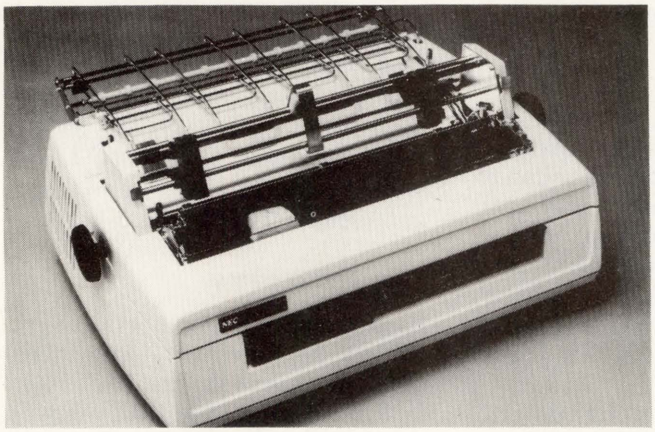
Price and delivery

Base prices for model 4114, 4114 Option 31, and 4112 intelligent graphics terminals are $17,500, $19,500, and $9600, respectively. Deliveries are 6 to 8 weeks ARO for the standard units and 12 weeks for the Option 31. Tektronix, Inc, PO Box 500, Beaverton, OR 97077. Tel: 503/644-0161.

For additional information circle 199 on Inquiry Card.



Character printers provide letter quality hard copy at 55 chars/s



Electrical and mechanical advancements lower the "cost of ownership" for the seven models in the Spinwriter 7700 series of letter quality character printers and reduce the number of parts by 27% as compared to the company's previous series. Product support, test, shipping, installation, and maintenance costs are claimed to have been halved for the OEM owner. Electronics are on a single board, and the power supply is a single unit. Digital control techniques improve print quality for speeds up to 55 chars/s. MTBF is predicted to exceed 2500 hours.

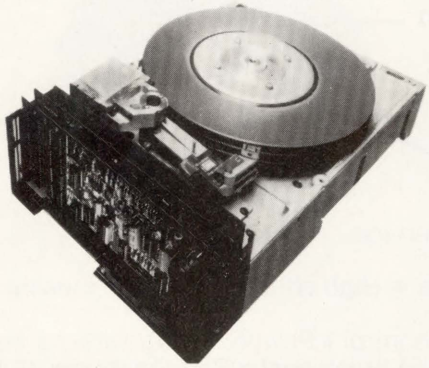
The seven models consist of two Qume- and Diablo-compatible OEM printer mechanisms—the 7700Q and 7700D—and five terminal models—the receive-only (RO) 7710 and 7715, the keyboard send-receive (KSR) 7720 and 7725, and the Centronics- compatible 7730. Models 7715 and 7725 are designated as Diablo- and Xerox- "compatible plus" versions.

Printer features that improve performance, reliability, and convenience include digital-drive head-positioning techniques that eliminate electrical adjustments and improve print quality, a dual-pressure roller assembly and 3-roller bail to eliminate paper handling problems and improve horizontal/vertical registration, and operator-interchangeable forms-handling options that can be installed or changed in minutes. Universal power supplies, switch-selectable to either 115- or 230-Vac operation at either 3- or 6-A output, provide for international operation. Some operator convenience functions and noise reduction covers are standard on the three terminal models and optional on the OEM mechanisms, while an enhanced diagnostic self-test feature improves overall performance on all models.

An optional word processing assist group for the terminal models allows the use of special print thimbles to provide user control of thimble position, carriage movement, and hammer energy. With this option the user can produce graphs, plots, and other non-standard printing; can automatically space proportionally spaced text; and can obtain other functions including half-line and negative half-line feed, automatic bold printing, shadow printing, and underscore offset selection. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.

Circle 200 on Inquiry Card

10M-, 20M-, and 60M-byte Winchester drives feature ANSI interface



Six models in a family of compact Winchester-type disc drives include ANSI interface and modularity to meet a variety of storage capacity and performance requirements. Four models in the 8400 series provide 10M- and 20M-byte unformatted capacities and two 8500 series models have 60M-byte capacities, with or without the data handling electronics for each capacity. Random average seek time of 65 ms is achieved in the 8400 series, which is based on stepper technology; while random average seek time of 29 ms in the 8500 series results from a high performance, voice-coil, servoed, rotary actuator. Both series transfer data at 933k bytes/s. Rotary actuators minimize the space and weight needed to accommodate standard flexible disc drive mounting dimensions. An ANSI X3T9/1226 rigid disc drive interface that handles up to eight drives is claimed to offer high performance at relatively low cost.

Modularity of the 8400 series allows one set of data handling electronics to operate either a 10M- or 20M-byte disc drive; in the 8500 a single electronics module controls up to four disc drives. While one disc module is seeking, either reading/writing or seeking may be initiated on another disc module. Although only one disc module can read or write at any given time, all four disc modules connected to one electronics module can be seeking simultaneously.

Each compact disc drive, including disc module and electronics module, fits into the same mounting bay as an 8" (20-cm) flexible disc drive—4.5 x 8.5 x 14.25" (11.4 x 21.6 x 36.2 cm)—with the same mounting holes, in vertical or horizontal configuration. An air flow system provides 29 circulation changes of air/min for a cleanliness of 10 or fewer 0.5 μm particles/ft^3/min.

Media densities are 219 tracks/in (86/cm) for 10M- and 20M-byte models and 693 tracks/in (273/cm) in 60M-byte models, and 8649 bits/in (3405/cm) for 10M- and 20M-byte models and 8555 bits/in (3368/cm) for 60M-byte models. Bit transfer rates are 7.47M bits/s or 933.3k bytes/s for all models.

Predicted MTBF is 10k hours or a life expectancy of 10 years. MTTR is 30 min for circuit cards or sealed disc module. Life expectancy of spindle bearings is 140k hours. Error rates are predicted to be 1 in 10^{10} recoverable, no retries, 1 in 10^{12} hard errors, and 1 in 10^{6} seek. **3M Co, Data Recording Products Div,** Box 33600, St Paul, MN 55133.

Circle 201 on Inquiry Card

adac...

Everything for LSI-11 data acquisition and control.

- mV Level A/D Conversion
- Temperature Measurements
- High Level, High Speed A/D Conversion
- TTL Level Digital I/O
- Discrete, High Voltage, AC/DC Interfaces
- Pulse Counters And Pulse Trains Out
- Optically Isolated Discrete I/O
- Contact Closure Sensing
- Discrete High Current Outputs
- Programmable Clock
- Serial Interfaces
- PDP-11 Unibus To LSI-11 Bus Translator
- Specially Designed Enclosures
- Screw Termination Panels
- Rack Mount System Cabinets
- CPUs/Memories
- Floppy/Tape Peripherals
- CRT Terminals
- Real Time Operating Systems
- FORTRAN, BASIC, Process Language

ADAC offers the widest selection of function cards and complete systems for LSI-11. Both analog and digital.

Call, write or circle the number below and we'll send you a complete packet of information, including ADAC's new Model Configuring Guide and Price List.

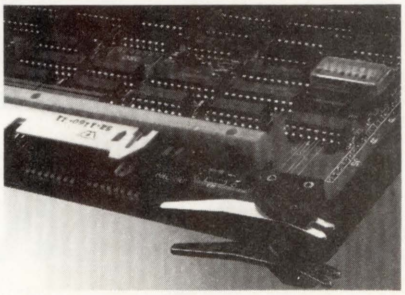
adac
CORPORATION
70 Tower Office Park • Woburn, MA 01801
(617) 935-6668

CIRCLE 95 ON INQUIRY CARD

PRODUCTS

Optimizers improve disc I/O rate by 80%

Add-on boards for the company's EDC series emulating disc controllers are based on a caching algorithm that transparently stores the most frequently used disc data in high speed onboard memory. The Turbo-21, a single-board unit, operates with the EDC-21 disc controller on Digital Equipment Corp's PDP-11 and VAX processors. Future models will function with the EDC-22 for Data General processors, with the EDC-23 for Perkin-Elmer processors, and the EDC-24 for DEC LSI-11 microcomputers.



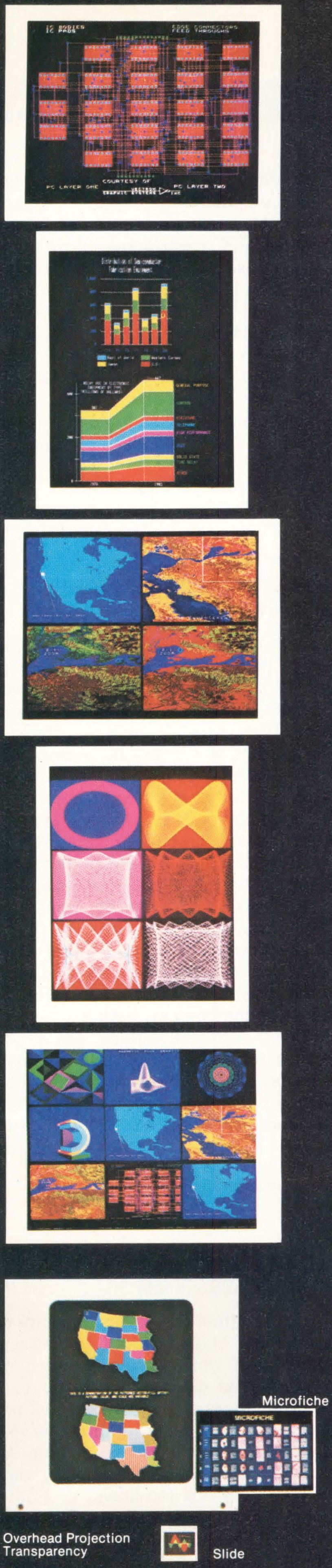
The presently available unit eliminates up to 80% of the seek and rotational latency time that occurs with conventional disc access. This action is completely transparent to the host operating system. The disc cache controller uses 128k bytes of dynamic onboard RAM with transparent refresh, allowing the board to store 256 sectors of data. A high speed onboard microcomputer uses a proprietary algorithm that caches the most frequently and recently used sectors on the board itself, eliminating the need for frequent disc accesses. An additional 32-bit error correcting code is included with each sector to ensure the same high degree of reliability as provided by the rest of the disc subsystem.

Table lookup and cache write operations occur in parallel with the data transfer. Since the disc cache operates in parallel with the controller, it can only increase performance, never degrade it. If a read is issued and the requested data are in the cache, the data are immediately transferred into memory via the controller. This eliminates the time normally spent on head positioning (seek time) and on waiting for the data to rotate under the heads (rotational latency), the greatest bottleneck in most systems. Data written to the disc are also written to the cache to maintain the same level of data integrity as an uncached operation.

The board is configured to fit into one hex-wide Unibus slot and attaches to the controller in the directly adjacent card slot. All communications with the host processor are done via the controller. The disc cache provides complete operating system independence and can be installed with no modifications to existing software.

Other features, requiring minor modifications to host software, further enhance the effect on system performance. In "lock" operation, up to 254 sectors can be locked into the cache memory. This allows the user to designate high-use sectors that will remain permanently in the optimizer memory until an unlock is issued. In "unlock," a locked sector, or sectors in the case of a multisector transfer, become unlocked from the cache and available as deletion candidates. "No cache" specifies that a particular transfer will not be cached if it is not already in the cache. This is useful for preventing the caching of large one-time transfers. **Minicomputer Technology,** 2470 Embarcadero Way, Palo Alto, CA 94303.

Circle 202 on Inquiry Card



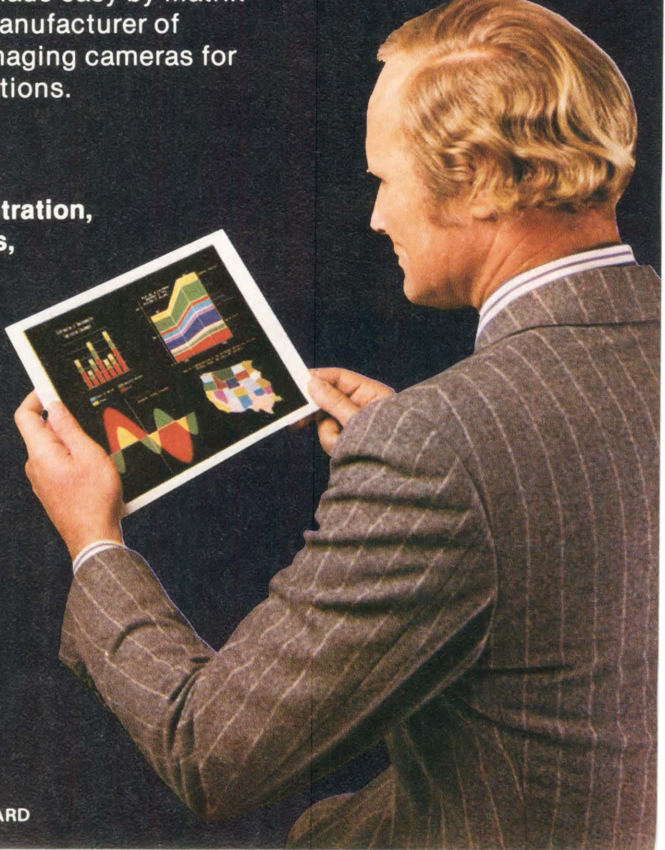
Color Graphics Hard Copy... Made Easy

The Matrix Color Graphic Camera System converts the output of any raster scan computer color terminal into brilliant, high resolution photographic hard copy. Both line and continuous tone images can be made with accurate, bright, saturated colors.

Our system does what no other instrument can do — it produces instant, on-the-spot results with Polaroid® 8 x 10 film, 8 x 10 color transparencies for backlit displays and overhead projection, 35mm color slides, 60 image color microfiche, and 16mm/35mm color animation films. All with one camera system. It also allows recording of multiple image formats. Related and sequential images can be recorded in orderly arrays, on a single sheet of 8 x 10 instant print film. The resultant ease of comparison and analysis is unmatched. The system is also fully modular and field upgradable . . . you purchase only the capability that you need now.

Microprocessor based electronics provide many automation, self-calibration, self-diagnosis and remote control functions. Color graphics hard copy made easy by Matrix Instruments, the leading manufacturer of precision electro-optical imaging cameras for diagnostic medical applications.

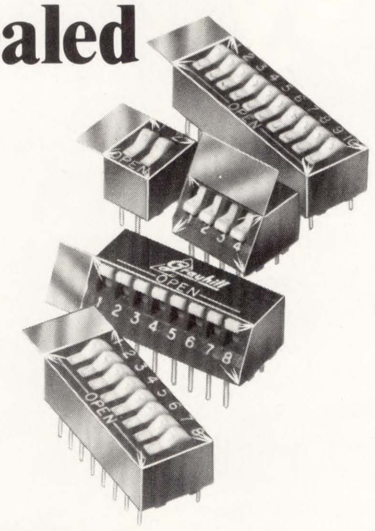
For more information,
film samples, or a demonstration,
contact Matrix Instruments,
230 Pegasus Avenue,
Northvale, New Jersey
07647.
Telephone (201) 767-1750
Or call toll-free:
(800) 526-0274.



MATRIX INSTRUMENTS

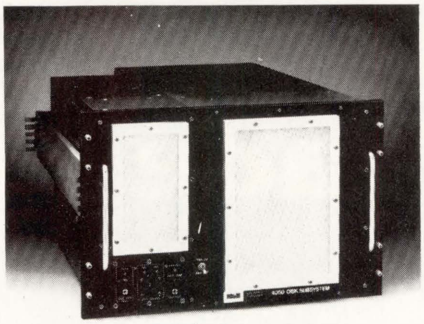
Hard copy shown reduced from original 8″ x 10″, slide, and microfiche films.
Multiple images recorded on a single sheet of film.
"Polaroid" is a registered trademark of the Polaroid Corporation.

CIRCLE 98 ON INQUIRY CARD



MEMORIES

MILITARY WINCHESTER DISC SUBSYSTEM



Model 4050 offers compact packaging, using 8″ (20-cm) Winchester technology to minimize chassis dimensions and maximize storage capacity. Requiring only 12.25″ (31.11 cm) of height in a 19″ (48-cm) RETMA rack, the unit provides 36.5M bytes of secondary memory in a 3.2-ft³ (0.09-m³) chassis, and is designed to meet shock and vibration specs of MIL-E-5400, MIL-E-4158, and MIL-E-16400. Model 4052 add-on drives provide additional storage capacity up to 142.4M bytes per disc controller. The entire subsystem consists of 6 field replaceable units. Head positioning is accomplished by a statically balanced rotary arm mechanism driven by a voice coil motor. Recording heads, disc media, and head positioning system are enclosed in a sealed clean area. Data transfer rate is 922k bytes/s. Access time is 42 ms average. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 203 on Inquiry Card

5.25″ WINCHESTER DISC

Packaged in the same proportional size as an industry std mini-floppy, 5.25″ (13.34-cm) Winchester disc provides low power requirements and an MTBF of 11,000 hours. The unit stores 6.38M bytes unformatted per drive and can access at an average of 170 ms. To maximize speed and accuracy, data are transferred at 5M bits/s. Using 2 discs/drive, information can be written and stored on all 4 sides. The drive includes a spindle mechanism, stepper motor, and head assembly with 4 read/write heads. Drive electronics that perform spindle-motor speed control, track stepping control, and basic read/write functions are located on 2 PC boards mounted under the disc. Heads and discs are built-in and tested as a single assembly, eliminating interchangeability and misalignment problems that cause mistracking. An integral fail-safe brake mechanism ensures head/disc reliability during start/stop operations by stopping disc rotation within 15 s. Sealed head to disc interface provides max protection against external contaminants even in harsh environments. **Texas Instruments Inc,** PO Box 202145 H-574, Dallas, TX 75220.
Circle 204 on Inquiry Card

30M-BYTE WINCHESTER/FLOPPY DISC SYSTEM

Model 880 is available with 8 single-sided (880 S/30) or double-sided (D/30) 8″ (20-cm) floppy discs. A Winchester drive provides DEC system users with high capacity memory. The unit is compatible with DEC hardware, software, and media, and requires no changes to the operating system with either a PDP-11 or LSI-11 based system. The system directly emulates 3 RL02 drives, providing 31.2M bytes of formatted storage, and can be used with either RT-11 or RSX-11 operating systems. The compact package, measuring 5.25″ (13.34-cm) high, contains a controller/interface card with bootstrap P/ROMs, and can be used in combination with a VT-103 intelligent terminal. Floppy disc in the unit can be used to back up the Winchester or to load diagnostics, or as a second random access device. **Data Systems Design, Inc,** 2241 Lundy Ave, San Jose, CA 95131.
Circle 205 on Inquiry Card

32k-BYTE BUBBLE MEMORY SUBSYSTEM

BLX-9252 offers 32k-bytes capacity on an 11-in² (71-cm²) board, operates at under 5 W, and is BLX microbus compatible. The device detects up to 3 random errors or an error burst 12 bits long, and corrects error bursts up to 3 bits long. Applications include airborne and shipboard systems, data loggers and POS terminals, and other memory systems requiring reliability, density, and nonvolatility. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Your speed machines are here. High speed, high performance Static RAMs.

For high speed mainframe, mini and micro memory applications, you can't beat the speed machines from Synertek.

There's a whole range of speeds available to meet your system needs. The SY2147 and SY2148 down to 55nsec. And the SY2149H down to 45nsec. For systems where speed is even more critical to performance, the SY2149H offers an enhanced Chip Select access time down to 20nsec.

The latest proven process technology—advanced high performance scaled N-channel MOS—is what makes these machines perform.

High Performance Selection Guide

Organization	Part Number	Speed	Operating Current (Max.)	Standby Current (Max.)
4Kx1	SY2147-3	55nsec	180mA	30mA
	SY2147L	70nsec	140mA	10mA
	SY2147	70nsec	160mA	20mA
	SY2147-6	85nsec	160mA	20mA
1Kx4	SY2148-3	55nsec	140mA	30mA
	SY2148	70nsec	140mA	30mA
	SY2148-6	85nsec	140mA	30mA
1Kx4	SY2149H-2	45nsec	150mA	*
	SY2149H-3	55nsec	150mA	*
	SY2149HL-3	55nsec	125mA	*
	SY2149H	70nsec	150mA	*
	SY2149HL	70nsec	125mA	*

*Not Applicable

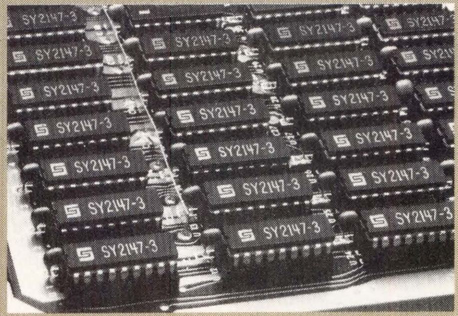
To exactly meet your system requirements, Synertek's speed machines not only deliver the performance you need, they deliver flexible organization, too. The SY2148 and SY2149H are organized 1Kx4 with common data I/O. For deeper high speed memory applications, there's the SY2147—organized 4Kx1 with separate data I/O.

You also get a choice of Automatic Power Down, available in both the SY2147 and SY2148. That can mean system level power savings of up to 80 percent.

Standard features include total TTL compatibility on all inputs and outputs, single +5V power supply, and three-state outputs. All use fully static circuitry. So you get identical cycle and access times with no clocks or strobes required.

Put yourself in the winner's circle. With the speed machines from Synertek. Contact your nearest Synertek distributor or representative. or call Memory Product Marketing direct at (408) 988-5611.

Synertek is a major MOS supplier of high volume parts with advanced technologies and techniques behind everything we make. Static RAMs. ROMs. Custom circuits. Single-chip Microcomputers. Systems. 6500 Microprocessors and Peripherals.



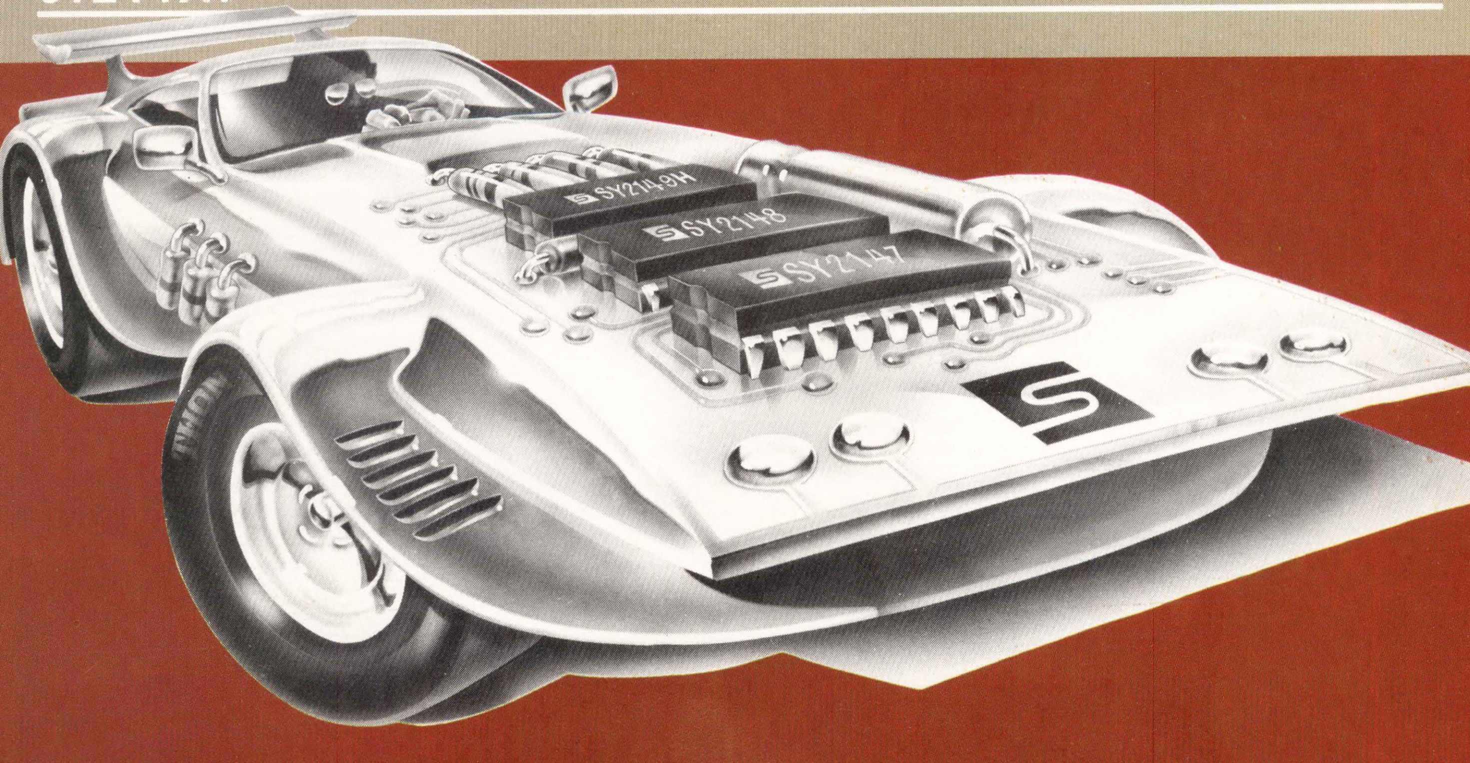
SYNERTEK

3001 Stender Way, P.O. Box 552
Santa Clara, California 95052
(408) 988-5600
TWX: 910-338-0135

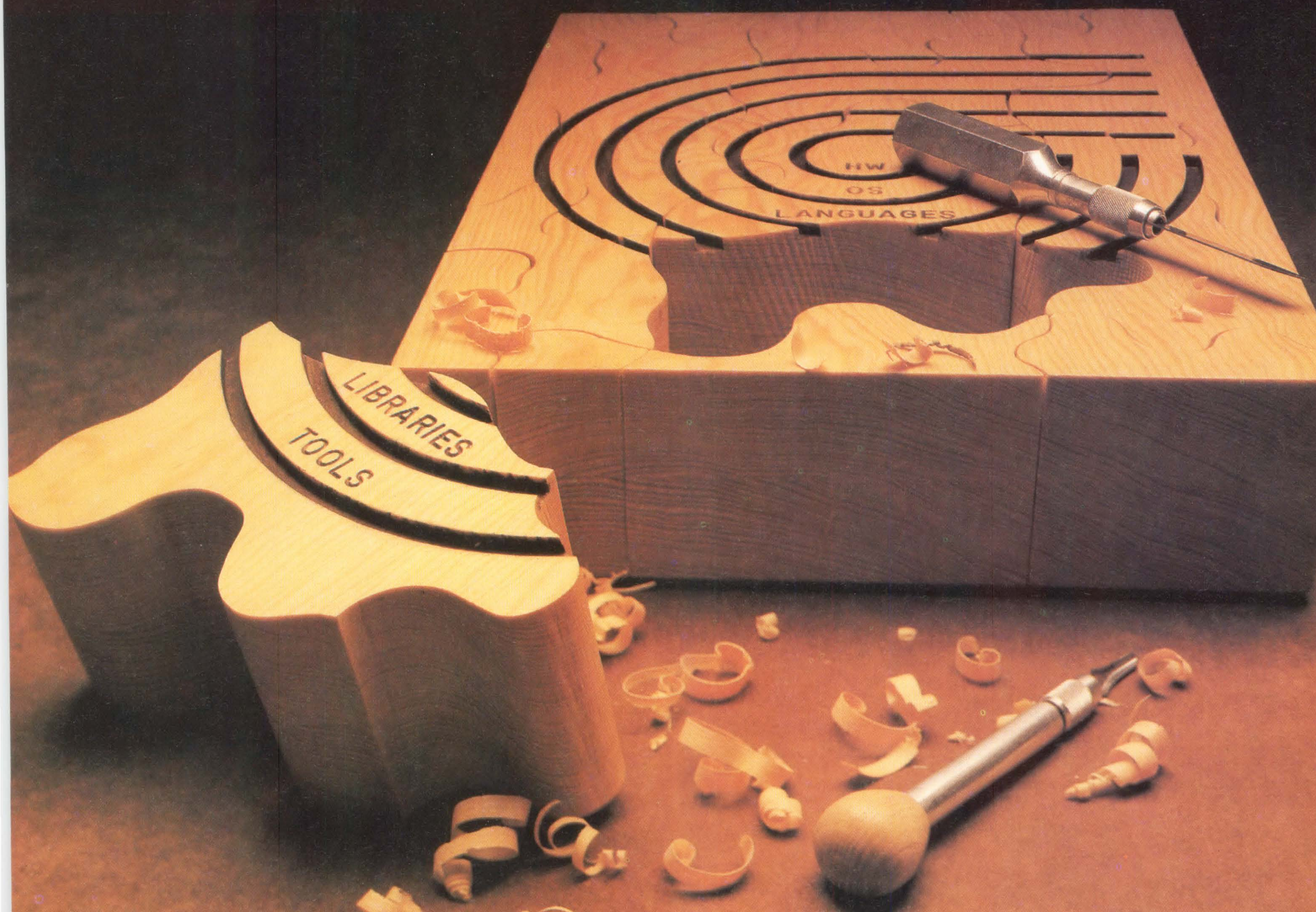
SY2147 — **55nsec**

SY2148 — **55nsec**

SY2149H — **45nsec**



Layered software for applications programming… helps the pieces fit.



Meeting each minicomputer user's software requirements is a difficult and time-consuming task for the systems integrator. Now, with a unique layered approach to software, SYSTEMS makes applications programming more efficient and less costly. Each layer addresses a related set of user programming problems. Within each layer, there is a choice of software aids that focus on specific user requirements.

In addition to most modern high-order languages and the advanced MPX-32 interactive, real-time operating system, SYSTEMS offers extensive software libraries. They contain prefabricated code to eliminate repetitive programming. SYSTEMS software tools and libraries allow the programmer to more efficiently generate, test, optimize and document applications programs and reduce development and maintenance costs. These tools also provide management with greater visibility and control.

SYSTEMS has the most comprehensive selection of software development tools and methodologies available today. We also offer the SOFTOOL 80™ package as a licensed part of our standard product line. Memory requirements and CPU overhead are never a problem as all the tools and libraries are removed after program development is completed.

SYSTEMS layered approach provides all the pieces for your applications programming needs …and they fit. Call or write the company with a lifetime of real-time experience and watch the pieces fall in place for you.

Systems Engineering Laboratories, Inc.,
6901 W. Sunrise Blvd., Ft. Lauderdale, FL 33313.
(305) 587-2900, 1-800-327-9716.

™Trademarked product of SOFTOOL Corporation.

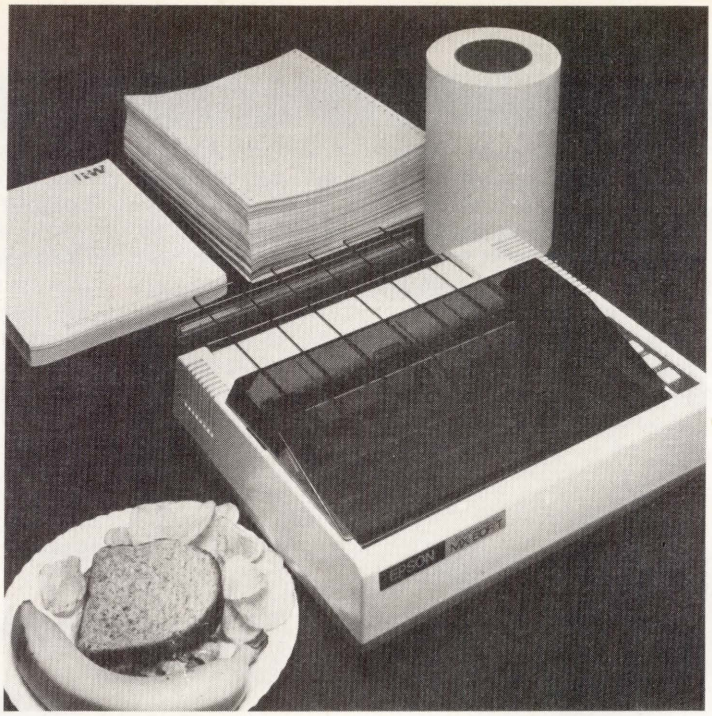
Proven COMPUTER Performance

SYSTEMS

A Subsidiary of GOULD INC.

Argentina•Australia•Belgium•Canada•Colombia•England
France•Italy•Japan•Mexico•Sweden•Thailand•West Germany

The new MX-80 F/T. You can feed it anything. Almost.



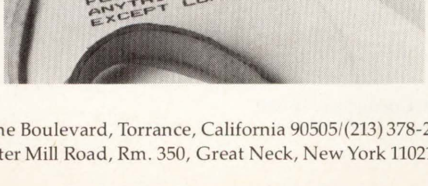
Epson.

This is Epson's newest and most versatile printer — the MX-80 F/T. It does everything the famous MX-80 does, and since it accepts both friction and tractor-feed paper, it prints on almost anything. So for many OEM uses, this printer may be the best printer you can buy.

It prints bidirectionally in your choice of 40, 80, 66, or 132 columns. And to make the throughput even faster than its 80 CPS, a logical-seeking function minimizes print head travel time.

It prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. And since all Epson printers are known for reliability — and the MX-80 F/T is no exception — it prints and prints and prints. You can expect 100,000,000 characters from the print head. And when the head finally wears out, it's so inexpensive you can just throw it away. To put in the new one takes only one hand and a few seconds of time. The MX-80 F/T is compact, weighs only 15 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor.

But here's the best part. The MX-80 F/T prints on just about anything you feed it. It has both a friction and a tractor-type pin-feed mechanism. So it prints on forms, labels, letterheads, roll or continuous fan-fold computer paper. Or even paper plates.



You can have the MX-80 F/T for under $750, and for even less in quantity. And for a printer that isn't finicky about what's for lunch, we call that chicken feed.

EPSON
EPSON AMERICA, INC.

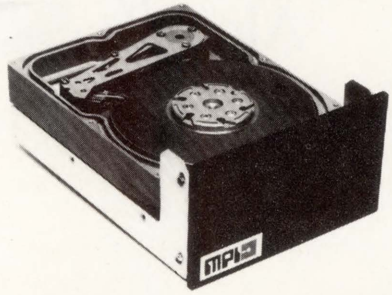
Western: 23844 Hawthorne Boulevard, Torrance, California 90505/(213) 378-2220 TWX: 910-344-7390
Eastern: 98 Cutter Mill Road, Rm. 350, Great Neck, New York 11021/(516) 487-0660

CIRCLE 102 ON INQUIRY CARD

41.6M-BYTE, 8″ WINCHESTER DISC SYSTEM

WINC-08 with controller and two 8″ (20-cm) Winchester drives fits into a package 5.25″ (13.34 cm) high to provide 4 times the storage capacity of a DEC RL02 drive in one-half the physical space. Providing 41.6M bytes of memory, the unit emulates the RL02 cartridge drive. Drives are partitioned into 2 logical sections so that each drive looks like 2 drives. The unit is software transparent to DEC operating systems. The system consists of 2 printed wiring board assemblies: the intelligent formatter/controller uses microprocessor based, high speed bipolar technology, and is housed with the disc drives; the host computer interface adapter is available as a dual-width card for LSI-11 users or as a quad-width card for the PDP-11. Interface boards generate the required DMA and interrupt sequences necessary to emulate the RL02. The controller accommodates 2 drives, providing formatted capacity of 20.8M bytes/drive. ECC identifies and corrects errors up to 5 continuous bits long. MTBF of drives is 10,000 hours. **Advanced Electronics Design, Inc,** 440 Potrero Ave, Sunnyvale, CA 94086. Circle 206 on Inquiry Card

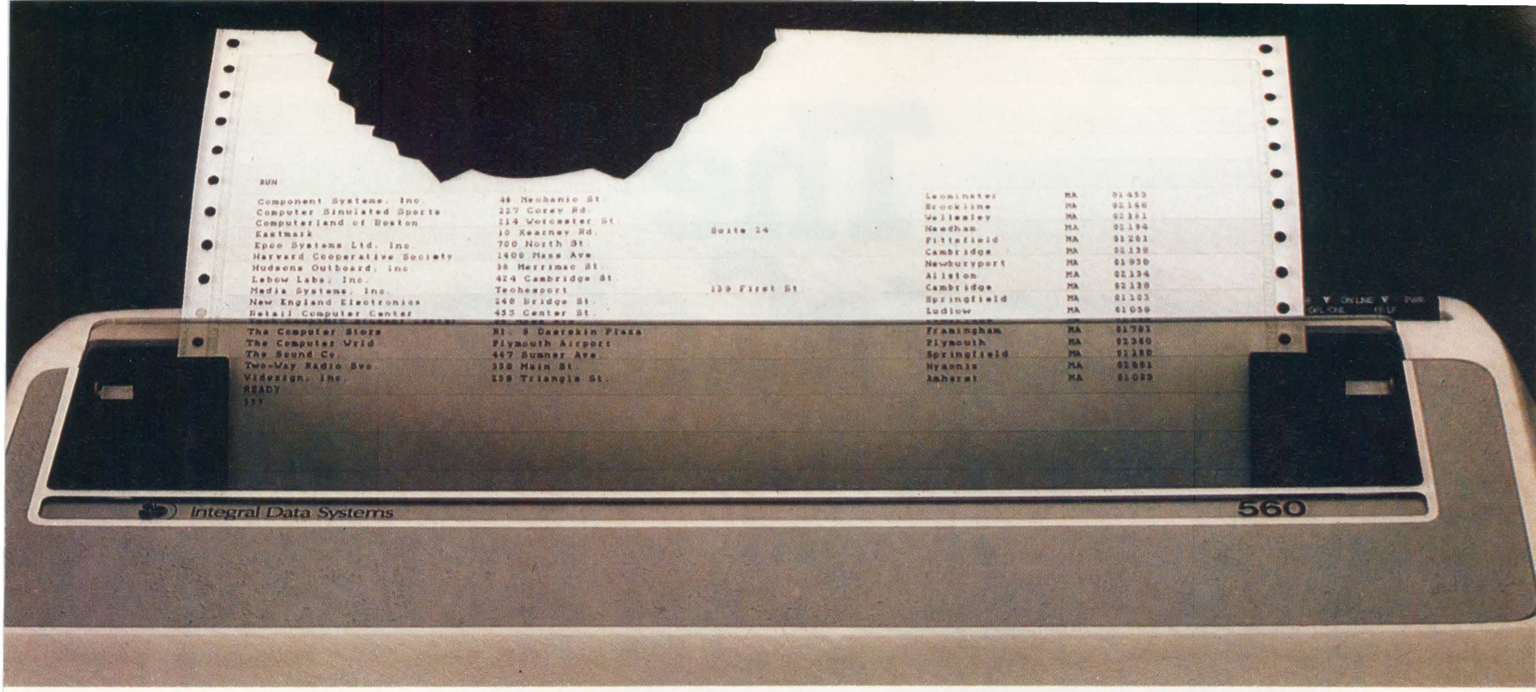
5.25″ WINCHESTER DISC DRIVE



Super-Micro model 10 is an intelligent 5.25″ (13.34-cm) fixed Winchester drive with unformatted capacity of 12.06M bytes, and average access time of 25 ms—3 to 4 times faster than comparable Winchesters. Each drive fits in the same slot and uses the same mounting holes as a 5.25″ flexible drive. Track to track access time is 3 ms. Data transfer rate is 5M bits/s. MTBF is cited as 10,000 hours; MTTR as 30 min. Hard error rate is 1 in 10^{12} bits read, and soft error rate is 1 in 10^{10}. **Micro Peripherals Inc,** 9754 Deering Ave, Chatsworth, CA 91311. Circle 207 on Inquiry Card

DISKETTE SUBSYSTEM

Model 8202 is completely compatible with DEC's LSI-11 microcomputer; it replaces DEC's RXV21 (LSI-11 RX02) diskette subsystem and is fully compatible with RXV21 register definition and command protocol. Subsystem operates, without modification, with operating systems and diagnostics designed for the RXV21. Controller electronics are included, and are mounted on a single dual-height card that plugs into std LSI-11, -11/2, or -11/23 Q-bus slot. Onboard bootstrap automatically boots single- or double-density diskette. **Dynalogic Corp, Ltd,** 141 Bentley Ave, Ottawa K2E 6T7, Canada. Circle 208 on Inquiry Card



Meet the Tiger with a bigger bite.

Introducing the remarkable 132-column Paper Tiger™ 560. The first full-width matrix printer to give you fully formed characters for a low $1695.*

The new 560 features a staggered nine-wire ballistic type print head that overlaps dots in both horizontal and vertical planes. It bi-directionally prints up to 150 dense, text quality characters per second.

The 560 also features a reliable cartridge ribbon that lasts up to four times as long as spool and cassette ribbons, separate heavy-duty stepper motors to drive the print head and advance the paper, plus true tractor feed.

```
presents a breakthrough in matrix printin
ering the user excellent print quality wit
ce of a matrix printer.  Employing a uniq
red column" head manufactured by Integr
 creates high quality printouts by overla
```

Paper Tiger 560 Print Sample

And famous Paper Tiger performance comes with every new 560. Like fixed or proportionately spaced text, programmable tabbing and business forms control, automatic text justification, print formats to 220 columns, parallel and serial interfaces, self-diagnostics, and more. All inside the most compact printer of its kind.

Need more stripes? Dotplot,™ our high-resolution raster graphics package, is standard on every 560.

For data processing, word processing and small business applications, this is your Tiger. The business-sized Paper Tiger™ 560.

It's a Tiger you can count on.

Call TOLL FREE 800-258-1386 (In New Hampshire, Alaska and Hawaii, call 603-673-9100.) Or write: Integral Data Systems, Inc., Milford, NH 03055.

Paper Tiger 560

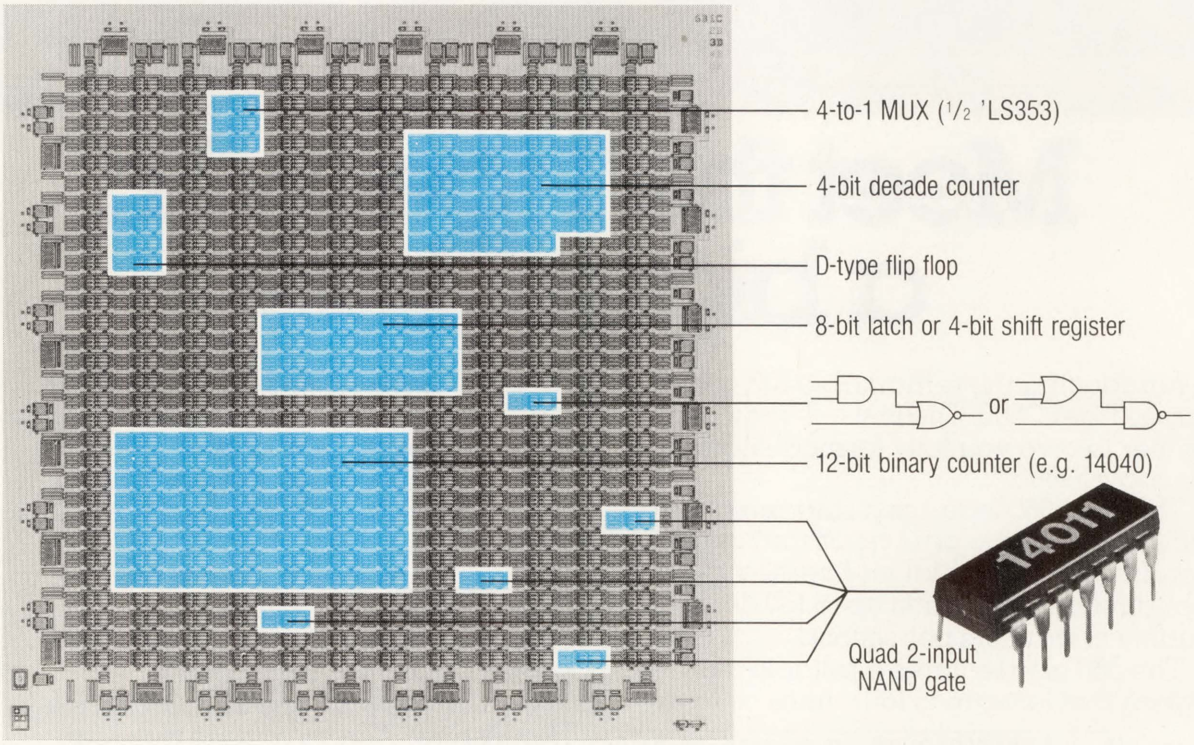
Integral Data Systems, Inc.

*Suggested single-unit U.S. price. Very generous OEM discounts available.

CIRCLE 104 ON INQUIRY CARD

The GarbageCollector

The little SystemChip™ for all the other stuff.



73% of the gates available left for your garbage logic.

Our small gate array chips let you compress all the miscellaneous logic garbage of your new system onto one circuit. We've got more than two dozen tried and true CMOS chips in our repertoire that give you high reliability, attractive pricing and your choice of packaging. And our in-house CAD gives you fast turnaround (how's five weeks sound?).

So if you've got the big system functions handled already with standard parts, you can leapfrog your competition with gate arrays as small as 50 gates or as big as 2240 or more. Put us to work. Send us your logic diagram for a quick confidential quote. We'll be happy to help you take out the garbage.

INTERNATIONAL
MICROCIRCUITS
INCORPORATED
Gate Array Leadership

3350 Scott Blvd., Santa Clara, CA 95051
Tel: (408) 727-2280, TWX: 910-338-2032

Now, Racal-Vadic has invisible dual and triple modems.

They're packaged inside TEXAS INSTRUMENTS' *Silent 700** 780 Series Data Terminals.

In the beginning...

When Texas Instruments designed the 780 Series of 120 character-per-second data terminals, Racal-Vadic was asked to solve a difficult engineering and packaging problem.

The requirement was for modems on a PC card that would operate full duplex at both 1200 & 300 bps; be compatible with Racal-Vadic's VA3400 and Bell 212A & 103 type modems; operate as a direct-connect modem or as an acoustic coupler; yet be small enough to fit inside TI's portable data terminals. An incredibly tough problem. But Racal-Vadic solved it.

Today...

Texas Instruments' Model 785 Portable Data Terminal includes a micro-processor controlled DUAL originate-only, acoustically coupled modem that operates at 1200 & 300 bps full duplex, and is compatible with Racal-Vadic's VA3400 & Bell's 103.

The modem for the TI Model 787 Portable Communications Data Terminal presented an even tougher challenge. The result is a full originate/answer TRIPLE modem that is direct-connect to the switched network (with an acoustic coupler option), and is compatible with Bell's 212A, 103, and Racal-Vadic's 3400 Series.

A truly universal modem packaged on a single PC board.

We did it for TI, and we can do it for you. Call or write us today.

Racal-Vadic Member IDCMA

RACAL
The Electronics Group

222 Caspian Drive
Sunnyvale, CA 94086
Tel: (408) 744-0810 • TWX: 910-339-9297

PHONE: (800) 543-3000, OPERATOR 507

Racal-Vadic Regional Offices: West: (408) 744-0810
East: (301) 459-7430 • **Central:** (312) 932-9268
Northeast: (617) 245-8790 • **Southwest:** (817) 277-2246

*Trademark of Texas Instruments

CIRCLE 106 ON INQUIRY CARD

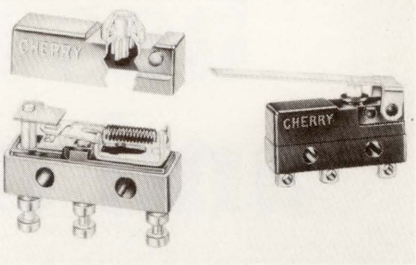
CIRCUIT COMPONENTS

T-1¾, T-1 LED LAMPS

LED 5665 and LED 3665 use a GaAsP chip encapsulated in a rugged, red diffused, epoxy dome. The 5665 has two 0.7" (1.7-cm) long leads that are typically 0.02" (0.05-cm) thick in a 5-mm T-1¾ package size. The 3665 has 0.02" thick leads that are 0.5" (1.25-cm) long in a 3-mm T-1 configuration. Visual light emission is in the 665-nm range, and typ luminous intensity is 0.7 mcd at 20-mA forward current (1.6-V forward voltage). **Opcoa Div, Refac Electronics Corp,** 330 Talmadge Rd, Edison, NJ 08817.

Circle 209 on Inquiry Card

SOLID BASE SUBMINIATURE SWITCHES



Series E91 switches are rated 5 A, 125/250 Vac; series E92 at 11 A, 0.25 hp, 125/250 Vac; and series E93 with gold crosspoint contacts are rated 0.1 A, 125 Vac. Insert molded terminals are available in single- or double-turret, solder/cross drilled, and 0.058" (0.147-cm) QC pin. Std actuators include external lever, roller, and simulated rollers. Two pivot positions are offered for std and high ratio operating forces. Sealed version features actuator button construction with elastomer boot moisture protection. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.

Circle 210 on Inquiry Card

SYNCHRONOUS LINE DRIVER

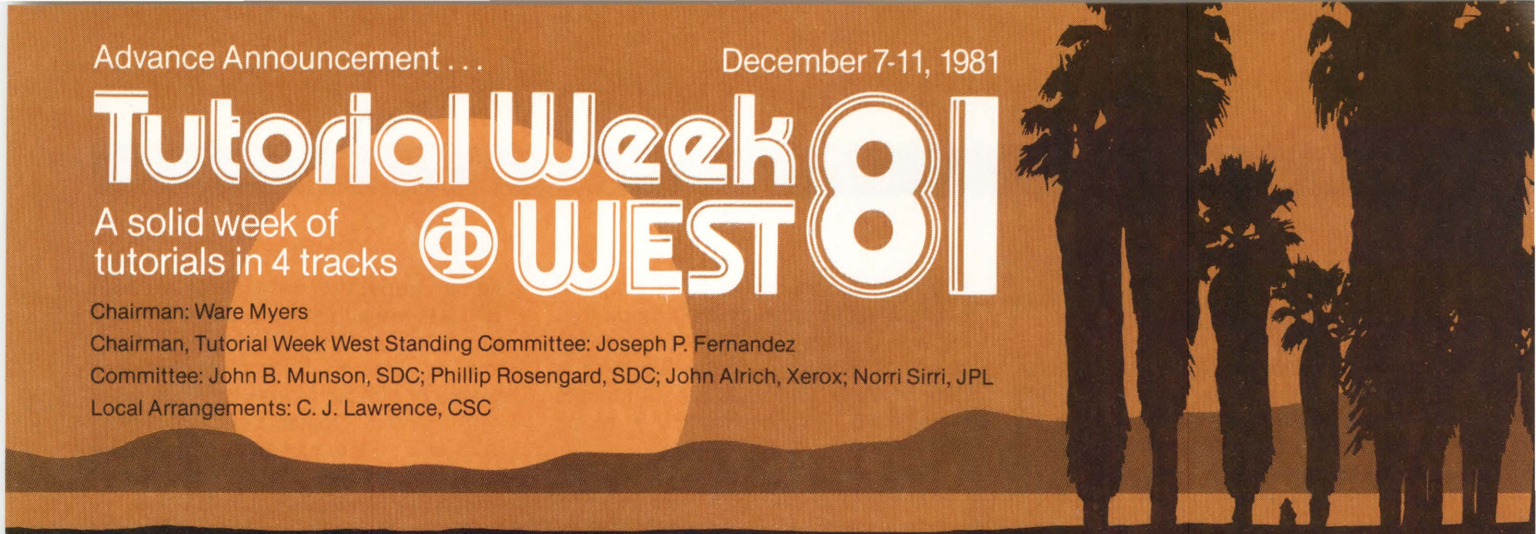
SLD-1 provides reliable data transmission over unloaded twisted pair at rates up to 19.2k bits/s. The driver can operate in a multipoint environment. An internal crystal control oscillator controls clock rates and a scrambler, which guarantees long term stability over the transmission link. The unit comes in both rackmount and standalone versions, and provides complete diagnostics, including status indicators. **Tri-Communications Industries, Inc,** 20 Fitch St, East Norwalk, CT 06885.

Circle 211 on Inquiry Card

LED INDICATOR LIGHTS

555 series includes 1- and 4-element arrays of green and yellow LEDs to complement the red units in the line. Green and yellow single-unit and QUAD-LEDs are available either with integral current-limiting resistors for 5-V, 6-mA operation, or without. Packages allow positive seating to the PCB surface, facilitating mounting and wave-soldering operations. Units are stackable with elements and leads on 0.100" (0.254-cm) centers. Additional design features include TTL compatibility and vibration and shock resistance. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.

Circle 212 on Inquiry Card



Advance Announcement . . .

December 7-11, 1981

Tutorial Week WEST 81

A solid week of tutorials in 4 tracks

Chairman: Ware Myers

Chairman, Tutorial Week West Standing Committee: Joseph P. Fernandez

Committee: John B. Munson, SDC; Phillip Rosengard, SDC; John Alrich, Xerox; Norri Sirri, JPL

Local Arrangements: C. J. Lawrence, CSC

Attendance limited to 100 per tutorial. Advance registration only: deadline — November 16, 1981.

MONDAY, 12/7	TUESDAY, 12/8	WEDNESDAY, 12/9	THURSDAY, 12/10	FRIDAY, 12/11
① **Introduction to Communication Architecture** Kenneth J. Thurber	② **A Pragmatic View of Distributed Processing Systems** Kenneth J. Thurber	③ **Office Automation Systems** Kenneth J. Thurber	④ **Local Computer Networks** Harvey A. Freeman	⑤ **Microcomputer Networks** Harvey A. Freeman
⑥ **Requirements Analysis and Definition** Peter Freeman Anthony I. Wasserman	⑦ **Software Design Techniques** Peter Freeman Anthony I. Wasserman	⑧ **Systematic Construction Techniques** Peter Freeman Anthony I. Wasserman	⑨ **Software Quality Assurance and Maintenance I** Edward F. Miller	⑩ **Software Quality Assurance and Maintenance II** Edward F. Miller
⑪ **Software Management I** Donald J. Reifer	⑫ **Software Management II** Donald J. Reifer	⑬ **Software Cost Estimating and Life Cycle Control I** Lawrence H. Putnam	⑭ **Software Cost Estimating and Life Cycle Control II** Lawrence H. Putnam	⑮ **Software Configuration Management** Stan Siegel
⑯ **Approaches to Algorithmic VLSI Design I** Ted Kehl	⑰ **Approaches to Algorithmic VLSI Design II** Ted Kehl	⑱ **Approaches to Algorithmic VLSI Design III** Ted Kehl	⑲ **VLSI from a User's Perspective** Rex Rice	⑳ **Custom Design of VLSI** Gary Kelson Bert White

Plus a special 3-part course for novices (Half-day sessions)

㉑ **An Intelligent Layman's Guide to Computers**
(includes three luncheons)
Ware Myers

Hotel del Coronado
San Diego, California

Register NOW!

Select up to one tutorial per individual per day.

FEES:	Per Tutorial	All Week
Members	$95	$425
Nonmembers	$110	$500

Includes bound tutorial text and luncheon. There will be a no-host reception Monday night.

Intelligent Layman's Guide — $50

HOTEL ACCOMMODATIONS: Reserve your room now. Write to:

Hotel del Coronado
Coronado, CA 92118
Attn.: IEEE Tutorial Week

RATES: Single or Double (main bldg.): $51.75
(new complex): $65.25
Lanai: $71.25

Mail to: Tutorial Week West 81, Box 639, Silver Spring, MD 20901

☐ I am interested in the following tutorials (please circle numbers):
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
Please mail me the complete program announcement.

☐ I want to register right now. Enclosed is $__________ to reserve space at the following tutorials (circle numbers as appropriate):
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21

☐ Check enclosed ☐ VISA/BankAmericard ☐ Master Charge

Card No.__________ Exp. Date______ Signature__________

Name__________ IEEE or IEEE-CS Membership No.__________

Street Address__________

City/State/Zip__________

IEEE COMPUTER SOCIETY

CIRCLE 108 ON INQUIRY CARD

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

CIRCUIT COMPONENTS

HIGH SPEED DATA DRIVER MODULE

Model 310 can transmit digital data through coaxial cable, parallel or 50-Ω source terminated, with minimum over/undershoot and aberrations. It incorporates an output inhibit mode that allows 3-state configuration when bused together with the input to a data receiver. Output is programmable over ±15-V range for 30-V pk-pk signal. Repetition rates greater than 10 MHz are achievable, depending on amplitude, with pulse widths as narrow as 20 ns. Switching time for enable or disable modes is 15 ns max, with inhibit spikes of less than 500 mV. **Versatile Integrated Modules,** 1283-A Mountain View-Alviso Rd, Sunnyvale, CA 94086.

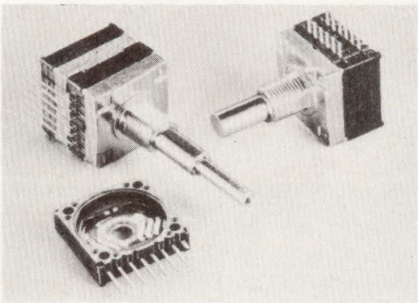
Circle 213 on Inquiry Card

HIGH RESOLUTION SLOTTED OPTICAL SWITCH

OPB820 series switches contain GaAs IR emitting LED and planar silicon phototransistor in 0.6 x 0.24 x 0.275" (1.5 x 0.61 x 0.699-cm) housing with slot width of 0.07" (0.18 cm). OPB820S10, OPB820S7, and OPB820S5 have apertures of 0.010, 0.007, and 0.005" (0.025, 0.018, and 0.013 cm) wide by 0.04" (0.10 cm) high, respectively. Min photocurrent for OPB820, OPB820S10, OPB820S7, and OPB820S5 at V_{CE} = 5 V and I_F = 20 mA are 500, 400, 300, and 170 μA, respectively. Max dark current is 100 nA at V_{CE} = 10 V. **TRW Optron, Div of TRW, Inc,** 1201 Tappan Cir, Carrollton, TX 75006.

Circle 214 on Inquiry Card

SEALED ROTARY SWITCHES

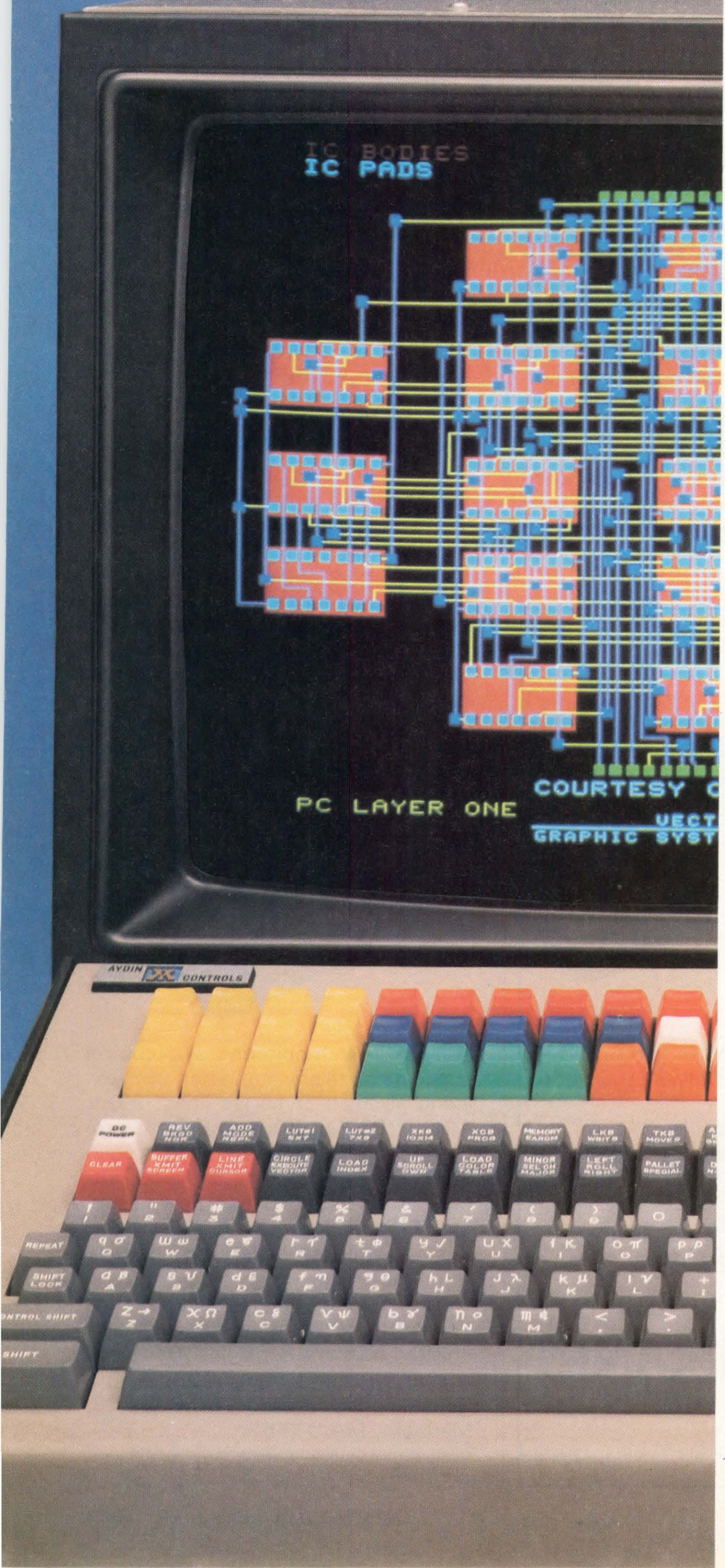


Measuring 0.85 x 0.85" (2.16 x 2.16 cm), series 850 is available with up to 28 positions, 4 sections, and 7 outputs plus common per section. Both std and special coded outputs are available, and mounting can be parallel or perpendicular to PC board. Rating is 250 mA at 28 Vdc max (resistive load at ambient temp). Op temp is −25 to 85 °C; vibration resistance is 10 G, 10 to 500 Hz; and shock resistance is 50 G. Available coding includes BCD, hexadecimal, and Grey. **Oak Switch Systems, Inc,** PO Box 517, Crystal Lake, IL 60014.

Circle 215 on Inquiry Card

Quickens Your Draw

Aydin user-oriented, full-color graphic systems let you tackle complex design and processing projects quickly and easily.



Aydin 5216 high-resolution multiprocessor-based color graphic systems lead the industry in fulfilling the needs of intricate process control CAD/CAM, simulation, C^3I, image processing and many other sophisticated applications.

Versatility is the result of the Aydin growing family of hardware and 2D, 3D, imaging and CORE software modules. The 5216 gives you both the flexibility and programmability to design and implement your ideas efficiently and economically; a true man-machine interface. For example, AYGRAF instruction sets provide both standalone and distributed processing capabilities to support 2D graphics in a standardized manner. The 3D system, which supports standalone and host-driven applications, is designed to give the user the full benefit of sophisticated graphics, all with interactive control that doesn't burden the host computer.

Aydin modular design also means that you can customize the 5216 to your strictest requirements, easily expand memories, add storage and utilize various user-programmable lookup tables. In addition, a host of interactive devices are available, including joysticks, trackballs, graphic tablets, touch panels and lighted or non-lighted function keys.

It all adds up to a user-oriented 5216 color system that is a reliable, flexible and economical solution to your graphics and image processing needs. Quicken your draw with Aydin, the industry leader in high-resolution, intelligent color graphics. For more information, contact Aydin Controls, 414 Commerce Drive, Fort Washington, PA 19034. Tel.: 215-542-7800. (TWX: 510-661-0518.)

Leadership Features:

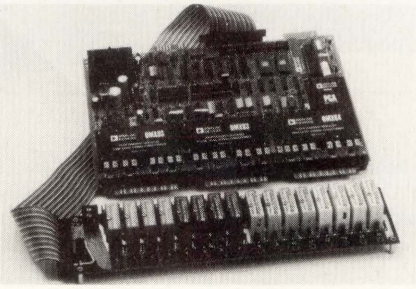
• High-performance multiprocessor bus architecture • Pixel or graphic DMA block mode data transfer (800 nanoseconds per 16-bit pixel) • Multiple pixels per word • Wide selection of display formats up to 1024 x 1024 x 16 • Video processing through lookup table RAM at bit rates to over 40mHz • High-speed hardware vector and character generation • Four sizes of alpha characters • High-speed hardware math • Both parallel and serial peripheral interfaces available • User programmable • 16-Bit microprocessor.

AYDIN CONTROLS

CIRCLE 110 ON INQUIRY CARD

DATA ACQUISITION AND CONTROL

DIGITAL I/O SUBSYSTEM



The 16-channel μMAC 4020 interfaces with μMAC-4000, a single-board measurement and control system, serving as a manifold that provides 8 input and 8 output channels. Users select the mix to suit the application. Modules convert high level ac/dc I/Os to TTL levels. Each module provides screw terminals for easy connection, optical isolation to 2500 Vac rms, individual plug-in fuses for high voltage surge and short circuit protection, and LED status light. Ac modules incorporate zero voltage switching to reduce emi and built-in RC snubbers to eliminate line voltage spikes. They can sense or switch ac voltages of 90 to 140 V or 180 to 280 V, and have 3-A current rating. Dc modules include contact debounce circuitry to provide clean switching. Dc signals can be 60 V on the output and 10 to 32 V on the input. **Analog Devices, Inc,** Rte 1 Industrial Park, Norwood, MA 02062.
Circle 216 on Inquiry Card

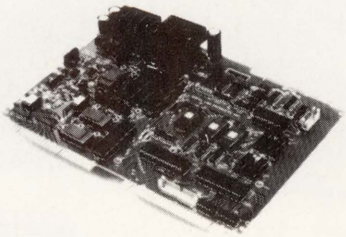
DATA ACQUISITION AND CONTROL SYSTEM

ICIS 850 is a compact modular microcomputer based system designed to gather, process, and record analog, digital, frequency, and event counter data in real time. The ICCS operating system has 2 timeshared partitions that operate simultaneously. User programs are written in an extended version of BASIC that includes data acquisition commands. The unit hosts a 26-slot card cage to interface each circuit card to a common bus. Dual 5.25" (13.34-cm minidisc drives are used for storage of programs and data. **Western Telecomputing Corp,** 202 E Kagy Blvd, Bozeman, MT 59715.
Circle 217 on Inquiry Card

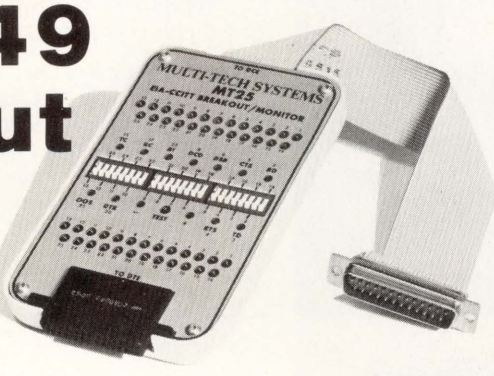
MICROCOMPUTER BASED DATA LOGGER

Model DL-901 measures and prints out analog voltage values in ±5-, ±10-, 0- to 10-, or 0- to 20-V range with 12-bit accuracy equivalent to 0.025%. It accumulates events in 16 individual counting channels and prints results in preset time intervals or upon demand; counting speed is 100 pulses/s. Unit functions as multichannel stopwatch/timer, accumulating time in 16 registers monitoring 16 inputs; accuracy is 4 ms in each channel. Data logger can also be used as printing event counter/timer or 16-channel printing digital voltmeter. **Columbus Instruments, International Corp,** 950 N Hague Ave, Columbus, OH 43204.
Circle 218 on Inquiry Card

ANALOG/DIGITAL I/O MODULE



SL-800M links monitoring and control applications to any computer using existing RS-232-C or RS-423 lines. 9.0 x 12.0" (22.9 x 30.5-cm) board provides 8 analog inputs (12-bit resolution), 8 digital inputs, 8 digital outputs, and 115/230-Vac power supply. Two analog outputs, differential analog inputs, interface panels, removable I/O connectors, power cable, and mounting hardware are optional. Up to 96 units can be daisy chained on same serial line. Baud rate is user selectable from 300 to 9600. **Serial Lab Products Inc,** PO Box 766, Marlboro, MA 01752.
Circle 219 on Inquiry Card



TECKNIT solves the toughest design and packaging EMI noise problems.

EFFECTIVELY. ECONOMICALLY.

#1 in EMI Shielding

- Knitted Wire Mesh
- Oriented Wire Gaskets
- Conductive Elastomers
- Shielding Optical Windows
- Shielding Air-Vent Panels
- Conductive Adhesives and Sealants
- Switch and Connector Seals

data guide:
a comprehensive source of Tecknit EMI shielding products

A. wire mesh

B. metal screen

C. oriented wire

TECKNIT

Write or Call for
the TECKNIT Data Guide
or
to discuss an
EMI shielding problem.

TECKNIT®

EMI Shielding Products
129 Dermody Street, Cranford, NJ 07016
(201) 272-5500

TWX (710) 996-5951
TELEX 685-3079TCKNT

CIRCLE 138 ON INQUIRY CARD

HOW FAST DO YOU WANT TO HIT THE STREET WITH YOUR MICRO SYSTEM?

During these last two years, thousands of companies have gone into business with the sole purpose of developing micro-based products.

And in an environment as explosive as that, you are either very quick. Or very dead.

So, although building your micro-based system from scratch could be a glorious experience, we would advise you to buy one of our single board computers. Or even better, our prepackaged systems.

If you call your local Data General industrial electronics stocking distributor* to order your development system this morning, you'll be able to start working on your software this afternoon.

And while your competition is pounding out assembly code, you'll be working with big computer languages. An MP/FORTRAN with multi-tasking. An MP/PASCAL that executes at assembly language speeds. An MP/BASIC that lets you write enormously complex programs that take up very little space. And MP/OS. A micro sub-set of AOS, the operating system anyone who knows operating systems will tell you is the most sophisticated in the world.

With system tools as powerful as these, you could be out selling your micro-based product while other guys are still trying to figure out how to use the wimpy tools that the semiconductor companies are offering.

And as you get bigger, and get into bigger systems, everything you've done will grow right along with you. Because Data General micros are compatible with every other Data General computer.

If you are still unconvinced, let us tell you a story.

A certain system house we know assigned two teams the same micro project using two different computer companies. The team using Data General finished in four months. The team not using Data General took nearly seven months.

Would you care to guess whose micros they are using now?

Data General
We take care of our own.

*SCHWEBER, HALL-MARK, KIERULLF, ALMAC/STROUM, R.A.E. in Canada.

CIRCLE 142 ON INQUIRY CARD

The EZ-PRO Development System

AA-591
Dual Disk

AA-570
Basic Development
Unit

AA-580 Interface Module equipped with eight AA-582 Memory Modules — used with bit slice systems.

THE EZ-PRO SYSTEM FEATURES:

Fixed Word Length Processors

- EZ-PRO supports a bunch and the bunch is getting bigger fast. Right now it's the 2650, 8X300, Z80, Z8001/2, 6800, 6802/8, 6805/146805, 6809, 68000, 6502/12, 6503-15 family, 3870/2/4/6, 8080, 8021, 8085, 8048 family. All are supported with real time in-circuit emulators.
- Emulators — Master/Slave type — Every resource in each slave is available to the user system including all interrupts and stack pointers.
- Trace and Logic Analyzer capabilities of course.
- EPROM Programmer, 2716/32. Adaptor for 8748.
- Complete Software Support — Each emulator is provided with a Relocating Macroassembler, Linking Editor, Debugger and a DEMO program to show how the software is used. Higher level languages available include PASCAL and STRUBAL.

Bit Slice Processors

- EZ-PRO supports them all — You name it — 2, 4 or 8 bits wide — ECL or TTL.
- Microprogram word widths from 16 to 128 bits — Depths to 8K words.
- Bipolar PROM Programmers — ECL or TTL — 4 and 8 bit wide PROMs — intermixed if you like — Fast enough for production — Gang program 8 PROMS at a time with a single programmer.
- Complete Software Support — You'll have to experience it to believe the power and ease of use of AABASM, our Meta Assembler — And the rest of the software has the same standard of excellence.

The Basic EZ-PRO System

- 32 KB of static memory, expandable to 80 KB.
- Two RS-232 ports with selectable baud rates — one for a high speed printer and the other for a video terminal — Current loop port also provided.
- Choice of floppy disk capacities.
- Software provided for use on all systems includes a Resident Monitor, Disk Operating System, Disk Formatter and an Editor.

Prices

A complete EZ-PRO system equipped with one in-circuit emulator, dual disk unit, printer and video terminal sells for about $8,500. Bit Slice systems start at about $11,000.

What to do now that you're semi-sold . . .

Write or call us if you need more information. Then order a system at no risk. Advise us within 28 days of shipment from our plant that you don't want the system and return it to us in an undamaged condition within 35 days and we'll promptly return your money.

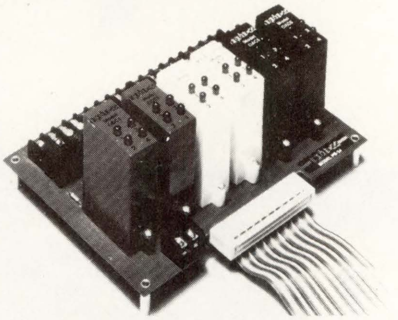
AMERICAN AUTOMATION

14731 Franklin Ave. • Tustin, California 92680 • (714) 731-1661 TWX 910-595-2670

CIRCLE 139 ON INQUIRY CARD

DATA ACQUISITION AND CONTROL

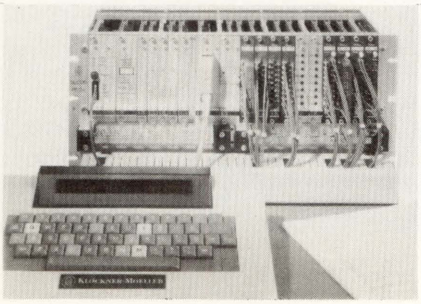
HIGH DENSITY INDUSTRIAL POWER I/O SYSTEM



High density system consists of universal mounting racks that accommodate plug-in Quad Paks, each containing ac input, ac output, dc input, and dc output circuits. LEDs on the module indicate operation status. Modules have 4-kV rms optical isolation to protect the microprocessor from transients and rfi. Logic signals are TTL compatible, having a 5-Vdc nom logic rating. Ac output module contains a snubber network to enhance performance when used with inductive loads; dc input module contains circuits to eliminate adverse effects of contact bounce. A direct replacement for std PB24 where space requirements are stringent, PB24Q accommodates 6 modules that provide 24 I/Os; PB32DEC provides a direct connection to LSI-11 via the DRV11J parallel line interface. Each rack handles up to 8 packs providing 32 points of I/O. Cable is available to provide a connection from DRV11J to PB32DEC; a second PB32DEC can be added to the DRV11J to provide total capability of 64 I/O points. **Opto 22**, 15461 Springdale St, Huntington Beach, CA 92649.

Circle 220 on Inquiry Card

PROGRAMMABLE CONTROLLERS



PS-24, a modular microprocessor based system that can be used standalone or as part of a network, is equipped with a 20-mA current loop/RS-232 data interface port that allows use with major computer systems or ASCII coded peripherals and interfaces. It is available with as many as 1024 inputs and 1024 outputs; outputs can double as inputs for flexibility. Programs can be created in user defined, program oriented, or mnemonic language, logic diagram, and/or standard ladder diagram format. The unit can cycle through 1k of EPROM or RAM in 1 ms; memory can be expanded up to 4k without affecting performance. Based on a std 19" (48-cm) rackmounted carrier frame, the system is available with a range of special function boards, as well as compact programmer, printer, cassette tape deck, and EPROM programmer. **Klockner-Moeller Corp,** 4 Strathmore Rd, Natick, MA 01760.

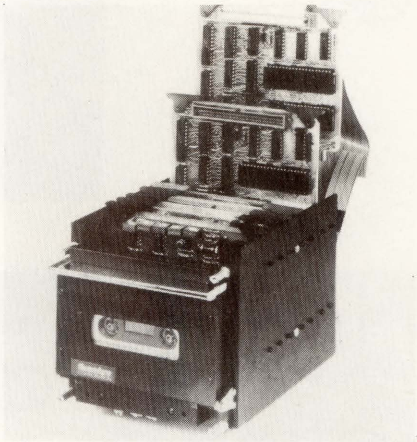
Circle 221 Inquiry Card

STANDALONE REMOTE SITE DATA LOGGER

An automatically charged battery within SABEL (standalone, battery energized logging) 81MC permits operation in the field or provides continued operation in case of power failure. Programming includes selection of channels for scanning, provides 2 simultaneous scan intervals, and permits channel by channel assignment of various signal conversion and linearization functions, and 2 alarm levels for each channel. Ax + b averaging programs are std. A 26-char display leads operators through programming sequence and permits display of data from any input point on command. Hardcopy records are produced with a printer. A built-in ECMA-34 cassette drive provides offline program and data storage. The basic system accommodates 50 input channels; each extension housing is capable of 190 inputs max. **Consolidated Controls Corp,** 15 Durant Ave, Bethel, CT 06801.

Circle 222 on Inquiry Card

DATA ACQUISITION/STORAGE SYSTEM



Based on the Z80 processor, M80/DAS samples up to 8 channels of analog data simultaneously; system uses 1 converter for each channel and multiplexes digitally to prevent degrading and skewing of data from analog multiplexing. Voltage inputs are differential with selectable ranges of ± 500 mV to ± 5 V. Common mode is rejected between ± 5 V, and input impedance is greater than 20 MΩ. Conversion is done by dual-slope technique, and resolution is 13 bits binary and includes overrange indication. **Memodyne Corp,** 220 Reservoir St, Needham Heights, MA 02194.

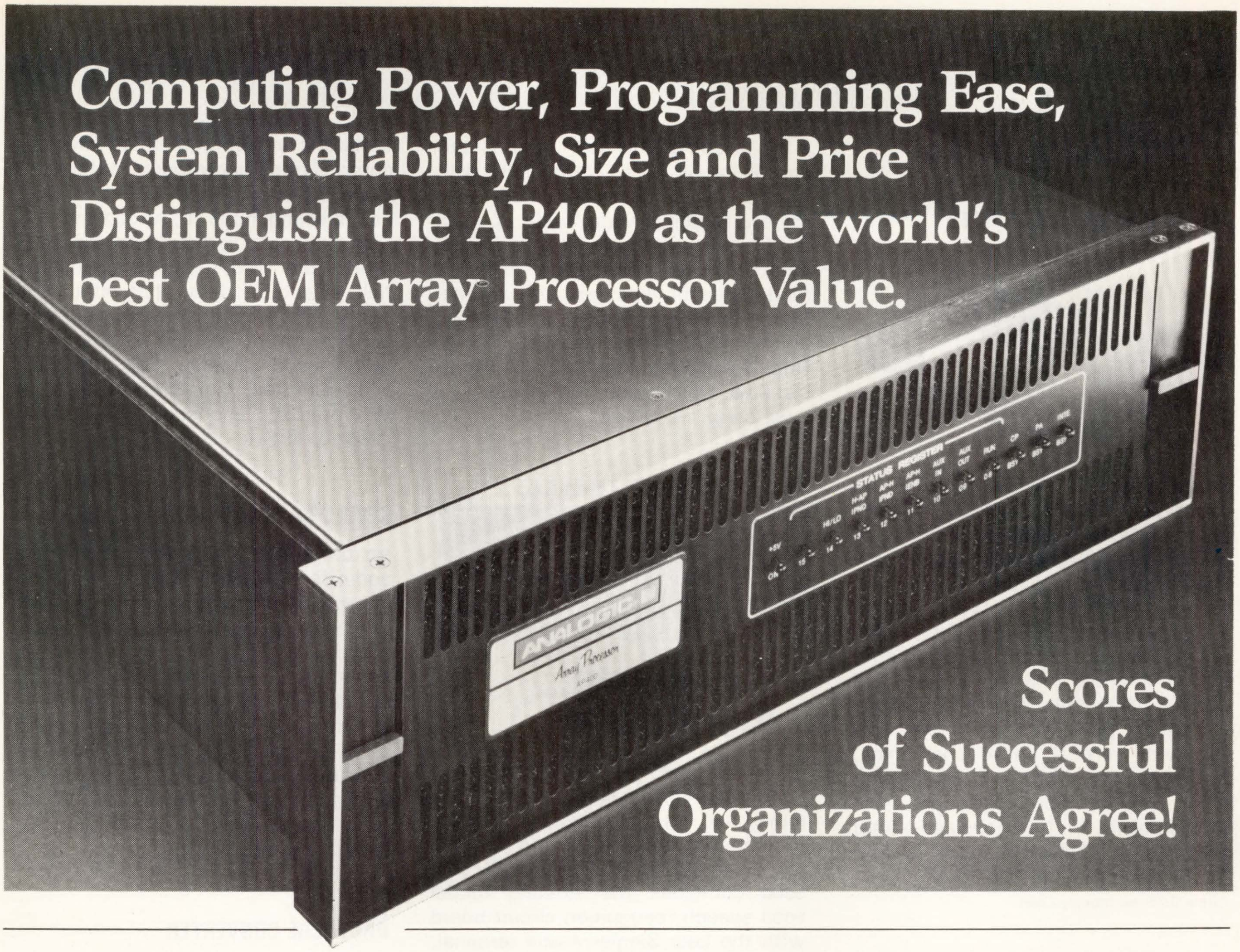
Circle 223 on Inquiry Card

PRINTERS/PLOTTERS

BIDIRECTIONAL SERIAL MATRIX PRINTER

Model 2350 produces subscripts, superscripts, and underscores, and features 2-color printing and a 5M-char head warranty. 136-col printer operates at speeds up to 350 chars/s and combines short line seeking logic and fast horizontal and vertical slew speeds to increase output. Features include 1k-byte input buffer, 96-char ASCII set, 2 condensed and 3 double-width fonts, and std Centronics- and Dataproducts-compatible parallel interfaces. RS-232-C and high speed parallel interfaces are also available. **Okidata Corp,** 111 Gaither Dr, Mt Laurel, NJ 08054.

Circle 224 on Inquiry Card



Computing Power, Programming Ease, System Reliability, Size and Price Distinguish the AP400 as the world's best OEM Array Processor Value.

Scores of Successful Organizations Agree!

Analogic began the design of the AP400 with the knowledge that OEM array processor users needed an order of magnitude more reliability, software maintainability and economy than anything available at that time. Now, less than two years since its introduction, system engineers, scientists and computer designers appreciate its performance and have designed-in over 500 AP400s in such diverse applications as ☐ X-Ray Tomography ☐ Ultrasonics ☐ Nuclear Magnetic Resonance ☐ Spectral Analysis ☐ Seismic Exploration ☐ Music Synthesis ☐ Digital Filtering ☐ Satellite Communications and more. Consider the advantages to the OEM.

You get just what you need

In its simplest form* the AP400 will tuck into your package, using your 5-volt power and your front panel. At the other extreme, the AP400 may incorporate 64K words of memory, and come as a complete, standalone, self-powered package. They can even be chained together to deliver total throughput equal to that of super computers — but at a fraction of the cost.

You pay far less for what you get!

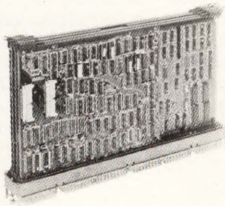
We know that OEMs are concerned with the total cost picture: initial price, costs of inventory, costs of software development and maintenance and costs of hardware maintenance.

In response to these concerns, the basic AP400 has been priced to reflect OEM quantity requirements. Software is inexpensive because we provide complete utility, application and system software and support in Host FORTRAN, Host Assembly and AP Assembly language...in standard or custom configurations. Further, the AP400 employs a familiar minicomputer-like hardware and software architecture and instruction set, similar to the host computer you're probably using now!

In addition, the AP400's straightforward system architecture and comprehensive diagnostics enhance reliability and simplify maintenance procedures. Analogic's sophisticated engineering design and reliability minimizes hardware maintenance cost.

The AP400 has a long product life expectancy

Continual development of a family of software-compatible machines ensures that all systems using the AP400 will keep their competitive edge for years to come.



**In its simplest configuration the AP400 is composed of 4-PC cards. It measures only 15½ x 10 x 2¼ inches.*

Technical information is available

Write for our comprehensive AP400 information package which includes a product selection guide, and a description of our technical services. Should you feel that a design conference would be helpful, tell us about your needs and we'll assemble a group of system architects, engineers and scientists to help you with your program. Analogic staff members are experienced professionals in meeting special customer needs such as inventory scheduling, special packaging and service arrangements.

Summary Specifications

- 10 million arithmetic computations per second
- 1024 point real FFT — 3.6msec, complex FFT — 7.4msec.
- Standard memory: 4K by 24-bit bipolar RAM
- Expandable 64K words in increments of 4K
- Power Requirements: 4-card set — 5Vdc @ 20A nominal; complete system with line-separated power supply — 117Vac or 240Vac, 50/60Hz, 130W nominal.
- 24-bit auxiliary input and output ports, standard

ANALOGIC®

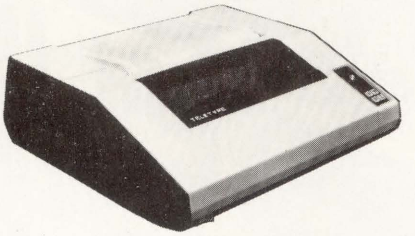
Solutions...not Slogans

ANALOGIC CORPORATION ☐ Audubon Road ☐ Wakefield, MA 01880 ☐ Tel. (617) 246-0300 ☐ TWX (710) 348-0425 ☐ Telex 94-9307

CIRCLE 140 ON INQUIRY CARD

PRINTERS/PLOTTERS

340 CHAR/s MATRIX PRINTER

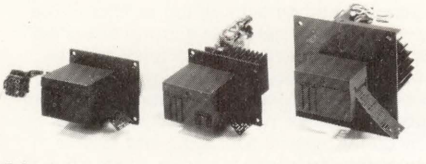


AP200 printer delivers printout on forms up to 6-ply. Operator replaceable printhead has life expectancy of 300M char. Adjustable tractors accommodate forms from 3.0 to 16.0" (7.6 to 40.6 cm) wide and 3.0 to 14.0" (7.6 to 35.6 cm) long. Max printing line is 132 char at 10 char/in (3.9/cm), and a 218-char line at 16.7 char/in (6.6/cm). Features include form feed, perforation skip over, soft roll with vertical paper positioning, fast slew rate, front or bottom paper load, snap-in ribbon cartridges, and status display for functions and printer diagnostics. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60077.

Circle 225 on Inquiry Card

INPUT/OUTPUT DEVICES

PUNCH TAPE READERS



Models R-30, R-150, and R-300 have speeds of 30, 150, and 300 chars/s, respectively. High current/high level output option on R-150 permits driving of any 5-V logic family hardware. R-150 is compatible with Addmaster, and R-300 is plug compatible with Decitek model 262. All feature solid state LED light source, wide opening read heads, self-cleaning tape heads, stepper motor drives, and ability to read tapes of all types and widths. Signal levels are TTL/DTL compatible, and MTBF for all models is 10,000 h. **Data Specialties, Inc,** 3455 Commercial Ave, Northbrook, IL 60062.

Circle 226 on Inquiry Card

VOICE DATA INPUT TERMINAL

Fully integrated voice data input terminal has an expanded vocabulary feature that doubles the std vocabulary from 64 to 128 words. Model 5300 combines the existing model 5000 speech recognition circuit board with the Lear Siegler ADM-5 terminal, offering availability of voice data input, without replacing keyboard entry. The terminal can accept either keyboard or voice input, or both simultaneously. **Heuristics, Inc,** 1285 Hammerwood Ave, Sunnyvale, CA 94086.

Circle 227 on Inquiry Card

DATA COMMUNICATIONS

BCD TO ASCII INTERFACE

Q-1008 modular interface automatically handles BCD to ASCII data transfers; a preprogrammed memory controls transfer protocol. Features include 32 bits of input (8 BCD digits); handshaking input bit; RS-232 and current loop output; field selected baud rates from 110 to 9600 baud; and field selectable data, start, stop, and parity bits. In std program supplied, carriage return and line feed are sent before each complete digit sequence is transmitted. **Quasitronics, Inc,** 19 W Water St, Canonsburg, PA 15317.

Circle 228 on Inquiry Card

KEYBOARD/AUTODIALING MODEMS

MD103J series is Bell 103J compatible and offers originate, auto-answer, and internal Direct Access Arrangement. The 300 PLUS (MD103J-3) offers network addressing capability with features that include keyboard dialing, autodialing of numbers stored in dynamic memory, repeat dialing, and camp-on dialing. Both models are available in standalone and rackmount versions. **Ven-Tel, Inc,** 2390 Walsh Ave, Santa Clara, CA 95051.

Circle 229 on Inquiry Card

PROTOCOL CONVERTER

CS-85 enables users to connect terminals with the RS-232 interface, both specialized and CRT, into networks using complex protocols, and allows communications between networks or computers using different protocols. The processor consists of a single-board microprocessor controller and a power supply, packaged in a standalone enclosure. The board is also available unpackaged. The basic unit has one DTE and one DCE port. An expander adds 4 additional DCE ports. **Sigma Systems, Inc,** 7221 NW 11th Pl, Plantation, FL 33313.

Circle 230 on Inquiry Card

COMPARE SMARTS.

Feature-for-feature our smart CRT terminals cost less than *their* dumb ones. Much less. Compare smarts. Then compare price. You'll pick TeleVideo.

Four different models to choose from. Each with features you'd expect to pay extra for. But with TeleVideo, they're standard.

We put a lot of engineering savvy into our CRTs. Their modular design means high reliability. It also lets us build in high volume. And sell to you at low prices.

Find out how you can make your next CRT buy a smart one. Contact TeleVideo today for information.

Nationwide Field Service is available from General Electric Co., Instrumentation and Communication Equipment Service shops.

TeleVideo®

TeleVideo Systems, Inc., 1170 Morse Avenue
Sunnyvale, California 94086
408/745-7760, 800/538-8725 (toll free outside CA).
TWX 910 338 7633

Model 920C shown.

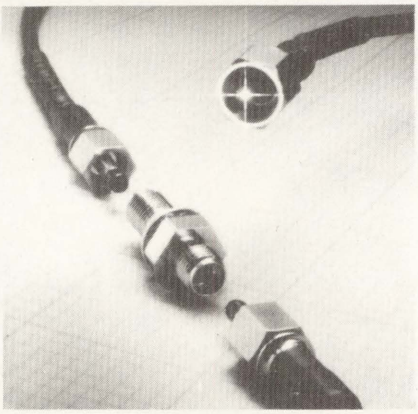
COMPARE PRICE.

CALIFORNIA Santa Ana (714) 557-6095 • Sunnyvale (408) 745-7760 • MASSACHUSETTS Boston (617) 668-6891
NEW YORK/NEW JERSEY Morris Plains (201) 267-8805 • TEXAS Dallas (214) 980-9978

CIRCLE 119 ON INQUIRY CARD

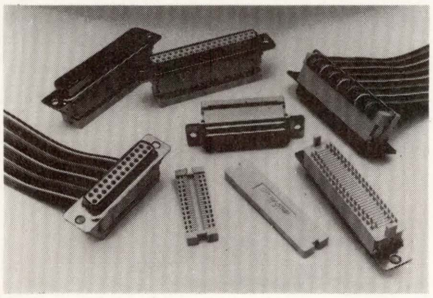
PACKAGING AND INTERCONNECTION

FIBER OPTIC CONNECTORS



Connectors accept single fibers as small as 125 μm and fiber bundles as large as 1140 μm with cable diameters from 2.3 to 4.9 mm, conform to proposed NATO and IEC standards for military and instrument applications, and are intermatable with existing SMA type connectors. Internal ferrule ensures axial alignment of fibers within 0.01°, and proprietary resilient tip provides accurate fiber to fiber centering without accessories. **AMP Inc,** Harrisburg, PA 17105.
Circle 231 on Inquiry Card

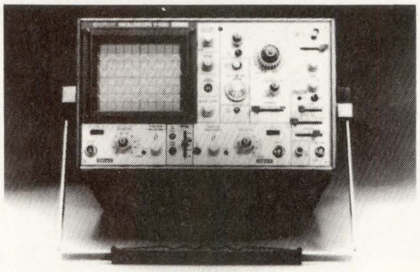
D-SUBMINIATURE CONNECTORS



817 series 25- and 37-pin and socket connector allows easy mass termination, providing an internal transition from std 0.054" (0.137-cm) connector contact spacing to std 0.050" (0.127-cm) flat ribbon cable spacing. Reliability is enhanced by double-slot insulation displacement design that provides gas-tight junction with each connector at 4 places. Units are packaged in metal shell and accept 28 and 26 AWG stranded conductors and 28 AWG solid conductors. **Spectra-Strip,** 7100 Lampson Ave, Garden Grove, CA 92642.
Circle 232 on Inquiry Card

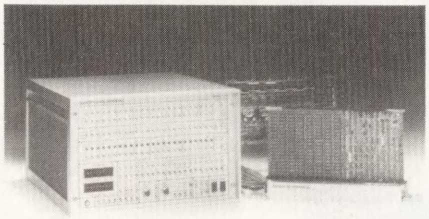
TEST AND MEASUREMENT

QUAD-TRACE, 100-MHz OSCILLOSCOPE



V-1050 features sensitivity of 500 μV/div (5 MHz), and 4-channel capacity that permits simultaneous display of 4 signals; a total of 8 traces can be seen with operation of alternate timebase feature. Frequency response of channel 1 and channel 2 vertical amplifiers is dc to at least 100 MHz (−3 dB) and rise time is 3.5 ns or less; frequency response of channels 3 and 4 is dc to 70 MHz (−3 dB). Accuracy is ±2% or less, without magnifier, and ±4% or less, with magnifier. **Hitachi Denshi America, Ltd,** 175 Crossways Park W, Woodbury, NY 11797.
Circle 333 on Inquiry Card

BENCHTOP RAM TEST SYSTEM



T-119 provides high speed testing for production and incoming inspection as well as design development assistance for semiconductor and core memory systems. A standalone system that includes performance board, test fixture, and required power supplies, unit automatically sequences 4 semiconductor test patterns and 5 industry std core test patterns for memory configurations up to 16M words x 24 bits. Plug-in performance boards enable the unit to test 15 different memory types. Features include selectable initial and ending address, manual or automatically sequenced voltage margining on the memory under test, cabling to the test fixture to allow burn-in chamber testing, error lamps and alarm, and variable cycle time clock and error strobe. The unit provides 24-bit address capability, and 24-bit data capacity. **Concept Development, Inc,** 3198 G Airport Loop Dr, Costa Mesa, CA 92626. Circle 234 on Inquiry Card

SUBASSEMBLIES

SINGLE-CHIP TTL FIBER OPTIC RECEIVER

MFOD624F, in a std 3-lead ferrule package, detects and converts optical input levels to logic level outputs through data rates up to 500k bits/s. The unit is compatible with plastic or glass cables, has a wide bandwidth, and is designed for use over short to intermediate distances. Its high (20-μW) sensitivity and rfi/emi rejection via compatible metal connector make it useful in industrial control systems. Optical port is 200-μm glass core with 0.7 NA. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 235 on Inquiry Card

PRINTER CONTROLLER

Series 5287 interfaces industry std non-IBM compatible printers to IBM 3270-type controllers, and provides both serial (RS-232) and Centronics-type parallel interfaces. Low profile enclosure contains logic circuitry and power supply and provides complete front panel control. The units support std ASCII interfaces as printer ports, including RS-232-C to 19.2k-baud serial with specifiable protocol, std Centronics parallel, and Diablo HyType II printer (1355HS, 1355WP). Throughput character rate for parallel interfacing is limited to printer being used. The controller connects to IBM 3274 or 2376 through a std IBM coax, providing users with 3440-char buffer, EBCDIC or logical unit 1 codes, and SCS (SNA) support. **Agile Corp,** 1050 Stewart Dr, Sunnyvale, CA 94086.
Circle 236 on Inquiry Card

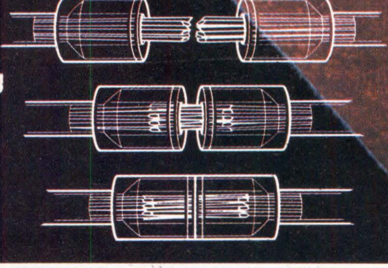
The state-of-the-art in PC design...

Bendix Low Mating Force Brush Connectors

Low mating force, bristle brush connectors by Bendix! They've advanced PC design to a new state-of-the-art!

A connector that's *dependable* (stable contact resistance), *durable* (up to 20,000 mates/unmates), *flexible* (20 - 400 contacts per connector), and *smooth* (mating force reduced by 70 - 90%)!

The brush "wiping" action of gold-plated wire bristles, meshing at highly redundant contact sites, creates multiple electrical paths, and intimate, gas-tight connection.



A masterpiece of simplicity. Available in a broad variety of connector/termination formats.

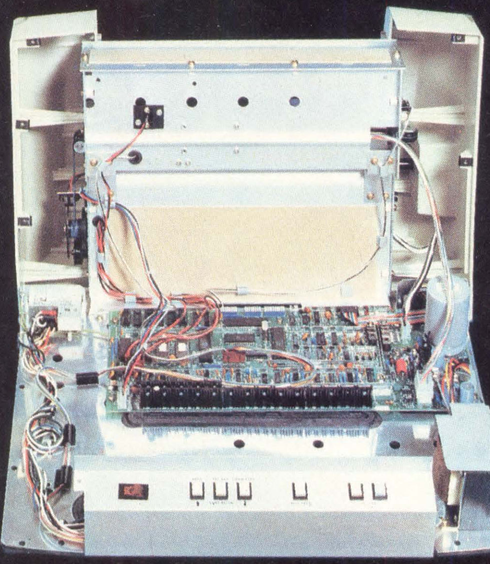
- compatible with High Speed Digital Switching
- greater board effectiveness by allowing more circuits per board
- stable electrical performance
- less need for exterior board supports
- no need for secondary activation procedures, typically required for zero-insertion force connection

That's the "broad brush" picture on our brush connectors. Get all the fine details in our new brochure, *LOW MATING FORCE*. Call 607 563-5302, or write The Bendix Corporation, Electrical Components Division, Sidney, New York 13838.

We speak connectors. Bendix

CIRCLE 112 ON INQUIRY CARD

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clamshell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

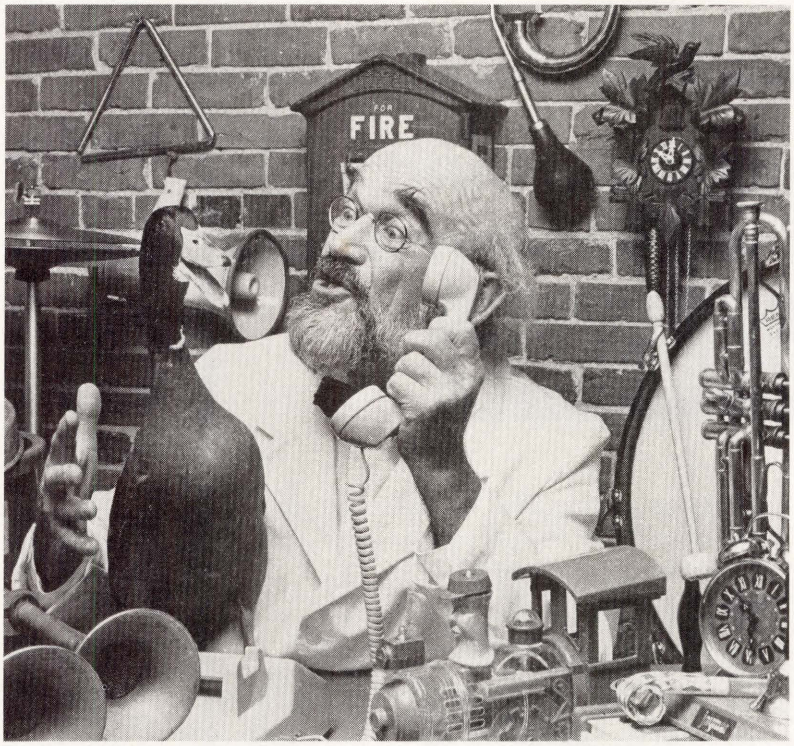
Anadex®
...the plus in printers

CIRCLE 113 ON INQUIRY CARD

...close please.

SALES OFFICES: San Jose, CA (408) 247-3933
Fullerton, CA (714) 871-0501 • Wakefield, MA (617) 245-9160 • Austin, TX (512) 327-5250

ANADEX, INC. • 9825 DeSoto Avenue • Chatsworth, California 91311, U.S.A. • Telephone: (213) 998-8010 • TWX 910-494-2761
ANADEX, LTD. • Dorna House, Guildford Road • West End, Woking, Surrey GU24 9PW, England • Tel: Chobham (09905) 6333 • Telex: 858762 ANADEX G



GET THE DTMF DECODER THAT OUTWITTED THE DIABOLICAL DR. GLITCH.

Talk to Teltone first...

YOU: Dr. who?

US: Glitch. A twisted mastermind who torments DTMF decoders in his secret laboratory.

YOU: How?

US: By whipping up sounds that drive DTMF decoders batty. Like whoops, screeches, screams. Steam engines, bagpipes, even duck quacks.

YOU: But no DTMF decoder can stand that kind of abuse.

US: The new Teltone M-927 can. Our 13 years of experience have made this 40-pin DIP more than a match for the diabolical doctor.

YOU: What? It's that selective?

US: Sure. For its small size, it has the world's best combination of the critical performance specifications—signal-to-noise ratio and speech immunity. Over a 36db dynamic range.

YOU: But how can I be sure?

US: Read our detailed testing procedures book. Then, test it yourself.

YOU: Fair enough. Is there anything else I should know?

US: Listen to this. The M-927 accepts DTMF signals or rotary dial pulses from telephones, radios, tone generators, or any other source.

YOU: But is it flexible?

US: Output provides binary, 2 of 8, 1 of 12 format, or blank. Clocks and strobe give you more versatility and control than you can imagine.

YOU: With all that, it must cost a small fortune.

US: Less than its predecessors.

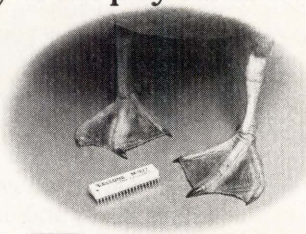
YOU: So, tell me more.

US: We'd love to. Give us a call or drop a line.

YOU: Say, it really does pay to talk to Teltone.

US: Well, better that you hear from us than Dr. Glitch.

YOU: Dr. who?



TELTONE

It pays to talk to Teltone.

Phone (800)426-5918. Teltone Corporation,
P.O. Box 657, Kirkland, WA 98033.

CIRCLE 114 ON INQUIRY CARD

SUBASSEMBLIES

QUAD-BOARD DISC CONTROLLER

Interfacing DEC LSI-11, -11/2, or -11/23 microcomputers with 2 Shugart SA4000, Fujitsu 2301 or 2302, or Memorex 101 or 102, microprocessor based DQ401 controller emulates the DEC RKV-11/RK05 disc subsystem and is compatible with RT-11 and RSX-11 software. It occupies one card slot of a Q-bus chassis, and interfaces to the drives via a jumper selectable single- or dual-cable arrangement. Features include data buffer for elimination of data late errors, automatic flaw compensation, data error checking, onboard bootstrap, and extended memory addressing to 256k bytes. **Distributed Logic Corp,** 12800-G Garden Grove Blvd, Garden Grove, CA 92643.

Circle 237 on Inquiry Card

MATRIX PRINTHEAD

With a repetition rate of 1200 Hz and 0.012" (0.030-cm) needles, 9-needle matrix head Mark IV WP produces either standard matrix style printing or high quality standard fonts such as elite simply by ROM change. Needle flight time is closely controlled to ±10 μs. This, combined with smaller than standard needle diameter, produces typewriter speed quality print at 5 times typewriter speed. Life is about 500M char. **Universal MicroPrinters, Inc,** PO Box 313, Shelton, CT 06484.

Circle 238 on Inquiry Card

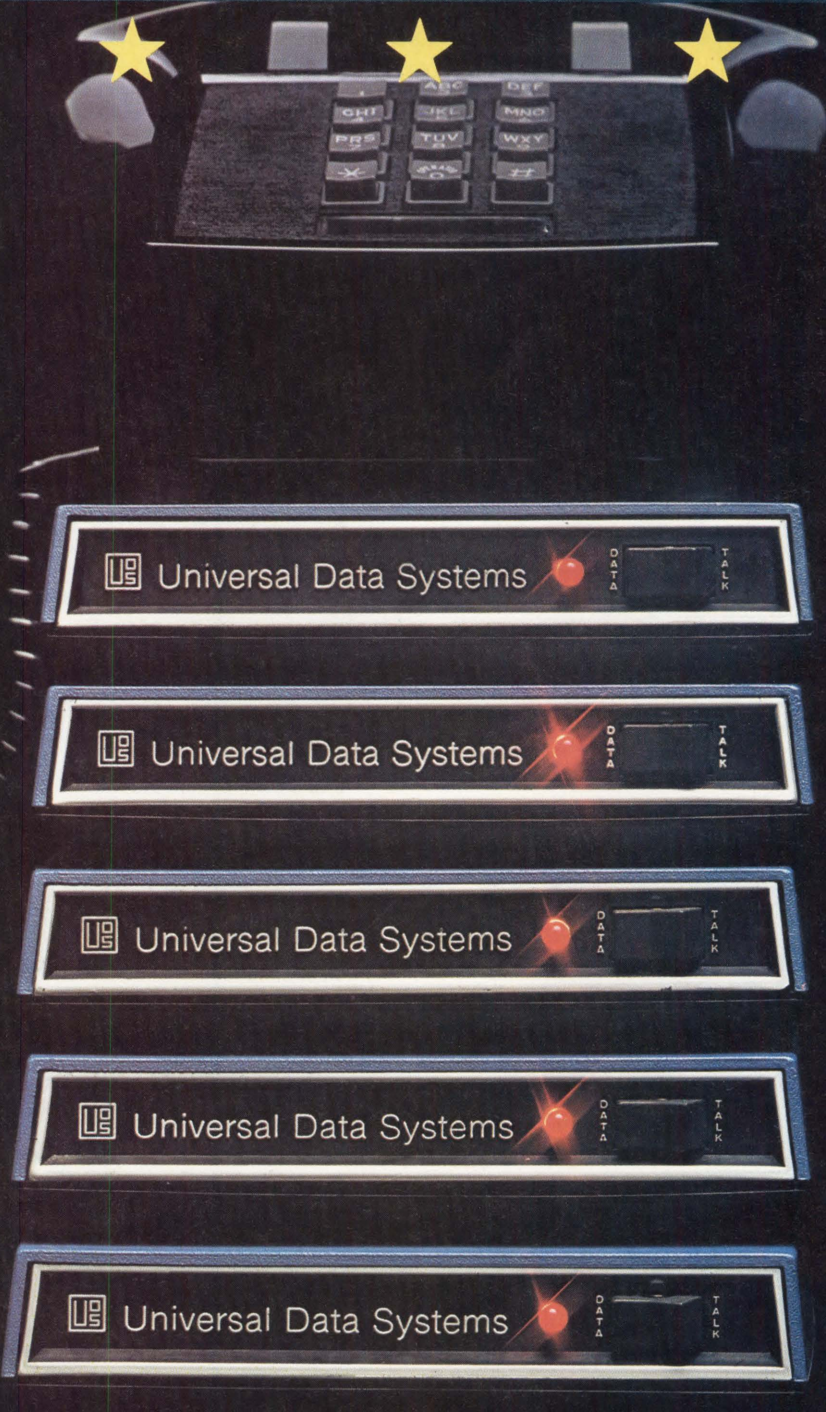
FLOPPY DISC DRIVE CONTROLLERS

A std Multibus board and an iSBX multimodule board control up to 4 industry std single- or double-density, single- or double-sided 8 and 5.25" (20 and 13.34-cm) diskette drives. iSBX 218 serves as a plug-in to iSBC 80/10B, 80/24, and 88/40 single-board computers. It communicates at board level using the iSBX bus protocol. The iSBC 208 uses the std Multibus concept for easy integration into systems using iSBC 80 and 86 single-board computers. The systems' 8272 floppy disc controller chip ensures read and write compatibility in double- and single-density formats. Diskettes recorded using either controller are interchangeable with other systems using these formats. Other features common to both controllers include programmable data record lengths of 128, 256, 512, and 1024 bytes/sector and a multisector and multitrack transfer capability. When operating in nonstandard applications, the unit can achieve record lengths of 8192 bytes/sector in double-density and 4096 bytes/sector in single density. **Intel Corp,** 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.

Circle 239 on Inquiry Card

FIVE OF A KIND

LOW POWER ★ LOW PRICED ★ LINE POWERED MODEMS



202S LP auto-answer 1200 bps	**$295** (quantity one)
202 LP 1200 bps	**$245** (quantity one)
103J LP originate/answer auto-answer 300 bps	**$245** (quantity one)
103 LP originate/answer 300 bps	**$195** (quantity one)
103 LP originate only 300 bps	**$185** (quantity one)

All UDS LP modems are FCC-certified for direct connection to the telephone network and require no AC power connection. For details, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Phone: 205/837-8100.

"Confidence in Communications"

Universal Data Systems

Member
IDCMA

DISTRICT OFFICES: **Summit,** NJ, 201/522-0025 · **Blue Bell,** PA, 215/643-2336 · **Atlanta,** 404/998-2715 · **Chicago,** 312/441-7450 · **Columbus,** OH, 614/846-7478 **Dallas,** 214/385-0426 · **Santa Ana,** 714/972-4619 · **Sunnyvale,** 408/738-0433 · **Boston,** 617/875-8868.

See us at
COMDEX/**SPRING'81**
Booth 2620

Created by Dayner/Hall, Inc., Winter Park, Florida

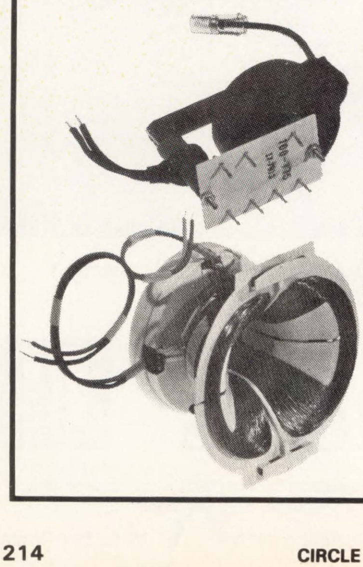
CIRCLE 116 ON INQUIRY CARD

POWER SOURCES AND REGULATORS

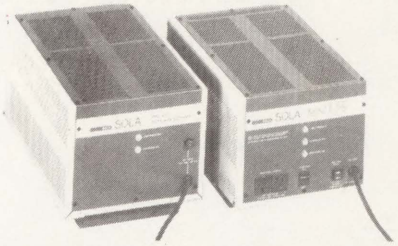
DC-DC TRIPLE-OUTPUT CONVERTERS

RDT multiple-output switching stabilizers function from 24- and 48-Vdc inputs. 24-V models work from 20 to 30 Vdc while the 48-V models accommodate inputs from 42 to 56 Vdc. Two output combinations are offered for each source voltage selection, a 5-V, 10-A logic output together with either ±12 V at 1 A or ±15 V at 1 A. Each output is fully stabilized with its own feedback loop. The 5-V, 10-A output has remote error sensing. All outputs are protected by an overvoltage detector of the squelch type. **Kepco Inc,** 131-38 Sanford Ave, Flushing, NY 11352.

Circle 240 on Inquiry Card



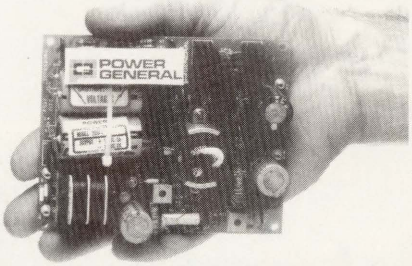
AUXILIARY UPS BATTERY



An auxiliary battery pack with self-contained battery charger provides additional dc power to the company's Mini UPS, permitting extended operation in blackout or severe low voltage condition. A sealed, maintenance-free lead acid battery furnishes an additional 60 min of dc power to the 400-VA UPS, and 30 min to the 750-VA model. For max standby power, 2 packs may be added to each UPS. When line power returns after a blackout, the auxiliary unit automatically recharges itself to 95% of full potential in less than 10 times the discharge time. Fuse protected input circuitry prevents damage in case of short circuit or extreme overload. The unit plugs into any std ac output and connects to the UPS by an external jack at the rear. **Sola Electric, a unit of General Signal,** 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 241 on Inquiry Card

50-W DUAL-OUTPUT SWITCHING POWER SUPPLY



Series 2050 supplies are true off-the-line switchers that are available in 3 models: 5 Vdc at 8 A and −5 Vdc at 2 A; 12 Vdc at 5 A and −12 Vdc at 2 A; and 15 Vdc at 5 A and −15 Vdc at 2 A. Input voltage range is jumper selectable for 90 to 130 Vac or 180 to 260 Vac, and input frequency range is 47 to 450 Hz. Line regulation is ±0.7%, load regulation is ±0.1%, holdup time is 16 ms, I/O isolation is 1500 Vac, op temp range is 0 to 70 °C, and storage temp is −55 to 85 °C. **Power General,** 152 Will Dr, Canton, MA 02021.

Circle 242 on Inquiry Card

- Motorola MC68000 16-bit processor
- Multi-tasking operating system
- Languages supported include C, PASCAL and BASIC
- Mass storage devices up to 10MB

- 19″ CRT
- 1024 x 768 high resolution color graphics
- 256 simultaneously displayable colors

- CAD/CAM
- Business Graphics
- Imaging
- Animation
- Process Control
- Scientific
- Graphic Arts
- Demography
- Cartography

- **CGC 7900** prices start at **$19,995.**

- Call toll-free 1-800-241-9467.

INTRODUCING THE WORLD'S MOST POWERFUL USE OF COLOR.

Chromatics™

The World's Most Colorful Computer Company.

Chromatics, Inc./2558 Mountain Industrial Boulevard/Tucker, GA 30084/Telephone: 404/493-7000/TWX: 810/766-8099

CIRCLE 118 ON INQUIRY CARD

POWER SOURCES AND REGULATORS

DISC MEMORY POWER SUPPLIES

Open frame linear ECV/ETV series supplies provide industry std power for disc drives with triple and dual outputs. ECV151, ETV651, ETV701, ETV801, and ETV851 feature universal transformer taps for international voltage requirements, 100% vacuum impregnated transformer, computer grade electrolytic aluminum capacitors, and hermetically sealed power semiconductor. Units meet high voltage isolation, grounding, and leakage current requirements of VDE 0804, and are UL listed and CSA certified. **ACDC Electronics, Div of Emerson Electric Co,** 401 Jones Rd, Oceanside, CA 92054.

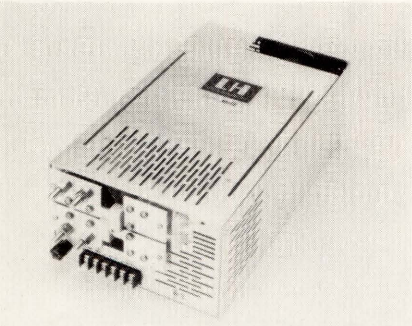
Circle 243 on Inquiry Card

STANDALONE DC-DC SUPPLY MODULE

Ultra-wide input, isolated 5-V, 5-A WP series offers direct output paralleling without power trimming, remote on-off control input, overvoltage protection, and 77% efficiency. Turn-on input range is 1.8 to 100 Vdc or open circuit; turn-off input range is ±0.5% max. Op temp range is −25 to 71 °C and storage temp range is −55 to 105 °C. "U" size package measures 2.56 x 4.56 x 0.83" (6.50 x 11.58 x 2.11 cm). **Stevens-Arnold, Inc,** 7 Elkins St, South Boston, MA 02127.

Circle 244 on Inquiry Card

1500-W CLOSED FRAME SWITCHER



Super Mite 81 employs 4 switching transistors, custom LSI control chip, and power MOSFETs to increase reliability and performance in add-on memory, ATE system, and high power ECL applications. Input range is 85 to 130 Vac or 170 to 260 Vac at 47 to 63 Hz; line regulation is 0.4% over entire input range; and output is from 2 Vdc at 337 A to 28 Vdc at 57 A. Std features include power fail detection, overvoltage protection on main output, remote on/off, remote sense on main input, and margining. **LH Research, Inc,** 14402 Franklin Ave, Tustin, CA 92680.

Circle 245 on Inquiry Card

±15-V, 100-mA MODULAR POWER SUPPLY

Model 22-100 allows user to obtain regulated ±15 V and unregulated ±24 V simultaneously; total current drawn can total ±100 mA. Supply measures 1.00 x 2.00 x 3.00" (2.54 x 5.08 x 7.62 cm), weighs 8.5 oz (238 g), and can be soldered directly to a PCB or mounted with model MK 015 or MK 08B mounting kits. Noise and ripple is 2 mV rms; tempco is ±0.01%/°C; output voltage accuracy is ±0.5%; line and load regulation is ±0.02%; and max case op temp is ±71 °C. **Calex Mfg Co, Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523.

Circle 246 on Inquiry Card

MISCELLANEOUS

UNIVERSAL PROGRAMMER

Programming semiconductor memories and logic devices without personality modules, socket adapters, or configurators, System 37 relies on software routines for device selection. Consisting of a central controller that doubles as an NMOS EPROM programmer plus 3 peripheral units, the unit contains 64k (8k x 8) of static RAM buffer, dot matrix alphanumeric display, RS-232 serial interface with modem handshake, and 16-bit bidirectional parallel interface. Central controller can program EPROMs from 4k through 256k, selectable from a thumbwheel switch for std 24- or 28-pin devices. Dot matrix display handles 40 programmer status messages. Program data can be entered from keyboard, RS-232 interface, master device, or 16-bit parallel interface. **Citel, Inc,** 392 Potrero Ave, Sunnyvale, CA 94086.

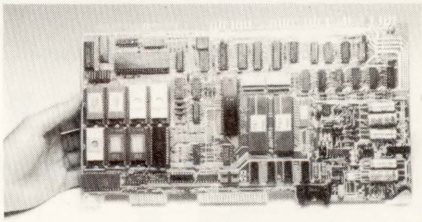
Circle 247 on Inquiry Card

UNIVERSAL LOGIC PANELS

Series 8186-UG159-2 logic panels with right angle header and 8162-LG912-2 logic panels with edge fingers are compatible with Augat's 8136 series plug-in card. Double-sided boards have 36 rows of 50 contacts on 0.300" (0.762-cm) spacing, and accept any combination of 2- through 40-lead components. Features include planar power distribution with proper edge connector pinouts for V_{cc} and ground. Power and ground planes are connected to additional sleeves outside of contact row for decoupling. **Stanford Applied Engineering, Inc,** 3520 De La Cruz Blvd, Santa Clara, CA 95050.

Circle 248 on Inquiry Card

SPEECH SYNTHESIZER BOARD



Speech 1000 features large vocabulary capacity, speech fidelity, and 3-way interfacing flexibility. The unit offers Multibus plug-in compatibility or can be interfaced through its TTL parallel port or RS-232-C serial port. A simple command protocol simplifies the host computer's interaction with the board, by permitting a CPU to download a sequence of commands and word pointers that specify the message and how it is enunciated. Seven memory sockets are available for vocabulary storage; depending on vocabulary size, 16k-, 32k-, or 64k-bit std EPROM or ROM devices are used. Speech data are analyzed and compressed for storage on the board using the linear predictive coding process. The std process compresses speech digitized at 120k bits/s to a rate of 2200 bits/s. **Telesensory Speech Systems,** 3408 Hillview Ave, Palo Alto, CA 94304.

Circle 249 on Inquiry Card

OCTOPLUS

The Sprague Monolithic Arrays That Provide the Muscle of 8 SCRs in a Single DIP.

Sprague UTN-2886B and UTN-2888A SCR arrays are expressly made for use with microprocessors which are strobing power loads. Compatible with TTL, LSTTL and CMOS, they will interface to high-current loads including lamps, relays, and solenoids.

Each array contains eight SCRs with integral current limiting and gate-to-cathode resistors. The combining of SCRs in one DIP reduces component count, assembly time, and circuit space while improving overall circuit reliability. Each of the isolated devices within the array is capable of continuous and simultaneous operation at 200 mA or 250 mA, at ambient temperatures to +50°C. The arrays operate from an unfiltered half-wave (50 or 60 Hz) or full-wave (100 or 120 Hz) rectified source.

For Engineering Bulletin 29401, write to: Technical Literature Service, Sprague Electric Company, 555 Marshall St., North Adams, Mass. 01247.

For application engineering assistance, write or call Mark Heisig, Don Bird, or Paul Emerald, Semiconductor Division, Sprague Electric Co., 115 Northeast Cutoff, Worcester, Mass. 01606. Telephone 617/853-5000.

For the name of your nearest Sprague Semiconductor Distributor, write or call Sprague Products Company Division, North Adams, Mass. 01247. Telephone 413/664-4481.

FOR FAST INFORMATION, CALL YOUR NEAREST SPRAGUE SALES OFFICE:

ALABAMA, Sprague Electric Co., 205/883-0520 • **ARIZONA**, Sprague Electric Co., 602/244-0154; 602/966-7233 • **CALIFORNIA**, Sprague Electric Co., 213/649-2600; 714/549-9913; R. David Miner Inc., 714/421-5586; Wm. J. Purdy Co., 415/347-7701 • **COLORADO**, Wm. J. Purdy Co., 303/777-1411 • **CONNECTICUT**, Sprague Electric Co., 203/261-2551; Ray Perron & Co., Inc., 203/268-9631; 203/673-4825 • **DIST. OF COLUMBIA**, Sprague Electric Co. (Govt. sales only), 202/337-7820 • **FLORIDA**, Sprague Electric Co., 305/831-3636 • **ILLINOIS**, Sprague Electric Co., 312/296-6620 • **INDIANA**, Sprague Electric Co., 317/253-4247 • **MARYLAND**, Sprague Electric Co., 301/792-7657 • **MASSACHUSETTS**, Sprague Electric Co., 617/899-9100; 413/664-4411; Ray Perron & Co., Inc., 617/969-8100 • **MICHIGAN**, Sprague Electric Co., 517/787-3934 • **MINNESOTA**, HMR, Inc., 612/831-7400 • **MISSOURI**, Sprague Electric Co., 314/781-2420 • **NEW HAMPSHIRE**, Ray Perron & Co., Inc., 603/742-2321 • **NEW JERSEY**, Sprague Electric Co., 201/696-8200; 609/795-2299; Trinkle Sales Inc., 609/795-4200 • **NEW MEXICO**, Wm. J. Purdy Co., 505/266-7959 • **NEW YORK**, Sprague Electric Co., 516/234-8700; 914/834-4439; 315/437-7311; Wm. Rutt, Inc., 914/834-8555; Paston-Hunter Co., Inc., 315/437-2843 • **NORTH CAROLINA**, Electronic Marketing Associates, 919/722-5151 • **OHIO**, Sprague Electric Co., 513/866-2170; Electronic Salesmasters, Inc., 800/362-2616 • **PENNSYLVANIA**, Sprague Electric Co., 215/467-5252; Trinkle Sales Inc., 215/922-2080 • **SOUTH CAROLINA**, Electronic Marketing Associates, 803/233-4637 • **TEXAS**, Sprague Electric Co., 214/235-1256 • **VIRGINIA**, Sprague Electric Co., 703-463-9161 • **WASHINGTON**, Sprague Electric Co., 206/632-7761 • **CANADA**, Sprague Electric of Canada, Ltd., 416/766-6123 or 613/238-2542.

4SS-1108

SPRAGUE®
THE MARK OF RELIABILITY

a subsidiary of **GK Technologies**
Incorporated

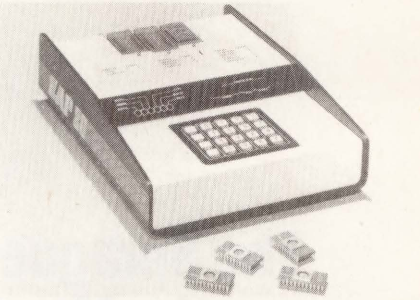
CIRCLE 120 ON INQUIRY CARD

MISCELLANEOUS

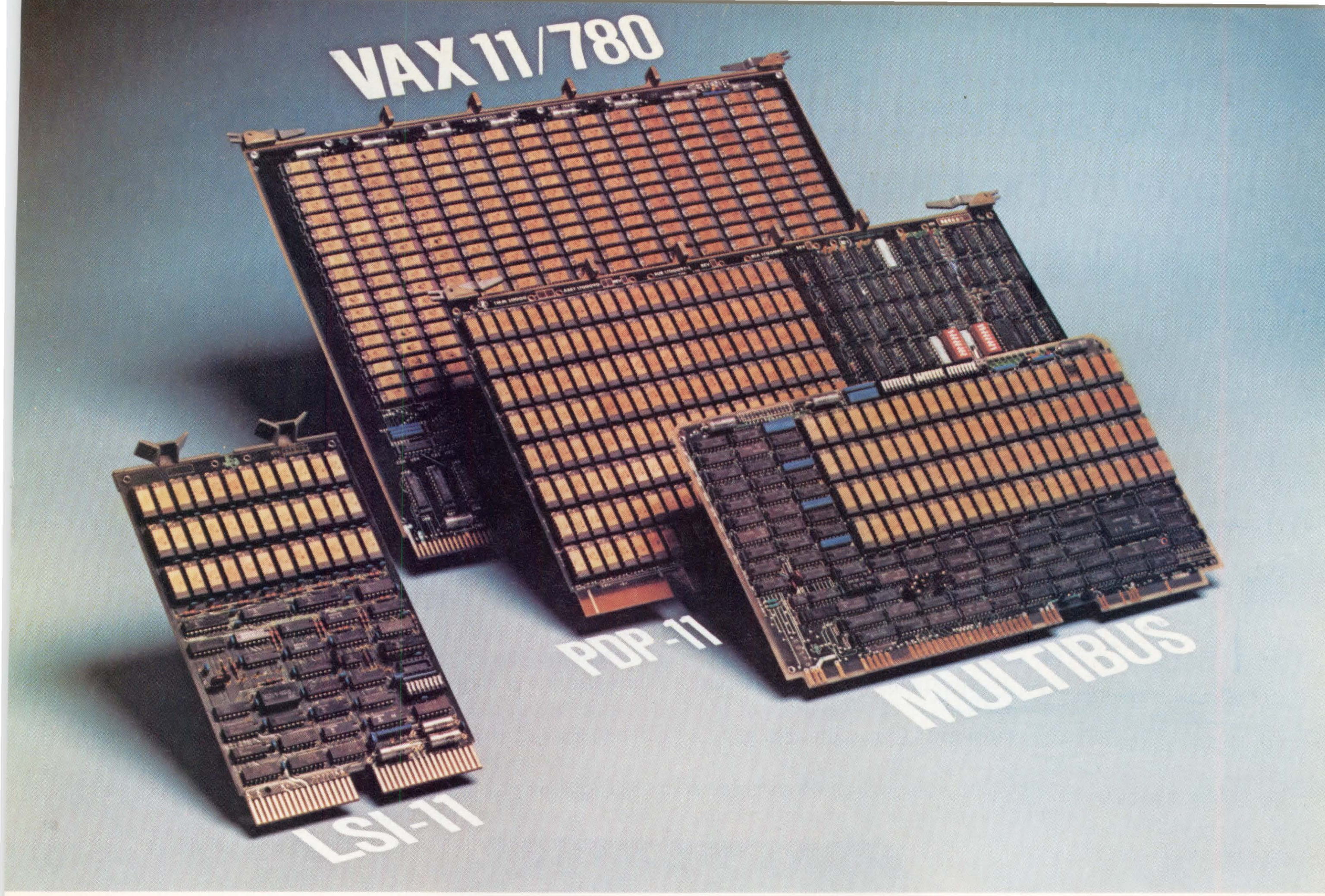
SPEECH RECOGNITION DEVELOPMENT SYSTEM

V1000 recognizes isolated words or commands in any language and may be used to enter data, activate machines, or control remote processes. It is trained to a user's voice print by simply pressing a word button and speaking into a microphone. It provides 99%+ accuracy even with inexpensive microphones, single training trials, variable telephone conditions, and noisy backgrounds. To achieve this, it incorporates digital filters, enhanced dynamic programming, and an innovative approach to noise immunity. The standalone development system contains all processing power, logic, and memory necessary to perform training and word recognition as well as interface to external equipment. It consists of an 11 x 18" (28- x 46-cm) front panel with 80 word buttons and 14 control keys. Up to 80 double-trained words may be entered using the training panel; up to 160 single-trained words may be entered through an external display and control processor. The unit can also be used for voice data entry into an online system. An optional switching unit allows direct voice activation of machinery or industrial loads. **Votan, Inc**, 26046 Eden Landing Rd, Suite 7, Hayward, CA 94545. Circle 250 on Inquiry Card

EPROM PROGRAMMER



With 64k onboard RAM, ZAP 80 provides editing, debugging, and self-diagnostic features as well as battery operation. The unit programs Intel's 2704, 2716, 2764; Mostek's 2708, 2516, and 2764; TI's 2508, 2732, and 2564; Motorola's 2758, 2732A, and MCM 68764; and TMS2716 and HM48016 EEPROMs. After the user keys in a device type on the 20-key pad, 3 LEDs indicate which socket to plug the device into; the type selected is displayed on a 7-segment, 8-digit LED display. The unit's 1802 microprocessor controls sequencing, pinouts, voltages, and timing with software controlled programming of all devices. Keypad controlled editing functions include peek, poke, move, checksum, complement data, clear RAM to state, and list data. In addition to the 64k-bit data RAM, the programmer has a 64k (8k x 8) P/ROM/ROM simulator. RS-232 serial interface or 20-mA current loop is provided. **Sunrise Electronics**, 524 S Vermont Ave, Glendora, CA 91740.
Circle 251 Inquiry Card



TI leadership. In 64K DRAM technology. In Memory Systems.

Whatever bus you're using — VAX†, PDP-11†, LSI-11†, or even Multibus‡ — TI can supply add-in memory system boards with dynamic RAMs from our own high-performance 64K series.

When you specify TI's high-density, low-power boards, you save rack space. So you have more room for I/O — or whatever else you need. And, the low-power consumption of TI 64K DRAMs, compared to the old-fashioned 16Ks, cuts temperature levels and increases reliability. The reduction in memory package count by as much as four boosts reliability even more.

System reliability will be higher, too. Thanks to error correction/detection available on many TI memory boards. Using our own bipolar EDAC chip helps cut component count and system temperature, as well as improving basic system reliability. The EDAC chip replaces about a quarter of a board of TTL circuitry.

All TI boards are 100% tested. 100% burned-in. All in TI's modern, high-capacity Houston facility. Delivery normally ranges from stock to four weeks.

Low cost

Representative pricing* for TI memory boards is as follows: $1600 for TMM10000-04 (192KB); $3800 for TMM20000-02 (256KB); $9000 for TMM30000-01 (1MB); $1845 for TMM40010-07 (64KB).

TI MEMORY BOARDS — CURRENT AVAILABILITY

System	TI Series	BYTES/BOARD						
		64K	128K	192K	256K	512K	768K	1M
LSI-11†	TMM10000[1]		X	X	X			
PDP-11†	TMM20000[2]		X	X	X	X		X
VAX†	TMM30000					X	X	X
Multibus‡	TMM40010[2]	X	X		X	X		

[1] Parity optional [2] EDAC standard

Custom capability

If you need custom memory systems in production quantities, be sure and talk to TI. We'll custom design boards for specific applications with the same meticulous attention to cost/performance effectiveness that our standard boards offer.

So for the latest DRAM technology, highest packing densities, lowest power consumptions, all at competitive prices, remember memory systems from Texas Instruments.

To find out more about TI boards call your local TI field sales office or authorized distributor. For details, call (713) 778-6549, or write to Texas Instruments Incorporated, Integrated Memory Systems, P.O. Box 1443, M/S 6404, Houston, Texas 77001.

TEXAS INSTRUMENTS
INCORPORATED

---

†Trademark Digital Equipment Corp.
‡Trademark Intel Corp.
*U.S. Single-unit price, subject to change without notice.

85215

CIRCLE 122 ON INQUIRY CARD

Do standard, low cost power supplies have to be tweaked and modified to work? Not with Sierracin power systems.

The power supplies we design are made to deliver a cost-performance ratio second to none. Our multi-output switchers are prime examples. Auxiliary outputs are pre-regulated by the switching section, then post-regulated with linear regulators. As a result, *each* output remains tightly regulated regardless of individual load changes. This means excellent dynamic response characteristics. No cross regulation. And "goodbye" to unexplained system crashes.

What about line transients? Our switchers have a wide ac input range of 90-132/180-264 volts which offers greater immunity to line noise and brownouts.

And those tight, little spaces? Our compact, low-profile line of 40 to 500 watt, open-frame dc switching power supplies will fit just about anywhere. Prices start at a low $45 — with OVP on every product including linears at no extra cost.

In short, we build affordable power supplies which keep on working — the first time, every time — you put them in your system. It's what you can expect from Sierracin/Power Systems. A young, dynamic 6-year-old company that's already a recognized industry leader.

See for yourself. Write for our new 1981 Power Supply Catalog. Or dial our toll free number.

For technical information or application assistance, call:

800-423-5569

In California, call (213) 998-6811 collect.

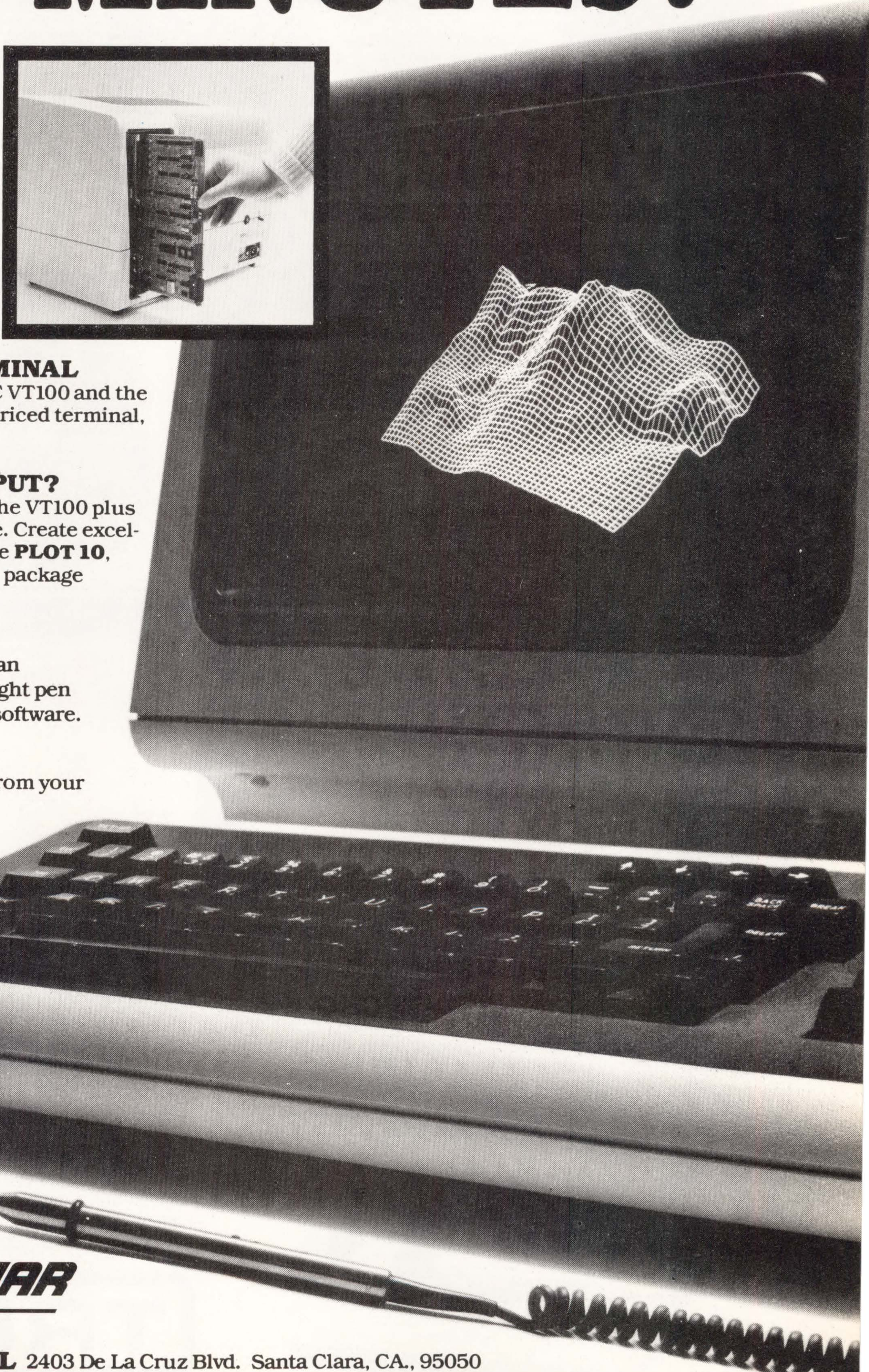
Sierracin/Power Systems

20500 Plummer Street, Chatsworth, California 91311
Telephone (213) 998-9873

CIRCLE 123 ON INQUIRY CARD

VT100 GRAPHICS IN 4.4 MINUTES!

From Selanar Of Course!



SIMPLY ADD A CARD

Adding the Graphics 100 PC card to your existing VT100 or VT103 gives you the most versatile CRT terminal on the market today. No other component or CRT changes are required.

OR BUY OUR GRAPHICS TERMINAL

The Selanar GT100 combines the DEC VT100 and the Graphics 100 into a very competitively priced terminal, designed to fit your application.

NEED TEKTRONIX 4010 OUTPUT?

Our GT100 has all the capabilities of the VT100 plus our new Tektronix 4010 emulation mode. Create excellent graphics displays with packages like **PLOT 10**, **DISSPLA & TELAGRAF**, or any other package with 4010 output mode.

HOW ABOUT SOFTWARE?

Selanar supplies • Calcomp type Fortran subroutines for: RT-11, RSX, VMS. • Light pen support software • Hardcopy support software.

CALL US!

Let us show you how to get the most from your computer terminals.

(408) 727-2811

ISI SELANAR

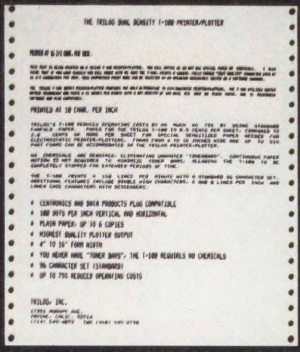
ISI SELANAR INTERNATIONAL 2403 De La Cruz Blvd. Santa Clara, CA., 95050

EUROPEAN HEADQUARTERS: ISI COMPUTER Alte Landstrasse 5 D 8012 Ottobrunn Telefon (089) 60 60 71-72 Telex 5216290

CIRCLE 124 ON INQUIRY CARD

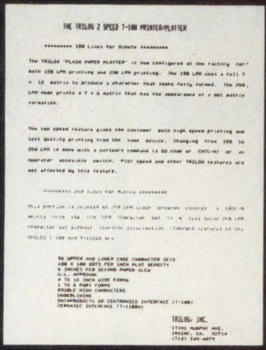
WITH TRILOG PRINTERS:

THE EXTRAS ARE FREE!



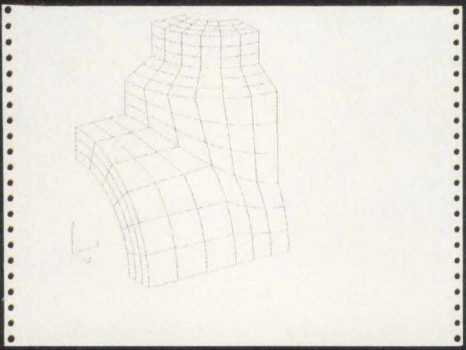
```
THE TRILOG DUAL DENSITY T-100 PRINTER/PLOTTER

PRINTED AT 16 2/3 CHAR. PER INCH.

PRINTED AT 10 CHAR. PER INCH

TRILOG'S T-100 REDUCES OPERATING COSTS BY AS MUCH AS 75% BY USING STANDARD
FANFOLD PAPER.  PAPER FOR THE TRILOG T-100 IS 0.5 CENTS PER SHEET, COMPARED TO
2.0  CENTS OR MORE PER SHEET FOR SPECIAL SENSITIZED PAPER NEEDED FOR
ELECTROSTATIC PRINTER/PLOTTERS.  FORMS FROM 4 TO 16 INCHES WIDE AND UP TO SIX
PART FORMS CAN BE ACCOMMODATED IN THE TRILOG PRINTER/PLOTTER.

NO CHEMICALS ARE REQUIRED, ELIMINATING UNWANTED "TONERBARS".  CONTINUOUS PAPER
MOTION IS NOT REQUIRED TO MINIMIZE TONER BARS, ALLOWING THE T-100 TO BE
COMPLETELY STOPPED FOR EXTENDED PERIODS OF TIME.

THE T-100 PRINTS A 150 LINES PER MINUTE WITH A STANDARD 96 CHARACTER SET.
ADDITIONAL FEATURES INCLUDE DOUBLE HIGH CHARACTERS, 6 AND 8 LINES PER INCH AND
LOWER CASE CHARACTERS WITH DESCENDERS.

* CENTRONICS AND DATA PRODUCTS PLUG COMPATIBLE
* 100 DOTS PER INCH VERTICAL AND HORIZONTAL
* PLAIN PAPER, UP TO 6 COPIES
* HIGHEST QUALITY PLOTTER OUTPUT
* 4" TO 16" FORM WIDTH
* YOU NEVER HAVE "TONER BARS", THE T-100 REQUIRES NO CHEMICALS
* 96 CHARACTER SET (STANDARD)
* UP TO 75% REDUCED OPERATING COSTS

TRILOG, INC.
17391 MURPHY AVE.
IRVINE, CALIF. 92714
(714) 549-4079   TWX (910) 595-2798
```

NORMAL AND COMPRESSED PRINTING

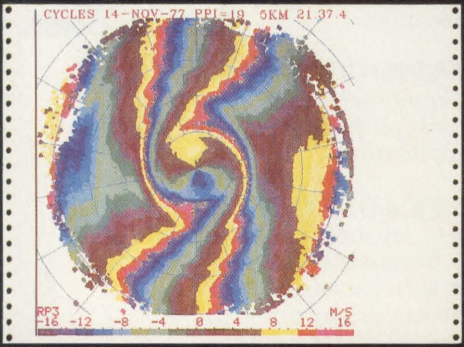


```
THE TRILOG 2 SPEED T-100 PRINTER/PLOTTER

     ********* 150 Lines Per Minute *********

The TRILOG "PLAIN PAPER PLOTTER" is now configured at the factory  for/
both 150 LPM printing and 250 LPM printing.  The 150 LPM uses a full 7
x  12  matrix to produce a character that looks fully formed.  The 250,
LPM mode prints a 7 x 6 matrix that has the appearance of a dot matrix
formation.

The two speed feature gives the customer  both high speed printing and
text quality printing from the  same  device.  Changing  from  150  to
250 LPM is done with a software command (a SO code or  CNTL-N)  or  an
operator  accessible  switch.  Plot speed and other TRILOG features are
not affected by this feature.

     ********* 250 Lines Per Minute *********

This portion is printed at 250 LPM under  program  control.  A  CNTL-N
shifts  from  the  150  LPM  character  set  to  a  less dense 250 LPM
character set without  operator intervention.  Standard features of the
TRILOG T-100 and T-1100A are:

          96 UPPER AND LOWER CASE CHARACTER SETS
          100 X 100 DOTS PER INCH PLOT DENSITY
          6 INCHES PER SECOND PAPER SLEW
          U.L. APPROVAL
          4 TO 16 INCH WIDE FORMS
          1 TO 6 PART FORMS
          DOUBLE HIGH CHARACTERS
          UNDERLINING
          DATAPRODUCTS OR CENTRONICS INTERFACE (T-100)
          VERSATEC INTERFACE (T-1100A)

                                        TRILOG, INC.
                                        17391 MURPHY AVE.
                                        IRVINE, CA.  92714
                                        (714) 549-4079
```

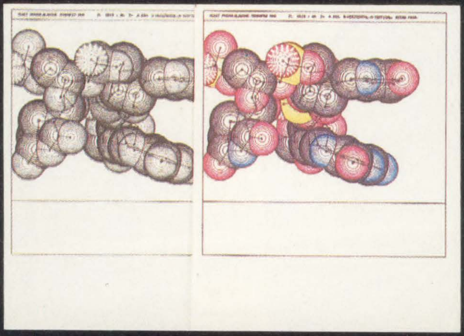
150 LPM AND 250 LPM



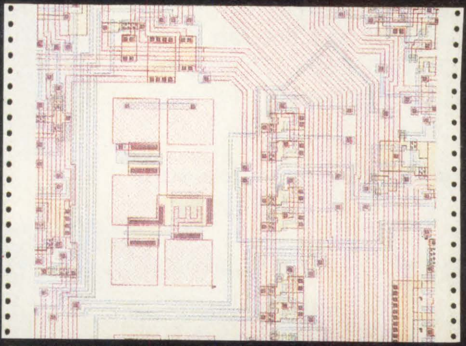
HI RES. STRESS ANALYSIS (PDA Eng.)



RADAR WEATHER MAPPING



SCIENTIFIC: MOLECULAR STRUCTURE (MIT)



CAD/CAM: IC CHIP LAYOUT (Silicon Systems Inc.)

ONLY the TRILOG COLORPLOT™ line printer has all the EXTRAS — at no additional cost!!! EXTRAS such as near letter quality printing at 150 LPM, and either matrix quality printing at 250 LPM, or text quality 150 LPM compressed print at 16 2/3 CPI for printing full 132 character lines on 8 1/2 inch paper. PLUS, high resolution black and white graphics plotted on plain paper at only 1/2 cent per copy. But, that's not all...the most exciting and unique EXTRA of them all is the ability to plot high resolution FULL COLOR graphics for applications such as: CAD/CAM, Scientific, 3-d Cartography, Computer Art, and Business Charts.

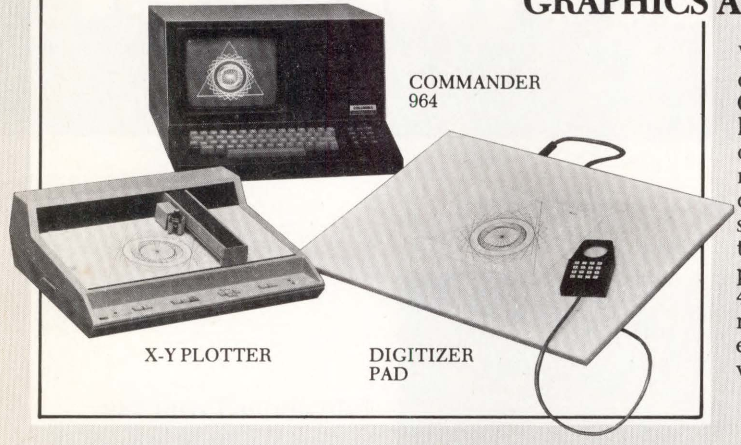
COLORPLOT™ is sold and serviced through the worldwide network of TRILOG distributors. For futher information contact your local TRILOG distributor, or request the "COLORPLOT Packet" by writing or calling: TRILOG, Inc., 17391 Murphy Avenue, Irvine, CA 92714 -- (714)549-4079. TWX(910)595-2798.

TRILOG

CIRCLE 125 ON INQUIRY CARD

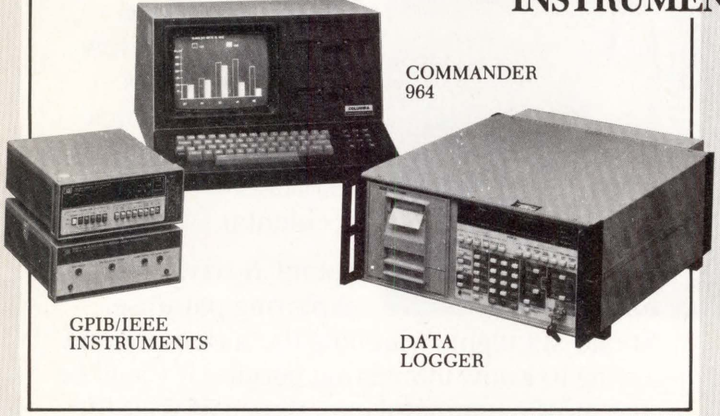
Our Microcomputer ... your world

GRAPHICS AND DIGITIZING



With all the self contained vector and point plotting capabilities of a sophisticated graphics terminal, our COMMANDER 964 lets you create bar charts, pie charts histograms and complex point-to-point plots. You can even output displays intended for a Tektronix® 4010 with our terminal emulator. And, the Model 964 provides you with a double processor Z-80A architecture so that display buffers, software, firmware and associated real-time constraints of the 512 x 256 graphics capability are all independent of the primary 64K memory processor system. As a result, the full 4.0 MHz processor speed is dedicated to the end user which means that you can run larger programs and enjoy faster execution times when using CP/M™ and PASCAL based software.

INSTRUMENTATION AND PROCESS CONTROL



Columbia's COMMANDER has the operating performance and interface flexibility to handle your instrumentation and control applications. It has four RS232 ports that can handle serial data up to 19,200 baud, four parallel ports and four independent, programmable-interval timer/counters. In addition, the dual Z-80A architecture with maximum RAM expansion to 128K, full 512 x 256 graphics capability together with optional DMA, GPIB/IEEE controller and 9511 Arithmetic Unit, make the COMMANDER a powerful, intelligent controller. All of this, and the availability of higher level languages such as BASIC, FORTRAN, PASCAL and ASSEMBLERS, makes our COMMANDER the best.

BUSINESS AND DATA COMMUNICATIONS

With CP/M capability, our Z-80A based COMMANDER allows you access to the largest microcomputer-based business applications software library ever. An applications software library that includes extensive time-proven Word Processing, Data Base Management, and Financial Control Applications. And, if you're concerned about expansion, the COMMANDER has a built-in floppy disk capacity of up to 1.6 million characters plus external Winchester disk capacity from 5 million to 40 million characters. Furthermore, we designed the COMMANDER with extensive peripheral I/O capability, including data rates from current loop asynchronous to RS232 synchronous communications. For your expanding business applications, the COMMANDER is the answer.

Columbia Data Products also offers a full complement of single and multi-user computer systems, with or without built-in terminals, to satisfy even more demanding applications . . . field proven hardware and software at prices you need to succeed.

Inquiries for custom configurations are welcome.

COLUMBIA
DATA PRODUCTS, INC.

8990 Route 108
Columbia, MD 21045
301-992-3400
TWX: 710-862-1891

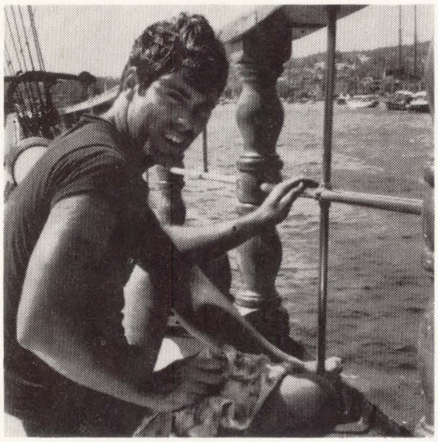
CIRCLE 126 ON INQUIRY CARD

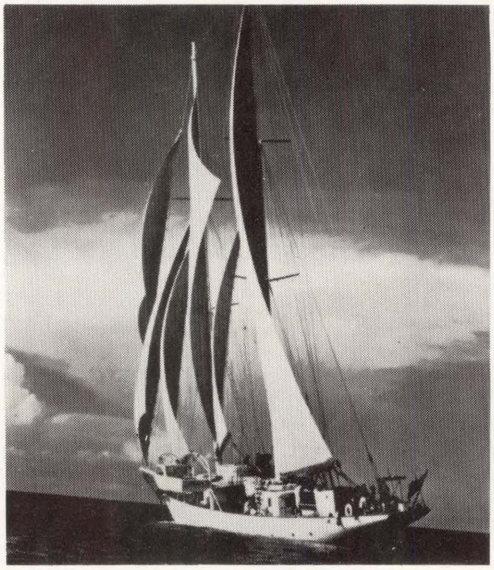
For once in your life...live.

A sleek graceful sailing vessel glides across the sometimes green, sometimes blue Caribbean. The cargo: you. And an intimate group of lively, fun-loving shipmates.

Uniform of the day: Shorts and tee shirts. Or your bikini if you want. And bare feet.

Mission: A leisurely cruise to remote islands with names like Martinique, Grenada, Antigua—those are the ones you've heard of. Before the cruise ends, you'll know the names of many more. You'll know intimitely the enchanting different mood of each...and its own beauty and charm.





Life aboard your big sailing yacht is informal Relaxed. Romantic.

There's good food. And 'grog'. And a few pleasant comforts... but any resemblance to a plush pretentious resort hotel is accidental.

Spend 6 days exploring paradise. Spend six nights watching the moon rise and getting to know interesting people. It could be the most meaningful experience of your life ...and it's easily the best vacation you've had.

A cruise is forming now. Your share from $400.Write Cap'n Mike for your free adventure booklet in full color.

Come on and live.

Windjammer 'Barefoot' Cruises
Post Office Box 120.
Miami Beach, Florida 33139
305/373-2090

For Reservations
Call Toll Free
1-800-327-2600.

Windjammer Cruises.

Name ____________________

Address ____________________

City ____________ State ____________ Zip ____________

Phone ____________________

P.O. Box 120, Dept. Miami Beach, Florida 33139

CIRCLE 127 ON INQUIRY CARD

IP8500...MORE IMAGERY, MORE FEATURES, LESS COST

DeAnza's new IP8500 image processing and display system introduces a new concept in imagery . . . more for less

It just may be the most powerful system you've seen.

It has 16 memory controllers handling an unprecedented capacity of up to 16 512x512x8 bit image memories. Its array processor easily handles 8 and 16 bit data with 32 bit results including real-time multipliers with 8 bit inputs and 16 bit outputs.

The IP8500 has up to four independent output channels with split screen capability, multiple look-up tables and 8 bit DACs for 256 levels of intensity for each primary color on a RGB color monitor or three separate mono monitors. It also provides high speed warp and rotation with anti-aliasing of a 512x512x8 bit image for warp/-distortion correction or image manipulation.

Features also include independent integer zoom of 2:1, 3:1, 4:1, 5:1, 6:1, 7:1, 8:1; pan feedback intensity translation tables, four independent alphanumeric overlays and dual cursor generators as well as high speed vector and special function generators.

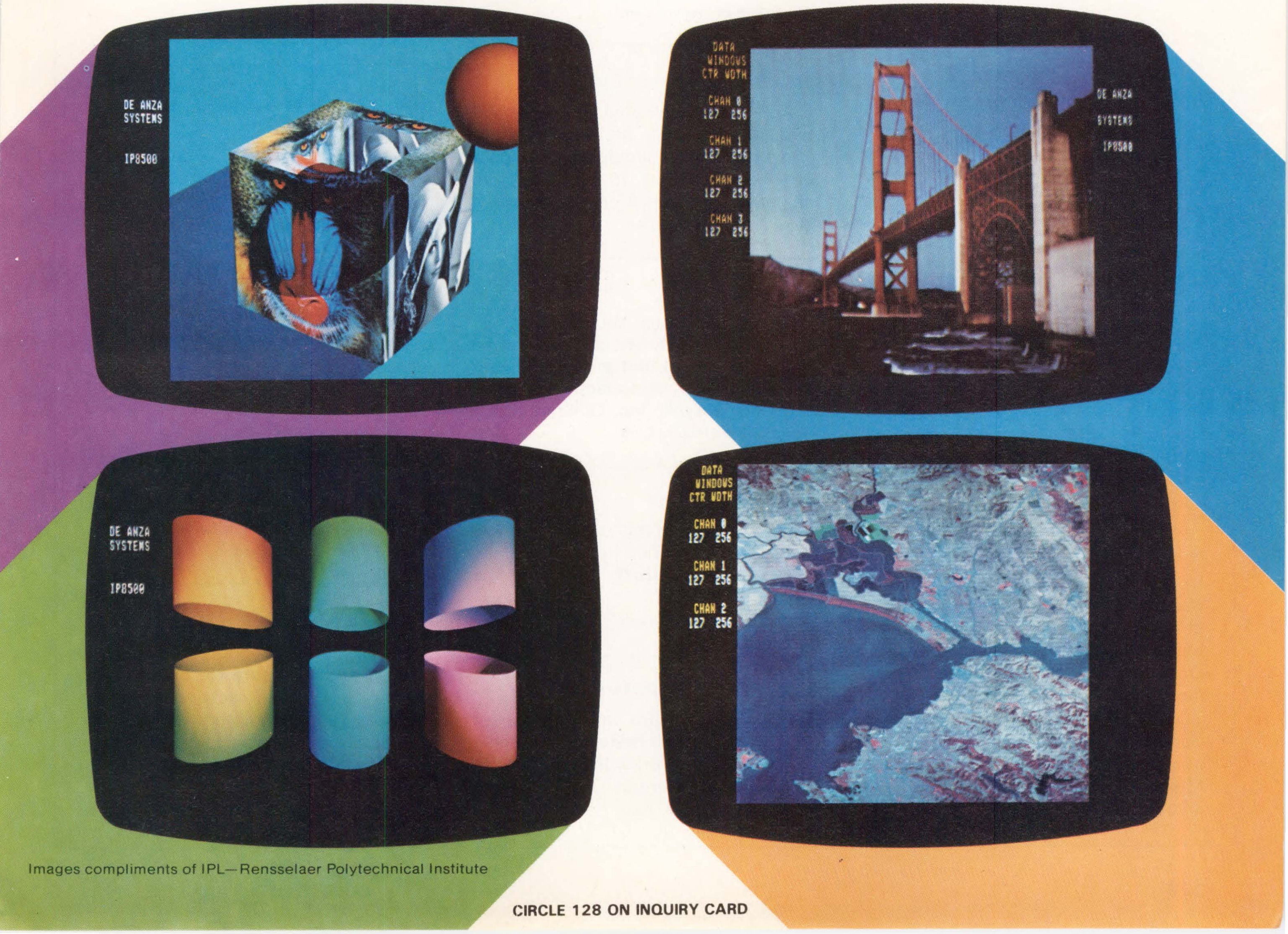
If you're responsible for LANDSAT analysis, NDT, process control synthesis, remote sensing, three-dimensional computer graphics or other image processing and analysis applications which call for single or multi-station high resolution color, multi-image mono or pseudo color displays, find out more about the new DeAnza IP8500.

Call or write today and find out why more is suddenly less.

De Anza Systems Incorporated

CORPORATE HEADQUARTERS: 118 Charcot Avenue, San Jose, CA 95131, (408) 263-7155, TWX: (910) 338-7656
REGIONAL OFFICES: 100 First Ave., N.E., Suite 114G, Cedar Rapids, IA 52401, (319) 364-1366 • 3918 Prosperity Ave., Suite 204, Fairfax, VA 22031, (703) 698-0600 • 500K Middle Country Road, Middle Island, New York 11953, (516) 736-3440

GIVE YOURSELF A BETTER IMAGE



Images compliments of IPL—Rensselaer Polytechnical Institute

CIRCLE 128 ON INQUIRY CARD

LITERATURE

Fiber Optic Cables

Series 2200, 2210, 2260, 2261, and 2270 are covered in catalog that includes spec sheets with cross-sections, physical dimensions, and optical power and attenuation charts. **Belden Corp,** Geneva, Ill.

Circle 300 on Inquiry Card

Connectors and Terminals

Catalog describes and illustrates wire, cable, panel, and component interconnection devices. **Berg Electronics Div, Du Pont Co,** New Cumberland, Pa.

Circle 301 on Inquiry Card

Statistical Multiplexers

Diagrams illustrating typical ring, hubbing, and satellite networks are included, along with specs and photos, in brochure detailing DCX836 and -840. **Rixon Inc,** Silver Spring, Md.

Circle 302 on Inquiry Card

Microcomputer Software

Brochure describes system software available for LSI-11/2 and -11/23, and RT-11 development operating system and its execute-only subset, RT^2. **Digital Equipment Corp,** Northboro, Mass.

Circle 303 on Inquiry Card

Computer Graphics Reference

Pocket-sized, 40-p ***Glossary of Computer Graphics Terms*** can be obtained by writing on company letterhead or by submitting business card with request to Marketing Dept, **Megatek Corp,** 3931 Sorrento Valley Blvd, San Diego, CA 92121.

Ada Reference

Dept of Defense ***Reference Manual for the Ada Programming Language,*** stock no 008-000-00354-8, is available for $5.50 from Superintendent of Documents, U.S. Government Printing Office, Dept 50, Washington, DC 20402. Send check, money order, or Superintendent of Documents deposit account number, or pay by Visa or Master Card, giving account number and expiration date.

Variable Resistive Devices

Guide to trimmers, precision potentiometers, and panel controls includes charts showing rating systems and performance parameters, and drawings of typical applications. **Variable Resistive Components Inst,** Evanston, Ill.

Circle 304 on Inquiry Card

Axial Fans

Performance data, dimensions, and illustrations of typical connections for Brutes, Demi Brutes, and Mini Brutes are provided in bulletin. **Gould Inc,** Watertown, NY.

Circle 305 on Inquiry Card

Standardized Fiber Optic System

HDC Interface is defined in brochure that contains information on materials, performance data, outline dimensions, and termination tooling. **ITT Cannon Electric,** Santa Ana, Calif.

Circle 306 on Inquiry Card

Low Insertion Force Connectors

Catalog describes physical, electrical, and mechanical parameters, and shows PC board, circular, and modular connectors with 1 to 320 contacts. **Hypertronics Corp,** Concord, Mass.

Circle 307 on Inquiry Card

DIP Switches

Catalog describes rocker, side actuated, double-throw, and front panel mount versions, and provides dimensions, circuitry, and electrical characteristics. **Grayhill, Inc,** La Grange, Ill.

Circle 308 on Inquiry Card

Solid State Relays

Catalog gives specs and extensive, detailed application data for new users. **Magnecraft Electric Co,** Chicago, Ill.

Circle 309 on Inquiry Card

Line Voltage Regulators

Description of Ultra Line high performance units, their features, and selection guide are provided in bulletin. **Cyberex, Inc,** Mentor, Ohio.

Circle 310 on Inquiry Card

EMI Filters

Supplied by data sheet are performance characteristics, physical specs, schematics, and reference guide for STE series. Stanford Applied Engineering, Inc, Santa Clara, Calif.

Circle 311 on Inquiry Card

Multiparameter Data Acquisition System

Photos and specs are shown in brochure that details features and capabilities of series 88. **Canberra Industries, Inc,** Meriden, Conn.

Circle 312 on Inquiry Card

Computer Cables and Interfaces

Catalog describes specs for EIA RS-232 and -449 assemblies; accessories include ribbon, coaxial kits, switching boxes, and plenum and molded assemblies. **Computer Cable Products Div, Vertex Electronics, Inc,** Farmingdale, NY.

Circle 313 on Inquiry Card

Microprocessor Based Programmable Controller

Brochure for EPTAK^{R} 700 includes specs, application information, and description of hardware, I/O modules, power supply, programming terminals, and software languages. **Eagle Signal Industrial Systems,** Davenport, Iowa.

Circle 314 on Inquiry Card

Subminiature Toggle and Pushbutton Switches

Photos, switching functions, specs, and actual size mechanical outlines, as well as selection and cross-reference guides, are found in catalog. **American Switch Corp,** Wakefield, Mass.

Circle 315 on Inquiry Card

IC Sockets, Contactors, Carriers

Catalog contains photos, drawings, specs, and test data for burn-in/test, production, and screw machine sockets, and contactors and carriers for flatpack, quad-pack, TO-5, and DIP devices. **Wells Electronics, Inc,** South Bend, Ind.

Circle 316 on Inquiry Card

Want high performance raster graphics?

Sanders Associates' new Graphic 8 offers you up to 256 simultaneous colors. High resolution. Dynamic operation with double-buffered refresh memory...

Plus upward-instruction compatibility with the Sanders stroke refresh Graphic 7 and its color and 3D options.

But there's more.

Both display systems – Graphic 7 and Graphic 8 – bring you built-in test, FORTRAN support, remote or local operation, interfaces to most computers, and other important user-oriented features.

Sanders' stroke refresh Graphic 7 and new raster Graphic 8 display systems: they put the best of both worlds at your fingertips. For more information, write or phone Sanders Associates, Inc.,
Information Products Division,
Daniel Webster Highway South,
Nashua, NH 03061. 603-885-5280.

The Graphics People
SANDERS

See us at NCGA Booth 520

CIRCLE 129 ON INQUIRY CARD

I'll probably come down the hall to see you.

"I like to tell anyone who has done a good job that I know it and appreciate it. As far as I'm concerned, being the President doesn't mean a big office with a closed door. It's not private dining rooms and splendid isolation.

"You see, I know success at ITT DCD is its people. Our most important asset is our people; the computers, the facilities–whatever else we have or buy–nothing works right without the right people. And when you find them you have to challenge them, then reward them when they meet the challenges.

"People work for recognition. OK, I know what you're going to say. It's the money they're after and the praise is only icing on the cake. But believe me, you can't buy loyalty. You can pay people for their talent... but you can't buy them.

"I really appreciate a special effort. And if you do something innovative, notable, different–I'm going to get up, go and see you, tell you what I feel. We've put millions into independent research this year, because we believe you should back original thought. As far as I'm concerned, today's bright idea is tomorrow's profit. You can't get any simpler than that! Corporate success is a collective success, and it's my job to build a better team.

"For me it was alway ITT. It was my first significant exposure to industry. I guess I'm a good example of the fact that staying can work for you. From a Project Engineer to President in 14 years. Yes, you're looking for a long term commitment and what it can do for you.

"And it looks like I'm here to stay–who would leave a life like this. I've got a wonderful house in Morris County, NJ. There I am, just 1 hour from Broadway, and I still have wild deer wandering across my lawn. A great place to bring up children–that wonderful mix of rural fantasy and Big Apple culture.

"Success? You could call it that. But success is just setting a goal and reaching it. Satisfaction is finding yourself exactly where you want to be."

If you want to align your career with a company that looks for ideas and backs them all the way to reality, consider ITT DCD. We have openings for degreed engineering/scientific professionals at all levels of experience in the following areas:

COMMAND & CONTROL COMMUNICATIONS
MESSAGE / CIRCUIT SWITCHING
VOICE / SIGNAL PROCESSING

- **Hardware Systems Design**
- **Software Systems Design**
- **Systems Analysis • Programming**

ITT DCD offers excellent salaries and a comprehensive benefits package that would be difficult to duplicate. Beyond medical, dental and life, we offer a superior system of educational support which encourages acquisition of credits and advanced degrees on our time at our expense. Relocation is another area of extraordinary effort on ITT DCD's part. We ease your move by coordinating all phases through our in-house relocation specialist. Please call or send resume to our Director of Professional Personnel.

Where engineers never stop learning

ITT DEFENSE COMMUNICATIONS DIVISION

An equal opportunity employer M/F

(800) 526-6292,(201) 284-2551

492 River Road, Nutley, New Jersey 07110

CIRCLE 143 ON INQUIRY CARD

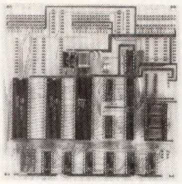
COMPUTER DESIGN System Showcase

MB 85 MICROCOMPUTER SYSTEM ...

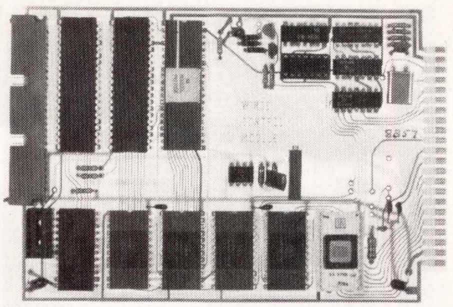
. . . offers the Multibus user a unique systems capability. Integrated into the system are: 12" CRT, full ASCII keyboard, 5MHz 8085 CPU, 64K RAM, and dual 8" floppy disk drives providing up to 2 million bytes of mass storage. Expansion capability is provided by the 9 slot Multibus card cage featuring 200 watts of usable power. Options include IBM compatible mag tape, hard disk drives, analog and digital I/O, printers, PROM programmers, and mini-floppies. The system comes complete with the CP/M operating system (Version 2.2) and a choice of high-level languages and proven application packages. Application assistance available. **COMARK CORPORATION,** 257 Crescent St., Waltham, MA 02154. (617) 894-7000.

CIRCLE 525

THE AE-85 SINGLE CARD COMPUTER FOR DEDICATED CONTROL



Based on an 8085 MPU the AE-85, fully expanded, has two crystal controlled timer/counters, 1536 bytes of RAM, 44 programmable bidirectional I/O pins, up to 4k of EPROM (accepts a 2708/16/32), and provisions for 190 wire wrap pins for the placement of various sockets and connectors. Also, on-board jumper definable logic allows the combining of different interrupt requests from the I/O ports and timer/counters so as to make effective use of the 4 hardware interrupts. These features make the AE-85 ideal for low cost dedicated applications. From $179.00 in singles. Call today for more information. **ADROIT ELECTRONICS, INC.,** 5 East Long Street, Suite 1012, Columbus, Ohio 43215. Phone: (614)221-3060 **CIRCLE 526**

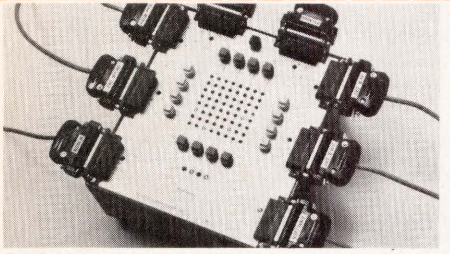


$94.20 SINGLE BOARD COMPUTER*

6800 MPU, serial I/O, parallel I/O, RAM, EROM, 44-pin 4½" x 6½" PCB.

EXPANSION MODULES

RAM, ROM, CMOS RAM/battery, analog I/O, serial I/O, parallel I/O, counter/timer, 488 GPIB, EROM programmer, power fail detect/power on reset. *100 piece price, model MCL11. **WINTEK CORP.,** 1801 South Street, Lafayette, IN 47904; 317-742-8428. **CIRCLE 527**



RS232 DATA SWITCHING MATRIX

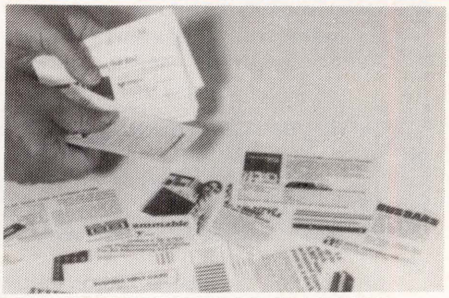
- Implements every possible connection between Tx Data and Rcvd Data for eight I/O ports.
- Manual Control and connection monitoring via built in key array and 8 x 8 LED display.
- Non-volatile memory for 16 connection arrangements.
- 20 ma, RS232, or TTL may be mixed.
- Remote selection via parallel TTL interface.

$995 (1-4, USA only), **DIGITAL LABORATORIES,**600 Pleasant St., Watertown, MA 02172. (617)924-1680.

CIRCLE 528

HEWLETT PACKARD 9845B/C & 9835A BINARY UTILITY PROGRAMS

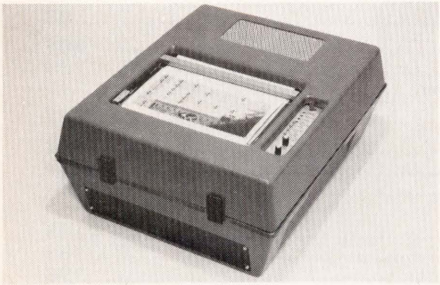
Binary programs to enhance program editing capabilities and provide new keyboard commands are now available. ● **SEARCH & REPLACE** Provides a program-global facility to change names of labels, functions, variables and subprograms on BASIC programs in memory. ● **SYMBOL FINDER** Searches BASIC program for identifiers and reports defining line number and all occurrences. ● **MEMORY MAPPER** Prints memory map to help programmers write BASIC programs which execute faster and use less memory. ● **CROSS REFERENCE** An invaluable aid in preparing documentation. Produces a cross reference table to show all identifiers and line numbers where they occur. ● **DUMP ALPHA** Copies the CRT display to the internal printer or an external hardcopy device. ● **COMMENT STRIPPER** Removes comments from BASIC programs to reduce memory requirements and improve execution speed. ● **OEMSEC** Enciphers BASIC programs to prevent listing, tracing or interrogation of program variables. Insures that algorithms and trade secrets embodied in programs remain secure. ● **NODUP** Prevents duplication of the program media. Works with tape, floppy, or hard disc based systems. **STRUCTURED SOFTWARE SYSTEMS, INC.,** Box 1072, Irick Road, Mt. Holly, NJ 08060. (609)267-1616 **CIRCLE 529**



LOW COST POSTCARD MAILINGS

Here's a way for your company to test new product acceptance, offer catalogs, find new applications, or support ongoing product lines. Computer Design's POSTAL MAILERS go to our 70,000 domestic subscribers 4 times each year. Rates start at $895 per card and go down with frequency. Next closing June 22, 1981.

Contact Maureen Sebastian, **COMPUTER DESIGN,** 11 Goldsmith St. Littleton, MA 01460. (617)486-8944. **CIRCLE 530**

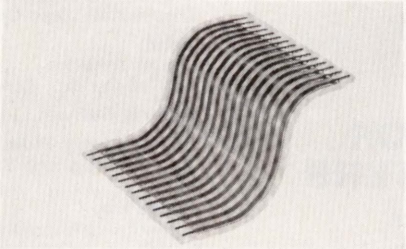


GRAY SCALE PRINTER

Remarkable gray scale resolution! Great detail! The CEC® 912 Gray Scale Printer offers 16 true gray scale steps. 200 picture elements per inch, hor. & vert. (or 40,000 per sq. in.)! High speed printouts on inexpensive paper. Archival quality. Unaffected by ambient conditions. Call Cliff Haber, (213) 796-9381 Ext. 2575.

BELL & HOWELL CEC DIV. 360 Sierra Madre Villa, Pasadena, CA 91109.

CIRCLE 531

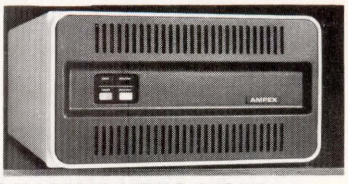


JUMPERS FROM STOCK

Sculptured ™ jumpers with strong, rigid, integral fingers. Thin and highly flexible conductors for maximum bending with least stress.

Save by soldering fingers directly into PCB, or plug into any commercial socket.

Lengths 0.5" to 8.0"; many center spacings; fingers 25 mils wide, 10 mils thick. All jumpers ready from stock. Also Sculptured interconnects for rotary and toggle switches. **ADVANCED CIRCUIT TECHNOLOGY, INC.** 118 Northeastern Blvd., Nashua, NH 03061 Tel: (603) 880-6000. **CIRCLE 532**



AMPEX EMULATING DISKS FOR DEC & DG

More capability for less money is one great reason to take a closer look at Ampex emulating disks.

Our Constellation Series emulating storage disk controllers offer DEC and Data General compatibility with the advantage of buying an independent disk drive.

Ampex disk subsystems offer important advantages in price/performance and a full line to support your subsystem requirements.

For all the facts, write Gary Owen, **AMPEX CORPORATION,** Memory Products Division, 200 N Nash Street, El Segundo, CA 90245, or call (213)640-0150. **CIRCLE 533**

TERMINALS FROM TRANSNET

PURCHASE PLAN • 12-24 MONTH FULL OWNERSHIP PLAN • 36 MONTH LEASE PLAN

	DESCRIPTION	PURCHASE PRICE	PER MONTH 12 MOS.	PER MONTH 24 MOS.	PER MONTH 36 MOS.
DEC	LA36DECwriter II	$1,095	$105	$ 58	$ 40
	LA34 DECwriter IV	995	95	53	36
	LA34 DECwriter IV Forms Ctrl.	1,095	105	58	40
	LA120 DECwriter III KSR	2,295	220	122	83
	LA120 DECwriter III RO	2,095	200	112	75
	VT100 CRT DECscope	1,595	153	85	58
	VT132 CRT DECscope	1,995	190	106	72
TEXAS INSTRUMENTS	TI745 Portable Terminal	1,595	153	85	58
	TI765 Bubble Memory Terminal	2,595	249	138	93
	TI Insight 10 Terminal	945	90	53	34
	TI785 Portable KSR, 120 CPS	2,395	230	128	86
	TI787 Portable KSR, 120 CPS	2,845	273	152	102
	TI810 RO Printer	1,895	182	102	69
	TI820 KSR Printer	2,195	211	117	80
DATAMEDIA	DT80/1 CRT Terminal	1,695	162	90	61
	DT80/5 APL CRT	2,095	200	112	75
	DT80/5L APL 15″ CRT	2,295	220	122	83
LEAR SIEGLER	ADM3A CRT Terminal	875	84	47	32
	ADM31CRT Terminal	1,450	139	78	53
	ADM42 CRT Terminal	2,195	211	117	79
HAZELTINE	1420 CRT Terminal	945	91	51	34
	1500 CRT Terminal	1,095	105	58	40
	1552 CRT Terminal	1,295	125	70	48
TELEVIDEO	920 CRT Terminal	895	86	48	32
	950 CRT Terminal	1,075	103	57	39
NEC SPINWRITER	Letter Quality, 55/15 RO	2,895	278	154	104
	Letter Quality, 55/25 KSR	3,295	316	175	119
QUME	Letter Quality KSR, 55 CPS	3,395	326	181	123
	Letter Quality RO, 55 CPS	2,895	278	154	104
HEWLETT PACKARD	2621A CRT Terminal	1,595	153	85	58
	2621P CRT Terminal	2,750	263	154	99
CENTRONICS	730 Desk Top Printer	715	69	39	26
	737 W/P Desk Top Printer	895	86	48	32

FULL OWNERSHIP AFTER 12 OR 24 MONTHS • 10% PURCHASE OPTION AFTER 36 MONTHS

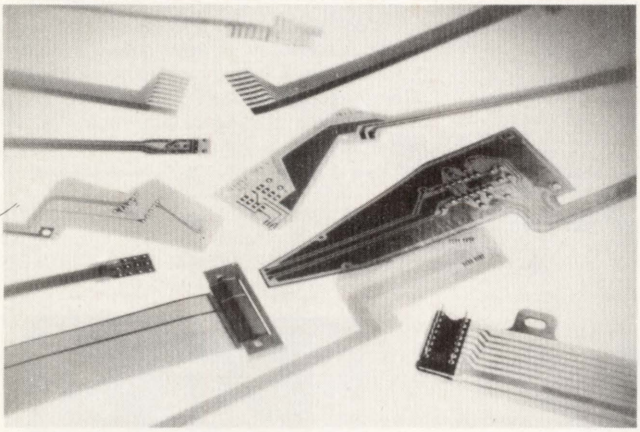
MICROCOMPUTERS—APPLE, COMMODORE, HP85, DEC LSI

ACCESSORIES AND PERIPHERAL EQUIPMENT

ACOUSTIC COUPLERS • MODEMS • THERMAL PAPER • RIBBONS • INTERFACE MODULES • FLOPPY DISK UNITS

TRANSNET CORPORATION
1945 ROUTE 22 • UNION, N.J. 07083 • (201) 688-7800
TWX 710-985-5485

CIRCLE 130 ON INQUIRY CARD



FLEX CIRCUITS FOR DISK DRIVES, PRINTERS

- Single and double-sided designs
- Reduce assembly costs, inspection time
- Reduce interconnect weight and volume
- Improve wiring accuracy and circuit performance

From design to volume production, quality flexible circuitry from Buckbee-Mears Company

BUCKBEE-MEARS COMPANY bmc
Precision Components Group
NASHUA DIVISION
100 NORTHEASTERN BLVD.
NASHUA, NEW HAMPSHIRE 03060
(603) 883-5541

CIRCLE 131 ON INQUIRY CARD

ADVERTISERS' INDEX

RESEARCH REPORT

MINI/MICRO
PERIPHERAL MARKETS

- Presents an overview of the mini/micro peripheral market, with an in-depth look at the significant issues concerning marketing, distribution and positioning of several mini/micro market segments for the business and household community.
- Defines current and expected future role of key-to-storage devices, portable dial-up terminals, card reading equipment, on-line terminals, optical character recognition and optical mark recognition equipment, with a look at user preference.
- Discusses the evolution of the mini/micro line printer, teleprinter and character printer markets, with an analysis of the relationship between microcomputer systems and "Intelligent" copier/printer devices.
- Reviews the state-of-the-art in memory and storage products including fixed and floppy discs, storage module drives and tape drives, with an evaluation of CRT's, data communications equipment and graphic systems.
- Ten-year forecasts, and a review of current and expected future strategies of several dozen leading suppliers.
- 208 pages, 59 exhibits; published January 1981; price $985.00.

For free descriptive literature and a detailed table of contents, contact:

INTERNATIONAL RESOURCE
DEVELOPMENT INC.

30 High Street
Norwalk, CT 06851 USA
Phone (203) 866-6914
WU Telex 64-3452

ird

CIRCLE 133 ON INQUIRY CARD

New BODINE
Stepper Catalog
Eases Application

- 1.8° stepper motors in 23, 34 & 42 frames
- Modular CMOS Controls
- Entire line U.L. Recognized
- 75 years of Bodine Quality

Catalog, motors and controls available from Bodine distributors or write today.

BODINE
ELECTRIC
COMPANY

2500 West Bradley Place
Chicago, 60618 USA
Telephone 312-478-3515
Telex 25-3646

CIRCLE 137 ON INQUIRY CARD

CD* SALES OFFICES

HOME OFFICE

Director of Marketing
Gene Pritchard

Direct Marketing Sales Mgr
Maureen Sebastian

Classified Advertising Mgr
John G. French

11 Goldsmith St.
Littleton, MA 01640
(617) 486-8944

NEW ENGLAND AND UPSTATE NEW YORK

Regional Sales Manager
Carol E. Fountain
11 Goldsmith St.
Littleton, MA 01460
(617) 486-8944

MIDDLE ATLANTIC STATES, LONG ISLAND AND SOUTHEASTERN STATES

DICK BUSCH, INC
Richard V. Busch
6 Douglass Dr., R.D. #4
Princeton, N.J. 08540
(201) 329-2424

MIDWESTERN STATES AND COLORADO

BERRY CONNER
ASSOCIATES
Berry Conner, Jr.
88 West Schiller St.
Suite 2208
Chicago, IL 60610
(312) 266-0008

WESTERN STATES AND TEXAS

BUCKLEY/BORIS
ASSOC., INC.
Terry Buckley
Tom Boris
John Sabo
22136 Clarendon St.
Woodland Hills, CA 91367
(213) 999-5721
(714) 957-2552
Terry Buckley
Barbara Arnold
P.O. Box 278
Campbell, CA 95009
(408) 866-8735
(213) 999-5721

*(TM)

The CØMPLØT® Series 7000 Digitizers Provide

An Extra Menu Area

The entire active area is surrounded by a 1.0″ menu area

Prices start at $2,950*

Now you don't need a separate pad for menus

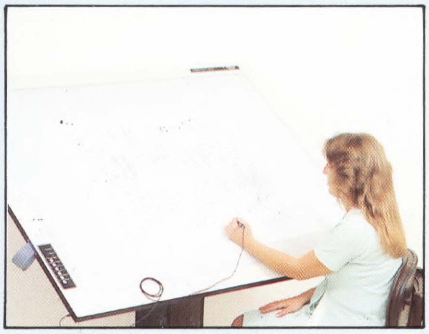
With the Series 7000 transluscent (at no extra expense, of course) digitizers, you get a full active area, 12″x12″, 17″x24″, 36″x48″ or 42″x60″, plus a border area especially designed for user-defined menus. Again, no additional expense.

And the innovative design concepts don't stop there. Imagine 40 user configuration controls and host computer down loads allowing you to tailor your digitizer to your specific application. Point, stream, switch stream and incremental modes, fixed or relocatable origins — of course.

Also — separate stylus/cursor plugs are located on each side of the digitizer for ease of operation for left and right-handed people. Power-tilt stands (with or without back lighting) are available for maximum flexibility and operator comfort.

Circle 134 For Literature.

What about this combination in one digitizer? Accuracy of ±0.005″ right up to the edge of the active area — up to 200 coordinate pairs per second digitizing rate. Resolution as fine as .001″ !!!



The Series 7000 digitizers give some additional blessings — no grid adjustment, no demagnetizing (biasing), no problem with temperature or humidity over the broad range of operating conditions — EVER.

Circle 135 to Have a Representative Call.

One might say the menu is matched by a complete digitizing meal . . . the Houston way.

We know these wonders have tempted your appetite, but CØMPLØT® Series 7000 digitizers have additional features that may intrigue you even more.

Get the complete story. Contact Houston Instrument, One Houston Square, Austin, Texas 78753. (512) 837-2820. For rush literature requests, outside Texas, call toll free, 1-800-531-5205. For technical information, ask for operator #6.

houston instrument
GRAPHICS DIVISION OF
BAUSCH & LOMB

* U.S. suggested retail price. OEM prices available.
® Registered trademark of Houston Instrument.
• Tested for FCC rules and regulations, Class A.

What's so special about Pro-Log's new 4 MHz Z80A card?

You can't tell by specs alone.

It's not just the state-of-the-art 4 MHz clock rate that makes our new 7804 STD BUS card something special.

It's not just the on-board counter/timer with four cascadable channels.

Or the byte-wide memory that allows mapping and strapping in any combination up to 8K bytes of RAM and 32K bytes of ROM and PROM, or up to 65K bytes with the companion 7704 memory card.

Dynamic RAM refresh, power-on reset, bi-directional address and control bus for DMA . . . all are features you can get from other STD BUS card manufacturers.

What's extraordinary is the quality.

Our new Z80A CPU card is built by Pro-Log—the people who designed the STD BUS concept.

Like every one of our STD 7000 series cards, this Z80A CPU card is built with proven, industry-standard parts. All components are 100% tested and burned-in. It's designed to work reliably with all of our STD BUS interface and I/O cards, and to keep on working and working in the field.

We're so proud of our high quality that we back it with a one-year parts and labor warranty.

That's why our customers ask us to build STD BUS cards they could get somewhere else. Because no one builds cards with Pro-Log's attention to quality and reliability.

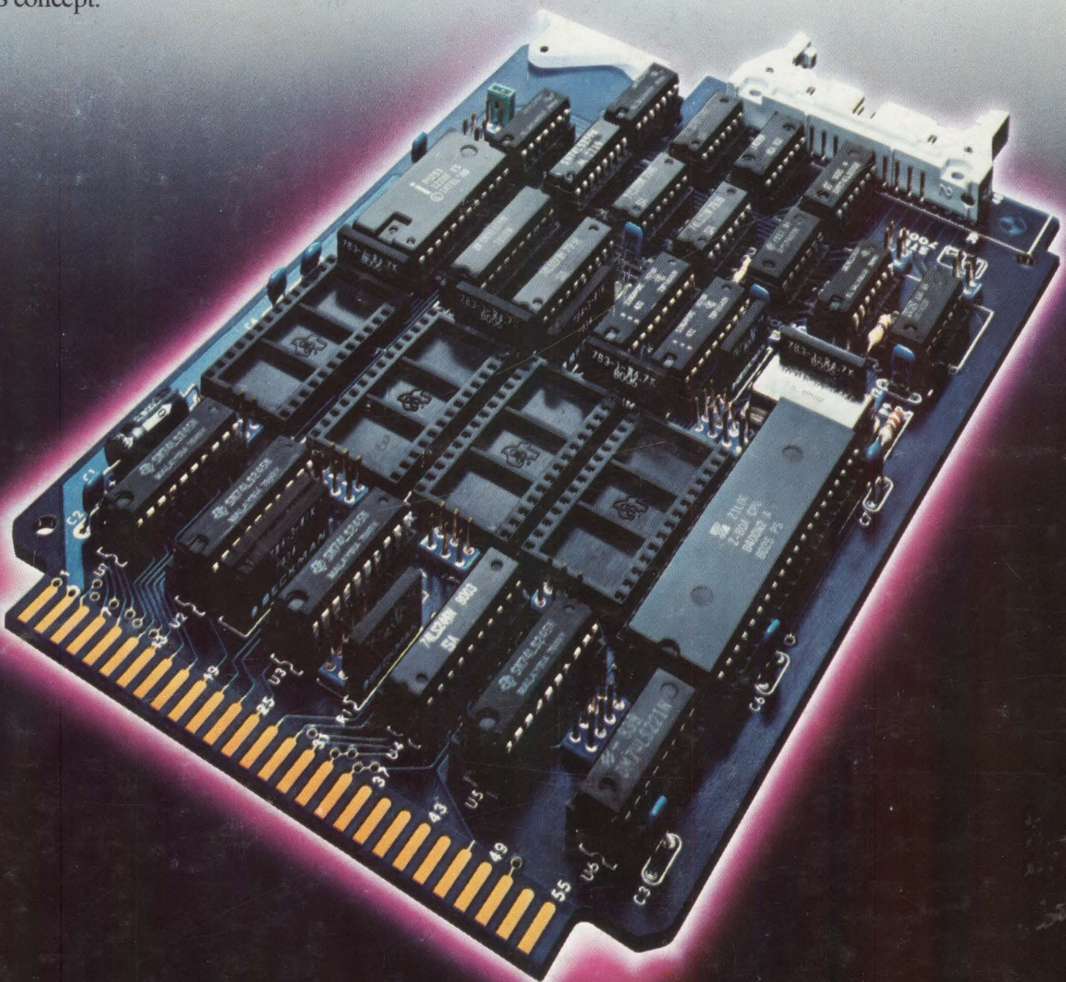
Ask our customers.

Find out what our customers say about using Pro-Log STD 7000 cards. Write or call for our STD BUS applications brochure, plus technical data on our new 7804 CPU card, its companion 7704 memory card, and our full line of STD BUS products.

Pro-Log Corporation, 2411 Garden Road, Monterey, CA 93940, phone (408) 372-4593.

STD BUS

PRO-LOG CORPORATION



CIRCLE 136 ON INQUIRY CARD