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COMPUTER APRIL 1981 DESIGN THE MAGAZINE OF COMPUTER BASED SYSTEMS

OPTIMIZING MICROPROCESSOR INPUT/OUTPUT TECHNIQUES INTEGRATED ARITHMETIC PROCESSING UNIT ENHANCES MICROPROCESSOR EXECUTION TIMES AUTOMATED NETWORK SYNTHESIZER COMPACTS VLSI DESIGN



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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN®

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THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

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OPTIMIZING MICROPROCESSOR INPUT/OUTPUT TECHNIQUES

by Lynn E. Costlow

Microprocessor based systems frequently offer a choice of I/O methods. Analysis of 12 fundamental I/O techniques identifies cost and performance trade-offs and helps in the design of the most efficient hardware and software interface

INTEGRATED ARITHMETIC PROCESSING UNIT ENHANCES PROCESSOR EXECUTION TIMES

by E. B. Croson, F. H. Carlin, and J. A. Howard

Arithmetic processing unit enhances microprocessor computation, increases speed, and reduces program overhead when integrated system design treats floating point software development as a natural extension of hardware interfacing

AUTOMATED NETWORK SYNTHESIZER COMPACTS VLSI DESIGN

by J. Robert Logan

VLSI design technique encodes functional requirements in numeric form and applies standard data reduction methods to realize greater compaction than techniques that accept schematic diagrams as input

DESIGN APPROACH TRIMS ONE-SHOT PROPAGATION DELAY by Vardhman Tatia

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CONFERENCES

MAY 4-7-NCC (National Computer Conf), McCormick Place, Chicago, III. IN-FORMATION: Gerard Chiffriller, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/558-3600

MAY 5-8—PICA '81 (Power Industry Computer Applications), Marriott Motor Inn, Philadelphia, Pa. INFORMATION: T. A. Suman, Philadelphia Electric Co, 2301 Market St, N3-1, Philadelphia, PA 19101. Tel: 215/841-6397

MAY 11-13-Electronic Components Conf, Colony Square Hotel, Atlanta, Ga. INFORMATION: T. G. Graw, Bell Laboratories, Whippany Rd, Rm 3B-312, Whippany, NJ 07981. Tel: 201/386-3000

MAY 12-14—Internat'I Sym on Computer Architecture, Minneapolis, Minn. INFOR-MATION: Harry Hayman, Computer Architecture, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MÁY 18-21-Spring DECUS (Digital Equipment Computer Users Soc) U.S. Sym, Miami Beach, Fla. INFORMATION: Paula Morin, DECUS, One Iron Way, MR2-3/E55, Marlboro, MA 01752

MAY 20-22—MIMICOME (Internat'I Sym on Mini- and Microcomputers in Control and Measurement), Hilton Hotel, San Francisco, Calif. INFORMATION: P. L. Hsu, McDonnell Douglas Astronautics Co, 5301 Bolsa Ave, Huntington Beach, CA 92647. Tel: 714/896-3311

MAY 27-29-Internat'l Sym on Multiple Valued Logic, Oklahoma City, Okla. IN-FORMATION: Dr S. C. Lee, School of Electrical Engineering & Computer Science, U of Oklahoma, 202 W Boyd, Rm 219, Norman, OK 73019. Tel: 405/325-4721

JUNE 1-4—Sym on Incremental Motion Control Systems and Devices, Hyatt Regency Hotel O'Hare, Rosemont, III. IN-FORMATION: Dr B. C. Kuo, PO Box 2772, Station A, Champaign, IL 61820. Tel: 217/356-1523 or 217/333-4341

JUNE 9-11-Data '81 Datacomm Conf and Exhibition, Winnipeg, Manitoba, Canada. INFORMATION: Laurie Whitsed, 55 Bloor St West, Toronto, Ontario M4W 3K2, Canada

JUNE 10-12-CONPAR '81 (Conf on Analyzing Problem-Classes and Programming for Parallel Computing), Nurnberg, West Germany. INFORMATION: Wolfgang Handler, Immd, Universitat Erlangen-Nurnberg, Martensstrasse 3, D-8520 Erlangen, West Germany JUNE 14-18-Second Annual NCGA Conf, Baltimore Convention Center, Baltimore, Md. INFORMATION: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

JUNE 23-25-COMDEX/Spring '81, Madison Square Garden and New York Statler Hilton, New York, NY. INFORMA-TION: Peter B. Young, The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

JUNE 29-July 1-Design Automation Conf, Opryland Hotel, Nashville, Tenn. IN-FORMATION: Harry Hayman, Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

AUG 18-21-VLSI (Very Large Scale Integration) '81 Internat'l Conf, University of Edinburgh, Edinburgh, Scotland. INFOR-MATION: Secretariat, VLSI '81 Internat'l Conf, 26 Albany St, Edinburgh EH1 3QH, Scotland

AUG 24-28-IFAC (Internat'l Federation for Automatic Control) World Congress, Kyoto, Japan. INFORMATION: IFAC '81 Secretariat, Kinki Hatsumei Ctr, 14 Kawahara-cho, Yoshida, Sakyo-ku, Kyoto 606, Japan

SEMINARS

MAY 11-13-SNA: The Blueprint for IBM's Telecommunications Future; AND Managing the Data Base Environment; MAY 13-15 AND MAY 20-22-The IBM 4300 Series, AND JUNE 1-3-Local Network Architecture; AND Strategies for Distributed Computing, various U.S. cities. INFORMATION: Technology Transfer Inst, 741 10th St, Santa Monica, CA 90403. Tel: 213/394-8305

MAY 16-Introduction to Pascal; AND JUNE 6-Distributed Processing, Princeton, NJ. INFORMATION: Bill Hafstad, EDUCOM, PO Box 364, Princeton, NJ 08540. Tel: 201/457-4055

JUNE 1-2—Microprocessors: Hardware, Software, and Applications, Worcester Polytechnic Inst, Worcester, Mass. INFOR-MATION: Ginny Bazarian, Office of Continuing Education, Worcester Polytechnic Inst, Worcester, MA 01609. Tel: 617/753-1411, X517

JUNE 8-11-ATE Seminar/Exhibit, Hynes Auditorium, Boston, Mass. INFORMA-TION: Test Conferences Registrar, Benwill Publishing Corp, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/ 232-5470 JUNE 9-11–Understanding and Using Computer Graphics, Chicago, III. INFOR-MATION: Bob Sanzo, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038 Tel: 212/233-1080

AUG 15-17-Distributed Computer Control Systems, Beijing (Peking), China. IN-FORMATION: Prof Liu-Shi-hua, Chinese Assoc of Automation, Research Inst of Electronic Technic Application, PO Box 927, Beijing, China

AUG 31-SEPT 1-Real Time Programming, Kyoto, Japan. INFORMATION: 1981 IFAC/IFIP Workshop on Real Time Programming Org Committee, c/o Prof T. Hasegawa, Dept of Applied Mathematics and Physics, Faculty of Engineering, Kyoto University, Kyoto 606, Japan

SHORT COURSES

MAY 4-5-Basic Elements of Digital Systems; MAY 6-8-Principles and Applications of Digital Devices in Monitor and Control Systems; MAY 13-14-Microprocessors in Control Systems; AND MAY 28-29 AND JUNE 11-12-Computer Process Control Strategies, Research Triangle Park, NC; Minneapolis, Minn; or Wilmington, Del. INFORMATION: Instrument Soc of America, Administrator, Continuing Education, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

JUNE 8-12-Machine Vision, Automatic Assembly, and Productivity Technology, Massachusetts Inst of Technology, Cambridge, Mass. INFORMATION: Director of Summer Session, Rm E19-356, MIT, Cambridge, MA 02139

JUNE 29-JULY 10-Microcomputer System Design, University of Ireland, Dublin, Ireland. INFORMATION: Dr D. P. McCarthy, Dept of Computer Science, Engineering School, Trinity College, Dublin 2, Ireland

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COMMUNICATION CHANNEL

Clock Recovery, Power Sequencing, and Deadman Timer **Modules for High Speed RF Modems in Local Bus Networks**

P. E. Wagner and D. G. Willard The MITRE Corporation Bedford, MA 01730

A bit clock recovery module that can be used to regenerate receive timing information from level transitions in recovered data in a modem demodulator was developed specifically for the 1M-bit/s radio frequency (rf) data bus modem described previously.* The module is equally adaptable to other modem designs. A separate module also provides two other functions that are critical to an rf modem intended

*D. G. Willard and P. E. Wagner, "RF Modem Design for Broadband Coaxial Local Area Networks," Computer Design, Aug 1980, pp 14-22

for high speed timeshared common channel applications. One function is the proper sequencing of supply voltages to eliminate extraneous transmissions that can be caused by different decay and charge times among the different voltage supplies. The other function is to prohibit abnormally long transmissions that could degrade the common channel traffic throughput. The clock regeneration module will be described first, followed by the power sequencer and watchdog timer module.

Clock Recovery Module

The timing recovery and reclocking circuit associated with a modem demodulator is illustrated in Fig 1. In the diagram, U1 provides a reset function to the clock divide-down chip U3 for each negative to positive transition of recovered data. U3 restarts its ripple through countdown after one-half clock period of the XN clock. When the N of the divider is selected to match the N of the times N supplied clock, positive transitions of the times 1 clock occur in the center of the recovered data bits. The properly phased times 1 clock is used by U4B to sample and reclock the recovered data to produce receive data. The circuit provides an option of generating locally the times N clock. The diagram includes an optional divide-by-N (U5) to provide an unphased times 1 clock for transmission purposes.

The recovered active high key signal is also reclocked by the rephased times 1 clock signal and made available as receive key. The recovered key also forces U1 to lock in a fixed state, inhibiting clock rephasing during periods of no reception.

(continued on page 18)



Fig 1 Timing recovery module. U1 uses data transitions to reset U3 divide-down to produce properly phased receive clock. U4 reclocks recovered data and key

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Fig 2 Power sequence and timeout module. Modulator enable line is pulled low when 5-V supply dips below 4 V or transmit key stays enabled for extended period

Power Sequencer and Timeout Module

The power sequencing and timeout circuit of a modem intended for multiple-subscriber bus applications is shown in Fig 2. The left side of the circuit removes power from the modulator when the 5-Vdc line falls below approximately 4 Vdc, as might happen during a power-down sequence. In many applications driving logic external to the modem passes through an unpredictable state during power-down, which can present an active transmit key level prior to the full removal of the 12-Vdc voltage. This condi-

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tion will cause the modem to emit a burst of carrier, that in turn will interfere with other bus traffic.

Because of the reference provided by the zener diode, the "A" section of the voltage comparator is held in the high output state as long as the 5-V line is greater than approximately 4 V. Whenever the voltage falls below the reference, the output will clamp the key control line low through R1, removing the enabling voltage from the rf modulator.

To prohibit any excessively long transmissions that might be attempted by external driving circuits, the right side of the circuit provides the transmit period override function for the modulator. Clearly, abnormally long transmissions would create havoc in a timeshared single-channel bus, and are prohibited by this simple circuit.

The active low transmit key input lead is monitored by the 2N3904 keeping the inverting input of the "B" section of the voltage comparator low during nontransmit periods. During each transmit period the inverting input charges toward 12 V as a function of the resistive-capacitive (RC) time constant. When the transmission duration is sufficiently long, this voltage exceeds the noninverting reference, causing the key control voltage to be pulled low, and disabling the rf modulator. Each transmission is controlled independently because the capacitor is discharged when the transmit key goes high at the end of each transmission.

Through an oversight, the address of one of the authors of last month's Communication Channel column was omitted. The byline should have read: J. Michael Kryskow, Gould Modicon, Haverhill St, Andover, MA 01810, and C. Kenneth Miller, Concord Data Systems, Inc, 430 Marrett Rd, Lexington, MA 02173.

Please rate the value of this article by circling the appropriate number in the "Comments" box on the Inquiry Card.

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EFX 050T-2	50W	+ 5V	6A	± 15V	± 1.0A	+24V	0.2A	7.25" x 5.00" x 2.00"
EFX 100T-1	100W	+ 5V	8A	± 12V	± 2.0A	+ 24V	0.5A	9.50" x 5.00" x 2.00"
EFX 100T-2	100W	+ 5V	8A	± 15V	± 1.6A	+24V	0.5A	9.50" x 5.00" x 2.00"
EFX 150T-1	150W	+ 5V	15A	± 12V	± 2.5A	+24V	1.0A	13.40" x 5.00" x 2.52"
EFX 150T-2	150W	+ 5V	15A	± 15V	± 2.0A	+24V	1.0A	13.40" x 5.00" x 2.52"
EFX 210T-1	210W	+ 5V	20A	± 12V	± 4.0A	+24V	1.0A	15.00" x 5.00" x 2.52"
EFX 210T-2	210W	+ 5V	20A	± 15V	± 3.0A	+24V	1.0A	15.00" x 5.00" x 2.52"

⁽¹⁾ There are two auxiliary outputs for plus and minus voltage.

⁽²⁾ Consult factory for other tertiary outputs between 5V and 24V.

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CIRCLE 14 ON INQUIRY CARD

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Computerized Telephone System Integrates Voice and Data Switching



Fig 1 Data terminal interface module. Front panel toggle switch originates call, disconnects call in progress, or manually answers incoming call. Six LEDs indicate power and DTI and data signal status. Switch mounted at rear of unit is used for testing and for switching to automatic answer mode A data communications feature has been added to its computerized business telephone system (CBX) line by Rolm Telecommunications, 4900 Old Ironsides Dr, Santa Clara, CA 95050. The new feature, using an interface to 3-pair telephone wiring and a data communications software package (Release 7), allows simultaneous switching of both voice and asynchronous data between terminals, computers, and transmission facilities.

The data communications feature can be added to any new or existing CBX installation by adding a data terminal interface (DTI), data line interface (DLI), and the Release 7 software package.

DTI desktop module allows transmission of asynchronous data over telephone wiring at 110 to 19,200 bits/s over distances up to 5000 ft (1524 m) from the CBX. It has a standard RS-232-C interface, operates in originate/answer mode, and can be connected to virtually any asynchronous terminal, computer, modem, or multiplexer port. The DTI emulates the full duplex 103/212 line signaling protocol to the terminal and connects to the CBX via a modular connector and two telephone twisted pairs. The DTI measures 12.5 x 6.75 x 2.5" (31.8 x 17.1 x 6.4 cm) and will fit under a standard telephone handset (Fig 1). It weighs 2.75 lb (1.25 kg) and requires 8 W at 115 Vac.

The DLI consists of two PC boards that are mounted inside the CBX. Each DLI supports 16 separate channels, each of which can operate at its own data rate independently of the others. Speeds, codes, and types of connected equipment may be mixed. The DLI interfaces and controls full duplex data communications to the time division multiplexer (TDM) bus for switching by the CBX.

The TDM control card expands the traffic carrying capacity of the system by *(continued on page 22)*



Fig 2 Typical CBX configuration with data communications feature. Three modems are shared by six local devices. When on-site users enter number of remote resource desired, software automatically searches for available modem and trunk line. Remote devices with modems as shown can connect to on-site devices by dialing number assigned to modem pool, and CBX will hunt for free modem

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- Controller Card with RL01 Instruction Set Compatibility

tems, CRDS systems are based on the DEC LSI-11/2 or LSI-11/23, with from 32K to 128K words of MOS memory. Peripherals available include a 21 megabyte Winchester fixed disk system; single- or double-sided floppy disk drives; and a 3M cartridge tape back-up for the Winchester disk. Software systems available include RT-11, RSX-11, and U/V6 (UNIX*).

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providing data submultiplexing. The CBX digital switch assigns two time slots to the digitized voice connection for the duration of a call. Since data rates are generally much lower than voice, in the order of 9600 bits/s or less, Release 7 software can submultiplex time slots to handle as many as 40 2400-bit/s data connections through a single pair of time slots-or 20 connections at 4800 bits/s, 10 at 9600, 5 at 19,200, or any combination, provided the product is less than 96k bits/s. In this way data communications are integrated with the voice switching system without compromising voice system performance.

Off-site data communications are handled by pooled modems (Fig 2) that are shared among users and are automatically allocated by the CBX as needed. Trunk lines for both voice and data are also shared to eliminate the need for separate trunks dedicated to data calls only, and no separate wiring for data terminals is required. A route optimization feature automatically selects the most economical outbound circuit for both voice and data. This can be WATS, DDD, FX, or tieline, among others. On-site communications require no modems at terminals or CPU.

Applications for the data communications feature include program development, timesharing, word processor communications, data entry, inquiry/ response, message switching, and minicomputer-based systems. First deliveries are anticipated in the summer of 1981.

Circle 487 on Inquiry Card

Additions to Series/1 Computer Systems Improve Communications Functions

Enhancements to its Series/1 computer that are designed to improve communications and networking functions have been announced by IBM General Systems Div, PO Box C-1645, Atlanta, GA 30301. The new features include two processors, a family of matrix printers, direct access 1/O devices, a local communication controller that supports multiple Series/1s in a cluster or ring configuration, and system software.

The new processors are designed to support networking environments. 4952 model c has up to 128k bytes of main storage and comes with a single or dual integrated diskette drive. The drive uses one- or two-sided dual density diskettes with up to 1.2M bytes per drive. Total capacity can be 2.4M bytes using an optional second drive. The 4952 model C provides economical low entry design for systems used in distributed data processing environments, as systems within a communications network, or for standalone applications. The 4955 model F processor doubles the Series/1 main storage to 512k bytes, allowing more active terminals on the system. Software support for the 4955 includes realtime programming system version 5, event driven executive version 3, and control program support.

The printers can be attached locally up to 4000 ft (1219 m) from the system, instead of being limited to 150 ft (46 m) as with earlier printers, or they can be remotely attached. Print speeds are 40-char/s correspondence quality or 160-char/s draft quality printing. Two *(continued on page 26)*

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printer models can be switched from draft to correspondence quality printing via Series/1 software.

The local communication controller is designed for high speed data communications between two or more Series/1 processors. As many as 16 processors can be attached in a ringconfigured link without requiring a master controlling station. Transmission speeds up to 2M bits/s can be realized. Systems can communicate using a peer to peer full duplex protocol to access common files, data, or other resources. Each station can direct messages to any other connected to the ring and can selectively broadcast to any or all of the units on the ring by means of userwritten programs. Circle 488 on Inquiry Card



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Bit error measurement system BERTS-325C includes MS-302 clock source, MN-302 transmitter, MB-302 receiver, and mainframe that contains dc supplies and cooling fans for modules, and comprises a complete modular test set for BER measurements up to 325 MHz. A product of Tau-Tron Inc, 27 Industrial Ave, Chelmsford, MA 01824, the instrument generates both pseudorandom and fixed 16-bit words for stimulating the system under test and measures the bit by bit errors as they are received from the system. BER on total errors on continuous data can be measured, or on burst data for such applications as TDMA testing.

The clock source generates the system clock signal from 1 kHz to 325 MHz, continuously adjustable over seven ranges. Specific test frequencies can be optionally provided by up to three crystal-controlled oscillators. Clock output is a 1-V signal suitable for driving the MN-302 transmitter.

The transmitter provides a choice of $2^7 - 1$, $2^{15} - 1$, $2^{20} - 1$, or $2^{23} - 1$ pseudorandom test patterns, and four different 16-bit words including alternating one-zero. Errors can be injected internally at a rate of 2 errors every 100 bits or at an externally controlled rate. Data output is selectable NRZ or RZ. A second data output, true or complemented, and delayed by 8 bits is also provided, as well as separate clock and sync outputs.

The receiver automatically selects and synchronizes on the reference pattern being received, or it can be set for manual reference selection and synchronization. It provides four different measurements, each with selectable display times of 1 s, 10 s, or hold. One measurement counts and displays total errors up to 6 digits plus overflow. Two

(continued on page 31)

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measurements display error rate, one with and one without auto range selection, of 10^{-2} through 10^{-9} . The fourth test measures input clock frequency in MHz with 1-kHz resolution. Data are also available at a rear panel connector for data logging.

Power requirement is $115 \pm 10\%$ or $230 \pm 10\%$ Vac, 48 to 66 Hz, 240 VA. Dimensions of the benchmount aluminum case are 9.5 x 17.75 x 17.9" (24.1 x 45.1 x 45.5 cm). Rack mount adapters are available. Net weight is 47 lb (21 kg). A GPIB (IEEE-488) interface is available as an option for automated test applications.

Circle 489 on Inquiry Card

Broadband Local Network System Handles Medium and High Speed Devices

High speed broadband-based System 40 LocalNetTM cuts CPU overhead and achieves throughput of more than 1M bits/s, according to Network Resources Corp, subsidiary of Sytek, Inc, 1153 Bordeaux Dr, Sunnyvale, CA 94086. The system connects a variety of medium and high speed devices to network nodes or adapters supporting mainframes and minicomputers typically attached to CPUS.

The resulting network can include host and support processors, mass memories, high speed work stations, RJE stations, multiple low speed frontend peripheral networks, and gateways to remote network facilities, all over broadband coaxial cable that can support 300 to 400-MHz communications bandwidth.

The system is implemented with 16-bit microprocessor architecture and 16-bit wide data paths, and is a companion to the company's System 20 introduced last year (*Computer Design*, Nov 1980, p 82) that provides communications capability for low throughput devices. Both systems are fully interconnective and can coexist on the same cable. Both are based on carrier sense multiple access/collision detection (CSMA/CD) access techniques.

The systems provide transparent protocol implementation and such services as packet assembly/disassembly, buffering, virtual circuit control management, error and flow control, protocol and code conversion, speed matching, and

(continued on page 33)

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This is 3M's HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

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Of course, the use of

microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which need updating. And fast random access, which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its \$32.50 high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.

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COMM CHANNEL

data security. Both systems coexist with other broadband facilities and can share the same cable with point to point systems, inhouse video, and voice communications. Attachment to the cable is via standard F-type fittings that do not affect system operation when a device is connected or disconnected.

Keys to system operation are LocalNet layered architecture and the network adapter unit (NAU) that connects user devices to the network and supplies distributed intelligence to the system. The architecture allows network intelligence to be applied on a regular schedule in order to phase in additional functions and facilities as required.

The NAU is a standalone 16-bit microprocessor controlled packet communications unit (PCU) based on paralleled Intel 8086/8089s with 64k-byte memory and DMA or channel I/O. It accesses the broadband medium through a software controlled frequency-agile transceiver that can handle five program selected 156-MHz offset full duplex channels with 2-MHz separation. Carrier synthesis is by program controlled phaselocked loop circuitry. Transceiver transmit frequency range is 40 to 70 MHz and receive range is 196.25 to 226.25 MHz. A variety of host interfaces can be accommodated. First system NAUS will provide a Unibus adapter for DEC VAX- and PDP-11 series; standard NAUS will be compatible with the Intel Multibus.

Other network components include System 40 Bridge standalone packet mode device that connects up to four channels; 40/20 Bridge for a logical bridge between low and high speed networks that includes speed matching and flexible concentrator/multiplexer services; and T-verter central transmission unit that simultaneously supports transmit/receive functions for both systems.

The CSMA/CD mechanism used for the system has an effective 2M-bit/s capacity even at high loads. The NAU, after protocol processing, can still achieve 1M-bit/s throughput while total average access time is typically about 10 ms.

Capacity per NAU is 128 simultaneous virtual circuits, and the system can accommodate multiple adapters running on as many as 5 channels. The broadband distribution system is a mid-split single or dual 75- Ω CATV cable using star, tree, or hub topologies. Circle 502 on Inquiry Card

Modular Modem Line Has Interchangeable Data Pumps, Interfaces

A novel approach to the mechanical configuration of modem functions in which the modulator/demodulator, line interface, and options are mounted on single interchangeable modules is a feature of the Advanced Intelligent Modem Series recently introduced by Timplex, Inc, One Communications Plaza, Rochelle Park, NJ 07662. The modems, developed at the company's Transmission Products Div based in Largo, Fla, come in three models that operate at primary speeds of 9600, 4800, and 2400 bits/s respectively.

Each of the three versions consists of a data pump, modulator/demodulator, and interface to the communications link and data terminal equipment (DTE). The CCITT-compatible data pump modules operate synchronously over 4-wire 3002 unconditioned leased voiceband channels.

The 9600-bit/s series has switchselectable fallback rates of 7200 and 4800 bits/s. The modem automatically drops back to half speed if signal quality deteriorates. Fallback rates of the 4800 series and 2400 series are 2400 and 1200 bits/s respectively.

The interface module contains all interfaces to communications lines and DTE. Standard interface is RS-232/V.24 compatible; RS-449 and MIL-STD-188-114 interfaces are available. Changes or future updates in the communications interface require the replacement of a single module rather than an entire modem (Fig 1).



Fig 1 Data pump/line interface arrangement. Each modem is designed with data pump (left) and interface/power supply on separate plug-together cards that occupy single card slot. Modem and controls may be changed from front panel by plugging new modem into interface module. Interface may be changed from back of card shelf by plugging new interface module into modem

(continued on page 34)



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COMM CHANNEL

Among the options are a 4-channel bandsplitter (9600 series) and a 2-channel splitter for both the 9600 and 4800 series. Options available to all models include an asynchronous to synchronous converter module and an async to sync converter that has automatic error detection and correction. The async to sync converter provides for operation of asynchronous remote terminals normally limited to the 1200-bit/s ceiling on async transmissions to be operated at up to 9600 bits/s. A full CRT 1920-char screen update is available in about 2 s, rather than in 10 to 15 s, the typical update time without the converter.

With the error control option, which also includes async to sync converter capability, the modem checks asynchronous format transmissions for errors. Upon detection of an error, an automatic request for retransmission (ARQ) causes the message to be retransmitted from the modem buffer, without the terminal operator being aware of the action taken.

Standard internal diagnostics in the series include local and remote analog and digital tests, using the data terminal equipment to control and provide the test data. Tests can also be run from the modem front panel using the self-test function to provide the data.

In a card cage configuration, up to 16 modems, in any speed combination, can be mounted in 10.5" (26.7-cm) vertical rack space (Fig 2). Table top models with integral power supplies are also available. The units require 20 W at 105 to 125 or 210 to 250 Vac, 47 to 63 Hz.



Fig 2 Rack mount card shelf configuration. Up to 16 modems can be accommodated in 10.5" (26.7-cm) vertical space. Modems occupy single PC card slots and are both electrically and mechanically interchangeable

Concurrently with the introduction of the modem series, the company announced the availability of interface control equipment as a component of interface management that will integrate its entire product line into complete turnkey private data networks tailored to individual customer needs. See at NCC Booth 3409

Circle 503 on Inquiry Card

X.25 Program Product Provides Additional Capabilities for IBM Series/1 Users

The x.25 communications package for IBM Series/1 users provided by Systar Corp, 1762 Technology Dr, Suite 208, San Jose, CA 95110, now includes support for the EDX operating system and also for the HDLC mode of x.25 framing. The software product allows attachment of the Series/1 to public data networks such as GTE-Telenet and Tymnet, as well as to point to point communications lines using the standard x.25 protocol.

Provided by the package is a user interface that has a set of subroutines called from user programs written in the EDL programming language for the Series/1. The subroutines permit users to initiate calls to remote sites, receive incoming calls, send and receive data, and clear calls. Levels 1, 2, and 3 of the X.25 standard, as well as packet assembly/ disassembly (PAD) functions, are implemented.

The system uses a small 4952A to act as a frontend processor (FEP) to the EDX system, supporting up to 20 simultaneous X.25 virtual circuits, and interfacing at speeds to 56k bits/s. Up to three EDX systems may be connected to the FEP via a high speed transmission link. The FEP may also be configured to support the company's Message/1 electronic mail system announced late last year.

The HDLC framing mode is supported in addition to the previously supported Bisync framing. The package permits simultaneous connection to multiple packet networks using any combination of the HDLC or Bisync framing procedures.

An encryption option provides improved security in data transmission between Series/1 systems. Enabling this option encrypts all data sent on the x.25 connection using a customer-specified 32-bit key.

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better. Even the cost is a lot better. You'll save *at least* 10% compared with what you're now paying for low-speed modems.

23/

The only way for you to know just how great our LSI Modem Modules are, is to have one for yourself.

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AMP means productivity.



TECHNOLOGY REVIEW

Distributed Data Processing System Doubles Memory Capacity and Throughput

Model 585, the most powerful of a family of distributed processing systems, offers up to twice the memory capacity and throughput capability of its predecessor, the 445. As a cost-effective solution in medium-size environments, it allows a combination of up to 16 data stations and printers to be attached to one processor, provides total disc storage capacity of 342M chars/system, and offers ability to locate data stations and printers up to 5000 ' (1524 m) from the processor.

In the system, Northern Telecom Inc, Data Park, PO Box 1222, Minneapolis, MN 55440, has used a multipleprocessor architecture to increase system efficiency. The main processor can be configured with from 128k to 512k char of main memory. Other processors are used in each peripheral controller, freeing the main processor to carry on its primary function of processing data.

The system's controller has a built-in 8" (20-cm) Winchester disc storage unit and uses a 0.25" (0.64-cm) 15M-char cartridge tape for program loading and software backup. The disc unit has a rated MTBF of more than 10,000 hours, requires no preventive maintenance, and has an average access time of 30 or 35 ms, depending on the number of platters used. Reliability is derived from a proprietary embedded servo and simple design. The closed loop servo provides precise read/write head positioning while it increases the tolerance needed for platter alignment. The intelligent servo positioner records head positioning information among the data on both surfaces of the platters, which allows both sides to be used for data storage. The unit's rotary actuator positions the head/arm assembly over data surfaces using the embedded information.

Each disc unit incorporates either two or three platters, and is driven by a direct drive ac motor. This design allows capacities of 11M or 22M bytes of formatted data/unit. Two units fit into a controller cabinet, to make a total internal capacity of 44M bytes/controller.

Housed in a desktop unit, the system's 2000-char data station incorporates a 15" (38-cm) screen. A remote data station and a remote printer may be used to

communicate with a system over telephone lines, so that smaller offices can use the system at low cost. The local Sprinter printer, a bidirectional, microprocessor controlled matrix printer, operates at 180 chars/s; remote printers operate at 72 or 144 chars/s. 300- and 600-line/min printers may also be used. Other optional peripherals include cassette, diskette, high capacity disc, and magnetic tape drives for data interchange and storage.

The unit's operating system can handle up to 32 COBOL and TAL 2000 tasks in any combination. (TAL 2000 is a proprietary language designed specifically for data entry programming). Word processing capability is obtained with the Omniword package.

Disc spooling, standard with the operating system, eliminates bottlenecks in peripheral devices and enables the entire data processing operation to flow smoothly. This permits multiple data stations to efficiently share a single printer or multiple printers. Job streaming also contributes to efficiency. With job streaming, a sequence of job steps can run automatically; job initiation keying errors are virtually eliminated because job steps are keyed only once.

Model 585 connects to the company's other systems through Omnilink, a resource sharing feature that allows disc files on any system in a network to be accessed by any other authorized system in the network. This link also permits systems to share peripherals such as magnetic tape drives, printers, and modems. Up to nine systems can share resources through this coaxial cable network arrangement.

Dual IBM 3270 emulators enhance communications by permitting interactive communications with two mainframe computers concurrently. IBM 3270 passthrough applications are also supported. Asynchronous, bisynchronous, and synchronous data link control transmission modes are offered at speeds up to 9600 bits/s. Communications programs include interactive remote job entry, batch transmission using IBM protocols, multileaving workstation support, and the company's network control system. Circle 505 on Inquiry Card

Small Business System Uses Multiple-Microprocessor Architecture for Expandability

SB700, a multi-user small business computer system, employs an advanced multiple-microprocessor architecture to achieve modular expandability, ease of use, and compatibility with existing software. Developed by Symcro Systems, Inc, 200 Office Ctr, 275 Commerce Dr, Fort Washington, PA 19034, the system can serve from 2 to 24 or more simultaneous users at individual keyboard or display workstations.

Multiple Zilog Z80 microprocessors within the system operate under control of proprietary Modular System Logic (MSL) software, which performs the system management functions required for multi-user operation. In addition, the CP/M software monitor, normally incorporated in the MSL, enables users to benefit from applications software written for use on Z80 based computers running under CP/M. At the same time, the system's architecture permits system expansion in building block fashion.

The basic system consists of four Z80 based processor modules (each having 65,536 bytes of memory), 10M-byte fixed disc drive, industry compatible 8" (20-cm) diskette drive, two keyboard/ display workstations, 150-char/s printer, and all operating software. Two of the four processor modules are normally allocated to user applications, while the other two are normally used for peripheral control and system management functions.

The central unit, housing the processor modules, fixed disc, and diskette drive, is a compact cabinet that requires no special air conditioning or power supply. Only three different types of circuit boards are used in the system. Each board has software checks and indicator lights to aid in fault diagnosis.

Additional workstations and processor modules, as well as printers and disc storage units, can be added at any time without replacing existing hardware or software. A system can include from 2 to 24 or more workstations, from 1 to 24 or more printers, and from 10M to 300M bytes of fixed disc storage.

There is no master software operating system in the conventional sense. A part (continued on page 42)

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TECH REVIEW

of the modular system logic software resides in each processor module, and performs module to module communication, task scheduling, resource allocation, file management, input/output handling, security, system services, and workstation operator commands. Workstation commands are tutorial in nature and are controlled by sequences of multiple-choice menus, thus making the system easy to operate with minimum training.

System resources are allocated dynamically, and one or more application processor modules are normally allocated to each active workstation. Flexible foreground/background processing capability permits two or more tasks to run simultaneously under the control of any workstation. As a result, any program that runs under CP/M can be initiated from a workstation and instructed to run in the background, freeing the workstation for an independent foreground activity.

Circle 506 on Inquiry Card

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Drum Plotter and Raster/Vector Controllers Cut Graphics Hard Copy Costs

Costs of electrostatic and pen plotting are reduced with controllers capable of generating graphics hard copy on both types, and by a 54" (137-cm) wide drum plotter that serves as an alternative to wider, more expensive units. California Computer Products, Inc, 2411 W La-Palma Ave, Anaheim, CA 92801, has introduced these units in response to needs articulated by users in computer aided design and manufacturing applications.

The vector to raster units provide one common controller for applications in which both electrostatic and pen plotters



Aimed at CAD/CAM users, model 1060, a 54" wide 4-pen plotter from Calcomp, provides alternative to users who previously had to acquire larger, more expensive unit to attain 54" width

are usually required. The ability to use a single controller can substantially reduce costs by eliminating the need for separate raster and vector processors as well as eliminating the need for both raster and vector data types for any given plot.

Both microprocessor based systems perform many functions previously assigned to the user's host system. The most significant is the conversion of the vector information describing the plot into the raster representation required by the electrostatic plotter. Since vector to raster conversion is performed on the controller, host computer time is significantly reduced over that required by raster systems and most competing vector processsors.

Model 953 is an offline/online controller that accepts the company's 921/925 tapes as well as online 907 format random vectors input across asynchronous and bisynchronous data lines. Both electrostatic and pen units with this controller can be driven either locally or remotely. The units feature an operator control panel designed to simplify creation of canned sequence and graphics manipulations, such as scaling, mirroring, windowing, rotation in 1-degree increments, selection of multiple EPP line widths or alternate pens, merging selected layers of a plot, or production of a negative image EPP plot. It can select any of eight electrostatic plotters or one pen plotter and can generate multiple copies of a selected plot.

System components include a microprocessor with 256k bytes of vector memory, operator control display, magnetic tape drive, and plot data processing, vector memory, vector to raster conversion, and raster output modules. Provision for megabytes of rigid disc memory or an additional 256k bytes of semiconductor memory supports complex plotting requirements while enhancing productivity and throughput.

For users who need only online capability, model 951 accepts the company's random vector plot data via an RS-232-C or bisynchronous serial interface. This controller's control panel allows users to perform graphic manipulations such as scaling, mirroring, rotation in 90° increments, clipping, or selection of plot strips. The user can select any of eight electrostatic plotter/ printers or one pen plotter, and can generate multiple copies of a selected plot. The unit comes with 256k bytes of vector memory, operator control panel, plot data processing, vector memory, vector to raster conversion, and raster output modules. Options include an additional 256k bytes of semiconductor memory and a 21M-byte rigid disc memory.

Combining the space saving features of a drum plotter with the performance of large flatbeds, the 1060 drum plotter has a drawing speed of 30 in/s (76 cm/s), uses linear pen actuation for the fast pen up/down times, and has an acceleration rate of 2G that allows the plotter to reach maximum speed in 0.04 s. Resolution is 0.0005''(0.127 mm).

With four program selectable pens, the unit accepts four media types. Continuous roll plotting is provided up to 120' (36 m; 60' or 18 m for mylar). Operator controlled speed and acceleration permit high plot quality to be obtained for pressurized ball point, liquid ink, nylon tip, and liquid ball pens. Circle 507 on Inquiry Card

The new data comm tester that obsoletes all others. ARC's INTERVIEW[®] 4500 Interactive Test System.

Now a total solution to problems encountered in data communications networks. ARC's new INTERVIEW 4500 Interactive Test System. Featuring a new concept in portable test equipment design that simplifies diagnostics of data comm problems and reduces the most complex testing to a few simple operations. **Three units in one.** The 4500 is an emulator, programmable monitor and high speed bulk recorder. Fully emulates CPU, terminal and node. And simplifies network performance measurements.

Special capabilities to emulate packet protocols and SNA. Seven codes are standard.

The first graphic display that guides the operator in entering timing relationships between data and interface leads.

B INTERVIEW 45

Self documented tapes allow user to build library of diagnostic tests. Unit records data and all test parameters, providing a record of system problems with the test that found the problem.

Selective recording of specific terminal, controller and logical channel eliminates time spent reviewing unrelated data. Reliable 72 Kbps recording is provided by a one megabit high speed bulk memory (optional).

Easy to understand code converted keyboard and self-teaching menus dramatically reduce training time. Easiest to use interactive tester. Unique triggers automatically locate problems by simultaneously looking for up to 16 test conditions. Significantly reducing time required locating problems in the network. Developing a test is no more complicated than responding

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CIRCLE 30 ON INQUIRY CARD

Introducing the Winchester for systems that are going places.



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In desktop systems, the requirements for portable disk storage are really getting tough. But no matter how you measure them, Shugart is setting industry standards with the SA600. Standards for reliability. For price/performance. And for manufacturing know-how and service.

Take reliability. With power off, the SA600's special design features protect it, so movement is no problem. Its automatic spindlelactuator arm lock and head shipping zone safeguard both heads and media. And its sealed bubble, with only the media and head/arm assembly under it, reduces contamination potential.

Then during operation, other innovative design features assure the SA600 will keep on working accurately. Features like microprocessor-controlled head positioning and electronic damping. And our Fasflex IV™rotary band actuator and extra large diameter capstan, which eliminate premature band stress.

But reliability isn't the whole story. Consider, too, the importance of getting exactly the price/performance you need. Again, Shugart sets the standard. With 3.33; 6.66; and 10-megabyte versions to choose from, now you can get the lowest cost per megabyte for your application.

Even more important is our experience in manufacturing and service. We know the needs of the portable, desktop system market, because we've been producing the Minifloppy™ and other low-cost disk drives for over seven years. And we offer the industry's most extensive testing, applications engineering, documentation, and service support including our exclusive, world-wide, underthe-bubble repair service.

So if you have a disk-based product that's going places, start with the Shugart SA600 – the industry standard. For further information

or a demonstration of the SA600, contact Shugart Associates, 475 Oakmead Parkway, Sunnyvale, CA 94086 (408) 733-0100.

Minimum moving parts under the bubble. SA600 with SA410!460 Minifloppy™ backup: a match for the '80s.



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Performance Tester Handles Digital LSI/VLSI Semiconductor Components

A general purpose, high speed performance tester of digital LSI/VLSI semiconductor components, the GR16 is based on an architecture that provides added levels of speed and precision with 10 times the throughput of existing systems. The power and versatility of the system make it useful in engineering characterization as well as production test of such devices as LSI/VLSI microprocessors, microcomputers, and their support chips, and for static and dynamic RAMS.

Key features of the system, developed by GenRad Semiconductor Test, Inc, 300 Baker Ave, Concord, MA 01742, include test rates up to 40 MHz, resolution of 125 ps, timing accuracy of less than 1 ns, and analog accuracy of 0.1%. High pin count is achieved by using one or two test heads, with up to 144 pins each. In addition, the unit offers parallel test capability for simultaneous static functional and parametric testing on two test heads, and an optional host computer interface via GRnetTM, an automatic test equipment data communications network, for high speed uploading and downloading of programs and data files. Fully automated self-calibration and self-diagnostics include a summary report of calibration values and printed circuit board level fault isolation, for low maintenance and repair costs.

The dual-bus architecture provides effective modularity by board, cabinet, pin channel, and dc power. Subsystems are partitioned into functionally integral elements and channels with direct high speed lines of communication. A range of options allows the system to be configured as a fully equipped engineering evaluation system or as a high throughput production tester. A minimum of discrete wiring is used, for ease of maintenance and flexible system expansion. The unit interfaces easily with handlers and probers.

When systems are configured as part of the GRnet, up to four program files can be transferred simultaneously at a data rate of 655k bits/s. The network interface contains its own microcomputer and presents no overhead to the main CPU when no files are being transmitted; it also allows for self diagnostics. Optional host/network arrangements are not essential to testing (enabling standalone operation), but each system in a network configuration can be set up for



Dual-bus architecture of GenRad's GR16 VLSI test system partitions subsystems into functionally integral elements and channels with direct high speed communication capability. Operational segments are computer system, functional test system, test head assemblies, and user interface system

testing, program development, and data analysis and reporting.

The computing system's CPU is a standard PDP-11/34 operating under the DEC RSX-11M operating system, configured with 128k words of MOS memory. The CPU writes, edits, compiles, and runs test programs; supports the system's peripherals, and interprets user instructions input from keyboard and keypad.

CPU in the test system offers users flexibility in configuring and connecting desired peripherals. A 500k-byte dual floppy disc and 10M-byte cartridge disc (continued on page 48)

It Pays To Have The New Mannesmann Tally T-3000.



New features from the leader in matrix line printers.

New capabilities. Expanded versatility. The Tally 300 line per minute printer takes advantage of the inherent flexibility of matrix line printing to give you more value. Now you can beat the band with host defined **downstream font selection** and change character styles midstream. No lost time, downtime, or messing around to change fonts. Plus, you can now print **double high characters** for highlighting text. Or, for those occasions when extra special print quality is called for, a new **multi-pass** model makes a double pass to enhance character appearance.

And now you can move the printer from the computer room and locate it where the information is used. A new Asynchronous Communications Adapter gives you 300 line per minute on-line **remote printing**.

Plus, look at the standard features of every T-3000. Quiet operation. Easy, front access, straight path paper loading. A reel to reel, prethreaded ribbon system for quick and clean ribbon changing. A time saving **diagnostic status display** that reduces service calls. It tells if a fault condition is operator correctable. If a service call is needed, it tells the service man what's wrong.

Dependable and durable, the T-3000 never requires preventive maintenance. Never needs adjustment. Character formation and line registration never waver. The T-3000. High reliability. Patented **flexure technology**.

There's more to tell so contact your nearest Mannesmann Tally Sales outlet. Mannesmann Tally, 8301 South 180th Street, Kent, WA 98031. Phone (206) 251-5524.

Printers for the long run.







TECH REVIEW

are supplied. The test procedure controller stores and runs test procedures under direction of the CPU. High speed program storage and execution take place at a rate of 5 MHz. Memory has single-bit error correction and doublebit error detection. The test procedure controller and CPU can combine to run two test programs in parallel, one for each test head. This parallel test capability improves throughput 20% to 50% for testers configured with two test heads.

Test pattern stimulus and response modules are responsible for dynamic testing. Timing control unit provides 16 time phase generators, each establishing 16 phase sets and periods selectable in real time. Timing is precise and the system can switch between algorithmic and functional test patterns on the fly at 40 MHz. The pin control truth table provides 16 fully encoded pin state functions for control of state changes at 40 MHz. The built-in data scope captures and reports the complete stimulus/ response status of any 256 steps for all 144 pins.

Each of the two 144-pin test heads has its own precision measurement unit and analog references, and can be functionally programmed directly from the CPU, bypassing the functional test system. Thus, each head can perform its own static testing without regard for the other's operation.

All pins are truly universal and have access to all system functions. Active programmable loads that switch at full 40-MHz test rates eliminate the need for dedicated load boards. These programmable loads can also be used for full parallel parametric testing on a per-pin basis with significant reductions in test times.

Circle 508 on Inquiry Card

Packaged 32-Bit Minicomputer Systems Designed for Transaction Processing

Two low cost hardware systems, based on the 32-bit model 3220 minicomputer, offer original equipment manufacturers and system builders economy in multiuser systems. Announced by Perkin Elmer Corp, Computer Systems Div, 2 Crescent Pl, Oceanport, NJ 07757, each system is intended for use with the company's multiterminal monitor or Reliance transaction processing software.

The 3220S includes a processor with 512k bytes of MOS memory; 800-char/in, 45-in/s (315/cm, 114-cm/s) magnetic tape unit; 80M-byte fixed disc; and four model 550 video display units. This package is configured with all system modules and peripherals required for a basic multi-user development system. Working with multiterminal 32-bit software, users can have up to 64 programmers doing concurrent development in any mix of high level languages, including ANSI standard COBOL, globally optimizing FORTRAN VII, Pascal, and RPG II.

For the commercial OEM interested in running Reliance application systems, the 3220C is configured with a processor having 512k bytes of MOS memory, magnetic tape unit, and 80M-byte disc. The video display unit used with this package is the model 1251, a sophisticated editing terminal.

Reliance transaction processing software eases operations and program development with its query facility, interactive screen forms design, and ANSI standard COBOL. It also protects the user's commercial data base from media faults and system failures. All operators can access the data base concurrently, safely, and effectively with its multi-threading feature.

Additional options can be attached to further tailor these systems to working requirements. Both systems can be packaged with dual-density tapes or 300M bytes discs.

Circle 509 on Inquiry Card

8" Floppy Disc Drive Uses Linear Stepper Motor to Reduce Mechanical Complexity

The model 8302S attains significant increases in industry standard reliability, serviceability, and flexibility through a combined reduction in major electromechanical moving parts and the use of microprocessor controls. Electronically, physically, and cosmetically compatible with Shugart's 851R double-sided 8" floppy disc drive, the unit, from Decitek Corp, 129 Flanders Rd, Westboro, MA 01581, uses a proprietary linear stepper motor design that allows a 37% reduction in total drive and positioner mechanism components and raises the unit's mean time between failure (MTBF) rate from the industry standard 8000 h to more than 12,000 h, a 50% increase.

Because the motor reduces the total number of drive components and requires no rotary to linear motion conversion, much of the wear that impacts seek performance has been eliminated. In addition, the drive is up to 50% quieter than other double-sided drives.

Four main components make up the drive: read/write head, head positioning mechanism for track selection, diskette drive mechanism, and read/write electronics and control electronics. The *(continued on page 51)*

GIMIX & MICROWARE present the 6809 PROFESSIONAL TOOLBOX

A GIMIX 56KB static RAM 2Mhz 6809 Dual Drive Mainframe System with MICROWARE's Multiuser OS9 Pro-Package --special combination price \$3968.09. This system includes the GIMIX Mainframe with 30 amp C.V. ferro-resonant power supply, SS50/50C Motherboard, 2Mhz 6809 CPU with time of day clock and battery back-up, 6840 programmable timer, 2 serial ports, 56K Bytes of Static RAM, and two 514.'' disk drives and double density controller installed in the GIMIX Mainframe with the same brownout protection and power supply, reliability that GIMIX is famous for.

MICROWARE's OS9 Pro-Package includes OS9 Level 1, the BASIC09 interactive compiler, Macro Text Editor, Interactive Assembler, and Interactive Debugger which gives you the necessary tools for efficient structured software development. All GIMIX Boards have gold plated bus connectors, and are burned in and 100% tested before shipping.

And this system is expandable. You can add memory, I/Os, video or graphics cards, Arithmetic processors, additional drive capacity, and other hardware now or in the future to this SS50 bus structured system from GIMIX or other SS50 bus compatible manufacturers. MICROWARE has other OS9 software such as the Stylograph Screen-Oriented Word Processor available now, and in the future will be announcing other languages and utilities that run under OS9. And coming soon from MICROWARE will be OS9 Level 2 that lets you address up to 1 megabyte of memory.

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See us at NCC Booth #971-2.





MICROANGELO

HIGH RESOLUTION GRAPHICS SINGLE BOARD COMPUTER 512 x 480 RESOLUTION MONOCHROME DISPLAY







RS-170 composite or direct drive output

Local or external sync generation

4 or 5 Mhz Z80 microprocessor

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IEEE S100 bus compatible



Light pen interface

Time multiplexed refresh

4K resident Screenware™ Pak I operating system

32K RAM isolated from host address space

High speed communications over parallel bus ports

Screenware[™] Pak I

A 4K byte operating system resident in PROM on MicroAngelo.[™] Pak I emulates an 85 character by 40 line graphics terminal and provides over 40 graphics commands. Provisions exist for user-defined character sets and directly callable user extensions to Screenware Pak I. TEKEM[™]

A Tektronix 4010/4014 graphics terminal emulator which is fully PLOT-10 and CP/M* compatible.

* CP/M is a registered trademark of Digital Research Corp.

Screenware[™] Pak II

An optional software superset of Pak I which adds circle generation, polygon flood, programmable split screen for separate graphics and terminal I/O, relative coordinates, faster vector and character plotting, a macro facility, full UCSD Pascal compatibility, and more.

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RASTER DISPLAYS... FOR THOSE WHO DEMAND PERFORMANCE.

TECH REVIEW



read/write head is a single-sided "button" style head with tunnel erase which produces an industry standard 0.013" (0.330-mm) wide data track. Erase gaps are approximately 0.008" (0.203-mm) wide between tracks. The head positioning mechanism consists of carriage and linear stepper motor. The carriage is a molded plastic part on which the read/ write head is mounted. A clamp, integral to the carriage, attaches the carriage to the stepper motor armature. Accurate head positioning is ensured by use of the linear stepper motor.

The linear stepper motor positions the carriage assembly, to which the read/ write head is attached. The stepper motor moves 0.020" (0.529 mm) from one stable position to the next by magnetically aligning square teeth in the outside armature (to which the carriage assembly is attached) to similar teeth on the inside stator. Successive energizing of the three coils on the stator causes the stator teeth to pull successive armature teeth, thus producing incremental linear motion of the armature and read/write head. The teeth on both the armature and stator are formed in a continuous helix. Rotation of the armature allows a fine linear adjustment of the armature due to the helix angle of the teeth. When armature and stator are in the desired position, a stiff magnetic force between aligned coil and armature locks them in position.

Positioning of the head through control of the stepper motor is performed through a microprocessor. Electronics controlling the write operation are digital. Signals generated during the read operation are analog and are converted to digital. Microprocessor control of electronic functions including seek and index (sector mark) generation results in design simplicity, since it allows hardwired functions to be replaced with discrete firmware elements.

Sharing a 95% parts commonality with the company's single-sided drive, which also uses a linear stepper motor, the 8302S uses a 1-piece positioner mechanism construction that eliminates the need for difficult alignment adjustments such as azimuth and head penetration. The entire positioner mechanism may be replaced in less than one-half hour by removing just one screw. This makes the drive easy to service by OEMs and does not require its return to the factory.

Storage capacity of the unit is 6.4M bits in hard sector, single-density mode, 4.0M bits in soft sector single-density, and 12.8M bits in hard sector double-density format. The unit provides a data transfer rate of 250k bits/s single-density or 500k bits/s in double-density. Seek time is cited as 6-ms track to track with 15-ms settling time. Access times are given as 83 ms latency and 254 ms average access. Price is \$670/unit in quantities of 100.

Circle 510 on Inquiry Card

See at NCC Booth 1750

Hardware/Software Package Extends Unibus Address Space, and Throughput

Permitting essentially unlimited address space on PDP-11 series computers, while maintaining the standard Unibus structure, a memory expansion technique offered by Programming Concepts, Inc, One Village Ct, Coram, NY 11727, uses a multivalued mapping of addresses to physical memory. This approach, developed jointly by Periphonics Corp and Brookvale Associates, allows use of memory spaces larger than the 248k bytes normally provided, while avoiding the additional processing power and cost of a larger (-11/44 or /70) computer, as well as the unwanted side effects of disc overlays and checkpointing.

In the Unibus architecture, as in that of most mini and microcomputers, memory is addressed by establishing a one to one mapping of bus addresses to physical memory cells. The Peripacs approach, however, uses a multivalued mapping of Unibus addresses to physical memory. A Unibus window is defined as a contiguous set of Unibus addresses which are controlled by Peripacs. Many devices or memory cells are present at each address within the window. The controlling device determines which will respond when a Unibus address is asserted. Memory cells are grouped into logical sets (planes) which do not have multiple mappings. One memory plane

(continued on page 54)

Bread & Bu

Count on a full selection of low-density PROMs from Signetics, your leading bipolar memory supplier.

As you inspect our menu of tempting PROM selections, don't overlook the bread-and-butter PROMs. Signetics' 256-bit, 1K, 2K, and 4K PROMs have long been and will continue to be the staple of the industry.

You'll find the PROM organization and specs you need from a wide selection of low-density parts. Both Schottky TTL and high-speed ECL, with your choice of three-state or open-collector outputs for maximum design flexibility. In memory or logic applications.

They're packaged and tested to commercial and military temperature ranges. And they offer a cost-effective programming yield that's the envy of the industry.

Once you've sampled our low-density, high-quality parts, you're sure to come back for more.

You'll also want to feast on other Signetics high-performance PROMs. Like our 8K power strobe device that cuts your power supply requirements by a factor of 10.

For dessert, high-speed 4K and 8K PROMs are the icing on the cake. Their access times are 45ns and 55ns, respectively—with even faster speeds in the oven.

Service is prompt and efficient. With new PROM production capacities for anything from a snack to a banquet we're ready to take reservations for your high-volume requirements.

ter PROMs.

BIPOLAR MEMORY SELECTION GUIDE

DENSITY	DEVICE TYPE	ORGANIZATION	OUTPUT CIRCUIT	ACCESS TIME (ns)	I _{CC} MAX. (mA)	DENSITY	DEVICE TYPE	ORGANIZATION	OUTPUT CIRCUIT	ACCESS TIME (ns)	IccMAX. (mA)
256-Bit	82S23	32X8	OC	50	77	8K	82S180	1024X8	OC	70	175
256-Bit	82S123	32X8	TS	50	77	8K	825181	1024X8	TS	70	175
256-Bit	10139	32X8	00	20	145	8K	82LS181	1024X8	TS	150	80
1K	82\$126	256X4	00	50	120	8K	82PS181	1024X8	TS	70	185
116	825129	25614	TS	50	120	8K	82HS181	1024X8	TS	55	175
116	10149	256¥4	00	20	150	8K	82\$2708	1024X8	TS	70	175
21	825130	51284	00	50	140	8K	82S183	1024X8	TS	60	175
24	825130	51284	TS	50	140	8K	82\$185	2048X4	TS	100	120
AN	020101	51274	TC	50	175	8K	82HS185	2048X4	TS	60	155
48	023113	51240	TC	00	175	164	020101	204070	TC	90	175
46	023141	51240	13	00	175	TUN	020191	204070	10	00	170
4K	82H514/	51288	15	45	155	IDA	8242131	204688	15	OU	1/5
4K	82S137	1024X4	TS	60	140	16K	82S195	4096X4	TS	70	155
4K	82HS137	1024X4	TS	45	140	32K	82\$321	4096X8	TS	90	175

To find out more about Signetics' broad PROM line, send the coupon below. Or contact your nearby Signetics sales office or authorized distributor. Signetics Corporation, 811 E. Arques Ave., P.O. Box 409, Sunnyvale, CA 94086. (408) 739-7700.



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- Send me general product reference material on all PROMs.
- I have an urgent requirement. Please have a PROM specialist phone me at once at:

Title

Division

and the second s

Name

Company ______

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MS State Zip

TECH REVIEW

controlled by Peripacs will be enabled by software, effectively placing that memory into the window. Up to 16 planes of 64k bytes each may be installed in a system, allowing a maximum of 1M bytes of added memory.

The basis of the patented technique for mapping logical (Unibus) to physical (Peripacs) memory is an active backplane. Software directives to physical memory cause activation or deactivation of memory slots in the backplane, which accomplishes placement of a memory plane within a window. Once within the window, the memory plane operates at normal Unibus/memory transfer rates. Contents of 64k bytes of main memory can be exchanged with previous contents with only two PDP-11 instructions, and with virtually no bus activity.

The DEC RSX-11M operating system provides the host environment with Pericheck software replacing the RSX LOADR program. RSX allocates main memory by an algorithm which uses partitions (a partition being a contiguous set of Unibus addresses). Pericheck provides a partition swapping mechanism that is an extension of the native checkpointing algorithm, and uses Peripacs controlled memory (rather than disc) for checkpointing of active, but not running tasks. This effectively increases the amount of main memory available for executable task images. Disc checkpointing is still available if the Peripacs space is totally used.

In a testbed installation consisting of a PDP-11/34A with 192k bytes main memory, 128k bytes of Peripacs memory, and RPR02 disc drives for checkpointing, an application environment was simulated by two tasks which computed and printed prime numbers. The tasks worked in sequence, passing the results of one calculation to the other to serve as basis of the next calculation. The results of the test showed that the system offered a throughput increase of 84.5%. Computed maximum possible increase is 115.5%.

Circle 511 on Inquiry Card

Desktop Business System Handles Winchester/Floppy Drives From Dual-Mode Controller

Vector 3005 is a desktop business data and word processing system that provides the speed, capacity, and reliability of Winchester hard disc storage. Introduced by Vector Graphic, Inc, 31364 Via Colinas, Westlake Village, CA 91362, it includes a 5.25" (13.33-cm) 5M-byte Winchester, a 630k-byte double-sided, quad-density floppy disc, and a Vector 3 display terminal and keyboard, plus an extensive array of software.

The hard disc stores a file of up to 5M bytes or 256 different files. A single disc can store a mailing list of up to 3700 names and addresses.

A dual-mode controller board controls both the Winchester and floppy disc drives and serves as the key to the system's error correcting capability. Using IBM based technology, it

(continued on page 56)



THE STD BUS PEOPLE.

INTERSIL'S SYSTEMS DIVISION ANNOUNCES A SPECTRUM OF STD BUS CARDS – OFF THE SHELF.

From the people whose total systems shipments to date have exceeded seven *billion* bytes of memory. The same people who've made a reputation in ultra-reliable cards and systems over the last ten years: Intersil's Systems Division.

Now introducing a broad new spectrum of STD BUS products. All available right now. And all *truly* STD BUS compatible. So you can mix and match cards with no surprises.

Plus, you can have your choice of microprocessors: 8085 or Z80. Either way, you get total compatibility throughout the family.

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CP/M[®] Disk Operating System (ICP/M) including text editor, assembler, debug, and disk and terminal I/O handlers Macro Assembler (IMAC) FORTRAN Compiler and Library (IFORT) BASIC Compiler (IBASC) BASIC Interpreter (IBASI) PASCAL Compiler (IPASC) Firmware Monitor (IFMON)

DEVELOPMENT SYSTEMS AND MUCH MORE - VERY SOON.

We're not stopping now. Because we're committed to having the biggest and best line of STD BUS cards in the business.

So in the very near future we'll be announcing a number of major additions to the family. Including parallel I/O, A/D and D/A cards. A PROM-burner card. A bit-oriented dual-channel synchronous communications card. A remote data acquisition controller card. Three new memory cards and more.

On the software side, we'll be introducing a firmware development system, including monitor, assembler and editor, PROM-burning software and multitasking control monitor.

And tying it all together there'll be a start-up designer's kit — plus a full-fledged STD BUS development system. So stay close and watch for more good news.

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Phone		1011
My program starte	ed/will start	
l anticipate an ann	ual usage of	cards CD48

TECH REVIEW



Desktop word and data processing system from Vector Graphic has 5M-byte 5.25'' Winchester disc and 630k-byte floppy disc for expanded processing capability. Disc controller features automatic error correction usually found only on larger systems

Microprocessor Designers Low-Power Switchers Work On All World Voltages

Without Changing Taps, Jumpers or Switches

Imagine you could design a microprocessor system that would operate almost anywhere in the world with a single switching power supply. Well, you can with Converter Concepts' low-power switchers!

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automatically corrects up to five erroneous bits in every 256 bits, eliminating errors due to disc contamination, aging, surface defects, and all but the most severe disc damage. The error correcting scheme also operates on floppy disc data. Since the floppies are used for Winchester backup, the error correcting feature adds to the system's overall reliability and integrity. The disc controller also features 256-byte sector buffering. This makes the system useful for communications and other realtime functions, since the buffering enables the CPU to simultaneously handle interrupts and data transfers in and out of memory.

Track to track access time of the Winchester is 3 ms; the companion floppy discs also have 3-ms track to track access. Both Winchester and floppy drives are housed in a compact unit approximately 8 x 6 x 12" (20 x 15 x 30 cm), which easily fits on a desktop adjacent to the display terminal.

All of the company's existing software operates on the systems, enabling users to upgrade to the disc based system or to mix various systems in an installation. Software provided with the system includes the CP/M-2 operating system, Scope editor, Raid debugger, ZSM assembler, and Microsoft Basic 80.

Circle 512 on Inquiry Card See at NCC Booth 2408

Microcomputer Based Interactive System Trains IBM Mainframe Computer Users

Trainer-3000 is a portable, voice response microcomputer system designed to provide effective, low cost, computer aided training for users of IBM mainframe computers. Announced by Computer Systems Research, Inc, 195 W Main St, Avon, CT 06001, the turnkey (hardware/software) package is described as a self-contained, ready to use system for computer aided instruction. Voice response capability humanizes the feedback on student responses.

The system uses the Course Structuring Facility (CSF) authoring language. This is the same language used in IBM's Interactive Instructional System (IIS), and permits courses to be authored and executed under either the Trainer-3000 or the IIS system. System components include interactive courseware, software package designated STARS (Student Training and Administrative Reporting

(continued on page 58

TOUGH

TOUGHER!

SECS 80: A complete family of systems designed around EMM's ruggedized versions of Intel's Single Board Computers

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Complete, Versatile Systems

These are complete systems, backed by a multitude of support modules — RAMs, ROMs, EPROMs, Digital Tape Recorder and Controller, 1553 and Multibus interface, analog and digital I/O, just to name a few. Software compatible, too, including the new iRMX* 88 Multitasking Executive and the iRMX 86 Multitasking Operating System.

*Trademark of Intel Corporation

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With all of these system components available and field proven, there's absolutely no need for you to invest hundreds of thousands of dollars to re-design a commercial computer to withstand hostile environments. We've already done it for you! And we do mean field proven. SECS 80 is currently being used in a variety of airborne, shipboard, and ground systems, as well as industrial applications involving tough environments.

ATR Compatible

SECS 80 modules are mounted on 9-inch by 6-inch shock and vibration resistant boards. A 1/2-ATR chassis can hold up to six boards.

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COMPUTER PRODUCTS FOR SEVERE ENVIRONMENTS

CIRCLE 39 ON INQUIRY CARD

The success of the Cheyenne is really an inside story.

From the outside, the Cheyenne sealed disc memory tells the story of its rugged reliability. But *inside*, you can see the result of more than 15 years experience building rotating memories.

The Cheyenne features SLI's unique rotary positioner and closed-loop dedicated servo track system. Capacity is up to *51.4 megabytes*, unformatted, on 4 discs, with 7.3, 22 and 36.7 MBytes available.

Other Cheyenne features include microprocessorbased drive electronics, with built-in diagnostics; SMD interface (others available); 478 TPI and 6500 BPI.

The A/C spindle motor is standard, as is 50/60 HZ with no hardware change required.

There's more ... inside the Cheyenne. Write or call Ray Kristiansen for the full story and our literature package.



TECH REVIEW

System), voice response unit, Apple II microcomputer, and two floppy disc drives. Courses are stored on floppy discs and include an operating manual.

Course material is designed to pretest students to determine what they already know, and concentrate only on what they don't know. It also provides for post-testing and final exams to determine what is learned. Currently available courses emphasize system operation and problem resolution for the JES3/MVS system. Planned for release this year are packages covering operation and technical problem resolution training for IBM 3081, 303X, 4300, and JES2/MVS systems.

Circle 513 on Inquiry Card

Dual-Processor Complex Upgrades Performance of IBM Compatible Family

The AS/9000DPC (Dual-Processor Complex), a tightly coupled system, provides 1.7 to 1.9 times the performance of the AS/9000, which is 2.5 to 3.0 times the processing power of the AS/7000. This IBM compatible general purpose computer has the function of an MP system, since it can also be operated as two independent uniprocessors.

In a minimum configuration, the system provides 16M bytes and 16 channels. The minimum AS/9000 configuration that can be expanded to the dual-processor configuration has 16M bytes, 16 channels, and an extended channel feature. All functions and options for the /9000 are available in the upgraded configurations, yielding a maximum of 32M bytes and 32 channels.

Concurrently announced by National Advanced Systems, 800 E Middlefield Rd, Mountain View, CA 94040, these enhancements include expansion of main memory to 32M-byte configurations in 4M-byte increments to provide greater performance when running IBM MVS/SP operating system. With extended channel capability, 24 channels can be attached. All but one channel can be block multiplexer channels and are capable of supporting data streaming protocol. Data streaming will be available without extended channel capability for a maximum of six channels and for all block multiplexers with extended channel capability. MVS/SP assist hardware, and microcode will provide improved performance when running MVS/SP release 3 and subsequent releases. Circle 514 on Inquiry Card

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MPP 80SAM

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It's pretty powerful stuff. But before you start to wonder if success has gone to our heads, let us assure you we're not seeing pink elephants. MPI's high performance mini floppy disk drive in the new 96 TPI configuration is a working reality. We've got the proof—the 96 proof. While others have been busy making

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In addition to these plusses are lower power consumption, automatic diskette ejection, automatic positioning, single PCB, and front door that protects media from foreign matter in either the Shugart configuration or our own. Finally, our 96 TPI drives can read 48 TPI diskettes.

If you're interested in hearing more about proven 96 TPI technology, MPI has a sales representative who will be glad to pour over details with you. Just give us a call and tell us when to set 'em up.

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N.C.C.BOOTH 5109





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from design to test and everything in between... a commitment to dynamic RAM state-of-the-art...

TMS4164 from Texas Instruments. Advancing the systems approach to 64K technology.

Using diverse resources and production-proven experience, TI developed a 64K dynamic RAM supported by a broad base of technical innovations — at all levels.

There's a systems approach to the advancement of 64K technology that assures our customers that TMS4164 is superior in design — and equally superior in the use of materials, processing and testing techniques.

Because improvements in one technology drive improvements in all the others, it's the shared learning experience between all TI semiconductor technologies that has brought TMS4164 to the leading edge of the state-of-the-art and beyond.

Design

Our unique grounded substrate design totally eliminates the need for a substrate bias generator — and its less effective method of establishing a negative voltage to control injected electrons. Enhanced noise immunity, greater tolerance to negative undershoot, wider operating margins and firmer transistor parameters are just a few of the breakthroughs TI has achieved with the grounded substrate technology.

Of course, there's much more to the design story, too—like our advanced 256-cycle, 4-ms refresh



 $Fabricating \ the \ TMS4164 \ cell \ on \ epitaxial \ silicon \ virtually \ eliminates \ substrate \ noise.$

architecture, low-power dissipation and fast cycle time.

Materials

Innovations are also incorporated into TI's use of materials. By depositing a thin, closely controlled layer of highly resistive P^- silicon onto a low resistivity P^+ substrate, we have virtually eliminated peripheral noise in the TMS4164.

The low resistivity substrate damps out capacitive coupling typically caused by clock bus line activation. Other benefits of this epitaxial (epi) layer are reduced algorithm sensitivity and immunity to address voltage bump. And, epi sets the stage for the future — the not-too-distant future of 256K devices — and the challenge of VLSI.

Processing

Processing advances in TI's TMS4164 mark major technology turns in high-performance DRAM production. TI has unequalled experience in the development of key equipment, like our own dry plasma reactors, and use of advanced low-temperature processing techniques. Our processing capability means device consistency, uniformity and reliability. And satisfied customers.

Testing

For consistently superior system performance, every 64K

DRAM is tested well beyond device specification. TI's meticulous attention to equipment accuracy and exhaustive algorithm testing result in high incoming quality. And, our own Test Data Management (TDM) system uses TI's 990 minicomputer to statistically track transistor parameters and other performance characteristics for constant process improvement.

Thanks to this kind of real-time process feedback, TI can assure every TMS4164 user of a more uniform product — and, built-in quality.

For the inside story on TI's TMS4164 64K dynamic RAM, and our leading edge systems approach, call your nearest TI field sales office, or write to Texas Instru-

ments Incorporated, P.O. Box 1443, M/S 6955, Houston, Texas 77001.



TEXAS INSTRUMENTS

CIRCLE 43 ON INQUIRY CARD

TECH REVIEW

SOFTWARE

Computer Graphics Software Increases Productivity of Scientific Users

Gifts 1100, a graphics oriented interactive fine elements timesharing system, provides a unified approach to model generation, model display, analysis, and result display. Made available to scientific users of Series 1100 mainframe computers by Sperry Univac, PO Box 500, Blue Bell, PA 19424, the package substantially increases productivity in the engineering and design community, thus saving time by freeing engineers from tedious work associated with the design process.

Based on software provided by the University of Arizona, the package works in conjunction with structural analysis programs such as NASTRAN and ICES/STRUDL, to provide graphic interfaces for generation of either 3-dimensional plate and shell or solid models. Once models are generated, its editing capabilities enable users to change and study the models, ie, a model can be repositioned to view it from any angle or can be enlarged for close scrutiny of certain portions.

Circle 515 on Inquiry Card

Data Management System Accommodates Needs of Industrial Research Scientists

Making computer technology readily accessible to scientists involved in research and development, RS/1, The Research System, provides a flexible working environment by combining data management, statistical analyses, and full graphics capability. Bolt Beranek and Newman Inc, 10 Moulton St, Cambridge, MA 02238, designed the system to enable investigators to maintain hands-on control of their research data. Using the software and a minicomputer. scientists will be able to immediately visualize experimental results instead of depending on centralized computer resources and overnight processing.

The system's conversational English language commands require no programming experience. Use of familiar research constructs for data storage and display make the system easy to learn for scientists who are accustomed to organizing their data in traditional laboratory notebooks. Data organization is based on the 2-dimensional data table concept universally applied by scientists. Users can create any number of tables, each containing more than 1M elements. Through a simple series of commands, a user can control layout of the tables as well as derive values based on data they contain.

In addition to data management and graphics capabilities, the software also provides commands to perform an extensive array of statistical analysis, including analysis of variance, linear and nonlinear regression, and parametric and nonparametric testing. Data trends can be visualized via a graphics terminal.

The package is available for the full range of DEC PDP-11 and VAX computers and can support a variety of Tektronix and DEC terminals, including color graphics. An add-on to the system will produce graphics and bar graphs on plotting devices.

Circle 516 on Inquiry Card

Remote System Diagnostics Added to Distributed Processing Environment

Remote system diagnostics for MODACS III realtime subsystems support configurations where a remote system may be unattended and require testing, or situations wherein the remote location is environmentally hostile. The tests, provided by Modular Computer Systems, Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33310, verify the performance of the link at the host and satellite, the CPU, memory, floating point or extended arithmetic unit, I/O processors, MODACS III controller, and other devices associated with the gathering of realtime information and control.

A typical functional configuration is a host Classic 7860 running the realtime multiprogramming operating system MAX IV that is communicating to several satellites via the operating system extension. Satellites are connected to the host via direct links. Operators may be selective in the tests that are executed or may define a set of automatic tests at system generation time. System degradation is minimized because the only component not functioning 100% is the specific satellite under test.

Circle 517 on Inquiry Card

Pascal Compiler Supports Large Programming Projects On Desktop Minicomputer

Pascal compiler offers language extensions that adapt it to large scale programming projects and make it suitable for systems programming. Introduced by Convergent Technologies, 2500 Augustine Dr, Santa Clara, CA 95051, for use on their desktop minicomputers, the language conforms to the current proposed ISO standard. Because the software compiles to the native machine code of the 16-bit central processing unit, program execution is substantially faster than interpretive P-code based systems, such as implementations of UCSD Pascal. However, the compiler is compatible with UCSD Pascal and includes such enhancements as interfaces and LSTRINGS.

The system supports independent compilation with cross type checking, has full 1M-byte addressability via long pointers, and provides a retype mechanism to control type interpretation. Data types include WORD, LSTRING, and SUPERARRAY. Added constants are hexadecimal, binary, octal, structured constants, and constant expressions.

Pascal object modules can be combined with those of other programming languages supported by the system via the linker. This capability permits writing applications that require different languages for different parts of the application.

The compiler is fully compatible with the company's virtual code facility, and supports Pascal programs whose code size is greater than the system's physical memory. In addition, it allows full access to all CTOS operating system services such as random access to disc files, interrupt handling, and process creation, thereby supporting various kinds of system programming. Circle 518 on Inquiry Card

COMPUTER DESIGN • APRIL 1981



















Scanner sense.

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systems for every conceivable application from non-impact printing to COM, command a capability and expertise that insures you a high performance system at a cost lower than you can do yourself.

For more information and scanner sense, contact: Tropel Division, Coherent, Inc., 1000 Fairport Park, Fairport, N.Y., 716 377-3200.



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The new solid state Fujitsu bubble detachable and portable. And easy to program, data locate, erase and re-use. Both cassette systems offer high-speed response, easy read and write features, non-destructive readout and excellent magnetic shielding.

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THE SMART SET

Members of this exclusive circle of PRIAM Winchester disc drives have some uncommon things in common. With capacities from 10.8 to 158 Megabytes, they have the same interface. And they all connect quickly and easily to microprocessor I/O busses through PRIAM's SMART or SMART-E Interface.

With a simple adapter your system can have the remarkable reliability of Winchester disc drives. And PRIAM's DISKOS drives give you the lowest costper-megabyte for your system database.

SMART Gets Smarter!

With its own sophisticated preprogrammed microprocessor, PRIAM's SMART Interface gives you comprehensive disc subsystem functions, including:

- Control of any combination of one to four PRIAM Winchester disc drives.
- Automatic alternate sector assignment for disc-defect transparency to the host processor.

In addition to all SMART functions, PRIAM's new SMART-E Interface provides ECC, streamlined software, sector interleaving, a 2048-byte buffer, and logical-sector addressing. Both the SMART and SMART-E come to you on a single 8" × 14" printed circuit board that is powered from the drive. And it piggybacks on the drive or mounts separately.

Meet The Elite! PRIAM's High-Capacity, Low-Cost 14-Inch Drives

PRIAM's high-technology 14-inch disc drives have capacities of 34, 68, or 158 megabytes, and they all fit in the same $7" \times 17" \times 20"$ package, including optional power supply. Fully servoed linear-voice-coil head positioning is reliable and fast—45 ms average for the 34 and 68 megabyte drives and 40 ms for the 158 megabyte version. Track to track is 8 ms.

Brushless DC spindle motors in all PRIAM drives assure mechanical simplicity, precise disc speed control, and operation anywhere in the world without change. No relays, mechanical brakes, brushes, belts, or pulleys. Pure, reliable electronic control. Elegantly simple.

The Talk Of The Town: PRIAM Eight-Inch-Disc Drives!

Debut a Winchester disc drive in place of a floppy disc with PRIAM's DISKOS 3450 and 7050, expanding your database to 35 or 70 megabytes. Thoroughbred performance goes with their linear voice-coil positioners; seek times are only 40 ms average and 8 ms track-to-track. If you need an even lower-cost drive, the DISKOS 1070 gives you a 10.8megabyte capacity with stepper-motor positioning. Seek times are 73 ms average and 23 ms track-to-track. And they're just as SMART as other PRIAM drives when used with PRIAM's SMART or SMART-E Interface.

More Basic Interface Options!

To those who have their own controller plans, PRIAM offers lower-cost drive-level interfaces. PRIAM's bit-serial NRZ data interface, similar to the evolving ANSI standard, has an 8-bit bidirectional control bus for easy connection to popular 8 and 16-bit microprocessors. Data separation is included in all PRIAM drives.

And if you have a Storage Module controller, you can use it and your software with PRIAM's SMD Interface to update your system with Winchester drives quickly and inexpensively.

For complete information about the SMART and SMART-E Interfaces and PRIAM's SMART SET of Winchester disc drives, RSVP by telephone or write to:



3096 Orchard Drive San Jose, CA 95134 Telephone (408) 946-4600 TWX 910-338-0293



FRESH IDEAS ARE GROWING AT ALTOS

Silicon Valley, California. At one time few places in the world were as abundant with orchards. Today, no other area is as technologically fertile. And nowhere on earth is the business climate as prolific with computer innovation.

Yet within this competitive environment, one microcomputer firm continues to grow above the rest. Altos Computer Systems. Recognized as a world leader in single board microcomputer technology, Altos flourishes on its ability to produce ideas and deliver them to the market while they're still fresh and packed with price performance value.



Fresh ideas like Altos' new ACS8000-6/MTU single board microcomputer system with a DEI ¼-inch cartridge tape back-up drive, and Shugart's 8-inch floppy and 14-inch Winchester hard disk drives, with total on-line capacities from 14.5 MBytes to 58 MBytes.

The ACS8000-6/MTU joins Altos' growing family of products that branch out to a multitude of single board system configurations to serve the OEM, the business sector, and many other end users. These systems range from the ACS8000-2 with its dual 8-inch floppy disk drives, to the powerful ACS8000-5, which is upgradable to any of Altos' hard disk and multiuser systems.

Altos supports three industry standard operating systems: single/ multi-user CP/M*, OASIS,† and Altos' proprietary AMEX.** Seven high level programming languages are offered which are CP/M or AMEX compatible.

Ideas aren't the only things growing at Altos. In three years over 4,000 field-proven microcomputer systems have been shipped worldwide to an ever-increasing customer base of over 300 companies. And recently a new facility has been acquired, expanding Altos' plot to over one-and-a-half acres of production facilities.

Weed through the microcomputer system alternatives. No matter what your application, you'll pick Altos.

For specific details about pricing or performance, call or write: Altos Computer Systems, 2360 Bering Drive, San Jose, CA, 95131, (408) 946-6700, Telex 171562 ALTOS SNJ.

Packed with Fresh Ideas



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new, high-performance processor with exclusive on-chip features to reduce chip count ... from Texas Instruments.

THE SEC

5
TMS9995

The fastest 8/16-bit processor available anywhere. From anyone. 16x16-bit multiply in 7.67 µs.

All you have to do is compare and you'll see that the biggest choice in 16-bits just got bigger. Faster. More powerful.

TMS9995 joins the industry's most complete 16-bit family of microprocessors, microcomputers, microcomputer modules, peripherals, software, and software and hardware development systems.

Now you have an easy upgrade to 16 bits, while retaining the economy of 8 bits. And, you'll get all the benefits of TI's all-pervasive family compatibility that lets you move from one product level to another — from single-chips to multi-chips to modules to systems protecting your software investment and development systems as you go no translators, no code converters, no extras.

And now there's TMS9995 — with all the inherent advantages of memoryto-memory architecture, plus 256 bytes of on-chip RAM.

And now there's TMS9995 — for all those tough tasks that demand 16-bit speed and processing power.

And now there's TMS9995 — with on-chip clock, 16-bit timer/event counter and 8-bit data bus for interfacing to everything from a minimum 3-chip system to a 16-megabyte memory system (just add the 99610 memory mapper).

TMS9995. Shrinking chip count and program size. Ready for VLSI.

Logical link

TI's TMS9940 was the first single-chip 16-bit microcomputer — and the first to transcend the limitations of high-speed and high-resolution. TMS9995 adds the ability to address off-chip memory to the TMS9940 — up to 64K bytes. Together they fill the requirements from small microcomputer-based systems to medium-sized systems, using on-board RAM and off-board ROM, to larger systems needing off-board RAM and ROM.

TMS9995—Key features

• 16-bit CPU

- 12 MHz clock with on-chip clock generator
- 256-byte on-chip RAM
- 16-bit on-chip interval timer/event counter
- 7 levels of vectored interrupts
- instruction prefetch
- automatic first wait-state generation
- MID macro-instruction detect interrupt
- single 5-V power supply
- 40-pin dual-in-line-package.

Performance plus

Three times faster than the TMS9900, TMS9995 executes a 16x16-bit multiply in just 7.67 μ s. A 32-bit number divided by a 16-bit number in just 9.33 μ s. TMS9995 can run with currently available fast memories of 120-ns access times, or by using automatically generated wait states, 450-ns access time memories.

256-bytes of fast on-chip RAM is organized as 128 x 16-bit words, allow-

Execution Time Benchmarks

a mana	Automated Parts Inspection (Seconds)	Computer Graphics XY Transform (Seconds)	Bubble Sort (Millisec)	Block Translation (Millisec)	16 Bit Multiply (Microsec)	Single Vectored Interrupt (Microsec)
9995 (12 MHz) w/120ns PROM	0.666	0.863	1.240	1.767	10.00	8.0
9995 (12 MHz) w/450ns EPROM	0.950	1.081	1.956	2.696	12.67	10.67
8088 (5 MHz) w/450ns EPROM	1.596	2.402	2.254	1.522	40.8	77.6
6809 (2 MHz) w/450ns EPROM	9.67	57.1	2.376	3.01	91.9	27.6

ing a full 16-bit word access in one clock cycle.

And, TMS9995 uses an intelligent pipelined architecture where the op code of the next instruction to be performed is prefetched. For example, the microcode for Branch and Jump instructions direct TMS9995 processors to prefetch the true next instruction instead of blindly prefetching from the next sequential memory location.

And now, a word about memory-to-memory architecture

The innovative architecture at the very heart of the 9900 Family reaches it's performance peak in the TMS9995 thanks to on-chip RAM. Comparison of execution speed benchmarks clearly show the advantages:

Support, support, support.

Necessary for any microcomputer family. TI's 9900 Family is supported by Pascal, Basic and Fortran software and software and hardware development systems, including a low-cost Evaluation Module, TMAM6095, for \$800.* TI also offers training, documentation and expert field assistance. Training, service and design assistance are available at Distributor System Centers, and TI's Regional Technology Centers.

Commitment to 16-bit leadership

The continuing introduction of new, advanced, high-performance 9900 Family CPUs, with TI's state-of-the-art technology and production-proven resources, clearly demonstrates a commitment to leadership. A commitment to choice. A commitment to the future.

For more information about the new TMS9995, or any other 9900 Family member, contact the TI distributor or field sales office near-

est you, or write to Texas Instruments Incorporated, P. O. Box 1443, M/S 6404, Houston, Texas 77001.



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INCORPORATED

TEXAS INSTRUMENTS

CIRCLE 47 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Training System Simulates Malfunctions in Machine System Interfaced to Programmable Controller

With the present emphasis on increased productivity, and the corresponding trend toward supervision of industrial equipment and processes by programmable controllers, new factors have been introduced into machine operation, maintenance, and troubleshooting. One result of this has been the need to train and retrain personnel to implement these functions in a digital environment. If training is carried out using the actual assembly line equipment, costly, time-consuming interruptions are introduced into the production process. Similarly, if production personnel do not practice maintenance procedures on the actual equipment, diagnostic and corrective actions will mean long interruptions when failures occur.

Therefore, it becomes practical to simulate the operation and potential malfunctions of a programmable controller and the machine or process that it controls and to train personnel within this simulated environment. Fortunately, the digital environment is particularly adaptable to simulation. This simulation approach has been taken by Ford Motor Co, Dearborn, MI 48121. Utilizing custom-designed selfinstructional training materials, a microprocessor based, standalone, turnkey system designated as a Machine System Simulator (MSS) is used in several of the manufacturer's facilities in conjunction with a programmable controller (PC), to train operators and maintenance personnel.

The simulator was developed by Ford Aerospace and Communications Corp's Instructional Systems Organization, 3100 E Foothill Blvd, Pasadena, CA 91107. This group developed the system approach and the training program, subcontracting hardware and software development to Instrumentation Technology Systems, 19360 Business Center Dr, Northridge, CA 91324.

System Description

Constructed in a deskmount cabinet, the MSS has three front panel sections: a machine control panel matching that of the simulated machine system, a test point array, and a simulator control panel relating to the training sequence (Fig 1). This 3-panel device interfaces with a programmable controller. The PCs



Fig 1 Front panel of machine system simulator (MSS) is divided into three sections. Machine control panel resembles actual automatic/manual drill press control panel. Test point panel represents terminal strip for voltage testing of drill press limit switches and pushbuttons. Simulator control panel provides training mode selection and feedback

that have been used in this application are the Bulletin 1774 PLC from Allen-Bradley, Cleveland, OH 44143, and the 184/384 from Gould Inc, Modicon Division, PO Box 83, Shawsheen Village Sta, Andover, MA 01810. When interfaced to this simulator, the controller operates as it would if it were interfaced to the machine system that is being represented. An automatic/manual drill press was selected as the common generic machine process to be used (Fig 2), and the MSS is programmed to simulate this device operating under the supervision of the PC.

The block diagram in Fig 3 illustrates how the drilling operation is simulated and how the MSS simulates malfunctions in either the controller or the drill press. This diagram is divided by dashed lines into four sections. Although there is some overlap, the principal functions of these sections are: A—central processing unit; B—simulation of machine/controller interface; C—interface between CPU and MSS front panels; and D—fault simulation.

As shown in Fig 3, the CPU for the simulator is a card that includes the 16-bit Pace microprocessor, from National Semiconductor, 2901 Semiconductor Dr, Santa Clara, CA 95051, and provides the interface, via the system data bus, that allows the exchange of data between all other elements in the subsystem. The CPU initiates and controls system timing with a 10.25-MHz crystal oscillator and divides the initial frequency to produce block outputs of 6.25 μ s (continued on page 74)

A video bandwidth of 30 MHz and a 1200-line resolution make this new CRT monitor the brightest and sharpest you can get.

C. Itoh's new model 1201BE in our QDM series is capable of receiving separate horizontal drive pulse, vertical drive pulse and video input at the TTL level. This separate signal mode eliminates composite sync and video signal processing. The CRT is equipped with its own power supply unit. P4 phosphor is standard, but optional P31 or P39 phosphors can be provided. Available options: Dynamic Focus, Skip Scan, a non-glare etched face and a 19.5 KHz horizontal frequency. The high performance and low price offered with this new CRT monitor give you all you need to really outshine your system's competition. For complete information contact your nearest C. Itoh representative or C. Itoh Electronics, Inc., 5301 Beethoven Street, Los Angeles, CA 90066; Tel. (213) 390-7778:

(213) 390-7778; Telex: (WU) 65-2451; or 666 Third Avenue, New York, NY 10017; Tel (212) 682-0420; Telex: (WU) 12-5059.

C. ITOH ELECTRONICS, INC.

Introducing the 12"CRT monitor for the systems designer with bright ideas.

See us at NCC - Booth 645 CIRCLE 48 ON INQUIRY CARD

DIGITAL CONTROL



Fig 2 Simulation of drilling operation by simulator. Correspondence is shown between process steps and

front panel pilot lights. Upper diagrams show interaction between machine parts and limit switches (LS)

and 2.56 MHz. In addition to processing bus information and generating system timing, the card also provides 4k bytes of ROM (four 2048 x 4 P/ROMs) to contain the processor/controller software.

At power-up, the CPU runs through an initialization process that sets the simulator and controller to receive and respond to inputs. Tests performed are a CPU operational test, a test of the random access memory (RAM), and a test of the ROM. After completion of the power-up test, which takes about 0.5 s, the power pushbutton lights up, signifying that the simulator is ready.

When the MSS is powered-up and operating, the CPU scans the 16-bit system data bus every 50 ms to detect any pushbutton input from the simulator front panel. The CPU senses the depressing of a pushbutton as the transition in status of the input lines on the parallel I/O interface card, whose input register provides a bit position corresponding to each pushbutton. When a bit changes, the CPU consults a lookup table to see which pushbutton was depressed, and then goes through a routine to process the input and provide an output to the controller corresponding to that pushbutton.

The command data interface card is the primary interface between the simulator and the programmable controller. Signals from this card are accepted by the LED driver/latch and optotriacs, converting the internal 5-V TTL of the MSS to 115 Vac that the controller receives and that the trainee can measure at the test point panel. Signals to the controller are output through the optotriacs. The controller processes those signals and outputs its response directing the next machine process step to occur. This is done through the MSS opto-isolator, which again converts the 115-Vac input to a TTL signal that the MSS can sense. This signal is then held in the bus buffers.

Still scanning the 16-bit system data bus, the CPU processes the output signal received in the command/data interface card from the controller and determines the next machine process step and the pilot light signal to be turned on. This signal then goes to the parallel I/O interface card and the lamp drivers and to the appropriate MSS pilot light. A signal is output to the controller, indicating that the machine action has occurred and that the pilot light

(continued on page 78)



THE ZENTEC SERIES 8000 INTELLIGENT TERMINALS

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With the Series 8000, Zentec successfully re-defines the words Human Engineering. Never before has there been a more powerful, more flexible, more operator-oriented video display terminal designed expressly for OEMs and system integrators.

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- UP TO FOUR FEET -

Communication and a second and a

standard with the 8000, and the OEM may add one or two of his own PCBs. The standard logic contains Zentec's unique minicomputer-like bus architecture under the control of a powerful microprocessor. Hardware for synchronous or asynchronous communications and printer I/O is standard. The Zentec 8000 may be configured with 16, 32, or 64KB of RAM and 4, 8, 12, or 16KB of ROM or PROM. That's flexibility!

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DIGITAL CONTROL



Fig 3 Block diagram of simulator. CPU, machine controller interface, CPU/front panel interface,

has been turned on, and then processed by the controller software. It is again output to the simulator for the next machine process step, to continue the cycle.

The above description outlines the simulator operation relating to the machine process step, pilot lights, and pushbuttons. Simulated solenoids are treated in a similar fashion, except that, when a solenoid action occurs, the software provides delays so that signal status remains fixed over the period that would be required for the actual solenoid to perform its action.

Fault Simulation

Several kinds of faults are simulated in the machine controller system. These include faults in the CPU of the controller, data errors in the serial bit stream between the processor and the I/O unit of the PC, machine system failures, and other miscellaneous faults. There are some variations in the kinds of faults generated and the mechanisms of generation, and fault simulation functions are associated with sections A, B, C, and D, respectively

depending on which of the two kinds of PC is used. However, in general, the simulations involving the two PCs are quite similar.

The RAM/RS-232 interface card is a key element in the generation of simulated program errors. This card contains 1k of RAM and an RS-232 serial interface including a UART that provides conversion to serial data format for transfer to the PC. By means of this interface, the simulator loads the proper ladder logic for machine operation into the controller. Under the direction of the simulator's CPU, this ladder logic can be modified to simulate faults internal to the controller, that may appear as memory failures or lost data in the ladder logic.

Interception of the data flow between the CPU and the I/O of the controller is implemented in the I/O bit fault generators. There the data streams from the controller and the simulator are combined, with the MSS data stream forcing input on or off, depending on the fault to be simulated. In order to generate bit errors in the CPU-I/O handshaking dialogue, without *(continued on page 80*)

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 TEAC 50C	960K	<10,000 Mainly in Japan	steel lead screw	100	865
Micropolis 1016/1015	1,100K	60,000	steel lead screw	96/100	365

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DIGITAL CONTROL

causing a more obvious catastrophic failure, it is necessary to sync the error bits to the clock cycle of the PC. This is achieved through the oscillator, sync, and clock generator elements of the MSS.

Machine system malfunctions include failures of limit switches, solenoids, and hydraulic elements of the machine. The software of the MSS generates them as perturbations in the corresponding outputs of the optotriacs causing the PC to indicate a malfunction or shut down.

Miscellaneous faults include failure of the PC master clock, a blown PC fuse, and pilot light failure. These indications are triggered in the Allen-Bradley controller by signals from the open collector line drivers on the MSS lamp driver board to a special I/O fault card mounted on the PC's I/O rack. In the case of the Gould Modicon PC, it is more efficient to simulate these kinds of faults in the program that addresses the PC processor.

Human Interface

The simulator's thumbwheel switches are used to instruct the CPU to process the inputs from the MSS front panel in a no-fault or fault condition. When a fault condition is loaded into the switches, and the load pushbutton is depressed and sensed by the parallel I/O interface card, the CPU sets the fault indicated by the switches, which may be a machine or controller fault. The trainee is then able to introduce a fault and observe its effects on the system.

In a more advanced troubleshooting mode, the MSS software provides random fault generation. The trainee attempts to diagnose the fault by observing the simulated machine system process steps, the machine system indicator portion of the front panel, and the controller operating components. He then determines the correction procedures on the basis of the indicators, enters his diagnosis in a workbook,

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DIGITAL CONTROL

and requests feedback via the simulator panel for identification of the simulated fault. The fault number is displayed on the 7-segment LEDs of the simulator control panel. This fault can be verified further by using solution indexes found in the workbook.

Summary

Used in conjunction with specifically designed instructional materials, the Machine System Simulator allows operations and maintenance personnel to experience all of the essential interactions with a machine system linked to a programmable controller, without interruption of the actual process. The extent of the potential downtime improvement achieved is indicated by the fact that personnel trained by this system can typically complete diagnostics and correction procedures in a few minutes, under fault conditions that, prior to this training, required hours or as much as a half day to eliminate. Interruptions of this sort can cost thousands of dollars for each hour that the production line is out of operation.

Although this system is being used only in certain specific applications, its potential usage is quite general. The simulator could be adapted to represent any machine or process operating under supervision of a programmable controller, subject to various kinds of faults. More generally, it could be adapted to simulate any process that is accessed through digital I/O interfaces, whether or not programmable controllers are included in the interface. Without disrupting production, this system and its general approach may prove to have considerable impact on the training of personnel in a wide variety of industrial situations. The ultimate implication of such approaches will be their long-term effects on the productivity of equipment and its operators.

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CIRCLE 53 ON INQUIRY CARD

A PenrWell Publication APRIL 1981
COMPUTER BASED SYSTEMS



NGC PRODUCT PREVIEW

The exhibition at NCC '81 will consist of many products of interest to designers of computers, peripherals, and computer based systems. Those products that have not previously been exhibited or covered in our editorial departments are described in

the following pages. Many manufacturers who were unable to meet the deadline for supplying information for these pages will also have innovative products on display in the Exhibition Hall at McCormick Place.

CRT Terminal Incorporates Custom LSI Chips to Simplify Design and Lower Price

Viewpoint, a fully featured CRT terminal, uses proprietary LSI circuits that reduce logic electronics to 11 chips to achieve a price 30% below that of other terminals currently available in OEM quantities. Designed for ease of use, high reliability, and serviceability, the terminal is manufactured in one standard configuration; the only option is a screen filter.



All logic circuits within the unit are contained on a single $6.5 \times 8''$ (16.5×20 -cm) card. A major component of the card is a custom LSI video controller chip which contains the equivalent of 148 individual chips. This controller works in conjunction with a Zilog Z8 microprocessor to translate incoming data from a host computer into signals that drive the CRT monitor and display characters on its screen.

A single memory chip is used for the video refresh memory circuit instead of the 5 or 6 chips required in earlier units. In addition to a lower price, the simplified design has resulted in reduced parts count, lowered assembly and testing costs, and improved reliability and serviceability of the finished product.

User friendliness is achieved through a movable keyboard, a 2-position tilting CRT screen, and a glare filter. Each feature makes the terminal comfortable to use for prolonged periods of time. The keyboard design emulates the Selectric keyboard and is attached to the CRT module by a coiled cable that allows it to be moved to an adjacent work area. Keyboard layout is designed in a typewriter like format. A separate 14-key cluster includes cursor control keys and an 11-key numeric pad laid out to ANSI standards.

The 12" (30-cm) display presents light characters on a dark background (reversible through switch selection). Visual attributes include normal video plus a choice of blinking, underline, reverse video, half intensity, or zero intensity. The cursor can be directly positioned through absolute address. All 96 displayable ASCII codes are formed using a 5 x 7 dot matrix in a screen format of 24 lines by 80 characters. Also available are UK/Netherlands, Danish/ Norwegian, Swedish/Finnish, German, French, and Spanish character sets. Refresh rate is 60 frames/s (50 optional).

Communication interface is EIA RS-232-C/CCITT V.24, operating through the range from 110 to 19,200 baud, switch-selectable. Conversational (character at a time) transmission takes place in switchselectable full- or half-duplex mode. An auxiliary interface for an EIA serial output peripheral is provided. The terminal will pass all received data to this interface and not react to commands from the data stream.

The CRT unit measures $12.33 \times 14.50 \times 14"$ ($31.32 \times 36.83 \times 35.6$ cm) and weighs 20 lb (9 kg). The keyboard measures $15.25 \times 7.125"$ (38.74×18 cm) and weighs 2 lb (0.9 kg). Power requirements are 110 V at 60 Hz, and operating temperature is 10 to 40 °C.

Price is quoted as \$650 for a single unit. In high volumes, this decreases to under \$450/unit. **Applied Digital Data Systems Inc**, 100 Marcus Blvd, Hauppauge, NY 11787.

See at Booth 745

Circle 321 on Inquiry Card

The Idea Is Retro-Graphics.



Retro-Graphics is quite literally changing the face of the display terminal marketplace. Because the line of graphic enhancement products that carries the Retro-Graphics name transforms some of today's most popular alphanumerics terminals—the DEC[®] VT100[®] terminal, for instance, and Lear Siegler's ADM-3A and 3A+ Dumb Terminal[®] products—into terminals that feature *full graphics capabilities.*

These enhanced terminals feature complete emulation of their Tektronix[®] counterparts, the 4010 Series graphics terminals. Additionally, they boast vector drawing and point plotting capabilities, selective erase, alphanumerics overlay, raster scan technology and, of course, complete compatibility with industry standard software, including Tektronix Plot 10[®] and ISSCO's[®] DISSPLA[®] and TELLAGRAF.[®] And Retro-Graphics delivers all of this while retaining the original alphanumerics features of the enhanced terminals.

Thousands of users who have put Retro-Graphics enhancements into action can attest not only to the performance benefits but, importantly, to the often dramatic cost savings over comparable terminals. Savings that have amounted to upwards of 50% and more. Together, high quality and low cost make Retro-Graphics one of the brightest ideas to come along in some time. The idea you can check out for yourself by calling your Digital Engineering distributor. Or contact us direct.



Retro-Graphics " is a trademark of Digital Engineering, Inc. Dumb Terminal® is a registered trademark of Lear Siegler, Inc. Tektronix® and Plot 10® are trademarks of Tektronix, Inc. ISSCO,® DISSPLA® and TELLAGRAF® are registered trademarks of Integrated Software Systems Corporation. DEC " and VT100 " are trademarks of Digital Equipment Corporation

NGG PRODUCT PREVIEW

Development System Increases Productivity and Improves Documentation

A Z8000[™] based multi-user development system, Z-LAB 8000 uses a powerful minicomputer operating system to perform microprocessor development tasks in a microprocessor based system. The Zeus operating system, an enhanced version of the seventh edition of Bell Laboratories' UNIX, is designed specifically for software development and text processing; it provides comprehensive software development and documentation tools, and supports emulation peripherals, to maximize programmer pro-

ductivity and documentation quality. Supporting up to 16 users, the system develops code for all Zilog CPUs.

Zeus features a large user base and a large software base of development related applications, as well as enhancements including file access controls, system generation capability, and a full screen-oriented editor. Its 3-layer architecture includes an operating system kernel, system utilities, and development tools that reduce user time required to develop 16-bit code.

The highly user configurable operating system layer consists of a multi-

user, multitasking environment with a hierarchical file system for efficient file organization. Compatible file, device, and interprocess I/O simplify programming and give programs increased general purpose functionality. The system utilities layer includes a command language comprehensive enough to write programs. A communication program allows the development system to communicate with other Zeus or UNIX based systems. Communication is also provided for emulation devices and development modules. Included in the third layer's development tools are extensive language capabilities, including C, Pascal, PLZ/SYS, PLZ/ASM, a compiler-writing system, and a general purpose macroprocessor. This outer layer also provides text processing capabilities, spelling error detection, and document formatters for printers and phototypesetters.

All the system boards in addition to a power supply are contained in the processor module. The module's Z8001A based CPU board contains 8 serial ports with programmable baud rates, 3 Z8010A memory management units, a parallel printer interface, and EPROM with bootstrap monitor and poweron diagnostics. Also included are a memory controller board, 1 or more 256k-byte memory array cards, an intelligent Z80B based Winchester disc controller, and intelligent Z80B based cartridge tape con-

> troller, and an optional serial I/O controller board. The peripheral module contains a 24M-byte 8" (20-cm) Winchester disc drive, standard 17M-byte cartridge tape drive, and power supply.

> Organized in modular fashion, system hardware supports growth to a 32-bit CPU. All system boards plug into a 10-slot backplane based on the high speed, 32-bit z-Bus Backplane Interconnect (ZBI), guaranteeing the system's future upgrade path. Two versions of the development system are available: model 20 includes a CPU, 2 intelligent controllers, 256k bytes of ECC memory, a 24M-byte

Winchester disc drive, and a cartridge tape drive; model 30 offers 512k bytes of ECC memory and 2 24M-byte Winchester drives.

Hardware options include additional 256k-byte memory boards, up to four 24M-byte Winchester drives, serial I/O controller, CRT terminals, and character and line printers. Planned hardware enhancements include a processor expansion module that increases the number of card slots to 20; 40M-byte Winchester drives that can be mixed on the same controller with the 24M-byte drives; and an intelligent serial I/O controller. **Zilog**, 10340 Bubb Rd, Cupertino, CA 95014.

See at Booth 2309

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32-Bit Minicomputer Handles Large



Programs Without Paging

Model 3230 is a midrange system in the Series 3200 family of Megamini computer systems that approaches the DEC VAX-11/780 in performance and yet is priced comparably to the VAX-11/750. Expandable to 8M bytes of directly addressable main memory, the system allows parallel development of large complex programs without cumbersome paging techniques. Machine characteristics are designed specifically to meet the power and flexibility needs of high performance applications that have cost constraints, and to provide program compatibility with other family members.

The machine incorporates 32-bit internal data paths, allowing parallel processing of data. Memory modules, general purpose registers, and writable/ fixed control store are also formatted in a 32-bit structure. There is a total of 128 32-bit general registers (in 8 sets of 16) that are provided as standard. They include 4 dedicated register sets for handling the 4 external interrupt levels. The remaining 4 sets are allocated by the operating system. The dual-bus architecture provides a high speed machine/machine communications path for interfacing secondary storage devices such as disc and tape units, as well as a medium speed man/machine communications path for interfacing devices such as printers, consoles, and card readers. Integral to the processor is a hardware memory manager that provides memory segmentation, relocation, and protection under operating system control. This device translates a program address into a physical memory address and also monitors all memory accesses to provide write and execute protection of a specified memory block. The technique ensures that a task exists in a fully protected environment.

Cache memory is configured as a 1k-byte direct mapped fast memory, and is organized into 64 blocks, each 16 bytes long. It consists of a high speed bipolar memory residing between the processor and the memory system and provides a significant performance enhancement. Cache implementation reduces the effective access time of main memory from 500 ns to 340 ns, based on an 80% cache hit ratio. The main memory system is made up of 512k-byte modules that achieve an access time of 500 ns. The minimum system has 0.5M bytes; two expansion configurations are available: one a 4M-byte unit and one an 8M-byte unit. Error correction is standard with the memory system.

The DMA I/O subsystem (DIOS) is a high performance, intelligent communications controller for the system. The subsystem offloads the CPU by providing DMA facilities between main memory and multiple-I/O devices that allow data transfers to take place with no processor intervention. The unit can support up to 63 2-wire or 31 4-wire data communications devices, and provide a peak throughput of 100k char/s.

Options include the high performance floating point processor that provides 48 single- and doubleprecision floating point instructions. It also contains eight 32-bit single-precision registers and eight 64-bit double-precision registers. Data can be transferred between single- and double-precision registers for mixed mode calculations. Accuracy is achieved via R-Star rounding that provides higher accuracy than conventional rounding over extended calculations.

Among reliability features incorporated into the system are memory ECC; error logger that keeps a journal of all errors detected through ECC; battery backup; self-test on power-up; multimedia diagnostic programs for processor, memory, and peripherals; and remote diagnostics. **Perkin-Elmer Corp**, Computer Systems Div, 2 Crescent PI, Oceanport, NJ 07757.

See at Booth 726

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Plus you get high-end sophistication like special graphics, software self-test, CRT Saver, even an optional large screen for improved readability in 132-column mode.

Already indebted to your host software investment? The DT 80/3 has keyboard compatibility modes for four popular terminals as a subset of its advanced features. They include our own Datamedia 1521A, ADDS Regent 25, Hazeltine 1420, and Lear Siegler ADM3A. Now you can dramatically upgrade without sacrificing your existing software investment.

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CIRCLE 56 ON INQUIRY CARD



500-MHz LOGIC ANALYZER



Model K500-D features a 500-MHz clocking rate and can record analog signals at bandwidths to 100 MHz. Noise pulses, transitions, and other events can be captured and sampled every 2 ns. Both analog and digital information may be displayed simultaneously, allowing comparison and correlation of 2 types of data in troubleshooting analog/ digital interfaces. The microprocessor based test system has an interactive keyboard and display and is compatible with the IEEE 488 interface bus for use in fully automated testing applications. Other features include 2k words of solid state memory, active high performance probes for each of its 8 channels, self-test routines, and switching instead of linear power supply. For logic analysis users can view up to 8 channels of timing diagrams or display data in binary, octal, hexadecimal ASCII codes, or a combination. Up to 8 timing channels may be recorded and viewed simultaneously, or the user can operate the instrument in scroll mode to record an 8-channel timing diagram 1 signal at a time. Analog capability includes 100-MHz bandwidth by a 4-bit ADC, resulting in resolution of 1 part in 16. The analog waveform can be displayed along with 4 other digital timing signals. Gould Inc, Instruments Div, Biomation Operation, 4600 Old Ironsides Dr, Santa Clara, CA 95050.

See at Booth 941

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NETWORKING SYSTEM FOR PERSONAL COMPUTERS

Allowing up to 64 devices to be attached to an economical high performance local network, Constellation II supports 1M-bit/s data transmission over up to 4000-ft (1219-m) shielded twisted pair. The system accommodates attachment of similar or dissimilar computers and allows for sharing such local resources as hard or floppy disc storage, printers, or gateways. No isolation circuits are required. Any network protocol can be layered onto the network links. The intelligent network interface controller transfers a message of any length error free from node to node without host software intervention. **Corvus Systems, Inc**, 2029 O'Toole Ave, San Jose, CA 95131.

See at Booth 3014

Circle 325 on Inquiry Card

STATISTICAL NETWORK PROCESSOR

A microprocessor controlled data communications device that functions as an intelligent concentrator and statistical time division multiplexer, the SNP-1000 features a multipoint option that allows the user to poll a number of remote sites along a single transmission line. This permits the network designer to optimize telephone line savings in applications where a conventional concentrator, FDM, TDM, or ITDM cannot be effective. The device is available in 2-, 4-, and 8-channel models that concentrate asynchronous inputs into a single high speed output for maximum operating efficiency. It can also be equipped with a command and diagnostics port that provides the capability of monitoring all system functions, and of altering most system operating parameters from a single centrally located console. Features include error checking routines, downline loading of changes in remote site operation from central location, and continuous self-testing. Completely transparent to terminals, CPUs, and software, it can be installed with no change in existing systems. Also on display will be 3 asynchronous limited distance modem products: the 1200bit/s ALD-XR; the ALD-LP with board mounted varistors that protect receive circuitry from high voltage surges; and the LP/XR, an extended range version. Prentice Corp, 795 San Antonio Rd, Palo Alto, CA 94303.

See at Booth 1604

Circle 326 on Inquiry Card

SOFTWARE DEVELOPMENT SYSTEM

System C/70 executes C language and UNIX^R operating system, and also provides a network services computer. Combined with the company's network nodes, it addresses a complete range of distributed processing applica-

tions. All assembler code is replaced with either c language functions or microroutines; the need for translation into assembler language is eliminated. C/70 is a microprogrammable 20-bit computer with a 32-bit microword length. Components include an 8k x 32-



bit micromemory, $1k \ge 12$ -bit dispatch memory, 32k to $1M \ge 20$ -bit macromemory, $1k \ge 20$ -bit register file, and ALU, all connected by source and destination buses. The architecture is specialized for efficient operation of c and UNIX by an instruction mapper and memory management unit. Function calls are performed in about 8 μ s. A number of enhanced program development tools and a complete library of c routines are available. The user can select which c support or c library routines are to be put into microcode. **BBN Computer Corp.** 33 Moulton St, Cambridge, MA 02238.

See at Booth 4500

Circle 327 on Inquiry Card

BOSCHERT. STAYING POWER IN EUROPE.

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BOSCHERT NOW OFFERS THE FIRST U.S. SWITCHING POWER SUPPLY TO WIN VDE 0730 CERTIFICATION.

Regulations of the Verband Deutscher Elektronika (VDE) set tough new operating standards for electronic equipment sold in West Germany and most of the rest of Europe. Now Boschert can help you gain VDE approval for your OEM systems in European markets, with the first American 200-watt switching power supply to comply fully with VDE 0730 safety specifications and meet VDE 0871 noise requirements. Thus improving the marketability of your products in Europe.

Introducing the XL 200-3501 — good news for any manufacturer of microcomputer-based systems. This superefficient switching power supply delivers up to 200 watts of power in a compact, lightweight, field-proven design. Its two jumper-selectable input ranges (95-130V and 190-265V AC), four output posts, and total regulation against power fluctuations make it ideal for word processors, intelligent displays, and the full range of small business computers.

Best of all, our XL200-3501 is here today to supply manufacturing runs of any size or requirement.

So remember, if you're marketing systems in Europe today, two things are certain: VDE 0730 is here to stay — and so is Boschert, with total support for all your power supply needs. From 25 to 1500 watts, from prototype to full production, Boschert leads the way.

For more information on the XL200-3501 or any of our open frame switchers or submodules, write Boschert Inc., 384 Santa Trinita Ave., Sunnyvale, CA 94086. Or call (408) 732-2440.







4-TERMINAL POWER MODULE



The 4T switching power module converts 110 to 220 Vac to an unregulated 50-Vdc output for driving switching 3T regulators. The switching transformer replaces bulky 50/60-Hz transformers and rectifiers with a small, light, and efficient module capable of up to 500-W output power. It meets stringent VDE 0730 safety requirements and is UL approved as well. A terminal block connector allows external section of ac capacitors. Having the same dimensions and mounting as 3T switching regulators, the unit offers low power dissipation and user changeable 110/220-Vac input, and is brownout proof and overload protected. Efficiency is 88% at 500-W output. Average output current ranges from 0 to 12 A; current limit is 15 to 18 A, and switching frequency is 22 to 26 kHz. Output impedance is 0.25 Ω , and inrush current is 36-A peak with cold start, 130-A peak with hot start. Boschert Inc, 384 Santa Trinita Ave, Sunnyvale, CA 94086.

See at Booth 1706

Circle 328 on Inquiry Card

128k-BYTE BUBBLE MEMORY CASSETTE

Plug-A-Bubble is a 128k-byte capacity bubble memory cassette designed to provide permanent memory storage in harsh environments or in critical data storage applications. Each ruggedized cast aluminum cartridge contains the 7110 1M-bit bubble memory component, along with the 7220 controller, and other bubble circuit chips. Up to 2 cassettes can be configured into each system interfacing with standard iSBX module bus. The system includes the capability to operate in DMA mode for flexibility in microprocessor based systems. Measuring 6.1 x 3.6 x 0.80" (15.4 x 9.1 x 2.04 cm), the cassette fits into a holder that measures 1.1 x 3.8 x 7.75" (2.8 x 9.6 x 19.7 cm). Each cassette has a 48-ms average access time and a burst data transfer rate of 12.5k bytes/s. Power requirements are std 5 and 12 V, totaling 12W/cassette. The system offers both the nonvolatile reliability inherent in bubble technology and automatic fire code error correction. Intel Corp, Memory Systems Operation, 1302 N Mathilda Ave, Sunnyvale, CA 94086.

See at Booth 611

Circle 329 on Inquiry Card

DESKTOP BUSINESS COMPUTER WITH 5M-BYTE WINCHESTER DISC

A totally integrated desktop business computer, System 1500 incorporates a 5M-byte Winchester disc drive that transfers data at 5M bits/s and can be configured to appear as one continuous unit with capacity for 5.2M bytes or as two separate 2.5M byte units. A 700k-byte double-sided, double-density flexible disc drive is used for hard disc backup and for program and data transfer via removable flexible diskettes. Eight diskettes back up the full Winchester capacity. An automatic error correction feature allows the disc controller to automatically correct up to 11 bits per physical sector. The system includes a high performance keyboard with 60-key typing array and 13-key adding machine cluster, up to 64k bytes of RAM, 12" (30-cm) CRT formatted in 24 lines of 80 chars/s, 8-bit z80 processor, and communications and printer interfaces. The system uses CP/M operating system and applications software packages provided with the company's other business computers. Digilog Inc, Microcomputer Div, Babylon Rd, Horsham, PA 19044.

See at Booth 1341

Circle 330 on Inquiry Card

DIGITAL IMAGE PROCESSING SYSTEM

Designed as an interactive standalone image processing system operating at 0.03 s, Vision One/10 has memory capacity of up to four 512 x 512 8-bit images and up to four 512 x 512 1-bit graphic planes. An LSI-11/02 computer controller with a P/ROM operating system is used, with additional RAM space available for user code. An inline realtime pipeline processor provides brightness enhancement and color modification. The system's pseudocolor processor has 8 bits to 24 bits out, with 8 blue, 8 red, and 8 green. Zoom feature



Carter warder

provides 1x, 2x, or 4x image enlargement. There is also a software operated histogram and bilinear zoom. Options include monochrome high resolution vidicon camera, 10-MHz ADC, small area brightness or color control, and image combination hardware to add, subtract, multiply, or divide two 512² images in real time. **Comtal/3M**, 505 W Woodbury Ave, Altadena, CA 91001.

See at Booth 2504

Circle 331 on Inquiry Card



Meet the Tiger with a bigger bite.

Introducing the remarkable 132-column Paper Tiger[™] 560. The first full-width matrix printer to give you fully formed characters for a low \$1695.*

The new 560 features a staggered ninewire ballistic type print head that overlaps dots in both horizontal and vertical planes. It bi-directionally prints up to 150 dense, text quality characters per second.

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presents a breakthrough in matrix printing ering the user excellent print quality with ce of a matrix printer. Employing a uniq red column" head manufactured by Integr creates high quality printouts by overlap

Paper Tiger 560 Print Sample

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VIDEO TERMINAL



Designed to enable existing and prospective users of the DEC VT52, Hazeltine 1500, and ADM 3A terminals to obtain all facilities of these units, the 4420 also offers switchselectable emulations in enhanced mode, improved video quality, greater operator convenience, and workstation layout flexibility. It also provides user control of formatting and video attributes, screen editing, smooth scrolling, and support for local printing and semigraphics facilities. The terminal consists of a compact display unit whose viewing angle is adjustable to suit the operator and a separate (serially connected) low profile keyboard. Nonreflective display gives 24 lines of 80 10 x 8 dot matrix chars. Char sets are available for major European and American requirements, each supported by an appropriate national keyboard style. Intelligence is based on the F-8 microcomputer system and is programmed to produce the emulations and additional functions in enhanced mode. The program also enables features traditionally handled by mechanical switches and PCB jumpers to be selected and changed by use of commands typed at the keyboard. Connection to the host is via a serial link with a choice of switch-selectable interface and protocol options. A local printer may also be connected using the software controlled printer port, enabling local dumping of screen contents or printing of data from the host, either alone or in parallel with display of data. Facit Inc, 66 Field Point Rd, Greenwich, CT 06830.

See at Booth 918

Circle 332 on Inquiry Card

SINGLE-CARD MODEM

CM2020 1200-bit/s direct connect modem measures 30 in² (194 cm²) and is compatible with Bell 2025. Microprocessor based unit features onboard auto-dial and auto-answer. Onboard test circuitry enables either self-testing or testing via DTE. The board also provides frequency sensitive carrier detect circuitry, and selectable call origination that supports auto-dialing, dial-through, and conventional dialing. Intertel, 6 Shattuck Rd, Andover, MA 01810.

See at Booth 874

Circle 333 on Inquiry Card

READ/WRITE MAGNETIC HEADS

A thin film 18-channel 0.5" (1.27-cm) tape head capable of greater than 0.5-mV output when operated in GRC (group code recording) mode, at 18,084 flux reversals/in (7119/cm) and 100 in/s (254 cm/s), will be shown. Also exhibited will be streamer heads, flexible disc heads, and 0.5" (1.27-cm) heads. Streamer heads for Winchester disc backup feature 2-channel serpentine with optional erase. The line is capable of 2, 4, 8, or 16 tracks on 0.25" (0.64-cm) tape. Flexible disc heads are patent pending Z-axis double-sided models with 96/100 tracks/in (37/39/cm). The 0.5" heads feature LTC lifetime ceramic tape surfaces, guaranteed to outwear hard chrome by a factor of 3 to 1. These heads are designed to be operational at 6250 bits/in (2460/cm) up to 200 in/s (508 cm/s) in GCR mode. Nortronics Co, Inc, 8101 Tenth Ave N, Minneapolis, MN 55427.

See at Booth 511

Circle 334 on Inquiry Card

EXPANDED KSR CRT TERMINAL



An enhanced version of the company's Ambassador line, Ambassador II 15" (38-cm) CRT terminal triples the number of programmable function keys to 48 for a total of 64 downloadable functions, and increases the number of bytes available for downloaded strings. A new function key initialize mode loads keys PF1 to PF12 with shift level functions. The define area qualification table has been expanded to allow up to 380 individual areas on the page to be defined as: accepting all keyboard input, numeric only, concealed entry, right justified, page tab stop, protected, or protected and guarded from transmission. An alternate cursor mode allows the host to write to the terminal via a blind cursor without interrupting the operator. Selfdiagnostics now include indication of checksum error or memory failure. The new features are added to the std capabilities of the previous version such as 60-line, 4800-char display and keyboard selectable baud rates of 110 to 19,200. Users of the previous versions may purchase updated ROMs to retrofit to their equipment. Ann Arbor Terminals, Inc, 6175 Jackson Rd, Ann Arbor, MI 48103.

See at Booth 208

Circle 335 on Inquiry Card



Forget about compatibility with the Multibus, Q bus, S-100 bus, Unibus or the host of others. Most systems have an RS-232 data port. So select an RS-232 compatible peripheral from Columbia Data Products and leave the bus confusion to others.

System compatibility isn't all you get with CDP peripherals. You also get microprocessor intelligence in our floppy disk, cartridge tape or RAM based storage systems.

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CIRCLE 60 ON INQUIRY CARD



RASTER MATRIX LINE PRINTERS

Model 150 prints at 150 lines/min and is field upgradable to 300 lines/min; the 300 prints at 300 lines/min and features non-stop printing. Both models space lines vertically at 6 and 8 lines/in (2 and 3/cm) and print on 1- to 6-part forms.

A graphics mode permits plotting with a resolution of 60 x 72 dots/in (23 x 28/cm). Normal printing is at 10 chars/in (3.9/cm). A compressed print mode shrinks character width to 16.5 chars/in (6.5/cm) so that 132 characters fit on 8.5" (21.6-cm) wide forms or 220 characters can be printed on 14.875" (37.8-cm) wide forms. Print matrix is 9 x 7 for std uppercase charac



ters and 9 x 9 for characters with descenders. The 300 has 2 independent printheads; a microprocessor shuts down either if a problem is detected so that users can continue operating until the malfunction is corrected. Other design features include endless loop ribbon cartridge with single stepper motor drive, dual microprocessors, multiple-character sets, compressed print mode, software selectable graphics mode, and full forms control, including forms length switch and down loadable UFU. Units have both a std RS-232 serial interface with multiple-protocol selection and a Centronics compatible parallel interface. Serial baud rate can be operator selected from 300 to 9600 baud, and a 7-line character buffer maximizes throughput for either interface. **Trilog, Inc,** 17391 Murphy Ave, Irvine, CA 92714.

See at Booth 1728

Circle 336 on Inquiry Card

PROCEDURE LIBRARY

Econometrics and Time-Series Library (SAS/ETS) offers full range of forecasting, modeling, and reporting tools for business and economic applications. FORECAST procedure provides an automatic method of generating forecasts for hundreds of variables. STATESPACE and ARIMA procedures analyze and forecast multivariate and univariate time-series data, respectively. COMPUTAB procedure organizes data into tabular form and prints row and column reports such as balance sheets, income statements, and other summary reports. Financial and econometric models are handled by modeling procedures for estimating, simulating, and predicting linear and nonlinear systems. Other system features include seasonal adjustments, picture formats, and financial functions. The SAS software system, required to use SAS/ETS, runs on IBM 360/370/303x/43xx and compatible machines under OS, OS/VS, and VM/CMS. SAS Institute Inc, PO Box 8000, Cary, NC 27511.

See at Booth 116

Circle 337 on Inquiry Card

DATA LINE MONITOR STORAGE SUBSYSTEM

MSU III mass storage unit is a dual-floppy disc companion to the DLM III data line monitor that expands the monitor's applications in unattended monitoring situations and for offline fault analysis of long data streams. The turnkey tech control solution provides, in a self-contained package, automatic monitors and alarms, network diagnostic facilities, network reconfiguration capabilities, and extra cabinet storage space for modem and cables. The microcomputer based units provide operating simplicity as well as expansion capabilities needed by sophisticated data communications applications. **Digilog Systems, Inc, Network Control Div,** Babylon Rd, Horsham, PA 19044.

See at Booth 1341

Circle 338 on Inquiry Card

14" WINCHESTER DISC DRIVE



Marksman M80 Winchester disc drive with three data surfaces and two 14" (36-cm) discs has a capacity of 81.96M bytes. Specs include 24k bytes/track, 480 tracks/in (188/cm), and 7545 bits/in (2970/cm). Data transfer rate is 960k bits/s. Access times are 20 ms (min), 50 ms (avg), and 100 ms (max), and latency time is 12.5 ms (avg). Options include an intelligent Marksman interface that provides the user with a means of attaching the drive to his particular CPU. **Century Data Systems, Inc**, 1270 N Kraemer Blvd, Anaheim, CA 92803.

See at Booth 2104

Circle 339 on Inquiry Card

UPGRADED RECEIVE-ONLY PRINTER TERMINAL

Replacing the earlier version of the 1201 printing terminal, Miniterm^R model 1201 offers as standard a 2k buffer, polling, self-test, serial interface, and selectable 50/60-Hz international power supply. Options now available include high resolution plotting, answerback, 4k buffer, 20-mA current loop interface, and 9600-baud communications. Print speeds are up to 50 chars/s. As in the previous model, the new version offers switch-selectable 80/132-col format, adjustable print darkness, 96-char u/lc ASCII code with underscore, remote terminal reset, and controls for paper feed, online/offline, and reset. **Computer Devices, Inc**, 25 North Ave, Burlington, MA 01803.

See at Booth 1232

Circle 340 on Inquiry Card



MINIATURE DISC DRIVE



Using thin film read/write heads, the ST512 5.25" (13.34-cm) micro-WinchesterTM drive offers 12.76M-byte unformatted and 10M-byte formatted storage capacity on two platters. Recording density is 10,202 bits/in (4016/cm) on a total of 1224 tracks at 270 tracks/in (106/cm). Thin film heads do not require write precompensation on innermost tracks. Avg latency is 8.33 ms, avg seek time is 100 ms, and settling time is 50 ms. Drive rotates at 3600 r/min and requires only 5 and 12 Vdc $\pm 5\%$. Reliability figures for the drive include soft error of 1 in 10¹⁰ bits read, hard error of 1 in 10¹² bit read, and seek error rate of 1 in 10⁶ seeks. MTTR is 30 min; MTBF is expected to be 11k power-on hours. The unit is compatible with the company's 6.4M-byte model ST506 drive. **Seagate Technology**, 360 El Pueblo Rd, Scotts Valley, CA 95066.

See at Continental Plaza Hotel

Circle 341 on Inquiry Card

DISTRIBUTED PROCESSING SYSTEM

Sovereign uses a multiple processor architecture to provide onsite information management. Its design allows users to assign each task to a separate computing element with its own memory and processing capability. It complements the central data processing center to make the mainframe system more efficient by providing preprocessed data, greater data accessibility, and lower information costs to remote users. Processing terminals in a system can work independently or together. The file processor in the system has its own operating software for maintaining, sorting, updating, retrieving, and outputting records and files. User programming is accomplished using an enhanced version of BASIC or an advanced version of ANSI 74 COBOL. Communications to the mainframe can be either batch or interactive, using various IBM protocols or those of other systems. In addition, the system can communicate concurrently with more than one mainframe or other computer systems from the company. Each terminal acts as a communications processor. Microdata Corp, 17481 Redhill Ave, Irvine, CA 92713.

See at Booth 852

Circle 342 on Inquiry Card

FIBER OPTIC COMMUNICATIONS SYSTEM

Consisting of optical link communications line interface and modem expander, system operates in full-duplex mode over a distance of 2 km. The optical link communication line interface is designed to link together 2 OP-1 display computers or any synchronous or asynchronous devices using standard RS-232 communications ports. The interface provides virtually noise free operation, high speed transmission, electrical isolation, and data security. The link transfers data at any switch-selectable synchronous baud rate from 9.6k to 2.46M using built-in clock generator, or from 9.6k to 300k baud using external clocks acquired from the 2 devices. It may also run at asynchronous rates from dc to 125k. The modem expander allows up to 4 or 8 OP-1 display computers to be interfaced into a standard modem or optical link line interface. It can be interfaced with any asynchronous or synchronous baud rate from 9.5k to 2.5M as well as any asynchronous baud rate from dc to 125k. The expander broadcasts messages from the host display computer to a max cluster of 8 display computers. It can also accommodate an optical line interface, allowing a cluster of computers to be located several thousand feet from the host. Ontel Corp, 250 Crossways Park Dr, Woodbury, NY 11797.

See at Booth 2805

Circle 343 on Inquiry Card

10M-BYTE 8" HARD DISC SYSTEM

Discus M10 is available for S-100 or Cromemco machines. Supplied complete with disc controller, cables, fan, power supply, cabinet, and CP/M operating system, the unit stores 10M bytes on an 8" surface. Up to 3 additional drives allow system storage of more than 40M bytes. The sealed media hard disc drives use S-100 controllers that incorporate intelligence to supervise all data transfers through 4 I/O ports (command, 2 status, and data). Transfers between drives and controllers are transparent to the CPU. Controller can also generate interrupts at the completion of each command, significantly increasing system throughput. Sectors are individually write protectable for multiuser environments. **Morrow Designs**, 5221 Central Ave, Richmond, CA 94804.



See at Booth 146 Circle 344 on Inquiry Card

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REALTIME NETWORK CONTROL SYSTEM



Network control information is provided in real time by the RM200. With up to 20 measures collected simultaneously and continuously for every line, control unit, and device in the network, users can identify network and line availability, response time categorized into network and host delays, retransmission measurement for line error analysis, and a variety of general measures such as messages statistics and polling data. Coupled with a network information data base of the line names, applications, line groups, and network configuration, the unit offers realtime color graphics displays, audible alarms based on user selected threshold values, and realtime hardcopy reports for trouble ticketing applications and archival storage. A basic menu and function key approach make it easy to view global network status or to zoom in on specific problem area. Support for BSC and SNA/SDLC as well as both synchronous and asynchronous lines make the unit applicable to many environments. Tesdata Systems Corp, 7921 Jones Branch Dr, McLean, VA 22101.

See at Booth 508

Circle 345 on Inquiry Card

BUSINESS GRAPHICS PACKAGE

Tell-A-Graph version 4.0 allows a user with no programming skills to create professional looking charts and graphs using conversational English commands. It provides improved graphics quality output and rigorous handling of char spacing in text strings. Package features fully annotated horizontal and vertical bar charts, enhanced pie chart design, sophisticated blanking capabilities, calendar axes, and the ability to create European graphs. It automatically generates a legend, scales axes to fit data, and centers and positions title and axis labels. The device independent package will draw on any graphics device that can be driven by a program on a host computer. Odyssey, an integrated system of mapping programs and geographic data analysis developed by the Harvard Lab for Computer graphics and Spatial Analysis, and Disspla, a general purpose graphics library of FORTRAN subroutines, will also be demonstrated. Integrated Software Systems Corp, 4186 Sorrento Valley Blvd, San Diego, CA 92121.

See at Booth 2513

Circle 346 on Inquiry Card

SMALL WINCHESTER DISC DRIVE

Cynthia D 505 is a 5.25" (13.34-cm) fixed disc drive packaged in the same dimension as an industry standard mini-floppy drive that stores 6.38M bytes unformatted. Access time is 170 ms avg, and data transfer rate is 5M bits/s. The drive has 7690-bit/in



(3028/cm) recording density and track density of 255 tracks/in (100/cm). Also shown are compatible disc drive subsystems for DEC LSI-11 Qbus and PDP-11 Unibus systems. **Cii Honeywell Bull**, 200 Smith St, Waltham, MA 02154.

See at Booth 563

Circle 347 on Inquiry Card

TAPE READER/PUNCH STATION



Designed to save space while offering advanced features, the desktop sized 4601 measures 19 x 10 x 5" (48 x 25 x 12.7 cm) and weighs 14 lb (6.3 kg). Single unit performs punching and reading functions simultaneously and/or independently. Featuring a microprocessor controlled interface with buffer memory, the station also has skip-delete and full tape editing features, an RS-232-C interface with a choice of 110, 300, 600, or 1200 baud rates, and low noise level. It handles all types of mylar and paper tape. The 75-char/s punch has an MTBF that exceeds 100M char. The reader features a carriage return delay and is able to read up to 120 char/s even when the tape is worn or of poor quality. In half- or full-duplex mode, the reader can send to either DTE or DCE, or both, and punch provides hard copy of incoming data. In local mode, it communicates with DTE and offers char at a time, line at a time, backspace, and skip editing facilities. The punch provides hard copy of data received from either DTE or reader. GNT Automatic Inc, 1560 Trapelo Rd, Waltham, MA 02154.

See at Booth 3004

Circle 348 on Inquiry Card

Introducing the Board-And-A-Half connector.

Ahhh, finally, an effective two-piece stacking connector system. No more need to choke a board to the point of death before designing in more capacity. A board-and-a-half. Mother and daughter—with the daughter stacked no more than .510" tall. It's called the Viking Stack-Con. Another excellent idea very neatly done.





CIRCLE 62 ON INQUIRY CARD



MINI-FLOPPY BASED COMPUTER SYSTEM



A Constellation series microsystem, SCORPIO is packaged with a DEC LSI-11/2 CPU, 64k bytes of memory, serial I/O port, and 2 double-sided, double-density 5.25" (13.34-cm) mini-floppy disc drives. The system provides 1.8M bytes of disc storage as opposed to 1M bytes for DEC systems. The drive has an average access time of 177 ms, a 0.25-s start-up time, and a 2-ms track to track step rate. This allows users to retrieve information on a realtime basis. The read mechanism provides increased disc life and greater reliability as an added feature. Emulating DEC's RX01 singlesided, single-density configurations and RX02 single-sided, double-density configurations, RXV21 drive operates in RX03 double-sided, double-density floppy systems providing twice the capacity of the RX02. This drive is included in the Gemini that will also be on display and which has LSI-11/2 CPU, 64k-bytes memory, DLV11 serial asynchronous I/O port, and 2 floppy discs. The RXV21 based Gemini Plus has an LSI-11/23 CPU, 256k bytes memory, QLV11 quad serial synchronous/asynchronous 1/0 port, and 2 floppy discs. General Robotics Corp, 57 N Main St, Hartford, WI 53027.

See at Booth 1665

Circle 349 on Inquiry Card

HANDHELD CONTROL/DISPLAY UNITS

HT/20 is a low cost control display device that features a tactile feel membrane keyboard that enhances operations in a severe environment. The compact unit can be panel mounted, handheld, or desktop. It provides an 18-element full-alphanumeric LED starburst display and uses front mounted shift keys. An RS-232-C interface is std; other industry interfaces are available as factory set options. The entire 128 ASCII code set can be generated and transmitted by the simple 24-key front panel. The unit measures 18 x 10.6 x 3.8 cm and provides 120-char/s std, or optional 30- or 960-char/s operation. Full- or half-duplex is available. Termiflex Corp, 17 Airport Rd, Nashua, NH 03063.

See at Booth 1350

Circle 350 on Inquiry Card

3-DIMENSIONAL GRAPHICS SOFTWARE

Locally intelligent 3-dimensional instruction set operates the company's 5216 display computer and receives instructions and programs from a host computer, 5116 display editor, or disc. The user can create, edit, display, and store in the hierarchical 3-D data base. Programmable with Forth or 8086 assembly language, the system supports both binary and ASCII instructions together with user programmable function keys, graph tablet, trackball, and joystick. It displays such primitives as surfaces, prisms, spheres, vectors, and text; gives shaded surfaces with hidden surface removal; provides logical entity detection; and supports hue intensity saturation, RGB, or specified pixel values. **Aydin Controls,** 414 Commerce Dr, Fort Washington, PA 19034.

See at Booth 790

Circle 351 on Inquiry Card

HIGH SPEED MATRIX PRINTERS

Office systems printers models OSP/120 and /130, for word processing, data processing, and communications applications, incorporate built-in automatic cut sheet feed, manual feed, and tractor feed in a single mechanism, and offer

faster throughput than comparable serial printers in either application. The printers also fill line printing requirements in the 300to 600-line/min range and provide graphics, multifont storage, fully formed chars, OCR printing, and labeling. Using the company's proprietary printhead technology, the machines offer a 600char/s rate for draft



output and a 150-char/s rate for letter quality output-12 times faster in draft mode and 3 times faster in letter quality mode than daisywheel printers. A patent pending triple paper path provides for automatic cut sheet feed, handform feed, and tractor feed with automatic bail control. Its paper exit path allows cut sheet paper output to be collated with the first page in front. All operator control is by pushbutton. Char fonts are changed without replacing print elements. Electronic fonts are stored in ROM or downline loaded into RAM, eliminating the need to change wheels, balls, or bands. The serial printers are suited to high speed communication printing at 2400 baud or higher without software considerations because of low print speed. Printhead life exceeds 1G chars. Interface is serial RS-232; Centronics, Dataproducts, parallel ASCII, current loop, and several communications protocols are optional. Florida Data Corp, 600D John Rodes Blvd, Melbourne, FL 32935.

See at Booth 3108

Circle 352 on Inquiry Card

POWER TO YOUR COMPUTER



Continental Power Systems presents a unique new design in uninterruptible power sources for all mini, small business and small/medium computers.

The PoweRotor ™ UPS System keeps your computer on-line through common power problems such as momentary interruptions, erratic voltages and transient spikes. Yet the PoweRotor generator maintains absolutely constant output frequency essential to computer operation. During a utility outage, the system provides 10 to 30 seconds ride-through for orderly downsequencing or switching to back-up power.



- Installation is easy, with only small footprint area required.
- Lower installed cost than static inverter/battery systems.
- Superior ride-through over motor generator sets.
- Only UPS with 3 year warranty. Get the complete story

on the better UPS from Continental Power Systems, Inc., One Landmark Square, Stamford, CT 06901. 800-243-9145.



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UNINTERRUPTIBLE POWER SYSTEMS

Providing computer quality power for small minicomputer and microcomputer applications, Mintaur[™] series 2.5-kVA systems offer an optional (internally packaged) solid state or electromechanical transfer switch. The system provides 125% overload for 15 min, 150% for 1 min, and 1000% for 5 cycles via the transfer switch. It delivers full-rated power over a temp range from - 20 to 50 °C. The system is designed for operation at 120 Vac and includes an output voltmeter, battery ammeter, and low battery alarm. Protection includes output short circuit, current limiting, and thermal protection. Proprietary circuitry protects the SCRs and eliminates need for fuses. The UPS includes an inverter operating at 87% efficiency. Battery charger and transfer switch assemblies are plug-in assemblies. Measuring 14 x 19 x 19" (35 x 48 x 48 cm), the system can mount in a standard 19" (48-cm) equipment rack. An optional rack mountable battery system in a 10" (25.4-cm) module is available and supplies up to 15 min of reserve power. Nova Electric Manufacturing Co, 263 Hillside Ave, Nutley, NJ 07110.

See at Booth 672

Circle 356 on Inquiry Card

COLOR GRAPHIC COMPUTER

Computer based CGC 7900 color graphic system has a 16-bit MC68000 processor and a 19" (48-cm) CRT, and can support a 10M-byte Winchester disc drive and 2 doubledensity flexible disc drives within a single cabinet. The processor features an ALU capable of both 32- and 16-bit operations. RS-232 and **RS-449** communications ports are available with selectable transmission speeds to 19.2k bits/s. Both ports have fully buffered input and out-



put. The CRT has 1024 x 768-dot resolution and viewable graphics memory of 1024 x 1024 dots. Flicker free display is provided by 30-Hz interlaced refresh rate and long persistence CRT screen. Bit map memory planes and color lookup table enable over 16M color combinations with 256 max displayable at any one time, including 256 shades of gray. Sixteen color planes max can be configured, allowing the system to have two completely independent full-image memories. **Chromatics, Inc,** 2558 Mountain Industrial Blvd, Tucker, GA 30084.

See at Booth 3007

Circle 353 on Inquiry Card

WINCHESTER DISC DRIVE



Designated DISKOS 15450, the 158M-byte 14" (35-cm) disc drive measures 7 x 17 x 20" (17 x 43 x 50-cm) and weighs 57 lb (25 kg) with built-in power supply. It uses Winchester technology with track density of 960 tracks/in (377/cm). Units having capacities of 34M and 68M bytes and three 8" (20-cm) drives have the same interface. Average head positioning time for the 158M-byte drive is 40 ms. Also to be displayed are a 70M-byte 8" drive that also uses the 960-track/in density to achieve high capacity in a unit having the same dimensions and mounting provisions as a standard 8" floppy drive and provides an average head positioning time of 42 ms, and the SMART interface that incorporates disc controller functions and includes error correction, expanded DMA capability, and sector interleaving. Priam Corp, 3096 Orchard Dr, San Jose, CA 95132.

See at Booth 4704

Circle 354 on Inquiry Card

SINGLE-BOARD EMULATING CONTROLLERS

Spectra 20, for Data General NOVA and ECLIPSE offers full multifunction emulation of the 6067 disc and 6021 tape subsystems under RDOS, AOS, IRIS, and BLIS/COBOL. Spectra 21, for Digital Equipment Corp's PDP-11, provides full multifunction emulation of the RM02/RM05 disc and TU10/TM11 tape subsystems under RT11, RSX-11M, RSTS/E, and UNIX operating systems. The units replace separate disc and tape controllers, attaching up to 4 SMD disc drives and up to 8 formatted tape drives without modifying operating system software. They support disc transfer rates up to 2M bytes/s, and tape transfer rates up to 320k bytes/s. Separate buffering for disc (3-sector) and tape (64-byte) allows simultaneous disc and tape transfers at full speed while eliminating data late errors. Dual bipolar microprocessor design simultaneously controls CPU, disc, and tape interfaces. Five versions of Spectra 20, plus 4 versions of Spectra 21, support 100" (254-cm)/s, 0.5" (1.27-cm) streaming or std start/stop formatted tape drives. Spectra Logic Corp, 1227 Innsbruck Dr, Sunnyvale, CA 94086.

See at Booth 3209

Circle 355 on Inquiry Card

"As OEMs discover the advantages of Quantum 8-inch Winchester drives, the demand grows daily. In Manufacturing, we're prepared to meet high-volume OEM commitments."

A very manufacturable disk drive.

Quantum's 10, 20, 30 and 40megabyte Q2000 disk drives were designed to be built in high volume at low cost.

Working as a team, Quantum design and manufacturing engineers created a drive that gives you better performance than the industry-standard Shugart SA1000, yet can be manufactured with simple, low-cost parts and fast, efficient production methods.

Low-cost, high-volume production.

To meet your low-cost, highvolume delivery requirements, we designed our manufacturing process as carefully as we designed the drive itself. Our unique conveyorized "cleanair tunnel" combines the best of proven techniques for Winchester drive assembly. The drive is assembled on a conveyor line, so production is more efficient than with independent assembly stations. And the laminar-flow clean-air tunnel completely eliminates the need for a large, expensive "clean room," cutting production costs and increasing worker efficiency.

Specially-designed automated testing equipment thoroughly exercises each drive through all its functions, to assure highest quality while keeping labor costs down.

Every manufacturing operation is planned for easy, smooth ex-

-Harold C. Medley, VP-Manufacturing, Quantum Corporation

pansion to meet growing OEM requirements.

In short, we're geared for lowcost, high-volume production of quality disk drives that we're proud to deliver to you.

Get to know Quantum now.

From manufacturing and engineering to management and customer service, Quantum has the very best people in the disk drive industry today. People who can help you plan an affordable growth path for your small computer systems.

For details on Quantum low-cost 8-inch Winchester drives, call Bob Teal, Quantum Corporation, 2150 Bering Drive, San Jose, CA 95131, phone (408) 262-1100.





ASSOCIATE PROCESSOR FOR PDP-11



MIPROC-16 AP, a complete software and hardware package, offloads preprocessing, postprocessing, and I/O handling from the host computer. It functions as a separate computer system operating on direct memory access arrangement with any Unibus^R or Q-bus^R PDP-11. A software handler links the host and associate processor, providing an easy way to shift programs and data on a DMA link. Software for the unit is developed on the host using a Pascal compiler that can produce both AP and PDP-11 programs. A macro assembler is available for high throughput requirements. A hardware floating point processor operates in parallel with normal instructions, performing a floating point multiply in 2.75 μ s typ. The processor can perform 4M instructions/s with 177 instructions available. Interrupt handling of 750 ns with 3 μ s for complete context switching makes it suitable as an I/O handler for frontending the host. The DMA transfer rate of up to 20M words/s allows creation of large buffers that enhance throughput between the 2 computers. The unit will operate in conjunction with RT-11, RSX-11M, IAS, and VAS, on any DEC PDP-11 computer from -11/03 to VAX-11/780. Plessev Microsystems, 19546 Clubhouse Rd, Gaithersburg, MD 20760.

See at Booth 256

Circle 357 on Inquiry Card

EMULATING DISC CONTROLLER



Single-board disc controller for 16- and 32-bit Perkin-Elmer minicomputers emulates mass storage module disc controllers. Designated EDC23, it can support as many as 4 SMD disc drives, including Winchester types, with capacities up to 675M bytes/drive. Unmodified P-E operating systems, including OS/16 and OS/32, run the controller. However, a standalone pack formatter/controller diagnostic is included

VIDEO DISPLAY TERMINALS

OPTI 900 model 940 features 16 operator programmable function keys, up to 12 independent scrolling regions, 80- and 132-col display formats, and extensive character verification. Options include 1 or 3 pages of display memory, tiltable display, operator changeable display filters, and graphic character sets. The screen can be divided into as many as 12 independent scrolling regions with 2 vertical segments and up to 6 horizontal segments. Each region can independently display separate blocks of information simultaneously, allowing the operator to compare data and transmit specified data from a single region. The terminal's detached keyboard divides clustered keys into typewriter, numeric, editing, and function keys. Character attributes include double-high, double-wide, and double-high/wide. Operators may dim or brighten the display with a multistep contrast control. The terminal offers a 128 ASCII displayable set with a 7 x 9 dot matrix font in a 9 x 11 cell, permitting descenders and underlining. The unit communicates with std EIA RS-232-C interface, offers asychronous full- or half-duplex, and has an auxiliary output port for hardcopy printout. Selectable transmission speeds range from 110 to 19;200 bits/s. Two 256-char FIFO buffers prevent data overflow. Texas Instruments Inc, Digital Systems Group, PO Box 1444, Houston, TX 77001.



See at Booth 1101 Circle 358 on Inquiry Card

for enhanced testing capability. The controller can support any combination of drive capacities (80M, 96M, 300M, or 675M bytes/drive), and most combinations of drive types, without P/ROM changes. Any mix of 4 MSM, CMD, SMD, FMD, or MMD drives can be accommodated. High speed bipolar LSI design enables the unit to be packaged on a single 15" (38-cm) board, eliminating interconnections and reducing power consumption for low cost and high reliability. In large systems, this construction minimizes the need for an extension chassis and interconnecting hardware. Additional features include data error control, multiple sector transfers, full sector buffers, sector interleaving, dualaccess capability, header error control, and data error recovery. **MiniComputer Technology**, 2470 Embarcadero Way, Palo Alto, CA 94303.

See at Booth 982

Circle 359 on Inquiry Card
Microcontrol Mastery with Signetics 8X300

Compact floppy disk controller handles multiple drives and formats.

How one design can meet several goals in firmware.

Today's floppy disk controllers need more than high-performance interface capability. That's why the goals for a design must be to

maximize flexibility and minimize board space. With enough performance for tomorrow's needs.

One approach—a programmable, intelligent I/O controller built around the 8X300 microcontroller and the 8X330, a new floppy disk controller chip achieves these goals.

Flexibility is achieved because the 8X330 can handle multiple disk

drives in any combination of single/double density on 5¼ or 8 inch media. With either standard or non-standard track formats.

The on-board 8X300 microcontroller minimizes host overhead by implementing userdefined macro commands. Designed-in flexibility also allows error correction within IBMcompatible formats. And, bipolar performance meets next generation drive requirements with 1 megabit/second data transfer rates. The 8X330 is the first floppy disk controller chip to integrate the PLL data separator and write precompensation. Result: board space is



Compact floppy disk controller occupies less than half of a standard 7"x12" PCB. A complete controller based on Signetics' 8X330/8X300 can consist of only 10 chips and a host interface.

minimized. An entire double-sided, doubledensity, dual drive disk controller with RS232 interface requires less than 30 square inches.

Greater flexibility, smaller size, and lower cost. All made possible by the 8X300 microcontroller and the new 8X330 floppy disk controller from Signetics. Find out how you can put Signetics' Microcontrol Mastery to

work in your system. Write us today. Or call any Signetics sales or distributor office. Signetics Corporation, 811 E. Arques Ave., P.O. Box 409, Sunnyvale, CA 94086. (408) 739-7700.



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Multiple Technologies from 8 Divisions: Analog, Bipolar Memory, Bipolar LSI, MOS Memory, MOS Microprocessor, Logic, Military, Automotive/Telecom

To: Signetics Publicat P.O. Box 409, Sun	ion Services MS27, nyvale CA 94086	811 E. Arques Av CD44	е., 81
 Please send technik 8X300 and 8X330 	ical information on t	he	
□ I need a more deta Bipolar LSI specia	iled explanation. Ple alist contact me toda	ease have a 1y at:	
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Address		MS	
City	State	Zip	



MICROPROGRAM CONTROLLER FOR VAX AND UNIBUS SYSTEMS

A replacement for the DEC DH11, the DH/DM microprogram controller meets communications needs for VAX and other Unibus systems. It connects any standard Unibus to 16 asynchronous communications lines, provides DMA output

capabilities, and is software compatible with the DH11 and DM11-BB. The device fits 16 lines on a single hex-width board that plugs into any standard SPC backplane slot.



Each unit stands alone and runs independently, and each presents one unit load on the bus. Power requirements are 5 V at 4.4 A, 15 V at 0.2 A, and - 15 V at 0.2 A. The controller design incorporates USARTS with internal baud rate selection and onboard clock. Programmable line parameters include 5-, 6-, 7-, or 8-bit character length, 1 or 2 stop bits for 6-, 7-, or 8-bit chars, 1 or 1.5 stop bits for 5-bit chars, odd, even, or no parity, full-duplex operation, and 0- to 9600-baud transmitter/receiver speeds plus 19.2k baud (replaces External A) and External B. Modem control is std on all lines for use as required. Onboard switches for address and vector selection eliminate jumpers, and diagnostic loopback connectors are built-in. A P/ROM set can be changed to accommodate proprietary OEM applications. Improved silo depth, four times that of the DH11, and transparent silo handling reduces system loading. Able Computer, 1751 Langley Ave, Irvine, CA 92714.

See at Booth 2608

Circle 360 on Inquiry Card

6800/6809 MOTHERBOARD

With the same Classy Chassis as 6800 systems, 6809 systems offer a 25-A ferroresonant transformer, fifteen 50- and eight 30-pin bus slots, a minimum of 32k of static RAM, and choice of I/O cards. System monitor options include GMXBUG 09 monitor/debugger and SWTP's SBUG-E monitor. The SS-50 processor board features selectable processor clock speeds of 1, 1.5, and 2 MHz, and has provisions for onboard devices, including a 9511 or 9512 arithmetic processor, 6840 programmable timer, time of day clock with battery backup, 1k of scratchpad RAM that can be CMOS with battery backup, and 4 PROM/ROM/RAM sockets that can hold up to 32k of onboard software. Memory management options include enhanced dynamic address translator and SWTP compatible DAT. Extended addressing allows the processor to address up to 1M bytes of memory space. Running on the system will be Flex, Uniflex, OS9, Forth, and other software, as well as applications programs such as Stylograph. The company will also show its graphics board and DMA controller for 5 and 8" (13 and 20-cm) drives. Gimix, Inc, 1337 West 37th Pl, Chicago, IL 60609.

See at Booth 971

Circle 361 on Inquiry Card

5.25" WINCHESTER DISC DRIVE

Model RMS 512 offers 12.72M-byte unformatted storage capacity on 4 platters, and requires less than 20-W power; in standby power save mode, drive dissipates only 14 W. Actuator is carried on a pivoting swing arm with center mounted head, and is electronically dampened for servolike positioning and stable settling. Built-in AGC and optional data separator prevent errors and allow use of more advanced data codes. An internal microprocessor simplifies diagnostics and control, and a buffered step mode increases track to track seek speed. Drive fits 3.25 x 5.75 x 8.00" (8.26 x 14.61 x 20.32-cm) mini-floppy form factor and can use std SA1000 floppy type interface. Only dc voltages are required. Electrical brake secures spindle in power-down mode, preventing media and head damage during moving or shipping. Rotating Memory Systems, Inc, 1031 A East Duane, Sunnyvale, CA 94086.



See at O'Hare Hilton Circle 362 on Inquiry Card

MICROCOMPUTER DEVELOPMENT SYSTEM

Scoutsystem D9524 development system for the Motorola family of processors meets SS-50 bus specifications and features 2-MHz 6809 CPU; dual 5.25" (13.34-cm) doublesided, octodensity floppy discs, providing 1.5M bytes of storage; and expandable 64k-byte RAM. System is available with 6800 CPU, 8" (20-cm) floppy discs, 10M- or 30M-byte 8" (20-cm) Winchester disc, and single- or multi-user capabilities. Development software includes Debug; macroassembler for 6800, 6801, 6802, 6803, 6805, 6808, and 6809; linkage editor; and EPROM programmer. Chieftain 9822 business oriented system also meets SS-50 bus specifications, and features 2-MHz 6809 CPU; dual 8" (20-cm) double-sided, double-density floppy discs, providing 2M bytes of disc storage; expandable 64k-byte RAM; business application software; and single- or multi-user capabilities. Also offered are Chieftain 98W10 and/or 98W30, and OS-9 multi-user operating system. Smoke Signal Broadcasting, 31336 Via Colinas, Westlake Village, CA 91362

See at Booth 584

Circle 363 on Inquiry Card

OUR NEW 5¹/4" WINCHESTER HAS A FIELD-PROVEN ANCESTOR.

We put more than 7000 8-inch Winchesters in the field before we built our first 5¹/₄-inch drive. That gives us the edge in Winchester manufacturing experience. So you get the quality edge in smaller Winchesters.

We've also built a reputation for delivery in volume. On time. You'll find the same Winchester know-how in our new 5¹/₄-inch drives. The same quality. The same

reliability. And even greater ruggedness.

We didn't just shrink 8-inches into a $5\frac{1}{4}$. We looked at the severe demands that systems place on these smaller drives. Then we began to build and test them.

While our competitors were spending most of their money announcing smaller Winchesters, IMI was actively designing, building and field-testing. We did it

with the 8-inch. Now we're doing the same with the 5¹/₄-inch version. We're also expanding production to meet your volume requirements.

Everybody claims to be the real leader in Winchesters. But no one has a Winchester family heritage like we do. You've already heard a lot of promises from others. But if you'd like the facts, contact IMI today.







DIGITAL CASSETTE TAPE TRANSPORTS

MT-2-23 and -24 incorporate a 2-track read after write head that records in 1600-bit/in (629/cm) double-density format to provide up to 760k bytes of formatted data storage. Both have a data transfer rate of 24k bits/s and high

speed search and rewind operations of 45 in/s and 75 in/s (114 and 191 cm/s), respectively. The 2-track head eliminates turning the cassette over. It accomplishes this by reading the track for side A or for side B on command. The units perform read or write opera-



tion at 15 in/s (38/cm). Separate read and write head gaps allow continuous read back and checking of data while writing. A high performance slit disc servo system provides smooth, stable, accurate tape speed for system reliability and quiet operation. Total size of either unit is $120 \times 105 \times 91$ mm. Weight is under 1.2 kg. Unit requires 12- and 5-Vdc supply voltages and is mountable in any position. **TEAC Corp of America**, 7733 Telegraph Rd, Montebello, CA 90640.

See at Booth 1084

Circle 364 on Inquiry Card

1M-BYTE ADD-IN SEMICONDUCTOR MEMORY

Using 16k rather than 64k RAMs to take advantage of the lower price/bit, DR-144S achieves 1M-byte capacity by use of vertical AMP pins interconnecting a max of 3 PC board assemblies. Only the motherboard of the 3-board memory

interfaces to the PDP-11/44 Unibus so that it presents only 1-unit load. Power consumption is minimized with the approach, since additional array boards on the motherboard are low



power MOS RAMS and not high power bipolar logic. A 256k version is available on a single hex-size motherboard; a 512k version is offered on a single assembly containing motherboard and 1 array board; motherboard with 2 array cards provides a full 1M byte. Designed to operate in DEC PDP-11 computers containing the Unibus, modified Unibus, or extended Unibus with a 12-V backplane, the memory may be operated with MS11-M, -FP, -JP, and -L, or in place of -M memories. The assembly contains the Unibus interfaces. control and status register, timing and control logic, refresh circuitry, and MOS storage array. The module also contains circuitry to correct single-bit errors and detect double-bit errors. Read time is 500 ns; write time is 1000 ns max. Read access time is 490 ns typ and 525 ns max without error. Max read access time with error is 600 ns; write access time is 200 ns max. Refresh cycle time is 500 ns typ. Dataram Corp, Princeton Rd, Cranbury, NJ 08512.

See at Booth 722

Circle 366 on Inquiry Card

WINCHESTER DISC CONTROLLER FOR MULTIBUS^R



Interfacing up to 4 Shugart Technology ST-506 small Winchester disc drives to a Multibus based computer system, the MSC-9025 is a single-board controller based on the MSC-9056 disc oriented I/O processor. Features include single Multibus compatible PC board, software transparent to iSBC 206 controller, and automatic error correction. The controller provides full sector data buffer, automatic error retry, and DMA data transfer. It is compatible with 8- or 15-bit systems, supports 20-bit addressing, and handles 128-, 256-, or 512-byte sectors. The controller automatically converts the iSBC 206 disc address to an ST-506 disc address. One platter (2 surfaces) of the 5440 series disc is emulated on each ST-506 drive equaling 5M bytes of data storage. The controller can support up to 20M bytes of storage by controlling up to 4 disc drives. MicroComputer Systems Corp, 432 Lakeside Dr, Sunnyvale, CA 94086.

See at Booth 3405

Circle 365 on Inquiry Card

LIGHTED PUSHBUTTON SWITCHES



Momentary action series 38 lighted pushbutton switches feature low profile modular design and variety of stripmount arrangements. Rated at 5 Vdc, 1 mA, the switches will withstand 15-Vdc, 50-mA surges. Switches have gold inlay contacts in Form A SPST-NO-SB, and have PC terminations only. They are offered in 4-, 8-, 10-, or 12-station modules, with a single-station version also available. Series 39 keycap switches will also be shown. These have bifurcated silverplated switch contacts to meet requirements of logic load switching. Contacts are self-cleaning, and configuration is in Form X SPST-NO-DB. Units are rated at 30 Vdc, 0.25 A max. Licon, Div Illinois Tool Works Inc, 6615 W Irving Park Rd, Chicago, IL 60634.

See at Booth 1319

Circle 367 on Inquiry Card

MORE OF THEM. MORE TO THEM.

The 1981 line-up of Memorex® OEM peripherals is bigger—and smaller—than ever before. Our 14-inch rigid disc drives, for instance, include mid-range units such as our under-100-mb Models 601 and 612, the 200-and 300-mb 677, as well as our latest, the Model 659, with 680 megabytes of capacity. Our eight-inch family features the Models 550 and 651 floppy disc drives, the 11.7-mb Model 101 and 23.4-mb Model 102 Winchester-type rigid disc drives and the new 25-mb Model 201, with 12.5 megabytes of fixed storage and 12.5 on a removable cartridge.

Together, these products represent a continuum of capacity and compatibility matched only by the continuum of quality that has always distinguished Memorex offerings. A continuum that reaches back through six generations of disc drive manufacturing experience and seven in disc packs and cartridges. And a continuum secured by Memorex's edge in technology, the investment in research and development and the fact that we create and control the key elements of our drives—the media, heads, PCBs. The bottom line is more products—and, of course, better products. Products that mean more to our customers because—be it in engineering, manufacturing, test, service and support—they are products that mean more to us. Products that mean that, more than ever before, Memorex is in the OEM business. Call your Memorex representative for *more*.

MEMOREX

There's MORE in Memorex OEM products.

San Francisco Area (408) 987-1373; Los Angeles Area (714) 891-2541; Boston Area (617) 890-0700; Dallas Area (214) 258-3510; Denver Area (303) 837-0205; New Jersey Area (201) 325-0164; Memorex International Headquarters: London, U.K. 01-572 7391.

See us at NCC in Booth #956





COLOR GRAPHIC DISPLAY MONITOR



HM-1719 features a 19" (48-cm) convergence free screen actuated by a proprietary inline gun, and provides a dot shadow mask of 0.47 pitch for increased clarity. Designed for optimum performance at 512 x 512 pixels with a capability of 720 x 540 pixel resolution, the unit incorporates single-PCB reliability, self-convergent inline gun, built-in high voltage regulator, video bandwidth of 25 MHz, and long persistence phosphor. In ddition to a 720- x 540-pixel resolution, no point on raster deviates from its proper position by more than 2% of raster light. The raster light regulation is less than a 1% to 0% change at peak 6 ft-L (long persistence phosphor), 15 ft-L (normal phosphor) luminance. Convergence does not deviate more than 0.028" (0.7 mm) from picture height in a centrally located area bounded by a circle whose diameter is equal to the picture height. Elsewhere, the deviation does not exceed 0.060" (1.5 mm). The unit complies with all safety rules established by the U.S. Department of Health. Controls include a contrast knob, brightness knob, degauss switch, and on/off toggle. All signal waveforms conform to the EIA RS-170 std waveform. Hitachi America, Ltd, 100 California St, San Francisco, CA 94111.

See at Booth 5412

Circle 368 on Inquiry Card

80M-BYTE 14" WINCHESTER DRIVE

Model 5830, a high density 80M-byte drive, is fully compatible with Control Data's SMD drives and interface controllers. The unit's 3 discs provide 5 data surfaces of 823 tracks each. Recording density is 6330 bits/in (2492/cm) on 429 tracks/in (169/cm). Data transfer rate is 1.29M bytes/s, max single track positioning time is 10 ms, avg access time is 35 ms, and latency time is 8.33 ms. Unit measures 7 x 19 x 22" (18 x 48 x 56 cm) and weighs 75 lb (34 kg). Power required is 3.1 A at 120 V, 60 Hz. Heads are positioned with voice-coil type actuator driven by a closed loop, proportional servo system synchronized to prerecorded tracks on lower surface of one disc. Drive operates standalone from CDC compatible controllers or can be daisy chained with SMD or mini-module drives. No operating system changes are required. Kennedy Co, 1600 Shamrock Ave, Monrovia, CA 91016.

See at Booth 1007

Circle 369 on Inquiry Card

LSI-11 PACKAGED SYSTEM

XL-2300 integrates a DEC LSI-11/23 processor with 96k to 256k bytes of memory, a 24M-byte 8" (20-cm) Winchester disc, a 17M-byte DC-450 tape cartridge as well as peripheral processors, backplane, power supply, and up to 8 communication ports into a compact tabletop or rackmount cabinet. The system runs all DEC compatible software without modification and supports third party software not previously available on an LSI-11. The company will also introduce its single-board dual-density tape controller for PDP-11 Unibus computers. The model 675 provides full TM-11 emulation and supports up to 4 industry standard drives running any combination of speeds. **Xylogics, Inc,** 42 Third Ave, Burlington, MA 01803.

See at Booth 5100

Circle 370 on Inquiry Card

50-Hz MINI-UPS

Mini-UPS operates on 50-Hz power for use in international markets and is available in 300- and 600-VA ratings. Selfcontained unit includes sealed, maintenance-free, lead-acid type battery and provides up to 24 min of regulated power at full load; when line power is restored, battery is automatically recharged to 95% of full potential in less than 10 times the discharge time. It operates from a singlephase 220- or 240-Vac input, and regulates output voltage to $\pm 3\%$ of nominal through input fluctuations as great as 10% to -15%. Input frequency fluctuations up to 10% of nominal are regulated at the output to ± 0.6 Hz. Unit provides emi filtering, attenuates electrical noise, and holds output harmonics to less than 3% single and 5% total harmonic distortion into a resistive load. Fuseprotected input circuitry protects device against short circuit or extreme overload; backup batteries are protected by inverter automatic shutoff. Also offered are a 60-Hz mini-UPS for domestic use, and the Micro/Minicomputer Regulator and Ultra Isolated Regulator line conditioning voltage regulators. Sola Electric, Unit of General Signal, 1717 Busse Rd, Elk Grove Village, IL 60007.



See at Booth 1629 Circle 371 on Inquiry Card

AMPEX EMULATING DISKS FOR DEC & DG.



Ampex offers two new disk subsystems that combine high technology emulating disk controllers with our full line of disk drives. You get complete cap-

ability for less money, and subsystems that are available and supported by one source: AMPEX.

Constellation-10 and -11, our new controllers, are matched with 80 and 300 megabyte removable media SMD disk drives as well as the DFR "Superwinchester" (32 to 96 megabyte) fixed/removable drive. The Constellation-10 emulates the DG 6061 and 6067 subsystems, offering total software transparency and 3 sector buffering.

The Constellation-11 emulates DEC RMO 2/3, RMO 4/5, RKO 6/7, offering media compatibility, software transparency, and 4 sector buffering.



MAKES THE DIFFERENCE

The new host resident, single board controllers use state-ofthe-art dual microprocessor architecture. Designed for our disk drives, these new

emulating subsystems will simplify your integration task and give you an extra edge in price/ performance.

For all the facts, contact Gary Owen at (213) 640-0150, or write to him at Ampex Corporation, Memory Products Division, 200 N. Nash Street, El Segundo, CA 90245.



DOT ADDRESSABLE COLOR GRAPHICS PRINTER



GP8001 is an intelligent ink jet printer with a Centronics compatible data port that interfaces with a variety of hosts and terminals. The 11.38" (28.9-cm) wide display has resolution of either 512 or 1024 pixels/line on continuous form paper. In either mode it prints 90 dots/in (35/cm) horizontally and 96 dots/in (37/cm) vertically. The unit uses 14.875" (37.8-cm) wide standard continuous form paper, and a disposable ink cartridge system for ink replenishment. Cartridge life depends on density of ink in display, but lasts 500 copies on the average. Cost per copy is approximately 10¢. Printing speed from command to finish is less than 3 min per 8" high display. The unit can print either bidirectionally or unidirectionally; an optional ASCII line printer mode is available. The printer uses droplet on demand technology. The print head simultaneously deposits 3 colors-cyan, magenta, and yellow-creating various colors by overlay or adjacent dotting. There are 12 jets in the print head (4 jets/color), and a wiper mechanism that prevents clogging automatically. PrintaColor Corp, 5965 Peachtree Corners E, Norcross, GA 30091.

See at Booth 771

Circle 372 on Inquiry Card

SOFTWARE DEVELOPMENT STATIONS

Software development stations MSC 8801 and 8802 are complete packaged systems running under CP/M that include a Multibus^R compatible Z80A based computer, 64k or 80k bytes of RAM, double-density 8" floppy disc drives, a 7-card slot Multibus chassis, and heavy duty system power supplies. The 8802 has a multiprocessor architecture that reduces software development I/O overhead as much as 80%. This system utilizes the 8009 and 8007A computer with 80k bytes of RAM to accomplish this throughput performance. Features include a key activated power on/off switch controlling all system power as well as 3 external ac outlets; provision for up to 8 serial communications channels; two 50-pin cable connectors for parallel I/O interfaces; 3 BNC connectors for video graphics applications, and 6

DOT MATRIX PRINTERS

The 800 series includes std split platen printers, flat bed slip document printers, and 51- to 96-col journal printers. All use the same drive system, head position sensors, ribbon transport mechanism, and components for max reliability and cost effectiveness. The unit's low profile printhead features a 7-needle vertical array with minimum friction, straight needle paths, low power consumption, and optimum heat dissipation. These design elements provide for a 100% duty cycle and average life of 100M characters. The needle array permits a variety of characters and fonts (5 x 7, 7 x 7, 9 x 7, double width) under user software control. Drive motor is rated at 8M print lines and printer body at 15M print lines (20M line feeds). Print speed is 150 char/s at 12 char/in (4.7/cm). The split platen model 820 does selective receipt printing at up to 5 lines/s; the flat bed 840 has side or front form insertion, top and bottom form sensors, and prints up to 40 cols on single- or multipart forms. Model 850 is a 51-col journal printer with top paper insertion, paper tear off blade, integral paper supply holder, and optional paper rewind. An 80-col journal printer that outputs up to 96 characters (576 print dots)/line, at 12 char/in, model 880 accommodates 3-ply paper, top loaded up to 9.6" (24.4-cm) wide. Westrex OEM Products, 1140 Bloomfield Ave, West Caldwell, NJ 07006.



See at Booth 110 Circle 373 on Inquiry Card

spare card slots in the computer chassis. Both units also include a 12" CRT terminal with a full ASCII keyboard, and an 80-char/s printer. Software support includes the industry standard CP/M 2.2 Operating System with a universal BIOS program that allows the user to develop and run software on any combination of standard or mini floppy disc drives, single- or double-density, single- or double-sided, single- or double-track. Disc format and copy routines are provided. Software can be developed in assembly language with the Editor and Assembler provided. BASIC or Pascal for high level language software are options. **Monolithic Systems Corp.** 84 Inverness Circle E, Englewood, CO 80112.

See at Booth 123

Circle 374 on Inquiry Card

Cortron announces a solid state keyboard at "bare bones" prices.

STANDARD BERNARD

Solid state intelligent keyboard for only \$45

If you are considering a low cost type keyboard, have we got an offer for you. The Cortron[®] CP-4550 Keyboard is a high quality, solid state, intelligent keyboard with full microprocessor capabilities.

Compare all the features of the Cortron Capacitance Keyboard—serial output, N-Key rollover, automatic repeat, custom codes—with "bare bones" type offerings. You be the judge of just how much more the \$45 starting price can buy volume keyboard users at Cortron.

Long-life, highly reliable keyswitch

We've designed a keyswitch with an exceptional, true linear feel. It's also environmentally superior to foam

pad design approaches. The keyswitch uses the full line of impressive Cortron keytops. All of this with a life test rating in excess of 100 million cycles.

TAB

FUNCTION

SHIFT



CORTRON DIVISION OF ILLINOIS TOOL WORKS INC THE KEYBOARD PROFESSIONALS AROUND THE WORLD

Ferrite Core and Capacitance...the best of both worlds

Cortron pioneered and built a reputation on the advanced ferrite core switching technology. Today, there are millions of ferrite core keyswitches in Cortron Keyboards around the world. We've applied this known expertise to further reduce keyboard costs. Cortron broadens the line with the introduction of the new capacitance keyboard. Now, you can choose the technology to fit your application needs from the best of both worlds. At Cortron, our people work hard at being responsive to your needs for advanced technology, cost efficiency, broad line and lower prices.

For full details and *free literature* on the Cortron CP-4550—\$45 Solid State Keyboard, call or write Cortron, A Division of Illinois Tool Works Inc., 400 West Grand Avenue, Elmhurst, IL 60126. Phone: (312) 279-9110. TWX: 910-254-0154.



UL LISTED 415-Hz UPS

Model 475 is rated at 75k VA and achieves efficiencies of 89% at full load, 86.7% at 50% load, and 84.5% at 33% load, the last being more than 10% better than that of competitive rotary or other solid state equipment. The solid state 50- to 415-Hz converter/ uninterruptible power system incorporates patented packaging techniques that yield low



repair rates—less than 30 min MTTR. Also exhibited will be the portable programmable model 3600 power line disturbance monitor. **Franklin Electric, Programmed Power Div,** 955 Benicia Ave, Sunnyvale, CA 94086.

See at Booth 1348

Circle 375 on Inquiry Card

PUNCHED TAPE READER/SPOOLER



A punched tape reader/spooler with RS-232 and 20-mA current loop I/O, RRS7156 provides 200-chars/s asynchronous or synchronous read speed and a 400-char/s tape positioning mode for rewinding or program cuing. Data rates are selectable from 110 to 9600 baud. The reader/spooler is available in 2 configurations: model G is 5.25" (13.34-cm) high and uses 6" (15-cm) reels containing up to 450' (137 m) of paper or mylar tape, and model D is 8.75" (22.23-cm) high and employs 7.5" (19.1-cm) reels with 700' (213 m) of tape. Both models mount in a std 19" (48-cm) rack and have an optional portable harsh environment enclosure available. MTBF is 16,000 to 20,000 h. **Remex Div of Ex-Cell-O Corp**, PO Box C19533, Irvine, CA 92713.

See at Booth 2604

Circle 377 on Inquiry Card

TELEPRINTER TRACTOR FEED

Providing choice of form or paper width as well as multiplepart forms to meet individual requirements, tractor feed T-43 mounts on any standard type 43 Teleprinter, and allows full benefits from electronic enhancements that are available to update the teleprinter. The unit is easily installed, and all of its moving parts are made of selflubricating materials to ensure reliability and long life. Mounting is accomplished with adhesive mounting pads. Instructions for optional hard mounting with pop rivets or thru-bolts are included with each unit. Optional paper-out sensor is available for friction feed models. PHD of Puerto Rico, Inc, PO Box 1084, Fajardo, Puerto Rico 00648.



See at Booth 226 Circle 376 on Inquiry Card

UNIBUS COMPATIBLE SERIAL LINE INTERFACE

Combining the functions of 5 modules on 1 board, the MDL-11 asynchronous serial line adapter for PDP-11 computers offers RS-422, buffer ready circuit, and other capabilities. The interface permits direct full- or half-duplex

communication between PDP-11 computers and terminals or modems via RS-232-C, 20-mA current loop, or RS-422 circuitry. Sixteen switch-selectable baud rates from 50 to 19.2k are standard.



Operating features of the DEC DL11-A, -B, -C, -D, and -E modules (ie, RS-232-C, current loop, selectable baud rates, limited and full modem control) are provided on the board. Selection of mode is made with PC mounted switches. Standard DEC command register, status register, and data buffer mechanization are used. The board is pin for pin compatible with DL-11 cable assemblies and existing cabling. The interface also offers a buffer ready/printer busy monitor circuit that allows connection to various RS-232 serial interface printers running at full speed. Modem interface circuits adapt the module to various dataset types; full dataset control is standard. MDB Systems, Inc, 1995 N Batavia St, Orange, CA 92665.

See at Booth 1090

Circle 378 on Inquiry Card

THE FIRST COMPLETE SENSOR-BASED MEASUREMENT AND CONTROL SYSTEM

THERMOCOUPLES RTD'S STRAIN GAGES_

mV AND V SIGNALS

4-20mA LOOPS



At last, there's a single board solution for both local and remote industrial measurement and control. It's μ MAC-4000 – the low-cost per channel, easyto-implement system that can be used anywhere a cluster of sensors and analog signals must be conditioned and digitized.

 μ MAC-4000 is a fully integrated, precalibrated, intelligent system, complete with sensor signal conditioning, multiplexing, A/D conversion, digital I/O and serial communications to any host computer. Its on-board microcomputer unburdens the host CPU by performing sensor linearization, scaling and conversion to engineering units, and limit checking. μ MAC-4000 was designed to accurately process low level transducer signals in the harshest environments. Its accuracy is assured by high quality signal conditioning, featuring input protection, \pm 1000V channel to channel and input to output isolation, high noise rejection, RFI/EMI immunity and low drift amplification. And with μ MAC-4000, you can readily mix and match sig-

nal conditioning modules as you require. For the full story, write Analog Devices, Box 280, Norwood, MA 02062, or call (617) 329-4700.

ANALOG DEVICES

WAYOUT IN FRONT.

Analog Devices, Inc., Box 280, Norwood, MA 02062; East Coast: (617) 329-4700; Midwest: (312) 894-3300; West Coast: (714) 842-1717; Texas: (713) 664-6704; Belgium: 031/37 48 03; Denmark: (02) 84 58 00; England: 01/941 0466; France: 01/687 3411; Germany: 089/55 03 19; Japan: 03/265 6826; Netherlands: 01620-51080; Switzerland: 022/31 57 60; Sweden: 08/282 740; and representatives around the world.



NGC PRODUCT PREVIEW

40M-BYTE WINCHESTER FIXED DISC DRIVE



Q2040, a 40M-byte version of the Q2000 series of 8" (20-cm) Winchester disc drives, offers 42.66M bytes of unformatted capacity per drive. Surface capacity is 5.33M bytes, 512 cylinders, and track capacity is 10.4k bytes. Features include full Shugart SA1000 series interface, mounting and power supply capability, proprietary moving coil rotary head actuator, temperature compensation servo track positioning system, and microprocessor control of drive function. The drive incorporates 4096 tracks, with 8 read/write heads, 4 discs, and 1 index. Rotational speed is 1000 r/min, and flux density is 6000 bits/in (2362/cm). Transfer rate is 4.34M bytes, and average access time is 65 ms with a 15-ms track to track access time and 100-ms max access time. Typical heat dissipation is 70 W. 10M-, 20M-, and 30M-byte series models are also offered. Quantum Corp, 2150 Bering Dr, San Jose, CA 95131.

See at Marriott Hotel

Circle 379 on Inquiry Card

COMPACT CRT TERMINAL

Model 401 measures 13 x 16 x 14" (33 x 41 x 36 cm) and weighs 14 lb (6.3 kg). It provides a 9" (32-cm) screen, full 128-char upper- and lowercase ASCII char set with descenders, 80-char x 24-line display format, and 7 x 9 char format. Features include dual intensity, reverse video with blinking and underlining, solid block addressable/ reader cursor with optional blink, and full cursor control keys, format protection, security blank fields, automatic char repeat, windowing, scrolling, 2-page memory, and 8 2-level function keys. Terminal communicates with the host asynchronously through std RS-232 interface, and operates in full- or half-duplex mode. Buffered printer port, daisychain interface, and line drawing set are optional. Informer, Inc, PO Box 91054, Los Angeles, CA 90009.



See at Booth 411 Circle 380 on Inquiry Card

DOUBLE-SIDED, DOUBLE/SINGLE-DENSITY FLOPPY DRIVES



Fully interchangeable with the Shugart SA85OR and with the full range of options and the same mounting dimensions,

M2894 and -2893 are fully IBM media and information compatible with no write precompensation required. The unit provides highly stable, error free double-density operation using all-ferrite MnZn heads in a gimbal mounted assembly with circular support spring. Virtually free from media wear problems, the drives show minimum media damage by tap test and minimum abrasion load wear. Wide readout window timing margins make the drives largely independent of disc performance characteristics; all popular brands of 2s2D discs perform reliably. The drives provide excellent media interchangeability using wide off-track readout margin that is maintained over the full range of temperatures and humidities specified. **Mitsubishi Electronics America, Inc,** 2200 W Artesia Blvd, Compton, CA 90220.

See at Booth 1464

Circle 381 on Inquiry Card

Grayhill totally sealed switches better than ever better than others

Total sealing

Each Grayhill SPST Rocker DIP Switch is now potted as part of the assembly process, to provide a more professional and economical bottom seal, with maximum seal integrity. Flux entry during wave soldering is totally prevented; contamination is eliminated; reliability is enhanced; and prices are unchanged... there is no cost premium for this important new feature. Grayhill also offers 3 topside sealing options, for raised or recessed rockers-a tape seal, applied at Grayhill; cards of tape seals, for your application; or re-usable protective covers. Whichever you choose, you get complete freedom during PC Board cleaning.

Exceptional reliability

All Grayhill DIP Switches incorporate our exclusive spring-loaded, sliding ball contact system. This highly reliable contact system provides positive wiping action, immunity to normal shock and vibration, and exceptional 50,000 cycle life.

Wide ranging choice

Grayhill Sealed Base Rocker DIP Switches are available SPST, from 2 to 10 rockers, with raised or recessed rockers. Grayhill also provides the Piano DIP[™] SPST side-actuated DIP Switch, sealed; the Toggle-DIP (SPDT or DPDT) for front panels, plus SPDT or DPDT back panel programming DIP Switches.

Off-the-shelf distributor availability

Procurement made simple-call Grayhill or your local distributor, for off-the-shelf delivery of most types. Only Grayhill offers you this purchasing convenience!

Make sure you have your copy of the most recent DIP Switch Catalog . . . free on request.

rauhill .the Difference Between Excellent and Adequate.





GRAPHICS DISPLAY TERMINAL



The DASHER[™] G300 offers intelligent graphics, extended alphanumeric capabilities, and compatibility with existing DASHER terminals, extending capabilities to presentation graphics in both business and technical areas, realtime process control, publication layout, and automated drafting. The unit consists of a detached keyboard and tilt and swivel display housing containing a 12" (30-cm) green phosphor screen. Terminal can display 1920 chars in 24 lines and 80 col. Graphics images are plotted on a 640- x 240-pixel matrix. Within the unit are ASCII, UK, French, German, Spanish, Swedish, and Danish char sets. The keyboard includes a typewriter style main keypad, 14-key numeric keypad, 15 program function keys, and 5 local function selection keys. A parallel printer port provides connection with a slave printing device. An asynchronous interface communicates with a host computer at speeds up to 9600 bits/s. Both RS-232 and 20-mA current loop interfaces are provided. Operation is supported on microNOVA, NOVA, and ECLIPSE computers running under RDOS, DOS, MP/OS, AOS, and AOS/VS operating systems. The graphics command interpreter within the terminal provides graphics intelligence, executing English-like high level graphics commands for relative and absolute positioning, plotting lines in polar and Cartesian coordinates, plotting arcs and straight lines, defining line style patterns, drawing solid rectangles and circles, filling closed shapes, defining graphic macros, and drawing text in a variety of formats. Data General Corp, Rte 9, Westboro, MA 01581.

See at Booth 826

Circle 382 on Inquiry Card

MATRIX PRINTER

Printer is member of 500 series Paper Tiger line and employs 18-wire high resolution staggered printhead that produces letter quality text at up to 150 char/s. High speed draft mode prints matrix characters at speeds in excess of 250 char/s. High resolution raster graphics feature is std. Integral Data Systems, Inc, Rte 13 S, Milford, NH 03055.

See at Booth 1732

Circle 383 on Inquiry Card

SMALL BUSINESS SYSTEMS

Single-user systems for small business applications, models 3450 and 3470 use 5.25 and 8" (13.34- and 20-cm) floppy diskettes with a hard disc option available. The multi-user model 4800 handles up to 8 users. All users can share a data base or do their own applications. A powerful and easy to use database management package is available for both single- and multi-user systems. Models 3431 and 3432 150-char/s heavy duty dot matrix printers will also be demonstrated. These printers are available with serial and parallel interfaces for use with various systems. TEI, Inc, 5075 S Loop E, Houston, TX 77033.

See at Booth 1561

Circle 384 on Inquiry Card

ACOUSTIC PRINTER CABINET

Quietizer cabinet 1720 for Teletype 40 OEM printers gives maximum noise reduction. A complete case for 80- and 132-col tractors, friction feed, forms access, and ROP units feeds and restacks a full box of paper with trouble-free front load and unload. Floor model steel outer shell is designed to put the machine at operational height. The unit, when installed in the



cabinet, is a pedestal stand, paper handling mechanism and acoustical enclosure. Cabinet is equipped with mounting rails, online/offline switch, and filtered ac wiring. **Van San Corp**, 16735 E Johnson Dr, City of Industry, CA 91745.

See at Booth 1329

Circle 385 on Inquiry Card

SOFTWARE METHODOLOGY SERVICE

Meta System 1000 is intended to present developments in the field of software engineering. The service includes original articles about software development as well as reprints of classic essays. Subscribers receive reviews of articles and books relating to software life cycle as well as critiques of available system development methodologies. Tutorials give how-to explanations and information about automated software tools. Documentation standards are suggested and explained through case studies. Project development guidelines address major technical and management issues. Structured analysis, structured design, structured programming, and walkthroughs are incorporated. **Structured Methods, Inc,** 7 W 18th St, New York, NY 10011.

See at Booth 1717

Circle 386 on Inquiry Card

The smallest 1/2 megabyte microcomputer has the biggest feature of all.

50 megabucks worth of software.

Sure, it's handy to get our HP 1000 L-Series microcomputer on just two boards—with a single board holding the full 1/2 megabyte of memory! But, before you consider buying any microcomputer, you should look beyond the hardware to the software.

After all, that's where most of the time and money is often spent in developing a microcomputerbased system. But you can eliminate almost all that effort by using an L-Series. With \$50 million worth of software development behind it, you only have to worry about developing your applications programs.

The L-Series offers you the ideal combination of HP's big system software and economical microcomputer hardware. So you can build cost-effective solutions for data acquisition and control, communications, factory automation and a whole range of other products.

Designer software.

With the minicomputer software that HP has been perfecting for more than a decade, plus our Model 10 Development System, you'll find it's easy to create the system you need.

You can start with either RTE-L or RTE-XL, our powerful multi-programming, multi-user operating systems. Their modular construction lets you build the realtime computing environment your applications programs demand — programs you can develop in Assembler, FORTRAN 4X, BASIC and PASCAL. And our HP DSN networking software makes it simple to put lowcost computing wherever you need it.

Data base management on a board computer? With our IMAGE DBMS, you've got a powerful tool for simple and efficient data management. And you can easily picture the possibilities offered by our GRAPHICS/1000 software. Like our other software packages, these are all upwardly compatible throughout the entire HP 1000 line, giving you an easy growth path to even higher performance.

Efficiency across the board.

How to handle all this software power? Simple. We used an advanced distributed intelligence architecture that puts a separate LSI I/O processor on each interface board. This means each processor has its own direct channel to the entire 1/2 megabyte memory. (We used state-of-the-art 64K RAMS to put the 512K bytes of memory on just one board.) And with the CPU free to concentrate on computation, you get significantly increased throughput and exceptional microcomputer performance.

A range of solutions.

The L-Series comes in a variety of configurations to meet your needs best—from boards and boxes to entire systems. Prices start at only \$1968 for a starter set that includes CPU, 64KB memory and one I/O board.

Like our other OEM products, the L-Series is backed by our full range of customer services—including worldwide software and hardware support.

If you'd like a hands-on demonstration, just contact your local HP sales office listed in the White Pages. Or write for more information, and our new OEM catalog, to Hewlett-Packard, Attn: Joe Schoendorf, Dept. 1296, 11000 Wolfe Road, Cupertino, CA 95014.



U.S. OEM prices in quantities of 100.





SINGLE-BOARD COMPUTER WITH ANALOG AND POWER I/O



The 4.5 x 6.5" (11.4 x 16.5-cm) module features a 6801 or 68701 microprocessor with 2k-bytes ROM, 128-bytes RAM, internal timer, and external watchdog timer. The 12-bit ADC can be configured for 8 single-ended or 4 differential inputs. The 8-bit DAC can be configured to output either 4 to 20 mA or 1 to 5 V. The 8 digital 1/0 lines can be configured for any mix of ac or dc inputs or outputs. Inputs sense the activity of ac or dc circuits; ac and dc outputs are triacs and solid state relays capable of switching 3 A. Serial 1/0 allows a half-duplex 20-mA current loop communication channel to a host computer at software selectable baud rates. **Wintek Corp**, 1801 South St, Lafayette, IN 47904.

See at Booth 1280

Circle 387 on Inquiry Card

MULTI-ACCESS TERMINAL SYSTEM

Terminal Master I interfaces with Telex, TWX, and DDD networks through a single terminal source. It consists of Model 43 KSR Teletype and a microprocessor with up to 16k of buffer storage. The buffer has the capability of operating

from 50 to 9600 baud, keyboard programmable. The DDD line can operate at 110 or 300 baud, and at 1200 baud with the 212A option. The 212A-Plus, when directly connected to the telephone line, offers microprocessor controlled automatic dialing of telephone numbers stored by the operator in the modem's memory. Up to 5 numbers of 22 digits each can be stored. The unit can



also link stored phone numbers so that an alternate number can be dialed automatically if the first number is busy. A built-in HELP feature displays stored number of operating instructions. The unit is compatible with Bell 212A-Plus and 100 series modem, providing 300-baud and 1200-baud full-duplex transmission of data over the switched network. **Terminal Systems Inc**, 11300 Hartland St, North Hollywood, CA 91605.

See at Booth 1761

Circle 388 on Inquiry Card

GRAPHICS WORKSTATIONS

WHIZZARD 6200 graphics workstation family provides high resolution 1024 x 1024 raster displays for computer aided design and manufacturing. Model 6245, with a 20" (51-cm) black and white monitor, and model 6255, with a 19" (48-cm) color monitor offer performance features of the 6250 workstation. The 6245 has a flicker-free 20" monitor with 1024 x 1024 resolution that operates noninterlaced at a 60-Hz refresh rate. Packaged with a keyboard and joystick control in a desk style cabinet, the terminal includes a graphics processor, display list memory, an RS-232 serial asynchronous interface, and room for optional modules. The 6255 consists of a 19" color monitor also offering 1024 x 1024 resolution. It is packaged with a keyboard and joystick control in a desk style cabinet. The terminal may have a data tablet and either additional display list memory or a hardcopy output device. The terminals provide the graphics features of the larger 7250 raster system. Both models incorporate a high speed digital vector generator, updating and manipulating complex pictures at rates from 30 to 60 times/s. The units offer a 4096 x 4096 virtual vector space that supplies a high level of detail in realtime steps from 1024 x 1024 through 2048 x 2048 and 4096 x 4096, providing capability of displaying the entire 4096 x 4096 area on the screen or of zooming in on any smaller viewport. Double-buffered bit planes of the 6245 and 6255 permit erasure of overlapping or intersecting lines in a drawing without causing breaks in the lines that remain in other planes on the screen. WAND 6200 software provides a high level of intelligence. **Megatek Corp**, 3931 Sorrento Valley Blvd, San Diego, CA 92121.

See at Booth 1251

Circle 389 on Inquiry Card

- Motorola MC68000 16-bit processor
- Multi-tasking
- operating system
 Languages supported include C, PASCAL and BASIC
- Mass storage devices up to 10MB
- 19" CRT
- 1024 x 768 high resolution color graphics
- 256 simultaneously displayable colors



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CIRCLE 72 ON INQUIRY CARD



FLOPPY DISC SUBSYSTEM



Consisting of a 5.25" (13.34-cm) quad-density singlesided drive and controller electronics that connect directly to the Sorcerer computer, each disc drive is capable of 308k bytes of data in a soft sectored format. Controller electronics allow 2 additional drives to be added to the subsystem for future storage requirements. Data format of the subsystem is completely compatible and interchangeable with that of the company's small business computer System 80. Voltage requirements are 100/110 or 200/240 V and 50- and 60-Hz cycles are std and user configurable. CPM operating system software is included with the controller and disc drive. **Exidy Systems, Inc**, 1234 Elko Dr, Sunnyvale, CA 94086.

See at Booth 1641

Circle 390 on Inquiry Card

INTELLIGENT DIGITAL DATA RECORDERS

Plug-in InteractorsTM for asynchronous RS-232 applications are available with digital cassettes for economy in low or medium speed data handling or flexible diskettes for high speed random access jobs. Both offer large capacity storage and microprocessor control with self-initializing operation. The reusable media also serve for archival storage. Working with data loggers or an intelligent system, the units communicate through RS-232 ports with terminals, modems, computers, or other like units under local or remote control. Micro-Disc recorder Model 981 provides capacity for 200k bytes/diskette. It operates at transmission rates to 9600 baud and provides editing capability. Data cassette tape units store 145k bytes/side and operate at up to 2400 baud. **Techtran Industries, Inc**, 200 Commerce Dr, Rochester, NY 14623.



See at Booth 441 Circle 391 on Inquiry Card

SINGLE-BOARD MICROCOMPUTER SYSTEM

Model 80-21 features a Z80 CPU; 32k bytes of RAM; 2 double-density, single-sided, 140k-byte mini-floppy disc drives; ASCII keyboard with 13-key alphanumeric pad and special function keys; 110- to 9600-baud serial communications interface; parallel line printer interface; power supply; and cabinet. Its 1920-char CRT display is packaged in its own pedestal mounting. Optional are an additional 32k bytes of RAM and double-density, double-sided, minifloppy disc drives. Std software for the system includes monitor, editor, and utilities; BAL language supported by BAL operating system; file management system including sequential, indexed sequential, and random access; and assembly language. CP/M operating system, including context editor, assembler, and debugger; MBASIC (both interactive and compiler); CBASIC compiler; COBOL, Pascal, and APL; and a CBASIC business applications package are optional. PORTAL portable microcomputer system, and series 80-30 small business microcomputer system, with 32k to 64k bytes of RAM; double-sided, double-density, mini-floppy drives; 1920-char CRT with graphics capabilities; and optional Honeywell Bull D120 (10M-byte) and D140 (20M-byte) hard discs are also offered. R2E of America. 32200 Solon Rd, Solon, OH 44139.



See at Booth 681 Circle 392 on Inquiry Card

OVERHEAD PROJECTION FILM

A prototype 8 x 10" (20 x 25-cm) film which delivers a high quality, full-color instant transparency for overhead projection offers a means for group presentation of computer-generated color graphics and other business data. Using technology similar to that of 8 x 10 instant color print films, the transparency is exposed in an easy loading filmholder and processed in a tabletop processor. The transparency is ready to view in approximately 4 min. In addition, instant color print films will be demonstrated on computer peripheral 3-color camera systems that use high resolution, distortion-free black and white CRT screens to sequentially display and expose instant films to color-separated color graphics images through appropriate red, green, and blue filters. **Polaroid Corp**, Cambridge, MA 02139.

See at Booth 5124

Circle 393 on Inquiry Card

Do standard, low cost power supplies have to be tweeked and modified to work? Not with Sierracin power systems.

The power supplies we design are made to deliver a cost-performance ratio second to none. Our multioutput switchers are prime examples. Auxillary outputs are pre-regulated by the switching section, then post-regulated with linear regulators. As a result, each output remains tightly regulated regardless of individual load changes. This means excellent dynamic response characteristics. No cross regulation. And "goodbye" to unexplained system crashes. What about line transients? Our switchers have a

wide ac input range of 90-132/ 180-264 volts which offers greater immunity to line noise and brownouts. And those tight, little spaces? Our compact, low-profile line of 40 to 500 watt, open-frame dc switching power supplies will fit just about anywhere. Prices start at a low \$45 – with OVP on every product including linears at no extra cost.

In short, we build affordable power supplies which keep on working — the first time, every time — you put them in your system. It's what you can expect from Sierracin/Power Systems. A young, dynamic 6-year-old company that's already a recognized industry leader.

See for yourself. Write for our new 1981 Power Supply Catalog. Or dial our toll free number.



For technical information or application assistance, call:

800-423-5569 In California, call (213) 998-6811 collect.





RUGGED PORTABLE OSCILLOSCOPES



Models 2335, 2336, and 2337 are 100-MHz dual-trace scopes with delayed sweep, 5-ns/div maximum sweep speed, and 5-mV/div vertical sensitivity. An improved triggering circuit using IC technology offers stable and dependable triggering capability beyond the rated bandwidth. CRT design provides a sharp, crisp trace and nearly 2 to 1 improvement in spot size over currently available portable units. Using a new design, deep drawn aluminum can, and CRT shielding, the series exceeds its 10-V/m electromagnetic compatibility. Units are built to withstand a 50-G shock and conform to MIL-T-2800 specs. Weighing 17 lb (7.7 kg), the scopes have a hinged front cover that contains several controls minimizing front panel clutter, achieving smaller size, and increasing front panel protection. The 2335 comes without electronics in the front cover; the 2336 contains B-trigger, delta time, and numerical LCD display readout in the front cover; and the 2337 includes B-trigger and delta time plus a general purpose 31/2-digit DMM in the cover. Units meet service measurement needs of TTL and CMOS based equipment in computer, telecommunications, control, and harsh field service applications, as well as in those in which emi is a problem. Tektronix, Inc, PO Box 1700, Beaverton, OR 97075.

See at Booth 817

Circle 394 on Inquiry Card

COMBINATION TELEPHONE/MODEM

Phonem model 370E2-12 is an originate mode Bell 103/113 compatible 300-baud modem combined with a pushbutton telephone. Lifting or replacing the handset automatically controls voice/data modes. Pressing the ''#'' key automatically redials the last number, and disconnect is accomplished manually by pressing the ''*'' key, or automatically via last carrier. Data interface is RS-232 and line connection is by means of std RJ11 or RJ45 modular jacks. Model 370E2-42 phonem performs auto answer and disconnect functions in addition to those performed by the originate-only version. **ComData Corp.** 8115 N Monticello, Skokie, IL 60076.

See at Booth 519

Circle 395 on Inquiry Card

80-COL BIDIRECTIONAL TERMINAL

Model 5080 printing terminal is a heavy duty printer designed to conform to most computer specifications including software on/off control, status feedback signals, and busy signal when the buffer becomes full. The stand-

alone unit meets requirements for both OEM and end users. Four interfaces are std: 8-bit parallel, RS-232, TTY, or IEEE 488. Users can print upper- and lowercase ASCII characters, at 100 char/s with full graphics capa-



bility (480 dot cols/line). The unit also has bidirectional friction and sprocket paper advance, 360-char buffer, selectable baud rate, self-test mode, and UL/CSA approval. It is packaged in a desktop case measuring $13 \times 18.5 \times 8''$ (33 x 47 x 20 cm). Victor Data Products, 3900 N Rockwell St, Chicago, IL 60618.

See at Booth 516

Circle 396 on Inquiry Card

COMPUTER DISPLAY KSR TERMINALS



Microprocessor controlled 722 display terminals provide asynchronous character by character transmission consistent with established TTY conventions. They can also be set to advanced mode operation for extended control functions. The 12" (30-cm) diagonal CRT has a capacity of 24 lines by 80 char/line for a 1920-char display of 8 x 10 dot matrix characters measuring 0.219 x 0.1" (5.56 x 2.54 mm). The units permit storage and display of the 95-char ASCII set, and 33 control code characters are provided. In advanced mode an additional 31-char line drawing set can be displayed. 85-key keyboard includes numeric pad and 12 special function keys, and N-key rollover. Data are highlighted by dual-intensity and blink. An interface for optional impact or nonimpact printers is provided. Transmission speed range is 110 to 19,200 bits/s. Control Data Corp, 8100 34th Ave S, Minneapolis, MN 55440.

See at Booth 811

Circle 397 on Inquiry Card

VT100 GRAPHICS IN 4.4 MINUTES!

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Adding the Graphics 100 PC card to your existing VT100 or VT103 gives you the most versatile CRT terminal on the market today. No other component or CRT changes are required.



OR BUY OUR GRAPHICS TERMINAL

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15" CRT COMPUTER TERMINALS



A std 15" (38-cm) monitor on Executive 80 series smart computer terminals results from reduced cost differential between 12 and 15" models. The bigger screen results in easier readability, increased accuracy, and reduced fatigue because of the 25% larger viewing area. Other std features include video highlighting, line drawing, status line, programmable function keys, and a horizontal split screen display. Also available are detached keyboards and an enhanced video package which can selectively display characters at normal font size, twice the normal height and width, or in 132-col 5 x 7 formats. Tilt capability allows for individual operator preference and comfort. Different viewing angles, further distances, and virtually total elimination. of reflection result from the combined effects of the large screen size and tilt features. In addition to the 15" (38-cm) screen, the unit features an easy viewing, green display with nonglare monitor to minimize eye strain. Sculptured key caps with audible feedback result in more efficient and accurate keyboard entry. Std typewriter keyboard layout ensures fast and simple training. Hazeltine Corp, Greenlawn, NY 11740.

See at Booth 741

Circle 398 on Inquiry Card

OFFICE MANAGEMENT SYSTEM

Capable of running on any MICOS hardware configuration, the office management system consists of six software modules. Word processing is a user friendly package supporting most standard word processing features; electronic filing is capable of automatically indexing, filing, and retrieving correspondence or documents on the basis of titles or content; and electronic mail distribution routes and distributes messages or memos between terminals in the system or systems at remote sites. Electronic mailing list creates and selectively retrieves a name and address data base. Electronic calendar/scheduling allows a calendar of events or meetings to be established, revised, and accessed on an individual, group, or company basis. Electronic call reporting permits telephone queries and messages to be recorded, updated, and dispatched by category, individual, or department. Mini-Computer Systems, 399 Fairview Park Dr, Elmsford, NY 10523.

See at Booth 1543

Circle 399 on Inquiry Card

REALTIME BUS STATE ANALYZER

An intelligent diagnostic tool that is designed specifically for use with microprocessors, Real-Time VERSAbus state analyzer has the ability to evaluate software. This addition to the EXORmacs development system consists of three fault-analysis triggering modes. The analyzer consists of two EXORmacs resident modules, with the "master" module containing the analyzer hardware control software and I/O ports, and with the "personality" module interfacing to selected VERSAbus signals. Features include 79 channels by 128 states trace memory. The unit displays signals using their mnemonics. It provides single trace, trace and compare with previous trace, trace a selected state only, trace inside or outside an address window, and trace through reset. An up to 7-step qualifier sequence can be used for trigger, and a trigger qualifier sequence can be restored on a given address state. Other features include trigger pulse output, histogram display address for software performance analysis, and discrete signal histogram display. Qualified triggering modes are continuous trace, sequential trigger, and window trigger. To reduce system redundancy, the EXORterm 155 terminal used by the operator to communicate with the EXORmacs development system also serves as a link to the intelligence aboard the analyzer. Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036.

See at Booth 1236

Circle 400 on Inquiry Card

INTEGRATED CRT DISPLAY DESIGN



Featuring a CRT-mounted circuit board that eliminates the need for a chassis, DC-955 12" (30-cm) display improves the accessibility to most electrical components without the need to remove the board. The unit has options of 18.6 and 19.2-kHz horizontal scanning frequencies for 80- x 25-char screen format. Features include 800-line resolution, separate horizontal, vertical, and video drives, internal controls for vertical frequency, size, linearity, horizontal size, centering, and focus, and optional external brightness and/or contrast controls. The unit complies with DHEW regulations for X-radiation, and components are designed to meet applicable UL standards. Audiotronics Corp, 7428 Bellaire Ave, North Hollywood, CA 91605.

See at Booth 323

Circle 401 on Inquiry Card

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If your VAX* computer memory can't handle your processing workload, you don't have to wait six months for additional memory. Monolithic System's MSC 3610 VAX Expansion Memory will be delivered in 10 days, cost is less than \$6,000 per megabyte, and is guaranteed plug compatible with your VAX 11/780.

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FLOPPY DISC CONTROLLER



Model 1180 is an Intel Multibus^R (IEEE 796) controller which will operate up to 4 model 299B or 277 drives. It is a single-(FM) or double-density (MFM) controller which operates with IBM diskette 1 or 2D formats. It employs a command set, common to existing 1070 and 1170 controllers, that allows data storage and retrieval at levels ranging from sector write/read to file management capabilities of advanced disc operating systems. It also provides diskette initialization and diagnostic commands all of which require only minimum host program routines, and generates and uses CRC characters for error detection during diskette operations. Also featured will be the 299B dual-head, doubledensity dual-diskette drive, an IBM compatible unit that reads and writes on both sides of 2 diskettes in a drive no larger than a standard floppy. With capacity exceeding 2.75M bytes formatted, the drive features voice coil positioning that enables a full stroke seek in 100 ms. Its patented read amplifier design allows users to choose to operate with or without write precompensation, ensuring compatibility with other systems. PerSci, 12210 Nebraska Ave, West Los Angeles, CA 90025.

See at Booth 680

Circle 402 on Inquiry Card

WORD PROCESSOR TO PHOTOTYPESETTING CONVERTER

Trans Media 500 system is designed to convert directly to phototypesetting from almost any word processing medium. One system can convert from 5 and 18" (13- and 20-cm) floppy diskettes, mag tapes, paper tapes, and asynchronous communications. It will accept input from many different systems and eliminates reproofreading, rekeyboarding, and correcting. The std system includes a computer terminal, 3 floppy disc drives, and a mounting rack. The customer may also select 4 diskette formats, with other formats available on request. **Applied Data Communications**, 14272 Chambers Rd, Tustin, CA 92680.

See at Booth 565

Circle 403 on Inquiry Card

WINCHESTER OPTION FOR MICROCOMPUTER

To provide greatly increased storage and faster access, model 311 Winchester drive is offered as an option for the Microlite microcomputer system. The drive is mounted within the console of the system, which is a desktop, standalone, multifunction microcom-



puter. Providing high recording density, storage capacity 30 times that of mini-floppies, and faster data access and data transfer capabilities, the unit uses a std Winchester ferrite head, and records data on the discs at approx 7500 bits/in (2952/cm). The drive includes 2 motor assemblies (stepper and spindle), a head assembly with 4 Winchester heads, and a disc assembly consisting of 2 discs. Other options for the computer include a quad density floppy disc drive, a 24 x 80 plasma display with graphics capability, and a system board containing 64k of RAM running at 4 MHz. All options can be housed in the basic console. **Q1 Corp.** 125 Ricefield Lane, Hauppauge, NY 11787.

See at Booth 1431

Circle 404 on Inquiry Card

SINGLE-BOARD BASED COMPUTER FAMILIES



A line of single-board microcomputers includes 8-bit z80 based computers serving 1 to 4 users with 48k RAM/user, 208k RAM total, supporting CP/M, MP/M, and AMEX operating systems, and 16-bit 8086 based computers serving up to 16 users with 128k- expandable to 1M-byte RAM, Multibus compatible, and supporting CP/M. MP/M, AMEX, OASIS, and XENIX (UNIX). Expandable mass storage on all systems includes dual-floppy 1M-byte, expandable (1M- to 58M-byte) dual-floppy, and 8" (20-cm) and 14" (36-cm) hard disc systems. Mag tape backup is available on all hard disc systems. Altos Computer Systems, 2360 Bering Dr, San Jose, CA 95131.

See at Booth 3604

Circle 405 on Inquiry Card

LET'S PLUG SOME COMMON SENSE INTO THE KEYBOARD DESIGN CONFUSION

FACT: For the great majority of today's keyboard applications, all you really need is a good, highly reliable, low-cost mechanical switch. Certain uses do require the more expensive types, but they're in the minority.

If you're in doubt about your application, ask Stackpole. You'll get straight answers drawn from our experience. And you may find that our high-quality keyboards to do the job right don't have to cost anywhere near what you thought. **FACT:** Conservative design is good, but it doesn't make economic sense to specify a 100-million-cycle switch for a five-year product.

Stackpole's rugged keyboard arrays, with typical life of 20 million cycles per station, give you reliable, heavy usage of five to nine years, are field-repairable and cost a whole lot less than 20-year keyboards.

FACT: Excessive cost-cutting can also be a mistake. The lowest-cost



keyboards may lack smooth performance, physical strength, reliability, and may not be field-repairable. Warranty service and lost customers can cost you far more than the keyboard arrays.

Our KS-200 non-encoded keyboards may cost a bit more, but consider what you get:

- Versatile main, numeric and ancillary arrays, standard or custom
- Excellent performance and "feel"
- Strong, rigid monolithic housings assure keycap alignment, eliminate PCB stiffeners, simplify inventory
- Replaceable, twin bifurcated contacts provide long life
- Arrays are wave-solderable
- Many options: arrays with or without keycaps or with bulk keycaps, with or without PCB, plus many others.
- Highest quality, good delivery, highly competitive prices.

Call or write your local Stackpole representative or the Marketing Department, Stackpole Components Company, P.O. Box M, Farmville, Va 23901. Phone: (804) 392-4111 TWX: 710-874-3710







PAPER TAPE READER/PUNCH TERMINAL



The microprocessor controlled RPT 18 is a self-contained tabletop paper tape terminal designed for quiet, reliable, and flexible operation. It incorporates the company's patented reader/punch mechanism, which operates at speeds up to 30 chars/s (300 baud). It can be supplied with either ASCII to NC (RPT 18/02) or ASCII to Baudot (RPT 18/03) code conversion capabilities. Connected to a keyboard send/receive printer, it provides automatic send/receive capabilities, or can be used as a standalone terminal. Punch mechanism employs magnet-controlled interposers, actuated by an oscillating bail, to positively drive and retract the punch pins. The reader sends tape photoelectrically with matched LEDs and phototransistors. The unit punches mylar as well as paper tape, and senses low tape supply and taut tape to the reader. It punches and reads fanfold tape. Standard features include terminal response to remotely generated or locally read codes plus code search functions for tape editing. Optional features include modem or current loop interface, answerback, and 4k to 12k internal buffer store. Trend-DLC, 280 Midland Ave, Saddle Brook, NJ 07662.

See at Booth 1628

Circle 406 on Inquiry Card

RASTER GRAPHICS COLOR DISPLAYS

Series 7000 includes 13" (33-cm) and 19" (48-cm) color CRT units with bandwidths ranging from 25 to 40 MHz and horizontal sweep frequencies from 15 to 35 kHz. Resolution is in the 512 x 512 and 1024 x 1024 dot range. Devices use either inline gun striped mask, or high resolution inline gun dot matrix CRTS. Delta gun delta matrix tubes are also available. Series 2400 19" high performance monochrome display will also be shown. It uses innovative CRTS and deflection circuits for high resolution high definition images. **Conrac Corp**, 600 N Rimsdale Ave, Covina, CA 91722.

See at Booth 1456

Circle 407 on Inquiry Card

150-CHAR/s MATRIX PRINTER

Series 6001 printer provides 150-char/s print speed with a 9 x 9 matrix. It is available with a Centronics parallel or RS-232 serial interface operating at up to 19,200 baud; active or passive 20-mA current loop is std. Printer interface has a 2k-byte buffer, expandable to 4k bytes; the printer will accept 80 additional chars after transmission of a busy signal. Sufficient storage to copy 1920 chars without restraint pauses is provided. Page length is adjustable from 3 to 22" (8 to 56 cm) in 0.5" (1.3-cm) increments. Vertical tabs of 4 or 6 lines and horizontal tabs modulo 8 are implemented. Automatic skip fold is switch selectable at 0, 4, or 6 lines. **Qantex, Div of North Atlantic Industries, Inc,** 60 Plant Ave, Hauppauge, NY 11787.



See at Booth 531

Circle 408 on Inquiry Card

DEC EXPANSION CHASSIS

General purpose WP909 is a 5.25'' (13.34-cm) rackmount chassis that accommodates 1 or 2 DEC 4-slot backplanes or one 9-slot unit. Designed for users that have run out of backplane room or those who prefer controllers or interfaces in separate containers, the chassis comes std with 5 V at 15 A and \pm 15 V at 2 A. Optional 25-A supplies are available. A snap-off front cover gives access to all PC boards for removal, insertion, or testing without dismounting the chassis. All units come equipped with rack slides, cooling fans, and mounting hardware. Also displayed will be controllers for DEC PDP-11 and LSI-11, Data General NOVA, and NOVA emulating computers. **Wesperline, Div of Wespercorp**, 14321 Myford Rd, Tustin, CA 92680.





WF'VF GIV GREEN LIGHT **Sprague Electric offers you the finest** and broadest choice of interface ICs

for driving fluorescent displays. From the outset, Sprague has led the way in IC interface for fluorescent display panels. Its UDN-6118A was the pioneer. Today, Sprague product capability spans low voltage performance (required for automotive and aircraft dimming), to split supply operation (permitted by the latest Sprague VF drivers-UDN-6138 & UDN-6148), to the highest voltage operation obtainable (110V guarantee for UDN-6118A-1-also often used for gas discharge

Sprague VF drivers incorporate output pulldown resistors and are guaranteed for less than 1.0V output OFF voltage (frequently a filament biasing concern). The use of proper interdigit blanking ($\geq 20 \mu S$) eliminates ghosting problems. Sprague VF ICs also have a maximum turn-off delay of 5µS (under normal display loads).

displays).

Recognized as the industry standard, Sprague VF display ICs are compatible with TTL & MOS logic. Plastic DIPs are supplied for 0°C to +70°C operation while both extended temperature range and hermetic versions are also available for automotive and other challenging applications.

For additional information or application assistance, write or phone Paul Emerald, Sprague Electric Co., Semiconductor Division, 115 Northeast Cutoff, Worcester, Mass. 01606. Telephone 617/853-5000.

	DEVICE TYPES	CHANNELS/DIP	MIN BV (OUTPUT)	DIP
THUTTUT	UDN-6116A-2, 6126A-2 UDN-6116A, 6126A	6	+ 60 V + 80 V	16 lead 16 lead
	UDN-6118A-2, 6128A-2 UDN-6118A, 6128A UDN-6118A-1, 6128A-1 Anode driver, gas discharge displays	8 8 8	+ 60 V + 80 V +110 V	18 lead 18 lead 18 lead
THITTE	UDN-6138A-2, 6148A-2 Split supply (+20 V, -40 V) UDN-6138A, 6148A Split supply (+40 V, -40 V)	8	60 V* 80 V*	20 lead 20 lead

*Output BV referenced to V EE Max. VEE -40 V

FOR FAST INFORMATION, CALL YOUR NEAREST SPRAGUE SALES OFFICE:

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a subsidiary of GK Technologies

<u>NGG PRODUCT PREVIEW</u>

SPACE SAVER CRT



With a 12" (30-cm) CRT, the L-style display unit occupies 12 x 13" (30 x 33 cm) of desk space, and weighs 18.5 lb (8.4 kg). An optional wall mount bracket allows the unit to be tilted and swiveled to achieve optimum viewing angle. In this mount it requires no desk space except for detached keyboard. 10L is a smart, single-page editor with user programmable function memory; 100L is a 132-col VT100 compatible unit with advanced video, bidirectional peripheral port, and user programmable function memory. Both are completely modular for quick and easy servicing without tools. **Teleray, Div of Research, Inc,** PO Box 24064, Minneapolis, MN 55424.

See at Booth 1530

Circle 410 on Inquiry Card

TAPE MAINTENANCE SYSTEM

MLC-304 tape maintenance system cleans, retensions, and evaluates condition of a 2400' (731-m) reel of tape in 3.3 min. Microprocessor control and several refinements eliminate troublesome calibration requirements as well as possible tape damage from operator error. Significantly, the system evaluates live data tapes without erasing stored information. Also on display are magnetic media products that include a high quality ANSI compatible cassette for TRS-80, Apple, Commodore, Atari, and other personal computers; a 5.25" (13.34-cm) miniflexible disc compatible with TRS-80, Apple, Commodore, and other drives that provides twice the storage capacity of other units by permitting users to record on both sides; color-coded magnetic cards with improved wear characteristics for use on IBM compatible magnetic card equipment; and 5.25" (13.34-cm) miniflexible discs in single- or dual-sided, double-density formats that are critically certified error free at 96 tracks/in. Dennison KYBE Corp, 82 Calvary St, Waltham, MA 02154.

See at Booth 1304

Circle 411 on Inquiry Card

DOT MATRIX PRINTER

Capable of 150-char/s print speed at 10 char/in (4 char/cm), model 150 dot matrix printer features bidirectional printing, logic seeking, adjustable snapon tractors, and cassette ribbon. Condensed printing capability adapts the unit to such types of com-



puter output as forms, financial data, labels, and listings. It handles roll, cut sheet, and fanfold paper, prints in 40-, 80-, or 132-col format, and is capable of 100% duty cycle. Full 1-line buffer is standard. Character set is 96-char ASCII with international set as an option. Data input is 7-bit ASCII parallel, TTL levels, with strobe, acknowledge, and busy. Eighth bit selects second character set. Also shown is the company's full line of matrix, band, and nonimpact printers. **Centronics Data Computer Corp**, Hudson, NH 03051.

See at Booth 933

Circle 412 on Inquiry Card

INTELLIGENT DRUM PLOTTER

The 3620 intelligent digital drum plotter is a 4-pen 36" (91-cm) drum plotter with 35 in/s (89-cm/s) axial speed, 4G acceleration, 0.00049" (0.0124-mm) resolution, and continuous feed paper for unattended multiple-plot operation. Intelligence is provided by two 16-bit microprocessors that control the linear actuator pens and proprietary servomotor drive system. Other intelligent features include windowing, LCD plot time display, and built-in diagnostics. Unit is equipped with RS-232 interface and/or optional IEEE 488 interface. The company will also be exhibiting the 5400 54" (137-cm) 4-pen plotter that operates at speeds of 35 to 50 in/s (89 to 127 cm/s), with 4G acceleration and resolution of 0.00049" (0.0124 mm), and 12" (30-cm) plotter models 1453 and 1553. **Nicolet Zeta Corp**, 2300 Stanwell Dr, Concord, CA 94520.



See at Booth 338 Circle 413 on Inquiry Card

PARAMETER LOADING MADE EASY... Set it up once... and forget it, with the...

KILOBYTE CARDTM READER/WRITER for process/machine control applications.

With the Vertel KB-31 System, there is no longer any need to manually enter the same program more than once. Simply enter the program into the system, as you normally would, then let the system record the program on our KILOBYTE CARD with our KB-31 Microloader; when you are ready to re-use that program simply insert the KILOBYTE CARD into the KB-31 and your program will be loaded automatically into your system.



Designed for microprocessor based systems, this rugged, low cost*, fieldproven performer is ideally suited for everything from intelligent terminals and instrumentation to machine tool controls and test equipment.

The 4-stripe magnetic KILOBYTE CARD can record up to 1,088 eight-bit bytes and with the microloader, it is the ideal peripheral for parameter loading, field program modifications, and user activated diagnostics.

*As little as \$199 in OEM quantities.

To learn how the KILOBYTE system can benefit your operations, call or write today

125 ELLSWORTH STREET, CUFTON, N.J. 07012 [201] 472-1331



MAN-MACHINE INTERFACE

Approximately the size of a standard keyboard, key-mat may be used to improve data processing and control applications, such as data entry and automated equipment control. Increased efficiency and productivity and decreased input errors result from simplified operating requirements. The interface consists of 1 switch panel and 1 removable cartridge mechanism. The switch panel features 96 variable keys, 24 page select keys, 12 function keys, and 48 fixed indicators with status lights. With 96 customized legends/page and 24 pages/cartridge, the device has 2304 legends for each cartridge. When employing the maximum 15 interchangeable cartridges, the unit makes 34,560 legends available. Any page is accessible to the operator in less than 1 s. Easy entry of numeric data is ensured by the 10-key numeric pad. System function keys are also provided. The key-mat is microprocessor controlled and may be programmed to supply all necessary information to a controller. Also displayed will be a line of inline high resolution color CRTs in 10, 12, 13, 15, and 19" (25-, 30-, 33-, 38-, and 48-cm) screen sizes, small business computers, and data entry terminals. Panasonic, 1 Panasonic Way, Secaucus, NJ 07094.

See at Booth 1216

Circle 414 on Inquiry Card

HIGH PERFORMANCE DISPLAY MODULES



Project Alpha series 12 and 15" (30- and 38-cm) 110° CRT display modules offer increased reliability, performance, and design flexibility. Design has been simplified and integrated circuits used extensively, resulting in improved overall reliability and increased MTBF. Enhanced video performance provides sharper alphanumeric presentation – 1200 lines center resolution, 950 lines corner (P4), 30-MHz bandwidth, 7% linearity, and 1% geometry. Electrically and mechanically adaptable, the units handle a range of signal input variation whether requirements call for composite video, true TTL sync compatibility, or direct drive. Other features include a streamlined chassis and optional horizontal scan rates. **Motorola Inc, Display Systems**, 1155 Harvester Rd, West Chicago, IL 60185.

See at Booth 1236

Circle 415 on Inquiry Card

SMART CRT TERMINAL



An editing CRT display terminal, the 132/15 features a 15" (38-cm) nonglare high resolution screen, 80- or 132-col format, 7 x 11 dot matrix characters in a 9 x 14 or 9 x 16 cell, and screen labeled soft keys. Eight soft keys make 100 functions accessible to the operator. English language prompts lead the operator through setup and operation modes. There is no need to learn a special language or refer to detailed manual instructions. Features such as bidirectional smooth or jump scroll, horizontal scroll, split screen, communications speeds to 19,200 baud, 4 pages of display memory, and fully displayed status line make the unit suitable for most applications. **Tab Products Co, Electronic Office Products**, 1451 California Ave, Palo Alto, CA 94304.

See at Booth 938

Circle 416 on Inquiry Card

ULTRAVIOLET RADIOMETER

UVX radiometer features LCD readout, self-test circuit, low battery indication, 120-h battery, automatic circuit protection, read/hold switch, external zero adjustment, and negligible emi/rfi influence. The handheld unit weighs

about 1 lb (0.45 kg). When incident radiation exceeds the maximum value of the range selected, the over range indication alerts the operator to switch to a higher range. Over range indication consists of the display of a 1 in the most



significant digit position with the remainder of the digit positions being blank. Interchangeable sensors are calibrated to measure one of the UV bands. Their linearity is proved and checked not to exceed $\pm 1\%$ over the operating range. One sensor measures shortwave radiation, one medium wave radiation, and one long wave (UV-C, UV-B, and UV-A). Internal temperature correction mechanism cancels all but the smallest portion of the sensor's sensitivity to temperature change. **Ultra-Violet Products, Inc,** 5100 Walnut Grove Ave, San Gabriel, CA 91778.

See at Booth 228

Circle 417 on Inquiry Card



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16 bits of information



1. Self-contained and upward compatible. The 8550 Microcomputer Development Lab is the single-user member of the new 8500 Modular MDL Series, which also includes the 8560 multi-user system and the 8540 Advanced Integration Unit for the host computer environment. The 8550 is a complete microcomputer design tool, covering both software development and integration into the prototype. The 8550 can also be used as a station on Tek's forthcoming 8560 multi-user system.

2. Real-Time Emulation. Takes the concept of emulation to a new performance level. Advanced circuitry eliminates the need for wait states during program execution and debugging. The emulator processor now functions in real-time, with its operation totally transparent to the user.



3. Multi-Vendor Chip Support. The 8550 MDL supports 26 chips in all. The broadest support available anywhere, covering a wide range of vendors. With microcomputers as well as microprocessors. The ultimate in design flexibility.

on the new 8550 MDL.

4. 16-bit Support. You'll be able to choose from an entire new generation of 16-bit processors. Tektronix has the high performance tools to make it possible. Assembler support is available now for the 16-bit chips listed below. The TMS 9900 and SBP 9900 are fully supported with emulation today. Real-Time Emulation and Pascal support will be available in stages for the 68000, Z8000 and 8086 beginning the third quarter of 1981.



5. 16-bit Trigger Trace Analysis.

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6.8-bit Support. Besides the most up-to-date microprocessor coverage, you can also take advantage of extensive 8-bit microcomputer support. All 8-bit chip support includes real-time emulation.

6800	8048	3870
6802	8039	3872
6808	8039-6	3874
Z80A	8035	3876
8080A	8021	F8
8085A	8022	1802
8049	8041A	6500/1

7. 8-bit Real-Time Analysis. An optional Real-Time Prototype Analyzer lets you extract both bus and hardware logic at full operating speeds. You capture 48-bit words for storage in a 128-word memory. Two triggers for precise data acquisition.

8. Split-Bus Architecture. The 8550 uses one processor and bus for system operation, and another for real-time emulation. This architecture assures that the emulator processor is denied access to system memory, preventing the possibility of a system crash during prototype program execution.

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13. MDL/ μ **Compiler.** Tektronix' advanced form of Basic, with many extensions for microcomputer development. Often the quickest route from concept to fully developed code.

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CIRCLE 80 ON INQUIRY CARD


GG PRODUCT PREVIEW

Many companies at NCC will be showing products that have either been displayed previously or described in recent issues of Computer Design. Some exhibitors were unable to supply adequate information on their products in time for processing as "first time

shown." These brief summaries are a sampling of additional equipment that NCC '81 attendees can expect to see while touring McCormick Place.

Anadex, Inc-80- and 132-column impact matrix printers models DP-8000 and DP-5000-Booth 2908

Alanthus Data Communications Corp – Small business system, teleprinters, CRT terminals, video and printer storage, and a statistical multiplexer with a switching option – Booth 3214

BASF Systems – Digitized customer engineer diskette for use in aligning 5.25 and 8" floppy disc drives, 5.25" rigid disc drive media, and 16M-byte front loading cartridge for CDC 9448 – Booth 952

Berger-Lahr Corp-2- and 5-phase permanent magnet stepping motors, drivers, and controllers-**Booth 330**

CalComp—Model 953 vector to raster controller, model 1060 54" drum plotter, Graphic 7 graphic display, and variety of plotters and digitizers—Booth 733

Central Data Corp – Multiuser microcomputer system that uses 16-bit processor to support from 1 to 32 users – Booth 5526

Chicago Switch Inc-150 series indicator lights, and 16x series rocker and paddle switches with adapters that fit a standard panel cutout-Booth 1319 **Cipher Data Products, Inc**—Tabletop version of the Microstreamer streaming 0.5" tape unit, 3200-bit/in Microstreamer[™], and vacuum column and tension arm tape drives—**Booth 311**

Computer Automation—Sprint high speed test simulator, Capable 4900M realtime functional test system, SyFA network processing system, and line of Naked Mini 4 computers and peripherals—Booth 2314





EXORciser^{*}I & II MEMORIES

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- Selectable in 4K Increments on either UVA or VXA Controls
- * Write Protect Control in 8K Byte Increments

MM-6800/16



\$849

16KB CORE — 1MHZ

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- Power Monitor for Data Retention
- * Write Protect in 2K Blocks
- * Module Select in 4K Increments
- * No Wait States or Refresh Delay

MM-6800S1



32KB STATIC — 1MHZ

- Single +5V Supply
- Even Parity with Jumper Selectable to NMI, to Parity Error or to IRQ
- Module Select in 4K Block Increments
- * Software Write-Protect in 8K Bytes from Terminal

SIZE

MODEL	PRICE	SPEED	POWE
MM-6800S1	\$650.00	450ns	18 Watt
MM-6800S	\$850.00	210ns	6 Watts

ns 18 Watts 32KX9 ns 6 Watts 32KX9

Temperature Cycled and Burned-in During Memory Diagnostic

ONE YEAR WARRANTY ON PARTS AND LABOR



*trademark of Motorola Corporation

Cyberex, Inc-UPS with printer enunciator display panel and megawatt range UPS-Booth 792

Data-MATE-Model 10860 computer/component equipment desk with suspended bay to house mini/ microcomputer equipment-Booth 974

Data Specialties – Paper tape peripheral equipment – Booth 401

Decitek Corp-See Technology Review, p 48-Booth 1750

Delpha Systems (UK) Ltd-Data transfer Telex system for direct conversion of handwriting into Telex Tape-Booth 1518

Delta Data Systems Corp—Intelligent/ programmable CRT terminals, models D2830, D2400, D7303, and D7586— Booth 2704

Diablo Systems Inc—High quality plastic and metallized daisywheel printers and terminals, forms handling devices, and printer supplies—Booth 1037

Digi-Data Corp-Series 2510 KSR and RO printing terminals, and synchronous 0.5" magnetic tape systems with imbedded formatters and interfaces for PDP-11, NOVA/Eclipse, and HP2100/21MX-Booth 553

Digital Associates Corp—1210 Chain-Train printer, 3601 band printer, and T510 dual-function word processing and data processing printers—Booth 1710

Digital Engineering, Inc-Retro-fit graphics enhancement for the DEC VT100 terminal that provides full graphics plus alphanumerics-**Booth 4428**

Digital Equipment Corp-VAX-11/750 computer system, 124M-byte RM80 Winchester disc unit for the VAX, and 300M-byte RM05 mass storage disc system for PDP-11 and VAX-11/780-**Booth 701**



Elgar Corp-Low cost 3-kVA ac power line conditioner for computer, process control, and high technology electronics-Booth 317

General Electric Co-Terminet 2120 teleprinter, model 200 split platen teleprinter, model 260 forms access unit, and model 510 correspondence printers-Booth 1052

Houston Instrument-See Product Feature, p 231-Booth 911

Integrex Ltd-Color matrix printer requiring no special absorbency paper for text, graphs, histograms, or color video display unit dumps-Booth 1520

Interface Mechanisms, Inc-Portable model 9400 bar code reader with alphanumeric pad for manual data entry as well as wand input-Booth 1541

Lortec Power Systems-15-, 30-, and 60-kW 3-phase uninterruptible power systems designed for maximum reliability and floor space savings-Booth 503

Lynwood Scientific Developments Ltd-Alpha and Beta visual display terminals operating at twice normal frequency for greater clarity-Booth 1611

Magnavox Display Systems-Orion-60 graphics display terminal with plasma display features, touch panel control, and rear projection capability-Booth 1434

Mag-Tek, Inc-MT-6400 hospital admitting system using a reader/writer that encodes 640 chars of data on a magnetic stripe card, and displays encoded information on a 9" swivel screen monitor-Booth 1526

Memorex Corp-Disc storage subsystems, other high technology products-Booth 956

Micropad Ltd-Computer terminal that provides for direct input of hand printed material to a computer system-Booth 1512

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MM-8086/16





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32K BYTES



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MSI Data Corp—User programmable handheld terminals and software as well as related communications products—Booth 3412

Nashua Corp, Computer Products Div-Discs from 5.25" to 14", storage modules, disc packs, and Phoenix compatible discs RL01 and RL02-Booth 4221

NEC Information Systems, Inc-Small business systems, personal computers, and peripheral products including Spinwriter printers, Trimliner 300- and 600-line/min printers, D2200 Winchester disc drives, and FD1160 dual-sided double-density diskette drives-Booth 641

Network Systems Corp-Hyperchannel network adapters that provide computers with universal channel interconnect capability and allow data transmission between system nodes at 50M bits/s-Booth 404

Nixdorf Computer Corp—Word processing, distributed processing, data entry, and small business systems—Booth 856

Pericom Data Systems Ltd-

Multicompatible video display unit, a 64k-byte workstation with disc attachments, can be used for data processing or as Viewdata terminal-Booth 1641

Pertec Computer Corp-Daisywheel printers, tape drives, flexible disc drives, and Winchester disc drives-Booth 832

Prime Computer, Inc-Interactive data processing and networking capabilities, hardware and software including Terminal Application Processing System and Office Automation-Booth 841

Printronix, Inc-300- and 600-line/ min impact matrix line printers with plotting and graphics capabilities-Booth 560



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SEE US AT NCC BOOTH 5412



Quest Automation Research Ltd-Electronic signature verification devices that recognize individual writing rhythms-Booth 1514

Racal-Milgo, Inc-4- or 8-channel Omnimux 40 asynchronous statistical multiplexer-Booth 1117 Rair Ltd-Black Box III microcomputers-Booth 1511

Haymond Engineering Inc- Model 6440 digital cassette recorder based on microprocessor control system that regulates tape speed, tension, and start/stop profile-**Booth 551**



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See us at NCC Booth 311 CIRCLE 87 ON INQUIRY CARD **Rianda Electronics** – Winchester disc and 3M cartridge tape controller on single-board interfaces up to 4 Winchester drives over 600M bytes and backs up 20M bytes in less than 5 min – **Booth 1363**

Rusco Electronic Systems—SAL 510 system activity logger records access events and generates alarm and action messages in several languages— Booth 150

Shugart Associates—SA600 series 5.25" Winchester disc drives and SA410/460 5.25" Minifloppy disc drives—Booth 1201

TEC, Inc-Series 630 Data Screen smart CRT video display terminals with detached keyboard and 12" screen-Booth 542

Time Utilizing Business Systems Ltd – Software tool for file, data entry, and report definitions – Booth 1515

Vector Graphic, Inc-See Technology Review, p 54-Booth 2408

Verbatim Corp-5.25 and 8" diskettes with reinforced hub rings, featuring improved lubricants, burnishing, and linear material for longer life and higher data reliability-Booth 1445

Vu-data Corp-25-MHz miniscope featuring triggered delayed sweep, digital readout of delay time and event counting-Booth 2906

Wabash Tape Corp—Magnetic media including premium Quadronix I tape and G tape made for stringent environmental requirements and Maxi-Byte 8" and Mini-Myte 5.25" diskettes—Booth 1407

Zenith Data Systems—289 computer with built-in floppy disc and 219 video display terminal, and 8" dual-sided, 247 dual-density floppy disc system for use with 289—Booth 4712

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NatioConformation

CIRCLE 89 ON INQUIRY CARD

OPTIMIZING MICROPROCESSOR INPUT/OUTPUT TECHNIQUES

Survey of commonly used I/O techniques reveals design guidelines that help optimize cost and performance for particular application requirements

Lynn E. Costlow

Sperry Flight Systems PO Box 21111, Phoenix, AZ 85036

he impact of microprocessors on the architecture of control systems has resulted in proposals that systems with large input/output requirements use a single dedicated microprocessor to manage the entire input/output function. Many multiple microprocessor architectures and distributed control system architectures have adopted this approach. Realtime control systems demand microprocessor based input/output controllers that efficiently handle "full blown" input/output requirements—discrete (single-bit binary), analog, and digital input/output. This goal must be achieved without excessive software time overhead or hardware cost.

Present popular microprocessors offer computer system designers a wide range of input/output (I/O) capabilities. Optimizing the numerous possibilities into an efficient choice among I/O techniques requires an exhaustive study consistent with cost and performance goals. The strategy should include several basic steps: identifying and characterizing all I/O methods for a selected microprocessor; determining candidate I/O methods and combinations of methods; and selecting the best I/O techniques on the basis of hardware/software and cost/performance trade-offs. However, if peripheral support chips for a given microprocessor type are available, this strategy may not be valid. Therefore, since support chip development typically lags microprocessor market introductions, the approach is best suited for the most recent microprocessors that are not compatible with existing peripheral chip families.

Architectural Background

Many computer based control systems must contend with a massive amount of I/O data. A given architecture might require many relatively slow I/O devices or a few high data rate devices (or combinations). Systems that must control wide bandwidth phenomena may easily saturate the I/O capability of many processor types. Realtime control systems, such as aircraft flight controls, can benefit from the inherent cost advantages of microprocessor technology, provided architectures are designed to be compatible with their abilities. The impetus for using a dedicated microprocessor to control I/O functions is the desire to replace numerous random logic control circuits inherent in previous I/O designs with the power, flexibility, and reduced hardware of a microprocessor based I/O controller. Obviously, hardware is reduced by performing as many I/O control functions in software as possible.

Many multi-microprocessor and distributed control system architectures have been designed recently. Some of these schemes use one microprocessor exclusively for I/O functions in order to offload the central system processor's basic monitoring and control functions. Others further offload the central processor by using excess I/O microprocessor capacity to perform certain additional functions related to I/O (filtering, scaling, formatting, monitoring, limiting, blending, interpolating, compensating) consistent with system growth and architectural criteria.

I/O Techniques

Most widely accepted microprocessors offer some or all of the following I/O capabilities: memory mapping, special I/O program control, external interrupts, and direct memory access (Table 1). Wide variations exist between competing microprocessors in the performance of a given I/O technique. These variations are largely a function of the operating nature of pertinent interfacing signals and the suitability of the instruction repertoire for a given 1/0 technique. Consider, for instance, the implementation of a memory mapping technique that must pass I/O data between a random access memory (RAM) location and a memory location dedicated to an I/O device. Without a memory to memory move instruction in the repertoire, a time-consuming load and store sequence would be necessary to pass data through microprocessor registers. Thus, many otherwise workable I/O techniques hamper a system's throughput or cost-effectiveness by their inefficiency.

		TABLE 1		
		Comparison of I/O Techni	ques	
Microprocessor	Memory Mapping	Special I/O Program Control	External Interrupt	DMA
Intel 8080	Memory references include move, logical, and arithmetic opera- tions, but no memory to memory transfers	256 I/O ports. IN and OUT instructions transfer bytes between accumu- lator and port using 2 status bits strobed onto data bus	Maskable, vectored, non- prioritized, hardware supplies next executable instruction	Bus access gained via Hold and Hold Acknowl- edge signals
Zilog Z80	Same as 8080 plus memory to memory block moves, searches, and bit manipulation	Same as 8080 plus register indirect port addressing and block transfer capability. Uses 12 instructions and 1 signal pin	One nonmaskable inter- rupt plus three maskable modes: 8080 type, restart, and hardware supplied vector	CPU relinquishes buses via Bus Request and Bus Acknowledge signals
Intel 8086	Many register/memory transfers with MOVE, but no memory to memory transfers	256-byte direct ad- dressed or 64k-byte indi- rect addressed I/O ports. IN or OUT instructions and Memory/IO signal handle I/O transfers	One nonmaskable (high priority) plus 255 mask- able, nonprioritized, vectored	Local bus access gained via Hold and Hold Acknowledge signals
Texas Instruments 9900	Many combinations of single register/memory transfers including MOV (word) and MOVB (byte)	Two variable (1-16) length serial, 3 single-bit, and 5 external control instructions work with 3 signal pins	Vectored, prioritized, 15 maskable and 1 nonmaskable RESET levels. No specific inter- rupt acknowledge signal capability	Bus access gained via Hold and Hold Acknowl- edge signals
Zilog Z8000	Extensive single and block memory refer- ences for load, ex- change, and string manipulation	64k-byte I/O ports, std I/O including block trans- fers, special I/O for memory management	One nonvectored, non- maskable and maskable vectored interrupts, hard- ware supplied 16-bit vector	CPU relinquishes bus via Hold and Hold Acknowl- edge signals
Motorola 68000	Extensive data move- ment (8-, 16-, and 32- bit) instructions	Provision for interface of 68000 asynchronous bus with synchronous 6800 series peripheral chips using 3 signal pins and 1 ''move peripheral'' instruction	Six levels priority masked, one level plus reset nonmasked, 256 interrupt and trap vectors	Bus arbitration managed via the Bus Request, Bus Grant, and Bus Grant Acknowledge signals

Memory Mapping

Memory mapping treats 1/O devices as memory locations. Therefore, a memory mapped 1/O interface is essentially the same as a memory interface. 1/O devices share the total address space with actual memory. Fig 1 shows a Texas Instruments SBP 9900 microprocessor and its memory mapped interface as a typical example. Since the 1/O devices are addressed as memory, they must decode addresses generated by the microprocessor. Transfer between "1/O memory" and RAM occurs under program control by execution of one of two software instructions—Move Word (MOV) or Move Byte (MOVB). Use of memory mapping also allows programmers to access 1/O devices via other memory reference instructions in the repertoire.

If an I/O device transfers data too slowly after receiving a decoded address, the 9900 must be forced into the appropriate number of Wait states, that are one clock cycle each, by using its READY signal. This will waste processor time and increase the MOV or MOVB instruction execution time. In addition to the obvious throughput penalty, system speed may be affected in other ways. For example, since interrupts are serviced only at the end of current instruction execution cycles, a longer instruction increases the worst case latency or interrupt service delay. Therefore, the memory mapping technique is most efficient when transferring data to or from I/O devices that incur little or no delay between the time an address is decoded and the time data become ready.

In addition to READY, three other control signals facilitate memory mapped data transfers with the 9900. Memory Enable ($\overline{\text{MEMEN}}$), when active (low), indicates that the address bus contains a valid memory address. Write Enable ($\overline{\text{WE}}$), when active (low), indicates that memory-write data are available for storage in memory. Data Bus In (DBIN), when active (high), indicates that the microprocessor has disabled its output data buffers, allowing the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when direct memory access transfers occur. Virtually all microprocessors have this kind of memory mapped I/O capability, since it is inherent in the ability to communicate with memory.

Special I/O Program Control

Although memory mapping is wholly under program control, it requires no special microprocessor instructions or interface signals that are uniquely associated with the I/O function. Many microprocessors feature special I/O instructions that transfer data to or from peripheral devices via I/O ports. The 8080 repertoire includes two such instructions, IN and OUT that transfer data bus content to or from the accumulator. The data bus contains data transferred to or from a peripheral device (I/O port) selected by the device address presented on the address bus lines during instruction execution. The device address is coded as the second byte of these 2-byte instructions. Since the device address is an 8-bit byte, 256 I/O ports form the maximum I/O address space of the 8080.



Fig 1 Microprocessor memory mapped interface. Memory mapped I/O requires I/O hardware that decodes address, sends or receives (writes or reads) data, and responds to microprocessor memory control signals—all functions that are also performed by RAM. Portion of total address space must be reserved for I/O, which subtracts from maximum memory capacity

Many microprocessors implement the I/O port concept using variations on the fundamental 8080 scheme. Fig 2 shows the special I/O program control capabilities of the 9900, the Communications Register Unit (CRU). The CRU adds a program-controlled, bit serial I/O capability that transfers words containing variable bit lengths (1 to 16) directly to or from the microprocessor. Single-bit instructions include Set CRU Bit to One (SBO) and Set CRU Bit to Zero (SBZ) for output and Test CRU Bit (TB) for input. For multiple (1 to 16) bit operation, Load CRU (LDCR) and Store from CRU (STCR) perform output and input respectively. Up to 4096 input or output data lines are addressed by a 12-bit address bus code that is present during each bit transfer. The interface signals CRUIN, CRUOUT, and CRUCLK handle the serial input data, serial output data, and output data strobe functions respectively.

External Interrupt

Interrupt capability is included in most microprocessors to increase throughput. Although not an I/O transfer technique in itself, the interrupt capability combines with other I/O techniques to synchronize the running program with some external event. With no interrupt capability, some kinds of I/O devices would require periodic software polling to ascertain whether I/O service is required. Microprocessor interrupts may be maskable (enabled or disabled by software), vectored



Fig 2 Communications register unit interface. 9900 devotes three signal pins and five instructions to its special I/O program control capability—in this case a bit serial, variable length, data transfer technique. Five more instructions use CRUCLK as output data strobe for software generated external control pulses

(capable of branching automatically to the interrupt service routine), or prioritized (multiple simultaneous interrupts contend for program service on a priority basis). For example, the Z80 microprocessor offers a versatile combination of one nonmaskable interrupt (typically used in power fail applications) and three maskable interrupt modes. In Mode 0, the peripheral device actually supplies the next executable instruction. In Mode 1, the Z80 responds to an interrupt by performing a restart at a predefined location. And in Mode 2, the Z80 vectors through a hardwired address to any of up to 128 subroutines.

As shown in Fig 3, the 9900 microprocessor interrupt interface features a maximum of 16 interrupt priority levels, the highest of which (level 0) is the RESET function used to initialize the processor. The other 15 levels may be used by external devices. At the end of each instruction, if the INTREQ line is active (low), the 9900 compares the interrupt code $(IC_0 \text{ through } IC_3)$ with the status register interrupt mask. When the level of the pending interrupt is lower than or equal to that of the enabling mask, the processor recognizes the interrupt and initiates a context switch, changing from one subroutine or program environment to another. The microprocessor then forces the interrupt mask to a value that is one less than the currently serviced interrupt (except for the level 0 interrupt, RESET, which loads zero into the mask). Thus, only interrupts of higher priority may interrupt the execution of an interrupt service routine. Since the 9900 design does not include a specific capability for acknowledging interrupts, provision must be made (using memory mapping or CPU outputs) to reset (acknowledge) the appropriate interrupt request before a service routine is complete. All interrupt service routines should terminate with the Return to Workspace Pointer (RTWP) instruction to restore original program parameters.



Fig 3 Interrupt priority levels. In (a), 9900 interrupt interface for up to four interrupts, requests set flipflops and software generated acknowledgments require other I/O hardware to reset flipflops. Interrupt codes IC₀ through IC₃ represent priority levels with IC₃ highest. In (b), 9900 interrupt interface for 5 to 15 interrupts, additional priority encoder hardware is required. Four interrupt lines now represent binary code with IC₀ as most significant bit. Higher binary codes have lower priority levels (binary 15 lowest priority) The 9900 interrupt structure embodies all three basic characteristics of external interrupts. Maskability is inherent in the Load Interrupt Mask (LIMI) instruction. Vectoring occurs via 16 dedicated byte pairs in low memory, which transfer control to interrupt service routines during a context switch. Finally, the 9900 includes a prioritized interrupt structure that prevents lower precedence events from interrupting higher priority servicing.

Direct Memory Access

A direct memory access (DMA) data transfer "disconnects" the processor (via proper control signals) from the address and data buses, allowing an I/O device to generate a memory address and perform a data transfer without processor intervention. The technique is useful for high speed interfaces (through which transfers may occur at memory speed after an initial delay), for avoiding processor I/O task saturation (as during block transfers), and for asynchronous data transfers (that proceed without program control) and/or unsolicited data transfers (that were not requested by the program).

DMA data transfer with any microprocessor involves the following sequence: I/O hardware requests control of system address and data buses from the processor. After the processor relinquishes bus control, I/O hard-



Fig 4 DMA interface. Handshaking controls using HOLD and HOLDA allow DMA transfer after processor yields bus control (and thereby gives up access to memory). Processor also relinquishes pertinent memory control signals to I/O devices during DMA process ware generates the proper memory address, depending on data type and/or I/O device involved. I/O data are then transferred from/to memory under I/O hardware read/write control. Block transfers may occur with appropriate initial address, word counter, and control hardware. Upon I/O transfer completion, the processor regains control of the system bus.

Using the 9900 again as an example to illustrate the general method applicable to any candidate microprocessor, hold facilities (Fig 4) allow both the processor and external devices to access shared memory. To gain bus control, an I/O device sends a Hold Request (HOLD) to the 9900. When the next available non-memory cycle occurs, the microprocessor enters a hold state and signals surrender of the memory bus to the external device via a Hold Acknowledge (HOLDA) signal. When HOLDA becomes active, the 9900 allows I/O control of the signals DBIN, MEMEN, WE, A_0 to A_{14} , and D_0 to D_{15} by forcing all processor drivers to the open circuit state. Reception of HOLDA allows the I/O device to access memory. After the DMA transfer, the I/O device deactivates HOLD, which allows the microprocessor to exit the hold state and regain memory bus control.

The delay that occurs between I/O request and processor release of bus control may be a large factor in limiting DMA throughput, especially for single word transfers. The 9900 delay and the time from $\overline{\text{HOLD}}$ active until HOLDA active is determined by the number of consecutive memory cycles required for the current instruction. The worst case instruction is RTWP, which requires three consecutive memory cycles.

Instruction Speed and Latency Timing

Remaining items in the I/O capabilities of a selected microprocessor relate to timing. A graphical layout of all pertinent I/O timing information for a given microprocessor provides insight into the relative timing characteristics of all I/O techniques. Using the 9900 example again, Fig 5 displays all of the pertinent I/O instruction execution delays and both internal and external 9900 hardware delays (ie, latency times) associated with all of the I/O techniques.

Typical of the time required for a request to propagate through a DMA priority encoder if multiple I/O devices contend for DMA transfers, the DMA REQ to HOLD delay time assumes that no higher priority DMA device has a current request. Some applications may have zero delay. For HOLD to HOLDA, the minimum delay occurs if a memory cycle is not in progress when HOLD is activated. Maximum delay occurs during RTWP instruction execution, which uses three consecutive memory cycles. The memory cycle entry gives the duration of one DMA transfer to or from memory. Multiple transfers occur if required by the 1/0 device (a block transfer situation). HOLD to HOLDA delay occurs at the end of a DMA transfer and can be made concurrent with the last memory cycle of a transfer by deactivating HOLD early enough.

The three times shown for MOV represent one instruction execution with various addressing modes. All cases assume the same addressing mode for both source and



destination operands. The times represent the following addressing modes: 7μ s—workspace register (WR) mode wherein both operands are contained in workspace registers; 11 µs-WR indirect mode wherein operand addresses are contained in workspace registers; and 15 μ s—three addressing modes consisting of (1) WR indirect auto-increment mode wherein operand addresses are contained in workspace registers and are automatically incremented with each use; (2) symbolic mode wherein the first and second program words after the MOV instruction contain the source and destination operand addresses respectively; and (3) indexed mode wherein the next program word contains an operand base address which is added to an index value in a workspace register to form an effective operand address.

For memory mapped single word transfers, the symbolic mode (15 μ s) should be the most useful, since it does not require indexed or auto-incremented action and no workspace registers are wasted. However, the

WR indirect auto-increment mode (also $15 \ \mu s$) is the most attractive for memory mapped block transfers because of its inherent operand address incrementing feature, which eliminates a separate instruction, Add Immediate in the indexed mode, for indexing both source and destination operand address index values. The times shown for MOVB are identical to MOV delays with one exception: the WR indirect auto-increment mode consumes only 13 μs instead of 15 μs .

SBO, SBZ, and TB, all single-bit CRU instructions, consume a fixed $6-\mu s$ interval. The short times (11, 13, and 15 μs) for LDCR represent the same addressing modes as for the MOV instruction to transfer one CRU bit from memory. Multiple (2- to 16-) bit transfers take longer as shown. STCR is the same as LDCR except that different times and data are transferred to memory. CKOF, CKON, LREX, RSET, and IDLE are the same as SBO, SBZ, TB. The 11 μs for interrupt latency represents the time required to accomplish a context switch after the processor recognizes an interrupt. The additional time is variable and exists because the processor checks for interrupts only at the completion of each instruction. Thus, the instruction mix affects the upper limit of interrupt latency. In addition, a system using DMA will also increase worst case latency. RTWP, the return instruction, consumes a fixed 7 μ s at the conclusion of each interrupt service routine.

Selecting an I/O Technique

As previously described, three fundamental I/O methods are possible with microprocessors: DMA, memory mapping, and special I/O program control. In addition, the interrupt capability may be used in conjunction with these methods. Each of the various I/O interfaces may require one of several combinations of the basic techniques for the desired performance at the least cost. With this in mind, the group of I/O control techniques is defined for further analysis in order to optimize I/O architecture (Table 2).

1/0 Program Control Alternatives

Program control of an I/O device involves any of the following software controlled actions: trigger, start, initiate, reset, and interrupt acknowledge. For most microprocessors, the two alternatives for I/O device program control are memory mapping and special I/O. For the 9900 example, memory mapping is preferable to the CRU method for two reasons: during single-bit I/O control operations, neither method has a significant speed advantage (MOV requires 7 μ s; SBO or SBZ requires 6 μ s); and I/O device address decoding hardware is 16 times more complex for a CRU (LDCR) 16-bit transfer than for a MOV because each serial CRU bit is selected by a separate address bus code.

Feasibility of I/O Candidates

Twelve candidate I/O techniques have now been recognized. The next procedure is to ascertain which techniques are feasible for each of the interface types encountered in control systems. Table 3 presents a matrix of I/O techniques versus interface types. Its purpose is to determine the workable (but not necessarily the optimum) I/O techniques for each interface.

The interface types are discrete, analog, and digital, with inputs and outputs for each. Discrete inputs are binary digital asynchronous input data that are sampled "raw" without using memory elements in the interface. Discrete outputs are binary digital output data that incorporate a latch per bit in the interface for data retention between output updates.

Analog inputs are data from a single analog to digital converter (ADC) using a multiplexed analog input and transforming multiple analog signals into a word serial, bit parallel data stream. The ADC is characterized by the requirement for a "start command" and a delay (typically 10 to 50 μ s) until "conversion complete," followed by successive delays and "conversion complete" data. Therefore, block transfers of analog to digital data cannot match typical microprocessor memory speeds.

TABLE 2

I/O Control Techniques

I/O MethodDefinition(1) DMAI/O Hardware "cycle steals" memory: software ignorant of all I/O data transfers(2) DMA under Program controlSame as (1) with addition of software capability to ini- tiate or otherwise control I/O devices (as opposed to data transfer)(3) DMA with interruptsSame as (1) with addi- tion of interrupts to notify program that I/O device ac- tivity has occurred, ie, "buf- fer complete" or "data ready"(4) DMA under program control with interruptsCombined features of (2) and (3)(5) Memory mapped I/O under program controlProgram performs all I/O using MOV (or equivalent) instructions(6) Memory mapped I/O under program controlSame as (5) with addition of program control of I/O devices(7) Memory mapped I/O under program controlSame as (5) with addition of program control of I/O devices(8) Memory mapped I/O under program con- trol with interruptsProgram performs all I/O using I/O ports and special instructions(9) Special I/O under program controlProgram performs all I/O using I/O ports and special instructions(10) Special I/O under program controlSame as (9) with addition of program control of I/O devices(11) Special I/O under program controlSame as (9) with addition of program control of I/O devices(22) Special I/O under program controlSame as (9) with addition of program control of I/O devices(23) Special I/O under program controlSame as (9) with addition of interrupts to indicate I/O devices(24) Special I/O under program control		NO CONTO TE	criniques
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12) Special I/O under Combined features of (10) program control and (11) with interrupts	11)	Special I/O with interrupts	Same as (9) with addition of interrupts to indicate I/O device activity to program
	12)	Special I/O under program control with interrupts	Combined features of (10) and (11)

Two types of analog outputs are considered: sample/ hold and multiple digital to analog converter (DAC). The sample/hold type consists of one holding register that drives one DAC which drives multiple analog sample/hold output circuits. Its operation is characterized by the following sequence:

All sample/holds in "hold" mode Read number for memory Load number in DAC holding register Delay for DAC output to settle Place proper sample/hold in "sample" mode Delay for sample/hold voltage acquisition Return sample/hold to "hold" mode Repeat above for next sample/hold

			1/0	Cont	TA rol T	BLE	3 ques	Matr	ix						
1/0	SOFT REQUIF	WARE REMENTS			UGRAM	TERRUPTS	UPTS CONTROL	PPING	M CONTROL	UPTS UP	VD INTERRICERAM	Sun	AND ONTROI	UPTS	VD INTERRUPTS
INTERFACE	PROGRAM INITIATION OF 1/0 BUFFER	PROGRAM KNOWLEDGE OF 1/0 BUFFER COMPLETION	PMG (1)	CONTAND PL	DINA AND	AND MA PROGE	C MEMORY	(C) MEMORY MI	MEMORY M	CONTENT	C SPECIAL	E SPECIAL LING	E SPECIAL LING	E SPECIAL 1/0	4
DISCRETE INPUTS	CONDITIONAL	CONDITIONAL	N	Y/N	N/Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
DISCRETE OUTPUTS	CONDITIONAL	CONDITIONAL	N	Y/N	N/Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	
ANALOG INPUTS	YES	YES	N	Y/N	N/Y	Y	N	N	N/Y	Y	N	N	N/Y	Y	
SAMPLE/HOLD TYPE ANALOG	YES	CONDITIONAL	N	Y/N	N/Y	Y	N	N	Y	Y	N	N	Y	Y	
OUTPUTS DAC/LATCH TYPE	YES	CONDITIONAL	N	Y/N	N/Y	Y	Y	Y	Y	Y	Ý	Y	Y	Y	
SOLICITED	YES	CONDITIONAL	N	Y/N	N/Y	Y	N	N	N	Y	N	N	Ν	Y	
UNSOLICITED	NO	CONDITIONAL	N	Y	Y	Y	N	N	Y	Y	N	N	Y	Y	
SOLICITED DIGITAL	YES	CONDITIONAL	N	Y	N	Y	N	N	N	Y	N	N	N	Y	
OUTPUTS UNSOLICITED	NO	CONDITIONAL	Y/N	Y/N	Y	Y	N	N	Y	Y	N	N	Y	Y	

The multiple DAC type consists of one holding register driving one DAC for each output. It operates faster than sample/hold (no delays incurred for DAC and sample/ hold settling) and may be updated at memory speeds.

Two categories of digital inputs—solicited and unsolicited—are considered. In the solicited type, data input time is determined by the program; in the unsolicited type, data arrival for input is determined by "outside world" timing. The two categories of digital outputs are the same as for digital inputs; data direction is the only difference. Both digital inputs and digital outputs commonly involve multiple interfaces.

In addition to 1/O techniques and interface types, Table 3 presents two software requirements for each interface type: program buffer initiation and program buffer completion knowledge. These requirements may vary with the application and/or the software 1/O architecture. The process by which the matrix squares is filled is somewhat subjective, but does allow unworkable 1/O combinations to be eliminated. In general, the definition of the interface, its software requirements, and the pertinent 1/O technique definition must all be considered in arriving at the results. Some of the results are debatable.

The matrix entries shown represent a particular application. An example of the process used to derive the entries is the case of the input discrete interface as implemented with I/O technique 2 (DMA and program control). Input discretes may or may not require program initiation of their input, and the program may or may not require knowledge that all input discretes have been sampled (buffer complete). I/O technique 2 does include the capacity to initiate I/O activity because of its program control feature. However, since the software will be ignorant of the ensuing DMA input buffer, the program has no way to detect "buffer complete." Therefore the matrix entry in this case is YES/NO (can initiate buffer/cannot indicate buffer complete). A single YES (or NO) indicates total compatibility (or incompatibility) of an interface type with an I/O technique.

Analysis of Candidate I/O Techniques

For the particular application shown, only three (4, 8, and 12) of the 12 I/O techniques have been found to be operationally compatible with all the types of interfaces. However, it should not be concluded that one of these three is the most desirable technique. A judicious selection of any of the workable types of the 12 techniques for each kind of interface should be based on hardware/ software trade-offs, hardware cost trade-offs, and speed requirements.

Hardware/Software Trade-Offs

As already stated, the total I/O implementation should minimize hardware at the expense of software, provided other constraints, such as timing, permit. Therefore,

Re	TABLE 4 lative Hardware Overhead		Maximum Blo	TABLE 5 ock Transfer Data	Rates
Interface Circuit Map decoder Interrupt encoder I/O device interrupt DMA controller I/O device DMA	Description Decodes 32 addresses Encodes 16 interrupts Interrupt circuit required on each I/O device Services 8 I/O devices DMA circuit required on each I/O device	Number of DIPs 5.5 5.17 2 12 4 to 10	<u>I/O Method</u> CRU (LDCR, STCR) Memory mapped (MOV) DMA Interrupt context switch with one MOV (15 µs)	Data Rate 29k to 38k 67k to 143k 1M 30k max	(words/second) , dependent on addressing mode
In A-D D-A (sample/ho UART ¹ (receive ARINC ² (receive Input discretes Output discretes Programmable F	tterface Id) or transmit) digital e or transmit) digital s RTC ³ ronous receiver/transmitter io, Inc	TAE Relative T Devic Data R (words/se 20k 8.33 5.21 417 to 20 20 1k	BLE 6 Throughput ate Number perces 1 1 2 UARTs 806 5 6 4 1 1 1 1 1 1 1 1 1 1 1 1 1	5	Effective Data Rate 20k 8.3k 20.8k 2k to 4k 120 80 1k 4.3k words/s max total

memory mapping or special I/O program control is preferred over DMA where interface speeds permit and if hardware costs less than DMA. However, because of the multiplicity of interfaces, the use of interrupts and/or DMA, the need for future growth, and the possible use of the microprocessor for tasks other than I/O control, the selected method(s) should never depend on softwaregenerated delays or timing loops. The initial goal of using software as much as possible must therefore be carefully limited so that the processor is not saturated for extended periods with I/O tasks.

Hardware Cost Trade-Offs

As mentioned previously, the 9900 CRU I/O is not competitive with memory mapping in terms of hardware cost. Moreover, for word transfers (as opposed to single-bit program control operations), memory mapping provides a speed advantage of a factor of two. (See Fig 5.) Therefore, I/O techniques 9 through 12 (special I/O and combinations) should not be considered further. The relative hardware costs of the remaining I/O techniques may be further compared with Table 4, from which the following information may be derived by using hypothetical averages. Dual inline packages (DIPs) required per memory mapped I/O device per address are

$$\frac{5.5}{32}\simeq 0.17$$

DIPs required per memory mapped I/O device per address when using an interrupt are

$$\frac{5.5}{32} + \frac{5.17}{16} \simeq 0.17 + 0.32 = 0.49$$

DIPs required per DMA I/O device are

$$\frac{12}{8}$$
 + (4 to 10) = 5.5 to 11.5

DIPs required per DMA I/O device when using memory mapped control and an interrupt are

$$(5.5 \text{ to } 11.5) + 0.17 + 0.32 = 5.99 \text{ to } 11.5$$

Thus, it can be concluded that memory mapping has a definite hardware advantage (even when used with interrupts) over DMA methods. The only remaining justification for DMA must therefore be based on timing considerations.



Speed Requirements

All of the fundamental I/O timing information has been presented in Fig 5. The relative comparison of I/O technique speeds may be better illustrated by deriving the maximum block transfer data rates for each method. All of the data rates in Table 5 represent processor "saturation" for the duration of the transfer. The CRU data rate is shown for reference only. Table 6 shows data rates for I/O interfaces encountered in a typical aircraft flight control application.

Thus, it is clear that memory mapping will not have the required speed to handle all interfaces if interrupts are used and/or future system expansion is desired; DMA must be used in spite of its costlier hardware.

I/O Technique Selection Algorithm

Fig 6 illustrates the series of decisions required in selecting the optimum I/O technique for each type of interface. After the designer has answered the four levels of questions, the flow chart recommends one of the 12 I/O techniques presented in Table 3. Possibly the most subjective decision to be made is the first one on speed. Factors influencing this decision are not only the speed requirement of the interface under consideration, but also the number of other devices with medium to high speed, the amount of growth capability desired, and the amount of program and program time the designer is willing to commit to I/O transfers. (DMA requires less.)

Summary

For realtime control system applications, microprocessor I/O techniques must be optimized in order to achieve desired levels of performance and costeffectiveness. Fundamental I/O methods available with most microprocessors are memory mapping, special I/O program control, external interrupts, direct memory access, and their combinations. Although several methods may be workable in a given application, they may represent an inefficient design in terms of system cost and performance. Optimizing system I/O design involves hardware/software trade-offs, hardware cost tradeoffs, and anaylsis of data rate requirements. Individual I/O interfaces require differing techniques to be identified and combined to achieve the most efficient design.

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INTEGRATED ARITHMETIC PROCESSING UNIT ENHANCES PROCESSOR EXECUTION TIMES

Hardware and software fundamentals stress efficiency and simplicity when interfacing an arithmetic processing unit to various popular microprocessors

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With the advent of 8-bit microprocessors as standard off the shelf components of modern digital systems, designers often face the need to incorporate arithmetic processing capabilities into microprocessor based systems. Conventional fixed point (integer) arithmetic is relatively easy to implement with minimal software overhead and reasonable execution times. However, floating point arithmetic and mathematical function evaluation involve considerable software overhead and relatively long execution times, and for these, integrated arithmetic processing units present a viable alternative to software arithmetic modules.

Architecturally designed for arithmetic operations, an arithmetic processing unit (APU) requires very little host microprocessor overhead. Its self-contained algorithmic execution results in powerful arithmetic capabilities at reasonably high speeds. An APU interface provides a microcomputer with hardware arithmetic and mathematical function capabilities that can be accessed by appropriate subroutine calls. Interfacing hardware capabilities to augment the computational abilities of a microcomputer is a common design approach that achieves enhanced computational power, higher speed, and reduced software overhead. Typical examples of this approach include interfacing a calculator chip to a microprocessor to obtain binary coded decimal floating point capability, and adding multiply/divide hardware to provide fast multiplication and division with minimal programming requirements.

Hardware Considerations

Chosen to illustrate general hardware and software interfacing principles, the AM9511 is a fully integrated, metal oxide semiconductor (MOS) device capable of performing 16- and 32-bit fixed point arithmetic, 32-bit floating point arithmetic, and a variety of floating point trigonometric and mathematical operations. All transfers between the host microprocessor and this APU use its 8-bit bidirectional data bus (DB_0 to DB_7), including status and command transfers. APU interface signals are conveniently partitioned into bus control signals and interface control signals (Fig 1).



Bus Control Signals

Bus control signals include Chip Select (\overline{CS}), an active low signal that conditions the Read (\overline{RD}) and Write (\overline{WR}) signals. In conjunction with \overline{RD} and \overline{WR} , the Command/ Data (C/\overline{D}) line establishes the types of transfers that occur on the data bus. When C/\overline{D} is low, APU read and write operations access data. When it is high, read operations return APU status and write operations enter APU commands.

The PAUSE output generally indicates that the APU is busy: valid data are not available and no additional commands or data can be passed to the APU. PAUSE always goes low in response to either a read or a write. During write operations, PAUSE stays low for a maximum of 50 ns while the APU transfers the requested byte to the data bus port. During a data read operation, PAUSE duration depends on the APU state. If the APU is not busy, PAUSE will be low only for the time required to transfer the requested byte to the data bus port, but if the APU is busy when a request for data is made, PAUSE will be extended until the APU has completed the operation and valid data are available. When reading status, PAUSE remains low only for the time required to transfer the status byte, regardless of whether the APU is busy.

Interface Control Signals

Interface control signals synchronize APU and host microprocessor operation. RESET initializes the APU by terminating any operation in progress, clearing the status register, and placing the APU into an idle state. The Clock (CLK) input pin furnishes an external timing source for the APU. This input can be obtained from the microprocessor clock circuitry-either directly or through appropriate down counting-or from an independent timing source. An End Execution (END) output indicates that the APU has completed execution of a previously entered command. It is cleared by the End Acknowledge (EACK) input, by RESET, or by any read or write to the APU. In a direct memory access (DMA) interface, END would be used as the DMA request line and EACK would correspond to the DMA request acknowledge line. In an interrupt driven interface, END could be used as an interrupt request source and EACK could be used as an interrupt acknowledge. If EACK is tied low, however, the END output will be a pulse of less than one clock period in width. This configuration provides a useful interrupt request source for an interrupt controller such as the AM9519 or the Intel 8259.

A Service Request (SVREQ) output indicates that the APU has completed execution of a command for which the service request bit was set. SVREQ is cleared by the Service Acknowledge (SVACK) input, by RESET, or by completion of a command that did not set the service request bit. SVREQ can be used as an interrupt request line in much the same way as the END signal. With a DMA interface, the SVREQ line could initiate an interrupt and signal the end of a series of DMA operations that was supervised by END and EACK signals.

Functional Operation

The APU is a stack oriented device; all arithmetic operations are performed using data in the top of stack (TOS) and next on stack (NOS) positions. For 16-bit operations, the stack is configured as an 8-level, 16-bit push down list [Fig 2(a)]. Stack operands are pushed onto the stack beginning with the least significant byte (LSB) and ending with the most significant byte (MSB). For 32-bit operations, the stack is configured as shown in Fig 2(b) and is limited to only four levels of data.

Most arithmetic operations take one or two operands from the TOS and NOS positions, popping the required number of operands from the stack and pushing the result as the new TOS. For example, to extract the square root of the TOS, the operation code for square root is sent to the APU, and the result replaces the TOS operand. (One exception is the exponentiation function, X to the Y power, which raises the NOS operand to the TOS power and replaces the TOS operand with this result, leaving NOS unchanged.) Apart from arithmetic and mathematical functions, several APU operations perform utility functions such as pushing or popping the stack, converting the TOS between fixed and floating point format, changing sign, and pushing the value of pi.

Fixed point APU data are encoded as 16- or 32-bit, 2's complement integers. Floating point data consists of two parts: an exponent and a mantissa [Fig 2(c)]. The mantissa is a 24-bit, signed, normalized value between 0.5 and 0.9999999 (or zero) decimal, encoded not in 2's complement form, but as a sign-magnitude value. The exponent is a 7-bit, 2's complement value ranging from -64 to 63 decimal. This floating point format can



represent decimal numbers in the range of $\pm 9.22 \times 10^{18}$ with a granularity of about 2.71 x 10^{-20} .

One important feature that helps to optimize software drivers is the APU status register (Fig 3). APU status can be accessed at any time by performing a read operation while C/D is high; however, status bits 0 to 6 are valid only if the busy bit (bit 7) is zero. Thus, the status byte indicates whether or not the APU is busy and, if it is not busy, indicates some critical features of the preceding operation. For example, following a division operation, bits 3 and 4 indicate whether division by zero was attempted. If it was not, the remaining bits indicate whether a carry was generated, whether overflow or underflow occurred, and whether the quotient was zero, positive, or negative. APU commands are a single byte, formatted as in Fig 4. The command byte is partitioned into three fields: an operation code (bits 0 to 4), a data field (bits 5 and 6), and a service request field (bit 7).

Upon application of power, a reset signal is required to initialize internal flags, registers, etc. Specifications state that reset must be applied for at least five clock periods. Also, there is a maximum reset time (not cited in the specification) which, if exceeded, may damage the



chip. Reset apparently floats certain internal signal lines. If allowed to float, a MOS gate input assumes a voltage about midway between power and ground and, unlike a transistor-transistor logic input, allows both gate output transistors to turn on, thus overheating the chip. A reset interval of 16 clock cycles is adequate to reset the device without causing damage.

Fig 5 solves the reset problem by providing a reset signal that does not depend on the duration of System Reset (SYRT). Upon application of SYRT, the 74193 counter is cleared. Then, when SYRT is released, the counter begins to count up. The Carry Output (\overline{CY}) is high during this time, gating SYRT through to the APU. After 16 clock cycles, \overline{CY} goes low, removing the reset from the APU and blocking any further clock pulses to the 74193.



APU Interfacing

A critical part of the APU interface design involves handling the difference in operating speeds between the APU and its host microprocessor. To allow for the disparity of speeds, the APU was designed to accommodate several different interface philosophies. First, one may use a forced wait approach in which the microprocessor is driven into a wait mode until APU operation is complete. Second, a polled approach can be used to monitor status continually until the current APU operation is complete. And third, the APU can interrupt the microprocessor upon completing an operation. Each of the three basic methods has its advantages, ranging from the simplicity of the forced wait approach to the most efficient use of microprocessor time with the interrupt driven method.

Forced Wait Interfaces

The forced wait interface is perhaps easiest to implement because PAUSE can force the microprocessor into a wait state while any APU operation is under way. PAUSE is asserted whenever an operation is in progress and either command entry or data access is attempted, or when the APU is not busy and either data entry or data removal is requested. The APU also asserts PAUSE for the time required to transfer its status byte to the output latch, whether it is busy or not.

In a Z-80A interface using the forced wait approach, the Z-80A address bus is decoded to provide \overline{CS} for a specified direct input/output (I/O) or memory mapped address space (Fig 6). Because the C/ \overline{D} signal is AB₀, read or write operations with AB₀ = 0 enter or remove APU data. With AB₀ = 1, a write to the decoded address space enters an APU command, and a read with AB₀ = 1 gates APU status onto the data bus. The PAUSE output from the APU connects to the Z-80A WAIT input through a noninverting open collector buffer, allowing other peripherals to access the WAIT input by means of a wired-OR configuration.

The APU clock is derived from the 4-MHz Z-80A system clock through a simple flipflop. As it need not be synchronous with the host microprocessor clock, it could also be independently derived. A typical operating sequence for the forced wait interface involves three steps. Data are loaded into the APU. A command is next sent to the APU, and data removal is attempted. If the APU is still busy, PAUSE goes low and forces the Z-80 into a wait state, where it remains until the current APU command is completed, at which time PAUSE goes high and data can be removed. A status read forces the Z-80A into a wait state





only until APU status information has been transferred to the output buffer and placed on the data bus.

Forced wait interfaces are simple and easy to implement. However, they have the disadvantage of being unsuitable for use with dynamic memories that rely on Z-80A refresh signals because APU commands with execution times exceeding 2 ms would cause dynamic memory to lose data while the Z-80A remains in its wait state. Therefore, the forced wait interface applies only to systems that use static memory or independent refresh generators (or those that execute only APU commands with suitably short execution times).

In a forced wait interface for the 8085, the PAUSE signal actuates the 8085 Ready (RDY) line [Fig 7(a)]. Fig 7(b) shows timing requirements that the circuit must meet. Once it has been selected by either \overline{RD} or \overline{WR} , the APU asserts PAUSE within 150 ns. The 8085, on the other hand, requires a "not ready" signal at least 110 ns prior to the rising edge of the clock. An 8085 running at 3.072 MHz has a low clock time of 163 ns. As shown in Fig 7(b), \overline{RD} is asserted on the falling edge of the clock and RDY must remain low for at least 110 ns before the rising edge of the clock in order to begin a processor wait cycle. If the APU generated PAUSE in less than

163 - 110 = 53 ns, the PAUSE line could be tied directly to RDY. However, since the actual time specification from the falling edge of RD to the falling edge of PAUSE is 150 ns for the APU, some additional lookahead circuitry is required.

To ensure RDY actuation within the required time, the circuit of Fig 7(a) uses FF1 to store the APU read request until the APU can generate the necessary \overline{PAUSE} signal. Following SYRT, FF1 is reset along with the APU, allowing RDY to go high. The occurrence of \overline{CS} (from the address decode logic) and Input/Output Read (\overline{IOREAD}) indicates an APU read request and clocks FF1. Then, the output goes high and holds RDY low, halting the microprocessor. When the APU generates its own \overline{PAUSE} , it resets FF1. In addition, RDY is held low through an open collector inverter. Then, when the APU removes \overline{PAUSE} , RDY is released and the microprocessor resumes operation.

Polled and Interrupt Driven Interfaces

With minor exceptions, polled and interrupt driven interfaces use essentially identical circuitry (Fig 8). Both





methods require a means of extending the read cycle to satisfy APU timing. This is not necessary with the forced wait approach because the PAUSE signal effectively stretches critical read cycles. The worst case APU read cycle lasts 5.5 T_{CY} + 300 ns, where T_{CY} is the clock period. Obviously, a Z-80A or 8085 operating at maximum speed has a RD signal that is much too narrow for the APU. A relatively simple scheme stretches \overline{RD} by forcing the Z-80A into a wait state when \overline{CS} and \overline{RD} both are active. When this condition occurs, the D flipflop is set, and WAIT is forced low. At the same time, the counter is enabled and begins to count APU clock cycles. When Q_3 of the counter goes high, eight clock pulses later, the D flipflop is reset and the microprocessor continues the current read cycle. System reset is NORed with the Q₃ output to ensure a known state on power up. A slight increase in speed can be achieved by decoding the sixth pulse rather than Q₃, but at the cost of added complexity.

In operation, data and commands are set to the APU using output instructions or memory writes, depending on the mapping scheme. Once an operation code is written to the APU, software reads the APU status and loops on busy (bit 7). When busy goes low, software exists the loop and pops the result from the TOS. Fig 8 includes the additional logic required to generate an interrupt once APU command execution is complete. If the most significant bit of the operation code (bit 7) is set, the SVREQ output will go high once a command has been executed and remain high until \overline{SVACK} is brought low. SVREQ is inverted to provide an active low interrupt request signal. It is reset by reading APU status or data, or by decoding \overline{SVACK} from \overline{RD} and \overline{CS} . In operation, a dummy status read resets SVREQ before a command is sent to the APU.

A slight variation of Fig 8 interfaces the APU with an IEEE-976 bus. Here, \overline{XACK} decoded from \overline{CS} and \overline{WR} provides an active low signal to inform the bus that a transfer is complete. The circuit of Fig 8 also allows use of the APU in an interrupt interface with the 8085. If the APU receives an operation code with bit 7 set, it asserts SVREQ once the operation is complete. SVREQ is reset when \overline{SVACK} is pulled low. SVREQ can be tied directly to an interrupt port, such as the 8259 Programmable Interrupt Controller, or to one of the 8085 restart inputs.

Using a polled interface, software monitors APU status continually until the APU clears its busy bit to indicate that an operation is complete. Although polling is the easiest means of synchronization, it can delay the APU by keeping it so busy loading status data that it cannot begin the operation. A simple solution is to insert a NOP instruction and thus extend the microprocessor polling loop, giving the APU ample time to initiate its operation. Status polling does not degrade performance once the APU has actually begun an operation.

The APU must be programmed with caution in an interrupt driven application. If two or more interrupt service routines use the APU, data status buffers must be unloaded at the beginning of each interrupt handler, saved, and restored at the end of the interrupt handler. The time spent shuffling data back and forth through a 1-byte data port could seriously degrade interrupt response time. Another major problem occurs when trying to restore the APU status byte. There is no convenient way to set APU status directly, and any routines that use the sign zero or carry bits of the status byte could therefore fail to recover properly from an interrupt.

Software Considerations

The method of connecting the APU to a microprocessor determines the ways whereby software can handle the APU, which appears to programmers either as an 8-bit I/O port (with an isolated I/O interface) or as a set of memory locations (using memory mapped I/O). Memory mapped I/O typically allows greater programming flexibility because many more microprocessor instructions reference memory space than reference I/O ports. For example, instructions that move register data to memory, move immediate data to memory, load or store an accumulator, reference 16-bit memory data, and perform arithmetic on memory operands can all benefit a memory mapped I/O interface. Some processors, such as the Z-80A, offer block move instructions that can be used to great advantage here. Drawbacks of the memory mapped approach include a slight reduction in available memory space and a slight increase in the time required to pass a byte of data to or from the APU.

The isolated I/O approach to APU interfacing leaves the memory space intact and simplifies transferring data to and from the APU. Again, even though data transfer is greatly limited under the isolated I/O approach, some processors such as the Z-80A offer certain special I/O instructions that enhance APU programming.

Regardless of the interface technique used, an APU programming philosophy should allow efficient use of the APU with a minimum of redundant program code and programming effort. For example, an isolated APU operation is easy to program by pushing the operands, issuing an operation code, and popping the result from the APU stack. On the other hand, complicated expression evaluation involving storage and retrieval of intermediate results becomes quite unwieldy if each state of evaluation is treated as a discrete operation. Efficient and effective use of the APU requires an efficient and effective interface in both hardware and software.

8080A and 8085 Programming

Transferring operands between memory and the APU stack presents a basic programming problem. Because they lack block move, transfer, increment, and repeat instructions, microprocessors such as the 8080A and 8085

are restricted in their ability to perform efficient multibyte transfers involving memory or I/O ports. Two small subroutines, FPUSH and FPOP, can transfer a 4-byte value between memory and the TOS:

FPUSH	INX INX INX MVI	H H H B,4	address LSB set byte count
FPS1	MOV OUT DCX DCR JNZ RET	A,M APUD H B FPS1	get byte output to port decrement pointer and counter loop until done
FPOP	MVI	B,4	set byte count
FPP1	IN MOV INX DCR JNZ RET	APUD M,A H B FPP1	get byte from port store it increment pointer decrement counter loop until done

These subroutines assume that floating point values are stored in memory with the exponent at the low byte address and the 3-byte mantissa at successively high addresses. For example, decimal 10 would be stored as the hexadecimal byte string 04, A0, 00, 00. To push this floating point value onto the APU stack, the two 00 bytes are supplied to the APU data port, followed by the A0 byte and finally the 04 byte. The reverse process retrieves APU data.

Other assembly language routines allow the 8080A or 8085 to handle APU data efficiently by using the FPUSH and FPOP subroutines to implement efficient chaining of mathematical operations. Each routine is entered with the address of one operand in the HL register pair; the second operand is assumed to be the TOS. For example, a floating point addition routine could be coded as

FADD	CALL	FPUSH	push to APU
	MVI	A.10H	get add command
	OUT	APUS	output to port
	JMP	FOVUN	wait for results

with subtraction (FSUB), multiplication (FMUL), division (FDIV), and other routines differing only in the operation code supplied as immediate data in the second statement. All routines exit through a common routine, FOVUN, which checks the APU status bits and branches to an error recovery routine if underflow, overflow, division by zero, or other error is detected. FOVUN also waits until the APU has completed its current operation. (For any series of operations, it makes little difference whether the processor issues a command to the APU and then waits for a result or waits instead until the APU is idle and then issues a command.) On normal exit from FOVUN, the APU top of stack contains the result of the operation, and the APU is set up for the next call to perform the next operation in the chain.

FOVUN	IN	APUS	get APU status word
	ANI	80H	loop on busy bit
	JNZ	FOVUN	CARLES AND ADDRESS OF
	IN	APUS	get status word
	ANI	18H	check error field
	JNZ	ERROR	jump to error routine
	RET		A A A A A A A A A A A A A A A A A A A

A floating point interpreter (Fig 9) can further simplify assembly language APU programming. The interpreter might be controlled by sequences of 3-byte control blocks, each directing one APU operation by specifying a 1-byte operation code and a 2-byte target address. An interpreter call can be followed by as many 3-byte control blocks as required to evaluate a complete expression, however complicated. The final control block invokes an exit operation to return from the interpreter and resume mainline processing. Assembly language macros that expand to produce the 3-byte operation blocks further streamline the programming required to evaluate complicated expressions. For example, by defining the macros

FPU	MACRO DB DW ENDM	ADDR 4 ADDR	(code for FPUSH)
FPO	MACRO DB DW ENDM	ADDR 8 ADDR	(code for FPOP)

and so on for each of the FADD, FSUB, FMUL, and other routines discussed earlier, evaluation of the floating point expression D = (A + B)/C can be programmed in its entirety with a strikingly economical and efficient result as

CALL	FINTP	enter interpreter
FPU	A	push A
FAD	В	add B
FDV	С	divide by C
FPO	D	pop result
FEX		exit interpreter

Z-80 Programming

Z-80A interface software benefits from instructions peculiar to the Z-80. With conventional memory mapping, for example, the Out Increment and Repeat (OTIR) and the In Decrement and Repeat (INDR) instructions offer a convenient means of transferring data to and from a memory mapped APU. If data storage is organized as four contiguous bytes with the LSB at the lowest address, the following macro or subroutine transfers data from memory to the APU:

LD	HL,DATA	load LSB address
LD	BC,256* 4+APUD	load byte count
OTIR		push APU data

Similarly, the reverse operation transfers results from the APU to memory:

LD	HC,DATA+3	load MSB address
LD	BC,256 * 4+APUD	load byte count
INDR		pop APU data

Memory mapped interfaces also benefit from Z-80 block move instructions, provided that the C/\overline{D} line is driven by A_2 of the address bus (or similar decoding) to prevent the APU from changing mode during a transfer. Then, program fragments to load or unload a memory mapped APU would be

LD LD LD LDIR	HL,DATA DE,DATIN BC,4	load LSB address load APU data address load byte count load APU data	
LD LD LD LDDR	DE,DATA + 3 HL,DATOUT BC,4	load MSB address load APU data address load byte count unload APU data	

Consider, for example, a general purpose routine to perform an arbitrary function on a 32-bit floating point number stored, LSB first, at location DATA. On entry to the routine, register A contains the APU operation code for the function to be performed and HL addresses DATA. Using a direct I/O interface, the function could be performed by

D PUSH	BC,4 *256+APUD BC	
DTIR	50	load APU data
TUC	(APUC),A	send command
DEC	ĤL	
POP	BC	
NDR		unload APU result

Even without using an interpreter, the entire operation—including 32-bit data transfer to and from the APU—requires only 11 bytes of program code. With a memory mapped interface, slightly more code would be required.

APU Software Philosophy

Programmers sometimes go to extremes in making use of a peripheral's intrinsic capabilities without first ensuring that the extra effort will pay off. Although it is rich in internal capabilities, the APU demands careful analysis of proposed applications to be certain of its effective use. APU execution times for arithmetic and derived floating point functions exceed the microprocessor overhead required to transfer data and control the APU by about an order of magnitude. In general, the microprocessor overhead will account for no more than 15% of the time required to perform most floating point operations. Therefore, when developing APU software, it is rarely worthwhile to expend inordinate effort to reduce software overhead by a few microseconds. Also, the earlier program examples show that program size is not a critical factor unless it is absolutely necessary to minimize program storage requirements.

The simplicity of the hardware interfaces and software drivers presented here points out obvious advantages in using an APU. There is a marked reduction in code size, particularly when floating point routines are necessary. In addition, the programmer can focus attention on the problem at hand without spending excessive time on support subroutines. And finally, the APU lends itself to applications requiring an increased throughput in computational speed. For example, the inline MACRO interpreter presented earlier is an ideal case wherein the intrinsic powers of the APU can be realized. Anoher example would be the embedding of the APU software drivers in the run-time package of a compiler. A Pascal

FINTP	POP MOV INX MOV INX MOV INX PUSH LXI ADD MOV MOV	H A, M H M D, M H J, TBL L, A A, H	get return address get op code point to low address move to target DE point to next op code save return address get jump table address add in op code and replace in HL don't forget carry
	ACI MOV LXI PUSH PUSH XCHG RET	O H, A B, FINTP B H	want to re-enter when done so push on stack next "jump" address need target address in HL jump to (top of stack)
FEXIT	POP RET	н	discard address of FINTP pick up main program
JTBL	JMP NOP	FEXIT	exit to calling program
	JMP NOP	FPUSH	push (HL) to FACC
	JMP NOP	FPOP	pop FACC to (HL)
	JMP NOP	FADD	add (HL) to FACC
	JMP NOP	FSUB	subtract (HL) from FACC
	JMP NOP	FMUL	multiply FACC by (HL)
	JMP NOP	FDIV	divide FACC by (HL)
	JMP NOP	FINT	integer function on FACC
	JMP	FBIN	FACC ->_HL, binary'
	JMP NOP	BINFL	HL, binary' ->FACC

Fig 9 Floating point interpreter. Program reads 1-byte operation code followed by 2-byte target address and calls appropriate floating point subroutine. Operation code 0 exits from interpreter back to inline assembly code

compiler, for instance, would greatly benefit from the speed of the APU in performing fixed point (integer) and floating point (real) arithmetic.

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FEATURE

AUTOMATED NETWORK SYNTHESIZER COMPACTS VLSI DESIGN

When a simple transformation converts schematic design input into numeric data, standard processing techniques can bring about economies that other VLSI compaction methods might miss

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arge scale integration has rapidly evolved beyond its former hard-to-achieve density levels. A quantum jump in the number of circuits per die has occurred over the past four or five years. However, there has been no parallel advance in either design philosophy or design automation, even though the much publicized Very High Speed Integrated Circuits program states this as one of its objectives. Meanwhile, a gap exists between large scale system implementation objectives and today's capabilities. Presented here is a step toward closing that gap: an approach to creating very large design data bases that permits them to be easily processed by design automation software.

Large scale integration (LSI) is developing successfully, and it is continually achieving higher levels of integration. Now we are faced with an order of magnitude increase in the significance of "large," so that very large scale integration (VLSI) is imminent. Today, a chip can be manufactured with 20,000 or 30,000 gates, and still be produced with reasonable yields. Our data processing expertise should allow us to handle the increased logic volume, but we are not always coping with the problems of today's quantities of logic. We have to master LSI before we will be ready for VLSI, but we have not entirely succeeded in doing this.

Here is a case in point. A large digital chip can be designed, reduced to accurate masks, and apparently made to handle its assigned task. Yet, large systems must be testable, and combining prime function and test functions—whatever the philosophy—can try the patience of the best engineer. If a design approach that would also show the resulting design almost at once could be developed, this "early look" at results would make experimenting with alternative approaches more feasible.

Problems of LSI Design

LSI engineers may have overlooked a few properties regarding design automation. First of all, the end products of LSI are monolithic chips which cannot be repaired. Therefore, it is not worthwhile to isolate functions as neat and identifiable packages within a chip. Since an LSI function buried inside a chip cannot always be debugged, it might just as well be incorporated with other functions in time and space, leaving room for devices like test structures.

Second, the VLSI chip is a fairly large data processing system whose design may not entirely be compatible with a precast library of macros (specially structured cells). Off the shelf hardware is inadequate for LSI chip design; instead, a library of custom cells is generally necessary. For instance, if programmable logic arrays (PLAs) are to be used, the specific needs of the system should determine the selection and use of these devices.

Finally, since we cannot avoid computer aids in LSI design, and certainly not in VLSI design, decisions made early in the design process can simplify computer aided design (CAD) and computer aided manufacturing (CAM) in such areas as increased pattern regularity and interconnections. Introducing computers and their capabilities into the design phase early, rather than on the verge of final system implementation, can exploit our knowledge of data reduction and streamline early stages of VLSI system design.

However, the above criticisms cannot detract from such successes as the S-1 project at Livermore. The foundation of this success is the repeated use of macros that were prepared before they were implemented in the supercomputer design. Advance preparation for as welldefined an entity as a computer and its components is not difficult; a finite set of macros can do the job.

VLSI digital systems answer problems and seek goals different from those of the supercomputers. Flexible systems that will serve virtually any purpose with relatively little lead time are needed, particularly for military applications. A building block approach necessitates an extremely large library of precast macros, however. Much more flexibility is provided by macros specifically programmed for particular design goals. Eliminating function boundaries provides design flexibility that can crystallize its own structures and substructures (eg, cells and gate arrays). Well-planned design automation systems can accomplish this and open new design dimensions.

Stored Schematics

Fig 1(a) shows in brief how a system design (which is known to implement a sound concept) is put together

for the first time. Its topology consists of interconnections of various elements to accomplish specific functions. Schematic drawings are the first step toward precise definition, and are immediately put into a form of computer accessible storage ("capture"). Hindering this "captured definition" process is the fact that schematics really are pictures. For logic data processing to have any meaning, the system logic—not pictures of it—has to be available for processing. Processing the schematics will produce only information about the pictures.

A stored schematic is not only an assembly of pictures, but also a network of interconnections in



schematic drawings define network interconnections (a), database management system can store, revise, and display schematics. However, pictorial representations are not always easy to analyze, optimize, and evaluate. When data are converted into numeric form (b), standard data handling techniques overcome these shortcomings which cartographic data must be included. Questions about where the symbols are on the page, where the page is in the volume, and how one connecting line differs from the others must be answered. If all such data are not accessible, the pictures cannot be recreated by the plotting facilities. Thus, the stored schematic is actually a sophisticated data base, for which database dictionaries are needed to record and map the various means by which data are addressed.

A good data base needs a database management system (DBMS), under which schematics can be captured, edited, refined interactively, and, if necessary, made into drawings. However, because of the pictorial nature of its data, no DBMS can identify the dozens of identical subfunctions that lie buried in decoders, multiplexers, random gates, and the like. These buried subfunctions, if they could be identified, might be decomposed into simpler functions with combined logics simpler than the original logic, and this could have a compacting effect on final silicon area. Unfortunately, these invaluable data are not available because they are masked out of sight by the pictorial version of the original logic.

Design by Numbers

The iconoclast in the design community might ask why some effort has not been invested in reviewing how the design data are represented, pointing out that some data processors are known as number crunchers. No one has ever accused a machine, not even a machine driven by the best DBMS, of being a picture cruncher. Why are the data not stored and processed in numeric form?

Sources for design data include proposed command structures, system block diagrams with their state tables, segments of earlier designs, sequential requirements, and combinational requirements. Any and all of these data can be converted to numbers and incorporated into a simple, if large, data structure. Fig 1(b) outlines design data that have been put into numbers and thoroughly manipulated ("preprocessed") by data processing methods classified under "synthesizer." This processing produces economized data.

Pictures become necessary again during final system implementation. The difference between a system designed through use of a numerical data base and a system designed with pictorials (schematics) from the start is that standard data processing methods can be applied to numerical design data. Synthesized design data can compact subfunctions by means of patterns that the human eye could never find.

Numerical Data Patterns

Pictures can be transformed into numerical data by automated conversion. Fig 2(a) shows a case in which the function F is defined by a schematic and is realized by five NAND gates. The logic equation in the illustration also expresses this function. A simple transformation is set forth in Fig 2(b); the letters of the righthand side of the equation have been changed into numbers. Four terms of the equation have become four lines of numbers. The lefthand side of the equation, the letter F,



Fig 2 Transformation maps pictures into numerical data. Schematic from design source (a) defines logic network to implement simple logic equation. In (b), four terms of equation become four lines of numbers—raw data for subsequent design stages. Automated conversion from schematic (a) to equivalent multiplexer circuit (c) would be difficult. However, using transformed data of (b), even widely distributed logic subfunctions are easy to identify has been transformed into the number 1. With the aid of mapping, the original logic equation can easily be written so that it (and logic equations in general) can be stored as numbers without loss of generality.

A computer program can be written to expand the numeric structure of Fig 2(b) to its original canonical form. For example, when the second term, 4* 3, is expanded through all its variables, it becomes

4*	3	2*	1*
4*	3	2*	1
4*	3	2	1*
4*	3	2	1

If all the terms in Fig 2(b) are expanded in this way, the total canonical form will have eight terms instead of the four of the original equation. Here is the logic in this canonical form

1	1	4*	3	2*	1*
1	2	4*	3	2*	1
1	3	4*	3	2	1*
1	4	4*	3	2	1
1	5`	4	3*	2	1*
1	6	4	3	2*	1*
1	7	4	3	2*	1
1	8	1	3	2	1

Patterns that are completely hidden in the schematic of Fig 2(b) can be found in these raw data. Fairly simple computer programs can find these patterns. A computer program written to identify those equations in which two or more variables went through all possible combinations would use the preceding canonical form. A multiplexer could be used in place of NAND gates. It is necessary to operate only on the multiplexer inputs to find the solution. When the inputs are traced through the mapping, the schematic in Fig 2(c) is produced. A and B (1 and 2) are the select lines because they go through all possible combinations. Furthermore, this schematic was not produced by a manipulation of the schematic of Fig 2(a), but by the selective processing of the raw logic that it represents. Most of the known LSI packages can be applied directly to the data base in this way.

A single multiplexer and an exclusive OR gate produced the sample logic function of Fig 2(c) from a body of raw data. It would be very difficult to convert the schematic of Fig 2(a) to the schematic of Fig 2(c) by means of picture manipulation alone. No matter how capable the DBMS, this kind of processing cannot be expected of it.

Since the group pattern is invariant regardless of signal mixes or term positions, it can easily be identified by a computer program. Even if the above logic had been distributed among many functions as subfunctions, and many kinds of gating circumstances had been employed in the original schematics, each occurrence of the logic grouping could have been identified within the large mass of raw logic representing the total system function.



Fig 3 Truth table representation. When raw data of Fig 2 are expressed in truth table format, left-most column can be viewed as Boolean function equivalent to original schematic. Then, decomposition of ØF2D pattern identifies potential for compaction. For example, in (b), binary counter variable C is equivalent to pattern ØFØF. Pattern ØØ22 is simply Boolean AND of D, B, and Ā. Therefore, since pattern ØF2D was decomposed via XOR into ØFØF and ØØ22, schematic (c) can realize entire function

Patterns in Boolean Functions

It can be proved that the greater the regularity of pattern in a Boolean function, the simpler, in terms of gate count, is its logic. Consider Fig 3(a). Here, the raw data are set up within the truth table they represent. The single column of binary data, and how it equates to the hexadecimal pattern 0F2D, can be called a Boolean function. This particular Boolean function represents the original raw data, so it also represents the schematics in Figs 2(a) and 2(c). Even though the pattern 0F2D is not particularly regular, it can be decomposed along exclusive OR lines into two Boolean functions that are fairly regular. Sometimes this maneuver produces a pair of functions whose combination is simpler (in terms of gate count) than the original logic. For example,

0		0		0
F	1	F	æ	0
2	-	0	v	2
D		F		2

There is good regularity in the pattern 0F0F (as shown by its Karnaugh map), and, therefore, 0F0F is considered to be a single variable—the variable C under the column heading "Binary Counter" in Fig 3(b). Note that its distribution is, indeed, 0F0F. The pattern 0022 is the AND combination of D, B, and \overline{A} ; again, the Karnaugh map is one easy way to demonstrate this. Since the original function was decomposed along exclusive OR lines, the simplified schematic equivalent is shown in Fig 3(c). Structure in raw data can represent a logic function; from that structure, other structures along different lines can be formed easily. This technique is powerful in developing compact LSI logic designs.

A system can be assembled from any kind of design source. Its pieces need not be optimized; they need only be correct. If the system is reduced to a homogeneous pattern of raw logic, many kinds of relatively simple data processing can produce a truly economized end result. An economized design, however, is also monolithic in that separate functions may not be identified easily. Thus, the system synthesis technique described here must be LSI-oriented, because the LSI chip also is monolithic and cannot easily separate functions. By the nature of its structure, a system designed through optimization of raw numerical data will have many regularities. Its testability factor will be high, and its test patterns will have good coverage.

Accessing different kinds of logic descriptions and automatically producing regular system structures is called automatic network synthesis. It is a viable alternative to designing systems from vast assemblies of pictures that are stored in sophisticated data bases.

Structure of the Network Synthesizer

Not only is there more than one way of storing numeric patterns, there is also more than one kind of hardware

that can be used for a selecting device as the multiplexer above was used. Consider the various design functions mentioned thus far. Their descriptions constitute the specifications for the component parts of a network synthesizer: the function generator, Boolean processor, and "agglomerator." (See Fig 4.) First, the function generator accepts all statements and produces Boolean functions, or numeric functions that are automatically incorporated into the growing data base.



Next, the agglomerator gathers data and provides ways of distributing and labeling them within the numeric structure. The agglomerator library is constantly increasing. Information gathering specifications are conceived and implemented in software, and become part of the agglomerator's processing library. Usually, this is done by making each data processing program responsive to an appropriate command within some operating base. Since the data base is such a simple structure, these programs are generally easy to write.

Finally, the Boolean processor, a software system, accepts Boolean functions and produces reduced or simplified logic expressions from them. Boolean functions may come from either the function generator or some other program that can create Boolean functions. Also in the Boolean processor is software to define a block of logic equations in the agglomerator base and to convert it into Boolean functions. Primitive data in the form of decision tables, where DON'T CARE fields are generated internally, are accepted by the Boolean processor, as are specially designed DON'T CARE functions, which are sometimes used in masking operations to identify function regularities. Output from the Boolean processor is directly convertible to the simple data base of the agglomerator. The Boolean processor works with sequential and/or combinational logics; its output is taken by the agglomerator and incorporated into the system data base.

Implementation of the Network Synthesizer

In an actual application of the automatic network synthesizer to a problem of instruction decoding and microprocessor control, thirty-eight 10-variable functions were to be implemented in a PLA—not a problem to undertake with pencil and paper. One of the 38 functions, equation 28, contained a total of 224 different 10-variable terms. The automated system first processed raw data to explore the existence of common subfunctions, ie, groups of terms duplicated signal-for-signal in more than one equation.

Forty common subfunctions were found, each identifiable as a logic equation. One such equation, which contained 86 terms, appeared as a subfunction four times in this system. When common subfunctions were applied as factors throughout the design, the original 224 terms in equation 28 were reduced to only 36 terms. Since it seemed likely that common subfunctions such as the 86-term equation would themselves contain some redundancies, each of these factors was next converted into a Boolean function and entered into the Boolean function processor. Following this step, the 86-term factor was reduced to only 9 terms, and its signal structure was also simplified.

Once common subfunctions have been identified and applied as factors, it follows that the residue must consist of uniquely occuring terms for which no common grouping exists. However, there is a high probability that individual terms will be duplicated, signal-forsignal, more than once within this residue. The final step scans for duplication of this sort and converts any duplications into single-factor terms. Once this process was applied to the actual design, equation 28 was reduced to 36 terms, each of only a single factor. Following automated network synthesis, each factor was a single term and each signal was ORed in the PLA OR plane. Because the system of factors is the AND plane with instructional groupings of terms set up in the OR plane, the 2-level PLA boundary condition was met. Repeating this process on the factors themselves would introduce multiple-level gating. Including decision tables in the original input would require sequential logic. However, if the total system had been frozen in a set of schematics, these schematics would have been formed into the chip without further consideration beyond the compression obtained through careful design of the cell library. In this case, a silicon area reduction of 30% to 50% might have been missed.

Conclusion

VLSI is now within our range of technology. Unfortunately, today's design automation capabilities often barely seem able to cope with LSI, which is an order of magnitude less complex than VLSI. Efforts to save silicon area have been directed mostly toward clever circuit layout work. As far as it goes, this has been quite successful. However, the same amount of attention is not being paid to configuring the design data base toward saving silicon area.

By storing design data in such a way that simple data processing methods can handle the compression task in short order, designers can capitalize on a system structure's proclivity to coalesce "naturally." The quantum jump in LSI fabrication technology requires parallel development in design automation technology. Only then will designers be able to handle the massive amount of data required for final implementation and take full advantage of the increased circuit densities soon to be available.

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J. Robert Logan is a staff engineer with Hughes Aircraft Company, where he has been involved with research in design automation for large scale integration and configurable gate arrays. His experience includes work with microprocessor systems, information management, logic synthesis, magnetics, and pattern recognition. Mr Logan holds BA and MS degrees in physics from the University of Pennsylvania.

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DESIGN APPROACH TRIMS ONE-SHOT PROPAGATION DELAY

Circuit design techniques reduce multivibrator delay by as much as 90%, achieving a single-gate propagation delay

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Since the 55- or 80-ns propagation delay for triggering from its B or A inputs that may be introduced by a monoshot (74121) is not desirable in most contemporary systems, the need arises to minimize these delays. Following are schemes showing how, by using Schottky gates, they can be cut to a singlegate propagation delay of as little as 5 ns.

In Fig 1, a trigger pulse with a width smaller than the monoshot output is applied at the B input. An early 1-0-1 pulse (the width decided by the monoshot resistor capacitor combination) is obtained by NORing B and Q_M outputs of the monoshot. The \overline{Q} output thus obtained is delayed by an amount equal to the propagation delay of the NOR gate (typical propagation delay equals 8 ns for 7402); the Q output can be obtained by inverting the \overline{Q} output or by ORing B and Q_M of the monoshot. Fig 2 shows the arrangement for a high to low triggering





Fig 1 Output pulse exceeds rising trigger pulse width

pulse with a width smaller than the output pulse width.

For the arrangement of a low to high and high to low triggering pulse that has a width greater than the output pulse width, see Figs 3 and 4, Fig 2 Output pulse exceeds falling trigger pulse width

respectively. It should be noted in these figures that despite the usage of a D flipflop (7474) in the arrangement, there is no more than one gate delay for the output because it is only used to derive the trailing edge



Fig 3 Rising trigger pulse exceeds output pulse width

difference between the input and the output. The same arrangements can be used for a 74123 or a delay line in contemporary applications.

The restriction on the external resistor and capacitor values, the input and output pulse widths, and the duty cycle are governed by the manufacturer's specifications of the monoshot and are not affected by the logic shown in Figs 1 to 4. Minimum and maximum resistor

Fig 4 Falling trigger pulse exceeds output pulse width

and capacitor values and output pulse width values are indicated in Table 1.

The reduction possible in the propagation delay is apparent in Table 2.

Timing Re	TABLE 1 sistor and Capacitor Values	
	Minimum	Maximum
External timing resistor (R) between pins 11 and 14 (V _{CC}) with pin 9		401-0
open	1.4k Ω	40k Ω
Timing capacitor (C) be- tween pins 10 and 11	0	1000 µF
Duty Cycle: R = $2k \Omega$ R = $40k \Omega$		67% 90%
Output pulse width		40 s

TABLE 2

Reduced Propagation Delay

Parameter	741 output	21 t (ns)	With high speed series <u>gate output (ns</u>)	With Schottky <u>gate output (ns</u>)
Propagation delay time to logical 1 level from B input to Q output	Min Typ Max	15 35 55	6.2 10	2 3 4.5
Propagation delay time to 1 level from A_1/A_2 inputs to 0 output	Min Typ Max	25 45 70	6.2 10	2 3 4.5
Propagation delay time to O level from B input to $\overline{\Omega}$ output	Min Typ Max	20 40 65	5.9 10	2 3 5
Propagation delay time to O level from A_1/A_2 inputs to \overline{O} output	Min Typ Max	30 50 80	5.9 10	2 3 5

MICRO DATA STACK

Interfacing Fundamentals: Bidirectional I/O Using Two Semaphores

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Department of Chemical Engineering Virginia Polytechnic Institute and State University Blacksburg, VA 24061

The 8255 programmable peripheral interface chip contains a bidirectional conditional input/output port that is particularly useful for interfacing a pair of microcomputers in a master/slave relationship. Bidirectional conditional input/output can be represented schematically as shown in Fig 1. In this case, the master microcomputer is on the left and the slave microcomputer is on the right. The buffer is a programmable peripheral interface chip that communicates directly with the master using accumulator input/output or memory read/write instructions. Strobe signals utilized by the master are the $\overline{RD X}$ and WR X device select pulses, which input and output data, respectively, and also clear the input and output semaphores.1 The buffer can store only a single byte of data. Thus, it can be viewed as a half-duplex parallel data transmission device: data can be transmitted from master to slave, or slave to master, but not in both directions simultaneously.

The slave microcomputer communicates with the buffer via the $\overline{\text{STB X}}$ and $\overline{\text{ACK X}}$ pulses. The $\overline{\text{STB X}}$ pulse loads slave data into the buffer and simultaneously sets the input semaphore; the $\overline{\text{ACK X}}$ pulse acknowledges the receipt of buffer data by the slave and simultaneously sets the output semaphore. In transferring a block of data from master to slave, only the output semaphore is tested by each microcomputer. After processing in the slave, the data may be sent as a block back to the master, in which case only the input semaphore is tested. Both semaphores are tested by the the two microcomputers if data



Fig 1 Bidirectional conditional I/O using semaphores. Data can be transferred from master to slave, or slave to master, but not in both directions simultaneously

bytes or words are continuously sent to the slave, processed in the slave, and immediately returned to the master.

The 8255 chip is interfaced directly to the address, data, and control buses of the master 8080A microcomputer. (See Fig 2.) This interface is simple: only two 74LS04 inverters and 16 wire interconnections are required. The slave 8080A microcomputer is interfaced to the bidirectional buffer (port A) and also to the preset and semaphore output signals of the IBF_A and \overline{OBF}_A semaphores.² Three 74LS32 OR gates generate the device select pulses, and two 74LS365 3-state buffers input the semaphore signals IBF_A and \overline{OBF}_A into bit positions D₅ and D₇, respectively, of the slave accumulator, where they are tested.

Both microcomputers employ the accumulator input/output (I/O) instructions summarized in the Table. Use of these instructions can best be seen by observing which pulses are needed to transfer a data byte from the master to the slave and back to the master. The master first tests the \overline{OBF}_A semaphore to determine whether or not port A is full. If it is not, an

(continued on page 186)

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Fig 2 Master/slave interface circuit. 8255 is operated in mode 2 configuration. $1 - k\Omega$ pullup resistors are used with \overline{OEF}_A and \overline{IBF}_A . Notations $\overline{O3H}$, $\overline{O4H}$, and $\overline{O5H}$ represent decoded 8-bit address pulses

OUT 80H instruction is executed, and data are transferred from the accumulator in the master to the 8255 buffer. Concurrently, \overline{OBF}_A is set. The slave uses the IN 03H instruction to input the semaphore bits into the accumulator, where they are tested for an output semaphore that is set. If \overline{OBF}_A is set, the slave executes the IN 04H instruction and inputs data to its accumulator.

Input and Output Instructions

Master 8080A Microcomputer

IN 80H	Inputs data from the 8255A port A and resets input semaphore IBF,
IN 82H	Inputs semaphore bits OBF and IBF
OUT 80H	Outputs data to the 8255A port A and resets output semaphore OBF
OUT 83H	Outputs control word to the 8255A control register
Slave 8080A M	icrocomputer
IN 03H	Inputs semaphore bits \overline{OBF}_{A} and IBF_{A}
IN 04H	Inputs data from the $8255A$ port A and sets output semaphore \overline{OBF}_{A}
OUT 05H	Outputs data to the 8255A port A and sets input semaphore IBE

After processing the data byte, the slave tests the IBF_A semaphore to determine that the input buffer is empty. If it is empty, the slave executes an OUT 05H instruction that strobes the data byte into port A and also sets the IBF_A semaphore. Next, the master tests the IBF_A semaphore. If it is set, the master executes an IN 80H instruction to input the data byte into the accumulator. Concurrently, IBF_A is cleared.

A set of master and slave microcomputer programs that transfer a block of 64 successive data bytes from master to slave, process it in the slave, and then transfer the processed bytes back to the master, is shown in Fig 3. The programs are in the form of a pair of flow charts incorporating 8080A assembly language instructions. The block output is given in the top half and block input in the bottom half.

Both programs were started at memory location 0300H. Either the slave or the master could be started first, with the semaphores and test loops (and the DCX H instruction in the slave) handling the necessary time and memory location synchronization. The 64 data bytes were located starting at memory location 0380H, and were transferred as a block to a group of memory locations starting at the same address in the slave. The processing of the block was performed by a subroutine located at 0340H in the slave. Once processed, the 64 bytes were transferred back to their original memory locations in the master. The transfer of a single data byte from master to slave, and then from slave to master, proceeded along the lines of the description given earlier.

Several measurements of execution times were made. With both microcomputers operating at 765 kHz, the master program, in the absence of a slave data processing routine at 0340H, required 15.0 ms, or approximately 117 μ s/byte of data transferred from one computer to the other. If both microcomputers were operated at 2.0 MHz, this data transfer time would decrease to only 44 μ s/byte. A 2.43-s delay, which simulated a data processing routine in the slave, produced a 2.43-s increase in the time required to execute the master program completely.

(continued on page 188)

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Fig 3 Flow charts and assembly language programs. Master microcomputer program is on left, and slave microcomputer program is on right. Both programs start at 0300H

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- 2. P. R. Rony, "Interfacing Fundamentals: The 8255 Semaphores," Computer Design, March 1981, pp 150-152

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An iAPX 86/10, based on the 8086-2 microprocessor, serves as the central processor. Its architecture includes four 16-bit byte addressable data registers, two 16-bit memory base pointer registers, and two 16-bit index registers, all accessed by 24 operand addressing modes to offer support for high level and assembly languages. For numeric processing, the optional iSBC 337 Multimodule numeric data processor extends the architecture and instruction set with 60 numeric instructions, and improves computational performance 10 to 100 times over conventional floating point math devices or software.

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On the board are 8k bytes of RAM and capacity for 32k bytes of EPROM. Both RAM and EPROM capacities can be doubled directly on the board using Multimodule boards that provide 8k bytes of RAM and capacity for 32k bytes of EPROM, respectively. Other standard onboard features are two programmable interval timers, 24 parallel 1/0 lines, serial 1/0 ports with programmable baud rates, and nine levels of vectored interrupt control.

Implemented using the 8255A programmable peripheral interface, the 24 programmable parallel I/O lines can be configured in combinations of unidirectional I/O and bidirectional ports. Sockets are provided for interchangeable I/O line drivers and terminators, allowing selection of those devices having required characteristics.

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Nine levels of vectored interrupt control, expandable to 65 levels, ensure system integrity. The highest level interrupt is tied to the CPU; the other eight are controlled by a programmable interrupt controller (PIC). Four priority processing routines can be selected; operating mode and priority assignments can also be dynamically reconfigured through system software. The PIC accepts interrupt requests from 23 sources, including all onboard 1/0 resources, the system bus, and the Multibus.

Three independent, fully programmable, 16-bit interval timers/event counters can operate in either BCD or binary modes. Two of them generate accurate time intervals under software control; the third provides the programmable baud rate for the serial port.

The microcomputer is software compatible with the iSBC 86/12A, giving existing users a new implementation option. Two realtime multitasking operating systems support the board: the iRMX 86 operating system and the iRMX 88 executive. For high performance, realtime applications, the compact iRMX 88 executive provides a software control layer for the 16-bit CPU that supports intertask communication, asynchronous 1/0 control, priority based resource allocation, and standard iSBC disc controller interfaces. Complementing the full featured iRMX 86 operating system. the executive can be totally EPROM resident or may be bootstrap loaded from a mass storage device into RAM, depending on application requirements. Circle 456 on Inquiry Card

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A high speed memory subsystem, an 8048 family emulation support package, and a peripheral access software system increase the versatility of the ECL-3211 microprocessor development system. The basic ECL-3211 system from Emulogic Inc, 362 University Ave, Westwood, MA 02090 (see *Computer Design*, Sept 1980, pp 166, 168), provides realtime emulation of 4- to 32-bit microprocessors.

Three quad-size board configurations of the high speed memory subsystem for the universal emulator system are available: 32k bytes of 45- or 70-ns access time RAM, and 64k bytes of 150-ns access time RAM. These boards permit the user to expand system emulation/simulation memory to more than 16M bytes.

Each memory module can be accessed from the LSI-11 bus and the ECL-3211 emulation bus, and through the memory control register/command stack. Since any word or byte within the module is modifiable through the memory control register, this access mode is used for



functions such as programming the virtual address for data from the emulation bus, setting priority for bus arbitration, and enabling/disabling a specific



memory module for memory management and similar tasks.

The ESP-8048 emulation support package provides complete facilities for assembly language software development and realtime incircuit emulation of any 8048 family chip. Included in this hardware/software package are the ASM-8048 macro-relocatable assembler, CD-8048 chip driver module, ECL.LINK general purpose linker, OBJ.FORM object code format converter, and the EP-8048 pod with cables for connection to the development system and to the user's target system. Each module carries its own identification and software interface, ensuring upward compatibility with future models of the development system. Software is supplied on an RX01 diskette.

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Included in the system are a programmable realtime clock, 4k-word main memory capacity, and all the necessary logic to expand the memory system to a full 32k 12-bit words. A separate 1k-word control panel memory holds user monitor and debug routines without occupying main memory space. Also provided are one optically isolated serial port capable of both 20-mA current loop and RS-232 interface levels; two 12-bit parallel input ports with handshake lines; one 12-bit parallel output port with handshake lines; a vectored, prioritized interrupt structure; and all required bus driving and interface logic for system expansion.

Two full 4k-word fields of RAM are provided by the 1202 8k-byte CMOS RAM memory module. The 1204 memory/ serial interface module provides 4k words of CMOS EPROM/RAM configured in any combination of type 6653 CMOS EPROMs and 6513 or 6514 RAMs in 1k-word increments. Its four serial RS-232 ports operate at data rates from 75 to 19,200 baud. Each port can be optically isolated from the external peripheral device to which it is connected. The 1206 memory and serial/parallel interface contains a single 4k-word memory field and two serial ports that are identical to those of the 1204, plus one 12-bit parallel input and one 12-bit parallel output port.

Two 12-bit parallel input ports and one 12-bit parallel output port are also supplied by the 1207 parallel 1/0 module. Each input port is optically isolated through low power isolators on all 12 input lines; the output port is isolated through opto-couplers with high driving capability.

The 1214 stack module contains a 256-word hardware push-pop stack, an absolute time clock/calendar function, two RS-232 serial ports, and a 4k-word field of EPROM/RAM memory. Primarily intended for subroutines and interrupt return-address storage for programs running in ROM, the stack can be enabled and disabled under program control.

The 1208 mass storage interface includes a DEC compatible RX01/RX02 floppy disc interface and a DEC compatible terminal interface in addition to hardware trap logic. The 1210 magnetic bubble mass storage module emulates the DEC RX01 floppy disc controller and interface and offers a storage capacity of 46k bytes, unformatted.

Sixteen single-ended or eight differential analog input channels, as well as one digital 12-bit parallel input port and one 12-bit parallel output port, are provided by the 1203 ADC module. A-D conversion time is 350 μ s maximum.

A set of EPROM and RAM chips that plug into the CPU module control panel memory sockets, the ZOOM monitor occupies no main memory space and provides a full complement of monitor and debugging functions. Typical functions include memory examine/modify, masked word search, multiple break point/proceed, memory dump, BIN format loader, and single step/trace. Circle 458 on Inquiry Card

Modules Interface CPU To Instruments Having IEEE-488 GPIB

Designated TM990/314, this single-board module interfaces a TM990 CPU to a general purpose interface bus (GPIB) and maintains IEEE Standard 488-1978 protocol. Offered by Texas Instruments Inc, PO Box 225012, Dallas, TX 75265, it allows any system having an IEEE 488 GPIB interface capability to be connected to a variety of digitally controlled instruments.

In accordance with IEEE Standard 488-1978, the module allows up to 15 instruments to communicate with each other over a common bus using the CPU as a listener, talker, controller, or system controller. It provides standard 488 functions such as device clear, trigger functions, service request, parallel/serial polling, remote/local (with local lockout), single/dual addressing modes, and secondary addressing. Direct memory access allows the module to attain control of the system and permit DMA transfers from the GPIB directly to and from memory, providing a higher data transfer speed. In the selfdiagnostic mode, two 8-bit I/O ports are used to apply inputs to the GPIB port to test and verify board operation.

The module's data rate is 200k bytes/s maximum in the receive mode, and 180k bytes/s maximum in the send mode. It measures 11 x 7.5 x 0.062'' (28 x 19.0 x 0.157 cm) and will fit TM990/510/520/530 card cages. Typical power requirement is 5 V ± 3% at 1 A.

Demonstration software for verifying the correct board operation is provided on two TMS2716 EPROM devices that plug into the EPROM memory areas on the TM990/10X microcomputer board or the TM990/210 memory board. The software is executed under the TIBUG monitor and uses I/O utilities provided by the monitor.

Circle 459 on Inquiry Card

Disc Based Microcomputer System Supports up to 255 Users

Accommodating up to 255 users, CompuStar is a multiuser, shared disc, microcomputer system. The system, from Intertec Data Systems, 2300 Broad River Rd, Columbia, SC 29210, is based on the company's SuperBrain video computer, and consists of a network of video display terminals, or video processing units (VPUS), that employ their own internal microprocessor and dynamic RAM.

The terminals are tied together in a network that shares the resources of a single Winchester or other hard disc device. This networking allows the sharing of a common data base while at the same time permitting individual users to maintain restricted data bases.

(continued on page 198)

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Gandalf Data, Inc., 1019 S. Noel Avenue, Wheeling, Illinois 60090 Tel: (312) 541-6060 Gandalf Data Communications Ltd., Gandalf Plaza, 9 Slack Road, Ottawa, Ontario, Canada K2G 0B7 Tel: (613) 225-0565 Gandalf Digital Communications Ltd., 4 Cranford Court, Hardwick Grange, Warrington, Cheshire, England Tel: 09-0276-28527 CIRCLE 105 ON INQUIRY CARD

System architecture is based on one of three disc storage systems: a tabletop 10M-byte Winchester drive that uses the Shugart 8" (20-cm) Winchester drive mechanism and a 32M- or 96M-byte Control Data Corp cartridge module drive with a 16M-byte removable, top loading platter and either 16M or 80M bytes of fixed disc storage. Four types of VPUs can be connected to the disc system via an 8-bit parallel interface. Model 10 is an intelligent video terminal with internal microprocessor and 64k bytes of RAM; programs can be downloaded from a host system or the disc storage system. Model 20 contains the same features but adds two doubledensity 5.25" (13.33-cm) floppy disc

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drives. Model 30 is the equivalent of model 20, with the addition of doublesided 5.25" (13.33-cm) floppy disc drives. Model 40 adds double-sided, double-density, double-track drives to model 30 features. All are full-featured terminals with a 12" (30-cm) diagonal non-glare screen, 24-line x 80-char display, and 8- x 10-char matrix. They feature visual attributes, fully addressable cursor by either discrete or absolute addressing, 18-key numeric pad, four individual cursor control keys, multikey rollover, and a 128-char upperand lowercase ASCII keyboard. Up to 255 VPUs, each of which has two RS-232 serial ports for connecting auxiliary printer and/or modem devices, can be connected in a daisy chain fashion in a single network

For remote or printer workstation requirements, the model 15 universal processing unit (UPU) features model 10 circuitry without the keyboard and CRT. This unit provides an RS-232 serial port plus a Centronics compatible parallel port, allowing character and line printers to be connected to the network. In combination with a modem, it permits remote terminal stations to be included as well.

Circle 460 on Inquiry Card

Interface Allows Processing of Real World Variables

APMOD allows Apple microcomputers to process analog variables such as temperature, light level, pressure, and voltage, and to control lamps, motors, pumps, and heaters. A product of Connecticut microComputer, Inc, 34 Del Mar Dr, Brookfield, CT 06804, the interface generates a bus from the computer and contains an 8-bit latch plus an 8-bit 3-state buffer, as well as necessary decoding logic.

A POKE statement to the interface causes eight bits to be latched by the interface on the address and control lines of the AIM16 16-channel ADC; each of the 16 inputs is converted into an 8-bit digital signal that can be read by the computer. The interface plugs into one of the I/O slots of the computer, providing the necessary port. The complete APSET1 system includes the interface, ADC, connecting cable, POW1 power supply, and MANMOD1 for connecting analog inputs to the converter. Circle 461 on Inquiry Card



The new MX-80F/T. You can feed it anything. Almost.

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This is Epson's newest and most versatile printer — the MX-80 F/T. It does everything the famous MX-80 does, and since it accepts both friction and tractor-feed paper, it prints on almost anything. So for many OEM uses, this printer may be the best printer you can buy.

It prints bidirectionally in your choice of 40, 80, 66, or 132 columns. And to make the throughput even faster than its 80 CPS, a logical-seeking function minimizes print head travel time.

It prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. And since all Epson printers are known for reliability and the MX-80 F/T is no exception—it prints and prints and prints. You can expect 100,000,000 characters from the print head. And when the head finally wears out, it's so inexpensive you can just throw it away. To put in the new one takes only one hand and a few seconds of time. The MX-80 F/T is compact, weighs only 15 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor.

But here's the best part. The MX-80 F/T prints on just about anything you feed it. It has both a friction and a tractor-type pin-feed mechanism. So it prints on forms, labels, letterheads, roll or continuous fan-fold computer paper. Or even paper plates.

You can have the MX-80 F/T for under \$750, and for even less in quantity. And for a printer that isn't finicky about what's for lunch, we call that chicken feed.



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Emulator Packages Ease Task of 8085 Software **Development/Debugging**



SPM-A13 integral insystem emulator (ISE) and SPM-A13-3 8085 emulator package provide designers with an efficient means of developing and debugging software for 8085 microprocessors. Intended for use with the STARPLEX development system, the packages are available from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051.

Composed of a target card dedicated to a particular microprocessor, a cable pod, and complete software, the

emulator interfaces between the integral ISE, the development system, and the 8085 based system under development. It plugs directly into the development system, offering the user realtime emulation of the 8085A and 8085A-2 microprocessors.

Operating in either single-card or standalone chassis mode, the integral ISE is composed of one bus connector, an 8-bit user status cable, and two logic boards. These two boards provide the user with 32k bytes (expandable to 64k bytes) of dedicated mapped memory, all the necessary logic for a 256 x 40-bit trace memory, and two bitprogrammable, 40-bit breakpoint registers. They interface with the target card through a specialized, high speed emulation bus connector and only the target card interfaces with the development system bus; therefore, when upgrading to future microprocessors, user investment is limited to the purchase of target cards. The integral ISE also features symbolic debugging, automatic testing, and inline assembly and disassembly.

 μ Computer Operates as **Slave Processor for Data Processing Networks**

Net/80 single-board microcomputer, a product of Musys Corp, 1451 E Irvine Blvd, Suite 11, Tustin, CA 92680, performs as a Z80 slave processor loosely coupled to an S-100 bus. Each slave operates independently of any other, except for resource queuing in the master; therefore, the entire system appears to be dedicated to each user, unless a large amount of shared resources is being accessed.

The board includes 64k bytes of RAM, a single-level interrupt, a console serial port, and a parallel port for communciation with the S-100 bus master CPU. Each slave is completely controlled by the master processor; the master can reset or interrupt a slave at any time. Transfer protocol is performed with Z80 block 1/0 instructions at near DMA speeds while retaining protection and validation capability for the master. A bootstrap P/ROM

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supplied with each slave uses this transfer technique to download the system software into RAM; the P/ROM is then switched out of the address space so that the 64k bytes are entirely available as RAM.

The slave processor system totally isolates the master CPU from errors in the slave and permits the customization of each serial port for various applications. An expansion bus on each slave allows users with unusual 1/0 requirements to access additional peripherals.

Most CP/M software is compatible with the system. CP/NET and its MP/M operating system are offered for the network master by Digital Research, and Action Computer Enterprises offers the DPCOS operating system that runs under CP/M for the master.

Circle 462 on Inquiry Card

STD BUS Compatible RAM/EPROM Boards Support Megabyte Addressing

DM-6420, a 64k-byte dynamic RAM card, and DM-6421, a 16k-, 32k-, or 64k-byte EPROM card support 1M-byte addressing of the company's DM-8800 CPU or can be jumpered for 64k-byte systems. Available from Desert Microsystems, Inc, Star Rte 1, Pasco, WA 99301, the boards operate with all STD BUS compatible processors.

The dynamic RAM's onboard RAM controller does not depend on offboard signals to command refresh, allowing the board to act like a static RAM. The card is available with either 5-V only, or 5-, -12-, and 12-V RAMS. The EPROM board can be used with 2716, 2732, and 2764 EPROMS. It can identify which sockets are populated with EPROMs and, in conjunction with the memory enable control signal, overlay RAM memory space when accesses are to the card.

Megabyte addressing is an expansion of the original STD-BUS standard, achieved by multiplexing the high order four address bits onto the data bus during the first part of the memory cycle. The boards latch these bits and decode them when the memory control signals are generated by the processor. Four jumpers select the memory segment, and a fifth disables high order decoding for 64k-byte systems. Both boards generate the wait request control signal that ensures that the data are correctly transferred regardless of processor speed. Circle 463 on Inquiry Card

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CIRCLE 109 ON INQUIRY CARD



Interface Card Converts Apple Computer to IEEE-488 Bus Controller

Any product supported by the IEEE-488 bus can be controlled by Apple II and Apple II Plus computers using the A488 interface card that permits the computers to act as IEEE-488 bus controllers. It plugs into any expansion slot in the computer chassis, and allows bus and system control with simple instrument string commands. SSM Microcomputer Products, Inc, 2190 Paragon Dr, San Jose, CA 95131, has used Motorola's 68488 LSI 488 controller circuit in the card, decreasing the number of IC packages required and software overhead.

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35 Brentwood Avenue • P.O. Box 781 • Fairfield, Connecticut 06430 (203) 384-1344 • Telex: 96-4348 Only Applesoft BASIC software is needed with the card which carries 2k bytes of firmware in EPROM; for special purpose firmware development, the EPROM can be replaced by a RAM. The driver firmware is linked to the string routines within Applesoft, allowing fast programming and the use of floating point processing of numeric data. Error checking within the firmware flags errors with English language statements for fast program debugging.

Up to 15 pieces of equipment can be connected to the card across a transmission distance of up to 20 m from the computer. The card is supplied with a 6 ' (183-cm) IEEE-488 bus cable with male and female connectors. Circle 464 on Inquiry Card

STD BUS Memory Card Allows Mixture of RAM And EPROM Devices

Providing a memory support capability of up to 32k bytes, the ST4202 STD BUS EPROM/RAM memory card meets the varied needs of STD BUS systems requiring EPROM, RAM or a mixture of both. Applied Micro Technology, PO Box 3042, Tucson, AZ 85702, supplies the card to support five types of 5-V IC memory devices: Intel/TI's 2508 and 2516 (2716) EPROM, Intel's 2732 EPROM, TI's 4016 RAM, and Mostek's 4801 RAM, all of which must be of common organizational type, such as all 1k x 8, 2k x 8, or 4k x 8.

With the card, system memory can be mapped in the smallest logical increments, depending upon the degree to which the card is populated, relieving the need to allocate entire 8k or 16k blocks to EPROM/RAM that uses only a portion of that block. Selectable memory addressing allows the card to be jumpered to occupy any logical memory address boundary.

In addition, the card offers selectable memory expansion enable. User selectable configuration areas allow the card to be enabled upon either the occurrence of a low active or a high active MEMEX signal. This feature essentially doubles the card's capacity, allowing implementation of two banks of memory.

The card measures $4.5 \ge 6.5''$ (11.4 x 16.5 cm), plugs into any STD BUS microprocessor system, and will operate at any speed up to and including 4 MHz. Voltage requirement is 5 Vdc, and operating temperature range is 0 to 55 °C.

Circle 465 on Inquiry Card

Chief Engineer

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Westlake Village, California 91362, (213) 889-9340

Smoke Signal Broadcasting, 31336 Via Colinas,

CIRCLE 112 ON INQUIRY CARD

Serial 1/0 Interface Supports Completely Interactive System

QLV11, a quad serial 1/0 interface for DEC LSI-11 based equipment, offers full DEC DLV11-E compatibility on any of the four RS-232 ports and uses one quad height QBUS module slot. Produced by General Robotics Corp, 57 N Main St, Hartford, WI 53027, the interface supports a completely interactive system; multiple terminals can be used simultaneously for input, processing of data, and retrieval of information.

Standard features include autoanswer support to Bell 103, 113, 202C, 202D,



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TEAC Corporation of America Industrial Products Division 7733 Telegraph Road, Montebello, CA 90640 (213) 726-8417 and 212 modems. All ports can also be individually selected to be synchronous serial 1/0 ports. Baud rates of 50 to 19,200 baud are individually switch selectable for each port. UART parameters can also be switch selected for each individual port.

Port 0 has independent switch selectable address and vector. Ports 2 and 3 are contiguously addressed from the switch selectable address and vector for port 1. All ports have RS-422 and RS-423 compatibility for 3-wire interfaces. Circle 466 on Inquiry Card

Multibus P/ROM Board Stores 2k to 128k Bytes

2k to 128k bytes of P/ROM can be connected to a Multibus system with this strap selectable P/ROM board from Central Data Corp, 713 Edgebrook Dr, Champaign, IL 61820. 8k- to 64k-byte P/ROMs, added to the board in multiples of two, allow the board to work with no changes in any 8- or 16-bit system. The board decodes the full 24-bit address bus, allowing a system wide address space of 16M bytes, and operates in read only mode for either 8 or 16 bits. Circle 467 on Inguiry Card

DAC Provides 64 Output Channels

Model SB-64 DAC converter board provides 64 output channels, each of which performs as a discrete DAC with digital input latches and an output amplifier. Digital Multi-Media Control, 2338 Patterson #12, Eugene, OR 97405, attained this density on the board by invisibly multiplexing a single 8-bit converter.

Each of the 64 outputs drives a 1-k Ω load, and has $\pm 0.4\%$ absolute accuracy from 0 to 10.625 V. Address decoding allows memory mapped 1/0 to any 256-byte sector. The converter is compatible with all s-100 bus microcomputer systems, and meets all IEEE specifications for S-100 bus interface devices. Available options include 10 digital outputs, fast 12-bit DAC with 3- μ s settling, \pm 15-V tracking regulator with 600-mA output, and 24-bit address decoding. Circle 468 on Inquiry Card

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CIRCLE 115 ON INQUIRY CARD

SOFTWARE

Languages and Utilities Extend Versatility of Heath Microcomputers

Additional programming languages and utility programs are being offered by Heath Co, Benton Harbor, MI 49022, for their H-8 and H-89 All-In-One computers. Included are a BASIC language interpreter, BASIC compiler, COBOL programming system, FORTRAN programming system, and three utilities.

Previously available for the Heath disc operating system (HDOS) only, Microsoft BASIC interpreter version 5.1 runs with Heath CP/M. Microsoft BASIC language compiler runs under the CP/M operating system, eliminating timeconsuming interpretation when running a program. It compiles each line of the program into machine code that runs faster and occupies less memory space.

Version 4.0 of the Microsoft COBOL programming system for use with CP/M exceeds the minimum specifications of ANSI-74 COBOL. It provides a variety of Level-II COBOL features, as well as optional modules that allow the use of COBOL programs for large computer systems. Features include debugging facilities extended from ANSI-74, and advanced screen handling that allows easy forms handling on CRT terminals with cursor control.

The Microsoft FORTRAN programming system also is being offered for CP/M as well as HDOS. This updated version is provided in either 5.25'' (13.33-cm) or 8" (20-cm) formats. The HDOS version is available on 5.25'' (13.33-cm) diskettes only.

Designed to work with CP/M, the DESPOOL spooler utility allows the computer to print one program through a line printer while the user works on another program. An advanced version of the CP/M DDT debugging utility combines the 8080 compatible SID debugging utility and the Z80 compatible ZSID debugging program into one package. Digital Research's MAC macro assembler is compatible with ASM assembly languages and can generate a SID compatible symbol table for use in debugging.

Except where noted, all releases are available in either 5.25" (13.33-cm) or 8" (20-cm) formats. In addition, the SOFTSTUFF line of languages, utilities, and applications programs for home and business is now available. All of this new software line will also operate on Zenith Data Systems' Z-89 computer. Circle 469 on Inquiry Card

ISO Standard Pascal Compiler Has Complete Support Subsystem

An ISO implementation of Pascal with microprocessor system engineering adaptations, Pascal compiler from Cogitronics Corp, 5470 NW Innisbrook Pl, Portland, OR 97229, allows modular compilation, dynamic memory allocation and deallocation, external procedures, and numeric operations in IEEE K-C-S standard single precision floating point representation. Statements are compiled directly into the source assembly language of the target processor.

The Pascal runtime support system contained in the package is composed of modular segments that can be selected to meet specific performance requirements. Only those modules actually required in the end product are used. These segments provide runtime stack definition, data manipulation, real number manipulation, error handling routines, and either standard or custom 1/0 procedures.

Pascal procedure modules can be designed by the user via block-structured programming techniques developed individually and compiled separately into source assembly language. From there, they can be assembled, debugged, and integrated into the system under development. Since the compiler produces source assembly language, the user has access to all of the development system tools provided by the host microprocessor development system.

All of the data and control structures of ISO Pascal are provided by the compiler. Extensions include the separately compilable modules; modular Pascal support routines; dynamically mapped variables; and custom I/O; plus embedded assembly language; interactive I/O; and binary, octal, and hexadecimal integer constants.

The compiler has two modes of operation: error scan and full compilation. The error scan mode processes the source code to detect syntax errors; the full compilation mode produces both source assembly language and listing outputs. It is currently available on the GenRad 2300, Tektronix 8002A, and Tektronix 8550 development systems, and produces the source assembly language of 8080/8085 and 280 processors. Circle 470 on Inquiry Card

Cross Assembler Program Transforms Computers Into Development Systems

This cross assembler software package generates programs for Intel 8048, 8049, 8041, 8021, and 8035 microprocessors on various computers. Combined with a Micro System Emulator, the package from Millenium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014, transforms the computer into a complete development system. Used with FASTPROBE guided probe software, it will generate diagnostic programs for production test and field service of 8048 based systems.

A MACRO assembler for generating absolute object code; a formatter that arranges the object program into a form that can be transmitted to the emulator, analyzer, or designer for execution; and a downloader that actually transmits the formatted program make up the package.

Written in ANSI standard FORTRAN IV for maintainability and ease of modification and installation, source code is provided on floppy disc or magnetic tape for compilation on the user's host system.

Minicomputers specifically supported by the cross assembler include DEC's PDP-11 and LSI-11 with either RT-11 or RSC-11 operating system, Data General's NOVA 1200 OF ECLIPSE with either RDOS OF AOS, HP 1000 OF 3000, and TI 99/10. The assembler can be installed on any host computer that includes a FORTRAN IV compiler, supports a disc or magnetic tape facility and a data word length of at least 16 bits, and provides at least 20k words of user available RAM. Circle 471 on Inquiry Card



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- 60

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DATA STACK

SOFTWARE

Operating System Offers Printing Efficiency, Backup, And Keyed File Access

OASIS version 5.5 operating system for Z80 microcomputers provides a shared printer, media-independent backup capabilities, and fast keyed file access. Developed by Phase One Systems, Inc, 7700 Edgewater Dr, Suite 830, Oakland, CA 94621, this version offers comprehensive program development support that includes high level BASIC with re-entrant runtime module, compiler, and interpreter; EXEC interactive job control language; text editors; relocating macro assembler; debugger; linkage editor; and diagnostic/conversion programs.

Maximum printing efficiency is achieved by the system's multiuser SPOOLEr, with up to 15 users accessing a single printer. Twenty-six user defined queues prioritize waiting jobs or execute special forms such as checks or invoices. Automatic reprints, multiple copies, and special alignment parameters can be specified.

Hard disc data on tape cartridge or multiple floppies are protected by the archive and restore backup utility. The utility can compress data to save storage space and provide readback check. Flexible options such as saving only data that has been changed or added since the last archive operation are also provided.

Keyed file capabilities, designed for files that are often updated but rarely accessed sequentially, complement the system's direct, sequential and ISAM files. Under keyed access, files are retrieved faster than under other methods, using less disc overhead in the process.

Other system features include flexibility in maintaining public, private, or shared files with security and accounting controls, and convenient interuser communications. File and automatic record locking ensure data integrity. Circle 472 on Inquiry Card

Software Development Package Uses Zilog Instruction Syntax

ZAS Z-8000 is a relocatable assembly language software development package that supports both the segmented Z-8001 chip and the nonsegmented addressing of the Z-8002, and uses standard Zilog instruction syntax. In the package, Western Wares, PO Box 48, Placerville, CO 81430, has included 26 directives that provide features such as "include files" and nested conditional assembly.

Programs are structured into named program, data, and absolute sections that can be combined and renamed with the ZLK task builder included in the package. The task builder accepts commands from the console or a command file, converting any or all program sections into absolute form. Task builder output consists of a section map file and an object file that can be used as task builder input in a subsequent operation.

Absolute object files are processed by the ZLD object loader. It creates a file that can be loaded and executed by the host operating system, assuming a Z-8000 CPU is present on the bus as an alternate bus master.

Designed for Z-8000 software developers and OEMs currently developing Z-8000 products, the package runs on 8080, 8085, or Z80 based microcomputer systems using either the CP/M or ISIS-II+ operating system. Including task builder and object loader, it is available on 8" (20-cm) single-density floppy disc, and requires at least 40k bytes of RAM with 48k bytes or more recommended for large applications.

Circle 473 on Inquiry Card

Pascal Language Package Supports Sequential and Random Data Files

AlphaPascal release 2.0, developed by Alpha Micro, 17881 Sky Park North, Irvine, CA 92713, for use on its business computer, supports both sequential and random data files when it is fully integrated into the company's multiuser, multitasking, timesharing operating system (AMOS). Compatible with AlphaBASIC, the programming language can separately compile and link Pascal modules to form one program, easing the task of developing and maintaining programs. Programs written in standard Pascal will require little modification to operate under AlphaPascal.

Among the language's features are the ability to add user defined routines to an external library and to call external assembly language subroutines, full 11-digit accuracy for real variables, and labeling of begin-end blocks. Full software support for this version is provided.

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AROUND THE IC LOOP

Programmable Array Logic Leads to Flexible Application of 8-Bit Wide Memories

Bernard Brafman

Monolithic Memories Incorporated 1165 E Arques Ave, Sunnyvale, CA 94086

The flexible application of memory devices in small microprocessor based systems has been enhanced by the introduction of 8-bit wide static random access memories. These devices have pinouts and operating characteristics that are similar to those of read only and programmable read only memories. Thus, the configuration of both read/write and read only memories can be simplified to meet changing system requirements. For example, this flexibility allows a single printed circuit board to be used in several different product configurations, from fixed program intensive (large read only memory requirements) to data intensive (large read/write memory requirements). Using programmable logic technology in conjunction with 8-bit wide memory devices adds even more flexibility and helps to reduce parts count.

To provide for the simple substitution of parts, a printed circuit (PC) board must be developed that allows interchangeability among the memory sockets of 8k-, 16k-, and 64k-memory devices, both random access memory (RAM) and programmable read only memory (P/ROM), or read only memory (ROM). A method must be created also to define flexibly the addressing of these parts to accommodate varying address space requirements. The first task is physicaleg, some 64k devices have 28 pins while others have 24 pins. To be most flexible, the PC board will have a 28-pin socket with jumpers to allow the use of either 24- or 28-pin devices. Socket interchangeability also necessitates an examination of the timing requirements of the target memory devices and microprocessor, since differences exist in setup or precharge, hold times for address and data, and control signal interactions. Some systems will need additional gating or delays to ensure flexibility. Such timing information is easily found in application notes published by both microprocessor and memory manufacturers.

The second task is to implement decoding schemes for the selection of the appropriate devices in the memory array. One method uses hardwired discrete logic. This alternative is not viable because high configurability requires an excessive use of space jumpers and also results in unused logic on the PC board. Programmable logic, on the other hand, implements the requisite configurability in fuses in silicon, not on the PC board, and consolidates several integrated circuit (IC) packages into one.

Design Tradeoffs

The choices in programmable logic are programmable logic arrays (PLAS), P/ROMS, and programmable array logic (PAL^R). PLAS must be ruled out since their 2-fuse array structure, while awarding some versatility, uses up too much board space. PLAs are implemented in 0.6" (1.5-cm), 28-pin packages; the job can be done with smaller 0.3" (0.8-cm), 16- or 20-pin packages when P/ROMs or PALs are used.

While P/ROMs are frequently employed in such applications, there are compelling reasons to consider the use of PAL. First, any P/ROM with an adequate number of input and output pins to replace the required external logic consumes more power than a comparable PAL. For example, providing control signals for four memory devices requires four chip enables and at least one output enable signal. These signals must be derived from at least six address lines and generally three and often four control signals. In such a case, the programmable logic device must have ten inputs and eight outputs. For a P/ROM, this would be an 8k, 24-pin device, organized as 1k x 8. Typically, a commercial 8k bipolar P/ROM has an I_{CC} of 190 mA over temperature, as compared with 90 mA for a 10-input, 8-output PAL. Even if external logic were employed, so that a 1k P/ROM, organized as 256 x 4 were used, the I_{CC} would be typically 130 mA over temperature.

PALs are not susceptible to the "glitching" characteristics of P/ROMs during the access time from address. To combat glitching, the P/ROM must be used with registers or, if the control signals are active low only, open collector with pullup resistors for the outputs. Generally, a processor control signal or its derivative serves as the clock for the register or output enable to the P/ROM, an example of increasing parts count and costs in an attempt to overcome an implementation detail. While the technique usually employed to generate the fuse pattern, or programming, for P/ROMs is manual, a useful and uniform design tool exists for configuring PALS. A FORTRAN IV program called PALASM (for PAL assembler) is available on the National CSS timeshare network or (continued on page 214)



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IC LOOP

as source code at no charge for any machine that supports a FORTRAN environment. PALASM converts logic equations describing the function of the target device directly into a fuse pattern format that is compatible with the several P/ROM programmers which support PAL programming. This assembler allows simple, rapid, and complete design and documentation of PAL configurations in a format useful for communication among engineers. Finally, like P/ROMs, PALs have a masked counterpart, hard array logic (HAL). HALs are plug compatible with the corresponding PAL, and offer significant cost reductions for high volume applications.

Implementation Example

A typical design with memory device interchangeability, the 6802 is a microprocessor based instrument required to have four sockets capable of accepting 2k x 8 static RAMs, 2k x 8 erasable programmable read only memories (EPROMs), or 4k x 8 EPROMs. The four chip enable signals (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3 , and \overline{CE}_4), the common output enable (OE), and the common read/write control (R/W) are compatible with the devices selected so that no special gating is needed. The programmable logic device will have as inputs the five high order address bits A₁₁ through A₁₅ and the control signals VMA (valid memory address) and E (enable). While R/W may be used directly for write enable (WE), it is needed to generate \overline{OE} . (See Fig 1.)

The programmable logic device requires eight inputs and five outputs. PAL10L8 and PAL12L6 meet



Fig 1 6802 based system. Block diagram outlines system's capability to accept 2k x 8 static RAMs, 2k x 8 EPROMs, or 4k x 8 EPROMs

both the input and output pin requirements.* The PAL10L8 has been selected for this discussion because the three outputs are left unused and are available for

*Bipolar LSI Data Book, 2nd ed, Monolithic Memories Inc, 1980

logic replacement. (See Fig 2.) Internally, the PAL10L8 generates eight 2-term OR sums, each sum composed of two 10-term AND products. Each of the products may be connected to any of the input signals or its complement.

While there are 81 unique combinations of the three memory devices in the four sockets, there are



Fig 2 PAL10L8 pinout. Device generates eight 2-term OR sums, each composed of two 10-term AND products

only 16 distinct decoding schemes implementing either a 2k- or 4k-deep device in any of the four sockets; these 16 schemes are set forth in "Address Ranges of 16 Device Combinations." See "PAL Design Specifications," which can also include a function or truth table, for a description of the arbitrary pinout shown in Fig 2; this pinout may be altered simply by switching the elements of the pin list on line 5 in both design specifications. Notice that the chip enables and output enable are inverted in the pin list and true in the equations. This is to keep expressions in the sum-of-products form for PALASM, which expects equations summed at the node before the inversion for active low PALS. Also, there are two unused inputs and three unused outputs that may be applied to reduce logic elsewhere in the system.

(continued on page 216)
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AVERST

CIRCLE 120 ON INQUIRY CARD

ADDRESS RANGES FOR 16 COMBINATIONS OF DEVICES

	IUN
800-1FFF 2k, 2k, 2k,	2k
800-27FF 2k 2k 2k	4k
000-27FF 2k 2k 4k	2k
000-2FFF 2k 2k 4k	4k
000-27FF 2k 4k 2k	2k
000-2FFF 2k. 4k. 2k.	4k
800-2FFF 2k. 4k. 4k.	2k
800-37FF 2k. 4k. 4k.	4k
000-27FF 4k 2k 2k	2k
000-2FFF 4k 2k 2k	4k
800-2FFF 4k, 2k, 4k,	2k
800-37FF 4k. 2k. 4k.	4k
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800-37FF 4k. 4k. 2k.	4k
000-37FF 4k 4k 4k	2k
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	800-1FFF 2k, 2k, 2k, 800-27FF 2k, 2k, 2k, 9000-27FF 2k, 2k, 2k, 9000-27FF 2k, 2k, 4k, 9000-27FF 2k, 2k, 4k, 9000-27FF 2k, 4k, 2k, 9000-27FF 2k, 4k, 4k, 9000-27FF 2k, 4k, 4k, 9000-27FF 4k, 2k, 2k, 9000-27FF 4k, 2k, 2k, 9000-27FF 4k, 2k, 2k, 9000-27FF 4k, 2k, 4k, 9000-27FF 4k, 2k, 4k, 9000-27FF 4k, 2k, 4k, 9000-27FF 4k, 4k, 2k, 4k, 9000-37FF 4k, 4k, 2k, 4k, 9000-37FF 4k,

PAL DESIGN SPECIFICATION

EXAMPLE 1

PALIDALS - PAL TYPE PN1001 - PATTERN NUMBER ADDRESS DECODER (EXAMPLE 1) - NAME OF DEVICE MMI, SUNNYVALE, CA	B. BRAFMAN 12/10/80	
VMA E ALL ALZ ALB AL4 ALS R/W NC GND NC /CE4 /CEB /CE2 /CEL /OE NC NC NC VCC } PIN	LIST OF SYMBOLIC NAMES	
$ \begin{array}{llllllllllllllllllllllllllllllllllll$	LOGIC EQUATIONS	
NOITHISZER THUTUO DNA ZEJBANE GINE ZETARENES TRAF ZA ZMAR JITATZ & X JS 5 GNA ZMONYO & X JS 5	ENABLE FOR FOLLOWS:	
CE10000-0FFF CE21000-1FFF CE32000-27FF CE42800-2FFF	OPERATION	
EXAMPLE 2		
PALIØLA PAL TYPE PN1002 PATTERN NUMBER ADDRESS DECODER (EXAMPLE 2) NAME OF DEVICE MTI, SUNNYVALE, CA	B. BRAFMAN 12/10/80	
VMA E ALL ALZ ALB AL4 ALS R/W NC GND NC /CE4 /CEB /CE2 /CEL /OE NC NC VCC } PIN	LIST OF SYMBOLIC NAMES	
CEL = /Al5 * /Al4 * /Al3 * /Al2 * /Al1 * VMA CE2 = /Al5 * /Al4 * /Al3 * /Al2 * Al1 * VMA CE3 = /Al5 * /Al4 * /Al3 * /Al2 * Al1 * VMA CE4 = /Al5 * /Al4 * /Al3 * Al2 * /Al1 * VMA CE4 = /Al5 * /Al4 * /Al3 * Al2 * Al1 * VMA /Al5 * /Al4 * Al3 * /Al2 * Al1 * VMA	* E * E * E * E + * E +	
NOITY AND	TPUT ENABLE FOR	
CEL0000-07FF CE20000-0FFF CE31000-17FF CE41000-17FF		N

Summary

The combination of 8-bit wide memory devices and programmable array logic allows designers to implement highly flexible microprocessor based designs with minimal chip count and reduced overall costs. PALASM serves as a useful tool for expediting prototype cycles and documenting PAL designs; this can reduce future problems when changes must be made by designers unfamiliar with the original design. Finally, products with high volume in a specific configuration may switch over to mask programmable array logic, HAL, to reduce costs further.

Please rate the value of this article by circling the appropriate number in the "Comments" box on the Inquiry Card.

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Low 727

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Designated MN375, a dual-inline packaged track and hold (T/H) amplifier offers a combination of precision performance and high speed. Its balanced performance specifications make it suitable for use in fast 13- and 14-bit systems. Linearity is guaranteed to be better than $\pm 0.005\%$ FSR over the operating temperature range. Offset and pedestal drifts are typically 50 μ V/°C. Aperture delay time is 5 ns, and aperture uncertainty is guaranteed to be under 100 ps. Acquisition time to $\pm 0.005\%$ FSR is typically 700 ns, and track to hold settling time (also to $\pm 0.005\%$ FSR) is 150 ns maximum. Pedestal, the unwanted step in output voltage as the amplifier switches from track to hold, is guaranteed to be less than 10 mV over the temperature range.

The device is designed to be adjustment free. Functional laser trimming of the thin film nichrome resistor networks results in linearity, gain accuracy, offset, and pedestal specifications that apply over the device's entire operating temperature range. From Micro Networks Co, 324 Clark St, Worcester, MA 01606, the device is packaged in a standard, hermetically sealed, 24-pin dualinline package and is specified for 0 to 70 °C or -25 to 85 °C operation. For military/aerospace and demanding industrial applications, it is available fully processed and screened to the requirements of MIL-STD-883, Method 5008.

Low aperture uncertainty (100 ps maximum) and linearity of $\pm 0.005\%$ FSR, maximum make it well-suited for use as an aperture reducer in high speed, high resolution data acquisition systems. At the 13-bit level, frequencies as high as 190 kHz can be accurately captured and held for a minimum of 120 μ s. Fully guaranteed performance specifications eliminate external trimming potentiometers and assure field interchangeability without the need for recalibration.

Circle 441 on Inquiry Card



Functional diagram of MN375 track/hold amplifier from Micro Networks Co. When TTL logic "O" is applied to T/H COMMAND (pin 5), device will be in "track" mode. In this mode, device acts as precision amplifier with gain of -1. When logic "1" is applied to T/H COMMAND input, device is placed in "hold" mode. In this mode, output will be frozen at value that was present when "hold" signal was applied

EDC Device Detects and Corrects RAM System Errors*

A general purpose EDC device can detect and correct errors in random access memory systems. The detection time of the LSI device is 34 ns, worst case, and 25 ns, typical. Correction time is 63 ns, worst case, and 40 ns, typical.

Am2960 EDC, from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, will work with any processor, can handle data words from 8- to 64-bits wide and may be operated in multiple modes to optimize performance or economy. In operation, the EDC generates a set of check bits that are stored with the data bits when a data word is written into memory.

On a read from memory the EDC examines both the data and check bits to determine if the data and check bits are correct. Single-bit errors, if present, will be corrected. Some double-bit errors also can be corrected. If an error is detected, flag outputs go active and may be used to interrupt the processor to stretch the memory cycle. For single-bit errors, the EDC will automatically correct the data which may then be rewritten into memory and sent on to the processor.

The EDC can cut field maintenance costs in two ways. First, since it corrects all single-bit hard errors, a bad RAM will not cause a system crash. The bad RAM can then be replaced at the next regularly scheduled maintenance session. Second, the EDC makes available the error syndromes that indicated which bit is in error. These syndromes can be logged and later examined to determine RAMs that exhibit increasing intermittent error patterns. A preventive maintenance program could then replace these RAMs before they permanently fail.

The Am2960 EDC comes in a 48-pin DIP and requires a single 5-V supply. It will also be available as the Am28160 which is optimized for Am28000 designs. Military temperature range parts are also available.

*This item appeared in the February issue with an incorrect company name and model number and appears again to rectify those errors.

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CIRCLE 122 ON INQUIRY CARD

512 x 8 CMOS PROM Utilizes Fuse Links

Utilizing polycrystalline silicon fusible links as programmable memory elements, the HM-6641 4096-bit CMOS PROM is packaged with a standard 24-pin pinout similar to 512 x 8 bipolar PROMs and 2k x 8 EPROMs. From Harris Semiconductor, PO Box 883, Melbourne, FL 32901, the PROM employs CMOS selfaligned silicon gate processing techniques to attain high speeds while maintaining low power dissipation. Worst case performance over temperature is 200-ns access time and $100-\mu A$ maximum standby current.

Onchip address latches are provided, easing the interface to those recent microprocessors that use multiplexed address/data bus structures, such as the 8085. The output enable controls, both active low and active high, further simplify microprocessor system interfacing by allowing output data bus control independent of the chip enable control.

The data output latches allow use in high speed pipelined architecture systems, and also in synchronous logic replacement functions. Applications include low power handheld microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, processor control store, and synchronous logic replacement.

Selected memory locations are permanently changed from their manufacture state of all low (v_{OL}) to a logical high (v_{OH}) , by the application of programming potentials and pulses. Both high v_{CC} (6.0 V) and low v_{CC} (4.0 V) verify cycles are specified to ensure the integrity of the programmed fuse.

The worst case programming time required is 37.4 s and typical programming time is approximately 4 s per device. The chip (\overline{E}) and output enable (\overline{G}) are used during the programming procedure. On PROMs that have more than one output enable control, \overline{G}_1 is used. The other output enables must be held in the active, or enabled, state throughout the entire programming sequence. All pins of the programmer's socket should be at ground potential when the PROM is inserted into the socket. V_{CC} must be applied to the PROM before any input or output pin is allowed to rise. Circle 443 on Inquiry Card



Functional diagram of Harris Semiconductor's HM-6641 4096 fuse link CMOS PROM. In read cycle, address information is latched into onchip registers on falling edge of $\vec{E}(T = 0)$. Minimum address setup and hold tie requirements must be met. After required hold time, addresses may change state without affecting device operation. To read data \vec{G}_1 and \vec{G}_2 must be low, and G_3 must be high. After access time, \vec{E} may be taken high to latch data outputs and begin TEHEL. Taking either or both \vec{G}_1 and \vec{G}_2 high or G_3 low will force the output buffers to high impedance state. Output data may be reenabled at any time taking \vec{G}_1 and \vec{G}_2 low and G_3 high. On the falling edge of \vec{E} the data will be unlatched

High Input Impedance Op Amps Introduced

Designated NE/SE 5512 (dual) and NE/SE 5514 (quad), two recently introduced operational amplifiers are suitable for applications that require stability under closed loop conditions, such as active filter designs, active integrator, and active differentiator circuits. The high input impedance (100M Ω) devices will perform in instrumentation areas where low bias current 10 nA maximum, and low offset voltage, 2 mV maximum, are required. These areas include high impedance transducer applications that formerly required FET input buffering or a current to voltage converter.

Available from Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, the NE/SE 5512 is pin for pin compatible with industry standard duals, such as the MC 1458. The NE/SE 5514 is pin compatible with the LM 124-324. Other features include distortion of 0.01% at 10 kHz, and interamplifier cross coupling of -120 dB and a typical slew rate of 1 V/ μ s. The signal voltage gain of 50,000 minimum for both chips is claimed to be superior to the gain of any general purpose dual and quad amplifier presently available.

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Wide Temperature Range 16-Bit DAC Settles in 10 μ s

The DAC72C 16-bit IC digital to analog converter (DAC), with internal reference and optional output amplifier, offers a maximum linearity error of $\pm 0.003\%$ of

FSR at room temperature, a 10- μ s settling time, and a maximum gain drift of \pm 15 ppm/°C over 0 to 70 °C. A second DAC with a temperature range of -25 to 85 °C is also available. Designated DAC72, the device exhibits a maximum linearity error of \pm 0.003% of FSR at room temperature and a gain drift of \pm 7 ppm/°C from 25 to 85 °C and ± 15 ppm/°C from -25 to 25 °C. Gain drift as a function of temperature for both DACs is shown in the Figure.

Three basic models accept complementary 16-bit binary or complementary 4-digit BCD TTL-compatible input codes. Fast settling switches and stable laser trimmed thin film resistors allow the selection of output voltages of 0 to 10 V (CSB and CCD) or ± 10 V (COB) and output currents of ± 1 mA or 0 to -2 mA. Input power is ± 15 and 5 Vdc. The device, from Burr-Brown, PO Box 11400, Tucson, AZ 85734, is packaged in a 24-pin dual-inline package.



Gain drift as function of temperature for Burr-Brown's DAC72 and DAC72C. Gain drift is measure of change in full scale range output over temperature expressed in parts per million per °C

For optimum performance and noise rejection, power supply decoupling capacitors need to be added. These capacitors (1 μ F tantalum or electrolytic are recommended) should be located close to the DAC. Electrolytic capacitors, if used, should be paralleled with 0.01 μ F ceramic capacitors for best high frequency performance.

Offset and gain may be trimmed by installing external offset and gain potentiometers. TCR of the potentiometers should be 100 ppm/°C or less. The 3.9M Ω and 510k Ω resistors (20% carbon or better) should be located near the DAC to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network may be substituted in place of the 3.9M Ω resistor. A 0.001 μ F ceramic capacitor should be connected from gain adjust, pin 22, to common so as to prevent noise pickup. If the full accuracy of the DAC is required, recalibration of gain and offset every 2 months is recommended. Circle 445 on Inquiry Card



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Dense 16k Static RAM Has 55-ns Access Time

Fabricated using high performance MOS technology, the 2167 static RAM offers a 4-fold increase in density over standard 2141 and 2147 RAMS. The device, from Intel Corp, 3585 SW 198th Ave, Aloha, OR 97005, is organized 16,384 words by 1 bit. The 2167's density, 55-ns speed, and static operation make it suitable for 2147 high speed mainframe and minicomputer applications such as main memory, buffer, and cache. High density and low power consumption also make it suitable for microprocessor systems that utilize the 2141. The device will be offered in these four speed/ power combinations: the 2167-55 with maximum access time of 55 ns. maximum active current of 125 mA, and maximum standby current of 40 mA; the 2167-70 with 70 ns, 125 mA, and 40 mA; the 2167L-70 with 70 ns, 90 mA, and 30 mA; and, the 2167-10 with 100 ns, 90 mA, and 30 mA.

The RAM is manufactured with three extra memory rows. If a defect is discovered during processing, the faulty row is replaced with a redundant row. The company expects to obtain increased yields from such redundancy, which should lead to improved parts availability.

A low power standby mode automatically reduces average device power consumption. While lowering power usage, the power-down feature maintains RAM operating speed and system data throughput and does not require clocking or complex power switching techniques. (See Figure.) Inputs and outputs are TTL compatible and are unlatched to ensure simple, static timing. No address setup and hold timings are needed. Unlike many other classes of MOS RAMS, the device does not require clocks or timing strobes. The device is contained in a 20-pin package with the industry standard 16k x 1 pinout and requires a 5-V power supply.

Also recently announced, a new board level product incorporates the 2167 into the company's Series 90 family of memory systems. The CM-92 memory module for general purpose computer applications makes the high density of the 2167 available to designers at the system level.

Circle 446 on Inquiry Card



quirements are reduced in less than one cycle after CS goes high. Standby mode continues as long as CS remains high

Controller Chip For 2816 EEPROM With Support Kit

The single-chip MF2801 is claimed to be the first integrated controller for the 5-V electronically erasable programmable read only memory (EEPROM). From Mark Five Systems Inc, 836 Fourth St, Ouray, CO 81427, the controller replaces over 40 TTL devices and generates the waveforms required by Intel's 2816 EEPROM. It is housed in a standard 40-pin package. An intelligent EEPROM controller, it supports a range of polled, interrupt driven or dualported memory subsystems. It interfaces directly to a main CPU via an 8-bit standard asynchronous system bus. The controller eliminates system overhead on ERASE, WRITE (programming), and READ bytes or blocks of 2816 EEPROM data.

Operations are fully buffered. Automatic verification and cycle timing are provided for ERASE, WRITE, and MODIFY operations. One to thirty-two Intel 2816 devices can be controlled in a 64k-byte address space. Both single-port

and dual-port EEPROM memory systems can be configured, allowing either a minimum component count system design or high speed access to the memory system for direct program execution.

An optional onchip PASSWORD protection system guards critical data in EEPROM against inadvertent modification. The PASSWORD protection is useful in high noise, multitasking, or reprogrammable applications such as industrial, numerical, and process control.

The device is housed in a standard 40-pin ceramic dual-inline package. External support circuitry consists of a crystal (1.0 to 6.0 MHz) and bypass capacitor (20 pF) or an optional TTL oscillator signal in the same range; a 5-V power supply; a reset capacitor; one to three Intel 8243 expanders; a 74LS00; a circuit to develop the non-TTL signals VPP and OE/ required by the 2816; and miscellaneous pull-up resistors.

SEEK 1 (System EEPROM Evaluation Kit) supports the device. Electronic circuits required to implement an EEPROM memory system (except for a 5-V, 1.5 A power supply) are included in the kit.

The kit supports buffered READ, WRITE, MODIFY, and ERASE operations for one to four, user supplied, 2816 EEPROMS (8k-byte maximum). It can be expanded to support a larger memory space and may be configured in a dual-port memory arrangement. The kit comes with tested components, schematics, data sheets, and applications information.

Circle 447 on Inquiry Card

Logic Array Family Supported by Automated Layout and Design Software

Fabricated in Schottky transistor logic (STL) technology, a family of high performance LSI master logic arrays are supported by a design and layout automation system. Two members of the STL array family from Texas Instruments Inc, Semiconductor Group, PO Box 225012, Dallas, TX 75265, are currently in production: the TAT008, a 1008-gate master logic array, and the TAT004 with 540 gates. Nominal internal array gate performance is 2.5 ns at 600 μ W. (See Graph.)



Average propagation delay time of internal gate of TAT series STL arrays from Texas Instruments Inc, are function of network interconnect length. Over 90% of metalized interconnect pattern to base lengths are less than 20 mils

The TAT008 has 108 I/Os and the TAT004 has 84. Both are offered in a variety of packages, including standard dual-inline packages, chip carriers, and 100-mil array of pins packaging. Operating voltages are nominally 5 V for I/O buffers and 2 V for internal logic. Devices are specified for operation over the ambient temperature range of 0 to 70 $^{\circ}$ C. Applications for the logic arrays range

from selective replacement of multiple small to medium scale integration functions, achieving, in many cases, complete board integration, to the implementation of totally LSI-based designs.

An integrated software design support system for the logic array family includes simulation, design verification, routability, and testability analysis. Automatic placement and routing typically result in 80% array utilization. The customer describes the array requirements in two high level structured design languages provided by the company. The first, HDL (Hardware Description Language), contains a behavioral as well as structural description that is similar in content to the function table and logic diagram contained in the data sheets of standard digital ICs. The second language, TDL (Test Description Language), is used to describe the required input stimuli and output response characteristics of the desired custom function.

Customer design support is available now from the company's Houston facility and will be made available later in 1981 from regional technology centers located in Boston, Chicago, and Los Angeles. Additional design support is provided by the HDL software macro library consisting of more than 70 functions that are equivalent to many standard low power Schottky TTL functions. In addition, the macro library has new functions that take advantage of the unique features of STL technology. Circle 448 on Inquiry Card

Family of CMOS Master Chips Introduced

Exar Integrated Systems Inc, 750 Palomar Ave, PO Box 62229, Sunnyvale, CA 94088, has announced a new family of CMOS semicustom gate arrays, or "Master Chips," based on a metal gate complementary MOS process. The initial series is comprised of a family of four gate array chips. Digital systems of 200- to 400-gate complexity can be customized into a monolithic LSI chip, at a fraction of the time and cost of a conventional custom design. Semicustom prototypes, using the CMOS master chips, can be fabricated within several weeks, and full production can start within two to three months after prototype acceptance. The four chips are directly compatible with similar gate arrays available from Interdesign Inc, and Master-Logic Inc. Circle 449 on Inquiry Card

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Voltage Programmable Signal Processing and Signal Generation ICs Offered

The CEM 3300 series of ICs from Curtis Electromusic Specialties Inc, 110 Highland Ave, Los Gatos, CA 95030, are signal generation and processing devices intended for applications in electronic voice synthesis, and precision low frequency test equipment. All four devices in the series feature linear or exponential voltage control of their functions over a range of 10,000 to 1, low noise and distortion, low temperature drift, and low feedthrough of the control signal into the output. The CEM 3310 voltage controlled envelope generator produces an output transient wave form for sweeping voltage controlled amplifiers or filters. CEM 3340 VCO is an accurate high stability oscillator that allows both the exponential and linear

sweep of frequency over a range of 50,000 to 1 minimum.

Well-suited for speech recognition and synthesis, the CEM 3320 is a voltage controlled filter, and CEM 3330 and CEM 3335 Dual VCA consist of two independent precision controlled amplifiers with low distortion, noise and control feedthrough. The 3320 voltage controlled 4-pole filter includes onchip voltage controllable resonance. Four independent sections may be interconnected to provide a wide variety of filter responses, such as low pass, high pass, band pass and all pass. A single input exponentially controls the frequency over greater than a ten octave range with little control voltage feedthrough. Another input controls the resonance in a modified linear manner from zero to low distortion oscillation. For demanding applications, provision has been made to allow trimming for improved control voltage rejection. Each filter section features a novel variable gain cell which, unlike the traditional cell, is fully temperature compensated, exhibits a better signal to noise ratio and generates its low distortion predominantly in the second harmonic.

The 3330 and 3335 self-contained, precision voltage controlled oscillators feature both exponential and linear control scales and up to four buffered output waveforms: triangle, sawtooth, square, and pulse with voltage controllable puse width. Full temperature compensation contributes to the stability of these vcos and eliminates the need for a temperature compensation resistor. The exponential and linear control inputs are virtual ground summing nodes, allowing multiple control voltages to be mixed within the device itself. Also included is provision for hard and soft synchronization of the frequency, and an output for adjustment of high frequency tracking. Circle 450 on Inquiry Card

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A new combination of ingredients

The 8051 family sets the standard for the next generation of single-chip microcomputers. And opens new application opportunities where a multiple-chip approach would have been necessary before.

For large program storage, there are 4K bytes of ROM/EPROM, 128 bytes of RAM for internal scratchpad, and 20 registers for controlling peripheral functions. Plus the memory space is expandable to 64K bytes each of RAM and ROM.

The 8051 also offers extended CPU processing capabilities, multiple addressing modes, and four 8-register banks. Furthermore, it's fast. Multiply and Divide execute in 4 μ s. Over half of the remaining instructions execute in 1 μ s; the rest in 2 μ s.

Then there's the 8051's full duplex serial I/O port, which allows it to talk to peripherals—such as terminals and UARTs—at a much higher data rate than could be achieved using software alone. At rates, in fact, from 122 to 31,250 baud. This port can also link multiple 8051s to achieve transmission rates up to 187,500 baud using standard asynchronous protocols and an address-driven automatic wakeup.

Added to that is the 8051's sophisticated interrupt system, with five sources, two priority levels, and a nested structure which allows exceptionally efficient monitoring of internal and external alarms.



Boolean bit manipulation

In addition to handling 8-bit binary and BCDarithmetic, plus 8-bit logic operations, the 8051 family offers an exclusive feature: extensive Boolean bit-handling—especially important in controller applications.

An integral part of the CPU, the Boolean processor has its own set of 12 instructions, its own accumulator, and its own bit-addressable RAM and I/O. With these instructions, now you can do bit manipulation without extensive data movement, byte masking/shifting, or testand-branch trees.

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Intel support further includes the ICE-51[™] in-circuit emulator, which lets you exercise your system at full processor speed with all of its I/O functions. So you can analyze test results quickly, even before your application system hardware is available. Or fully debug your system in logical segments before committing code to EPROMs or ROM. Thus getting a more reliable product to market faster.

Come and get it

A direct descendant of the industry-standard 8048, the 8051 family is the beginning of the new MCS-51[™] series of high-performance devices. In addition to the ROMbased 8051, the other two members of the immediate family are the 8751 EPROM version, intended for prototyping and low volume production, and the 8031, which relies on external program memory.

For further details on the 8051 family and its development support, contact your local Intel sales office/ distributor. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

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PRODUCT FEATURE

Microprocessor Based Digitizers Combine High Accuracy, Speed, and Resolution with Low Price



Flexibility, built-in menu area, and capability to be downloaded for CAD or OEM applications are said to give Houston Instrument's 7000 series digitizers added importance to the industry. Four models, based on tablet sizes, are offered. Available with choice of cursor, each unit consists of translucent tablet, cursor, controller, and interconnect cable between tablet and controller.

Design Features

Five sets of DIP switches enable users to operate the microprocessor based digitizers with a number of different computer systems. With those 40 switches, located on the controller's rear panel, users can make parameter changes in the field that ordinarily would require returning a unit to the factory. Switch positioning allows users to change tag and terminating characters, to block data transfer, or to enter a delay after each character set.

Each tablet has an additional area of 1.2" (3 cm) in both X and Y directions around its perimeter that is intended for menu applications. For example, a 12×12 " (30.5 x 30.5-cm) tablet actually can provide a 14.4 x 14.4" (36.6 x 36.6-cm) active area with only a slight downgrade in accuracy. Because this additional area has an accuracy of ± 0.010 "

(0.254 mm) [compared to overall 0.005" (0.127-mm) accuracy], it can be used effectively as an active digitizing area.

Ability to download enables the unit to be operated directly from the computer in choice of mode, removing the need for the operator to make decisions. Action of any of the 40 DIP switches can be duplicated by the computer.

Dual connections on each tablet, one per side, simplify use. To accommodate the left- or righthanded operators, the cursor can be plugged in on either side so that the cord need not be in the way during any digitizing procedure. In addition, the tablet's smooth surface offers easy access to its full area without interference. A built-in annunciator, standard on all units, provides an audible signal as each bit of information is digitized. A switch permits the operator to bypass this feature.

Three types of input devices are offered. A single-button unmagnified cursor is standard on all models, and a stylus and 12button cursor are available as options. Each cursor has a magnet in its base so that the operator can hang it up at the end of a procedure by placing it on the metal area surrounding the tablet. A flexible, light, and reliable singleshielded cable is standard with all cursors. Dual-tablet operation is also possible. Any tablet can be fieldconverted to serve as either master or slave. Standard options include power lift stand, light box for the two largest tablets, visual display, and magnified (2x) cursors.

As with any digitizer, a precision grid network determines positioning. With these digitizers, however, a precision printed circuit board is used for the grid network.

Specifications

Four tablet sizes are available. Model 7012 has a 12 x 12" (30 x 30-cm) tablet, model 7024 has a 24 x 24" (61 x 61-cm) tablet, model 7048 has a 36 x 48" (91 x 122-cm) tablet, and model 7060 has a 42 x 60" (107 x 152-cm) tablet. Accuracy is ±0.005" (0.127 mm), and standard resolution is 0.001" (0.025 mm), although operator selectable to 0.005 to 0.010" (0.127 to 0.254 mm). Standard speed is 200 coordinate pairs/s, but operator selectable at 1, 2, 5, 10, 20, 50, or 100 pairs/s.

Switch selectable output is parallel BCD or binary. Dual-port asynchronous RS-232-C output is available as a factory installed option. Output is also operator selectable in either inch or metric units. The origin is operator selectable and relocatable. Operating modes are point, switch stream, stream, and increment.

Price and Delivery

Prices for model 7012 will start at \$2900. OEM discounts are available. Delivery is 60-90 days ARO. Houston Instrument, 1 Houston Sq, Austin, TX 78753. Tel: 512/ 837-2810.

For additional information circle 200 on Inquiry Card.

See at NCC Booth 911

Just think what you can do with that speed. At 240 1pm, 80 characters per line, you can copy a full 24 line CRT screen in 6 seconds...or deliver a memo by phone at 1200 baud.

No problem. Because the TH 240's clean design and unique thermal dot matrix printhead deliver that speed reliably and without a sound. With thousands installed and field proven, you can buy with confidence. What's more, the TH 240 has self test diagnostics and three easily replaceable subassemblies for the ultimate in serviceability...and you get the support of 40 service centers nationwide. You don't need to maintain a TH 240 inventory...we do it. Call or write for details today.

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CIRCLE 170 ON INQUIRY CARD

Now! Raycorder II A Digital Cassette Recorder That Thinks For Itself

Raymond Engineering's new Raycorder II Model 6440 digital cassette recorder utilizes the latest microprocessor technology to provide a new standard of excellence for the '80's at a low, low price.

The only moving parts on the Model 6440 are the two

reel motors. A unique digital-processorbased servo controls the reel motors to provide constant tape speed and uniform tape tension, regardless of the amount of tape on either reel. Tension is also precisely controlled during starting and stopping.

While engineers will appreciate its per-



formance and reliability, users will appreciate the ease of cassette loading and removal.

Adding the advanced technology of Raycorder II to its previous achievements, Raymond leads again in digital cassette recorder design!!

Ask for free literature on the Raycorder II.

Raycorder Products Division **Raymond Engineering Inc.** 217 Smith Street Middletown, Connecticut 06457 (203) 632-1000



Intelligent Graphic Display System Reduces Software Development Effort

The GS8000 dual-processor architecture executes the full range of operations required in an interactive graphics environment. The integral MC68000 with full function set and 16M-byte addressing range is capable of managing and manipulating a high precision graphics data base. Display processor controls raster frame buffer, and performs raster conversion of vectors, circles, and filled areas. High level graphics operations are provided for both input and output. Graphics functions are modeled after the ACM SIGGRAPH GSPC core proposed software std for computer graphics. The system uses a 31-bit word coordinate system that provides a virtual resolution of 4G points/axis. It accepts graphics primitives, including lines, circles, filled polygon areas, and text, described in the coordinate system, and retains them in a data base in graphics processor memory. Data base is segmented under user control to permit incremental updates. Extensive windowing capabilities are provided, the user defines multiple windows on the coordinate system that can be refreshed out of the internal data base. Std hardware configuration includes 16/32-bit graphics processor with 64k-bytes RAM and up to 24k-bytes P/ROM, display processor, and high speed parallel interfaces. Graphics processor options include additional RAM in 128k increments (max of 1M byte), RS-232-C host interface for remote use, and interfaces to input devices including keyboard, data tablet, digitizer, trackball, and joystick. Resolutions are 640 x 512 or 1280 x 1024. Lexidata Corp, 755 Middlesex Tpk, Billerica, MA 01865.



Circle 201 on Inquiry Card

Automatic Power Supply Test System Handles Specialized Test Requirements



Through use of an automatic program generator and universal test programs, programming of the POWERTEST for 11 std power supply tests can be accomplished by nontechnical personnel in 15 min. More specialized testing is accommodated through availability of 2 IEEE STD 488 I/O channels and BASIC-488, a high level language incorporating commands to IEEE Std 488 and power supply testing. The unit accommodates up to 8 field installable loads with power of 250, 1000, and 2500 W. For testing the logic state of power supply control signals, there are 8 digital inputs with programmable references and 2 event timers. Programmable digital outputs provide for computer control of the supply's internal relays and solid state switching circuitry. The unit uses a 12" (30-cm) display that handles 24 lines with 80 chars/line, 96 ASCII u/lc alphabet. The keyboard has 91 keys in a standard typewriter style and adds 11 special function keys and 2 transmission keys. The central processing unit, a Z80 microprocessor, operates at 4-MHz clock frequency and has 64k bytes of dynamic RAM, floppy disc controller, IEEE STD 488 controller, I/O slave processor, DIN/DOUT controller, and general purpose relay controller. 256k bytes of formatted mass memory is provided on one 8" (20-cm) single-density floppy disc drive with 31.24k-byte/s transfer rate. N H Research, Inc, 16601 Hale Ave, Irvine, CA 92714.

Circle 202 on Inquiry Card

video, audio, and other data communications over the same cable system without interference. In point to point configuration, up to 14 full-duplex circuits per TV channel may operate simultaneously. Additional features include initialization controls, allowing each device to be configured for individual applications, point to point or multidropped connections, and built-in diagnostics and status indicators (CD, X-CLK, RD, SD, DSR, RTS) that permit rapid fault analysis. The unit operates in simplex, full-, or half-duplex modes using a synchronous data format, and biphase shift keyed carrier (BPSK) modulation. There may be 42 duplex circuits/cable system. Bit error rate is 1 x 10⁻⁸ at required C/N ratio. Transmitter provides 35 dBmV +0, -15 dB, adjustable transmit level with ±1-dB stability over temperature. Receive level is $-7~dBmV~\pm10~dB$ and carrier detect level is -25~dBmV~-10,~+15~dB, adjustable. Amdax Corp, 160 Wilbur PI, Bohemia, NY 11716. Circle 203 on Inquiry Card

Rf Modem Handles High Speed Data Transmission Over Broadband Coax



DAX 1140, an important adjunct to the IBM 3274 control unit, supports the CCITT V.35 interface and is capable of supporting data transmission speeds up to 56k bits/s. Designed for high performance duplex operation over broadband coaxial cable, the modem utilizes bandwidth efficiently, permitting Introducing the Butterfly $^{\mbox{\tiny M}}$ switch. The first key Tronic capacitive

keyboard with linear For years our feel. have been customers using tactile successfully feel, however, we've had input from the field that a lot of you like linear feel. Key Tronic now offers both. We want to be your keyboard supplier.

This patented solid-state keyboard uses the same electronics as our proven tactile design. You still get N-key rollover (a must in any medium to high speed data-entry environment) at no extra charge. The same double-shot molded keytops with over 20,000 legends and over 300 shapes are still available from the leader. TM

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Division of Farrand Industries, Inc. 99 Wall Street Valhalla, NY 10595 (914) 761-2600 Telex: 646640

PRODUCTS

Microprofile 58-Key Sealed Keyboard Meets European Safety Standards



Model MK 038-001 keyboard meets ergonometric standards (safety regulations) required by European countries (VED, DIN, VDI, and ZH documents). Overall keyboard profile is approx 0.400" (1.016-cm), allowing improved packaging for portable and desktop applications. The keyboard provides a crisp tactile feedback to the operator, which coupled with the shorter 0.060" (0.152-cm) travel allows faster throughput. The patented 2.8-oz (79-g) force keyswitch construction provides hysteresis that eliminates teasing. Metal dome keyswitches are sealed from the environment to extend the life of the keyboard. Legends are graphically applied on the bezel to provide advanced styling, or can be added to the buttons to allow more than one operating mode for the keyboard. The unit mounts from the front of the enclosure or flat panel via 8 male mounting studs. Key spacing, operating force, and row offset are that of a conventional typewriter. Nom specs include 15M MCBF, 2-ms bounce, and 2- Ω contact resistance. Switch outputs are terminated at 0.025" (0.064-cm) straight pins located on the backside of the PC board. Switch matrix is an 8 x 8 array. Advanced Input Devices, PO Box 1818, Couer d'Alene, ID 83814. Circle 204 on Inquiry Card

Portable Information Media Integrates Dynamically Updatable Memory

The Information Key is a small lightweight key-shaped device of strong ABS plastic construction that encapsulates an alterable nonvolatile random access memory. Data stored may be read, written, or updated in whole or in part

when the key is inserted into any device with an appropriate receptacle. Random access to data in the key occurs at millisecond speed utilizing electronic devices with no mechanical parts to



wear or misalign. With normal usage, the electrically alterable memory has a tolerance of 10° read accesses between writes and 10° erase/write cycles. The device may contain any data set or sets. Information for specific uses can be stored in secure format within the key. Multiple concurrent information uses can coexist, and may be managed by access devices. **Datakey**, **Inc**, 7710 Computer Ave, Minneapolis, MN 55435.

HOW TO IMPROVE THROUGHPUT IN PRODUCTION PROM PROGRAMMING.

Select a PROM programming system designed specifically for production.

The new Data I/O production PROM programming system combines a Data Control Unit (DCU) for storing all your production programming data and a production programmer that's easy on the operator.

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The DCU can store enough data on a single diskette to replace 41 master PROMs (2716 type) or 2,000 feet of paper tape. Programs can be assembled in engineering, downloaded from an MDS or computer via RS-232C to a diskette, then sent to manufacturing for controlled production.

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CIRCLE 135 ON INQUIRY CARD

PRODUCTS

PACKAGING AND INTERCONNECTION

FLUOROPOLYMER FOAM

For use as insulation in RG-8, -11, -59, and -62 computer coaxial cable constructions, HALAR^R 555 fluoropolymer is supplied as a 1-part resin system that is processed to a 55% void content. Because the foaming agent is an integral part of the resin system, no additional processing equipment is required. Power limited coaxial cable constructions using the foamed insulation and HALAR ECTFE jacketing have been listed by UL for use in 600-V wire and cable constructions, such as those in computer interconnect applications. Allied Chemical Corp, Fluoropolymers, Fibers and Plastics Co, PO Box 2332R, Morris Township, NJ 07960.



Circle 206 on Inquiry Card

SUBMINIATURE HIGH DENSITY CONNECTOR

M-D series crimp connector features rear release retention system and conforms to performance requirements of MIL-C-24308. Plug and receptacle housings, available in sizes 9, 15, 25, 37, and 50, provide retaining fingers that eliminate need for spring clips on each contact; size 20 stamped and formed contacts accommodate wire sizes #20 through #28. Current rating is 7.5 A, contact resistance is 7.5 mΩ max, and temperature range is -55to 125 °C. **Contact Electronics Inc**, 30 Plymouth St, Fairfield, NJ 07006.



Circle 207 on Inquiry Card

ELASTOMER FLAT CABLE CONNECTOR

MOE connects flat cable with closely spaced wires to PC boards without using sockets or soldering, matching signal wires spaced on 0.05" (1.27-mm) centers and the pairs of ground lines between them. Ground line contacts are shorted and signal line contacts flare out to wider pads that press against corresponding PC board pads. Fixture accurately aligns connector paths with appropriate stripped cable wires; these wires remain accurately in place if stripped length is less than 0.25" (0.64 cm). Hulltronics, Inc, 333 Byberry Rd, Hatboro, PA 19040.

Circle 208 on Inquiry Card

2-PIECE HEAT SINK



6031 series forced air cooling package is a 2-piece modularly constructed unit designed for mounting and cooling electronic components. Constructed with a fin design that offers less air flow resistance and results in maximum heat transfer and optimum thermal performance, the device is intended for use with a mini boxer type fan [3.200" (8.138 cm) sq]. It is available with steel or glass filled nylon end plates. The 2-piece quadrant construction is offered in any length and can be provided without shelf for stud mounted devices. Heat Sinks Plus, 28042 Del Rio Rd, Temecula, CA 92390. Circle 209 on Inquiry Card

DOUBLE-ROW SOCKET STRIPS

Strips have from 2 to 32 contacts at 0.10" (0.25 cm) in row and 0.10" (0.25 cm) between rows; any number of strips can be arranged to maintain grid pattern. Terminals are short solder type or 0.5" (1.2-cm) long solder type, and are bused to other rows, providing a common 1-row pin out. All contact styles allow stacking

arrangements for breadboarding or vertical packaging, and accept ICs and components with lead cross section of 0.015 to 0.022" (0.038 to 0.055 cm). **Samtec Inc**, 810 Progress Blvd, New Albany, IN 47150. Circle 210 on Inguiry Card

PCB HEADER ASSEMBLIES

0.100" (0.254-cm) centerline headers have 2 through 28 circuit positions and 0.025" (0.063-cm) square post; 0.156" (0.396-cm) centerline headers have 2 through 24 circuit positions and 0.045" (0.114cm) square angle posts and 0.045" (0.114-cm) square or round straight posts. Flat, locking, and polarizing thermoplastic header wafers are available. Units are compatible with most crimp type or insulation displacement female connectors. **Panduit Corp**, 17301 Ridgeland Ave, Tinley Park, IL 60477.

Circle 211 on Inquiry Card

DIN CONNECTORS



Aladdin line of PC board, 2-part, DIN and EIC std connectors offers two basic configurations: STV-C96, a 96-contact pair (3 rows on 2.54-mm grids) with a male wave solderable connector and a female with 96 wirewrap 0.6 x 0.6-mm pins 13 mm in length for up to 4 modified wirewraps, and a 2-row style with 64 contacts on a 10-mm grid. Connector ratings range from high power 20-A contact to nominal 4-A high density types. **Erni Components Corp**, 3316 Commercial Ave, Northbrook, IL 60062.

Circle 212 on Inquiry Card

PRODUCTS

SOFTWARE

COMMUNICATIONS SOFTWARE PACKAGE

Developed for Honeywell Level 6 hardware, package handles interfacing of the Votrax voice response unit, providing all protocol handling and a simple direct interface to any language supported by the computer. Capable of supporting up to 256 phone lines, the system is composed of system level hardware/software interface, new call monitor, and autonomous file transmission monitor. The first two work together to provide applications program support for talking and listening to the caller. The third is a standalone subsystem that periodically scans a scheduling file to determine if any files are to be transmitted. The interface program controls all traffic to and from the voice unit. Line numbers and timing are user transparent. Only speak and listen operations need to be performed by the user program. Automatic line buffering, computer down

monitoring, and other operations are handled by the package. Hardware configuration is automatic, requiring only a std Honeywell configuration file parameter card in the CLM (configuration load manager) file. Local and remote voice units, as well as any valid transmission protocol, may be configured within the same computer system. **Communications and Special Software, Inc,** 8406 Center Dr, Spring Lake Park, MN 55432. Circle 213 on Inquiry Card

BATCH SYSTEM GRAPHICS SOFTWARE

Pie, bar, and line charts are produced using an easy to learn set of procedures that enable users to design charts in a range of formats, colors, and patterns. Device independent, the graphics option runs on most hardware currently available; procedures are integrated into the batch system. Plots produced can be labeled, with user defined u/lc titles, footnotes, and comments. All plots can be previewed interactively before final production begins. **spss**, **Inc**, 444 N Michigan Ave, Chicago, IL 60611. Circle 214 on Inquiry Card

VIRTUAL MEMORY SOFTWARE PACKAGE

Written in Pascal or C, VM is accessed by subroutine calls, allows programmers to handle up to 10 files of arbitrary size without concern for disc I/O and buffering, and provides efficient use of main memory. Package runs on Data General Eclipse under AOS, and on DEC PDP-11 under UNIX, RSX-11, and RT-11. Additional separate program allows any file to be displayed interactively in octal, hexadecimal, decimal, and character format. **Giordano Assoc, Inc, Software Ctr,** 629 Godwin Ave, Midland Park, NJ 07432.

Circle 215 on Induiry Card



MFE's auto-reloading, onemegabyte, two-track cassette transport.

MFE's 452 series two-track transport automatically reloads itself for the second track. So in effect you get twice the storage of ordinary transports from a single load — up to one megabyte.

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PRODUCTS

DATA COMMUNICATIONS

DATA ENCRYPTION DEVICE



Two versions of Secre/Data model BU 102, a standalone unit with power supply and a plug-in module for rack cage mounting, feature automatic cipher synchronization, nonlinear coding, 200M code settings behind a locked front panel, and clear/encrypt mode selection. A 19" (48-cm) card cage for 12 units, power supply for 6 units, and asynchronous-synchronous converters are also available. **Com/Tech Systems Inc**, 505 Eighth Ave, New York, NY 10018. Circle 216 on Inguiry Card

PDP-11 COMPATIBLE SERIAL LINE CONTROLLER

Hardware and software compatible with the DEC DL11, SLC11 interfaces the PDP-11 Unibus with an asynchronous serial device. DL11 A, B, C, D, and E features are provided on one board with switch-selectable convenience. Onboard DIP switches allow 16 baud rate selections from 50 to 19.2k for transmit or receive section, data format, address selection, and vector address. Pin for pin compatibility with DL11 cable assemblies simplifies installation. The controller requires 5 Vdc for operation; 12 Vdc is generated onboard to operate EIA circuitry. Computer Extension Systems, Inc, 17511 El Camino Real, Houston, TX 77058.

Circle 217 on Inquiry Card

300/1200-BIT/S MODEM



MT212A Bell 212A compatible modem is available in standalone and rack mounted configurations and operates in full duplex mode over dial-up lines; asynchronous or synchronous operation is selectable in 1200-bit/s mode. Unit provides originating and automatic answering capability; for originating applications, unit connects to telephone via RJ11C, RJ11W, or RJ45S modular connections. Voice to data transferring is via pushbutton on chassis. Multi-Tech Systems, Inc, 82 Second Ave SE, New Brighton, MN 55112. Circle 218 on Inquiry Card

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PR-320T	Yes	36	549.00
PC-1000	Yes	72	1,050.00
PC-1100	Yes	72	1,050.00
PC-2000	Yes	144	1,795.00
PC-2200	Yes	144	1,795.00
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PC-4400	Yes	288	3,295.00

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Low ESR	1.0 ~ 1,000	6.3 to 200	PLU108
CS Low Profile	100 ~ 2,200	10, 16, 25, 35	CS040
PL-B, PL-BG High Ripple	47 ~ 2,200	160 to 450	PLB108
RD High Temperature	0.47 ~ 1,000	10 to 100	RD050
Bipolar	1.0 ~ 100	50, 63	BP376
Computer Grade Can	120 ~ 1,000,000	6.3 to 450	CG018
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All from a top name in electric motors for just about everything—Gould. These Brutes feature Gould's open frame design and patented Recirk™ bearing lubrication system for extended life.

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G A

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12.72 megabytes in a four-platter 5¹/₄-inch drive.

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> Rotating Memory Systems, Inc. 1031-A E. Duane Avenue Sunnyvale, California 94086 (408) 730-1346



SMALL BUSINESS Computers by Lazor Systems, Sunnyvale, CA



PRODUCTS

SUBASSEMBLIES AND CIRCUIT COMPONENTS

COMMON MODE AND DUAL-FUNCTION EMI FILTERS

Designed to meet federal and international specs for line to line and line to ground isolation of generated power noise, filters include A and B series for general purpose applications in 3-, 5-, and 10-A current ratings; C series for international standards and high insertion losses in 3-, 6-, and 10-A ratings; and E, F, and G series for use in switching power supplies. K series units are designed for low impedance loads and high insertion loss capabilities; LD/TD and LY/TY series for 3and 4-phase filtration of balanced and unbalanced loads with Delta power distribution systems, and N series for direct, plug-in capability with IEC specified power line connectors. Genisco Technology Corp, Components Div, 18435 Susana Rd, Rancho Dominguez, CA 90221. Circle 219 on Inquiry Card

ALPHANUMERIC LCDs

DAYSTAR minimum logic modules offer electrical interface, mounting, and cutout dimensions that are identical to those on corresponding earlier modules. The family includes 1 x 16, 2 x 16, 1 x 40, and 2 x 40 modules, an optional ASCII controller IC, and cables. All displays are 5 x 7 plus cursor dot matrix devices. Each requires ±5 Vdc at less than 1 mA. The optional CMOS controller IC reduces system development time by providing an ASCII interface, cursor control, character generation, timing, and refresh functions. Industrial Electronic Engineers, Inc, 7740 Lemona Ave, Van Nuys, CA 91405.



Circle 220 on Inquiry Card

7-SEGMENT COMMON CATHODE LEDS

Pin and function compatible with Hewlett-Packard 10-pin common cathode displays, two 7-segment displays are available in std red, yellow, green, orange, and high efficiency red, providing low power consumption and fast switching for multiplex use. Features common to all units are highly visible bold solid segments, solid state reliability and long operating life, impact resistant plastic construction, high luminosity with high contrast, std 10-pin DIP configuration, and wide angle viewing at 150°. The 0.300" (7.62-mm) series MAN58A, -78A, -88A, -3680A, and -3980A displays are capable of a min luminous intensity ranging from 125 to 510 µcd and have a max forward voltage from 2.0 to 3.0 V, depending on the display color. Each can be mounted in arrays with 0.40" (10.16-mm) center to center spacing and is directly compatible with integrated circuits. The 0.40" (10.16-mm) series MAN 4580A. -4680A, -4880A, and -4980A displays feature min luminous intensities ranging from 200 to 510 µcd, depending on display color. Max reverse current is 100 mA for both digit segment and decimal point. General Instrument, Optoelectronics Div, 3400 Hillview Ave, Palo Alto, CA 94304.

Circle 221 on Inquiry Card

TERMINAL CLUSTER CONTROLLER

Model 132-74U provides an interface between a Univac host computer and up to 12 model 132B terminals and 4 serial printers. Communications between the controller and host computer is at 9600-baud synchronous and via Univac Uniscope interactive protocol; communications between controller and its peripherals are at 9600-baud asynchronous. Terminals and printers operate with 7 data bits, odd parity, and 1 stop bit. **DatagraphiX**, PO Box 82449, San Diego, CA 92138.

Circle 222 on Inquiry Card

SLIDE BASE LEDS

Telephone slide base lamps in 6SB package incorporate high efficiency LEDs instead of incandescent bulbs. LED packages include a built-in resistor so that operating voltages can be selected in the range of 3.6 to 48 Vdc; the lamp can also operate at up to 15 Vac. Available in red, amber, or

green, the package is 0.66" (1.68-cm) long. Color coded cathodes identify the voltage range of the lamp. **Data Display Products**, 303 N Oak St, Inglewood, CA 90302. Circle 223 on Inguiry Card

LOW POWER MOSFETS

Combining low on-resistance with voltages ranging from 60 to 400 V and current ratings from 1.3 to 4 A at 25 °C case temperature, HEXFET IRF510, -610, and -710 series are packaged in compact TO-220 plastic cases. Devices switch in less than 10 ns with std $50-\Omega$ driver outputs. On-resistances as low as 0.6 Ω make them suitable for driving larger bipolar transistors or larger power MOSFETs. International Rectifier, 233 Kansas St, El Segundo, CA 90245. Circle 224 on Inguiry Card

MODULAR FLOATING POINT ADC

ZAD8000 is a modulo 1+2+12 ADC composed of a sign bit, 2 gain ranging bits, and 12 magnitude bits. Designed for applications requiring digitization of audio type signals, the device provides a significant reduction in the perchannel cost, by providing 16-bit performance for critical lower level signals (up to ± 0.625 V) and using 2 bits of automatic gain ranging to decrease effective resolution to 13 bits of performance for larger signals (over ± 2.5 V). **Zeltex**, **Inc**, 940 Detroit Ave, Concord, CA 94518. Circle 225 on Inguiry Card

LED PC BOARD MOUNT

Inserting leads of a T-1 LED into the PCL 490 results in proper spacing for circuit board hole mating. In both vertical and horizontal mounting positions the unit provides the support and stability required for wave soldering operations. The mount has a specially designed lens which incorporates striated lines and fresnel rings resulting in a 125% increase in apparent brightness and viewing angle of 180°. Designed for front panel display use, the device eliminates hard wiring to the panel and allows lens to be flush mounted, recessed, or extended through panel for full visibility. Visual Communications Co, PO Box 986, El Segundo, CA 90245.

Circle 226 on Inquiry Card

Exclusive new Zenith CRT Display with L-Power for logic circuits means lower system cost.

This is no ordinary CRT Display. It also provides the power for your terminal logic circuits. This unique, scan-derived system replaces conventional power supplies, and results in CRT Display systems that are compact, uncomplicated, and have fewer parts. You get optimum reliability, a cooler-running terminal and lower system cost.

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thousands of hours, under extreme humidity, vibration, altitude, and temperature conditions. And exhaustive analyses of components and subassemblies, including electron microscope and thermograph scans in the Zenith Reliability Lab.

All Zenith CRT Displays: 5", 9", 12", and 15" are available with this innovative new L-Power system. For further information write: CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call (312) 773-0074.

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20-CHAR MATRIX PRINTER/PLOTTER

PRINTERS/PLOTTERS

12-Vdc DOT MATRIX PRINTER

SP-314 alphanumeric printer features 12-Vdc operation, allowing complete independence from power lines. Buffered 40-col impact printing, RS-232 serial and parallel inputs, crystal controlled baud rate, 96-char ASCII set plus double-width, and a self-test routine are standard. In addition, this unit includes graphic capabilities for special printer applications. Crystal controlled baud rate is jumper selectable for 110, 150, 300, 600, 1200, 2400, 4800, and 9600 baud. Physical dimensions are 8.5 x 5.75 x 8.5" deep (21.6 x 14.6 x 21.6 cm). Syntest Corp, 169 Millham St, Marlboro, MA 01752.

Circle 227 on Inquiry Card



Sprinter 20 provides up to 110 full 20-char lines/min utilizing a graphic 140 x n dot matrix, producing hard copy of a 280-line CRT display within 28 s. Users may choose parallel 7-bit ASCII or serial RS-232 with selectable baud rates from 110 to 9600. Print mode is twenty 5 x 7 dot matrix chars/line with 96 ASCII u/lc characters. Printer connects with TRS 80, Apple II, Atari 800, Commodore Pet, Mattel Intellevision, and other computers using std interfaces. **Alphacom, Inc,** 3031 Tisch Way, San Jose, CA 95128.

Circle 228 on Inquiry Card

ALPHANUMERIC DOT MATRIX PRINTERS

P2010 with RS-232-C interface and P2020 with IEEE 488 interface feature 2-color, 31-col printout with mixed char, 7 x 7 dot matrix char, and integral paper feed. P2010 interfaces with microcomputers, computer communications, and other 75- to 48-baud applications; P2020 couples with instrumentation, computer peripherals, and test equipment. Both print at 2.4 lines/s, have 7.2-lines/s paper feed at 6 lines/in (2.4/cm), printing 31 chars/line in black and red. Operating temp is 0 to 40 °C. Measurements are 11.2 x 4.3 x 7.9" (28.4 x 10.9 x 20.0 cm). Canon Business Machines, 3191 Red Hill Ave, Costa Mesa, CA 92626.



Circle 229 on Inquiry Card

LSI-11 SYSTEMS FROM ANDROMEDA Any size you want.



No matter what your LSI-11 system needs are, Andromeda can satisfy them.

For example, the 11/M1 system shown on the right weighs only 14 pounds yet contains 102kb of mini disk storage

(expandable to 389kb), 64kb of RAM, space for up to 16kb of EPROM, 4 serial ports, and the LSI-11/2 CPU. All of this for less than \$4000. While the 11/M1 will run the RT-11 operating system, it is best suited for dedicated applications where its small size but large processing power are needed.

Near the other end of the scale is the 11/H23-DDF system shown at the left. The mobile enclosure includes the LSI-11/23 processor, 256kb main memory, 10mb of storage on the double density RK-05 cartridge disk and 1.2mb on the double density floppy disks. This system also has 4 serial ports and 7 empty dual width slots for additional interfaces. The \$22,500 price includes the video terminal shown, a 150 CPS matrix printer, and the RT-11 operating system.

These are just two examples of the many LSI-11 based systems available from Andromeda. And the standard systems are just starting points; we will provide any combination of pack-



age, processor, memory, interfaces, and peripherals to meet your requirements. In addition to general purpose systems, we also have turnkey packages for word processing, time-sharing, data acquisition, and graphics.

We also provide individual boards, software and accessories to support LSI-11 systems.

LSI-11, RT-11, and RK-05 are trademarks of the Digital Equipment Corp.



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CUSTOM SWITCH PANELS (Unlimited colors and graphics)



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SNAP DOME SWITCHES (The Heart of all our Products)

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Another ISC breakthrough: Affordable dot addressable color graphics.



Introducing the world's lowest priced high resolution color graphics.

Now high prices don't have to keep you from high performance graphics. ISC's new 8000 Series "I" terminals and desktop computers display color vectors and arcs with full-screen, 480 x 384 individual dot precision — note the close-up photo above. Impressive? With terminals starting at a quantity 100 price of \$3,355, try incredible.

For any application requiring critical picture definition.

ISC's new "I" series is suited for process control, energy management, MIS –virtually any application needing sophisticated color graphics. Available in contemporary or industrial cabinets, each model features an 80 cpl by 48-line character format and RS-232C interface. Individual dots displayed in any of 8 colors can shade to a wide spectrum of color combinations.

ISC's "I" series desktop computers include File Control System Disk BASIC, 8K to 24K RAM, and 80K to 26-Megabyte disk. OEM prices start at \$4,635, quantity 100.

With ISC's new "I" series, you can now get dot addressable color graphics for a third less than anything else on the market. And we include the keyboard! See for yourself why ISC is the world's largest manufacturer of color graphics systems – call **800-241-4310** for the name of your nearest ISC rep.

Note to current 8001G users: You can easily add ISC's dot addressable option to your unit. This is the kind of upward compatible growth you can expect from ISC! Consult our customer service department for complete details.

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The new VISUAL 200 terminal has the features of competitive terminals and will codefor-code emulate them as well. A flick of a switch on the rear panel programs the VISUAL 200 for compatibility with a Hazeltine 1500, ADDS 520, Lear Siegler ADM-3A or DEC VT-52. This allows you to standardize on the new, reliable VISUAL 200 for virtually all of your TTY compatible video terminal applications, with no change in the software you've written for the older, less powerful terminals. And you're not limited to mere emulation; you can outperform them at the same time by taking advantage of the additional features and human engineering of the VISUAL 200. such as:

- Detachable Solid State Keyboard
- Smooth Scroll
- Tilt Screen (10° to 15°)
- Large 7 x 9 Dot Matrix Characters
- Others in the Feature Comparison Chart

For a pleasant surprise on prices, call or write us today.

FEATURE	Visual 200	Hazeltine 1500	Hazeltine 1420	Lear Siegler ADM-3A	Digital VT-52	ADDS 520	ADDS Regent 20	ADDS Regent 40
24 x 80 Screen Format	STD	STD	STD	STD	STD	STD	STD	STD
7 x 9 Dot Matrix	STD	STD	NO	NO	NO	NO	NO	NO
Background/Foreground	STD	STD	STD	NO	NO	NO	NO	STD
Insert/Delete Line	STD	ŞTD	NO	NO	NO	NO	NO	STD
Insert/Delete Character	STD	NO	NO	NO	NO	NO	NO	NO
Clear End Line/Field/Page	STD	STD	NO	NO	STD	NO	NO	NO
Blink	STD	NO	STD	NO	NO	NO	NO	STD
Security Mode	STD	NO	STD	NO	NO	NO	NO	STD
Columnar and Field Tab	STD	NO	STD	NO	NO	NO	NO	STD
Line Drawing	STD	NO	NO	NO	STD	NO	NO	STD
Upper/Lower Case	STD	STD	STD	OPT	STD	NO	STD	STD
Numeric Pad	STD	STD	STD	OPT	STD	NO	NO	STD
Composite Video	STD	NO	NO	NO	NO	STD	NO	NO
Current Loop	STD	STD	NO	OPT	OPT	STD	STD	STD
Serial Copy Port	STD	STD	OPT	STD	OPT	NO	STD	STD
Hold Screen	STD	NO	NO	NO	STD	NO	NO	NO
Detachable Keyboard	STD	NO	NO	NO	NO	NO	NO	NO
Solid State Keyboard	STD	NO	NO	NO	NO	NO	STD	STD
Typamatic Keys	STD	STD	STD	NO	NO	NO	STD	STD
Cursor Addressing	STD	STD	STD	STD	STD	STD	STD	STD
Read Cursor Address	STD	STD	STD	NO	NO	NO	NO	STD ·
Cursor Control Keys	STD	NO	STD	NO	STD	NO	NO	STD
Secondary Channel	STD	NO	NO	STD	NO	STD	NO	NO
Self Test	STD	NO	STD	NO	NO	NO	NO	STD
Baud Rate to 19,200	STD	STD	NO	STD	NO	NO	NO	NO
Smooth Scroll	STD	NO	NO	NO	NO	NO	NO	NO
Microprocessor	STD	STD	STD	NO	STD	NO	STD	STD
Tilt Screen	STD	NO	NO	NO	NO	NO	NO	NO
Switchable Emulations	STD	NO	NO	NO	NO	NO	NO	NO

FEATURE COMPARISON CHART

The new VISUAL 200 obsoletes competitive terminals without obsoleting the software.



Visual Technology Incorporated 540 Main Street, Tewksbury, MA 01876 Telephone (617) 851-5000

DATA ACQUISITION AND CONTROL

PROCESS CONTROLLER

Operating standalone or as a smart remote in data acquisition and/or supervisory control systems, Total Process Controller (TPC) 2000 supports 8 transient protected, multiplexed 12bit analog inputs (expandable to 64 single-ended, 32 differential); 3 optically isolated, hardware debounced 16-bit pulse accumulators; 16 optically isolated, hardware debounced digital inputs (expandable to 48); 16 30-V at 300-mA open collector outputs (expandable to 48); 4 Form c 10-A relay outputs; and one 8-bit analog output (expandable to eight 12-bit channels. Microprocessor based controller has a basic interpreter tailored to run directly on the unit that provides realtime 1/0 extensions, floating point arithmetic, logic functions, Y^X operations, and trig and log

functions. The unit has serial communications capability (RS-232-C compatible) to interact with std peripherals. In addition, it can host up to 24k of EPROM and 4k of RAM. **Advanced Logical Solutions**, 7074 Commerce Cir, Pleasanton, CA 94566.



Circle 230 on Inquiry Card

MODULAR DATA ACQUISITION SYSTEM



SDS500 series data acquisition and process control computers feature CRT with 16 x 32 chars and optional 256 x 256 pixels graphics, ac operation, and elaborate firmware and software. Systems utilize a 280 processor and a line of I/O interfaces, and are compatible with SDS1000 series. Units offer rugged metal construction and high emi and rfi immunity. **Sonotek Ltd**, 2410-5 Dunwin Dr, Mississauga, Ontario L5L 1J9, Canada. Circle 231 on Inquiry Card



MEMBRANE TOUCH SWITCH SYSTEM



Electronic Packaged System (EPS) provides fully integrated switch/control package to meet manufacturer's switch control requirements. Designated control and diagnostic functions can be designed into system for variety of end products. Polymer membrane touch-in-panel switch, singlechip microprocessor, and other components combine to form complete control system. **Oak Switch Systems, Inc,** 100 S Main St, Crystal Lake, IL 60014.

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Sequenced gold-plated pin connection permits module removal with the power on. Plug-in slots provide flexibility to interchange modules with no effect on field wiring. Color coded modules: white for input, red for output.

Universal panel or rack mounting 16-channel card cage takes only 5-1/4" rack space.

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mocouple inputs. Good

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tion to eliminate ground

loops and to save other

RFI immunity, plus

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Ribbon cable for front-ending popular analog I/O boards such as Intel/National 711/724/732

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The first easy-to-apply analog 1/0 boards such as Intel/Na-A/A signal conditioning system for real world analog inputs.

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mable controllers. Series 1800 conditioners accept low level analog signals such as mv, thermo-

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The 1800 system can be powered by any ± 15 v power supply and operates over a wide (0° to 70°C) ambient temperature range. Wide bandpass options available.

Call your Acromag representative for technical details on this new, low cost, computer-compatible system. Or write for Bulletin 8-180.0.

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POWER SUPPLIES & REGULATORS

150-W QUAD-OUTPUT SWITCHER

SHQ-150W provides 5-, 12-, and -12-V fixed outputs, plus a user-selectable fourth output (5, 12, 15, or

24 V). Features include a compact, fully enclosed package that provides safety and application convenience. The unit has 115/230-Vac input capability, and hold-up time rating of



bedded microformatter and interface to PDP-11/VAX, LSI-11, NOVA/ECLIPSE, RS-232, IEEE-488 or Dual Buffered I/O. \$6985-800 bpi/ NRZ or \$7885-NRZ/PE Dual Density in single unit quantity. Contact us today.



TDX PERIPHERALS Division of GAW Control Corp. 150 New York Avenue, Halesite, NY 11743 (516) 423-3232

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munity to ac line disturbances and brownouts. All outputs are fully regulated $(\pm 0.1\%)$, and internal emi/rfi filtering is included. **Power-One, Inc,** Power One Dr, Camarillo, CA 93010.

20 ms minimum, that provides im-



Circle 233 on Inquiry Card

50-W TRIPLE-OUTPUT SWITCHER

Series 3050 features models with 5 Vdc at 6 A and ±12 Vdc at 1 A or 5 Vdc at 6 A and ± 15 Vdc at 1 A. Basic specs include 80% efficiency, 90- to 130- or 180- to 260-Vac input voltage range, jumper selectable, 47 to 450-Hz input frequency range, 20-kHz internal clock oscillator, ±0.1% line and load regulation, and 50-mV pk-pk output noise. Response time is 300 µs to 1% for a 25% load change, and hold-up time is 16 ms. The unit provides 1500-Vac I/O isolation. Tempco is ±0.02%/°C. Output current limit and soft start are std on both models. No external heat sink is required. The entire supply is mounted on an FR4 grade PC board. All I/O connections are made through turret solder terminals. Schottky rectifiers minimize the voltage drop across the rectifiers to improve overall efficiency. MTBF per MIL-STD MIL-HDBK-217B is 40k hours minimum. Power General, 152 Will Dr, Canton, MA 02021.



Circle 235 on Inquiry Card

Multiwire Optimizes ECL.

These traces tell the story.



Wirewrapped and multilayer circuit boards can handle the high speeds of emitter-coupled logic. But Multiwire does it better. With Multiwire, *board impedance is precisely controlled* to meet circuit specs and is *consistent* from signal to signal and board to

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A typical example of the circuit density achievable with Multiwire circuit boards.

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Multiwire, 31 Sea Cliff Avenue, Glen Cove, NY 11542. Phone (516) 448-1307



*Multiwire is a U.S. registered trademark for the Kollmorgen Corporation discrete wired circuit boards

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With LSI 11/PDP 11 Software Compatible Disc/Tape Controllers Offering Single Board Low Power μP Based Design and Low Cost... Plus Many Other Good Reasons!

The reasons start with DILOG'S (Distributed Logic Corp's.) full time engineering and design staff. Not outside suppliers. That means when you contact DILOG for product selection or after sale service, you'll get "first hand" assistance...along with years of experience manufacturing μ P based controllers that interface with DEC 11 CPUs.

The intelligent products you'll discuss all utilize common proprietary architecture and DILOG automated design techniques—products with exceptional reliability and cost efficiency...mostly available from stock. And when you plug a DILOG controller into your DEC CPU it's ready-to-run because it's fully operating system software compatible.

These high performance data storage interface products also feature • minimum bus/space requirements • up to 60% less power • 10 to 50% lower cost • automatic self-test... and numerous other features for easy system integration.

Consult the DILOG/disc-tape compatibility table for your needs. Then ask for detailed data on existing, or future products from DILOG...#1 in single board DEC 11 compatible disc/tape controllers.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643, Phone: (714) 534-8950 • TELEX: 681 399 DILOG GGVE

MAGNETIC TAPE DISC 1/2" REEL-TO-REEL STD. & STREAMER CMD CARTRIDGE MODULE 2315/5440/RK05 CARTRIDGE CLASS WINCHESTER 51/4", 8" OR 14" SMD STORAGE MODULE AMPEX AMPEX AMPEX AMPEX BASF CIPHER CONTROL DATA CAELUS **CENTURY DATA** CONTROL DATA CONTROL DATA CENTURY DATA CONTROL DATA FUJITSU DIGI-DATA CONTROL DATA **BALL COMPUTER** KENNEDY KENNEDY DEC MITSUBISHI MEMOREX MICRODATA DIABLO PRIAM PERTEC IOMEC SHUGART TANDBERG DATA (IDT) MICRODATA SEAGATE WANGCO PERTEC QUANTUM WANGCO TDX IMI WESTERN DYNEX DRI

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NUMBER 1 FOR

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CAPACITIES 2.5 TO 300 MB



CIRCLE 155 ON INQUIRY CARD

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DISC/TAPE DRIVE MANUFACTURER COMPATIBILITY CHART

*Trademark Digital Equipment Corp.

POWER SOURCES AND REGULATORS

FLOPPY DISC SWITCHING POWER SUPPLY

EPS175-5-12-5 is designed for all 5.25" (13.34-cm) floppy discs that require 5 V at 0.5 A and 12 V at 1 A. Depending on power requirements, it can power up to 3 floppy discs. The 5-V at 20-A output is sufficient to independently power small to medium microprocessor systems. Dc output voltage is 5 V at 20 A; 12 V at 3 A; and 5 V at 1 A. All outputs are floating and have remote sensing. **Elpac Power Systems**, 3131 S Standard Ave, Santa Ana, CA 92705. Circle 236 on Inquiry Card

PRECISION REGULATED LINEAR POWER SUPPLIES

With voltage ranges from 5 to 28 Vdc and current up to 35 A, 40 single-, dual-, and triple-output modules range in efficiency from 52% to 66% over load and line variation. The IC regulation circuit (0.05% accuracy) is encapsulated in thermal epoxy for environmental protection and stability. Std features include universal input 115/230 ±10 Vac, 47 to 440 Hz; adjustable OVP on all 5-V models; remote sensing on each output; fully adjustable foldback current limiting; ±5% voltage adjust; industry standard case sizes; and 2-yr warranty. Motion Products Corp, 10474 Plano Rd, Dallas, TX 75238.



Circle 237 on Inquiry Card

MULTI-OUTPUT OPEN FRAME SWITCHER



Model MDS-75 is designed with factory adjustment that allows selection of output voltages within the 75-W continuous power range. The unit accepts 115/230 Vac ±20%, 47 to 63 Hz, and provides outputs of 5 Vdc at 1.6 to 8 A, 12 Vdc at 0.5 to 2.6 A (3.3 A pk), and -12 Vdc at 0.06 to 0.3 A, 12 Vdc at 0.2 to 1 A. Line regulation is 0.2% with all outputs at 50% load; load regulation on 5-V outputs is 0.3%, 20% to 100% load; 5% on ±12-V outputs at 20% to 100% load. Condor, Inc, 4880 Adohr Lane, Camarillo, CA 93010. Circle 238 on Inquiry Card

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For more information: Dr. Linda Leffel, Center for Continuing Education, Virginia Tech, Blacksburg, VA 24061. (703) 961-5241.





DATA TERMINALS AND DISPLAYS

CRT DATA TERMINAL



TDV 2200 has a 15" (38-cm) tube that displays 0.175" (0.444-cm) capital letters to ensure readability and make reading distance less critical. The EQUILITETM video system displays both horizontal and vertical lines with the same intensity, making the text easy to read. A light-colored background is used for text on the screen to obtain a correct relationship between light output from the CRT and from other environmental elements, such as reflections. The intensity control affects both text and background light, rendering optimal contrast under all lighting conditions. Problems of reflection from the surface of the tube are solved by use of an anti-reflex tube, and a tilt and swivel mechanism used in combination with the effects of the background light. Tandberg Data, The Export Council of Norway, 800 Third Ave, New York, NY 10022. Circle 239 on Inquiry Card

HIGH RESOLUTION GRAPHICS MONITOR

Model 1275 uses a 19" wide x 15" high (48 x 38-cm) CRT that can write a high resolution line at a brightness of 40 ft-L (137 cd/m²) at 0.5" / μ s. In an ambient light of 40 ft-L, contrast ratio is 8 to 1 or better, which allows a graphics system to work with 6 different line intensities (shades of gray). Bandwidth of the magnetic deflection system is 3 MHz. At a typical refresh rate of 60 Hz, the unit can put up 66 lines or 100 characters each. **Orwin Associates**, 35 St Nicolas Ave, Lake Grove, NY 11755.

Circle 240 on Inquiry Card

STRIP CHART RECORDER SIMULATOR

Eight-color recorder simulator package for IDT-2000 color graphics terminal permits rapid, multicolor visual presentation for comparison/correlation of many variables. Package displays more than 1000 points/s in either a horizontal or vertical plane on the high resolution 512 x 512 terminal display. **Industrial Data Terminals Corp**, 1550 W Henderson Rd, Columbia, OH 43220. Circle 241 on Inguiry Card

BUFFER ENHANCEMENT FOR TELEPRINTER TERMINAL

Telexbuffer-43 provides internal buffer and offline editing, giving Teletype 43 terminal users improved performance, quality, and reliability. It can dial a number from its directory of frequently used numbers and automatically redial without operator assistance until message is transmitted. System uses EAROM to set options unique to the user without equipment modification. Memory sizes range from 2k to 16k chars. **Edge Technology**, 2735 SE Raymond, Portland, OR 97202. Circle 242 on Inquiry Card

COMPACT KEYBOARD/DISPLAY TERMINAL



TransTerm utilizes 64-char 5 x 7 dot matrix LCD organized in 32-char lines to display the std 96-char ASCII complement, and communicates in full duplex RS-232 serial asynchronous ASCII. 20-mA current loop and RS-422 are options. Switch selectable baud rates of 300, 1200, 2400, and 9600 are available. Terminal measures 11.7 x 6.9 x 1.75" (29.7 x 17.5 x 4.44 cm) and consumes 10 W of power via 115-Vac wall plug-in transformer. **Computerwise, Inc,** 4006 E 137th Terr, Grandview, MO 64030.

Circle 243 on Inquiry Card

DATA TERMINAL



Microprocessor controlled VP-3301 interactive terminal provides color graphics, reverse video, programmable and resident character sets, selectable baud rates and data formats, and flexible membrane keyboard. Char display format, 40 char x 24 lines or 20 char x 12 lines is software selectable. Individual or all char may be displayed in 1 of 8 colors or gray scales on B/W monitor. Communications interface is asynchronous RS-232-C or 20-mA current loop. CMOS circuitry makes unit suitable for use in hostile environments. RCA MicroComputer Products, New Holland Ave, Lancaster, PA 17604. Circle 244 on Inquiry Card

DISPLAY SYSTEM ENHANCEMENTS

Host monitoring aids, including online indicator, response time measurement, line trace, and disclose mode have been added to model 310 remote display system. Enhancements for model 320 local display system include response time measurement, channel trace, and disclose mode. Aids can be used for problem determination, application development and testing, and monitoring system performance. Lee Data Corp, 10206 Crosstown Cir, Minneapolis, MN 55344. Circle 245 on Inguiry Card

CRT DISPLAY TERMINAL

'Log 53 offers complete emulation of and keyboard and software compatibility with Data General's model 6053 CRT display terminal. Keyboard contains the full complement of 15 function keys that perform all 60 function sequences of higher level Data General terminals. Features include 1920-char (80 x 24) display and serial printer port with EIA RS-232-C interface. Terminal measures 13.25 x 16.25 x 20.25" (33.65 x 41.27 x 51.43 cm) and weighs 30.0 lb (13.5 kg). Emulog, Inc, 3730 Yale Way, Fremont, CA 94538. Circle 246 on Inquiry Card

Our new 208 A/B is adaptable to dial-up or dedicated. What's your line?

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CIRCLE 158 ON INQUIRY CARD

COMPUTERS AND COMPUTER SYSTEMS

INTERRUPT DRIVEN **INDUSTRIAL CONTROL COMPUTER**

Interrupt driven CINCHTM microprocessor based control computer provides fast response to realtime process requirements, operator terminals,

other CINCH units, and supervisory computers. Added CINCH-BASIC language capabilities include high speed PID and T/C linearization. A powerful editor simplifies programming in CINCH-BASIC. In addition, experienced programmers can add assembly routines directly to the language. Control Logic, Inc, 9 Tech Circle, Natick, MA 01760. Circle 247 on Inquiry Card



IMAGE FRAME BUFFER SYSTEM



Modular high resolution GMR 260 series systems feature a 1024 x 1024 resolution and image memory capacities up to 24 bits. Complete line drawing vector graphics and alphanumerics are provided. Additional std features include image pan and zoom, intensity transformations, and pseudocolor assignment. All models are complete systems with 16-bit parallel, TTL compatible, bidirectional interface. Plug compatible, DMA parallel interfaces are available for most minicomputers. Video output is RS-343 compatible and drives std high resolution TV monitors. Systems are housed in std rackmount chassis. Grinnell Systems, 2159 Bering Dr, San Jose, CA 95131. Circle 248 on Inquiry Card

SPEECH/DATA PROCESSOR

Model 6860 provides simultaneous quality voice and 1200-baud data transmission over a 4-wire tie line, offering users significant savings in communications line costs. A voice and data link between remote video display terminals-such as at a district or subsidiary office-and central computer is a typical application. Voice conversation may be conducted point to point or PABX to PABX, in which case any extension phone at one location may call any extension phone at the second. Providing a voice circuit with quality equal to, or better than, conventional low pass circuits with bandwidths of 2200 to 2400 Hz, the device also provides a 1200-baud data channel on the same communication line. The speech processor portion of the system uses a voice compandor to provide a low noise circuit, and includes E&M signaling to interface with PABX or PBX. Modem portion features data distortion of less than 1%, a modem loopback switch, and LED display of digital functions. The digital interface is EIA RS-232-C or CCITT V.24 through 25-pin connectors. By avoiding digital techniques such as those used in vocoders, the unit avoids the synthetic sound which often fails to identify the speaker. RFL Industries, Inc, Powerville Rd, Boonton, NJ 07005.

requires the reading of punched cards, mark sense cards, badges, or special forms, start with these capabilities:

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Circle 249 on Inquiry Card

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CIRCLE 160 ON INQUIRY CARD

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INPUT/OUTPUT DEVICES

GRAPHICS GENERATOR WITH REALTIME VIDEO DIGITIZER

Using onboard high speed microprocessor and fast dual-port 307k-bit image memory, model 2000 digitizes, stores, and displays live video pictures or scenes in 0.017 s; 4 independent graphics displays can be driven simultaneously. Features include 320 x 240 x 4 pixel matrix, high speed random pixel access, block fill, vector generation, multifont character generation, and DMA block transfers. Unit is contained on 15 x 15" (38 x 38-cm) PC card, and plugs into any Data General microcomputer. Software is supplied and runs under RDOS or AOS. Octek Inc, 7 Corporate PI, S Bedford St, Boston, MA 01803. Circle 250 on Inquiry Card

OPTICAL BAR CODE INPUT TERMINAL

6028 terminal, with alphanumeric keyboard and lightpen, allows manual and automatic entry of bar coded information. Built-in microprocessor intelligence permits buffered storage of up to 1k chars; 32-char dot matrix blue-green display provides high visibility. Resolution is available to 0.007" (0.178 mm), with accuracy greater than 99%. Versions are available for hostile environments. **Identicon Corp**, One Kenwood Cir, Franklin, MA 02038.



Circle 251 on Inquiry Card

LIGHTPEN



Featuring high emi immunity, LTP 105 A uses optical switching to eliminate mechanical contact bounce, and is activated by depressing push tip against CRT screen. Pen provides max scan rate responses up to 5000 cm/ms; light spot size is 0.010" (0.025 cm), and optical field of view is 0.080 to 0.160" (0.203 to 0.406 cm). Power required is 5 Vdc. LTP 105 B for graphics applications features optical push switch on barrel that can be activated up to 6" (15 cm) from CRT. **Ampower Instrument Co, Inc,** 26 Just Rd, Fairfield, NJ 07006.

Circle 252 on Inquiry Card



INFOSCRIBE 1000.

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It's a Giant Step

And now the INFOSCRIBE 1000: a smarter, faster serial matrix printer with a host of features system designers crave but seldom get at a price they like. Plus the bonus of complete compatibility with its sister printer, the INFOSCRIBE 500.

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INFOSCRIBE 1000 uses a closed loop servo for precision head positioning and quieter operation. Throughput is significantly increased by vertical and horizontal tabbing, two-way logic seeking, and a printhead that cruises at 180 cps. Good vertical and horizontal resolution lets you print a broad range of graphics. And the ability to download character sets from the host CPU offers all kinds of versatility.

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Thanks to its elegant design and genuine craftsmanship, **INFOSCRIBE** 1000 prints almost ad infinitum. It's built for simple, straightforward

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Distributor/Representative inquiries welcome, too.

INFOSCRIBE

Handing You a Line CIRCLE 164 ON INQUIRY CARD

TEST AND MEASUREMENT BENCHTOP LINEAR TEST SYSTEM



Benchtop system tests op amps, ADCS, DACS, regulators, and other linear devices and has production tester capabilities. LTS 2010 is programmable in BASIC and offers performance comparable with large, centralized test systems. Intended for decentralized production testing, the unit can also be programmed for simple go/no-go testing at incoming inspection or engineering component characterization. Typ test times are 800 ns for op amps and 5 s for DACs. Test capabilities range from a 15-A pulse for regulator testing to femtoamp level leakage current detection for precision op amp testing. The unit tests DACs of up to 16 bits of resolution and $\pm 0.01\%$ accuracy. Std features include data logging, statistical analysis, yield analysis, fill in the blanks programming capability, automatic handler interface, IEEE interface, and uni- and bidirectional RS-232 interfaces. **Analog Devices, Inc, Component Test Systems Div**, 10 Corporate PI, Burlington, MA 01803. Circle 265 on Inquiry Card

FLOPPY DISC DRIVE EXERCISER

Useful for routine maintenance of both std and mini-floppy disc drives, model 103B can be used to check out and repair floppy disc drives in a costeffective manner. In addition to features of its predecessor, the 103, the unit provides switch-selectable step rates of nominally 3, 10, and 40 ms; compatibility with any drive using Shugart or ANSI X3T9 interface, and 18-ms seek settle time delay on direction change. Low write current interface line is provided on 8" (38-cm) drive interface, and unit can automatically perform alternate seeks between any 2 track addresses. Two interface connectors are provided: 34-pin for mini-floppy drives and 50-pin for 8" drives. The unit uses power from the drive under test. Interface cables are optional; power cables are included with interface cables. The unit can write a pattern of all 1s or 0s from index to index, for single- or double-density drives. Surface select for double-sided drives is provided. **Ava Instrumentation, Inc,** 9672 Manzanita Ave, Ben Lomond, CA 95005.



Circle 266 on Inquiry Card



CIRCLE 165 ON INQUIRY CARD

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(Nobody knows more about Colorgraphics)

Get the most out of your computer graphics with a monitor from Ramtek.

Choose the right monitor for you from our complete line of more than forty models—13 to 25 inches, color or monochrome, cabinet or rackmount.

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CIRCLE 167 ON INQUIRY CARD

MEMORIES

RUGGEDIZED WINCHESTER DISC SYSTEM



Available in 10M- or 20M-byte capacities, the 9800R comes complete with 8" (38-cm) Winchester drive, embedded controller, and power supply (all shock mounted) plus a CPU interface card. Designed for use in data gathering and process control, the system can travel over rough terrain to location, where it monitors data as received, eliminating the expensive repeats associated with tape storage. Unformatted capacities of 10M or 20M bytes can be expanded with additional systems. Each system includes shock mounted 8" (38-cm) disc and switching power supply packaged in a 7.25" (18.42-cm) high RETMA enclosure. Specified to take 5Gs on all axes (nonoperating) and 2Gs (error free, operating), the drive has been tested to MIL-STD 810C (Curve B,AR). An embedded z80 based controller, plus minicomputer interface and cabling are provided. To operate, the user simply installs an appropriate interface board into the computer and attaches the system. **Dataflux Corp**, 1050 Stewart Dr, Sunnyvale, CA 94086.

Circle 253 on Inquiry Card

1M-BYTE SEMICONDUCTOR STORAGE MODULE

Available in 256k-, 512k-, and 1024k-byte capacities, MaxiRam module has a read cycle time of 550 ns, write cycle time of 750 ns, and max access time of 474 ns. Error correcting circuitry enables single-bit errors to be corrected and double-bit errors to be detected. Ouside edge of the assembly contains an LED display enabling faulty RAMs to be identified down to the replaceable chip level. Both core and semiconductor modules are compatible and can be mixed within the same system. **Imperial Technology, Inc,** 831 S Douglas St, El Segundo, CA 90245. Circle 254 on Inquiry Card

FIXED HEAD DISC FOR H 316 COMPUTERS

Megastore 316 electronic nonvolatile disc replacement is available in 0.5M-and 1M-byte capacities and operates through direct multiplex control or as a program I/O device. 0.5M-byte unit protects 64 tracks in 4-track increments; 1M-byte unit protects 128 tracks in 8-track increments. It is offered complete with controller, power supply, and interconnecting cables in 7" (18-cm) high std 19" (48-cm) rack mounted chassis and provides transfer rates of 19 to 297 kHz. **Ampex Corp**, 200 N Nash St, El Segundo, CA 90245. Circle 255 on Inquiry Card



Now, Racal-Vadic has invisible dual and triple modems.

Model 785

Racal-Vadic Custom Modem Board

They're packaged inside TEXAS INSTRUMENTS' Silent 700* 780 Series Data Terminals.

n the beginning... When Texas Instruments designed the 780 Series of 120 character-per-second data terminals, Racal-Vadic was asked to solve a difficult engineering and packaging problem.

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> *Trademark of Texas Instruments CIRCLE 175 ON INQUIRY CARD

The new Spectra-Strip 817 is the IDC D-subminiature connector for those of you who've become disenchanted with D-Sub's.

With our D-Sub, you can mass terminate your flat cables without separating each and every strand. Without stocking up on weird-pitched cable. Without a mechanical kluge tacked onto the back of the connector to go from .054-pitch pins to .050-pitch cable.

It terminates our Twist 'N' Flat,[®] 3C[™] Color Coded and that great old standby Spectra-Zip[™] with no fuss, no hassle.

And only the 817 comes with a metal shell so that it's *fully* intermateable and intermountable with any of the other real D-sub's.

If that sounds like the way to build a D-Sub, call your nearest Spectra-Strip distributor. He can also tell you about what we've got for you in our other IDC connectors, flat cable and assemblies.

They're simply superb.



When you're down to the wire.

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SUBASSEMBLIES

DUAL-VOLTAGE AXIAL COOLING FAN



Fans operate at 60 and 50 Hz, 120 and 240 V, and are available in 3 designs for mounting on 4.1 or 3.1" (10.4- or 7.9-cm) centers. Units feature open frame design, patented Recirk bearing lubrication system, and corrosion inhibitor coating on metal parts. **Gould Inc**, Electric Motor Div, 1831 Chestnut St, St Louis, MO 63166.

Circle 256 on Inquiry Card

PRECISION TIMING STEP MOTORS

High torque to inertia ratio motors are offered in sizes with 19, 23, 28, to 46 oz-in (0.133, 0.161, 0.196 to 0.322 N·m) of torque and up to 5000 PPS. Packages allow for sleeve, roller, and ball bearing configurations, and are available with several voltages, stepping angles, lead positionings, and shaft and mounting configurations. Motors can be fitted with gear boxes if desired. IMC Magnetic Corp, Sub of Hansen Manufacturing Co, Inc, Princeton, IN 47670.

Circle 257 on Inquiry Card

SYNCHRO/RESOLVER SIMULATOR

Model 5310, used as benchtop simulator via front panel controls or as programmable device for ATE systems under computer control, features full remote programmability for line to line level, reference levels, synchro or resolver mode, and output angle. Remote control is user selectable parallel BCD or binary (18-bit) busable 3-state. Unit measures 9.5 x 3.5 x 14.1" (24.1 x 8.9 x 35.8 cm). North Atlantic Industries, Inc, 60 Plant Ave, Hauppauge, NY 11787. Circle 258 on Inguiry Card

15-BIT A-D CONVERTER

A true 15-bit A-D converter that converts in only 2 μ s, the 1215H is available as an A-D converter on a PC card or in a fully integrated data acquisition system with sample/holds and multiplexers. Features of the unit include accuracy of $\pm 0.0065\%$, input impedance of 10 M Ω , and tempco of 10 ppm/°C. Analog input range is $\pm 10, \pm 10.24$ V, and power requirements are $\pm 15, \pm 5$ V. Package size is 5.5 x 4.5 x 0.5" (13.9 x 11.4 x 1.27 cm). Phoenix Data, Inc, 3384 W Osborn Rd, Phoenix, AZ 85017. Circle 259 on Inquiry Card

BRUSHLESS DC MOTOR



Made in 1 to 6" (2.5 to 15.2-cm) diameters, motors use 3, 4, or 6 switching transistors; switching system is a Hall effect generator that replaces commutator and brushes. Units are available with or without electronic drive circuits: electronics are packaged either internally or separately from motor housing. Motors feature outputs from subfractional to 1 hp, low input power, ball bearing construction, high r/min, low audible and magnetic noise levels, and low weight/hp ratio. Eastern Air Devices, 1 Progress Dr, Dover, NH 03820. Circle 260 on Inquiry Card

LOW PROFILE 14-BIT D-R CONVERTER

MDRC accepts 14-bit digital angle input and a reference excitation and outputs 6.81-V rms sine and cosine. Output is short-circuit proof and fully protected to prevent converter damage. Modules operate from ±15- and ±5-Vdc power sources and meet MIL-STD-202E requirements. Dimensions are $3.125 \times 2.625 \times 0.43''$ (7.937 x 6.667×1.09 cm). Units are available for operation at 55 to 105 °C and at 0 to 70 °C. ILC **Data Device Corp**, 105 Wilbur PI, Bohemia, NY 11716. Circle 261 on Inquiry Card

LINE PRINTER INTERFACE

ZBX-349 allows SBC-80/10B, SBC-80/24, or ZX-80/05 users to run a Centronics line printer by simply plugging in the module. The module plugs directly to the SBX connector and bolts down to the card with nylon hardware. Cable is 8' (2.4-m) long and connects at one end to a 50-pin edge on the module; the other end plugs directly into the parallel connector on a Centronics line printer. Software protocol is as simple as reading in a port and testing for busy bit false. **Zendex Corp**, 6680 Sierra Lane, Dublin, CA 94566. Circle 262 on Inquiry Card

HIGH RELIABILITY DC-DC CONVERTERS

Y-95 series, with output voltage ranges from 2.8 to 250 Vdc and 100 W, meets 30k hours MTBF at stress levels of 95 °C base temperature, and has 25-kHz switching frequency to ensure 80% max efficiency. Line regulation is $\pm 0.1\%$, 5 mV; rms ripple is 0.2%, 10 mV; op temp is -55 to 95 °C; and source voltage range is 21 to 30 Vdc. **Technipower Inc, A Penril Co,** PO Box 222, Danbury, CT 06810. Circle 263 on Inquiry Card

BRUSHLESS DC COOLING FANS



Muffin fans, available in 6 models, operate on 12, 24, or 48 Vdc and offer greater air volume than conventional ac fans while reducing power consumption. Brushless design minimizes emi and rfi in critical installations. Construction features all metal venturi, thermoplastic propeller, permanently lubricated stainless steel ball bearings, and solid state motor. EG & G Rotron, Commercial Cooling Products Group, Shokan, NY 12481. Circle 264 on Inquiry Card





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LITERATURE

Supplies and Accessories

Brochure describes products that support company computer equipment, including magnetic media disc packs, cartridges, diskettes, and tape, in addition to printer and terminal supplies. Data General Corp, Westboro, Mass. Circle 281 on Inquiry Card

Pascal Instruction

Folder describes 3-part videotape course covering beginning, intermediate, and advanced levels; each part consists of ten half-hour lectures. Colorado State University, Fort Collins, Colo,

Circle 282 on Inquiry Card

Modems/Multiplexers

Bulletin describes private line and direct distance dialing modems, statistical and time division multiplexers, telephones, modem switching device, and diagnostic equipment. Rixon Inc, Silver Spring, Md.

Circle 283 on Inquiry Card

Power Supplies

Illustrated brochure features specs. dimensional drawings, voltage/current ratings, and accessories for single-, dual-, triple-, and quad-output switchers. Deltron Inc, North Wales, Pa.

Circle 284 on Inquiry Card

Intelligent Switching System

Illustrated booklet describes Dataswitch[™] multichannel onsite communications networks; diagrams, software configurations, operator language and control, in addition to functional and physical descriptions of modular components, are presented. Develcon Electronics Inc, Doylestown, Pa.

Circle 285 on Inquiry Card

High Resolution Data Converters

Brochure profiles A-D, D-A, and voltage to frequency converters, as well as sample-hold amplifiers, supplying specs, applications, and selection criteria. Analog Devices, Norwood, Mass.

Circle 286 on Inquiry Card

Electromechanical Relays

Featured in catalog are subminiature and miniature relays, detailed by graphs of operating ranges, life and performance curves, and time values, in addition to wiring diagrams, drill plans, and specs. ITT Components, North Andover, Mass. Circle 287 on Inquiry Card

Distributed Process I/O Controller

Illustrated data sheet profiles controller, listing interface options. Computer Products, Inc, Fort Lauderdale, Fla.

Circle 288 on Inquiry Card

Digital ICs

Product guide describing COS/CMOS circuits illustrates a broad range of small, medium, and large scale functions; diagrams, specs, and selection charts are included. RCA Solid State Div, Somerville, NJ. Circle 289 on Inquiry Card

EMI/RFI Suppression Filters

Brochure furnishes specs, differential mode/common mode attenuation vs frequency graphs, dimensional drawings, and product selection chart. Siemens Corp, Iselin, NJ. Circle 290 on Inquiry Card

Data Communications

Short form catalog describes range of microcomputer products that address problems of line costs, transmission errors, and computer port utilization. Micom Systems, Inc, Chatsworth, Calif.

Circle 291 on Inquiry Card

Bare Board Test System

Brochure features N221 automatic test system, outlining hardware elements, architecture, and operation. Teradyne, Inc, Boston, Mass. Circle 292 on Inquiry Card

Process Microcomputer

CHAMELEON TM is presented in brochure that describes features and applications of user programmable device. Fischer & Porter Co, Warminster, Pa. Circle 293 on Inquiry Card

Implantable Energy Sources

Catalog contains discharge performance graphs, cross-sectional and dimensional drawings, specs, and applications information for battery models BCX72, CSC93, and CSC150. Electrochem Industries, Inc, Clarence, NY. Circle 294 on Inquiry Card

64-Bit Array Processors

Brochure and spec sheet present cost/ performance advantages of transferring high precision complex arithmetic from mainframes to minicomputers. CSPI Inc, Billerica, Mass. Circle 295 on Inquiry Card

Militarized Cartridge Recorder

Nine-track read/write ECR-10 is described in data sheet containing performance, environmental, and electrical/mechanical specs as well as mounting dimensions. Genisco Technology Systems Div, Rancho Dominguez, Calif. Circle 296 on Inquiry Card

Interactive Graphics Systems Architecture

Brochure focuses on rapid changes in technology and economics of minicomputers, microprocessors, RAM, and raster scan displays, relating these developments to advances in graphic system design. Lexidata Corp, Billerica, Mass. Circle 297 on Inquiry Card

Standard Keyboards

Bulletin provides data about models 753, 756, and 771, in addition to information about 10- to 98-key models: educational, industrial, and military applications are described. George Risk Industries, Inc, Kimball, Neb. Circle 298 on Inquiry Card

Battery Specification

Handbook contains commercial specs and discusses battery applications; charts and tables set forth rating curves, discharge load profiles, charging methods, and recharging characteristics. Ratelco, Inc, Seattle, Wash.

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OEM MODEMS AND COUPLERS Multi-Tech's OEM 300 bps modems are available in FCC-Direct Connect and/or acoustic-coupled configurations, in standard or custom sizes. Also available are 1200 bps modems, with 202 or 212A-compatibility. We would like to discuss your application with you. Contact Mr. Jan Hubbard, **MULTI-TECH SYSTEMS, INC.**, 82 Second Avenue S.E., New Brighton, MN 55112. (612) 631-3550. **CIRCLE 580**



BOARD LEVEL TINY BASIC MICROCOMPUTER

K-8073 with on-chip Tiny BASIC microinterpreter, eliminates machine language programming, provides cost effective Industrial Control and drastically reduces New Product Development Time. $4\frac{1}{2}$ " × $6\frac{1}{2}$ " board supports 1K Local RAM (expandable to 8k), 2K ROM Utility Firmware, 8K EPROM, EPROM Programmer, R.T. Clock, Cassette Tape I/O, RS-232, STD (MOD) Bus Structure, 2 Sense Interrupts, ART/RC (single wire PCM Remote Controller), PPI (24 Bi-Directional I/O's), and Multi-Tasking. 5 Volt operation. \$388. **TRANSWAVE CORPORATION**, Vanderbilt, PA 15486. (412) 628-6370. **CIRCLE 581**

AMPEX MAKES PDP 11/34 OUTPERFORM PDP 11/70

That's what happened at San Francisco General Hospital Medical Center. With the addition of Ampex Megastore to a PDP 11/34, processing time was reduced by more than 1/3 of the time previously required.

For more information about how you can put Megastore to work performing for your system, call Cal Goshi at 213/640-0150. Or write Ampex Corporation, Memory Products Division, 200 North Nash Street, El Segundo, CA 90245. CIRCLE 577

AMPEX

MAKES THE DIFFERENCE.

COMPUTER DESIGN

ABLE COMPUTER CAN MAKE YOUR UNIBUS SYSTEM RUN BETTER THAN EVER



ABLE DH/DMTM (16-LINE COMBINATION DH11 & DM11 REPLACEMENT)

INSTALLS IN: UNIBUS systems...1 hex SPC slot. DATA RATES: 14 standard rates plus 19.2K baud and a user programmable rate. PROCESSING ADVANTAGES: Word transfer (in lieu of byte DMA) cuts bus time in half. OPERATING MODES: Full duplex with modem control. IMPLEMENTATION ADVANTAGES: On-board self-test/display. One bus load. **ABLE COMPUTER**, 1751 Langley Ave., Irvine, CA 92314 (714) 970 2020

CA 92714. (714) 979-7030. CIRCLE 582



hanneasa

QUADRASYNC/CTM (4-LINE DL11 REPLACEMENT/CL)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. DATA RATES: 7 independently selectable baud rates for each of 4 channels (150-9600). ELEC-TRICAL: 20MA current loop (Send : Receive). VECTOR/ADDRESS SELECTION: Vector and address values to be set on boundaries of 00₈ or 40₈. 16 continuous word address for Vector or Address.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 561



ABLE DV/16 (16-LINE DV11 REPLACEMENT) INSTALLS IN: All PDP-11's; in less than one half the space of DV11. DATA RATES: 16-line throughput of up to 30,000 char/sec (19.2K baud full duplex for each line) total. PROCESSING ADVANTAGE: Word transfers (in lieu of byte DMA) permit user to operate within one half the DV11 bandwidth for data transfers. OPERATING ADVANTAGE: User may mix sync and async lines in combinations of 4 or 8 lines.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 564



QUADRASYNC/ETM (4-LINE DL11-E REPLACEMENT)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. DATA RATES: 7 independently selectable baud rates for each of 4 channels (150-9600). ELEC-TRICAL: EIA standard RS232C – with modem control. VECTOR/ADDRESS SELECTION: 16 continuous word address for Vector or Address – starting values selected on any boundary.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 562



ABLE DZ/16 (16-LINE DZ11-E REPLACE-MENT)

INSTALLS IN: All PDP-11's in any standard hexwidth SPC slot; takes half the space at half the bus loading imposed by the DZ11-E. DATA RATES: All 15 standard DZ11 baud rates (50-9600). IMPLEMENTATION AD-VANTAGES: On-board pencil switches allow address and vector selection flexibility without the need for jumpers. Data format is program-selectable for each channel.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 565 ABLE GENERAL PURPOSE PRODUCTS



QUADRASYNC/BTM (4-LINE DL11 REPLACEMENT/EIA)

INSTALLS IN: All PDP-11's; 4 lines per SPC slot at one unit load to Unibus. DATA RATES: 7 independently selectable baud rates for each of 4 channels (150-9600). ELEC-TRICAL: EIA standard RS232C (Modem control not supported). VECTOR/ADDRESS SELECTION: Vector and address values to be set on boundaries of 00g or 40g. 16 continuous word address for Vector or Address. **ABLE COMPUTER**, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 583



QUADRACALL[™] (4-LINE DN11 REPLACE-MENT)

INSTALLS IN: All PDP-11's; 4-lines per SPC slot at one unit load to Unibus. PERFOR-MANCE: Interfaces up to 4 Bell 801 ACU's. INPUT/OUTPUT: 5-input signals from ACU are handled by EIA RS232 receivers 6-output signals are transmitted using EIA RS232 drivers. VECTOR/ADDRESS SELECTION: Allows selection of device address and vector by use of pencil switches.

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ONIVERTERTM (O-BUS TO UNIBUS CON-VERTER OR UNIBUS TO O-BUS CONVERTER) INSTALLS IN: LSI-11, LSI-11/23, PDP-11/03 and PDP-11/23 via quad-width card. AP-PLICATIONS: Allows Unibus-compatible controllers and memories to be used with LSI computer systems, or LSI-based peripherals to be used with PDP-11 computer systems. FEATURES: Supports features of LSI-11/23 including the full 128K address capability. **ABLE COMPUTER**, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. **CIRCLE 566**
COMPUTER DESIGN

REBUSTM (BUS REPEATER-DB11 REPLACE-MENT

INSTALLS IN: All PDP-11's; without using any additional backplane space. MECHANICAL: One dual-width card plugs into the same pair of connectors as the Unibus extension cable. COMPATIBILITY: Allows for 18 additional bus loads. Requires no software changes. Bus cycle time unaffected for devices on CPU side of REBUS — increased by 250 nsec max. for devices on outboard side. ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 567



usidim

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BUSLINK/UNI, LSI OR U TO Q (CPU TO CPU LINK)

INSTALLS IN: All PDP-11's and/or LSI-11's via pairs of hex-width, hex/quad-width, or quad-width cards and supplied cables. AP-PLICATIONS: Provides full DA11-B (Unibus or Q-bus link) compatibility on single cards. BUSLINK operates at DA11-B transfer rates over distances of up to 50 feet.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 570





CACHE/434TM (4K WORD CACHE MEMORY) INSTALLS IN: PDP-11/34 and -11/34A without using any additional backplane space! CAPACITY: 8192 byte (4K word). ENHANCE-MENT FACTOR: Run time reductions to 40% (70% speed improvement) are achievable. CACHE PARITY: Automatically goes off-line in event of any data or address error. RANGE SELECTION: User may optimize hit ratio by upper/lower switch settings. Cache action monitor indicates hit range.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 573



DUAL I/O[™] (GENERAL INTERFACE-DR11-C REPLACEMENT)

INSTALLS IN: All PDP-11's; in any SPC slot via quad-width card. APPLICATION: Dual I/O is equivalent to two (2) DR11-C's. OPERATING ADVANTAGE: Provides user the hardware/software equal to a dual DR11-C in one-half the space and one-half the bus loading of DR11-C's.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 568



SCAT/45TM (ADD-IN FASTBUS MEMORY) INSTALLS IN: PDP-11/45, -11/50 and -11/55. EXPANDS IN: 32K word increments/board. One-half of the available Fastbus space will accept full 124K word complement. ADDRESSES ON: Any 4096 word boundary across entire 124K word range. User has full memory complement at 330 nsec cycle-time memory instead of 32K word limitation imposed by the computer manufacturer.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 571



EMULOADERTM (ODT/BOOTSTRAP LOADER REPLACEMENT)

INSTALLS IN: PDP-11/05, -11/10, -11/35, -11/40, -11/45, -11/50 and -11/55. MECHANICAL: Dual width card replaces standard Unibus termination; requires no additional backplane space. OPERATING ADVAN-TAGE: Provides fixed console emulator (ODT) and bootstrap loaders for DL11, PC11, RF11, RK06, RK11, RP04/05/06, RP11, RS03/04, RX11, TC11, TM11 and TU16.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 574



INTERLINK/UNI (DR11-B AND ½ DA11-B REPLACEMENT)

INSTALLS IN: All PDP-11's in any SPC slot via hexwidth card. APPLICATIONS: Provides full DR11-B (DMA INTERFACE) and one side of DA11-B (UNIBUS LINK) capability on a single card. OPERATING ADVANTAGES: Requires only one hex-width card in each computer to effect link. Exhibits one bus load. Directly software transparent as a DR11-B or DA11-B equivalence.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 569



CACHE/45TM (CACHE BUFFER MEMORY)

INSTALLS IN: PDP-11/45, -11/50 and -11/55. CAPACITY: 2048 byte (1K word). ENHANCEMENT FACTOR: Run time reductions to 50% (100% speed improvement) are achievable. CACHE PARITY: Automatically goes off-line in event of any data error. RANGE SELECTION: User may optimize hit ratio by upper/lower limit switch settings. SPECIAL FEATURE: Cache/45 can be enabled via software or console switches.

ABLE COMPUTER, 1751 Langley Ave., Irvine, CA 92714. (714) 979-7030. CIRCLE 572 ABLE has three more *''show-stoppers''* for you in Booth 2608 at NCC '81.



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You can't tell by specs alone.

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