COMPUTER DESIGN

THE MAGAZINE OF COMPUTER-BASED SYSTEMS

JUNE 1980

DATA DRIVEN SYSTEM FOR HIGH SPEED PARALLEL COMPUTING — PART 1: STRUCTURING SOFTWARE FOR PARALLEL EXECUTION

BUS ARBITER STREAMLINES MULTIPROCESSOR DESIGN

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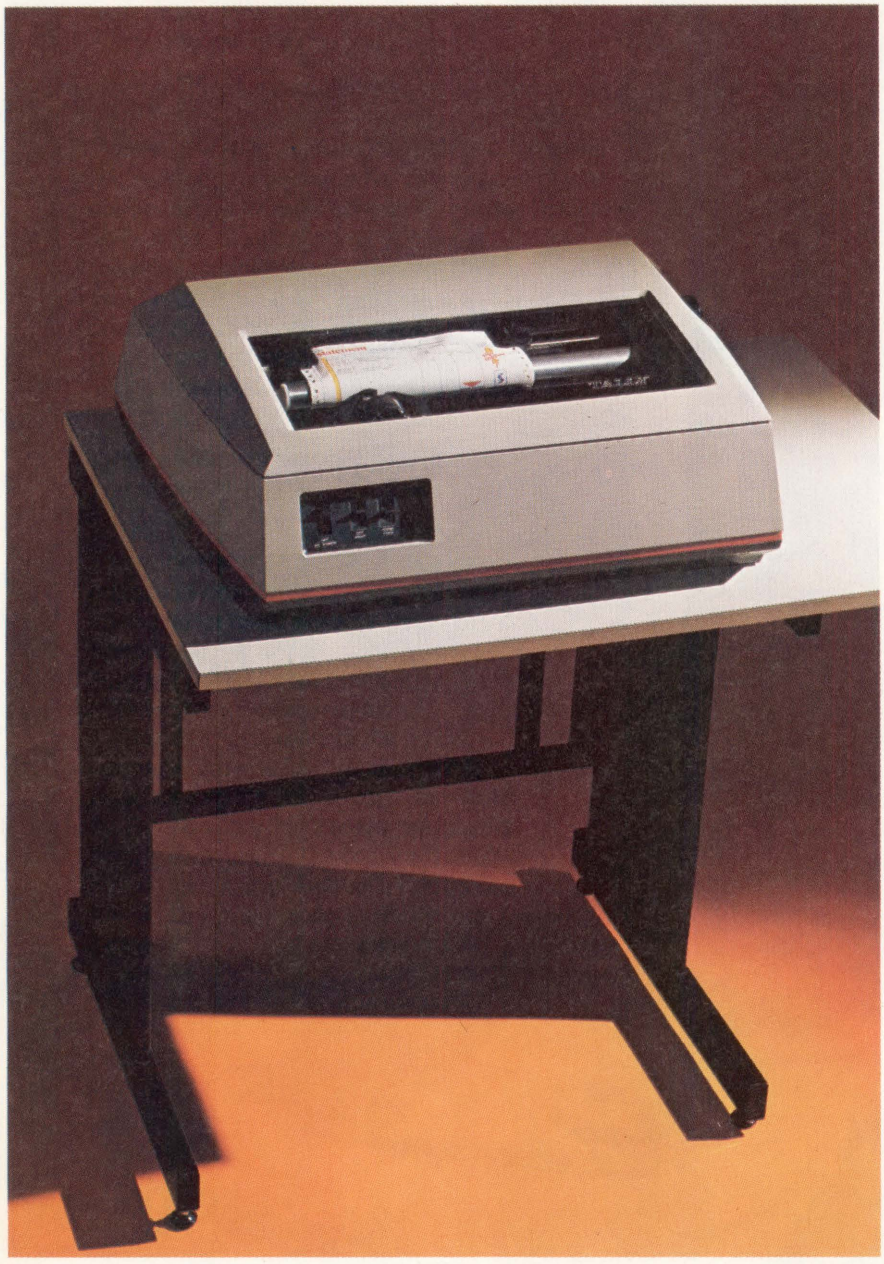

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THE MAGAZINE OF COMPUTER-BASED SYSTEMS

VOLUME 19, NUMBER 6 JUNE 1980

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The task of executing apparently simple decimal arithmetic procedures in a processor requires fairly complex microcode. Hardware simplifies and speeds such operations

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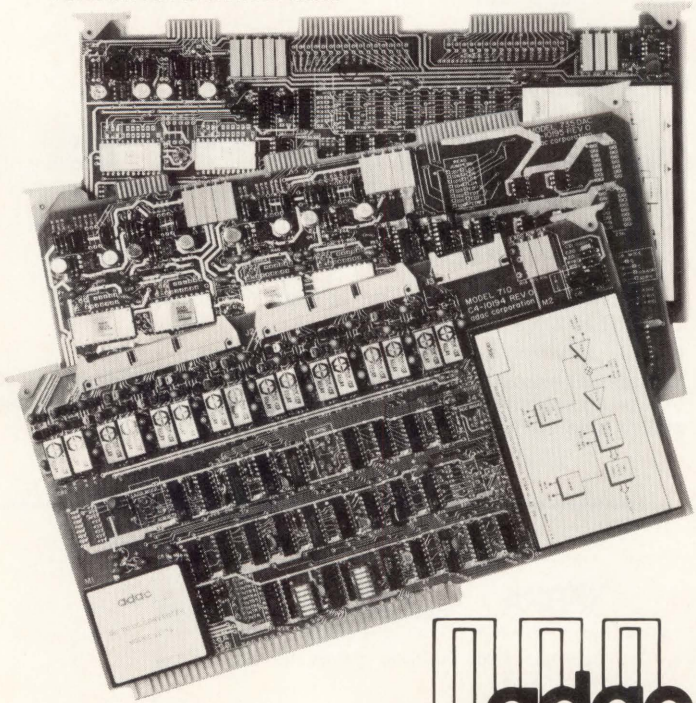

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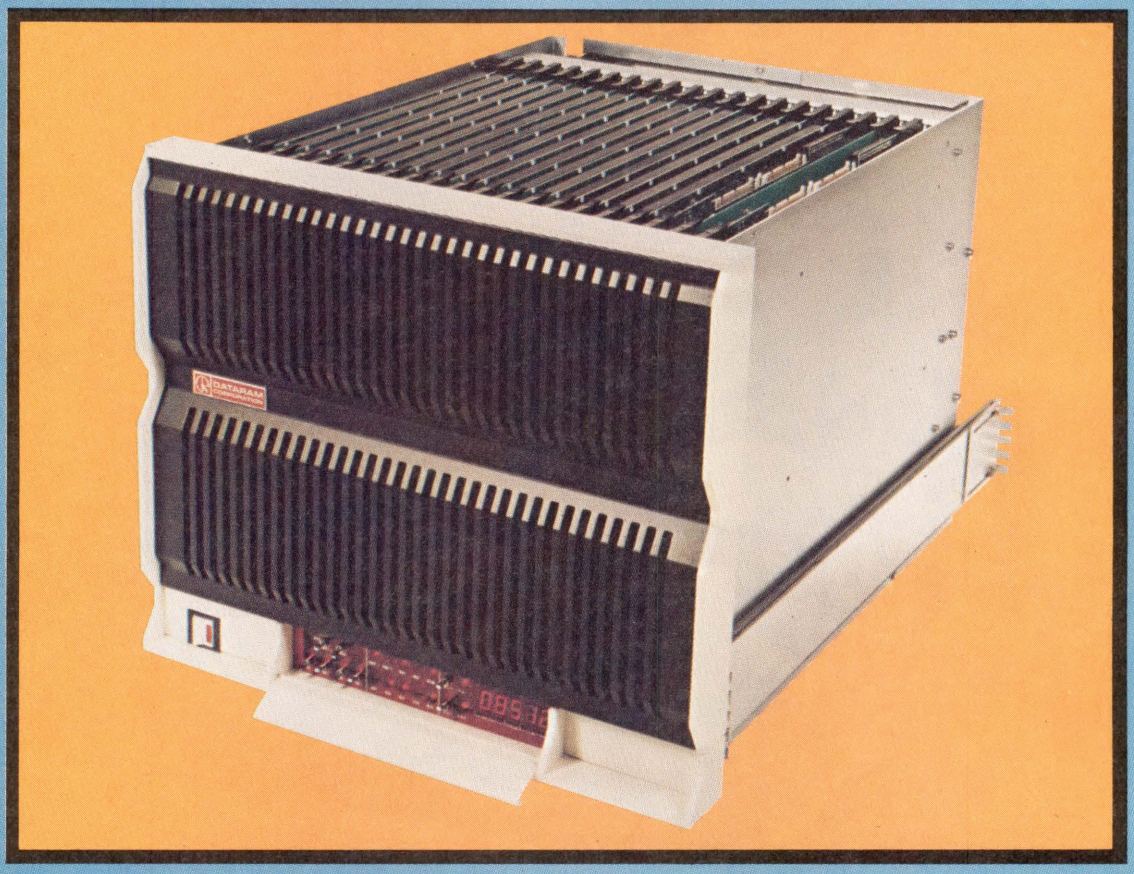

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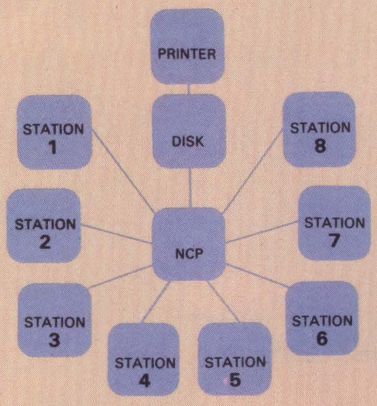

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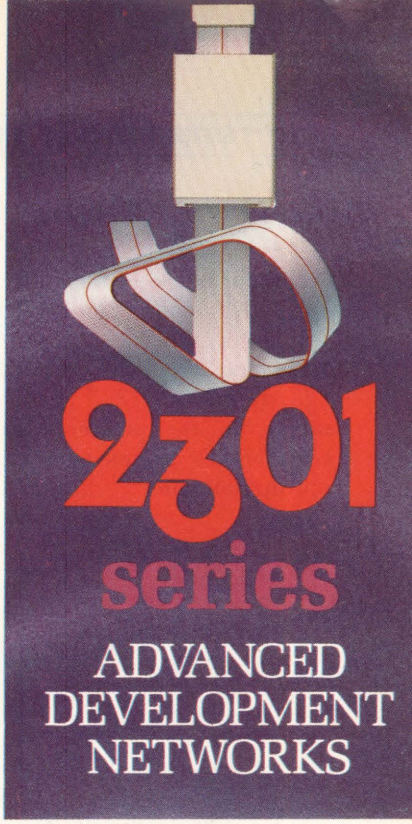

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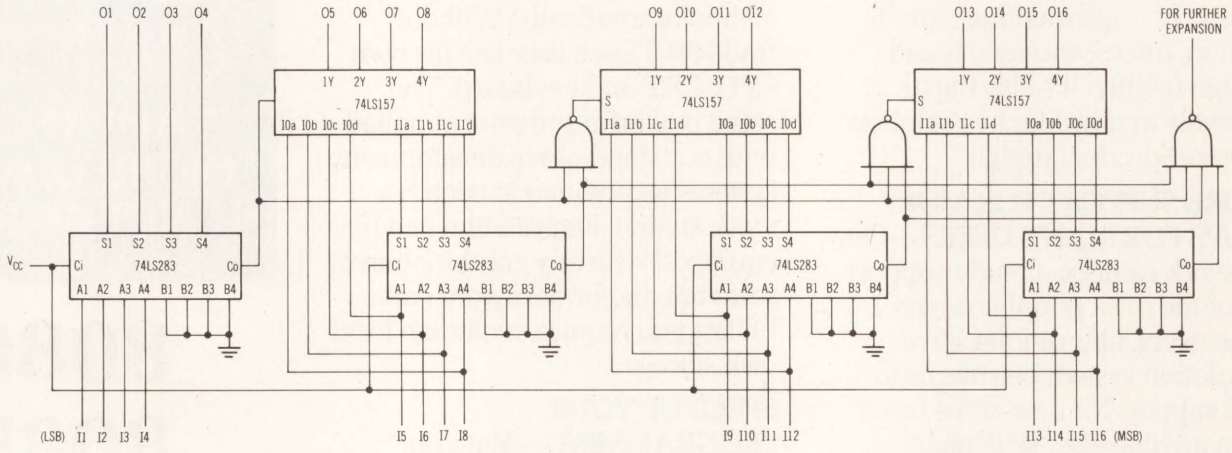
LETTERS TO THE EDITOR

To the Editor:

I read the article in *Computer Design* (July 1979) on "Practical Hardware Solutions for 2's Complement Arithmetic Problems" by Thinh V. Nguyen (pp 105-112). I agree with the author on the problems associated with the 2's complement arithmetic and the solutions.

I would, however, like to point out that the improved adder circuit shown in Fig 2 (p 107) fails with certain input combinations. One such input combination is 100 0110 1111 0101. With this as input, the output of the circuit shown in Fig 2 is 100 0111 1111 0110, whereas the correct output should be 100 0110 1111 0110. The circuit shown gives the correct output for all input combinations but at the cost of a few more nanoseconds delay (associated with NAND gate).

K. Krishnamurthy
Aeronautical Development Establishment
Bangalore, India



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CALENDAR

CONFERENCES

JULY 1—IEEE Indy Microcomputer Show, Sheraton Motor Inn East, Indianapolis, Ind. INFORMATION: Harry D. Bostic, IEEE Indy Microcomputer Show, Naval Avionics Ctr, D/810, 6000 E 21st St, Indianapolis, IN 46218. Tel: 317/353-3047

JULY 1-3—EFOC '80 (European Fiber Optics and Communications Exposition), Hotel Sofitel, Paris, France. INFORMATION: Michael A. O'Bryant, Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

AUG 12-14—Computer Graphics 80 Internat'l Conf and Exhibition, Birmingham, England. INFORMATION: Paula Stockham, Online, Cleveland Rd, Uxbridge UB8 2DD, England

AUG 12-15—1980 Joint Automatic Control Conference, Sheraton-Palace Hotel, San Francisco, Calif. INFORMATION: David Hullender, Dept of Mechanical Engineering, U of Texas at Arlington, Arlington, TX 76019. Tel: 817/273-2561

AUG 18-21—Nat'l Conf on Artificial Intelligence, Stanford U, Stanford, Calif. INFORMATION: American Assoc for Artificial Intelligence, Stanford U, PO Box 3036, Stanford, CA 94305

AUG 25-27—Summer Computer Simulation Conf, Olympic Hotel, Seattle, Wash. INFORMATION: Katy Lang, Boeing Computer Services, PO Box 24346, MS 87-06, Seattle, WA 98124. Tel: 206/773-7370

AUG 26-29—1980 Internat'l Conf on Parallel Processing, Boyne Highlands Convention Ctr, near Harbor Springs, Mich. INFORMATION: Kay Garringer, Dept of Computer Science, Wright State U, Dayton, OH 45435. Tel: 513/873-2491

SEPT 3-5—Electronic Business Communications Conf and Exhibition, Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: John Sodolski, Electronic Industries Assoc, 2001 Eye St, NW, Washington, DC 20006. Tel: 202/457-4934

SEPT 3-12—1980 Internat'l Machine Tool Show, McCormick Place, Chicago, Ill. INFORMATION: National Machine Tool Builders' Assoc, 7901 Westpark Dr, McLean, VA 22102. Tel: 703/893-2900

SEPT 15-18—1980 European Solid State Device Research Conf, U of York, York, England. INFORMATION: Clive Jones, The Institute of Physics, 47 Belgrave Sq, London SW1X 80X, England

SEPT 16-18—FOC '80 (Internat'l Fiber Optics and Communications Exposition), Hyatt Regency Embarcadero, San Francisco, Calif. INFORMATION: Michael A. O'Bryant, Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

SEPT 16-18—WESCON, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEPT 22-25—Software INFO (National Software Package Conf and Exposition), Hyatt Regency, Chicago, Ill. INFORMATION: Professional Exposition Management Co, Suite 545, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-3131

SEPT 23-25—COMPCON Fall '80, Capitol Hilton, Washington, DC. INFORMATION: Harry Hayman,COMPCON 80 Fall, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

SEPT 25-28—Mid-Atlantic Personal and Business Computer Show, Philadelphia Civic Ctr, Philadelphia, Pa. INFORMATION: National Computer Shows, PO Box 678, Brookline Village, MA 02147. Tel: 617/524-0000

OCT 1-3—Fault Tolerant Computing Systems, Kyoto, Japan. INFORMATION: Prof John Meyer, Dept Elec and Computer Engineering, U of Michigan, Ann Arbor, MI 48109. Tel: 313/763-0037

OCT 6-9 AND OCT 14-17—8th World Computer Congress, Tokyo, Japan, and Melbourne, Australia. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100

NOV 6-12—Electronica '80, Munich Fairgrounds, Munich, West Germany. INFORMATION: Franc D. Manzolillo, Rm 6015, U.S. Dept of Commerce, Washington, DC 20230. Tel: 202/377-2991

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AUG 21-22—Microprocessors: Hardware, Software, and Applications, Worcester Polytechnic Institute, Worcester, Mass. INFORMATION: Ginny Bazarian, Office of Continuing Education, Worcester Polytechnic Institute, Worchester, MA 01609. Tel: 617/753-1411, X517

SHORT COURSES

JULY 21-25—Introduction to Ada Computer Programming Language, George Washington U, Washington, DC. INFORMATION: Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: 202/676-6106

JULY 21-25—Digital Communications Systems; JULY 21-25—Mini- and Microcomputers; Their Structures, Characteristics, and Applications; JULY 28-AUG 1—Interactive Computer Graphics; and JULY 28-AUG 1—Microcomputer System Design and Applications, U of Michigan, Ann Arbor, Mich. INFORMATION: Viola E. Miller, Engineering Summer Confs, 300 Chrysler Ctr, North Campus, Ann Arbor, MI 48109. Tel: 313/764-8490

JULY 30-AUG 1—Computer Systems Architectures; and AUG 5-7—Communications Protocols and Computer Networking, Santa Monica, Calif. INFORMATION: Computer Technology Institute, 1024 Pico Blvd, Suite 101, Santa Monica, CA 90405. Tel: 213/376-3003

AUG 11-15—Videodisc/Microcomputer Institute, Logan, Utah. INFORMATION: Life Span Learning Programs, UMC 01, Utah State U, Logan, UT 84322. Tel: 801/750-1690

AUG 18-22—Key Aspects of Information Systems Technologies: Database Systems, Telecommunications, and Performance Evaluation, MIT, Cambridge, Mass. INFORMATION: Director of Summer Session, Rm E19-356, Massachusetts Institute of Technology, Cambridge, MA 02139

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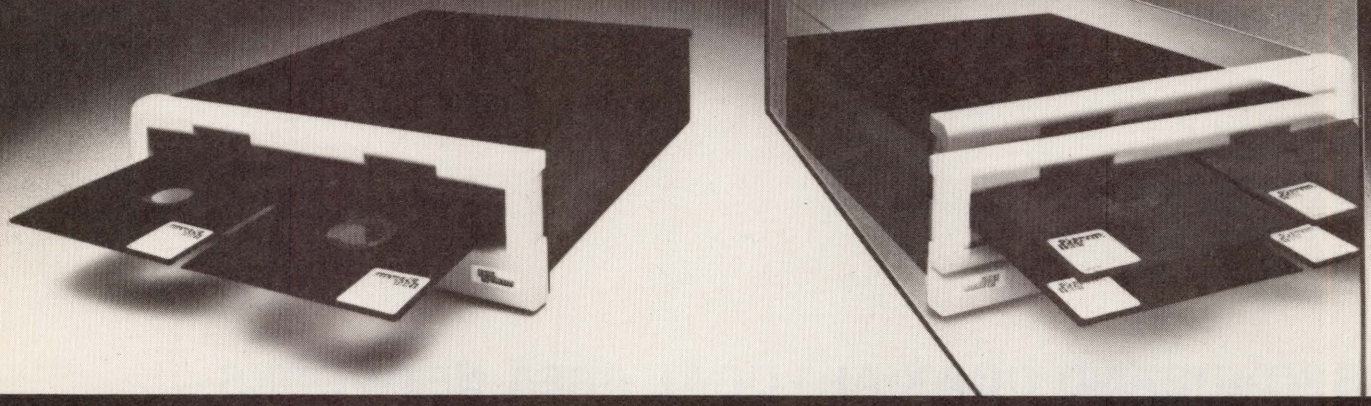

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CIRCLE 9 ON INQUIRY CARD

BROADBAND COAXIAL LOCAL AREA NETWORKS— PART 1: CONCEPTS AND COMPARISONS

Mark A. Dineson

Sytek Inc, Northwest Engineering Laboratory
13333 NE Bellevue-Redmond Rd, Bellevue, WA 98005

There has lately been an almost logarithmic growth in limited distance computer and terminal networks and in multimode communications facilities. Because of this, much attention has been concentrated on transmission media capable of high performance data transfer. Conventional media, such as twisted pair and leased lines, are being replaced at an increasing rate by upgraded networks. These changes are brought about by requirements for high speed, high channel density, and low error rate performance. As intelligent terminals, microcomputers, minicomputers, and specialized services grow in their respective environments, so do the requirements for high performance communications.

Transmission media of the new decade include fiber optics, and baseband and broadband coaxial cable. Of these, the latter two are the oldest and most proven by previous installation. In the realm of these media, coaxial cable capabilities supersede their twisted pair counterparts by several orders of magnitude. Coaxial cable affords the distributed data processing or large terminal network designer unparalleled flexibility and performance, as well as a means for upgrading existing networks.

There is a growing number of corporate and industrial environments that require multimode services. Such services might include interactive terminal support, graphics, microprocessor development, facsimile, electronic document transfer, and voice and video services. These applications have traditionally been tied to differing transmission media, depending on the data rates and bandwidths required for adequate service. This has resulted in a proliferation of physically separate and totally different cable types in the same duct or conduit, and in the continuing expense associated with installation, upgrade, and management.

Fitting the Medium to the Application

Experience tells us that there is no one ideal solution to each and every problem encountered in configuring a data network. When one searches for the most capable medium for long term installation growth in a multimode local environment, one must begin by comparing the characteristics

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When you need Winchester-type disk drives in 20-, 40- or 80-megabyte capacities, take a hard look at the NEC D-1200 Series disks.

You'll find packaging, features, reliability and technology that are the results of 15 years of building high-performance disk systems.

Take the read/write head of the D-1200. It is loaded with technical enhancements. Like contact fixed read/write capability that reduces ambient errors. Like LSI preamplification in every head, which further reduces errors by improving signal-to-noise ratios. Like address mark detection for faster seek-and-search. Like high-speed data transfer rates of 1.2 megabytes per second. And with two fixed-head-per-track options to improve seek time and speed up overall performance even more.

Every NEC D-1200 disk has an industry-standard storage module (SMD) interface, so it is immediately connectable to any mainframe or mini that uses storage module disks. But with higher speeds (8.3 millisecond latency time) and greater configurability (its dual-port option lets two CPUs share a single disk) than many other SMD disk drives.

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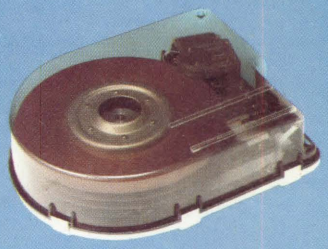
Join the growing number of systems builders who rely on NEC D-1200 disk drives to make their total system more attractive. For more information, contact our nearest sales office.



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NEC Information Systems, Inc.

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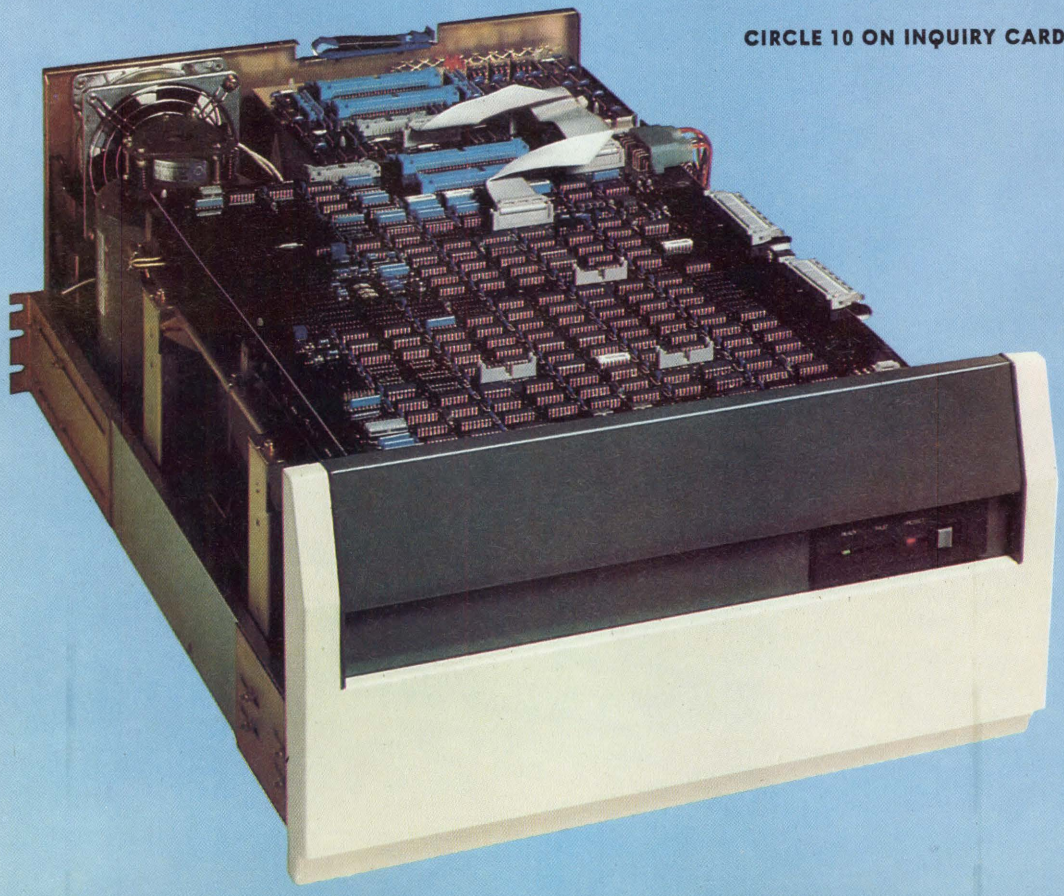
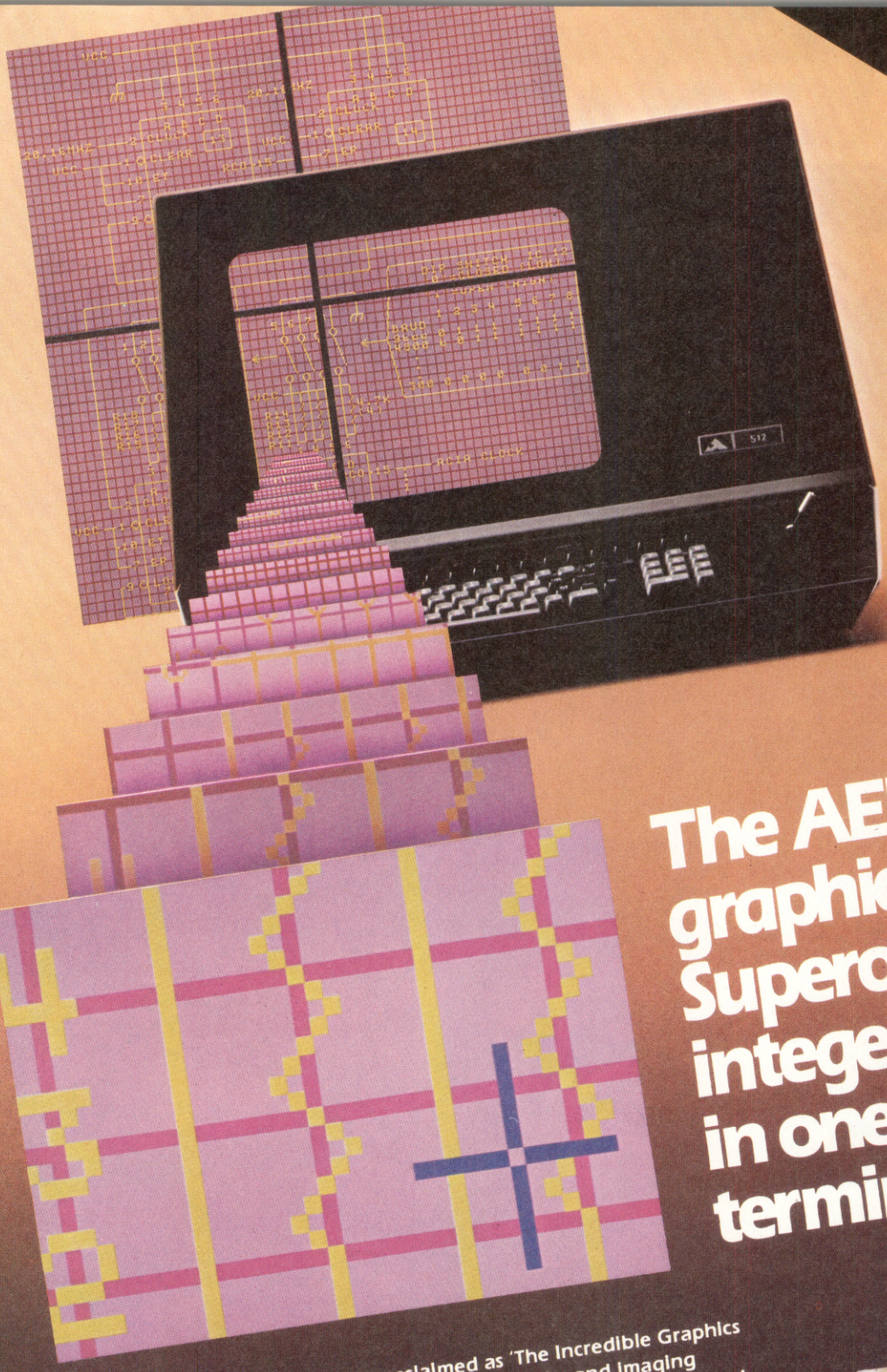
CIRCLE 10 ON INQUIRY CARD

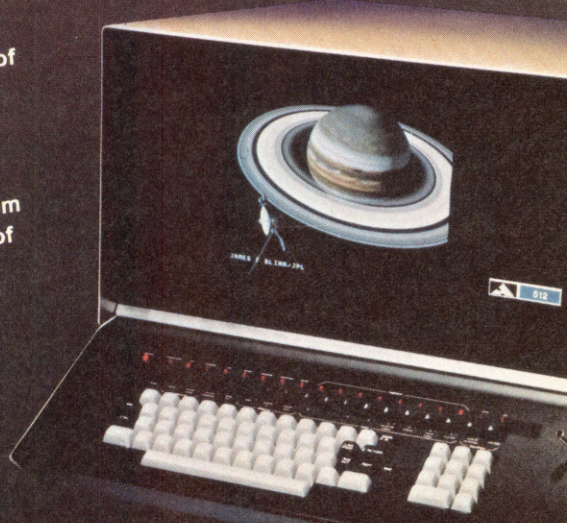


See you at NCGA '80 and SIGGRAPH '80



The AED 512... graphics, imaging, Superoam™ and integer zoom in one desktop terminal!

At the Siggraph '79 Show, it was acclaimed as 'The Incredible Graphics Machine!' Since then, the AED512 full-color graphics and imaging terminal has more than lived up to its reputation among sophisticated users. Its ability to display 256 simultaneous colors (from a total palette of 16.8 million) on a 512 x 483 pixel screen; zoom at integer increments to x16; pan continuously via joystick; perform full-screen DMA transfer in 0.5 second; emulate Tektronix 4014 software; allow overlaying TV images with computerized graphics; permit animation by using read/write masks and colorblink make its under $20,000 price tag seem small. Add to this its unique ability to Superoam an expanded image of 1024 x 1024 pixels and you'll see why the FIVE-TWELVE is features ahead of the competition. For more information contact Jerry Kennedy, Advanced Electronics Design, 440 Potrero Ave., Sunnyvale, California 94086, phone (408) 733-3555.



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CIRCLE 11 ON INQUIRY CARD

Basic Media Comparison

	Fiber Optics	Baseband Coaxial	Broadband Coaxial
Aggregate data rate (bits/s)	300M + half duplex	Up to 50M half duplex	100M + full duplex
Multidrop	Limited to repeaters	Up to 100	Several thousand
Distance (km)	10 +	1-3	10 +
Noise immunity (approximate)	Unaffected by EMI	50-60 dB isolation	85 dB isolation
Approximate cost/ft	$2.00	$0.20	$0.30

Note: Table compares relative costs and capabilities of various high performance local network media. It does not take into account costs associated with interface drivers. Fiber optics takes lead in long distance (trunk) applications for point to point services. Baseband coax looks good for computer to computer multidrop bus systems, but lacks large scale capability in plant distribution. Broadband coax has large capacity supported by high multidrop capability, ideal for data distribution networking

of the available means of transmission in a relatively basic form (see Table, "Basic Media Comparison"). This comparison can be somewhat deceptive unless the application is more fully defined. All three media listed in the Table may perform equally well in high speed point to point applications. Broadband coaxial cable is a logical choice where many microcomputer, minicomputer, terminal, or graphics links are to be established and distributed. One application of high speed baseband coaxial cable is shown in Fig 1.

All three media, some with certain restrictions, may be used for lower speed applications. Fiber optic links are increasingly being applied to connect terminal devices and processors (Fig 2). Normally, these links must be point to point, restricting designers to multiple fiber cable requirements when they are used as links for terminals and distributed data processing equipment.

This same observation holds true for IBM's 3270 type system, which uses pulse width coded signals at a fixed rate to communicate on baseband coaxial cables. Although terminals may be multidropped on the cable under some circumstances, only one port can appear at the controller end of the cable. Designers are again faced with a proliferation of coaxial cables, in some cases thousands, emanating from terminal devices.

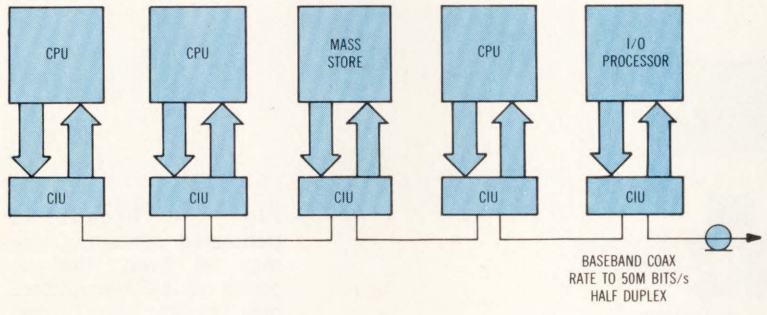

Fig 1 High speed baseband coaxial bus usage. Baseband coax is used in channel-oriented processor interconnection system by means of channel interface units (CIUs) for each processor whose channel must connect to another channel-based device. This allows communication from an IBM machine to DEC, 7600, or Cray through special interfaces. Data are distributed on coax "bus" via specialized form of packet data communication at rates approaching 50M bits/s. However, throughput is totally function of interface firmware

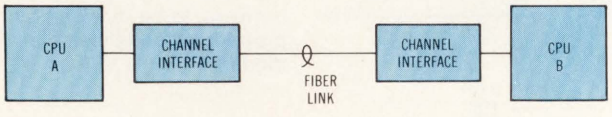

Fig 2 Typical fiber optic link. Such links are especially useful where very high data rates are used between processors. They not only isolate systems electrically, but provide low noise data path which may be hundreds or thousands of meters long. They are logical choice as transmission media for direct channel communications at rates of 50M to 60M bits/s or higher

One of the ultimate and perhaps the most widely known approach to increasing the capabilities of baseband coaxial cables is Ethernet® by Xerox Corp. This broadcast mode packet network makes very efficient use of a single-channel baseband coaxial cable, and provides many of the services required in a multiple minicomputer or terminal network. Also, controlled "gateways" allow access to other local networks and increase resources available to the user.

The Broadband Network Approach

Broadband coaxial cable local area data networks have been available for some time. One of the first of these, the Manhattan Community Antenna Television (CATV) system, resulted from the inability to procure local data lines in metropolitan New York. Several user organizations required high speed data traffic, with the result that data modems were designed that would utilize the local CATV system as their connecting medium. These services have been implemented elsewhere in the past few years. Several large automotive industry manufacturers have installed networks of this type for process control, management information systems, and television services. Banks, aerospace companies, universities, government institutions, and military organizations have done the same.

The term "broadband coaxial local area network" defines the medium and not the applications to which it is assigned. In its most efficient mode, it may be used as a branching coaxial cable carrying voice, video, telemetry, security, and telephone EPABX trunks, all at the same time and on a single cable. Each channel is assigned by frequency. The addition of packet network technology or time division multiplex (TDM) techniques does not change this basic configuration.

A direct hardware analogy to a broadband coaxial cable local area network is a satellite network, in which users may access or be accessed in any of the following modes: time division multiple access (TDMA), assigned point to point channel, and carrier sense multiple access (CSMA). As with a satellite network, all channels are assigned by frequency and bandwidth slots, whether their data rate be 110 or 6M bits/s. Channels are then stacked to fill the available spectrum of the medium.

Basic operation of a broadband translated system is shown in Fig 3. Like the satellite system, there is a central retransmission facility for all signals transmitted to it. It receives these signals, converts them to a different frequency, and retransmits them over a broad area, so that many receivers may access the information sent from one source.

The Broadband Difference

One area of difference between fiber, baseband coaxial, and broadband coaxial media that goes beyond the concept of "virtual" interconnection capability is that of synchronization. Each channel assigned on a single coaxial cable of a broadband network operates independently of any other channel; there is no requirement to synchronize channels. Each frequency division multiplex (FDM) derived channel

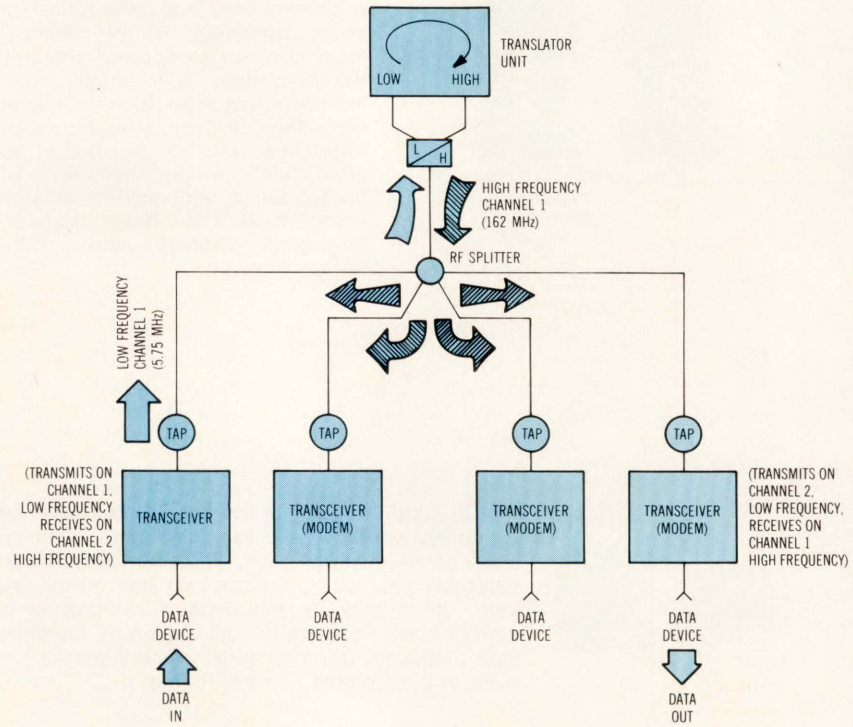

Fig 3 Broadband translated system. Cable may be 2-way; that is, group of low frequencies may be directed to travel in one direction, with high frequencies in the opposite. Translator is provided at central location to allow any tap site in the system to reach any other. When transceiver transmits on low frequency, it is routed to translator, converted to specific high frequency, and distributed via coax to all points of network, to be received by properly channel-selected modem

(continued on page 21)

What standard line gives you more than a standard choice in subminiature D?

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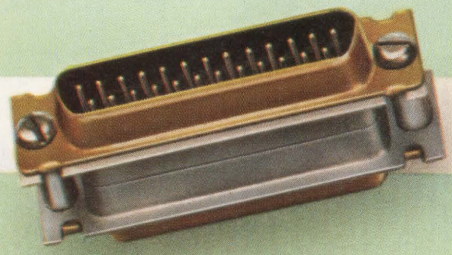

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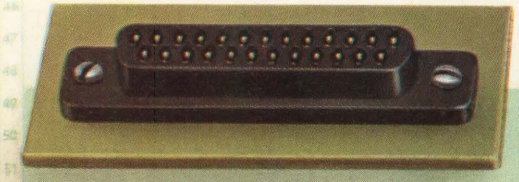

Press fit our all-plastic headers with compliant pins.

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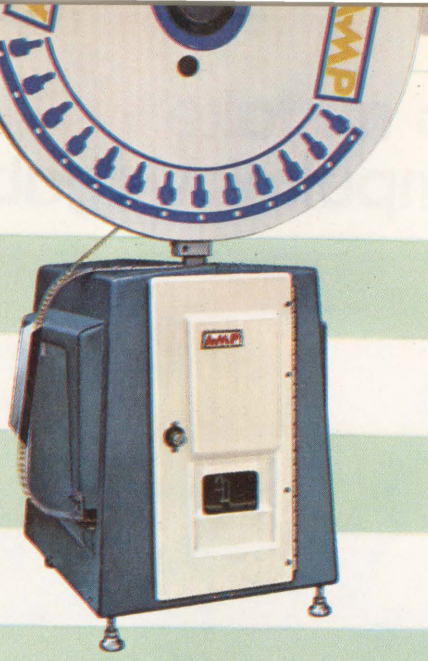
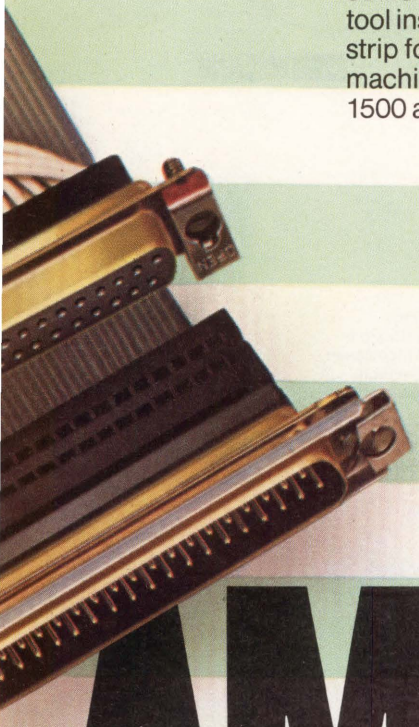


Pick your tools for termination.

Our wide choice of contacts come in loose form for hand tool installation. Or in continuous strip for our stripper crimper machines that terminate up to 1500 an hour.



Hardware that saves everywhere.

Meet the latest communication specs with the RS 449 type latch. Or match your need with our easy one-piece slide or two-piece slide latches. For quick and easy connects and disconnects, our squeeze-to-release latch is a one-of-a-kind convenience. And there is a complete range of strain relief shells, including a metal style for shielded cables.

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connectors.

You couldn't ask for more innovation in subminiature D interconnection.

That's how our standard line of AMPLIMITE product responds to the changing needs in the high density connector market.

Above standard.

A good example is the way we accommodate future specs right now. For the upcoming RS 449 we have 9- and 37-position sizes, latching hardware, and even pre-wired adaptors for interfacing to RS 232. Wire-to-wire, wire-to-board, AMPLIMITE connectors and tooling stay ahead so you can do more than keep up.

To know more, call the AMPLIMITE Information Desk, (717) 780-8400. Or write us. AMP Incorporated, Harrisburg, PA 17105.

These facts are worth knowing, too.

Electrical Characteristics
Contact Current Rating (with No. 20 AWG/0.5—0.6 mm^2/wire): 7.5A
Contact Resistance: 73 Milliohms (max.)
Dielectric Withstanding Voltage: 1000 V (min.)
Insulation Resistance: 5000 Megohms

Mechanical Characteristics
Contact Engagement Force: 120 Oz./3.4 N/(max.)
Contact Separation Force: 0.75 Oz./0.2N/(min.)
Contact Retention: 10 lb./44.4 N/(min.)
Connector Mating Force (per contact): 8 Oz./2.224 N/(max.)

Filtered Connector Data (20 Series)
Cutoff Frequency: 5 MHz
Insertion Loss: 55 db from 1 GHz to 18 GHz (per MIL-STD-220)
Insulation Resistance: 500 Megohms at +25°C (min.)
Dielectric Withstanding Voltage: 250 VDC for 5 sec.
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". . . We have successfully utilized thousands of them in a variety of Sanders' graphics products and systems. . . ."

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Sanders Associates, Inc., Information Products Division, produces a variety of high speed, interactive graphics products for a broad range of government and industrial uses.

1 bit in 10^{12} error rate for local networks on coaxial cable

William Bernstein, Vice President, General Manager, IPD of Sanders Associates, Inc. talks about Computrol modems. *"The Computrol coaxial cable modem was selected after a careful evaluation of alternative products and approaches, taking availability, reliability, performance and cost into consideration.*

We have successfully utilized thousands of them in a variety of Sanders' graphics products and systems.

Its flexibility gives our designers freedom to readily incorporate the modem into new systems."

Sanders uses Computrol modems to build fast, reliable distributed computer graphics systems. You can profit, too, from features like these:

- **Operates at all data rates from DC to 2 Megabits/sec without readjustment**
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- **Multidrop up to 255 devices on a single coaxial cable without directional couplers**
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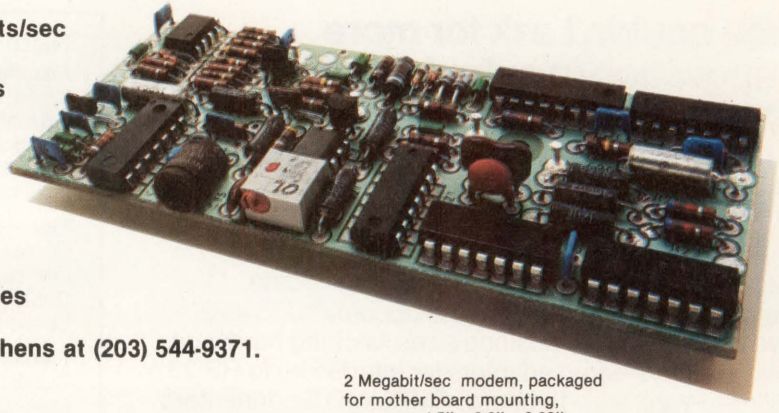

2 Megabit/sec modem, packaged for mother board mounting, measures 4.5" x 2.0" x 0.38"

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CIRCLE 13 ON INQUIRY CARD

may operate via its own control mechanism, from a simple point to point protocol-transparent link to a shared multipoint packet network. This powerful concept, coupled with the almost totally independent interconnect characteristics of broadband, generates a useful and flexible medium for local area networks. The approach allows implementation of other services simultaneously on the available spectrum. In Mitrenet, an example of such a system, the packet network coexists with security, television, and point to point data transmission.

Broadband coaxial cable makes a tremendous variety of services available to network architects and designers. Given the ability to assign channels and data circuit functions with relative independence, many multimode configurations are possible. The simplest application, an asynchronous point to point data link, may reside "right next door" to computer file shipping channels on the spectrum. In the aggregate, usage may grow from 30 to 40 full duplex services supporting point to point terminal applications, to a heavily loaded system supporting everything from timesharing to file shipping, with no wiring changes required in the main system. These networks provide complete data communications services, supporting literally thousands of local users, as well as interconnection into more conventional long haul data communications utilities.

Rather conveniently, the appearance of all signals on the same coaxial cable simplifies broadband network monitoring. Spectrum surveillance equipment is an important aid in the tasks of monitoring signal levels and detecting failures. Monitoring systems may contain a realtime minicomputer with resident data base which may monitor signals, command loopback functions, and operate remote test equipment to isolate faults. They may also monitor, on a polled basis, the status of repeater units. It is much simpler to monitor signals on one coaxial cable than it is to contend with a complexity of baseband coaxial cables or twisted pairs. Existing technical control systems are capable of generating remote system status displays and of suggesting fault diagnosis techniques to repair personnel.

Other attractions in the broadband arena include frequency agile modems, capable of manual or computer-driven slot assignments; virtual trunk telephone modems; multiple channel packet networks, in which the traffic is offloaded to alternate channels during peak activity periods; and user-controlled multiprocessor access through channel assignment. The continuing development of these techniques makes broadband an even more attractive alternative for data network implementation.

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In next month's issue, Part 2 of this column discusses hardware components available for implementation of broadband local area networks.

Thinking CRT Cursor Control?

For Military or Rugged Industrial Applications

Librascope's Magnetic Trackball, with integral electronics, provides simultaneous X and Y scalar increments as inputs for digitally driven graphic displays, to position cursors, to add new data, or to modify existing data. Functions are generated by positioning two magnetic encoders with a hand driven ball to generate the orthogonal digital signals.

Designed for harsh environments, Librascope trackballs operate in the temperature range −55°F to +180°F and from sea level to an altitude of 50,000 feet. The unit complies with the environmental specifications of MIL-E-5272, Procedure 1 and MIL-T-5422.

Write or call for complete specifications. Librascope Division, The Singer Company, 833 Sonora Ave., Glendale, Calif. 91201. Telephone (213) 244-6541.

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Librascope's magnetic encoders are the most reliable source of digital signals to represent a shaft angle. They offer long, maintenance free life in the harshest military or industrial environments. Output signals drive TTL integrated circuits directly. All models operate reliably in the temperature range −55°C to +125°C.

CIRCLE 14 ON INQUIRY CARD

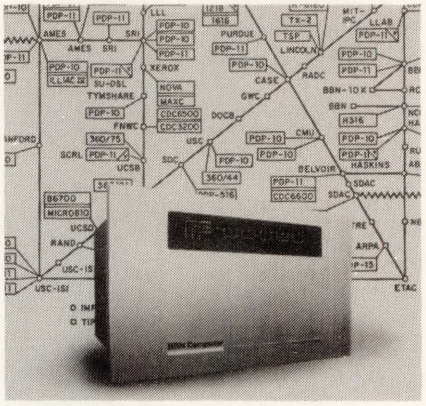
Packet Switching Processor Provides High Throughput, Adaptive Routing

Designed specifically for high speed communications environments, C/30 processor is a microprogrammable 20-bit computer capable of running more than 130 packets/s, each packet of 1008 bits or less, full duplex communication line throughput. According to the manufacturer, BBN Computer Corp, 33 Moulton St, Cambridge, MA 02238, it is the only medium speed communications processor to offer adaptive routing. This feature provides flexible network configuration, and automatically transmits each packet to its destination via the shortest path available, reducing line costs and allowing automatic bypass of failed nodes.

The C/30 is based around a CPU with an instruction set designed for communications. Basic elements are 1k x 20-bit register file, 512 x 32-bit microcode ROM containing loader, debugger, and console logic, and 2k, 4k, or 8k x 32-bit microcode memory containing the macroinstruction set and I/O emulation.

Complex I/O logic is performed for the most part by the central microprocessor. This reduces I/O component count by a factor of 3 or 4, and allows one basic I/O device to be configured by firmware (microcode) as many different devices. As an example, the basic serial communications line device can accommodate asynchronous devices at speeds from 50 to 19.2k baud (with or without modem control), synchronous, or binary synchronous devices to 56k baud, all by simply changing microcode. As a result, there are only 12 ICs in the C/30 bisynchronous interface, compared to 80 ICs in traditional interfaces. A 100k-bit microcassette is used to load microcode in RAM, allowing the system OEM to use a small number of I/O designs for a large number of varying applications.

The basic chassis supports 4 cards: CPU, memory, and two I/O cards. An expanded chassis having eight slots and a larger power supply is an option. Error detection and correction (EDAC), providing 6 bits of checking and allowing detection of all double-bit failures



Software used in C/30 processor has been running for more than ten years on ARPANET. Software and hardware are optimized for packet switching I/O and sophisticated routing algorithms. C/30 provides speeds of more than 130 packets/s

and correction of all single-bit failures, is standard. Optionally, the C/30 is supplied with the ARPANET interface message processor (IMP), or terminal interface processor (TIP) software.

The C/30 has four basic I/O designs: medium and high speed asynchronous/synchronous; high speed HDLC/SDLC; and high speed 1822/ARPANET. Each design has a number of daughter boards to provide voltage conversion as required, and associated microcode to handle the interface for a specific line protocol.

The unit draws 300 W from 120 Vac 60 Hz, 220 Vac 50 Hz, or 12 Vdc. It mounts in a standard 19″ (48.3-cm) rack cabinet and occupies 12.5″ (31.8-cm) vertical space. Weight is 40 lb (18 kg).

Circle 517 on Inquiry Card

Patents Granted for Bus Communications Systems

Two patents for digital bus communications systems have been awarded to Mitre Corp, PO Box 208, Bedford, MA 01730. Both systems operate in time division multiple access (TDMA) mode and include a number of terminals coupled to a common signal path or bus. The digital communications buses are designed to coexist with other services, such as television or cable telephone, on a CATV cable network, and to use only a small portion of the available spectrum.

In the first system, a slotted bus is used. Time slots are allocated to various requesting terminals in order to establish communication links over the bus. One version of this system enables communication at 7.4M bits/s and can accommodate hundreds of such subscriber devices as CRT terminals, printers, and host processors. Dedicated time slots for high duty cycle, and commonly shared slots for low duty cycle terminals can be supported simultaneously.

The second system uses an unslotted bus, where each subscriber contends for service on the common channel, using a carrier sense multiple access (CSMA) technique. Two versions of this system have been configured, operating at 307.2k bits/s and 1M bits/s respectively. The unslotted system is also capable of handling hundreds of connected subscriber devices.

Terminal Control Unit Handles Limited Communications

Designed to meet requirements of small or new communications applications, the 1270 model 8 terminal control unit (TCU) provides functions necessary to allow an IBM System/360, 370, 303X, 4300, or compatible CPU to communicate with a variety of local and remote data communications terminals.

Recently introduced by Memorex Corp, San Tomas at Central Expy, Santa Clara, CA 95052, the TCU is a hardwired 8-line functional replacement for the IBM 2701 data adapter unit, 2702 and 2703 transmission controls, 3704 and 3705 communications controllers including the 4331 adapter

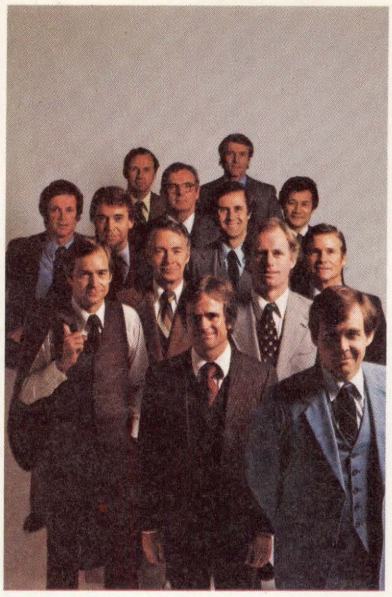
DEC controls DEC.

The companies at right control the disk and tape drive market.

And we've got the controller-formatters that put the two together.

No matter which of these 13 companies are selling you a disk or tape drive for you to integrate into your DEC-based system, you're going to need a controller.

Which one? Ask your peripheral salesman. Chances are he'll recommend Emulex.



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These 13 men have a controlling interest in DEC

It should come as no surprise that the leading tape and disk drive manufacturers have a strong interest in our family of software transparent microprogrammed controllers for PDP-11 and LSI-11 cpu's. Or that they recommend our products. They do it for purely selfish reasons. With an Emulex controller, integrating their drives into your DEC system is predictably fast and easy.

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All of our controllers are fully transparent to the cpu hardware and software, insulating you from system revisions. Because they're fully compatible, just plug them in, and you're running DEC diagnostics and operating systems in minutes. Plus we give you added features: automatic self-test, built-in pack formatting, programmable bandwidth control—and more.

It makes no difference which DEC-11 series cpu you're using, or what storage device. We support 59 different drives from these 13 manufacturers. Including all the latest varieties of 14-inch SMD and Winchester class disks; NRZ, PE, NRZ/PE and GCR tapes. And we're adding more all the time.

So when your disk or tape drive salesman calls, tell him you can't control yourself. Without Emulex. Or call or write for our free Buyer's Guide, today.

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CIRCLE 15 ON INQUIRY CARD

in emulation mode. It is compatible with 270X software support, and attaches directly to System 360, 370, 303X, 4300 or compatible byte multiplexer channel.

Three available versions of the model 8 TCU differ only in the number of wideband lines supported. Model 81 handles eight lines at speeds to 9600 bits/s as standard, any line operating asynchronously or isochronously. Model 82 can activate one wideband BSC line at speeds to 56k bits/s instead of one of the eight standard lines. Model 83 extends the 82 option to two wideband BSC lines.

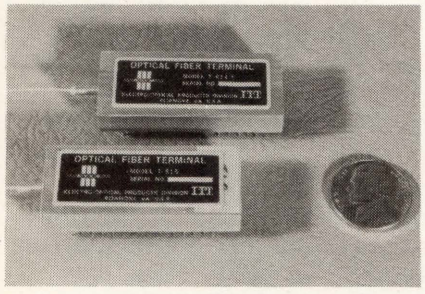
Standard features are automatic polling, synchronous transparency, automatic speed detection and protocol selection for asynchronous lines, TTY II (ASCII), IBM type I (2741) and IBM BSC (both EBCDIC and ASCII) support.

Additional cost options include an alternate channel switch, automatic dialing, code conversion, IBM type III (2260) support, and built-in asynchronous modems.

Delivery is scheduled for July 1980. Purchase prices range from $14,500 for model 81 to $18,550 for model 83. Lease rates are available.

Circle 518 on Inquiry Card

Fiber Optic Modules Offer Moderate Data Rate Communications



Designed to operate at moderate data rates, the T-6006 transmitter and T-6056 receiver modules can be used in such digital transmission applications as data buses, industrial controls, monitoring links, computer interconnect links, and inter- and intra-facility links. The modules are available from ITT Electro-Optical Products Div, 7635 Plantation Rd, Roanoke, VA 24019. The transmitter unit uses a high brightness IR-emitting diode, and the receiver a sensitive PIN photodetector.

When used with appropriate ITT optical fiber, the modules can handle data rates from dc (zero data) to 5M bits/s NRZ over cables as long as 1.5 km without repeaters. Since data transitions need not be present at the data input for operation, arbitrarily long strings of TTL high or low data, or even data bursts, can be accommodated without receiver dc drift problems.

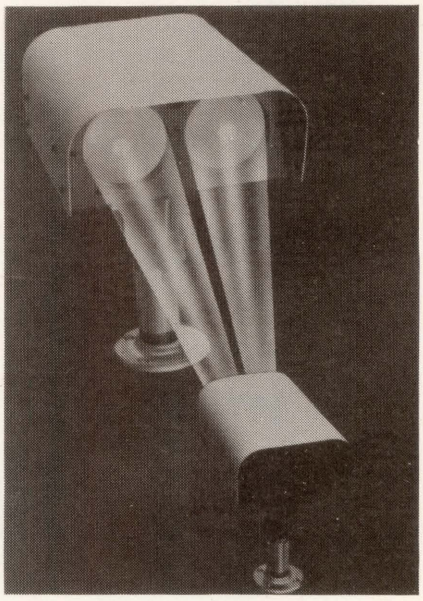
Each module has a fiber optic pigtail, whose type may be specified by the customer, for connection to the main fiber optic cable. Electrical interfaces are TTL compatible. A regenerated digital signal is present at receiver output. Pulse distortion is minimized over a wide dynamic range by internal circuitry.

The modules are suited to PCB applications with as little as 0.5″ (1.25-cm) spacing between the boards. PCB mounts for the modules are available. As an option, the optical pigtail can be provided with a factory-installed termination such as an ITT low loss single fiber connector. The modules are priced at $750/set and are available from stock.

Circle 519 on Inquiry Card

Infrared Light Link Transmits High Speed Data

Offered as an alternative to traditional telephone lines for line of sight data communications, Lite-Link™ places raw data on a beam of modulated IR light, eliminating the cost of such hardware as modems, and charges for leased line facilities. The system was originally developed for computer communications on the Boulder campus of the University of Colorado, and is now made commercially available by Newport Data, Inc, 126 Thames St, PO Box 750, Newport, RI 02840.



Lite-Link transceiver mounts on standard 2″ pipe. Elevation and azimuth adjustments are incorporated for alignment with transceiver at other end

The system operates on optical transmission using the IR spectrum of LEDs at distances up to 1 mile (1.6 km) at data rates to 500k bits/s. Operation is full duplex, synchronous or asynchronous.

No licensing is required. Standard terminals, concentrators, and communications adapters can be connected directly to the optical link. The system can accommodate a single high speed data stream, or, through an optional integral multiplexer, several lower speed data streams at separate ports.

Circle 520 on Inquiry Card

Software Product Family Extends Resource Sharing To 3270 Communications

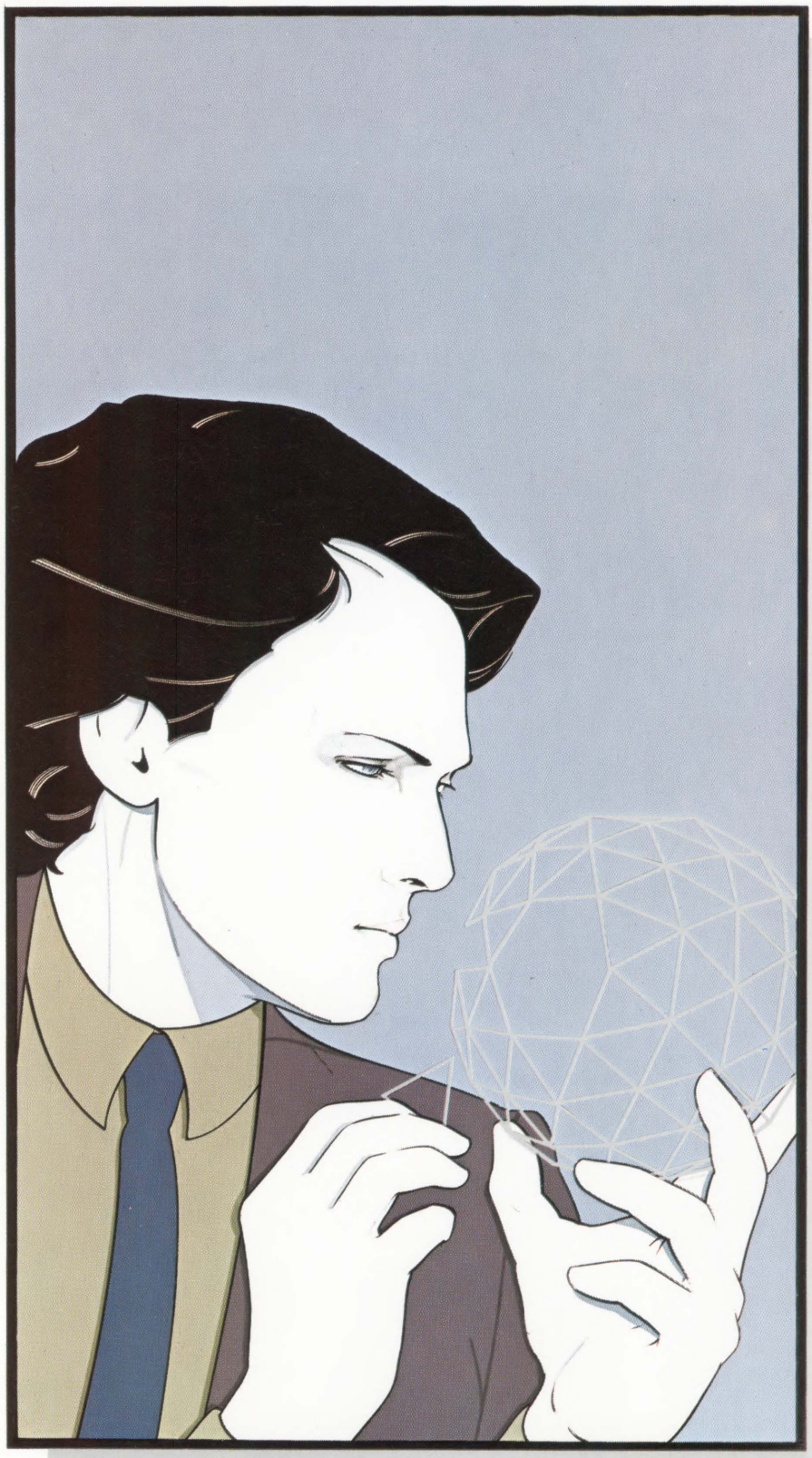
A family of software products for sharing communications facilities among multiple processors, ARCCOM™ permits interactive processing between Attached Resource Computer™ (ARC) systems and remote mainframes. First

(continued on page 29)

There is only one high performance VLSI computer solution.

Intel delivers it.

Architecture for hi



How Intel's 8086 microsystem, with its powerful structured architecture, helps designers meet the complex performance requirements of the '80s.

You need more than a CPU alone to meet the performance requirements of the '80s, because today's success lies in powerful new, structured approaches to system design. By logically segmenting and distributing system functions, structured design allows greatly increased throughput—and shorter design cycles. For example, with the 8086 family, using classical mainframe multiprocessing techniques, you can achieve I/O bandwidths of from 2 to 20 megabytes per second. That's at least 10 times wider than other systems. The object code for the 8086 family is 30% denser than the code for any other microcomputer available today. And, using our 8087 co-processor, you'll be able to perform 64-bit floating point arithmetic in less than 15 microseconds, surpassing existing systems by factors of 10 to 1000.

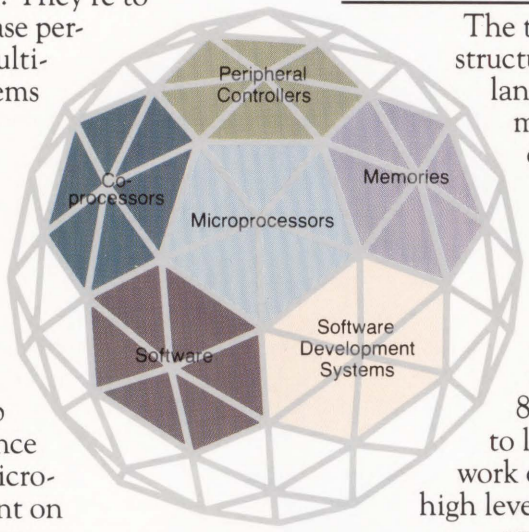
Intel's 8086 microsystem is the only 16-bit solution designed specifically to accommodate efficient multiprocessing schemes. What's more, only the 8086 is supported today by the VLSI building blocks you need to implement these high powered multiprocessing designs. Intel's new HMOS* 8089 I/O processor, for example, can increase through-

gher performance.

put by a full order of magnitude in I/O intensive designs. And look to Intel for high-integration co-processors, such as 8087 numerical data processors. They're to help you increase performance in multi-processing systems using our 8086 CPU. Or, for even faster processing, use our new 8086-2. It's the 8MHz CPU, available today, that delivers the top price/performance of any 16-bit microprocessor. Count on Intel for optimum price/performance in the future, too, as we add memory management and protection, and software modules in silicon.

Intel lets you implement powerful designs in an 8-bit format, too, with our 8088. The 8088 is hardware compatible with your 8-bit designs and software compatible with our 8086, to help you get tomorrow's performance in your system today.

You'll find other ways to unburden your CPU and increase throughput with Intel's 5 data communication peripherals, 7 device controllers, 6 slave processors, and 8 system interface circuits—all compatible with the industry standard Multibus™ bus. For high performance program memory, choose from Intel's 16K and 32K EPROMs, including our new high speed 2732A. Intel also delivers the world's largest selection of 5-volt static and dynamic RAMs, including our new 16K 2118 Dynamic RAM.



Intel Structured System

New fluency in high level languages

The trend toward structured high level languages is one more reason to choose Intel's 8086 system solution. Of all the 16-bit microcomputers, only the architecture of the 8086 is made to let designers work effectively in high level languages and achieve fastest possible system throughput with them. Because the 8086 is memory based, it allows up to 30% shorter high level language object programs and correspondingly faster instruction fetching. And Intel lets you match your language precisely to your task with Pascal, PL/M, our ASM86 macroassembler, and ASM89 assembler. You'll get even more flexibility in the future with Intel's FORTRAN and COBOL.

Development tools for higher performance

To help designers shorten design cycles and save development costs in the '80s, Intel delivers a full complement of structured software and hardware development tools. Our revolutionary new RMX/86™ multitasking operating system, for example, puts you months closer to market with complete file manipulation, task scheduling, and interrupt capabilities. And since this software package is here today, you can start developing your applications software immediately.

To improve the performance and productivity of your entire development team, use Intel's Intellec® Microcomputer Development System and our ICE-86™ and ICE-88™ In-Circuit Emulators. They're the fastest tools available for developing and debugging 16-bit microcomputer systems. For even faster time to market, get Intel's already tested and debugged iSBC86/12A™ single board computer.

Meeting the demands of a new decade today

Everything you need to improve performance, reduce complexity, and speed your time to market is here from Intel today. For more information on our complete 8086 VLSI system solution, mail us the coupon on the other side of this page.

*HMOS is a patented Intel process.

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Your first step toward higher performance

How to get more information on 8086 VLSI system solutions.

To find out more about our solutions, fill out the information requested below and send it to Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Indicate what your particular interests are, including workshops, and we'll make sure you get the appropriate material. If you don't have a pair of scissors handy, give us a call at 408/734-8102 (Literature Department) and we'll rush the material out to you. Or call your local Intel distributor.

Intel wants to help you meet the performance requirements of the '80s. It all starts right here.

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Please put the letter corresponding to your yearly requirements in the line to the left of those products of interest.

w for 1-10 per year
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y for 99-999 per year
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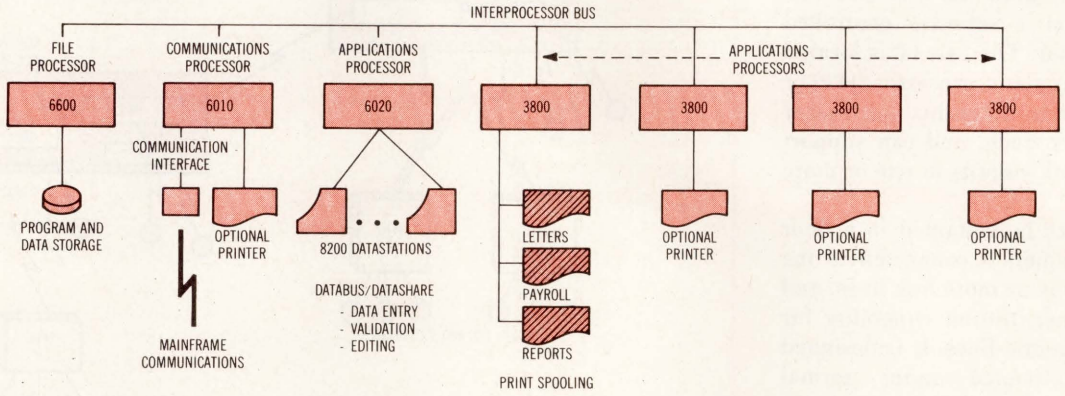
___ A 16-bit Microprocessors
___ B 8-bit Microprocessors
___ C Single-Chip Microcontrollers
___ D Peripheral Controllers
___ E RAMS
___ F EPROMS
___ G Bubbles
___ H Single Board Computers
___ I Development Systems
___ J Debug Tools
___ K High-Level Languages
(_____)
Indicate languages
___ L Macroassembler
___ M Operating Systems (RMX/86™)
___ N Telecom Products
___ O Military Products
___ P Workshops

Circle No. 100 for information.



ARCCOM configuration. Software products extend concept of resource sharing to communications. Communications processor handles all mainframe communications, while other system processors proceed with own tasks without communications overhead

in the family, ARCCOM 3270 is an interactive communications and emulation package that runs existing 3270 applications without mainframe hardware or software modification. The ARCCOM family, from Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, is compatible with such languages as COBOL, DATABUS®, RPGPLUS, and BASICPLUS. New high level language 3270 applications can be written for local processing and for operator-transparent mainframe inquiry.

A 6000-series processor that emulates a 3271 control unit handles communications between applications processors and the mainframe. The interprocessor bus connects the 6000 communications processor to the ARC system, and a 9481 communications adapter, synchronous modem, and leased lines connect it to the mainframe. Data transfer uses EBCDIC code and BSC protocol, at rates to 9600 bits/s. Provision is made for attachment of a local printer to emulate an IBM series 328X. A 6010 communications processor can emulate up to eight, and a 6020 up to 32 IBM 3277/328X devices.

Processor software (AC3271B) maintains a runtime screen display that specifies processor poll address, line and modem condition, number of transmitted and received blocks, and line errors. A trace feature provides a hex display of characters transmitted and received via the communications adapter for visual monitoring of the line during operation.

Emulator utility software (AP3277) allows any 3800 processor on the system to execute existing 3270 applications without modifying mainframe hardware or software. Utility software includes such features as status indication, keyboard entry blocking, automatic cursor positioning, field highlighting, repeat action keys, upper/lower case display, and auto skip.

The communications and emulation software is available without charge when ordered with new equipment. For those with existing equipment, there is a onetime $500 license fee. Monthly maintenance fee is $15.

Circle 521 on Inquiry Card

Multiplexing System Performs Remote Concentration

Microprocessor controlled 3400 LPS multiplexing system, designed to perform remote concentration functions, allows as many as 31 remote start/stop, BSC, and SDLC terminals to be linked to the host processor by single or multiple circuits. It will operate within the company's 3650, 3670, and 3690 systems, and will attach multiple remotely located terminals and cluster controllers, extending the network into areas where the full capabilities of a 3600 communications processor are not economically justified. The system, available from NCR Comten, Inc, 1950 W County Rd B-2, St Paul, MN 55113, adaptively multiplexes data from remote start/stop, BSC, and SDLC devices to a 3600 frontend or remote communications processor.

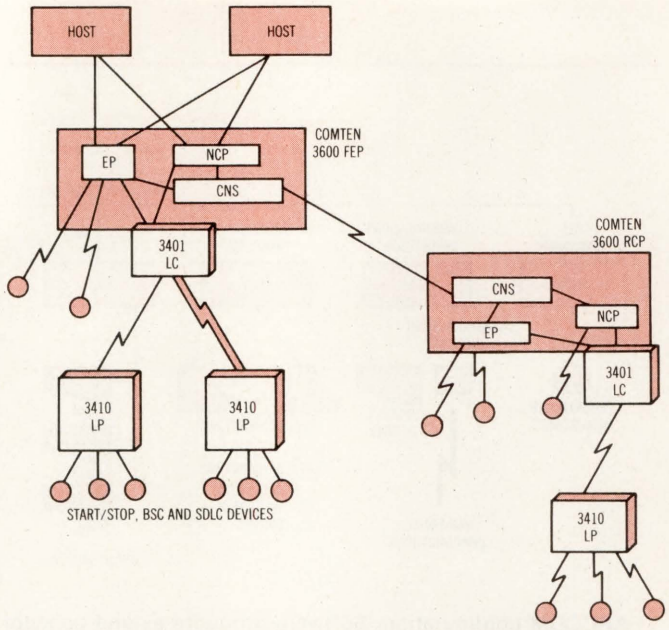
The system consists of three components: 3401 link controller (LC), one or more 3410 link processors (LP), and 3400 software. Both the 3401 and 3410 are based on a software controlled microprocessor. The 3410 LC is located at the 3600 frontend processor (FEP) or remote communications processor (RCP) network node, and can support up to four link circuits to one or more 3410 LPs.

The 3410 LP is contained in a floor standing cabinet, is connected to the 3410 LC via one or more link lines, and provides concentration capability for up to 31 terminal lines. It is designed to run unattended under normal operation. Any required reloads or diagnostics may be run from the 3600 site. The system supports LC to LP link speeds to 19.2k bits/s under a modified SDLC protocol. Terminal line speeds up to 9600 bits/s are supported for start/stop, BSC, and SDLC. Automatic baud rate detection is provided for start/stop terminals up to 1800 bits/s. The 3410 LP provides external clocking for terminals that are colocated and locally attached.

Software support of the system is under Comten emulation processing (EP), partitioned emulation processing (PEP), network control program (NCP), communications networking system (CNS), and data switching system (DSS). Software is generated under network definition procedures (NDP), and requires system control software release 62.0 and above.

The link processor system includes such features as error checking, data compression, and remote autodialing and autoanswer. It is transparent to terminals and software in an IBM 360/370/303X/40XX or compatible host computer. Cost effective networking can be implemented with no changes to host software or terminal operator procedures.

Circle 522 on Inquiry Card

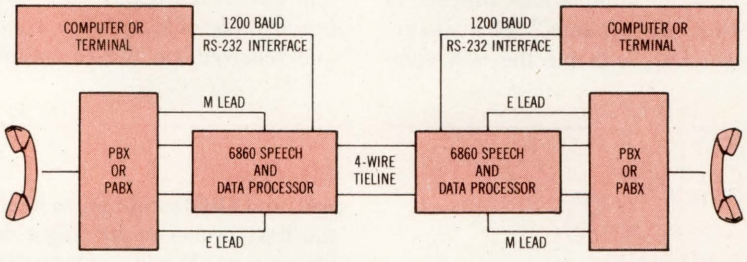


Typical 3400 LPS configuration. Total link speed of lines attached to 3410 LP can be larger than speed of link connecting it to 3401 LC. Terminal procedure delays, operator think time, half duplex protocols, and idle time on lines produce actual data character rates that are lower than full duplex link data rate

Processor Transmits Simultaneous Voice and 1200-Baud Data

Simultaneous transmission of speech plus full duplex, 1200-baud data over a 4-wire office to office tieline is the primary application of the 6860 speech/data processor, available from RFL Industries, Inc, Boonton, NJ 07005. Two offices can exchange 1200-baud data and at the same time the tieline can be used for a PABX to PABX speech circuit.

The speech processor portion of the system uses voice companding to provide a low noise circuit. E & M signaling



6860 speech/data processor arrangement. System offers low data distortion and speech of good intelligibility using C1-conditioned lines

(continued on page 34)

Introducing The Glitch Grabbers.™

Philips presents the two most original logic analyzers in the field. A 100MHz logic analyzer that can spot a 3ns glitch. And the only combination 10MHz logic analyzer and real-time scope on the market. Both brand new. Both with the most-wanted performance features. Both backed by Philips Test & Measuring Instruments, Inc. When there's a better, more innovative way to design new test equipment, rely on Philips to do it! Now, choose *your* Glitch Grabber.™

The PM3500 100MHz 16 Channel Logic Analyzer

- Performs state and timing analysis both synchronously and asynchronously.
- Choose binary, hex, octal, mapping, or timing display.
- 505 X 16 bits memory format, or two 249 X 16 bit active memories in compare mode.
- Internal triggering from word preset on front panel toggles.
- External triggering through separate input.
- Triggering can be delayed up to 9999 clock pulses, which can be set to walk or run through the data stream.
- Data input 5:1 probe tips matched for 100MHz operation and can be grouped or used singly.

The PM3540 10MHz Logic Analyzer and Real-Time Scope

- Accepts 16 channels of input data.
- Checks software and hardware together.
- Choose binary, hex, or octal coding.
- 64 X 16 bits active memory, plus separate 64 X 16 bit compare memory.
- Data input via 2 multi-lead probes, which permit up to 8 channel connections plus one ground connection per probe.
- Digital delay of up to 9999 clock pulses.
- "Store Trig" provides quick and convenient paging both upstream and downstream.
- Microproccessor- equipped for display and basic logic analyzer functions plus comprehensive self-testing.

For more information call 800-631-7172, except in Hawaii, Alaska and New Jersey. In New Jersey call collect (201) 529-3800, or contact Philips Test & Measuring Instruments, Inc., 85 McKee Drive, Mahwah, New Jersey, 07430.

From Philips, of course.

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CIRCLE 16 ON INQUIRY CARD

'Vise-grip' Contacts

TEST RESULTS

Test	Procedure	Results
Corrosive Atmophere	Ammonium Polysulfide Nitric Acid	Final R_C=9.3 m Ω Final R_C=8.4 m Ω
Salt Spray	MIL-STD-1344, Method 1001	No Damage R_C=11.7 m Ω
Humidity	MIL-STD-1344, Method 1002	No Damage R_C=14.8 m Ω
Thermal Shock	MIL-STD-1344, Method 1003	No Damage R_C=11.7 m Ω
Mechanical Shock	MIL-STD-1344, Method 2004	No Discontinuity
Vibration	MIL-STD-1344, Method 2005	No Discontinuity
Socket Durability	500 mating/ unmating cycles	Initial R_C=11.8 m Ω Final R_C=11.8 m Ω
Temperature Life	MIL-STD-1344, Method 1005, 1000 hours	Insulation Resistance > $5x10^9$ Ω Initial R_C=11.1 m Ω Final R_C=14.9 m Ω

PRODUCTS TESTED: IDS-26-G30 and IDH-26-S1-G30

Unique RN "vise grip" contact clamps cable firmly for gas-tight reliability (microphoto above). Total normal force is applied directly against cable. Vector arrows show normal force is maximized to clamp conductors tightly. No chance for gas penetration or corrosive buildup . . . even in hostile environments. And a special cut-out evenly distributes stress for long spring life and maximum reliability.

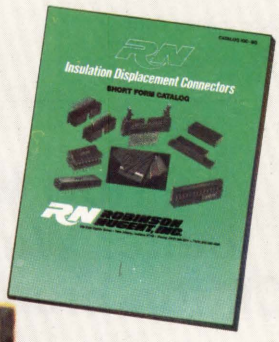
...assure gas-tight reliability

in RN IDC flat cable system

Robinson Nugent's unique contact design (microphoto shown at left) offers consistent, long-term dependability in your IDC flat cable interconnect system. Tests prove conclusively that RN "vise-grip" contacts maintain low contact resistance—even in corrosive atmospheres or under severe vibration. Plugs, sockets, edge card and transition connectors all provide the same low electrical resistance and gas-tight reliability—for a highly reliable, trouble-free flat cable system.

Simple, one-piece connector design allows high speed assembly using IDC tooling already in place. Fewer pieces mean reduced inventory. And you get assured compatability of cable, connectors and headers . . . because RN supplies them all.

Call or write today for the new Robinson Nugent IDC Flat Cable System catalog—complete with all specifications and technical details.



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CIRCLE 17 ON INQUIRY CARD

leads are included to interface the office switches.

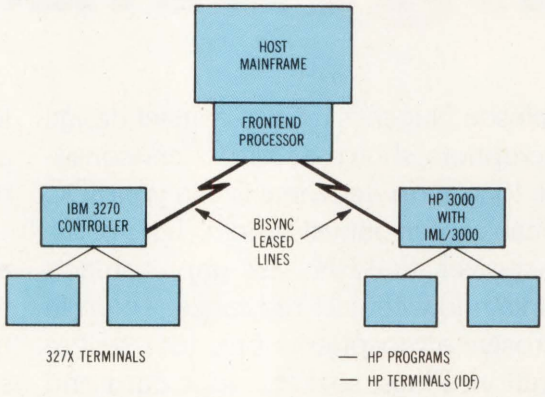
Data ports at each office, either from a computer, terminal, or other equipment are connected to the system via a 25-pin RS-232-C or CCITT V.24 connector. An FSK modem handles serial, binary, baudot, or ASCII code, 5- to 11-unit bit length. Data distortion is less than 1% and clear-to-send delay 140 ±10 ms. Self diagnostics, modem loopback switch, and LED display of digital functions are provided.

The data port may also be used in a supervisory/control system for carrying alarm, status monitoring, control, and other signals.

Circle 523 on Inquiry Card

Interactive Communication Enabled by Software Product

Interactive mainframe link/3000 (IML/3000) software makes interactive communication possible between HP 3000 series II or III computer systems and IBM or other mainframes that use IBM software, such as Amdahl, Itel, or Magnuson, using 3270 BSC protocol. IML interfaces with the synchronous communication line via the intelligent network processor (INP) recently introduced by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304 (*Computer Design*, Oct 1979, p 26.)



IML/3000 3270 emulator allows user written programs in high level languages and HP terminal users to communicate interactively with IBM and IBM compatible mainframes

Using IML, HP 3000 programs in COBOL, FORTRAN, BASIC, or the company's Systems Programming Language (SPL) can pass data to or read data from application programs on the mainframe via CICS or IMS.

The package also provides an inquiry and development facility (IDF), allowing HP 3000 terminals to be used as IBM 3277 or 3278 terminals connected to a mainframe. With IDF, it is possible to log on to timesharing option (TSO) to perform file maintenance, program development, or to actually enter data into host application programs. Used in conjunction with HP distributed network architecture (HP-DSN), IML/3000 makes data bases distributed across both mainframes and HP 3000 computers available online.

List price for the software product is $3500 (U.S.), plus $125/month for support. □

Circle 524 on Inquiry Card

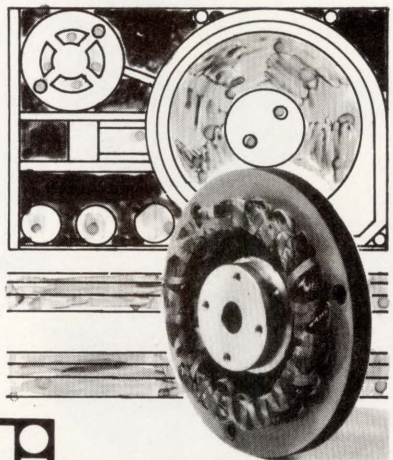
How to design a better Winchester drive: Clifton brushless dc motors.

Clifton's brushless dc motors for Winchester drives offer you these important advantages:

- Better speed control to help you meet tight specs
- Fewer linkages and moving parts, resulting in higher reliability
- Small size, for easier packaging and better air flow design
- Higher torque, for lower power consumption
- Optional control electronics in a single self-contained package

Plus, you get Clifton's over 30 years of experience in high technology rotary component design and manufacturing.

Clifton has the capability to provide a wide range of brushless dc motor packages to meet virtually any set of requirements. To review your needs, call Carey Walter at (215) 622-1000 today.



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Rumors of the tape drive industry's death were greatly exaggerated. In fact, these days a lot of people are all wrapped up in tape.

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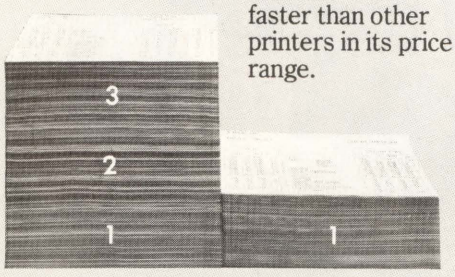
CIRCLE 19 ON INQUIRY CARD

Output for Versatec's

A new generation of OEM printer/plotters delivers more output for less money.

Faster printing. The new Versatec V-80 prints 1000 lines per minute, more than three times faster than other printers in its price range.

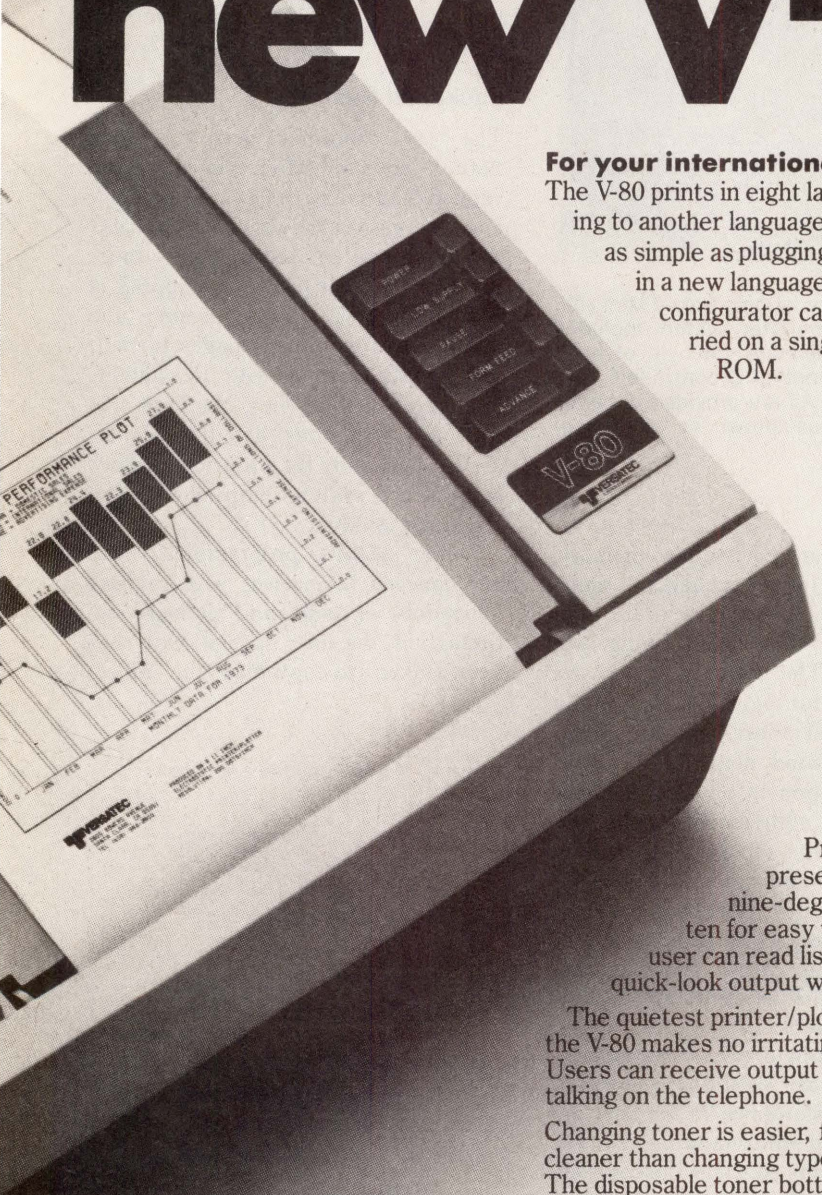


Graphics. The Versatec V-80 gives you better image quality than other printer/plotters. Get true high quality graphics with 200 dot per inch resolution. Plot an 11 by 8½-inch page in just seven seconds.

Hard copy from display. V-80, with an optional controller, makes quick, archival quality copies from storage tube displays or digital sources within twenty seconds.

Easy to integrate. Use V-80 with any popular computer. Styled to complement your computer-based system, the V-80 is suitable for any office or laboratory environment. The V-80 can be mounted directly into your system console, placed on a table, or be carried on its own optional utility stand. Weight is only 75 pounds.

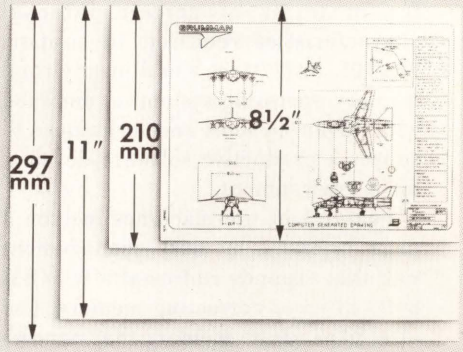
the 80's. new V-80.



For your international customers. The V-80 prints in eight languages. Changing to another language is as simple as plugging in a new language configurator carried on a single ROM.

The V-80 has been designed to meet both UL and VDE standards. Re-positioning one electrical plug adapts the printer/plotter to different voltage requirements.

Paper widths of standard 8½ and 11-inch *and* international A4 (210 millimeter "Portrait" and 297 millimeter "Landscape").



Easy to use. Printed output is presented on a nine-degree sloped platen for easy viewing. The user can read listings and other quick-look output without standing.

The quietest printer/plotter ever built, the V-80 makes no irritating clatter. Users can receive output even when talking on the telephone.

Changing toner is easier, faster and cleaner than changing typewriter ribbon. The disposable toner bottle inserts directly into the printer. No pouring. No mess. The toner is sealed away from hands and clothes.

Easy to maintain. Electrostatic writing is simple, because it's electronic rather than mechanical. Versatec has reduced mechanical part count to just 135, and that includes screws. Improvements in electronic design include microprocessor control, new LSI technology, and low power Schottky TTL logic. Fewer mechanical and electronic parts reduce spares requirements.

More profit. V-80 gives you better output specifications for less money. Excellent OEM margins assure more profit per system.

For more information, circle our readers' service number for the free brochure — "Output for the Eighties." To arrange a demonstration, call your local Versatec representative.

See the new V-80 at NCGA, Washington, D.C. and Siggraph, Seattle.

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Versatec European Headquarters
27/35 London Road
Newbury, Berkshire, England
Telephone: (0635) 42421
Telex: 847259

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Top of Line and Packaged End User Systems Added to Minicomputer Line

Naked Mini 4/95 and 4/97, an OEM computer, 30% faster than its predecessors, and a packaged end user system characterized as a "software factory," are high performance processors with memory management expansion capability to 8M bytes and an effective memory access time of 120 ns. From a hardware standpoint, the computers, introduced by Computer Automation, Inc, Naked Mini Div, 18651 Von Karman, Irvine, CA 92713, are similar in performance but differ in utilization.

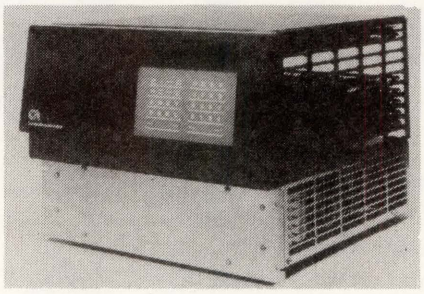
The 4/95, intended for OEM board level users, and the 4/97, for use in driving the PROTOS™ software system, differ in terms of certain internal characteristics required to support PROTOS. In PROTOS, a multiuser virtual memory operating system is combined with advanced tools and techniques to supply a productive software development environment.

Features of the machines include a page oriented memory management unit that expands addressability to 8M bytes of error correcting memory. Use of a 50-ns cache memory that handles approximately 85% of all read and fetch operations reduces overall access time to about 120 ns. Additional opportunities to increase throughput are provided when applications are structured to advantageously use hardware features.

Both units have a stack-relative addressing mode and 22 added instructions that use it, including stack-relative memory reference instructions. These enhancements contribute to efficient implementation of block oriented languages that can be measured in terms of faster CPU execution time. Another added class of instructions offers ability to access a bit field regardless of where it is in memory and without regard for word boundaries, providing efficient access to arrays of nonstandard size data types.

Board Level Computer

In the 4/95 design, engineers have combined memory management, cache memory, error correcting memory, wide memory (micro cache), and memory protection features to attain high performance while maintaining low price levels. The MMU translates the machine's 16-bit logical address into a 22-bit physical address and manages 16 page oriented maps of 2k bytes each. In addition to physical memory mapping and address conversion, the unit controls the access mode in each memory page and indicates status information. One of 16 maps is reserved for system programs, leaving 15 for user programs. DMA transfers are mapped to allow access to all physical memory locations.



Computer Automation's Naked Mini 4/95 board level computer system includes CPU, cache memory, 1M byte of error correcting memory, I/O controllers, and power supply. All are provided either in split chassis as shown or other configuration

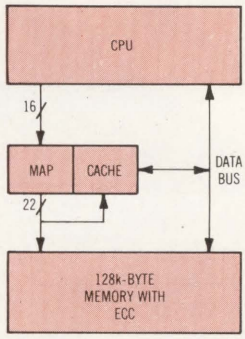
A 50-ns, 2k-byte cache memory integrated into the MMU board compensates for the slowdown in memory access associated with mapping. The set associative cache contains the contents of the most frequently addressed memory locations. Then, by monitoring all read addresses from CPU to physical memory, it can intercept an address when it contains the contents of that location.

A separate 64-bit memory array, microcache is a 125-ns, 4 x 16-bit wide memory that copies the last memory location addressed plus three adjacent locations into latches. A comparator determines if the next address to come down the bus is in one of the latches; thus capturing one-third of all instructions missed by main cache, and increasing the total hit rate to 90%.

Packaged System

The 4/97 computer used to drive PROTOS software offers the same advanced features as the 4/95. To ease use and increase productivity, AUTOMAP allocates program and file space to individual users. It provides mapping of files onto task virtual memory and allows users to replace pages in their virtual address space with the contents of regions of data files. Machine control, data structures, and flow control are supported by the proprietary block structured system implementation language, ALAMO.

Under ALAMO, programmers need not concern themselves with register allocation, or code and memory optimization because special care has been taken to optimize the object



Naked Mini 4/95 and 4/97 computers are based on CPU board, memory management unit board with 2k-byte cache memory having 50-ns access, and RAM board with error correction. Set associative cache contributes a 30% improvement in access time; added instructions further speed throughput

(continued on page 42)

ROLM's New ARTS Is A Fast Real-Time System. With WCS, It's Even Faster.

ROLM's Mil-Spec ECLIPSE® Computers now have a software/hardware combination that zeroes in on today's tough, real-time military applications.

The total package is fast, compact, and configurable. A real-time operating system designed for both time-critical and hostile environments.

ARTS (Advanced Real-Time System) expands the performance range of our Mil-Spec ECLIPSE line of computers by adding true real-time multiprogramming, multitasking capability. WCS (Writable Control Store) provides the additional hardware to access our microprogrammed processor and increase throughput for high-speed applications.

As a compatible subset to Data General's AOS (Advanced Operating System), ARTS is loaded with outstanding real-time features. It's configurable and

modular, providing memory support from 64KB to 2048KB. ARTS can be memory-only or disk-based, depending on the needs of the application. Other features include: high order language support, (FORTRAN 5, PL/I, DG/L™ system programming language), memory resident file structure, and efficient interprocess communications.

The optional hardware part of the package, WCS, maximizes the computing power of our Mil-Spec ECLIPSE processors. And at the same time, it minimizes the critical path execution time for high-speed functions or processes. In time-critical operations, specialized functions can be tailored precisely to the application.

ROLM's Mil-Spec ECLIPSE Computers with ARTS and WCS give military system designers the optimum system. It solves today's real-time problems... with tomorrow's technology.

That's Why We're #1 in Mil-Spec Computer Systems

ROLM MIL-SPEC Computers

4900 Old Ironsides Drive, Santa Clara, CA 95050.
(408) 988-2900. TWX 910-338-7350.

In Europe: Muehlstrasse 19, D-6450, Hanau, Germany,
6181 15011, TWX 4-184-170.

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CIRCLE 21 ON INQUIRY CARD

If you're an OEM or system builder, no doubt you've been subjected to the 8-inch Winchester hustle.

Well, Century Data thinks it's time to rack up the facts and lay them on the table.

First off, the 14-inch Winchester is rebounding. Just as predicted. And Century's new Marksman disk is the perfect example.

Sure 8-inch drives will be available some day. But can you afford to wait?

Today, the need for more storage and less cost is forcing many companies to go Winchester. And we think your best shot is our Marksman drive.

Marksman is the no-risk disk with enormous expandability and optional built-in intelligence. It's also one you can get today.

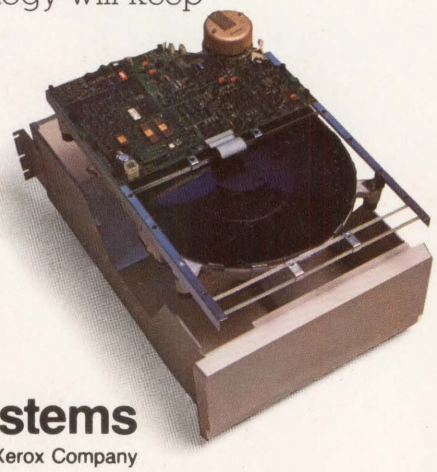
Built-in intelligence means you won't get behind your competition by spending months designing, testing and debugging your own disk controller. We've already done most of the work. You're up and running in days, not months.

Built-in growth means you won't have to start over when your applications increase. Marksman comes in 10, 20, and 40 MB models, and a lot more to come soon.

For more flexibility, Century offers everything from a 2½ MB Diablo cartridge disk to the 600 MB removable-pack Trident — with lots of mixed and fixed storage in between.

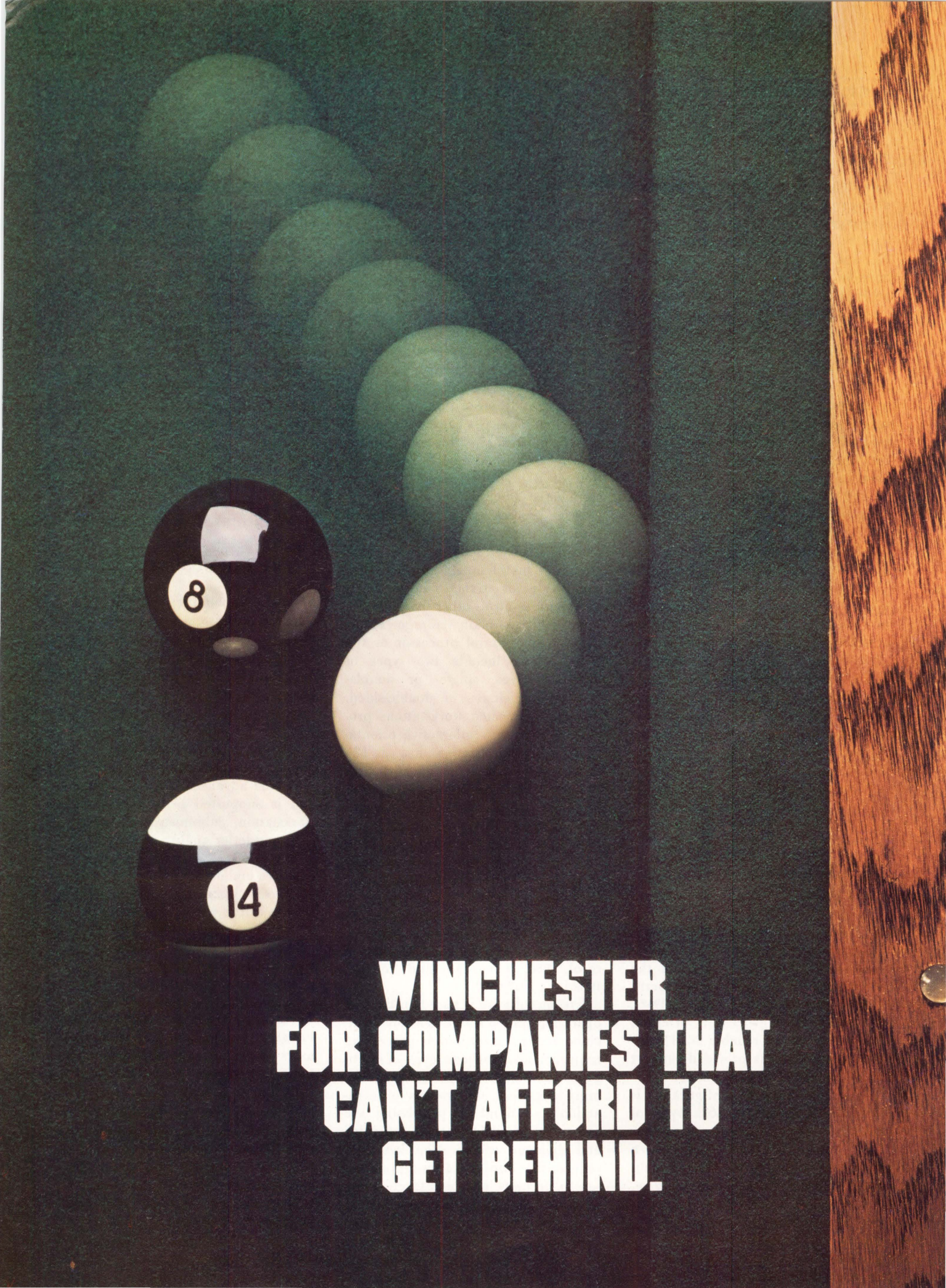
So if you can't afford to get behind, call Century Data, a Xerox Company specializing in mass storage for over 11 years. Our early delivery will put you ahead. Our advanced technology will keep you there.

Century Data Systems,
1270 North Kraemer Blvd.
Anaheim, CA 92806
Phone: (714) 632-7500



Century Data Systems
A Xerox Company

CIRCLE 22 ON INQUIRY CARD



WINCHESTER FOR COMPANIES THAT CAN'T AFFORD TO GET BEHIND.

code. Thus the time spent writing and debugging code is reduced. The language allows address arithmetic, data types including bits, bytes, double, and real, data structures, and recursion. I/O library and time/date and other standard utilities are provided.

PROTOS files are structured in a hierarchical resource catalog that provides direct access to all system resources. The system contains utilities for file management, task coordination, and system control. Its text processing package includes an interactive editor and document formatter. The editor contains a regular expression recognizer and supports local and global contexts; the document formatter enables users to produce attractive hardcopy printout.

Prices of the 4/95 range from $8500 for CPU, MMU with cache, and 128k-bytes ECC memory to $30,000 for a 1M-byte system with chassis and two power supplies. The 4/97 PROTOS system package will be available for delivery in October of this year. A typical system will consist of 4/97 computer, flexible and hard disc drives, line printer, and from two to eight terminals plus a virtual memory software system.

Circle 420 on Inquiry Card

Interactive Computer System Combines Functionality and Capacity

General purpose System 80 combines capacity and functionality of mainframes with low system cost. In the system, Sperry Univac, Div of Sperry Corp, PO Box 500, Blue Bell, PA 19424, has used microprocessor oriented hardware with fast reliable ECL LSI circuit design and has provided support for a wide range of peripherals.

Minimum hardware configuration is composed of CPU with 262k bytes of main storage, and microprocessor based control units connected to a 118M-byte integrated disc storage subsystem, console/workstation, diskette, and printers. The central processor complex contains CPU, control storage (COS), main storage, console/workstation, I/O channels, integrated control units, and integrated disc.

CPU architecture incorporates LSI microprocessors and microprogrammed logic. Reliability is enhanced by the ECL circuitry and the use of extensive parity generation and checking, automatic instruction retry, and main storage error correction. Growth is achieved by addition of an input/output microprocessor (IOMP) which supports the addition of three peripheral controllers and six additional communications lines. Processor performance can be increased 55% by addition of a high performance control storage (HPCOS).

Disc processing is accomplished through a microprocessor controlled channel that directly accesses main storage. This channel supports eight removable or fixed media discs. Peripheral controls other than disc are interfaced to main storage either through the central processor or the IOMP. These include two types of diskette drives, single- or double-density and single- or double-sided. Radially connected workstations provide the system's interactive orientation. Each workstation has a 12" (30-cm) display station with keyboard. Printers operate at up to 1200 lines/min and may be intermixed with card readers. Up to eight magnetic tape units can attach to the system. In addition, the system supports as many as eight communications lines. Asynchronous operation at 2400 baud is available with standard terminal interfaces; synchronous modes include Uniscope 100 and 200 and UTS 400 protocol, BSC, nine thousand remote, REM-1, and UTS 700.

System software is based on the OS/3 operating system with extensions to include today's information processing requirements. Fourteen levels of multiprogramming, a range of programming languages, and systems for transaction and database processing are supported. A screen format generator and dialogue specification language reduce the burden of programming screen formats and constructing interactive dialogues. For transaction processing, the machine offers the OS/3 information management system for online query and update functions. IMS interfaces with the CODASYL defined database management system facility to provide multiple users with concurrent access to database information.

First deliveries are scheduled for December. Purchase prices range from $55,869 to $94,647. Program products are priced separately; with software, maintenance, and support, a typical system will incur charges of from $2469 to $9154/mo.

Circle 421 on Inquiry Card

Sophisticated Software Capabilities Form Office Automation System

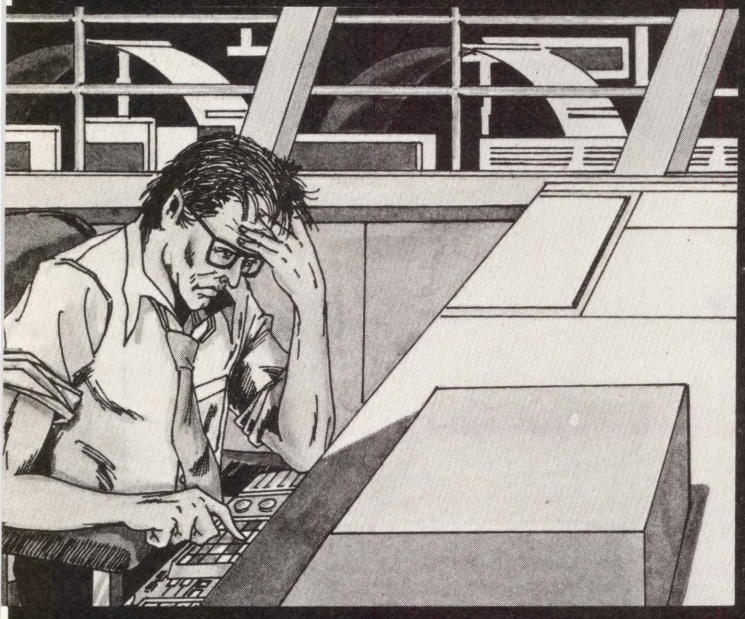
Software capabilities of the Office Automation System let users perform data processing and information management functions from a single workstation. Operating on any 50 Series computer system, the software, introduced by Prime Computer, Inc, 3 Newton Executive Pk, Newton, MA 02165, encompasses word processing, management communications and support, and advanced text management, and is supported by a management workstation, administrative workstation, and letter quality printer.

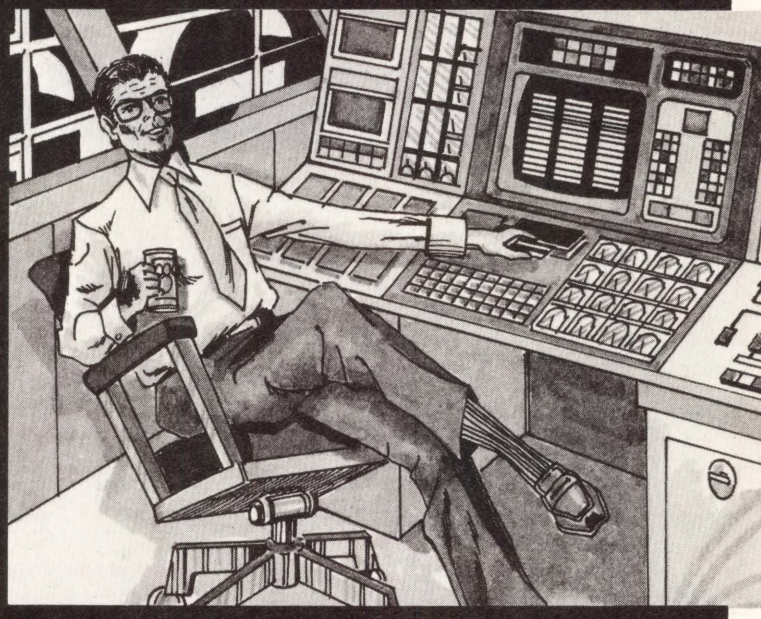
The Office Automation System operates under the interactive PRIMOS multiuser operating system which resides in the virtual address space of all 50 Series processors. This virtual memory and embedded design is complemented by time scheduling, memory management, and procedure data sharing. Distributed Processing Terminal Executive (DPTX) and PRIMENET networking software allow users to create complex communications networks.

Designed to interactively support many users, each able to perform multiple tasks from a single workstation, the system is multifunctional, operating simultaneously with normal data processing functions. It uses the PT45, a block mode terminal, as a management workstation; the PT65, an intel-

(continued on page 46)

Put an end to program reloading.



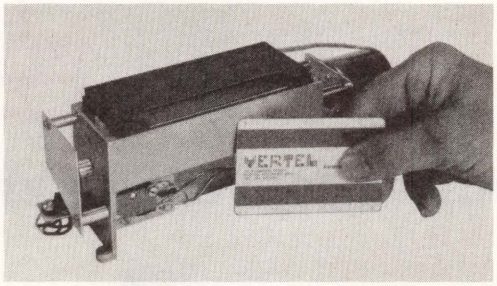


Set it up once . . . and forget it with the KILOBYTE CARD™ READER / WRITER.

With the Vertel KB-31 System, there is no longer any need to manually enter the same program more than once. Simply enter the program into the system, as you normally would, then let the system record the program on our KILOBYTE CARD with our KB-31 Microloader; when you are ready to re-use that program simply insert the KILOBYTE CARD into the KB-31 and your program will be loaded automatically into your system.

Designed for microprocessor based systems, this rugged, low cost*, field-proven performer is ideally suited for everything from intelligent terminals and instrumentation to machine tool controls and test equipment.

*As little as $192 in OEM quantities.



The 4-stripe magnetic KILOBYTE CARD can record up to 1,088 eight-bit bytes and with the microloader, it is the ideal peripheral for parameter loading, field program modifications, and user activated diagnostics.

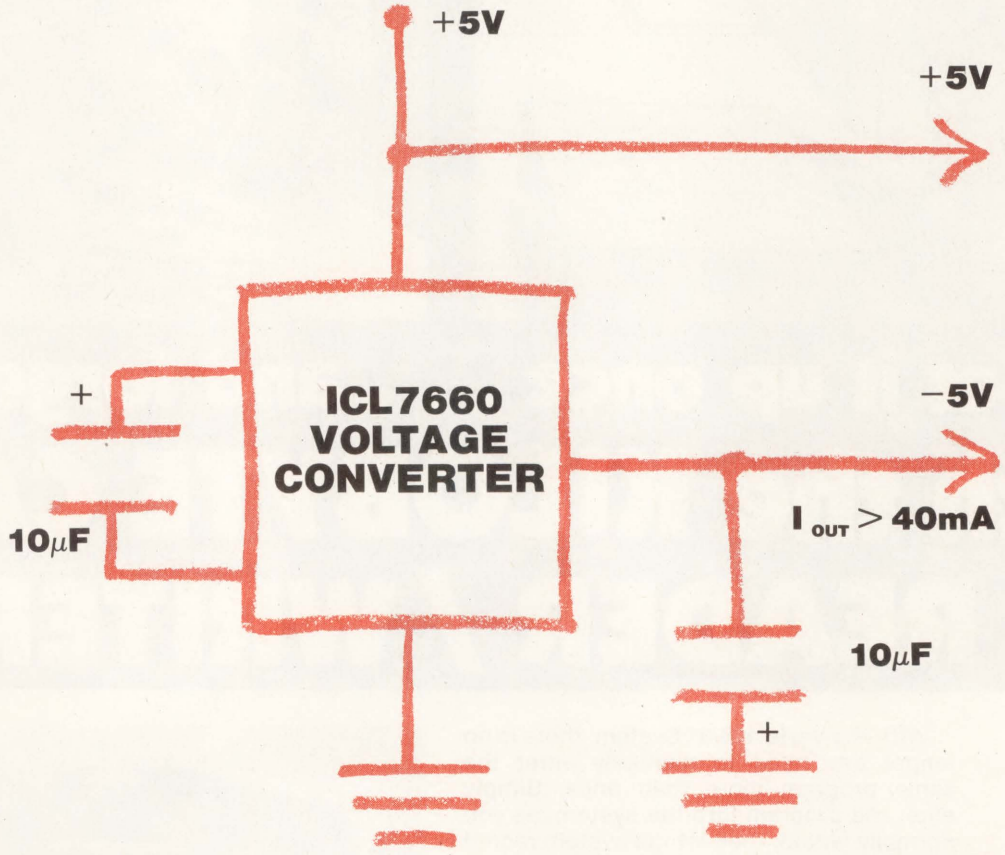
To learn how the KILOBYTE system can benefit your operations, call or write today for details on our free, thirty-day trial offer.

VERTEL

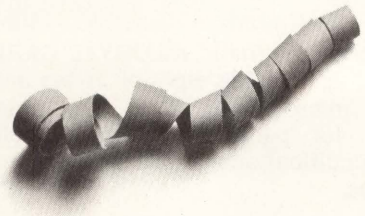
CIRCLE 23 ON INQUIRY CARD

125 ELLSWORTH STREET, CLIFTON, N.J. 07012 [201] 472-1331

OF COURSE YOU NEVER VOLTAGE CONVERTER.



POWER CONVERSION EFFICIENCY −98% @R_L=5KΩ



HEARD OF A MONOLITHIC WE JUST INVENTED IT.

+5V IN. −5V OUT.

Now, you can power your analog circuitry from your digital power supply. With a single chip. The ICL7660 monolithic voltage converter generates the negative voltages required by the analog functions in your system. Or, one ICL7660 provides −5V for a board-full of dynamic RAMs. +5V in. −5V out. Or, +1.5V to +10V in and −1.5V to −10V out. Require higher negative voltages? Cascade 7660's. Need more current? Just put 'em in parallel.

EFFICIENCY PLUS.

Intersil's MAXCMOS™ process brings you another first. A monolithic voltage converter with a voltage conversion efficiency of 99.9% ($R_L = \infty$). Power conversion efficiency of 98% ($R_L = 5K\,\Omega$). And I_{OUT} capability greater than 40mA ($R_{OUT} = 55\,\Omega$). You simply can't beat it. Period.

NO MORE KLUGES.

One chip and two caps. Put 'em wherever you need 'em. And the ICL7660 virtually eliminates EMI problems caused by inductive converters.

GOOD NEWS.

- Monolithic
- Short circuit protection
- Latch-up proof
- 1.5 to 10V operation
- Direct parallelling for more output current
- Operates in simple voltage multipliers: $V_{OUT} = -nV_{IN}$.

MORE GOOD NEWS.

The ICL7660 monolithic voltage converter costs just $1.95 in lots of 100 (8-pin epoxy DIP). Be sure to ask for quantity prices.

THE SYSTEMS APPROACH.

The Intersil MAXCMOS™ process, coupled with our broad experience in data acquisition products, has led to a continuing series of high performance, low-power analog and data conversion products. Analog products that operate from a ±5V supply. And now, a monolithic voltage converter that powers analog functions from your digital supply.

MORE INFORMATION?

Call your Intersil Sales Office, Franchised Distributor, or return the coupon below. The ICL7660 is available now. In prototyping or production quantities.

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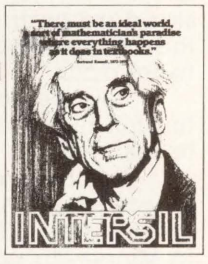


Gentlemen:

+5V in and −5V out? Monolithic? Send me the details on your ICL7660.

_____ While you're at it, send me your 20" x 24" Bertrand Russell poster.

Name_____

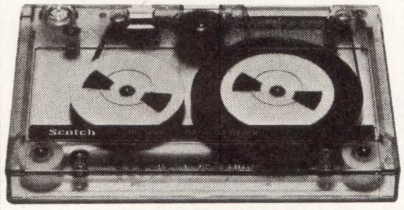
Company_____

Address_____

City_____ State_____ Zip_____

CD 680

THE FIRST DATA CARTRIDGE THAT ALWAYS FINISHES LAST.



3M's DC-300-XL Data Cartridge always finishes last because it records and stores at a field-tested rate of 6400 bpi on 450 feet of tape. And that's 150 feet more than standard data cartridges.

Which means you won't have to change it so often. And you'll have fewer cartridges to mess with. Or lose.

Like all 3M DC-300-A data cartridges, the DC-300-XL has the same metal baseplate. And the ANSI three-point positioning system.

What's more, it's the exact same size as other 300-foot cartridges. So you can use it in any drive that accepts standard cartridges. Yet the DC-300-XL stores 50% more data.

You see, sometimes finishing last has its advantages, too.

For information about where to get the DC-300-XL, call toll-free, 800-328-1300. In Minnesota, call collect: (612) 736-9625. Or write: Data Products/3M, 223-5E, 3M Center, St. Paul, MN 55101.

3M

CIRCLE 25 ON INQUIRY CARD

ligent editing terminal, as the administrative workstation; and the 3175 letter quality printer for hardcopy output.

Word processing capabilities of the system, derived from the first software module, include full text creation and editing, full deletion and insertion capabilities from different documents, footnote handling, and conversion of document sizes. This module operates alone or in conjunction with the management communication and support module which provides electronic mail and administrative support, and with the text management module.

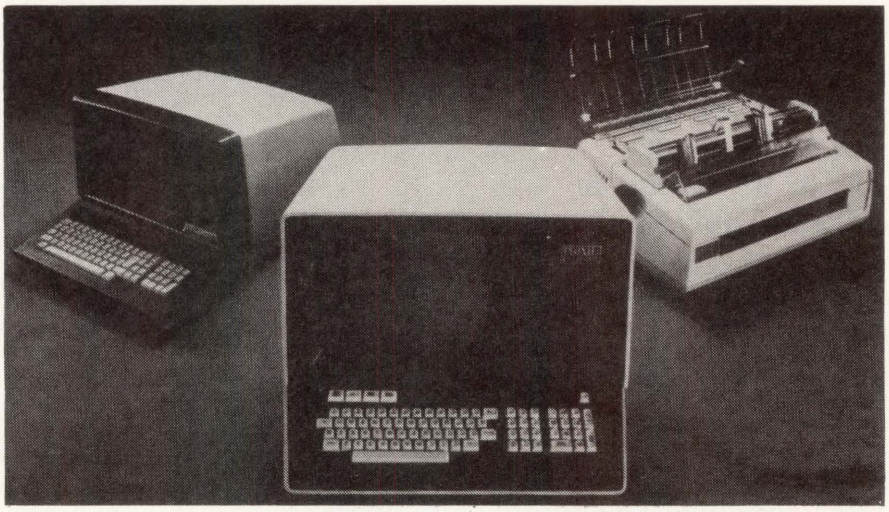
The workstations both have multiple function keys to enter commands under edit mode. The administrative station provides formatting functions, performing all data manipulation within the terminal itself to leave the CPU free for other users. Both stations have an industry standard 80 char x 24 line display and run at baud rates from 300 to 9600.

Text created using the word processing module can be electronically distributed by the management communication and support module which offers a sophisticated filing and retrieval function for originators and recipients of communications. The software also maintains personal diaries and schedules for managers. Diary and in-basket functions process notes and messages, and handle scheduling of appointments. Users can review mail and appointment schedules by simply logging on to a terminal.

Mainframe level capability of the system is used by the advanced text management module to provide a 60,000-word multilanguage dictionary that is user maintained, allowing addition of nomenclature and trade or generic names used in various industries. This dictionary provides for automatic hyphenation, proofreading, and language translation.

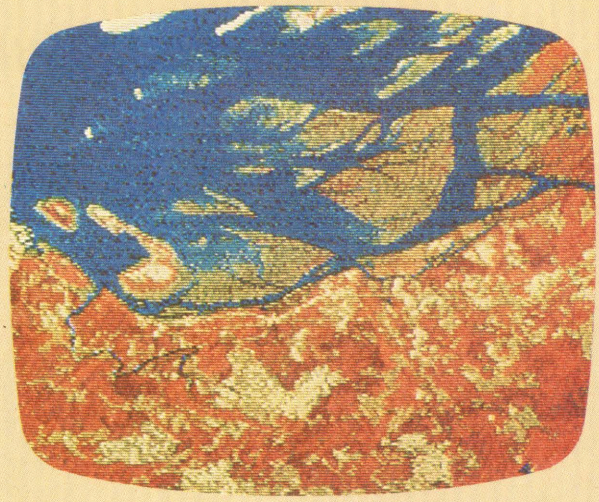
The Office Automation System operates on 50 Series computer systems with 512k bytes of main memory and a magnetic tape unit. A typical system for 25 users includes a 550 CPU, 5 administrative workstations, 20 management workstations, and 2 letter quality printers; price for this hardware plus necessary disc storage, software, and interfaces is approximately $250,000. Software modules are also priced individually; $15,000 each for word processing and management communications, and $10,000 for advanced text management.

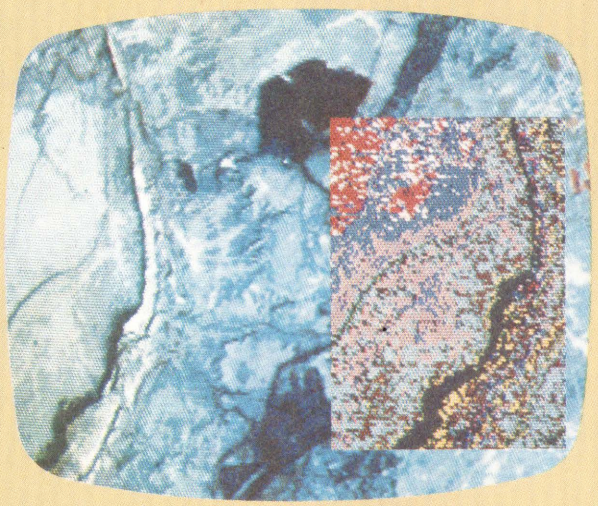
Circle 422 on Inquiry Card



Integral to Prime Computer's Office Automation System, management workstation (left), administrative workstation (center), and letter quality printer (right) combine with 50-Series processors and modular software to create, access, and retrieve information generated

Image processing. Your way.





Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

The GMR-270 combines the best features of our proven GMR-27 line of high speed graphic display systems with a special package of sophisticated image processing features. The result is a modular image processing system that can be furnished with any or all of the following:

- Convolution
- Image multiplication and ratioing
- Zoom and pan
- 512 x 512 panning window on a 1024 x 1024 image
- Function memories
- Pseudo-color tables
- Video digitizers with frame averaging
- Split screen and image toggling
- Full graphics and alphanumerics
- Up to four overlay memory planes
- Independent cursors
- Trackballs and joysticks
- External synchronization
- Plug compatible interfaces for most minicomputers

In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 512 to 1024 x 1024.

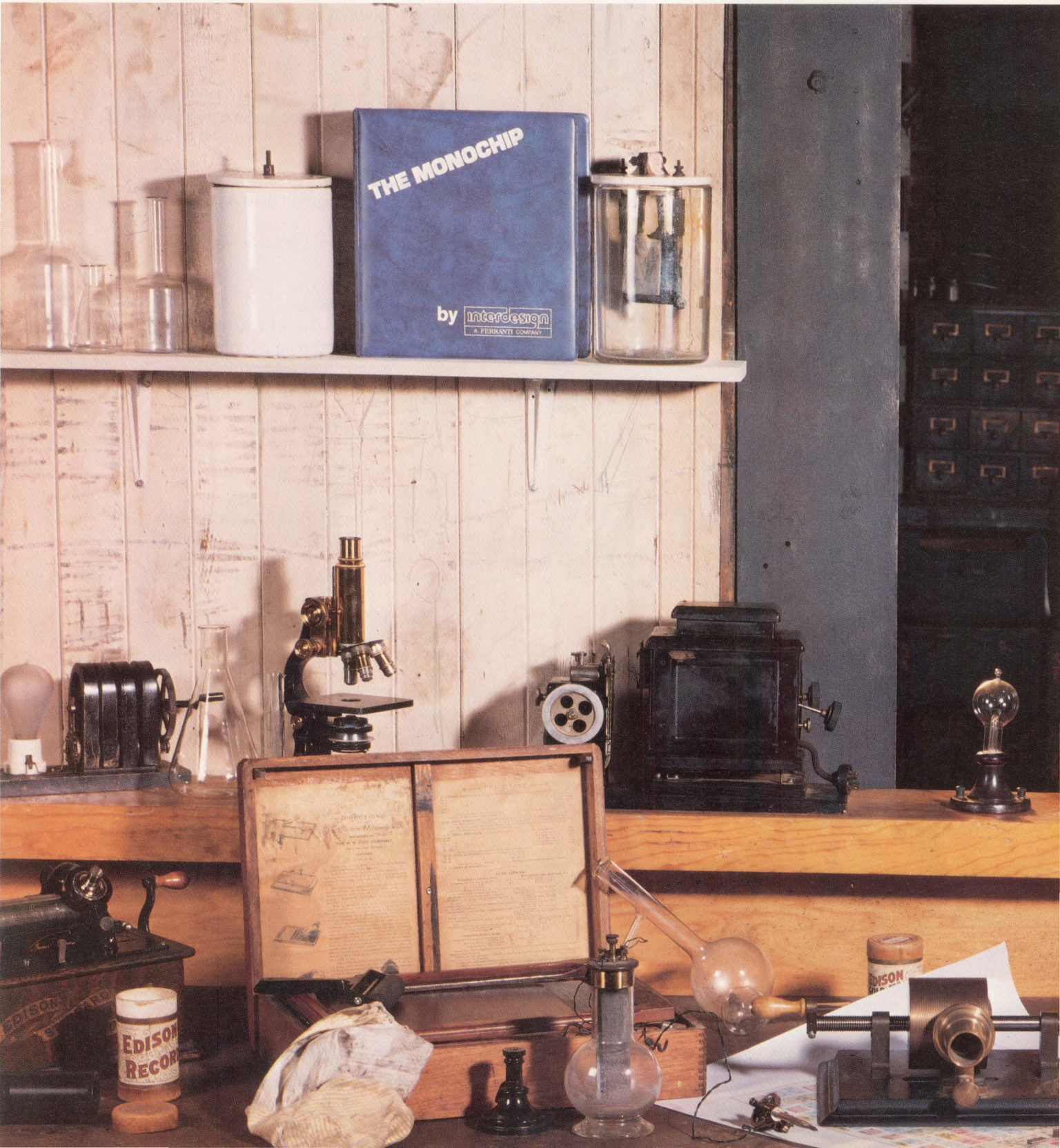
So, whether you want to analyze images from outer space or monitor a process in a plant, Grinnell has a system that can do it. For detailed specifications and/or a quotation, call or write today.

Photographs provided by Stanford University Department of Applied Earth Sciences, Palo Alto, California.

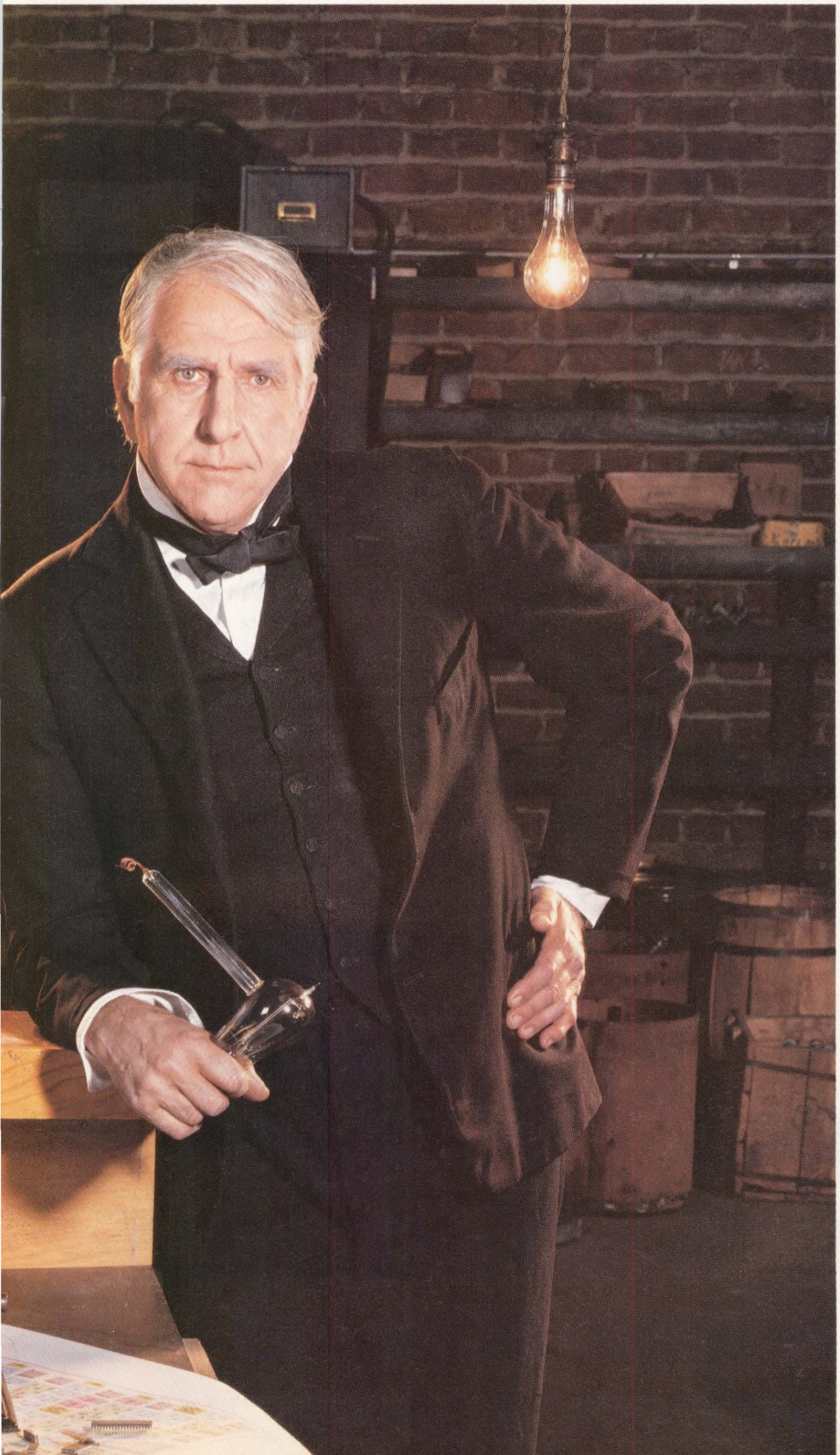
GRINNELL SYSTEMS

2159 Bering Drive, San Jose, California 95131 (408) 263-9920

CIRCLE 26 ON INQUIRY CARD


THE MONOCHIP
by Interdesign
A FERRANTI COMPANY
EDISON
RECORD

If Thomas Edison had used a Monochip,™ think how far he could have gone...

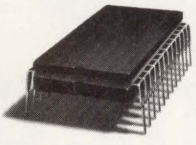


If Thomas Edison had used a Monochip,™ his electric pen might have been a color copy machine. His lightbulb might have been a laser. And his phonograph might have been a stereo system. Why? Because with Monochip, IC turnaround time could have kept pace with the speed of his imagination and the limitations of his budget.

Monochip is the semi-custom IC. That means its circuit components—the first five layers—are already in place when you start designing. All you do is tell us how to connect them to make the circuit your application requires. Working from your layout, we etch the sixth layer and deliver prototypes in only 6 to 8 weeks for $5,000 or less. Once you've approved them, we'll make production runs of 1,000 to 500,000 parts. It's that easy. Monochip Design Kits are only $25 to $59 each, and include everything needed to develop your own custom linear, CMOS, NMOS, CML or bipolar IC.

There's no telling what Edison might have designed if he could have used a Monochip. Now, just imagine how far *you* can go. Call or write for more information. Interdesign, 1255 Reamwood Avenue, Sunnyvale, CA 94086. (408) 734-8666.

Interdesign



Monochip.™ the semi-custom IC.

Interdesign is a Ferranti Company.

CIRCLE 27 ON INQUIRY CARD

Systems and Peripherals Added to Intelligent Modular Terminals

Display and printer based systems, peripherals, and an advanced programming language increase flexibility in configuring workstations while protecting against equipment obsolescence. Included in the announcement, made by Burroughs Corp, Detroit, MI 48232, were BMT systems—MT 300 printer based validation and receipt terminals, MT 700 programmable display based terminals, and MT 900 series general purpose displays—and a Transaction Programming Language (TPL) compiler for use on the company's large systems. TP 300 series journal, validation and receipt, universal document, and passbook printers; microcassette; TP 500 transaction authorization system; and TP 100 keyboards further extend the line. All terminals provide freestanding intelligent modular workstations. Display screens, keyboards, printers, and other components are separate units that can be combined to fit specific requirements.

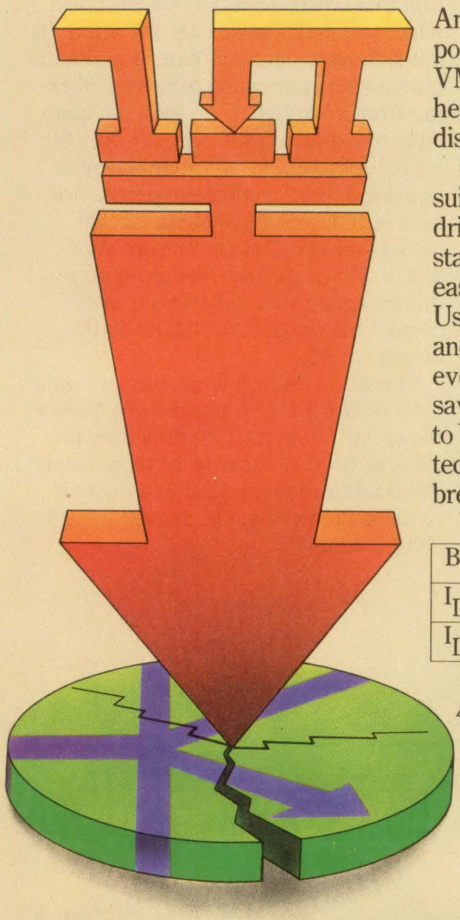
All terminals incorporate a microprocessor that supplies processing intelligence for displays, printers, keyboards, and related devices, and for application programs, data storage, and peripheral control. The processor enables terminals to operate online to host computers or as independent units for offline applications. Terminals can communicate with the company's host computers and with those of other manufacturers. They provide a choice of standard data communications protocols with data transfer rates ranging from 1200 to 38,400 bits/s, and can share communications lines with other terminals and terminal computers.

Peripheral interface throughout the series is accomplished by means of a serial I/O subsystem that acts as a general interface between the microprocessor subsystem and peripheral devices. Serial connection consists of a single serial I/O port on each host system and an I/O port on each peripheral. Reliability of the units is enhanced by a confidence test routine that operates each time the system is turned on, as well as a maintenance routine that tests individual components.

MT 300 printer based terminals feature either a 4.5 or 8.5" (11.4- or 21.6-cm) validation/journal printer which houses the microprocessor. A 44-key numeric function keypad and 40-char Self-Scan™ display are also standard. Optional are a 5 or 9" (12.7- or 22.9-cm) display monitor.

(continued on page 52)

Siliconix VMOS ends bipolar dominance



Announcing a breakthrough in power economy: new Siliconix VMOS Quad power FETs. They're here today, in volume, and on distributor shelves.

Our new Quads are ideally suited to power today's peripheral drive equipment. Housed in one standard 14-pin DIP, Quads mean easier, more economical handling. Use automatic insertion equipment and you lower production costs even further. Add this to the savings you gain when you switch to VMOS (no predrivers, no protective circuitry) and you've got a breakthrough in power economy.

VQ1000 Specifications

BV_{DDS}	60	$t_{(on)}$, $t_{(off)}$	10
$I_{D\,(on)}$	0.3	$P_{D\,(max.\,total)}$	1.2
$I_{D\,(on)\,pulsed}$	1.0	$R_{DS\,(on)}$	5.5

For more information call (408) 496-6660. Or write "VMOS Quads" on your business card and send it to: Siliconix Inc., P.O. Box 4777, Santa Clara, CA 95054.

Siliconix

The Quad breakthrough in power economy

CIRCLE 28 ON INQUIRY CARD

If you're going to copy it, at least do it right.

You see them every day.

Copycat terminals, with flashy features, all claiming to be as good as the renowned Dumb Terminal® video display terminal. Some even claim the same reliability that made the Dumb Terminal a household word.

But none can claim the ADM-3A's field-proven average of 15 months between service calls. Which means you spend less time and money on repairs. That's why the Dumb Terminal has become the industry standard—and why we've sold over 100,000 of them. It makes us feel that our extensive burn-ins and grueling quality control have been worth it.

We didn't load the Dumb Terminal with fancy frills—just dependable features that get the job done. Like a 12" diagonal screen, full or half duplex at 11 selectable data rates (75-19.2K baud), 1920 characters in 24 rows of 80 letters, RS232C extension port, and direct cursor addressing. Plus a host of sensible options. All for just $895.

DUMB TERMINAL. SMART BUY.

So don't be fooled by Dumb Terminal imitations. Because there's simply no substitute for Dumbness.

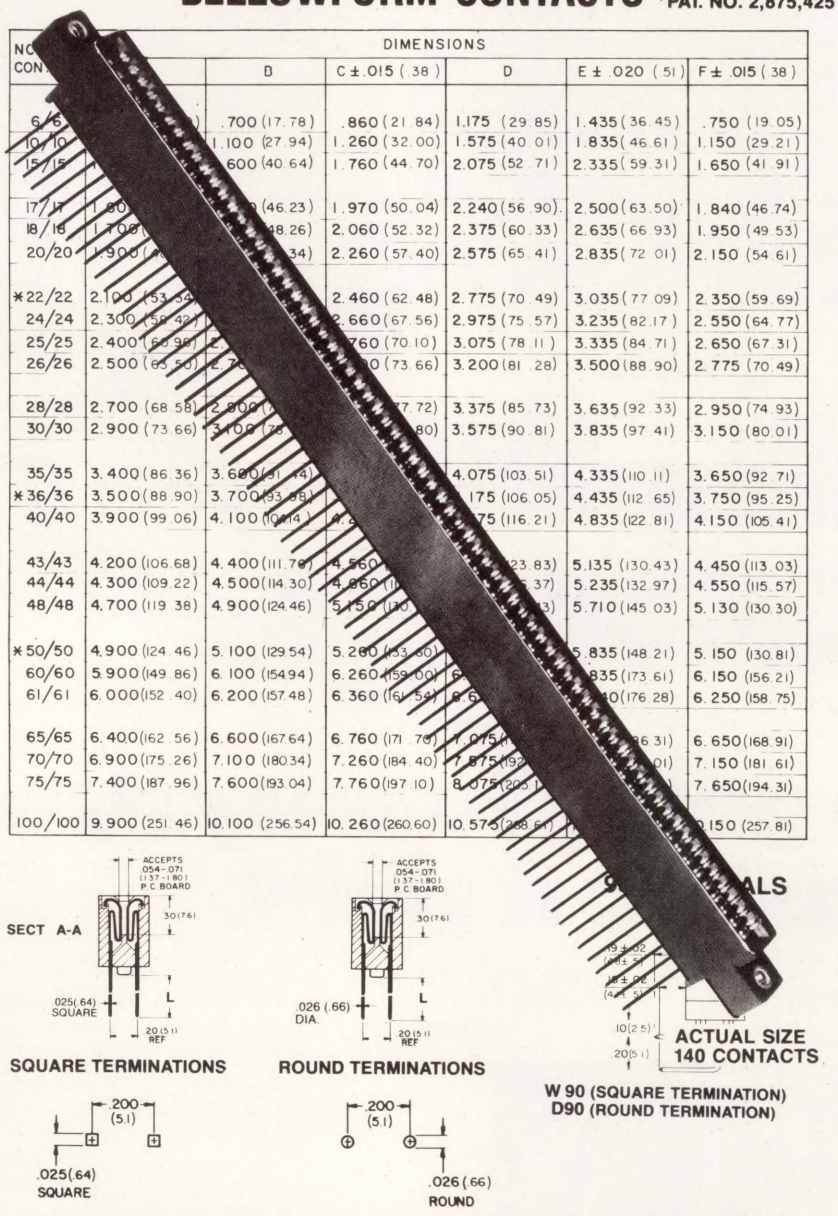
Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803, 800/854-3805. In California 714/774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: San Francisco 408/263-0506, Los Angeles 213/454-9941, Chicago 312/279-5250, Houston 713/780-2585, Philadelphia 215/245-1520, New York 212/594-6762, Boston 617/423-1510, Washington, D.C. 301/459-1826, England (04867) 80666.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

Dumb Terminal® is a registered trademark of Lear Siegler, Inc.

CIRCLE 29 ON INQUIRY CARD

4 THRU 200 CONTACTS
.025 (.64MM) SQUARE TERMINATION
.026 (.66MM) ROUND TERMINATION
DUAL READOUT .100" x .200" GRID
BELLOWFORM CONTACTS *PAT. NO. 2,875,425



NO. CONT.	DIMENSIONS					
	A	B	C ± .015 (.38)	D	E ± .020 (.51)	F ± .015 (.38)
6/6		.700 (17.78)	.860 (21.84)	1.175 (29.85)	1.435 (36.45)	.750 (19.05)
10/10		1.100 (27.94)	1.260 (32.00)	1.575 (40.01)	1.835 (46.61)	1.150 (29.21)
15/15		600 (40.64)	1.760 (44.70)	2.075 (52.71)	2.335 (59.31)	1.650 (41.91)
17/17	1.80	(46.23)	1.970 (50.04)	2.240 (56.90)	2.500 (63.50)	1.840 (46.74)
18/18	1.700	48.26)	2.060 (52.32)	2.375 (60.33)	2.635 (66.93)	1.950 (49.53)
20/20	1.900	34)	2.260 (57.40)	2.575 (65.41)	2.835 (72.01)	2.150 (54.61)
*22/22	2.100 (53.34)		2.460 (62.48)	2.775 (70.49)	3.035 (77.09)	2.350 (59.69)
24/24	2.300 (58.42)		2.660 (67.56)	2.975 (75.57)	3.235 (82.17)	2.550 (64.77)
25/25	2.400 (60.96)		760 (70.10)	3.075 (78.11)	3.335 (84.71)	2.650 (67.31)
26/26	2.500 (63.50)		0 (73.66)	3.200 (81.28)	3.500 (88.90)	2.775 (70.49)	
28/28	2.700 (68.58)		77.72)	3.375 (85.73)	3.635 (92.33)	2.950 (74.93)
30/30	2.900 (73.66)		80)	3.575 (90.81)	3.835 (97.41)	3.150 (80.01)
35/35	3.400 (86.36)			4.075 (103.51)	4.335 (110.11)	3.650 (92.71)
*36/36	3.500 (88.90)			175 (106.05)	4.435 (112.65)	3.750 (95.25)
40/40	3.900 (99.06)			75 (116.21)	4.835 (122.81)	4.150 (105.41)
43/43	4.200 (106.68)			23.83)	5.135 (130.43)	4.450 (113.03)
44/44	4.300 (109.22)			37)	5.235 (132.97)	4.550 (115.57)
48/48	4.700 (119.38)			3)	5.710 (145.03)	5.130 (130.30)
*50/50	4.900 (124.46)				5.835 (148.21)	5.150 (130.81)
60/60	5.900 (149.86)				835 (173.61)	6.150 (156.21)
61/61	6.000 (152.40)				40 (176.28)	6.250 (158.75)
65/65	6.400 (162.56)				86.31)	6.650 (168.91)
70/70	6.900 (175.26)				01)	7.150 (181.61)
75/75	7.400 (187.96)					7.650 (194.31)
100/100	9.900 (251.46)					10.150 (257.81)

For our nearest direct sales representative or distributor, see your electronics directory.

CONTINENTAL CONNECTORS

CONTINENTAL CONNECTOR CORPORATION ▪ WOODSIDE, NEW YORK 11377
PHONE: (212)899-4422

A programmable display based terminal system, the MT 700 uses programming logic to provide explicit prompting instructions to the operator. This unit offers 5, 9, or 12″ (12.7-, 22.9-, or 30.5-cm) screen sizes, and up to 96k bytes of programmable RAM. Application programs are written in TPL; object programs are loaded from the host, an optional controller, or from microcassette.

Emulating the TD 830 display system, the MT 900 series uses a 9 or 12″ (22.9-or 30.5-cm) display and application program. Users have three keyboard options and may attach journal printer and 80k- or 160k-byte microdisc unit.

Printer models added to the series communicate directly to the host terminal through the standard serial I/O interface or can be addressed separately on a data communications line. Included in the range are the TP 323 validation and receipt printer and the TP 334 journal frontfeed printer that can handle 2-ply, 8″ continuous feed paper. Universal document and passbook printers TP 364/374 handle single or dual frontfeed forms, passbooks, or 8.5 or 15.5″ continuous forms. TP 384/394 are capable of posting multipage passbooks up to 8.5″ wide.

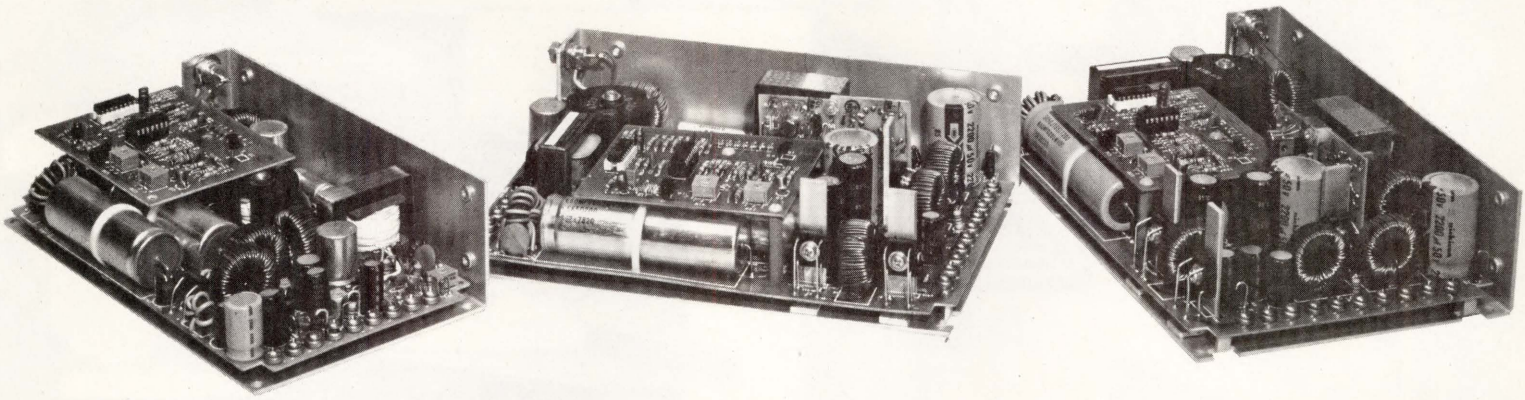
The TP 480 microcassette serves as program loader for RAM memory or to capture transaction input data for batch processing. Encoding capacity is 100k bytes. TP 510 magnetic stripe reader enters account numbers when a magnetic card is passed through the slot in the reader. It is a manually driven device which provides Track II or III capability to a host terminal.

Keyboards for use on BMT systems include the TP 110 alphanumeric transaction keyboard which consists of 59 keys, 6 special purpose keys, 5 function keys, and 6 indicator lights. TP 119 source data keyboard is a keypunch style unit; and TP 130 is an expanded alphanumeric function keyboard with 13-key numeric keypad, 62-key typewriter style keyboard, 22 function control keys, and 9 user definable function keys.

Circle 423 on Inquiry Card

MULTIPLE OUTPUT SWITCHING POWER SUPPLIES

THE SWITCHER COST BREAKTHROUGH YOU'VE BEEN WAITING FOR!



Power/Mate introduces Econo/Switch Multiple Output Switching Power Supplies priced to give substantial savings, yet provide the performance and reliability you depend on in a quality switcher.

The use of Power/Mate's new monolithic chip permits the reduction of parts count by 20% for a much higher MTBF, backed up with a two year warranty. Reliability has been greatly improved by use of computer-aided "worst-case analysis," individual testing of every IC and semi-conductor, and a comprehensive burn-in program.

These carefully packaged units have extremely high component density for maximum wattage per cubic inch. The standard unit has a 5V primary regulated output and two 12 or 15V regulated outputs, plus 5V and 24V semi-regulated outputs. Special units are manufactured to order with voltages specified from 5 to 28V for each of the three regulated outputs and 5 to 50V for the two semi-regulated outputs. Total continuous output power of the unit is 100, 200 or 300 watts. (See charts)

The Econo/Switch multiple output supply gives you exceptional versatility, combined with reliability, efficiency and compactness... at low cost.

Features.

- Up to five outputs, three regulated and two semi-regulated.
- Choice of voltage and current on all outputs up to maximum wattage total.
- Voltage adjustable on all regulated outputs.
- Brownout protection.
- OVP standard on primary output.
- Overload protection.
- Short circuit protection.
- Reverse polarity protection.
- Soft start protection.
- Adjustable current limiting on regulated outputs.
- Meets UL and CSA standards.
- Convenient 2-surface mounting.
- Convection cooled.
- Remote sensing.
- Advanced EMI filtering.
- Isolated Returns. (Note 3)

ESM-100 Series—100 Watts $199.

	Model	Output 1	Output 2	Output 3	Output 4	Output 5	Max. Cont. Output Power
Standard Models	ESM-100-5001	5V@10A	12V@3A	12V@3A	5V@2A	24V@2A	100W
	ESM-100-5002	5V@10A	15V@3A	15V@3A	5V@2A	24V@2A	100W
Customized Models	ESM-100-xxxx	*@10A	*@3A	*@3A	*@2A	*@2A	100W

ESM-200 Series—200 Watts $319.

	Model	Output 1	Output 2	Output 3	Output 4	Output 5	Max. Cont. Output Power
Standard Models	ESM-200-5001	5V@20A	12V@4A	12V@4A	5V@2A	24V@4A	200W
	ESM-200-5002	5V@20A	15V@4A	15V@4A	5V@2A	24V@4A	200W
Customized Models	ESM-200-xxxx	*@20A	*@4A	*@4A	*@2A	*@4A	200W

ESM-300 Series—300 Watts $399.

	Model	Output 1	Output 2	Output 3	Output 4	Output 5	Max. Cont. Output Power
Standard Models	ESM-300-5001	5V@30A	12V@6A	12V@6A	5V@4A	24V@4A	300W
	ESM-300-5002	5V@30A	15V@6A	15V@6A	5V@4A	24V@4A	300W
Customized Models	ESM-300-xxxx	*@30A	*@6A	*@6A	*@4A	*@4A	300W

* User specified. Consult factory or local sales office. Minimum 250 units.

Note 1: Maximum specified current cannot be drawn from all outputs simultaneously. At no time should the average current exceed the maximum continuous output power. Above this point, output voltages and currents will be automatically reduced on all outputs. **Note 2:** Output 1 must be loaded to 15% of total output power to maintain proper regulation of other outputs. (Supply will not be damaged by no-load condition on Output 1.) **Note 3:** On ESM-200 and ESM-300 models, all five outputs are isolated. On ESM-100 models outputs 4 and 5 have a common return. All other outputs are isolated.

Options: Crowbar up to 8 Amps $8, greater than 8 Amps $16. Add Suffix V to Model No. Cover $10. Add Suffix C to Model No.

Specifications.

AC Input. 95-132 and 190-264 VAC, 47-63Hz.

Regulation. Line −0.2% within AC limits specified above. Load regulation first three outputs ±0.2%. Load regulation last two outputs ±5%, cross regulation ±3%.

Noise and Ripple. 50mV p-p on first output, 150mV on all other outputs.

Temperature Coefficient. 0.02% per °C on first output, 0.05% per °C on all other outputs.

Efficiency. 65 to 80% typical.

Transient Response. Recovery to 1% in 2 milliseconds for a 50 to 100% load change.

Remote or Local Sensing. Provision included for improved overall regulation.

Overload and Short Circuit Protection. Solid state short circuit protection. Automatic electronic current limiting circuit limits output current to a preset value, thereby providing protection for the load as well as the supply. Units cannot be damaged by prolonged short circuits.

Overshoot. No voltage spikes on turn-on, turn-off or power failure.

Overvoltage Protection. Built in on primary output.

Energy Storage Time. The output voltage will remain within regulation for a minimum of 16 milliseconds after loss of AC input power (from nominal line voltage).

Polarity. May be either positive, negative or floating up to 300 volts DC.

Soft Start. Provides input current limiting at turn-on.

Long Term Stability. 0.1% for 8 hours after 20 minute warm-up.

Ambient Operating Temperature. Continuous duty from 0°C to 71°C. Full rating from 0°C to 50°C, derate linearly to 50% of rating at 71°C.

Storage Temperature. −55°C to +85°C.

Quality Control. In accordance with MIL-I-45208.

POWER/MATE. THE SWITCHER COMPANY.

514 S. River St./Hackensack, New Jersey 07601/(201) 440-3100/TWX (710) 990-5023
3303 Harbor Blvd./Costa Mesa, CA 92626/(714) 957-1606/TWX (910) 595-1766

The world's largest supplier of quality switching power supplies.

CIRCLE 31 ON INQUIRY CARD

THE ULTIMATE INTERFACE

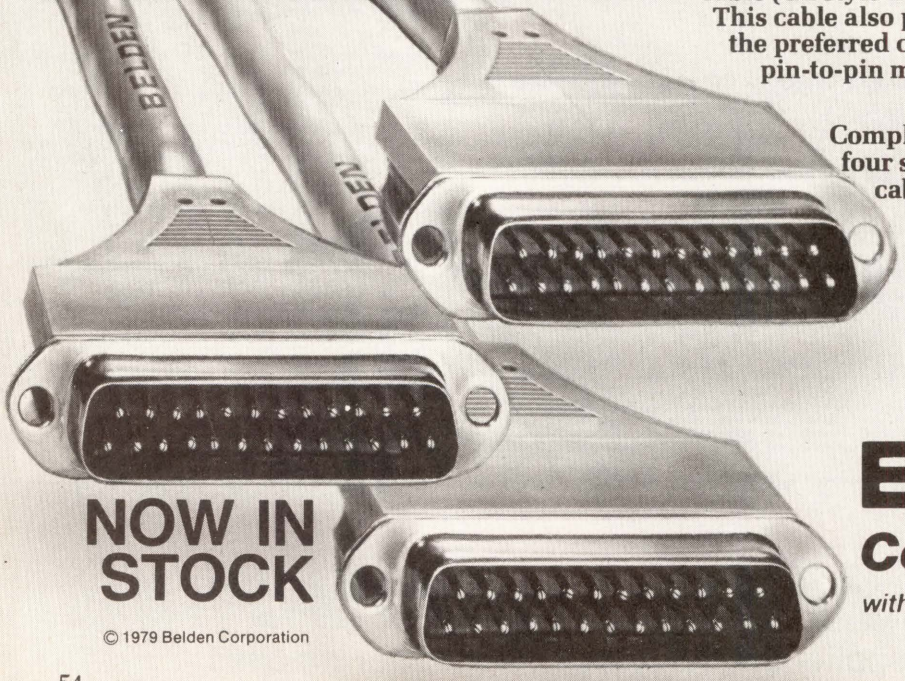
BELDEN EIA RS-232-C CABLE ASSEMBLIES

It's fast. Simple. Reliable. Accurate. In fact, it's the ultimate interface for your data terminal and communications equipment employing serial binary data exchange.

Belden's new 25 conductor molded cable assemblies are designed and built to meet EIA standard RS-232-C and types A through M standard interfaces.

These are cables you can count on. Belden's rugged 8459 cable (UL style number 2576) is used in these assemblies. This cable also passes the FR-1 vertical flame test and is the preferred cable for critical interfaces. And positive pin-to-pin mating using subminiature "D" type plug connectors means no mix-up.

Complete cable assemblies are now in stock in four standard lengths of up to 70′ (21m). Bulk cable is available in put-ups of up to 1000′. Custom designed assemblies are also available on special request. Belden Corporation, Electronic Division, P.O. Box 1327, Richmond, IN 47374; 319-966-6661. Out West contact our Regional Sales Office in Irvine, CA 714-833-7700.



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with new ideas for moving electrical energy

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CIRCLE 32 ON INQUIRY CARD

Hardware/Software Add Power To Mil Spec Computer

A realtime operating system and writable control store extend the processing power of Mil-Spec Eclipse computers. Developed by Rolm Corp, 4900 Old Ironsides Dr, Santa Clara, CA 95050, both features add to the performance of the ruggedized computers in military or commercial use.

A compatible subset of Data General's Advanced Operating System (AOS), the Advanced Realtime System (ARTS) emphasizes realtime processing, resulting in a system that runs faster and requires less memory than its commercial counterpart. ARTS is configurable and modular, providing memory support from 64k to 2048k bytes. It can be a memory only operation, depending on user needs, and has features that include high order language support, memory resident file structure, efficient interprocess communication, and a flexible process/task scheduler.

The software supports up to 32 realtime processes, each with up to 64k bytes of directly addressable memory. Processes may be divided into 32 tasks that compete with other tasks and processes for CPU time. Memory is subdivided into 2048-byte pages that are allocated as shared or unshared memory. Operation of multiprocess applications is supported by provision of a memory resident file structure, mapped overlays, cache-like collection of shared pages maintained on a least recently used basis, and interprocess communication. Multitasking provides the rapid asynchronous service needed by device interrupt routines, time-out routines, and alarm routines, as well as structured control of event driven processes. ARTS handles interrupt/device servicing and scheduling at highest priority levels while system call processors execute at user levels, improving data systems utilization. System code is written to absolute limits to the time in which interrupts are disabled. Internal structure coupled with guaranteed interrupts-off time ensures minimum task scheduling latency

(continued on page 58)

How to Improve Your Image

The Problem: Glare. And poor image-to-background contrast. They wash out displayed information, cutting operator efficiency and lowering productivity.

The Solution: OCLI Contrast Enhancement. It reduces glare by 17 to 1 over untreated glass. It's working now for some of the biggest names in display technology, including IBM, Four-Phase and Tektronix. Write us. We'll explain how it can work for you.

I'd like to improve my image.

Tell me more about OCLI Contrast Enhancement for CRTs.

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Company: _____

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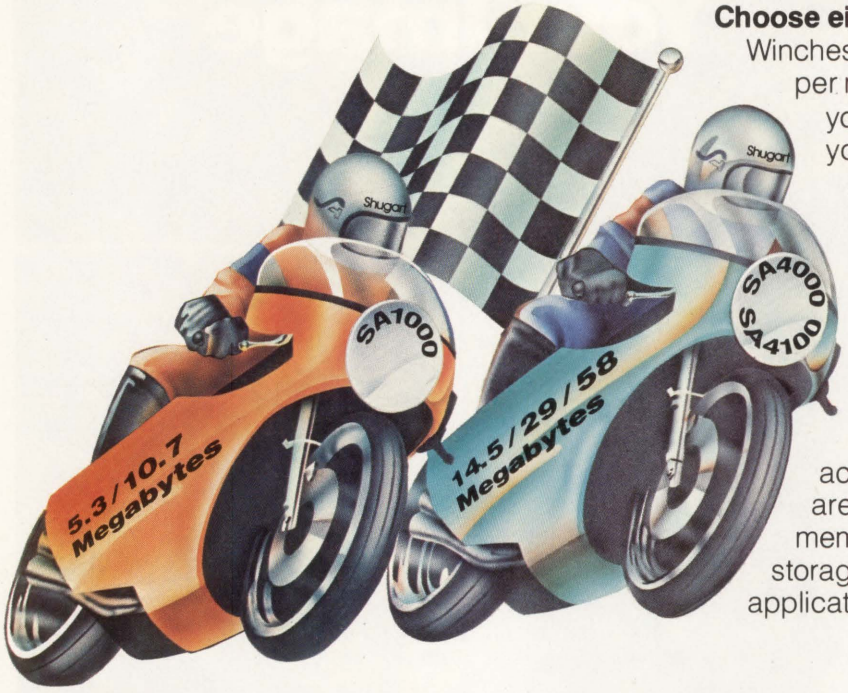
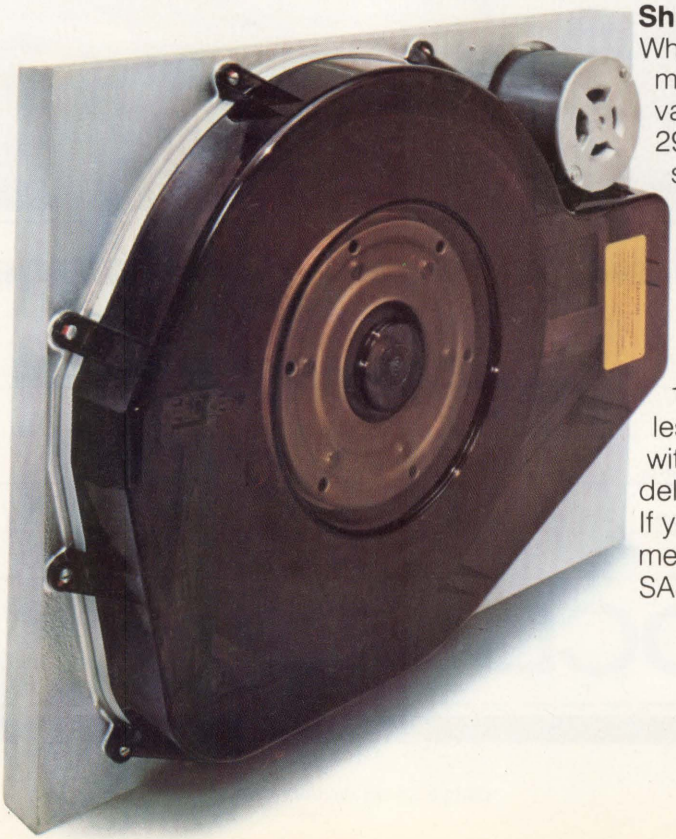
CD-80

CIRCLE 33 ON INQUIRY CARD



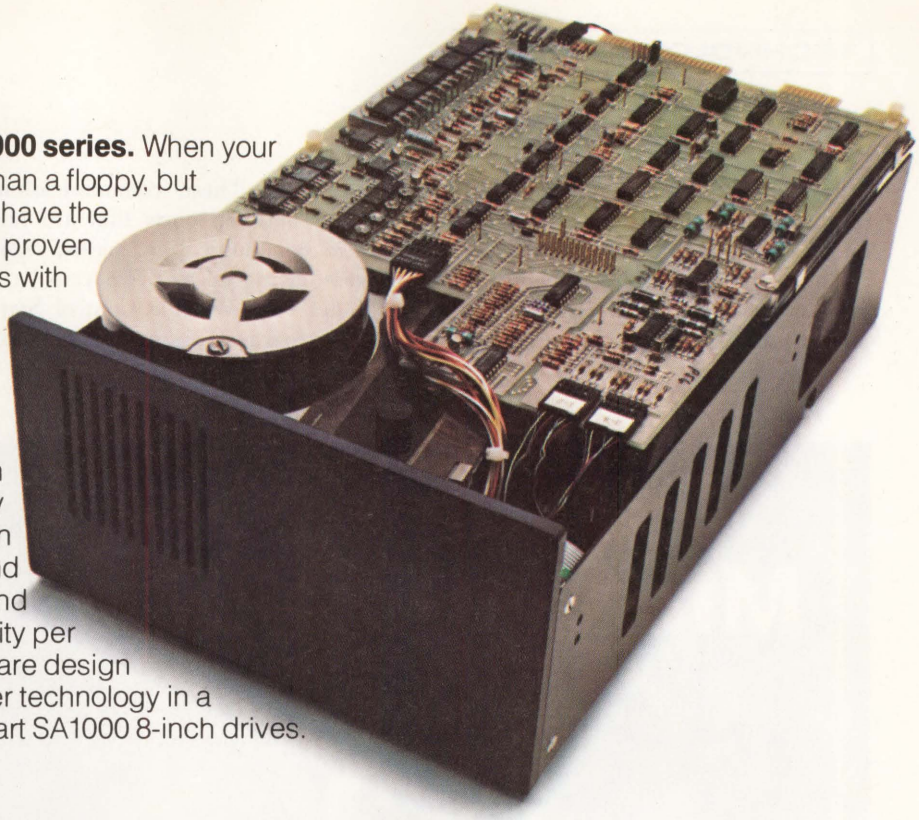
Choose either way and you win, too. Both of our Winchester disk drive families offer the lowest cost per megabyte in their capacity ranges. Whether you choose Shugart 8-inch or 14-inch models, you'll get more data storage for less money. And you'll find that upgrading to fixed disk is easy with Shugart. Drive interfaces and electronics are similar to those used in your existing floppy-based system. Either drive can share a power supply with your floppy. Compact design simplifies system configuration. Both families feature proven Winchester data reliability. Both have our Fasflex™ band actuator for fast, sure data access. And both are the right choice for system resident memory, operating system storage, or mass storage memory. But which is best for your application?

The cost per mega SA1000, SA4000/



Shugart 14-inch drives. The SA4000/4100 series. When you need capacity of more than ten megabytes, the SA4000/4100 series is the best value in Winchester technology. Available in 14.5, 29 and 58 megabyte (SA4100) capacities, the series offers the lowest cost per megabyte of any disk drive in its capacity range. In fact, the unit price of SA4000/4100 drives is less than that of many 8-inch fixed disk drives with less capacity. Weighing under 40 pounds, the SA4000/4100 uses a mere 5.25 inches of panel space and mounts easily in a 19″ RETMA rack. No other 14-inch Winchester drive weighs less or occupies less space. The SA4000/4100 has proven itself with OEM's around the world, too. We've been delivering for two years, with thousands in the field. If you want more capacity with lowest cost per megabyte, and you need it now, specify Shugart SA4000/4100 14-inch drives.

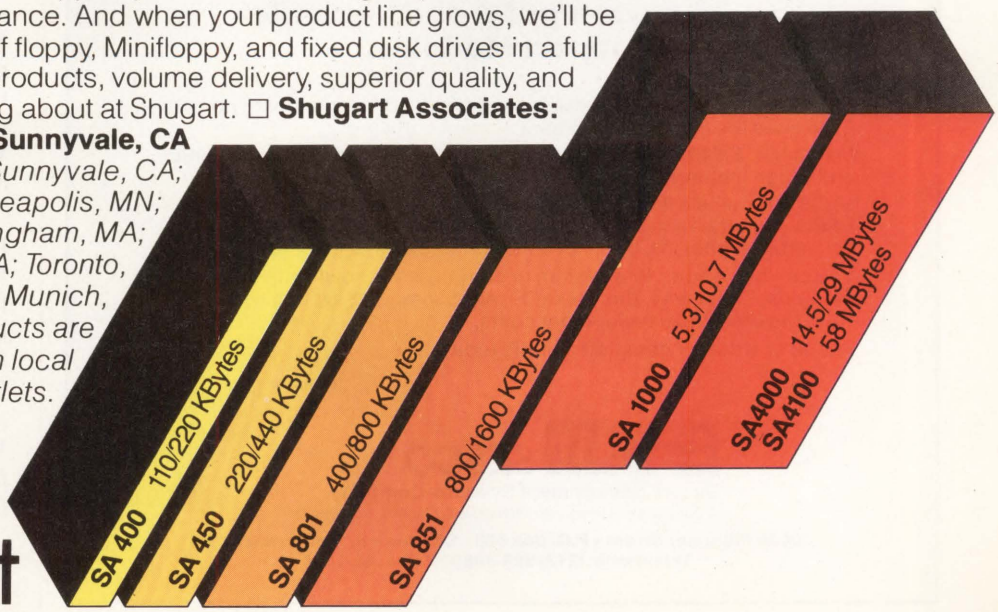
™ Trademark of Shugart



Shugart 8-inch drives. The SA1000 series. When your application calls for more capacity than a floppy, but requires a floppy sized package, we have the compact solution. We packaged proven Winchester technology in 8-inch models with five and ten megabyte capacities. And again, Shugart made it affordable. In fact, in OEM quantities, the five megabyte version costs less than $1,000. The SA1000 matches the physical configuration of our 8-inch floppys and it's much more electrically compatible than competitive drives. In fact, you can daisy chain both fixed and floppy drives from the same controller. And since the SA1000 has the same capacity per track as the double density SA850, software design is a lot easier. When you need Winchester technology in a floppy-sized package, specify Shugart SA1000 8-inch drives.

byte race is fixed. 4100. The winners.

Choose the Headstrong fixed disk drives. No matter which of our fixed disk drives you select, you get the competitive edge when you go with Shugart. We are Headstrong about helping to keep you competitive too, with high volume deliveries of drives that offer superior reliability, quality, and value. This Shugart commitment is also backed by all the support you need including helpful technical services, in-depth documentation, and design assistance. And when your product line grows, we'll be there with a complete family of floppy, Minifloppy, and fixed disk drives in a full range of capacities. Reliable products, volume delivery, superior quality, and value. That's what we're Headstrong about at Shugart. □ **Shugart Associates: 475 Oakmead Parkway, Sunnyvale, CA (408) 733-0100.** *Sales & Service: Sunnyvale, CA; Costa Mesa, CA; Minneapolis, MN; Richardson, TX; Framingham, MA; Landing, NJ; Atlanta, GA; Toronto, Ontario; Paris, France; Munich, Germany. □ Shugart products are also available off the shelf from local Hamilton/Avnet outlets.*



Shugart

Headstrong about fixed disk value

CIRCLE 34 ON INQUIRY CARD

time. A realtime clock maintains a time of dat counter, timing out events, task queuing and scheduler time delays.

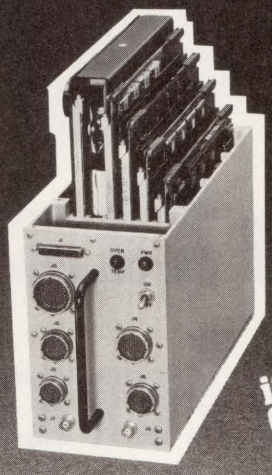
The software provides a facility for processes to communicate via free format messages, allowing process synchronization. These communications are sent between ports that are full-duplex communication paths; each process having up to 127 ports.

Model 1728 Writable Control Store (WCS) provides microprogramming capability for MSE/20 and /30 computer systems. It is supported by the 1774 Micro Control Panel which allows external control of the microprogram execution and 9725 software support which consists of microprogram, assembler, microloader utility program, and FORTRAN 5 runtime loader routines.

The WCS has capacity for 2048 words of 64 bits that are available for user programming of up to 16 specialized functions at one time, and can be dynamically loaded over the CPU's I/O bus. Flexibility is provided by its organization as two blocks of 1024 words, each of which can be configured with RAM or P/ROM. Standard RAM is a 2114L2 static memory chip organized as 1024 x 4 and having a 300-ns microcycle time; 200-ns microcycle time is optional. P/ROM is a 93453 bipolar device organized as 1024 x 4 with 200-ns microcycle time. Contents of the WCS can be read into the CPU via the I/O bus to verify contents of RAM, ensuring the reliability of the device.

Circle 424 on Inquiry Card

Ruggedized Microcomputer



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It's Easy to Design Your Severe Environment System Using our Ruggedized Version of Intel's 80/10A Microcomputer and Versatile Support Modules.

SECS 80 is a ruggedized version of Intel's iSBC* single-board computer. Even uses the same development system software.

Meets MIL-E-5400, 4158, 16400, making it perfect for military, avionics, and tough industrial environments.

SECS 80 comes with a multitude of support modules: RAM, ROM, EPROM, digital tape recorder and controller, 1553 interface, A-D converter, digital I/O, high-speed arithmetic unit, and more.

You can buy a complete system or configure your own with individual modules. Either way, this versatile microcomputer system will save you valuable time and development costs.

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Tabletop Printers Use Blade Matrix Printhead To Reduce Noise

Sound levels of less than 60 dBA and long life of TermiNet[R] 2000 impact matrix printers are accomplished with a unique blade matrix printhead. Models 2030 and 2120, first in the multimicroprocessor based line from General Electric Co, Data Communications Products Business Dept, Waynesboro, VA 22980, have print rates of 30 and 120 char/s, respectively.

The 7-wide by 9-high dot matrix printhead mechanism uses blade mounted pins to insure quiet reliable printing. A dc servomotor controlled printhead mechanism allows bidirectional printing without fill characters. Catchup rates of 60 and 150 char/s are provided. Print density is selectable at 10, 13.2, and 16.5 char/in (3.9, 5.2, and 6.5/cm) over the 13.2″ (33.5-cm) print line.

Paper handling is provided by a standard friction feed platen. Feeding can be accomplished from the back or

THE MTOS FAMILY OF MULTI-TASKING OPERATING SYSTEMS FOR MICROPROCESSORS

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for the 8086. In service since October 1979, useful and productive in a wide variety of applications. Options include multiprocessing, networking and file systems. Don't wait, MTOS-86 is here.

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Real-time operating system for the 8080.
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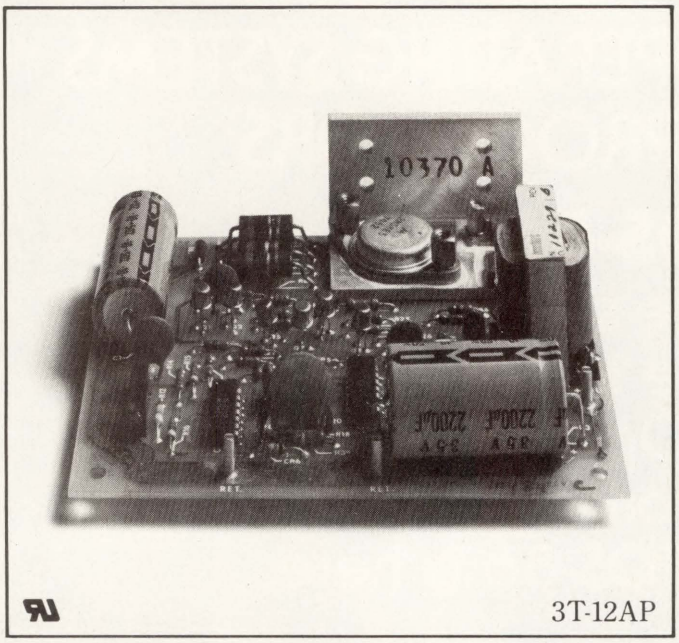
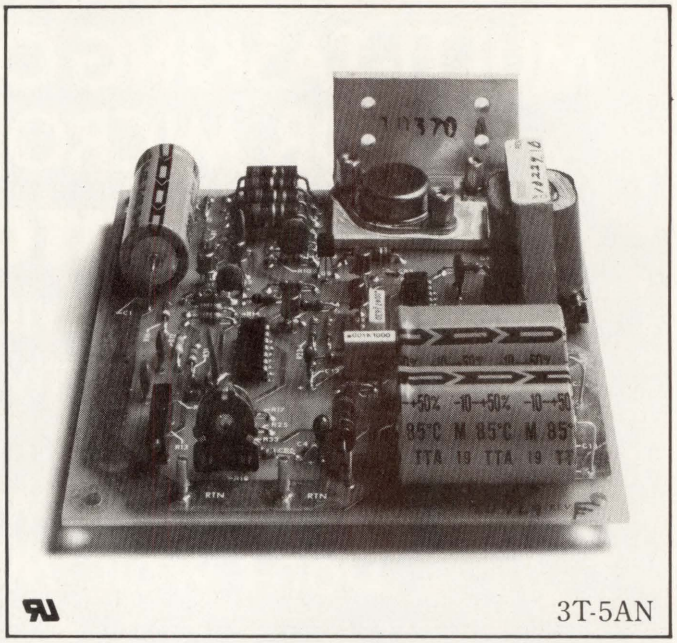


3T-12AP



3T-5AN

because only Boschert offers a totally new concept in power regulation: 3T switching regulators.

Boschert 3T switching regulators can completely change the way you think about power regulation. See for yourself by answering true or false:

In a switching power regulator, input-output voltage differentials must be kept low.

False. With Boschert 3Ts, you can start with 10 to 40 volts and get 4.5 to 30 volts out, without a power penalty.

To get negative voltage out, you need negative voltage in.

False. Our 3T-5AN lets you take positive dc in and produce negative dc out.

Regulation is inherently inefficient.

False for 3Ts. They offer 70-90% efficiency over the entire operating range.

The magnitude of output voltage must be lower than the input.

False. Our 3T-5AN lets you set the output magnitude less than, equal to or greater than your input voltage.

	3T-12AP	3T-5AN
Input Voltage	+10 to +40	+10 to +40 volts
Output Voltage	+4.5 to +30	−4.5 to −30 volts
Output Current	0 to 12	0 to 5 amperes
Efficiency	70-90%	70-90%
Output voltage and current limits are adjustable.		

Multiple output voltages require multiple tap transformers.

False. All 3T regulators can be powered from the same dc source.

Designing for a wide line voltage range means wasted power at normal line. False. Efficiency is virtually independent of the transformed line voltage input to 3Ts.

Battery backup of multiple voltages requires multiple batteries or a special UPS design.

False. You can backup the input to multiple 3Ts, using one standard battery.

With Boschert 3Ts, you can build better power supplies, build battery backup or single-battery multiple-voltage systems, even add extra voltages to an existing system without redesigning your supply. You see? Boschert 3Ts have already changed your ideas about power regulation. We've got 3Ts in stock, in volume, so you can put your ideas into practice today. For more information, contact your Boschert representative or write us: Boschert Inc., 384 Santa Trinita Ave., Sunnyvale, CA 94086. Or phone (408) 732-2440.

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CIRCLE 37 ON INQUIRY CARD

bottom of the units, which can provide up to three copies, including the original.

The microprocessor scanned keyboard uses capacitive key switches. An ANSI typewriter paired arrangement is standard on U.S. models; ANSI/APL layout is available. The international version has a standard ECMA arrangement with a modified ECMA/AZERTY/YZ interchange available.

Printers meet VDE RFI standards and employ switching type regulators. Using dual 8085 microprocessors, they also offer a received data buffer and feature nonvolatile configuration memory. Both units incorporate modular software and provide a full RS-232-C data interface (CCITT V.24). A 300-baud modem, extended 16k data buffer, and 32k edit buffer are among planned options.

Circle 425 on Inquiry Card

Development System Takes Hardware Approach To Programming

With the Software Synthesizer, engineers can assemble software from existing components, writing only those parts necessary to implement new functions. Introduced by Scientific Enterprises, Inc, 6900 SW Haines Rd, Tigard, OR 97223, the system allows software engineers to take a "hardware" approach to program development.

The system centers around two elements: Software Synthesis Language (SSL) and a 16-bit minicomputer with 256k-byte memory, 38M-byte capacity Winchester disc system, 4 video terminals, and 13M-byte cartridge tape for disc backup and archiving. The system supports four programmers through remote CRT terminals supplied with the system. Each programmer has an RS-232 port for downloading and communicating with local peripheral devices.

SSL promotes the synthesis of programs from components. Existing components are combined with additional parts needed to construct complete programs, much as standard hardware components are combined with custom LSI chips to produce hardware systems. The component feature also allows four programmers to work efficiently on the same project, further speeding development efforts.

Each component consists of an interface and an implementation. The interface can describe all capabilities implemented in the component or can hide those not required. It also allows multiple implementations of components to be used interchangeably.

The software shows the user of a component only that component's interface. This controls the way in which components depend on one another, making systems easier to debug, improve, replace, or reuse.

SSL, as a language, offers no inefficient features, yet it is structured to give extensive support for software development. Components can be passed between program components, and exception handling is simple and straightforward.

Included in the synthesizer is a document formatter which encourages users to simultaneously build both software and documentation. Since the compiler's parser is generated from the same text file used to generate the reference manual, agreement between program and reference is guaranteed. Revised programming automatically produces revised documentation.

Initially, the system supports the Motorola MC68000 16-bit microprocessor, and is specifically designed to offer transportability of programs between 68000, Z8000, Z80, and 6809 microcomputers and minicomputers or mainframes such as PE Series Sixteen, DEC PDP-11, and IBM System/360 or /370. Price is $83,000 including computer, software, and terminals.

System options will include a high speed dot matrix printer, remote in-circuit emulators, and remote P/ROM programmers. Software options will include code generators for 8-bit/byte addressable mini and microprocessors and a set of programming tools to automate compiler construction.

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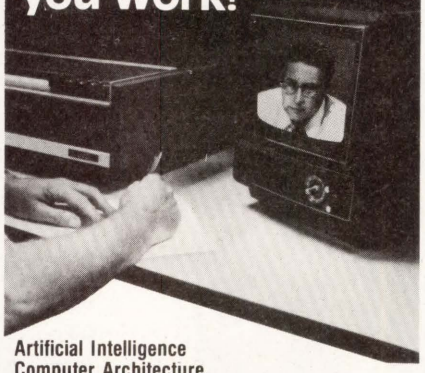

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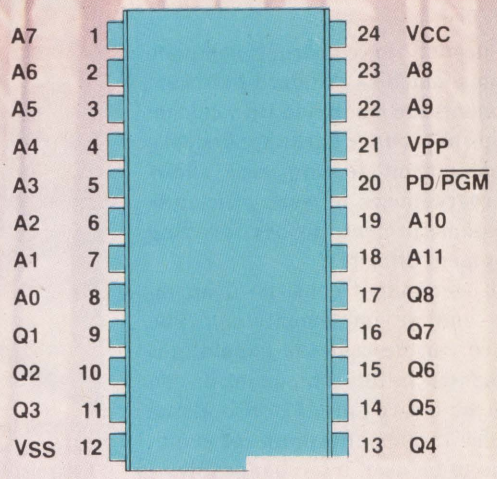
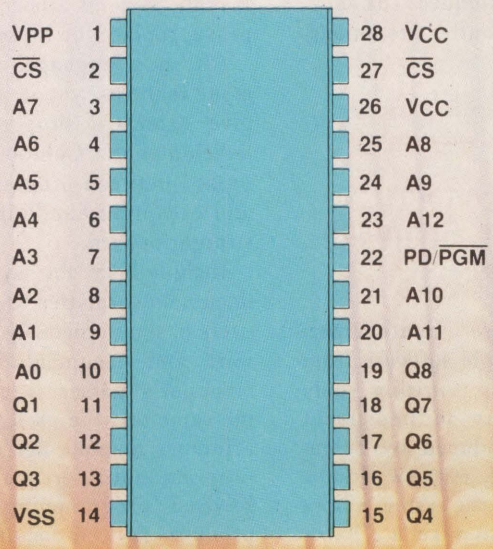
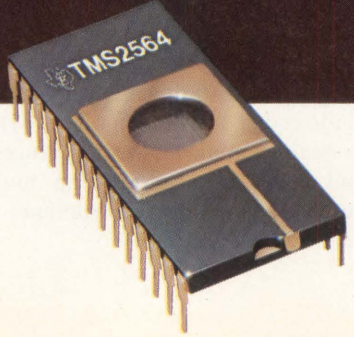
TMS 2532
32K EPROM



TMS 2564
64K EPROM



MOVING AHEAD IN MEMORIES



8Ks, 16Ks, 32Ks, and now...

The first 64K EPROM. From Texas Instruments. Naturally.

Introducing the TMS2564. The industry's first 64K EPROM. The densest yet. With all the high-performance features of TI's 5-V EPROM family. Features like 8-bit word configuration, fully static operation, automatic chip-select/power down, and low-power.

Pin compatibility

TMS2564 is offered in a 600-mil, 28-pin dual-in-line package. But, it's compatible with industry standard 24-pin 64K ROMs, as well as less dense EPROMS.

This is because pins 3 through 26 of the TMS2564 are compatible with pins 1 through 24 of the 24-pin devices. Compatibility is enhanced by reserving both pins 26 and 28 for the 5-V supply. So, with a supply trace to pin 26, both 24 and 28-pin devices can be used, with no jumpering.

Fully static

Like all TI EPROMS, the TMS2564 maintains the fully static tradition that makes designing easier.

No timing signals. No clocks. No strobes. No refresh. No problems. Simply, cycle time equals access time.

Lowest power ever

Operating at an access time of 450 ns with a power dissipation of only 840 mW maximum or less than 13 μW per bit, it's the lowest power per bit ever achieved in EPROMS.

Easy programming

The TMS2564 is designed to facilitate rapid program changes in high density, fixed memory applications.

All that's needed for simple, in-system programming, is a single TTL level pulse.

You can program in any order. Individually. In blocks. At random. So, programming time is reduced to a minimum. And, you can use existing 5-V PROM programmers.

Erasing? Simple ultraviolet. Just like any other EPROM.

Widest choice

By adding the new TMS2564 to our fast-growing EPROM family, we offer the designer a product breadth unmatched by any other supplier.

All TI EPROMS are available in 600-mil packages with JEDEC compatible pin-outs.

And they all share the reliable N-channel process technology.

TI's growing EPROM family. For all your present and future memory requirements.

For more information about the first 64K EPROM, or any other family member, call your nearest field sales office or authorized distributor. Or write to Texas Instruments, P.O. Box 1443, M/S 6955, Houston, Texas 77001.

Fifty Years of Innovation

TI'S GROWING EPROM FAMILY

Device	Description	Power Supply	Max Power (0°C) Operating	Standby	Access Time
TMS2564	64K	5 V	840 mW	131 mW	450 ns
TMS25L32	32K	5 V	500 mW	131 mW	450 ns
TMS2532	32K	5 V	840 mW	131 mW	450 ns
TMS2516-35	16K	5 V	525 mW	131 mW	350 ns
TMS2516	16K	5 V	525 mW	131 mW	450 ns
TMS2508-25	8K	5 V	446 mW	131 mW	250 ns
TMS2508-30	8K	5 V	446 mW	131 mW	300 ns
TMS2716	16K	+12, ±5 V	720 mW	—	450 ns
TMS27L08	8K	+12, ±5 V	580 mW	—	450 ns
TMS2708	8K	+12, ±5 V	800 mW*	—	450 ns
TMS2708-35	8K	+12, ±5 V	800 mW*	—	350 ns

*T_A = 70°C

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85126 A

CIRCLE 39 ON INQUIRY CARD

Technical Computers Use Two Processor Chips To Distribute Intelligence

L-series HP 1000 computers use two CMOS/SOS LSI chips to create a distributed intelligence architecture. With a 1-chip CPU and a processor chip on every board, the series, introduced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, offers I/O flexibility in a compact low cost unit. Use of SOS technology extends benefits of high speed, low power consumption, high circuit density, improved reliability, and design ease to processors and high speed custom interface circuits.

The L-series processor, complete on a single printed circuit board, has a single-chip CPU that performs all computation and control functions. This chip executes the basic instruction set and contains the time base generator and memory protect features. In addition to the processor and its support circuitry, the 6.75 x 11″ (171- x 279-mm) PC board has two 2k x 8-bit ROMs housing a variety of standard boot loaders, comprehensive self-test, and virtual control panel firmware. This firmware enables any terminal to act as computer control panel with full access to the machine's internal registers, and allows remote access and diagnosis of the machines via hardwired or modem links. The whole processor has been reduced to 1 board containing 65 circuit packs; this processor previously occupied 3 larger boards with 337 packs.

A separate SOS chip equal in complexity to the CPU chip, the I/O processor executes all processor I/O instructions and provides built-in capability for DMA operations. Every interface board carries one of these chips, contributing to the distributed intelligence architecture and providing full DMA capability. In the systems, a self-configuring or chained DMA mode can be invoked to set up and execute several DMA transfers without interrupting the CPU. Overall I/O bandwidth is greater than 2.7M bytes/s. The I/O processor shares the same backplane as CPU and memory boards, significantly improving I/O performance, flexibility and throughput.

Also implemented in SOS, an HP-IB interface chip provides the complete logical and electrical interface to the company's implementation of the IEEE Std 488 bus.

The instruction set, a subset of that used in other HP 1000 series machines, is efficient when operating between memory and registers. CPU instruction times range from 4.1 ns for loads and stores, 4.5 ns for adds from memory, to 28 μs for a multiply.

Offered as boards, rack-mountable processors, or in systems, the series is compatible with other HP 1000 units. They have multiprogramming, real-time executive operating systems, support program development in FORTRAN IV, BASIC, and assembly language, and execute Pascal. Memory is 64k bytes of 16k RAMs with 681-ns access time and parity. Interfaces containing the I/O processor include the HP-IB interface, an asynchronous serial interface with EIA RS-232-C, RS-422/423, or RS-449 compatibility; a multipurpose parallel interface having data rates up to 1.1M words/s; a P/ROM storage module providing 64k bytes of offline nonvolatile storage for operating system and user application software; and special purpose breadboard interface for fast design and implementation of custom interfaces.

The board level HP 2103LK, containing 64k-bytes memory, is priced at $2250; the HP 2103L rackmount in a 5.25″ (13.3-cm) high enclosure, with CPU, 64k-bytes memory, power supply, time base generator, memory protect, and eight I/O slots, costs $4450. A model 10 system, consisting of 2103L computer, CRT terminal, 1.2M-byte flexible disc drive, cabinet, and 12M-byte Winchester disc drive, is priced at $22,500. Prices are single quantity and subject to OEM discounts.

Circle 427 on Inquiry Card

Microprocessor Designers . . .

Low-Power Switchers Work On All World Voltages

Without Changing Taps, Jumpers or Switches

Imagine you could design a microprocessor system that would operate almost anywhere in the world with a single switching power supply. Well, you can with Converter Concepts' low-power switchers!

WIDE INPUT VOLTAGES Only Converter Concepts produces 15 to 100 watt switchers that operate on any voltage from 90 to 250VAC or 10 to 40VDC — without switches, jumpers, taps or other modification.

BROWNOUT PROTECTION You get reliable operation during power failure, too, on power as low as 50VAC, with minimum degradation of output voltage.

LATEST SWITCHER CONCEPTS Our advanced switchers use a single transistor, single transformer flyback design with soft turn-on characteristics and short circuit protection. You get less complexity, higher reliability and efficiency, and a cost that's competitive with linears.

MANY OPTIONS
Four input power ranges and single, dual or triple output options are available in low-cost printed circuit board, open frame or RFI-resistant enclosed packages.

RIGOROUS QUALITY CONTROL We're building a reputation for tough QC, so you're buying confidence with every Converter Concepts' switcher. Call us today for engineering assistance, our latest engineering catalog, prices and your nearest CCI representative.

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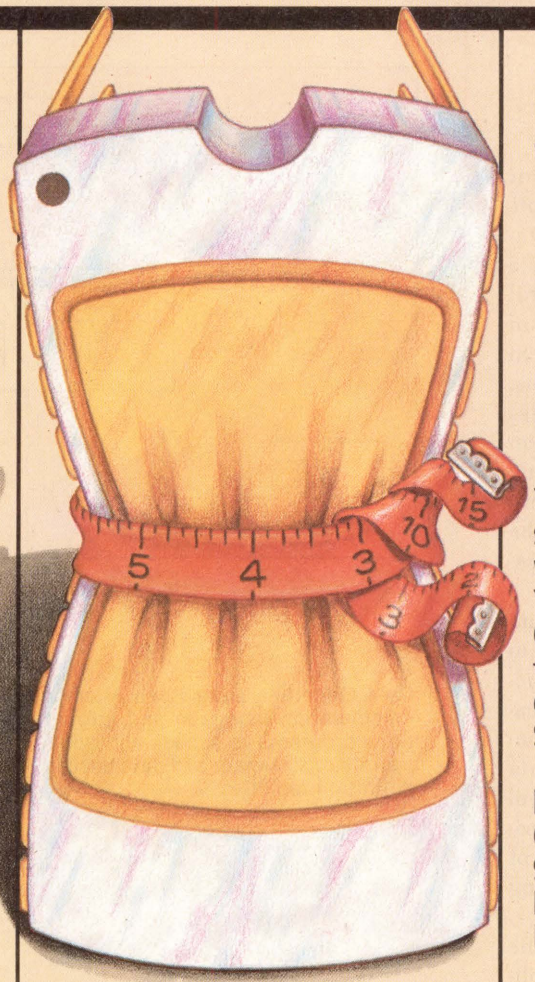
12-BITS, 16 PINS. THE END OF THE FAT DAC.

THE 12-BIT DAC FOR TIGHT LAYOUTS.

Our compact new AD7542 is the world's first and only 12-bit D/A converter in a 16 pin DIP. It needs only ⅓ the board space of the usual 24 pin DIP, and since data is brought in as three 4-bit words, only 4 data lines are required rather than 12, which saves lots of PC board track. This makes the AD7542 ideal for applications requiring several DAC's per board.

DIRECT AND EASY μP INTERFACE.

Our slim, new DAC is designed specifically to interface directly to the data and control buses of 4, 8, and 16-bit microprocessors. The AD7542 interfaces to a μP as static RAM, with data loaded into it in three 4-bit words, using simple memory WRITE instructions. It even has a separate asynchronous clear input to simplify initialization during power up.



AND IT'S AN HONEST 12-BITS.

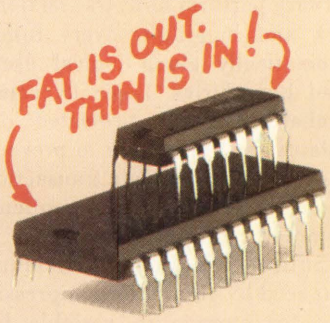
The AD7542 is a *real* 12 bit DAC, offering *true* 12 bit performance. Its monolithic CMOS construction gives you guaranteed 12 bit linearity over temperature (±½ LSB from T_{min} to T_{max}), and a low gain TC (typically ±2ppm/°C).

It operates on a +5V supply and features latch-up free operation. It also has all the analog versatility of CMOS DAC's, including 4-quadrant multiplication, and a low 40 mW power consumption.

ALL FOR AN UNBELIEVABLE $9.50.

You might think the world's smallest 12-bit DAC comes with a big price tag. It doesn't. You can get our AD7542JN (±1 LSB max linearity error) for only $9.50 in 1000's, or our AD7542KN (±½ LSB) for $10.50 in 1000's.

For the full story on this lean, new DAC, contact Doug Grant or Don Travers at (617) 935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062



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CIRCLE 41 ON INQUIRY CARD

SOFTWARE

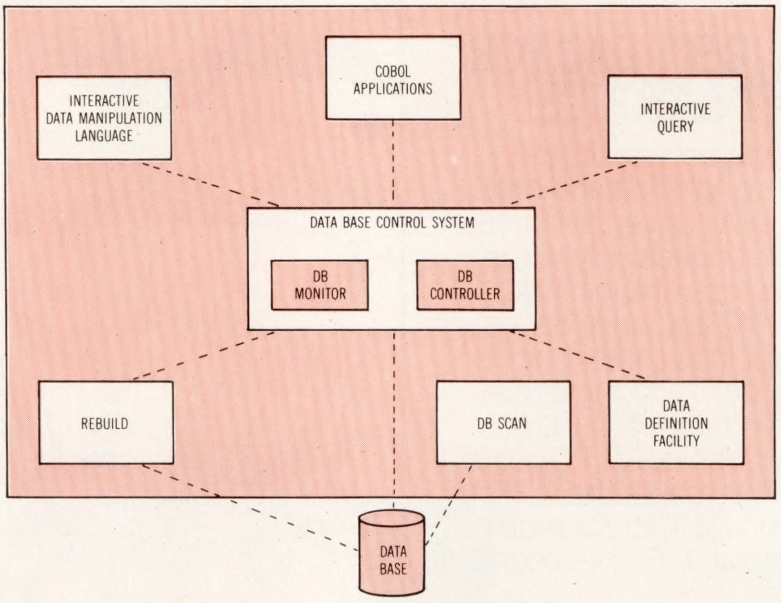
Software Packages Support Online Distributed Processing Environments

CODASYL Data Base Management System incorporates design concepts for online distributed processing environments with mainframe DBMS functions. Developed by Data General Corp, Rt 9, Westboro, MA 01581 to run under the Advanced Operating System on commercial Eclipse data systems, the DG/DBMS implementation manages up to 4.4G characters of data stored on up to 16 disc subsystems. Concurrently released were an Interactive Query package for use with DG/DBMS, and the high performance INFOS II file management package.

Interfacing with the COBOL programming language DBMS is designed to handle data with a network data structure, and is based on 1978 specifications for data base systems recommended by the Conference on Data Systems Languages. A flexible tool that can cut programming costs, it provides an efficient and secure method of maintaining files while performing online simultaneous updates.

Data integrity mechanisms in the software perform both transaction rollback and logging/recovery functions automatically along logical user defined boundaries. Logically complete databases are fully protected; partial updates are rolled back to prevent the existence of incomplete transactions in the database. Data independence is promoted through use of a Data Definition Facility. Efficiency is enhanced by automatic compression of data for storage in variable length records.

Assuming functions ordinarily performed by the application program, the management system stores or retrieves data for application program or for interactive query facility, maintains logical organization of data and internal indices, logs transactions and performs backup and recovery functions, and controls access to data for security purposes. Access strategies that may be used to add or retrieve data in the environment include sequential, random, and multi-key indexed sequential.



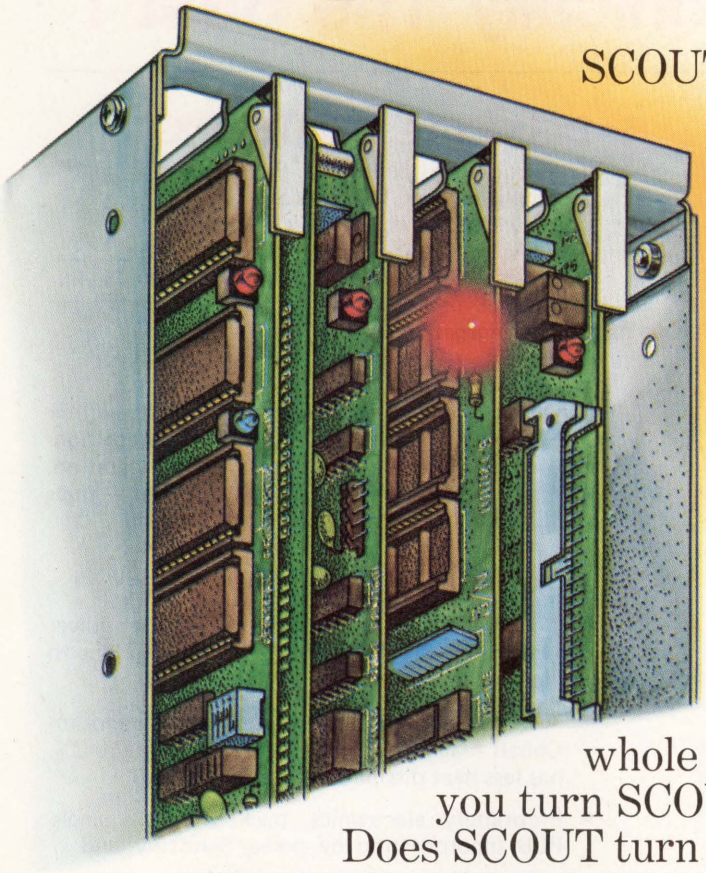
Data General's Data Base Management System allows interactive data manipulation language and interactive query utilities as well as applications programs to access and update data base through data base control system. Maintenance of data base is offered through rebuild, DMSCAN, and definition facilities

The database management system is made up of two runtime monitors that operate as separate processes under AOS and four related standalone utilities. The monitors form the database control system that handles all access to and from the data base on disc and an optional log, usually on magnetic tape. Controlled through the system's operator console, the data base monitor keeps track of open data bases and current users, handles error conditions, and initiates and terminates processes of the second monitor, the data base controller, which interprets and executes data manipulation commands. The four utilities, data definition facility, interactive data manipulation language, rebuild, and DBACAN, support data base operations.

Interactive Query, an optional read only utility reduces programming costs by allowing users to interactively enter requests into the data base through display terminals. Users can rerun query streams using a built-in macro facility with parameter capabilities.

INFOS II file management system works with the company's implementations of PL/I, FORTRAN, RPG II, Assembler, IDEA, and COBOL, and includes a logging and recovery facility that offers users the option of complete hard crash protection. It also provides key and data compression, check pointing, and support for concurrent updates. Circle 428 on Inquiry Card

Speak SCOUT, speak.



SCOUT™ is a smart minicomputer. He can tell you when one of his boards is bad. Good SCOUT!

How does SCOUT do this? SCOUT has ISOLITE.™ Do you see the red light? It means ISOLITE is testing the board. If the light stays on, the board is bad. Bad boards don't get to play anymore. They get replaced with a spare 6.25″ x 8.3″ card in about three minutes.

Isn't ISOLITE neat? It can even test your whole system every time you turn SCOUT on.

Does SCOUT turn you on?

Think what three-minute maintenance could do for your bottom line. Think what it could do for your product line. Everyone will love your products. You will grow very rich.

You will save up front, too. SCOUT starts at less than $1K for a 16-bit CPU, I/O, 32K Byte RAM and card cage. So, SCOUT also speaks to value.

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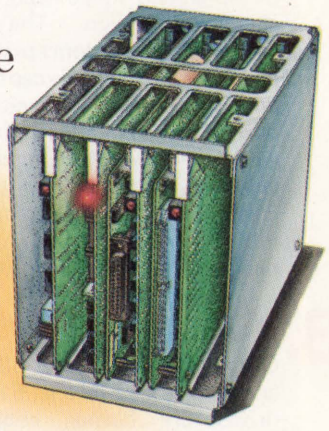

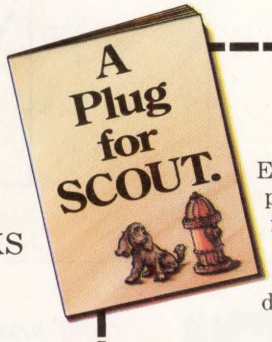

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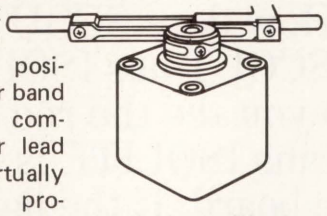
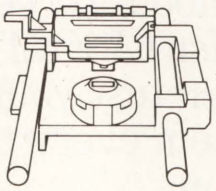


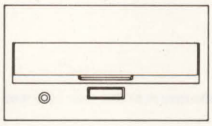
MPI's patented stepper-band positioner provides the industry's fastest access time (5ms) and most accurate positioning. The stepper band is simpler in design compared to a cam or lead screw. It is virtually frictionless, which provides extremely accurate and reliable positioning, yet requires the lowest power. As a result, it moves five times faster than other positioning systems.

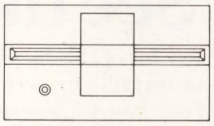
2. HEAD & CARRIAGE



Our high-performance mini floppy drive was developed as a dual-head, double-track, double-density unit. It is not an up-graded single-head, single-density design. The carriage and head concepts are based on IBM's – except for one important innovation: our bottom head is fixed, while only the top head loads. The heads are centered between two parallel rods (not cantilevered) to eliminate radial-positioning errors. To minimize media wear, we designed the longest head carriage which insures flater head landings.

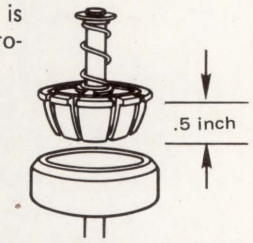
3. HUMAN ENGINEERING





Our dual-head (Model 52) and single-head (Model 51) drives are human engineered. Key features include: a full-closing, push-button front door to provide greater media protection; a patented ejector mechanism that makes diskette removal easier; and a choice of bezels.

4. DISKETTE CENTERING



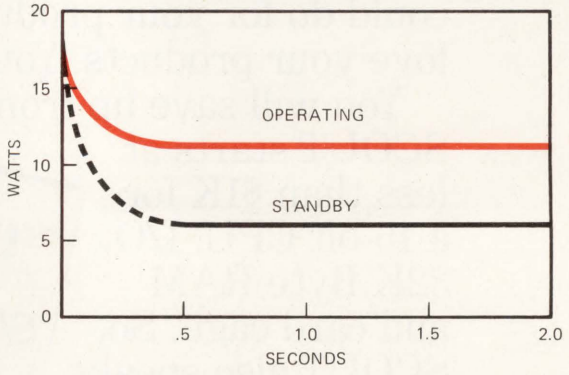
True diskette centering is accomplished by MPI's proprietary clutch mechanism. As the front door is closing, our extra-long clutch expands and gently engages the mylar media. When the clutch is seated, the diskette is locked securely in position to within .0008 inches. The result: most accurate positioning, longer diskette life, and trouble-free operation. MPI's diskette ejector – an industry first – pops the diskette out within easy finger-tip reach.

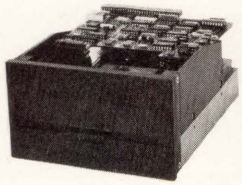
5. POWER CONSUMPTION

MPI drives have the industry's lowest power consumption (6W standby, 12W operating) due to the following:

- A high-precision stepper motor with Samarium-Cobalt magnets. This motor is accurate to 3%, has less heat dissipation, and longer life;
- Proprietary electronics, packaged on a single PCB, incorporating low-power Schottky; and
- A low-friction positioning mechanism.

OPERATING AND STANDBY POWER





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SOFTWARE

Compiler Supports C Language On HP 1000 Computers

A full implementation of the C programming language for the Hewlett-Packard System 1000, HP/C runs under RTE-IV and RTE-IVB. Announced by Corporate Computer Systems, Inc, 675 Line Rd, Aberdeen, NJ 07747, the compiler is completely integrated with the existing HP software base, including FORTRAN and assembler subroutines.

The compiler supports the full C language, including integer, unsigned, character, long and double-float arithmetic, along with pointers, structures, and functions. Recursion is permitted because of the language's use of runtime storage management routines. However, users may elect to have the compiler produce nonrecursive code for application where stack overhead is not necessary.

Output of the compiler is HP assembler code which is processed automatically by the RTE assembler to produce mixed listings and relocatable object modules. Consisting of a single pass with an optional macro prepass, the compiler processes between 300 and 400 lines of C source code to relocatable object code each minute.

The compiler was developed by CCS under contract to Hewlett-Packard. HP/C compiler and runtime library cost $4000/copy; sources are available at $10,000. HP holds exclusive license for sales to the Bell System and the U.S. Government.

Circle 429 on Inquiry Card

Screen Processor, Report Writer Extend DBMS Capabilities

A high level language interface for external application module programming, a self-contained screen input processor, and a report writer language enhance the DRS database management system. Introduced by Raxco Inc, 3336 N Flagler Dr, West Palm Beach, FL 33407, the products operate on the same database files without logical or physical redefinition.

XBS, a higher order language (HOL) interface for external programming of application modules, allows multiple logical views of the data file to be activated within a single program. Routines are made available for simplified query and update.

Simplified definition of transaction displays on CRT terminals is provided by the screen input processor (SIP) which permits rapid system development for transaction driven database management systems. The package also offers automatic cursor positioning, control of display formats, and procedural error check routines.

RPW, the report writer language, supports efficient coding of complex reports with branching, looping, conditional, and subscripting capabilities. It also allows fixed or relative positioning of output data, summarization at multiple control breaks, and automatic paging.

DRS, an English language based command system, runs on a range of computers including DEC VAX and -11 series, IBM, CDC, and Univac systems. Database structures range from simple flat files to complex relationships having as many as 16 levels. Both batch and interactive modes are supported.

Circle 430 on Inquiry Card

Pascal Development Systems Run On H-P Desktop Computers

Pascal-35 and -45 development systems, derived from the UCSD Pascal development system, take advantage of human interface and other capabilities of desktop HP9835A and HP9845B computers. Developed by International Electronic Machinery, Inc, 125 W Crestridge Dr, Suite 307, Fort Collins, CO 80525, the systems give users a choice of Pascal or BASIC on the machines.

All familiar features of UCSD Pascal are present; however, the top level command structure has been altered to permit execution of a compiled program by merely typing its name. Package components are Pascal compiler, linker, file by name file management, and full screen editing.

The systems take advantage of HP hardware features. User memory can extend to 512k on the 9845B and to 246k on the 9835A. Mass storage can consist of any mix of tape cartridge, flexible disc, or hard disc. Typewriter and teletypewriter keyboard modes are supported.

Optional capabilities are available to expand the system. These include Pascal access to graphics and plotting, and special predefined procedures for I/O programming including IEEE 488 (HPIB). A runtime support package will enable users to develop standalone application programs, and end users to run the programs without learning the development system. □

Circle 431 on Inquiry Card

Microcomputer Controller Applications— As Seen By IECI '80

Once again the IEEE's Industrial Electronic and Control Instrumentation Society based its annual conference on applications of microcomputers (although minicomputers were mentioned in the conference title and were represented by an occasional paper). Recognition of the microcomputer and its countless possible applications has been the core of IECI conferences since the first meeting, held in 1975. Although those applications have ranged over a wide area including process control, automation, data acquisition, energy monitoring, power distribution, and instrumentation, nearly all have been relatively realistic, with few that could even be considered blue sky.

This year, however, there was a very noticeable shift that may indicate something of concern to American industry. During each of the preceding years, there have been increasing numbers of conference papers presented by foreign speakers. This year fully 50% of the papers were written by persons from outside the U.S.

IECI officials did point out that special efforts had been made to obtain papers by foreign speakers. However, the quality of papers accepted from foreign speakers was just as high as those from U.S. speakers. Therefore, the question arises—as it has risen previously, based on evidence from other sources—on whether or not U.S. industry and research are falling farther behind a number of foreign countries in the application of microcomputers—or any computers, for that matter—for process control, automation, and data acquisition.

In any case, IECI '80 included more than 80 papers by speakers from the U.S., Hungary, Japan, Spain, Saudi Arabia, Canada, India, Egypt, France, Italy, England, Poland, Brazil, Mexico, Greece, and Nigeria. One paper was to be presented from the U.S.S.R., but the speaker was not permitted to travel to Philadelphia even though he is currently a visiting instructor at the University of Wisconsin. Representative papers are summarized in the following sections.

Evening sessions were held on Tuesday and Wednesday evenings. One provided an opportunity for a number of vendors to describe their microcomputers and related products; the other was a discussion of available software. Full-day separate tutorials were presented Monday on data acquisition system technology and mini/microcomputer applications.

Process Control and Automation

Economy was a factor considered in most designs described at this conference, and at least one system was based upon a "personal" computer available as an across the counter item. Other systems used off the shelf microprocessors or single-board or single-chip microcomputers. Only a relatively few involved specially designed processors.

Lumber Kiln Control

A system developed at the University of New Hampshire for control of a small, research oriented lumber kiln[1] uses a Radio Shack TRS-80 personal computer programmed in BASIC as controller. Both Commodore PET and Heath H-8 microcomputers were also considered and appeared to satisfy important criteria, but the authors said that final choice was based on reliability and convenience of service at a local store.

In practice, commercial kilns store large amounts of green lumber under climatically controlled conditions to remove moisture that otherwise would cause the wood to split or warp before or after use. Besides being a lengthy process—60 days or longer—the procedure causes the wood to shrink appreciably. Research underway at the Wood Products Laboratory of the University of New Hampshire to shorten the drying period, decrease the energy usage, and reduce loss of wood area revolves around an open loop control system driven by a microcomputer. Unlike standard kilns, the experimental unit holds only about 500 board feet of lumber.

Because of slow time constants of the plant, there was no need for high computational speed. However, more critical considerations included adequate reliability to run unat-

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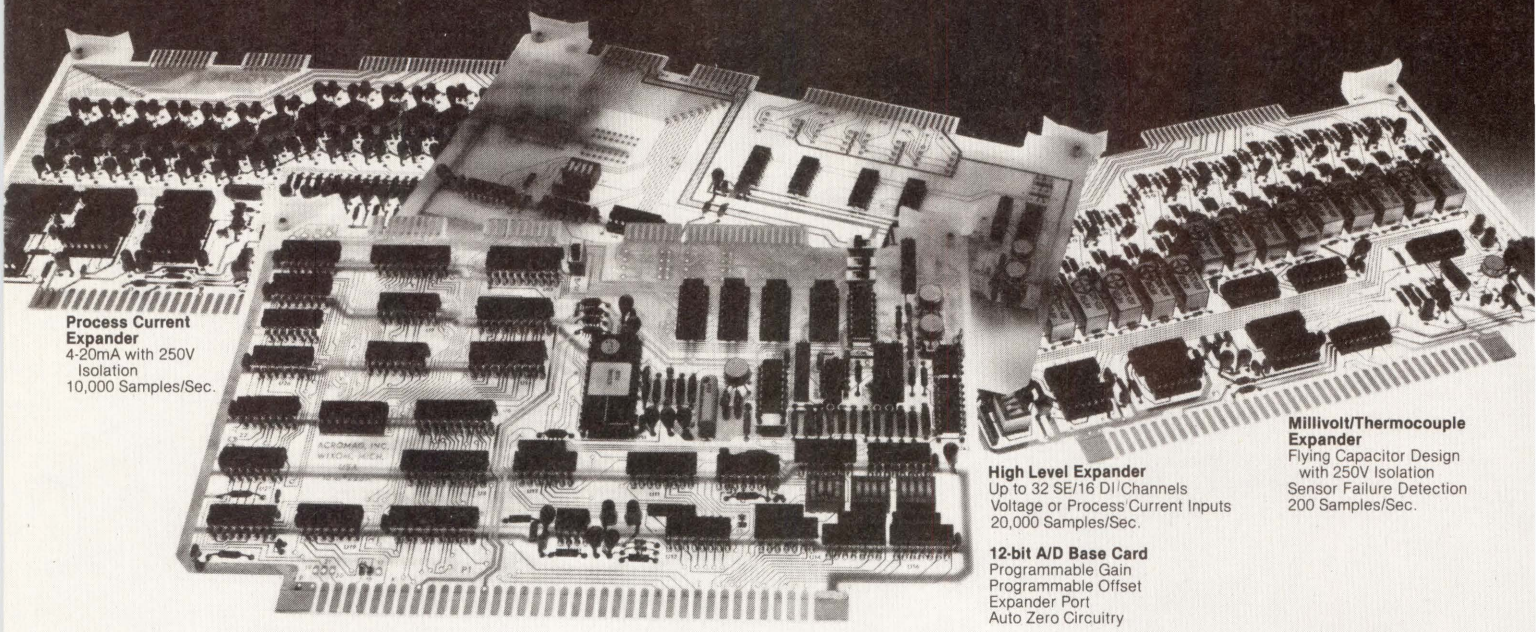

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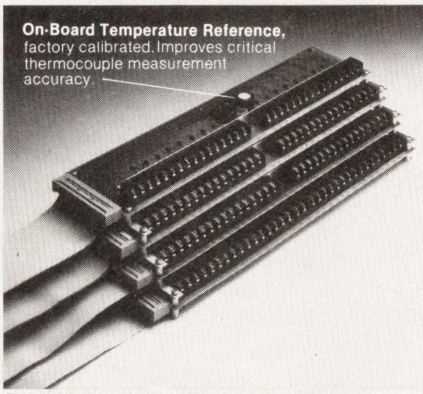

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tended for hours, easy repair or replacement in case of failure during a drying run, simple operator input and retrieval of data in both display and hardcopy forms, ability to interface a controller between the computer and the plant, availability of both high and low level languages, and offline nonvolatile memory for program and data storage. Above all was the need to keep the costs low.

Interface hardware, on two wirewrap circuit boards, is housed with two power supplies, a 6-V battery and charger, three solid state relays, and an alarm buzzer in a 12 x 10 x 8″ (30 x 25 x 20-cm) metal box. The microcomputer bus provides computer interface signals to the hardware.

Wet and dry bulb temperatures are sensed with thermocouples, while moisture content is sensed using probes that measure electrical resistance between two points in the wood. This resistance is then used to generate a voltage that can be correlated to moisture content. All sensor voltages are fed to Fairchild 9708 analog to digital converters whose outputs can be selected by the program as input data.

Steam, heat, and vent solenoids are driven by the solid state relays within the interface box. On/off controls are linearized using a pulse width modulation scheme implemented in hardware. Duty cycle and length of each PWM output are selected by the program.

Approximately 20k bytes of memory were used for program and lookup tables. The general sequence of program operations was: (1) sample input channels, average each class of channels, and test for sensor error; (2) convert averaged data to meaningful units and test for range error; (3) compare values to interpolated values of desired setpoints; (4) output appropriate control signals; (5) update realtime clock; (6) output the average of selected data to bulk memory every six hours; and (7) test for end of run.

Although extensive offline tests have been made of the system and it has been used online, a complete drying run has not been made with the computer base system. Variables within the kiln have been sensed and controlled successfully. Current work on the system includes sensor improvement, system expansion with a line printer and a direct link between large online and small offline computers, development of a mathematical model for the kiln, and simplification of the optimization algorithm to hopefully result in realtime operation.

Control of a Natural Gas Converter

Successful development of a realtime water vapor concentration meter over a period of several years has been used as the basis for a project in Hungary to provide microcomputer based control for a natural gas converter.[2] A modified 6800 type microcomputer receives information from the conversion process; compares measured and required output signals and intervenes if necessary; computes output signals by means of the mathematical model, based on input signals; operates actuating devices on the basis of the various measured parameters; supplies information for the operator by printing values lying outside the normal range of process parameters or parameters requested by the operator; computes new set values whenever the flowrate is changed; and controls the process under abnormal service conditions.

Possible conditions encountered are deviation of process measurements, but within preset parameters, which require no intervention; deviation reasonably beyond those parameters, causing only computation and correction; and deviation far beyond the parameters, causing an alarm to sound. In this last case the deviation is printed out and feed is cut off.

Sugar Crystallization Control

Shorter crystallization time and more uniform grain have resulted from automation of the sugar crystallization process.[3] This project, conducted in Japan, was based on development of an intelligent vacuum pan controller that can handle up to six different sugar product types. The controller receives two 1.5-V signals from the process, and in return provides 4- to 20-mA signals to position water and syrup valves as well as to open steam or seeding valves.

Based on an 8085A microprocessor, the controller allows for different process sequences, crystallization algorithms, and operational parameters for each product type. All sequence segments and crystallization algorithms necessary for various products are stored in 8k bytes of ROM as subroutines, and the control scheme for each product type is specified by selecting and combining these subroutines in an internal data table with their operational parameters.

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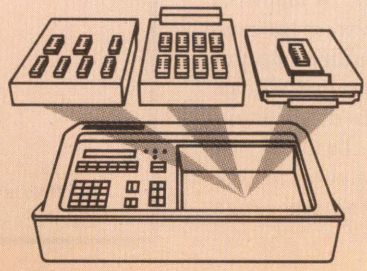
System 19/UniPak gives you design and purchasing freedom. This means you can select the best PROM for each application, and you can second-source for the best price and availability.

Semi-house approvals and easy calibration help maintain higher device yields. UniPak has earned written approval from device manufacturers. And easy calibration lets you keep performance within PROM manufacturers' specifications.

UniPak algorithms shorten programming time enhancing System 19's use as a production tool. UniPak is the first module to use a newly developed algorithm which makes it possible to program a 64K EPROM in less than half the time it takes to program a 16K EPROM using standard methods.

And the System 19/UniPak is easy to operate, with a minimum of operator training.

New System 19 concept is open ended to keep it state of the art. The System 19 is designed around a standard main frame and plug-in modules.



Modules available now include the UniPak, a gang programming pak for MOS devices, and a series of programming paks for logic devices and individual PROM families.

23 communication formats including six for development systems. Development systems, computers, teletypes and CRT terminals interface easily with the System 19. The System 19 accepts micro-processor instruction codes from Motorola, Intel, Tektronix, Fairchild, FutureData and other development systems without intermediary equipment.

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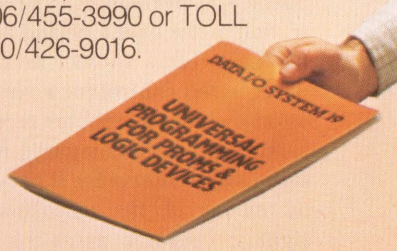

DATA I/O

CIRCLE 45 ON INQUIRY CARD

Hardware components include 1.5k bytes of RAM, process I/O circuits, power supply, and simple operator's console for product code entry and for manual operation.

During development stages, the program was stored in a FAMOS type EPROM to simplify program modification; however, once a proven program has been determined, it will be switched to electrically compatible ROM. Low power CMOS RAM, with lithium battery backup, is used for operational data and storage of process parameters.

Because the sugar crystallization process must be carried out in an electrically noisy environment, all circuits used in the controller design were chosen for their ability to withstand high noise. In general, however, the advantages of digital technology overcame other faults.

Operationally, the microprocessor periodically monitors process status and internal instrument hardware and alerts the operator with an alarm code on a panel display when any alarm condition happens. The microprocessor itself is continuously monitored by an integrated monitor circuit.

Hardware design for this system was simplified wherever feasible. For example, a single digital to analog converter serves for both analog input and output functions. For analog output, the DAC acts as an ADC and converts digital data from the microprocessor to a corresponding analog signal. An output circuit samples and holds the ADC output after multiplexer conversion to a 4- to 20-mA signal and transmits to the process. For analog input, the DAC's output is compared directly with a given input signal by an analog comparator, and the comparison result is read back to the microprocessor in digital form. The microprocessor performs the successive approximation algorithm by its program and emulates the A-D function bit by bit.

Field experience to date shows that crystallization time has been reduced from a minimum of 17 hours to a typical period of 10 hours. In addition, uniformity of crystal grain size over different batches has been improved to 0.294 from 0.354 by conventional means with 50% improvement of the product color value.

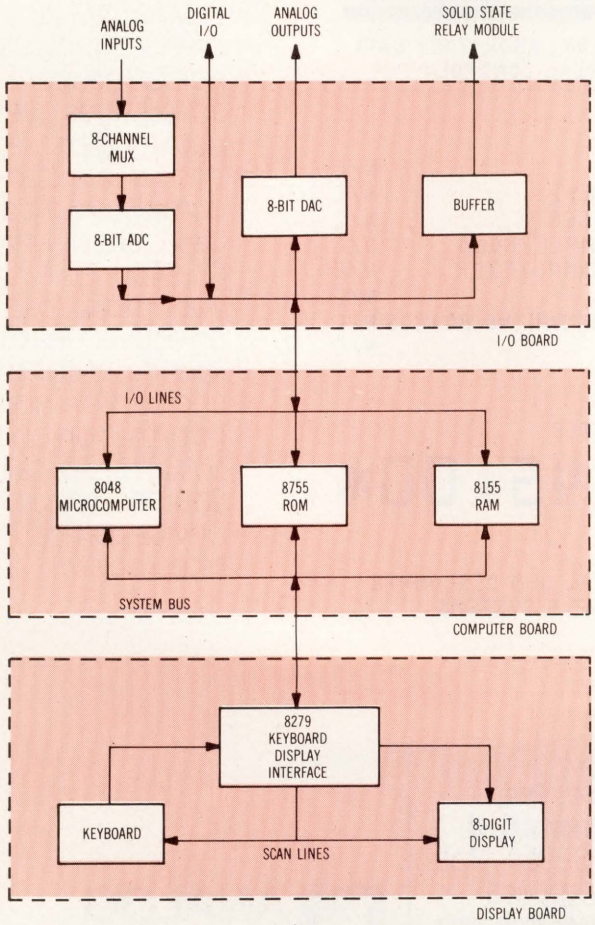

Fig 1 Georgia Tech temperature control system.[4] All components are on four boards—I/O interface, computer, and keyboard display shown here plus power supply. Success of design has shown that commonly available single-chip microcomputers can serve as effectively as minicomputers or specially designed microcomputers

Temperature Control

Investigation of a modular process control computer system at the Georgia Institute of Technology's Computer Ar-

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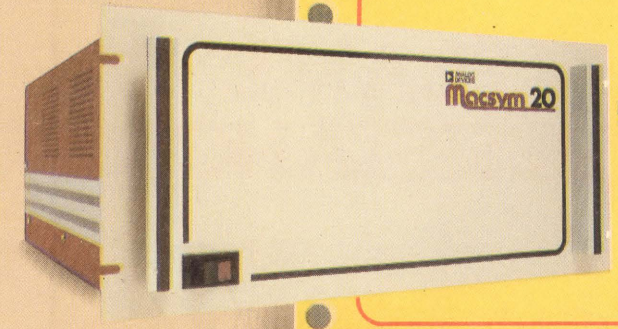
16K RAM (RANDOM ACCESS MEMORY)	N/C
DUAL RS-232C SERIAL INTERFACES	N/C
PRECISION 12-BIT ADC AND SAMPLE/HOLD	N/C
SOFTWARE PROGRAMMABLE GAIN AMPLIFIER	N/C
REAL TIME CLOCK	N/C
16 SLOTS FOR I/O SIGNAL CONDITIONING BOARDS	N/C
USER PROGRAMMABLE EPROM	N/C



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CIRCLE 48 ON INQUIRY CARD

chitecture Laboratory proved that the present generation of inexpensive single-chip microcomputers offer a cost-effective alternative to the previously used larger systems.[4] In the control system, input from a thermistor is corrected by piecewise linear interpolation, temperature is calculated by an integration routine, and the result is used by the control algorithm as output to set fluid control valves. Operator input is via a keyboard. Software requirements are only 1k bytes of ROM and 32 bytes of RAM.

As shown in Fig 1, one of four boards in the system contains an Intel 8048 microcomputer, two 2k-byte 8755A EPROMs, and a 256-byte 8155 RAM. This board provides 66 latched parallel I/O lines to interface with other boards over the backplane. The microcomputer itself consists of an 11-MHz, 8-bit processor with 2k bytes of internal ROM, 128 bytes of internal RAM, 27 I/O lines, and an interval timer; each of the EPROM devices has two 8-bit I/O ports; and the RAM device has 22 I/O lines plus a 14-bit programmable counter.

On the I/O interface board are a Datel MC8B 8-bit ADC (which also serves as an 8-bit DAC), buffers that drive an Opto 22 microprocessor I/O system to control ac or dc loads, an 8-channel multiplexer, and a prototyping area for custom signal conditioning circuitry. The display board consists of an 8279 keyboard/display interface chip, eight 7-segment displays, and a hex keyboard. The interface chip multiplexes the displays, encodes the keyboard, and buffers data, thus providing more microcomputer time for the control problem.

A multitasking monitor and several software utility programs were developed to aid applications programming. The monitor provides the capability to schedule tasks to run on any of four cycles, and initializes the various I/O devices after a power reset occurs. An internal timer or an external interrupt monitor times cycles and provides a realtime clock for use by other routines.

Utility programs include keyboard and display routines, A-D conversion, and 16-bit arithmetic routines. The keyboard routine returns a number entered on the keyboard, while the display routine outputs a number or message to the display. An ADC routine selects the appropriate channel, starts the ADC, and reads in the converted value. Value from the ADC is corrected using piecewise linear interpolation. A 16-byte table is required for each transducer. The 16-bit arithmetic routines include add, subtract, multiply, divide, load, and store.

Machine Control

Problems encountered in a manual operation of a hole punching machine at a manufacturing plant have been remedied by design of a microcomputer system.[5] In this system, an Intel SDK-80 single-board computer automates operation of a hole punching machine used to produce structural steel building elements for forming floating marina units.

Three modes of operation—manual, program, and automatic—are provided. In manual, the operator uses a set of nine control panel pushbuttons to operate the press. Under software control the system checks the validity of each input command before performing the requested action. In program and automatic modes, the same action occurs except that the sequence of commands is stored in RAM (see Fig 2).

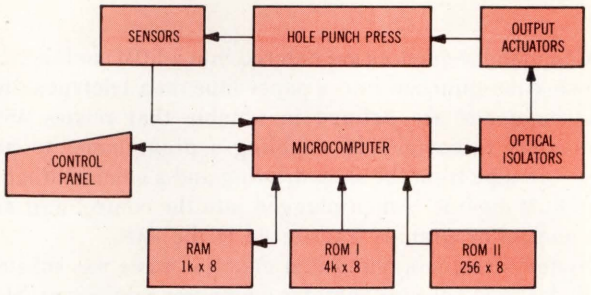

Fig 2 Automatic control system for hole punch press.[5] ROM II is programmed from information punched into paper tape and then plugged into control unit. When operator presses switch, program is transferred to RAM

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CIRCLE 49 ON INQUIRY CARD

Command sequences are entered into a ROM module from information punched into a paper tape on a teletypewriter. All commands are defined in a table that relates ASCII characters to commands, enabling a programmer to produce the tape from the shop drawing and a command table. The ROM module is then plugged into the control unit and the control program is transferred to the RAM.

System designers found that material waste was substantially lowered because operator action was minimized. Storing commands in ROM also reduced job setup time and assured that the machine setup would be correct.

Industrial and Commercial Controllers

Several other control systems discussed at IECI '80 included an industrial robot, an amusement ride, an engine/generator, and radar headway for automobile cruise speed. As shown, each has proven to be at least feasible.

Robot Control System

A 16-bit microcomputer, the SP-990/16, was developed in Torino, Italy, for direct numerical control of a 5-axis industrial robot.[6] Based on a Texas Instruments TMS 9900 microprocessor, the controller acquires data on the position of each axis, drives motor controls, accepts operator input via panel controls and a programming unit, and provides the interface for the necessary I/O.

Because the robot will have to cope with harsh environments, particularly electrical noise, all signals between the robot and the controller are transmitted through optical couplers. This frees the system from electromagnetic interference as well as from damage that might occur if high voltage lines were short circuited.

The robot continually follows the movement of a theoretical point along a chosen path. Each axis movement is controlled by closed loop architecture with two feedback levels. An inner velocity loop handles tachometer generator voltage signals, and a position control outer loop processes signals from incremental shaft encoders.

Each robot function is stored in P/ROM. The 3-part program consists of a movement control module, an interrupt management module, and a supervisor module that functions in the work mode.

Movement control is activated by a realtime clock interrupt. This routine provides coordinate computation from the shaft encoder counters' data; computation of the next point, in a cartesian coordinate system, to be reached at the next sampling period; transformation from cartesian coordinates to the jointed spherical coordinate system of the robot; position error evaluation and output to the motor drives; and at the end of each block, execution of special functions.

Results to date indicate that maximum speed for this robot is 0.7 m/s along a straight path, no matter how oriented; minimum speed is 7 mm/s. Worst case overall position error is less than 0.2 mm along a straight path. Repeatability errors are well below 0.05 mm.

Amusement Ride Controller

In an application considerably more involved that those usually found for microcomputers in the entertainment industry, an Intel MCS-85 has been installed as controller for a transportable parachute drop amusement ride.[7] The microcomputer controls drive motors to move the ride up and down, a stepping-motor-positioned valve to regulate speed, and an electric brake. Indicators provide data on ride speed, position, and safety factors, permitting the computer to offer flexible, but failsafe, operation independent of the skill or experience of the operator.

The microcomputer is made up of an 8085 CPU, an 8755 for EPROM and I/O, and an 8156 for RAM, counter and further I/O. All control signals are provided via the 8156's I/O ports and all data output from the ride mechanism use the same ports. This system is said to have proven successful and valuable as an example for further application in amusement rides.

Engine/Generator Control System

Realtime control of engine speed and generator voltage has been accomplished with a system based on a 6800 8-bit microprocessor with 256 bytes of RAM and 3k bytes of ROM.[8] Data on fuel level, oil pressure, and temperature from the 50- to 5000-kW diesel engine/generator are updated at least every 20 ms.

For the engine, the control system provides closed loop speed control in the single-set mode, closed loop load control in parallel mode, continuous temperature and oil pressure monitoring with alarm and trip functions, speed monitoring with overspeed trip, and display of speed and

(continued on page 83)

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TI745 Portable Terminal	1,595	153	85	57
TI765 Bubble Memory Terminal	2,595	249	146	94
TI810 RO Printer	1,895	182	101	68
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TI825 KSR Printer	1,695	162	90	61
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ADM31 CRT Terminal	1,450	139	78	53
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North Star has quadrupled the disk capacity of the Horizon computer but prices have increased a modest 15 percent. On a dollar per byte basis, that's a bargain that is hard to beat!

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CIRCLE 51 ON INQUIRY CARD

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Hazeltine announces the smart terminal for the eighties.

Executive 80™ is a beautiful new concept in smart terminals, designed to meet the needs of the new decade.

It's beautifully featured. Video highlighting, line drawing, smooth scrolling, programmable function keys, split screen display and variable character size are just the beginning of a long feature list, organized for such applications as data entry, form fill, data inquiry and software design.

It's beautifully flexible. There are two basic models. Executive 80, Model 20 is optimized for top price/performance in buffered or conversational environments. Model 30 is designed for high performance editing. Each can be ordered with detachable keyboard, and a 15 inch smooth scrolling monitor — the standard is 12 inch — which selectively displays either 80 or 132 column formats in normal size or double height and width.

It's beautifully reliable. The terminal has Hazeltine's traditional quality, to be sure. Executive 80 adds powerful self diagnosis, enabling the terminal to isolate its own failures. That means faster, less expensive maintenance.

It's beautiful to work with. High resolution characters are easy on the eyes. So is the non-glare screen, the full use of non-reflective surfaces and the user selectable double size characters. There's even a tilt display which when combined with the detachable keyboard lets users select the most comfortable work positions. A sculptured keyboard design takes the drudgery out of data entry.

With Executive 80, you can configure and feature your terminals for the maximum price/performance in your application. You can build in all the smarts your work demands. In the seventies, it was cute to be dumb. But in the eighties, smart is beautiful. That's why Executive 80 is such a beautiful buy.

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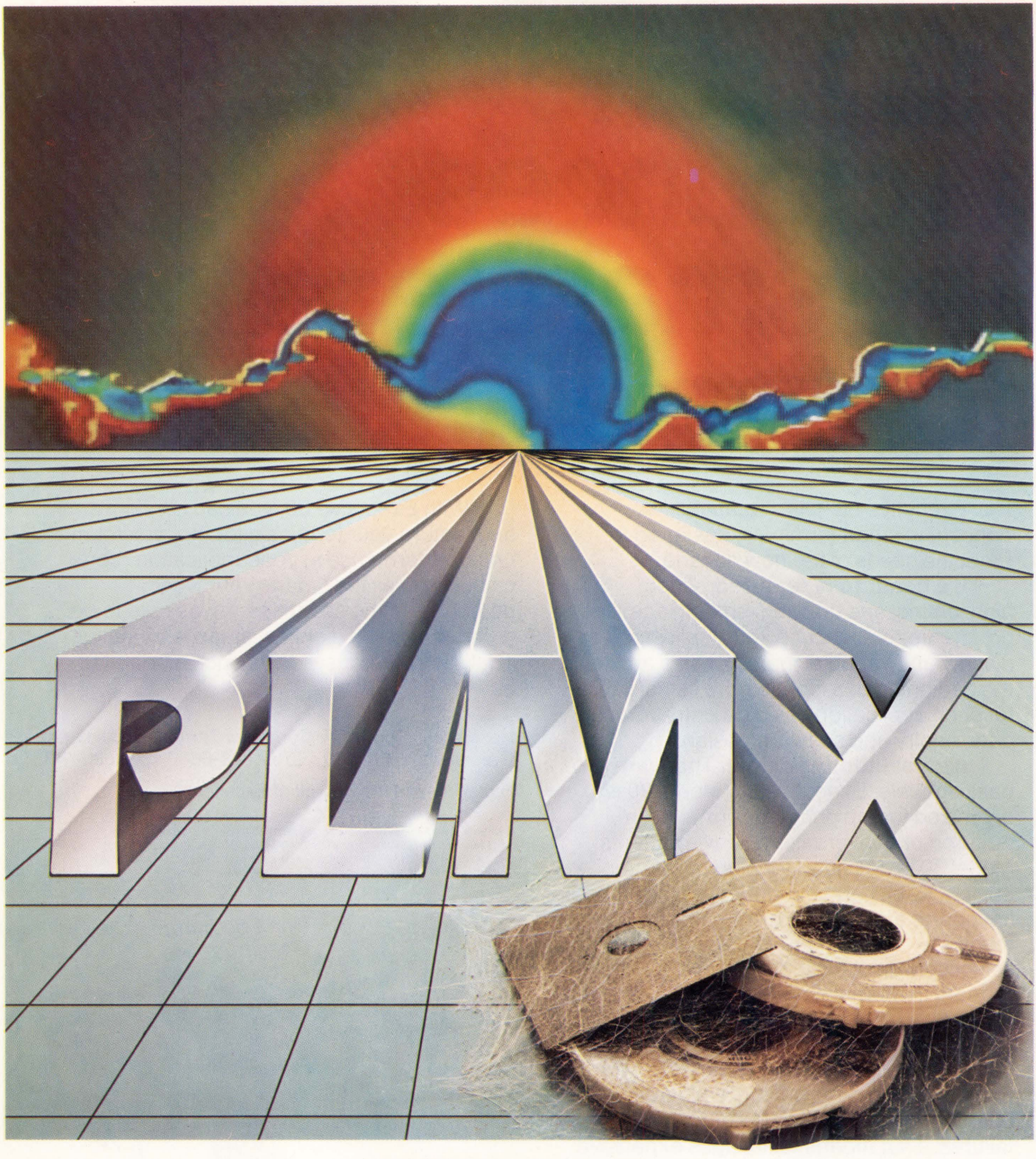
Hazeltine Executive 80

Answers for the Eighties

CIRCLE 52 ON INQUIRY CARD



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CIRCLE 53 ON INQUIRY CARD

temperature values. Generator control functions consist of closed loop voltage control in single-set mode, closed loop voltage and KVAR control in parallel operation mode, continuous temperature monitoring with alarm and trip functions, and display of voltages, current, power, power factor, frequency, and temperature values.

Automobile Headway Cruise Control

For the automobile driver who finds standard cruise control to be an advantage in highway traffic but is annoyed by having to occasionally manually accelerate or decelerate to avoid other vehicles, a system is in development that measures headway to the next vehicle and automatically adjusts speed of the automobile.[9] In this developmental system, an RCS 1802 microprocessor in a full size station wagon interacts with a radar unit that senses the distance to the next vehicle. The closing rate with respect to that vehicle is calculated and the throttle is adjusted automatically to maintain a safe distance between the two vehicles. Braking remains a manual operation.

Required data used in the throttle equations are sampled every 0.5 s. Test results show that the throttle can be controlled using digital techniques and not produce any jerking sensation; a properly designed radar can be used to sense range to a target, with a minimum of false targets to cause erroneous control decisions; and a car can be made to perform in the capture and headway following mode in a pleasant and predictable manner.

References

All of the following items are from the *IECI '80 Conference Proceedings.*

1. R. G. Fluet *et al,* "A Microcomputer Controller for a Kiln," pp 1-2
2. E. Simonyi, "Chemical Reactor Control with a Microcomputer," pp 10-14
3. K. Takahashi *et al,* "Intelligent Sugar Crystallization Controller," pp 15-17
4. J. O. Hamblen and C. O. Alford, "An Inexpensive Modular Process Control Computer," pp 71-73
5. P. S. Milligan and D. Rummer, "Microprocessor Control of Steel Punching Machine," pp 227-231
6. M. Bertino and M. G. Furxhi, "A Microcomputer Robot Control System," pp 367-372
7. V. P. Nelson and H. L. Fellows, Jr, "The Ripcord: A Microprocessor Controlled Amusement Ride," pp 373-376
8. G. R. Phillips, "A Microprocessor-Based Engine/Generator Control System," pp 377-380
9. W. R. Lile and M. Ilovich, "Radar Headway Control of an Automobile," pp 417-422

Copies of the *IECI '80 Proceedings, Applications of Mini and Microcomputers,* containing the text of most regular session papers presented, are available from the IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854. (Catalog #80CH1551-1.) The price is $25/copy.

IECI '81, again covering applications of mini and microcomputers, will be held in San Francisco from November 9 through 13. Tutorial and special evening panel sessions will be included.

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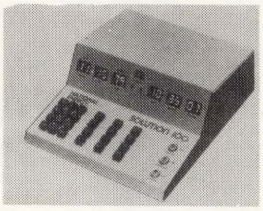
DC & AS BRIEFS

Energy System Controller Operates Over Existing Lines



Energy Systems Control, Inc, 90 Madison St, Worcester, MA 01608, has introduced the Solution 100, a wireless programmable energy system controller that communicates with remote teleswitch sensors over existing ac lines in a building to eliminate costly hardwiring installation. The desktop unit is user programmable from a central location, can store 85 individual programs, and can control any number of teleswitches. It accepts 24 to 480 Vac, and includes a locking keyboard for program security and a 16-h battery backup. Night/weekend setbacks, duty cycling, subcycling, and manual override are provided.

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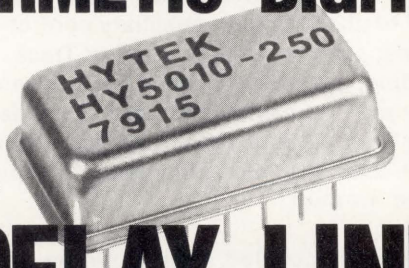

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Monitor/Control System Operates Remotely

As many as 40 remote monitoring and control systems from H. B. Engineering, div of the Madison Group, Inc, 722 N 5th St, Reading, PA 19601, can share the same transmission link and can operate in both directions simultaneously. Each REMOTEM can receive or transmit up to 16 intermixed analog parameters from or to a remote station via any common twisted pair, telephone line, or voice grade facility. High-low limit setpoints activate visual and aural alerts. Relay outputs are optional for remote control applications. Visual display, printer, and RS-232 computer interface are available.

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Single-Board Microcomputer Serves as Data Acquisition Unit

DAQ800-16, a complete data acquisition system, consists of an 8085 microprocessor, 16 analog input channels (8-bit resolution), 4k of EPROM, 4k of static RAM, two EIA RS-232 serial I/O ports, 44 parallel I/O lines, and two timers. Although originally developed by B. I. Inc, 1906 13th St, Boulder, CO 80302, for analog data logging, it is suitable for general purpose industrial applications. A P/ROM-resident montitor program provides many common debugging features including single-step operation.

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CIRCLE 57 ON INQUIRY CARD

DC & AS BRIEFS

UPS Systems Intended for Large Industrial Process Control Computers

Uninterruptible power supply systems rated at 75, 100, and 150 kVA have been introduced by Sola Electric, 1717 Busse Rd, Elk Grove Village, IL 60007, for use with large mainframe computers such as those in some process control installations. Operating efficiency is rated at 87 to 91%. A 12-pulse, phase controlled rectifier and a 12-step, pulse width controlled inverter using impulse-current commutation of the system's SCRs control output voltage are employed in the design. The inverter produces an ac voltage regulated to ±1% of rated voltage, while holding total harmonic distortion at the output to less than 5%. All status indicators are arranged in a "mimic bus" layout, with indicator lamps located on a system bus schematic, as a visual representation of the system power flow.

The systems measure 70 x 36 x 88" (178 x 91 x 223 cm); weights for the 75-, 100-, and 150-kVA models, respectively, are 4600, 5600, and 7000 lb (2086, 2540, and 3175 kg), not including the battery banks. Standard models are 120/208 Vac; 60 Hz; 3ϕ, 3- or 4-wire. Also available are 277- to 480-Vac models. Circle 446 on Inquiry Card

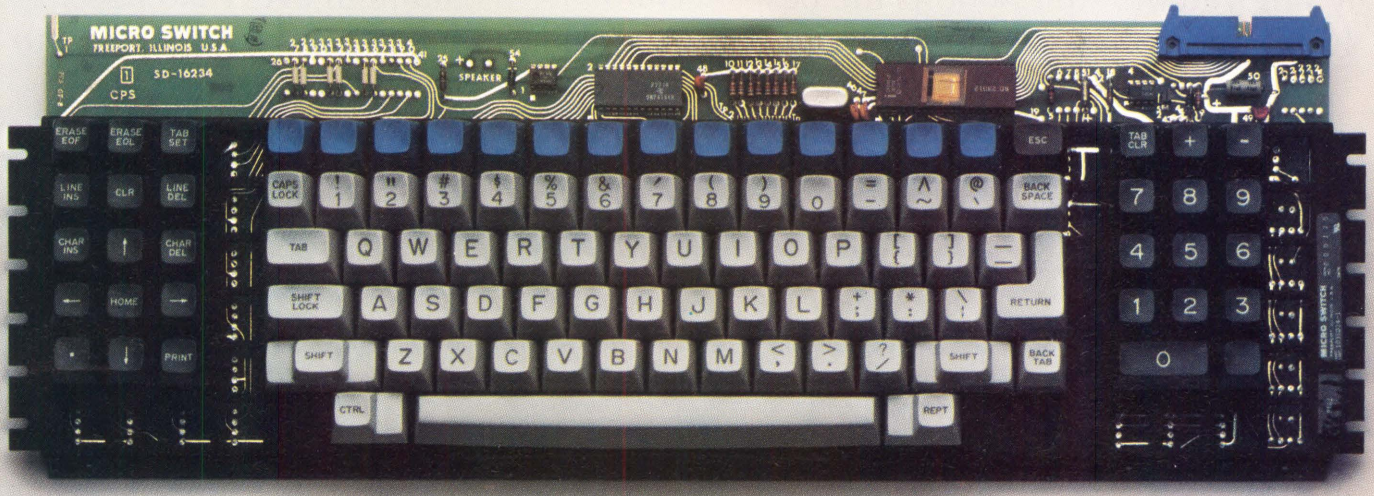
Plotting Program Generates Representation of NC Path

UCC-NC-PLOT II, an enhanced numerical control plotting program for users of UCC-APT on Digital Equipment PDP-11 systems, can generate and display a graphic representation of the machine tool cutter path to aid the programmer in verifying accuracy of the part program. Available from University Computing Co's Computing Services Div, Exchange Park, Dallas, TX 75235, the UCC-APT postprocessor generates a graphics data file to be displayed using the appropriate graphics display utility and online plotter. This graphics file contains the tool position data with default scale factors and the user defined frames, and can be interactively plotted using the utility routine. The interactive option permits the user to change the view, the scale factor, and the window selection of a plot to verify machining of the part. Translation and rotation can also be altered interactively. Circle 448 on Inquiry Card

Microprocessor Based Controllers Function in Industrial Environments

PC-744 series microprocessor based controllers are intended for use in industrial environments to interface with heavy duty type controls such as limit switches, pushbuttons, and solenoids. All input and output devices are optically coupled to the logic section and interfaced to the user's process by heavy duty barrier type terminal blocks. Available from Datatran Labs, Inc, PO Box 384, Sussex, NJ 07461, the controller is supplied either complete with the user's program debugged and stored in ROM or unprogrammed for those who prefer to write their own software packages including a fast floating point program. Modification of programs may be accomplished by replacement of a plug-in memory board. Standard features include an 8-bit 6800 series microprocessor with 4k of RAM and 8k of ROM. An RS-232-C serial port provides for operator interface. There are 32 digital inputs, 16 digital outputs, and 4 interrupt inputs that handle operating requirements. A heavy duty card cage assembly, with motherboard and power supply, provides noise immunity. □

Circle 447 on Inquiry Card



To sell the best terminal, buy the best keyboard.

The keyboard is one of the most critical components in your computer system. Which is why the first thing to consider when you buy a keyboard is reliability.

That alone is probably good enough reason to specify a Hall effect solid state keyboard from MICRO SWITCH. It's the most reliable keyboard you can buy. From the beginning, it will help you and your customers save money on repairs.

As a result of design innovations, the Hall effect keyboard is competitively priced against lower-performance, less reliable keyboards. Innovations like the microcomputer that gave you the first "intelligent" keyboard, the three terminal keyswitch module and single-sided printed circuit boards.

In addition, there's our Value Engineering Program.

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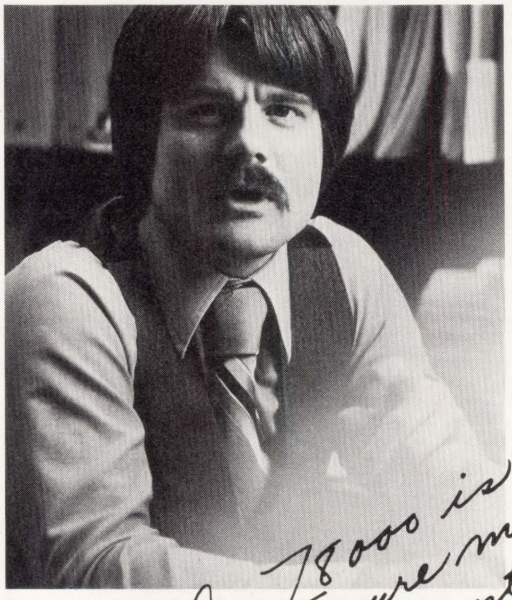

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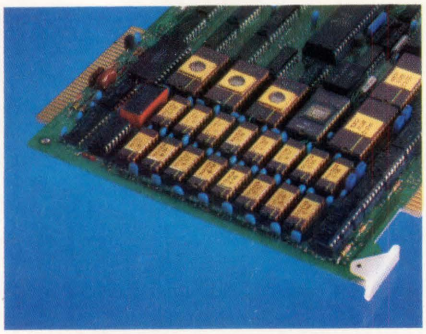

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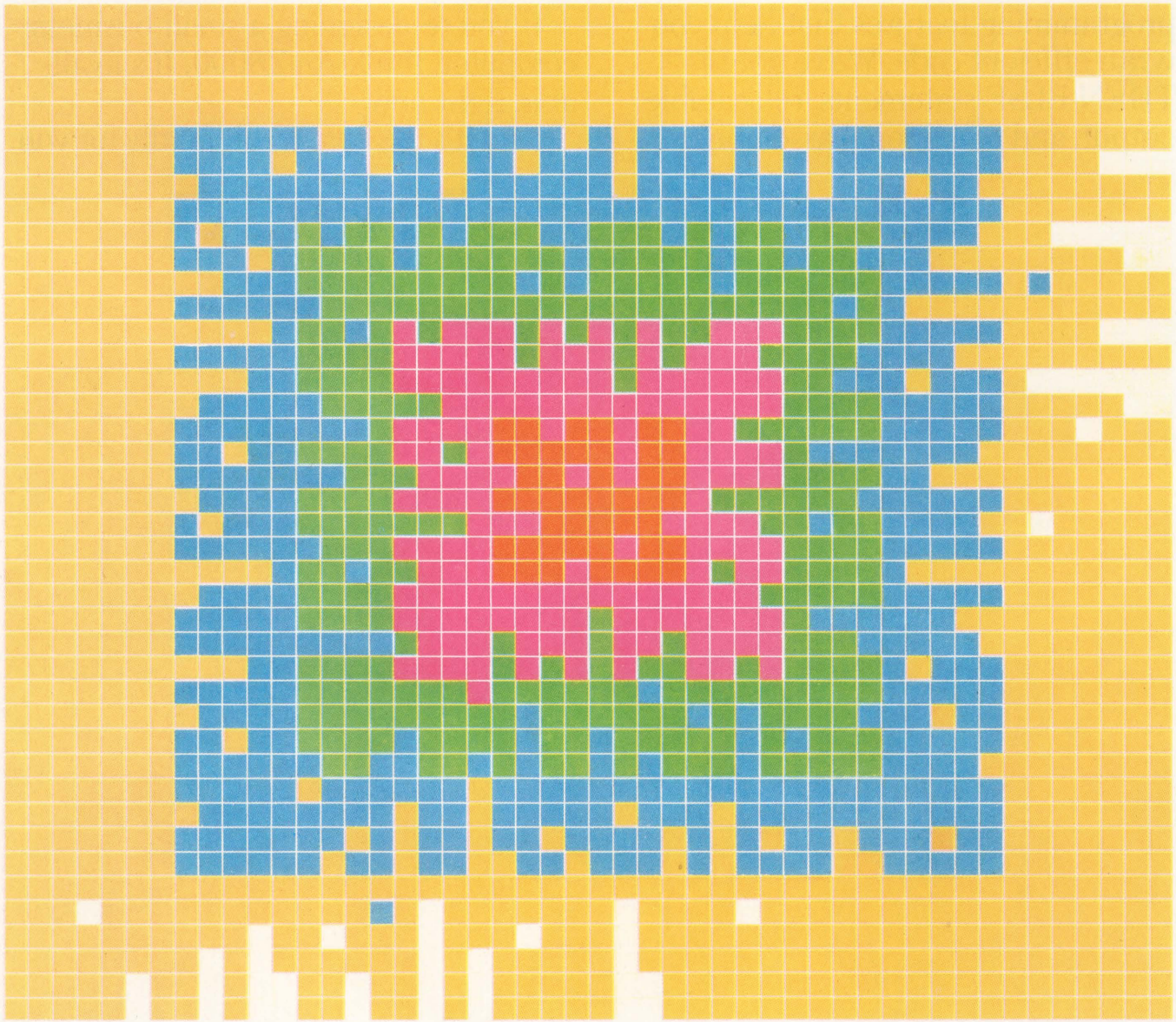

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DATA DRIVEN SYSTEM FOR HIGH SPEED PARALLEL COMPUTING— PART 1: STRUCTURING SOFTWARE FOR PARALLEL EXECUTION

Two-dimensional flowgraph model of program execution abandons the classical concept of using a program counter for sequential instruction execution. Alternative data driven approach helps achieve full potential for programming sufficient parallel activity into software to keep parallel hardware fully occupied

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Very high speed computer organization has become an area for extensive research because of the continuing demand for such systems. Part 1 of this 2-part article discusses the result of one such research effort, suggesting that the classical approach to computing be abandoned in favor of a data driven model that allows the full potential for parallelism both in hardware and in software. Part 2, to appear in July, will describe the architecture of a prototype system that implements the data driven model of computing.

An unwritten equivalent of Parkinson's Law has been known for years to apply to computer systems: No matter how large and fast a system is produced, someone, somewhere, always wants one more powerful. Thus, just as the potential of large vector and parallel computers is beginning to be realized, the National Aeronautics and Space Administration has initiated studies of machines up to 100 times more powerful for such tasks as aerodynamic simulation and weather forecasting.[1,2] No doubt other tasks are too vast to commit to even the largest of today's computers.[3] It is not surprising, therefore, that very high speed computer organization has become a fertile area for research, both in industry and in academia.

Although improvements to existing technology play an important role in increasing computing power, all recent large commercial and experimental computers also embody architectural innovations aimed at further improving their performance.[4] Invariably these innovations are based on some form of high level parallel activity in the system hardware, in the form of either a pipeline or a separated cluster of loosely coupled processors. Such approaches have proved successful in many ways; however, in every case permitting

large amounts of parallel activity, it has proven far more difficult to obtain parallelism in software than to provide it in hardware. In view of the nature of parallel hardware systems and the practical difficulties of keeping them running at full speed, data driven programs emerge as a natural reinterpretation of conventional programs with parallel execution in mind.

Basic Hardware Structures

The two basic parallel hardware structures are the pipeline and the parallel array. Both may be either synchronous or asynchronous structures. Parallel computers rarely consist of only one such structure; rather, they rely on a mixture of several basic types in a hybrid cluster. It is instructive to study the performance of such systems for the lessons to be learned about efficient use of parallel hardware.

Perhaps the simplest way of viewing the basic pipeline structure (Fig 1) is to imagine that each stage comprises an input register followed by some combinational logic that forms the output of the stage. Each stage has an associated time delay, as data pass into the register and through the combinational logic, and a clock arranges transfer of all stage outputs into the following input register after waiting for the longest delay in the pipeline. This is a synchronous scheme, and it makes sense to have delays all of about the same duration.

Some systems, such as CRAY-1, use no registers and arrange for all paths through the combinational logic to be of exactly the same length. In systems where the pipeline stages are more complex, and stage delays of different durations occur, it may be worthwhile to use an asynchronous scheme. In this approach transfer of data to the next stage occurs after enough time has elapsed to perform the current stage activity, provided that the next stage is ready for input. Such schemes normally use an output register for each stage, so that a stage can begin its next operation even if the following stage is unable to accept input immediately. Conversely, when a stage completes its task, it may have to wait for input to arrive before starting the next operation.

Synchronous systems afford optimum throughput when there is a task for every stage in the pipeline. Every clock period, Δt, then produces a result. An N-stage pipeline produces N times more results than one complete operation involving all pipeline activities, giving an apparent N-fold speedup. If, for any reason, a pipeline stage remains inactive for a period, results are produced more slowly. In the case where, on the average, only a proportion, f, of an N-stage pipeline is occupied, the time between results increases to $\Delta t/f$.

Similar reasoning applies in asynchronous pipeline systems where the variable delay between results makes it more difficult to give precise expressions for throughput. Asynchronous pipeline throughput slows when input registers must wait for results being produced as output from the previous stage. If only a fraction, f, of asynchronous pipeline stages are occupied, on the average, the average time between results increases to $\Delta t^*/f$, where Δt^* is the maximum average stage delay.

Fig 2 shows a simple parallel array structure. Individual parallel units perform relatively complex tasks and take long periods of time to produce results. There are several ways of arranging work for parallel array structures. Sometimes, as in the CDC 6600, they are fed from the output of a pipeline, and the units receive tasks in rotation simply to allow the slow parallel array units to accept work at a suitable rate from the fast pipeline.[5] Such structures may be synchronous or asynchronous according to the nature of the pipeline. Other synchronous systems, such as ILLIAC IV, lock the parallel array units in step with one another so that all perform the same action at the same time, usually on different sets of data.[6] Certain asynchronous systems, such as C.mmp, allow complete autonomy in the parallel array units, except when accesses to shared memory conflict.[7]

Performance of parallel array structures depends on the delays in each unit (T_i), the number of units (N), and the average fraction of units that are occupied (f). The average time between results is

$$\frac{1}{f \sum_{i=1}^{N} \frac{1}{T_i}}$$

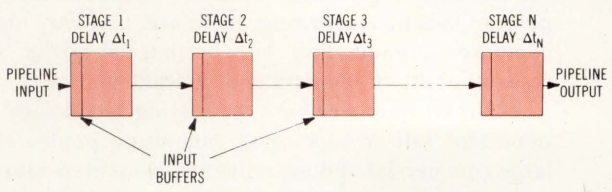

Fig 1 Basic synchronous pipeline structure. Each stage contains input buffer register, and each transmits output to next stage. Ideally, stages should be independent, with uniform delay Δt. Overall pipeline delay is then $N\Delta t$. Pipeline produces results at maximum rate of one every Δt, but input starvation and interdependence between stages limit activity to some fraction (f, on the average) of stages. Results then appear once every $\Delta t/f$, on the average. Asynchronous pipelines are similar, but stages may have very different delays. Figures remain valid if Δt is average maximum delay

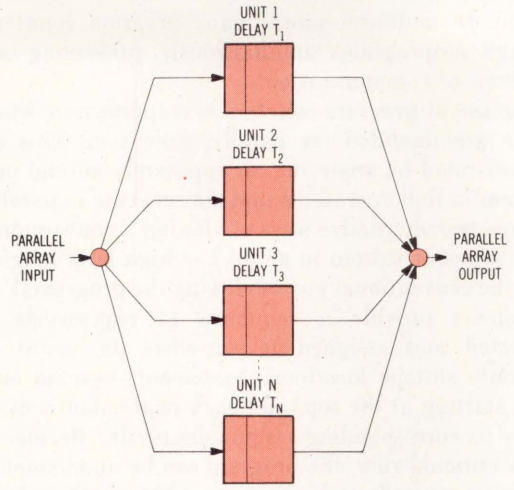

Fig 2 Basic parallel array structure. Inputs and outputs arrive or leave either in parallel or via pipeline structures. Each unit buffers its input. Unit delay is relatively long, but multiple results produced in any one delay time improve throughput up to N-fold. As with pipelines, events conspire to leave some units idle. If only fraction, f, of N identical units with delay T are occupied, maximum throughput is one result every T/N and expected throughput averages one result every T/Nf

When the parallel array units have identical time delays (T), this reduces to T/N f.

Hybrid Structures

Most practical attempts to use parallel hardware combine pipeline and parallel structures, allocating lengthy independent tasks to a parallel array structure and assigning to a pipeline brief tasks that depend on previous tasks for input. Paralleled tasks typically include arithmetic—particularly multiplication and division—and complete instruction execution in lockstep systems. Typical pipelined tasks include instruction fetch and decode, operand fetch, and even some arithmetic (eg, in the AP120B floating point array processor).[8] A typical hybrid structure, the CDC 6600, uses a pipeline for fetch and decode tasks, followed by a parallel array of two adders, two multipliers, a shifter, and a divider.

In parallel structures, the major design goals are to match connected section throughputs and to minimize idle time so that performance is optimal. In many systems built to date, it has proved difficult to keep the parallel hardware fully occupied. The table summarizes problems encountered in different kinds of parallel system. As might be expected, all departures from optimum performance result when part of the parallel hardware is idle. Thus, in instruction pipeline systems like the IBM 360/91, instruction flow disruptions due to branching, especially conditional branching, cause the most trouble.[9] Observation has verified theoretical analysis, showing a sharp decrease in performance as the frequency of branches increases.[10, 11]

Machines with data pipelines, such as CRAY-1 and the CDC STAR, encounter similar problems when their data streams are interrupted.[12] This typically occurs at the beginning and end of array arithmetic operations. It causes maximum disruption when processing scalars—arrays of length 1. CRAY-1 also exhibits such discontinuities at every 64th element of large arrays. Parallel lockstep systems, like ILLIAC IV, often have only small disjoint data sets on which to perform the common operations. This naturally degrades performance by leaving large amounts of hardware idle.

Systems with parallel operation units, such as the CDC 6600, contend with another problem. They must be sure that operation unit output registers contain valid data before using the registers as operands for different operation units. This form of memory access conflict also occurs at the parallel processor unit level. For example, shared memory multiprocessors, such as C.mmp, have problems with physical address conflict during memory access.

Two logical difficulties in programming parallel systems overshadow the hardware problems. Each complete pro-

Comparison of Representative Parallel Hardware Systems

Parallel Hardware Arrangement	Representative System	Problematical Program Features
Instruction Pipeline	IBM 360/91 CDC 6600 MU5 Amdahl 470 V/6	Branch Instructions
Vector Operation Pipeline	CDC STAR CRAY-1	Scalar and Short Vector Operations
Lockstep Parallel Array	ILLIAC IV ICL DAP	Nested Branching Through Data Set
Operation Parallel Array	CDC 6600 IBM 360/195	Register Access Conflict
Instruction Parallel Array (Shared Memory Multiprocessor)	C.mmp Cm*	Bad Partitioning of Application: Lockout and Memory Access Conflict
Process Parallel Array (Message Passing Multiprocessor)	CH_0PP	Application Partitioning: (Message Synchronization)

gram must be decomposed into a suitable number of smaller program segments that can execute on the individual parallel units. It is rarely easy to make these segments similar in complexity; instead, longer segments continue to execute after the shorter ones have finished, leaving some parallel units idle. Furthermore, when implementing semaphores or other intersegment communication mechanisms, a unit often must "lock" certain memory areas to guarantee sole access to storage. Concurrent access to locked memory causes other units to idle until the memory is unlocked.

Recent attempts to overcome such problems led to the concept of message passing parallel multiprocessors.[13, 14] Program partitioning remains a problem, even in message passing multiprocessors, and idling still occurs while processors wait for messages to arrive.

Essential Software Features

Programs must exhibit some form of regularity if they are to perform well in a particular parallel hardware structure. The form of regularity required varies with the structure. This is not surprising, but it is problematical because regularity rarely exists in necessary quantities to allow these systems to run near their optimum speed. Some applications obtain impressive results using multiprocessors, but only after a large programming effort devoted to partitioning the program. Ideally, one would like a hardware structure in which the sole problematical program would use a totally sequential algorithm. This can be achieved only by changing programming language conventions.

The underlying trouble with most current attempts to use parallel hardware is that they are based on traditional concepts of programming. These concepts in turn are based wholly on the serial von Neumann computer design, with instructions executed one at a time. In particular, use of a program counter remains obligatory. In instruction pipelines, no attempt is made to alter the basic von Neumann model. In vector and array processors, one instruction may operate on many pieces of data, but only one instruction executes at a time. In multiprocessors, many program counters step through subprograms simultaneously, presenting complex problems of communication.

The use of program counters is inappropriate when programs are intended for parallel execution. This can be demonstrated by analyzing an apparently normal program segment to find operations that may execute in parallel. Fig 3 shows two alternative ways of viewing a conventional program segment written in an *ad hoc* high level language.

In the conventional way of viewing the program [Fig 3(a)], statements provide a sequence of expressions to be evaluated and assigned to variables (ie, saved in appropriate storage locations). Statements execute one at a time, starting at the top, and each expression is evaluated before its corresponding assignment occurs. Because this is a conventional view, the program can be understood by executing it mentally and determining the changes of value in various storage locations holding the assigned variables.

Alternative Programming Concept

The alternative way of viewing the program [Fig 3(b)] is less familiar, although the program text retains the same format. The meaning is now defined by superimposed arcs that indicate certain time dependencies between expression evaluations and assignments. These are called data dependencies, of which two kinds are shown.

A solid arc shows assignment (as generation of data) at its tail, with subsequent consumption of data (during expres-

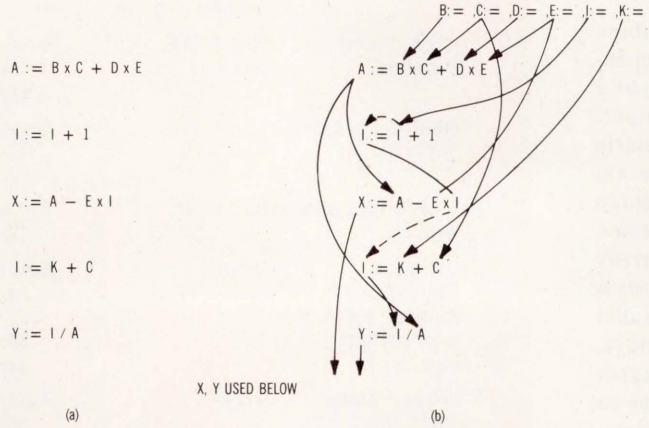

Fig 3 Segment of conventional, high level language program. In (a), program is viewed normally as sequence of expression evaluations and appropriate assignments to storage. In (b), data dependency arcs superimposed on program distinguish expressions that must evaluate in sequence from those that may evaluate concurrently. Solid arcs show that data must be generated before being consumed. Broken arcs indicate programmer reassignment of storage location whose old value must be consumed before being overwritten. Execution allows data to flow down solid arcs. Expressions are evaluated when all needed data arrive

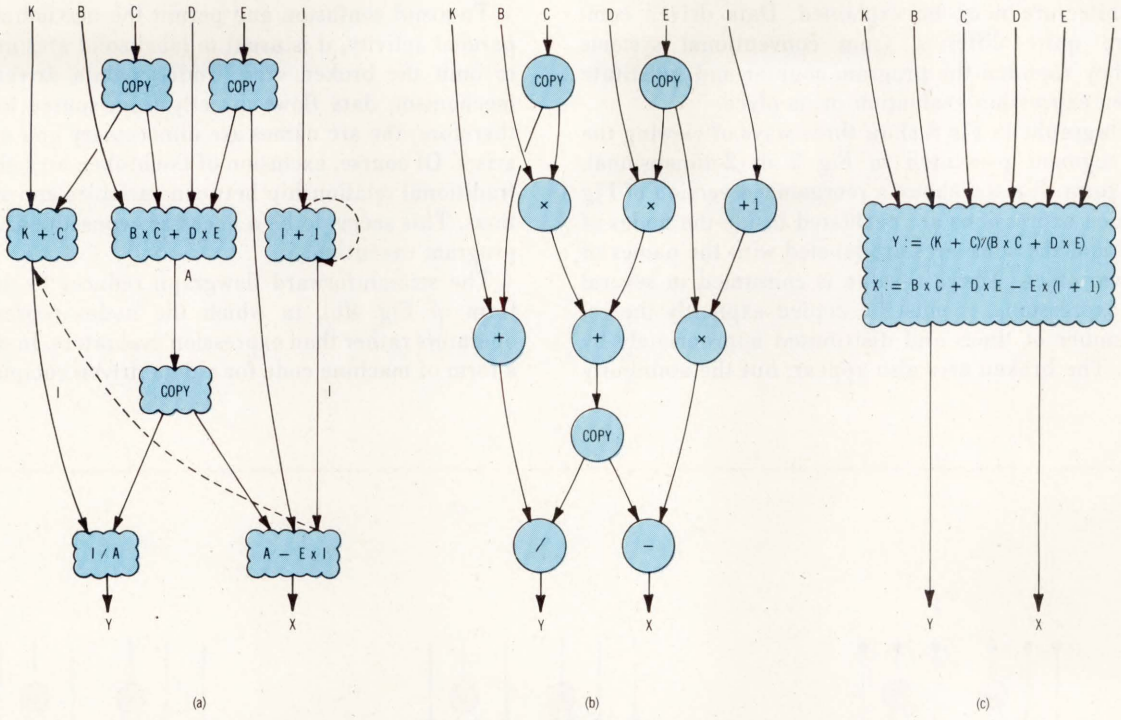

Fig 4 2-dimensional data flowgraphs. Program segment from Fig 3 is reorganized (a) into 2-dimensional form. Expression evaluations become nodes in graph, with solid arcs showing data paths between nodes. Arcs are labeled with variable names. Broken arcs are unnatural, in this form, since they show sequential reuse of storage. Abandoning this view, and adopting unique naming scheme for solid arcs, eliminates need for broken arcs. In reduced form (b), flowgraph nodes are primitive operators provided in data driven computer machine code. In (c), high level form of (a) and (b), entire program segment appears as composite function that consumes six inputs and produces two outputs

sion evaluation) at its head. Naturally, generation of data must precede its consumption. A broken arc indicates reuse of a storage location by programmer dictated reassignment. In this case, the assignment (generation of new data) is at the head of the arc, while consumption (of previous data) is at the tail. Because of the conventional meaning of the program, this consumption must precede reassignment of the variable's value. No arcs in the program point upward. This will hold true for all blocks of assignments that are reinterpreted by superimposing data dependency arcs.

These two ways of viewing a program constitute two different models of computation. The models are equivalent, since the end results of both interpretations are the same. However, the second makes it easier to find activities that can execute in parallel. These activities become more apparent because the model does not use the concept of a program counter, stepping through statements and activating them one by one; instead, it uses the solid data dependency arcs to transmit data directly from the point of generation to the point or points of consumption, and activates expression evaluation upon arrival of all required data. Imagining execution under this mechanism, it is easy to see that several statements in the program are completely independent and could execute simultaneously.

Data Driven Computing

This single step toward reinterpreting the meaning of programs is all that is strictly required for the transition from conventional computing to data driven computing. However, consequences of the change need refining in at least three ways in order to show the considerable potential of data driven computers.

The data dependency notation of Fig 3(b) needs improvement. Because it is superimposed on the program text, it tends to obscure rather than clarify the situation. Unfolding the program into a 2-dimensional map helps this to a large extent, but also makes it obvious that the broken arcs can represent an unnecessary impedance to parallel execution and could be removed usefully.

Moreover, other types of high level language statements must be reinterpreted. No practical program consists solely

of assignments to scalar variables. In fact, the traditional control structures for conditionals, iterations, and recursions all must be modeled.

Finally, implications of the data driven model for computer architecture must be explained. Data driven computers are quite different from conventional systems because they abandon the program counter and substitute data driven expression evaluation in its place.

Data flowgraphs in Fig 4 show three ways of viewing the program segment presented in Fig 3 in 2-dimensional, graphical form. Fig 4(a) shows a reorganized version of Fig 3(b) in which expressions are evaluated inside the nodes of the graph and the solid arcs are labeled with the names of assigned variables. Where a value is consumed in several different expressions, it must be copied explicitly the requisite number of times and distributed appropriately by solid arcs. The broken arcs also appear, but the ambiguity of different solid arcs with the same name at head and tail clarifies their artificiality. Broken arcs may point upward, indicating that their implied reassignment could delay parallel execution unnecessarily.

To avoid confusion and permit the maximum amount of parallel activity, it is usual to label solid arcs uniquely and to omit the broken arcs. Under a data driven execution mechanism, data flows directly from source to consumer; therefore, the arc names are unnecessary and no confusion arises. Of course, exclusion of the broken arcs abandons the traditional relationship between variables and storage locations. This seems to be a necessary consequence of parallel program execution.

The straightforward flowgraph reduces to the primitive form of Fig 4(b), in which the nodes represent simple operators rather than expression evaluators. In effect, this is a form of machine code for a data driven computer capable

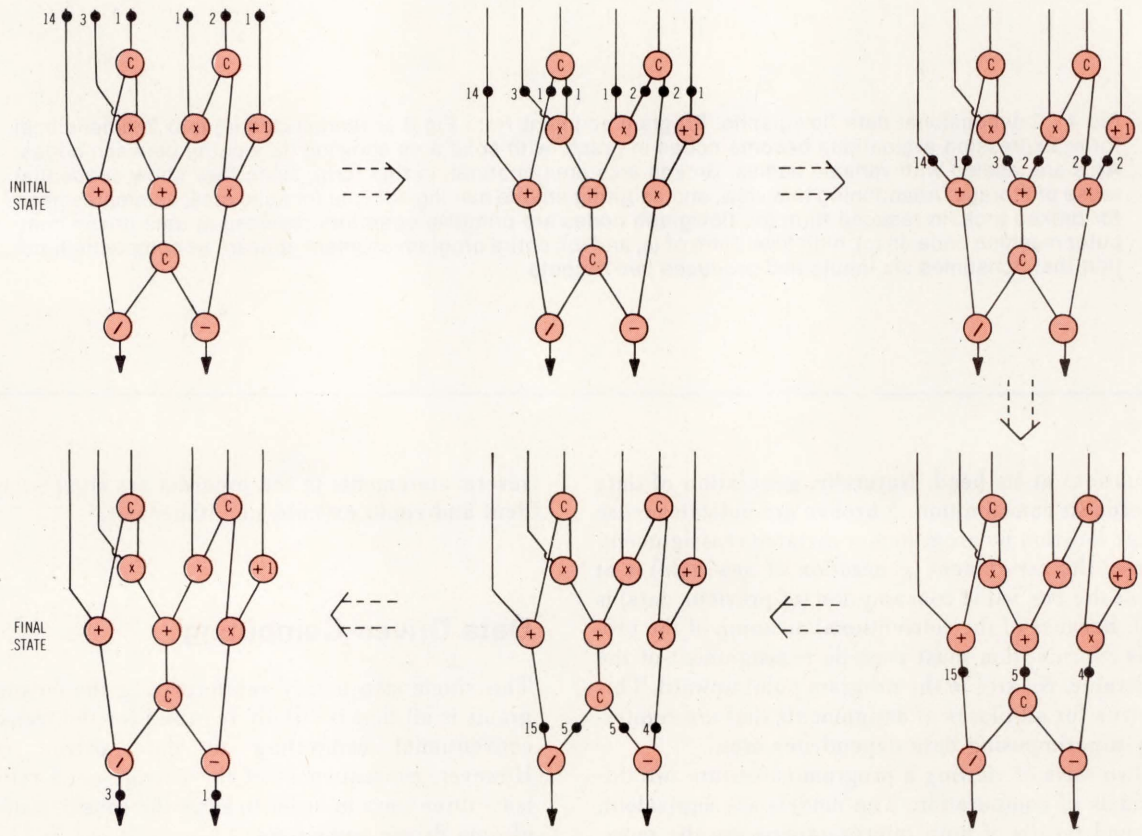

Fig 5 Data flowgraph execution mechanism. Data values pass through graph as tokens, shown as solid discs resting on arcs of primitive flowgraph from Fig 4(b). Value appears alongside token. Execution snapshots follow firing rules and show how computation might progress from initial presentation of six input values to final production of two output values

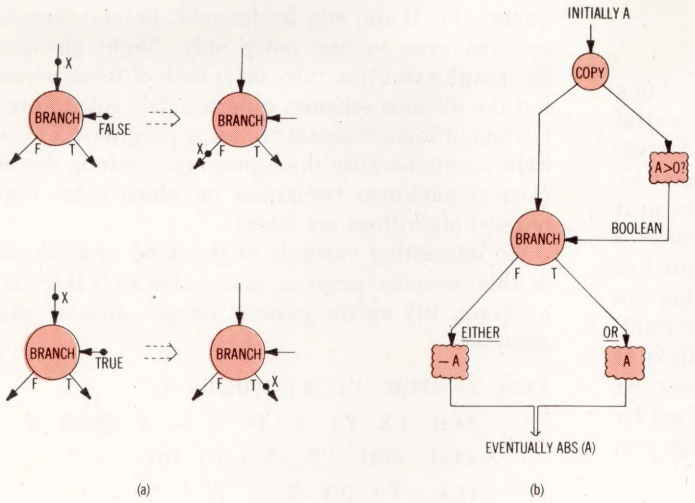

Fig 6 Conditional computation. Flowgraph (a) shows two possible firing sequences for primitive branch operator. Input data token feeds one of two output arcs, according to value of Boolean input control token. In (b), high level conditional expression evaluation for ABS := IF A≥0 THEN A ELSE –A, either A or –A results according to the value of Boolean expression A ≥ 0. Under no circumstances are both expressions evaluated

of performing addition, subtraction, multiplication, and so on. The copy operation must be part of the instruction set.

Fig 4(c) shows how the entire program segment might be viewed by the rest of the program. The main program sees a node that requires six input values and yields two output values, which are functionally related to the inputs by the expressions given. In the limit, any program consisting entirely of assignments can be expressed as a single node consuming its input and eventually producing its output. Inside a computer, however, it will be represented by its primitive form.

Parallel Execution Mechanism

While the graphs in Fig 4 reflect data dependencies inherent in the program segment, they indicate no way of executing the program. Fig 5 presents an execution mechanism for the machine code form of the flowgraph.

During program execution, data values pass through the flowgraph on tokens represented by solid discs traveling along the arcs. Tokens always travel from the tail of an arc to its head. They may travel at any speed, independent of one another. Any necessary synchronization of tokens occurs at the head of an arc, before the operator is invoked. Each node in the graph waits until every arc pointing toward it contains a token. At this stage, it is said to fire. It proceeds to consume all incoming tokens—one from the head of each arc—and to perform the appropriate operation on the input data. After a time, it produces new tokens of appropriate value on the tails of its outgoing arcs.

Repeated application of the rules for tokens, arcs, and nodes, in any order and in any number, eventually yields the required results. Fig 5 demonstrates the potential for parallel activity in the given program segment by showing the shortest possible evaluation sequence. The executing system would need at least three parallel units to achieve this shortest sequence.

It is convenient to discard those vestiges of the conventional model of computation that seem unnatural in the data driven model. In particular, the basic notation changes from 1- to 2-dimensional form; a token based, data driven model of execution supplants the serial, program counter model; and the traditional relationship between variables and storage locations is abandoned. Acclimatization to the new model stops at this point, and further refinements to the data flowgraph notation are independent of similar refinements to the basic von Neumann model. Any similarities are due only to the common influences that led to the need for improvements in both models.

Conditional Execution

The first refinement is the ability to compute a value conditionally, based on some predicate. A data flowgraph achieves this by using a primitive branch operator that selects one of two output arcs on which to place its first input data, according to the state of a second Boolean input value. The two possible firing states lead to the execution sequences shown in Fig 6(a). The operator can be used to achieve conditional expression evaluation at a higher level. Fig 6(b) shows a natural translation of the high level conditional "assignment":

ABS := IF A ≥ 0 THEN A ELSE –A

Conditional flowgraphs should be constructed with caution, since the absence of tokens flowing down some arcs might leave other tokens stranded at inputs to nodes. Conditional expressions, such as the one in Fig 6(b), are "safe"

provided that both THEN and ELSE expressions are stated and are of the appropriate type. Traditional conditionals are generally troublesome and require substantial modification to massage them into a "safe" form.[15]

Iteration and Recursion

Provision of conditional evaluation alone does not lead to a completely general model, but it proves extremely powerful when combined with cyclic or reentrant flowgraphs. For example, an iterative or loop construct can be implemented by conditionally deciding whether to send tokens to the next block in a program, or to recycle them through the current block. Fig 7 gives a simple example of such a construct in primitive form. This program evaluates the factorial of the left-hand input, N, given a starting value of 1 on the right-hand input. It achieves this by repeated multiplication of cumulative total Y (initialized to 1 by the external starting value) and successive X values from N to 1 (initialized by the external value). A conventional, high level language program might express this as

```
X := N
Y := 1
WHILE X > 0 DO BEGIN
      Y := Y * X
      X := X - 1
      END
FACN := Y
```

This deceptively simple example demonstrates a major problem associated with some cyclic graphs. The problem arises because one of the recycled values, Y, is not used to evaluate the Boolean condition governing the loop. If, for example, multiplication takes a long time compared with all the other primitive operators, the loop might generate many values of X asynchronously, queuing Boolean tokens on arc L and X tokens on arc M, while waiting for corresponding Y tokens to be created.

Of course, it is essential to maintain such queues in sequence, but it also may be desirable to limit them in length, perhaps even to one entry only. Slight changes to the flowgraph execution rules meet both of these requirements, but the obvious schemes unfortunately rule out correct execution of some compact recursive programs. This is doubly unfortunate because these programs include the important class of nonlinear recursions on which many high speed, parallel algorithms are based.

An interesting example of this kind of algorithm is the double recursive program that evaluates N factorial. In this program, DIV means positive integer division with no remainder.

```
FACN := FFAC (1,N) WHERE
      FFAC (X,Y) := IF X = Y THEN Y
      ELSE FFAC (X,(X + Y) DIV 2) *
      ((X + Y) DIV 2 + 1,Y) ;
```

This program evaluates N! in a period of time proportional to $\log_2 N$, making it the fastest known solution. The important characteristic of the algorithm is the way it repeatedly splits the problem into two roughly equal halves, which it evaluates simultaneously until it can form the required result with just one multiplication. This kind of parallel, divide and conquer approach provides fast solutions to many programs. It seems essential to implement it in the data flowgraph model.

Fig 8 shows the basic form of a flowgraph program for the double recursive factorial algorithm. An added symbol—the rectangular node—indicates a recursive call to the named function; in this case, the program graph itself. There are two approaches to implementing such nodes. The first scheme copies the functional flowgraph each time tokens

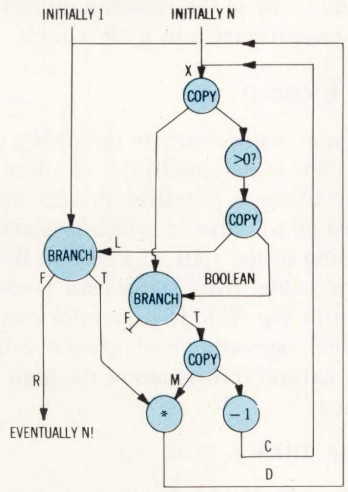

Fig 7 Iterative or looping computation. Flowgraph evaluates N! by repeatedly multiplying values from N down to 1. Computation begins by feeding initial values 1 and N into loop inputs X and Y. Then, Y is multiplied by X and X is decremented repeatedly, until X = 0. At this stage, Y = N! and is directed to graph output. Because updated value of Y is not needed to decide whether loop is finished, subloop generating values of X can race ahead and produce many tokens on arcs L and M, all waiting for corresponding Y values to be produced. These tokens must be queued on arcs or else labeled and combined in some systematic way

are directed to it.[16] An advantage in this case is that hardware queuing on the arcs allows correct execution; however, it requires runtime copying of graphs, consuming both time and space in a system.

The alternative scheme reuses a single copy of the recursive graph in much the same way that a conventional recursive procedure reuses its instruction list. Fig 8 shows that two logical problems must be solved to make such a scheme viable. There must be some means of encapsulating each application of the single graph so that tokens from different calls do not get confused with one another. Secondly, there must be a means for directing output from the single graph to different destinations—for example, the two inputs to the multiplication node.

In the second scheme, separate calls to a function are embedded in an interface which relabels all ingoing tokens uniquely and delabels (the reverse of relabeling) the outgoing tokens. It is helpful to imagine this process as "coloring" the tokens. Tokens that logically belong together receive the same color.[17] Each token must now carry a label and color, as well as a data value, and the flowgraph execution rules must be adjusted so that only tokens with the same label cause a node to fire.

Since these tokens may need to be selected in an indeterminate sequence, strict queuing of tokens on arcs must not be used. To achieve the variable routing of function output, the delabeling system also arranges to direct the delabeled tokens to the appropriate destination points.[18, 19] Precise details of the relabeling and delabeling mechanism are beyond the scope of this article, but it is worthwhile to point out the immediate consequences of colors as a mechanism for distinguishing levels of usage in a reentrant flowgraph.

Parallel and recursive function calls are achieved without copying graphical code. The mechanism can also be applied to iterations, thus averting a contradiction in the need for arcs to queue tokens. For example, in the loop of Fig 7, the tokens can be relabeled incrementally at points C and D, and delabeled as they exit at point R. In whatever order the rules are applied, the graph achieves the desired solution. It is also possible for the colors to distinguish elements in data structures. The penalty for all this generality is that every token must carry a label, a small price to pay compared with the runtime copying of code otherwise required.

Data Structures

Flowgraphs are a powerful set of templates for implementing the high level control constructs: conditionals, iterations, and recursions. However, practical languages also provide high level data structures, such as arrays and records, which a flowgraph model must handle. There are several ways of approaching this problem, but little consensus exists as to the best scheme. Records, arrays, and streams are the three most popular structures being tested.

Records are merely logical groups of arcs that go under a common "variable" name. They require no new understanding of flowgraphs, and languages provide them merely

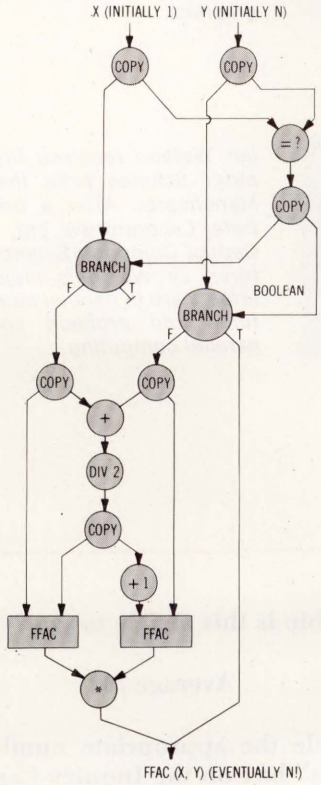

Fig 8 Recursive computation. Flowgraph performs high speed evaluation of N! by recursively splitting the range of numbers to be multiplied so that it can multiply all adjacent pairs, then all pairs of pairs, and so on, until last product forms answer. Square nodes represent parallel recursive calls to program graph itself, implemented either by copying graph each time it is entered or by uniquely labeling (coloring) tokens entering recursive calls to distinguish tokens by call. Program illustrates parallel, "divide and conquer" technique used in high speed solutions to many problems

as a convenience to programmers. Other structures are distinct extensions to the basic machine recognized data objects. Arrays and streams have been suggested because they fit neatly into the various data flowgraph models, with or without coloring.[20, 21, 22, 23] In the labeled scheme, elements of an array are held on different colored tokens that travel down common flowgraph arcs. Each element's color indicates its position in the array. Streams are similar, but their lengths are not bounded in the same way as array lengths.

Although these constructs seem successful in small simulation studies, there is too little experience with them to say whether they will remain the major data structures. However, the popularity of arrays in conventional programming languages implies that they are not likely to be abandoned without very strong reasons.

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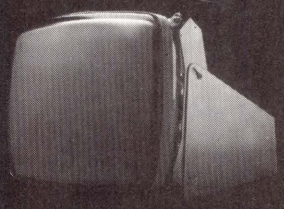

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BUS ARBITER STREAMLINES MULTIPROCESSOR DESIGN

Arbiter coordinates 8- and 16-bit microprocessors' access to a shared, multimaster bus and offers flexible operating modes to accommodate different system configurations

James Nadir and Bruce McCormick

Intel Corporation
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Performance improvements and cost reductions afforded by large scale integration technology have spurred the design of multiple microprocessor systems that offer improved realtime response, reliability, and modularity. In multiprocessing, more than one microprocessor shares common system resources—such as memory and input/output devices—over a common multiple processor bus (Fig 1). This concept allows system designers to partition overall system functions into separate tasks that each of several processors can handle individually and in parallel, increasing system performance and throughput.

The 8086 family of 16-bit microprocessors and support components permits the designer to select only those components that are necessary to meet cost and performance requirements. One method for achieving this building block approach to system design uses a compatibility mechanism of the 8086 and the MULTIBUS™ multiprocessing bus standard. However, multiprocessing systems require devices that can coordinate the use of global or shared resources. The 8289 bus arbiter (Fig 2) provides this multiprocessing coordination in conjunction with MULTIBUS architecture.

MULTIBUS Approach

MULTIBUS architecture in a multiprocessor system allows each processor to work asynchronously. Therefore, a fast microprocessor operates at its own speed regardless of the speed of the slowest microprocessor. This technique tolerates duty cycle and phase shift variations, and offers hardware modularity. When new system functions are desired, additional microprocessors can be integrated without impacting existing task partitioning.

The MULTIBUS approach implements this asynchronous processing structure by synchronizing all microprocessor bus requests to a high frequency reference system bus clock that can operate at up to 10 MHz. Synchronized requests are then resolved by a priority encoder. As a result, the number of resolving circuits common to all microprocessors is minimized. The synchronizing or arbitrating function is integrated into the bus arbiter, allowing it to resolve arbitration problems of a shared system bus in a multimaster, multiprocessing environment.

Critical code sections in memory can be identified by a flag or word, called a semaphore, which is set by one of the microprocessors. The bus arbiter prevents use of the shared memory bus while a microprocessor is setting the semaphore, creating a "locked test and set" condition. In addition, the bus arbiter provides a flexible, definable set of bus modes so that a designer can configure a system to meet a variety of applications.

The bus arbiter operates in conjunction with a bus controller that generates memory and input/output (I/O) signals to interface the multiprocessors to a multimaster system bus (Fig 3). Unaware of arbiter presence, a microprocessor sends out control signals as though it has exclusive use of the system bus. If a microprocessor does not have use of the multimaster system bus, the bus arbiter prevents the bus controller, data transceivers, and address latches from accessing the system bus, ie, all bus driver outputs are forced into the high impedance state. Since system commands are not issued, no acknowledgement (transfer acknowledgement) is returned, causing the microprocessor to extend its transfer cycle by entering into wait states. The microprocessor extends its transfer cycle until the bus arbiter acquires access to the multimaster system bus, then,

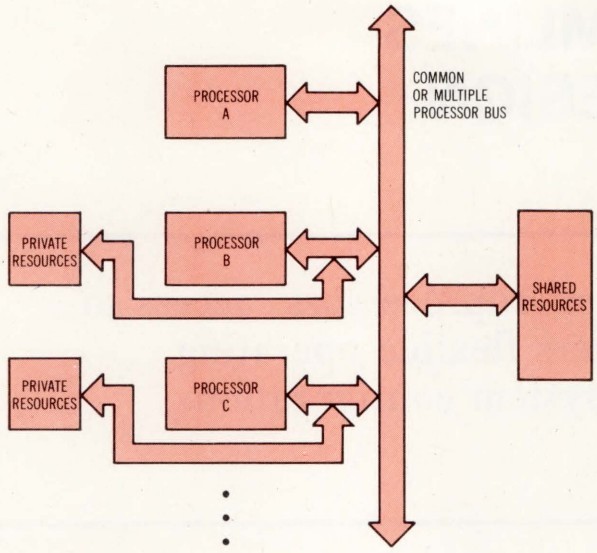


Fig 1 Multiprocessing system using common bus. Several processors sharing expensive resources, such as disc drives or line printers, is efficient and cost-effective. Bus contention problems inevitably arise on common system bus unless steps are taken to arbitrate usage

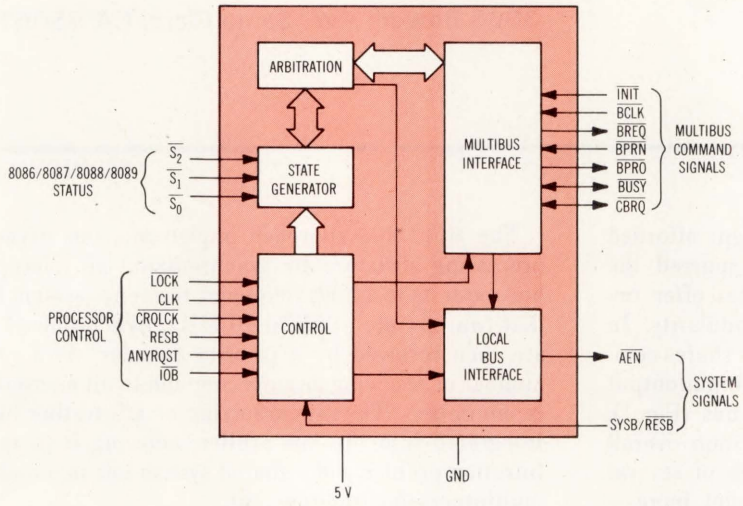


Fig 2 Bus arbiter block diagram. 20-pin, 5-V-only, bipolar arbiter for use with medium to large multimaster, multiprocessing systems provides system bus arbitration for systems with multiple bus masters, as well as bipolar buffering and drive capability

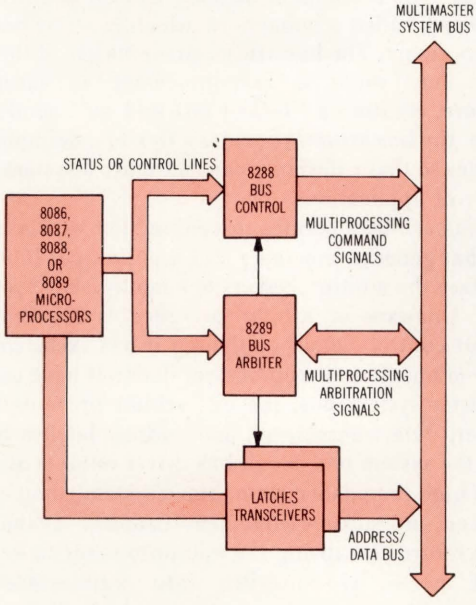


Fig 3 Bus arbitration chip aids multiprocessor design. 8-bit 8088 and 16-bit 8086, 8089 microprocessors are designed for use in multiple microprocessor systems. To prevent contention for common system bus, arbiter provides several methods for arbitrating bus use

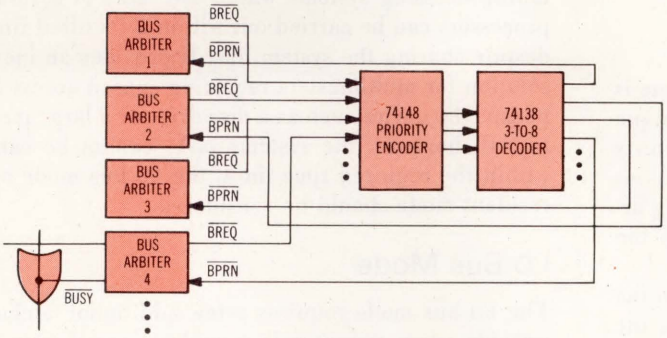


Fig 4 Parallel resolving technique synchronizes asynchronous requests. Requests for common bus use (BREQ) are sent by each microprocessor's bus arbiter to encoder-decoder circuit, which responds to arbiter with highest priority by returning bus priority in signal (BPRN). Bus arbiter then provides its microprocessor access to system bus

the arbiter allows the bus controller, data transceivers, and address latches to access the system bus.

After the bus controller issues its control line signal and a data transfer has taken place, a transfer acknowledge signal is returned to the microprocessor. Then the microprocessor completes its transfer cycle. Thus, the arbiter serves to coordinate microprocessor, or bus master, access to the multimaster system bus.

Priority Resolving Techniques

Since there can be many bus masters on a multimaster system bus, a technique for resolving simultaneous requests among bus masters must be provided. The bus arbiter offers several resolving techniques; all are based on the concept that at a given time, one bus master has higher priority. These techniques include parallel priority resolving, serial priority resolving, and rotating priority resolving.

Parallel Priority Resolving Technique

In the parallel priority resolving technique, a separate bus request (BREQ) line is connected to each of several arbiters on the multimaster system bus (Fig 4). Each BREQ line enters a priority encoder which generates, as output, the binary address of the highest priority BREQ line asserted at its inputs. The output binary address, after being decoded, selects the corresponding bus priority in (BPRN) line to be returned to the highest priority requesting arbiter. The arbiter receiving priority (BPRN true) then allows its associated bus master access to the multimaster system bus as soon as the bus becomes available.

Even when one bus arbiter gains priority over another arbiter, it cannot immediately seize the bus. It must wait until the present bus occupant completes its transfer cycle, ensuring transfer integrity. Upon completing its transfer cycle, the bus occupant determines that it no longer has priority and surrenders the bus, releasing BUSY.

Serial Priority Resolving Technique

The serial priority resolving technique eliminates the need for a priority encoder/decoder arrangement by daisy chaining the bus arbiters. This setup is accomplished by connecting the higher priority bus arbiter bus priority out (BPRO) line to the BPRN line of the next lower priority arbiter (Fig 5). The highest priority bus arbiter has its BPRN line grounded, signifying to the other arbiters that is always has highest priority when requesting the bus. Priority is passed in series

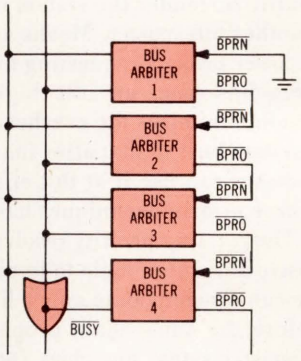


Fig 5 Serial priority resolving technique. Simpler daisy chain scheme provides effective bus arbitration for system designs that do not have more than three arbiters and microprocessors vying for bus access. Connected in order of priority from top to bottom, first arbiter has priority at all times because of grounded state of its BPRN line. When not using bus, arbiter 1 sends low state signal to next higher priority arbiter via its BPRO line

from a higher priority arbiter on the chain, when it does not need the system bus, to any requesting lower priority arbiter.

Rotating Priority Resolving Technique

Arrangement of the rotating priority resolving technique is similar to that of the parallel priority resolving technique except that priority is dynamically reassigned. The priority encoder is replaced by a more complex circuit that rotates priority in standard time increments among requesting arbiters, guaranteeing each arbiter equal access to the multimaster system bus.

In all three techniques, lower priority masters obtain the bus when a higher priority processor is not accessing the system bus. A strapping connection is available, however, that allows the multimaster system bus, completing its transfer cycle, to be surrendered immediately to any bus master requesting the bus, other than itself, regardless of priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus as long as its associated processor has not entered the halt state. The bus arbiter does not voluntarily surrender the system bus and has to be forced off by another bus master. Means and conditions do exist whereby a lower priority requesting bus master can acquire the system bus from an idle higher priority bus master. This action minimizes the overhead required to obtain use of the system bus; so that after the bus has been acquired, the processor can use it at full efficiency.

Each of the three priority techniques has advantages and disadvantages. The rotating priority resolving technique requires an extensive amount of logic to implement, while the serial technique can accommodate only a limited number of bus arbiters before the daisy chain propagation delay exceeds the multimaster sytem bus clock ($\overline{\text{BCLK}}$) period. The parallel priority resolving technique is generally the best compromise. It allows many arbiters to access the bus without requiring excessive logic for implementation.

System Bus Modes

The bus arbiter provides several definable system bus mode configurations for microprocessors. In the I/O peripheral bus mode, the arbiter permits a microprocessor access to both a private I/O peripheral bus and a multimaster system bus. In the resident bus mode, the arbiter allows a microprocessor to communicate over both a resident bus and a multimaster system bus. A resident bus is defined as a private bus that has both memory and I/O devices, as opposed to an I/O peripheral bus that has only I/O devices. Other configurations provide communication across several multimaster buses.

A particular configuration determines the technique by which the arbiter requests and surrenders the system bus. If the arbiter is configured to operate with a non-I/O microprocessor (normal processor), which has access to both a multimaster system bus and a resident bus, then the arbiter requests the use of the multimaster system bus only for system bus accesses. While the processor is accessing the resident bus, the arbiter permits a lower priority bus master to seize the system bus. An I/O processor configuration with both I/O peripheral and system buses behaves similarly.

Single-Bus Mode

The single-bus mode is the simplest mode. It is sufficient for multiprocessing systems where the tasks of several microprocessors can be carried out within a required time frame despite sharing the system bus. It provides an inexpensive solution for multimasters requiring shared access to an expensive I/O device such as a disc drive or a large memory array. If, however, the systems tasks cannot be carried out within the required time limit, the I/O bus mode or system resident mode should be considered.

I/O Bus Mode

The I/O bus mode requires a few additional latches and is suitable when throughput considerations dictate that the overall bus structure be separated into an I/O bus and a memory or system bus. This mode is commonly used with the 8089 I/O microprocessor, in its remote configuration, to separate I/O space from memory space. With this processor, all instructions operate on either system or I/O address space, treating all peripherals as memory mapped devices. Memory for program code or buffering can be placed on either the system bus or the local I/O bus. The 8086 and 8088 microprocessors are constrained to exclusive use of I/O instructions when referencing I/O space. If this constraint is a limitation and it becomes desirable to allocate some of the processor functions to private resources, then the resident bus mode should be considered.

Resident Bus Mode

The resident bus mode allows maximum flexibility for a microprocessor, yielding access both to local resources and to system resources. The central processing unit (CPU) can interact with local resources at full speed without contention on the system bus. System bus accesses can be minimized to those of swapping in and out from mass storage or the use of expensive resources that should not be duplicated on the processor local bus. By using a programmable read only memory (P/ROM) for memory mapping, memory space is altered easily.

Bus Interfaces

To fully describe the bus arbiter functions, each of the three operating modes is examined. Typical examples describe a single-bus configuration, an I/O bus configuration, and a resident bus configuration.

Single-Bus Interface

Fig 6 shows a typical multiprocessing system configuration with the bus arbiter in the single-bus mode. In this system design, each of the three bus masters is assigned a priority ranging from priority 1, the highest, to priority 3, the lowest. Priority is established using the parallel priority scheme; disregard, for now, the dashed signal interconnects.

Each bus arbiter monitors its associated processor and issues a $\overline{\text{BREQ}}$ whenever this processor requests bus access. A common clocking signal, $\overline{\text{BCLK}}$, runs to each arbiter in the system.

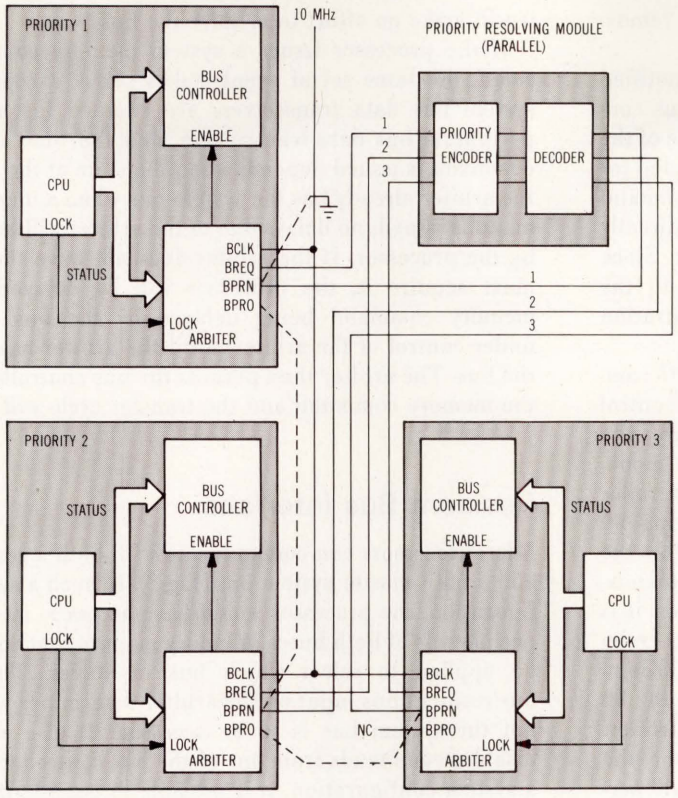


Fig 6 Parallel and serial resolving techniques. Each microprocessor circuit module and its bus arbiter (color) are shown connected in a parallel mode (solid lines) or serial mode (dashed lines) configuration

If the serial priority resolving mode is used, the system is connected by the dashed signal lines from the $\overline{\text{BPRO}}$ of one arbiter to $\overline{\text{BPRN}}$ of the next lower priority arbiter (Fig 6). The $\overline{\text{BREQ}}$ lines are disconnected, and the priority encoder/decoder arrangement is removed. This serial priority mode is more straightforward than the parallel priority mode except in that the daisy chain propagation delay from the highest priority bus arbiter $\overline{\text{BPRO}}$ line to the lowest priority bus arbiter $\overline{\text{BPRN}}$ line, including the setup time requirement ($\overline{\text{BPRN}}$ to $\overline{\text{BCLK}}$), cannot exceed the $\overline{\text{BCLK}}$ period. This period is nominally 100 ns, but it can be stretched by slowing down the maximum clock frequency of 10 MHz. The penalty is longer waits for bus arbitration.

This configuration dictates that the number of arbiters that can be daisy chained together for a given $\overline{\text{BCLK}}$ frequency be limited. Of course, the lower the $\overline{\text{BCLK}}$ frequency, the more arbiters can be daisy chained together. Three arbiters can be daisy chained when using the maximum $\overline{\text{BCLK}}$ frequency of 10 MHz.

How quickly bus arbiter 1 can acquire the bus depends upon the configuration and the strapping connections of the arbiter from which it is trying to acquire the bus. For example, if the $\overline{\text{LOCK}}$ input to arbiter 2 is active (low) at the time, then arbiter 1—even though it is of higher priority—cannot acquire the bus until after $\overline{\text{LOCK}}$ is released (goes high). Another factor to be considered is the microprocessor state, in its transfer cycle, at the time the arbiter is instructed to yield the bus. If the transfer cycle has just started, it will take longer for the bus to be released than if the cycle is just ending.

Higher priority bus masters force a lower priority bus master arbiter to surrender the bus by the reassignment of priority. If generating a $\overline{\text{BREQ}}$, a higher priority bus master would cause the present bus occupant to lose its $\overline{\text{BPRN}}$. Lower priority bus masters acquire the bus by pulling down the open collector signal, common bus request ($\overline{\text{CBRQ}}$). The present bus occupant recognizes $\overline{\text{CBRQ}}$ whenever it is not accessing the system bus; when it is activated, the bus is released. Priority is established to the next highest requesting aribter, and the requesting arbiter then acquires the bus.

I/O Bus Interface

In the I/O bus mode, the processor communicates with and controls a host of peripherals over the peripheral bus. An 8089 I/O microprocessor can use either memory or peripherals on its local bus. When the I/O processor needs to communicate with system memory, it is done over the system memory bus. Fig 7 shows a typical I/O processor in its REMOTE mode. Resident memory exists on the peripheral bus to provide programmed I/O routines and buffer storage. Resident memory is treated as an I/O peripheral. When a peripheral device needs servicing, the I/O processor accesses resident memory for the proper I/O driver routine and services the device, transmitting or storing peripheral data in a buffer storage area of resident memory (or sending it directly to system memory if necessary). The resident memory buffer storage area can then be emptied or replenished from system memory via the system bus. Using the I/O bus

interface allows an I/O processor the capability of executing from local memory (on the peripheral bus) concurrently with a host processor, enhancing system performance and removing the burden of I/O from the host processor.

Like the arbiter, the bus controller also must be notified of the operating mode. In the I/O bus mode, the bus controller issues I/O commands independently of the state of the arbiter. It is assumed that all I/O commands are intended for the I/O bus and, hence, that there is a separate I/O command bus from the controller. All I/O commands are sent directly to the I/O bus and are not influenced by the arbiter. Since memory commands are assumed to be directed to the system bus, they must still be influenced by the arbitration mechanism provided by the arbiter.

For example, suppose the processor issues an I/O command. The bus controller generates the necessary control signal to latch the I/O address and to configure the transceivers in the correct direction. In the I/O bus mode, the peripheral data enable (PDEN) pin of the controller serves to enable the I/O bus data transceivers during I/O commands. Similarly, data enable (DEN) serves to enable the system bus data transceivers during memory commands. Signals PDEN and DEN are mutually exclusive, so that it is not possible for both sets of transceivers to be on, thereby avoiding contention between the two sets. Since the I/O commands are generated independently of the arbiter in the I/O bus mode, the I/O bus has no delay effects due to the arbiter. During the time in which the processor is accessing the local I/O bus, the arbiter—if it already has the bus—will permit it to be surrendered to either a higher or lower priority request (via $\overline{\text{CBRQ}}$) independently of where the processor is in its transfer cycle (for example, independent of the machine state). If the arbiter does not already have the bus, it will make no effort to acquire the bus.

If the processor issues a system memory command instead, the same set of events takes place, except that the system bus data transceivers are enabled instead of the peripheral bus data transceivers, and the time at which a command is issued depends upon the state of the arbiter. If the arbiter already has the system bus when a memory command is issued, no delays due to the arbiter will be detected by the processor. If the arbiter does not have the bus and must acquire it, the processor will be delayed (via the memory command being delayed by the bus controller under control of the arbiter) until the arbiter has acquired the bus. The arbiter then permits the bus controller to issue the memory command and the transfer cycle will continue.

Resident Bus Interface

Microprocessors can communicate with both a resident bus and a multimaster system bus (Fig 8). In such a system configuration, the processor would have access to memory and peripherals of both buses. Memory mapping techniques can be applied to select which bus to access. The system bus/resident bus input on the arbiter determines whether or not the system bus is to be accessed. It also enables or disables commands from one of the bus controllers. In such a system configuration, it is possible to issue both memory and I/O commands to either bus and, as a result, two bus controllers are needed, one for each bus.

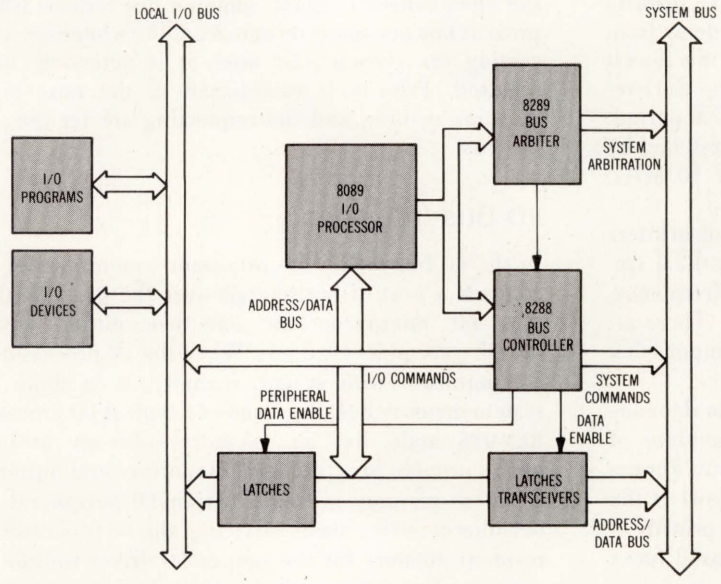


Fig 7 I/O bus interface. By halving bus structure into local I/O bus and common system bus, 8089 I/O processor has exclusive access to its peripherals but can also communicate with system bus. Commands to local bus are not under control of bus arbiter and will never be delayed by it. Requests for system bus must proceed through arbitration and can be delayed in event that arbiter does not have access to bus at time of request. Only one bus controller is needed to implement this technique

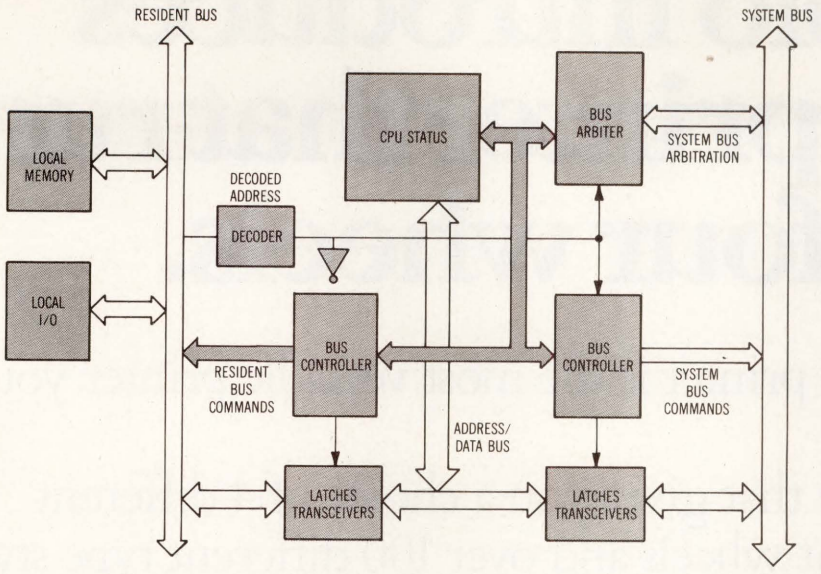


Fig 8 Resident bus scheme for additional performance. In resident bus mode, single 8086 or 8088 has access to both common system bus and local resident bus. Processor can be handling resident bus-oriented operation while other system processors use system bus. Many tasks can be carried out simultaneously, increasing overall performance. As in I/O bus mode, only one arbiter is required but two bus controllers must be used

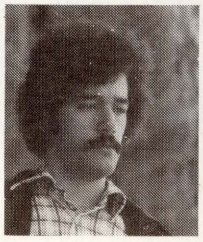
In Fig 8, memory mapping techniques are applied on the resident bus side of the system rather than on the multiprocessor or system bus. Both sets of address latches (resident bus and system bus) are latched with the same address in this case, by their respective bus controllers. The system bus address latches, however, may or may not be enabled, depending upon when the arbiter has bus access. The resident bus address latches are always enabled; hence, the memory mapping technique is applied to the resident bus.

A simpler system with an 8086 or 8088 microprocessor can exist if it is desirable to have only P/ROM, read only memory, or read only peripheral interfaces on the resident bus. These microprocessors additionally generate a read signal in conjunction with the bus controller signals. By using this read signal and memory mapping, the microprocessors can operate from local program store without having the contention of using the system bus. Using this technique eliminates the need for a second bus controller.

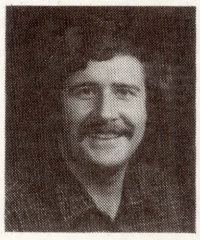
In actual operation, both bus controllers respond to the processor status line and both simultaneously issue an address latch enable (ALE) strobe to their respective address latches. Both bus controllers issue command and control signals unless inhibited. The purpose of the memory mapping circuits is to inhibit one of the bus controllers before contention or erroneous commands can occur.

Summary

A bus arbiter brings a powerful dimension to system design architectures by allowing 8-bit and/or 16-bit microprocessors to execute easily in a multimaster, multiprocessing environment. With the flexible modes of the arbiter, a designer can define one of several bus architectures to meet cost and performance needs. Modularity, improved system reliability, and increased performance are some of the benefits that a multiprocessing system provides.



James Nadir is a project engineer at Intel and has designed some of the 8086 microprocessor family support circuitry and their interface to the MULTIBUS™ system bus. He graduated from Rutgers University with a BSEE.



Bruce McCormick is one of the product managers for the 8086 family of microcomputers. His experience includes applications and product engineering work as well as product marketing at Intel Corporation. He holds BSEE and MSEE degrees from Purdue University, and an MBA from Santa Clara University.

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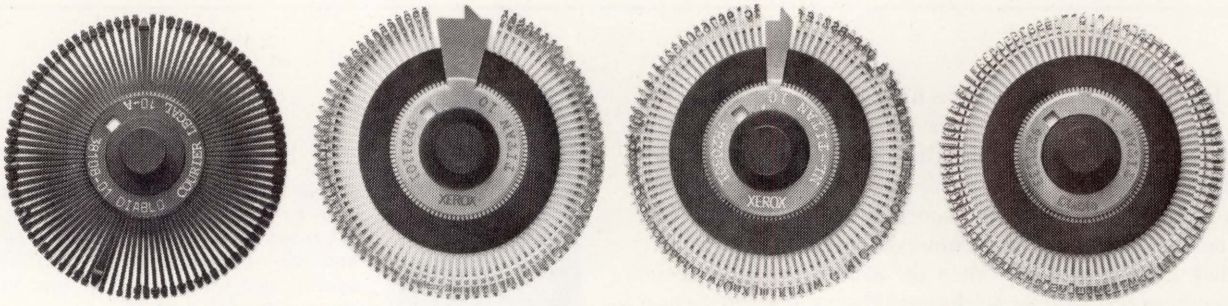

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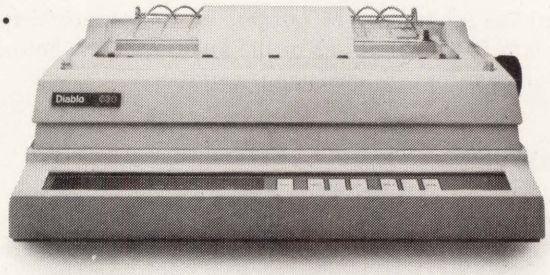

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THE VANISHING DISC INTERFACE

Evolving disc technologies present the system designer with new options and tradeoffs as intelligent drives obsolete the familiar controller and formatter in many applications

Lynn J. Moore

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The rapid evolution of disc technologies and devices, ranging from mini-floppies to super capacity disc drives, has masked a parallel development which, in its own way, promises an even greater impact on the flexibility, architecture, and cost performance of future disc storage systems. Recent introduction of a new generation of intelligent disc drives is symbolic of this change. These devices offer unprecedented capabilities, but their most important impact will be subtractive rather than additive. In effect, they signal the final disappearance of a familiar but costly element in nearly every computer system block diagram: the disc controller and formatter.

The net effect is to give original equipment manufacturer (OEM) system designers a new set of options and economic tradeoffs. Every innovation has its costs, and the vanishing controller interface may be an unacceptable alternative in certain applications. However, in the majority of cases, elimination of the disc controller as a separate hardware element will produce immediate savings in terms of space, cost, and complexity. Subtler benefits will also accrue. The particular way in which the new disc intelligence is implemented can reduce system design time from months to days. A simplified, standardized disc interface allows OEM system designers to respond rapidly to changes in market requirements and take quick advantage of developments in disc storage technology. They can also offer their customers low cost, easily implemented expansion options, and reduce the risk that installed systems will become obsolete as other storage techniques become available.

Dispersed Intelligence

Introduction of the new, intelligent drives will also accelerate the trend toward future dispersed computer systems where memory will be the one essential element at every site. Rotating discs, the preeminent data storage device for two decades, can therefore serve as natural nuclei for one (or for most) of the new intelligence centers. This raises the question, "Why has it taken manufacturers of disc drives so much longer to add a measure of intelligence to their products than it has taken manufacturers of less sophisticated devices, such as terminals and printers?" Part of the answer lies in the complexity of the disc storage technique. To execute a seek command, for example, the disc control system must identify device, cylinder, surface, and rotational position. Seek is only one of more than 30 identifiable functions that must be performed in the process of transferring data between the central processing unit (CPU) and the storage device.

More importantly, the rotating disc has always lived a double life. Disc drives are nominally a part of the host computer input/output (I/O) structure. A removable disc cartridge can be compared to a tray of punched cards. Unlike most other peripherals, however, the principal function of most disc systems has been to serve as extensions of computer main memory, where they have a direct impact on the speed, efficiency, and throughput of the entire data processing system. Because the drives become integral parts of the system architecture, computer designers have jealously

guarded the right to determine such variables as data format, sector size, error detection techniques, and I/O protocol. System, not disc, considerations dictate whether data transfers are to occur on the standard I/O bus, on a direct link to memory, or on both.

Small wonder, then, that manufacturers of disc drives, the most sophisticated of peripherals, chose to keep their drives as dumb as possible, leaving it up to the computer manufacturer or system designer to resolve the interfacing problems for a particular host computer, operating system, and type of disc. It quickly became clear, however, that the intelligence required to implement complex disc storage functions represented an excessive overhead burden. As a result, disc control functions moved progressively out of the CPU and into a separate box, the controller and formatter.

This auxiliary unit needed expensive, new components, such as a buffer memory that would allow both disc and CPU to transfer data at their optimum rates. To spread these costs, most controllers were designed to support a number of disc drives on the assumption that the computer could, in any case, communicate with only one disc at a time. It was a reasonable solution because the data capacity of a single-disc spindle was still relatively limited, and multiple-spindle systems were commonplace.

Microprocessor Control

Cost, complexity, and nature of the disc controller made it a natural candidate for microprocessor control as soon as this technology became available. Large scale integration (LSI) microprocessor and memory chips reduced the dimensions and power requirements of the disc control circuitry. The controller enclosure shrank in size, and the stage was set for its initial disappearance—but in the wrong direction. Controller formatters have had, by definition, two interfaces. There is a data and control interface between controller and disc, largely dictated by the nature of the disc drive itself. There is also a data and control link between controller and CPU, largely dictated by the nature and capabilities of the controller (Fig 1). This has required, in turn, a specially designed host adapter plugged into the CPU I/O bus.

All of these factors added up to a snarl of problems for the OEM designer who was anxious to incorporate disc devices and capacities beyond those anticipated by his particular small computer supplier. Odds are high that, if he wanted to accommodate a "foreign" disc, the designer had to deal with an equally foreign controller and formatter, and face the task of designing his own host adapter. Odds are also high that the designer had to violate his sacrosanct operating system with an alien I/O driver, and was forced to add new utility programs and diagnostics that were wasteful of memory. The separate controller box added to the space requirements of the OEM system, and the designer had to suffer the expense of another power supply, as well as the field service uncertainties of two separate connector interfaces.

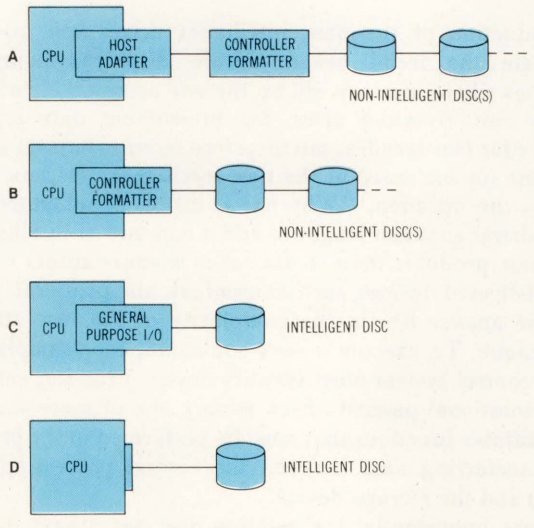


Fig 1 Vanishing disc interface. Diagram A shows conventional, standalone controller and formatter interfaced to CPU through host adapter. B eliminates one interface but returns intelligence to CPU environment. C shows intelligent drive interfaced through general purpose I/O board. D reduces intelligent drive interface to LSI chips on CPU board itself

A Partial Solution

Introduction of microprocessors eased some of these burdens. A more general purpose controller could be designed and reprogrammed, within limits, through the use of firmware or floppy-resident instructions loaded into random access memory. LSI chips also allowed the controller to be packaged on a single board, hidden in the CPU enclosure, and plugged directly into the I/O bus structure. This resulted in the embedded disc controller, a major improvement over the standalone box. One of the mechanical interfaces was all but removed, and overall space was saved. Elimination of the separate power supply helped cut costs in half.

CPU enclosure space is also at a premium. Physically, at least, the intelligence reflected by the controller and formatter moved back into the CPU environment. There are other faults to this approach. The restricted space generally reduced controller capabilities.

One minor but typical problem, for example, was that only two or four spindles could be supported. This is not as serious a limitation as before, since spindle capacities have

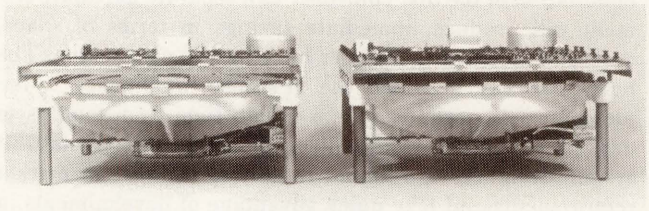


Fig 2 Intelligent (right) and nonintelligent drives. Form and fit factors are identical. Rigid, 14-in disc has up to 40M-byte storage capacity; drive uses Winchester technology to ensure maximum data integrity

increased sharply, and most users would prefer the cost and throughput advantages offered by a smaller number of higher capacity drives.

What is of much greater concern is that nothing has been done to resolve the special nature of the controller itself. Within the limits of microprocessor reprogramming, the controller must be uniquely designed for the host CPU and the discs to be controlled. There is still a probable requirement for specialized utilities and diagnostics, plus a new I/O driver. Moreover, any change in the external data storage system is likely to require a completely new controller card, I/O driver, and supporting software.

Floppies Pave the Way

The opportunity to resolve nearly all of these problems—and to put the disc intelligence where it belongs, within the disc drive itself—came from an unexpected source: the floppy disc. Like their larger counterparts, floppies perform a dual function, serving as both I/O peripherals and as extensions of main memory. However, the priorities are usually reversed; the medium is always removable, and the limited capacity and speed of floppy discs restrict their use as extensions of main memory except in very small systems or for non-demanding tasks. As a result, computer designers have been much less concerned with the floppy disc interface, storage format, and I/O protocol. We can also assume that when floppies were first introduced, system designers began to realize the price they were paying for their earlier insistence on dictating the parameters of larger disc subsystems. In either case, floppy disc manufacturers have been able to standardize the floppy interface from the start, and small computer suppliers tended, for the most part, to adapt their side of the interface to these standards.

Taking the route of least resistance, physical interface and control signals have closely followed the pattern set for other I/O peripherals, such as line printers and high speed paper tape readers and punches. In fact, a majority of small computer manufacturers now offer general purpose or utility I/O boards that can adapt easily to all of these devices. A similar standardization occurred in terms of the I/O drivers supplied with operating systems. The next step was the inevitable introduction of LSI chips that can be mounted directly on the CPU board, eliminating the need for even a general purpose I/O board.

An Expanding Requirement

Floppy disc maufacturers were quick to capitalize on these developments. Because highly specialized controller formatters were no longer required, general purpose circuitry, performing the same functions, could be incorporated directly into the drive itself. Floppy discs have the distinction, therefore, of becoming the first rotating disc devices to earn the "intelligent" accolade. However, data storage systems tend to follow a Parkinson's Law of their own: the requirements for data storage inevitably fill all of the available space. More capacity is needed, and usually the most cost-effective method is to move to higher capacity drives, rather than to duplicate existing devices.

It is no coincidence, then, that the first of the rigid disc drives to become intelligent were units designed for OEM applications that outgrew the upper limits of floppy disc devices or that required the faster transfer rates and increased throughput obtainable with a rigid disc design. There was an immediate need for a disc device that would offer a direct expansion capability for an intelligent floppy. Ideally, the new, intelligent, rigid disc drives should also be capable of direct connection to the CPU, using the same general purpose I/O board or the same set of LSI chips.

The Intelligent Marksman is an example of this new generation of drives, chosen primarily because it is also available in a non-intelligent model, allowing direct comparisons to be made. The unit is based on Winchester technology, has non-removable media, with a present upper limit capacity of 40M bytes. There is no reason why the same interface cannot be applied to higher capacity models of this device and, eventually, to removable media cartridge and storage module drives with capacities of up to 600M bytes.

With such data storage devices on the horizon, OEM system designers will be able to plan on complete upward flexibility in the size and nature of their data storage subsystems. Moreover, they will know that at each stage in this progression, they will enjoy the cost and space savings that result from the elimination of the separate, standalone controller and formatter. They can also plan on future upgrades of existing systems with minimum impact on the physical form and software structure.

Self-Contained Intelligence

The effect on form and fit when intelligence is added to a disc drive is shown in Figs 2 and 3. In the case of the Intelligent Marksman, there are no visible changes; all the new intelligence is within the drive envelope. Yet there is a dramatic alteration in the capabilities of the device. Table 1 lists typical functions that must be performed in the process of transferring data between a disc drive and its CPU. Nearly all of these have normally been performed by a standalone or embedded controller and formatter. Now, with a few exceptions, they are accomplished by the drive itself.

As presently implemented, the intelligent drive performs all disc control functions except for auto seek, offline offloading, search, and copy. Only the first two of these tasks have been performed, in a restricted number of cases, by the controller. Search and copy are normally supervised by the operating system in the CPU, but could conceivably be

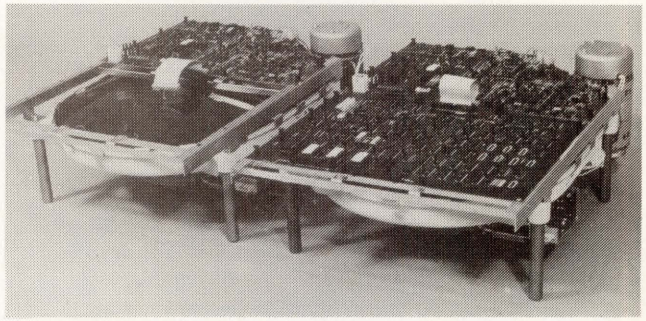


Fig 3 Expanded circuitry of intelligent disc. Nearly all capabilities of standalone or embedded controller and formatter are provided at significant saving in cost, space, and development time

TABLE 1

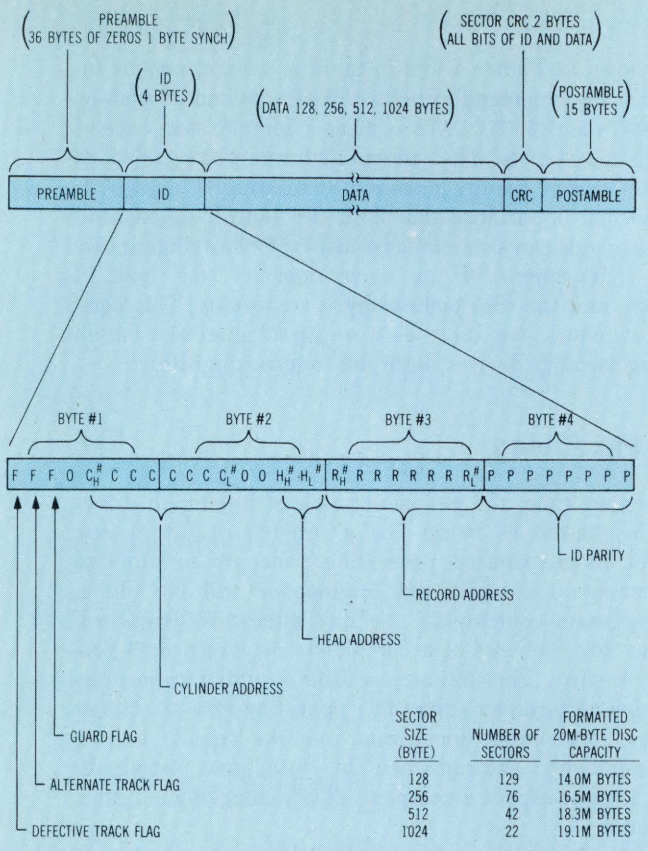
Disc Data Transfer and Control Functions

Disc Control	
	Track to track positioning (seek)
	Auto seek
	Read
	Write
	Write protection
	Status communication
	Search
	Copy
	Offline offload
Addressing	
	Physical/logical device addressing
	Single/multiple drive addressing
	Logical/physical data addressing
	Extended addressing
	Alternate tracks and sectors
	Interleaving of sectors
Formatting	
	Formatting
	Separate/embedded ID fields
	User flags
Data Transfer	
	Buffering
	Data rate adjustment
	Multiple sector transfers
	Byte/word translations
Data Validity	
	Error detection
	Error correction
	Defective tracks
	Defective sectors
	Defect skipping
	Diagnostics—internal
	Diagnostics—external
System Generation	
	Sector sizes
	Type of drive
	Dual access (drive)
	Dual port (controller)
Startup and Power	
	Power sequencing
	Power fail/recovery
	System reset
	Selective reset (abort)

TABLE 2

Nonintelligent Disc Interface

Command/Status	High-active bidirectional 8-bit wide bus used to transfer commands and status
Control Request	High-active line from controller, used in conjunction with Control Acknowledge line to form a handshake between controller and drive
Control Acknowledge	High-active line from drive to controller
Control Ready	High-active line from drive to controller indicating drive is in output mode and is waiting for command
Control Status	High-active line from drive to controller indicating that drive has placed byte of status information on command/status bus
Drive Ready	Positive-true line from drive to controller to indicate that drive is up to speed and dc power is safe
Reset	Low-active line from controller that provides drive with an unconditional reset
Index	High-active line from drive used to indicate physical beginning of track data
Sector	High-active line from drive used to indicate physical beginning of data record within a track
Write Unsafe	Positive-true line from drive to controller to indicate unsafe write process was attempted
Write Data	Positive-true line from controller to drive used to transmit serial write data to drive
Write Clock	Positive-true line from drive to interface used to clock write data from controller
Write Gate	Negative-true line from controller to drive used to write data on selected head
Read Data	Positive-true line from drive to interface used to transmit serial data to controller
Read Clock	Positive-true line from drive to controller used to clock read data from drive
Read Gate	Positive-true line from controller to drive to start lockup of phase lock loop in data separator
MPU Clock	1-MHz clock provided for use by controller in functions that do not require synchronization to disc speed



SECTOR SIZE (BYTE)	NUMBER OF SECTORS	FORMATTED 20M-BYTE DISC CAPACITY
128	129	14.0M BYTES
256	76	16.5M BYTES
512	42	18.3M BYTES
1024	22	19.1M BYTES

Fig 4 Sector size is switch selectable. Large sectors increase effective disc capacity and potential throughput, but may waste space in CPU main memory. 15-byte postamble facilitates transfer of successive sectors by allowing time for new read or write commands

added to the repertoire of future intelligent devices. Switch selectable interleaving of sectors (up to a level of seven) can support alternate track and sector addressing. Other specialized addressing functions, which are now accomplished by the I/O driver, host adapter, or controller, will eventually be added to the intelligent disc capabilities.

Data storage format is shown in Fig 4. The 4-byte identification field is embedded in the data blocks. No provision is made for user flags. All data transfer functions are accomplished by the intelligent drive. Except for error correction, it also performs all of the functions normally associated with validating the data and making certain that the drive itself is functioning correctly.

A dual-inline package switch within the intelligent drive establishes sector and buffer sizes. Any one of the four different sector sizes shown in Fig 4 can be chosen. The drive also performs all of the startup and power functions associated with initialization of the drive subsystem.

Parallel Data Interface

From the OEM system designer's point of view, the relatively few functions not performed by the intelligent disc are a small price to pay for the ease with which it can be interfaced into a system. Tables 2 and 3 compare the new parallel data interface (PDI) with the data and control lines required for the nonintelligent disc. The number of control lines has been reduced from 14 to 7, but these figures tell only half the story. All of the time-sensitive control signals have been eliminated. Sequence and timing functions are all performed by the intelligent disc circuitry.

TABLE 3

Parallel Data Interface (PDI)

Data/Command/Status	Two high-active 8-bit wide buses or one 8-bit wide bidirectional bus to transfer data, commands, and status between drive and CPU
Input Ready	High-active line from drive to CPU indicating that CPU is ready to accept commands or data
Control Request	High-active line from CPU used in conjunction with Control Acknowledge line to form handshake between CPU and drive
Control Acknowledge	High-active line from drive to CPU
Control Ready	High-active line from drive to CPU indicating drive is in input mode and waiting for command
Control Status	High-active line from drive to CPU indicating that data being sent to CPU are status information
Reset	Low-active line from CPU to provide drive with an unconditional reset
Abort	High-active line from CPU causing drive to abort current command

TABLE 4

Nonintelligent Disc Commands

SEQUENCE	Directs disc drive motor to power up or power down
REZERO	Causes heads to be repositioned to cylinder zero, head zero
STATUS REQUEST	Places current status of drive on command/status bus
SEEK	Positions heads over specified cylinder and selects addressed head
HEAD ADVANCE	Facilitates sequential sector accesses across head boundaries by advancing head address more rapidly than can be done with SEEK command
SET SECTOR	Overrides sector-size switch setting and defines number of sector pulses per revolution

TABLE 5

Intelligent Disc Commands

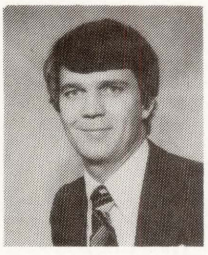
SEQUENCE	Directs disc drive motor to power up or power down
REZERO	Causes heads to be repositioned to cylinder zero, head zero, and verified
STATUS REQUEST	Commands drive to return desired status byte as normal ending status
SEEK	Positions heads over specified cylinder and selects addressed head
WRITE BUFFER	Places data from CPU into buffer
WRITE DATA	Commands drive to write contents of buffer on cylinder and head specified by last SEEK command
READ DATA	Reads data from specified sector into buffer
READ BUFFER	Transfers data from buffer to CPU
FORMAT	Formats disc (Fig 4)
BOOT	Positions heads over cylinder zero, head zero. Record zero is then read into buffer and transferred to CPU

As shown in Tables 4 and 5, there is a simultaneous increase in the command structure. New commands, such as READ DATA and WRITE DATA, replace a complex sequence of control line signals. The command formats are coded so that they can be readily managed by existing I/O drivers. It is of special importance that both the control signals and the commands can accommodate any type of intelligent disc drive, independent of the drive capacity, the type of medium, and the disc technology it represents. This command structure can serve as a universal interface for all rotating memory devices, both now and in the future.

Looking Ahead

At the same time, the new generation of intelligent drives must be viewed as being just a preview of future disc systems. As distributed processing concepts continue to gain momentum, additional intelligence will be added, allowing us to contemplate the day when disc drives will serve as key elements of a completely dispersed data processing facility. The first step will be to add specific functions now performed by the CPU's operating system, such as password protection, encryption, and the type of editing now commonly accomplished by intelligent terminals. Later, we can expect a complete data management system to be added.

In applications where data entry is the dominant activity, the line between satellite computer systems and intelligent terminals, is already blurred. In memory-intensive applications, the intelligent disc of the future could also play a dominant role in the computer system of the future by executing a large percentage of the total software now limiting the efficiency and throughput of the CPU.



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TECH NOTE

Hardware Design Enhances Direct Decimal Calculations

Incorporating certain hardware elements into a processor significantly improves performance in execution of decimal arithmetic instructions

T. L. Jeremiah

IBM Corporation, Systems Division

Endicott, NY 13760

Digital processors use various techniques to compute decimal results from decimal inputs. Some computer architectures lack decimal instructions and rely on software subroutines to simulate decimal arithmetic using binary operations. A general purpose architecture, however, may provide decimal instructions that simplify the programming required to handle decimal data. These instructions help programmers immensely but pose a challenge to logic designers and microcoders who must implement them.

Overall, the IBM/4341 processor executes instructions approximately 1.6 times as fast as the IBM/3148 processor. However, the 4341 typically executes a decimal add instruction five times as fast as a 3148, and it executes a decimal multiply instruction 15 times as fast. This increased performance results, primarily, from incorporating specific items of hardware in the processor, which operates directly on multibyte, signed, decimal operands.

The apparently simple task of adding two decimal numbers is fairly complex when all applicable rules are examined. Consider the requirements for computing the sum of two decimal operands in IBM System/370 architecture.[1] Decimal numbers are stored as variable length fields, from 1 to 16 bytes long, with two digits packed into each byte. Each decimal digit is represented by its binary coded decimal (BCD) equivalent.[2] The least significant digit position in the field supplies the sign of the operand (Fig 1).

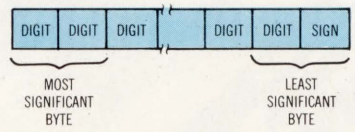

Fig 1 Packed decimal format. Operands can be up to 16 bytes long. Least significant byte always contains least significant decimal digit and operand sign. Instruction designates operand length. Decimal data are represented in BCD form

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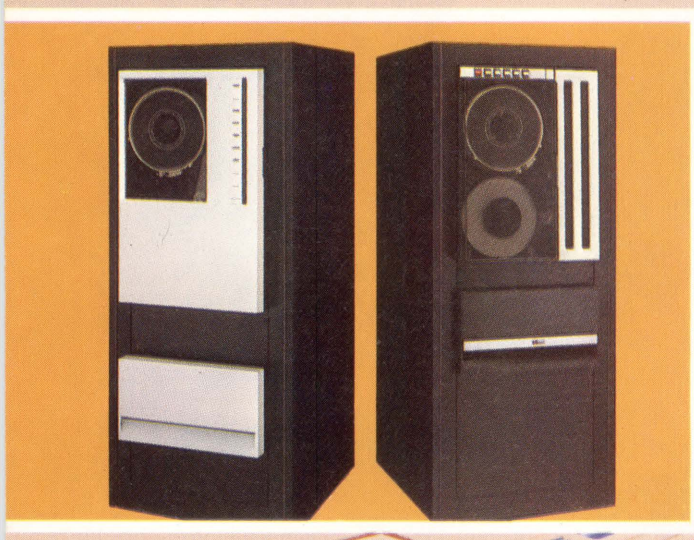

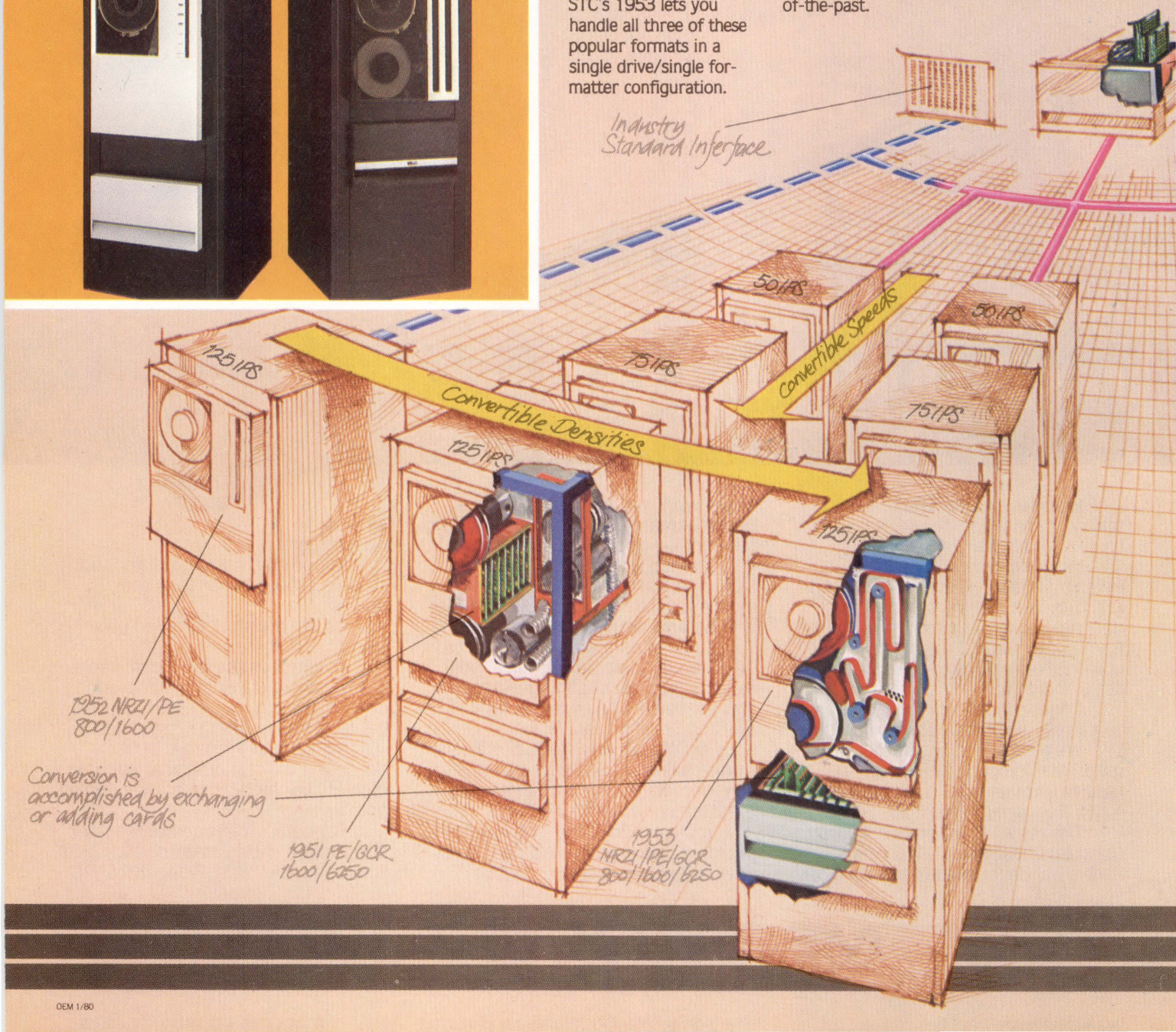

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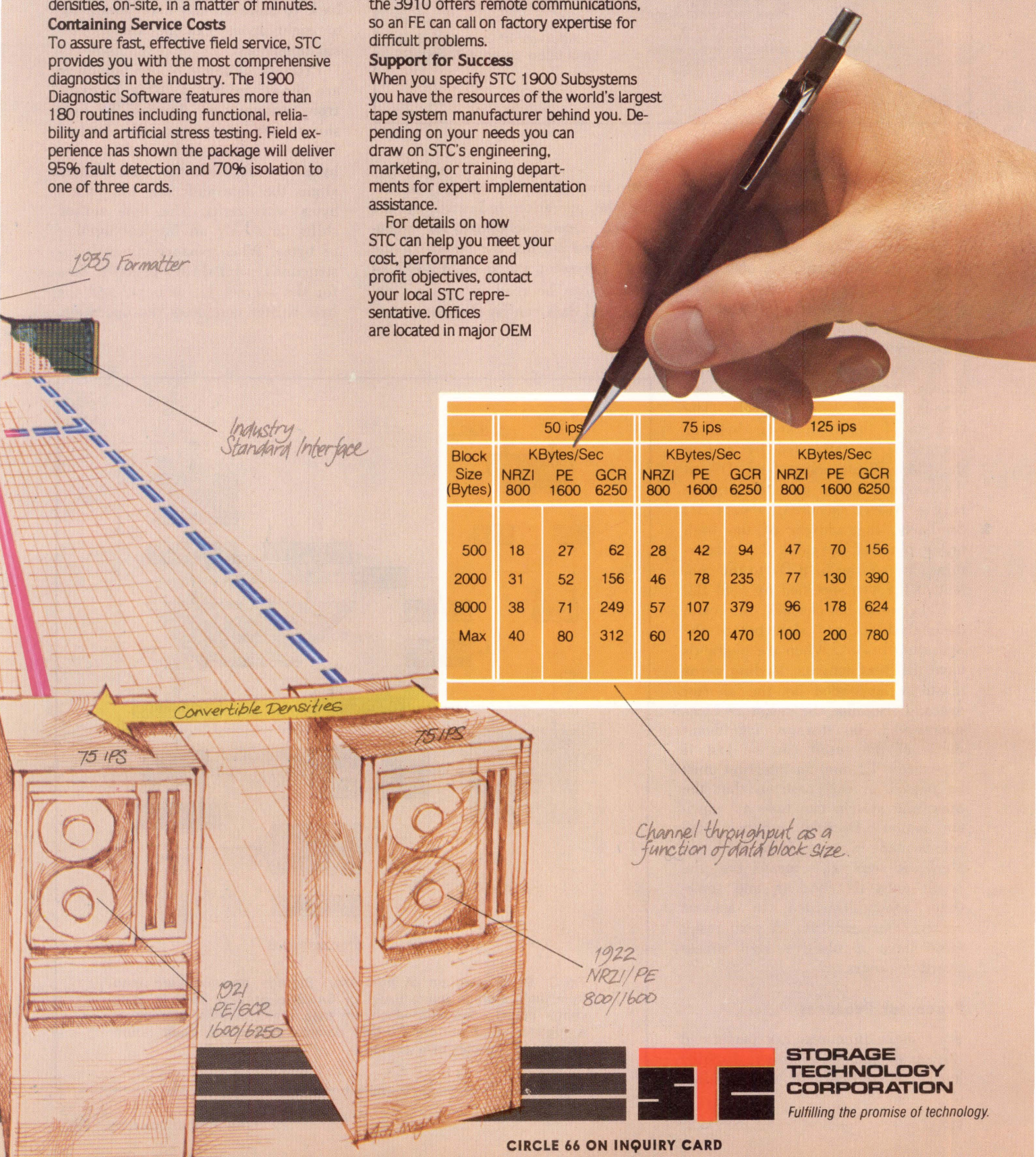

Block Size (Bytes)	50 ips KBytes/Sec NRZI 800	PE 1600	GCR 6250	75 ips KBytes/Sec NRZI 800	PE 1600	GCR 6250	125 ips KBytes/Sec NRZI 800	PE 1600	GCR 6250
500	18	27	62	28	42	94	47	70	156
2000	31	52	156	46	78	235	77	130	390
8000	38	71	249	57	107	379	96	178	624
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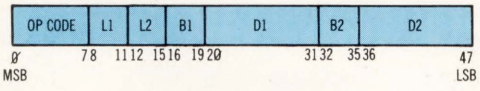

FIELD NAME	FIELD LENGTH	FIELD DEFINITION
OP CODE	8 BITS	DEFINES OPERATION TO BE DONE
L1	4 BITS	OPERAND 1 LENGTH IN BYTES
L2	4 BITS	OPERAND 2 LENGTH IN BYTES
B1	4 BITS	OPERAND 1 BASE ADDRESS REGISTER
D1	12 BITS	DISPLACEMENT TO BE ADDED TO CONTENTS OF B1 REGISTER
B2	4 BITS	OPERAND 2 BASE ADDRESS REGISTER
D2	12 BITS	DISPLACEMENT TO BE ADDED TO CONTENTS OF B2 REGISTER

Fig 2 Storage to storage instruction format. The 24-bit address of operand 1 is created by adding content of GPR specified by B1 field to 12-bit displacement in D1 field. Result addresses most significant byte of operand 1. Address of operand 2 is calculated using B2 and D2

Decimal addition, subtraction, multiplication, and division are all storage to storage (ss) operations. That is, operand 1 and operand 2 are obtained from storage, the operation is performed, and the result replaces operand 1 in storage. Fig 2 shows the format of an ss instruction. The operation code defines the operation to be performed, while L1 and L2 denote the length, in bytes, of operands 1 and 2, respectively. The address of the high order byte of operand 1 is calculated by adding the 12-bit displacement field, D1, to the content of a general purpose register (GPR) specified by field B1. Similarly, the address of the high order byte of operand 2 is determined by adding field D2 to the content of the GPR specified by field B2.

Data must be checked for valid decimal digits and sign before the operation begins. When the operands have different lengths, leading zeros must be appended to the shorter operand. Because the result replaces operand 1 in storage, significant digits of the result can be lost if L2 exceeds L1, and an interrupt must be posted in this case so that the operating system can take appropriate action. Decimal numbers are represented in true form with an algebraic sign. This means that the result must be checked, and sometimes recomplemented, to achieve correct representation. A zero result must have a positive sign unless overflow occurs.

Processor Features

Four main functions are performed during decimal operations: fetching and aligning operands, and padding with zeros where necessary; executing the operation indicated by the operation code; checking for exceptions; and storing the result. In the 4341 processor up to eight bytes of storage can be read in a single access, and data can be aligned properly as they enter the processor. The arithmetic and logic unit (ALU) can add or subtract 8-byte operands. Exception checking is designed to optimize execution of the normal or nonexception case, which is the typically encountered situation. Data can be aligned as they are written back to storage, and here again, up to eight bytes can be transferred simultaneously.

Primary elements of the processor are shown in Fig 3. Data accessed from storage pass through the byte shifter and are temporarily latched in the D register. If fewer than eight bytes are fetched, the byte shifter aligns the data and pads the vacant bytes with zeros. The byte shifter shifts data only an integral number of bytes. When performing shift instructions, a bit shifter preshifts data for the correct bit amount, and the byte shifter completes the operation.

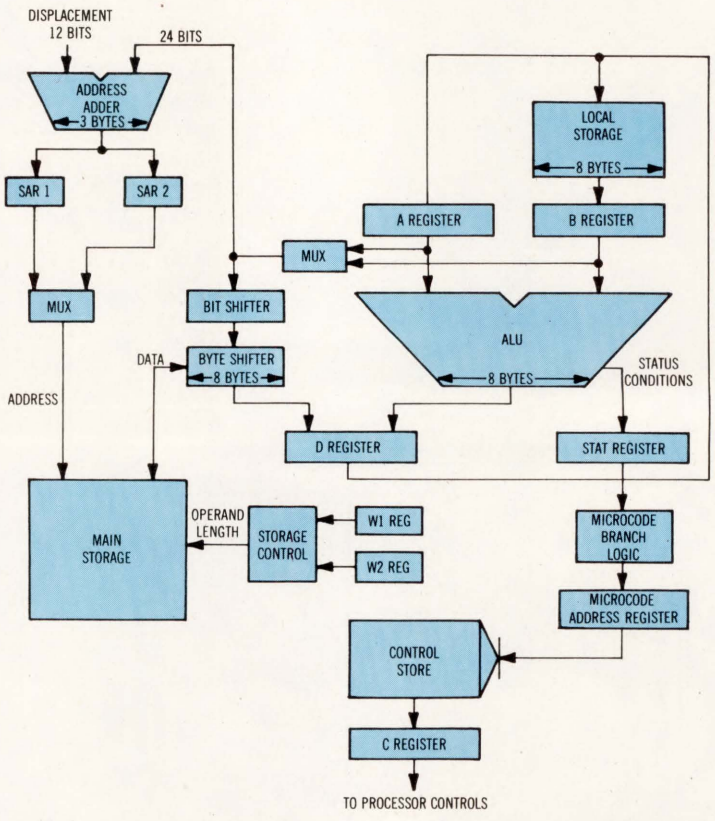

Fig 3 Block diagram of processor. Storage operands are read from main storage using SAR1 or SAR2 to provide address. Byte shifter aligns operands, which are then saved in local storage or A register. ALU performs 8-byte decimal operations. Data return to storage through byte shifter

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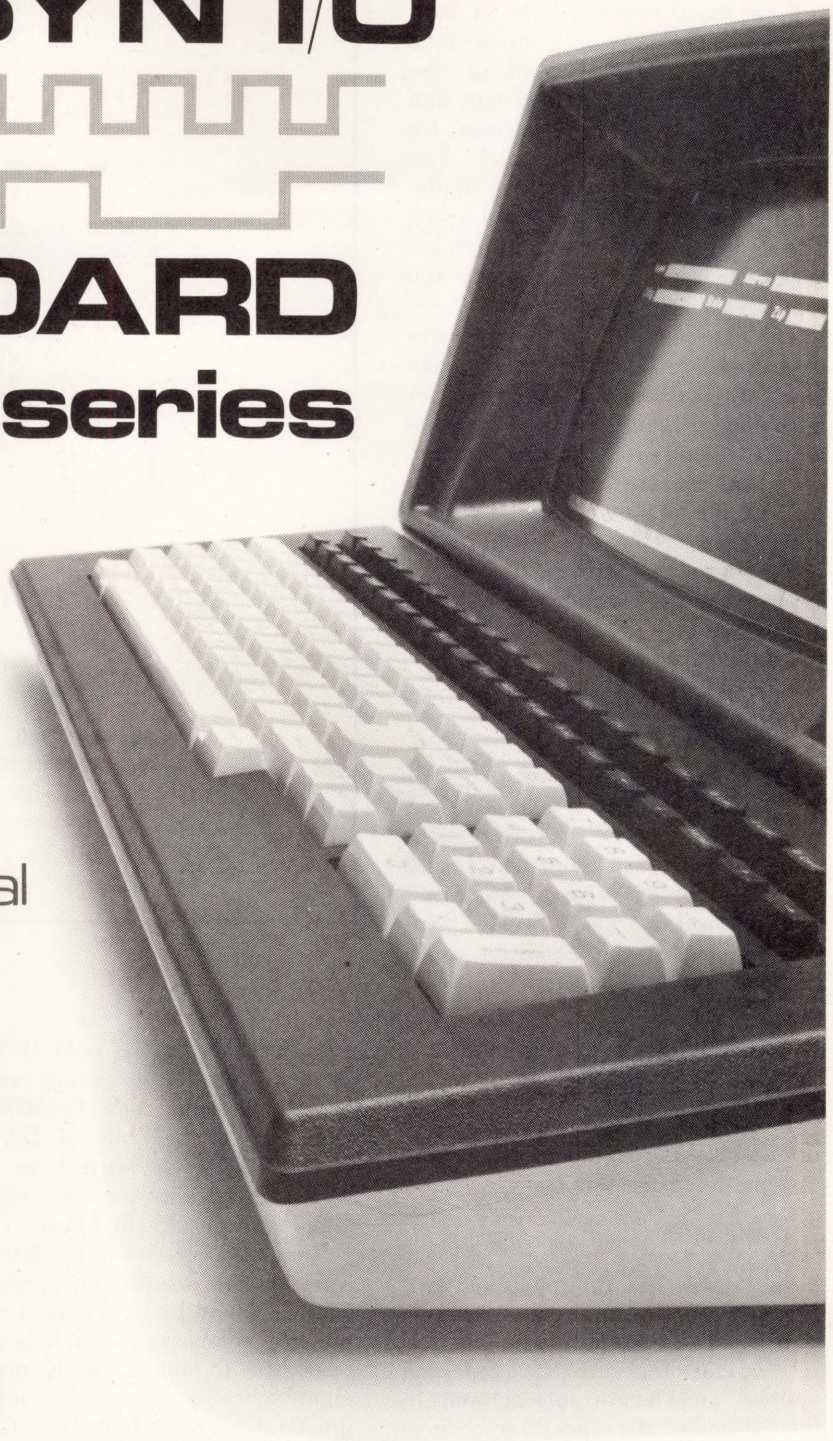

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From the D register, data are written into local storage, which is a high speed array containing the GPRs, the floating point registers, and a number of working registers for temporary use by the microcode. The A (temporary) register is implemented outside the high speed array. The B register acts as a buffer between the array output and the ALU input.

The ALU can add up to eight bytes of binary or decimal data in one pass. Operand sign digits need not be removed before adding or subtracting. Hardware analyzes operand signs and generates the correct result sign at the ALU output. ALU results are latched in the D register before being stored in the A register or in local storage. Status conditions generated in the ALU are kept in the status (STAT) register.

Operand lengths reside in the W1 and W2 registers, which are set from the L1 and L2 fields of the SS instruction. Storage addresses are kept in storage address registers 1 and 2 (SAR1 and SAR2). The C register controls processor sequencing and contains the microword accessed from control storage. Branch decisions are made using condition codes stored in the STAT register.

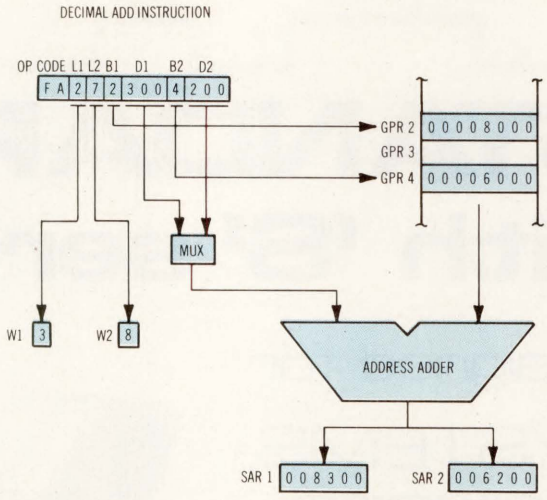

Fig 4 Processor registers after initialization. Decimal addition initializes address and length registers as shown. One separate cycle through address adder creates each operand storage address

Decimal Addition Example

To demonstrate the sequence of operations performed by the processor in a typical decimal calculation, assume the instruction is

FA2723004200

hexadecimal. The first operation performed when executing any instruction is to decode the instruction and set various registers with operand address and length information. In this example, the operation code is FA, which directs execution to the decimal add routine in microcode (Fig 4).

The L1 field indicates that the length of operand 1 is three bytes, and the W1 register is set accordingly. Field L2 designates the length of operand 2 as eight bytes, and W2 is set to this value. The GPR specified by the B1 field (GPR2) is fetched from local storage and its content (assume 00008000) is added to the D1 field. This result, 008300, is loaded into SAR1. Similarly, the GPR specified by the B2 field (GPR4) is fetched from local storage and its content (assume hex 00006000) is added to the 12 bits of D2. This result, 06200, is latched in SAR2. The storage addresses of operands 1 and 2 are now ready to use.

Next, W2 is tested to determine whether the length of operand 2 exceeds eight bytes. There are four possible combinations of lengths for operands 1 and 2: both may be eight bytes or less; both may be greater than eight bytes, or one may be greater than eight bytes, while the other is not. The particular combination of operand lengths determines which of four different microcode sequences is followed.

In this example, operand 2 is eight bytes long, so it is read from storage at address 6200 and saved in working register 1 in local storage. The W1 register is now tested to establish the length of operand 1. Since operand 1 is three bytes long, it is fetched from storage, shifted right five byte positions (vacant byte positions are padded with zeros) and latched in the A register.

Both operand 1 and operand 2 are not present in the internal registers, properly aligned, and ready for addition. Working register 1 is accessed and operand 2 is placed in the B register. In this example, operand 1 is +12345, decimal, and appears as

000000000012345A

in the A register (Fig 5). Operand 2 is +49736 and in the B register is represented as

000000000049736C

The low order digit of the A register is the sign of operand 1, and the low order digit of the B register is the sign of operand 2. A, C, E, and F are all valid plus signs, while B and D are minus signs.

Upon entering the ALU, both operands are checked for valid decimal digits and signs. If an invalid condition is detected, the invalid decimal format bit is set in the STAT register

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for later use by the exception handling microcode. Hardware analyzes the sign bytes and, depending on the outcome of analysis, instructs the ALU to perform either a true add or a complement add. In this case, both operands are positive and the instruction is add, so the ALU will do a true add. If either one but not both operands were negative and the operation was add, the ALU would execute a complement add. If both operands were negative and the operation was add, a true add would be performed. If the operation were subtract and either operand (but not both) were negative, a true add would be performed; otherwise, a complement add would be executed.

The sign of operand 1 determines the result sign generated by the ALU. In this case operand 1 is positive, so a C, the preferred plus sign, is generated directly at the ALU output. If operand 1 were negative, a D, the preferred minus sign, would have been generated instead. The generated sign is correct unless the ALU is performing a complement operation and the magnitude of operand 2 exceeds the magnitude of operand 1. If this condition does exist, the ALU generates a result in 10s complement form with an algebraically inverted sign. This situation sets the STAT register recomplement bit. If a recomplement is required, it is performed in a subsequent cycle. Recomplementing consists of subtracting the result digits from zeros and reinverting the sign. The ALU provides a recomplement function for this purpose.

Subsequently, the hardware zeros out the sign of operand 1 before it enters the binary adder section of the ALU. The operand 2 sign is forced to F by the hardware, and each decimal digit of operand 2 is increased by six as it passes through decimal logic translation (Fig 5).

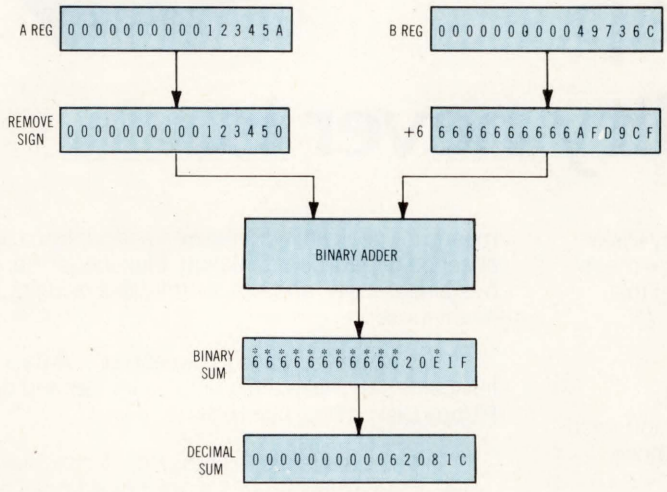


Fig 5 Decimal operands at various levels in ALU. A and B registers are set to values shown. At next ALU level, sign of operand 1 is zeroed, sign of operand 2 is set to F, and all remaining B input digits are increased by six. Binary result must be corrected, decreasing by six value of each digit that did not produce a carry (identified by asterisks). Hardware forces sign of result to C

Altering the sign allows a carry to propagate through the sign position if a carry is present; a carry-in would be present for a complement add. Increasing the operand 2 digits by six causes the carry to propagate correctly from digit to digit. If a complement add is necessary, the digits of operand 2 are altered by negating each bit instead of increasing each digit by six.

Operand 1, as it enters the binary adder portion of the ALU, is now

0000000000123450

while operand 2 is

6666666666AFD9CF

After a binary addition occurs, the data digits are ready for correction, which is required for each digit that does not have a carry-out. If a carry-out occurs, the digit is already correct; otherwise, a minus-six translation is performed automatically. Fig 5 shows the binary addition of operand 1 and operand 2. Each digit that did not have a carry-out (and, as a result, requires correction) is identified by an asterisk. The low order digit of the binary sum is discarded because the result sign will be used in its place. The result, after correction, is

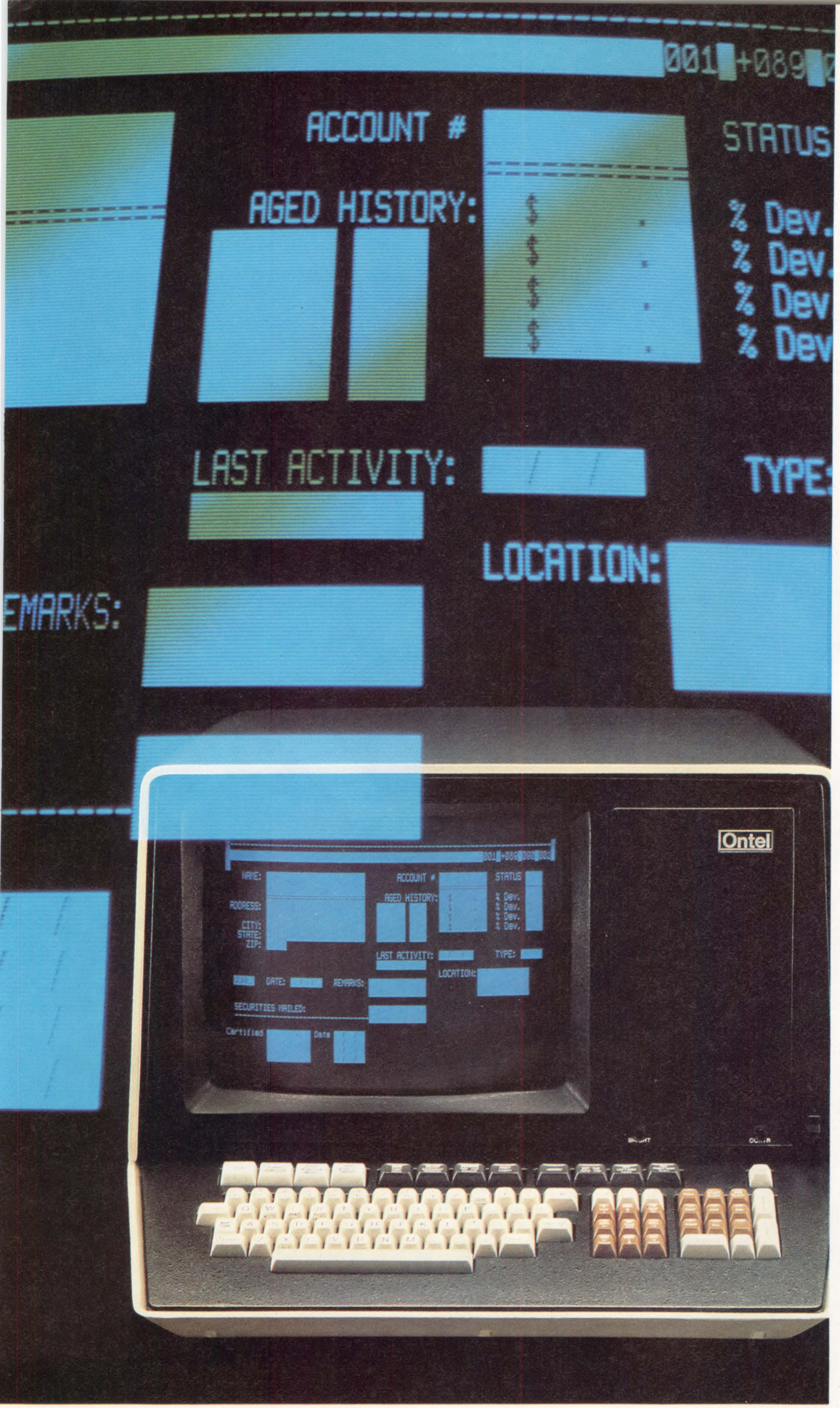
000000000062081C

the BCD equivalent of +62081.

Once this sequence is complete, the 8-byte, signed, decimal result is latched in the D register and then stored back into working register 1. Additional status is also generated at this time. If nonzero digits are detected in the result data outside the bounds of the operand 1 length, or if an overflow occurs from the ALU high order byte, the STAT register size exception bit is set. Another status condition generated is "ALU output not equal to zero," which is required to determine whether the generated decimal sign is correct.

All status conditions are combined in a single-branch test so that only one test determines whether the result is ready to return to storage; a zero result, a decimal format error, a size exception, or a recomplement condition all require further action. Very often these conditions

(continued on page 130)



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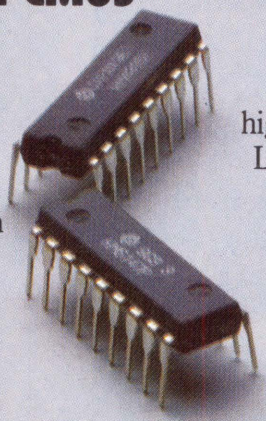

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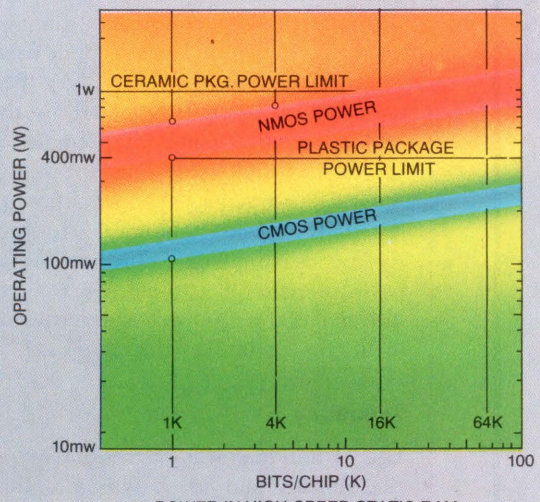

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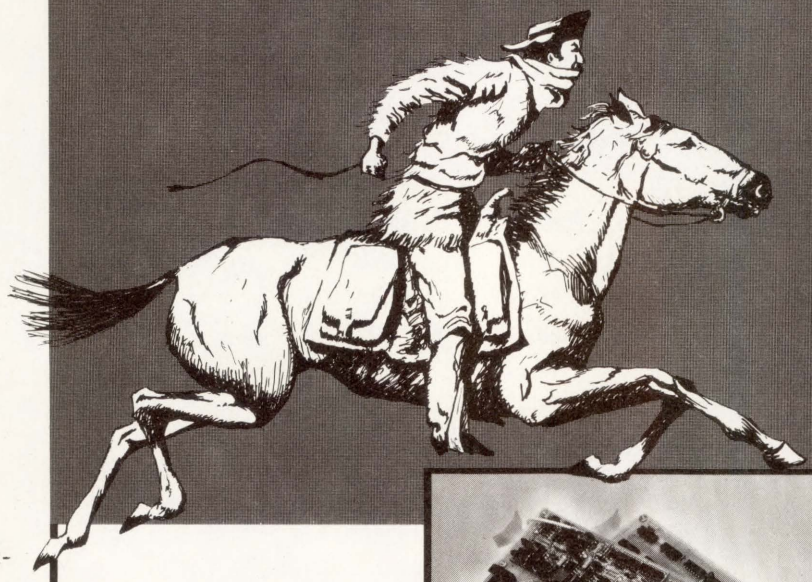

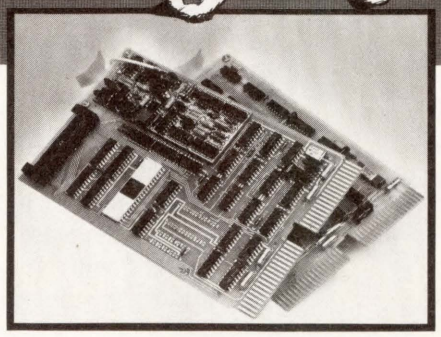

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are not present, so the correct result has been generated and can be returned immediately to the operand 1 location in main storage. (For simplicity, the example was chosen so that no exceptions would result.) Should an exception be present, a branch to an exception handling routine occurs. Here, the cause of the exception is determined, and the appropriate action is taken. The final operation stores the content of working register 1 into main storage, using SAR1 as the storage address and W1 as the length.

Additional cycles through the add routine are used when either or both operands exceed a length of eight bytes. If a second pass through the ALU is necessary to complete the add, two bits in the STAT register, set on the first pass, are needed to control the second pass. One of these bits, ALU carry, remembers the carry-out of the high-order byte on the first pass and is used as the carry into the low order byte on the second pass. The other bit, complement decimal, reflects the result of analyzing the two operand signs and the operation performed in the first pass. If the ALU does a complement operation in the first pass, this bit is set to continue a complement operation in the second pass.

Whenever operand 1 is longer than eight bytes, SAR1 is updated in the address adder using the length of the first storage access as the increment. If required, SAR2 can be updated in a similar manner. This updating mechanism helps processor performance by eliminating the requirement for an extra microword to do the update in the main ALU.

Summary

Use of 8-byte storage access, a versatile shifter, and an 8-byte ALU that can add two signed, decimal operands in a single pass provide a considerable performance improvement during execution of decimal instructions.

References

1. *IBM System/370 Principles of Operation*, GA22-7000, IBM Corp, System Products Div, Poughkeepsie, NY, 1974
2. R. K. Richards, *Digital Design*, Wiley-Interscience, Chap 7, 1971

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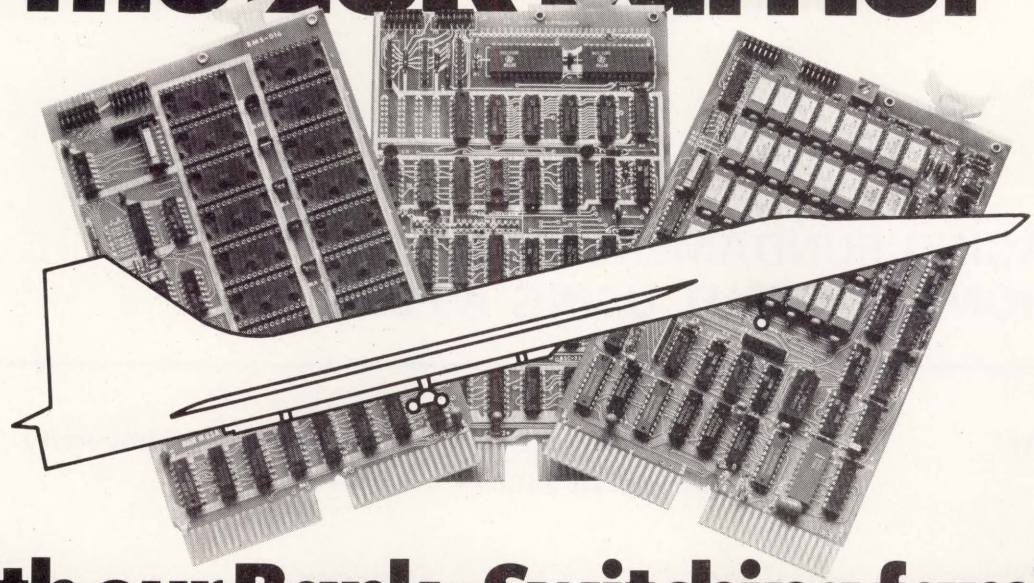

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CIRCLE 72 ON INQUIRY CARD

INTERFACING FUNDAMENTALS: CONDITIONAL OUTPUT USING A FLAG

Peter R. Rony

Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

As was the case for conditional *input* using a flag,[1] conditional output techniques that employ flags can be distinguished by whether or not there is a buffer between the microcomputer and the output device. The block diagrams presented as Figs 2 and 3 of Ref 2 meet both of these situations, provided that the modification made in Ref 1 is again made; ie, there is no connection between Q and the output device in Fig 3 of Ref 2. Thus, the flipflop in the figure acts as a flag rather than as a semaphore.

Fig 1 of this month's column, which can be compared to Fig 1 in Ref 1 and 3, depicts the data transfer between a microcomputer (source) and an output device (acceptor) in the presence of a single flag. A low (logic 0) condition for the flag indicates to the microcomputer that previous output data have been accepted. A high (logic 1) condition indicates that the previous data have not been accepted. When a flag is used, only the microcomputer tests its logic state, as can be seen by the direction of the dotted line and the decision symbol, "Flag sensed low?," in Fig 1. The output device does not know when new data are available. Therefore, as was the case in Ref 1, the microcomputer alone has the responsibility for the synchronization of data transfer.

This flag is used to synchronize data transfer between the microcomputer and the output device. To see how that occurs, consider Fig 2, which gives the timing diagrams when a single flag, but no output buffer, is present. The flag is reset by the positive edge transition of the $\overline{\text{ACK X}}$ pulse, which is generated by the output device, and set by the logic 0 condition of the $\overline{\text{WR X}}$ pulse, which is generated by the microcomputer.[3] As a result, the output device sends an

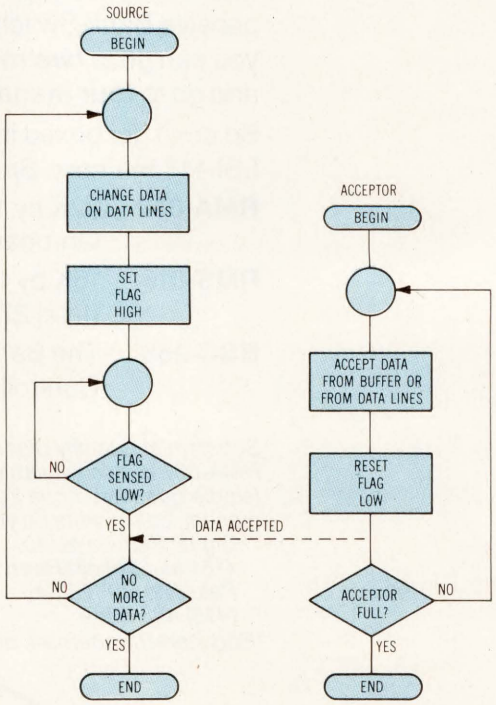

Fig 1 Flow charts for source and acceptor. Single flag, which communicates only with microcomputer, indicates, when in low state, that output data has been accepted and processed

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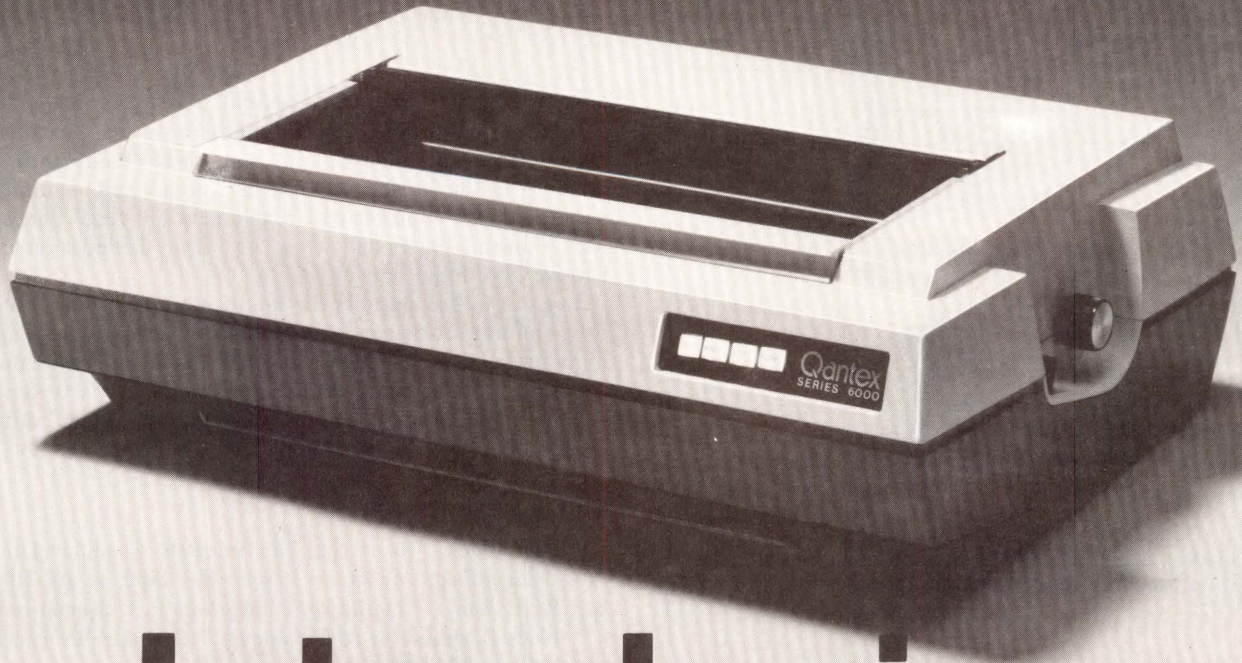

Introducing

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$\overline{\text{ACK X}}$ signal that clears the flag and indicates to the microcomputer that the previous data have been received and processed. Then, after a period of time, the microcomputer places new output data in the accumulator, enables the data bus, and generates a $\overline{\text{WR X}}$ pulse that sets the flag and causes the output device to latch the data from the data bus. At this point, the output device has the data, but it must do something with them, such as convert them to analog voltages, print them, store them on disc or tape, or display them. In other words, the output device must process the data before it sends another $\overline{\text{ACK X}}$ pulse, which indicates its readiness to receive additional data. The repetition rate at which the output device can receive data can be estimated from a full flag period, from positive edge to next successive positive edge.

Output devices that can generate an acknowledge signal, $\overline{\text{ACK X}}$, typically also have an output buffer, so the situation depicted in Fig 2 is the exception rather than the rule. The more commonly encountered situation is given in Fig 3, which shows the timing diagrams for an output device that has both a flag and a output buffer. As shown in that figure, the acceptance and processing of previous data is acknowledged by the $\overline{\text{ACK X}}$ signal, which resets the flag. After a period of time, new data to be output appear in the accumulator and then on the data bus. Finally they are latched by the buffer with the aid of the microcomputer generated $\overline{\text{WR X}}$ pulse, which also sets the flag. The next $\overline{\text{ACK X}}$ pulse appears only when the output device is ready to receive additional data.

Use of the flag permits the microcomputer (source) to ignore the output device (acceptor) for as long as the flag is high (logic 1). Such a characteristic frees the microcomputer to perform other processing tasks while it waits for an acknowledge signal, and is very useful with "slow" output devices (500 bytes/s or less).

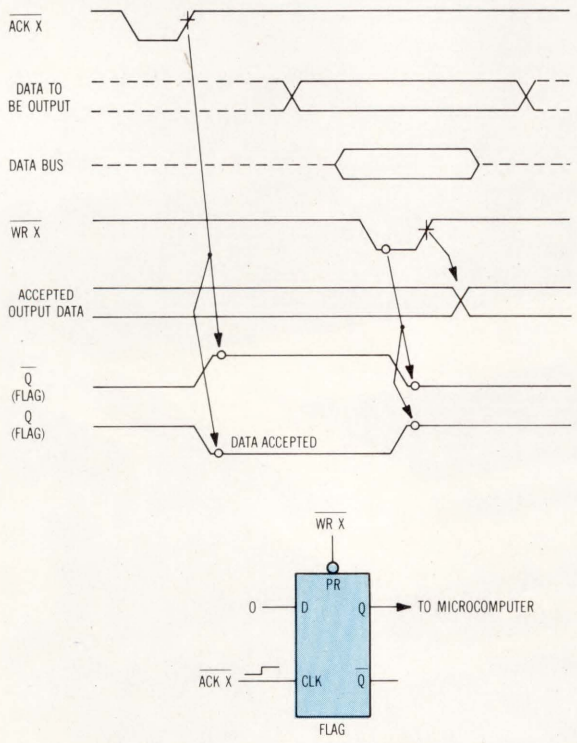

Fig 2 Conditional output with flag and no buffer. Timing diagrams demonstrate sequence of timing signals and data transfers for microcomputer output using flag shown

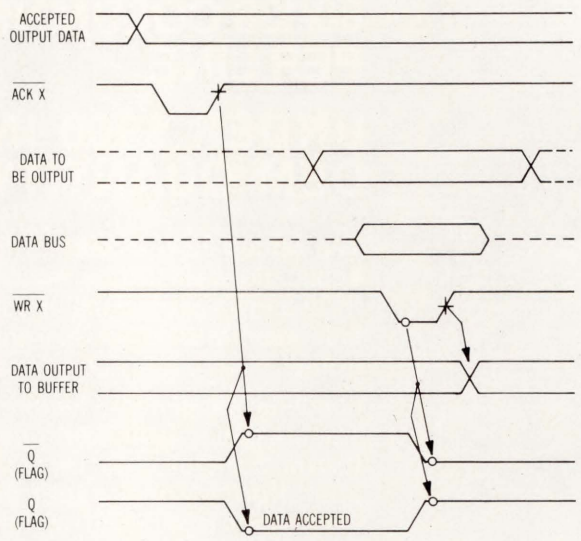

Fig 3 Conditional output with flag and buffer. Timing diagrams demonstrate sequence of timing signals and data transfers for microcomputer output using flag shown in Fig 2

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1. P. R. Rony, "Interfacing Fundamentals: Conditional Input Using a Flag," *Computer Design,* May 1980, pp 208-210
2. P. R. Rony, "Interfacing Fundamentals: A Comparison of Block Diagrams for I/O Techniques," *Computer Design,* Feb 1980, pp 175-177
3. P. R. Rony, "Interfacing Fundamentals: Conditional I/O Using a Semaphore," *Computer Design,* Apr 1980, pp 166-167

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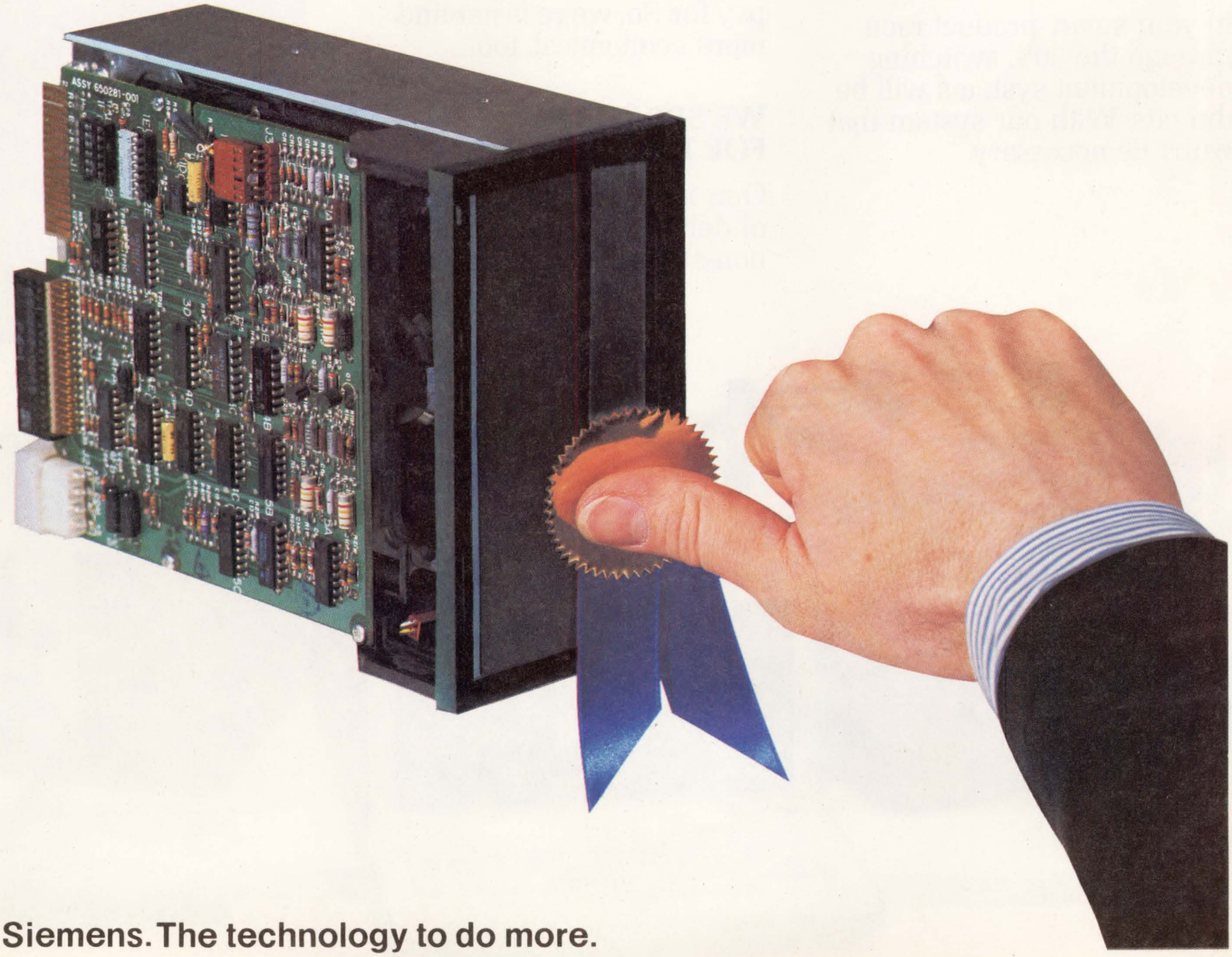

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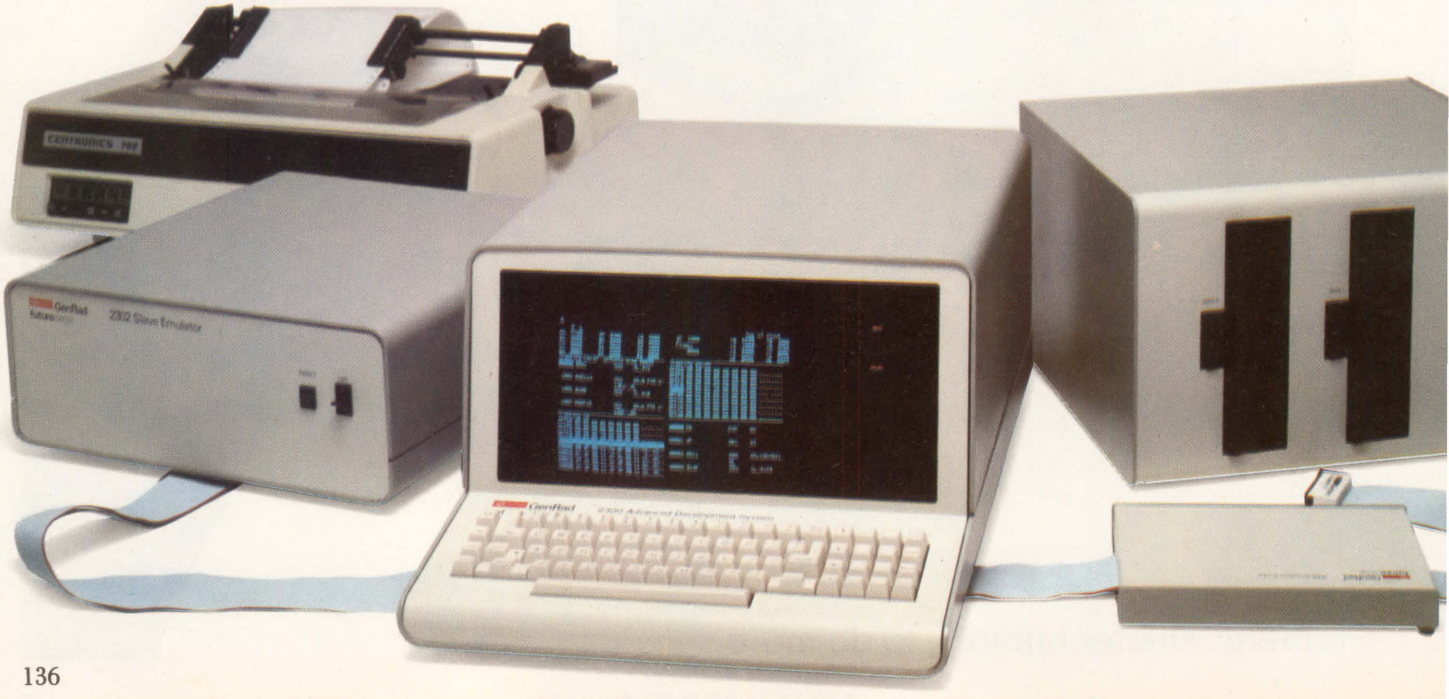

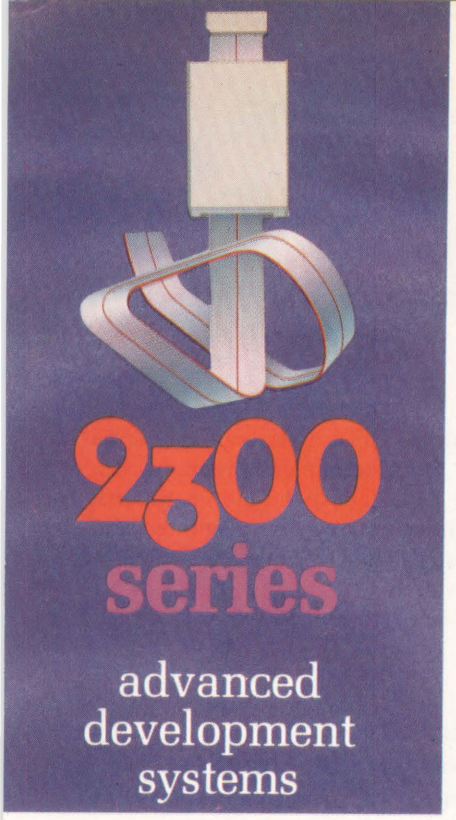

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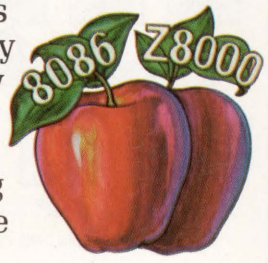

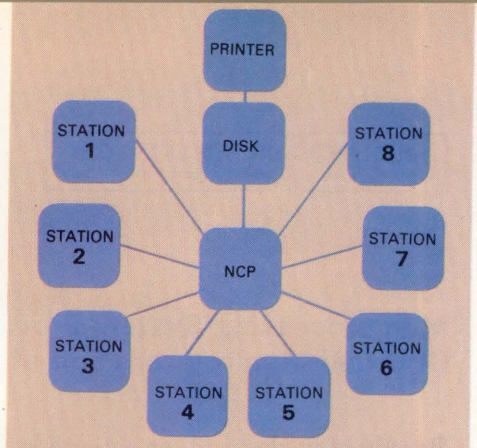

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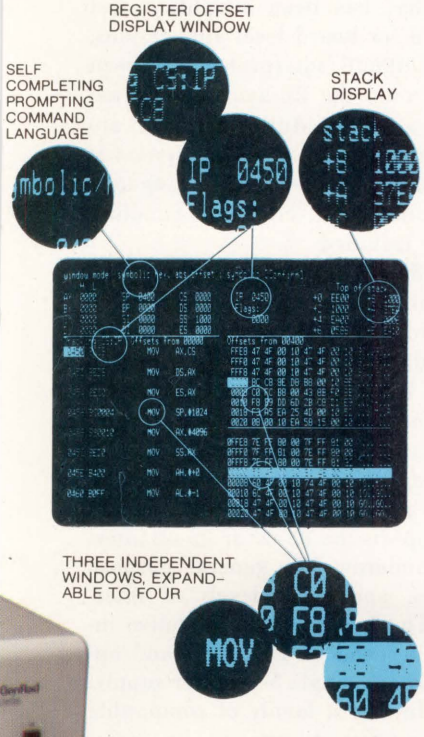

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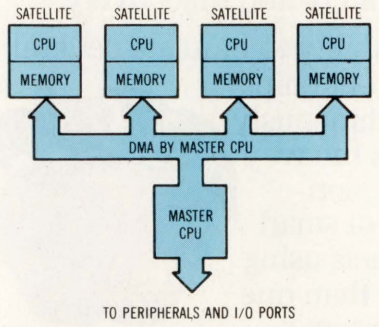
Each standalone workstation in the system, designed and manufactured by Micromation Inc, 1620 Montgomery St, San Francisco, CA 94111, is based upon a Z-64 CPU board containing a Z80A microprocessor and 64k-byte dynamic RAM, operating at a full 4 MHz. A fully configured workstation also has a floppy disc controller board and an I/O board. Eight boards would be used in a 4-station system: a master Z-64, multiuser I/O, four satellite Z-64s, a hard disc controller, and a floppy disc controller. This system would provide 320k bytes of RAM, up to four double-density floppy disc drives, 20M bytes of Winchester hard disc storage, four terminals, and two printers.

Because the satellites do not require direct access to I/O ports, bus arbitration is simplified. Each satellite is polled at 8-ms intervals by the master CPU, which performs all I/O by directly accessing the indicated memory location of the satellite.

Any standard CP/M program could be executed at each workstation while a master Z80A CPU ran an enhanced version of MP/M, arbitrating bus usage and performing I/O functions for the satellite workstations. The system is fully interrupt driven for fast operation.

All queuing and arbitration are performed by the enhanced and adapted MP/M operating system, resident on the master Z-64 board. There are no bus I/O conflicts between satellites. I/O and disc read/write functions are fully interrupt driven such that, when a character is generated at a satellite console, the I/O UART interrupts the master CPU, which then directs the signal to the satellite Z-64 according to the priorities established in the MP/M operating system.



Micromation Z-System. Multi-user, multiprocessing computer has microcomputer board with its own 62k-byte memory in each satellite workstation, all controlled by master CPU. Any standalone workstation can fail without interfering with operation of other three

Similarly, when a file is read from disc, the master CPU determines the relative location of the desired information to the read/write head and sets up an interrupt to occur when the information has nearly reached the read/write head. The master CPU then proceeds to poll satellites, handle console and printer I/O, and read or write to other discs until the interrupt signal occurs.

Four RS-232 serial ports with full handshaking are provided on the multiuser I/O board to drive the workstations independently. Baud rates are individually switch selectable from 0 to 9600.

Two parallel output ports and three parallel input ports are provided to drive a parallel printer, and the floppy disc controller has a serial port for the serial printer. An optional Centronics interface, including cable and software drivers, is also provided. An interval timer on the I/O board is configured as a realtime clock. Users can access the time from terminals; programs can print day, date and time on reports; and interrupts can be generated and executed based on either real time or intervals.

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This 3.94 x 6.3″ (10 x 16-cm) Z8-SBC board, introduced by Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, can accommodate up to 8k bytes of RAM, ROM, or EPROM and is designed for fast data processing and data acquisition. It contains two counter/timers, five 8-bit parallel I/O ports, a programmable asynchronous serial channel that supports the RS-422 or RS-423 interface standards, 124 general purpose registers, and three levels of interrupts. The board has an effective instruction speed of 3.72 MHz and operates from a single 5-V power supply.

The first of a family of compatible microcomputer boards to be introduced, this Z8-SBC board will be available in July. Later boards will include floppy disc controller, single-board terminal, universal memory, and digital and analog I/O. Interface among boards will be via a specially developed bus structure to 96-pin high density pin and socket connectors.

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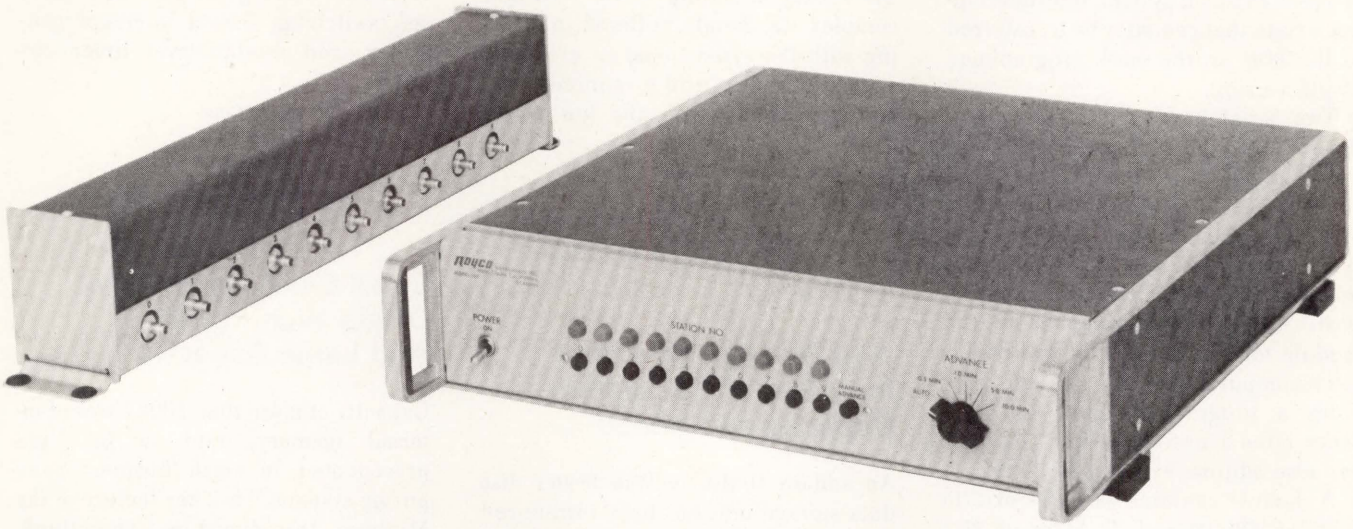

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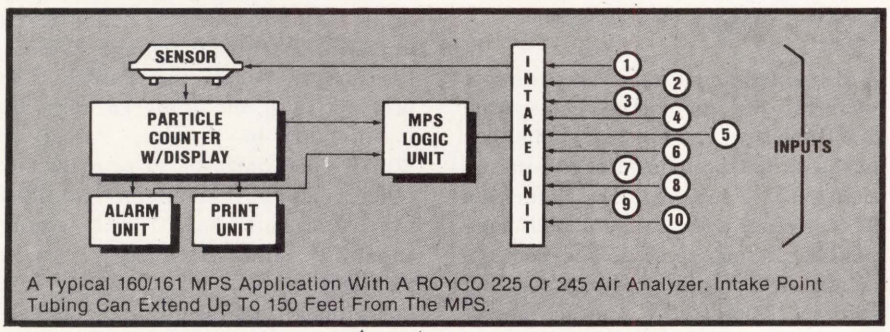

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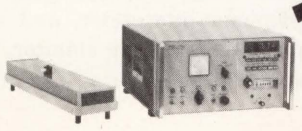

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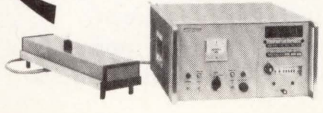

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CIRCLE 76 ON INQUIRY CARD

software for systems based on the Z8 single-chip microcomputer. The Z8 development module uses the 64-pin version of the microcomputer to prototype a Z8-based system, thus developing a code that can later be transferred to the ROM on the mask programmed 40-pin version.

Two serial RS-232-C interfaces allow the 11 x 14" (28 x 36-cm) board to be used standalone with a CRT, or to be connected to one of the company's PDS or ZDS-1 series development systems. Cable connection to a host system permits the transfer of software from the host—where it is developed—to the module for testing. One of two 64-pin microcomputers on the module provides a program monitor CPU, the other offes a user-accessible CPU that can also address external memory.

A module contains 4k bytes of 2716 monitor EPROM and 2k bytes of 2114 user static RAM. In addition, a socket is provided for 2k bytes of 2716 EPROM that may be used in place of the available 2k bytes of RAM to test a ROM based version of the user's code. A 40-in² (258-cm²) wirewrap area accommodates additional customer interfaces or special application circuits. Monitor/debug software, resident in EPROM, provides commands for control, I/O, and debug. This program consists of terminal handler, debugger, command interpreter, and upload/download handler.

Circle 466 on Inquiry Card

64k RAM Module for EXORcisor Has Transparent Refresh

A 64k-byte dynamic RAM micromodule, the M64EX™, has been announced by Percom Data Co, Inc, 211 N Kirby, Garland, TX 75042, for use with the Motorola EXORcisor and other EXORcisor bus compatible systems. It features transparent refresh and optional parity check and includes an exclusive address translator circuit that accommodates program controlled memory allocation for applications such as multitasking. Any combination of 4k blocks of RAM—within the upper 32k bytes of memory space—can be enabled or disabled with an onboard DIP switch, permitting the address translator to implement functions such as write protection of program selected memory blocks. Other features include DIP socket mounting of all RAM and complex ICs, 3-state buffered interfacing with the system bus, an extensive capacitor bypass grid to minimize circuit generated noise, and low power drain.

Circle 467 on Inquiry Card

Add-On Hard Disc Unit Increases MDS System Capacity and Speed

An add-on 10M-byte Winchester disc data storage unit has been introduced by Advant Corp, 696 Trimble Rd, San Jose, CA 95131, for use with all Intel MDS development systems. The MicroSupport™ model 105 uses environmentally sealed Shugart 8" (20-cm) discs and is transparent to users. Operation is the same as with floppy discs except that speed and data capacity are greater. Error correction is built in. Microprocessor based controller and power supply are included.

Circle 468 on Inquiry Card

Software/Interface/Printer Package Fits CP/M and MP/M Based Systems

A combination package consisting of powerful file management, versatile S-100 interface, and low cost printer has been introduced by MicroPro International, 1299 Fourth St, San Rafael, CA 94901, for use with CP/M and MP/M compatible microcomputers. The package combines WordStar™ word processing software, I/OMaster™ interface board, and 55-char/s NEC Spinwriter parallel printer at a price nearly $600 less than the total of their individual costs.

Drivers and functions normally found in more expensive serial printers are contained within the software and the interface. Increased printing speed and optional twin-sheet feeding are available with the parallel printer. Other features include simultaneous use of high speed line printers, dual synchronous/asynchronous serial ports with FIFO buffering to prevent loss of keystrokes during disc I/O and MP/M task switching, 8-level interrupt controller, and dual-interval timer circuitry.

Circle 469 on Inquiry Card

Small Business System Offers High Speed And Large Capacity

Capacity of more than 100k bytes of internal memory, said to be "unprecedented in small business computing systems," is a key feature of the Minimax. Introduced by Computhink, 965 W Maude Ave, Sunnyvale, CA 94086, the 6502 microprocessor based systems retrieve data from dual-density floppy disc drives at 15k char/s. Minimax I has a file storage capacity of 800k bytes, while the II version maintains 2.4M bytes of online disc storage.

Features include full screen data entry with capabilities for character deletion or insertion, and individual field editing with field protect and automatic skip to the next field. Split screen operation allows the operator to have two processes online at the same time.

The 2-MHz CPU executes all standard microprocessor instructions as well as 64 additional user definable instructions. At initialization these instructions are microprogrammed to execute the 64 instructions of the FIFTH universal machine language (a combination of FORTH and Pascal). The user may also microprogram these 64 instructions to perform Pascal or FORTH operations, or to emulate any other computer. Maintained in ROM are Microsoft BASIC with string capability and extended precision floating point, a complete DOS operating system including random access data files, high resolution graphics commands, a FIFTH language microprogrammed interpreter, and a complete machine language monitor.

Circle 470 on Inquiry Card

WINCHESTER DISKS
FLOPPY DISKS
DEC® RX02 COMPATIBILITY
LSI-11® Q-BUS
IN A SINGLE ENCLOSURE!

COMPATIBILITY . . .

Add 10M bytes of Winchester disk and 1M bytes of floppy disk storage to your LSI-11 computer with the SMS DSX01172 Disk System 11X. Plug any configuration of LSI-11 modules (including LSI-11/23) into the Disk System 11X's 8 quad slot Q-Bus backplane. Enough power is provided for up to (13) dual height cards and the SMS dual height "Flinchester" controller.

The single dual head floppy disk is hardware, software and media compatible with the DEC RX02. Software selectable IBM 3740, 2/2D formats provide diskette interchange with IBM and other non-DEC systems. On-board bootstrap loads (from Winchester or floppy) and runs your RT-11, RSX-11M and other software automatically at power up. All this plus resident diagnostics in a single 10-1/2" package.

AND MORE PERFORMANCE . . .

The latest 8" Winchester disk technology gives you up to 20% faster data transfers than DEC's RL01. Extended mode operation allows multiple sector and contiguous across track block transfers during Winchester or floppy access. The DSX01172 also runs floppy disk fill and empty buffer operations over 34% faster than RX02. Automatic error retry and automatic flaw mapping are standard features during Winchester disk data transfer.

PLUS GROWTH

For storage needs beyond 10M bytes, the SMS WIN 1426 add-on Winchester disk provides up to 26.4M bytes for Disk System 11X. Choose either a DSX01172 resident 10M bytes Winchester disk or an add-on 26.4M byte 14" Winchester in a low profile 5-1/4" enclosure. The WIN1426 cable connects directly to the SMS "Flinchester" controller resident in the Disk System 11X. And the WIN1426 provides twice the data transfer performance and five times the storage capacity of DEC's RL01.

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PDP-11 or LSI-11 Winchester plus floppy disk add-on storage in a single 5-1/4" package!

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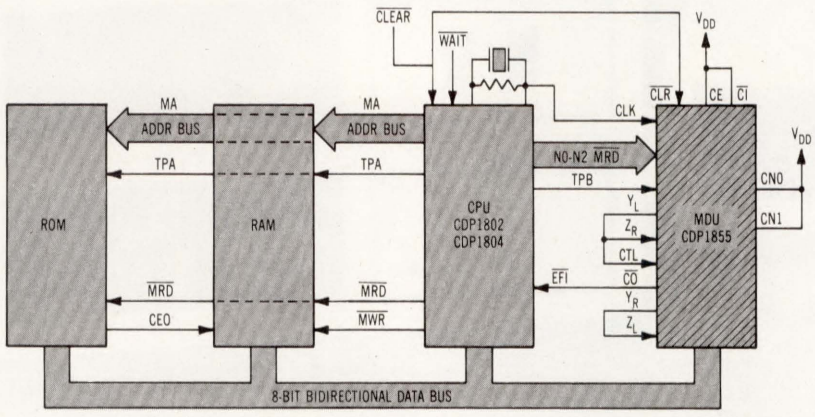
CIRCLE 77 ON INQUIRY CARD

Multiply/Divide Units Increase Microprocessor Capabilities



RCA multiply/divide unit in typical microprocessor system. Units provide instructions and coded subroutines that microprocessors generally do not have or that require considerable memory and execution time

CDP1855 and 1855C 8-bit multiply/divide units introduced by RCA/Solid State Div, Rte 202, Somerville, NJ 08876, perform 8-bit by 8-bit multiply or 16-by 8-bit divide operations on unsigned, binary operators in 5 μs at 5 V. They are structured to permit cascading identical units to handle operands up to 32 bits. Each unit can do a 16N-bit by 8N-bit divide yielding an 8-bit result plus an 8N-bit remainder. The multiply is an 8N-bit by 8N-bit operation with a 16N-bit result. (N represents the number of cascaded CDP1855s and can be 1, 2, 3, or 4.) Multiply/divide is based on the method of multiplying by add and shift right operations and dividing by subtract and shift left operations.

Features include low power, static CMOS circuits; single, noncritical voltage supply; compatibility with CDP1800 series microprocessor systems; easy interface to general 8-bit microprocessors; and significant increase of microprocessor throughput in arithmetic calculations. Up to four units can be cascaded for 32-bit by 32-bit multiply or 64 by 32-bit divide.

The units are functionally identical and differ only in that the 1855 has a recommended operating voltage of 4 to 10.5 V while the 1855C operates at 4 to 6.5 V. Both are supplied in 28-lead hermetic dual-inline ceramic as well as plastic packages.

Circle 471 on Inquiry Card

Options Added to Logic Development System

Five assemblers and a disc drive have been announced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, as options for its model 64000 logic development system. The relocating macroassemblers support the 6805/6809, 8048/8021, 9900, 1802, and F8/3870 microprocessors. Previously, the system supported on the 8080, 8085, Z80, and 6800. All assemblers operate at 4000 lines/min regardless of source file size. Each can be ordered as a separate unit to modify and extend capabilities of existing systems or as an option to a new system.

The model 7910H 12M-byte Winchester technology fixed drive, a complete standalone unit, includes a self-contained HP-IB (IEEE-488) controller and power supply in a tabletop cabinet. Modular design and sealed environment reduce complexity and increase reliability.

Circle 472 on Inquiry Card

Winchester Approach Backs Up Data Sector By Sector On Floppy Disc

A key feature of the Winchester type 18M-byte hard disc enhancement for Horizon computers is the incremental backup technique developed by North Star Computers, 1440 Fourth St, Berkeley, CA 94710; only data that are modified each day are backed up on the disc, on a sector by sector basis. This keeps costs to a minimum while using the computer's integral 5.25" (13.34-cm) floppy disc drives.

Up to four 18M-byte discs may be connected by daisy chaining with this hard disc system for a total capacity of 72M bytes. Average access time is 78 ms; average latency is 12.5 ms. The

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Recognition was based on the following performance criteria:

ACHIEVEMENT

These features have helped Class IV to achieve championship status.

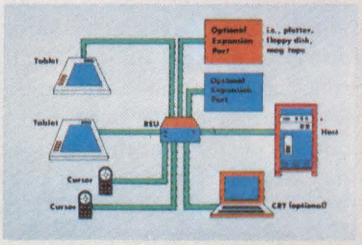
- Dual channel tablet and transducer
- Repeatability to .0005"
- Expansion capabilities
- New technology for greater data stability
- Completely electronic pen with no mechanical switch
- Choice of 4, 12, or 16 button cursor
- "SMART" option available
- Active surfaces ranging from 12"x12" to 44"x60"
- Choice of standard, back-lighted, or rear project surfaces
- External controls for frequently changed parameters

STAMINA

The Class IV is encased in a metal frame with a ruggedized surface to stand up to heavy-duty operation. The environmental requirements for Class IV are as follows:

- Operating temperature 15° C to 40° C
- Storage temperature 0° C to 70° C
- Humidity 0 to 95% non-condensing

VERSATILITY



The Class IV is a flexible system utilizing a *Multibus standard compatible card module with expansion capabilities which allow for dual tablets, dual cursors, and interfacing to additional peripherals such as tape drives, printers, and floppy disks. This exciting new capability now enables the user to develop his own off-line system.

ACCURACY

The Class IV employs microprocessor based technology and uses a patented bidirectional scanning technique to obtain accuracy of .005" and repeatability to .0005".

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For further information please call or write:
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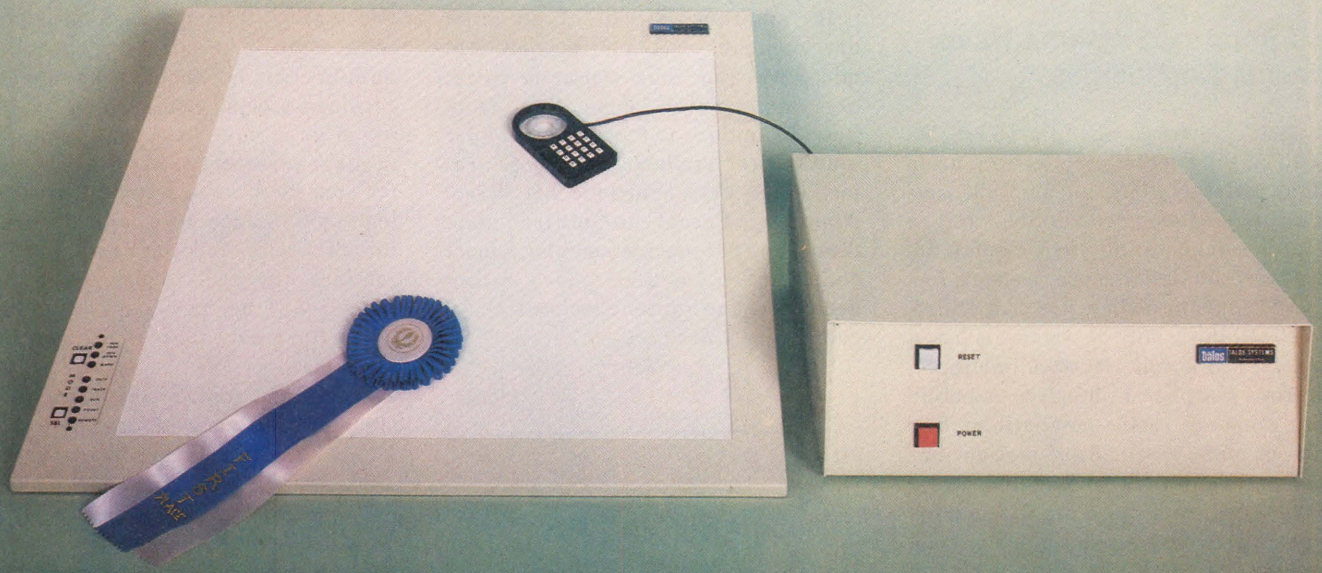
7419 East Helm Drive
Scottsdale, AZ 85260 (602) 948-6540



talos INTRODUCES THE CLASS IV/800 SERIES

CIRCLE 78 ON INQUIRY CARD

HDS-18 hard disc subsystem connects to an existing computer through the standard parallel I/O port connectors.

Components of the drive are the Century Data Marksman hard disc, enclosure, power supply, controller, cables, and software. An interleaved sector format on the hard disc allows multiple sector transfers per revolution. Also included are a bootstrap from the floppy disc controller and error checking/error retry logic.

Software consists of a hard disc operating system (HDOS) and North Star BASIC. Data transferred to or from the disc is placed in a buffer on the disc controller; the operating system then transfers the data from the buffer through the parallel port using an interruptible software routine. Each system includes a resident file manager, backup and recovery system, and a command processor that supports all North Star floppy disc DOS and Monitor commands. The company's BASIC has been modified to work with hard disc files as well as with diskette files.

Circle 473 on Inquiry Card

μComputer Systems Have Pascal Capabilities

R68K-Q systems consist of a 16-bit CPU with 32-bit internal architecture, up to 256k bytes of RAM, a comprehensive Pascal language capability, and a multi-user operating environment. Introduced by Renaissance Systems, Inc, 11760 Sorrento Valley Rd, San Diego, CA 92121, the family of systems is based on the Motorola MC68000 microprocessor. Peripheral interface capabilities include SMD compatible disc drives, IEEE-488 instrumentation bus compatible devices, analog and digital I/O devices, high speed graphic and image display devices, and industry compatible 800- and 1600-bit/in (315 and 630/cm) magnetic tape drives, as well as custom interfaces.

Available software includes an operating system, macroassembler, and RSI Pascal (both interpretive and native code). The operating system is a complete Pascal operating environment including screen oriented editor, filing system, and sophisticated command interface. It supports RSI Pascal and all of its extensions, and can support UCSD Pascal (Regents of the University of California) as a subset. RSI Pascal closely conforms to the Pascal draft standard. Several language extensions, designed to support advanced program concurrency and modularity concepts for the operating system, are also available.

System model -Q1 includes 128k bytes of RAM, 4-channel serial interface board, CRT, realtime clock, 110-char/s line printer, and two double-density floppy disc drives. The -Q2 includes a 21M-byte Winchester disc drive with 15M-byte streamer backup in place of floppy disc drives.

Two versions of a related Pascal interpreter, the MEX68KDM, are available. One is compatible with RSI Pascal operating system, the other with UCSD Pascal. The interpreter requires a minimum of 5k bytes and does not currently support floating point or long integers, although both will be available in the future. Device drivers can also be provided for environments other than the development board.

In addition, a set of program development tools for the MC68000 microprocessor allow a user to create executable native code files from Pascal and/or RSI macroassembler source files. Available programs, written in RSI Pascal, include RSI Pascal compiler, Pascal to native code translator, RSI macroassembler, object code linker, mixed code listing generator, and runtime support.

Circle 474 on Inquiry Card

4-Drive Controller Reads/Writes Single And Double Density

DD-100 is a North Star compatible, dual-density disc controller for any standard 5.25″ (13.34-cm) floppy disc drives, directly replacing the North Star MDS-CTRL-D-ASM. The controller can read and write single- and double-density, with mixed formats on a single diskette.

A disc drive is required that uses a hard sectored, 10-sector format diskette and has a Shugart compatible connector on the drive's electronics card. The drive may be single- or dual-headed, and single- or double-density.

A controller can handle up to four drives for a maximum capacity of 1.44M bytes online. Low power Schottky circuits are used on the board to minimize power requirements and maximize noise immunity. A crystal controlled oscillator generates all clock signals for compatibility with other computers.

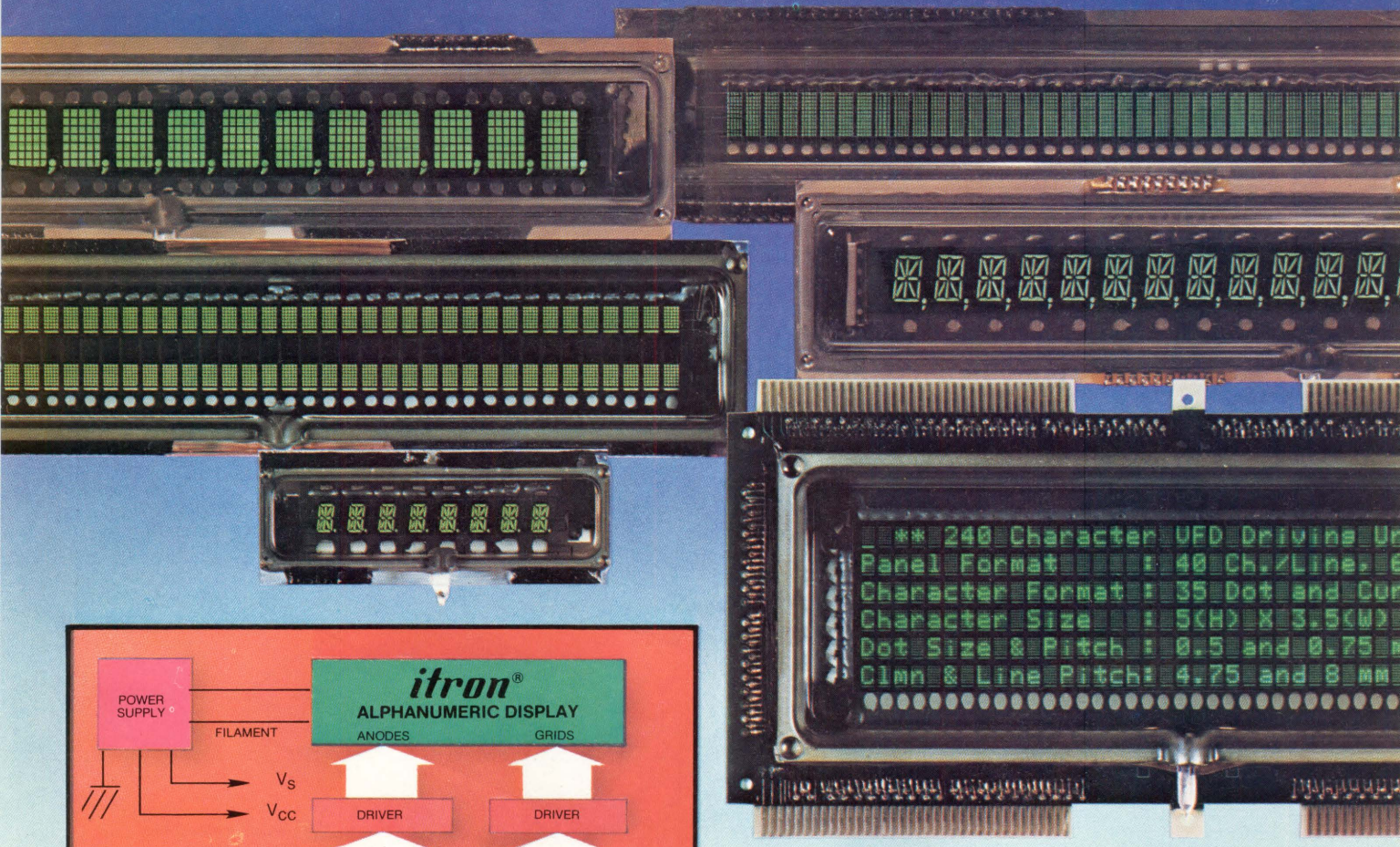
Motor-on times are jumper selected to turn the drive motors on for 4, 8, 16, or 32 s after each access. Standard boot address is E800; an optional DIP switch allows the user to set the boot address at any 1k boundary above 32k.

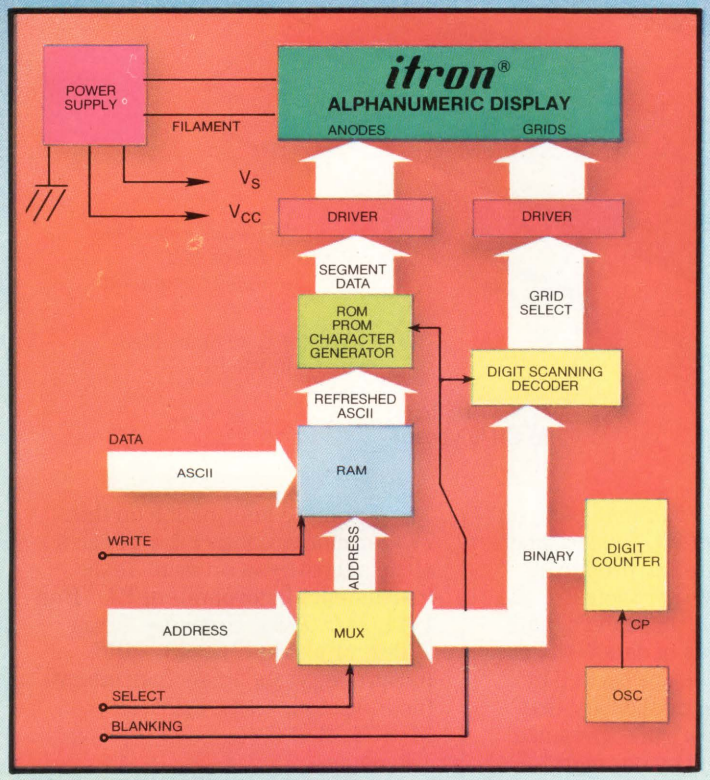
Micro Applications Inc, PO Box 8268, Newport Beach, CA 92660, supplies a copy of MicroDos on a diskette with each controller. The standard version runs on the North Star Horizon computer, but I/O can be modified to work with any computer. Similar to the North Star DOS, the system has added refinements. These features include a built-in rename function, automatic conversion of keyboard commands to upper case, auto start, and disc error message reporting in English. The buffer area doubles as a storage area for boot-up messages. Disc copy, file copy, initialization, and disc compaction routines are built to use the buffer space below the operating system. Fully commented source listings are available.

Single- and dual-drives in cabinets are offered along with the controller. Tandon TM-100 dual-headed drives are used. Dual-drive systems come in a side by side configuration with the drives in a vertical orientation to prevent the drive from resting on the read/write heads when not in use and to reduce dust build-up. A power supply is built into the rear of each cabinet.

Circle 475 on Inquiry Card

Itron Advanced Alphanumerics. They'll put your readouts upfront.





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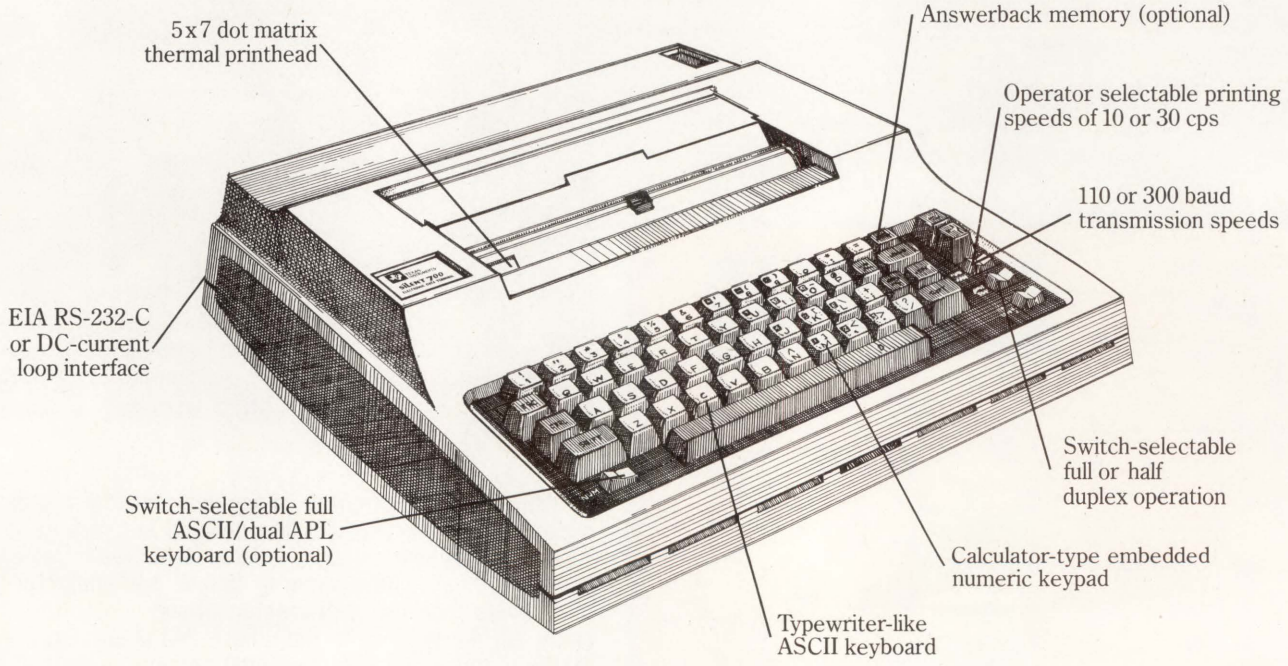

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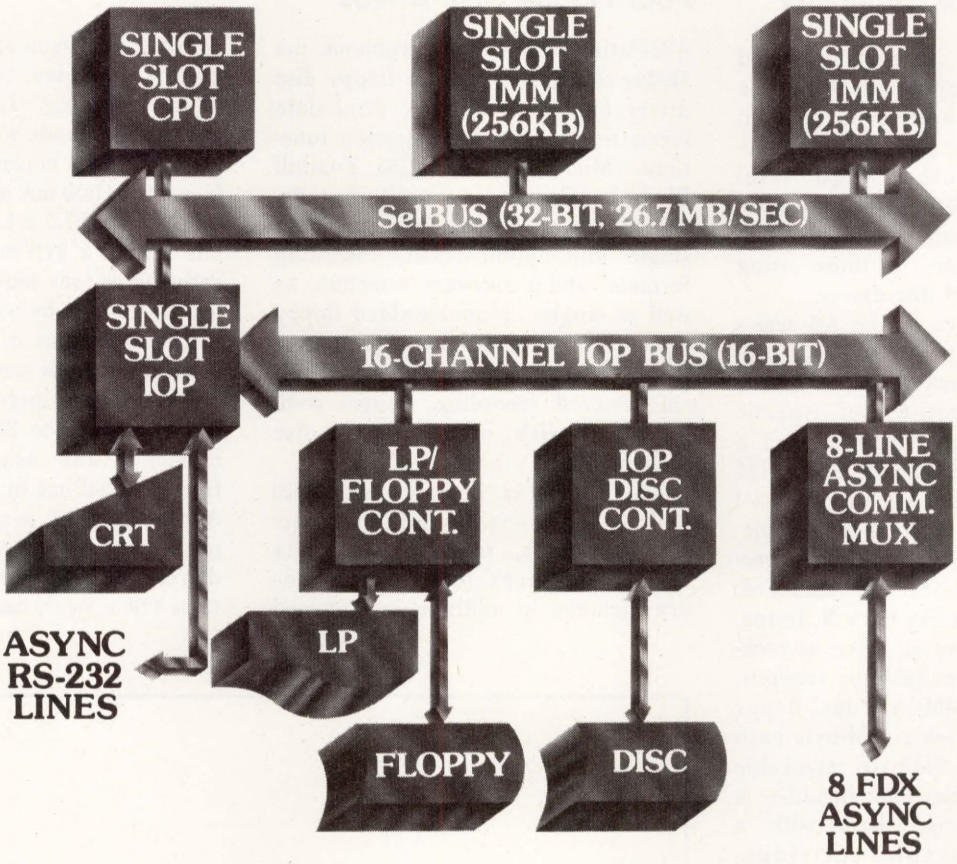

The trouble with most small minicomputers is that they started out as big minis and were simply scaled down. Same functionality. Similar performance. Lower cost. (You've seen the ads). If you're an OEM, you also know those "minis" retained all their complexity. Big mini interfaces. Expensive memory. Costly device controllers. Complex architecture. A big machine, in a cumbersome cabinet. Functionality? Sure. But with all the problems still there for you to solve with your bucks.

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CIRCLE 81 ON INQUIRY CARD

Small Computer Systems Highlight Multi-User, Multiprocessor Capability

General purpose, microprogrammed small business computers feature data handling and software sophistication; large-scale programming may be done in BASIC and other high level languages. The multitasking, timesharing computers span the range from floppy disc systems to those using large capacity hard disc drives.

Common features of the AM series 1011, 1031, and 1051 are a 16-bit processor, two onboard serial I/O ports, one parallel I/O port, 64k of dynamic RAM, floating point hardware, and a realtime clock. Expandable to 1M bytes in the standard chassis, the RAM contains full error correction logic. Eight levels of DMA and multilevel vectored interrupt lines are standard. Alpha Micro, 17881 Sky Park N, Irvine, CA 92714, configures all three as rackmount or standalone tabletop versions.

The 1011 has 2.4M-byte dual floppy disc drives; 1031 uses a 10M-byte hard disc drive with a 5M-byte removable cartridge, and the 1051 includes a 90M-byte hard disc drive with a 15M-byte removable cartridge. Peripheral expansion includes multiple hard disc drives, line and character printers, magnetic tape transports, CRT terminals, and other communication devices.

The Alpha Micro Operating System (AMOS) supports timesharing, multitasking, multiprocessor operations. A comprehensive macroinstruction set is included. Software consists of a macroassembler; the company's versions of BASIC, LISP, and Pascal; AlphaVUE™, a word processing, text editor package; and utility programs. An optional business applications software package is available for the 1031 and 1051.

The existing line of AM 1010, 1030, and 1050 systems, based on the AM 100 16-bit, S-100 bus compatible CPU, have also been packaged to encompass similar configurations. This maintains applications software compatibility between the two computer lines.

Circle 477 on Inquiry Card

STD BUS Compatible Module Controls Up To Four Floppy Disc Drives

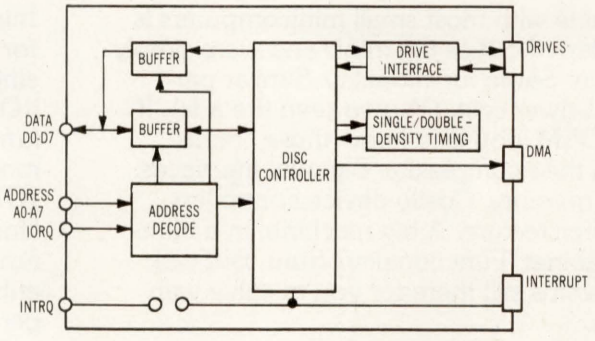
Alleviating mass storage problems, the SB8500 controls up to four floppy disc drives, handling all drive control, data formatting, and error detection functions. Micro/Sys, Inc, 1353 Foothill Blvd, La Canada, CA 91011, has designed the board to support both single- and double-density recording formats, under software selection, as well as single- or double-sided floppy disc drives. Over 4M bytes of storage can be controlled using the latter. IBM soft-sectored recording assures compatibility with other floppy disc systems.

The controller operates with 8085 and Z80 processors. Powerful multisector, multitrack, parallel seek, data search, and track format commands are included in addition to standard home, seek, read, and write commands. Also featured are programmable drive parameters and record lengths.

Automatic peak shift precompensation is provided for double-density mode recording. The controller can operate in a mode with the addition of an SB8341 DMA controller. Requiring 5 V ±5% at 600 mA max, the 4.5 x 6.9 x 0.5" (11.4 x 17.5 x 1.3-cm) board takes one slot in a STD BUS backplane. Addressing as four sequential I/O ports is user selectable by wirewrap jumpers.

Characteristics of the floppy drive interface include step rates from 1 to 16 ms in 1-ms increments, head load timing from 2 to 256 ms in 2-ms increments, and head unload timing from 0 to 240 ms in 16-ms increments. Additionally, it generates all signals necessary to operate four 2-sided drives on single daisy-chained cable.

Circle 478 on Inquiry Card



Meeting STD BUS general mechanical specifications, controller from Micro/Sys handles up to four floppy discs in single- or double-density recording formats

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CIRCLE 82 ON INQUIRY CARD

DS BRIEFS

Precompiler Allows Flexibility for Writing BASIC Programs for Microcomputer Systems—EZ-CODER, a BASIC precompiler for North Star microcomputers, allows mnemonic variables of arbitrary length as well as meaningful labels for line references. All variables, labels, and user defined functions are cross-referenced, and source files are created with a text editor for each modification and manipulation of source codes. A translator, EZ-TRANS, is also available from Demerco Industries, PO Box 2396, Van Nuys, CA 91404. . . .**Software Package Contains Floating Point to ASCII Conversion Routines**—Sorenson Software, Raiffeisenstr 1, D-6104 Seeheim, West Germany, has announced a software package for the 8080/8085 and 6800 microprocessors that features routines to convert floating point numbers from and to decimal ASCII representations, as well as to convert from and to 32-bit integer format to decimal ASCII. The floating point format, but not the conversion routines, is that of the 9511 arithmetic chip. Float to decimal requires from 2.2 to 23 ms; decimal with exponent to float, 1.5 to 11 ms; integer to decimal, 0.5 to 3.9 ms; and decimal to integer, 0.3 to 2.2 ms.

Memory Modules Expand S-100-Bus Microcomputers—Designed for Sol, Cromemco, North Star, and other S-100 bus microcomputers, the CI-S100 memory module, introduced by Chrislin Industries, Inc, 31352 Via Colinas, #102, Westlake Village, CA 91361, can be expanded to 500k bytes with a bank select feature. Users can select up to eight 64k-byte memory cards. Onboard hidden refresh requires no outside intervention. . . .**Assembly Language Development System Adds Z80 Operations**—Relocating macroassembler, interactive editor/assembler, trace debug/monitor, text and linkage editors, and relocating loader are included in the PDS Z80/8080 assembly language development system. Offered by Allen Ashley, 395 Sierra Madre Villa, Pasadena, CA 91107, the system extends Z80 operations to implement four additional byte registers by allowing individual access to the two halves of the index registers . . . .**16-Bit μComputer Provides Individual Board Functions**—Series 990E industrial microcomputer systems offer 20 digital and analog interface boards for process and machine control and other rugged environments. The systems, available from Erni & Co, 3316 Commercial Ave, Northbrook, IL 60062, are compatible with Texas Instruments 990 series microcomputers and 5T1 programmable controllers. They are fully expandable to 4k I/O lines in up to eight chassis.

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Select one of our Series 300 recorders for reliable, low cost data storage...and you get much more. Choose the 300C for its comprehensive search and edit capability to satisfy file management, word processing and data storage/retrieval applications with up to 2.25 Mbytes capacity. Or select the 300D for remote operation with serpentine recording and power fail/auto restart for uninterrupted data acquisition, auto answer for remote data polling over phone lines, and up to 3.86 Mbytes capacity.

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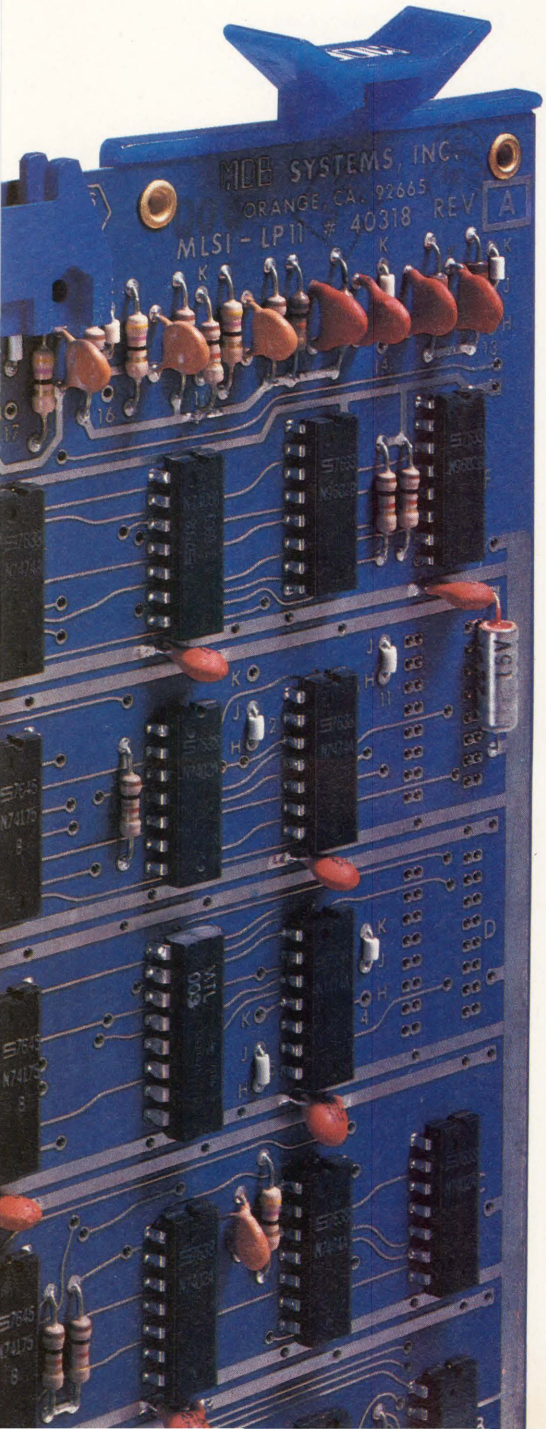

MDB does it! Lets you pick and choose the exact line printer with the exact speed and performance you need for your system. Because MDB interfaces PDP*-11/03 through 11/70, LSI*-11 & 11/23, VAX* 11/780, PDP-8, Nova,** Eclipse,** P-E, IBM Series/1 and HP 2100, 21MX and 1000 to (ready?) Centronics, Dataproducts, Data 100, Data Printer, Documation, Printronix, GE TermiNet,™ Houston Instrument, Innovative Electronics, Okidata, LA180, Florida Data, CDC and many other line printers. That makes over 100 possible computer/printer combinations including the one you need. Long line options for all combinations are available which allow full speed parallel data transmission at distances up to 3,000 feet.

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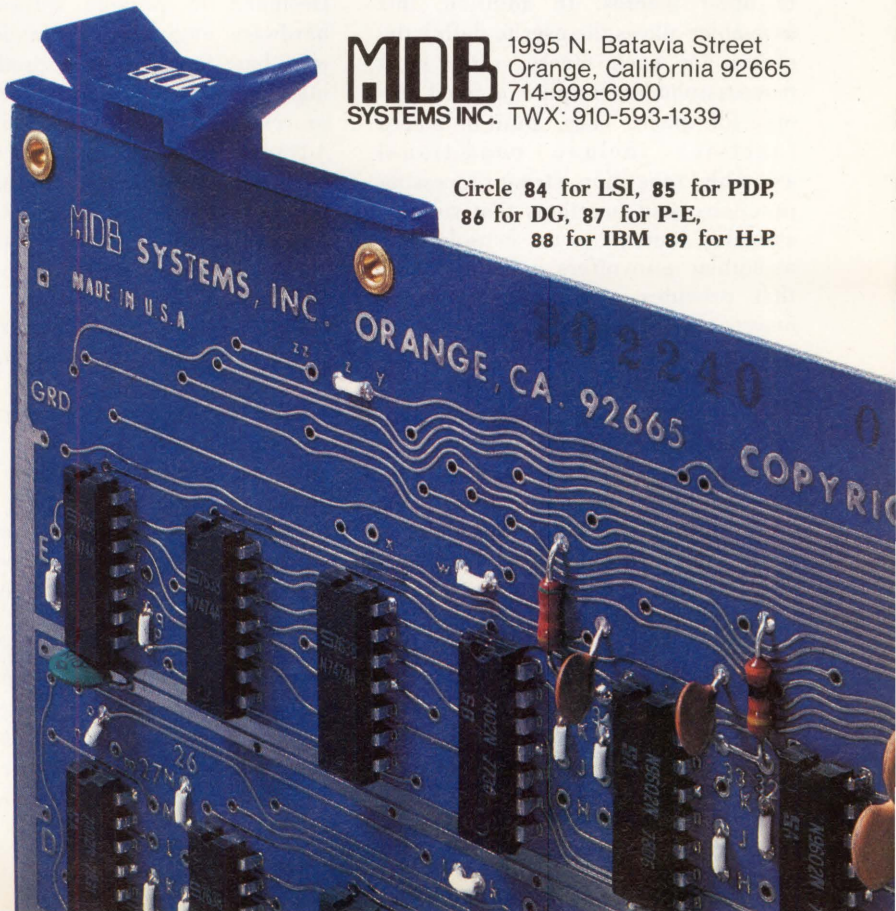

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TWX: 910-593-1339

Circle 84 for LSI, 85 for PDP, 86 for DG, 87 for P-E, 88 for IBM 89 for H-P.

SOFTWARE

Performance Increases Added to Software Development Package

A revised 8086/8088 software development package includes high level assembler with macros and conditional assembly, higher performance PL/M-86 compiler with a high speed floating point math library, and complete linkage and relocation utilities, as well as other software development utilities. It is available from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, at no charge to users of the previous package.

ASM86, the high level assembler, is much more powerful than facilities normally provided in an assembler. Whereas many macroassemblers allow only one macro call per line in the operation field, ASM86 macros can appear anywhere, such as in an argument to other macros. In addition, this assembler allows the user to define the syntax for each macro, while most macroassemblers require a fixed format for macro calls. Built-in macro functions include conditional assembly, repetition, string processing functions, and functions that support assembly time I/O to the console. The assembler also offers a listing mode that provides a complete trace of macro expansion at all levels of nesting.

The revised PL/M-86, a structured high level systems language and compiler created specifically for developing software for the 8086 and 8088, includes an enhanced floating point math library that executes 4 to 10 times faster and produces 2.5 times less code than the previous version. In addition, overall compiler performance has been improved about 10% and it now produces 10% more efficient object code.

Other enhancements include CONV86, a converter utility program that translates 8080/8085 assembly language source code to 8086/8088 source code, and translates all macros and standard assembler controls; LINK86, a utility program that combines separately compiled or assembled 8086/8088 programs into a relocatable module; LOC86, a relocation utility program that allows the user to code modules without having to know the final location of object code in memory; LIB86, a library manager program with new command abbreviations; and OH86, a utility program that converts 8086/8088 absolute object modules to a symbolic hexadecimal format. LOC86 is 1.7 times faster than the previous version and OH86 is 2 to 3.5 times faster.

Circle 479 on Inquiry Card

Pascal Based μProcessor Cross Support Offered As Common Base

Designed to provide software and hardware engineers a common software base for developing products using the S2200, S6800, and S9900 microprocessors, the first of its Pascal based Advanced Support Tools have been introduced by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051. The present software packages run on the Tektronix 8002A MDL, Motorola EXORciser, or AMI MDC-100; by the third quarter of this year a package will be available for the Intel MDS.

The first three software packages are complete cross support systems and use identical assembler formats and directives, text editors, linking loaders, and operating systems. Full macroassemblers support local and global labels. Arithmetic and logic operators include plus, minus, 1s complement, exclusive OR, multiplication, truncating division, remainder division, OR, AND, equal, and not equal.

Simulators for the S2200 have capabilities similar to those of in-circuit emulation but without hardware interaction. Facilities include breakpoint, dump memory, alter memory, single step, set up I/O, and observe I/O. Cross support packages are compatible with other Advance Support Tools soon to be announced, including an AMI Pascal compiler and in-circuit emulators for the S2200, S6800, and S9900. Cross support packages are available for the 8080 and Z80 microprocessors.

Circle 480 on Inquiry Card

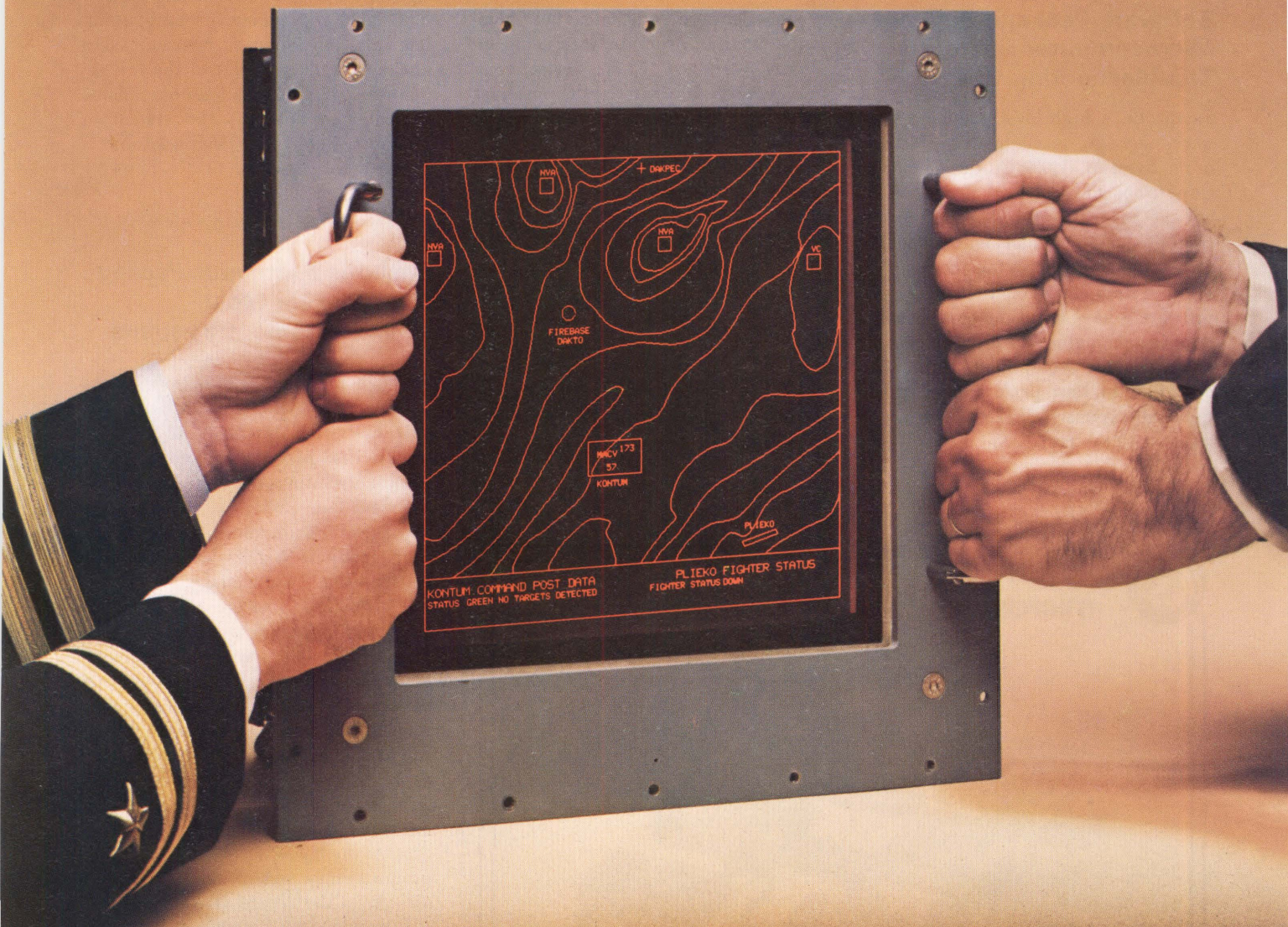
Software Package Aids 6502 Microprocessor System Development

The TEC microprocessor development aid introduced by Thorson Engineering Co, 6225 76th St SE, Snohomish, WA 98290, is a hardware/software package for the Rockwell AIM 65 microcomputer and microprocessor 6502 systems. It consists of a programmer for 2716 type EPROMs and firmware for the AIM 65 that will cause the microcomputer to simulate a full-duplex terminal through the onboard serial port, supporting bit rates up to 2400 baud; allow object files in microprocessor assembler format to be downloaded through the terminal simulator to microcomputer RAM at speeds up to 2400 baud; program 2716, 2758, TMS 2516, or equivalent EPROMs; copy EPROM contents into microcomputer RAM; and verify EPROM contents against microcomputer RAM.

Software editing and assembly can be performed on a timesharing system, minicomputer, or other computer that has sufficient memory and file storage resources for efficient assembly. The object code can then be downloaded to the microcomputer for realtime debugging or EPROM programming for the target system. The user can call subroutines from an executive program to perform automatic sequencing through a downloading and programming task. A source listing of firmware is provided

Circle 481 on Inquiry Card

Until today you couldn't get your hands on a plasma display without the terminal. Today you can.



Introducing Interstate's PDA 300 Plasma Head. Tough, bright, with more than 10,000 hours of service life.

Now you have the flexibility to design in a rugged, long-life plasma display in tough system environments with Interstate's flat-panel PDA 300 Display Head. It displays alphanumerics/graphics, and is TTL compatible for easy interface. Inherent memory eliminates display refresh, and the unit is totally digital with no analog circuits. It has a thin profile and is designed to help meet your system RFI/EMI requirements. Optional equipment includes a touch panel, variable brightness control, rack mount, and remote-mounted power supply.

Today, for your best buy decision, consider how the PDA 300 designs into your display system. Deliverable Immediately.

For more information, call or write Don Poulos, Product Manager, Interstate Electronics, 1001 East Ball Road, P.O. Box 3117, Anaheim, CA 92803. (714) 635-7210.

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CIRCLE 24 ON INQUIRY CARD

SOFTWARE

Software Package Reduces Microcomputer System Troubleshooting Costs

Fastprobe, a high level language software package, is claimed by Millennium Systems, 19020 Pruneridge Ave, Cupertino, CA 95014, to dramatically cut the cost of troubleshooting microcomputer systems. Designed specifically to work with the company's MicroSystem Analyzer, the interactive software is said to fill the gap between nonprogrammable testers and costly automatic test equipment, forming a combination that performs the functions of expensive ATE systems at a fraction of the cost.

The package runs on a host computer linked to the analyzer using industry standard RS-232 serial communication. It controls the analyzer operation to stimulate the circuit under test and to guide the operator automatically to the fault in the system under test. Programs include software development processes (editing, data entry verification, learn mode operations, and update operations) and execution with routine library files.

Three technologies—in-circuit emulation, signature analysis, and time domain analysis—are used to troubleshoot microprocessor based systems. A guided probe feature offers seven major modes of operation: field service assumes solder runs to be correct and does not probe all node ends; manufacturing checks even the continuity of the solder runs; retry backs up probing operations to repeat any test; no-probe permits various points to be skipped during a test sequence; bus-breakdown prioritizes the enable signals on the IC bus to catch a problem early and reduce probing; jump lets an experienced operator skip ahead to a desired part of the test sequence; and feedback loop breakdown automatically permits the system to diagnose a fault in a feedback loop.

Circle 482 on Inquiry Card

Realtime Arithmetic Package Available for Most μC Development Systems

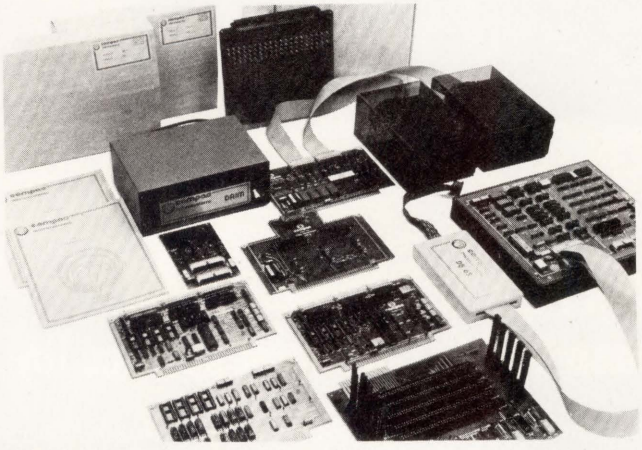
MART, a modular arithmetic realtime package for 8080/8085 and Z80 based systems with AMD-9511A or 9512 arithmetic processors, contains a library of routines that may be selected as needed to configure an optimized set of runtime functions. Macroinstructions facilitate higher level language constructs and are compatible with Intel PL/M. The package simplifies interaction between application programs and the arithmetic device through a multilayered hierarchical architecture. Application programs may interface directly with any level of control at any time without causing system or device corruption. At the highest level, application programs may submit expressions in ASCII representation. At the lowest level, an application program may submit an instruction directly to the device driver.

Introduced by Systems & Software, Inc, 2801 Finley Rd, Suite 101, Downers Grove, IL 60515, the software package fully exploits AMD-9511/12 capabilities by allowing asynchronous operation at the hardware level through interrupt control and by arbitrating the use of the arithmetic device by multiple programs. The package applies equally to the implementation of high level languages as well as single- or multitasking dedicated applications. It is available in source form for use with the more popular microcomputer development systems and minicomputers with cross assemblers.

Circle 483 on Inquiry Card

compas microsystems

6500 USERS



We offer the most complete line of 6500 support tools available — both hardware and software. Our CSB family of single board computers get your project running quickly. The DAIM floppy disk system turns your AIM 65 into a serious development system. The DB/65 provides the debug system you have been looking for. Cross assemblers are available for many popular computers plus CSL/65 — *the* high level language for the 6500 family.

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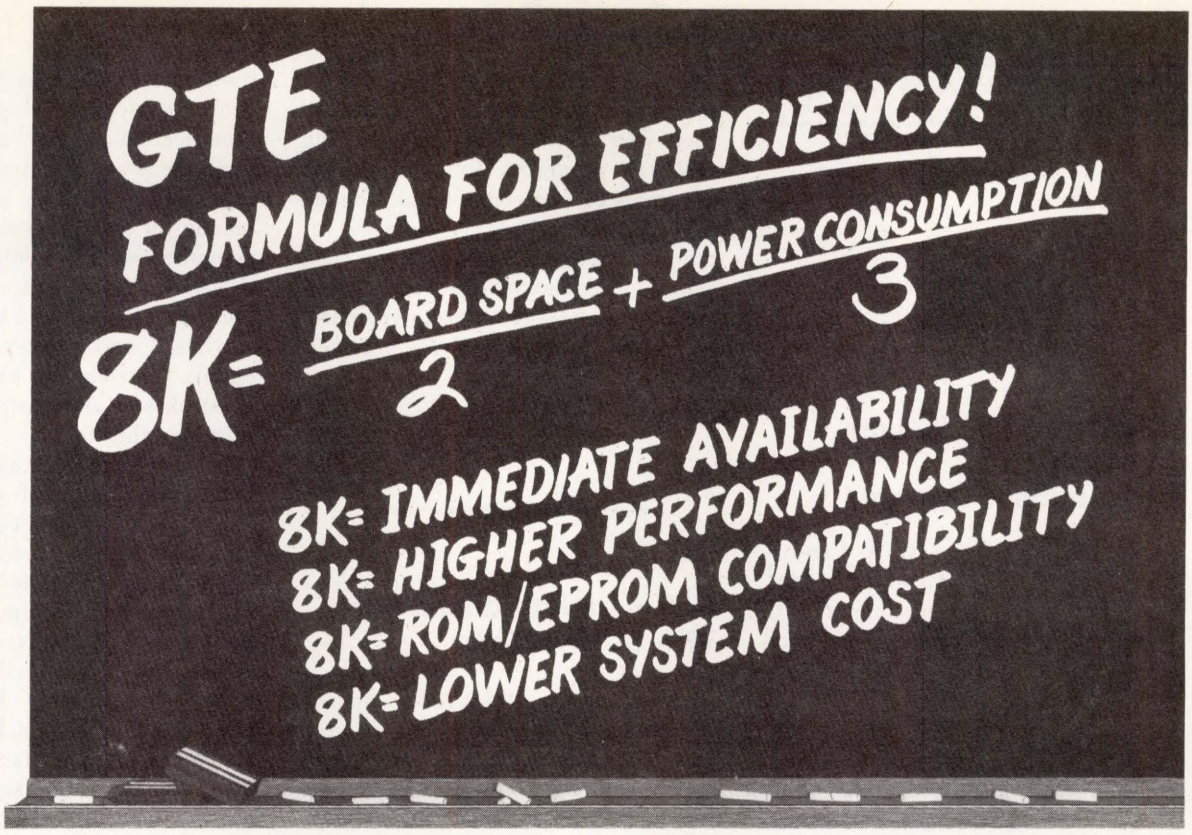
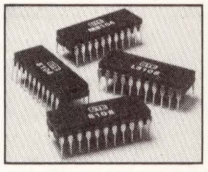


That's right! If you're still using 1K or 4K Static RAMs...you're wasting valuable board real estate and using too much power.



But never worry... GTE's 8K Static RAMs allow you to reduce board space by 1/2 and power consumption by 2/3.

Anyway you measure it, that's a formula for efficiency!

When GTE Microcircuits talks about 8K Static RAMs, people listen. The reason...because we're talking about a family of standard products that are *available NOW!* In fact, GTE's proven 8K process technology (based on 5 years of 2114 production experience) not only offers significant power savings, but guarantees ultimate reliability and lower system cost...plus the convenience of an 8-bit bus I/O structure. And what's more, GTE's 8K is the only Static RAM with an announced second source.

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Anyway you measure it, GTE 8K Static RAMs will provide you a proven formula for memory efficiency.

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8K Static RAMs

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CIRCLE 91 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

SOFTWARE

FORTRAN-80 Version Available for Development Systems

GenRad/Futuredata, 6151 W Century Blvd, Suite 1124, Los Angeles, CA 90045, has announced an agreement with Microsoft, Inc of Bellevue, Wash to offer a version of Microsoft FORTRAN-80 that is compatible with the firm's 2300 series development system. A compiler for 8080, 8085, and Z80 based systems, FORTRAN-80 supports all features of ANSI Standard FORTRAN X30-1966 except complex data types. Several extensions are allowed. The compiler outputs assembler language source.

This agreement extends the use of the company's development systems to users who wish to write or use existing FORTRAN programs. In addition, the programs can be compiled and linked to programs written in assembly or other languages. The resulting code can be executed using development system resources or on prototype hardware using the company's in-circuit emulators.

Circle 484 on Inquiry Card

Software Introduced For TRS-80 Systems

Three products— the VTOS 3.1 operating system, VTOS 3.1 reference manual, and VTOS 3.1 system kernel—have been announced by Virtual Technology, Inc, PO Box 340069, Dallas, TX 75234, for the Radio Shack TRS-80 model I level II microcomputer system. The operating system includes modifications to Format, Backup, and Chain utilities to improve service for single-drive users, modifications to the Patch utility that facilitate system maintenance by the user, added Memory and Alloc commands for quicker memory and disc resource management, and several drivers for cassette tape, TRS-232 interface, screen print, and blinking cursor. Keyboard and printer speed buffers enable type-ahead without missing keystrokes or allow printing while performing other tasks.

The reference manual describes the detail functioning of each command and operating system call and provides an insight into the theory of operation upon which the I/O software and DOS were designed. Information on creation of multiple tasks and compatible device drivers is provided for the experienced assembly language programmer. The system kernel contains all file maintenance facilities required by an assembly language program, but has no operating system utilities. It is available to software vendors under a license agreement. □

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FAST COMPANY!

PRIAM'S MATCHED SET OF WINCHESTER DISC DRIVES

PRIAM's high-performance, low-cost Winchester disc drives speed up throughput and expand data storage from 20 megabytes to 154 megabytes. And a single controller can be used to operate 14-inch-disc drives with capacities of 33, 66, or 154 megabytes or floppy-disc-size drives holding 20 and 34 megabytes. So it's easy to move up in capacity, or reduce package size, without changing important system elements or performance.

High Performance and Capacity at Low Cost

Fast, linear voice coil positioning gives you high system throughput, without traditional high cost. Track-to-track positioning time is less than 10 milliseconds for all models, and average positioning takes just 50 milliseconds. PRIAM's use of IBM 3350-level Winchester disc technology gives you high capacity at amazingly low cost.

Simple, efficient design makes both types of PRIAM drives reliable and economical. Brushless DC motors eliminate belts, pulleys and mechanical brakes. They also save you money and let any PRIAM drive operate anywhere in the world.

Compact Sizes, Light Weight

Small size and light weight make PRIAM drives a cinch to fit into your systems. The space-saving DISKOS 3350, 6650, and 15450 weigh a mere 33 pounds. The DISKOS 2050 and 3450 have exactly floppy-disc-drive dimensions and weigh only 20 pounds. Compact, light steel rod frames permit easy flow of air in the system, improving system reliability. In the 14-inch drives, the optional power supply can be fully enclosed within the disc drive assembly.

High Reliability

PRIAM's proprietary head-disc assembly air system assures long-term reliability by maintaining positive pressure at the spindle-bearing seals. Data reliability is guaranteed by fully servoed head positioning; dedicated servo tracks eliminate the positioning errors to which other low-cost drives are vulnerable. Microprocessor control reduces component count and cost and improves reliability and flexibility.

Easy Interfacing

PRIAM's low-cost serial data interface is the same for both 8-inch and 14-inch drives, and all PRIAM drives include data separation. To make interfacing easier than ever, PRIAM's optional Parallel Data Interface provides functions that permit interfacing directly to the I/O bus at the byte level. It controls up to four drives, and provides serialization and deserialization of data, disc formatting, sector buffer, polled or interrupt operation, defect mapping, overlapped commands, implied seek, selectable sector sizes, and resident microdiagnostics. A simple interface to the CPU is all that's needed, eliminating tedious and expensive controller development.

SMD Interface

If you have an SMD controller in your system, you can move quickly to Winchester technology performance, reliability and economy by using PRIAM's optional interface. It matches up conveniently with existing Storage Module interfaces and it is available with all of the following PRIAM models.

THE PRIAM LINEUP

Model/Disc Size	Capacity	Transfer Rate	Size
DISKOS 3350 (14")	33 Mbytes	1.03 Mbytes/Sec	7" x 17" x 20"
DISKOS 6650 (14")	66 Mbytes	1.03 Mbytes/Sec	7" x 17" x 20"
DISKOS 15450 (14")	154 Mbytes	1.03 Mbytes/Sec	7" x 17" x 20"
DISKOS 2050 (8")	20 Mbytes	1.03 Mbytes/Sec	4.62" x 8.55" x 14.25"
DISKOS 3450 (8")	34 Mbytes	1.03 Mbytes/Sec	4.62" x 8.55" x 14.25"

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CIRCLE 93 ON INQUIRY CARD

LSI IMPLEMENTATION OF THE DATA ENCRYPTION STANDARD

Milan Momirov

Fairchild Camera and Instrument Corp
464 Ellis St, Mountain View, CA 94042

In January 1977, the National Bureau of Standards adopted, as a standard, a data encryption algorithm that had been developed at the IBM Watson Research Center. This algorithm, now known as the Data Encryption Standard or DES*, specifies a method for enciphering data blocks to maintain privacy. The need for security becomes particularly acute whenever data are saved on a storage medium that is accessible through a computer system, especially a large timesharing system used by many persons or as part of a computer network. Similar security problems occur in the transmission of voice or data over a common carrier net.

The common approach to encryption is to use a method that is basically well-known but has a vast number of variations that are selected by a key. A straightforward substitution, for example, where a given character of text is replaced by another, is effective, even though it may be widely known that this method is being used. Since there are so many different ways of making substitutions, the process of cracking the cipher would be quite involved without knowledge of the substitution pattern or key. When one character is simply substituted for another, frequency of occurrence eventually leads to deciphering the code, but more elaborate substitutions, such as replacing groups of characters, make the process of cracking much harder.

Another approach is the transposition cipher, where the original characters are retained but are scrambled in location. Again, the number of ways to scramble a 20-character string is huge, making the task of deciphering without the key formidable. A third encryption method, a product cipher, combines both transposition and substitution to generate a code even more resistant to cracking.

Use of a key as an approach to encryption relies little upon secrecy, since only the key need be kept secret while the algorithm may be publicly known. Furthermore, the key may be changed as often as necessary—every month, every day, or every transmission. The advantage to large scale use of the same algorithm is that two arbitrary parties can communicate securely simply by agreeing on the key or keys to use. Adoption of an encryption algorithm standard by the National Bureau of Standards**, therefore, aids the overall growth of generalized secure communication networks.

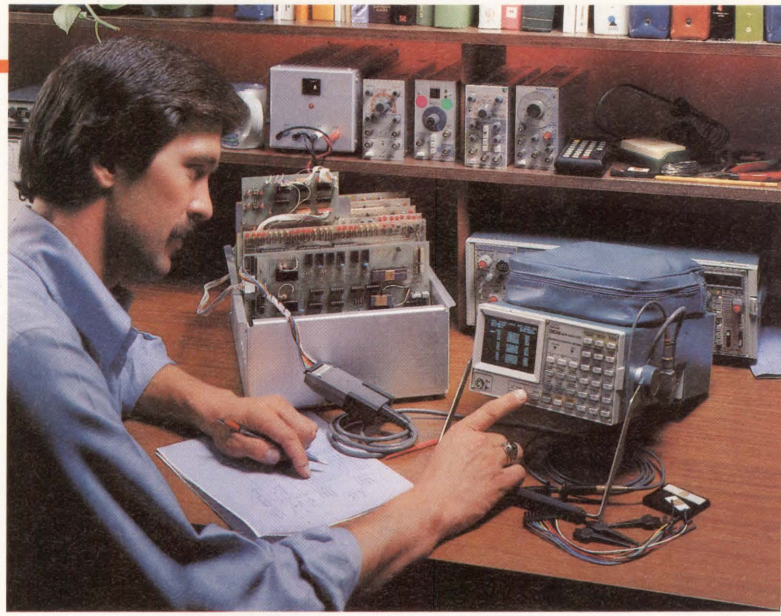
*Copies of the *Data Encryption Standard* (FIPS PUB 46) are available from the National Technical Information Service, U.S. Department of Commerce, 5285 Port Royal Rd, Springfield, VA 22161.

**Copies of the *Compatibility Requirements for Use of the Data Encryption Standard* (Federal Standard 1026) can be obtained from General Services Administration Specifications Sales, Bldg 197, Washington Navy Yard, Washington, DC 20407.

308 DATA ANALYZER

Big power in a small package.

The 308 operates in four modes: parallel state, parallel timing, serial state and signature analysis.



The 308 Data Analyzer. From Tektronix.

The new 308 Data Analyzer packs an impressive array of logic analysis capabilities inside its trim, 8 pound (3.6 kg) frame. For instance, it operates in the serial and signature modes as well as parallel state and timing. And samples both synchronously and asynchronously up to 20 MHz. With a variable voltage threshold that covers all logic families in addition to TTL.

Two separate memories, acquisition and reference, allow automatic data comparisons. If there's no data difference, the sampling process is repeated until a discrepancy appears. And the acquisition memory can be automatically searched for any given word.

Word recognition can be up to 25 bits and includes an external output to trigger other instruments. And the trigger itself can be delayed up to 65,535 clock pulses past the trigger point. The 308 features a latch mode (5 ns), a memory "window" to let you closely examine portions of the memory and state tables which are displayed in binary, hex and octal.

The 308 Data Analyzer, from Tektronix. Performance? Uniquely versatile. Size? Conveniently compact. Price? Exceptionally reasonable.

If you're interested, contact your local Tektronix field office, or write us at:

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The DES Algorithm

The DES algorithm is a product cipher that is easy to implement and offers a high level of security. It operates on a 64-bit block of data, with a user specified 56-bit keyword, to generate a 64-bit block of enciphered text. The strength of the algorithm lies in the 56 bits of key, with $72(10)^{15}$ possibilities for the keyword, making exhaustive search of all possible keys an awesome task. In addition, the need to process eight bytes of data in one encryption or decryption excludes the possibility that an intruder could, by observing and storing pairs of enciphered and deciphered data, eventually compile enough pairs to partially decipher text by table lookup. To decipher 64 bits of information by table lookup alone would require a table with 2^{64} entries, each of 64 bits.

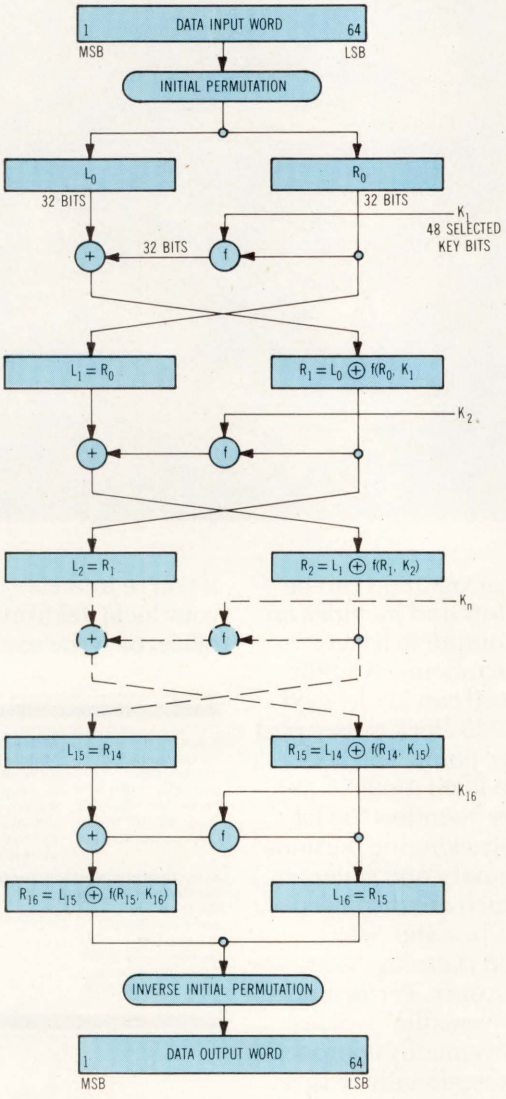

Fig 1 Flowchart outlines logic of DES algorithm. Process involves 16 cycles of permuting, XORing, keyword shifts, and bit swapping

In the implementation of the DES algorithm (Fig 1), the 64-bit input block is first passed through an initial permutation IP, followed by 16 complex key-dependent computations, and finally through IP^{-1}, the inverse of the initial permutation. Deciphering uses the same key as enciphering, but the algorithm is performed in reverse order.

IP is a straightforward transformation in which the 64 bits of the input word are ordered into eight 8-bit rows of a matrix. The output is formed by taking eight 8-bit columns from the matrix to provide a new 64-bit word. This word is split into two 32-bit words by taking even columns to the left register, L_0, and odd columns to the right register, R_0.

In a parallel operation, the 64-bit keyword is transformed in a row-column operation similar to IP. The least significant bits of each byte are parity, appearing in the first column of the resulting matrix, and are dropped to leave a 56-bit word. A total of 48 of these bits are selected for K_1.

At node "f" (in Fig 1), K_1 and the output from R_0 are brought together in a cipher function, which is illustrated in Fig 2. The 32-bit output from R_0 passes through an expansion function, E, in which each 4-bit input group is expanded into a 6-bit group by including a bit from each of its adjacent 4-bit groups. This provides 48 bits, which are exclusive ORed to the selected 48 bits of the key to form eight 6-bit addresses to eight selection tables (ROMs). The resulting output, P, provides 32 permuted bits, which are exclusive ORed to the output of L_0 and sent as input to R_1 (see Fig 1). Furthermore, the untransformed output of R_0 is directed to the input of the next left register, L_1.

This permuting, ORing, and swapping is done 15 more times. The final output undergoes a reverse initial permutation to become an output data word.

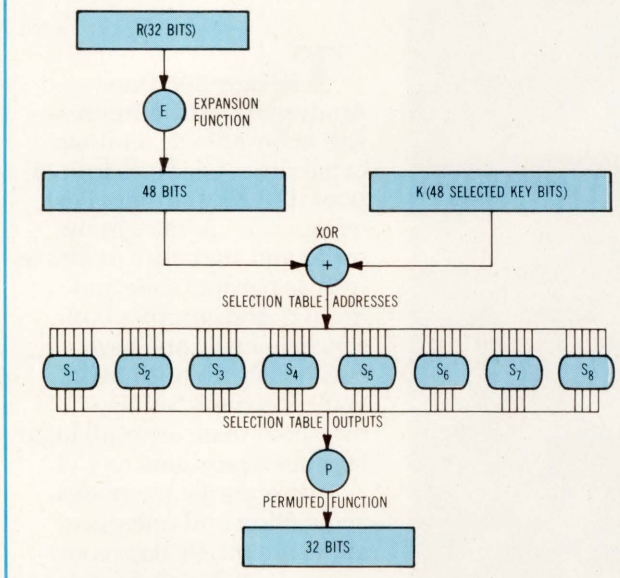

Fig 2 Cipher function combines permuted data and key bits in XOR function to address selection tables. Address redundancies prevent code cracking through attempt to work backward from outputs

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During encryption, the 54-bit keyword is left-shifted a predetermined amount, and a next set of 48 bits is selected for K_2. Sixteen such shifts generate the keywords K_1 through K_{16}. During decryption, the keyword is then right-shifted 16 times to develop sequential keywords.

The lookup tables are publicly known and do not change, but since part of their inputs come from the 56-bit key, the tables alone will not give the solution to decryption. Since the selection function tables have more inputs than outputs, attempting to work backward from an output results in an exponentially growing number of different possible combinations of data and keys that would produce the same output.

LSI Implementation

Implementation of the DES algorithm in software alone is feasible only for the lowest speeds of communications. Most practical data communication and storage applications require that encryption and decryption be performed in hardware. The algorithm is well-suited for implementing in custom IC chips that can be conveniently mounted at the front ends of communication systems. Since the announcement of the standard, a number of manufacturers have developed such products.

The Fairchild 9414 data encryption set consists of four similar 40-pin isoplanar integrated injection logic (I^3L^{TM}) LSI devices (Fig 3). Major elements of one of the chips, shown in Fig 4, include a pair of data registers, four 8-bit shift (key) registers, control logic, and two 64-word by 4-bit ROMs.

A keyword consists of 64 bits in 8 bytes. Bit 8 of each byte is parity, leaving 56 bits of key. Bits 1 through 4 go to both chip 1 and 2, and bits 4 through 7 go to chips 3 and 4. The four chips together store the 64-bit plain text or cipher text word. These chips have separate data inputs and outputs, allowing the block of data to be processed to be input as the previous block is being output.

The key register is capable of hold, left shift (encipher), or right shift (decipher) by one or two positions, as required by each of the 16 rounds of the algorithm. ROMs (64 x 4) in each device implement the S-boxes of the algorithm. The masking of the ROM codes and the key bits selected as ROM addresses are the major differences among the four devices. As shown in Fig 3, a set of eight output signals (P_{1-8}) and inputs signals (F_{1-8}) are interconnected between chips to implement the permutation function P of the algorithm. An additional set of outputs P_X and P_Y and inputs F_X and F_Y are used to interconnect the chips as required for expansion of 32-bit half-words to 48 bits, involving redundant bit usage.

Implementation of the Algorithm

Initial permutation is accomplished in the chip set by the manner in which the data are loaded. The D_{IN0} input of chip 1 loads bit 1 of each byte; D_{IN1} of chip 1 loads bit 2 of each

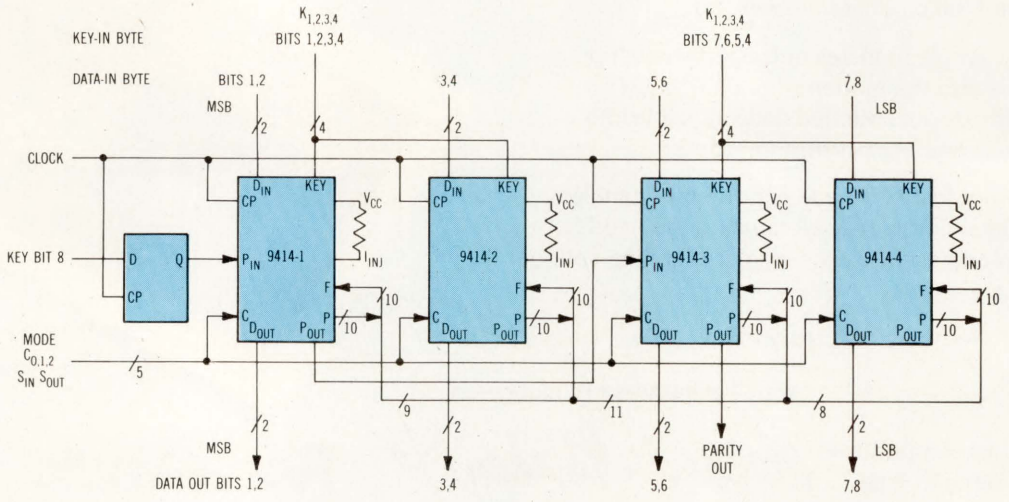

Fig 3 Encryption set uses four LSI chips. Key features include low power consumption, high speed, and TTL compatibility

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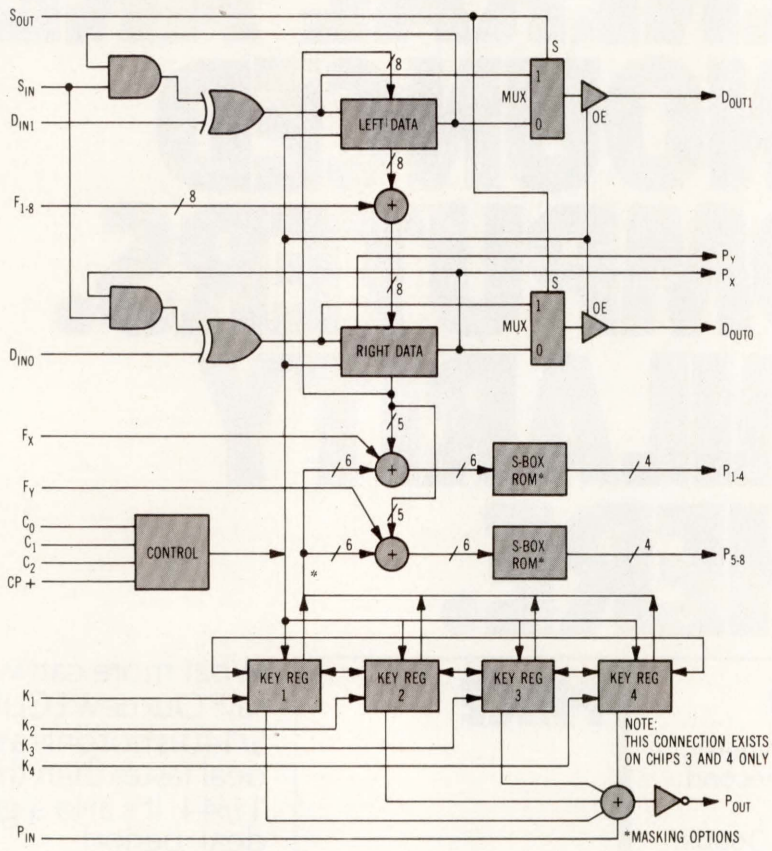

Fig 4 Block diagram of 9414 circuit. Implemented in isoplanar integrated injection logic, chip contains 6 registers, 2 MUXs, control logic, and pair of 64 x 4 ROMs

byte; D_{IN0} of chip 2, bit 3 of each byte, etc. After eight clock cycles, the four registers receiving data bits 2, 4, 6, and 8 of each input byte comprise the L_0 block of 32 bits in permuted order within the four devices (see Fig 1). The four registers receiving bits 1, 3, 5, and 7 of each byte hold the R_0 block. Therefore, each chip slice contains one byte each of the L_0 and R_0 blocks. Further shifting of the bits and extracting outputs from the right end of each byte implements the inverse permutation IP^{-1}.

The 28 key bits in the first half of the key permutation function are duplicated in the key registers of 9414-1 and 9414-2, while key bits in the second half occupy the registers of both the 9414-3 and 9414-4. In each device, key register 4 holds the last four bits of both halves of the key permutation function. Each of the 16 iterations involves a left rotation (encipher) or right rotation (decipher) of the key registers. During the key shift schedule, chips 1 and 2 bypass the right half of key register 4, and chips 3 and 4 bypass the left. This results in the key alignment returning to its original position after a total of 28 shifts from the 16 iterations. Thereafter, the key need only be loaded upon power-up or when a new key is desired.

An internal 1-bit right realignment is required by a change from encipher to decipher after the key has been entered. This, and the reverse left realignment for decipher to encipher, are performed by the control logic, which must be stable prior to the loading of the last data byte. Whenever clocked at the same time as a load key, the data registers will all fill with logic 1s.

Summary of Chip Characteristics

The data encryption set described here uses primarily integrated injection logic to perform the DES algorithm in a 4-chip set. Substitution tables are implemented as TTL ROMs to obtain the highest throughput; TTL at the outputs ensures full TTL compatibility. This mixture of technologies is designed for fast implementation of the algorithm. The 5-MHz clock frequencies are fast enough for all standard asynchronous and most synchronous transmissions. Eight clock cycles load a 64-bit data block, and 16 clocks perform the algorithm for 64 bits in 24 cycles of 200-ns clocks, or a 13.3-MHz bit rate. Power consumption per chip is 0.5 W from V_{CC} for the TTL ROMs and outputs, and 0.175 W at the injector pin for a 0.675-W total.

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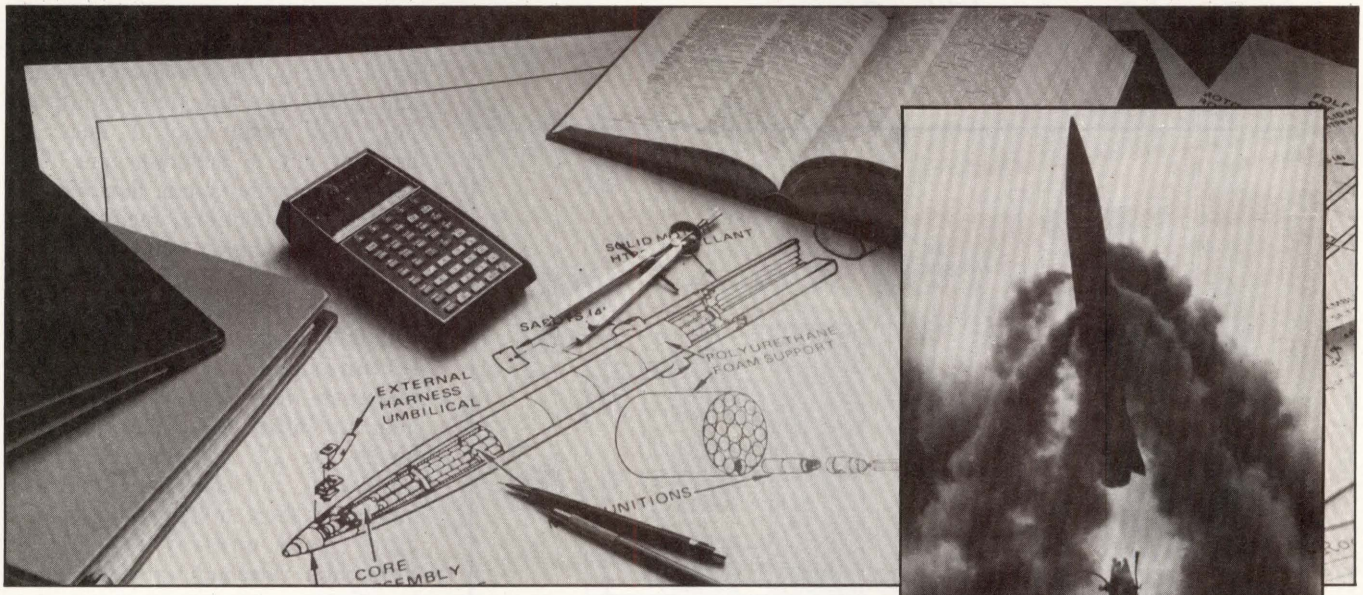

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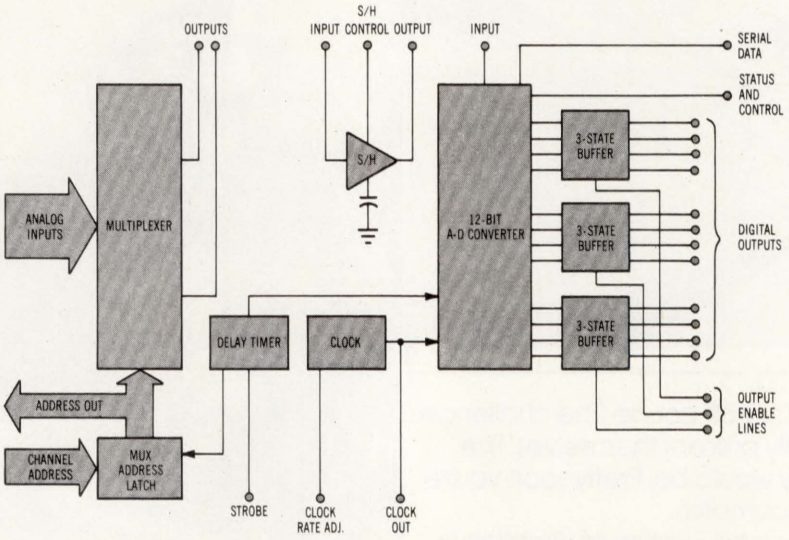


16-channel, 12-bit hybrid data acquisition system. Burr-Brown's SDM854 system operates in 8-channel differential or 16-channel single-ended mode

Providing a ±0.012% max linearity error and 12-bit resolution, with accuracy of ±0.024% at a 27-kHz throughput rate, a complete data acquisition system from Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734, is contained in a 2.2 x 1.7 x 0.22" (55.9 x 43.2 x 5.6-mm) ceramic package. The SDM854 accepts analog inputs over a ±10-V range. Low level inputs can be accommodated by connecting an external instrumentation amplifier to the output of the multiplexer and to the input of the sample/hold amplifier.

This miniature system is said to offer all the functions available in large modular systems. Included are an analog multiplexer, address register, sample/hold, 12-bit ADC, delay timer, clock, voltage reference, and 3-state output buffers that simplify 4-, 8-, and 16-bit data bus interfacing. The device can be configured to accept either 8-channel differential or 16-channel single-ended signals and can be expanded almost without limit with external multiplexers.

Two CMOS ICs make up the analog multiplexer. Pin interconnects are used to select single-ended or differential operation. In single-ended operation the MUX can be used in a pseudo-differential mode by connecting an external amplifier's inverting input to common remote signal ground. Channel selection is made by an internally latched 3- or 4-bit binary word, for differential or single-ended operation, respectively.

A complete standalone circuit, the sample/hold amplifier features buffered output, 10-μs acquisition time, and 100-ns aperture time. Input, output, and mode control lines are brought out to separate pins. This allows maximum system flexibility for performing functions such as automatic gain ranging, with no loss of aperture time.

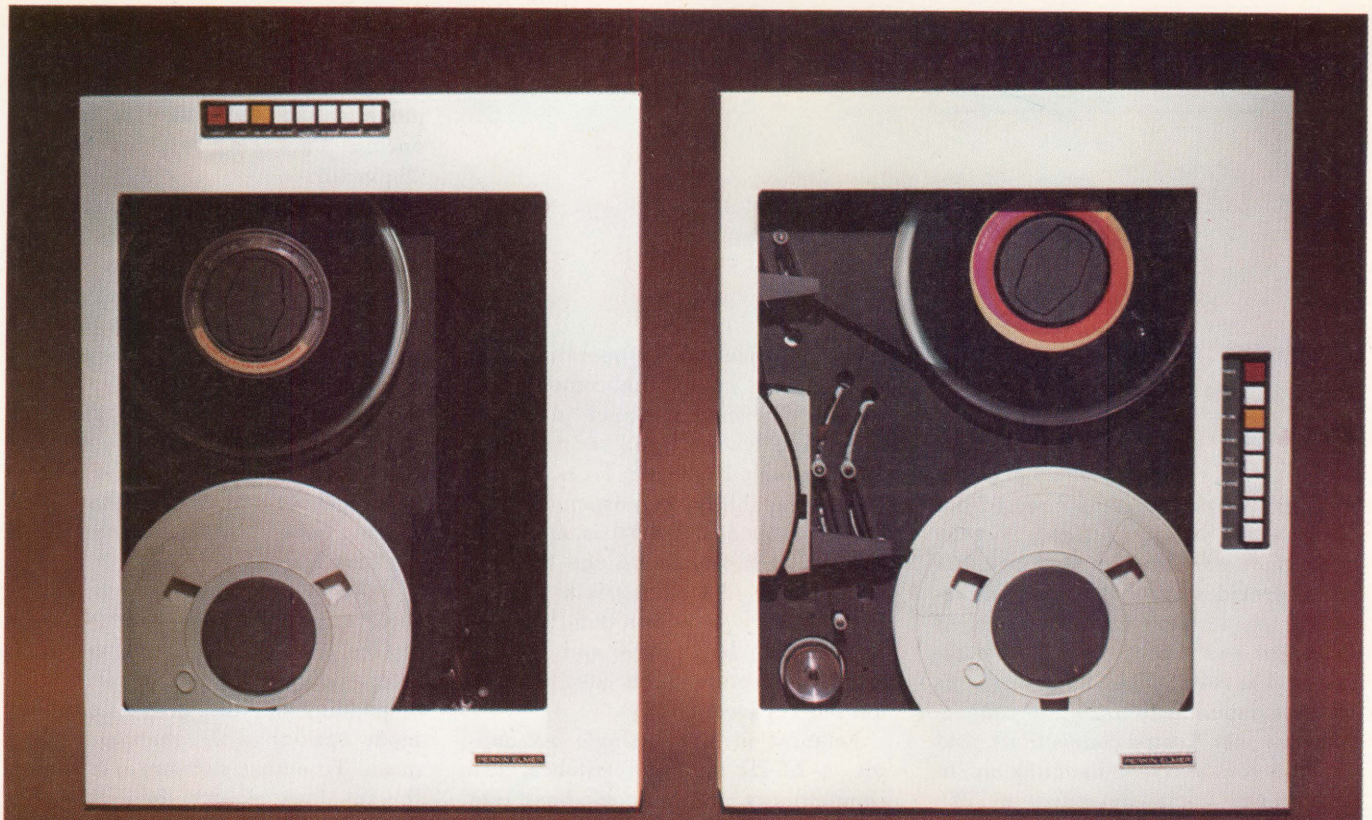
The ADC is a 12-bit, 25-μs converter with 0.01% linearity error. Its features include positive and negative reference voltage outputs, external gain and offset adjustments, straight binary or 2's complement output, serial data and clock outputs, status output, a short cycle feature, and a clock rate control for higher throughput rates at lower resolution or accuracy.

Settling time for the MUX and sample/hold circuits is provided, before conversion begins, by the delay timer. The delay is adjustable over a wide range by use of an external resistor or capacitor. This allows for longer settling time if an external instrumentation amplifier is used and is operating at high gains, or shorter settling time for lower resolution operation.

Up to 2 in² (13 cm²) of board space is saved in the acquisition system by a design that allows circuit traces to run under the package without added insulation or special treatment. The proprietary 80-pin quad-inline ceramic (alumina) substrate design offers total isolation and a heat sink efficiency that allows the chips to be mounted directly on the single substrate. Temperature specifications provide for operation over a range from −25 to 85 °C. Low cost is emphasized by the manufacturer, with the price in 100s as low as $165.

The device's high input impedance, $5 \times 10^9\ \Omega$, is desirable in 10-V signal applications. Internal circuitry is protected when input signals range up to 20 V higher than the unit's positive or negative supply—an advantage in electrically noisy industrial environments.

Circle 501 on Inquiry Card



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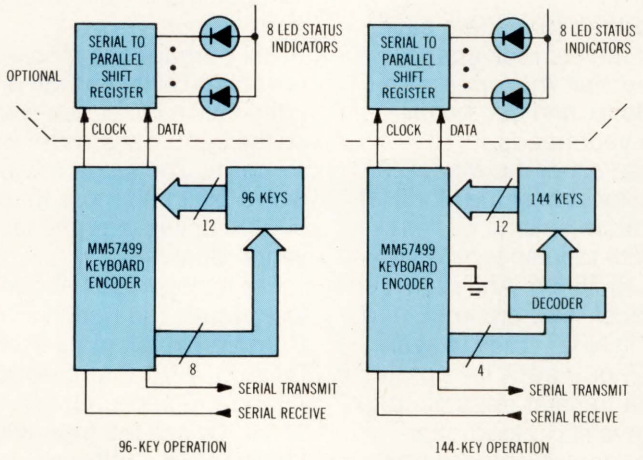
Monolithic Encoder Interfaces Between Keyboard and CRT

A single NMOS integrated circuit from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, provides all of the functions required to interface between a detached keyboard and a cathode ray tube terminal. The MM57499 keyboard encoder reduces the usual 18 to 24 interconnections to only 5 wire connections, and has the capability of handling up to 144 keys. It is designed to aid manufacturers of systems incorporating large terminals or word processors.

For a typical 96-key operation, the chip requires no external components. It provides simple, direct interface, with serial transmit and receive, to a 12 x 8 matrix keyboard. To expand to 144-key capability, an inexpensive 4-12 line decoder (DM74LS154) is attached, and a direct connection can then be made to the 12 x 12 matrix keyboard. If the user requires less than 96 keys, or a number between 96 and 144, no extra connection is needed at the unused key locations.

Features include a single 5-V supply, a 2.5-kΩ max on-resistance, TTL compatibility, and an onchip baud rate generator. An onchip oscillator utilizes the standard 3.58-MHz color burst crystal. The circuit provides full upper and lower case ASCII codes, with numeric pad and function encoding onchip. Packaging is provided in a 28-pin DIP.



Two options for National Semiconductor's MM57499 serial keyboard interface chip. In 96-key mode, std 8 x 12 matrix keyboard is required, X-Y matrix lines are connected directly to keyboard, and pin 21 is used as strobe line. When 144-key mode is used, external 4-12 line decoder interfaces between chip and keyboard, while pin 21 is strapped to ground to activate 144-key codes

The IC interfaces to a standard X-Y keyboard matrix. Strobe lines walk down the keyboard X matrix lines (or external decoder) and are detected on the Y inputs if a key is pressed. Diode isolation is required in the key matrix to guarantee that if two keys and a control key are simultaneously pressed, the keyboard interface will process the correct key sequence. This maintains 2-key lockout and ensures that an erroneous control, shift, or repeat key is not encountered.

Valid key closures are detected by recurring strobe-scan events. The interface strobes rows of the matrix at rates unique to the configuration (depending on either the 96- or 144-key mode option) of the number of keys down. To ensure debounce, it verifies the key down closure, then recognizes the key as valid and processes the ASCII code. Before the next key is processed, the previous key must have been up for three scan times. If a continuing dwell on the key is encountered, the interface will go into an automatic repeat mode until the key is detected to be up.

In many terminal applications a certain word or phrase is required periodically. It may also be necessary that indent spacing or a predetermined tab sequence be recalled. This device has the capability of storing a programmable phrase up to 14 characters long. The 14 strokes, stored for later recall by a single keystroke, are not restricted to key characters, but can also be control codes.

A 400-word/min burst rate (typ) makes the device fast enough to keep up with the most recent CPUs. With the addition of an external DM74164 shift register, it also has the capability of driving eight status indicators to show power on/off, system error, self test, programming mode, etc. Status is an 8-bit data word and is clocked into the status latch 0.178 ms after detection of a stop bit.

Absolute maximum ratings require that the voltage at any pin (relative to ground) stay between −0.5 and 7 V. Allowable ambient temperature limits are 0 to 70 °C in operation and −65 to 150 °C in storage. Power dissipation must not exceed 0.75 W at 25 °C nor 0.4 W at 70 °C.

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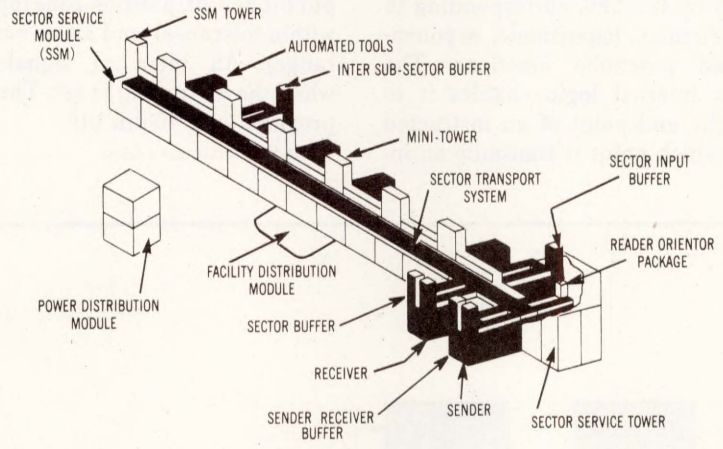


IBM's manufacturing line sector, QTAT, produces LSI circuits in highly automated operation. Sector diagrammed here is on order of 100′ long. Facility uses eight parallel sectors and includes 100 automated tool subsystems

International Business Machines Corp, Data Systems Div, East Fishkill, Rte 52, Hopewell Junction, NY 12533, now employs a highly automated computer controlled manufacturing line to facilitate the production of LSI circuits for inhouse utilization in products such as the System/38 and 4300 processor series. The manufacturing line, designated QTAT (quick turn around time), consists of more than 100 automated tool subsystems grouped into eight sectors.

Silicon wafers measuring 3.25″ (82 mm) in diameter are partially completed, before entering the manufacturing line. In the line, electron beam tools define interconnections on three layers of components within the chips, and automated tools then perform the remaining manufacturing processes. The finished chips are 4.6 mm on a side, and incorporate up to 706 circuits, 3 levels of wiring, and approx 100 I/O connections.

Wafers are moved from one tool to the next by a sector transport system (STS) that uses air jets within enclosed tracks, minimizing friction and contamination. Inter-subsector buffer stations (ISSB) provide wafer storage at strategic locations on the line.

Other capabilities of the line include automatic wafer identification through laser scanning of serial numbers, a wafer routing system operating under software control, and computer terminals for monitoring processing operations and for providing access to all levels of computer process controls. Automated data collection and analysis are used to control precision process parameters such as temperature, pressure, deposition rates, and voltages. A software program formats the data in chronological order with identifying information such as wafer serial number, operation performed, tooling sector, time, and other appropriate production data.

The capability for fast turnaround that is provided by this manufacturing line is seen by this manufacturer as an essential response to the increasing demands in the industry for accelerated production of an ever greater variety of circuit components. As an example of this proliferation, it is noted that the facility where QTAT is employed now designs and produces a hundred times more bipolar chip part numbers than it did five years ago. Very flexible design and manufacturing systems are seen as a necessary adaptation to this trend.

Quad Differential Drivers and Receivers Meet Bus Standard

A series of interface circuits from Texas Instruments, Inc, PO Box 225012, Dallas, TX 75265, optimized for bus applications, meets the EIA RS-422 standard. These quad-differential line drivers and receivers provide balanced multipoint data bus transmission at data rates up to 10M bits/s over distances as great as 4000′ (1.3 km). The SN75172 driver and SN75173 receiver are pin compatible with the AM26LS31 and AM26LS32 devices, respectively, while the SN75174 driver and SN75175 receiver are pin compatible with the MC3487 and MC3486.

These devices offer an interface for exchange of serial binary information between a host computer and various pieces of peripheral equipment such as an input terminal or a printer. Each of the products features high positive and negative common mode range,

operates from a single 5-V supply, has 3-state outputs, and presents low power requirements. Up to 32 driver/receiver pairs can be connected to a common bus.

Significant features of the drivers include standby power of 53 mW/channel, and high output impedance with power off (or in 3-state) over a common mode range from 12 to −7 V. Positive and negative current limiting, in addition to thermal shutdown, automatically protects the drivers in case two or more are simultaneously enabled.

The receiver circuits feature ±200-mV input sensitivity over a common mode range of 12 to −12 V. They also have 50 mV of hysteresis for increased noise immunity and 12-kΩ input impedance (min). These features make the driver-receiver pairs ideal for party line applications in noisy environments. All four devices are characterized for operation from 0 to 70 °C and are offered in 16-pin plastic or ceramic DIP packages (N and J suffix).

Circle 503 on Inquiry Card

NMOS Chip Controls 16 x 64 Video Display

Interfacing easily to any computer or microprocessor, a cathode ray tube controller, designated the CRT 96364, controls all the functions required for a 16-line x 64-char video display. Functions include CRT refresh, character entry, and cursor management. An internal oscillator produces the composite sync output. The device can also serve as a standalone video processor through such standard functions as erase page, erase line, and erase to end of line.

There are two versions of this chip from Standard Microsystems Corp, 35 Marcus Blvd, Hauppauge, NY 11787. The model having an A-suffix generates a 50-Hz vertical sync, while that having a B-suffix generates a 60-Hz vertical sync. Implemented in COPLAMOS® N-channel silicon gate technology, each requires a 5-V power supply at less than 100 mA. Units are available in 28-pin DIPs.

Circle 504 on Inquiry Card

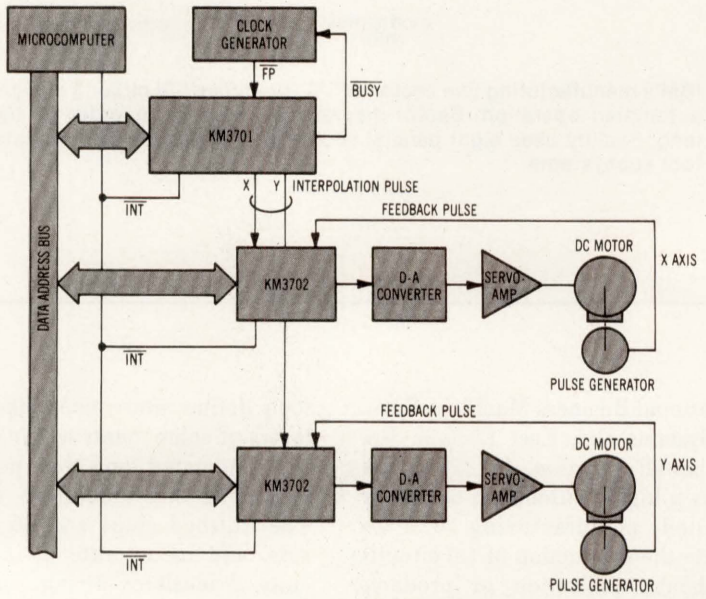
μComputer and 2 Chips Provide System for Numerical Control

Designed for use in numerical control equipment, two CMOS LSI chips produced by Toko America Inc, 5520 W Touhy Ave, Skokie, IL 60077, can interface directly with 8-bit microcomputer. The resulting combination constitutes a complete numerical control system. Charactristics include TTL compatibility, single 5-V power supply, and utilization of a bidirectional data bus with open drain output.

One of the chips is the KM3701, an interpolation pulse generator. It generates interpolation pulses, as instructed by the CPU, corresponding to linear, circular, logarithmic, exponential, and parabolic functions. The device's internal logic enables it to detect the end point of an instructed job, at which point it transmits an interrupt signal ($\overline{INT}$) to request a new job. It also has the capability of controlling the pulse distribution rate, which, for linear interpolation, is 10^5 pulses/s with a 1-MHz clock. Packaging is provided in a 28-pin DIP.

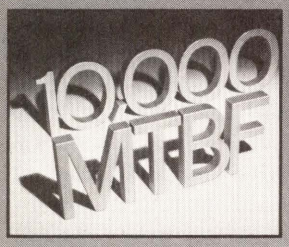
The companion chip is the KM3702, a servomotor controller, which contains two 24-bit up-down counters—a command counter and an error counter. It accepts the interpolation pulses from the generator chip and feedback pulses from a servomotor, and then transmits a digital output (8 to 16 bits), specifying the correction, to a DAC, whose outputs go through a servo amp to drive the motor. This circuit can accept conditions designated by the CPU establishing a saturation zone (D-A output bit depth), position zone (operation within tolerance), and alarm zone (over range). An interrupt signal occurs when the alarm flag is set. The chip is provided in a 40-pin DIP.

Circle 505 on Inquiry Card



Numerical control system from Toko configured for 2-axis position control. For n-axis control, system would use n servomotor control chips (KM3702), with single interpolation pulse generator chip (KM3701) required for each pair of control chips

RELIABILITY. IT'S WHAT MAKES FUJITSU THE WORLD'S LARGEST MANUFACTURER OF OEM WINCHESTERS.



That's right! Fujitsu produces more Winchester technology disk drives for the OEM market than any other manufacturer in the industry. The reason for this success is the unequalled reliability of Fujitsu products.

For instance, Fujitsu's M228X Winchester drive delivers more than 10,000 MTBF power on hours of high performance. That's 40% better than the industry standard. And the M228X is fast: 6ms track-to-track (27 ms average) access time. With this kind of performance, up to 169 megabytes of unformatted storage, and Fujitsu's competitive pricing—there is no other choice! Optional head-per-track capacity of 655 kilobytes also available with this series.

80 and 50 MB cartridge drives with SMD interfacing

Fujitsu's advanced technology does not stop at Winchesters! The two front-loading cartridge drives with SMD capability shown here, have statistics only Fujitsu could guarantee. Like access times of 6ms track-to-track (30 ms average), and a reliability factor of over 6,000 poh MTBF. That's 50% better than the industry standard.

And whether you order the M2211 (80 MB) or the M2201 (50 MB) drive you can say goodbye to data staging. Plus you get a servo/track record system that assures the cartridge interchangeability you need. With features like these it's no wonder Fujitsu's got the world on a platter.

For technical information, (outside California only) phone toll-free 800-538-8175. For sales and service, or evaluation unit, contact: Fujitsu America, Inc., 2945 Oakmead Village Court, Santa Clara, CA 95051. Phone 408-985-2300, Telex 357-402, TWX 910-338-0047.

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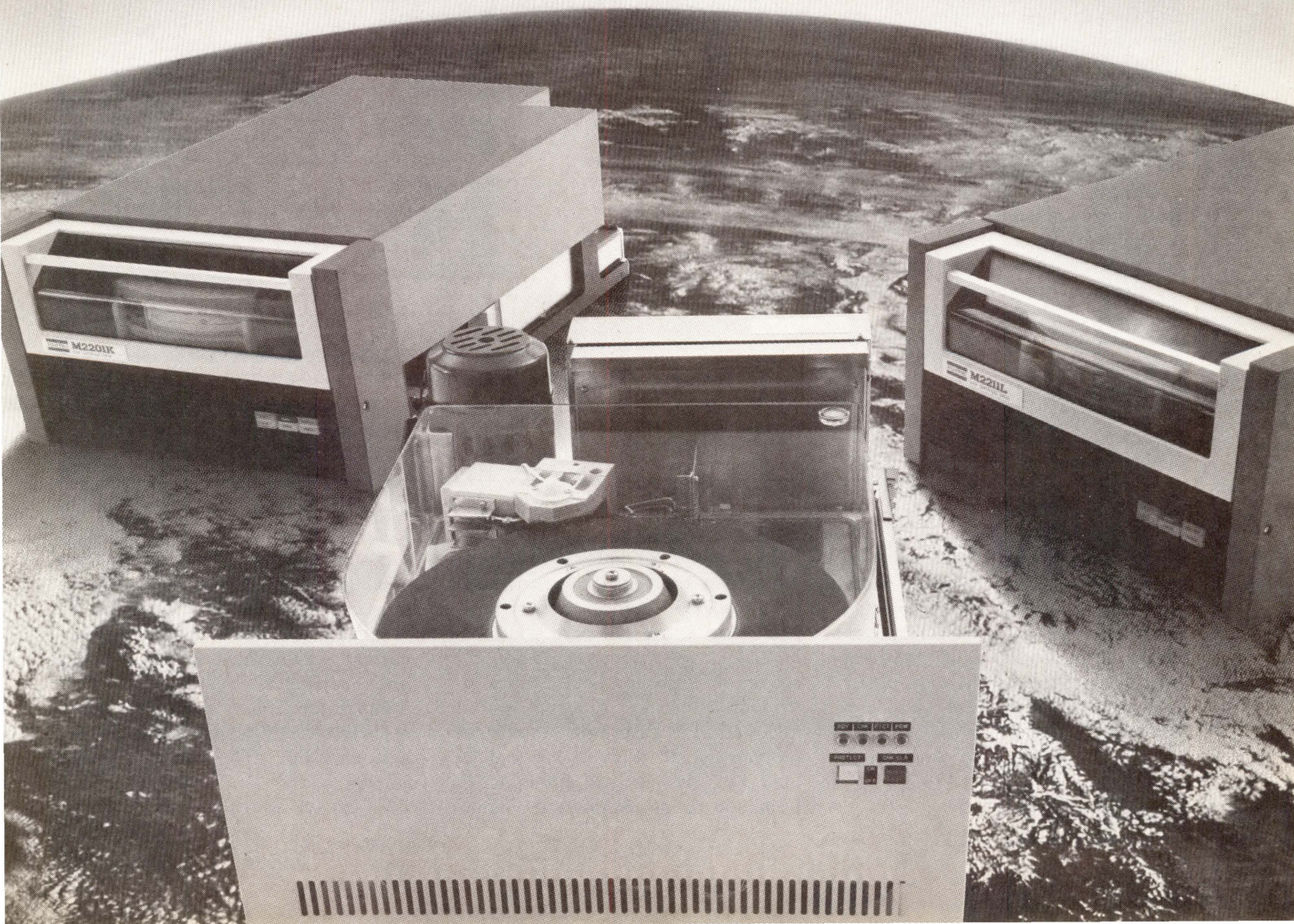


Hybrid Module Contains 14-Bit S-D Converter

A 14-bit synchro to digital or resolver to digital converter from ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716, utilizes two custom designed monolithic chips in a single hybrid module. The HSDC-8915 Monobrid™ series is available in two accuracy grades. The standard grade provides a max error of ±5.27 minutes of angle (±4 LSB) and the high accuracy version provides a max of ±2.64 min (±2 LSB). These accuracies, which include quantizing error, are maintained under all static and dynamic conditions at speeds up to 2 r/s. Because the conversion is ratiometric, the accuracy is not affected by carrier amplitude variation.

The converter will accept broadband inputs of either 360 to 1000 Hz (400 Hz nom) or 47 to 1000 Hz (60 Hz nom). Output angle is in natural binary code with parallel positive logic and is TTL/DTL/CMOS compatible.

Principal features include a 3-state output in two bytes (of 8 and 6 bits), and a transparent latch that allows the converter to keep tracking even while an inhibit is being applied. Also featured are an analog velocity signal, error voltage outputs, solid state signal and reference isolation, broadband input, and accommodation to nonstandard line to line voltage levels.

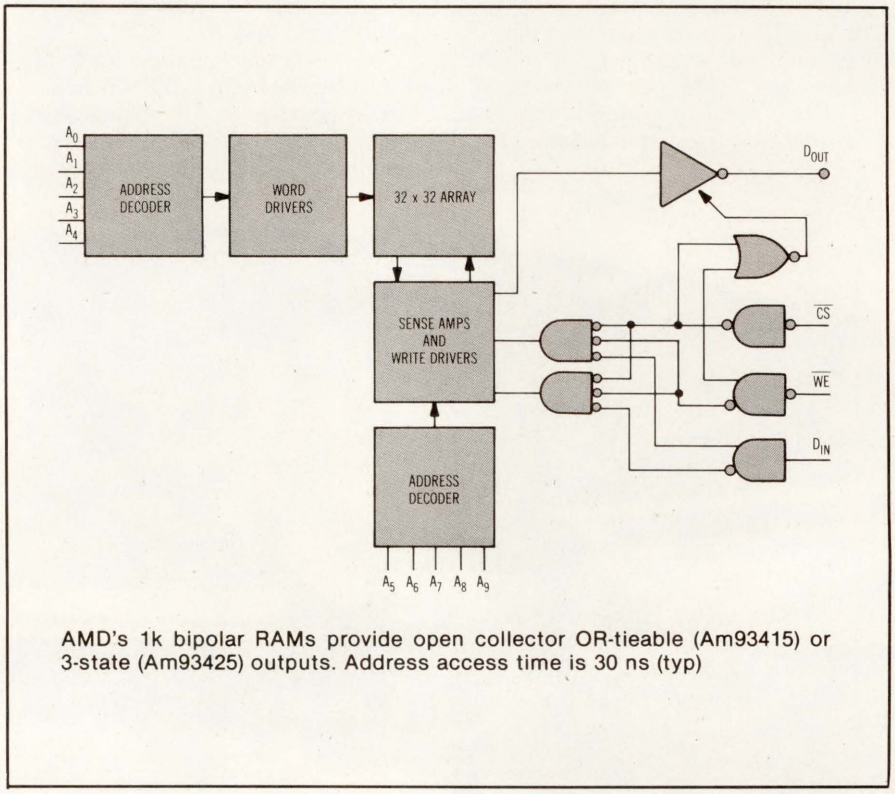
Only one 15-V power supply is needed for the converter, and the voltage may vary from 11 to 16.5 V with no degradation in performance. All logic inputs and outputs are buffered to accommodate any external TTL or CMOS logic level between ±4.5 V and the supply level.

These units are processed to MIL-STD-883 and are designed to operate under severe environmental conditions. They find uses in multiplexing and microprocessor interfacing, particularly in remotely located and hard to access equipment where low power requirements, small size, and high MTBF are critical. The converters are packaged in standard 36-pin, double-width DIPs.

Circle 506 on Inquiry Card

1k Bipolar RAMs Offer Very Fast Access

Two fully decoded, bipolar, 1024 x 1-bit random access memories have been announced by Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086. The RAMs utilize Schottky diode clamped transistors in conjunction with internal ECL circuitry to achieve a typical address access time of 30 ns. They find use in high speed control and buffer memory applications.



AMD's 1k bipolar RAMs provide open collector OR-tieable (Am93415) or 3-state (Am93425) outputs. Address access time is 30 ns (typ)

The Am93425 provides a 3-state output, while the Am93415 provides an open collector output. Both devices employ an active low chip select ($\overline{CS}$) input for easy memory expansion and active low write line ($\overline{WE}$). During the write cycle, output circuitry is preconditioned to eliminate the write recovery glitch. With $\overline{CS}$ low and $\overline{WE}$ high, both devices read out stored information on the noninverting output (D_{out}). When not reading, D_{out} is in a high impedance state.

Worst case delay from address to output is 45 ns for commercial parts and 60 ns over the full military temperature range. The devices undergo 100% reliability assurance testing in compliance with MIL-STD-833. Both memories are plug-in replacements for the like numbered Fairchild parts.

Absolute maximum ratings require that supply voltage (relative to ground) remain between −0.5 and 7 V. The dc voltage applied to outputs for high output state must stay in a range from −0.5 to V_{CC} max, and dc input voltage must stay between −0.5 and 5.5 V. Maximum allowable output sinking current is 20 mA, and allowable dc input current is −30 to 5.0 mA. Temperature must remain between −55 and 125 °C, ambient, under bias, and between −65 and 150 °C in storage.

Circle 507 on Inquiry Card

Shugart's fixed disk back-up solution. You can get started today.

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The low cost solution. We've solved the cost problem, too. First you get the lowest cost per Megabyte fixed disk drives in the industry. Next, add a realistically priced intelligent controller and either a floppy drive or a 1/4-inch streaming tape drive. Back-up media costs are minimal and you only need a single power supply. And design costs are low because you get started faster. The Shugart solution. An intelligent approach to back-up that combines fast start-up with significant system savings. If this is what you've been waiting for, contact your nearest sales office today.

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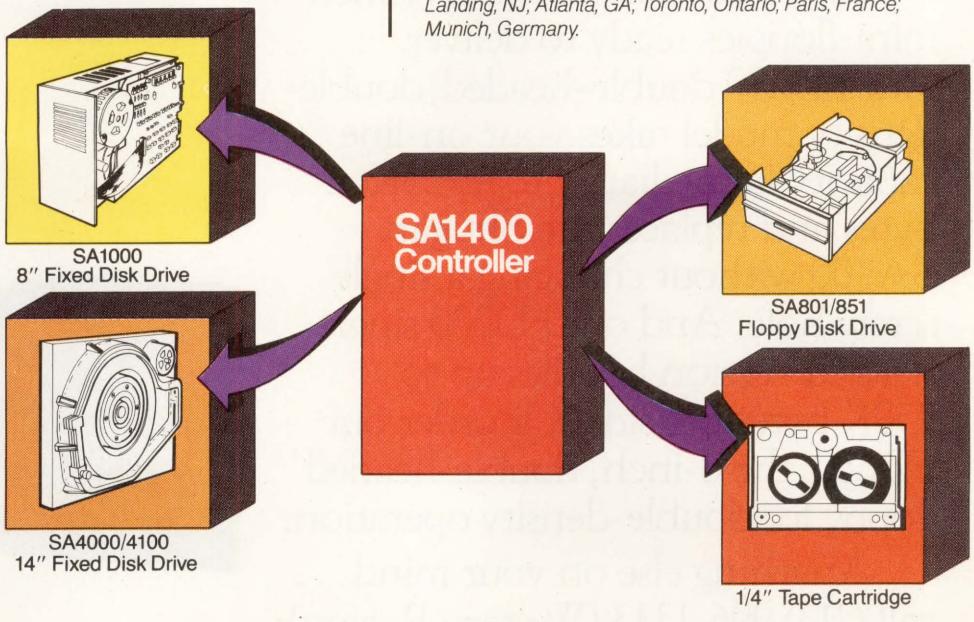

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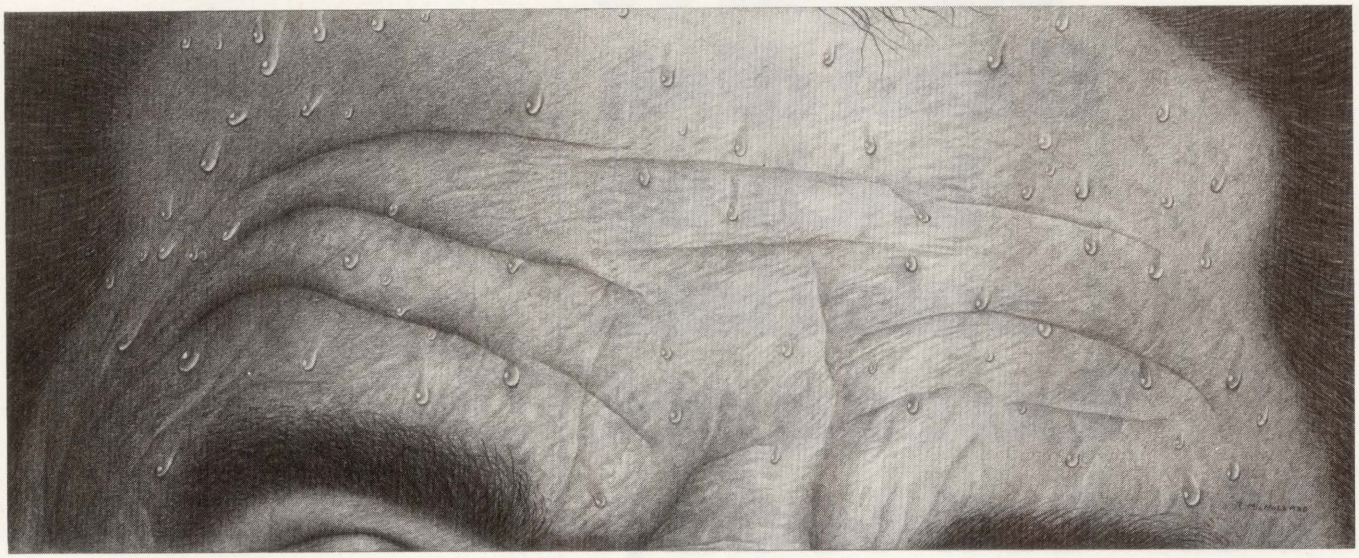

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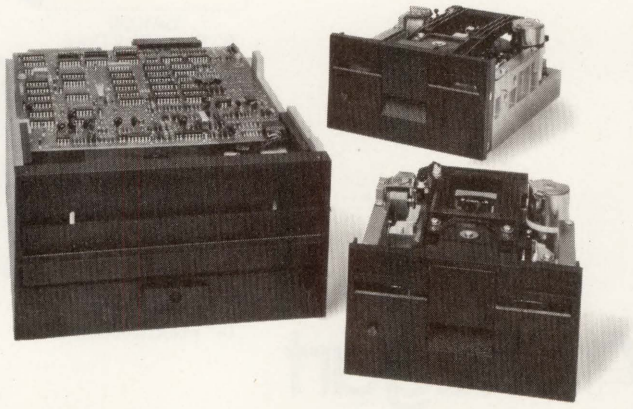

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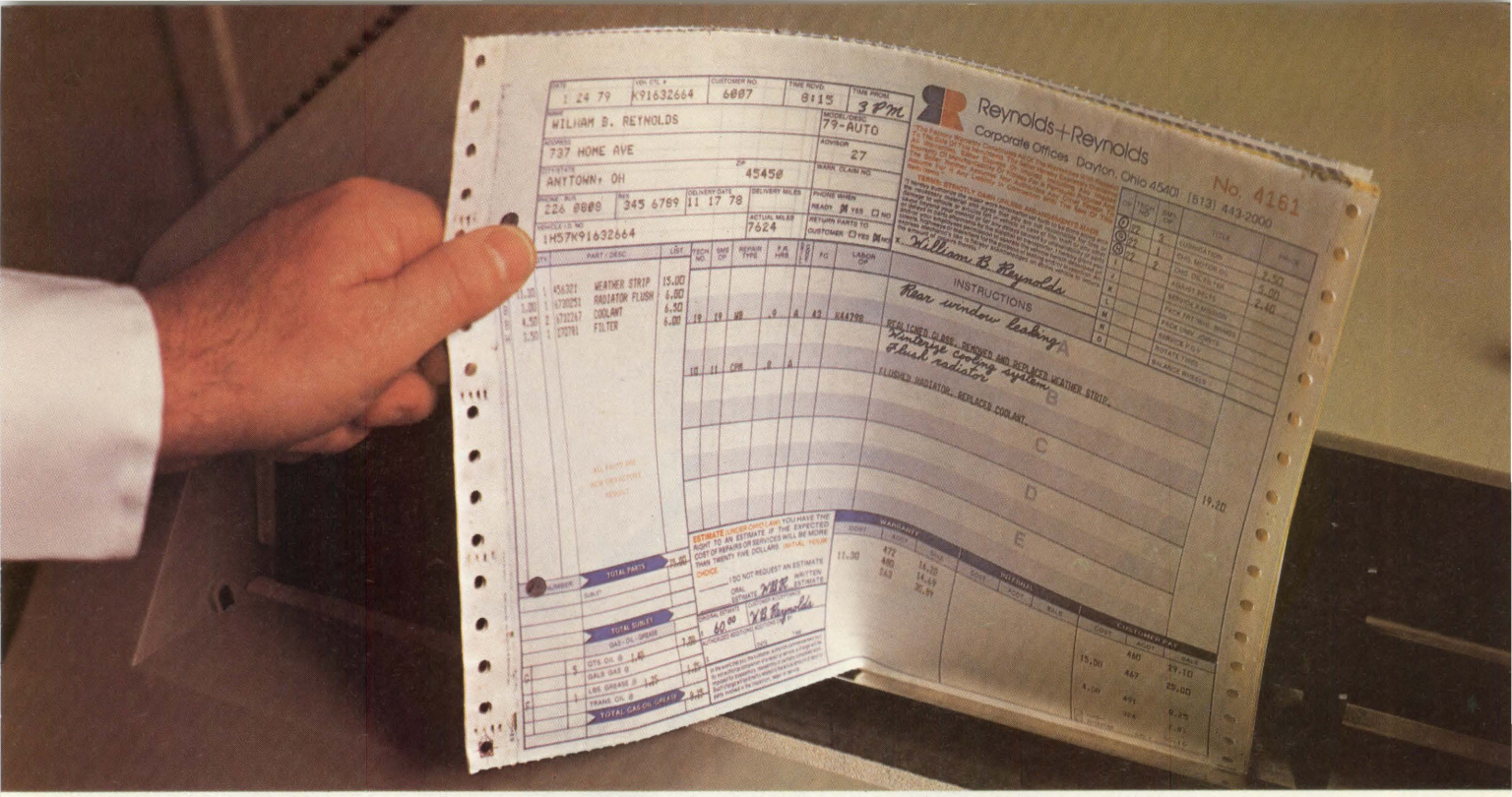

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CMOS MUX Family Is Implemented On Single Chips

The MP7501 is a monolithic CMOS, 8-channel device, which switches one of eight inputs to a common output, depending on the state of three binary address lines and an enable input. Identical characteristics are provided in the MP7503, except for the fact that its enable logic is inverted.

Another member of this line of monolithic CMOS analog multiplexers, from Micro Power Systems, 3100 Alfred St, Santa Clara, CA 95050, is the MP7502, which is a dual 4-channel differential device. Depending on the state of two binary address inputs and an enable, it switches two output buses to two of eight inputs.

Features common to all three devices include DTL/TTL/CMOS direct interface, 30-μW power dissipation, 170-Ω R_{ON}, and output enable control. Silicon nitride passivation processing ensures reliability and guaranteed long term stability. These devices are pin compatible with Analog Devices' AD7501/7502/7503.

Circle 508 on Inquiry Card

Fast Switching VMOS IC Includes Four Power FETs

A switching speed of 10 ns and a typical ON resistance of 5 Ω characterize the VQ1000 quad VMOS device from Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. The circuit is suitable for level shifters, LED digit strobe drivers, incandescent lamp drivers, line printers, and thermal printers. Low resistance, zero offset features also make it appropriate for applications in high speed line drivers, disc drive controls, and analog switches.

This IC mounts four 60-V, 0.5-A VMOS power FET chips in a single 14-pin plastic dual-inline package. It is oriented toward large volume, dense circuit configurations where users want to locate a number of repetitive functions on a single printed circuit board.

Zener protection between each gate and source reduces the static sensitivity of the device. Also, the source pin, which is grounded in many applications, is located between the gate and the drain pins, thereby enhancing isolation between input and output. Low input capacitance of each VMOS gate, typically 50 pF, contributes to the fast switching characteristic. The low input capacitance also ensures that TTL driver circuits will not be adversely loaded.

Because VMOS power FETs exhibit high input impedance, it is possible to use this device as an interface element where a single stage is all that is needed to control up to a 60-V, 0.5-A load from a low level logic input. Although each individual FET is rated at 0.5 A, total on-current of all four devices in the package is limited to 0.5 A. This ensures that the 1.5-W dissipation capability of the package is not exceeded.

Circle 509 on Inquiry Card

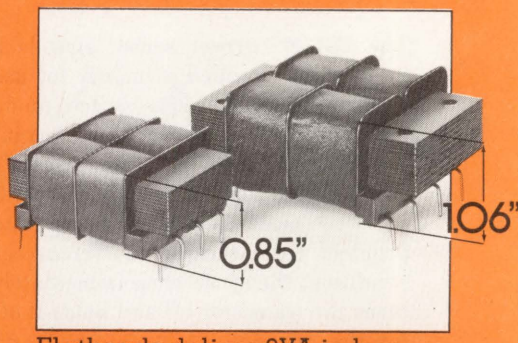
Complementary Power MOSFETs Come in 14-Lead DIPs

The low power dissipation of a complementary output, high voltage capabilities, 10-ns switching speeds, and driver currents ranging from 0.5 to 4.0 A characterize three families of complementary power MOSFETs from Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94086. These characteristics make the quad drivers suitable for applications such as display drivers, bubble memory drivers, printer drivers, and solenoid drivers.

N-channel parameters for the VC13 family include a current rating of 1 A and an on-resistance of 10 Ω. Corresponding values for the VC01 are 2 A and 4 Ω, and, for the VC02, 4 A and 2 Ω. P-channel parameters for each family are obtained by halving the current rating and doubling the on-resistance. All three families are available in 40-, 60-, 80-, and 90-V versions. Drivers with voltages up to 250 V will be available by second quarter 1980.

Circle 510 on Inquiry Card

Flathead® transformers for one-inch spaced PC boards



Flatheads deliver 6VA in less than 0.85" H. or squeeze 12VA into 1.06" H. Flatheads use Signal's split-bobbin, balanced-coil, hum-bucking construction. This semi-toroidal configuration significantly reduces magnetic field radiation which can cause havoc with sensitive IC's or low-level circuits. And the LP's split-bobbin provides unprecedented insulation and isolation. Minimal electrostatic coupling suppresses line noise and prevents false triggering of digital circuits.

Signal Transformer Co., Inc., 500 Bayview Avenue, Inwood, N.Y., 11696 Tel. (516) 239-7200.

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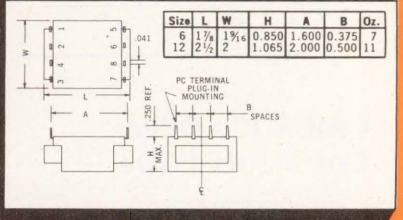
LP-10-1200	12	10V CT @ 1200 MA	5V @ 2.4 A	12.50
LP-12-450	6	12.6V CT @ 450 MA	6.3V @ 900 MA	10.15
LP-12-900	12	12.6V CT @ 900 MA	6.3V @ 1.8 A	12.50
LP-16-350	6	16V CT @ 350 MA	8V @ 700 MA	10.15
LP-16-700	12	16V CT @ 700 MA	8V @ 1.4 A	12.50
LP-20-300	6	20V CT @ 300 MA	10V @ 600 MA	10.37
LP-20-600	12	20V CT @ 600 MA	10V @ 1.2 A	12.85
LP-24-250	6	24V CT @ 250 MA	12V @ 500 MA	10.37
LP-24-500	12	24V CT @ 500 MA	12V @ 1A	12.85
LP-34-170	6	34V CT @ 170 MA	17V @ 340 MA	10.37
LP-34-340	12	34V CT @ 340 MA	17V @ 680 MA	12.85
LP-40-150	6	40V CT @ 150 MA	20V @ 300 MA	10.37
LP-40-300	12	40V CT @ 300 MA	20V @ 600 MA	13.10
LP-56-100	6	56V CT @ 100 MA	28V @ 200 MA	10.60
LP-56-200	12	56V CT @ 200 MA	28V @ 400 MA	13.10
LP-88-65	6	88V CT @ 65 MA	44V @ 130 MA	10.60
LP-88-130	12	88V CT @ 130 MA	44V @ 260 MA	13.45
LP-120-50	6	120V CT @ 50 MA	60V @ 100 MA	10.60
LP-120-100	12	120V CT @ 100 MA	60V @ 200 MA	13.45
LP-230-25	6	230V CT @ 25 MA	115V @ 50 MA	10.60
LP-230-50	12	230V CT @ 50 MA	115V @ 100 MA	13.45

*Regulation of Size 6 units is 30%, i.e., no load-secondary voltage is 30% higher than full load. Regulation of Size 12 units is 20%.



Size	L	W	H	A	B	Oz.
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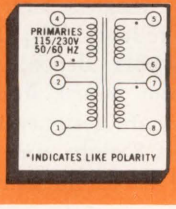
12	2½	2	1.065	2.000	0.500	11



signal TRANSFORMER

13

Chip Provides Fast Digital Current Limiting

The SG1549 current sense latch is a linear chip intended primarily for use in current limiting for switch mode power supplies. It monitors current buildup each time the power supply's switching transistor conducts, with each ON cycle treated as a separate problem. Upon sensing an overcurrent condition, the sense latch immediately turns the transistor off and holds it off for the duration of the normally ON period.

This device from Silicon General Inc, 11651 Monarch St, Garden Grove, CA 92641, is said to be the first IC chip to utilize digital rather than linear current limiting. By eliminating the linear feedback loop, digital current limiting overcomes the stability and speed limitations inherent in the linear approach.

Input threshold for the latch circuit is 100 mV. Delay (reaction time), using pulse by pulse sensing, is 180 ns. Common mode input voltage can range from ground to 40 V. High- and low-going complementary outputs are provided, and both the supply voltage and the reset clock signal can be taken directly from an associated PWM control chip such as the SG1524, MC3420, or the TL494. Required supply current is only 2 mA.

The chip is available in both ceramic and plastic 8-pin minidip packages. Three operating temperature grades are offered: −55 to 125 °C, −25 to 85 °C, and 0 to 70 °C.

Circle 511 on Inquiry Card

CMOS ICs Drive Dot Matrix LCDs

Four models of large scale integrated circuits produced by Hughes Aircraft Co, Solid State Products Div, 500 Superior Ave, Newport Beach, CA 92663, drive large dot matrix liquid crystal displays. They are designed for use with 5 x 7 or 5 x 8 alphanumeric dot matrices, as well as custom arrays. Features common to all of these chips include an onchip oscillator, cascadability for larger displays, and CMOS construction that assures wide supply voltage range, low power operation, high noise immunity, and wide temperature range. They can be defined as dumb drivers since they drive the display with proper voltage level ac waveforms, using a multiplexed scheme, but do not handle refresh or character encoding.

The HLCD 0538 is organized as 8 rows x 26 columns, and thus can handle up to five characters by itself. When more than 26 columns are required, it is supplemented by the HLCD 0539. This support chip is described as having an organization of 0 rows x 34 columns, meaning that it provides no row drivers. Both of these circuits take serial inputs to maximize the number of output pins and minimize the number of control pins.

A 4-bit parallel input which minimizes the time needed to load data characterizes the remaining two chips in this series. The HLCD 0541 is organized as 8 rows x 23 columns (or 24 columns by mask option) and can handle up to four characters by itself. HLCD 0542 is organized as 0 rows x 32 columns and is added when more columns are required.

Circle 512 on Inquiry Card

8k Static RAM Stores 8-Bit Words

Organized as 1024 words by 8 bits, a static random access memory, designated 8188, is particularly suited to microprocessor applications. This memory, from GTE Microcircuits Div, 2000 W 14th St, Tempe, AZ 85281, is available with a max access time of either 500 ns (-5 suffix) or 300 ns (-3 suffix). It is offered in a 24-pin cerdip package and is pin compatible to the 2708 EPROM.

The device has common I/O pins for connection to a data bus, requires only a single, 5-V power supply, and is TTL compatible on all inputs and outputs. It has a low power disabled mode which dissipates less than 60 mW. Enabled power usage is less than 270 mW max, and there is no max limit on the chip enable pulse width.

Each 8-bit word is addressed by simultaneously decoding the X addresses for the rows, and the Y addresses for the columns. Data are written or read in parallel on eight common I/O pins. Operation is controlled by chip enable ($\overline{CE}$) and write enable ($\overline{WE}$). When $\overline{CE}$ is high, all outputs are in an inoperative high impedance state and power is supplied only to the memory elements. With $\overline{CE}$ low, the memory is enabled for reading and writing.

Absolute maximum ratings require that voltage on any pin with respect to V_{SS} stay between −0.5 and 7.0 V. Power dissipation must not exceed 1.6 W, and max allowable output current is 50 mA. Allowable temperature ranges are 0 to 70 °C (ambient) in operation, and −65 to 150 °C in storage.

Circle 513 on Inquiry Card

8k and 16k EPROMs Are Second Sourced

Electrically programmable read only memories having capacities of 8192 and 16,384 bits are available from Oki Semiconductor, 1333 Lawrence Expy, Suite 405, Santa Clara, CA 95051. The 8k memory is the MSM2758, which is pin compatible with the 2758 from Intel; the 16k memory is the MSM2716, which is pin compatible with Intel's 2716.

These EPROMs share the properties of the existing devices in operating from a single 5-V power supply, dissipating a max of 525 mW in operation and 132 mW on standby, and providing a max access time of 450 ns. They are TTL compatible on inputs and 3-state outputs. Operation is over a 0 to 70 °C temperature range.

Fabricated using N-channel silicon gate MOS, the devices can be erased by irradiation with ultraviolet light. Since they can be easily electrically reprogrammed onsite, they are ideal for quick turnaround processor programs and prototype designs. Minimum programming time is 50 s for the 8k version and 100 s for the 16k version. Multiple chips may be combined by wired-OR connection for easy memory expansion. □

Circle 514 on Inquiry Card

Lear Siegler brings you the smart terminals designed for easy OEM customizing.

PERSONALITY PROMS AND FACTORY ASSISTANCE MAKE USER-REPROGRAMMING A SNAP.

At Lear Siegler, you don't have to decide among dozens of smart terminals, each slightly different, but none quite right for you.

We have just two smart terminals. But they can handle a range of tasks equal to four, five, or even six models from other manufacturers.

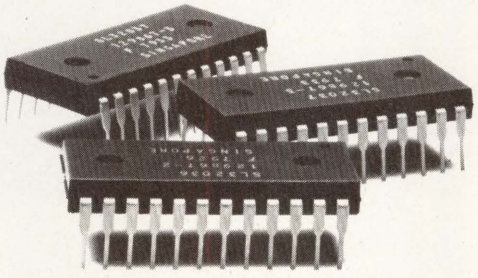
After all, we want to make your life simpler, not more complicated.

THE ADM-31 & ADM-42 WILL LET YOU CHANGE THEIR MINDS.

When we designed the ADM-31 and ADM-42, we realized that no matter what capabilities we offered, somebody would always want something different. So we did the next best thing.

We gave each a truly flexible personality by putting the instruction sets inside their PROMs. So, unlike the hardware, the firmware is capable of easy OEM reprogramming.

We even have a special Application Engineering Staff to answer any questions you may have about reprogramming, interfacing or special applications.



Feeling your life getting simpler yet?

ALL THE TERMINALS YOU'LL EVER NEED.

Even if you decide not to reprogram their PROMs, our two terminals come with all the standard smart terminal features. And then some.

Features like full editing capabilities. Formatting. Reduced intensity for identification of protected fields. Blinking, blanking, and reverse video. High resolution monitors. Even limited line drawing capabilities.

What's more, both the ADM-31 and ADM-42 come equipped with a microprocessor and function keys making them even more reliable and easy to use.

THE CHOICE IS SIMPLE.

You can choose your new smart terminal one of two ways. Start sifting through dozens of data sheets, talking to dozens of salesmen, and looking at dozens of expensive, slightly different terminals.

Or look at two smart terminals from Lear Siegler—the ADM-31 and ADM-42. Complete with user-reprogrammable personality, function keys, and an eager and willing Applications Engineering Staff to help you with any reprogramming problems.

The choice seems pretty easy to us. But if you want more information, call or write to us at Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, California 92803, (800) 854-3805. We'll be happy to tell you all about the ADM-31 and ADM-42. And show you how you can make your terminals behave.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

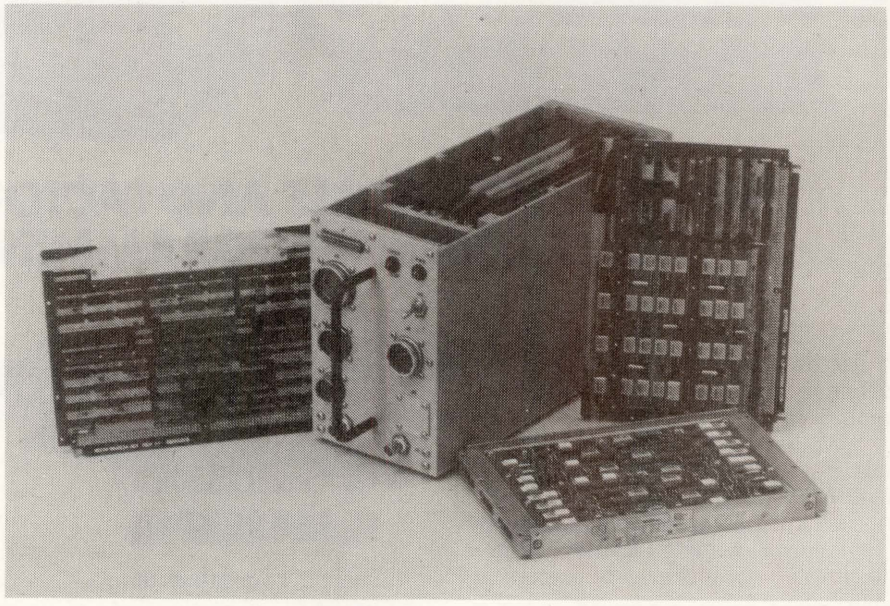
CIRCLE 105 ON INQUIRY CARD

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803, (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 245-1520. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (04867) 80666.

PRODUCT FEATURE

Severe Environment Minicomputer Fully Compatible with PDP-11/35

SECS 2, a ruggedized computer system fully compatible with the DEC PDP-11/35, is now being manufactured by EMM/SESCO under license to Digital Equipment Corp. The 16-bit minicomputer is designed for use in a range of severe environments, including process control as well as avionics and military. It can be used with all PDP-11 operating systems and applications software and offers all advantages of the DEC computer, plus the capability to operate under adverse conditions of high and low temperatures, high vibration, high shock, and corrosive atmosphere.



System Description

All features of the PDP-11 system are available, such as hardware multiply and divide and floating point arithmetic, plus the ability to meet or exceed requirements of standards MIL-E-5400, MIL-E-4158, and MIL-E-16400.

The basic ruggedized computer package is available in both half- and full-ATR (air transport rack) system configurations, including power supplies, or as individual cards. It is FAA certified for commercial passenger aircraft. Fully MIL-spec qualified support modules include single-board electrically programmable read only memory (EPROM), single-board random access memory (RAM), and core modules; 60k-baud RS-232, 100k-baud RS-422, and 1553 bus interface serial I/O boards; peripheral device interface and bus interface controllers; and tape system controllers.

Execution times are equivalent to those of the PDP-11/35, with a typical add requiring 1.92 μs. The DMA channel operates at 1M words/s.

Operating temperature range is -55 to 85 °C at 0 to 95% humidity with condensation. Environmentally, the computer functions at 5G vibration from 5 Hz to 2 kHz, and at 15G shock for 11 ms. Altitude operating range is sea level to 70,000 ft (21 km). MTBF is greater than 25,000 hours at 55 °C.

Support Modules

Memory modules include EPROM, RAM, and core, all in 16-bit format. Ultraviolet light erasable EPROM boards provide 2k, 4k, 8k, or 16k words. Average erasure time is 20 min with a 12-mW/cm² UV lamp. An available EPROM card programmer can program every location on the card in less than 24 min. Access time is 600 ns; full cycle time is 960 ns.

RAM cards of 16k, 32k, 48k, and 64k capacity use MIL-STD-883 16k x 1 dynamic devices. A strapping option on the rear panel connector enables selection of contiguous address segments. All data written into or read from memory are buffered, and all data, address, and command signals on the bus are TTL compatible. Access time is 300 ns and cycle type is 480 ns.

Think Twice

Intel's new 8272 controller for double density floppy disks lets you command shorter design times.

Why have second thoughts about designing a double density floppy disk drive into your system, when Intel's 8272 is available now. With a powerful command set, microprocessor compatibility, Intel's HMOS* technology and the ability to reduce CPU overhead, our controller for IBM compatible single or double density floppy disks is the logical choice for system designers.

Now, you don't have to spend months building and programming an entire board of interface logic to control one, two, three or four double density floppy disk drives. Just incorporate Intel's new 8272 controller into your design to save time and space. Our double density floppy disk controller does more than reduce your parts count 50 to 1. It gives you enough flexibility to shorten your design cycle. And Intel's 8272 offers you the freedom of designing in the 5-volt world.

Freedom for the CPU.

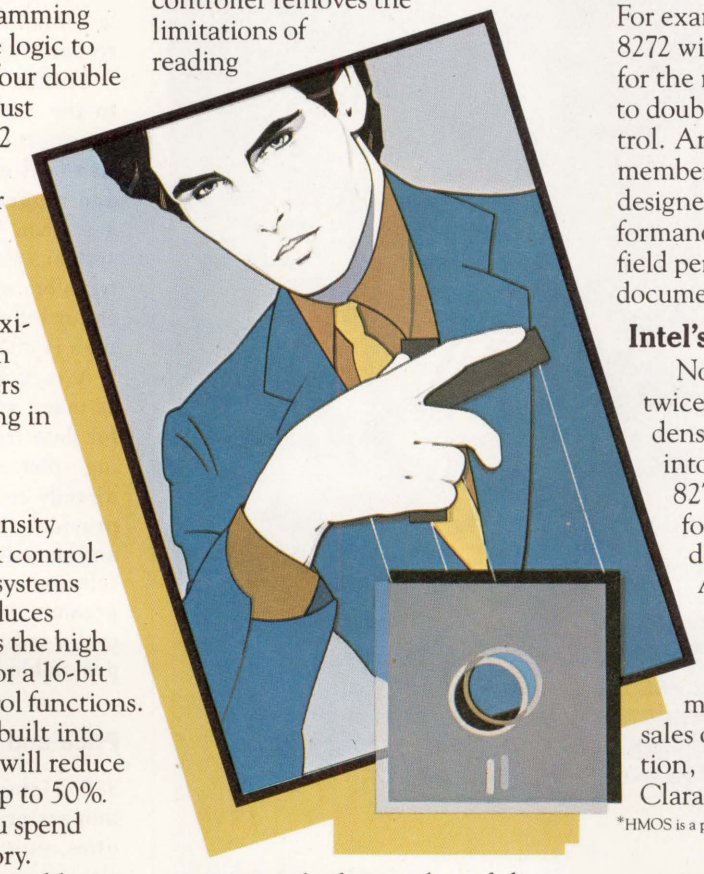
Our new 8272 double density floppy and mini-floppy disk controller is the right solution for systems designers. It saves time, reduces power dissipation and slices the high cost of burdening an 8-bit or a 16-bit CPU with floppy disk control functions. A powerful instruction set built into Intel's new 8272 controller will reduce your programming efforts up to 50%. Less code is required, so you spend less time and use less memory.

Intel's 8272 solution also tackles the problem of CPU overhead and software intervention. Our double density floppy disk controller has the capability of scanning a single sector or an entire track's worth of data fields. Data on the floppy disk gets compared byte-by-byte with data in your system memory. And, since a single command locates and compares the data, no additional software is necessary.

Faster data access.

Our new 8272 controller does more than drive up to four floppy disks simultaneously. It handles parallel seek on up to four disks for faster data access.

With multi-sector and multi-track transfer capabilities, the CPU is freed from time-consuming I/O commands. Our new double density floppy disk controller removes the limitations of reading or writing only the number of characters a physical sector allows. The 8272 automatically transfers data across the disk's consecutive sectors... and, as a result, the CPU isn't forced to wait until the next sector is positioned. With Intel's new 8272, you not only free the CPU, you get the assurance of higher system performance.



Easy microprocessor compatibility.

Intel delivers the new 8272 double density floppy disk controller into the 5-volt world. That makes our controller an easy, compatible interface with Intel's family of microprocessors like our 8086, 8088 and 8085.

As part of the Intel peripheral family, the new 8272 complements our other dedicated LSI performers. For example, you can team our 8272 with an 8237 DMA controller for the most bus-efficient solution to double density floppy disk control. And like our other family members, the 8272 offers systems designers highly reliable performance... plus the support of field personnel and complete documentation.

Intel's new 8272, here today.

Now, you don't have to think twice about designing a double density floppy disk controller into your system. With Intel's 8272, you won't have to settle for fewer features or a long design cycle, either. Why wait. Already second sourced, our 8272 is on your distributor's shelves today.

For more detailed information, contact your local Intel sales office or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

*HMOS is a patented Intel process.

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Two serial I/O cards perform asynchronous data transfers in accordance with RS-232-C requirements or a 20-mA current loop TTY interface. Each card has two I/O ports. One card (/232) performs data transfers at rates up to 60k baud. On the second card (/422), single-ended I/O devices of the other card are replaced with differential line drivers and receivers to permit data transfer rates of up to 100k baud. Both devices are full-duplex.

A 1553 card provides an interface between the MIL-STD-1553 bus structure and that of the minicomputer bus. The basic card consists of microprogrammed controller, memory port, and dual redundant 1553 bus interfaces. When functioning as a bus controller, the interface acts as an I/O channel; when acting as a remote terminal, it monitors both 1553 buses and responds to commands having its remote terminal address. Intermessage gap is 4 μs minimum and remote terminal response time is 4 to 12 μs.

Unibus peripheral devices connect to the SECS 2 EMMbus via a software transport converter. This permits both standard commercial DEC peripherals and ruggedized versions to be used in a system. The complete bidirectional system element enables DMA data transfers without additional multiplexers or other special hardware. Latency time is 300 ns.

A tape system controller interfaces as many as four SETS-1 tape recorders for data transfer rates of 48k bits/s using phase encoding. It interfaces directly to the minicomputer bus and provides Manchester data encoding and decoding. Data are written onto a selected single tape track with 4-byte preamble, variable length data record, cyclic redundancy check bit, and two postamble bytes.

Price and Delivery

SECS 2 minicomputers in full configuration are priced at $6000 in small quantities; support modules average $3000, also in small quantities, but differ in price depending on complexity. Delivery is six to nine months. EMM/SESCO, 20630 Plummer St, Chatsworth, CA 91311. Telephone: 213/998-9090.

For additional information circle 199 on inquiry card.

Three Best Sellers for the 80's

1 New 1980-81 Catalog

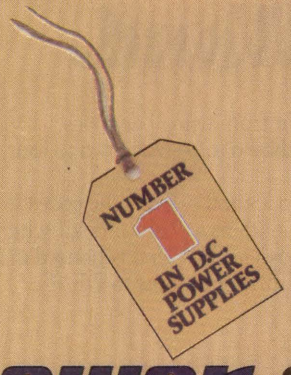
28 colorful pages with complete details on over 100 standard open-frame and switching D.C. power supplies. Full specs, photos, O&M drawings, and prices on each model.

2 New Tour Guide — A Trip Through Power-One

The next best thing to a personal visit. Our new Tour Guide takes you on a photographic trip through our modern new facility. See why Power-One is the most automated, efficient producer of D.C. power supplies in the world... and why we've been able to hold our prices steady for over 5 years!

3 New Open Frames and Switchers... At Our Same Old Prices!

More new open-frames to choose from — plus new special-purpose models for specific applications such as Microprocessor and Floppy-Disk systems. Also, Power-One now offers a growing line of switching D.C. power supplies with the same quality and high reliability as our open-frame models.



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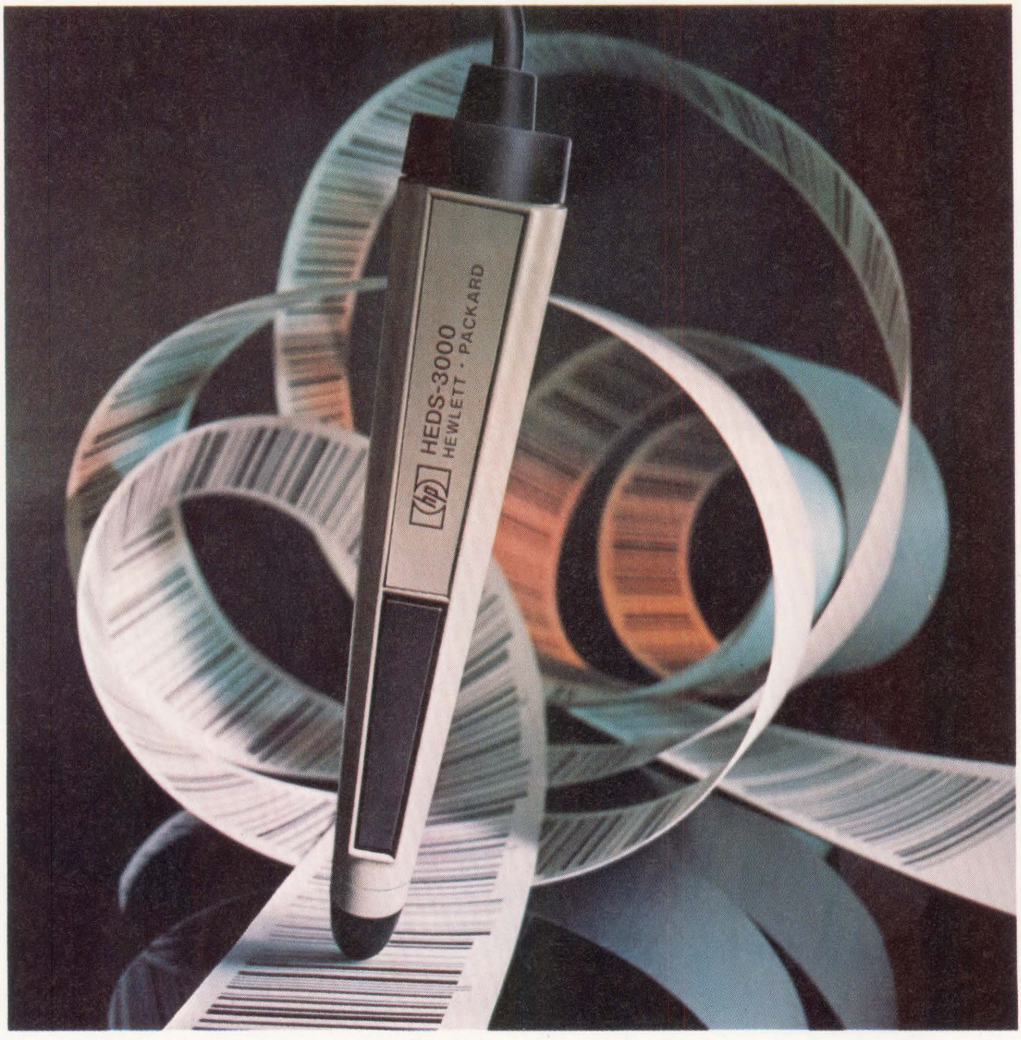
CIRCLE 108 ON INQUIRY CARD

SURPRISE!



HP Introduces the World's First Digital Bar Code Wand.

Anyone now using a keyboard or push buttons for data entry could benefit from using bar codes. Depending on the number of characters being entered, bar code scanning has been shown to be from two to four times faster than key entry.

HP's new HEDS-3000 Digital Bar Code Wand can scan black-and-white bar codes and convert the codes to microprocessor-recognizable digital output. Fully specified and guaranteed, the Wand contains a push-to-read switch which conserves power. It is well suited to portable systems as well as those with line power. The Wand is housed in a rugged, stylized, molded plastic case with attached cord and connector. Of even further interest to OEM's, the HEDS-3000 can be manufactured in custom colors with desired logos.

In quantities 1-99, the Wand is priced at $99.50* each.

For more information or immediate off-the-shelf delivery, contact your nearest HP Components franchised distributor. In the U.S. contact Hall-Mark, Hamilton/Avent, Pioneer Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd.

HEWLETT PACKARD

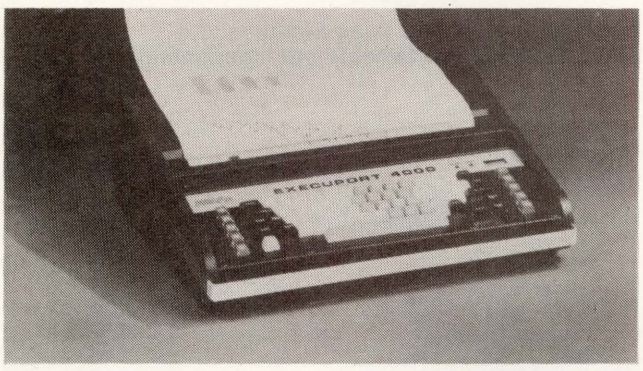
01906

*U.S. Domestic Price Only

CIRCLE 109 ON INQUIRY CARD

PRODUCTS

Portable Send/Receive Printing Terminal Provides Alphanumeric or Graphics Hardcopy



Only a regular telephone line and electric power are required to place the Execuport 4000G terminal in operation. Connection to a computer is made by inserting the telephone handset into a built-in acoustic coupler that features increased sensitivity and sound isolation. The completely portable send/receive printing terminal weighs 16 lb (7.25 kg) and provides either 136-or 80-col printout on paper or transparent film.

Switch selectable odd, even, or mark parity operation enable half- or full-duplex communication with all timesharing services as well as between organizations with different parity EDP systems. Data are entered through a full size typewriter style alphanumeric keyboard that generates all 128 ASCII characters, as well as via a color coded calculator-format, embedded numeric cluster.

Choice of graphics or standard alphanumeric operation is switch selectable. Graphics output uses a modified ASCII print code with special graphic characters, whereas alphanumeric output uses the full code. The thermal printer produces lines in 40 x 48 format at 1920 points/in^2 (298/cm^2). In graphics mode, transparent film hardcopy can be shown immediately on an overhead projector without additional processing. Printing is true upper and lower case.

Standard features include tabbing, 3-digit LED printhead position indicator, self-test key that produces a full sequential printout of the complete keyboard character set, parity error display, and out of paper alarm. True subscripting and superscripting or underlining of data are provided at no decrease in size of printed characters. A data logging capability is available as an option.

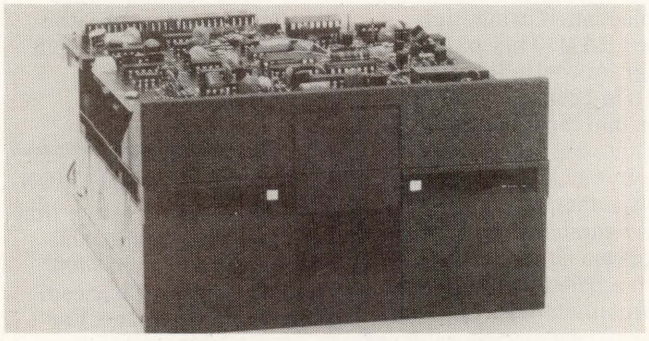
Parity errors are specified and pinpointed by an error character that is printed a quarter step above the line of data output. A factory set answerback memory can be supplied to transmit an identification code of up to 30 ASCII characters when triggered by receipt of a remote ENQ code. **Computer Transceiver Systems, Inc,** E 66 Midland Ave, Paramus, NJ 07652.

Circle 200 on Inquiry Card

Mini-Floppy Disc Drives Offer Up to 1M-Byte Storage and 3-ms Access Time

A line of 5.25″ (13.34-cm) high speed, random access, mini-floppy disc drives offer up to 1M-byte unformatted storage and 3- or 5-ms track to track access times. All TM-100 models feature the patented "fixed bottom head," plus a gimbaled top head to maintain the transducers in operative relation for maximum flux interchange, without introducing undue wear or requiring long head settling time. Recording heads provide up to 20k hours of media contact wear and 4 x 10^6 passes/track.

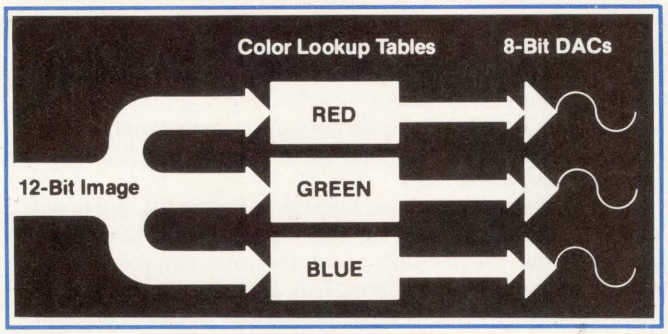
Single-head model -1 has a 250k-byte unformatted storage capacity, 40 tracks/diskette; -3 has a 500k-byte capacity on 80 tracks/diskette; both feature 5535-bit/in (2180/cm) recording densities and 5-ms track to track access times. Double-head model -2 features unformatted capacity of 500k bytes and has 80 tracks/diskette; -4 has a 1M-byte capacity and 160 tracks/diskette. Both -2 and -4 have 5877-bit/in (2314/cm) recording densities and 3-ms track to track access times. Up to



4 drives can be daisy chained on a single bus to provide unformatted capacities of 1M bytes for the -1, 2M bytes for the -2 and -3, and 4M bytes for the -4. **Tandon Corp,** 9333 Oso Ave, Chatsworth, CA 91311.

Circle 201 on Inquiry Card

How to display 4096 colors, while keeping track of 16.7 million more.



Completely independent color lookup tables map up to 12 bits of intensity data into three, eight-bit outputs.

Do it with the Lexidata System 3400 image and graphics processor.

If high-quality color is an essential part of your computer graphics or imaging requirements, the System 3400 can provide you with fast access to a virtually unlimited palette of color shades. As part of its array of over three dozen system building blocks, the 3400 offers color lookup tables that make it possible to display up to 4,096 colors simultaneously.

The lookup tables are implemented using high-speed RAM. They handle program-controlled mapping of up to 12 bits of intensity data into three eight-bit outputs, one for each color gun in a RGB color monitor. Thus, a total of 2^{12}, or 4,096, colors can be selected and displayed simultaneously from a palette of 2^{24} -1, or approximately 16.7 million colors. If even greater display flexibility is required, the System 3400 can also be equipped with a gray scale lookup table that can be operated in parallel with the color lookup table. Up to 256 shades of gray can be selected from a palette of 4,096 shades and displayed simultaneously.

The System 3400 provides a high degree of output versatility. Standard RGB output is RS-170 or RS-343A compatible, and other output rates are available on request. To assure high quality display of color images in a variety of application environments, the 3400 will drive medium, high and ultra-high resolution monitors with bandwidths up to 40 MHz. Also, for video recording applications, the 3400 provides NTSC output with color subcarrier regeneration capability.

GET MORE INFORMATION

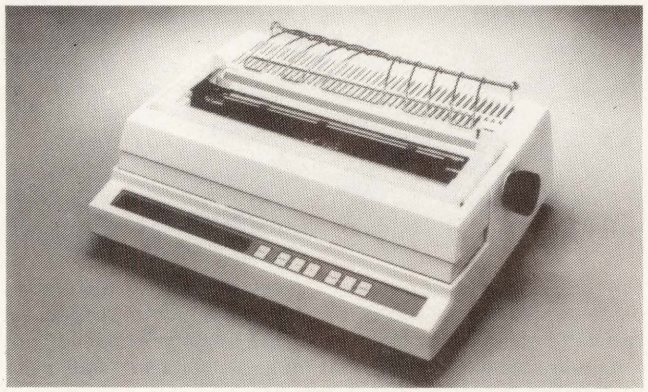
Send today for literature that will help you evaluate how the Lexidata System 3400 can help improve your computer graphics image. For immediate response call (617) 273-2700.

LEXIDATA CORPORATION
37 NORTH AVENUE, BURLINGTON, MA 01803

CIRCLE 110 ON INQUIRY CARD

PRODUCTS

Serial Impact Printer Uses Plastic and Metallized Printwheels Interchangeably



Improved overall operating reliability and flexibility of operation, resulting from denser component packaging as well as use of LSI and microprocessor controllers, are evident in model 630 serial impact printers. The first of their type to use plastic and metallized printwheels interchangeably, these daisywheel printers vary in speed from 32 to 40 char/s, depending on printwheel, type style, and text, and produce typewriter quality output. Over 100 different 88-, 92-, and 96-char plastic and metal printwheels, in 10- or 12-pitch or true proportional spacing, can be used.

Printer mechanism, electronics card cage for up to 4 PC boards, and optional power supply are housed in the printer's base. Each major subassembly—including all electronics boards, motors, cables, power supply, frames, and switches—can be replaced in less than 15 min. The factory adjusted carriage assembly requires no field adjustment during customer use.

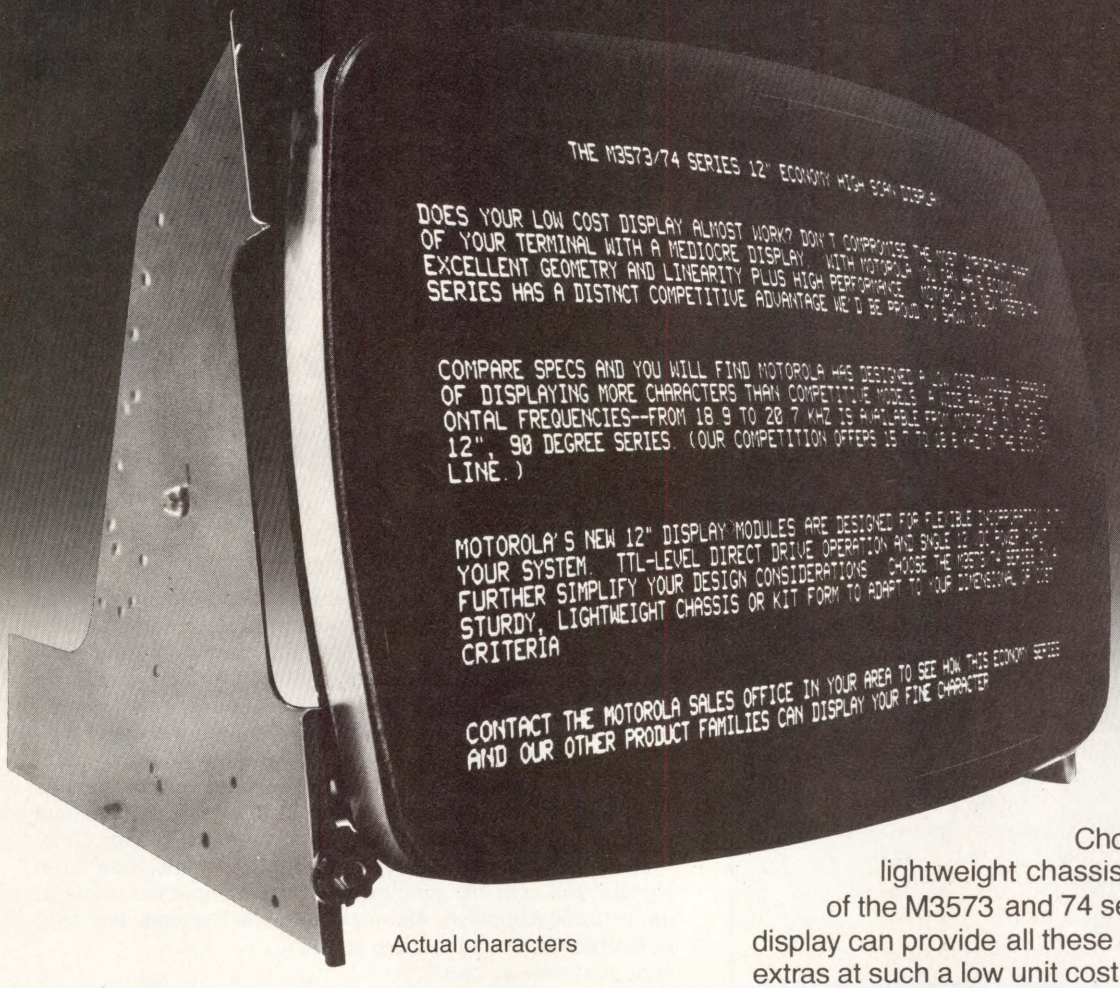
An electrostatic discharge immunity system in the structural foam plastic base prevents interruption of the printing process at up to 15 kV of static electricity. One portion of a 2-part foam plastic cover provides the overall housing; the other part serves as an access cover that surrounds the platen mechanism for noise reduction as well as for protection.

Carriage movement is bidirectional in 0.008″ (0.2-mm) increments, with bidirectional paper motion of 0.02″ (0.5 mm). Paper feed is 4 in (10.2 cm)/s plus a minimal settling delay. Printer dimensions are 8.25 x 22.4 x 18.25″ (29.96 x 56.90 x 46.36 cm). Weight is less than 60 lb (27.2 kg).

A microprocessor bus interface contains 8 bidirectional data lines and 6 unidirectional control lines. Serial interface is RS-232-C/V.24; 110 to 9600 baud; Bell 103A, 113A, 212A modem compatible. Current loop interface is 20 or 60 mA, active or passive, half-or full-duplex. **Diablo Systems Inc,** 24500 Industrial Blvd, Hayward, CA 94545.

Circle 202 on Inquiry Card

Motorola presents a character building alternative to the low-cost CRT compromise.

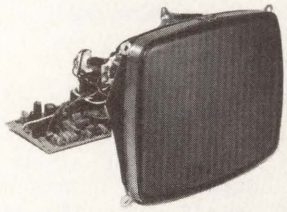


Actual characters

These low cost modules actually can display more characters than comparable competitive units. The new 12″, 90° series provides excellent geometry and linearity within a wider range of horizontal frequencies—18.9 and 20.7 KHz. This increased scan rate means up to two extra character rows for your terminal. (The M3573 offers an 80 x 25 format; the M3574 displays an 80 x 26.)

Motorola's new M3573 and 74 offer economy without compromising quality. They demonstrate excellent resolution—900 lines center; 750 corners (50 more than the competition). Video amplifier response up to 22 MHz also increases the display capability while providing consistently distinct characters.

Choose either lightweight chassis or kit versions of the M3573 and 74 series. No other display can provide all these performance extras at such a low unit cost. *Just one more example in which experience—Motorola experience—can benefit you.*



Motorola displays the character of your business.

MOTOROLA
Display Systems

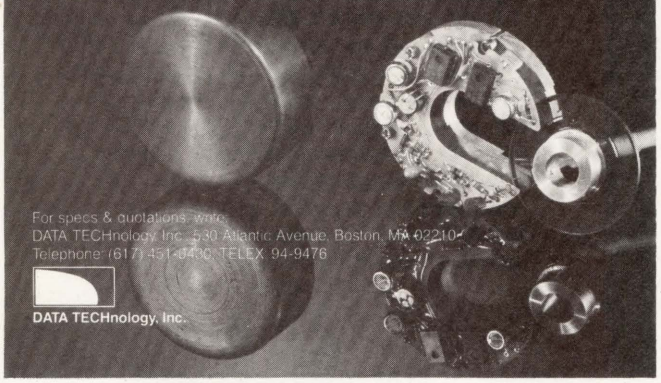
1155 Harvester Road West Chicago, IL 60185
312/231-4400

CIRCLE 111 ON INQUIRY CARD

There's only one modular encoder worth buying. DATA TECHnology's M-20.

Reflect on that!

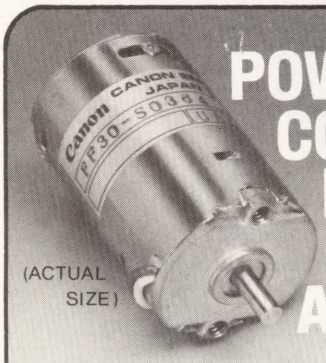
Over three years in development. M-20, the best performing modular encoder in the industry. Well engineered. Dependable. 100's of applications. Factory pre-alignment makes installation time minimal. The only tool required is an allen wrench. Compare costs and specs. Then, compare performance. M-20, the only modular encoder worth buying!



For specs & quotations, write:
DATA TECHnology Inc., 530 Atlantic Avenue, Boston, MA 02210
Telephone: (617) 451-0430 TELEX 94-9476

DATA TECHnology, Inc.

CIRCLE 54 ON INQUIRY CARD



(ACTUAL SIZE)

POWERFUL COMPACT DC MOTOR WITH AC TACH

Available in OEM quantities, the FF 30 DC motor with integral 8 Hz AC tachometer provides high efficiency, long life and low electrical interference and mechanical noise. Available with AMP 110 terminals. 30mm dia., 48mm long.

- *Varistor ring and high quality brush material for low electrical noise*
- *2 V RMS AC tach output controls speed*
- *Maximum efficiency more than 60% at 12V*
- *7 slot core for smooth operation*

SPECIFICATIONS

Rated Voltage:	12V	No Load Current:	115 mA
Rated Load:	75g-cm	Starting Torque:	280 g-cm
Rated Speed:	4700 ± 500 rpm	Stalled Current:	1800 mA
No Load Speed:	6450 rpm	Motor Regulation:	23 rpm/g-cm
		Rotation:	CCW

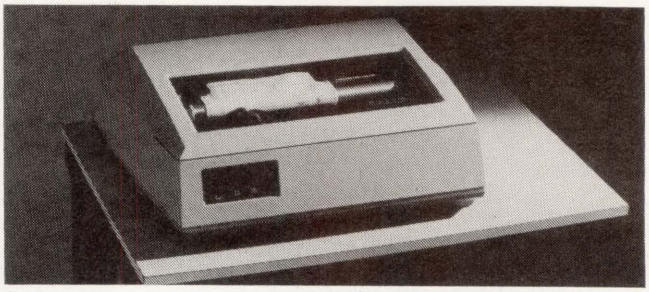
For complete technical information:

Canon

Canon, U.S.A., Inc.
Electronic Components Div.
10 Nevada Drive,
Lake Success, N.Y. 11042
516/488-6700 Telex: 96-1333
Cable: Canon USA LAKS

PRODUCTS

SERIAL PRINTER



Featuring LSI electronics and an advanced printhead design, the TI705 serial printer has a buffered RS-232 interface. The fully configured machine is equipped with features that are usually extra cost options. Printing at 160 char/s the printer is enhanced by microprocessor controlled optimized bidirectional head travel to achieve throughput speeds up to 200 lines/min. Printhead design effectively doubles life. Rugged and reliable, the printer requires no preventive maintenance. It features dual-tractor paper handling to assure positive paper positioning and control, switch selectable 6- or 8-lines/in (2.3 or 3.1/cm) spacing, self-test, and double-wide character printing. **Tally Corp,** 8301 S 180th, Kent, WA 98031.

Circle 203 on Inquiry Card

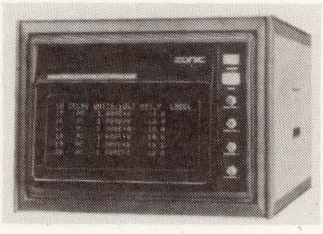
HIGH AND LOW LEVEL ANALOG INPUT SYSTEMS

Low level analog signal measurement capabilities are provided to MODACS II systems with process interface cards models 1870-1 analog input basic and 1872-X mercury wetted relay multiplexer that can acquire and digitize full scale signal levels from ± 10 mV to ± 1.28 Vdc in severe electrical environments demanding high noise immunity and ability to withstand high common mode voltage. High level models 1860-X analog input and 1861-X analog multiplexer expander cards provide 16-channel differential multiplexer, 4-gain range sample/hold amp, autorange control circuit, 12-bit successive approximation ADC, RAM data storage, and control logic. Low level signals read in at 180 samples/s; high level input can occur at up to 30,000 samples/s. **Modular Computer Systems, Inc,** 1650 W McNab Rd, Ft Lauderdale, FL 33310.

Circle 204 on Inquiry Card

MULTIPLE-CHANNEL FFT ANALYZER

For use as a simple multiple-channel FFT analyzer or combined with peripherals and computers to operate as a 128-channel realtime analyzer, high speed data acquisition system, or modal analysis system, the 6080 provides data acquisition and analysis capabilities in a field portable instrument. Mainframe houses from 2 to 8 parallel channels of data acquisition and can be expanded up to 128 parallel channels using slave chassis units which support up to 12 channels each. Proprietary bus concept allows a large number of data acquisition cards, each with its own auto gain stage, 12-bit ADC, and antialiasing filters, to be connected to common signal processing and CPU buses. **Zonic Technical Laboratories, Inc,** 2000 Ford Cir, Milford, OH 45150.



Circle 205 on Inquiry Card

CIRCLE 55 ON INQUIRY CARD

For years, manufacturers of computers, processors and other electronic equipment have improvised all too freely when running interconnecting cables *outside* cabinets. The results have been cumbersome, unattractive, often costly and sometimes hazardous.

Brand-Rex, long a leading supplier of Tape Cable® for internal use, now has the answer for external applications. A line of UL-listed jacketed Tape Cable. With shielding or without, it's made to fit a full range of temperatures and voltages up to 105°C and 600 volts. Now, interconnections can be efficient, economical, hazard-free, often even invisible.

Get complete information about Brand-Rex jacketed or shielded-and-jacketed flat cable. Write to Brand-Rex Company, Electronic and Industrial Cable Division, Willimantic, CT 06226. Or call 203/423-7771.

BRAND-REX

ELECTRONIC AND INDUSTRIAL CABLE DIVISION

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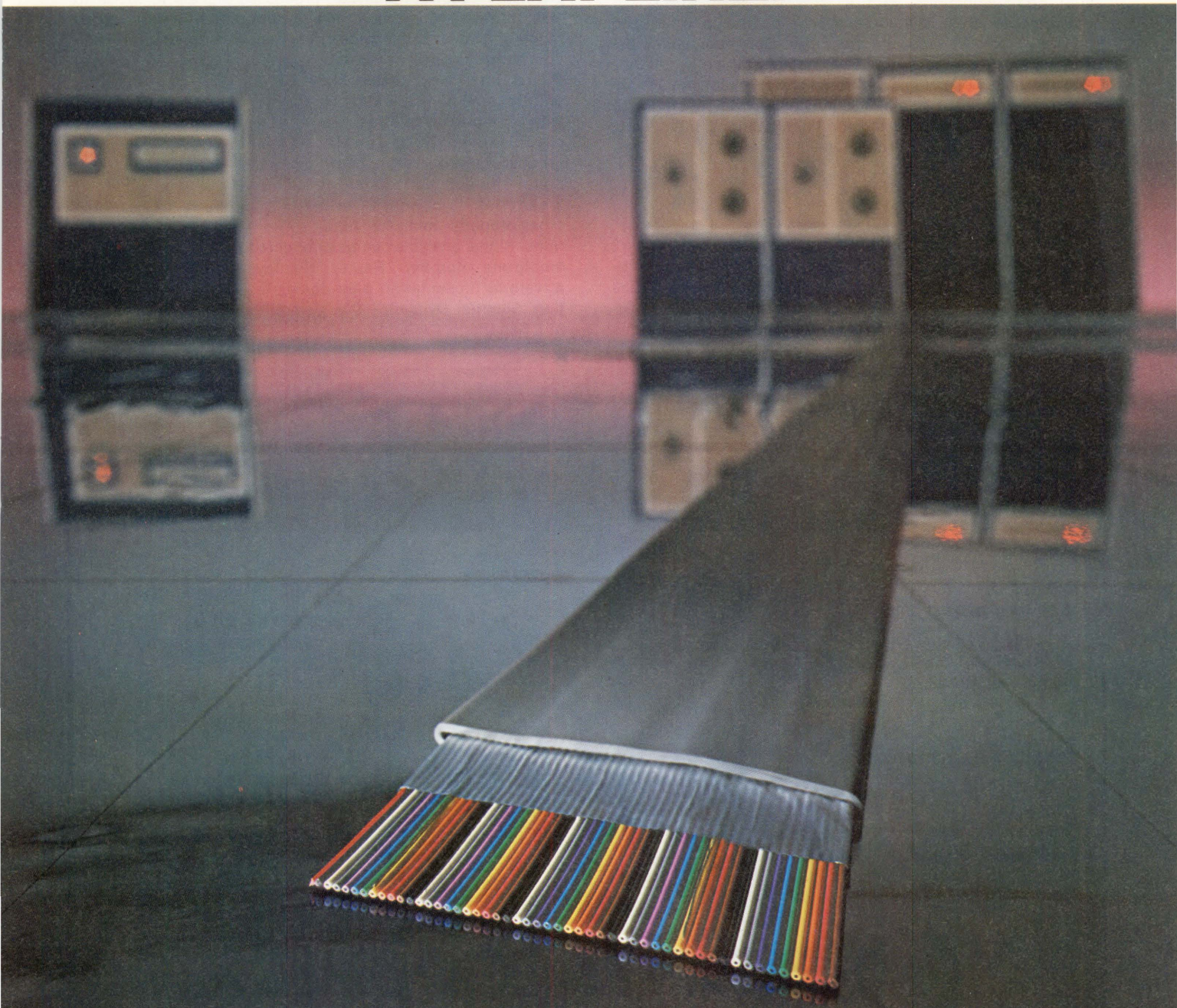
Telecommunications Cable Division: wire and cable
Teltronics, Inc.: telecommunications products

BRAND-REX COMPANY, A PART OF AKZONA INC.

THE SAFEST CONNECTION BETWEEN TWO POINTS IS NOW A FLAT LINE.

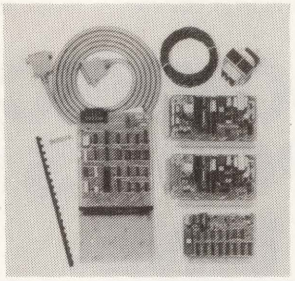


STATE-OF-THE-ART-SOLUTIONS

CIRCLE 113 ON INQUIRY CARD

PRODUCTS

REMOTE DATA ACQUISITION SYSTEM KITS



Permitting automatic polling and digital data transmission from up to 256 remote stations with 12-bit accuracy over a single twisted pair of wires, REM-DACS™ (remote data acquisition and control system) consists of 2 types of remote station cards, a receiver/transmitter card, and an RS-232 card for serial communications with a host computer. Remote stations may be located up to 1 mi (1.6 km) away from the receiver/transmitter. Communications between remote stations and receiver/transmitter are handled by serial transmission using a multidrop party line concept. Channels may be added or changed by moving the remote station to another location or connecting additional stations. **Intersil Inc,** 10710 N Tantau Ave, Cupertino, CA 95014.

Circle 206 on Inquiry Card

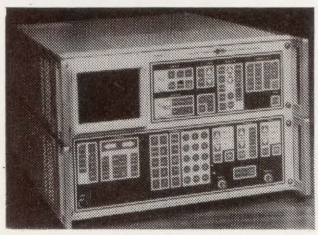
FIBER OPTIC TRANSMITTER/RECEIVER

Designed for low cost, moderate speed, long distance applications, the DIPLINK 2 minisystem consists of TTL and CMOS compatible, pigtailed, fiberoptic transmitter/receiver pair. Packed in 24-pin DIPs, both transmitter and receiver modules are pigtailed with 0.5-m of strengthened fiberoptic cable, compatible with AMP Optimate or Multimate inline or bulkhead splices. Transmitter module incorporates a temperature compensated IR source operating at 820 nm which couples 150 μW or more into the 220-μm core plastic clad silica pigtail. Receiver module exhibits sensitivity of 0.50 μW peak into the 400-μm core plastic pigtail, allowing operation from true dc to 2.0M bits/s-NRZ at 10^{-8} BER over distances to 2 km. **LeCroy Fiberoptic Systems,** 10024 York Rd, Cockeysville, MD 21030.

Circle 207 on Inquiry Card

DUAL-CHANNEL SPECTRUM ANALYZER

Model SD375 Dynamic Analyzer II, a microprocessor based 2-channel spectrum analyzer, processes signals in the 0- to 100-kHz range, correlates their mutual properties in a broad range of modes, and provides direct answers to structural and communications problems. Digital interfaces enable the unit to communicate directly with computers, plotters, or calculators. Functionally grouped controls on a touch panel select 33 different 2-channel, 1-channel, and cross-property analysis functions. Signal analysis can be conducted in time, frequency, or amplitude domain. Raster display includes 2-channel waveform presentation plus complete alphanumeric annotation. **Spectral Dynamics Div, Scientific Atlanta, Inc,** PO Box 671, San Diego, CA 92112.



Circle 208 on Inquiry Card

You can bank on Pittman® D-C motors— performance at an affordable price

LO-COG®
Servo Motors
3 series: 1.2, 1.6 & 2.0″ O.D.
Stall torques:
about 1 to 128 oz.-in.

PITMO® Gearmotors
2 series: 1.38 & 2.00″ O.D. gearboxes.
Torque limits with standard gearing:
100 & 175 oz.-in.

PITMO® Motor-Tachs
2 series: 1.2 & 1.6″ O.D.
Standard tachometer gradient:
2 volts/1,000 rpm

Samarium Cobalt Field 4-Pole Motors
1.00″ x 1.25″ cross-section.
Stall torques:
12 to 24 oz.-in.

PITMO®

THE PITTMAN CORPORATION
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Harleysville, PA 19438
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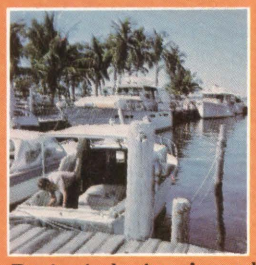

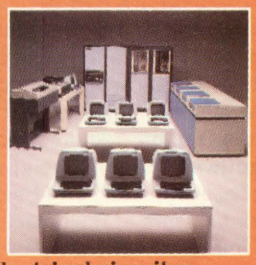

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AIRPAX magnetic circuit breakers are available in so many sizes, capacities and models, you're bound to find exactly what you need with just one phone call to us.

Some models carry up to 600Vac, others up to 125Vdc. We've got models with ratings from milliamps to 100 amps. Choose from mil-spec, UL-listed, UL-recognized, CSA-certified, or SEV-approved models.

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Interested in aesthetics? Choose from models that feature illuminated rocker, colored paddle or baton handles. Just right for front-panel design.

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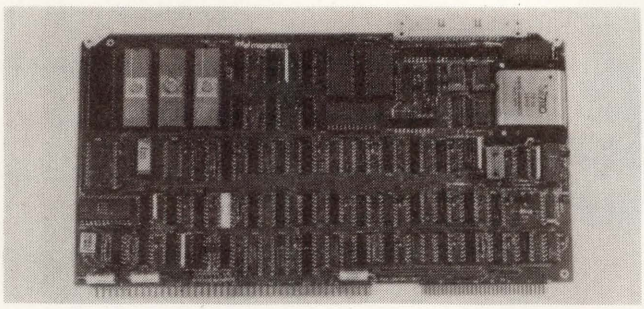
CIRCLE NO. 115 FOR IMMEDIATE NEED
CIRCLE NO. 116 FOR REFERENCE ONLY

1M-BIT BUBBLE MEMORY BOARD



iSBC 250 is a std, 6.75 x 12″ (17.1 x 30-cm) PC board that contains a 7110 1M-bit bubble memory module, an 8085A based controller, and standard components. Designed to interface directly to the Multibus™, the board can be used with the iSBC single-board computer family or in Intellec® microcomputer development systems. The memory contains a 7230 current pulse generator and a 7242 dual formatter/sense amplifier, 2 ICs that provide a power-fail protection and automatic error correction for the board. The device operates with a 40-ms average access time within a temperature range of 0 to 50 °C from std ±12- and 5-V power supplies. When plugged into a Multibus card slot, the bus master CPU communicates with the board's 8085A controller through a set of registers via I/O commands. **Intel Magnetics Inc,** 3000 Oakmead Village Dr, Santa Clara, CA 95051. Circle 209 on Inquiry Card

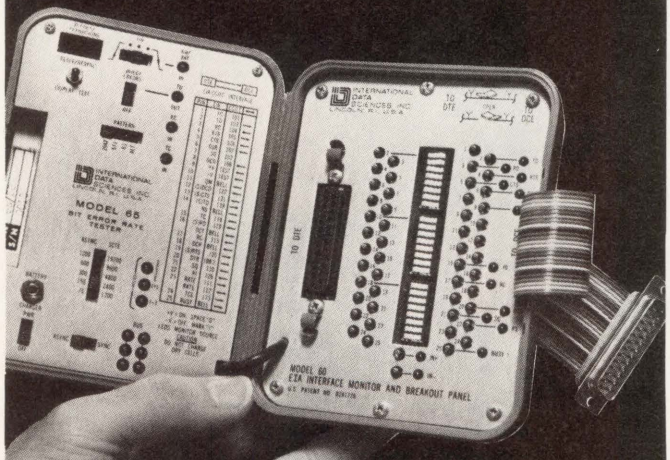
INTELLIGENT DATA SWITCH AND PORT CONTENTION UNIT

Improving service to terminal users and giving the operations manager complete control of access to all computers, TL 460 features user camp-on if a port is busy, console control, call transfers, redundancy, and billing statistics. The unit accommodates up to 4000 terminations and up to 2000 simultaneous cross connects even if all are operating at 9600 bits/s. Terminations may be any combination of ports or lines. Data transparent, the switch requires no changes to existing frontends or software. The unit compares terminal speed and request for access with classes of service authorized for the users, and informs users of their place in the queue if no ports are available. Improved efficiency is achieved by allowing a large number of lines to contend for a limited number of ports. **Infotron Systems Corp,** Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003. Circle 210 on Inquiry Card

The 'Red Box'. Our dynamite duo!

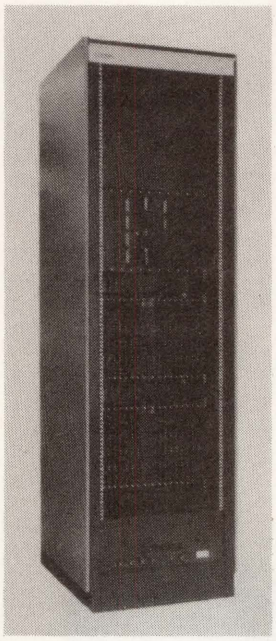
Bit Error Rate Test Set – EIA Interface Breakout Panel in pocket size package.

IDS'S MODEL 65/60 lets you both analyze and test at the EIA interface between a modem and terminal. Combines our popular "Blue Box" model 60 with a new bit error rate test set. All in one light, portable, hard plastic case.
Works on rechargeable batteries. Available now.



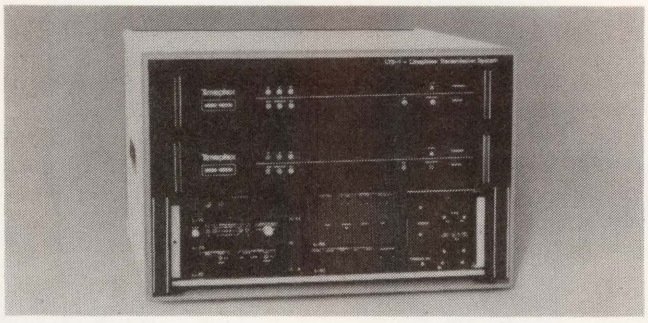
INTERNATIONAL DATA SCIENCES, INC.
7 Wellington Rd., Lincoln, R.I. 02865
Tel. 401-333-6200 TWX 710-384-1911
Export: EMEC, Box 1285,
Hallandale, Fla. 33009 Telex 51-43-32

INTELLIGENT MATRIX SWITCH



A programmable, microprocessor based unit, the intelligent matrix switch (IMS) is an automatic patch panel that makes data channel connections electronically in response to commands entered at a single operator terminal. Programmability allows alternate routing configurations, stored offline in nonvolatile memory, to be loaded online with a single command. This directs the automatic crosspoint switching of any input port to any output port. The terminal controlled digital matrix switching feature provides an operator oriented interface allowing configuration instructions and status reports to be entered and displayed directly on the terminal screen. The IMS also performs analog switching. **Codex Corp,** 20 Cabot Blvd, Mansfield, MA 02048. Circle 211 on Inquiry Card

DATA TRANSMISSION SYSTEM



Lineplexer™ is a complete self-contained transmission system that functions as alternative to wideband facilities required for 19,200-bits/s data service. The system includes Lineplexer II units, M9600 modems, cables, and enclosures. With a system at each end of the circuit, the LTS-1 provides 19.2k-, 14.4k-, 9.6k-, and 4.8k-bits/s operation over voice grade circuits. To accommodate higher data rates, high speed data is split into two data streams, allowing operation over 2 independent telephone channels. System initiates automatic data rate fallback if line degradation prevents operation at the highest desired data rate. Independent channel fallback maintains single channel operation if any channel becomes completely inoperable. **Timeplex, Inc,** One Communications Plaza, Rochelle Park, NJ 07662. Circle 212 on Inquiry Card

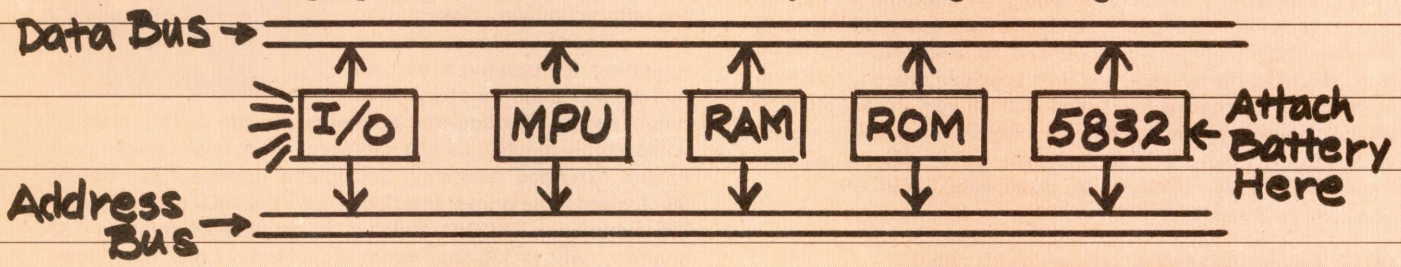
To: D. Richards, Microprocessor Project Manager

From: B. Jones, Design Engineering

Let's Talk!

Subject: A nifty new buck-saving, space-saving solution from OKI - a Realtime MPU Clock/Calendar on a single chip!

This ought to earn us some brownie points: OKI has come up with a Realtime MPU Clock/Calendar, MSM 5832. Timekeeping with a single IC! Now we can substitute just one simple 4-bit CMOS device, for that fistful of discretes we've been kluging into bus-oriented micro systems to get timing.



You're the guy who likes things tidy. Wait till you see how the 5832 tidies up a board...for only $4.80 at 100 pieces. Instead of around $30 for the make-do job. We're talking a whopping cost-saving - over 80%!

Spend less, get more. Even back-up battery operation down to 2.2 volts. So the on-chip 32.768 KHz crystal-controlled time base continues to provide I/O data when main power blacks out:

TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	99	7

You get data access control via 4-bit address, chip select, read, write and hold inputs. Plus a test input, format selection and manual ±30 second correction. All in a single component for a change.

5832 is available now. In volume. We're all fed up with one little MOS circuit in short supply hanging up an entire MPU project. Let's cut the problem down to size, and give OKI a shot in that new system we're working up now. Actually it's so easy to plug in the 5832, we should consider an OKI retrofit anytime any micro system rolls around for a design upgrade.

The coupon attached will get you full specs. Or call Jerry Crowley or Jim Brennan at OKI to save time: (408) 984-4842. (Be sure to ask them to tell you the one about Rex the Wonder Dog!)

B. Jones

P.S. Just found out those hard-to-get 4K CMOS RAMs are easy to get from OKI. We ought to get them in here - OKI's into memory product in a big way!

Please rush specs on:
☐ MSM 5832 Clock/Calendar
☐ 4K CMOS RAMs

Name_____

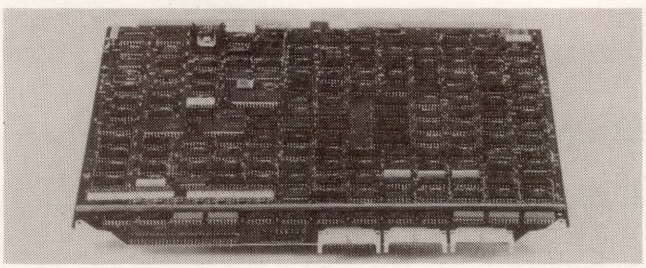
Title_____

Attach coupon to company letterhead (jot down your MPU application for a special deal), and send to: OKI Semiconductor, 1333 Lawrence Expressway, Santa Clara, CA 95051. (408) 984-4842

OKI

CIRCLE 118 ON INQUIRY CARD

INTELLIGENT HIGH DENSITY DISC CONTROLLER



A single-board controller that is plug-compatible with TI-990 minicomputers, the MSC-1990 has operational features such as error correction code, normally found in larger systems, and provides control for up to 3 high density storage module disc drives. Completely resident on one TI compatible board, the unit uses a microprocessor for functional compatibility with the existing TI operating system. It is completely software transparent to the system, and thus provides users with a plug compatible alternative to Trident disc drives. To accomplish this transparency, the unit maps a number of perceived logical units into 1, 2, or 3 of the SMD type drives. **Microcomputer Systems Corp,** 432 Lakeside Dr, Sunnyvale, CA 94086.

Circle 213 on Inquiry Card

HIGH PERFORMANCE MINICOMPUTERS

GA-470 and -480 minicomputers, designed to provide high performance in larger memory configurations, are priced as much as 40% below the company's -460 computer line. -470 is a 240-ns processor with 128k bytes of 22-bit error correcting memory. It includes a comprehensive memory protection subsystem, autoload bootstrap, interactive programmers console, RS-232 and current loop serial I/O interfaces, and chassis with power supply. The -480 is a 240-ns processor with 256k bytes of 22-bit error correcting memory, expandable to 2M bytes. It includes multimap memory management system, autoload bootstrap, interactive programmer's console, RS-232 and current loop serial I/O interface, and chassis with power supply. **General Automation,** 1055 SE St, Anaheim, CA 92803.

Circle 214 on Inquiry Card

300-LINE/MIN BAND PRINTER

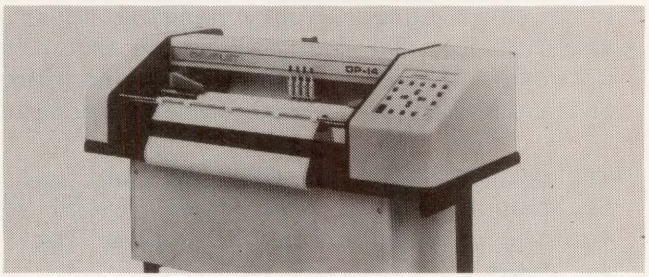
Model 1655 has a stainless steel printband which requires no lubricants and is lighter and easier to maintain than conventional chain printers. Designed for reduced power consumption the printer offers cooler operating temperatures and an automatic band motor drive on/off switch. Friction-free hammers provide quality printing while simple mechanics and microprocessor based electronics ensure extended reliability. Configured to accept 48-, 64-, or 96-char sets, the printer interfaces with the 1600 data processing system in EBCDIC code. It is capable of printing 132 char/line, with a 136-char line option. **Harris Corp, Data Communications Div,** 16001 Dallas Pkwy, Dallas, TX 75240.

Circle 215 on Inquiry Card

ELECTRONIC BADGE READING TERMINAL

Micro-Terminal reads invisibly coded cards through simple hand insertion and communicates with any computer, data and reply, over a single twisted pair. Address polling allows for multiple units on the same data line. The terminal is polled by an address code (30 addresses are jumper selectable) allowing multiple units to be connected in series, limited by voltage and data rates. The reader contains internal battery backup and charging circuit which allows the reader to operate, during a power failure, for more than 1000 transactions over a 1-wk period. Data line is 20-mA current loop (55 V max).**Interlock Inc,** 44 Till Rock Lane, Norwell, MA 02061. Circle 216 on Inquiry Card

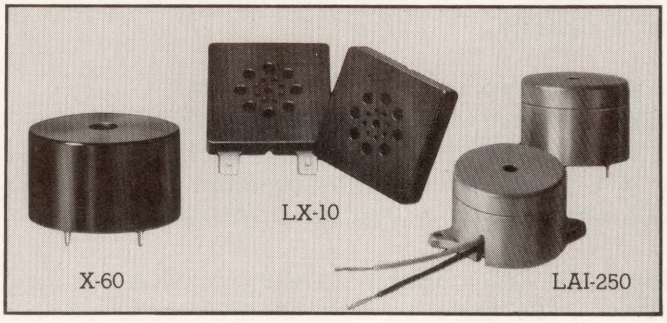
MICROPROCESSOR BASED DIGITAL PLOTTERS



CPS 14/15 systems offer std 4-pen plotting capability under program control and produce 4-color drawings in A, B, C, and D sizes on paper, mylar, or vellum. Comprised of digital plotter and microprocessor based controller, systems are available in widths from 22 to 34″ (56 to 86 cm). Each accepts data from either a std EIA RS-232-C or 20-mA current loop data source and can be operated in online or remote timeshare environment. Systems feature up to 172 firmware generated symbols containing both u/lc alphanumerics, positive paper feed, and circular buffer memory. Writing speeds of 10 and 15 in/s (25.4 or 38 cm/s) are selected by panelmounted pushbuttons. **Houston Instrument,** One Houston Sq, Austin, TX 78753.

Circle 217 on Inquiry Card

Sound Performers.

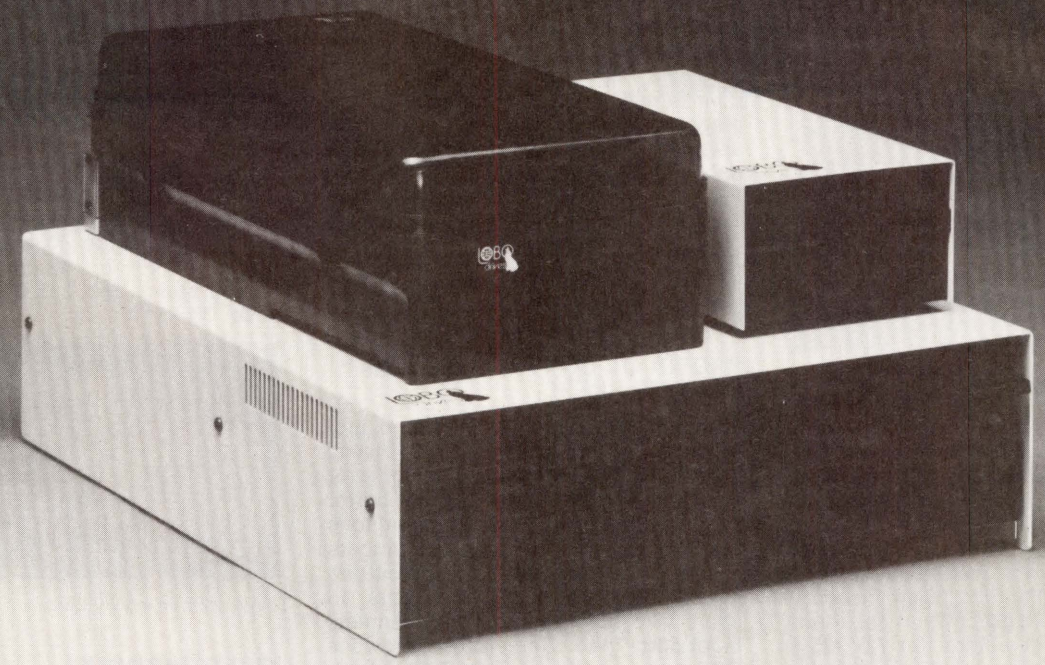


New Low Frequency Piezo Audio Indicators.

54 to 84 dBA at super-low frequencies of 2.0 and 2.3 KHZ make Projects Unlimited's new LAI-250, LX-10, and X-60 piezo audio indicators standout performers. Along with compact size, get 1000 hour-plus design life . . . choice of wires or P.C. pins . . . and from 3.0 to 20 VDC operation. For specs, write: Projects Unlimited, Inc., 3680 Wyse Road, Dayton, Ohio 45414. Phone: (513) 890-1918. TWX: 810-450-2523.

projects® unlimited

NEW FROM LOBO:

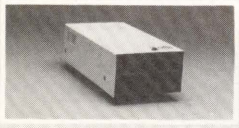


An Entire Family of Disk Drives for APPLE, TRS-80*, and S-100 Computers

Only LOBO DRIVES offers you an entire family of fully-compatible disk drives to select from. Whatever computer you're using, APPLE, TRS-80, or S-100, you can add a LOBO drive now, with the peace-of-mind of knowing there's a whole family of drives available when you're ready to expand.

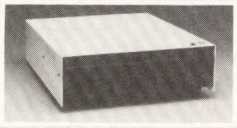
And every drive you order comes complete with chassis and high reliability power supply. Each drive is 100% calibrated, burned-in, and performance tested on either an APPLE, TRS-80, or S-100 computer before it's shipped. We are so proud of our drives . . . our quality, reliability, and performance, that we back-up every drive with a one year, 100% parts/labor warranty.

400 SERIES FLOPPY DISK DRIVES



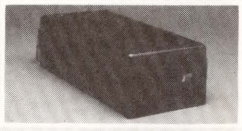
Meet our low-cost 5.25-inch mini drive that records data in either hard or soft sectored format. It is available in single or double density configurations, with a total storage capacity of 220K bytes.

800/801 SERIES FLOPPY DISK DRIVES



Here is our dual 8-inch Floppy disk memory unit. It records and retrieves data on standard 8-inch diskettes to provide 800K bytes of data storage unformatted, or 512K bytes in IBM format per drive. It is also available with double-sided, double-density capabilities, for a maximum storage capacity of 1.6 Megabytes.

7000 SERIES HARD DISK DRIVES



The latest member of our drive family, the Series 7000 is an 8-inch, 10 Megabyte Winchester Technology, hard disk drive. It is fully hardware/software compatible and comes complete with disk controller. Now you can have the convenience, speed, reliability, and all the storage capacity you need.

Call or write for the complete LOBO DRIVES story. Find out just how competitively priced a quality drive can be.

Quantity discounts available –
Dealer inquiries invited.

Yes, I want to know more about LOBO Drives and what they can do. Send me information on:
☐ TRS-80 ☐ APPLE ☐ S-100

☐ 5 1/4-in. Floppy drive
☐ 8-in. Winchester hard disk, 10 Mbyte drive
☐ 8-in. Floppy drive Single sided Double sided
☐ Double density expansion interface

Name _____
Company _____
Address _____
City _____ State _____ Zip _____
Phone No. _____
If dealer, provide resale no. _____

LOBO drives INTERNATIONAL

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Goleta, California 93017
(805) 685-4546

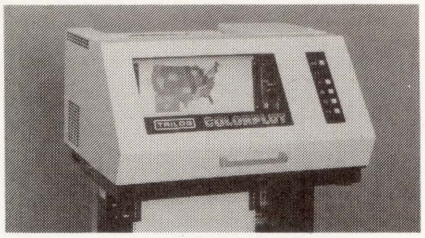
"CAN YOU REALLY AFFORD TO PAY LESS?"

*TRS-80 is a registered trademark of Radio Shack, a Tandy Company.

CIRCLE 120 ON INQUIRY CARD

PRODUCTS

COLOR COPIER FOR CG TERMINALS



Colorplot C-144 can do double duty: the unit makes multicolor hardcopies from Chromatics CG series terminals on plain fanfold paper; it also operates as a line printer at 190 lines/min with a 96-char u/lc set. In multicolor mode, hardcopies are made with the Tri-Color ribbon and bidirectional paper drive system. It uses raster scan impact technology with a resolution of 100 dots/in (39/cm) horizontal and 144 dots/in (57/cm) vertical, forming a symmetrical picture 10 x 7.5″ (25.4 x 19 cm) high. **Trilog, Inc,** 17391 Murphy Ave, Irvine, CA 92714.

Circle 221 on Inquiry Card

RANDOM ACCESS MODEM

RAM-11 uses advanced carrier current techniques to transmit digital information over ac power lines with low bit error rates. Wireless random access offers versatility in interconnecting office products and data terminals, allowing random formation of data paths by simply plugging into an ac power outlet. The asynchronous modem is capable of full-duplex transmission at up to 9600 baud. RS-232-C interface is std. **Data-Control Systems,** PO Box 860, Commerce Dr, Danbury, CT 06810.

Circle 222 on Inquiry Card

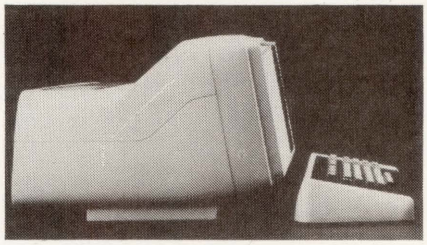
PROTOCOL CONVERTER WITH 32k-BYTE BUFFER

Procon III Data merging buffered protocol converter receives 2770 bisync data and stores up to 32k bytes of error free data in its semiconductor buffer memory. It also receives asynchronous data that normally passes through to its asynchronous output port, permitting asynchronous and bisync inputs to share a common computer or terminal input port. The bisync protocol provides CRC error checking. **Epic Technology,** 2730 NW 1st Ave, Boca Raton, FL 33432.

Circle 223 on Inquiry Card

MULTIPLE PROTOCOL COMPUTING TERMINAL

Interfacing with all major mainframes, the model 4000 offers communications multiprotocol options for IBM, Burroughs, Honeywell, NCR, ICL, Univac, DEC, HP, and others. An information resource management terminal, the unit is designed for distributive information networks and as a companion to the model 4500. Features include printer interfaces to Centronics 700 series, Diablo Hy/Type, DEC LA series, NEC Spinwriter, and Teletype Model 40; and communications at 75 to 19.2k baud. **ECS Microsystems, Inc,** 215 Devcon Dr, San Jose, CA 95112.



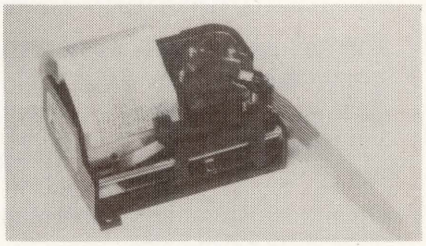
Circle 224 on Inquiry Card

VIDEO TERMINAL

The MDL-6053 emulates the operating features of the Data General Dasher line of video terminals. Each of the 10 function keys issues two distinct codes when used in combination with the shift and control keys. Other std features include the 12″ (30-cm) green phosphor nonglare CRT with high resolution 9 x 14 dot char cell, EIA RS-232-C and 20-mA current loop interfaces on main port, 10 externally selectable baud rates from 75 to 19.2k baud. **Cybernex Ltd,** 2457 Dunwin Dr, Mississauga, Ontario L5L 1T1, Canada.

Circle 225 on Inquiry Card

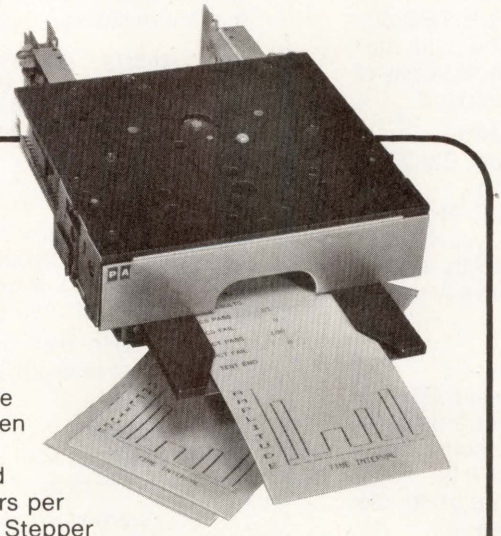
MINIATURE ALPHANUMERIC PRINTERS



Microprinters print either on electrosensitive paper (model EUY-2E) or thermally sensitive paper (EUY-2T). Both versions print 15 char/line. Characters are formed by a 2.7-mm high 7 x 5 matrix. The -2E can print 2 lines/s, while the -2T prints at 1.5 lines/s. Both versions measure 72-mm wide x 33.5-mm high x 56-mm deep and print on 36-mm wide paper. Expected life of the units is 5 x 10^5 lines. The -2E requires 5 and −31 Vdc, while the -2T takes 5 Vdc only. **Panasonic,** 1 Panasonic Way, Secaucus, NJ 07094.

Circle 226 on Inquiry Card

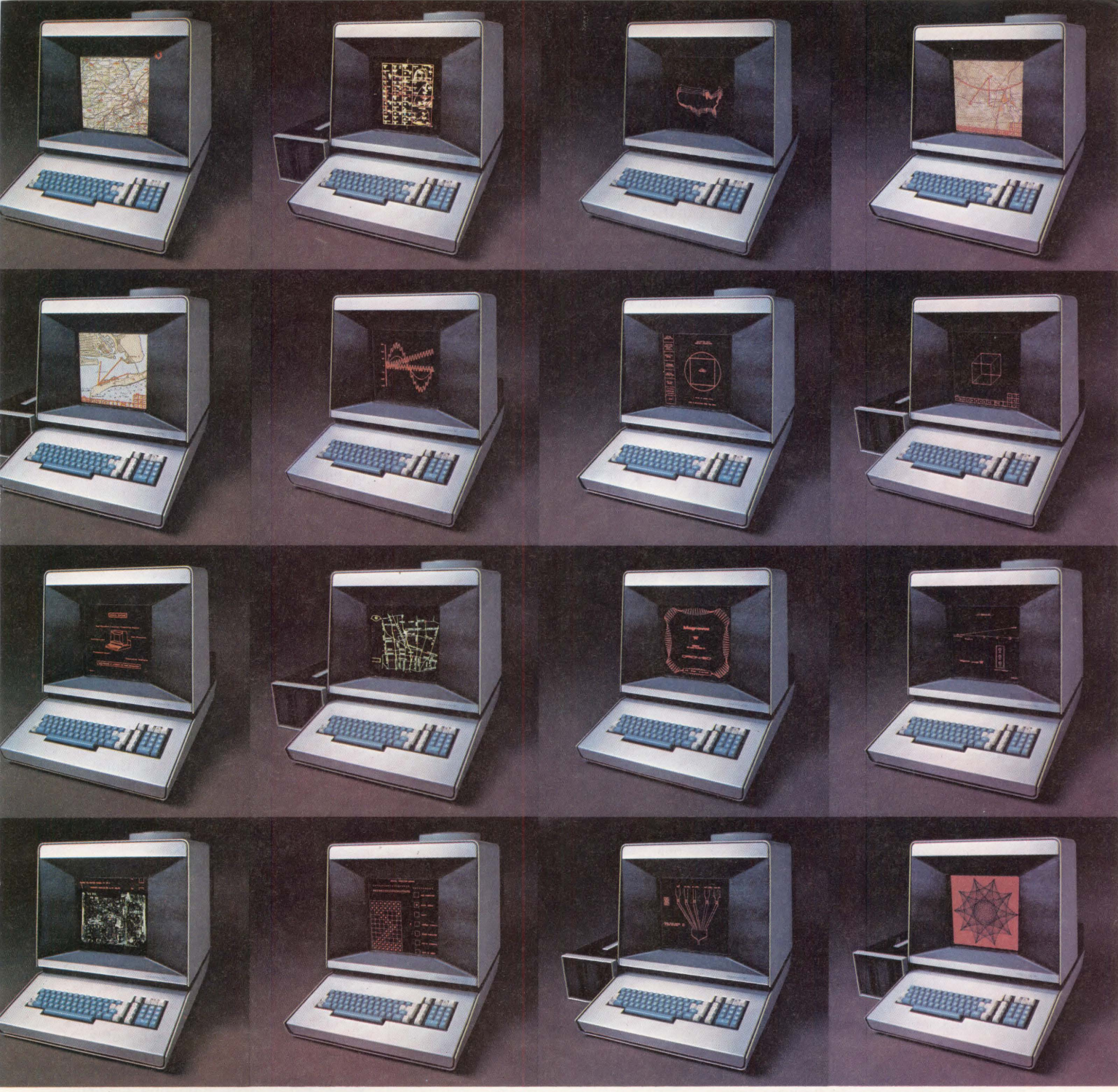
Our Alphanumeric Ticket Printer



For total versatility use our DMTP-9 programmable ticket printer to print the full alphanumeric ASCII character set. Print with ribbon on standard tickets, cards or single-sheet forms, or use impact-sensitive paper for multiple copies. Even program character pitch to handle standard or enhanced printing of up to 48 characters per line on 39- to 59-line tickets. Stepper motor advance for 6 lines to the inch or .110″ for graphics.

Mountable on tabletop or wall, the DMTP-9 does it all with advanced stepper motor control electronics and a long-life needle matrix print head. For still more versatility, get it with the optional controllers, power supplies and interconnect cables systems for complete microprocessor/microcomputer compatibility, too. But first, write or call to get more details. Ask for Bulletin 924.

P A **PRACTICAL AUTOMATION, INC.**
Trap Falls Road, Shelton, Conn. 06484/Tel: (203) 929-5381



WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60 STANDS ALONE.

A display terminal that won't stand alone can't be as versatile or as adaptable as the Orion-60, the modular plasma display system that stands by itself or interfaces with existing hardware to let you create your own programs.

To begin with, the Orion-60 is an easy touch: besides offering full alphanumeric, floppy disc and rear-projection capabilities, it lets you create displays and enter data simply by touching the screen with your finger.

That means you can project a slide onto the screen coordinates and plot your own course over it. You can program your own character sets. You can generate vectors of any length to absolute screen coordinates. In short, you'll have a flexible terminal that will keep up with your needs today—and grow with your operations tomorrow.

Of course, since Magnavox was a leader in the development of plasma terminals, you can be sure your Orion-60 will have a bright, high-contrast display free from jitter and distortion.

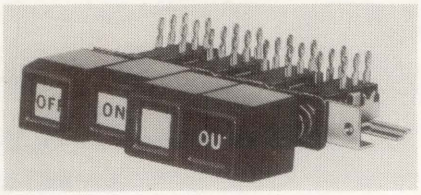
There's a lot more you should know about the ways this remarkable terminal can help you get more out of graphic displays. For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 S. Coliseum Blvd., Ft. Wayne, IN 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

CIRCLE 121 ON INQUIRY CARD

PRODUCTS

MULTIPLE-STATION PUSHBUTTON SWITCH



Subminiature Tini DW Multi-Switch, series 92000 features the snap slide switching technique and a variety of mechanical functions, such as interlock, nonlock, push-lock/push-release, and all lock switching. The pushbuttons are slightly separated on 15-mm centers. Other characteristics include up to 8-C (8pdt) switching per station, full 0.5 A, 125 Vac or dc rating, and a choice of std solder lugs or printed circuit terminals. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630

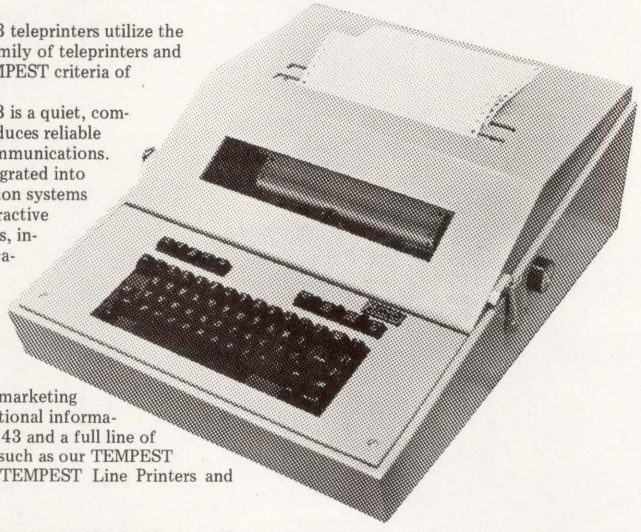
Circle 227 on Inquiry Card

TEMPEST T5143 TELEPRINTER

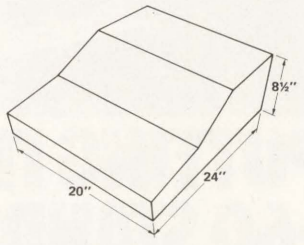
The TEMPEST T5143 teleprinters utilize the TELETYPE® Model 43 family of teleprinters and are tested to meet the TEMPEST criteria of NACSEM 5100.

The TEMPEST T5143 is a quiet, compact teleprinter which produces reliable and economical printed communications. This unit can easily be integrated into most existing communication systems in use today, making it attractive for a variety of applications, including message communications, time sharing, computer I/O and more. The T5143 is an outstanding value with its initial low price and dependable performance.

Why not contact our marketing department today for additional information on the TEMPEST T5143 and a full line of other TEMPEST products such as our TEMPEST VIDEO DISK SYSTEM, TEMPEST Line Printers and TEMPEST CRT'S.



- Pin feed prints up to 72, 80, or 132 char/line at 13 Char/in and 6 line/inch on fan-fold forms 12 inches wide.
- 9-wire dot matrix impact printhead.
- Prints full 94 ASCII character set (upper/lower case).
- 64-character Received Data Buffer.
- Typewriter-like keyboard generates full 128 ASCII.
- Back Space, operator and on-line.
- N-Key Rollover: 8-character burst buffer.
- Caps Lock, Repeat, Return, Line Feed, Shift and Control keys.
- Transmission Asynchronous at 110 or 300 BPS.
- Code: 1968 ASCII.
- Interface: EIA (RS232) (MIL STD 188C optional).



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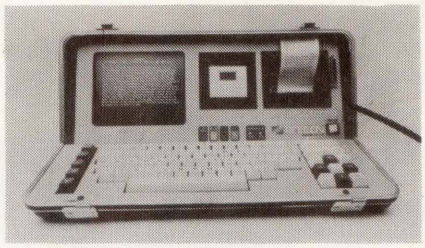
SYSTEMATICS GENERAL CORPORATION
National Scientific Laboratories Division
2922 Telestar Court, Falls Church, VA 22042 Attn: Marketing Division
Telephone: (703) 698-8500 TWX 710-831-0840

PORTABLE CRT PRINTING TERMINAL



The Ambassador I, combining full screen capability and hard printing in one typewriter size case, weighs less than 17 lb (7.6 kg) and fits under aircraft seats. Features include instantaneous cassette memory up to 80k, auto word, and text editing. The terminal permits communications anywhere in the world, via std ANPA bureau protocol, conventional or timesharing, with transmission in 5-, 6-, 7-, or 8-level code at a keyboard selectable data rate anywhere from 45.5 to 9600 baud. **Telcon Industries,** 1401 NW 69th St, Ft Lauderdale, FL 33309.

Circle 228 on Inquiry Card

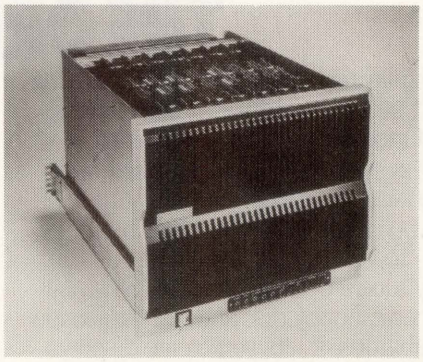
BAND PRINTER

Map P/ROMs control the band in the LP25 285-line/min printer. The -AA model has a 64 ASCII char set. The -BA version features user replaceable fonts, up to 3 co-resident map P/ROMs, and an optional 96-char set. Optional bands print 15 char/in (6/cm) rather than the std 10 char/in (4/cm). European and Japanese char set bands are optional. Universal power supply is jumper-plug adjustable. **Digital Equipment Corp,** 444 Whitney St, Northboro, MA 01532.

Circle 229 on Inquiry Card

DISC EMULATION SYSTEM

BC-301R Bulk Core Fixed Head Disc emulation system for Rolm's 1602 minicomputer emulates the Rolm 3340 Disc Control and Fixed Head Disc. The 7″ (18-cm) disc system contains two 256k-byte bulk core modules, for a max capacity of 512k bytes. The 15.75″ (40-cm) chassis holds 8 bulk core modules, with a max capacity of 2.0M bytes. The avg access time is 2.0 μs and the data transfer rate is 4.0 μs for a 16-bit word. Parity generation and checking are std. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512.



Circle 230 on Inquiry Card

The accelerating growth in modem technology at Universal Data Systems has now produced the Company's first 9600 bps unit on a super-compact OEM board. Occupying about 100 square inches of PCB space, this microprocessor LSI modem offers dramatic space savings for designers who wish to package data sets internally in microcomputers, minicomputers or interactive terminals. The traditional UDS economy and reliability are inherent in the new 9600 bps modem.

Contact UDS for complete technical details, or phone your UDS representative. Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone: 205/837-8100.

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CIRCLE 123 ON INQUIRY CARD

PRODUCTS

COMPUTER INTERFACE FOR SELECTRIC TYPEWRITER

ESCON (Electronic Selectric Conversion) interface unit converts any IBM Selectric typewriter (model 72 or 82) into a letter quality computer output printer. Models are offered for such small computers as the Commodore PET and the Radio Shack TRS-80. RS-232, S-100, IEEE-488, and Centronics compatible models are for general purpose use. Installation is completed in approx 6 h using ordinary hand tools. All necessary mounting hardware is included. **iPex International, Inc,** 16140 Valerio St, Van Nuys, CA 91406.

Circle 231 on Inquiry Card

For demanding applications

SUMMAGRID™

The full-sized digitizer with uncompromising accuracy

Designed to meet the rigid requirements of aerial cartography, integrated circuit layout, printed circuit board design, architectural drawing and other uses where dependable accuracy and resolution are required, Summagrid delivers *provable* —

RESOLUTION: 0.001″ (0.025mm)

ACCURACY: ±0.005″ (0.125mm)

Despite variations in temperature and humidity.

Available in opaque or backlighted models with active areas as large as 42 by 60 inches. A product of the world's largest digitizer manufacturer.

Designed for easy integration into almost any data processing system, it offers RS232, IEEE and 8/16-Bit Parallel interfacing. A wide range of accessories and programming features are available.

If accurate digitizing is important in your system, you should ask for full details on Summagrid.

Summagraphics corporation

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(203) 384-1344 • Telex: 96-4348

CARTRIDGE DISC DRIVES

Vanguard I is available in 5M-, 10M-, and 20M-byte versions and is compatible with existing cartridge disc drives and interfaces. Design enables use for data backup on large scale disc pack oriented systems. 24″ (61-cm) depth fits into small business computer systems and meets size requirements for desk mounted peripherals. The drive can be disassembled to basic subassemblies in <7 min, and reassembled quickly with minimum tools. **Perkin-Elmer Corp, Memory Products Div,** 7301 Orangewood Ave, Garden Grove, CA 92641.

Circle 232 on Inquiry Card

INTEGRATED LED LAMPS

HLMP-31XX and -36XX series combine LED, current limiting resistor, and reverse protection diode in a subminiature, TTL compatible package. A 5-V source directly drives the HLMP-3105 (std red), -3600 (high efficiency red), -3650 (yellow), or -3680 (green) devices. HLMP-3112 (std red) is designed to interface with a 12-V source. Available in panel mountable T-1¾ package, each device features 0.64-mm sq leads that are suitable for wirewrapping. Lamps exhibit viewing angle of 90°. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 233 on Inquiry Card

MAGNETIC SWITCHING REGULATOR

Two modules, the 5TR200/160-S1 and the -S2, each measuring 2 x 4 x 1.3″ (5 x 10 x 3.3 cm) comprise a 5 V at up to 20 A magnetic switching system. The modules are designed to operate from 40 V peak, 20- to 40-kHz square wave with any input module or set of modules with sufficient power rating. The dc output voltage is regulated by a magnetic switching phase control. The units have 78% typ efficiency and offer overvoltage/overcurrent protection. **Powercube Corp,** 8 Suburban Pk Dr, Billerica, MA 01821.

Circle 234 on Inquiry Card

ANTIREFLECTION, CONTRAST ENHANCEMENT CRT FILTERS

Retrofit kit eliminates reflection problems and improves display contrast on existing CRT displays. Kit consists of CP-70 circular polarizer contrast enhancement filter and self-adhesive mounting brackets that attach to bezel around display screen. Operator eye fatigue is reduced by improved readability of displayed material and elimination of reflection of ambient light back into operator's eyes. **Polaroid Corp, Technical Polarizer Div,** Cambridge, MA 02139.

Circle 235 on Inquiry Card

ENGLAND KNOWS TOSHIBA DELIVERS 14 MILLION 16K DYNAMIC RAMs A YEAR.

In England it's no secret that Toshiba delivers. More than a million 4116-type 16K Dynamic RAMs every month. In all three speeds: 150, 200 and 250 nanoseconds. And with all that volume, our actual customer rejection is less than 1/10 of 1%! Much less. That's documented quality. Toshiba quality. They know all about it in England. All around the world, in fact. You can find out, too. Just give us a call.*

CIRCLE 125 ON INQUIRY CARD

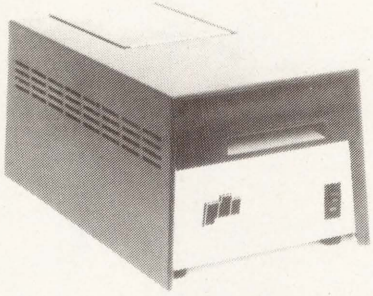
TOSHIBA AMERICA, INC.

People around the world have fond memories of us.

*Ask for our Memory and Microprocessor Product Guide while you're at it. We'll be happy to send you a copy.
Toshiba America, Inc., 2151 Michelson Drive, Suite 190, Irvine, CA 92715 (714) 955-1155

PRODUCTS

BROAD SPECTRUM MARK-SENSE READER

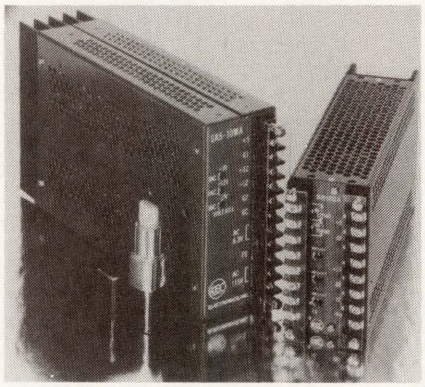


Series of information processing peripherals combines a hand fed reader and a broad spectrum sense head in a miniaturized, self-contained unit for use in a wide range of data acquisition systems. The broad spectrum head enables the series 100 MBS readers to read various marking instruments, including felt-tip markers, ballpoint pens, pencils, and other normally available writing instruments. **Peripheral Dynamics, Inc,** 1730 Walton Rd, Blue Bell, PA 19422.

Circle 236 on Inquiry Card

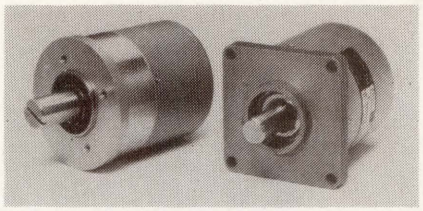
MULTIPLE-OUTPUT SWITCHING POWER SUPPLIES

SAM and SBM series feature 115- and 230-Vac inputs, 3 output voltages that are individually adjustable, brownout protection, tight regulation, and MTBF of 100k hours. SAM units are available with outputs of 5 V at 10 A and any 2 combinations of ±12, ±15, 9, or −5 V at 1 A. Regulation is 0.3% line and 0.8% load from no load to full load. SBM series is available with outputs of 5 V at 5 A and any 2 combinations of ±12, ±15, 9, or −5 V at 0.5 A. **KEC Electronics, Inc,** 21535 Hawthorne Blvd, Torrance, CA 90503.



Circle 237 on Inquiry Card

HEAVY DUTY ABSOLUTE SHAFT POSITION ENCODER



Developed to withstand industrial environments the heavy duty model 76 features a large shaft and rugged bearings that can withstand shaft loading of up to 70 lb (32 kg). Supplied in gray code, natural binary, or 8421 binary coded decimal, the unit offers choice of 10 resolutions with DTL and TTL compatible outputs. The rugged frame is available in two mounting configurations. Measurements are 3 x 2.65″ (7.6 x 6.73 cm). **Litton Encoder Div,** 20745 Nordhoff St, Chatsworth, CA 91311.

Circle 238 on Inquiry Card

INTELLIGENT FLEXIBLE DISC SYSTEM

Comprised of Shugart 8″ (20-cm) flexible disc drive, microprocessor based controller, and firmware package, Instor/80 uses IBM 3741 floppy disc format (IBM diskette 1), producing diskettes that are read/write compatible with IBM systems and peripherals, including 3741 and 3742 data entry stations and Systems/32 and /34. The unit interfaces via an RS-232-C asynchronous port and requires only a few operating system commands to communicate with user's system. **Instor Corp,** 175 Jefferson Dr, Menlo Park, CA 94025.

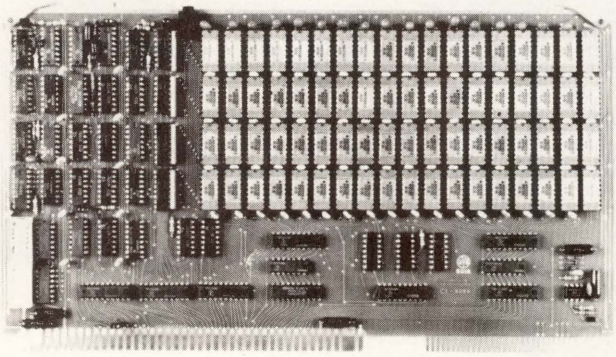
Circle 239 on Inquiry Card

MIL-STD-1553 TRANSCEIVER

Low power hybrid transceiver for use with the military's 1553 interface data bus, the BUS-8553 has a specified external transformer (BUS-25679). The hybrid is one section of a modular remote terminal whose function is to receive or transmit 1-MHz serial data between the bus and a Manchester II encoder/decoder as instructed by the bus controller. The TTL compatible device meets MIL-STD-883 and 38510. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.

Circle 240 on Inquiry Card

128K X 9 MULTIBUS MEMORY
Only $1500



WE'VE DONE IT AGAIN — State of the Art Multibus® Memory Design. First to offer up to 512K on one board, and Chrislin again brings pricing sanity to the memory market. Why pay over $2000 for our competitor's 64K x 8 memory board when we will give you the CI8086 128K x 9 memory for just $1500 or better yet, the CI8086 512K x 9 memory module for $8700.

Up to 512K bytes in a single option slot. Available in 64K, 96K, 128K, 256K or 512K configurations. On board parity generator checker, for both 8 bit or 16 bit systems. Off shelf deliveries.

DON'T ASK WHY WE CHARGE SO LITTLE, ASK WHY THEY CHARGE SO MUCH.

Multibus is a trademark of the Intel Corp

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Computer Products Division
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Sylvania breaks the color barrier.

Introducing America's first 19-inch color data display tube.

Not just a tube with color.

A tube with gorgeous, glorious, sharp Sylvania color.

Color that provides clearer images and better contrast than anything available anywhere.

Color that makes small characters a breeze to read, with less fatigue.

Crystal clear color created by a high density tri-dot mask.

Color sharpened by a multiple-beam electron gun and enhanced by a Chromatrix dark surround negative guard band, and a rare earth phosphor system.

Sylvania color.

It's completely changed the picture in data display tubes.

Write Product Marketing Manager for our latest catalog:

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Data Display Tube Division
700 North Pratt Street
Ottawa, Ohio 45875

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CIRCLE 126 ON INQUIRY CARD

"I went flat instead of fluffy."

"As an engineer, I used to get pretty frazzled whenever I had to use twisted pairs.

Heaven knows, I needed the performance, but the labor costs drove me wild!

Then one day Dave from Spectra-Strip stopped by and solved all my problems—he showed me their new Twist 'N' Flat.®

How fantastic—twisted pairs in a flat cable with flat, parallel sections that I can mass terminate wherever I need them on the cable. (Standard spacing is 18″ of twist with 2″ of flat, but if I order as little as a thousand feet at one time, they'll put in any spacing I want!)

Well, let me tell you—this has reduced termination time by 97% and cut our costs by 36%. I liked their thinking so much, I checked them out and found that they were a terrific source for all my flat cable needs—cable, connectors, and even complete terminated jumpers and custom assemblies, fully tested and ready to go.

If you're as concerned about your interconnect performance and costs as I am, you really ought to write Spectra-Strip, 7100 Lampson Avenue, Garden Grove, CA 92642, telephone (714) 892-3361. In the East, call (203) 281-3200.

But don't ask for Dave—he's at home taking care of the baby."

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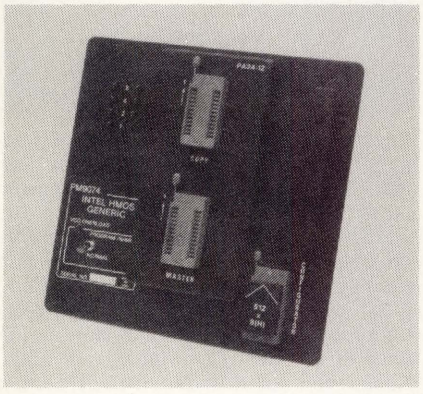
SPECTRA-STRIP An Eltra Comp

When you're down to the wire.

CIRCLE 152 ON INQUIRY CARD

PRODUCTS

PROGRAMMER MODULE FOR 2732A EPROM



A generic module that enables Series 90 P/ROM programmers to program Intel's 2732 HMOS EPROM, the PM9074 generic personality module also accommodates other HMOS EPROMs and higher density P/ROMs (for example, 64k P/ROMs) as they are developed. When plugged into a series 90 P/ROM programmer master control unit, the module provides the control lines and timing necessary to list, program, duplicate, and verify these devices. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 241 on Inquiry Card

KEYBOARDS

Thinswitch, a hi-rel, sealed keyboard designed for severe environment applications, meets requirements of MIL-E-16400 and MIL-E-5400. The momentary contact spst device has row/col outputs in 3 x 4, 4 x 4, and 4 x 5 configurations. Panelswitch features illuminated pushbutton keys and low profile lightweight construction. Momentary contact spst action with discrete outputs and common ground in 3 x 4 and 4 x 4 configuration is std. Thriftswitch is designed for commercial keyboard applications needing a low profile, reliable mechanical switch matrix. **Industrial Electronic Engineers, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405.

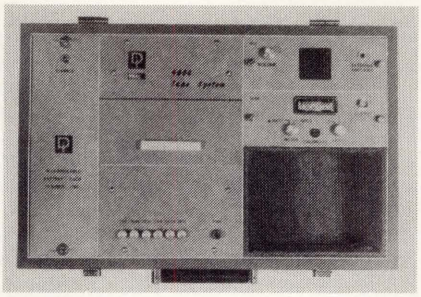
Circle 242 on Inquiry Card

LOW INDUCTANCE CAPACITORS

Aluminum electrolytic capacitors offer 5- to 6-nH inductance due to internal construction; terminal tabs extend from the wound-foil electrolyte one above the other, separated by an insulator, with fully interactive electromagnetic fields. For high frequency applications from 20 to 400 kHz, type 350 units are packaged in enclosures, that mechanically secure a conventional internal wound section within the case. **Sangamo Capacitor Div, Sangamo Weston, Inc,** PO Box 128, Pickens, SC 29671.

Circle 243 on Inquiry Card

INSTRUMENTATION TAPE RECORDER



Series 4000 cassette recorders are battery powered, lightweight instruments, offered in single-channel fm record/reproduce or optional 4-channel, 4-speed fm record only versions. Both offer voice record/playback capability. At 3.75 in/s (9.52 cm/s) data frequencies of dc to 2000 Hz may be recorded. Optional speeds provide proportional frequency response capability. A meter indicates peak level of recorded signal and monitors condition of battery. **Dallas Instruments, Inc,** 10205 Plano Rd, Dallas, TX 75238.

Circle 244 on Inquiry Card

LOW COST EDGE CONNECTOR

Contact loading concept and selective plating reduce manufacturing costs of CARDCON connector while staying within performance parameters of MIL-C-21097. A CDA 260 spring brass contact is plated with 20 μin (0.51 μm) of gold over 50 μin (1.3 μm) of copper on the contact area. Tails are plated with gold flash over 50 μin (1.3 μm) of copper. The connector is loaded from the rear and snapped into the UL rated 94-VO insulator. **TRW Cinch Connectors, TRW, Inc,** 1501 Morse Ave, Elk Grove Village, IL 60007.

Circle 245 on Inquiry Card

GRAPHIC CONTROLLERS

Magnetic tape readers models 916 and 920 are interconnecting devices between the user's online controller and host computer; controller models 918 and 922 are intelligent interconnecting devices between the company's plotters and host computers. All are freestanding units with a 10.5″ (26.7-cm) read only magnetic tape transport, control panel, and operator message display. Tape formats include 7-track 200, 556, and 800 bits/in (79, 219, and 315/cm); and 9-track 800 and 1600 bits/in (315 and 630/cm). **California Computer Products, Inc,** 2411 W LaPalma Ave, Anaheim, CA 92801.

Circle 246 on Inquiry Card

FREE. 1980 JADE Computer Products catalog chuck full of special inflation fighting prices. Send for it today.

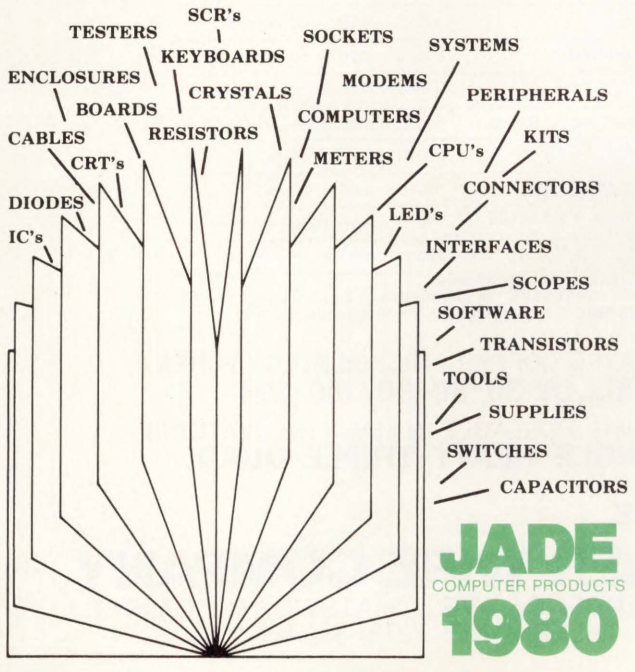
Name _____ Phone _____

Company _____

Address _____

City/State/Zip _____

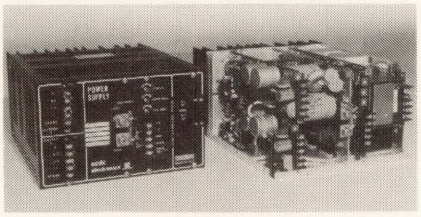
JADE Computer Products 4901 W.Rosecrans, Hawthorne, CA 90250



For customer service or technical inquiries call 213-973-7707

PRODUCTS

300-W, 3-OUTPUT SWITCHING POWER SUPPLIES



RS/RT switcher models use isolated auxiliary outputs and 115/230-Vac inputs that are internally changeable to 180 to 264 Vac. Std units meet VDE0875 for emi and optionally meet input isolation requirements of VDE0804. Designated RT305 at 5 V/60 A, 15 V/4 A, and 12 V/5 A; RT306 at 5 V/60 A, 24 V/2 A, and 12 V/5 A; and RT307 at 5 V/60 A, 24 V/2 A, and 15 V/4 A, all are packaged in std 5 x 8 x 10″ (12.7 x 20.3 x 25.4 cm) T30 cases with 300-W total power rating. **ACDC Electronics, Div of Emerson Electric Co,** 401 Jones Rd, Oceanside, CA 92054.

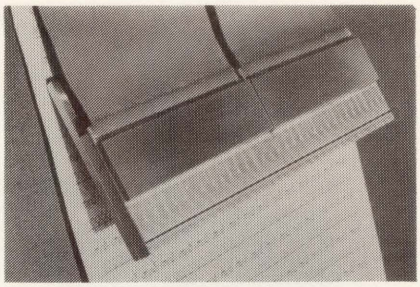
Circle 247 on Inquiry Card

FULL COLOR GRAPHICS OUTPUT DEVICE

Videoprint 3000 and 5000 series equipment eliminates problems associated with off the screen photography and other hardcopy computer graphics reproduction methods. Both systems are self-contained and fully automatic for minimizing optical distortion, with color, brightness, and exposure adjustments under microprocessor control. Both produce 4 x 5″ (10 x 12-cm) hardcopy prints in seconds. Also available are Polaroid SX-70 and 35-mm sizes. **Image Resource,** 2260 Townsgate Rd, Westlake Village, CA 91361.

Circle 248 on Inquiry Card

PREGANGED THERMAL PRINTHEAD ASSEMBLIES



Factory preganged, yet individually adjustable and replaceable, GM series thermal printheads offer dot densities from 50 to 100 dots/in (20 to 40/cm). Printing widths range from 4.1 to 8.9″ (10 to 23 cm). Rigid edge to edge mounting and precise fabrication makes the printing gap between printheads virtually undetectable. Using 5 x 7 dot matrix char, up to 132 col of printing may be attained. **Hybrid Microcircuit Dept, Gulton Industries, Inc,** 212 Durham Ave, Metuchen, NJ 08840.

Circle 249 on Inquiry Card

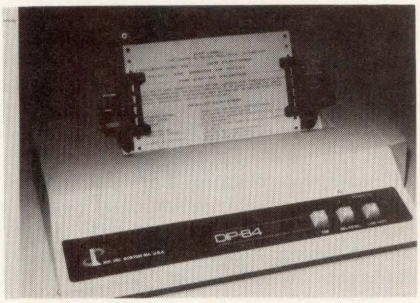
MAG TAPE SYSTEM FOR UNIBUS COMPUTERS

Tridensity magnetic tape storage system for PDP-11 and VAX 11/70 computers, the 806 tape system, enables DEC users to record in 6250-(GCR), 1600-(PE), and 800-(NRZI) bit/in (2460, 630, and 315-bit/cm) formats and to store more than 150M bytes on a single 2400′ (730-m) reel. The max data transfer rate of 780k bytes is nearly 4 times faster than the fastest conventional 1600-bit/in (630/cm) system. **Aviv Corp,** 6 Cummings Pk, Woburn, MA 01801.

Circle 250 on Inquiry Card

DOT MATRIX IMPACT PRINTER

DIP-84 is a low cost, high reliability, dot matrix impact printer, with tractor paper feed. It features 7 x 7 or expanded 14 x 7 matrix printing, u/lc char set, 100-char/s bidirectional printout, roll or fanfold paper, ribbon cartridge loading, and low profile. Tractor adjusts for paper from 2.5 to 9.5″ wide (6.3 to 24.1 cm) and is stepping motor controlled for better forms control. With full 96-char ASCII set, unit prints both u/lc at 80, 96, or 132 char/line on 8.5″ (21.6 cm) paper. **DIP, Inc,** 121 Beach St, Boston, MA 02111.



Circle 251 on Inquiry Card

magnet wire

FINE & ULTRA FINE

INSULATIONS AVAILABLE - SINGLE

INSULATION	TEMP RATING	SIZE RANGE	NEMA SPEC.
POLYURETHANE	105°C	AWG 31-56	MW-2C
Vinyl Acetal FORMVAR	105°C	AWG 31-46	MW-15C
SELF-BOND (POLY)	105°C	AWG 31-56	MW-3C
Polyurethane-Nylon POLY-N 130	130°C	AWG 31-56	MW-28C
SELF-BOND (POLY/NYLON)	105°C	AWG 31-56	MW-29C
SELF-BOND (Polyamide) (Polyamide Outercoat)	120°C	AWG 31-56	N.A.
*SOLDERABLE Modified POLYURETHANE 150	150°C	AWG 31-56	N.A.
*SOLDERABLE POLYESTER 170 ESTERMIDE 170	170°C	AWG 31-56	MW-26C
Modified Polyester ESTERMIDE 180	180°C	AWG 31-56	MW-30C

*UL & MILITARY SPECIFICATIONS
NOTE: POLYURETHANE 150 - Solderable in 2 to 3 seconds at 370°C.
ESTERMIDE 170 - Solderable in 2 to 3 seconds at 450°C.

INSULATED COPPER - NICKEL ALLOY WIRES -
ALLOY 30-60-90-180-294

30-44 AWG AVAILABLE IN MANY INSULATIONS -
SINGLE-HEAVY-TRIPLE-QUAD

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TELEPHONE: (213) 882-8311

DIGI-DATA SERIES 40

the more OEMs demand of tape systems, the more we deliver.

OEMs are demanding. They want different models for different applications, the highest possible reliability, and value that reflects in their final product. Our Series 40 continues the 17 year Digi-Data tradition of satisfying these OEM requirements.

More Selection

Within our Series 40 family, they can choose from 192 combinations of NRZI, PE and NRZI/PE models with reel sizes from 7 to 10.5 inches and speeds from 12.5 to 75 ips — all featuring a new control block with more functions, such as a density select switch and an optional unit select switch.

More Reliability in a Simpler Package

Microprocessor controlled imbedded formatter improves reliability by reducing chip count as much as 50%. All versions occupy a single board, simplifying cabling and reducing spares requirements, while eliminating the need for separate outrigger housings. Improved transport modularity facilitates field upgrading, particularly data density and tape speed.

More Value

Our low inertia tension arm design provides gentle tape handling that ensures data reliability without the cost, complexity or maintenance problems of vacuum columns. Advanced transport packaging includes a metal frame door and self-aligning rack mounting.

OEMs who interface the PDP-11, Nova, Eclipse or HP-21MX can specify Digi-Data's complete microcomputer based tape systems at a cost savings of 20 to 50%.

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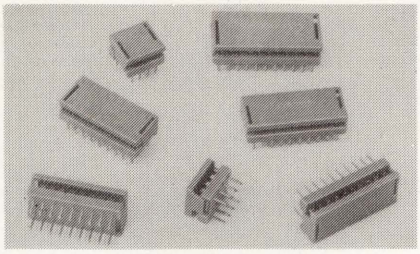
8580 Dorsey Run Road
Jessup, MD 20794
(301) 498-0200

®... First In Value

CIRCLE 129 ON INQUIRY CARD

PRODUCTS

LOW PROFILE DIP PLUG CONNECTORS



BLUE MACS[R] DIP plug connectors mass terminate 8-, 18-, 20-, and 22-position DIP plugs. The cable is simply inserted and crimped with either hand or bench tooling. The 22-position unit has 0.400″ (1.016-cm) row spacing that is compatible with industry std 22-position DIP sockets. A 1-piece body design with self-aligning cable grooves helps reduce production time. Patented Tulip[R] contact design assures reliability and superior electrical performance through 4 points of contact with each cable conductor. **T & B/Ansley Corp,** 3208 Humboldt St, Los Angeles, CA 90031.

Circle 252 on Inquiry Card

DIRECT CONNECT AUTO ANSWER MODEM

M103A is an originate, answer, auto-answer modem compatible with Bell 103A and 113B modems. Connecting directly to the telephone network using the conventional RJ11C modular phone jack, it eliminates cost and need for Bell DAA. The modem operates from 0 to 450 baud and allows any terminal with RS-232 or 20-mA interface to automatically answer incoming phone calls, establish data link, and receive or transmit information without aid of a terminal operator. **Modtech, Inc,** 1958 Helsinki Way, Livermore, CA 94550.

Circle 253 on Inquiry Card

TRIPLE-OUTPUT POWER SUPPLY MODULES

TMP 15/200-5/500 and 12/200-5/500 offer performance advantages and design features in a PC board mountable encapsulated module measuring 3.5 x 2.5 x 1.56″ (8.9 x 6.3 x 3.96 cm). Units operate from 115 Vac ± 10% at 60 to 440 Hz. Full rated output is provided over an amb temp range of −25 to 71°C with no derating. Storage temp range is −25 to 85 °C. Series includes output current limiting protection, 0.05% line regulation for 5-V output and 0.02% for 15- or 12-V output. **Datel-Intersil,** 11 Cabot Blvd, Mansfield, MA 02048.

Circle 254 on Inquiry Card

INTELLIGENT CRT TERMINAL

A 14 x 12 x 18″ (35 x 30 x 46 cm), 20 lb (9 kg), low power (50 W) terminal, the MASter, utilizes two microprocessors—a Z8 to control the video display, and a 6800 to provide the intelligence. 48k of RAM is available to the user, and system routines are contained in 4k of ROM. The terminal can be downloaded from any remote device. The video display includes a 12″ (30-cm) 7 x 9 dot matrix in a 9 x 13 field displaying all 128 ASCII codes. **Micro Application Systems, Inc,** 5575 N County Rd 18, Minneapolis, MN 55442.

Circle 255 on Inquiry Card

4-CHANNEL ASYNCHRONOUS MULTIPLEXER

Bit by bit multiplexing technique gives the Sprint/Mux an efficiency of 99.5%. The digital multiplexer eliminates the need for set up switches for asynchronous terminal channels; no set up is required for speed, parity, or word length. Composite must be synchronous, and can run up to 19.2k bits/s. Terminals should be 1/4, 1/8, 1/16, or 1/32 of the composite. The multiplexer works within the 0.01% frequency clock tolerance specified in RS-334. **Compre Comm, Inc,** 51 Chester, Champaign, IL 61820.

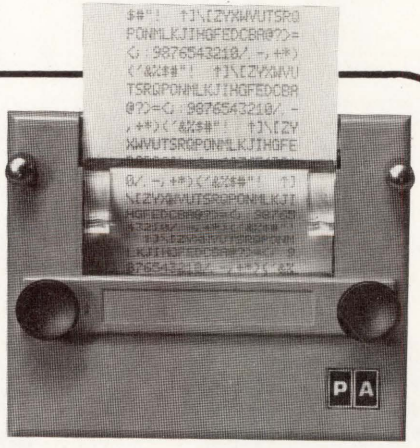
Circle 256 on Inquiry Card

FRONTEND NETWORK PROCESSOR

Datanet 6661 is designed for use with DPS 8 systems as well as Level 66/DPS and Level 68/DPS systems. The processor uses 16k MOS technology in addition to bulkhead connectors designed to ease installation and configuration of data cables. Basic unit includes a front-end network processor, 64k bytes of memory, heavy duty communications console, direct interface adapter and host connection, and up to 32 communications lines. **Honeywell, United States Information Systems Group,** PO Box 6000, Phoenix, AZ 85005.

Circle 257 on Inquiry Card

Today's Smallest Impact Printer Leads a Double Life...



Stand our DMPT-3 Miniature Alphanumeric Printer upright for "first line down" data printing, or flip it for "first line up" text. Either way, it not only packs double printing versatility, it comes with its own controller. So you can put it's 120 cps, 20-column capability to work alone as a basic OEM printer, or with its own microprocessor interface and power supply as part of a system. And for more choice, even use it with either parallel or serial ASCII input, at speeds as fast as 1200 baud.

Whichever life the DMPT-3 leads, it keeps your costs down by printing by impact on ordinary adding machine rolls. Saves time by eliminating ribbons. Saves problems, with our unique print-head in 5×7 dot matrix design. See for yourself; call or write for details today.

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Trap Falls Road, Shelton, Conn. 06484/Tel: (203) 929-5381

Is the honeymoon over with your floppy disk manufacturer?

If you're getting a little sore at inconsistent disk quality, poor delivery and lack of technical support, consider switching to KYBE.

We've been building high performance magnetic media for OEM's for years. And delivering products that consistently meet specification. We start with a base material proven in over 50 million disks worldwide. We manufacture with state-of-the-art equipment in the industry's newest plant. And we test each product using our unmatched experience as the company that invented and perfected media certifying.

We make all types of flexible disks, data cassettes and mag cards. Each is competitively priced, backed by an unconditional 90 day warranty and in stock for fast delivery.

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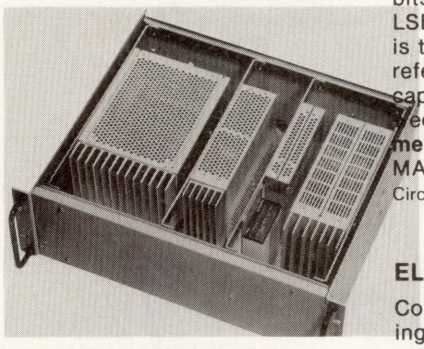
Tel. (617) 899-0012; Telex 94-0179
Offices & representatives worldwide

CIRCLE 131 ON INQUIRY CARD

PRODUCTS

CUSTOM POWER SUPPLY ASSEMBLIES



Rackmount systems allow users to combine custom arrangements of high efficiency switching power supplies. RA-40, a 5.25 x 19″ (13 x 48-cm) housing, mounts 300-W, 150-W, and 3-output 75-W unit, and a 10-W 2-output switcher. A second system measures 3.5 x 19″ (9 x 48 cm). Rack adapters are provided with removable front and rear panels and are drilled for chassis slides. **Kepco, Inc,** 131-38 Sanford Ave, Flushing, NY 11352.

Circle 258 on Inquiry Card

HIGH SPEED ADCS

Available in both industrial and military versions, the 2850 family of analog or digital converters features max total conversion times of 1.7 μs, 850 ns, and 650 ns, for accuracies of 12, 10, and 8 bits, respectively. Linearity is within 0.5 LSB max, and noise at major transitions is typ less than 0.2 LSB. Internal −10-V references are available, as well as capability for an external reference between −9 and −11 V. **Dynamic Measurements Corp,** 6 Lowell Ave, Winchester, MA 01890.

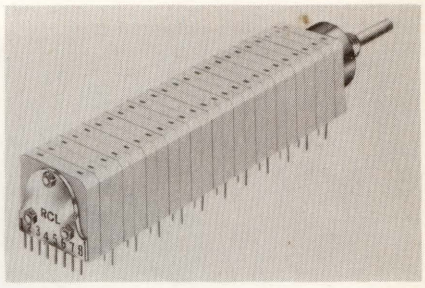
Circle 259 on Inquiry Card

ELECTRONIC CONTROL MODULE

Controlling such functions as sequencing, timing, level sensing, flow rate, and automated assembly, the 811 P/ROM module is permanently programmed for a user's specific requirements. The module has 11 input functions and 8 open collector outputs, each capable of controlling 2 Adc at up to 50 V. Sequence timing is accomplished either by internal clock or by four independent time delays with a range of from 0.2 to 120 s. **Control Technology Corp,** 82 Tpk Rd, Westboro, MA 01581.

Circle 260 on Inquiry Card

MULTIDECK PC BOARD SWITCH



Designed for insertion into PC boards, miniature rotary switch is engineered to withstand stress and strain, is totally enclosed, and eliminates all point to point wiring. Adjustable stops are provided on 12-position units. Life expectancy is >25,000 mechanical operations. There are 12 active positions/deck, with any combination of shorting and nonshorting actions available on any single deck. **AMF Inc, Electro-Components Div,** 2713 Gateway Dr, Pompano Beach, FL 33060.

Circle 261 on Inquiry Card

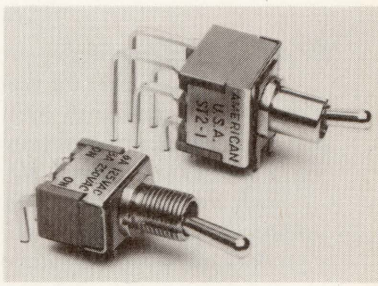
LOW GOLD CONTENT DIP SOCKETS

Solder tail DIP sockets are gold plated in the critical contact area for high reliability and low contact resistance, but tin plated on the leads for solderability without contaminating the solder bath. Side-wipe contact design is used. The gold cannot be degraded in use by being scraped because only the flat smooth side of the IC lead meets the gold contact point. **Robinson Nugent, Inc,** 800 E Eighth St, New Albany, IN 47150.

Circle 262 on Inquiry Card

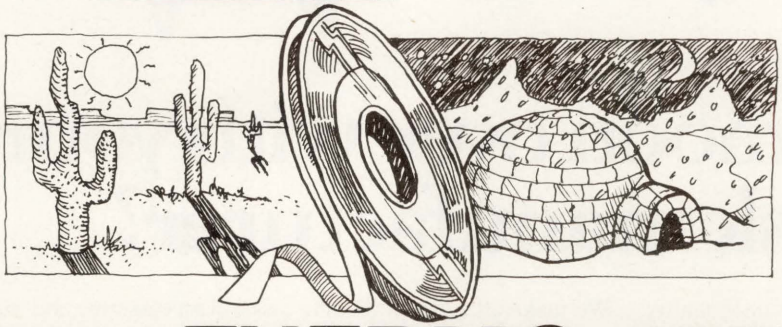
PC BOARD SWITCHES FOR POWER APPLICATIONS

Right angle, horizontal and vertical mounting, miniature toggle switches consisting of single- and double-pole units include UL approved designs for mounting on PC boards. Solid coin silver contacts provide long life and are rated at 6 A, 125 Vac. All models have rugged construction and are rated for 250,000 cycles of electric life, dielectric strength of >2000 Vac, and initial contact resistance of 3 mΩ max at 3 Vdc, 0.1A. **American Switch Corp,** 134 Water St, Wakefield, MA 01880.



Circle 263 on Inquiry Card

The real world is a tough place for conventional magnetic tape



Rely on THERMO-465®

superior digital/audio tape for severe environments — proven to retain data at **+400°F** and **−65°F**

Applications: • Military data systems • Commercial aircraft, ships • Remote or field recording • Metal-tape replacement • Safe wide-temperature data storage

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217 Smith Street, Middletown, CT 06457
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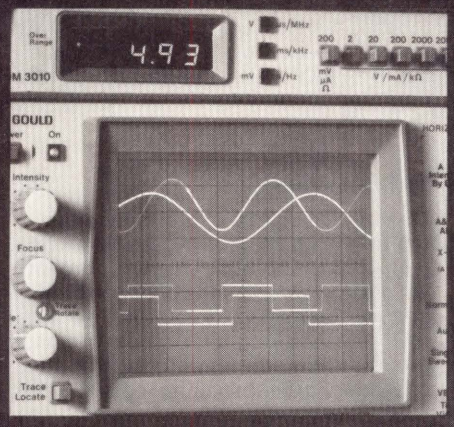
Now—Gould quality in a 100 MHz oscilloscope.

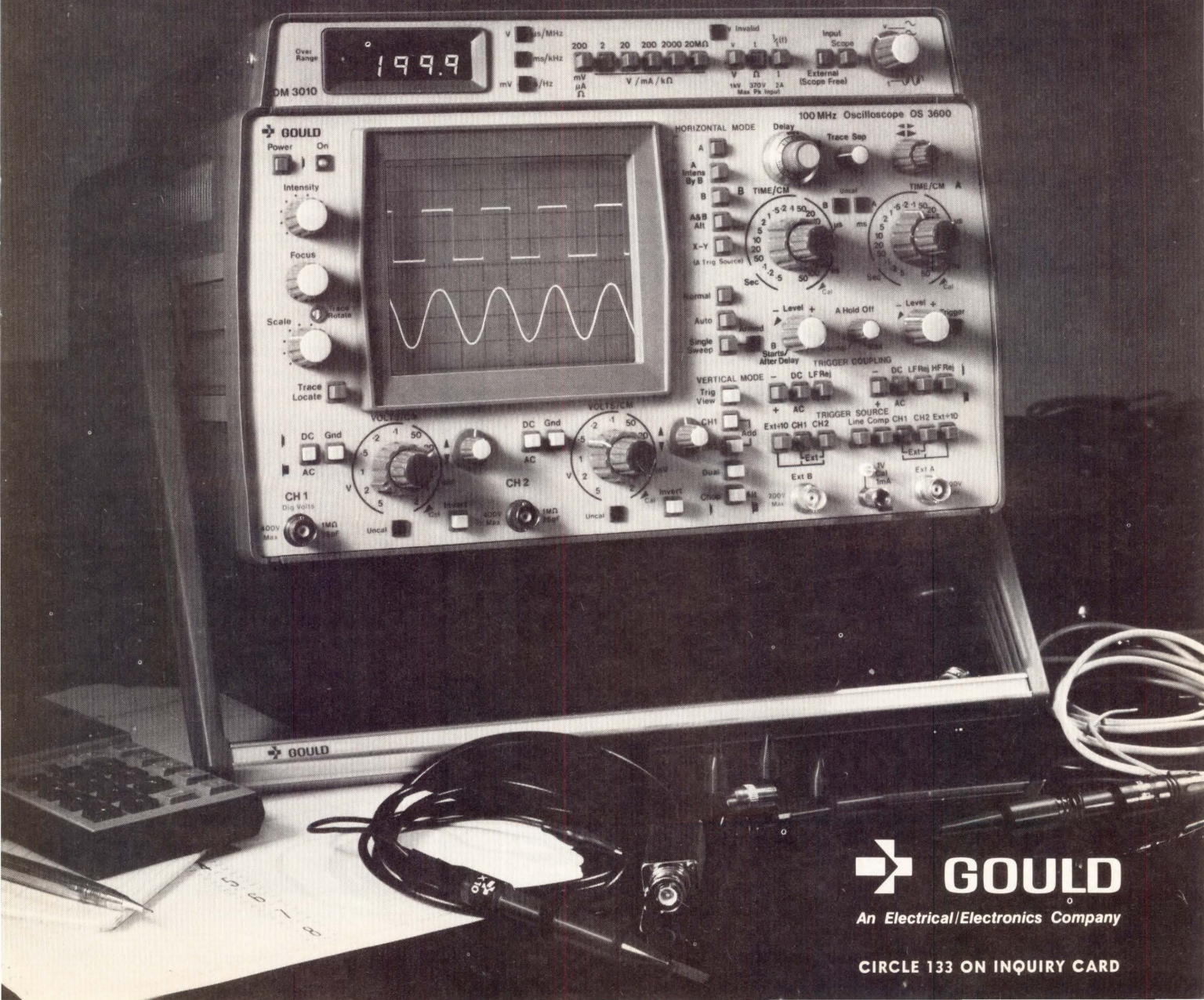
No scope on the market has more of the features you need than the new Gould OS3600 with optional DMM. You can use the OS3600 on any electrical/electronic circuit from digital to conventional with exceptional results.

With vertical sensitivity of 2mV/cm up to 85 MHz, the OS3600 can examine extremely low level signals. The 4-trace capability allows comparison of original and delayed sweeps.

The bright, flicker-free CRT displays even narrow pulses with low repetition rates. The optional 3½ digit DMM is available as a factory fit or retrofit. Plus, the OS3600 is backed by a worldwide service network and a unique 2-year warranty that covers all parts and labor (exclusive of fuses, calibration, or minor maintenance).

Write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, OH 44114. Call toll free 800-331-1000 (in Oklahoma, call collect 918-664-8300).





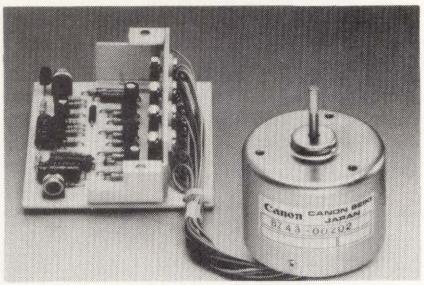
GOULD

An Electrical/Electronics Company

CIRCLE 133 ON INQUIRY CARD

PRODUCTS

NOISE-FREE BRUSHLESS DC MOTORS



Available in rated voltages of 12 and 24 V, motors feature rated speeds of 1800 and 2000 r/min, rated loads of 50 and 150 g-cm, and no electrical or mechanical noise. Diameters are 35, 43, and 52 mm. Direction is controllable and speed can be varied by means of an external variable resistor. Electronic control circuit holds selected speed to close tolerances under variations in load and input voltage. **Canon U.S.A. Inc, Electronic Components Div,** 10 Nevada Dr, Lake Success, NY 11042.
Circle 264 on Inquiry Card

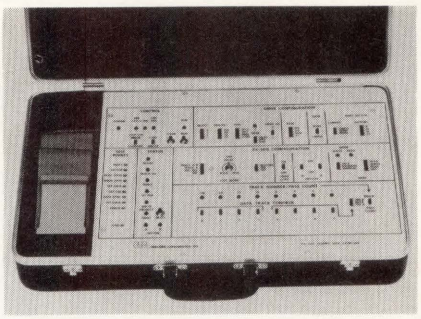
PRINTER CONTROLLER FOR MULTIPLE CRTS

Output of up to 6 CRTs is hard copied one at a time on the PC-1 which connects directly with any serial RS-232 printer. Containing 6 independent contention-logic channels, it remains operable even if one or more of the connected CRTs are down or off. A printer-select button at each CRT station gives the terminal operator exclusive access to the printer; an indicator confirms printer access. **Teleray Div of Research Inc,** Box 24064, Minneapolis, MN 55424.
Circle 265 on Inquiry Card

EAROM BOARD

Multibus compatible nonvolatile memory offers up to 4k x 8 capacity, using plug-in EAROM ICs. Memory contents are electrically alterable under computer control, permitting it to function as a RAM, but with long-term unpowered data retention. Either word or block erasure is possible. Contents can be read with any 8080 memory read instruction. The erase-write cycle is controlled by a 16-instruction subroutine. **Schneider Instrument Co,** 8115 Camargo Rd, Madeira, OH 45243.
Circle 266 on Inquiry Card

FLOPPY DISC EXERCISER



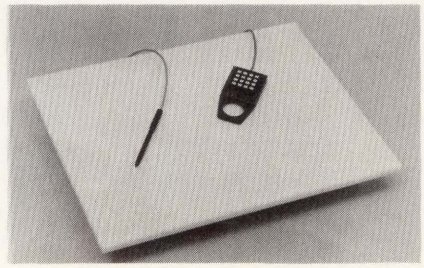
New adapters allow the model FX-500 floppy disc Exerciser to check out Pertec model 514, Calcomp 143, Persci 288/299B, and Persci 277 floppy disc drives. Switches on the tester permit testing drive functions that include hard sectoring; 32-, 16-, 10-, or 8-sector pulses; separated or composite data and clock; single/dual heads; and 250k/125k/500k-bit/s transfer rates for std density. Six exercising modes are included. **Wilson Laboratories, Inc,** 2237 N Batavia St, Orange, CA 92655.
Circle 267 on Inquiry Card

MIL-STD-1553B DATA BUS TRANSCEIVER

Serving as an interface between avionic subsystems and the multiplexed data bus, the 1553 is hermetically sealed in a 24-pin DIP. The thick film hybrid device can be used with MIL-STD-1553A or -1553B data transmission systems. The receiver accepts Manchester II differential data and outputs a biphase TTL signal. The transmitter accepts complementary TTL data and produces a 30-V nom pk-pk differential signal across a 40-Ω load. **Microelectronics Div, Aeroflex Laboratories, Inc,** South Service Rd, Plainview, NY 11803.
Circle 268 on Inquiry Card

INDUSTRIAL X-Y DIGITIZER

Measuring 1.7″ (4.3 cm) high, single-unit Digi-Pad™ digitizer has no adjustments, requires no preventive maintenance, and has all electronics built into its base. Crystal controlled electromagnetic ranging technique used in conjunction with a free-movement cursor allows digitizing on materials up to 1″ (2.54 cm) thick. Precision PC grid array tablet has 11 x 17″ (28 x 43 cm) active area and provides resolution of 0.001″ (0.025 mm) with accuracy of ±0.005″ (0.127 mm). **GTCO Corp,** 1055 First St, Rockville, MD 20850.



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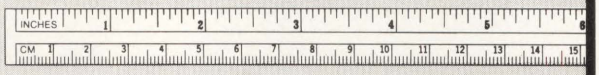
for best results...
first convert to IMC



IMC BOXER FAN

Here's a compact fan that's rugged and reliable. Its whirlwind delivers from 70 to 117 cubic feet of air per minute and can convert to a large variety of uses. AC & DC—high & low voltage available. The IMC Boxer Fan is a natural for computer room use—has long life and saves time and money. Literature on request! For further information please call Stan Barbas, Sales Manager at 603/332-5300 or write.

imc
IMC MAGNETICS CORP.
NEW HAMPSHIRE DIVISION
ROUTE 16B, ROCHESTER, NEW HAMPSHIRE 03867

Winchester users we did it!

We've put a price tag on your backup dreams.

DEI is happy to announce our new 10 and 20 MByte high density streaming cartridge tape drives.

The basic 10 MByte is $415, the 20 MByte is $525. And here's what you get for the price:

Speed: Transfers data at 5 MByte/ per minute.

Capacity: Just what you want. 10 or 20 MBytes. A perfect match for the 8" or 14" Winchester.

Reliability: We certify our cartridges to provide it for you.

Ease of Use: Cartridge operation is simple enough for a person without any computer training to use.

Size: Compact enough to be interchangeable with flexible disks.

Streaming Electronics: Optional formatter and streaming controller with automatic gain control and interdispersed resynchronization. Error correction is also available as an option.

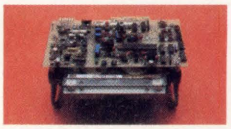
Delivery: Right now!

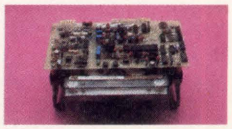
Now that we've got them, all we can say is "come and get it." They're your backup dreams come true!

DEI

Data Electronics Inc.

10150 Sorrento Valley Road, San Diego, California 92121.
Call (714) 452-7840. Telex 69-7118.


10 MByte Cartridge Tape Drive


20 MByte Cartridge Tape Drive

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LITERATURE

D-Subminiature Rectangular Connectors

Photos, drawings, and charts in catalog cover part numbers by shell sizes, standard materials and finishes, electrical data, mechanical features, and wire wrapping and PC applications of connectors. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 300 on Inquiry Card

Computer Science Titles

Catalog lists available books about computers, from introductory information and programming to software and advanced technology. **Hayden Book Co, Inc,** Rochelle Park, NJ.
Circle 301 on Inquiry Card

Winchester Disc Backup

Brochure discusses considerations for medium selection, need for backup, recording methods, and system control; also described are streaming and incremental digital cartridge tape drives. **Data Electronics, Inc,** San Diego, Calif.
Circle 302 on Inquiry Card

10M-Computation/s Array Processors

Brochure describes AP400 series discussing architectural and software concepts, specs, characteristics, interfaces, applications, and system implementations. **Analogic Corp,** Wakefield, Mass.
Circle 303 on Inquiry Card

Ceramic Capacitors

Selector guide for monolithic and disc capacitors, EIA classification system, packaging for automatic insertion, plus performance data, physical characteristics, and specs are featured in catalog. **Centralab, Inc, A North American Philips Co,** Milwaukee, Wis.
Circle 304 on Inquiry Card

Computer Systems in Manufacturing Environment

Hardware and software features of ECLIPSE® data and commercial systems and their manufacturing applications are highlighted in brochure, with discussions of systems compatibility and software offerings. **Data General Corp,** Westboro, Mass.
Circle 305 on Inquiry Card

16-Bit Microprocessor Family

Selection guide lists hardware and software support plus peripheral and interface ICs for the TMS9900 family, and describes TM990 series microcomputer modules. **Texas Instruments Inc,** Houston, Tex.
Circle 306 on Inquiry Card

12 and 15″ Touch Screen Digitizers

Given in illustrated brochure are specs, applications, and principles of operation of digitizers for 12 and 15″ (30- and 38-cm) screens as well as descriptions of retrofit kits. **TSD Display Products, Inc,** Bohemia, NY.
Circle 307 on Inquiry Card

Computer and Business Equipment Noise Emission Standard

Procedures for measuring and reporting noise emission and methods for installing equipment are defined in ANSI S1.29-1979, available for $15 (prepaid) from **Acoustical Society of America,** DEPT STD, Back Issues Dept, American Institute of Physics, 335 E 45th St, New York, NY 10017.

Dc Power Supplies

Catalog presents 23 open-frame series-regulated models and provides specs, mounting diagrams, and information on custom design and modification capability. **Power-One,** Camarillo, Calif.
Circle 308 on Inquiry Card

Fast Poll Modem

Dial backup, fast poll, training sequence, and system integrity of the V.27 bis and V.27 ter compatible GDC 480ZE(D) modem are outlined in illustrated data sheet. **General DataComm Industries, Inc,** Danbury, Conn.
Circle 309 on Inquiry Card

Memory Digital Readout For Machine Tool Applications

Illustrated brochure defines 14 push button functions and 3 operating modes, lists performance features, and supplies specs for memory Digiline Arrow readouts with programmable error compensation. **Itek Measurement Systems Div,** Newton, Mass.
Circle 310 on Inquiry Card

8 x 8-Bit Multiplier

Block diagram of MPY-8HUJ, I/O schematics, specs, and glossary of terms are supplied in data sheet along with note on interfacing multiplier with 8-bit microprocessor. **TRW LSI Products,** El Segundo, Calif.
Circle 311 on Inquiry Card

Process Control Instruments

Catalog lists programmer-controllers, microcomputer programmers, temperature controllers, set point systems, high-low temperature alarm devices, and mercometers for industrial systems. **Thermotron Industries, Automatic Control Systems Div,** Holland, Mich.
Circle 312 on Inquiry Card

LSI-11 Microcomputers

Brochure details software, architectures, and operational features of the LSI-11/2, -11/23, and LSI-11 family modules, and summarizes specs of the -11/2 and -11/23. **Digital Equipment Corp,** Maynard, Mass.
Circle 313 on Inquiry Card

Data Communications Terminal

Brochure describes chained terminal capability that eliminates need for controller and printer control capability when dumb printers are used in network environment. **Beehive International,** Salt Lake City, Utah.
Circle 314 on Inquiry Card

Electronic Packaging

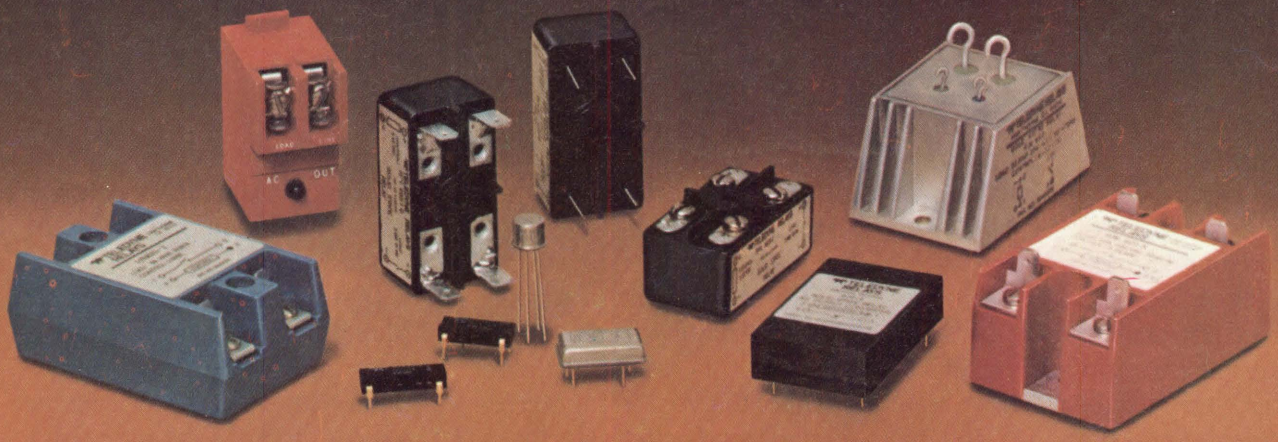
Diagrams, specs, truth tables, and dimensional data describe IC sockets, I/O and PCB connectors, flat cable interconnect systems, card files, and thumbwheel switches featured in handbook. **Stanford Applied Engineering,** Santa Clara, Calif.
Circle 315 on Inquiry Card

Magnetic Measuring Instruments

Portable digital readout gaussmeters, automatic hysteresigraphs, core loss testers, and permanent magnet magnetizers and calibrators are among equipment featured in catalog with photos and specs. **LDJ Electronics, Inc,** Troy, Mich.
Circle 316 on Inquiry Card

SSR UPDATE

AC Solid State Relays: We have more answers than you have questions.



Whatever your AC solid state relay switching problem, the odds are we have the answer sitting on our shelf. With more than 90 different models ready to meet your needs, you have to look long and hard to find a problem we can't answer.

The features tell the story. Voltage ratings up to 800V peak. Steady state load current ratings up to 40 Amps. High transient immunity. Optical isolation. Zero cross-over switching. A variety of packages for pc board, chassis or heat sink mounting. Even a family of military SSRs designed to meet MIL-R-28750. It's industry's most complete line of AC SSRs.

If you still can't find your answer, we'll help you. The industry's most experienced engineering staff is available to give you applications support. After all, the more effectively you use our solid state relays, the better off we both are. So call or write us today, and tell us your problem.

TELEDYNE RELAYS

12525 Daphne Avenue, Hawthorne, California 90250 • (213) 777-0077

CIRCLE 136 ON INQUIRY CARD

Mini/Micro80

Small computer showdown at the Golden Gate

The sixth Minicomputer/Microcomputer Conference and Exposition puts the small computer world under one roof—in beautiful San Francisco, October 14-16.

The newest and most significant small computers, peripherals, and systems will be displayed and demonstrated in more than 300 exhibit units in Brooks Hall and Civic Auditorium. 24 applications-oriented technical sessions will be presented concurrently in adjacent lecture halls. And more than 8000 technical and business executives will participate.

It's the only small computer event of the year in the superactive, trend-setting Northern California territory—and Mini/Micro80 is designed and organized for the most effective information-transfer. It's a professional event for computer professionals.

Mark your calendar now for Mini/Micro in San Francisco—and return the coupon for detailed technical program, exhibit, and special-event information as soon as it's available.

Mini/Micro80

32302 Camino Capistrano, Suite 202, San Juan Capistrano, California 92675

Sirs:
Please make sure I receive all the information about Mini/Micro80 in San Francisco, Oct. 14-16, 1980.

☐ Please send information on exhibiting immediately.
☐ Please send technical progam and expo information.

Name _____

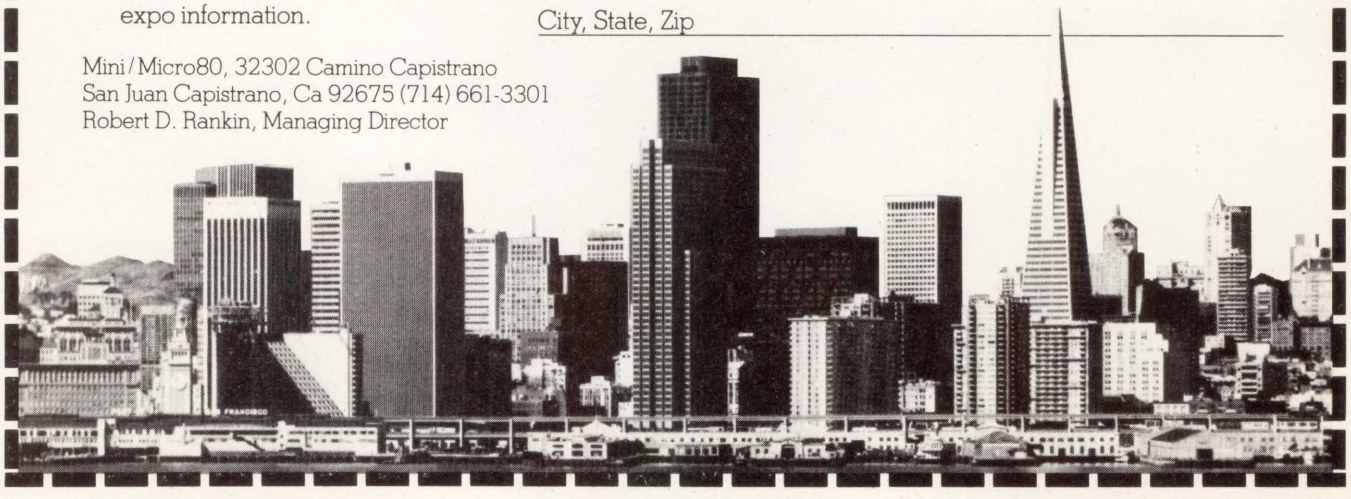
Title _____

Company _____

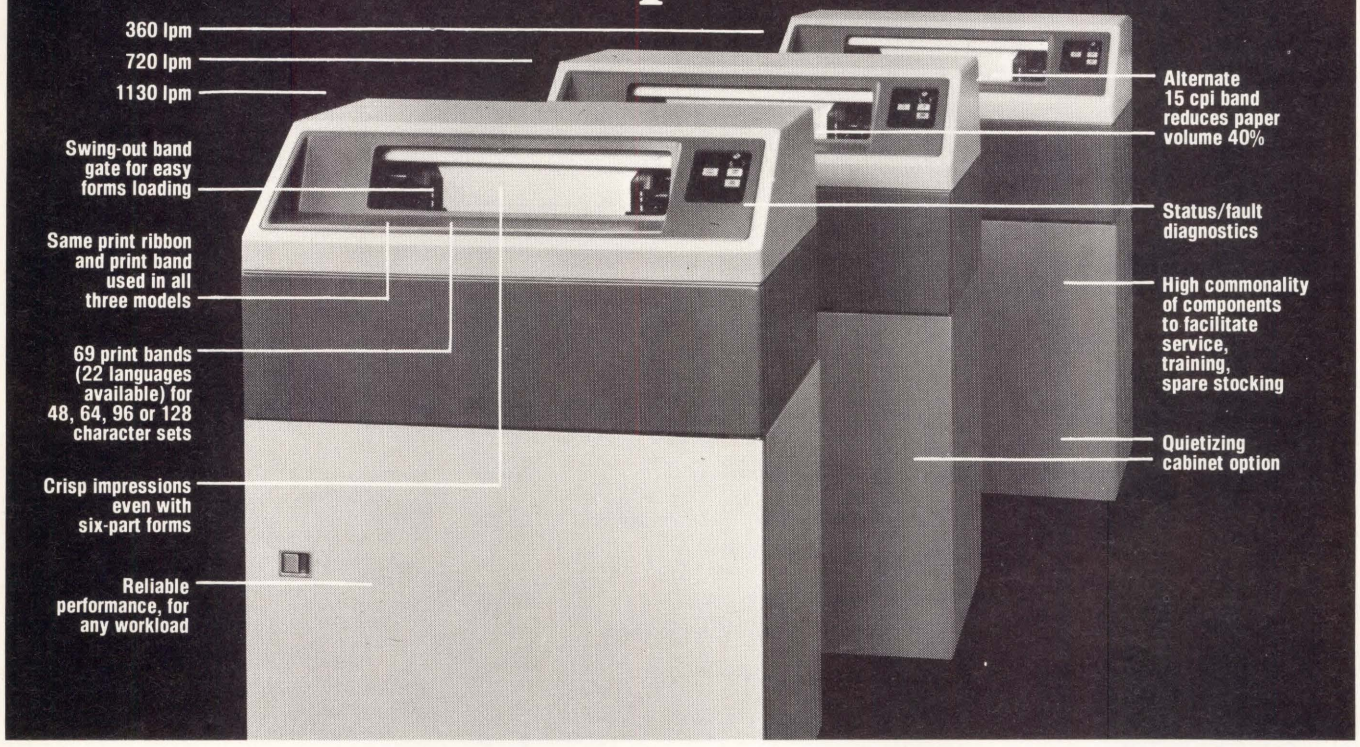
Address _____

City, State, Zip _____

Mini/Micro80, 32302 Camino Capistrano
San Juan Capistrano, Ca 92675 (714) 661-3301
Robert D. Rankin, Managing Director



Quality impressions are made easily with OEM band printers from CDC



If you're an OEM, you already know what Control Data has done for disk technology. Now we're determined to earn the same reputation for excellence in band printer technology. By giving *you* versatility and maintainability. By giving *your customer* reliability, superior print quality and economical operation.

Engineered for component commonality

All three members of our 9380 family of band printers look pretty much alike. Inside and outside. So your servicing, training and inventory requirements are simplified. Yet you can choose from three print speeds, 69 print bands and lots of other options.

Built with the features and economy to attract end-users

Our 360/720 lpm models offer a compressed pitch option. That saves your customer money in paper expense. And gives him the capability to print 132 columns on standard 8½ by 11 inch paper. Bands switch in seconds. Paper loading is easier. Operator controls and adjustments are minimal. And your customer will like the clean, crisp impressions delivered by our proven hammer technology.

Put quality behind your nameplate. Let us send you data sheets and print samples. Call us at 313/651-8810 or if in Europe, contact one of our European representatives. Or return coupon to:

CD 60

Control Data Corporation
1480 N. Rochester Road, Rochester, MI 48063

Please send literature and sample printouts on your band printers.

Name_____ Title_____

Company_____ Phone_____

Address_____

City_____ State_____ Zip_____

CONTROL DATA CORPORATION

Addressing society's major needs

CIRCLE 137 ON INQUIRY CARD

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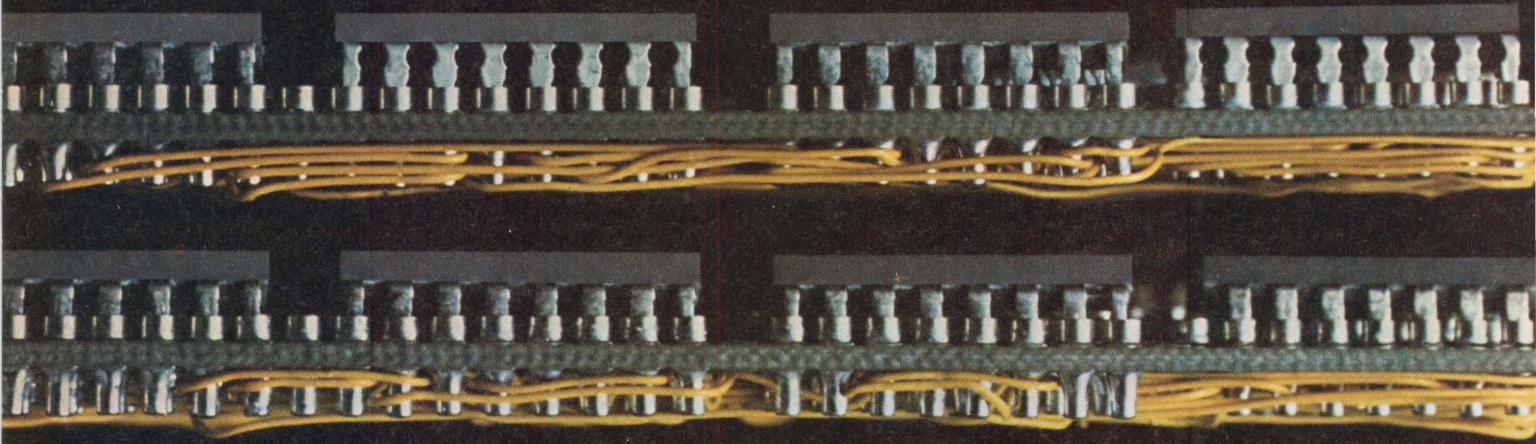
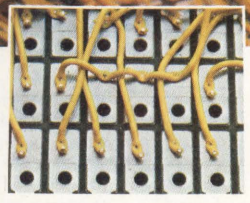
AUGAT'S SOLUTION TO PACKAGING DENSITY AND DESIGN FLEXIBILITY... THE PLANAR STITCH-WIRE SYSTEM.



Planar socket-type boards on 0.5 inch centers. Photograph shown 2x size.

Augat's Planar stitch-wire concept is unique. This patented, high-speed, low-cost system reduces the substantial engineering time of complete circuit card prototyping and debugging. As a result, turn-around time can be cut by one-third to one-half. Augat's stitch-wire system works like this: after components or sockets are mounted on the Planar boards, a stitch-wire machine welds Teflon-insulated nickel wire to stainless steel pads. In certain configurations, the bare board may be wired first.



Wiring instructions can be furnished using key-punch card or wire lists. Your logic design can be debugged using our Data-Logic program. We provide all final wiring documentation, or can supply total wiring service at any of our four service facilities located in—Van Nuys, CA, Houston, TX, Attleboro, MA, Fresnes, France.

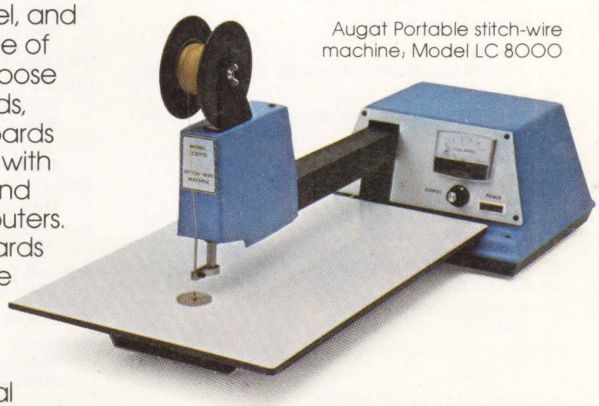
Changes can be made by stitch-wire machines or by hand soldering. Adopting stitch-wire is easy, because Augat provides the wiring machines, including portable models (LC 8000 shown), a high-speed, numerically controlled model, and a wide range of general-purpose Planar boards, including boards compatible with most mini- and micro-computers.

These boards feature large etched power and ground planes making them ideal for high-speed logic. We can design and produce stitch-wire boards to your specifications, or provide the boards and equipment you need to do the job in your own shop.

Augat stitch-wire offers density and flexibility advantages you can't get anywhere else. To find out how to start with Planar stitch-wire, write or call, Augat Inc., Interconnection Systems Division, 40 Perry Avenue, P.O. Box 1037, Attleboro, MA 02703. Tel. (617) 222-2202.

Europe—Augat SA, B.P. 440 Cedex/94263 Fresnes, France. Tel: 668.30.90. Telex: 201.227. AUGSAF.

Augat Portable stitch-wire machine, Model LC 8000



AUGAT®

Augat interconnection products, Isotronics microcircuit packaging, Alco subminiature switches and Datatex computer-aided design and wire-wrapping services.

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ok

EW-8 Wire Wrapping Tool

EW-8 $85.11*
EW-8-BF $92.90*
VIT-1 $15.00*

NEW ELECTRIC WIRE WRAPPING TOOL

O.K. Machine and Tool Corp. has introduced its new model EW-8 electric wire-wrapping tool. The tool is interchangeable with its previous model EW-7D, and incorporates a number of improvements at no increase in price. Rated to accept bits for wire sizes 22-30 AWG, model EW-8 features a reinforced Lexan™ housing, RFI reducing circuitry, and a high reliability motor and indexing mechanism. The tool is double insulated and weights only 14 ounces. Available with optional anti-overwrapping device as model EW-8-BF. Also available with accessory tool VIT-1 which permits easy resetting of indexing position in 45 degree increments.

Available ex-stock from

™ General Electric

OK Machine & Tool Corporation
3455 Conner St., Bronx, N.Y. 10475 U.S.A.
Tel. (212) 994-6600 Telex 125091

*Minimum billings $25.00, add shipping charge $2.00
New York State residents add applicable tax

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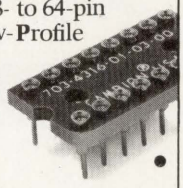

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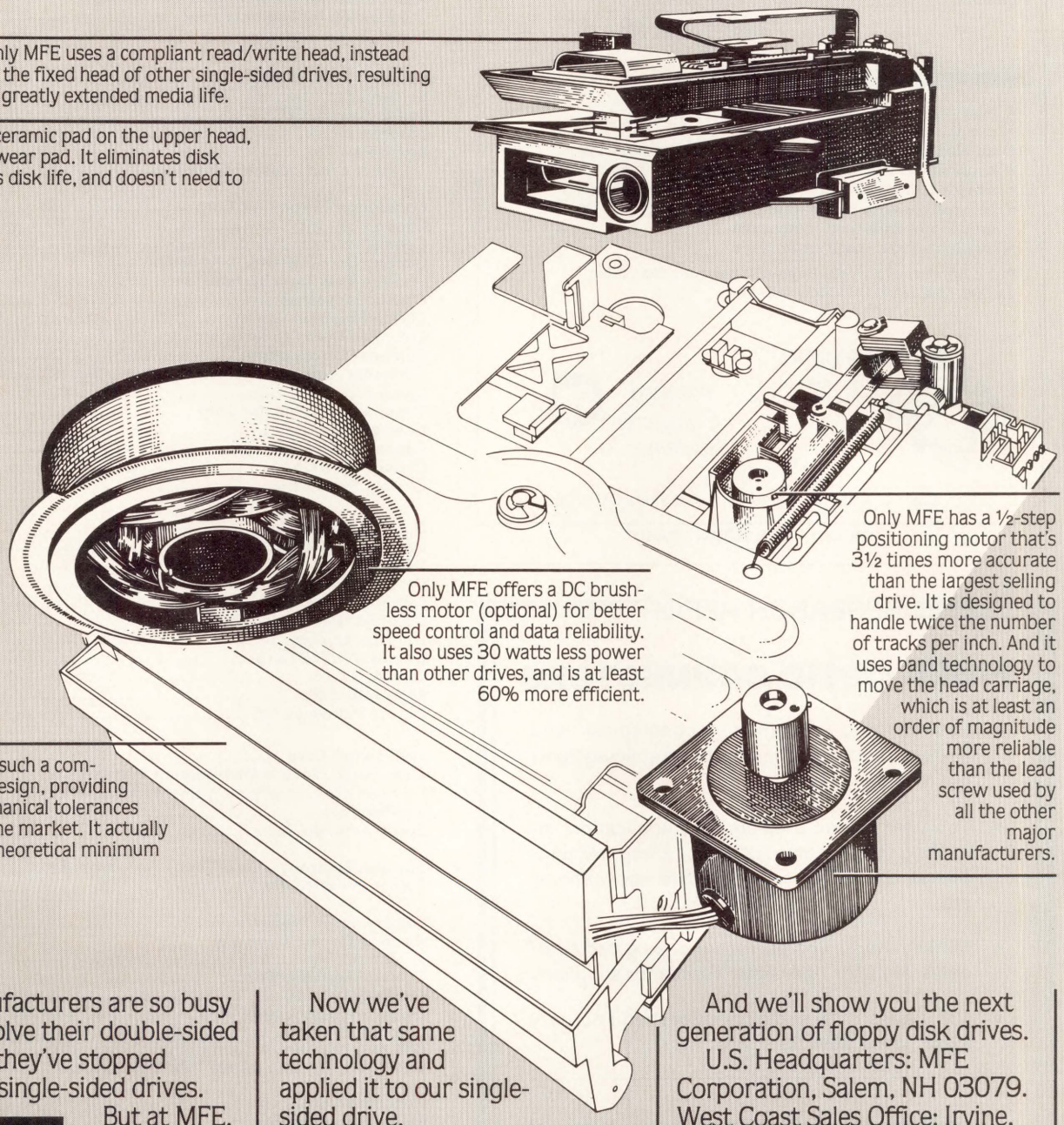

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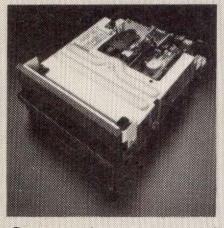

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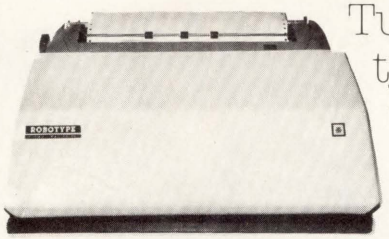

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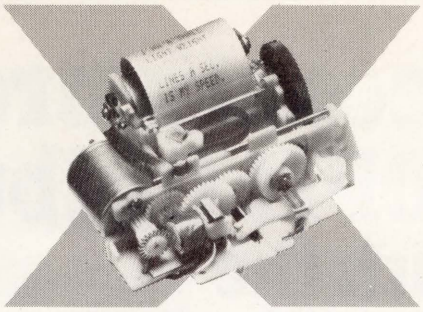

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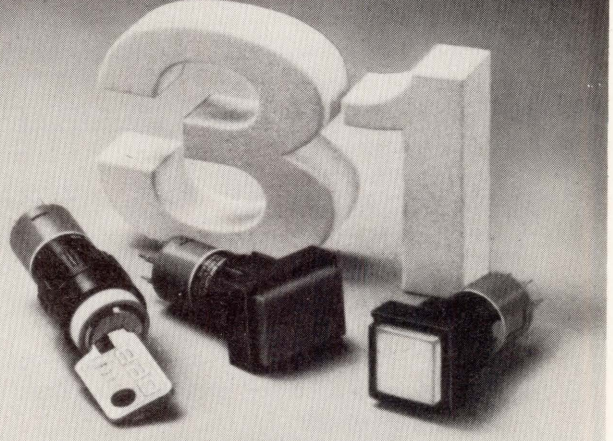

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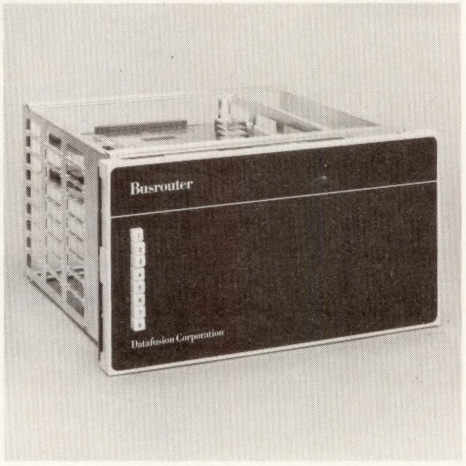

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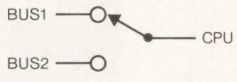
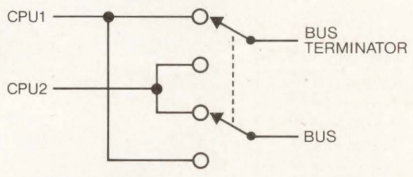


The application shown here is a situation opposite the first, where one peripheral bus can be switched between two cpu's with the cpu not selected being terminated.



Many more configurations are available such as sharing multiple peripheral devices between multiple cpu's and then selectively choosing to switch each one or all to one cpu or another.

Other PDP11 products available are a bus repeater, bus cable tester, and an associative processor for high speed text search—a hardware approach.

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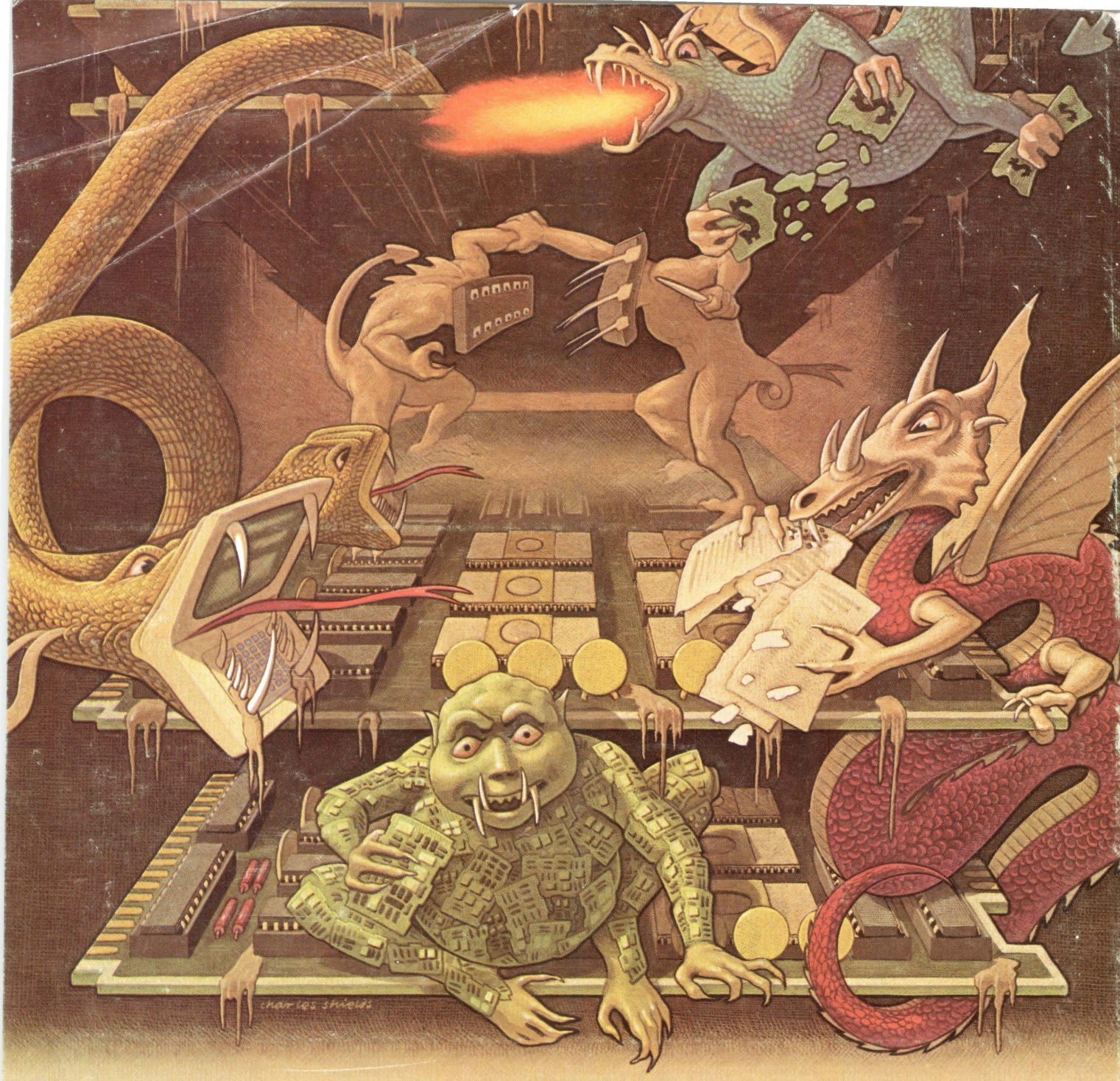

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