COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

FEBRUARY 1980



ENCODING/DECODING TECHNIQUES DOUBLE FLOPPY DISC CAPACITY MULTIPROCESSING SYSTEM MIXES 8- AND 16-BIT MICROCOMPUTERS SEMICONDUCTOR MEMORY UPDATE—PART 3: HIGHER DENSITY DEVICES

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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The IEEE Industrial and Electronics Control Instrumentation Society sponsored spring conference and exhibit will present details on the application of mini and microcomputers in areas ranging from process control and data acquisition to energy monitoring and testing systems



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CALENDAR

CONFERENCES

MAR 14-16-West Coast Computer Faire, Civic Auditorium and Brooks Hall, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

MAR 17-19—Industrial Control & Instrumentation Applications of Mini & Microcomputers (IECI), Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr Paul Russo, RCA Labs, Princeton, NJ 08540. Tel: 609/452-2700, X3234

MAR 17-20-Interface '80. Miami Beach Convention Ctr, Miami Beach, Fla. INFOR-MATION: Peter Young, Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

MAR 19-21-Design Technology for Computers & Datacomm Systems '80, Disneyland Hotel Convention Ctr, Anaheim, Calif. INFORMATION: Industrial & Scientific Conf Mgmt, Inc, 222 W. Adams St, Chicago, IL 60606. Tel: 312/263-4866

MAR 24-27-Powercon 7, Town and Country Hotel, San Diego, Calif. INFORMA-TION: Ed Gragda, Powercon 7, PO Box 5226, Ventura, CA 93003. Tel: 805/985-6978

MAR 25, MAR 27, AND APR 28-Invitational Computer Conf, Dallas, Tex; Houston, Tex; and Atlanta, Ga. INFORMA-TION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

APR 8-10—Internat'l Reliability Physics Sym, Caesar's Palace, Las Vegas, Nev. IN-FORMATION: Glen T. Cheney, Bell Laboratories, 555 Union Blvd, Allentown, PA 18103. Tel: 215/439-7628

APR 21-24—Internat'l Magnetics Conf, Sheraton-Boston Hotel, Boston, Mass. IN-FORMATION: D. I. Gordon, Conf Chm, Naval Surface Weapons Ctr, White Oak, Silver Spring, MD 20910. Tel: 202/394-2167

APR 28-MAY 2—Society for Information Display Internat'l Sym, Town and Country Hotel, San Diego, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193

Architecture, Casino, La Boule, France. INFORMATION: Jacques Lenfant, Irisa Campus de Beaulieu, 35042 Rennes, Cedex, France

MAY 13-15-ELECTRO, Boston-Sheraton/Hynes Auditorium, Boston, Mass. INFORMATION: Dale Litherland, Electronic Conventions, Inc. 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 19-22-National Computer Conf, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100

MAY 20-22-CENCON '80 Industrial Electronics Conf, Public Auditorium Arena, Cleveland, Ohio. INFORMATION: Mike Lapine, Cleveland Electronics Conf. Inc, 2728 Euclid Ave, Cleveland, OH 44115. Tel: 216/241-5515

MAY 29—Computer Networks Protocol Sym, NBS, Gaithersburg, Md. INFORMA-TION: Helen M. Wood, Conf Chairperson, National Bureau of Standards, Washington, DC 20234. Tel: 301/921-2834

JUNE 3-5-Networks '80, Bloomsbury Centre Hotel, London, England. INFORMA-TION: Online, Cleveland Rd, Uxbridge UB8 2DD, England

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MAY 6-8—Internat'l Sym on Computer

Angela Turvey, 4910 Butternut Dr, Rockville, MD 20853 JUNE 25-27—IFAC Sym on Large Scale Systems: Theory and Applications,

Toulouse, France. INFORMATION: Symposium Secretariat, AFCET-156, Bd Pereire-75016 Paris, France

MA 02146. Tel: 617/739-2022 MAY 7-8 AND JUNE 4-5-Microprocessors: Hardware, Software and Applications, WPI Campus, Worcester, Mass and Boston, Mass. INFORMATION: Office of Continuing Education, Worcester Polytechnic Institute, Worcester, MA 01609.

Tel: 617/753-1411, X517

JUNE 17-19—Internat'l Microcomputers

Minicomputers Microprocessors/

DATACOMM '80 Conf, Palais Des Exposi-

tions, Geneva, Switzerland, INFORMA-

TION: Industrial & Scientific Conf Mgmt, Inc,

222 W Adams St, Chicago, IL 60606. Tel:

JUNE 19-Computer System Integrity,

Technical Sym of the ACM and NBS In-

stitute for Computer Sciences and

Technology, National Bureau of Stan-

dards, Gaithersburg, Md. INFORMATION:

SEMINARS

MAR 10-12-Digital Switching Trends,

Digital Communication and Signal Pro-

cessing, and Fiber Optical Communica-

tion, Dallas, Tex. INFORMATION: Ann

Siegenthaler, Dir of Sem, Information

Gatekeepers, Inc, 167 Corey Rd, Brookline,

312/263-4866



MAR 10-11-Digital Electronics for Instrumentation and Automation; MAR 12-14-8080-8085-Z80 Microcomputer Interfacing, Design, and Software; and MAR 17-18-TRS-80 Interfacing and Programming for Instrumentation and Control, Virginia Polytechnic Institute and State U, Blacksburg, Va. INFORMATION: Dr Linda Leffel, CEC, Virginia Polytechnic Institute, Blacksburg, VA 24061. Tel: 703/ 961-5241

MAR 19-21 AND MAR 24-26-Software Reliability Models and Design of Digital Control Systems, George Washington U, Washington, DC. INFORMATION: Dir, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

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LETTERS TO THE EDITOR

To the Editor:

I found the July 1979 article "Practical Hardware Solutions for 2's Complement Arithmetic Problems" by Thinh V. Nguyen, (pp 105-112) rather interesting. I noticed, however, that the circuit given in Fig 2 (and incorporated in Fig 3) produces a correct answer for only 88.3% if the possible inputs. For example, if the input is 00F0H, the output will be 01F1H; but 00F0H + 1 = 00F1H.

As an alternative, I propose the circuit in the accompanying diagram. Since the A1 to A4 adder inputs are always 0, the generate inputs to carry lookahead are also always 0; and since the propagate signal can be produced with simple AND gates, a more complex ALU is unnecessary. As the 74182 uses negative logic for its P and G inputs, NAND gates are used and the G inputs are tied to Vec.

Typical propagation delay would be

12 ns 74Ls40 NAND

7 ns 74S182 carry look ahead

15 ns 74Ls283 adder

34 ns

By incorporating three data selectors controlled by the carry outputs of the carry lookahead, delay would be reduced to 28 ns.

George M. Hutnick Allentown, Pa





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CRT	Delta gun Dot shadow mask 0.31mm dot pitch	In-line gun Dot shadow mask 0.31mm dot pitch	In-line gun Dot shadow mask 0.31mm dot pitch	Delta gun Dot shadow mask 0.61mm dot pitch		
Display Capability	4,000 char. Analog	4,000/2,000 char. Analog	4,000/2,000 char. Analog	2,000 char. Analog		
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CIRCLE 12 ON INQUIRY CARD



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Think you've got it tough?

See page 174

To the Editor:

I feel obliged to write to you concerning an unfortunate error that appears in the July 1979 issue in the article "Practical Hardware Solutions for 2's Complement Arithmetic Problems" by Thinh V. Nguyen, pp 105-112.

The error occurs in the fast add 1 circuits of Figs 2 and 3, which are referred to several times in the text. The problem is that the circuit shown gives the wrong answer whenever a carry is produced by a stage in the absence of a carry from the preceding stage.

A circuit that overcomes this problem is shown. In this circuit the signal to the 74Ls157s only selects the outputs of an adder if the carries from all preceding stages are present-as must be the case for correct operation. Note that the A and B inputs on the second and subsequent data selectors have been swapped as compared to the first data selector due to the negative logic output from the NAND gates. This circuit adds a further 9 ns (typ, LS/TTL) to the add time of 24 ns quoted in the article, which still represents a speed advantage (albeit small) over the ripple carry method for 16-bit numbers.

The circuit can be conveniently extended to word sizes of up to 36 bits without increasing the addition time. This limitation comes about because each stage that is added requires a NAND gate with one more input than the one at the previous stage. Wider NAND gates from the Schottky range could be used (74S133, 74S134) but these would soon run the carry from the first stage out of fanout since it has to drive all the levels above it.

If a further gate delay could be tolerated then an extra 2-input NOR gate for each of the upper stages will extend the method to 68 bits, which should be enough for most systems.

For the upper 8 stages the select signal is implemented as

$$S_{9+n} = C_9 \bullet C_{10} \bullet C_{11} \bullet \ldots \bullet C_{9+n-1} + \overline{S_9}$$

n = 1 to 8

where S_m is the select signal to the mth stage, C_m is the carry signal to the mth stage, and

 $\overline{\mathbf{S}_9} = \overline{\mathbf{C}_1 \bullet \mathbf{C}_2 \bullet \mathbf{C}_3 \bullet \mathbf{C}_4 \bullet \mathbf{C}_5 \bullet \mathbf{C}_6 \bullet \mathbf{C}_7 \bullet \mathbf{C}_8}$

Since the select signal is now positive the A and B inputs to the data selectors will need to be reversed for the upper stages.

Craig Clapp Bracknell, England

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In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.



CIRCLE 16 ON INQUIRY CARD

The Author replies:

The circuit in Fig 2 (p 107, "Practical Hardware Solutions for 2's Complement Arithmetic Problems," *Computer Design*, July 1979) is of course inadequate. This is simply because there is a missing AND gate at the output carries from the adders. The correct circuit is shown in the diagram.

Thinh V. Nguyen ITT General Controls Glendale, Calif

To the Editor:

I was very pleased with the editorial care expended on my article, "Reliability Computations on a Handheld Programmable Calculator," in the November 1979 issue of *Computer Design*, p 138. Looking again at my just published article I discovered a few mistakes (my fault!) in the program listing on page 142. The following corrections should be noted:

1. After step 001 (LBL A), step 027 (LBL B), and step 056 (LBL C) insert CF1 $\,$

2. Correct step 002 from $Y \longleftrightarrow Y$ to $X \longleftrightarrow Y$

3. After step 111 (LBL D) insert SF1

4. Delete step 120 (STO 1)

5. After step 151 (RCL 1) insert $X \leftrightarrow Y$, ?F1, RCL 5

Cass R. Lewart System Development Corp Eatontown, NJ

To the Editor:

First I would like to thank you for the listing of Cecil Beeson's program for minimizing multiple output Boolean functions featured in the January 1979 issue. There was a problem



in implementing the program that other readers also may have encountered.

I used the FORTRAN subroutines for the IOR, IAND, and IONES functions. The program does not work if the arguments are passed to the subroutine by value, eg, subroutine IOR (A,B,C).

The subroutine does not give the correct answers if A and B are variables with the same name. However, if the last two arguments are passed by location, SUBROUTINE IOR (A,/B/,/C/), the program works

properly and the solutions agree with the given sample problems.

I. Phillip Jenkins Bendix Flight Systems Div Teterboro, NJ

Letters to the Editor should be addressed:

Editor, Computer Design 11 Goldsmith St Littleton, MA 01460

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EST SOC	CK	E	T																							N	IORMAL FORCE
1.					+																						410 grams
2.		, .																								ñ.	465 grams
3.							.,		* 1																	•	480 grams
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10				* *			1	•				• •	*											*	1		425 grams

* NORMAL FORCE means force perpendicular or at right angles to IC lead. The single ICL contact exerts this kind of force against the IC lead when inserted into the socket.



COMMUNICATION CHANNEL

COMMUNICATIONS IN DISTRIBUTED SYSTEMS-PART 1: INTERFACING TECHNIQUES

Melvin G. Gable

Ford Motor Company Dearborn, Michigan

ecent advances in communication technology and the evolution of the microprocessor have made distributed computing a practical system design approach. Distributed computing can be considered as the physical separation of the intelligence of the system into separate, logically organized units dedicated to the overall task of performing a given function. For the total system to operate and function properly, it is necessary that the separate systems be able to communicate with each other. This requirement is accompanied by the problem of interfacing the various intelligent units in a manner that provides efficient and timely communications. Delays, or response of the communication interfacing technique, should not degrade total system performance.

There is a tendency in distributed systems to be either loosely or tightly coupled in functional organization. Tightly coupled multiprocessor systems usually require communication response times that are less than a hundred times their instruction execution rate (Fig 1). Such tightly coupled processor applications range from matrix array computing, signal processing, pattern recognition, and frontend communication processing. The requirements of energy management, laboratory automation, process control, and plant machine monitoring generally result in loosely coupled systems having relaxed constraints on communication response. Communications in loosely coupled systems are usually by messages, and, in most cases, message delays greater than a thousand times the execution speed of the processor do not degrade system performance. This is because each unit is organized to operate with less dependency on the total system. In loosely coupled systems, the bandwidth of the communication bus is not as critical; therefore, the bit serial interface method becomes more attractive due to its simplicity. On the other hand, in tightly coupled systems where performance is important, the high bandwidth of a parallel bus outweighs the increased complexity of the communication interfacing technique. Fig 2 illustrates serial, parallel, and first in, first out buffer interfaces, as well as shared memory design approaches. Such schemes have been used in various system designs to achieve the desired system performance.

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CIRCLE 19 ON INQUIRY CARD



Parallel Interface

Communication interfacing of two processors can be easily accomplished through the use of either bidirectional or unidirectional parallel interface design. Such interfaces have input and output registers as well as control inputs and outputs for handshaking during data transfer. The major disadvantage in using parallel ports for communication is that the processors must be synchronized for the exchange of data to be completed.

Use of local buffering within the interface will diminish latency and synchronization problems. A first in, first out (FIFO) buffer memory automatically stores words in the order in which they are entered at the input, and permits their extraction from the output in exactly the same order. In addition, data entry and extraction from the FIFO buffer can be accomplished asynchronously. Because of these properties the FIFO buffer memory is ideal for this application.

Such FIFO memory devices are available from various semiconductor manufacturers. As an example, the Fairchild 16-word by 4-bit TTL 9403 permits data entry and extraction in either parallel or serial format. A minimum of hardware is needed to design a communication interface, since the buffer memory and associated control functions, as well as the serial-to-parallel and parallel-toserial conversions, have been combined into a single integrated circuit.

In the Zilog Z8000 family of microprocessor components,¹ a FIFO buffer can be used to configure parallel processors, peripherals, and local and common memory into a network. The z-MBU and z-FIFO components are organized as 8-bit wide asynchronous bidirectional FIFO buffer units. The z-FIFO is used to expand the depth or word width of the microprocessor buffer unit (MBU) and does not contain the microprocessor bus and control interface logic as does the MBU. The FIFO buffers permit asynchronous communications between parallel processors, and also have the capability to connect various subsystem components operating at different speeds. Key to their operation is that the FIFO accepts data and holds them until they can be processed by another device in the system. The system is not slowed down by having to wait until the receiving device can accept the data.

Shared Memory

When there are multiple communication paths in a system configuration, the number of FIFO buffers grows accordingly. A shared memory approach solves the problem of predefining all data communication paths. The microprocessors can be connected to the common memory through the use of a shared bus approach. Each processor uses the common bus to fetch instructions and data from memory and to read and write input/output (I/O) devices or memory. As a result, the common bus becomes a bottleneck to overall system throughput, and this constraint severely limits total system performance.

Shared bus utilization can be minimized by implementation of an alternate dual-bus structure, as in the Intel MULTIBUSTM system architecture. Each processor in the system has its own local memory and I/O that it uses for most operations. This procedure reduces the frequency of service requests for the shared system bus. Access to the shared bus is only necessary when global memory locations or I/O devices are referenced in the program. In the MULTIBUS systems, the local and global distinction is made through the physical address of the reference.

Two or more processors may simultaneously request the shared bus. In such an event, arbitration is required to resolve this multiple access contention.² In the MULTIBUS structure, arbitration is accomplished through either a serial or parallel hardware priority technique.

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY

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MICRO-DAC[™] Series is the easiest way from D to A.



The DAC1000 is the first of a series of 10-bit four-quadrant multiplying D/As that are truly μ P-compatible. That's because each DAC looks like a memory location or an I/O port and has all control functions right on the chip. So you get easy interface with any 8- or 16-bit data bus.

With National's "end point" linearity spec only two adjustments are needed: Zero and Full Scale. Set these, and the linearity specification is met. And linearity is maintained even with a 10-to-1 reduction in reference voltage.

. The MICRO-DAC 1000 Series can be used not only for D/A conversion systems, but also as building blocks for digitally controlled amps, alternators, active filters, and even oscillators.

These DACs are also more flexible than any other: 4-quadrant multiplying, double buffered, single supply operation from +5V to +15V, right- or left-justified data format, micropower operation (2mA max), and output current mode setting time of 500ns in a 20-pin DIP.

For non- μ P interfacing needs, National has the DAC1020 and DAC1220. These DACs are direct replacements for, and are priced 30% to 300% lower than, the AD7520, AD7521, AD7530, AD7531 or AD7533.

These inexpensive D/As start at \$4.00 at 100 pieces. And because of National's volume capacity, no one can sell for less. 2

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Introducing STARPLEX with ISE.

The fully developed development system.

The Practical Wizards have done it again.

They've created an easy-to-use development tool that helps design engineers do their whole job on the STARPLEX development system.

STARPLEX can not only develop software for 8080, 8048, 8049, 8050, 8070, NSC800, 8085, and Z-80 microprocessors plus BLC/SBC Series 80 boards, but now with ISE (in-system-emulation) you can also test, analyze and debug prototype hardware/software for the same products.

Multiprocessor capability.

The ISE module is a separate unit incorporating its own CPU, 32K bytes of user-programmable memory and all the necessary logic for breakpoints, tracing and memory mapping. With ISE, you can simultaneously run two prototype microprocessors (in any combination). So for the first time, you can have real-time emulation or debugging in a multiprocessor environment.

Better yet, since ISE does not share the STARPLEX BUS, the system does not have to compete for memory access with its STARPLEX host. So ISE is the only development tool available that offers real-time emulation with 32K real-time map memory.

There's ISE and there's ISE.

National's easy-to-learn ISE software comes completely integrated into the STARPLEX system, including the unique Automatic Testing or "In-File" capability. In-File is an automatic testing mode that will implement a predefined sequence of tests. ISE can also record those results to show exactly how each part of the system performs during the tests. Our symbolic debugging capability provides not only the usual breakpoint conditions, but also a "coast" command which allows you to continue executing a program after the breakpoint combination has been satisfied.

Look into our ISE.

ISE 8048 has all the 8080 features mentioned above plus the ability to read and disassemble internal ROM; make patches in assembly code; support 11 MHz components; support the entire 8048 family; and use prototype crystal clocks.

The Z-80 ISE is a bus-compatible board that plugs directly into STARPLEX. It can support 2-4 MHz Z-80s; provide 4 tracing options; supply relational and regional breakpoints; and provide refresh for prototype memories.

STARPLEX with ISE offers features not found in any other development system, yet it costs substantially less to own and operate than any competitive system.

Practical Wizards, indeed.

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H

Single-chip CRT controllers need less support.



DP8350 Series of programmable controllers most widely used among major CRT makers.

National's powerful CRT controllers require considerably less support circuitry than any other CRTC available. Due in part to single-chip bipolar circuitry, the DP8350 Series CRTCs serve as fully dedicated CRT display refresh circuits in 40-pin packages.

This, combined with the DP8350's enhanced versatility provides an unprecedented ease of system design.

Single-chip versatility.

The DP8350 Series, which includes the DP8350, DP8352 and DP8353 CRTCs, offers a wide range of programmability using internal mask programmable ROMs. In the character field, for example, both the total number of dots per field (up to a 16 x 16 dot matrix) and the number of scan lines per character may be specified. The number of characters per row (from 5 to 110) and character rows per video frame (from 1 to 64) may be programmed as well.

A complete set of video outputs is available including cursor enable, programmable vertical blanking and programmable horizontal and vertical sync.

In addition, the DP8350 CRTCs feature an internal dot rate crystal controlled oscillator. For those systems where a dot rate clock is already provided, the DP8350 Series may use an external clock input. Either way, the buffered dot rate clock output ensures system synchronization.

The DP8350s also provide such system sync and program inputs as 50/60 Hz control, system clear, external character/line rate clock and a character generator program. Also featured are three on-chip registers for external loading of the row starting address, cursor address, and top-of-page address. Twelve bits (4K) of bidirectional TRI-STATE[®] character memory addresses allow interface to character memory.

DP8350 at the heart of the best designs.

The popular DP8350 Series has already been designed into the terminals made by nearly every major CRT terminal manufacturer. Because the Wizards at National not only offer superior controllers, they also produce a wide variety of complementary design components. Character generators, μ Ps, memory products, just to name a few.

And what's more, it's all ready for immediate delivery.

Showcasing National's new family of 8-bit A/Ds.

National's 8-bit A/Ds not only interface to any μ P bus, they also feature absolute or ratiometric operation, and require just a single 5V supply at almost no current at all.

Of all the 8-bit A/Ds on the market, only National offers single-channel differential analog input A/Ds in 20-pin DIPs – the ADC0801/2/3/4. In addition, their ADC0808/9 8-bit converters feature 8-channel analog input multiplexers, each in a 28-pin DIP. The top-of-the-line ADC0816/17 each contain a 16-channel analog input mux in 40-pin DIPs.

The new line of 100μ sec A/D converters eliminates the need for external zero and full-scale adjustments and features an absolute accuracy as good as $\pm 1/4$ LSB.

National, the leader in innovative, cost-effective data acquisition products, now has the best price/performance of any A/D available. In 100-piece lots, the ADC0804 costs only \$2.95; the

ADC0809 a low \$3.60; the ADC080819 Practical Wizardry strikes again - all costs just \$7.95. the way down to the bottom line. 2 START ADC0808/9 8-BIT A/D INTERRUPT CONTROL & TIMIN ~ 8 ANALOG INPUTS 0 MPARATO 0 8-BIT OUTPUTS SWITCH TREE 3-BIT ADDRESS ADDRES AND ADDRESS 2568 RESISTOR LADD

LM335-hot new linear temperature sensor.

The LM335 is a two-terminal I.C. that looks like a zener with a +10mV/°K temperature coefficient. The LM335 is rated for operation over -55°C to +150°C, and has an over-range up to +200°C. Initial accuracies are available at 1°C, 3°C, 6°C but a third lead makes the LM335 very easy to calibrate. Typically, 1°C accuracy is achieved over the entire range when it's calibrated at only one temperature.

The low operating current means low error even for remote temperature measurement. Further, the LM335 eliminates the need for linearizing circuits, thus

making interfacing to a readout or to control circuitry even simpler still. Whether you're designing measurement control, protection circuitry, solar heating, environmental control or thermostats, National's new series of temperature sensors have a lot going for them. At only \$.95, it's time to start sensing temperature with I.C.s. 3

UTPUT 10mV °K

New LM385 12 μ W micropower reference. The lowest power reference available.



LM385 Design Features

- operating current of 10µA to 20mA
- -1% and 2% initial tolerance
- low voltage reference (1.235V)
- stable under large capacitive loading
- low temperature coefficient
- low noise, good long-term stability
- -1Ω dynamic impedance
- replaces older devices with a tighter tolerance

The new LM385 is yet another example of National Semiconductor's commitment to supply high-performance references. Where power is a primary concern (as in battery-powered equipment, portable meters, or generalpurpose analog circuitry with battery life approaching shelf life), this device provides performance unmatched by traditional discrete devices.

For applications requiring other reference voltages or performance specifications, National Semiconductor has the device you're looking for. For example: -Vref 2.5V; 5.0V; 6.9V; 10V

- Initial Tolerance as low as .01% -TC max as low as 0.5ppm/°C

Is it any wonder that more and more design engineers are looking to National Semiconductor's linear references to 2 solve problems?

LM359 amplifies on current amplifiers.

When design engineers said they needed a low-cost dual that was similar to the guad LM3900, but with operation in the video frequency range, the R&D Group at National Semiconductor came up with the answer. It's the LM359 Dual, High Speed, Programmable, Current Mode Norton Amplifier.

The primary design emphasis was placed on high frequency performance and providing user-programmable amplifier operating characteristics.

Each amplifier is broadbanded to provide a high gain bandwidth product, (up to 400 MHz), a high 60V/usec slew rate and stable operation. They're designed to operate from a single supply and can accommodate input commonmode voltages greater than the supply.

The LM359 solves a lot of applications problems: general purpose video amplifiers; high frequency, high Q active filters; photodiode amplifiers; wide frequency range waveform generation circuits.

Now design and application engineers have what they need, thanks to National Semiconductor. 3





AF100 active filtersa universal solution to cost problems.

In the past, the easiest and least expensive means of active filtering was with discretes. But this is no longer the case thanks to National's new AF100 universal active filters.

The AF100s are internally adjusted to provide center frequency accuracies of $\pm 2.5\%$ (for the AF100-1CN model) and $\pm 1\%$ (for the AF100-2CN model).

And because of their small size and low external parts count, the AF100 active filters lend themselves perfectly for use in MODEMs and many other telecommunications applications that require lowpass, highpass, or bandpass filter configurations.

But there's more to the price/ performance story than just design versatility and decreased manufacturing costs. The AF100 universal active filters are attractively priced as well. By way of illustration, the AF100 is currently available in large quantities for less than \$3.00 each.

Just another example of Practical Wizardry cutting your costs to the bone.

Data Acquisition-A National perspective.







In the serial scheme, requests for service on the shared bus are ordered by priority on the basis of bus location. Each processor on the bus notifies the next lower priority processor when it needs to use the bus, and monitors the bus request of the next higher priority unit. The highest priority unit in the system will receive bus mastership. A busy line is used to inhibit higher priority users from destroying a current bus transfer already in progress by a lower priority requestor.

In the parallel technique, bus mastership is resolved through the use of an external hardware arbitrator. The bus request lines from the various processors in the system are fed to a priority encoder that generates a code representing the highest priority device currently requesting the shared bus. This coded level is decoded into a bus access line for each processor in the system. Through this technique, bus access is granted to the highest priority master.

Serial Interface

The multiprocessor communication techniques discussed so far have been based on such parallel bus schemes as parallel registers, FIFO buffers, and shared memory configurations. Where processors are geographically dispersed, as in process control and laboratory automation systems, bit serial interface methods become very attractive. Serial interfaces have the advantage of reducing long distance wiring costs over those entailed by parallel techniques. They are also capable of interfacing to standard voicegrade telephone lines.

Many of the system configurations used in interconnecting processors with parallel techniques apply as well to serial interfaces. The connections can form star, ring, and totally connected structures. In a star configuration (Fig 3) one processor forms the center and acts as a network controller (master) with a separate line to the other





processors (slaves). This structure can be hierarchical, since a slave processor to one star structure can be the master for a different star configuration. In the multidrop scheme, one line acts as a bus to all the processors. Communication is handled by polling from a master processor, and communication between processors is only possible by sending messages through the polling processor. In a ring configuration, each processor is connected to the other processors in a loop arrangement. Data packets from one processors retransmit the packet until the destination is reached. Usually, there is a network master to delete packets not acknowledged by a receiving node.

None of these system configurations adapts well to partial communication failures. When a master fails in a star configuration, the slave processors go offline. Redundancy is required at all levels of the system to avoid the problem of a master failure. In the multidrop arrangement, if the polling computer fails, no processor can communicate. In a ring system, any processor failure inhibits normal communications.

References

- 1. The Z8000 Family of Microcomputer Components, Zilog, Inc, Cupertino, Calif, 1978
- W. Plummer, "Asynchronous Arbiters," IEEE Transactions on Computers, Jan 1972, pp 37-41

Editor's note: a feature article closely related to the subject addressed in this column can be found on p 137, this issue.

Part 2 of Mr Gable's column discusses common bus and shared resource schemes, and will appear in the March issue.

For IBM mainframe and major mini-computer users, Adage 4000 Series systems now offer the same superior performance that has made us, for years, the recognized leader in interactive graphics. All systems feature host channel speed interfaces, host computer off-loading, image buffer, local hard copy output, and highspeed interactive displays.

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and direct interfaces to popular mini-computers.

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Check with your systems manufacturer when you need additional supplies. Or simply call 800-328-1300 for more information. (In Minnesota, call collect: 612-736-9625.) Or write: Data Products, 223-5E, 3M Company, St. Paul, MN 55101.



Econo/Mate. More power for your power supply dollar.

Power/Mate's new Econo/Mate open frame linear power supplies now pack a bigger punch. They offer up to 33% more power from the same case size than many competitive models, at no increase in cost. That means you can achieve even greater reliability from the Econo/Mate by operating at a percentage of full load. Or, alternatively, pack more power in a smaller space.

You get more features as standard. OVP on all 5 volt outputs, standard. Dual 105-125/210-250 VAC inputs on all supplies, standard. Remote sense capability on all supplies is standard, except EMA-A and ETA-B.

Fifty Econo/Mate models from 5 to 24 VDC, up to 25 Amps. Single, dual, and triple outputs including the popular disc drive supplies. Think of them as the new old standby.

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EMA-5CCV EMA-5DV EMA-5FV	5V @ 11.0A 5V @ 15A 5V @ 25A	\$ 74.00 \$ 94.00 \$149.00	EMA-12/15D	15V @ 5.0A 12V @ 8.8A 15V @ 8.0A	\$ 94.00	ETA-515BV	5V@1.2A	12V @ 0.5A 15V @ 0.5A	\$ 48.00	ETR-122EV ETR-132EV	5V @ 6A	+12V @ 1.5A +15V @ 1.3A 18V @ 1.0A	-12V @ 1.5A -15V @ 1.3A 12V @ 1.5A	\$115.00 \$115.00
EMA-6A EMA-6B	6V @ 1A	\$ 27.00	EMA-12/15F	12V @ 16A 15V @ 15A	\$149.00	ETA-515CV	5V @ 3.0A	12V @ 1.5A 15V @ 1.3A 12V @ 3.0A	\$ 68.00			20V @ 1.0A 24V @ 1.0A	15V @ 1.3A	0110.00
EMA-6C EMA-6CC	6V @ 5.5A 6V @ 10A	\$ 59.00 \$ 74.00	EMA-18/20A	18V @ 0.4A 20V @ 0.4A	\$ 27.00		01 6 0.04	15V @ 2.8A	- 40.00	Disk D	rive Power	Supplie	s, Dual Out	put
EMA-6D EMA-6F	6V @ 13A 6V @ 22A	\$ 94.00 \$149.00	EMA-18/20C	18V @ 2.5A 20V @ 2.3A 18V @ 1.2A	\$ 59.00 \$ 35.00	ETA-524BV ETA-524CV ETA-524DV	5V @ 1.2A 5V @ 3.0A 5V @ 6.0A	24V @ 0.4A 24V @ 1.0A 24V @ 2.3A	\$ 48.00 \$ 68.00 \$ 96.00	Model ED-512AAV	Output 1 +12V @ 1.1A (Av)	Output 2 + 5V @ 0.7A		Price \$ 41.00
EMA-9/10A	9V @ 0.75A 10V @ 0.75A	\$ 27.00		20V @ 1.0A 24V @ 1.0A	• 00.00	ETA-12/15B	12V @ 0.5A	12V @ 0.5A	\$ 48.00		+12V @ 1.7A (Pk)			
EMA-9/10B	9V @ 1.8A 10V @ 1.8A	\$ 35.00	EMA-18/24CC	18V @ 4.5A 20V @ 4.0A	\$ 74.00	ETA-12/15C	15V @ 0.5A 12V @ 1.5A	15V @ 0.5A 12V @ 1.5A	\$ 68.00	Disk D	isk Drive Power Supplies, Triple Output			
EMA-9/10C	9V @ 3.8A 10V @ 3.6A	\$ 59.00	EMA-18/24D	24V @ 3.8A 18V @ 7.1A	\$ 94.00	ETA-12/15D	15V @ 1.3A 12V @ 3.0A	15V @ 1.3A 12V @ 3.0A	\$ 96.00	Model	Output 1	Output 2	Output 3	Price
EMA-9/10CC	9V @ 8A 10V @ 7.5A	\$ 74.00		20V @ 7.0A 24V @ 6.5A	Sec. The		15V @ 2.8A	10V @ 2.8A		ED-5240V	24V @ 1.7A(Pk) 24V @ 3.0A (Av)	+ 5V@1A	-5V@0.5A	\$ 72.00
EMA-9/100	10V @ 10.5A	\$ 94.00	EMA-24A	24V @ 0.4A	\$ 27.00					ED-5240V	24V @ 3.4A (PK) 24V @ 5A (Av)	+ 5V @ 3A	-5V@0.5A	\$ 94.00
EMA-12/15A	12V @ 0.5A	\$ 27.00	EMA-24C EMA-24F	24V @ 2.3A 24V @ 12A	\$149.00						24V @ 6A (PK)	101 @ 04	UV @ 0.0M	\$120.00
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Model	Mounting Surfaces	Dimensions	
EMA-A	2	3.78" x 3.03" x 2.15"	
EMA-B	3	4.87" x 4.00" x 2.07"	
EMA-C	3	5.62" x 4.87" x 2.95"	
EMA-CC	3	7.03" x 4.90" x 3.23"	
EMA-D	4	9.00" x 4.87" x 3.20"	
ETA-B	2.	4.90" x 4.03" x 2.25"	
ETA-C	4	7.90" x 4.03" x 2.93"	
ETA-D	4	9.40" x 4.90" x 3.23"	
ETR-E	4	11.00" x 4.90" x 3.23"	
EMA-F	3	16.75" x 4.87" x 4.94"	
ED-AA	3	6.50" x 4.00" x 2.07"	
ED-B	4	10.25" x 4.00" x 2.95"	
ED-C	4	11.00" x 4.87" x 3.20"	
ED-D	4	11.00" x 4.87" x 3.20"	



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The design headstart

A lot of work is done beforehand: Hardware design. PC board layout, manufacturing, testing. TM990 modules come preassembled, pretested. Shortening your design cycle. Getting you to market faster.

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TM990 modules are specified to operate over the full commercial temperature range of 0° to 70° C.

All components must pass strict quality assurance criteria before assembly. Every assembled module is tested, temperature cycled, burnedin, and retested to assure highly reliable operation.

Precision performance

The TM990 modules incorporate TI's 16-bit microprocessors — already a standard in the world of process control. The architecture is more powerful, the instruction set richer. The modules are backed by high-level languages for easier, faster programming. Result: more programmer efficiency, more operational precision.

Wide choice available

TI distributors stock TM990 modules for off-the-shelf delivery.

Your broad choice includes modules for evaluation and OEM applications. Memory expansion. Data entry and display. Digital I/O expansion (see listing in the next column).

Interfacing to motors, generators, contactors, etc., is simplified by industrial ac and dc I/O modules, optically isolated for system protection. A series of A/D and D/A interface modules is also available.

On-going leadership: A floppy disk controller and a bubble memory module have just been added to the TM990 Series. Soon to come: A speech module. And industrial communication modules.

Forward-looking bus: From day one, all TM990 modules have communicated over the same fully documented bus which simplifies system integration and development of customized modules. The TM990 Bus definition supports memory expansion to 16 megabytes as well as multiprocessing applications.

Ready-to-use software support

The affinity of TI's 16-bit microcomputer modules for high-level languages contributes substantially to programmer efficiency. Ready for use immediately:

Power Basic: This English-like language speeds programming even for the novice. It is easy to learn, to

Way to Go

TM990 microcomputer modules are making a significant impact on the industrial market. They daily prove themselves the ideal means for quickly bringing 16-bit economy and performance to end products ... to the production line. Choose the TM990 Series and you join the best of companies. To name a few: Varian, Analog Devices, Dow Chemical, ITT, Loral, Autotrol, U.S. Steel, Owens-Corning, Gulf Oil, Chrysler, Lockheed, Boeing, Teledyne, Delco, Litronix... and, of course, TI.

TI's TM990 Microcomputer Series

Microcomputer Modules: TM990/100M TM990/101M

Evaluation Module: TM990/180M

Educational Module: TM990/189

Memory Expansion Modules: TM990/201 EPROM/RAM TM990/203 Dynamic RAM TM990/206 Static RAM TM990/210 Bubble Memory TM990/303 Floppy Disk Controller

> I/O Expansion Modules: TM990/305 TM990/310

Industrial I/O Modules: TM990/5MT Series

A/D and D/A Interface: TM990/1000 Series (Analogic) TM990/1240 Series (Analog Devices)

use, to document. It has I/O features for process control and enhanced speed for real-time applications. It is designed for use on a single microcomputer module or in an expanded module system.

TI Microprocessor Pascal: This new high-level language, which TI has pioneered, provides the most extensive support available. It enables you to solve application problems without getting involved with the intricacies of machine architecture. You have fewer errors because the code is easy to write, document, read, and modify.

Ready-to-use development system

The AMPL* prototyping lab maximizes software productivity. It contains, in one versatile unit, everything required to develop your software and to check out your system hardware.

Available either as a floppy-based system or multi-user hard disk system, the AMPL lab supports Basic, Pascal, Fortran, and assembly language.

The very affordable modules

Considering the performance and reliability you get... the savings in design time and programming... and the elimination of those expenses associated with make-ityourself modules, the TM990 modules are the best buy in the industry—16 bits for the price of 8.

Choose your help

When you bog down, dial (713) 776-6632. That's the Houston hot line. TI application engineers stand by to answer your technical questions.

If you want a firsthand look at the TM990 modules, or the AMPL lab, call or visit your local TI distributor Systems Center where TI-trained applications engineers will arrange demonstrations.

TI Regional Technology Centers hold monthly courses on the TM990 modules, the 9900 Family microprocessors, Power Basic, Microprocessor Pascal, and the AMPL lab. Check your nearest TI distributor or TI field sales office for dates, locations, and fees.

For a copy of the latest brochure containing more complete information on the TM990 mi-

crocomputer modules, call your TI distributor. Or write Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Texas 77001.



*Trademark of Texas Instruments Incorporated

TEXAS INSTRUMENTS

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Distributed Processing System Communication Links Eliminate Need for TP Software



ities as well as over land lines

Communications capabilities of the ResponseTM coordinated network processing system, recently introduced by Paradyne Corp, 8550 Ulmerton Rd, Largo, FL 33540, are based on the company's line of LSI and microprocessor based high speed modems, the ANALYSIS network management and control system (Computer Design, July 1978, p 18), PIX II virtual

data links (Computer Design, June 1978, p 28), and PIXNET networking systems (Computer Design, Aug 1978, p 30).

Response distributes intelligence throughout the network and provides full duplex SDLC-type communications without conventional IBM teleprocessing access schemes such as VTAM, TCAM, or NCP. Elimination of the TP software decreases overall processing workload on mainframes. Polling, error correction, routing, and application selection requirements are implemented within the network itself, without host intervention.

Communications in the Response system are controlled by attached communications processors (ACPs) that are integrated into the Response

NEC Spinwriters. Super terminals.

Six feature-laden models to fit any teleprinter network.

NEC Spinwriter[™] terminals are fine-quality communications devices that are enriching thousands of terminal networks.

Users call them "super" terminals because Spinwriter devices are versatile, user-configurable, quiet, dependable, and print at rates up to 55 CPS.

They come in six models, including an APL/ASCII model. They have numerous operator convenience features. They are available in both RO and KSR configurations. And they offer a wide variety of forms handling options.

Our APL/ASCII model, for example, supports the APL programming language and character set. Automatic tab setting simplifies printing of columns. And our unique 128character print elements allow you to convert easily—by switch or under software control—from APL to ASCII mode.

Spinwriter terminals offer more forms-handling options than other terminals: vertical, horizontal or bidirectional tractors; and pin-feed, friction-feed, bottomfeed, front-feed and cut-sheet devices. Most are operator-changeable. NEC Spinwriter terminals are the most rugged, and the quietest, typewriter-quality terminals you can buy. Our 2000hour MTBF assures maximum uptime. Our 60 dbA sound level lets you put them in an office.

For more information about NEC terminals, call our nearest sales office.

NEC. Going after the perfect printer.

NEC NEC Information Systems, Inc.

me Office and Eastern Region. 5 Militia Drive, Lexington, MA 02173, (617) 862-3120 Central Region: 3400 South Dise Drive, Dayton, OH 45439, (513) 294-6254 Nestern Region: 8939 S. Sepulveda Bivd., Los Angeles, CA 90045, (213) 670-7346 Southam Region: 2965 Flowers Rd, South, Atlantis, GA 30341, (404) 456-7014



"ZIF connectors help me innovate with microprocessors. And AMP makes more ZIF connectors than anyone."



1. Large boards mate easily without damage

2. ZIF Connectors replace card guides



3. All board edges can be used for I/O's

AMP ZIF connectors—for Zero Insertion Force—give you more ways than ever to take advantage of microprocessor technology. While providing you with extra benefits of their own.

Benefits that allow you to design-in such features as larger pc boards, higher density packaging, and modular "addon" capability.

ZIF connectors will also eliminate problems. Such as back panels, worn contacts, and board damage during test or insertion. And when you use ZIF connectors as card guides, all four sides of the board are available for interconnect, so you can shorten circuit traces, reduce voltage drops, and separate power and signal circuits, economically.

To help you accomplish all this, AMP provides three principal types of ZIF connectors: Rotary Cam Actuated Edge connectors, Linear Cam Actuated Edge connectors, and our exclusive Stacking connectors.

All of them are designed to enhance your interconnections while providing easy board insertion. Just open the contacts with the cam, slide in your board from the edge or the top, and close the contacts the same way. No auxiliary devices or mallets. And later access to the board is easier, too.

Of course, AMP ZIF connectors also come with full engineering support for technical assistance, whenever, or wherever you need it.

For more information about the advantages of ZIF connectors and how you can use them in your innovative designs, simply call or write us.

AMP has a better way.





4. Stacking ZIF's eliminate backplanes

5. Ideal for test equipment

Some facts worth knowing about AMP ZIF connectors:

Rotary Cam Actuated

- .100" x .200", .125" x .250", or .156" x .200" contact centers
- sizes up to 65-dual positions
 open or closed ended with pc board
- registration lockavailable in versions that sequentially actuate
- ground, power and signal circuits

Linear Cam Actuated

- .100" x .100" or .125" x .125" centers
- available as complete assemblies or separate components
- sizes up to 140-dual positions
- high normal force design eliminates the need for gold board edge fingers
- top or side entry for maximum design flexibility

Stacking

- .100" x .100" centers, ideal for bus organized circuits
- provides shorter electrical paths between boards
- · eliminates need for backplanes
- sizes up to 50-dual positions

Where to call: ZIF Connector Information Desk, (717) 780-8400.

Where to write: AMP Incorporated, Harrisburg, PA 17105.

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43

Winchester users we did it!

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Spring



We've put a price tag on your backup dreams.

Fulfilling your backup dreams for the Winchester was one thing. Doing it at the right price was quite another. DEI is happy to announce success on both scores. Our new 10 and 20 MByte high density streaming cartridge tape drives are less than half the price of Winchesters.

The basic 10 MByte is \$415, the 20 MByte version is just \$525. And here's what you get for the price:

Speed: Transfers data at 5 MByte/per minute.

Capacity: Just what you want. 10 or 20 MBytes. A perfect match for the 8" or 14" Winchester's capacity. Reliability: We certify our cartridges to provide it.

Ease of Use: Cartridge operation is simple enough for a person without any computer training to use.

Size: Compact enough to be interchangeable with flexible disks.

Streaming Electronics: Optional formatter and streaming controller with automatic gain control and interdispersed resynchronization. Error correction is also available as an option.

And at DEI we're so sure our new products are the answer to your backup dreams that we've backed up our own production capacity with another 77,000 square feet of plant space.

Now that we've got them, all we can say is "come and get it'. They're your backup dreams come true!

Data Electronics Inc.

20 MByte Cartridge Tape Drive



"I went flat instead of fluffy."

"As an engineer, I used to get pretty frazzled whenever I had to use twisted pairs.

Heaven knows, I needed the performance, but the labor costs drove me wild!

Then one day Dave from Spectra-Strip stopped by and solved all my problems—he showed me their new Twist 'N' Flat.[®]

How fantastic—twisted pairs in a flat cable with flat, parallel sections that I can mass terminate wherever I need them on the cable. (Standard spacing is 18" of twist with 2" of flat, but if I order as little as a thousand feet at one time, they'll put in any spacing I want!)

Well, let me tell you—this has reduced termination time by 97% and cut our costs by 36%. I liked their thinking so much, I checked them out and found that they were a terrific

© Spectra-Strip Inc. 1979

source for all my flat cable needs—cable, connectors, and even complete terminated jumpers and custom assemblies, fully tested and ready to go.

If you're as concerned about your interconnect performance and costs as I am, you really ought to write Spectra-Strip, 7100 Lampson Avenue, Garden Grove, CA 92642, telephone (714) 892-3361. In the East, call (203) 281-3200. But don't ask for Dave—he's at home taking

care of the baby."



When you're down to the wire.

transaction processor. Major ACP elements include 32k processor, byte multiplexer channel adapter, line controller module, and peripherals controllers. Remote peripheral devices are attached to the ACP, which connects to the byte multiplexer channel on the Response processor. ACP communicates with a PIXNET network control unit (NCU) which communicates with a local control unit (LCU) attached to the byte multiplexer channel of the IBM host (see Figure). Each NCU can support up to seven lines for communication with other ACPS and/ or other transaction processors.

PIXNET communications capability allows CRT terminals, with proper authority, to directly access any application in the network as a local device. Response applications can also access facilities of other interactive systems, communicating as if they were local 3270s. A high speed read/ write transfer facility is provided for transmission of bulk data files.

Response is a fully integrated distributed processing network system using two models of a 32-bit processor. One, a 400-ns entry level system has up to 1M bytes of memory and supports as many as four integrated channels. The second, a 240-ns version, has up to 2M bytes of memory and up to seven integrated channels. Both are IBM System/370 oriented and are optimized for transaction processing tasks. Both processors have 1-bit error correction, 2-bit error detection, and memory 1/0 transfer rates of approximately 7M bytes/s. Circle 400 on Inquiry Card

Supervisory System Design Speeds Network Control Functions

Communication line supervision, EIA interface surveillance, communication system fallback, and rapid network reconfiguration are the functions of network control addressed by the Network Control SystemTM. The system adds a second level of modularity to conventional tech control concepts in the physical configuration of its test, patch, display, alarm, and switching modules. Modems and computer port cables are attached to the rear of the system racks, with the functional modules removeable from the front via edge connectors.

With this arrangement, each EIA interface can be equipped with a module for displaying major EIA interface signals and producing alarms on selected error conditions, or a module for bit error testing, or a patching module, or one that can switch a computer port between modems. Programmable options also permit alarms and switching to be either manual or automatic. This cabling and module configuration is said to speed detection and correction of technical problems in the network.

The system, designed and manufactured in Europe by Tech-Nel Ltd, is now being manufactured and marketed under license in the U.S. by Digi-Log Systems, Inc, Babylon Rd, Horsham, PA 19044.

Each EIA RS-232 interface is monitored constantly for eight possible fault conditions. The network can be reconfigured by modules that contain port, modem, and monitor receptacles. Any communication port can be addressed by means of a 10-key numeric pad and connected to the supervisory system bus for failure analysis in conjunction with the company's DLM II data line monitor and tape trap for centralized troubleshooting. Channel failures are resolved by any of four automatic/manual fallback techniques.

Main system modules are as follows: supervisory alarm module monitors EIA interface channel integrity; alarm module monitors all channels for failure; a programmable switching module, with a capacity for 16 switching routines, manually or automatically switches a port between two modems; switch contoller and interface unit controls up to 256 switching modules. Any of 16 resident programs in each module can be selected, and programs can be created and loaded as required; error test module generates 511-bit pseudorandom test pattern and gives visual indication of bit and block error counts as well as calculated error rates.

In addition to the main modules mentioned, the user may configure line drivers, modem eliminators, modem sharing devices, data line monitors, and tape recording equipment. The system can be furnished for standard 19-in (48-cm) rack mounting, or integrated into desktop consoles.

Circle 401 on Inquiry Card

New coach for PDP-11 team is full-color graphics system.

The coach of PDP-11's team is our new AED512 graphics generating system that makes the blackboard obsolete. Now, when he plots the plays, the FIVE TWELVE's compact video terminal will display all the action in highresolution detail using up to 256 simultaneous colors and 16.8 million different hue/intensity combinations on a 512 x 480 pixel screen. The AED512 is microprocessor controlled, and has the largest refresh memory of any system in the league.

Other features that make the new PDP-11 'coach' a cost/performance leader include:

- DMA interfaces (Q-BUS^R or UNIBUS^R) available.
- 2:1, 3:1 . . . 16:1 zooming. Panning via integral joystick.
- Vector and circle generation. Curve fill. Single-point addressability.
- Crosshair cursor with programmable color.
 SUPEROAM panning over 1024 x 2048
- contiguous pixels.Programmable character fonts and
- 8 programmable special function keys.
- \$8,875 with two colors only, excluding monitor and DMA.

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CIRCLE 30 ON IN



Grow with the MSC 3605

The MSC 3605 is an add-in, single-board semiconductor memory system, designed to extend the capabilities of DEC computers, utilizing full hex-wide UNIBUS or Modified UNIBUS slots. On-board provisions include a standard parity Control Status Register (CSR) for parity generation and checking. Expandable in 32K byte increments to 128K bytes with or without parity, the MSC 3605 provides OEM designers and end-users with a number of important operating advantages:

Design Versatility The MSC 3605 is switch selectable between Modified UNIBUS and Standard UNIBUS interfaces. On-board DIP switches allow the user to quickly set up starting address and





storage capacity in 1KW boundaries and CSR address.

Memory Reliability Low power consumption and fewer components contribute to the high reliability inherent in the MSC 3605. Predicted MTBF is over 40,000 hours.

Future Growth Socketed elements provide for both simplified maintenance and future expansion.

For additional information on the MSC 3605 and our other 41 Monolithic Systems Corp. products and systems, please contact us at 14 Inverness Drive East, Englewood, Colorado 80112. (303) 770-7400. Telex: 45-4498.

Extending the limits of information.



MSC Regional Sales Offices: Eastern Region 1101-B9 State Road, Princeton, NJ 08540, (609) 921-2240; Central Region 7200 East Dry Creek Road, Suite #B203, Englewood, CO 80112, (303) 773-1060; Western Region 49 South Baldwin, Suite D, Sierra Madre, CA 91024, (213) 351-8717

Fiber Optic Link Operates to 200k Bits/s



Like its high speed predecessor previously introduced (*Computer Design*, July 1978, p 18), this TTL-compatible link offers secure transmission, electrical isolation, and protection against electromagnetic interference. It operates from dc to 200k bits/s, using an NBZ format with no coding restriction. The fully assembled and tested link has a bandwidth of 100 kHz, comes in cable lengths up to 1 km, and is available from 3M Company, Dept EP9-19, Box 33600, St Paul, MN 55133.

The link consists of two transceiver modules and preterminated flat or round cable. Each module contains an infrared-emitting GaAs LED light source, and a PIN photodiode detector. The connecting cable is made up of two plastic-clad silica fibers in a PVC jacket for full duplex operation. Two cable types are currently available; a flat version in lengths to 150 m, and the other a round cable in lengths to 1 km. Typical cable attenuation is 25 dB/km, and connector attenuation is less than 2 dB/mated pair.

Power requirement is 5 V. Price of the data link, less cable, is \$228. Reinforced preterminated cable is \$4.10/m. Delivery, eight weeks ARO.

Circle 402 on Inquiry Card

New fullback for PDP-11 team is single-card RMO2 emulator.

The fullback for the PDP-11 team is AED's new STORM-02, a hex-card controller/formatter for storage module drives.

We tried out a lot of fullbacks for the team but STORM-02 was the only player that could offer everything! Single hex-card electronics: RH11, RM02 and RM03 emulation: the ability to plug right into the SPC slot on your PDP-11: plus the ability to get along with the media. That's the kind of compatibility we like!

A standard single board STORM-02 handles 4 SMDs. With an optional second hex-card, the STORM-02 can accommodate four more drives for a total capacity of over 500 megabytes.

Our big surprise was the bottom line on the contract. The OEM price for the STORM-02 is just \$2595 for the hex-card electronics — far less than any fullback in the league. The complete system with one 80-megabyte storage module drive, in quantities of one, is \$13,995... about half the price of a comparable DEC fullback.

For the complete statistics and quick delivery, call or write Bob Deisher, Rigid Disk Products Manager.



COMPUTER PERIPHERALS DIVISION 440 Potrero Ave., Sunnyvale, CA 94086 Phone 408-733-3555, Boston 617-275-6400



Protocol Converter Adds Intelligence to Dumb Terminals

GoBetween[™] Translation 100 is a microprocessor based protocol converter that enables ASCII, CRT, and printer terminals to emulate Burroughs, DEC, Honeywell, NCR, and Univac remote devices, and allows them to be online compatible with any CPU or frontend processor. The unit operates asynchronously at speeds to 9600 bits/s, with automatic up/ down speed conversion. Internal DIP switches allow selection of specific addresses in a polled multidrop environment. The device is a product of Modemsplus, Inc, One Perimeter Way, Suite 260, Atlanta, GA 30339.

Polling and prompting capability, 4k P/ROM, 2k RAM, and complete self diagnostics are standard features. Options include 4k RAM, synchronous operation adapter, function key prompting, and forms control.

In standalone applications, the unit has its own power supply; when used as an internal device, power is drawn from the associated terminal. The converter can be tailored to fit virtually any configuration.

Circle 403 on Inquiry Card

COMMUNICATION CHANNEL



Teleprocessing Network Performance Parameters Displayed in Real Time

Net/Alert[™] is a microprocessor based monitoring system that provides realtime, online performance information from every terminal on every line in a teleprocessing network. A series of multilevel display screen formats can track the current status of the entire system, or of a single or group of applications. A color CRT graphics display grades system conditions: green, normal; yellow, potential trouble; and red, operator attention may be required.

Network status screen is the highest level summary display. It shows in simplified block diagram form the entire system status, and displays transaction volume and error rates for all lines in each line group. Among other data displayed are response times for individual terminals, as well

*Patent pending

as smoothed averages over operationsspecified intervals.

Level 2 display, line status, called up by lightpen, joystick, or keyboard entry, shows the state of individual lines within a specific line group, and details current status of each terminal on each line.

Terminal status screen is the most detailed presentation, showing current status of each terminal on a single line plus response time comparisons with prior periods. Also shown are transaction and error rates for each terminal.

The system, a product of Avant-Garde Computing, Inc, 21 Olney Ave, Cherry Hill, NJ 08003, monitors for three kinds of trouble in real time: response time unacceptable, line unavailable, and line marginal. Heart of the system is the microprocessor line set (MLS),[°] attached to the network at the point where data enter the computer facility (see Figure). MLS includes a microprocessor, local memory, and intelligent line interfaces. Each line to be monitored is attached to an MLS by a "T" connection either at the modem RS-232-C connector or at a communications panel rack. Line status and performance are derived by interpretation of modem signals: transmitted and received data and control characters, and modem status indicators.

MLS performs serial to parallel conversion on the bit stream between modem and transmission control unit (TCU), and interprets data and control characters according to the speed, protocol, and coding specified for the line. It monitors bisynchronous, asynchronous, and HDLC protocols, and can interpret the transmission to determine block and transaction counts, error retries, response times, status messages from remote control units, polling frequency, and protocol validity. Maximum MLS bandwidth for synchronous protocols is 56k bits/s.

The MLS is invisible to the host, TCU, remote control units, and all other hardware units in the system. It is also invisible to all levels of system software.

Circle 404 on Inquiry Card

Software Package Adds Versatility to Laboratory Distributed Networks

MINC NFT (network file transfer) is a software package that permits a MINC or MiniMINC laboratory computer system to interact with PDP-11 or vax-11/780 computer systems in distributed networks. It is fully compatible with DECnet communications software. File transfer can be from local to remote, remote to local, and remote to remote. The software can also be used for local management tasks such as copying, deleting, and displaying local files. It is licensed at \$1400, and is available from the Laboratory Data Products (LDP) group of Digital Equipment Corp, Maynard, ма 01754.

The option is applicable to computer systems using RSX-11, IAS, and VAX/VMS operating systems, and is compatible with MINC BASIC software. Connections between a DECNET host and MINC or MiniMINC systems can be via direct cable, acoustic coupler,



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What's the best display system for you? Ramtek has the right choices to fit your needs – and budget.

Graphic displays make your computer data work harder. Color, gray scale, or black and white, simple or sophisticated, you'll find what you need in Ramtek's broad line of raster scan systems, the most complete in the business.

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Special for process control.

The 2000 series is specially designed for process-control applications, and includes the 2500, a one-card character graphics display.

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Ask us about our 3000 series, color and black and white graphics and imaging systems designed to off load your CPU.

More monitors than ever.

Ask us about our 37 different models of monitors. We offer color, gray scale, black and white, a choice of phosphors, a variety of screen resolutions to 1024 lines, and screen sizes to 25".



about Colorgraphics)



What else can you ask for?

Our hard copy color cameras and large screen projection systems, about interfacing to hard-copy color copiers, printer-plotters, and about our complete line of interactive devices: keyboards, light pens, joysticks, trackballs and graphic tablets.

Intelligent alphanumeric terminals, too.

Ask us about our 8000 alphanumeric terminal series. There are three basic models (including one especially for UNIVAC users) plus options to customize them for almost any data entry or telecommunications use.

Why raster scan?



Raster scan has become the preferred technology whenever computer-based information and images must be displayed. To find out what raster scan is and how it compares with alternative display technologies, write for "Raster scan, the display technology of the 80's." It's Issue Number 2 of Ramtek's "USE OUR EXPERIENCE" series.

Ask today.

For complete information on the Ramtek system that best fits your needs, write Ramtek, 2211 Lawson Lane, Santa Clara, CA 95050. Or, call your nearest Ramtek Office.



REGIONAL OFFICES: Santa Clara, CA (408) 988-2211, Newport Beach, CA (714) 979-5351, Seattle, WA (206) 838-5196, Albuquerque, NM (505) 298-2200, Dallas, TX (214) 422-2200, Maitland, FL (305) 645-0780, Huntsville, AL (205) 837-7000, Chicago, IL (312) 956-8265, Cleveland, OH (216) 464-4053, Dayton, OH (513) 278-9461, Washington, DC (301) 656-0350, Metropolitan NY (201) 238-2090, Boston, MA (617) 862-7720, Netherlands 31 2968 5837.

"Designing our own LSI The hard part is finding with some flexibility."

The inflexibility of most LSI manufacturers can be really frustrating. The fact is, they're just not set up to handle "customer designed" projects.

You'll find things a lot different at AMI. We're the *only* major LSI company with a group specially organized to handle these jobs. It's our sole responsibility. Last year, we ran more than a hundred circuits designed by a wide variety of customers. And the list is growing fast.

"We want to do it our way."

That's okay with us. No two customers bring us a job at the same stage of development anyway. So it would be a waste of our time and your effort to set up a lot of hard and fast requirements. Instead, we make it as simple as possible for you to interface with us at almost any design or production phase.

You can supply us working plates, pattern generator or data base tapes, complete test programs or test vectors. We'll take it from there. And we'll provide components at any of these stages: wafers, prototype circuits, or complete, fully tested assemblies.

We don't limit your choice of process, either. We work in 25 variations of four basic MOS disciplines. What's more, our manufacturing capability is large enough to set aside an entire fab line for fast turn-around circuit prototyping. And allocate other fab lines for production runs.

"What makes AMI so great?"

In a word: experience. We have the longest history in custom, with a record of more than 1200 circuits designed and produced since 1966. And we've been involved in customer designed projects for six years, longer than anyone else, completing more than 300 circuits.

We're geared to work with your in-house MOS designers or an independent design firm. Or we can handle your

We're flexible enough to work with you at almost any stage of your circuit development. After all, you're the customer.



COMPUTER DESIGN/FEBRUARY 1980

circuit isn't the problem. a manufacturer

	P Chan Hi V _T Metal	P Chan 1 ² Metal	P Chan SiGate	N Chan SiGate	Comple- mentary MOS	N Chan 1 ²	N Chan 1 ² + dep Lds.	VMOS
Speed (per unit area)	6	4	5	3	2	3	1	0
Power Consumption (low speed)	6	2	4 -	5	1	5	3	3
Area (per logic function)	4	3	3	.2	5	2	1	0
Noise Immunity	4	2	5	5	1	4	. 3	3
Logic Flexibility	3	1	3	3	1	2	1	1
On-Chip Clock Generation	4	2	5	4	1	3	2	2
Bipolar Compatibility	5	2	3	1	. 1	1	1	0
Power Supply Latitude	4	2	4	4	1	3	2	3
Process Simplicity	1	2	2	2	6	3	4	6

AMI offers 25 variations of four basic MOS processes. So you can pick the one that fits your product and budget.

job from scratch, giving it the full custom treatment that has made us the leader in this field.

We're also in a unique position to advise you on the best way to tackle your application. As we also produce standard 4, 8 and 16-bit microprocessors (the S2000, S6800 and S9900), we may be able to show you a cost-effective way to mix standard MPUs and custom peripherals. Or customize a standard MPU specially for you.

"Fine, but I need more details."

We have all the documentation you need, from design and test parameters to production schedules. And we've also just published two new brochures describing AMI's involvement in the custom LSI business. These are "Six Steps to Success with Custom LSI" and "MOS Systems Solutions: A Dozen Case Histories Using Custom Circuits and Microprocessors."

You can get hold of copies by writing to AMI Customer Tooling Marketing (II), 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330. Or from one of these AMI sales offices: California, (213) 595-4768; Florida, (305) 830-8889; Illinois, (312) 437-6496; Indiana, (317) 773-6330;

Massachusetts, (617) 762-0726; Michigan, (313) 478-9339; New York, (914) 352-5333; Pennsylvania, (215) 643-0217; Texas, (214) 231-5721, Washington, (206) 687-3101.

And, if you'd like a "live" show, we'll make a 30-minute presentation right in your office. That should be long enough to convince you how flexible an LSI company can be.



COMMUNICATION CHANNEL

or modem interface, with software selectable baud rate and synchronous or asynchronous operating mode.

MINC NFT is available on diskette. Built-in user aids, including a "help" feature, assist in operations. The system has 20 commands, separated into file commands for local file operations;

calendar commands for data and time; and network commands for data transfer between systems.

MINC and MiniMINC are economical laboratory computer systems that incorporate an LSI version of the PDP-11 minicomputer.

Circle 405 on Inquiry Card

Statistical Multiplexer Adds Multipoint Multiplexing Capability

Multipoint multiplexing capability has been added for UNIBUS^R-based systems using the DCA 205/11 statistical multiplexer to access DCA's integrated network architecture (INA). Configured in a master/slave arrangement, the munications Associates, Inc, 135 Technology Pk, Norcross, GA 30092.

System 205/11 connects remote terminals to DEC PDP-11, VAX, or 2020 computers as an alternative to using DEC DZ-11 asynchronous terminal interface boards, which support eight interface ports. 205/11, on a single circuit board, supports up to 128 ports, provides statistical multiplexing, and takes up only one UNIBUS slot.



205/11 is the master controlling slave units multidropped from a single line. Slaves can be either DCA system 115 or 105 statistical multiplexers, or both. The added multipoint multiplexing capability allows additional savings in telephone line costs, as well as a reduction in the number of multiplexers and modems required in the network, according to Digital ComThe system also provides error-controlled trunk links, choice of fixed baud or autobaud, and choice of modem signal protocols, loop echoplex and character transparency.

Interface is RS-232-C/CCITT V.24/ V.28, with choice of male or female connectors to trunk-link modem. Speed is up to 9600 bits/s, synchronous. Circle 406 on Inquiry Card

-Powell Electronics Huntsville ARIZONA Phoenix—Kachina Electronic Distr. Tucson—Inland Electronic Supply ARKANSAS Tucson—Inland Electronic Suppl ARKANSAS Little Rock—Cariton-Bates CALIFORNIA Los Angeles—Electric Switches Fisher/Brownell Riverside—Electronic Supply San Diego—Fisher/Brownell Sun Valey—Richey Electronics Sun Valey—Richey Electronics COLORADO Denver-Electronic Parts Newark Electronics CONECTICUT Bathel—Heilind Electronics Greenwich—Wise Components Wallingford—Midan Electronics FLORIDA FLORIDA Miami Springs—Powell Electronics Oakland Park—Peerless Radio Orlando—Hammond Electronics ILLINOIS Indiao-rhammond Electronics Addison-LCOMP-Chicago Chicago-Newark Electronics Elgin-Allied Electronics Elk Grove Village-Pioneer/Chicago Northbrook-Classic Components Supply Peoria-Klaws Radio INDIANA Evansville-Hutch & Son Ft. Wayne-Ft. Wayne Electronics Supply Indianapolis-Graham Electronics Ra-Dis-Co. South Bend-Radio Distributing IOWA South Bend—Radio Dia IOWA Cedar Rapids—Deeco KANSAS Wichita—Radio Supply Cedar Rapids—Deeco KANSAS Wichita—Radio Supply MARYLAND Beltsville—Powell Electronics Gaithersburg—Pioneer/Washington Rockville—Capitol Radio Wholesalers MASSACHUSETTS Dedham—Gerber Electronics Hingham—Sager Electric Supply North Adams—Electronic Supply Center Worcester—R.M. Electronics MICHIGAN Livonia—Pioneer/Michigan. R. S. Electronics Oak Park—Newark Detroit Electronics St. Claire Shores—Spemco MINNESOTA MINNESOTA Minneapolis—Newark Electronics St. Paul—Gopher Electronics MISSISSIPPI Jackson—Ellington Electronic Supply MISSOURI Kansas City—LCOMP-Kansas City Maryland Heights—LCOMP-St. Louis St. Louis—Olive Indust. Electronics NEBRASKA Lincoln—Scott Electronic Supply NEW HAMPSHIRE Hudson—Heilind Electronics NEW JERSEY East Hanover—State Electronics Parts Corp. Springfield—Federated Purchaser NEW MEXICO Springfield—F Alburguergue-International Electronics Walker Radio Company NEW YORK NEW YORK Binghampton—ASI Electronics Bohemia—Car-Lac Electronic Industrial Sales Buffalo—Summit Distributors Farmingdale—Arrow Electronics Lynbrook—Peerless Radio Rochester—Simcona Electronics Vestal—Harvey/Federal Electronics NORTH CAROLINA NORTH CAROLINA Greensboro—Hammond Electronics Pioneer Carolina Raleigh—Southeastern Radio Supply OHIO Cincinnati—Hughes-Peters URI Electronics Cleveland-Pioneer/Cleveland Columbus-Hughes-Peters Dayton-ESCO Electronics Pioneer/Dayton OKLAHOMA klahoma City—Electro Enterprises Ilsa—Oil Capitol Electronics OREGON -United Radio Supply Portland — United PENNSYLVANIA PENNSYLVANIA Erie-Mace Electronics Harrisburg-Cumberland Electronics Philadelphia-Almo Electronics Herbach & Rademan Powell Electronics Pittsburgh-Cam/APC Pioneer/Pittsburgh Reading-George D. Barbey RHODE ISLAND Warwick-W H. Edwards RHODE ISLAND Warwick—W.H. Edwards SOUTH CAROLINA Columbia—Dixie Electronics Greenville—Hammond Electronics TENNESSEE Nashville—Electra Distributing TEXAS Dallas—Solid State Electronics TI Supply El Paso—International Electronics Fort Worth—Allied Electronics Houston—Harrison Equipment Kent Electronics UTAH Statford—Southwest Electronics Salt Lake City—Standard Supply Richmond—Sterling Electronics WASHINGTON

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DIGITAL TECHNOLOGY REVIEW

Plug-In Voice Recognition Module Offers 100-Word Vocabulary



Capable of identifying up to 100 words or phrases with 99% accuracy, Interstate Electronics' VRM analyzes speech with 16-filter spectrum analyzer. Module may be used standalone or with host processor since it includes all necessary logic and memory.

A single-board, high accuracy OEM voice recognition module, the VRM can handle vocabularies of 40, 70, or 100 words. Supported by hardware and software development tools, the microprocessor based module, introduced by Interstate Electronics Corp, 1001 E Ball Rd, Anaheim, CA 92803, contains all logic and 1/0 interfacing necessary to convert spoken words into computer codes on a single standard MultibusTM size card.

The discrete word, speaker dependent device provides recognition accuracies in excess of 99% regardless of dialect, accent, or language. A discrimination threshold, to reject undesired inputs, is switch selectable or may be controlled by a host processor. Communication protocol is compatible with high level languages such as FORTRAN, BASIC, and Pascal, easing the job of host programming for incorporation of voice capability.

Support for the system includes an emulator package that serves as a tool

in software development and vocabulary definition. Based on the company's intelligent voice data entry system, the emulator allows potential software systems to be tested without requiring modifications in host programming or logic. A programming workshop in the form of an intensive training course offers a means of acquiring the necessary software skills and hardware familiarity to skillfully use VRM and development support tools. A portable control chassis, the Voterm-I contains all power, switches, and indicators necessary to quickly interface a VRM with a host computer for product development.

The VRM contains a microphone preamplifier and preamplifier bypass switch, allowing direct input using lightweight sM-10, boom mounted Telex cs-75, or equivalent microphone. Alternately, the onboard preamplifier may be bypassed, and an audio signal used. Input is ac coupled and terminated with a resistance of greater than 10 k Ω . Useful audio bandwidth is from 200 to 7000 Hz.

Input speech (80-ms minimum length, 200-ms between-word pause) is analyzed by a 16-filter spectrum analyzer and converted to a digital representation of the characteristics of the spoken input. These digital data are then converted to a fixed size pattern that preserves the information content of spoken inputs while discarding redundant features. During word training these patterns are used to derive templates for each vocabulary item, which are then used in the recognition process for comparison with incoming spoken words. Vocabulary templates are stored in onboard RAMS, while processing algorithms reside in ROM, operating in conjunction with a microprocessor.

During training, the VRM automatically rejects utterances that do not sufficiently agree with the same utterance from previous training samples of that word. This prevents a vocabulary reference pattern from being significantly altered by spurious noises such as coughing or speaking inconsistencies.

First and last word indices may be specified when selecting the mode of operation. Consequently, any contiguous sequence of vocabulary words may be selected for use with the operation. This ensures that only valid responses are accepted as input to the system. A second, common vocabulary level of syntax enables users to select a second contiguous sequence of vocabulary words to be appended to the first set in the recognize mode. Thus, without complex or redundant vocabulary structuring, command and edit words can be automatically appended to the specified set of valid input words. Both functions may be selected with the total vocabulary resident in VRM memory minimizing the need to download small vocabularies.

The unit's serial interfaces are switch selectable to Rs-232-C or 20mA current loop. A full duplex, 8-bit wide parallel signal interface uses common TTL signal levels for easy connection to a host computer communications port or to the digital control logic typical of control system panels. An option replaces the parallel interface to the host with a second serial interface that permits full compatibility with standard communication ports and associated software drivers.

(Continued on page 62)

the more OEMs demand of tape systems, the more we deliver.

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CIRCLE 37 ON INQUIRY CARD

Shugart delivers the lowest cost per megabyte in an 8-inch Winchester drive. The company with more experience in low-cost Winchester technology than anyone else in the industry has broken the \$1,000 price barrier with its SA1000 series of 8-inch fixed disk drives. Here's your 5 or 10 megabyte system upgrade at an affordable price. Here's Winchester performance in a compatible floppy-sized package. Here's an 8-inch drive that will be built in the guantities that you need for your marketplace, using Shugart's high volume manufacturing technology. Introducing the SA1000. Packed with valuable features. And priced to give you the competitive edge.

Introducing the 8"fixed disk drive

It's easy to upgrade your system. Our design objective for the SA1000 was to create an 8-inch Winchester drive as mechanically and electrically identical to our floppy disk drives as possible. The result is a drive that has the same physical dimensions and mounting holes as our 8-inch floppy drives. Also, the SA1000

has a simple "floppy-like" interface and command structure. And drive control signals use the same pin assignments as our SA850/851 floppy drives so you can daisy chain both fixed and floppy drives from the same controller. Software development is simple too, because the SA1000 has the same capacity per track as the double-density SA850. Even the power voltages are the same. All this means that we've made it easy and economical for you to increase data throughput to 4.3 Mb/sec., average access time to 70 msec., and capacity to 5 or 10 Mbytes. Shugart gives you value where it counts. Product reliability—we're Headstrong about it. The SA1000 has 40% fewer parts than a floppy drive. That means high MTBF—8000 power-on hours of typical duty. And no preventive maintenance is required. Error rates equal 1 x 10¹⁰ soft (recoverable), 1 x 10¹² hard (non-recoverable), and 1 x 10⁶ seek. The belt-driven AC spindle drive motor eliminates the need for a separate power supply. Our new Fasflex[™] III ball bearing-supported actuator provides more precise head-to-track positioning. Data reliability? We've eliminated possible media contamination and further protected your data by locating the AC drive and stepper motors outside the media chamber and by shock-mounting the drive on three points within its casing. We don't take shortcuts when it comes to

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Shugart's Headstrong about product availability. From initial product concept through manufacturing, Shugart has designed the SA1000 for high volume, highly mechanized production and backed it with it's own dedicated engineering and manufacturing organization. This kind of commitment has

made it possible for us to bring you the lowest cost per function 8-inch fixed disk drive available today. We'll be delivering the SA1000 drives in the first quarter of 1980. Optional controller and data separator will also be available. The new SA1000 from The Headstrong Company. Contact your nearest sales office. Shugart headquarters: 435 Oakmead Parkway, Sunnyvale, CA 94086 (408) 733-0100; West Coast Sales/Service: (408) 737-9241; Midwest Sales/ Service: (612) 574-9750; East Coast Sales/ Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 17-60-06.



CIRCLE 38 ON INQUIRY CARD

DIGITAL TECHNOLOGY REVIEW

With a TTL signal level parallel I/O interface, a 40-word vocabulary VRM costs \$1650 in quantities from 1 to 9. A 70-word unit with the same interface sells for \$1815, and a 100-word unit has a tag of \$1980. Circle 175 on Inquiry Card

Wideband Signal Digitizer Uses Priority Arbitration For Versatile Operation

WBD-210 is a high speed signal digitizer and storage system designed to interface with the PDP-11 computer via the Unibus. Developed by Banncomm Corp, 1121 San Antonio Rd, Palo Alto, cA 94303, the powerful unit can process analog signal data up to 8-MHz analog bandwidth, all under software control of the host computer.

High speed analog to digital converters permit 8-bit sampling at each of two input ports at any rate up to 10-MHz sample rate (read only) or a single port at up to 20-MHz using high byte/low byte packing in memory. Digital to analog conversion rates are equivalent for write only operation. Rates for simultaneous read and write are half the read only or write only rates.

The memory has a 32k-word (16bit) capacity and is partitioned into 32k-byte (8-bit) high and low byte sections. Memory appears to the PDP-11 as a standard 32k-word RAM and can be used either for storage of captured data or as general purpose computer memory. In addition to high byte/low byte partitioning, the memory can be further partitioned into 256 subpartitions whose size, address range, and allocation (read, write, or general storage) are under full software control.

Key to versatile operation of the digitizer is the priority arbitration and control section. Priorities can be established for read (one or two ports), write (one or two ports), simultaneous read/write, and PDP-11 interrupt. The control section sets the software controlled sample rates, address locations, and in general controls the bidirectional flow of data between the memory and the Unibus.



Interfacing with PDP-11 via Unibus, Banncomm's WBD-210 permits 8-bit sampling on two input ports at up to 10 MHz. System functions are under software control from host. Memory appears to host as standard RAM and can be used either for storage of captured data or as general purpose memory

In operation, the unit serves as a powerful tool to capture and analyze wideband signal data. Signal data cycling through the memory can be continuously analyzed for feature recognition. Once recognized, the data segment of interest may be captured for further analysis, modification, or transmission to external analog or digital analysis equipment. The transmission rate is under software control, independent of the input rate, and can be synchronized to an external clock.

Housed in a DEC H909-BA enclosure, the unit weighs approximately 75 lb (34 kg). Dimensions are $5.25 \times 19 \times 19^{"}$ (13.3 x 48.3 x 48.3 cm) rack mount, and power requirements are 500 W.

Circle 176 on Inquiry Card

Software Combines Word/Data Processing Across Product Line

Extending the applications range of Eclipse systems running AOS, Data General Corp, Office Products, Rt 9, Westboro, MA 01581, has offered AZ-TEXT software and a letter quality printer for the systems. This integrates word processing and data processing functions, and allows the word processing function to benefit from an intelligent multiprogramming system with a sophisticated file security mechanism, various peripherals, and system communication capabilities.

Security features of the Aos software protect documents from unauthorized access but allow sharing of documents when authorized. This se-

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DIGITAL TECHNOLOGY REVIEW

curity mechanism provides the compatibility necessary for transportability of documents between Eclipse systems either via magnetic media or through a communications network.

Menus displayed on the terminal screen allow operators to select the tasks to be performed, such as document creation, editing, or printing. Menus are also used to define print format options such as the number of lines per page, top and bottom margins, and the number of copies.

A template is placed on the keyboard of a Dasher D2 display terminal to indicate function key command assignments. These assignments include insert/delete copy and move blocks of text, insert/delete characters, and find and replace words or phrases. A HELP feature displays commands with their descriptions when the operator needs assistance.

By combining the text editing software with a 55-char/s letter quality printer that provides fully formed characters and changeable print styles, the user attains a versatile word processing system. The printer operates over a standard serial interface so that it can be located anywhere within the office. Its automatic sheet feeder allows the use of standard letterhead paper.

AZ-TEXT is available on all Eclipse datasystems from C/150 to M/600 as well as on scientific processors equipped with character instruction set options. Menus and HELP files are stored separately in memory to allow easy translation into other languages, and the software supports the international character set options on Dasher displays.

Circle 177 on Inquiry Card

Graphics/High Reliability Options Added to ATE Analysis System

Management communications for standard and high reliability testing applications are offered through two options for the Integrator[®] II, a host computer system that provides a central data base for processing and analyzing data generated by automatic test systems (see *Computer Design*, Jan 1979, pp 42, 47). The graphics option, introduced by Fairchild Camera and Instrument Corp, Test Systems Group, 1725 Technology Dr, San Jose, cA 95110, consolidates data from multiple sources into a 1page summary presented in graphic form, while the high reliability software option tracks and tailors reports to operators and managers for sophisticated high reliability facilities.

Large quantities of tabular data are reduced to a single page of 4color concise information that focuses attention on and helps in understanding complex data with the aid of the graphics option. The 4-color pen plotter/digitizer, fully compatible with the Integrator, produces charts, wafer maps, shmoo plots, and composites with boundaries, line and curve drawings, and 3-dimensional illustrations. Included in the graphics package are enhanced video keyboard terminal with dual minicartridge storage devices, Graphics 1000 software/ firmware, and Fairchild software/ firmware. The package is intended for use on any Integrator 11 standard 1/0 interface.

A computer software package that is designed specifically to solve complex data collection problems of high reliability test facilities, the hi rel program efficiently accommodates requirements for data collection, serialized devices, time point testing, sorting and merging, delta calculations, device conditioning, and data archiving retrieval. It provides complex control over specific device data during complex series of test exercises.

Data are collected in realtime, including a test number with each test result and a serial number for each device. Each lot is maintained by control and device number at the same time point. Data are identified consistently in both internal data management and external operator control and archival data. A directory shows the current status of all logged data.

The software sorts test data into appropriate serial number sequence category, then merges that data with data from the same lot at another test point. From this, reports comparing test data on absolute or percentage difference and evaluated against a limit can be prepared with operator selected heading, serial number range, test number limit, time points, and delta measurements. Devices may be rejected or classified at time of comparison and space between time points is unlimited.

The graphics option is available for \$17,600. The high reliability option costs \$11,000. Circle 178 on Inquiry Card

Word/Data Processing Integrated with Electronic Message Systems

Word processing and electronic message systems overlaid or integrated with existing data processing and voice communications extend the multifunction capabilities of the line of .business processors offered by Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284. Based on the Attached Resource Computer[™] system architecture, these products form the core of the integrated electronic office, which will increase office productivity.

Capabilities available under the word processing system allow users to view text exactly as it will appear in print, including right justified margins. Standard formats may be stored and used or modified as needed. Users can easily change modes from the workstation to access data files for appending or inserting into text. Electronic message capability permits this text to be placed in message form and transmitted to its intended recipient.

Extending beyond the keyword index of other WP systems, the Associative Index Method (AIM) random association research and recall feature offers a universal search ensuring that any document can be located from limited information concerning the text. Any word, key phrase, partial word/or name can be entered and the system will search out all documents containing these factors and list the names of the documents containing them on the screen. The user can then electronically scan the text until the correct document is located.

Other features provide easy to learn commands to simplify editing, flexible format elements for page justification, line spacing, and tab settings. The ability to scroll stored text over the screen offers convenience in editing and correction.

The electronic message system operates with the same processors as the data and word processing systems. A 6600 series advanced business processor functions as the electronic network controller. This processor is dedicated to collection, routing, delivery, and costing of messages. Dedicated disc storage contains all information on message status and all undelivered messages.



Among the system's features are flexible priorities, encryption, verification of delivery, and acknowledgement of receipt options, full management and accounting reports, and the ability to transmit messages within a building, between buildings, and to remote sites. Control of this function is assured by priorities and verification features.

Increased security is provided through encryption and use of the AIM feature in addressing messages. Senders may enter a code within highly confidential messages that will ensure their encryption. These messages will be scrambled and transmitted through the system in encrypted form until decoded by the recipient. The AIM feature automatically appends mailstops to mail, ensuring that messages are not routed to incorrect parties.

Supplementing and enhancing these activities, the Long Distance Control System and Light Link provide the capability to transmit information beyond the constraints of the office. With the long distance control system, users can interleave voice and message traffic, providing a costeffective method of transmitting messages. Messages with destinations within a 2-mi range can be transmitted via the Light Link device. Circle 179 on Inquiry Card

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Oh, oh! See the red light? It means SCOUT^{*}does not feel good. That can sometimes happen with minicomputers.

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Multifunction Standalone And Cluster Systems Share Central Data Base

Office Mate, Mini ClusterTM, and Maxi ClusterTM systems incorporate a system architecture that allows standalone terminals, complete with processor software and disc storage, to connect to a large central data base having its own file management software. This combination was designed by XMARK Corp, 3176 Pullman St, Suite 119, Costa Mesa, CA 92626 to provide small business users with powerful, flexible word processing systems that can also handle many information management applications.

Priced in the \$9500 to \$14,500 range, standalone Office Mate systems contain an intelligent input terminal, 48k BAM, two built-in 5.25" doublesided, double-density floppy disc drives with 600k-byte capacity, high speed NEC Spinwriter printer, and software. Where more than one workstation is required, the Mini Cluster information processing system performs data and communication processing as well as word/text processing with a common file structure for word, data, and communication data bases. In a standard configuration, this unit is composed of master processor, an intelligent information storage module (IISM) that consists of the New World 2M-byte Winchester technology disc in combination with an 8" floppy disc, multifont printer, and up to four secondary processors.

Maxi Cluster, a shared resource hard disc system designed for multiple users, supports up to four 20Mbyte hard disc drives or two 96Mbyte drives and up to 32 terminals. This configuration can include a file controller and up to eight master processors, each supporting up to four secondary processors each having its own printer.

In two other configurations of this system, each master processor consists of a Mini Cluster with its own local memory storage. These systems operate as true shared resource systems with each processor functioning as an independent standalone drawing on its own processor and local memory while accessing the common data base of the hard disc system.

All systems are programmable in BASIC, FORTRAN, BTL, DEAR, and Pascal. Communications processing uses asynchronous, remote data base diagnostics, 2780/3780, UT200, and Burroughs and 3270 disciplines. Circle 180 on Inquiry Card

SLAVE COMPUTING: AN INNOVATIVE ALTERNATIVE TO MULTI-PROCESSING.

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Working in parallel with a master, up to four 4/10S computers can process all kinds of off-loaded tasks. Like communications protocol jobs. Process control work. Even complex calculations. All without slowing down the hosts' own processing chores.

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Slave I/O

CIRCLE 43 ON INQUIRY CARD

Midrange Minicomputer Offers Large System Capacity/Performance

Large system features of the midrange PDP-11/44 include 1M-byte memory, integral 8k-byte cache memory, microprocessor controlled programmer's console, and provision for optional floating point and commercial instruction set processors. Designed to fit between the top of the line -11/70 and the -11/34, the unit from Digital Equipment Corp, Maynard, MA 01754, provides twice the performance of the /34 at a price only 20% higher.



The general purpose minicomputer is available in standard system configurations and as a separate CPU. CPU features include a minimum 256k bytes of ECC MOS memory, two serial line units, microprocessor controlled ASCII interface, 8k-byte cache memory, and power supply. System configurations are made up of CPU, dual TU58 DECtape II drives, DECwriter III terminal, and choice of mass storage devices. Storage options include the 10M-byte RL02, 28M-byte RK07, and 67M-byte RM02 disc drives, and the 45-in/s, 1600-bit/in Ts11 tape subsystem.

Functional features of the system permit economical development of large database applications. The machine uses the full -11/70 instruction set, and extends capabilities of the midrange machine toward the top of the line. Reliability and maintainability features include a microprocessor controlled console with built-in diagnostics to promote fast, efficient troubleshooting, and an optional remote connection between the computer and a company operated diagnostic center.

Operating software encompasses RSX-11M, RSX-11M-PLUS, and version 7 of the multiuser, multitasking RSTS/E system. This version provides twice the performance of previous releases with features such as software disc cache, shared RMS, and expanded file handling capabilities. Bundled in are a multikeyed records management system and sort utility. Circle 181 on Inquiry Card

Dual-Channel Digitizer Samples at 200 MHz, Retains 8-Bit Accuracy

Dual-channel waveform digitizer model 7612D offers full programmability and incorporates GPIB compatibility to allow its use in either user designed or company supplied waveform processing systems. A proprietary digitizer within the unit, from Tektronix, Inc, PO Box 500, Beaverton, OR 97077, achieves a 200-MHz sampling rate while retaining 8-bit accuracy.

Providing an important performance improvement over single-channel instruments, the unit has two

COMPUTER DESIGN/FEBRUARY 1980

Data storage for militarized and hostile environments

20

The US Navy Standard Peripheral Magnetic Tape Unit is just one of our products.

In addition to the AN/USH-26, we build the Model 3400 with up to 17.2 megabytes tape cartridge storage capacity for hostile and militarized environments.

Our rugged Model 5100 tape cartridge storage system meets the requirements of MIL-E-16400 and MIL-T-21200.

All systems are supplied complete with formatters and interfaces to most computers.







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Division of North Atlantic Industries 60 Plant Avenue, Hauppauge, NY 11787 (516) 582-6060 TWX 510-227-9660

CIRCLE 45 ON INQUIRY CARD

Lear Siegler brings you the smart terminals designed for easy OEM customizing.

COMPUTER DESIGN/FEBRUARY 1980

At Lear Siegler, you don't have to decide among dozens of smart terminals, each offering something slightly different, each not quite right for you.

We have just two smart terminals for you to look at. But they can handle a range of tasks it takes other manufacturers four, five, or even six models to accomplish.

ize that some terminal manufacturers might say that two models aren't enough to

gualify as a complete line. But we like it that way.

After all, we want to make your life simpler, not more complicated.

THE ADM-31 & ADM-42 WILL LET YOU CHANGE THEIR MINDS.

When we designed the ADM-31 and ADM-42, we realized we couldn't second-quess our customers. Because no matter what capabilities we gave them, somebody out there might want something different. So we did the next best thing.

We gave each a truly flexible personality by putting the instruction sets inside their PROMS. So, unlike the hardware, the firmware is capable of easy OEM reprogramming, thanks to the fully-documented programming instruction manual we provide. And you end up with a terminal that performs to your exact specifications.

We even have a special **Application Engineering Staff** to answer any questions you may have about reprogramming. Consult with you on interfacing problems. Help you set the terminals' personality. Explain the features and functions. Talk about



Of course, we real PERSONALITY PROMS AND FACTORY ASSISTANCE MAKE USER-REPROGRAMMING A SNAP

special applications. Or even suggest something you maybe never thought of.

Feeling your life getting simpler yet?

THE ADM-31 & ADM-42. **ALL THE TERMINALS YOU'LL** EVER NEED.

Even if you decided not to reprogram their PROMS, our two terminals come with all the standard features you need in a smart terminal. And then some.

Features like full editing capabilities. Formatting. Reduced intensity for identification of protected fields. Blinking, blanking, and reverse video. High resolution monitors. Even limited line drawing capabilities.

What's more, both the ADM-31 and ADM-42 come equipped with a microprocessor, making them even more reliable and easy to use. Because their design architecture has a microprocessor with multiple microprocessor-based controllers that tie into the master.

Nor did we forget those indispensable function keys. Naturally, both the ADM-31 and ADM-42 have them.

On the ADM-42 for example. you get 16 function keys, shiftable to 32 functions, and optionally programmable to store up to 64 characters. This lets you store escape code func-

tions (such as personality modifications) to reduce several escape sequences to one key stroke. And you can store frequently-used phrases up to 64 characters, which provides you with

> impressive time savings. When you get right down to it, the ADM-31 and ADM-42 are really functions of your imagination.

THE CHOICE IS SIMPLE. THE CHOICE IS YOURS.

So the ball's in your court. Choosing your new smart terminal can go one of two ways. You could start sifting through dozens of data sheets, talking to dozens of salesmen, and looking at dozens of expensive, slightly different terminals.

Or you can look at two smart terminals from Lear Siegler the ADM-31 and ADM-42. Complete with user-reprogrammable personality, function keys, and an eager and willing Applications Engineering Staff to help you with any problems you may run into during the reprogramming.

The choice seems pretty easy to us. But if you want more information, call or write to us at Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, California 92803, (800) 854-3805. We'll be happy to tell you all about the ADM-31 and ADM-42.

And show you how you can make your terminals behave.



Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803. (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 968-0112. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (4867) 80666.

DIGITAL TECHNOLOGY REVIEW

channels with two independent time bases. Rather than the fixed format memory of other digitizers, each channel has a 2048-word memory that can be formatted as one 2048-, two 1024-, four 512-, or eight 256-word records. The ability to switch the sampling rate up to 13 times within each record provides time resolution appropriate to both fast changing and slower changing portions of the waveform without wasting memory space.

Heart of the digitizer is a CRT A-D converter for each channel. Inside the CRT, a rectangular electron beam is projected on an 8-column photodiode array that is laid out in Gray code format and provides beam deflection that is proportional to the analog input of the digitizer. Output



Tektronix' model 7612D dual-channel waveform digitizer provides independent time bases on two channels, and achieves 8-bit accuracy while offering sampling rates to 200 MHz



of the array is therefore an 8-bit Gray code representation of the analog input. This approach provides a significant improvement in digitizer speed and accuracy over past implementations.

Vertical accuracy of the digitizing process is specified by feeding a negligible distortion into the digitizer and comparing the digitized signal point to point with the results obtained by digitizing the same sine wave with an 8-bit digitizer. Overall accuracy achieved is greater than 7.8 bits at 300 kHz and over 6.0 bits at 20 MHz. On the horizontal axis, a crystal controlled sampling clock allows time interval measurement with accuracy approaching 0.001%. Ultimate accuracy depends on the nature of the waveform and the means used by the computer to interpolate waveform values between sample points.

Front panel selectable record length enables the user to divide each channel's memory into eight records or to concatenate channels A and B to achieve a 4096-word record. Regardless of record length, the time base sweep rate can be switched up to 13 times/s to most efficiently use storage capacity when digitizing complex records. Pretrigger mode of operation is selectable in integer multiples of eight samples from zero up to eight less than the number of samples in the first record segment. Posttrigger position is selectable in integer multiples of eight from zero to the record length.

A built-in GPIB interface ties the unit to waveform processing computers, waveform displays, and other GPIB instruments without additional hardware. Waveform data is transferred in binary block format over the GPIB to allow high speed data transfers. Values range from 0 to 377₈. In addition to the GPIB interface, the unit provides analog X, Y, and Z equivalents of stored waveform data to drive a refreshed display monitor.

SPS BASIC software facilitates configuration of waveform processing systems based on PDP-11 minicomputers. The unit is also available in wP 3000 signal processing systems consisting of 7612D, minicomputer or programmable calculator, peripherals, and software.

Circle 182 on Inquiry Card

SIEMENS

The Maxi-Mini-

Maximum storage capacity in minimum space. Siemens offers a 500K byte capacity in a compact drive half the size of a standard 8-inch. And our plug-toplug compatible Maxi-Mini disk drives are available for immediate delivery.

Siemens Maxi-Mini disk drives utilize Wangco technology which has been proven in over 20,000 installations. Available with either single or double head, these mini-disk drives also provide many other important features. Such as a true anti-crunch mechanism which prevents cover closure until the diskette is fully in place. This helps avoid data loss and provides a very real dollars and cents savings on disk replacement. There's also a wide mouth which permits easier, more convenient insertion of media, shortening load/unload time.

Also available from Siemens are single- and double-sided 8" floppy disk drives and mini-disk controllers. For immediate delivery of the Maxi-Mini or information about other OEM products from Siemens, contact us at:

Siemens Corporation

OEM DIVISION 1440 Allec Street Anaheim, CA (714) 991-9700 District Offices: Boston, MA (617) 444-6580 Iselin, NJ (201) 494-1000 Chicago, IL (312) 671-2810 Dallas, TX (817) 461-1673

The technology to do more.

CIRCLE 48 ON INQUIRY CARD





Big news from the printer giant.

Dataproducts introduces the 180 cps matrix printer with the features systems builders want.

A name you know you can trust.

We're the world's largest independent printer manufacturer.

(The giant, you might say.)

For 18 years, we've built printers for the biggest OEMs in the business—customers with some pretty tough standards. All our printers must be proven reliable before we can attach those big names to the cabinets. Our new M-120 matrix printer is now available with *our* name attached to the cabinet. Or with your name.

The M-120. Easy to recommend. Easy to own.

The M-120 is priced to be competitive with ordinary printers.

But this is no ordinary machine. This one prints as many as six copies at once. With crisp, easy-to-read print. In condensed, standard or expanded characters. It's designed for minimum cost of ownership. There's no preventive maintenance needed whatsoever.

Its unique removable head is good for 200 million characters at least. Then the operator simply replaces it. No service call is required.

Its long-life ribbons come in cassettes, so they're easy to load, clean to handle.

It has its own diagnostics with LED status display available. The operator can identify troublespots and often correct them in a snap, without waiting for a service representative. Downtime is less.

Fully compatible with our 340 cps printer.

For customers who need a faster printer, we offer our M-200 model.

It combines the economy of matrix printing with remarkable speed—340 characters per second.

Its 14-wire printhead lasts through a 300 million character life. Over two years of typical use. No one else has anything like it.

30 day delivery.

Often we can deliver a partial order even faster than that. If time is a problem, give us a call.

Available locally. And around the world.

Some people prefer to deal with our sales offices directly.

Others like the convenience of a distributor nearby.

We have more than 50 distribution points in the United States alone.

Call for information.

Call (213) 887-8451 to learn more about the M-120 or the M-200.

Or write to our marketing department at 6200 Canoga Avenue, Woodland Hills, California 91365.

P Dataproducts

CIRCLE 49 ON INQUIRY CARD



The first family of bubble memory systems. Non-volatile. Compact. Easy interface. From Texas Instruments.

TI's family of bubble memory systems offers you the non-volatility of magnetic storage media, plus compactness, silent operation, solidstate reliability, and lower error rates and faster access times than disk and cassette systems.

Because TI bubble memory systems are easily interfaced to microprocessor systems, many designers have already made their choice.

And, they've chosen from the TI family of bubble memory systems.

It's a design decision that makes sense. That's why you'll find TI bubble memory systems improving the performance of intelligent terminals, word processors, industrial process controls, instrumentation and telecommunications equipment, add-on buffer/cache memories and more.

Because bubble memories are so small and lightweight, they're ideally suited to portable applications such as small computers, data loggers and a variety of educational and home entertainment products.

And the innovations keep on coming. In product breadth. Technology. Production.

New bubble memory systems with storage capacities ranging from 23K to 768K bytes are being supplied. All the custom-designed peripheral and support circuitry for bubble memory systems are available.

New wafer processing techniques, including state-of-the-art planar construction — coupled with TI's innovative two-micron technology — are making newer and better things happen all the time.

TI's eight years of experience in bubble memory design and production have provided keen insights into customer requirements.

Requirements that demanded we deliver. And we have. In fact. TI has delivered more bits of bubble memory than all other suppliers combined.

Only Texas Instruments can offer you a full family of bubble memory systems. A family built on knowhow and experience. A family that reinforces TI's established position as the leader in bubble memory technology — and products.

Systems components

TI's complete family of bubble memory systems is comprised of component devices with capacities from 92K bits to 1 megabit. With access times from 4.0 to 11.2 ms.

These various capacities, along with the necessary support circuits, offer you a wide choice of compact systems for ease of use and design configuration flexibility.

The 1 megabit TIB1000, for example, is electrically and physically interchangeable with family members TIB0500 at 512K and the 256K TIB0250. Both are supported by the same comprehensive line of custom interface circuits.

The planar processing techniques, and new refinements in photolithography allow TIB1000 to offer the highest commercial bit density ever - by a factor of two.

Custom support circuits

All TI bubble memory systems con-

tain a complete set of interface and peripheral circuits — including two custom controllers. One for the 92K devices. One for the megabit family. So, it's not necessary to emulate controller function and you save a design step. Both are available.

These circuits, designed specifically for bubble memories, encompass state-of-the-art bipolar and MOS integrated circuit technologies. This provides high level interface between all of today's popular microprocessors and all of TI's bubble memory products.

The 92K TIB0203 is supported by its own family of custom peripheral circuits. The binary TIB0250, TIB0500 and TIB1000 are all supported by a common set of interface circuits.

TI'S FAMILY OF BUBBLE MEMORY SYSTEMS					
PART NUMBER	STORAGE CAPACITY	COMPONENTS	BOARD FORMAT		
TM990/210-1	23K Bytes	2 92K-bit	TM990		
TM990/210-2	46K Bytes	4 92K-bit	TM990		
TM990/210-3	69K Bytes	6 92K-bit	TM990		
TBB5005	64K Bytes	1 512K-bit	OEM Board		
TBB5010	128K Bytes	1 1024K-bit	OEM Board		
TM990/211-1	128K Bytes	1 1024K-bit	TM990		
TM990/211-2	256K Bytes	2 1024K-bit	TM990		
TM990/211-3	512K Bytes	4 1024K-bit	TM990		
TM990/211-4	768K Bytes	6 1024K-bit	TM990		

Custom support circuits for all families of devices include: coil drivers, sense amplifiers, function drivers, controllers and function timing generators.

An advanced family of support circuits, coming soon, has been designed for parallel operation as well as error correction.

Bubble memory systems

To provide ease of use and a convenient production board, each new member of TI's bubble memory family is available on a completely assembled, fully tested, compact printed circuit board.

TBB5005 and TBB5010 systems

Non-volatile bubble memory systems assembled on a 4" x 6" board with custom controller and all other peripheral devices and using the new family components. Features common to both systems include: up to 128K bytes of memory capacity, interface with TMS9900, 8080 and Z80 microprocessors, access times of 11.2 ms, data transfer rates of 85K bits/sec., system expansion capability and a choice of board connector styles.

TM990/210 system

Here's a non-volatile bubble memory system using the productionproven 92K bit TIB0203 device. Up to 69K bytes assembled on a single board, including a full complement of custom control circuits. Interfaces directly with TMS9900-based microcomputer modules. This system is in stock and available for immediate off-the-shelf delivery from your TI distributor.

TM990/211 system

A non-volatile bubble memory system utilizing the TIB1000 with up to 768K bytes capacity. Bus compatible with TM990/100 microcomputer modules, the TM990/211 system features 11.2 ms access time with data transfer rates of 85K bits/ sec. A new module, coming, will be able to be combined with the TM990/211 system to provide a megabyte bubble memory system with on-board error correction, direct memory access, and compatibility with TM990 file management.

And the innovations keep on coming

Texas Instruments is firmly committed to innovative, cost-effective bubble memory technology and product development.

So, for a full line of bubble memory systems - standard or customized to your application - turn to the leader - turn to Texas Instruments for magnetic bubble memory products.

For complete, detailed information and specifications,

send for a copy of our Fifty Years new 12-page brochure, CL-473. It's free. Write to Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.



TEXAS INSTRUMENTS INCORPORATED

DIGITAL TECHNOLOGY REVIEW

Typing Unit Produces Synthetic Speech To Verify Input Data

An audio typing unit produces synthetic speech with an unlimited vocabulary to help blind typists to independently produce error-free copy. Announced by the Office Products Div of the International Business Machines Corp, Parsons's Pond Dr, Franklin Lakes, NJ 07417, the unit attaches to any of four magnetic media typewriters, allowing the operator to review and proofread typed material by listening to information as it is stored on the magnetic media, and resulting in error free copy.

Using voice synthesis technology, the audio typing unit produces sounds that correspond to the keys that have been touched. These responses are created by combining a stored set of basic speech sounds (phonemes) according to preprogrammed pronunciation rules stored in memory. A voice synthesizer produces and blends the phoneme sounds to form continuous speech.

The unit consists of audio keypad, audio console, and optional headset, and attaches to IBM Mag Card II, /A, Memory, or Memory 100 typewriters. A typist uses the audio keypad, installed next to the typewriter, to activate audio responses that include pronunciation and spelling of individual characters, words, or lines of text. The unit also verbalizes punctuation and capitalization, provides audio prompts to guide in use of the typewriter, and gives audible indication of typing position on the page. Circle 183 on Inquiry Card

User Query Language And Report Writer Run on VAX-11/780

An English like query language for direct data access and a nonprocedural report definition language are

Non-returnable Capacitive Keyboards

Practically Speaking, that is!

When AMKEY ships a keyboard, it's likely that we'll never see it again. And that's because our products pass the most stringent and exacting quality controls. Our QC program assures durable characteristics in every keyboard we sell. For example, a 10Kv static charge won't disturb the strobing process. Steel top plate construction prevents warping under most conditions. To our customers, it all adds up to uninterrupted operation. Reliable Capacitive Keyboards — We've been delivering them for years.



both supplied by HARVEST. A product of International Data Base Systems, Inc, 2300 Walnut St, Suite 701, Philadelphia, PA 19103, the software runs on the DEC VAX-11/780.

The query language uses six commands (display, let, show, report, set, and exit) to define temporary variables, to do arithmetic calculations, and to provide automatic functions for total, maximum, minimum, and average values for a field or temporary field. Using the where command, the user designates the portion of the data base to be used to answer the query.

As HARVEST automatically finds the optimum access path to the needed records, the user need not know the database structure, but may treat the data base as a flat file with easily specified fields and retrieval conditions.

SEED, a CODASYL-type database manager, supports the report definition language. Page headings and footings, column and line labels, control breaks of up to 15 levels, automatical calculation of percentages of cumulative totals, and a choice of line printer or terminal directed output are included in the report writer. It can produce financial statements, inventories, patient charts, or student transcripts. Circle 184 on Inquiry Card

ANSI X3.9-1978 FORTRAN Runs on 990/10, /12 Minis

Designed around the recently approved ANSI FORTRAN version X3.9, 1978, DX10 FORTRAN-78 runs under the DX10 operating system. Developed by Texas Instruments Inc, Digital Systems Div, PO Box 1444, Houston, TX 77001, the language will run on models 4 through 30 of the DS990 computer family, and any system based on the 990/10 or 990/12 minicomputers.

The high level programming language allows natural expression of algebraic formulas and numerical problems. Scientific, industrial, engineering, and business applications are programmable in FORTRAN. DX-10 FORTRAN-78 includes process control extensions recommended by the Instrument Society of America, a mathematical/statistical library, plus interfaces to a generalized forms language, sort/merge, and database management. Circle 185 on Inquiry Card

OUR QUALITY COMES IN QUANTITY.

6789:1 <=

6789:1 <=> 789:1 (=)?@

3456789: 1 <=>?@ABCDEFGHIJ 3436789: 1 <->?@ABCDEFGHIJKI

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THEIR SIXTH COPY

Many printers can give you good print quality on a first copy. The real challenge is to give you that same quality, copy after copy, on multipart forms.

OUR SIXTH COPY

Obviously, most printers can't. The further they get from the first copy, the more their quality fades. But, as you can see here, the quality of Printronix' sixth copy continues sharp and clear.

This superior quality is achieved through a simple printing mechanism guite unlike any other. It forms characters by printing one dot row at a time, overlapping rows vertically and horizontally, while maintaining uniform hammer impact energy. The result is unequalled print quality and characters that appear solid. This same design approach also

requires fewer moving parts. eliminates most bearing surfaces, and employs simple hammer drive circuits. All of which means there's less to go wrong. And that's why Printronix can give you a full one-year warranty, not the 90-day warranty typical of most other printers. For more information on the

complete line of Printronix printers. call: (714) 549-7700. Or write:

> Printronix Inc.. 17421 Derian Ave., P.O. BOX 19559. Irvine, CA 92713.



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When you need a custom circuit, make sure it's you pulling the strings.

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As the industry matures and develops, design of custom proprietary circuits is moving out of the semiconductor houses and back to the user. It's created a tremendous demand for design talent that can only continue to outstrip the available talent pool. To learn how VLSI may impact you and your design team, send for our brochure, "The Future of VLSI."

And remember. To get ahead of the competition, take your C.O.T. to the company that made its mark in custom. Take it to Synertek. To control the design. To control the costs. With no one but you pulling the strings. Contact Custom Product Marketing direct at (408) 988-5671. TWX:910-338-0135.

Synertek performs as a major MOS supplier of high volume parts with advanced technologies and techniques behind everything we make. ROMs. Static RAMs. EPROMs. Custom circuits. Single-chip Microcomputers. Systems. 6500 Microprocessors and Peripherals.



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CIRCLE 24 ON INQUIRY CARD

Meet two new Printers from Anadex:

Resolutionary!



Both models employ a new, Anadex-manufactured 9-wire print head with 150 million character life (optionally, 650 million) that makes them ideal for high-resolution printing requirements including high-density graphics where print quality and reliability must go hand in hand.

The full standard 96 character ASCII character set, including descenders and underlining of all upper and lower case letters, can be printed bidirectionally on up to 5 crisp copies at speeds up to 200 CPS. Adjustable-width tractors, accommodating paper from 1.75 to 15.6 inches wide, allow the printers to adapt to your application. The three ASCII compatible interfaces (Parallel, RS-232-C, and Current Loop) are standard in every printer; so interfacing is usually a matter of "plug it in and print." With simplified interfacing, the printers also feature sophisticated communications capability including control of Vertical Spacing (6 or 8 lines/inch), Form Length and Width, Skip-Over Perforation, Auto Line Feed, and full point-to-point communications capability.

Other standard features are a 500 character FIFO buffer (optional, an additional 2048 character buffer), shortest distance sensing logic, self test, and replaceable ribbon cartridge with 6 million character life.

For complete details, attractive OEM pricing, and a demonstration, contact Anadex today.



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Here at Teltone, we make Dual-Tone Multi-Frequency (Touch Tone) decoders for the telephone industry. Since 1968, we've made hundreds of thousands of them. To exacting telephone standards. And you could use them to interface with 25 million existing Touch Tone telephones as potential data terminals. **So here's the deal:**

We have decoders in stock and we'll send you a sample. You hook it up, test it, bounce it off a wall, do whatever you need to do.

After you see how well it works, give us a shout and we'll give you a quote. In other words, you make us prove we've got both better quality and a better price. We plan to do both.



CIRCLE 52 ON INQUIRY CARD

DIGITAL TECHNOLOGY REVIEW

High Speed COBOL Compiler Automatically Segments Virtual Memory

COBOL-PLUS, a full ANS '74 standard COBOL compiler and runtime system, will run on any PDP-11 or LSI-11 with 56k-bytes of memory. The high speed compiler produced by S & H Computer Systems, Inc, 1027 17th Ave S, Nashville, TN 37212, runs under the RT-11 operating system or under TSX, a timesharing extension for RT-11 that allows up to 10 users.

Designed to run programs much larger than physical memory, the compiler allows automatic virtual



Whenever you need alphanumeric, dot matrix discharge printers—whether small and portable 12 column or 16 and 21 column work-horse varieties that can go over 100 million characters without trouble; or our largest 48 column, 144 character/second unit for larger printout capability—come to Hycom. With the smallest about \$50 and the largest about \$125 in 100 quantity, we're low priced too.

Evaluate one today; and do it easily with our Interface Board. We're brand X, but better.

Call or write: Hycom 16841 Armstrong Ave. Irvine, CA 92714 (714) 557-5252

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memory program segmentation by a least recently used technique that keeps the most active set of segments in memory. Runtime routines for OPEN-CLOSE, I/O, and ISAM are managed the same way.

Support of data types, including display and computational items, provide programming flexibility. Display items may have leading, separate, trailing separate, or trailing nonseparate signs and may be up to 18 digits long. Computational data items may be one, two, or four words long.

The compiler executes approximately four times faster than DIBOL-11 running under the CTS-300 operating system. Running the U.S. Steel COBOL benchmark program on an 11/34 gave a productivity index factor of 40 compared to 22 for the COBOL-11 running on the same machine. Circle 186 on Inquiry Card

Large Scale Memory Testers Formed From Common System Base

Compatible models within the series 6000 large scale memory tester line have been formed from a common system base to cover individual user needs as closely as possible. System control and pattern generation consist of a fully implemented microcomputer and ultrastable ECL microprogrammed pattern unit and check circuitry.

Intended primarily for testing large systems such as plug compatible memory units for IBM 360-xxx and 303X computers, the system, developed by Testmaster, 3191-D Airport Loop, Costa Mesa, CA 92626, is also applicable in burn-in memory testing. System features include 16M words of memory (up to 72 bits in length), 10-MHz max clock rate (20 MHz in interleaved mode), and 16-way interleave controller (20 MHz). Address and data bit control are front panel functions. Realtime error RAM automatically logs errors without reducing test throughput.

System peripherals can include a dual single- or double-density diskette operating system, that operates on Rs-232-C, TTY current loop, or parallel 8-bit 1/0 interfaces. Software support consists of disc operating system, assembler, editor, ROM based monitor, interpreter for test pattern generation, ROM based diagnostics, and disc handler routines. Optional are FORTBAN and BASIC languages. Circle 187 on Inquiry Card

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Online Control of a Laboratory Instrument By a Timesharing Computer

George Horner*

Xerox Research Centre of Canada Mississauga, Ontario, Canada

Data acquisition in a laboratory often necessitates the use of instruments that require repetitive operator intervention, often a tedious procedure. An example of such an instrument is a Zeiss microdensitometer—essentially an optical microscope with a built-in photomultiplier and a precision aperture. When examining a specimen, the instrument can select only a small portion of the viewing field for light intensity analysis. The microscope stage, therefore, must be moved in a predetermined pattern in X and Y directions—and a light intensity reading must be made at each point.

An initial attempt was made to automate the procedure by interfacing it to a dedicated Data General Nova 2 minicomputer with 2k memory. Since that computer system did not include a disc, it was cumbersome to operate and was used only as a controller for raw data acquisition. Subsequently, the data were transferred to a Nova 830 computer for offline processing.

It was then decided that the occasional use of the microdensitometer did not justify dedicating a computer to the control of this instrument. Therefore, a more flexible and less costly approach was chosen that added an intelligent controller to the original microdensitometer and ran the instrument on a timesharing basis under the control of a remote commercial computer through a standard serial communication port. Although this idea is not unique,¹ it was conceived independently at Xerox Research Centre of Canada. In addition, the resulting project was much smaller and custom tailored to the specific application.

System Design

As noted, the microdensitometer measures light transmission at various points of a material specimen in a series of repetitive moves. Under control of the timeshare computer (Fig 1), programmed commands cause the instrument's stage to move so as to bring a particular point of the sample into the measuring aperture. The instrument then measures the light intensity (or optical density) at that point and the value is transmitted to the computer. All commands are forwarded to the microdensitometer through the microprocessor based controller.

Essentially, this intelligent controller serves three functions. The first is to share or "switch" the serial line. Normally, this line connects an ASCII terminal to the computer. However, on command the controller disconnects the terminal and starts communicating with the computer. At the end of a series of measurements, the terminal is reconnected. This is one point where the approach differs from the procedure in Ref 1, where the microprocessor emulates a particular terminal with all its required features.

In its second function, the controller serves as a command decoder and data encoder. Because the computer link is a standard communications line (ASCII), it is advisable to encode all data and control transfers into 64 ASCII printable characters. That way the controller becomes completely transparent to the timesharing computer. Commands were encoded using all 128 ASCII characters since it was possible to transmit both control and lower case codes from the computer. However, the input into the computer was restricted to upper case only since the control codes would have been intercepted by the operating system.

The third controller function is to provide interface to the particular laboratory instrument. In this case, it generates appropriate pulses to the stage stepping motors and controls the 12-bit analog to digital (A-D) converter. That again differs radically from Ref 1, where the system could support many different instruments, with a variety of requirements, simultaneously.

*Currently with Sonotek Ltd, Mississauga, Ontario, Canada

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The combination of minicomputer power and directed syntax using soft keys means you spend less time memorizing syntax, referring to instruction manuals, doing routine searching and entering line-by-line program changes. The 64000 handles most of those routine tasks

917				
		LX1 D, DMSA	START OF DISPLAY MEMORY	
920		CALL READ	GET THE DATA	
921		MOV H, A	STORE THE UPPER BITS	
326		CALL READ	GET MORE DATA	
923		MOV L.A	STURE THE LOWER BITS	
924		DHU U	GENERATE THE REAL START HUDRESS	
925		CHLL READ	DUT IT DUDY	
926		THY H	NEXT LOCATION	
921		ING ENDE	SEE TE END ENCOUNTERED	
929		ORA A	SET THE FLAGS	
930		JZ WRTM1	JUMP IF NOT END	
			HN I THE REAL PROPERTY OF	12:1
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DIGITAL CONTROL AND AUTOMATION SYSTEMS



Fig 1 Block diagram of microdensitometer control system tied to timesharing computer. Controller disconnects terminal when computer is online and reconnects it other times

System Implementation

For this application, the controller is a Motorola Semiconductor MEK6800D2 microprocessor evaluation kit. Although that may seem like an overkill, in this instance it proved to be a very cost-effective solution because the kit provided all the system elements required for a single application. Those elements included working processor, read only memory (ROM), random access memory (RAM), serial input/output (I/O) for communication, and parallel I/O for interface. Additional benefits of the kit were keyboard and display for interfacing with the operator. Fig 2 shows the block diagram of the controller, and Fig 3 depicts assignment of PIA 2 (programmable interface adapter) I/O lines.

Microdensitometer stage motion control requirements call for $100 \cdot \mu s$ pulses spaced at 5 ms on one of four lines (+X, -X, +Y, -Y). When the stage finishes its motion the analog signal (0 to 5 V) corresponding to the light intensity at the given point has to be converted to 12-bit binary value. It was decided that for operator's convenience the converted value would be displayed in binary coded decimal (BCD) on the kit display. This was accomplished by writing a binary/BCD conversion routine and a 4-digit display routine. Fig 4 shows the encoding format for the stage motion commands and the 12-bit returned value.

Among the command codes the two redundant ones $(40_{16}, 60_{16})$ corresponding to -Y = 0, -X = 0 were used as special "switch" characters to disable and enable the terminal connection. Upon receiving these characters, the controller through PIA 2 line CA2 controls the gates of the line switching network (Figs 2 and 3).



Fig 2 Block diagram of controller. In addition to switch function (via asynchronous communications interface adapter), controller serves as command decoder and data encoder and interfaces to microdensitometer via programmable interface adapter

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As shown in the main program flowchart (Fig 5), the program was designed so that upon initialization the terminal communicates with the computer in the normal manner and the controller monitors the serial line waiting for the occurrence of the switch character. When that character is found, the controller switches into measurement mode; ie, it disconnects the terminal and proceeds further in the program. Once in the measurement mode the controller receives the stage motion command (one byte), executes it, and returns the reading (two bytes). Then it waits for the next command.

This loop continues until a special character (60_{16}) is received; execution is then stopped and the terminal is reconnected to the line. While in this loop, the echo from the timesharing computer must be disabled.

Since the microprocessor evaluation kit uses a multiplexed drive of the display and keyboard, the 4-digit display routine must run continuously.² Therefore, the receive section of the asynchronous communications interface adapter (ACIA) had to be operated in the interrupt mode. Interrupts are handled in two ways depending on the interpretation of the received character. If this character, when examined, does not result in a stage motion, the return from the interrupt is orderly, ie, via RTI instruction. On the other hand, if the stage is to move, there is no reason to return to the interrupted program. The execution becomes faster if it jumps straight into A-D conversion routine after the stage finished motion. In this case, the stack pointer has to be reset and the interrupt mask flag cleared. The entire program occupies less than 400 bytes and resides in a programmable read only memory (P/ROM).

It is important to note that this program was designed to suit a specific application (and a particular computer). Under different conditions it might have been advantageous to send a string of commands, execute them while storing the acquired readings in the controller's RAM, and transmit all the readings to the remote computer only after the execution. Such an arrangement utilizes the microcomputer capabilities to a greater extent and indicates the superiority of the programmable logic concept. This and other tradeoffs depend on many aspects of the particular application.

System Performance

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arant Hardware Company .

Two computers were studied in setting up the system. Originally considered was a Data General Nova 830, already available in a different laboratory of the research center. This system runs under RDOS with foreground and background. The controller was connected to a foreground serial port running at 4800 baud. Once the system was operating successfully, a Xerox Research timesharing computer that runs on XDS Σ 9 was tried. That machine, located in Webster, NY, was connected to the laboratory through an acoustic coupler and telephone line running at 300 baud.

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Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.



When testing the operation speed, it was decided to eliminate the effects of stage motion. Therefore, the test program was set up to read 1000 times at the same point. Based on this test, throughput of about 2 to 3 measured points/s was experienced when going to the timesharing computer. This slow speed is about 50 times faster than taking the measurements manually. The main limiting factor was the setup of the timesharing port. That resulted in swapping the tasks with extensive memory 1/0, because of the transaction oriented timesharing operating system structure. Therefore, single- and double-byte transactions were very inefficient. Using a dedicated serial port on the Nova 830 (running at 4800 baud), the throughput of 65 readings/s became execution limited. In real application this throughput would decrease, depending on the extent of the stage motion required.

A further point of interest is that after power-up, the operator has to enter the configuration pattern for ACIA. This allows the user to select the serial transmission format (seven or eight bits, number of stop bits, parity). The same approach could be used for selecting the proper communications protocol (number of bytes in and out, optional carriage returns, etc), thereby making the controller truly universal when talking to any computer systems.

Summary

In both described cases, system performance was satisfactory. Speed of measurement was orders of magnitude higher than when performed manually. At the same time, the measured values were directly available in the machine form. Replacement of the original Nova 2 resulted in capital and energy savings without performance degradation. The simple standard interface was an additional benefit of the design.

This approach appears to have adequate universal value to be used in various applications. Examples of such applications include calibration of nonlinear de-



For Low-Cost Winchester Data Storage, Using Your Existing Controller!

Now you can add Winchester disc drives to your systems using your present Storage Module Drive controller. PRIAM'S DISKOS 3350 provides capacities of 33, 66, and 154 megabytes, at costs far lower than other Winchester drives of comparable capacities. And you get the improved reliability, compact size, and environmental tolerance that only highlevel Winchester disc drive technology can provide.

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Compare the low cost-per-megabyte that PRIAM'S DISKOS 3350, 6650, and 15450 can bring to your system with the costs of drives using disc packs or cartridges and other Winchester drives. Compare PRIAM'S easy upgrade, through identical size, performance, and interface for all capacities. Compare the convenience and low cost of packaging PRIAM'S Winchester disc drives in the computer cabinet instead of in a separate cabinet. Consider the important economy and time saved in extending the life of your SMD controller to another, new generation of disc drive systems.

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PRIAM'S DISKOS Winchester disc drives use IBM 3350-level technology for efficient, reliable data recording. Fully servoed linear voice coil head positioning assures high data density and increased future capacity. A brushless DC motor reduces size, cost, and mechanical complexity. Small size, only 7" x 17" x 20", including optional power supply, fits the DISKOS family to almost any enclosure.

For a brief and handy history of Winchester technology and its advantages, call or write to PRIAM and ask for a copy of WHO'S SELLING RIFLES TO THE INDIANS? A Winchester Disc Drive Technology Primer. It's FREE!



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Find out today how quick and easy it can be to move up to this generation's disc storage. Send for PRIAM'S DISKOS 3350 specifications and more information about how to make the SMD CONNECTION! Call or write to



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A process-control engineer wants a highspeed, low-cost computer to monitor and control a factory operation. He checks out the Supercomponent[®] specs and moves on to the next project. This job's done.

A systems engineer is designing a blood analyzer on a really tight schedule. He needs a digital controller to record, analyze, compare, file and retrieve data. He reviews the Supercomponent technical manual, then moves on. The job's done.

A systems designer wants to control a radar telemetry system. There are special software considerations, and real-time data is needed. (Last year, a design just like it took him six months.) He spends a couple days with Supercomponent specifications and moves on. The job's done.

Here come the Supercomponents!

Advanced Micro Devices announces a family of LSI-intensive boards built to save the serious systems designer a whole lot of time and money. Supercomponents are changing the make-or-buy rules. Here's why:

They're absolutely state of the art. They are designed-in like components and they think like VLSI. They save you a ton of interface design time. They're plug-in ready. All are iSBC80* compatible and have a Multibus*. And, of course, we have all the enclosures and power supplies and card cages and back planes and software you need to cut your costs and accelerate your project.

Now for the big reason: Supercomponents are better because the parts are better. They're made from the finest, freshest, most advanced LSI in the business.

You picked a terrific time to be in this business. Supercomponents are here.

The Am95/4005.

Our single-board computer, The Monoboard,[™] is very powerful. It has all the features

others in its class have, but—over and above —it includes a sophisticated arithmetic processor, four DMA channels and speeds up to 3 megahertz!

The Am95/6110.

Our floppy disk controller has its own built-in intelligence. It has its own Am8085A CPU plus a high-speed buffer and its own PROM-based firmware. A DMA is included. There's much more. You'll have to read the full specs to believe it.

The Am95/1128.

128K bytes of RAM on a board <u>plus</u> parity with its own built-in refresh. The RAM can be dual-ported. Smaller capacities can be achieved by depopulating the board. The Am95/1128 has twice the capacity of its nearest competitor.

These are just a few members of our Supercomponent family. Call or write us for the facts on all of them.

*iSBC and Multibus are trademarks of Intel Corp.





Fig 5 Main program flowchart. Terminal is online until receipt of switch character by controller, which then switches microdensitometer into measurement mode to receive stage motion command. When special character is received, controller reconnects terminal to line

vices, measurement of frequency/phase response of linear systems, tabulation and plotting of parameters of multivariable systems, or any measurements where a response to a stimulus is investigated.

Advantages of using a timesharing computer lie in its high level processing capabilities. That is, complex algorithms and statistical routines may be applied to the acquired data and, if desired, a "feedforward scanning technique"** can be realized.

The procedure is transparent to the remote computer, it is simple and inexpensive to install, and it allows large volume data acquisition straight into the large computer with subsequent on- or offline processing. The concept can be easily adapted to a variety of laboratory instruments. In many cases where there is no onsite computer and the occasional need for measurements does not justify the installation of one, this approach could provide an attractive solution.

**Feedforward scanning is the technique whereby the previously measured values are used to determine the future X, Y scanning trajectory. Disadvantages are occasional slow response (this is not realtime processing), slow communication (serial line at low baud rates), and vulnerability of communication connection, since it uses common carriers. In this specific application, as well as many others, these factors are of no importance—making this method of computer control perfectly feasible.

Acknowledgement

The idea of this project was originated by Mr Larry Marks who also wrote the 1/0 driver routines for the timesharing computers and carried out the mechanical construction of the system.

References

- 1. S. G. Zaky and K. E. Torku, "A Microprocessor System for Data Acquisition and Control of Experiments Using Interactive, Time-Sharing Service," *IECI '77 Proceedings on Industrial Applications of Microprocessors*, The Institute of Electrical and Electronic Engineers, pp 137-141
- 2. MEK 6800D2 Evaluation Kit II Manual, Motorola Semiconductor Products, Inc, Phoenix, Ariz, 1977

308 DATA ANALYZER

Easily acquire the data you need.

Select parallel state, parallel timing, serial, or signature operation. Simply press the appropriate key.

Choose synchronous or asynchronous sampling. Use the clock of the system under test or the 308's own internal clock. In either case, sampling rates up to 20 MHz are possible.

1. 2. 3

Enter the word you want to use as a trigger to acquire data. Other keys let you select an external trigger and trigger delay.

Press "start" and you're done. Now, you can view the acquired data in the format you want. Or, store the data in the reference memory by pressing the "store" key. Other function keys allow you to acquire new data and compare it with the reference memory.

PRL STATE DATAD-0A EXT 0=X	(HEX) SMPL POST POS DLYW-6000 SMPL- 245
HE WORK	76543210 OCT 00101000 050 00101001 051 00101011 053 00101100 054
HALL ON	00101101 055 00101111 057 00110000 060 00110010 062
334 34 36 37	00110011 063 00110100 064 00110110 066 00110111 067
And the second second	

In each data acquisition mode, all measurement parameters are displayed for your convenience.

Minimum keystroking with the new 308 Data Analyzer from Tektronix. Of course, the 308 Data Analyzer can do a lot more than we've shown here. For example, there's a self-test routine at power-up, plus seven diagnostics, to ensure accurate results. And the 308 weighs only 8 pounds (3.6 kg), for easy portability.

For the full story, contact your local Tektronix Field Office, or write us.

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Manufacturing Control System Monitors and Expedites Operations

Activity and status levels of semiconductor circuit manufacturing operations at the Fullerton, Calif plant of Hughes Aircraft Co are to be monitored by the first production control system delivered by Digital Datacom, Inc, 17951 Skypark Circle, Irvine, cA 92714. In this or other production operations, the system can function either as a standalone device or as a terminal subsystem in a distributed network to track, control, and measure the movement of work in near real time.

Components of a system include controller, CRT terminal/console, 132-col serial printer, from 1 to 30 card/badge readers, and applications programs. The controller, a 232-2 data station, consists of a microprocessor, 4k RAM buffer, and two 3M DCD-1 cartridge transports. A standard module generates man/machine readable tab card job travelers that accompany the product being manufactured through the production area. These travelers are marked by production or quality control personnel with a pencil and then inserted into one of the mark sense card/badge readers distributed throughout the manufacturing operation to collect data such as part numbers, serial numbers, employee numbers, operation numbers, and failure codes. Transaction date and time are recorded to the nearest minute. Each cartridge can store 9600 transactions.

System commands, entered through the terminal, are carried out by the controller. Operator actions are prompted through a menu of steps to generate data on the job travelers, to design report forms, and to summarize collected data. Circle 450 on Inquiry Card

NOW YOU CAN AFFORD TO IMPROVE YOUR IMAGE.



BLACK AND WHITE MODEL 3400



COLOR MODEL 3450



Production control system monitoring position. Menu prompts operator through required procedures to maintain near realtime knowledge of manufacturing activities. As many as 30 card/badge readers can be located at individual work stations throughout plant. Production personnel mark job travelers and insert them into readers to supply job status data

We've made raster technology affordable. So OEM systems designers can finally buy flicker-free graphic display terminals with high resolution and rapid response once available only on customdesigned systems.

CLEARLY A CASE OF BLACK AND WHITE.

The microprocessor-based Genisco 3400 generates a full-screen raster, black and white pattern with 768 horizontal lines and 1024 pixel locations along each line.

This ultra-high, full-bit-mapped screen density practically eliminates distortion and stair-stepping. And makes it possible to selectively change picture elements in a fraction of a second.

A NEW KIND OF COLOR GRAPHICS.

The Genisco 3450 is the first reasonably priced graphics terminal with precise color control at each pixel location. That's a resolution with 384 lines and 512 addressable pixel locations.

With 3450 you get diagrams in up to

8 colors while enjoying fast response, selective erase, a 60 frame per second refresh rate and most features found in more expensive systems.

Both the Genisco 3400 and 3450 represent an economic breakthrough for systems designers. They provide the latest technology with a new low price tag.

It never can hurt to improve your image.

better image through I	better graphics.
lame	Title
Company	Division
treet	Telephone
City/State	Zip
Genisco is a Division of (7805 Sky Park Circle 714) 556-4916 TWX 91	Genisco Technology Corp. Dr., Irvine, CA 92714 10-595-2564

THE PERFECT PICTURE PEOPLE.



The new 3220 from Perkin-Elmer. A 32-bit supermini so fast, so powerful, so advanced, it may not be for everyone.

Here are 5 ways to tell if it's for you.

1. You need 32-bit hardware and software performance: Your transaction processing system requires instantaneous terminal response. Your real-time control system must offer very high throughput. Your scientific programs must run incredibly fast and yield exceptionally accurate results.

2. You need help to develop programs quickly and easily: You need one language – COBOL – for all business applications, whether batch or transaction processing. You require multiple high-level languages. The faster you can identify programming errors, the faster you can correct them – so you really appreciate the value of our globally optimizing FORTRAN VII. It has a separate development compiler that produces object modules at a speed of 2,000 lines per minute. And with our Multi-Terminal Monitor, you can have 32 programmers working simultaneously with COBOL, FORTRAN, CAL MACRO, or RPG II.

3. You need a system with unmatched integrity: Your commercial data base needs to be fully safeguarded from media faults and system failures. Your scientific results require single- and double-precision floating point accuracy. And your time-critical, memory-resident programs for real-time control applications need the protection of our dynamic memory relocation and protect hardware.

4. You need 32-bit performance at 16-bit prices: The Perkin-Elmer Model 3220 starts at \$33,500 (U.S. only). And our OEM terms and conditions are *unmatched* in the industry.

5. You need a vendor that stands behind its products: Perkin-Elmer maintains a worldwide field service operation and offers a variety of support program contracts. We offer comprehensive hardware and software training courses. And we pride ourselves on responsive systems and software support.

The Perkin-Elmer Model 3220. It may not be for everyone. But if even one of these points touched a nerve, you should find out more about this remarkable supermini. Send the coupon for a fact file. Or call toll free 800-631-2154. In New Jersey: (201) 229-6800.

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Title			
Company			
Street			
City	State	Zip	CD2

PERKIN-ELMER





Data Warehouse. When Floppies aren't enough. But you can't live without them.

There comes a time when your system outgrows flexible disk drives.

You need more storage capacity and higher throughput. But you don't want to give up the input/output convenience of floppies.

The Remex Data Warehouse storage system just solved this dilemma. It gives your system 20MB Winchester capacity, reliability and speed. Plus, it gives you the flexibility of floppies.

And Remex put it all together in one selfcontained package under the common command of an advanced controller/formatter.

THE BRAINS BEHIND THE DATA WAREHOUSE.

The most complex and time-consuming task in building your own disk subsystem is designing the controller. We've done it for you.

Our very intelligent, microprocessor-based controller gets you to market quickly, with "capabilities previously associated only with large disk-oriented systems," to quote *Computer Design* magazine.

In fact, our built-in controller is so powerful that it increases throughput by 40% or more over existing systems.

Normally about half of I/O overhead is between CPU and disk. We've cut these communications to a bare minimum with techniques such as DMA (direct memory

access) of commands and status, as well as data.

PACKET POWER SUPER-CHARGES YOUR SYSTEM.

Whenever data is transferred to or from the disk, the controller retrieves



packets containing all command data via DMA. The starting memory address of these packets is stored in the programmed I/O portion of the CPU. And that's all the CPU needs to instruct the controller to retrieve data, perform functions, transfer data and communicate status of that function to the CPU. When the function is complete, the controller returns the starting memory address of the packet to the CPU.

With DMA, multiple sector transfers of up to 64K words are accomplished with a single command.

The Data Warehouse also copies "off-line" so that updated or newly-created files can be safely stored outside the system.

Simply, the Data Warehouse distributes intelligence to the disk and frees your CPU for computing.

AVAILABLE NOW. SO YOU DON'T HAVE TO LIVE WITHOUT IT.

The Data Warehouse is built for 19" rack mounting and includes its own power supply. Only one CPU slot is needed for interfacing. And a variety of interface cards for minicomputers and microprocessors are available.

Best of all, Data Warehouse is available today in OEM quantities. Write Remex Division, Ex-Cell-O Corporation, 1733 East Alton Avenue, P.O. Box C19533, Irvine, CA 92713. Or call (714) 957-0039.

Ex-Cell-O Corporation REMEX DIVISION DATA WAREHOUSE

CIRCLE 70 ON INQUIRY CARD

RASTER DISPLAY SYSTEM DESIGN NOTE 1.

How to display a 1280 x 1024 image that doesn't flicker





System 3400's fast rise time and minimal ringing yield sharp, uniform pixels at 60 Hz refresh.

Competitive systems typically must run slower to minimize slow rise time and ringing problems.

Do it with the Lexidata System 3400 image and graphics processor.

If you're designing highresolution raster scan video display systems, only Lexidata can give you a 1280 x 1024 picture that doesn't flicker.

The high-speed, microprocessor-controlled System 3400 is unique among video processors in its ability to generate a pixel in only nine nanoseconds. This means you get a refresh rate that's at least twice as fast as other processors on the market. And your happy system users get none of the eye fatigue common with conventional systems.

But a display that doesn't flicker is just one of the ways the System 3400 can help improve your image. Its extensive line-drawing and tonal imaging capabilities make it a perfect fit in a wide range of color, gray-scale and monochrome display applications. So, whether you're designing a specialized system for medical imaging, or mass producing systems for a variety of CAD/CAM applications, the 3400's repertoire of over three dozen standard and optional features can give you the ideal mix of hardware and software tools to handle the job. And at a price you're sure to like.

Send For New Detailed System Description

To find out more about the System 3400, send for a copy of our new 12-page system description booklet. Or, if you need information immediately, call us at (617) 273-2700.



DIGITAL CONTROL AND AUTOMATION SYSTEMS

Onboard Computer Provides Multifunction Service for Automobile Driver



Onboard computer for automobiles. Joint BMW/Siemens AG development mounts on dashboard. It has 12 keys for inputting commands, digital display to output information, and both audible and visual alarms

An automotive computer that looks somewhat like a pocket calculator but mounts on the dashboard to the right of the steering wheel is currently in the test stage of development. Commands are entered through 12 keys. As with other similar computers (*Computer Design*, June 1979, pp 74-79), several functions are served.

Normally the display shows time of day; however, pressing key 1 calls for a reading of outside temperature for 8 s. If the outside temperature goes below 3 °C (37 °F), an audible alarm sounds and a red LED is illuminated to warn the driver to watch for slippery roads.

The computer stores distances up to 999 km and on command will display the remaining distance to destination or the estimated time of arrival (based on current average speed). Other commands will display current fuel consumption, average speed, and how many miles the car can travel on the remaining fuel supply. Fast drivers can enter the posted speed limit and both audible and visual alarms will activate if the speed limit is exceeded. These drivers can also enter the distance from a turnoff—as noted on a highway sign—and the computer alarms will notify them before the turnoff is reached.

A command can be entered to start the heater at a specified time. Still another can be used to enter an arbitrary 4-digit code that protects against unauthorized use of the vehicle. If the wrong code is entered three consecutive times, the computer sounds the horn.

Being developed jointly by BMW and Siemens AG of the Federal Republic of Germany, this product is not yet commercially available. It is intended for overseas applications and will not be marketed in the U.S.

CIRCLE 71 ON INQUIRY CARD

"Frankly, IDC connectors used to be a pain in the neck."

"My problems were monstrous.

When I could find the connectors I needed, I would have to go digging around for the cable. If the price was right, the products weren't. And on and on, eon after eon.

Until one day my doctor suggested Spectra-Strip.

Of course! They've been making flat cable longer than anybody, so they would have to know how to make ends meet!

They do, and now I get all my IDC receptacles, headers, DIP plugs and sockets, PCB transitions and card-edge connectors from a single, reliable source: Spectra-Strip.

When things get really busy at the lab, I even have them or one of their value-added distributors provide completely terminated and tested jumpers and custom assemblies.

Their products are just what the doctor ordered, their Q.C. has real teeth in it. and their prices never put the bite on my budget.

For the name and number of your nearest distributor or rep, write Spectra-Strip, 7100 Lampson Avenue, Garden Grove, CA 92642, telephone (714) 892-3361. In the East, call (203) 281-3200.

And tell them Frank sent you."



When you're down to the wire.

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See us at booth 907 at NEPCON WEST.

DIGITAL CONTROL AND **AUTOMATION SYSTEMS**

DC&AS BRIEFS

Servo Drives Engineered for Machine Tool Applications

The Hyamp III line of 3-phase half-wave, bidirectional SCR servo drives has been expanded by Hyper-Loop Inc, 7459 W 79th St, Bridgeview, IL 60455, to include models with armature supply voltage and current ratings of 40, 60, and 90 A continuous for 90-, 120-, or 15-V motors. In machine tool applications, the drives satisfy requirements for closed velocity and position loop applications; they also can be used in special purpose machine systems such as welding, metal forming, or transfer lines. Package size is 14 x 9.625 x 6.75" (35.6 x 24.45 x 17.15 cm). Hinged circuit boards allow access to SCRs and test points aid troubleshooting. The drives operate motors from 0.1 to 15 hp. Optional linear acceleration and deceleration ramps help extend motor and machine life. Other options include fault detector output signals for phase loss, power supply loss, tachometer loss, and over-speed and over-temperature monitors.

Circle 451 on Inquiry Card

Up to 100 Transducer Measurements Monitored by Microprocessor Based System

Temperature, humidity, solar radiation, pressure, and flow as well as other variables measurable by transducers can be monitored from data collected by the CSD-936 monitoring and alarm system. Hy-Cal Engineering, 12105 Los Nietos Rd, Santa Fe Springs, CA 90670, says that the microprocessor controlled and firmware programmed systems allow the user to determine sequencing, data storage and presentation, printing format, and alarm limits. Limits can be set or data entered through keyboard, thumbwheel switch, or toggle switches. Depending on input sensor types, as many as 100 inputs can be scanned. A 3-digit channel indicator advances as input channels are scanned.

A math option permits data to be operated on as variables in equations selected by the operator; an RS-232-C serial output allows the system to communicate with computers for data accumulation and with printers for data formatting. Battery backup retains data in up to 4k words of memory for 10 days if power is turned off. A realtime crystal controlled clock has a 6-digit readout for hours, minutes, or seconds.

Circle 452 on Inquiry Card

ADC Mounts Up to 250 ft From Computer For Remote Data Acquisition

RAD1, a high speed, high performance analog to digital converter intended for use with the company's RIM line of remote instrumentation modules, has been introduced by Precision Data Systems, 2030 N Forbes, Tucson, AZ 85705. Designed for realtime computer controlled remote data acquisition and control applications with either mini or microcomputers, this A-D converter module receives all control signals, data, and power from a single cable at up to 250 ft (76 m) from the computer. At reduced rates it can operate at a distance of 3300 ft (1 km) with up to 16 modules daisy chained to a single line.

Resolution is 12 and 14 bit, and linearity is $\pm 1/2$ LSB. A 16-bit quantization D-A converter section (in model .A1 but not in .A2) of the module can be used as a 14-bit output for calibration or general use or to increase accuracy and resolution of the analog input channels. Specifications include 20-µs conversion time, 5-µs transfer interval, 10-µs channel change time, 6µs acquisition time, and 4-MHz transmission rate. A MUX1 multiplexer external accessory box permits up to 64 channels with switched gain to be accessed; an RTD1 resistance temperature converter permits one of the four analog input channels to be used for precision temperature measurements.

Circle 453 on Inquiry Card

DAC Outputs Provide Direct Drive of **Process Control Actuators**

The 8-bit DAC1420 and the 10-bit DAC1422, said to be the industry's first such devices to be powered entirely from the loop supply voltage over the 10- to 36-V range, feature 4- to 20-mA outputs to drive process control actuators. Accuracies are $\pm 0.2\%$ and $\pm 0.05\%$, respectively, with both guaranteed to be monotonic over their full 0 to 70 °C op temp range. Introduced by Analog Devices, Inc, PO Box 280, Norwood, MA 02062, these devices will also supply a 5-V output to power external CMOS circuitry, a voltage reference output, and span and offset adjustability of $\pm 10\%$. If computer power fails, each DAC will hold the last data word in its latches. Specs include integral and differential linearity of $\pm 1/2$ LSB, and offset and span tempcos of 25 and 50 ppm/°C, respectively. Package sizes are $2 \ge 2 \ge 0.4''$ ($5 \ge 5 \ge 1$ cm).

Circle 454 on Inquiry Card

Portable Data Acquisition System Functions in Severe Environments

A portable microcomputer for mobile or remote data acquisition applications in severe field or industrial environments has been introduced by Applied Systems Corp, 26401 Harper Ave, St Clair Shores, MI 48081. The 8085 microprocessor based unit contains plug-in cards for CPU, memory modules, analog and digital I/O, and optional data displays as well as space for an operator's control panel and ac or dc power supplies. A standard data display can contain from 16 to 40 alphanumeric characters; custom options allow up to 240 characters to be displayed. Modules are available for multiple ADCs and DACs, high or low level analog multiplexers, and communications interfaces. Available units operate on 120 Vac, 12/24 Vdc, or battery power supply. **Circle 455 on Inquiry Card**

Solid State Sequencer Replaces Electromechanical Components in Process Control Systems

Intended to interface directly with microprocessor based process controllers, the model 42S programmable sequencer replaces cam timers, stepping relays, drum programmers, and tape readers. The all solid state unit, offered by Electronic Services, Inc, 16 E Franklin St, Danbury, CT 06810, has 21 to 42 output channels with up to 4096 completely reprogrammable steps (via keyboard). An Rs-232-C connection for a computer or cassette deck is available as an option for remote program loading.

Circle 456 on Inquiry Card

Industrial Control Computer Built from Replaceable Function Cards

By choosing the specific cards required from among a number of available choices, a designer can build a microcomputer that exactly meets his needs. Users of the industrial microcomputer system, made by N V Philips' Gloeilampenfabrieken, Elcoma Div, PO Box 523, 5600 AM Eindhoven, the Netherlands, can select a CPU card with 1k RAM and 4k EPROM; 8k- or 16k-byte P/ROM card; 4k- or 8k-byte RAM card; input and output cards with two 8-bit ports each; teleprinter card with Rs-232 interface, current loop with optocoupler, and audio cassette interface; debug and display cards; and MODEST software development cards. The cards mount in a standard 19" (48-cm) Eurocard rack and connect through a common back panel that operates as an asynchronous system bus.

Circle 457 on Inquiry Card

Speech Synthesizer Enables Verbal Instructions For Industrial Applications

Basic technology used in the company's Speak & SpellTM talking learning aid and the Language Translator have now been applied to industrial and commercial operations. The TM990/306 speech synthesizer module from Texas Instruments Inc, PO Box 1443, MS-6404, Houston, TX 77001, offers an opportunity to provide verbal instructions or signals where indicator lights or audible alarms are now being used, such as in learning aids to prompt trainees or to alert operators for maintenance procedures.

Sentences—having human but relatively flat inflection —can be constructed from a 160-word industrial vocabulary. Numbers from 0 to 12 and the full alphabet are also included, and by combining certain letters and words the basic vocabulary can be expanded. (N can be combined with "crease" to produce "increase"; D can be added to "crease" to make "decrease"; and B, R, N, C, and Y can be used for "be," "are," "in," "see," and "why.")

The plug-in board speech synthesizer module is fully compatible with other TM990 microcomputer modules. An onboard amplifier can drive an $8-\Omega$ speaker with a 2.5-W output, but more output power can be provided by connecting an external amplifier to the module's preamplifier output.

Circle 458 on Inquiry Card

Laboratory Automation System Processes Throughputs up to 125 kHz

A family of four factory configured and one user configurable analog I/O systems for laboratory automation, LAB-DATAX models are microprocessor based instrumentation packages. Each contains an LSI-11/2 CPU, 64k bytes of RAM, and instruction sets for both fixed and floating point arithmetic. All operate under the DEC RT-11 realtime operating system in FORTRAN IV. A standard Q-bus compatible backplane enables full use of all LSI-11/2 Q-bus compatible peripherals. Available from Data Translation Inc, 4 Strathmore Rd, Natick, MA 01762, each unit is contained in a 5.25 x 19 x 21" (13.3 x 48 x 53-cm) rackmountable enclosure containing a multiple-output power supply rated 5 V at 25 A and 12 V at 3 A, a cooling fan, and an internal card cage that holds up to 16 dual-height, single-board analog I/O systems. DT4021 and 4023 include 16 digital inputs, 16 digital outputs, and 21 control lines; 4022 and 4024 include 32 each digital inputs and outputs. The high throughput model, DT4023, processes 125-kHz, 12-bit ADC words.

Circle 459 on Inquiry Card





IECI '80

Sheraton Philadelphia Hotel Philadelphia, Pennsylvania March 18-20



Paul M. Russo General Chairman



David L. House Keynote Speaker



J. David Irwin Technical Program Chairman

The Spring Conference and Exhibit on Industrial, Control, and Instrumentation Applications Of Mini and Microcomputers will be sponsored by the IEEE Industrial Electronics and Control Instrumentation Society. Under the direction of technical program chairman J. David Irwin, professor at Auburn University, 16 program sessions will present topics ranging from process control and interfacing instrumentation to energy monitoring and testing systems. The conference, under the general chairmanship of Paul M. Russo, RCA Laboratories, will include two evening panel sessions, one Tuesday and one Wednesday evening, plus two all-day tutorials to be conducted the day before the conference, Monday, March 17. The keynote address will be delivered Wednesday, March 19, by David L. House. Mr House, operations manager at Intel Corp, Microcomputer Components Div, will speak on trends in microcomputers.

The first session of the conference, Tuesday morning, March 18, will advance several specific uses of mini and microcomputers in process control. A controller for a lumber kiln, chemical reactor control, and improvement of process control measurement accuracy are the microcomputer uses to be presented. Also to be discussed are software design of a minicomputer based transducer calibration system and an intelligent sugar crystallization controller. System design aids and techniques to be examined at another Tuesday morning session will include a Petrie net based industrial sequencer, design automation of microprocessor based control systems for industrial sequential processors, a higher level language to simplify programming of microcomputer control systems, challenges in design aids for microprocessor systems, and using minicomputers to solve decision making problems in interactive design. The third Tuesday morning presentation will feature aspects of motor control. The papers will include the use of microprocessors in electrical variable speed drives, performance improvement of microprocessor based digital PLL speed control systems, microprocessor controllers for a modified thyristor converter, and microprocessor control of a 3-phase inverter.

Process Control II, the first of the three Tuesday afternoon sessions, will expand the process control coverage. Paper topics will include a microprocessor based high level programmable controller, an inexpensive modular process control computer, a universal process control interface, and a microprocessor based adaptive control system. Power converters are the subject of the second session slated for Tuesday afternoon. Microprocessors figure in three of the papers: control of thyristor converters, a minimum time settling control scheme for line computated converter output, and a multimicroprocessor

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system to measure speed and control motors. Also to be presented are a microcomputer based continuous output PWM inverters controller, and the analysis, design, and test results of realtime digital controllers. Programmable battery test cyclers, a dynamic monitoring system for motor bearings, a microprocessor based controller for an IC wafer prober, and an alignment and test system for TV remotes are among the intelligent testing systems to be reviewed in the final Tuesday afternoon session.

Wednesday morning finds sessions covering management, distributed systems, and power applications on the agenda. The management papers will offer a corporate approach to software, a method emphasizing productivity to develop software, and a paper contrasting micros with other computers. A decentralized computing system based digital blending system, a microprocessor based parallel processing system for the relaying of power transmission lines, and a supervisory control and monitoring system for water and sewage treatment works will be explored during the session focusing on control applications of distributed systems. Power applications to be discussed will include a microprocessor based system to control a low head hydroelectric generation facility, and a microcomputer based control system for power system simulation at the Hydro-Quebec Institute of Research. Other applications to be presented will include a high voltage power system monitoring interface, microprocessor based control of a photovoltaic solar power system for an am radio station, and DIMS for EHV substation control hardware and software design efficiency.

Automated manufacturing, energy monitoring system, and interfacing instrumentation are the subjects scheduled for discussion during Wednesday afternoon sessions. Microprocessor aids to be presented during the automated manufacturing session will include control for an automated low loss optical fiber connector termination machine, control of a steel punching machine, and modifications to a LeBlond precision lathe to improve safety of machining high explosives. Also discussed will be use of microcomputers in mining process control and an automatic optical axes manipulating system for optical fiber communication devices. Engineering monitoring systems will report on functional partitioning in distributed processing energy control systems, as well as two uses of micros in energy monitoring systems to augment solar systems. One of the latter is a microcomputer based, 2-axis tracking collector for a concentration solar collector; the other details use of microprocessors for solar circuit control. Papers to be presented during the interfacing instrumentation session will discuss a portable self-contained wind generator statistical analyzer, a microprocessor based flux wire evaluation and analysis system, intelligent data acquisition instrumentation for nuclear material assay data analysis, and a universal approach in asynchronous serial interfacing.

Several facets of data acquisition will be explored in one of the three Thursday morning sessions. Topics to be considered include microprocessor based CTDS equipment, a low cost optical data acquisition system, a dynamic scheduler for realtime multiport data acquisition system, design of the digital interface and computation portion of an automotive data acquisition system, and a high speed data acquisition and hardware signal processor for the TM990/101 microcomputer. Among the communications applications to be reviewed will be a multiterminal timesharing display system, the design of a programmable protocol translator, a microprocessor controlled user interactive telephone information dissemination system, the call process system, and a multiprocessor remote terminal. Biomedical applications of minis and micros will be presented in the third Thursday morning session. An extrasystole monitor using FIFOs, a microprocessor system for quantitative chromatographic data analysis, a pressure chamber control system for research in hyperbaric physiology, and a computerized technique for body surface isopotential maps will be described.

Thursday afternoon sessions on microprocessor based controllers will feature a robot control system, a control system for industrial sewing machines, a microprocessor controlled amusement ride, and an engine/generator control system. Under the heading signal processing, papers covering a programmable function generator based on a microcomputer, data acquisition with the Motorola MC68000 microprocessor, minicomputer aided analysis of eddy current signals, a microprocessor implemented fast Walsh transform, and software modem realization will be presented. The final session of the conference will examine transportation applications. Application of a microcomputer to dead reckoning of an electric cart, a hybrid traffic controller for isolated intersections, automatic monitoring system for the CCR and Aerodrome lighting system on airport runways, and radar headway control of an automobile will be detailed.

Tuesday evening's panel session will consist of vendor presentations. There will be eight 15-minute presentations by vendors having exhibit suites at IECI '80. The Wednesday evening special session will discuss software engineering techniques for microcomputer based systems.

Two parallel tutorials are scheduled for the day before the conference, Monday March 17. Tutorial 1, Data Acquisition System Technology, will be instructed by Richard C. Jaeger, professor at Auburn University. The course will provide a foundation for understanding the characteristics of data acquisition system components, including both analog and digital 1/0. Microprocessor interfacing and standard buses will also be covered. Tutorial 2 on Mini/Microcomputer Applications will be taught by Michael Andrews, professor at Colorado State University. This course, intended for engineers, physical scientists, and managers who understand minicomputers and have some knowledge of microcomputers, will supply further information about applying microcomputers, with handson explanation of several current hardware offerings. For additional information regarding cost and registration for the tutorials, please contact Vince Giardina, IEEE Education, 445 Hoes Lane, Piscataway, NJ 08854. Tel: 201/981-0060.

Conference registration before March 1 is \$70 for IEEE members and \$75 for nonmembers. Registration at the door is \$85/members and \$90/nonmembers. These fees include one copy of the proceedings and the awards luncheon. One-day registration at the door is \$55 and includes one copy of the proceedings. For more information, contact V. K. L. Huang, Room 2D109, Bell Telephone Labs, Murray Hill, NJ 07974. Tel: 201/582-4630.



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ENCODING/DECODING TECHNIQUES DOUBLE FLOPPY DISC CAPACITY

Double-density storage increases standard disc capacity without requiring modifications to the drive unit. Evaluation of different encoding, decoding, and format schemes shows how each impacts critical design considerations

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Ever increasing data storage requirements have caused designers to investigate new methods of expanding the 410k-byte single-density capacity of the standard 8" (20-cm) floppy disc. Double-density encoding, double-sided recording, and double-track density are the methods most often evaluated. Of these three, only double-density encoding has the advantage of doubling the system disc capacity with the same floppy disc drive used for single density. Additionally, improvements in head and media resolutions have made double-density encoding a highly reliable storage technique.

To double disc data density, one of several different encoding and decoding schemes can be implemented. Of these, modified frequency modulation encoding has become virtually the industry standard because of support by IBM as well as by several floppy disc controller chip manufacturers. With this method, twice as many data bits can be written on the disc medium than with single-density encoding. This increased storage impacts the design of the disc controller and the format of the medium. It also makes the decoding of data bits more susceptible to bit shift problems, in which bits are shifted away from their nominal positions. These effects must be carefully considered in the design of a doubledensity disc controller if soft error rates comparable to those of single-density drives (1 in 10⁹ bits) are to be maintained.

Single-Density Encoding Schemes

The fact that double-density controllers are more complex in design is easily explained by examining the differences between single- and double-density encoding. Parameters of various single- and double-density schemes are compared in the Table.

Frequency modulation (FM), based on the IBM 3740 method of encoding (Fig 1), is the industry standard

Single- and Double-Density Encoding Parameters

Parameter	Re FM	cording To MFM	echnique M ² FM	GCR
Bit Cell	4 µs	2 µs	2 µs	1.6 µs
Flux Changes/Cell	2	1	1	1
Flux Changes/in	6536	6536	6536	8170
Data Rate (kilobits/s) Storage Device System	250 250	500 500	500 500	625 500
Frequency Ratios	2/1	2/1	2.5/1	3/1
Bit to Bit Spacings	2 μs 4 μs	2 μs 3 μs 4 μs	2 μs 3 μs 4 μs 5 μs	2 μs 3.2 μs 4.8 μs
Diskette Capacity (kilobytes)	410	820	820	820

method of single-density encoding. With this scheme, a clock bit is written at the beginning of each bit cell, and data bits are written between clock pulses. Each bit cell is 4- μ s wide with the data bit written in the middle of the cell, or 2 μ s after the clock bit. Effectively, this scheme amounts to two flux changes per bit cell.

To decode a data bit in single-density recording, the data separator generates a $2 \cdot \mu s$ data window 1 μs after the clock pulse. Therefore, the data window—centered around the expected position of the data bit—allows the presence or absence of a data bit to be detected. Due to the $2 \cdot \mu s$ size, bits, even if shifted, are still likely to remain inside the window.

A constant bit cell reference, provided by the clock bit, simplifies encoding and decoding with this scheme (Fig 2). Many large scale integrated (LSI) disc controller chips are available to handle single-density data encoding and disc drive interfacing. The data separator circuit required to decode single density usually consists of simple timing circuits that generate the 2- μ s data window.

Higher-Density Encoding Schemes

Three double-density encoding schemes are presently used to increase floppy disc capacity: modified frequency modulation (MFM), modified-modified frequency modulation (M^2FM), and group coded recording (GCR). Each scheme increases disc capacity by replacing clock bits with data bits, using slightly different techniques. In each scheme, data rate as well as drive capacity is increased. The increased data rate might not affect controller design since most controllers incorporate a data buffer to transfer data asynchronously. Encoding schemes, however, do affect disc controller design.

MFM Encoding

With available head and media technology, MFM encoding is the most easily implemented and may become the industry double-density standard. It is used in the IBM System/34 and in all available double-density LSI disc controller chips. MFM encoding doubles floppy disc data capacity to 820k bytes by replacing the clock bit positions (used in FM encoding) with data bits (Fig 1). This scheme reduces the size of the bit cell by one-half to 2 μ s, thereby doubling data bit capacity.

Clock bits are still used, but are written only when data bits are not present in both the preceding and the current bit cell. As a result, there is only one flux change per bit cell. Clock bits are written at the beginning of the bit cell, while data bits are written in the middle, or 1 μ s after the bit cell's leading edge.

To decode data bits in MFM encoding, a data separator must generate a $1-\mu s$ data window and a $1-\mu s$ data window complement for a clock window. Because not every bit cell has a clock pulse, the data/clock windows cannot be timed from the clock pulse. Instead, the data separator must continuously analyze the bit position inside the windows so that the data/clock windows remain synchronous with the data/clock bits. Ideally, the bit will appear at the center of the window. However, data bits can shift outside the $1-\mu s$ data window due to bit-shift effects.

Consequently, data separator design, as well as overall disc controller design, for double-density encoding is more complex than for single-density encoding. Present LSI controller chips can handle the drive interface, doubledensity encoding function, and bit-shift pattern detection. However, bit-shift compensation circuits and a high resolution analog data separator must be added (Fig 2).



Fig 1 FM vs MFM encoding schemes. MFM encoding doubles number of data bits on disc media by replacing clock bits used in FM encoding with data bits. Scheme reduces bit cell width from 4 to 2 μ s and reduces data window to 1 μ s

Despite these constraints, disc controller design for MFM is simpler than that for either of the other two doubledensity encoding schemes.

M²FM Recording Scheme

Until recently, M²FM has been the commonly used doubledensity encoding scheme, because the resolution of the medium and the read/write head was not adequate for the 1- μ s data window used in MFM. In M²FM, a clock is written only if no data or clock bit is present in the preceding bit cell, and no data bit occurs in the current cell. Because clock pulses are relatively isolated on the medium, the effect of bit shift on clock pulses is minimal. Therefore, a narrower clock window can be used to decode the clock pulse. The width of the data window can thus be increased to 1.2 μ s, which allows more margin for shifted data bits.

Today's ceramic based read/write heads have much better resolution than those used in the past. This head design reduces the effects of bit shift, and makes the window margin provided by $M^{2}FM$ unnecessary. Additionally, $M^{2}FM$ is subject to a droop problem, which occurs in the read amplifier circuit when a low frequency pattern is read.

GCR Encoding

GCR encoding evolved from methods used in magnetic tape recorders. This method translates four data bits



Fig 2 Single- vs double-density circuits. Effects of bit shift require more complex circuits for double-density floppy disc controllers than for single-density controllers. In addition to different encoding circuits, bit-shift compensation circuits are necessary, as well as high resolution analog data separator into a 5-bit code during a write (Fig 3). During a read, the 5-bit code is retranslated to four data bits; no clock bits are generated. Using data rates specified by drive manufacturers, this scheme results in an 80% increase in density rather than a 100% increase. If the data rate is increased to provide double density, the number of flux changes per inch increases beyond reliable limits for floppy disc drives. This method requires more circuits to code, decode, and provide necessary lookup tables, and costs more than either of the other two double-density encoding schemes.

Bit-Shift Calculations

Bit shift occurs on any NRZ (nonreturn to zero) recorded medium—single or double density. Using the NRZ method, data are recorded by reversing polarity of current flow for each flux transition. This shift is, however, more noticeable with double density due to smaller bit cells and resulting smaller data/clock windows. Some aspects of bit-shift phenomena are predictable; other aspects are not.

Predictable bit-shift effects result from normal read/ write head operation. Data are written when the read/ write head generates a flux change in the gap of the head, which causes a change in magnetization of the medium oxide. In reading, a current is induced into the read/write head when a flux transition on the medium is encountered. The current change is not instantaneous, since it takes a finite time to build up to peak and then to return to zero (Fig 4). If flux transitions are close together, the current buildup after one flux transition declines, but it does not reach zero before a second transition begins. When current pulses are summed by the read/write head, the peaks are shifted. A negative flux change, for example, appears late because it has been added to the remnant of a positive transition.

This type of bit shift is predictable. Spacing between bits results in greater bit shift on the inner tracks (43 to 76) of the floppy disc (Fig 5). On those tracks, bits can be expected to shift up to 350 ns. On the outermost tracks (00 to 42), bit shift is negligible.

However, other causes for bits shifting from the position where they are written are not predictable. Variations in disc drive rotational speed can cause bits to shift by a constant, but unpredictable, amount. Drives are specified as 360 r/min $\pm 2\%$ rotational speed. The 2% variation includes a 1% allowance for 120-Vac line frequency variations and a 1% allowance for belt pulley tolerances. These variations will shift bits by as much as ± 40 ns from their originally written positions.



Fig 3 GCR encoding scheme. Four data bits are translated into 5-bit code during write; for example, data pattern 1101 is encoded into serial bit stream 01101, according to GCR encode rules. To decode, data window is generated around expected position of each bit. Result is serial read data of 01101, which must be decoded to 1101 by lookup table circuitry



Fig 4 Bit-shift effects. During reading, bits are shifted predictably from their written positions as result of normal read/write head operation. When flux change occurs on medium, current is induced into read/write head. Current change is not instantaneous, since finite time is required to build up to peak and then to return to zero. If flux transitions are close together, current buildup after one flux transition declines, but does not reach zero before second transition begins. Peaks shift when current pulses are summed by read/write head



Fig 5 Bit shift vs track position. Significant bit shift occurs on innermost tracks of floppy disc (43 to 76) because bits on these tracks are packed closer together and therefore are more susceptible to bit shift. On outermost tracks (00 to 42) bit density is less, so that predictable bit shift is minimal

Instantaneous speed changes, although smaller than rotational speed changes, also cause bits to appear shifted; this shifting effect varies from drive to drive. Write over, or incomplete erasure of, previously recorded data can also shift bits. These shifts can range up to ± 50 ns; again, they are variable and unpredictable. Other variable components of bit shift include electrical noise, radial alignment (offtrack), and nonsymmetry of the read/write head and associated electronics.

A bit shift of up to ± 450 ns can be expected. This number is obtained using observed figures for predictable and unpredictable components of bit shift.

Double-Density Controller Chip Design

Both predictable and unpredictable bit shifts must be accommodated in the design of a double-density disc controller if data are to be read reliably. Controller chips reliably perform MFM encoding and decoding. To compensate for predictable bit shift, however, compensation circuits must be added, and the data separator circuit must generate and position a high resolution data window so that a bit can be read reliably even if unpredictably shifted.

Despite the problems posed by bit shift, double-density controller design has been simplified with the recent introduction of LSI controller chips. For example, the NEC uPD765 and the Western Digital FD1791 perform MFM encoding and decoding as well as pattern detection to provide signals that identify which bits will be predictably shifted. These chips also perform serial/parallel conversion, generate cyclic redundancy check (CRC) characters for error detection, provide write current switches to reduce write current as density increases on the track, perform address mark detection for the IBM double-density format, and furnish intelligent status reporting. Both chips interface to commonly available 8-bit microprocessor based interface systems. Although they differ in software overhead and in hardware interface signals, the two chips are functionally the same.

Discrete logic circuit implementation of the same controller chip functions typically requires at least 60 to 70 integrated circuits (ICS), including a dedicated microprocessor, although greater format flexibility is possible than with the LSI chips, which require fixed gap lengths in the formats. Bipolar logic implementations of the same controller chip functions also result in a larger part count. Because some error detection functions can be performed in software, the bipolar parts count is somewhat less than that of discrete logic parts. Still, either method is substantially more complicated than the LSI chip implementation.

Bit-Shift Compensation Circuits

Since some aspects of bit shift can be predicted, it is possible to compensate for this shift within the design of the disc controller. Two methods currently being used are precompensation and postcompensation.

With precompensation, bits are deliberately shifted in the direction opposite that of the expected shift. As data are being written, the LSI controller chip detects bit patterns. From these bit patterns, the controller calculates which bit will shift in which direction. Since bit shift is negligible for the first 43 tracks of data, the controller issues no precompensation signals until after track 43.

For example, a 4-bit pattern of 0110 on an inner track would cause the third bit to appear as much as 350 ns later than its nominal position. The controller chip, after detecting this late bit-shift pattern, would generate an early signal, indicating that the third bit should be written earlier to make it appear closer to its nominal position when read. Conversely, if the third bit were going to appear early, a late signal would be generated so that the bit could be written later.

How early or late the bit should be written is a function of its position in the data pattern and its track position, among other factors. The shift at middle and outer tracks can range from 50 to 350 ns. For optimum precompensation in all cases, 150 to 175 ns of precompensation is recommended for both early and late bits. Timing circuitry that achieves this precompensation includes counters, shift registers, delay lines, and 1-shot delay circuits.

For example, a 1-shot precompensation circuit (Fig 6) is connected to the controller chip early- and late-bit signals. Based on precompensation of 175 ns, a 300-ns delay is used for an on-time bit, a 125-ns 1-shot delay is used for a bit to be written early, and a 475-ns 1-shot is used for a bit to be written late. The trailing edge of



Fig 6 Precompensation circuit. To compensate for predictable bit shift, circuit writes early bits that would normally be shifted late during reading. Conversely, bit expected to appear early is written late

each of these 1-shot pulses fires a fourth 1-shot to provide a standard width write pulse to the disc drive.

Postcompensation alters the read signal rather than the write signal. Since bit shift is, in part, a function of read channel frequency response (phase characteristics), post-compensation circuitry changes the read signal after track 60 to compensate for bit shift. This IBM method is relatively new; floppy discs written on System/34 are incompatible with disc drives that do not use postcompensation.

Data Separation

Substantial reductions in the amount of bit shift can be achieved using either a pre- or post-compensation method. However, unpredictable bit shift can still occur. Therefore, special design consideration must be given to the type and resolution of data separator used in reading data bits from the disc.

The bit stream transferred from the disc to the controller consists of composite clock and data bits. With single density, a data bit is decoded by a data window that is generated from the clock bit. In double density, the lack of consistent clock bits makes it impossible to generate a data window in this manner. Instead, the separator circuit must first determine the nominal position of clock and data bits and then generate a $1-\mu s$ clock and data window that is centered around the bit positions. The more accurately the bit position can be determined and the tighter the resolution of the data window, the lower the soft error rate of the disc.

The $1-\mu s$ data window must be centered on a bit that can potentially shift as much as ± 450 ns. This shift leaves less than a 50-ns margin to the edge of the window; a data bit appearing on the edge of the data window could be read as a clock bit. The total error from the data separator circuit must therefore be less than ± 50 ns. To determine the nominal bit position around which to center the window, the data separator must track data bit frequency changes. In this manner, even if an unpredictable bit shift occurs, the data separator can adjust the window's position to compensate for the change. Otherwise, the shifted bit could be positioned outside the window. To remain within the error rate specified by drive manufacturers, not more than 1 in 10⁹ bits can appear outside the window. With present technology, only an analog data separator based on a phase-lock loop technique can provide the necessary reliability.

Digital data separators have lower resolution than an analog phase-lock loop type of separator, and cannot accurately determine the nominal position of the data bit around which to position the window. As a result, error rates higher than those specified may result from the use of digital data separators.

For clarity, the performance of a typical digital data separator is examined. To generate a data window, a crystal clock is divided down by a value preloaded in a counter to create a 50/50 data/clock window. Assuming that a 20-MHz clock is used, the smallest increment to which the window can be adjusted is the least significant bit (LSB) of the counter, which in this case is 50 ns. The separator determines the nominal bit position around which to center the data/clock window by sampling bit positions within the window. From sampling results, the data separator adjusts the window position using a feedback mechanism that changes the preload value in the counter. This effectively shifts the window position relative to the nominal bit position.

The 50-ns resolution, however, creates a problem. As shown in Fig 7, if a bit is shifted a maximum of 450 ns in one direction, the digital data separator will compensate by moving the window 1 LSB or 50 ns in that direction. If a subsequent bit is then shifted 450 ns in


Fig 7 Data separator timing diagrams. Unpredictable bit shift is handled differently by digital and analog data separators. Typical digital data separator, using 20-MHz clock, provides 50-ns resolution. Assuming two worst case bit shifts in opposite directions, data bit would appear outside data window. Analog data separator, however, provides 1-ns resolution. As result, it can handle unpredictable bit shift more reliably than digital data separator

the opposite direction, that bit will appear 50 ns outside the window, resulting in a misread.

An analog phase-lock loop separator, on the other hand, has tighter resolution $(\pm 1 \text{ ns})$ and handles bit frequency changes more reliably (Fig 7). With this method, a phase-lock loop locks onto the basic frequency of data bits read off the disc, and determines nominal bit positions for data and clock bits by sampling every bit (clock and data). It uses the phase relationship between a bit and its window to vary the position of the window. By sampling each bit, the phase-lock loop determines the phase error between a bit and the frequency being generated.

Changes in the data window position depend both on an integration factor and on the amount of bit position error. For an integration factor of 100:1, the data window would move 1 ns per bit cell for each 100-ns change in bit position, until the entire error had been compensated.

Using the same example as described for the digital data separator, the phase-lock loop would detect the data bit shifted late by 100 ns. Then, the data window would be adjusted so that it appeared 1-ns late. If the next bit is shifted early, the analog separator would also detect that shift and position the next data window, not late, but early. In this manner, the phase-lock loop reliably tracks frequency changes. A block diagram of a typical phase-lock loop circuit is shown in Fig 8.

Double-Density Formats

In double density, data are encoded differently from single density, but are formatted more or less identically on the disc. Each of the 77 data tracks on a standard 8'' (20-cm) floppy disc is organized in data records, which are also referred to as sectors. Two methods of sectoring currently exist: hard and soft. In the more prevalent soft sectoring, the number of sectors and their length can vary. Optimum sector size for systems with small main memories and smaller data bases may be as low as 128 bytes. For those systems with larger main memories and large data bases, 256 or 512 bytes per sector may be optional.

Soft sectoring is supported by IBM in both double- and single-density controllers. The double-density format shown in Fig 9 is used in the IBM System/34 and will likely become the industry standard. It is also the format supported by available LSI disc controller chips. Similar in most respects to the standard single-density format, the double-density format has the same number of sectors (26), each with twice as many bytes (256).

Double-density format differs from single-density format in the way an address mark is detected. An address mark flags the beginning of every index, identification (ID), and data field. In both single- and double-density recording, the address mark is unique in terms of its clock pattern; the single-byte single-density address mark contains two or three missing clock pulses.

This method is modified for double density because dropping two or three clock bits in a row could cause the data separation circuit to lose synchronization. In double density, each of the first three bytes of a 4-byte address mark has one active data bit followed by four zero data bits. According to double-density encoding protocol, the three zero data bits should have an associated clock pulse. However, to make the address mark unique, the middle clock pulse is dropped. The respective address marks for index, identification, and data fields are made unique by their associated data pattern. For example, an index address mark has three C2 bytes (hexadecimal), followed by an FC byte; an ID address mark has three A1 bytes followed by an FE byte; and



Fig 8 Analog phase-lock loop data separator. Input selector selects write clock signal as input to phase detector until start logic has detected synchronized area preceding address mark of formatted disc. At that point, input selector switches from write clock to read data as input to phase detector. Phase detector then begins sampling difference between read data and output of voltage controlled oscillator (VCO). A \div N counter continually divides VCO frequency down to same frequency as read data. Finally output of \div N counter becomes data/clock window

data has three A1 bytes followed by an FB byte. This bit pattern is automatically generated by the controller chip, as is the CRC character at the completion of the data and ID field.

Obviously, LSI controller chips simplify disc formatting, but offer some limitations on format flexibility. If a designer chooses to configure a custom format, certain design guidelines for gap length must be observed if data are to be recorded reliably.

Gap 1 of 22 bytes must be present if an index address mark is used to separate the index address mark from the first identification field. Gap 2 of 22 bytes, which separates the identification and data fields, is necessary to protect the ID field from erasure during a write. Gap 3 of 54 bytes is a speed tolerance gap, which again protects the ID field if the medium is interchanged between drives with different rotational speeds. Gap 4 is also a speed tolerance buffer. This gap length is determined by the difference between the format length and the actual track capacity, which may vary from drive to drive. A double-density format (shown in Fig 9) is, with some exceptions, the same as a single-density format with gaps and data fields that are twice as long.

Summary

Improvements in head and media resolution have made double-density encoding a reliable method of doubling the capacity of a floppy disc from 410k to 820k bytes. A minifloppy drive, using double density, can increase its capacity from 110k to 220k bytes. Research analysis into the problems of bit shift has enabled designers to reliably compensate for bit-shift effects so that a minimum soft error rate in excess of 1 in 10⁹ is possible with double-density encoding. LSI controller chips have made double-density system design less complex, less time consuming, and therefore less costly. In addition, doubledensity floppy discs with doubled capacity can be implemented on single-density drives. These capabilities



should broaden the applications of floppy disc drives and make systems with multiple floppy disc drives more compact.

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MULTIPROCESSING SYSTEM MIXES 8- AND 16-BIT MICROCOMPUTERS

Combining different single-board computers on a single bus and assigning to each the tasks most suited enable a cost-effective multiprocessing system configuration with improved throughput and reliability

Joseph P. Barthmaier Intel Corporation, Hillsboro, Oregon

wo or more single-board computers can share a common system bus to provide improved performance, reliability, and cost-effectiveness in medium to large scale applications. Interfacing multiple computers across a system bus affords a dual-bus architecture in which global system traffic is isolated from local traffic on the board buses. This allows a straightforward design of modular multiprocessing systems that combines different computer boards, and allocates to each that portion of the overall system function to which it is best suited.

In a typical design, 8- and 16-bit single-board computers (sBCs) communicate across a system bus to service an application that requires both realtime data acquisition and extensive signal processing. Partitioning system tasks and assigning each to the appropriate SBC optimizes performance without adding components. Dualport memory provides a convenient way to synchronize processes on different SBCs. Because most system functions are isolated on one SBC, reliability and throughput are increased, and implementation is facilitated.

Single-Board Computer Concept

In earlier SBC design, the fundamental goal was to provide a board containing all the resources required for a large variety of microprocessing applications. A typical processor board supplies an 8080A processor, 4k bytes of random access memory (RAM), sockets for up to 8k bytes of erasable programmable read only memory/read only memory (EPROM/ROM), a serial input/output (I/O) interface, 48 parallel I/O lines, three timer/counters, and eight levels of priority interrupt. With this hardware configuration, many small applications can be served with no need for additional memory or digital logic.



Because larger applications require additional resources, an external bus structure was defined. The MULTIBUSTM system bus was designed for communication between SBCs and system expansion boards. Address, data, and handshake lines were defined for memory and I/Otransfers between SBCs and expansion boards. There are bus expansion boards for system expansion in areas of RAM and ROM storage, serial and parallel I/O, analog I/O, and peripheral controllers.

In Fig 1, two buses interconnect a system with an SBC and two expansion boards. An onboard bus accesses local resources, and the system bus accesses global resources. A key advantage of this structure is that an SBC may not require the system bus for a large portion of its memory or 1/0 transactions. In many applications, less than 10% of the time is taken by system bus accesses. The large amount of potential system bus capacity makes this architecture a natural candidate for multiprocessing applications. As additional SBCs are included in the system, the incremental amount of system bus bandwidth required is usually small.

Motivations for Multiprocessing

Certain system applications benefit from using more than a single SBC. Motivations for constructing multiprocessing systems with SBCs include:

Resource sharing. In a multiprocessing system designed around the resource sharing concept, two or more processor boards share a common resource, such as a high speed mathematics board or a peripheral controller. These boards perform independent functions with no relationship to one another except for the shared resource. Low cost is the obvious motivation for using a resource sharing multiprocessing configuration. If two processor boards share the same diskette controller, for example, overall system costs are considerably reduced. Enhanced system throughput and performance. In many applications, significant improvements in performance may be achieved by using more than one processor in the system. Two ways of allocating or partitioning system functions among multiple processors, such as pipeline and parallel partitioning, are shown in Fig 2. In pipeline partitioning, system functions (tasks) are divided among several processors, so that data flow through the system is primarily serial. Each processor performs its portion of system functions, and then calls upon another processor to perform another set. An example of pipeline partitioning is when one processor performs data acquisition and buffering, while a second uses the data to perform digital signal processing.

Parallel partitioning allocates system functions among several processors in such a way that each processor performs a separate system task in parallel. An example is a system where one processor performs an industrial process control loop, while another monitors and controls a varying parameter, such as temperature.

Few systems may be characterized as totally parallel or pipeline partitioned, but designating systems in this manner can often be helpful during the system design phase, particularly when interprocessor communication software is being designed.

Modularly configured systems. A primary design goal, particularly in systems that are produced in low volume,

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Fig 2 Pipeline and parallel partitioning. Single processor A performs tasks X, Y, and Z. Pipeline partitioning among three processors allows processor B to perform task X and pass result to processor C; processor C to perform task Y and pass result to processor D; and processor D to perform task Z. Each processor except first must wait for input data generated as output from another processor. partitioning Parallel allows each processor to perform its task independently

is often flexibility of system configuration. Using modularly configured systems, independent hardware and software modules are designed and implemented with individual processors or intelligent slave boards. When a particular configuration is required, the system designer selects the necessary hardware and software modules and combines them with interprocessor communication software. Shortened system development time, simple debugging, and a convenient upgrade path for system expansion are the benefits of such a technique.

High reliability. Multiprocessing may be used to isolate system tasks on individual processors in applications where a high degree of reliability is a requirement. If a processor fails, the remainder of the system continues to operate. Redundant designs, where a second processor may be dynamically assigned to perform the functions of a disabled processor, are a possibility.

Multiprocessing With Single-Board Computers

The MULTIBUS architectural design facilitates multiprocessing because multiple bus masters are accommodated, bus masters generate and acknowledge bus interrupts, and dual-port memory and intelligent slave architecture can be implemented.

Multiple Bus Masters

A bus master is a dynamic board that takes control of the bus by asserting address and control lines. Only one bus master may control the bus at any given moment. Examples of bus masters include single-board computers and direct memory access (DMA) controllers. A bus slave is a passive element on the bus that does not assert address and control lines. Examples of bus slaves include memory or I/O expansion boards and intelligent slaves.

Several control lines exist on the bus so that potential bus masters can exchange control. These control lines, plus logic on the master boards, implement a priority scheme in which the highest priority master requesting the bus obtains control. There are two priority resolution schemes for exchange of the bus, serial and parallel. Using serial priority resolution, there may be up to three bus masters in the system; the parallel technique allows up to 16. A bus master is always given the opportunity to complete a bus transaction before being preempted by a higher priority master. In addition, bus masters may retain control of the bus by "locking" the bus. The bus lock feature is required when a master must have exclusive control of the bus for such functions as testing and setting software semaphores and completing operations involving I/O devices.

Since SBCs have extensive onboard resources, system bus transactions are not required for all I/O and memory accesses. Depending on the application and system design, multiple bus master systems with a small number of transactions can be configured. The system design goal is to use onboard resources whenever possible. Frequently executed or time critical code should be stored in onboard memory to minimize system bus accesses and to avoid delays while contending for the bus.

Interprocessor Interrupts

Eight interrupt lines exist on the system bus. In addition to interrupts from I/O slave boards or DMA controllers,

these interrupt lines can be used for communication between master SBC boards. Individual master boards may either generate interrupts or be interrupted from one or more of the interrupt lines. Interprocessor interrupts provide a fast and effective way for multiple SBCs to communicate over the system bus.

Dual-Port Memory

Single-board computers have been designed with onboard RAM containing two access ports. Dual access ports permit the onboard CPU to access the RAM directly using the onboard bus. Other SBCs also access the RAM using the system bus. The amount of memory available for system bus access may be selected from all memory accessible to no memory accessible, in increments of one-half or onequarter of available memory size. This ability to block RAM access from the system bus provides memory protection for data and code stored in those nonaccessible areas of the dual-port RAM. Fig 3 illustrates an example of two SBCs accessing the dual-port memory of one SBC.

Two important benefits are gained by using the dualport architecture. First, in a multiple-processor system, if two processors communicate through shared memory, only one must access the memory using the system bus, and the amount of system bus traffic may be significantly reduced. Second, in a multiprocessor configuration where limited RAM storage is required, a separate memory board is not needed. Such small systems have all the required system bus-accessible memory on one or more of the SBCS.

Intelligent Slave Architecture

To distribute intelligence in larger systems, the intelligent slave concept was developed. An intelligent slave is a board that contains a CPU, some dedicated I/O capability, and a dual-port RAM for interfacing to the system bus. For example, the isBC 544^{TM} intelligent communications controller contains an 8085A processor, four 8251A serial I/O devices universal synchronous/asynchronous receiver/transmitters (USARTS), 12 levels of priority interrupt, and 16k of dual-port RAM. All communication between a master processor board, such as an isBC $86/12A^{\text{TM}}$ board, and the 544 takes place using the 544 dual-port RAM (Fig 4). The 8085A processor does not have the capability of taking control of the system bus (becoming a bus master) and accessing other system resources.

The 544 board was designed to operate using only onboard resources. The master SBC in the system transfers blocks of data and parameters to or from the 544 using the onboard dual-port RAM. To facilitate communication with the 544, an interrupt occurs when a master SBC writes into the lowest byte of memory of the dual-port RAM. The intelligent slave board can interrupt a master SBC by asserting one of the system bus interrupt lines with an I/O instruction. The address space occupied by the dual-port RAM may be set anywhere within 1M bytes; 20 address bits are decoded.

Primary advantage of intelligent slave architecture is the ease with which multiprocessing applications may be implemented. The intelligent slave may be sent a buffer of data and commands with an interrupt occurring, via a write to the lowest byte of memory, as a start command. The master SBC may continue operation with other functions to be notified, via an interrupt or a status byte in dual-port RAM, when the slave has completed a task. Since the intelligent slave may not access system resources via the system bus, no interference with the master SBC can occur.

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The 86/12A Board

The isBC 86/12A single-board computer¹ has many of the architectural features of 8-bit boards (serial and parallel I/0, multiple interrupt levels, and timer/counters) but includes a 5-MHz 8086 microprocessor and larger amounts of RAM and EPROM/ROM storage. The 16-bit 8086 permits byte and word transfers, hardware multiply/divide, 1M-byte addressability, extensive string manipulation instructions, and many other features. The 86/12A contains 32k bytes of dual port RAM and sockets for up to 16k bytes of EPROM/ROM, doubling the memory available on previous boards. If more RAM or EPROM/ROM storage is required, memory expansion modules permit doubling RAM and/or EPROM/ROM storage to 64k bytes of RAM and 32k bytes of EPROM/ROM.

Memory expansion modules are small printed circuit boards that attach to the 86/12A board using sockets and nylon bolts. Use of the expansion modules is advantageous from a price/performance point of view. Price of either of the memory expansion modules is significantly less than that of an equivalent separate memory expansion board with its own system bus interface and support circuitry. Memory expansion modules also offer higher performance since it is not necessary to use the system bus for memory transactions. All transactions take place using the onboard bus with no additional wait states or bus contention. sented to the microprocessor on its low order data lines, D0 through D7. When a byte transfer is requested from an odd address, data transfer must occur on the high order data lines, D8 through D15. When a 16-bit (word) transfer is requested, data are transferred on all 16 data lines, D0 through D15. When an 8-bit microprocessor (8080A or 8085A) is used, however, all byte transfers must take place on data lines D0 through D7, the only lines available.

To maintain compatibility between boards with 8-bit and 16-bit processors, a system bus transfer protocol has been developed where all byte transfers, regardless of whether from an odd or even address, take place on the low order system bus data lines, DATO/ to DAT7/; word transfers, however, use all 16 data lines, DATO/ to DATF/. To accomplish these byte transfers, an 8-bit buffer is used on 16-bit master and slave boards for transferring data from the high order data lines on the board to the low order data lines of the system bus. An additional signal line, byte high enable, (BHEN/) indicates whether a word transfer is taking place on the high order and low order data lines or whether a byte transfer is taking place only on the low order data lines. Fig 5 illustrates 8- and 16-bit transfers and the use of the additional buffer for transferring the signal to or from the high order data byte.

Multiprocessing System Example

A data acquisition and signal processing system design demonstrates the capabilities of a multiprocessing system, where improved performance is mandatory. General application of the system is power spectrum analysis of vibration and acoustic signals. Application areas for such

8- and 16-bit MULTIBUS Compatibility

The 8086 microprocessor performs 8- or 16-bit transfers to or from memory or I/O devices. When a byte (8-bit) transfer is requested from an even address, data are pre-



Fig 5 Three mechanisms for byte and word transfers. All byte transfers use DAT0 to DAT7. Only word transfers use high order bus lines DAT8 to DATF. Slash (/) after name indicates active low signal

systems include vibration analysis in mechanical structures such as electric motors, automobiles, aircraft, and buildings, as well as speech, sonar, and low frequency radar analysis.

Design objective is to monitor the condition of large electric motors. Power spectra of vibration signals from various points on the motor are calculated in order to detect bearing wear and to predict an impending motor failure. Calculated power spectra are compared with reference spectra, and, if thresholds in various regions of the spectra are exceeded, an operator alarm is activated. Information regarding the state of the motors and the reference spectra is stored on disc.

The system monitors 16 channels of analog input signals generated by pairs of accelerometers mounted on each of eight motors. Sampling and calculations for the two channels of a single motor are performed simultaneously; then the next motor in sequence is monitored.

Fast Fourier transform (FFT) of a buffer of samples from an analog to digital converter (ADC) performs power spectrum calculations. Real and imaginary parts of the FFT results are squared and summed to form a power spectrum that is compared to the reference power spectrum in order to determine if the motor vibrations are within acceptable tolerances. A CRT displays calculated and reference power spectra. At periodic intervals, data are stored on disc for archiving the condition of each of the motors. If the motor spectra exceed the reference spectra, the CRT display and a control panel indicator alert the operator.

System Hardware

As shown in Fig 6, the 711 analog input board, containing a 12-bit ADC, samples the 16 analog signals from the motors. The 80/05 processor board drives the 711 analog board and handles all system data acquisition activities. The 80/05 contains an 8085A CPU, 512 bytes of RAM, up to 4k bytes of EPROM/ROM, a timer/counter, parallel and serial 1/0 lines, and four levels of priority interrupt. The 86/12A board is the main system processor. The 8086-based board performs all the signal processing functions, displays the spectra on the CRT, drives the system control panel, and transfers motor condition data onto disc using the 204 single-density diskette controller.

Increased system performance is the design motivation for using two processor boards. The 86/12A board, with its 5 MHZ 8086 CPU, 16-bit multiply/divide capability, 64k bytes of dual-port RAM, and 32k bytes of EPROM/ROM, is used for the mathematically intensive power spectrum calculations.

The 80/05 processor board is used to offload data acquisition activities from the main processor. It assumes all the overhead of handling the 711 analog board. Sampling is performed at 250-µs intervals using the onboard timer; data from the two channels are scaled, demultiplexed, and stored in a buffer. The 8-bit processor board



was chosen for this function because it had the necessary onboard resources, yet was low in cost. Throughput performance improvements of up to 40% can be achieved using this 2-processor approach.

The 80/05-711 combination assumes the role of an intelligent analog subsystem, when viewed by the 86/12A processor. The 86/12A sends the 80/05 commands via a parameter block, and the 80/05 collects the data samples in buffers. When a buffer is complete, the 80/05 signals the 86/12A using the parameter block. Thus, the 80/05 acts as an intelligent DMA controller for the 711 board.

System Software

Due to the large RAM requirements of the system, the iSBC 300TM RAM expansion module is used to increase RAM capacity to 64k bytes. Memory has been configured to make 16k bytes of memory accessible to the system bus, with the remaining 48k bytes reserved for use by the onboard 8086 and not accessible to the system bus. The amount of 86/12A dual-port RAM that is system bus accessible may be configured in 16k increments from zero (no memory accessible) to 64k (all memory accessible). The parameter block used for interprocessor communication and a pair of buffers used for storage of the analog samples are stored in the memory accessible to the 80/05. Memory not accessible to the 80/05 contains the data and buffers used for the calculated averaged power spectra, reference spectra, CRT displays, and disc data. The 16 bytes of the parameter block contain all information required for communication between the two SBCs in the system, including buffer addresses, status, size, sample rate, and start and end channel.

Fig 7 is a flow diagram illustrating how buffer status bytes are used to synchronize the filling and processing of the data buffers. Each buffer may be in one of two states, FULL or EMPTY. Initially, both buffers are EMPTY. At initialization, the 80/05 fills buffer 0, sets its status to FULL, fills buffer 1, sets its status to FULL, and waits for buffer 0 to become EMPTY. It then fills buffer 0, sets its status to FULL, waits for buffer 1 to become EMPTY, etc. Initially, the 86/12A waits for buffer 0 to be FULL, processes it, sets its status to EMPTY, waits for buffer 1 to be FULL, etc. Using this simple technique, the two processors synchronize each other with a minimal amount of overhead.

The parameter block approach is used to provide a simple means for interfacing the two SBCs. At system initialization, the 80/05 board needs only to know the base address of the parameter block. Once this is known, all other information required for the 80/05 to function properly is available. The end application and even the specific type of SBC that calls upon the 80/05 for data samples remain irrelevant to the 80/05. Driver software for the 80/05 is therefore highly modular and may be used in a variety of applications and configurations with no changes required.

A key capability of this system design is that the 86/12A board does not use the system bus to access data samples, thus minimizing execution time for the highly iterative FFT computation. The 80/05 processor takes the samples from the analog board and stores them directly into the 86/12A dual-port memory. Therefore, except for occasional disc transfers by the 86/12A, the 80/05 is the only processor using the system bus. This increases system throughput and eliminates contention for the system bus.

Signal Processing Software

The algorithm used for the FFT in this application is known as "time decomposition with input bit reversal."² Using this algorithm, an in-place FFT has been programmed for an input frame size of 128 complex points. Sixteen-bit integer mathematics is used for all internal calculations of the FFT. The 86/12A board computes the 128-point complex FFT in 110 ms. Computation of the averaged power spectra is performed using a double pre-



cision integer format. The 16-bit integer real and imaginary values which result from the FFT are squared and summed to obtain a 32-bit power spectrum. Thirty-two frames of data are processed and summed to form the averaged power spectrum.

Summary

Two reasons for the slow growth of multiprocessing have been the limited selection of sBCs and the relatively small application base. These conditions are changing rapidly due to the large number of sBCs now available. These boards contain dual-port RAM and newer 8- and 16-bit CPUs, and provide system designers with a comprehensive set of tools for tackling applications that require the power of multiprocessing. Thus, the sBC application base has grown significantly in recent years.

The system application combines a low cost 8-bit SBC and a high performance 16-bit SBC in a configuration designed for both data acquisition and signal analysis. The 8-bit SBC relieves the 16-bit SBC of all system data acquisition functions. Because the 16-bit board spends full time processing data, system throughput can be increased by as much as 40%.

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SEMICONDUCTOR MEMORY UPDATE —PART 3: HIGHER DENSITY TECHNOLOGIES

Merging memory technologies have evolved magnetic bubbles, charge-coupled devices, Josephson junction, and gallium arsenide techniques that hold the promise of megabit and gigabit densities, impacting immediate and potential computer storage

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Parts 1 and 2, published in December and January, revised and updated data on the status of read only and random access memories, respectively. Together they have managed to yield the memory storage necessary for most applications. Increasingly, however, microprocessors are demanding greater storage. Thus, as shown in Part 3, the growth of larger capacity memories is evolving naturally from this existing technological memory base, appearing as magnetic bubbles, charge-coupled devices, Josephson junction logic circuits, and gallium arsenide LSI circuits.

he discussion of metal oxide semiconductor and bipolar random access memories in Part 2 dramatically demonstrated that these two technologies are indeed merging. Address access times of metal oxide semiconductor are approaching those of bipolar more rapidly than bipolar access times are being reduced. Both are powered from a single 5-V source, with bipolar power dissipation decreasing to approach that of metal oxide semiconductor. Random access memory storage cell sizes of both are comparable since device geometries are

smaller and similar for the same density random access memory due to die scaling; in addition, the number of masks used for high performance metal oxide semiconductor is equivalent to that used for bipolar.

Fabrication complexity increases as high density and high performance designs are implemented. When compared with the 10 to 12 masks needed in 2-metal transistor-transistor logic (TTL), advanced (scaled) metal oxide semiconductor (MOS) processes clearly are as complex to implement as most intricate bipolar technologies. Thus, the advantage of MOS over bipolar will tend to disappear. For example, a 2-poly $2-\mu m$ HMOS process uses 10 to 12 masks and a 2-poly VMOS process uses 11 masks. Table 1 compares several bipolar and MOS processes from this masking viewpoint.

Therefore, with these developments, manufacturing costs for the same density bipolar and MOS random access memories (RAMS) should approach each other as well. Fig 1 shows the effects of merging bipolar/MOS technologies and how they relate to RAM usage. The TTL memory share of microcomputer through mainframe applications will dwindle through 1982 due to increased performance of MOS. After 1982, MOS will be the dominant RAM technology for microprocessor controlled systems through large computers. Emitter-coupled logic (ECL) will dominate the high end of the performance scale for super computer and large, high performance applications. TTL will still be used, but sparingly; it will not be the primary memory technology.

Magnetic Bubble Memories

If a storage capacity (bit density) of greater than 64k bits is needed, the logical choice is magnetic bubble technology. Memory systems based on magnetic bubble technology have a number of significant potential applications, notably in filling the prominent speed/cost and capacity/cost gaps in conventional memory hierarchies, as well as serving as microperipherals. Magnetic bubbles can be viewed as a solid state implementation analogous to rotating electromechanical memories such as discs, drums, and tape recorders. Also, magnetic bubble memories offer a combination of high demand capabilities: nonvolatility of stored data, reasonably fast access time compared to mechanical storage systems (but slower than semiconductor RAM systems, 7 to 10 μ s), relatively low power drive requirements, and high reliability. Just as attractive is the very high density of 1M bits and more in a package slightly bigger than a large dual-inline package.

Large memory systems, such as multiple disc drives, derive their low cost per bit by spreading the high fixed cost of electromechanical components over a very large number of bits. If the actual data capacity needed in a system is less than a few megabits, disc cost per bit rises dramatically. The minifloppy disc drive is a partial answer to reduced storage requirements, but actually the cost per bit goes up even as the hardware cost comes down.

Bubble memory components, however, permit the memory system to be expanded in smaller increments (64k-, 92k-, 254k- or 256k-, and 1M-bit steps) with

Technology	Logic	No of Masks*	(Or Implants)	Epitaxial	(Or Poly)
Bipolar	STTL	7 to 10	4	Yes	1
	STTL	9 to 12	4	Yes	2
Bipolar	Local Oxidation	7 to 12	4	Yes	2
Bipolar	IIL	7 to 12	3 to 4	Yes	1
MOS	Metal Gate	5 to 7	1 to 2	No	1
MOS	Silicon Gate	6 to 8	1 to 2	No	1
MOS	Scaled NMOS	8 to 10	2	No	2
MOS	VMOS	9	1	Yes	1
MOS	Double Poly/ Triple Poly	9 to 11	1 to 2	No	2/3
MOS	CCD	4 to 9	1	No	2
MOS	CMOS	6 to 8	2 to 3	No	1
MOS	CMOS/SOS	6 to 8	2 to 3	No	1
GaAs	-	6 to 10	2	Yes	2 to 4
Magnetic	and - Constanting and	4	0	No	2

TABLE 1 Technology Comparison

*Exact number of masks used is determined by an individual supplier's process refinements. Consequently, a range is listed for most technologies to account for these variations from manufacturer to manufacturer.

currently available products. As a result, the optimum memory size for a system can be designed in immediately. Then, the system can be expanded in inexpensive blocks, with the cost per bit staying low at all times.

Presently, traditional full floppy disc memory systems offer a larger storage capacity than do available magnetic bubble chips. However, technological developments will soon bring bubble chip cost down to that of a disc system. The two technologies can be melded to provide fast access to frequently used data, yet minimize mechanical wear and access delays. Bubble memory technology in harsh environments is already cost-competitive, and there are some applications where no other device can do the job. Costs of 50 to 100 millicents per bit are competitive in severe vibration, contaminated atmosphere, and continual access situations.

How rapidly bubble memories achieve equality with semiconductor and disc memories depends on the ability of the semiconductor industry to solve existing technology problems: the significant difference of magnetic bubbles from static and dynamic RAMs that requires diverse design rules; lack of standardization in package, pinout, organization, function, and architectures; and need for test and characterization equipment, as well as support circuits. Until these problems and the lack of second sources are solved, bubble chips having IM-bit and larger densities will not be in high volume production in the near future.

In current devices, small cylindrical magnetic domains, called magnetic bubbles, are formed in single crystal thin films of synthetic ferrites or garnets when an external magnetic field is applied perpendicularly to the surface of the film (Fig 2). A rotating magnetic field is used to move the bubbles along a path outlined by a deposited layer of metal on the surface of the magnetic filter in a shift register fashion; the presence of a magnetic bubble represents a digital 1, and the absence a digital 0. Types of material and techniques used for processing magnetic bubbles are similar to those used for semiconductor memories. However, with fewer mask levels and without stringent alignment requirements in processing, the bubble memory price per bit should be lower than that of silicon integrated memories.

Before bubbles can be shifted through the magnetic film, they must be generated and must correspond to input data. A microscopic 1-turn metallized loop, located in a secondary layer just above the magnetic film, is used to produce the magnetic bubbles. A precisely defined current pulse passing through the loop alters the local magnetic field and generates a magnetic bubble.

In addition to the onchip bubble generating circuit, special control functions for destroying, transferring, and sensing are also required to write, swap, and detect bubbles, respectively. All these functions are performed in aluminum-copper patterns deposited over the magnetic film. Also deposited on the chip are permalloy (80%Ni, 20% Fe) metal patterns; these form an easily magnetized layer on the chip above the aluminumcopper metal and are separated from it by an oxide deposition. The permalloy pattern defines the path that the bubbles travel in the magnetic film. A commonly used pattern is the chevron structure. Once a bubble



Fig 1 Computer trends vs semiconductor technology. Advances in NMOS technology will squeeze bipolar RAMs only in high performance applications utilizing ECL techniques. Standard TTL RAMs should eventually phase out





is created, it moves along the path determined by chevron shaped patterns (guides) of soft magnetic material deposited on the magnetic epitaxial film. Under the influence of the rotating magnetic field, these chevron guides set up magnetic polarities that shift the magnetic bubble domains (Fig 3).



A feasible, recent development for constructing devices capable of storing 25M bits in an area of only 1 in^2 (6.5 cm²) departs from the conventional chevron pattern. Developed by IBM, the contiguous disc approach to bubble control permits bubbles to ride on the edge of a guide rather than beneath it. This results in a smaller bubble size and a denser memory, but uses conventional photolithographic techniques.

Forming closed tracks or loops, permalloy paths contain a fixed number of bit positions. Major and minor loops are formed on the chip. A major loop holds one bit from each of the large minor loops, which actually store the data. Contents of the same relative bit positions of each minor loop in the chip represent a block of binary data. Data are typically entered at the generators through transfer-in switches to a major loop. The desired data block is then lined up on the major loop with the desired minor loops that will actually store the block, and the entire data block is written into the minor loops. Other circuits on the chip perform the read operation. Replicate transfer gates reproduce a data block from the minor loops to the read major loop. This nondestructive readout technique prevents accidental data loss if the wrong signals are fed to the memory.

Basically, packaging consists of a bubble memory chip surrounded by two orthogonal coils. The coils, sandwiched between two permanent bias magnets, provide nonvolatility and stable domains. This entire grouping is then enclosed in a magnetic shield to prevent external magnetic fields of up to about 20 Oe from affecting the data. The bubbles, being magnetic dipoles, interact strongly and must be separated from each other by several bubble diameters. In practice, a spacing of four bubble diameters (center to center) minimizes this interaction. Bubble diameter, however, is a function of material composition and applied bias field strength at a given temperature.

A magnetic bubble memory needs various circuits to operate as a complete memory system. These circuits include a controller to provide a central processing unit interface and to generate enable pulses for a function timing generator, coil and function drivers, and a sense amplifier to increase the bubble detector signal. As a high level interface between the microprocessor and the bubble memory, the controller performs parallel to serial conversion from microprocessor to bubble memory, and serial to parallel conversion from bubble memory to microprocessor. Primary controller functions are to stop and start bubble movement, maintain page position, and raise or lower flags for such bubble memory functions as generate, swap, block replicate, and redundancy replicate. Control signals from the controller are sent to the function timing generator-a monolithic integrated circuit (IC) that provides the precise timing signals necessary to operate the function driver, coil driver, and sense amplifier during each field cycle. The function driver circuit converts TTL level signals from the function timing circuit into current pulses required by the bubble memory control elements. The coil driver circuit and diode array produce the rotating magnetic field by generating currents with triangular waveforms in the bubble module coils. The coil driver receives TTL inputs from the function timing generator and produces a higher level driving voltage. The coils integrate this voltage into a ramping current that produces the desired triangular waveforms.

The sense amplifier receives voltages from the detector that are too small to be directly useful in the system. The bubble signal is amplified, level detected, and latched by signals provided by the function timing circuit. Data output is then coupled to the MOS controller.

Although bubble technology scores high on adaptability, it differs in this respect from IC memories. Partitionability is about the same, but garnet chips carry more bubbles. Lower defect densities, smaller cells, and simpler processes allow economical integration to levels higher than are possible with silicon. Logic, memory, and switches can be intermixed on a finer scale within the garnet because no restructuring is needed. Bubble serial bit speed is slower, about 1 μ s, but system throughput may approach that of the highest speed silicon RAMS, where associative and parallel processing can be used.

Magnetic bubble memories combine most of the outstanding capabilities of solid state and mechanical magnetic storage; however, they perform better against some of these competing technologies than against others. In comparison with fixed head and floppy discs, bubbles have higher reliability and lower error rate since they employ no moving parts. Other assets are faster access time, lower power consumption, smaller physical size, simple interfacing, and lower entry price all resulting from the elimination of mechanical elements. Data transfer rates are lower than those of fixed head discs, though, and their per bit cost at present is much higher than that of floppy discs, except in small systems.

A comparison with semiconductor memories is somewhat indirect since bubbles will probably work in conjunction with RAMS. Due to dramatically better access times, higher data transfer rates, and simpler interfacing requirements, RAMS will hold their ground as main memory, transferring data into and out of bubble storage. In relation to charge-coupled devices (CCDS), bubble chips have the advantage of nonvolatility and high packing density, but suffer from slower access times and slower data transfer rates.

Presently, the Texas Instruments (TI) 92k-bit TIB0203 and 254-bit TIB0303, the Fujitsu 64k FBM31DB/ FBM32DA and 256k FBM42DA/FBM43DA, the Intel 1M-bit 7110, and the Rockwell RBM256 256k-bit magnetic bubble memory device and support circuits are commercially available, reflecting a similar frenzied development/production pace previously encountered in static and dynamic MOS RAMS. Storage of 1M bits on a single chip is a significant achievement since it paves the way for very high density but small size memory system development. This certainly is the beginning of a new era in data storage applications and system design.

In September 1979, TI introduced its new family of 256k, 512k, and 1M-bit magnetic bubble circuits that share packaging and semiconductor support circuits. The strategy is to offer a family of physically and electrically interchangeable bubble memories for easy system upgrading and maximum flexibility. Based on 2-um diameter bubbles and using a block replicate structure, the TI devices are organized differently than the Intel 1M-bit device. With an access time of 11.2 ms, the binary 1M-bit device (TIB1000) is organized as 512k x 2, while the 512k-bit device (TIB0500) has a 512k x 1 organization. Initially, these TI products will be offered only as fully assembled memory boards, such as Intel offers. In addition, the National Semiconductor 256k-bit NBM2256 will be sampled in early 1980. Furthermore, NEC, Motorola, IBM, and Western Electric are developing magnetic bubble circuits and memory systems.

Table 2 summarizes both current and expected magnetic bubble memories. Table 3 summarizes various parameters of magnetic bubble memories and compares them to available 64k CCDs. The CCDs exhibit lower power dissipation and faster drive speed. In 1981 to 1982, TI and Rockwell should announce 1M-bit magnetic

Manufacturer	Part No	Capacity (Bits)	Organization	Package (Pins)	Available
Fujitsu	FBM32DA	64k bits	Major/minor	18	Yes
	FBM31DB	64k bits	Serial	18	Yes
	FBM43DA	256k bits	Maj/min block rep	20	Yes
	FBM42DA	256k bits	Major/minor	16	Yes
Intel	7110	1M bits	Maj/min block rep	Leadless	Yes
National	NBM2256	256k bits	Maj/min block rep	16	Early 1980
Rockwell	RBM256	256k bits	Maj/min block rep	18	Yes
		1M bits	Maj/min block rep	18	Yes
Texas	TIB0203	92k bits	Major/minor	14	Yes
Instruments	TIB0303	254k bits	Maj/min block rep	28	Yes
	TIB1000	1M bits	Maj/min block rep	24	Yes
	TIB0500	512k bits	Maj/min block rep	24	Yes
	TIB0250	256k bits	Maj/min block rep	24	2nd Qtr 1980
Motorola*	RBM256	256k bits	Maj/min block rep	18	Late 1980
Siemens*	RBM256	256k bits	Maj/min block rep	18	Late 1980

TABLE 2 Magnetic Bubble Memory Availability Summary

*Second source to Rockwell RBM256

TABLE 3 Magnetic Bubble Memory and CCD Chip Characteristics

		Storage Capacity*	Average	Max Transfer	Power	Standby
Manufacturer	Part No	(bits)	Access Time	Rate (bits/s)	(W)	Power
Magnetic Bubble N	lemory Chips					
Texas	TIB0203	92k	4 ms	50	0.7	N/A
Instruments	TIB0303	254k	7.3 ms	100	0.9	N/A
	TIB0250	256k (256k x 1)	5.6 ms	100	1.2	N/A
	TIB0500	512k (512k x 1)	11.2	100	1.2	N/A
	TIB1000	1M (512k x 2)	11.2	100	1.2	N/A
Rockwell	RBM256	256k	4 to 6 ms	100	0.82	N/A
National	NBM2256	256k	7 ms	100	0.75 typ	N/A
Intel	7110	1M	40 ms (50-kHz shift rate)	†	1.9	0.29 W
Fujitsu	FBM31DB	64k	370 ms	100	0.5	N/A
	FBM32DA	64k	4.5 ms	50	0.5	N/A
	FBM42DA	256k	8.5 ms	50	0.67	N/A
	FBM43DA	256k	6.0 ms	100	0.67	N/A
Charge-Coupled Do	evices					
Texas Instruments	TMS3064	64k	410 µs	5M	0.26	26 mW
Fairchild	F464	64k	410 µs	5M	0.34	66 mW

* Effective capacity is normally higher due to extra loops/bit in case of nonfunctional loops/bit. †Max data rate is 100 kHz (active is 78 kHz); R/W time is 6.5 μ s.

N/A-Not applicable

bubble memories, followed by similar devices from National Semiconductor. Bubble diameter decreases to 1 μ m by 1985 will enable 5M- and 10M-bit magnetic bubble memories.

CCD Memories

CCDs are low cost alternatives for bulk storage applications, filling a void between magnetic memories and semiconductor RAMS. While CCDs are volatile semiconductor storage devices, they are not likely to compete with RAMS. However, CCDs have benefited from fabrication techniques developed for MOS RAMS and are manufactured by the same production facilities.

Architectures, processes, and clocking schemes all affect CCD characteristics. Three major architectures, each having its own cost/performance tradeoffs, are serpentine, line addressable RAM (LARAM), and serialparallel-serial (SPS), as shown in Fig 4. Serpentine or synchronous is the simplest organization; this architecture has a wide operating frequency range. Additional parameters are good density, high power, high clock loading, and average latency. LARAM is a combination of CCD and RAM architectures. While this type has low power dissipation, low clock capacitance, and excellent latency, it lacks the high density required for low cost. Its frequency range is also limited. SPS is the best organization for high density, because serial to parallel and parallel to serial conversions involve clocking the cells in different directions, and it needs little overhead logic. While SPS has lower power dissipation, it also has limited frequency range and poor latency.

Charge coupling is the process by which mobile minority charge carriers are collectively transferred from one semiconductor storage element to a similar, adjacent

Operat Temp (ring Packaging PC) (Pins)	Onchip ECC	Second Source	Available Support
0 to 5 0 to 5 0 to 5 0 to 5 0 to 5	$\begin{array}{cccccccccccccccccccccccccccccccccccc$	No No Yes Yes	None None None None	Controller chip, coil driver, sense amp, function driver, function timer TIB0902/0903/0904 controllers, 0953/0954 function time gen, 0863/0864 read function gen, 0883/0884 write function gen, 0804 coil driver, 0923/0824 duel-channel amp
-10 to 7	(1.3 x 1.4 x 0.37) 70 18 (1.2 x 1.2)	No	Motorola Siemens	Controller board, magnetic bubble memory board
0 to 7	70 16 (1.2 x 1.1 x 0.36)	Yes	None	Not yet available: INS82851 controller, DS3615 function driver, DS3616 coil driver, DS3617 sense amp
0 to 7	70 20 Nonstandard (1.7 x 0.43)	Yes	None	7220 controller, 7242 SA/formatter, 7230 current pulse gen, 7250 coil predrivers, 7254 quad transfer packs
0 to 5	5 18	Yes	None	
0 to 5	(1.22 x 1.1 x 0.433) 55 18 (1.22 x 1.1 x 0.394)	Yes	None	Complete memory cards up to 32k bytes;
0 to 5	5 16 (1.22 × 1.1 × 0.204)	Yes	None	no individual support circuits
0 to 5	5 20	Yes	None	
0 to 7	0 16	No	NEC	Not required
0 to 5	5 16	No	Motorola	Not required

storage element by manipulating the external voltage. Information in each element is represented by the amount of electrical charge present. The storage elements are interconnected through the substrate, reducing space requirements.

The first commercial CCD, introduced in 1975 by Fairchild, was a 9216-bit device whose simple architecture demonstrated the feasibility of the CCD memory concept, in which regions of charge move. Subsequent architectural advances, while boosting density and performance, were expensive in the long run. More recently, high volume RAM and CCD manufacturing technologies have merged, and the viability of now familiar fabrication techniques made production of a dense, low cost, bulk storage device possible. By 1978, CCD memory chip capacity increased sevenfold to 64k bits.

In the Fairchild 64k dynamic CCD, bits are organized as 64k x 1 in 16 randomly accessible SPS shift register blocks of 4k bits each. Four TTL compatible address inputs are provided to select one of 16 blocks for read/ write or read only operation. Each block is implemented with an interlaced SPS structure in which each serial input register stores 32 bits, using 64 electrodes that service 64 parallel shift registers. In conventional (noninterlaced) SPS structures, each serial shift register bit serves only one parallel shift register. The interlaced SPS structure doubles packing density, and an 8-phase ripple technique shifts data in the parallel registers at a rate almost twice the speed of 2-phase systems.

Prior to 1978, the interest in CCDs, because of their bit density, was high and a proliferation of products was available. CCD memories were intended for applications involving data storage in large blocks where access times of 100 μ s or so could be accepted. However, this intention has changed. The advent of the 64k dynamic



Fig 4 CCD architectures. Major types of CCD approaches comprise serpentine, serial-parallel-serial, and line addressable random access. Serial-parallel-serial has higher density and lower power than either of other two

n-channel MOS (NMOS) RAM and its performance, density, and cost implications coupled with CCD processing and design problems that result in lack of product availability, has led many companies to switch their next generation systems design from CCDs to MOS RAMS. This has virtually signaled the demise of the CCD as a widespread memory component. National, Intel, Motorola, and others have already ceased CCD memory efforts. Actions of the remaining CCD suppliers (TI and Fairchild) are to support a limited select application base and not to solicit new areas.

However, things do not remain static in the semiconductor industry very long. IBM announced that it has produced experimental 256k CCD memories. This may be the impetus required to elicit an interest in CCD devices again, because IBM has recently gone to the commercial market (16k and 64k dynamic RAMs) to supplement its own manufacturing capability. Whether this will cause a revival by semiconductor manufacturers of commitments to CCD technology remains to be seen.

Siemens is also designing a 256k CCD memory and Hitachi has had a 262,144-bit CCD memory in research and development for the past two years. The IBM announcement may pave the way for commercial devices by the second quarter of 1980. Thus, the 256k level will be the crucial focal point.

While magnetic bubble memories represent the future and highest form of data storage possible at the lowest potential cost per bit, the future of CCDs—forecast as the panacea of bulk storage support—is dim. The only possibility of saving CCD as a viable technology would be the introduction and production of a 256k-bit CCD in late 1980. Whatever IBM chooses to do will determine the future of CCD memories.

Josephson Junction Circuits

Due to increased emphasis on subnanosecond logic by mainframe computer manufacturers, future generations of computers (ie, super computers) might well utilize superconducting Josephson junction circuits.* These circuits are based on cryogenic operation at near absolute zero temperature (-273 °C).

The theory of Josephson junctions centers primarily on four physical properties:

(1) Certain materials, known as superconductors (for example tin, lead, and niobium), when cooled to a temperature a few degrees above absolute zero (-273 °C), lose all resistance to the flow of electric current. If current is made to flow in a loop or ring of such material, it will flow continuously.

(2) Magnetic flux cannot penetrate an "ideal" superconductor because shielding supercurrents are set up to oppose external magnetic fields. Consequently, magnetic flux can be trapped in superconducting rings, where it threads through a hole in the ring and is linked with persistent circulating currents in the ring.

^{*}This section is partially excerpted with permission from "Computing at 4 degrees Kelvin," W. Anacker, *IEEE Spectrum*, May 1979, pp 26-37.

(3) When a material becomes superconducting, it forms a macroscopic quantum mechanical system of paired electrons, called "Cooper pairs," which react in unison to external electrical and magnetic disturbances and account for all superconducting properties. The electrons participating in the pairing process are taken from the electron population of the metal and leave behind a "superconducting energy gap" in the electron energy spectrum of that metal.

(4) If two superconducting materials form a junction with a very thin oxide layer (about 40 Å thick) sandwiched in between, the oxide, normally an insulating barrier, allows a current to flow by a tunneling mechanism.

Although still in its infancy, Josephson junction technology has now reached the level where the capability for total digital computer technology—that is, for constructing all digital logic and all necessary memories, both large and small—is within reach. This technology has already succeeded experimentally in implementing and verifying four basic logic elements: OR, AND, invert, and LATCH.

In contrast with the voltage driven logic of present semiconductor circuits, Josephson junction logic circuits are current-driven elements. When inputs of more than one logic circuit are to be connected to a single circuit output (fanout), their control lines are incorporated serially along the output lines. The control lines, or fanout sections, constitute inductive discontinuities in the output line. When properly matched to the line impedance, these discontinuities transmit the output signals unaltered but with additional delay. The fanout delay curtails the otherwise unlimited serial fanout capability of Josephson junction circuits in accordance with total permissible delays. When properly designed, each fanout contributes about 5 ps to the signal delay along the output line.

A special capability of Josephson junction logic circuits is that they operate in a latching mode. They must, therefore, be periodically reset and then reactivated. Applying trapezoidally shaped voltage pulses to the voltage bus, with the leading edge of each pulse activating all circuits connected to the bus, accomplishes this. Logic functions are carried out during the time the trapezoidal pulses are fully established; resetting of the switched circuits is accomplished by the trailing edges of the pulses.

Since Josephson junction circuits operate equally well with positive and negative gate and control currents and voltages, the positive and negative trapezoidal voltages can be alternated. This circuit capability leads to an ac power supply for Josephson junction circuits sinusoidal generators that produce alternating trapezoidal voltage-pulse sequences. The generators operate at room temperature in conjunction with integrated thin-film transformers and voltage-clipping Josephson regulator devices arranged on chips. Typical strings of four Josephson switching devices connected between the voltage bus and ground are integrated on the chip to form the ac power regulators. Current thresholds of these regulators are virtually suppressed for this application, so that they clip the sinusoidal voltage amplitude at about 10 mV and thus provide the desired alternating trapezoidal pulse sequence.

Storage of binary data in memory cells relies on the phenomenon of trapping magnetic flux in a superconducting ring, which permits a persistent circulating current to flow. As long as the ring remains entirely superconducting, the amount of magnetic flux threading the hole of the ring cannot increase or decrease. Magnetic flux can be admitted or released, however, when the superconducting path is interrupted somewhere in the loop with a Josephson switching device.

Under development are two types of RAM cells: a nondestructive readout (NDRO) cell for use in ultrafast access arrays, and a memory cell for high density arrays designed to operate in the destructive readout mode. Memory cells, drivers, and decoders needed for the construction of a fast RAM array have already been experimentally evaluated, and decoder delays of 30 ps/stage have been measured. These and other results support the estimation that NDRO memory arrays, with 2048 bits, approximately 1-ns access time, and 2-ns cycle time, can be fitted on a chip area of 6.4 x 6.4 mm. Chip power dissipation will amount to about 5 mW. Current semiconductor memories with comparable density exhibit about 20 times longer access times and dissipate about 1000 times more power.

An experimental high density memory array, comprising about 2000 cells, has been operated in write and read modes with only about 10 ns of total delay through decoder, driver, array, and read circuits. Estimates from this experiment indicate that 16k-bit arrays with about 15-ns access and 30-ns cycle times can also be arranged on 6.4 x 6.4-mm chips. Power consumption of these arrays is extremely low. Onchip standby power is zero while data are being stored, and dissipated power is 40 μ W (including power consumed in peripheral circuits) when the array is operated at full speed. Low power levels of peripheral, driver, decoder, and logic circuits are obtained by use of loop logic-switching devices connected to superconducting loops rather than to terminated transmission lines. Logic and decoder operation is slower in this case, but still fast enough for access times on the order of 10 ns.

Despite fundamental differences in physics and mode of operation between Josephson junction and silicon devices, processing tools and procedures for Josephson large scale integration (LSI) chip fabrication are similar to those used in semiconductor LSI technology. In principle, photo and electron beam lithography techniques are the same, even though different materials, multilayer structures, and permissible temperature profiles may require adaptation of process parameters. Thin-film deposition by evaporation and sputtering is relied upon in both technologies, although perhaps to a larger degree in Josephson junction technology. Other process steps, such as ion implantation, high temperature diffusion, and epitaxial deposition, are not needed. Unique to Josephson junction technology is the preparation of tunnel barriers.

Josephson junction circuit chips are typically made of silicon wafers, chosen for their compatibility with microcircuit processing procedures, not for their semiconducting properties. A typical Josephson LSI "vertical" structure on a wafer may comprise about ten thin-film layers—four superconducting, four insulation, one resistive material, and, of course, tunnel barriers.

The IBM Thomas J. Watson Research Center has developed a high speed Josephson junction technology called current injection logic (CIL). The experimental CIL family consists of 2- and 4-input OR gates and 2- and 4-input AND gates. Experimentally measured logic delay averaged over four gates is claimed to be 30 ps/gate (an average fanin of 4.5 and an average fanout of 2.5). Average power dissipation for the family has been measured at 6 μ W, while that of the 2-input OR gate has been measured at 2.6 μ W. Previously fabricated Josephson junction circuits of comparable geometries (5- μ m diameter Josephson junctions and 2.5- μ m minimum linewidths) exhibited average switching delays of 60 ps—twice as long as the average numbers for CIL devices.

The CIL family is based on two types of superconducting devices. A magnetically controlled 3-junction interferometer, which provides isolation through magnetic coupling, is used for the 2-input OR function; a direct coupled, current injection gate is used for gain and as a 2-input AND function. The interferometer has been used in previous Josephson junction circuits, but in this case, it has been optimized for a large operating margin on the control current.

Areas that require much additional work in implementing Josephson junction technology are applying logic circuit design techniques to LSI circuits; developing and implementing LSI circuit design guidelines; investigating physics of materials and fabrication processes; producing suitable packaging to allow operation at cryogenic temperatures, while not degrading subnanosecond access/cycle times; maintaining cryogenic temperatures continuously and reliably; evolving mainframe construction techniques for handling cryogenic environment (liquid hydrogen) and associated heat transfer; and developing connections able to maintain picosecond switching speeds. The potentially high reliability of the cryogenic environment may eventually allow the construction of extremely large (multiprocessor) mainframes with perhaps millions of logic circuits, billions of memory bytes, and computing power on the order of 109 instructions per second, if the need exists and adequate auxiliary storage and I/O devices can be provided. Characteristics of such a proposed super computer are listed in Table 4.1

TABLE 41

Mainframe Characterist Computer Using Josephson Attribute	ics of Hypothetical n Junction Technology Value
Performance	70M instructions/s
CPU cycle time	4 s
Cache capacity	32k
Main RAM capacity	16M bytes
Cache access time	4 ns
Main RAM access time	20 ns
I/O data rate (max)	360M bits/s
Power at 4 °K	7 W
Power at 300 °K	15 kW
Volume of mainframe	4 liters
Volume of cryostat	460 liters

The cost per circuit of Josephson junction and semiconductor LSI with comparable dimensions is similar because circuit density, process complexity, and chip yield can be expected to be similar. Overall performance lead of Josephson junction technology over analogous LSI semiconductor technology is currently estimated to be ten- to twentyfold, and there is no reason to believe that this advantage will be substantially reduced in the future. Hence, a cost/performance advantage results for Josephson junction technology.

Technology aspects—not performance or cost/performance—are most likely to influence whether Josephson junction computer designs will reach the marketplace. The technology data base assembled thus far is still small. It is not yet known how long it will take and how much it will cost to understand and control materials and fabrication processes well enough to produce commercial Josephson LSI computer hardware. However, because of the tremendous amount of development effort being spent on Josephson junction devices, commercially available products should be offered by 1985.

Gallium Arsenide LSI Circuits†

Semiconductor technology has been dominated by devices made from silicon. The industry has progressed from the single transistor to the IC to large scale integration of thousands of devices on a chip. The widespread use of silicon ICs has been driven by the achievement of about twice as many operational functions per chip each year, at a lower cost per function. As a result, applications of silicon LSI chips are growing prodigiously, and a new revolution in the form of very large scale integration (VLSI) is possible, with systems or subsystems placed on a single chip.

In the background of the silicon LSI/VLSI revolution, gallium arsenide (GaAs) is quietly gaining momentum. It could possibly become the first major "second wave" beyond silicon technology, with potential gigabit circuitry having gate switching times of less than 100 ps and dynamic switching energies of less than 0.1 pJ. Consequently, GaAs is of great interest for its VLSI potential.

Application of silicon ICS, particularly LSI chips, has been limited to low data rates and has not invaded the microwave regime (Fig 5). Various silicon IC technologies, including complementary MOS/silicon on sapphire, NMOS, and ECL (bipolar), generally have gate propagation delays of 1 ns or more. Except for small scale ECL (eg, high speed prescalers), clock rates and function execution times are well under a gigabit. In contrast, GaAs digital ICs made with depletion-mode metal semiconductor field-effect transistors (MESFETS) and Schottky diodes have demonstrated gate propagation delays of less than 100 ps, breaking the gigabit barrier and moving directly into the microwave area. The low power, high speed advantage of GaAs MESFET ICs stems directly from the high electron mobility and

[†]This section is partially excerpted with permission from F. A. Blum, "Gigabit Logic: Prospects for GaAs LSI," *Microwave Systems News*, Feb 1979, pp 57-63.

semi-insulating substrate of the GaAs MESFET, which gives it high transconductance and unity current gain bandwidths of approximately 80 GHz for 1- μ m gate devices (compared with about 12 GHz for a similar silicon MESFET). Of course, these same properties are the basis for the current attention given to the development and use of discrete microwave GaAs fieldeffect transistors (FETs).

Since the principal advantage of GaAs is its high electron mobility, a feature best exploited in a majoritycarrier device technology, most GaAs IC efforts have been based on the use of n-channel FETs of various types. Fig 6 summarizes the various GaAs device types and circuit technologies that have been modeled, fabricated, and investigated. Of these, the Schottky diode-FET logic (SDFL) structure, which uses high speed Schottky diodes for most logic functions, and low power depletion mode MESFETs for inversion and gain hold much promise for LSI circuit application. SDFL achieves speeds $(t_d = 75 \text{ ps})$ close to those of buffered FET logic (BFL) at much lower power levels ($P_D = 200 \ \mu W$ to 2 mW/gate), promoting chips of much higher complexity. SDFL does, however, require a more sophisticated fabrication approach in order to optimize both diodes and FETS.

Two independent studies by Rockwell's Science Center and IBM's Thomas J. Watson Research Center project just what the speed advantage will be if LSI circuits are fabricated on GaAs instead of silicon, using MESFETS. Although the research is tackled differently—IBM uses computer simulations for its projection while Rockwell



Fig 5 Speed/power performance of IC technologies.² Map of gate propagation delay vs power dissipation shows advantages of low power, planar GaAs MESFET logic compared with Si technologies

bases its projection on actual device measurements both arrive at the same answer: all things being equal, GaAs MESFET LSI circuits exhibit a sixfold speed advantage over silicon MESFET circuits for the same powerdelay product; GaAs circuits exhibit a 25 to 40 times lower power dissipation than silicon for the same t_d ; and GaAs ICS operate up to 200 °C without changes in t_{AA} or P_D .

Gate delays and power-delay products of the enhancement-mode MESFETs are orders of magnitude better than those of today's n-channel transistors—but the devices are formed with gate widths of 1 μ m and less. For 1-V logic swings, Rockwell expects gate delays of 60 ps and power-delay products of 35 fJ in its 1- μ m MESFET technology. The Rockwell GaAs program has an aggressive goal of putting no fewer than 1000 gates on a GaAs substrate within two years, and integration certainly will not stop there.

Rockwell has fabricated and tested long chains of NOR gates, chains of D-flipflops, and other medium scale integrated (MSI) circuits. Examples include a 24gate, 3-stage binary ripple counter (divide by 8) implemented with T connected D-flipflops, and a 33-gate. 3-stage synchronous counter. Power dissipation per gate for these MSI circuits has been running in the fewmilliwatt range, somewhat higher than that of the ring oscillators due to higher supply voltage requirements (approximately 3 V). However, the speeds have been maintained. For example, the first stage divide by 2 of a ripple counter has been operated at clock frequencies of 1 to 2 GHz, implying gate switching times of approximately 100 ps. The few-milliwatt power dissipations yield PDtd's of a few hundred femtojoules per gate, which is much lower than that achieved with BFL. Finally, complete 8:1 data multiplexers and demultiplexers containing approximately 60 gates have been fabricated, as has a 93-gate array. MSI GaAs circuits are the largest ever fabricated and represent a significant step toward demonstrating LSI chip operation. In April 1980, a 2 x 32 shift register containing 532 gates should be available.

While performance results achieved for GaAs TCs have been outstanding, there has been some disagreement about these results, with some ascribing them principally to the 1- μ m geometries and semi-insulating substrates used in GaAs IC work, rather than to superior GaAs electronic properties and FET characteristics. It is extremely important to note that the GaAs devices that have been fabricated to date use 1- μ m geometries, while scaled NMOS uses 2.0- to 3.0- μ m line geometries and bipolar uses a 3.0- to 4.0- μ m geometries (although TRW's high performance triple-diffused process is fabricated with 1.5- μ m geometries).

However, a comparison of experimental data on short channel GaAs and silicon FETs² shows that for any given $V_{\rm gs} - V_{\rm p}$ bias, the saturated drain current and transconductance values for the GaAs MESFET are at least six times larger than the values for the silicon MESFET. These transconductance characteristics are also reflected in superior microwave properties (gain, noise figure, etc) for GaAs MESFETs.

GaAs MESFETS give much better performance characteristics, particularly at low biases, than silicon FETS.



* VOLTAGE SWING LIMITED BY GATE CONDUCTION

** WORK IS AT VERY PRELIMINARY STAGE TO QUOTE RELIABLE RESULTS

Fig 6 GaAs IC hierarchy. Most models which have been probed are based on n-channel FETs to achieve high electron mobility

For any given logic voltage swing (or $P_{\rm D}t_{\rm d}$ product), the GaAs MESFET IC will be over six times faster than the silicon MESFET circuit. On the other hand, if equal propagation delays are demanded from both circuits, the GaAs device can achieve the speed with much smaller logic swings and hence enormously lower speedpower products than the silicon IC. This is, of course, extremely important for high speed VLSI applications.

To date, the performance attained with GaAs ICs has been excellent. However, the most serious concerns about the future of GaAs, particularly for LSI and VLSI applications, are focused on the questions of producibility and yield. On the basis of silicon IC experience, it seems unlikely that LSI circuit complexities could be achieved with mesa GaAs IC fabrication approaches. In addition, the single layer (epitaxial or uniform implant) available with these techniques also results in some restrictions in circuit approach. More recently, a fully planar GaAs IC process making use of multiple localized implantations directly into a semi-insulating GaAs substrate has been developed which avoids these problems. Because multiple implantation steps make it possible to optimize more than one type of active device with this process, it has been extensively used to fabricate SDFL type circuits.

Attainment of LSI or VLSI circuit complexities in high speed logic requires low gate dissipations and hence ultralow $P_{D}t_{d}$ products. This implies relatively low logic swings with relatively low pinchoff voltage MESFETS, if depletion-mode logic is used. The FET pinchoff voltage must be controlled to a small fraction of the logic swing, the achievement of which has proven quite difficult in GaAs MESFETS, due to the extremely thin (1000 Å) active layers involved. Also, MESFET drain currents must be reasonably well matched for optimum circuit function.

As mentioned before, the goal of the current Rockwell program is to demonstrate the operation of approximately 1000-gate LSI parts within two years. While this is aggressive, very significant progress has been made in the past two years and the basic LSI compatible process technology and circuit design techniques have been demonstrated. LSI GaAs is clearly on the horizon. Roadblocks in both the processing technology and the quality of semi-insulating GaAs substrates are expected; the main obstacle will be the smooth transition from current 93-gate parts through 523-gate parts to 1000gate parts.

With the proper resources and effort, these goals and more would seem to be in the offing for the 1980s. Apparent extensions of GaAs digital LSI technology are development of analog circuitry and combinations of analog and digital circuitry. While the performance demands of analog circuits can be stringent indeed, the technology being developed should lend itself nicely to refinement for analog applications. The recently demonstrated GaAs CCD would complement the digital technology for such applications as high speed filtering. Also, high speed analog to digital (A-D) converters made from GaAs will certainly attract the interest of many systems engineers. Possible combinations of silicon and GaAs on the same circuit substrate are also foreseen.

Once GaAs enters the LSI stage, VLSI lies around the corner, presuming that material quality and processing technology can keep pace. Performance-wise, improvements in the technology will push GaAs toward the lower lefthand corner of Fig 5, and femtojoule GaAs ICs would seem to be a real possibility. This can be achieved in two ways. First, capitalizing on the current development of submicron device technology using electron beam and/or x-ray lithography, shorter FET gate lengths (0.25 to 0.5 μ m) can be employed to bring switching times into the 10- to 20-ps range. Indeed, a high power, buffered FET inverter with 0.5-µm FET gate lengths was recently operated by Hughes with a 34-ps switching time. Alternatively, cryogenic cooling of GaAs ICs may be acceptable for such applications as mainframe computers. Bulk n-type GaAs can have mobilities in excess of 100,000 cm²/V-s at liquid nitrogen temperature. If FET channel mobilities close to this value can be achieved on a reliable basis, the devices would be extremely fast. Indeed, a combination of submicron geometries and low temperatures could yield ICs with properties rivaling those of Josephson junction circuits, which currently have much more formidable requirements of operation at liquid helium temperatures.

Besides Rockwell, the list of companies investigating this technology is impressive: Texas Instruments; Lockheed Space and Missile Systems Div anticipates development of smart satellites using superspeed processing of GaAs LSI; Hewlett-Packard has opened a small pilot or prototype line at Santa Rosa, Calif, for MSI circuits to be used in counters; and TRW Defense and Space Systems Group continues work with A-D converters that may find application in 60-GHz spread spectrum links, or in a radio on a chip used for sophisticated pseudonoise coded signals in air to air missile guidance.

Even with the existing performance demonstration, skepticism exists. To become a proven entity, GaAs technology must move from the laboratory to the production line. Within the next five years, the true potential of digital and analog GaAs ICs should become clear.

Summary

The microprocessor is creating a demand for more semiconductor memories—programmable read only, read only, and random access memories. Further increasing the impetus for high density RAMS (4k, 16k, 64k, and greater) is the replacement of core memory with semiconductor memory in computer systems, which began in 1976. Within the next several years, the merging and coalescing of bipolar and Mos technologies for RAMS should take place.

A wide and diverse base of semiconductor memory elements exists from which designers may select to meet application objectives. It is from this grouping that the next generation of semiconductor memories will be derived, thus providing the impetus for the super computer. The future will see the memory categories discussed in Parts 1, 2, and 3 implemented with VLSI technology. As such, the need for submicron technology with onchip fault tolerance, built-in test, and error detection and correction will be common to all.

A rational prediction has been attempted as to the new products in each memory category that will become available, and the timing as to when this will occur. Many factors have entered into these projections which are achievable if certain designs, processes, and support equipment requirements are met. The type of memory technologies that will find widespread use in super computers are ECL, scaled MOS, magnetic bubble, and Josephson junction devices. In the long term, the fastest access times will be found in technology based on insulating substrates, such as GaAs.

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Benefits and Limitations of Wire Matrix Printer Technology

Serial matrix technology is steadily evolving to satisfy medium speed line printing and high quality word processing applications

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R ecent serial wire matrix printer developments are producing line and character speeds of 300 lines/min and 600 char/s, respectively, with the reliability for print volume applications previously dominated by medium speed line printers. Parallel developments are demonstrating print quality equaling those of daisy wheel and inkjet technologies.

The first matrix printer, introduced in 1970, operated at approximately 66 char/s. Shortly afterward, a 165char/s serial matrix impact printer appeared. These first wire matrix printers used solenoid wire drivers with the stylus directly attached to the solenoid armature.

Development of free flight and ballistic printheads improved heat efficiency and doubled printhead life, achieving print speeds of 180 to 200 char/s. Development of a stored energy printhead further improved efficiency and head life, increasing print speed to more than 250 char/s. Use of a double column of wires vertically offset from each other increased print speed to more than 300 char/s. Recently, development of magnetic stored energy wire drivers has boosted print speed to 600 char/s. Ongoing technology developments will continue to achieve significant gains in performance.

The emerging demand for systems supporting both data processing and word processing applications will challenge printer manufacturers to offer multi-utility printers that will satisfy both requirements in one printer. The advantages of technological maturity, multi-part printing, low cost, and manufacturing experience should give serial wire matrix printers the competitive edge over inkjet and laser print techniques for the next several years.

Speed Considerations

Serial wire matrix printers use a printhead that moves horizontally across the paper (Fig 1). Actual printing is accomplished by actuation of various combinations of wire hammers that are configured in a vertical column. Each wire, when activated, impacts the end of the associated wire into an ink ribbon and onto the paper to create a single dot. Each

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character is formed by firing the wires at selected intervals, forming a dot matrix array.

Primary factors determining maximum print speed of a wire matrix printer include maximum wire cycle rate, number of wire sets per printhead, and number of printheads. The majority of existing wire matrix printers use a solenoid wire actuation technique to drive the wire onto the paper. Maximum cycle rates for solenoid actuators are approximately 1000 cycles/s, or 180 to 200 char/s, for standard printing.



Actual throughput of a serial matrix printer is also a function of the line length to be printed. Since the printhead is moving at a constant velocity, the time to print a line is directly dependent on the length of the line. Short lines take less time to print than long lines. However, the curve is not exactly linear because of the additional time required to feed the paper and to reverse printhead direction.

Use of more than one printhead increases print speed and throughput. Two printheads can share print load of a line by dividing the paper form in half with each printing its respective half. Multiple printheads can reduce the effective line length for each printhead and, thus, the time to print a line. However, this technique is only effective for long lines. For example, a serial matrix printer at 150 char/s with a printhead velocity of 15 in (38 cm)/s can print a full line of 132 ten-pitch characters in 0.88 s. Two printheads, each printing 150 char/s and moving at 15 in (38 cm)/s but printing one-half of the line, can print the line in 0.44 s. If the lines to be printed are only 66 characters in length, the time to print is 0.44 s for both a single- and dualhead printer since the second head never has data in the second half of the page to print. Thus, the extra throughput speed of two printheads is only effective with lines longer than one-half the page width. Mechanical complexity and added cost have generally eliminated this approach from current developments.





The use of two sets of vertical wire elements in one printhead can increase effective print speed by almost a factor of two (Fig 2). A matrix printer with two sets of vertical wires using solenoid wire actuators can achieve over a 300-char/s print speed. Each wire set operates at a maximum cycle rate and alternates the printing of each dot column of the matrix. Because the two wire sets are in one printhead, the advantage of higher throughput is independent of line length.

Recent developments in magnetic stored energy wire actuators have enabled wire cycle rates to exceed 3000 cycles/s, a speed that translates into 600 char/s or more than 400 lines/min for average width text. The stylus wire is attached to a cross flexure spring that is held in a cocked position by a magnet (Fig 3). A coil is energized to cancel the magnetic field, releasing the spring and achieving wire flight times as short as 180 µs. More efficient magnetic materials, such as samarium cobalt, have reduced the weight of these printheads, and the efficiency of the stored energy hammer has reduced the power dissipation by a factor of four over solenoid actuators, thus extending life.

Print Quality

The main drawback in present matrix printer design is the quality of the printed characters. Generally, a dot matrix of $5 \ge 7$, $7 \ge 8$, or $7 \ge 9$ produces a character with noticable gaps between the dots, and character shapes are limited by the points on the grid at which a dot can be placed. New developments, using higher resolution dot densities and more precise location of dots, have alleviated these deficiencies.

Print quality, a measure of appearance and legibility, depends on such variable factors as printer technology, ribbon, paper, and subjective judgement. The de facto industry standard of high quality or word processing quality print is the output, with carbon or film ribbon and bond paper, of a maintained daisy wheel or IBM Selectric printer. These printer types form solid characters from an engraved ball or daisy wheel impacting the paper through the ribbon. This benchmark of quality has been



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reduced slightly with the acceptance of the IBM inkjet, using ink dots to form characters, as acceptable word processing quality.

Matrix printers generate high quality print by placing dots on paper exactly and accurately. The dot diameter of these printers varies from 0.010 to 0.020" (0.254 to 0.508 mm). The smaller the dot, the more dots are required to form a solid character, while allowing higher resolution print. Exact dot location is a difficult printing parameter and is essentially the limiting factor of matrix printer resolution.

Some problems in dot placement are due to the requirement of precise paper motion and position control. The major problem is controlling the location of the dot impact. Since the printhead is moving horizontally while printing, dot position must be determined by actuating the wire and anticipating its impact on the paper. Wire flight times may vary due to mechanical tolerances, and interaction of wire actuators for one or simultaneous multiple wire impacts. Also, heat buildup in the print element causes flight time variances.

Integration of electronics to compensate for wire flight time variations, and the development of more efficient wire actuator technologies such as magnetic stored energy, which do not deteriorate with heat or usage, have alleviated dot placement problems. Generally, printing acceptable word processing quality characters requires dot placement within a $\pm 0.002''$ (0.051-mm) tolerance.

Two common techniques of generating high density dot placement are multipass print and staggered overlapping wires in the print element. The multipass technique fills in the vertical dots on each successive pass of the printhead, as the paper is moved vertically one-half of a dot position (Fig 4). A character is generated on two passes with 16 dots overlapped vertically. By using a printhead with 14 or more wires that overlap the dots vertically, one pass can generate the same vertical dot resolution. Printhead complexity and cost are increased due to additional wire actuators in the printhead and more electronics. Horizontal dot placement is most efficiently devel-



Fig 3 Magnetic stored energy printhead. Magnetic energy is stored by cross flexure spring held cocked by magnetic field at pole tip gap. Energized coil cancels magnetic field of gap, releasing spring and allowing wire to impact paper at high speed



Fig 4 Printhead and paper movement. Printhead moves horizontally and prints odd rows during first pass. Then, paper moves one-half dot position, approx 0.0078" (0.1981 mm) vertically. Printhead moves in reverse direction and prints even row dots

oped with vector generation algorithms that reduce the amount of memory required to store a character shape.

The tradeoff of speed for quality is almost linear. Creating a word processing quality character requires approximately four times the number of dots used in a standard 5 x 7 matrix character. Character speed is thus reduced by a factor of four. For example, to print word processing quality characters, a standard 5 x 7 matrix printer would be slowed from 600 to 150 char/s. However, character speed is slightly misleading since character pitch is also important. Because the wire cycle rate and the printhead velocity are generally held constant, a high pitch character (for example, 12 pitch) is printed at a faster character speed than is a low pitch (for example, 10 pitch) character. A machine that prints quality 10-pitch characters at 150-char/s can print quality 12-pitch characters at 180-char/s. Higher pitch characters require fewer dots horizontally to generate quality print.

With the use of microprocessors and low cost memory, character fonts can be stored in read only or random access memory. Since the characters are formed by overlapping dots, the matrix printer has the flexibility of changing character fonts, varying character sizes, and printing graphics without changing print elements. This multifunctional flexibility is not available with solid character print elements. Because speed and quality can be varied in inverse proportion, the matrix printer can satisfy the need for both high speed draft output and high quality final copy. The matrix printer offers multi-utility for word processing and data processing applications with multi-copy capability.

Reliability

Matrix printer reliability is usually measured as the life time of printable characters of the machine. Duty cycle and page density have a significant bearing on printable life since they determine the time the printer is printing versus nonprinting. In general, character print life of a matrix printer is limited by the character life of the printhead. Wire matrix technology has seen significant improvement in reliability over the past few years. Development of ballistic or free flight solenoid actuators has significantly increased printhead life. Ballistic printheads are achieving character print life of 300M characters as compared to 60M just a few years ago. Magnetic stored energy heads are now achieving a print life exceeding 1G characters.

In regard to band printers, the matrix printer compares favorably. Presently, the life of an individual character on a print band is limited to approximately 30M characters. If that character is a high usage character, such as a zero or a lower case e, the life of the band is a function of the life of the zero or e. A 5 to 10% usage of the zero, for example, will net a band life of 300M to 600M characters. The cost to replace a band is several hundred dollars, which is similar to the replacement cost of a matrix printhead. The simplicity of matrix printers with fewer parts and lower cost makes them a formidable

competitor with medium speed line printers.

Summary

The inherent flexibility of the matrix printer coupled with technological improvement in speed, print quality, reliability, and cost continue to make it a strong contender in data processing, graphics, and word processing systems for the next several years.

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CIRCLE 83 ON INQUIRY CARD

A Row Buffer LSI Controller For CRT Refresh

Row buffer technique for CRT refresh in a raster scan video terminal utilizes an LSI controller design and eliminates both DMA controller and special dynamic RAM interface parts

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wo basic types of large scale integration cathode ray tube controllers have evolved in recently designed data terminal systems. One type employs a row buffer cathode ray tube technique that uses a direct memory access controller to update two row buffers inside the controller. This technique, although not requiring a microprocessor for data transfers for cathode ray tube refresh, occupies excessive processing time due to direct memory access controller use of the data bus for row buffer update. The second type eliminates the direct memory access controller and row buffers, and directly addresses random access memory, which is shared with the microprocessor.

This direct memory access (DMA) type cathode ray tube (CRT) controller provides data from random access memory (RAM) directly to the character generator read only memory (ROM). However, the clock rate of the microprocessor must be compatible with the video output rate to the CRT since the memory is shared. If a biphase clocked microprocessor is used, CRT RAM is accessible to the processor 100% of the time; this is accomplished by operating the CRT on clock ϕ l and the microprocessor on clock $\phi 2$. If a singlephase microprocessor is used, modification of the CRT RAM may be done only during the horizontal and vertical blanking periods with the second type of CRT controller.

The MC6845 CRT controller has been designed principally to use, but is not limited to, transparent DMA for screen refresh. In addition, this CRT

controller may be implemented to work with an external row buffer without a DMA controller. This alternate method allows the MC6800 system bus, or other type of microprocessor, to operate at its own clock frequency. Operation and update of the row buffer occur at a divisional rate of the video clock. For example, with a character dot size of 5 x 7, the character dot matrix size would be 7 x 10. Update of the row buffer would occur during the blank scan line preceding the first scan line used for data presentation. The row buffer would be loaded with a new character every seven video clock pulses, which becomes the character rate. When dynamic RAM is used as the shared RAM. the video clock rate is limited to the slower clock rate.

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System Design

The row buffer technique of CRT refresh allows the implementation of dynamic RAM. This CRT controller system design (Fig 1) provides sequential row addressing often enough for refreshing. During the longest nonrefresh period (video blanking), the time without refresh is less than the permissible 2 ms. A DMA controller is not required since the CRT controller has its own memory address output lines (MAO to MA13).

An 80-character by 24-row 9" (23-cm), M-2000 CRT display is used in this design. Only 64 American Standard Code for Information Interchange (ASCII) characters are decoded in this system design by D0 to D5, but 128 characters are possible by presenting another bit to the MCM6674 character generator ROM through the 2-AM2847 row buffer.

Character data are accessed by the CRT controller during zero scan line time of each character row for each character. Data stored in 8-MCM6616 RAM are transferred to the 80-character row buffer. This buffer circulates its contents at the character clock rate of every 648.4 ns. As each character circulates, it is presented to the character generator ROM for the character clock period. These data, along with the scan line address inputs (RSO to RS3), select ROM data that are output on the D0 to D4 outputs of the character generator. Data bits are strobed into a 74LS165 serial shift register and shifted out as serial register data at the video clock rate. Video serial register data are then conditioned for output through two NAND gates and a D-type flipflop for VIDEO OUT.

CRT Controller and Row Buffer Principles

The CRT controller performs the interface functions of a microprocessor system to the raster scan CRT display. It contains logic for generating the vertical and horizontal synchronization pulses required, with their output


times under software control. In addition, memory address lines MAO to MA13 point to the address of the data (D0 to D7) required to refresh the CRT. Using this technique, memory address for each character is presented to memory only once per screen refresh. Data retrieved are stored in an 80-byte row buffer that is shifted, except during blanking, at the character rate. The row buffer is updated during scan line 0 of each character row. Because each character circulates through the buffer 10 times (once for each scan line), the amount of time the CRT controller must access memory for refresh is minimized. Memory address data must be buffered and multiplexed by four 3-state octal buffers (4-71LS95) so that memory address inputs have only a single source at any one time. The reason is because dynamic RAM uses 7 of the 14 address bits, bits 0 to 6, for row address select (RAS), and the remaining seven address bits, bits 7 to 13, for column address select (CAS). Only seven bits of address may be presented to dynamic RAM at any one time. In addition, two sources of the full 14-bit address are present, one from the CRT controller and the second from the microprocessor.

The CRT controller also outputs the scan line count (or address) as RSO to RS3. These outputs are presented to the character generator and the control logic. Blanking—or display enable (DE)—is also output from the CRT controller to control when the video data being shifted out are valid.

RAM Operation

A 16k-byte dynamic RAM is shared by both the CRT controller and the microprocessor. System design organization requires the memory timing circuits to generate pulses from two different clock sources. To operate with the microprocessor, the bus $\phi 2$ signal from an MC6875 clock register is used to derive 1-MHz memory timing synchronous with $\phi 1$ and $\phi 2$. The CRT controller and row buffer, however, operate at the character clock rate, which is one-seventh of the video clock rate. The origin of memory timing during row buffer update is based on character clock (C CLK). Memory clock generator logic derives the memory clock (MCYC) pulses from these two asynchronous sources, thus allowing access to shared RAM from two asynchronously timed address ports (A0 to A13 and MAO to MA13). This timing design allows row buffer operation with the CRT controller.

System Memory Timing

Two timing sources, $\phi 2$ for the microprocessor and character clock for the CRT controller, need to be controlled to interact with the shared RAM and not cause conflict for either microprocessor or CRT controller (Fig 2). Since the shared memory timing is asynchronous, the microprocessor must be halted during the CRT controller accessing period. The CRT controller updates the row buffer during each zero scan line time; this is accomplished by requesting a halt of microprocessor operations on its Go/Halt



CIRCLE 85 ON INQUIRY CARD





COLUMN ADDRESS TIME STROBE (NEGATIVE EDGE)

₱4 SYSTEM TIMING PULSE, GENERATED BY MC6875 CLOCK CHIP, IS THE 1-MHZ TIMING PULSE REQUIRED BY M6800 SYSTEMS. IT IS IN PHASE WITH MPU ¢2. TRAILING EDGE OF \$2 IS DATA TRANSFER TIME IN AN M6800 SYSTEM

2.MHz TIMING SIGNAL IS AVAILABLE FROM MC6875. ITS CONSISTENT PHASE RELATIONSHIP WITH $\phi2$ PROVIDES MEANS OF DECODING PULSES 1/2 WIDTH OF \$2, OR APPROX 250 ns

4 x fo

4-MHz SIGNAL PROVIDED BY MC6875 BECAUSE OF ITS PHASE CONSISTENCY WITH ϕ 2 AND 2 × fo PROVIDES MEANS OF DECODING PULSES % WIDTH OF ϕ 2 OR APPROX 125 ns

MCYC

THIS MEMORY CYCLE STARTER PULSE USES THE MC6875 DERIVED SIGNALS, ¢2, 2 × fo, AND 4 × fo, TO INITIATE MEMORY CYCLE. BA FROM MPU AND DMA REQ THEN DETERMINE WHEN MCYC SIGNAL SHOULD BE BASED ON CRT CONTROLLER TIMING

MEMORY READY

500-DE NEGATIVE-GOING PULSE DEPICTS TIME PERIOD OF MEMORY CYCLE ITS NEGATIVE LEADING EDGE CAUSES ROW ENABLE, RAS, AND CAS 1-SHOTS TO FIRE

ROW ENABLE

SELECTION OF ROW ADDRESS AND COLUMN ADDRESS IS DONE BY ROW ENABLE. 250-ns NEGATIVE PULSE SELECTS ROW ADDRESS BITS FROM MPU. WHEN IT RETURNS HIGH, COLUMN ADDRESS FROM MPU IS SELECTED

RAS

ROW ADDRESS SELECT'S NEGATIVE EDGE STROBES ROW ADDRESS LATCHES INTERNAL TO DYNAMIC RAMS TO CAPTURE ROW ADDRESS BITS FROM MPU. THIS POSITIVE PULSE IS APPROX 100-ns IN LENGTH. RAS SIGNAL REMAINS LOW UNTIL NEXT MEMORY CYCLE BEGINS

CAS

COLUMN ADDRESS SELECT'S NEGATIVE EDGE STROBES COLUMN ADDRESS LATCHES INTERNAL TO DYNAMIC RAMS TO CAPTURE COLUMN ADDRESS BITS FROM MPU. CAS ALSO LATCHES DATA INTO RAMS WHEN A WRITE OPERATION IS PERFORMED FROM MPU TO MEMORY. CAS REMAINS LOW UNTIL NEXT CYCLE BEGINS 300-ns POSITIVE PULSE

C CLK

CHARACTER CLOCK IS DERIVED FROM VIDEO CLOCK CIRCUIT BY DIVIDING IT BY 7. THE TOTAL HORIZONTAL QUANTITY IN THE CHARACTER MATRIX

BUS AVAILABLE (BA)

THIS MPU SIGNAL IS GIVEN BY MC6800 WHEN HALT IS RECEIVED. SIGNAL INDICATES TO CRT SYSTEM HERE THAT DMA TRANSFERS TO UPDATE ROW BUFFERS MAY BEGIN

MCYC THIS SIGNAL IS NAND FUNCTION OF DMA REQ, BA, AND C CLK. IT INITIATES EACH MEMORY CYCLE USED DURING ROW BUFFER UPDATE PERIOD. FREQUENCY IS BASED ON C CLK AND IS 1.5432 MHz

MEMORY READY

500-ns NEGATIVE-GOING PULSE DEPICTS TIME PERIOD OF MEMORY CYCLE. ITS NEGATIVE LEADING EDGE CAUSES ROW ENABLE, RAS, AND CAS 1-SHOTS TO FIRE

ROW ENABLE

SELECTION OF EITHER ROW ADDRESS AND COLUMN ADDRESS IS DONE BY ROW ENABLE. 250-ns NEGATIVE PULSE SELECTS ROW ADDRESS BITS FROM CRT CONTROLLER. WHEN IT RETURNS HIGH, COLUMN ADDRESS FROM CRT CONTROLLER IS SELECTED

RAS

ROW ADDRESS SELECT'S NEGATIVE EDGE STROBES ROW ADDRESS LATCHES INTERNAL TO DYNAMIC RAMS TO CAPTURE ROW ADDRESS BITS FROM CRT CONTROLLER. POSITIVE PULSE IS APPROX 100 ns IN LENGTH. RAS SIGNAL REMAINS LOW UNTIL NEXT MEMORY CYCLE BEGINS

COLUMN ADDRESS SELECT'S NEGATIVE EDGE STROBES COLUMN ADDRESS LATCHES INTERNAL TO DYNAMIC RAMS TO CAPTURE COLUMN ADDRESS BITS FROM CRT CONTROLLER. CAS REMAINS LOW UNTIL NEXT CYCLE BEGINS 300-ns POSITIVE PULSE

Fig 2 Dynamic RAM timing diagram. Circuit design eliminates special dynamic RAM interface parts by using two asynchronous clock timing sources-MPU and CRC controller.

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($\overline{\text{C/H}}$) input. When the scan (RS0 to RS3) line count equals nine (the highest reached for ten scan lines), the request for the microprocessor to halt is issued synchronously with ϕ 1. When a bus available (BA) signal is received, the memory pulse circuits are started by each character clock. When scan line 0 time begins, two 3-state buffers for addressing memory from the CRT controller are enabled. With each succeeding character clock, one of the 80 characters for the character row is read from memory and stored in the row buffer.

The system design, as implemented, makes no distinction between the last scan line of the last row to be displayed and the last scan line of any character row. Thus, a DMA request (DMAREQ) flipflop is set at the end of the display time and causes Halt to be output to the microprocessor during the entire vertical blanking period. Additional logic may be incorporated into the design to prevent the halting of the processor during this period. The only requirement is that the microprocessor be halted and the bus available signal be issued prior to the start of scan line 0 after the vertical blanking period.

Summary

By not requiring a direct memory access controller, a cathode ray tube controller design reduces parts count and, therefore, system cost. Dynamic memory may also be employed due to the screen refresh time being less than the memory refresh time, further reducing cost.

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MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

INTERFACING FUNDAMENTALS: A COMPARISON OF BLOCK DIAGRAMS FOR I/O TECHNIQUES

Peter R. Rony

Virginia Polytechnic Institute and State University Blacksburg, Virginia

D ifferent types of input/output techniques are available for use with microcomputers. One such method employs a concept, handshake cycle, which is defined in the IEEE Std 488-1978¹ as: "The process whereby digital signals effect the transfer of each data byte across the interface by means of an interlocked sequence of status and control signals. Interlocked denotes a fixed sequence of events in which one event in the sequence must occur before the next event may occur."

The simplest technique can be called unconditional input/output (I/O), a form of data transfer in which it is assumed that the external I/O device is always available and ready for communication with the microcomputer.² Other techniques can generally be included in the category called conditional I/O, in which data are transferred to or from an external I/O device only when it or the microcomputer is ready for the transfer. Status bits, in the form of individual flipflops that can be either set or reset, are communicated between the microcomputer and the external device, indicating when a condition exists or when an event has occurred.

Figs 1, 2, and 3, respectively, compare three types of I/O techniques for both input and output data transfers: unconditional I/O, conditional I/O in which a single flag is used, and conditional I/O in which one semaphore is used. Both the flag and the semaphore indicate when a condition exists or when an event has occurred. In the context of the three Figures, the flag outputs its information only to the micro-computer, whereas the semaphore outputs its information to both the microcomputer and the external I/O device.

Following are typical conditions and events associated with the use of either a flag or a semaphore:

Busy/Done

Data not available/Data available

Data not accepted/Data accepted

Data not valid/Data valid

Data available/Data accepted

Not ready for data/Ready for data

Data accepted/Data available

Busy/Ready

The bar represents the logic 0 condition of the flag. The term semaphore is attributed to Dijkstra,³ who applied it to the synchronization of parallel software processes. (For further information, refer to the books by Freeman⁴ and Tanenbaum.⁵)

Fig 1 depicts commonly occurring unconditional I/O data transfers, numerous examples of which have already been given in previous columns in this series. RD X and WR X are device select pulses, which simultaneously choose the I/O device and initiate the I/O data transfer. Quantity X is the device code or device address, typically an 8- to 16-bit quantity. When 8080A, 8085, or Z80 microcomputers are employed, these two pulses are labeled IN X and OUT X, respectively, and data transfer occurs between the accumulator and the I/O device. The data bus is











Fig 2 Conditional I/O with flag. External input or output device transfers data only when it is ready; single flag outputs information on status of I/O device to microcomputer





Fig 3 Conditional I/O techniques with semaphore. As in Fig 2, prepared external I/O device transfers data in conjunction with semaphore, which can communicate to external device and microcomputer

bidirectional; one of the arrows associated with the data transfer path has been omitted for clarity in each of the three Figures.

Fig 2 delineates the equally common conditional 1/0 data transfers in which a single flag serves to communicate the status of the I/O device to the microcomputer. For microcomputer input (top of Fig 2), a strobe signal (STB) from the input device sets the flag to a logic 1, thus indicating to the microcomputer that data are available. Upon detecting this logic 1 state, the microcomputer proceeds to input the data and at the same time clears the flag, with both operations being accomplished by the RD X pulse. For microcomputer output (bottom of Fig 2), the WR X pulse simultaneously writes data into the output device and also sets the flag. The output device acknowledges the receipt of these data by sending an ACK pulse to clear the flag.

Fig 3 demonstrates the use of a semaphore, the basic principle behind the conditional I/O technique known as strobed, or handshaking, I/O. A single flipflop is used, as it was in Fig 2, but in this instance the output from the flipflop-the semaphore—is sent both to the microcomputer and to the I/O device.

With the input device, the buffer stores a single input data byte or word. When the buffer is full, the semaphore is at logic 1; when empty, the semaphore is at logic 0. An input device first tests the semaphore to determine that the buffer is empty, and if so, simultaneously inputs a new data byte and sets the semaphore to logic 1 using an STB pulse. The microcomputer tests the semaphore to determine when it becomes logic 1; at that time the microcomputer simultaneously inputs the data from the buffer and uses the RD X pulse to clear the semaphore to logic 0. The distinction between a semaphore and a flag is thus clear: a semaphore is tested by both the microcomputer and the input device, whereas a flag is tested by only one of the two devices, typically the microcomputer.

In the case of the output device in Fig 3, the microcomputer first tests the semaphore to determine that it is logic 0; that is, the buffer is empty. When this condition is satisfied, the microcomputer simultaneously outputs a data byte to the buffer and sets the semaphore using the WRX pulse. The output device tests the semaphore to determine when the buffer is full; when such a condition is detected, an ACK pulse simultaneously transfers data from the buffer to the output device and clears the semaphore.

Clearly, both the microcomputer and the I/O device are interlocked with the use of a semaphore; the combined system consisting of the microcomputer and I/O device exhibits a fixed sequence of events in which one event must occur before the next event can occur. Integrated circuits that exhibit strobed I/O are the 8155 and the 8255. Although the asynchronous preset and clear inputs to the flipflops are the ones used in the examples in Figs 2 and 3, a more common situation is the use of one asynchronous input, such as the clear input, and one edge-triggered input-the clock input. Timing diagrams for unconditional and conditional I/O techniques will be discussed in subsequent columns.

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Key feature of the language is that application and standard systems programs can be transferred from one microprocessor to another. Its modular structure allows one interface to the processor and another to the operating system, without modifying the compiler. In addition, large programs can be divided into modules that are programmed, debugged, and tested separately and then linked together. Maximum module size, roughly proportional to the number of source code lines, is limited by the amount of program memory available to the compiler.

Syntax of the user oriented language is identical to that of Intel's PL/M. This allows PL/M programs to be compiled under PLMX, and used on microprocessors other than the 8080 and 8086.

Runtime routines and high level executive procedures allow simple interface to the operating system. The compiler runs under TEKDOS on the Tektronix 8002A universal microprocessor development system, as well as under CP/M, an operating system that supports 8080 based systems. Microprocessors currently handled by the compiler are the 8080, 8085, Z80, and 6800. Systems Consultants, Inc, 4015 Hancock St, San Diego, CA 92110, intends to introduce interfaces to other operating systems and to support the 9900, 1802, 8086, and Z8000 microprocessors during 1980.

The compiler's structure, which is transparent in use, consists of a machine independent portion (approximately 85%) that produces intermediate code, an executive module (5%) which is dependent on the operating system, and a machine dependent portion (10%) that provides final code (see Figure). PLMX source code compiles first to an intermediate code, which is then converted by the modular code generator into assembly language code for the particular microprocessor. The programmer has access to the code at any point after the compilation for modification or manipulation.

Features of the language are simple, compact notations; free format with comments occurring anywhere in source text, except within reserved words, identifier names, and numbers; and based variables and pointers for manipulating microprocessor memory. Expressions of arbitrary complexity are allowed for programming at a high level; programming may also be done at the assembly or machine language level and later linked to the PLMX output.

Resident on an 8" (20-cm) diskette, the \$1000 compiler may also be placed on hard disc. The user invokes the compiler to start the process. Final code is space optimized, suiting the language to ROM based programs; PLMX, in addition, keeps ROM and RAM areas separate. A future version will allow the user to opt for either faster execution speed or optimized space. Circle 410 on Inquiry Card

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COMPUTERS, ELEMENTS, AND SYSTEMS

128k-Byte Dynamic Read/Write Memory Card Appears As Static RAM

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A memory read/write control sets the memory configuration, either byte or word oriented; the attribute-read/ write disabled, read only, write only, or read/write-is assigned manually or under program control to each bank. Partitioning is in 32k-byte increments. The memory in 8-bit systems is normally configured as two pages of 64k bytes each that are switched in and out of memory space under program control. The 16-bit systems with 1M bytes of address space have memory positioned on any 128k-byte address boundary via onboard jumpers.

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Performance Jumps 60 Percent With 16-Bit Central Processing Unit

Production designs that were originally developed with 8-MHz capability built-in can be upgraded with the addition of the 8-MHz, 16-bit 8086-2 microprocessor, retaining total software compatibility with existing applications. Fabricated using HMOS-II technology, the CPU achieves a 60% increase in performance. This solves design problems encountered with fast, high precision processing and control systems. Price in quantities of 100 is \$200.

Support is provided by the existing family of 5-MHz 8086 LSI peripheral, dynamic and static memory, and bipolar bus devices. In addition, use of the 8089 I/o processor—as a coprocessor—in an 8086-2 system increases I/o capabilities. I/o programs and the main program are thus executed concurrently.

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, expects the microprocessor to provide expansion into new applications. These cover such areas as telecommunications, distributed processing, small business computers, data processing, and realtime process control. In addition, reduced program development time is achieved through combined higher CPU performance and increased code generation efficiency of PL/M 86. Performance levels of assembly language programming are reached with high level languages. Finalizing PL/M programs with assembly language modifications maximizes the 8086-2's performance.

Program storage is available with the new 2732A 32k-bit, 200-ns EPROM (introduced in "Around the IC Loop," p 199); other storage units are the 2716 16k-bit ервом, 2732 32k-bit EPROM, and interchangeable, mask programmed ROMS. The 2732A EPROM supports the 210-ns 8086-2 requirements, while eliminating the need of wait states for program store memory requirements. Static and dynamic RAMS, particularly 4k-bit static RAMS in the 2114A, 2142, and 2148 families, serve as data memory. The 16k-bit 2118 dynamic RAM family functions with large memory systems.

Bipolar support components include the 8284 clock generator and driver, 8282/8283 octal latches, 8286/8287 octal bus transceivers, and 8288 bus controller. The clock generator and bus controller, in addition to the microprocessor, support the MultibusTM architecture for multiprocessing uses. The transceivers and controllers extend the bus structure for medium and large systems. Dedicated and general purpose interface and control devices are available for peripheral equipment. The UPI-41ATM universal peripheral interface microcomputers (8041A/8741A) handle custom interfaces.

Since the 8086-2 is a family extension, it also utilizes existing development tools for the 8086 and 8088 microprocessors. These include the Intellec^R microcomputer development system, the ICE-86TM in-circuit emulator, and the SDK-86 system development kit. The isBC 86/12A[™] computer, based on the 8086, allows hardware prototyping and volume production. Resident Intellec software supports modular high level PL/M 86 and assembly language ASM 86 program development. In addition to PL/M, the 8080 and 8085 families are supported by Pascal, FORTRAN, BASIC, and COBOL.

Circle 412 on Inquiry Card

Development System Increases Programmer Performance

Software development that previously required the use of timeshared facilities or several standalone systems is eased by the MUDS-11 multiuser microprocessor development system. Increased performance on minimum hardware is achieved through several programmers simultaneously performing program generation, assembly, and simulation. The assembled programs can be downloaded to an online MDS or in-circuit emulator for final realtime emulation.

The DEC PDP-11 based system, with memory, tape, disc, and terminal peripherals, configures to a range of 8- and 16-bit microprocessors. Included are utilities, operating system software, and FORTRAN IV. International Data Services, Inc, 453-D Ravendale Dr, Mountain View, cA 94043, performs the system generation for the user's configuration.

Both relocatable and absolute cross assemblers feature macro facility, con-

ditional assembly capability, list control pseudo-ops, and alphabetically organized symbol or cross-reference table listing. The 2-pass assemblers produce an object module file and output listing. Larger programs are segmented into diverse modules that are assembled and debugged separately using the relocatable version. These modules are then combined into a single absolute object program using the linking loader.

Functioning in interactive or batch mode, the simulators perform interpretive execution of the object module or program. It supports simulation of I/O operations, interrupts, operand and instruction breakpoints in RAM/ ROM mode, as well as dump, patch, and trace routines. Error messages and cumulative cycle counts are generated and displayed. Circle 413 on Inquiry Card

Plug-In Intelligent Printer For uComputers Doubles As Typewriter

Simplifying text printout for personal computers, the HY-Q 1000^{TM} contains five built-in microprocessors. The letter quality daisy wheel printer plugs into a microcomputer, without complex software. The unit automatically converts simple codes into instructions for text formatting functions that include justification, proportional spacing, automatic tabbing, and underlining.

Xymec, 17791 Skypark Circle "H," Irvine, CA 92714, also features Quadra-PitchTM-10, 12, or 15 characters/in (4, 5, or 6/cm) or proportional spacing; up to 198 characters/line; 100 characters in English, Italian, Spanish, French, and German without changing the daisy wheel; and 21 typestyles in five colors. Reverse printing produces white characters on a black background for added emphasis.

The printer further functions as a typewriter, made by Olivetti Corp. As such, it provides a 224-character, 2-line memory; a nonvolatile 1024character memory for common phrases, margins, and tabs; automatic paper positioning; electronic margin reset; and a digital readout of column position and remaining lines to end of page.

Circle 414 on Inquiry Card

Until now, computer graphics suffered from terminal high cost.

If you've ever considered displaying Tektronix* graphics data from a host computer, you know all about terminal high cost. A hunk of hardware like a Tektronix 4010 graphics terminal can set you back quite a few kilobucks. It's enough to drive a person of modest means to the drafting table.

The Affordable Alternative

ABW Corporation has just made graphics display as practical as the personal computer. With TEKSIM. The Apple II/Tektronix 4010 Simulator. TEKSIM is a read-only memory (ROM) that plugs directly into an inexpensive Apple II* computer. Combining an advanced programming technique known as distributed processing with Apple's high resolution plotting capabilities enables TEKSIM to emulate Tektronix 4010-series terminals at a fraction of the cost. (A symbolic representation of TEKSIM in operation is provided below for the technically minded.)

Outstanding Features

The TEKSIM-Apple combination functions in the same way as a Tektronix terminal, displaying graphical output from a host computer without any modification to the host-resident program. You can also input data to the host using game paddles or a joystick. And a TEKSIM-Apple terminal even has features not available in the 4010-series. Six-color "palette" for multicolored displays. Selective erase. Video output to allow any size television to serve as the screen. Plus the added benefits of a powerful Apple II computer to use both in and out of graphics mode. Any compromise? Just one. Apple's resolution is about a fourth that of a Tektronix terminal. Still more than adequate for most applications.

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Dealer inquiries invited.	06020



Here's how TEKSIM works: First, Tektronix data comes out of the host computer.

.so it can be displayed on the Apple's TV screen



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CORPORATION

CIRCLE 92 ON INQUIRY CARD

MICRO DATA STACK

6800 Single-Board Memory System Features Diagnostic ROM

PCM 16-32 is a 16k RAM and 32k EPROM OF ROM board for 1- to 2-MHz operation with M6800, 6801, 6802, 6809, and 650X series microcomputers. RAM expands in 4k-block increments to 16k, while the EPROM/ ROM expands from 2k to 16k with 2716 type parts and 4k to 32k with 2732/2532 parts. Interchange ROM parts can provide up to 32k of permanent memory, as well as 48k with no RAM.

Addressable via the 86-pin card edge, the board has separate RAM and EPROM enables. The user can configure address schemes with eight memory maps. ROM and RAM address can be overlapped with ROM/EPROM taking priority. The single board from Phoenix Digital Corp, 3027 N 33rd Dr, Phoenix, Az 85017, also offers write protect capability. With 16k of RAM and 32k of EPROM, the system draws 1.6 A from a single 5-V supply. Using 16k of CMOS RAM dissipates less than 160 mA per 4k block while active and less than 400 μ A standby. Industrial and commercial temperature versions are available.

Onboard power-on reset circuitry protects the RAM during system initialization. Separate power busing is provided to each 4k block of RAM. RAM is enabled via a programmed gate array.

Signature analysis test techniques designed into the system allow memory system test, diagnostics, and troubleshooting. A diagnostic ROM performs incoming inspection tests, system and field tests, and diagnostics. Stimulating nodes within the memory interface, timing, and memory elements, the ROM contains such test strategies as alternating patterns and soft error detection algorithms. Circle 415 on Inquiry Card

Packaging Technique Permits Economical Program Development

During the prototyping stage, programs can be stored economically in separate EPROMS in this ROMless version of the Z8 single-chip microcomputer. Z8-03 MPE (Microcomputer ProtopackTM-Emulator) simplifies prototype development and preproduction of mask programmed, Z8 based applications. The 40-pin package from Zilog Inc, 10460 Bubb Rd, Cupertino, cA 95014, offers the same capabilities as the standard Z8 and 64-pin Z8-02 MPD (see Computer Design, Nov 1979, p 180).

Protopack carries a piggyback style 24-pin socket for direct interface to program memory. The socket provides 12 ROM address lines, 8 ROM data lines, and control lines for use with 2716 EPROMS. Unlike usual EPROM versions of single-chip microcomputers, this one allows separate EPROM program storage. In applications where the same hardware configuration is used with many programs, the result is cost-effective program development.

Circle 416 on Inquiry Card

WHY CAN'T MICROPOLIS DO THINGS LIKE EVERYONE ELSE?

Development Tool Aids Programming of 6502 Series Microprocessor

Users of the 6502 family may write programs and debug both hardware and software with the MDT 1000. Comprised of a 12" (30-cm) CRT display, 54-key keyboard, software, and 5-V power supply, the development tool is compatible with Motorola's Exorciser/Micromodule bus, which permits the addition of standard digital and analog boards. Interfaces are included for a dual cassette, and serial and parallel printers; the latter interfaces are located on the CPU card. The RS-232-C interface uses the sy6551 ACIA with programmable baud rates of 110 to 19.2k baud. Video interface permits display of 25 lines of 80 upper and lower case characters (from the 128character set), with two intensity levels.

Other components are a 4k-byte static RAM board (8k and 16k RAM versions are also offered by Synertek Systems Corp, 150 S Wolfe Rd, Sunnyvale, CA 94086); 2716 and 2732 EPROM programmer; sockets for four ROMS, system RAM, and ACIA for serial communications; and a 4-slot motherboard with two sockets installed.



Full text editing and assembling capabilities are performed with the resident assembler/editor (RAE-1), contained in 8k bytes of ROM. Among the functions of the editor are character string search, block insert, editing line numbered text, tabbing, and error messages. This facilitates entering and modifying source code.

The assembler provides macro and conditional assembly capability; 16 assembler pseudo ops; 23 error codes; and hexadecimal, binary, and decimal nonsymbolic data types. Source may be assembled from memory or tape. The relocatable machine code that is produced may be directly executed or burned into EPROM. Large programs are assembled through the dual cassette interface using the cassette or RAM for source entry and object output.

A 4k monitor in ROM, containing debug features, is similar to sym-1 and runs with sym software. An 8k floating point BASIC in ROM (BAS-1) is optional. Additional software handles CRT control, printer and cassette interfacing, EPROM programming, and the keyboard. Circle 417 on Inquiry Card

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Micropolis Corporation, 21329 Nordhoff Street, Chatsworth, CA 91311. For the telephone number of your nearest OEM rep, call (213) 709-3300.

Microcomputer Combines High Speed of NMOS With Low Power Needs of CMOS

Fabricated using double poly CMOS, the NSC800 family of one CPU and two memories incorporates architectural features of the 8085 microprocessor with those of the Z80. The combination of these three devices into one device reduces chip count and power. The 40-pin NSC800 CPU uses the multiplexed address/data bus structure of the 8085 with the Z80 register structure and instruction set. Providing memory and general programmable interface capabilities, the NSC810 RAM-I/O timer and NSC830 ROM-I/O dedicated peripherals contain onchip logic for interfacing directly with the multiplexed bus.

The P²CMOS process, developed by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, combines steps of CMOS and NMOS fabrication techniques to improve performance. This silicon gate process uses oxide isolation rather than diffusion isolation. Two levels of polysilicon interconnects increase density over standard CMOS. To ensure producibility, geometries of 5- μ m lines and spaces are used, although reductions to 3- or 3.5- μ m geometries will produce further improvements. P²CMOS uses electron beam masks and 4" (10-cm) wafers.

A minimum 3-chip system of these elements has 2k bytes of ROM, 128 bytes of RAM, two timer/counters, five interrupts, and 32 1/0 lines. The CPU is capable of $1-\mu s$ instruction cycle times. The system dissipates only 100 mW, due to the lower power consumption. This also allows increased component density with reduced package size. The devices operate from a single power supply with a range of 3 to 12 V.

Sample quantities of the family will be offered during the first quarter of 1980, with initial pricing for a set of three components in plastic expected to be \$175 in quantities of 100 and up. The existing line of CMOS components-memories, analog interfaces, logic devices, and general or dedicated function peripherals-support this family. In addition, a line of P^2 CMOS memory and interface components are being developed.

The CPU has an 8-bit data bus that internally communicates with



the register array, arithmetic logic unit, and status registers, as well as between the data/address buffers and instruction register. Also included are a 16-bit address bus and 22 registers accessible to the programmer. A total of 65k bytes of memory are directly addressed, as are 256 locations in separate I/o memory space.

Identical to that of the 8085, the multiplexed bus structure saves on pin functions and simplifies PC board layout. The instruction set is Z80 software compatible; all Z80 instruction set features such as block, I/O, and memory transfers, and bit sets, resets, tests, and indexed addressing apply to the NSC800.

A power save function, when activated, causes the CPU to stop all internal clocks at the end of the current instruction, while maintaining all internal status and data register values. Power dissipation is halved during power save, because only the

oscillator and system CLK output are operating.

NSC800A is a speed selected version with a $1-\mu s$ execution time. The company plans to provide development support with the STARPLEX development system.

Containing 1k bits of static RAM organized as 128 x 8 bits, the 40-pin NSC810 contains 22 programmable I/O bits arranged as three separate ports with each bit definable as input or output. The timer portion operates over a range from dc to 4 MHz; it consists of two programmable 16-bit binary down counters that function in six modes.

The 40-pin NSC830 contains 16k bits of ROM arranged as 2048 x 8 bits. 1/0, arranged similarly to the 810, consists of 20 programmable 1/0 bits. For prototyping work or when onchip ROM is not required, the NSC831 is a ROMLess version.



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CIRCLE 94 ON INQUIRY CARD

100 taken directly - hard copy can MICRO DATA STACK COMPUTERS, ELEMENTS, AND SYSTEMS

Computer's Interfaces Promote Rapid Data Exchange Between Devices

A self-contained microcomputer, the 580 is based on a 4-MHz Z80A microprocessor, backed by a 65k-byte dynamic RAM. It supports two RS-232 serial ports, two parallel ports and a parallel printer port, one hard disc port, and one floppy disc drive connector for two external mini or 8" (20-cm) floppy disc drives. Two standard double-density minifloppy drives with DMA controller store 400k bytes online; with the system's disc controller, total capacity through combinations of drives can exceed 3.4M bytes.

A high speed DMA channel may be programmed to interconnect most interfaces with the internal RAM, keyboard, and video display. Zeda Computers International, 1662 W 820 N, Provo, UT 84601, has included this capability so that the devices may transfer data quickly.

The video screen displays 25 lines of 80 characters. The 108-key keyboard has 24 software programmable keys to produce 48 special functions. In addition, 128 alphanumeric and line-drawing video characters may be reprogrammed to facilitate foreign language or graphics video displays. Other components are a realtime clock, audio beeper, and parity checking logic.

ZEDOS, the disc operating system, is CP/M compatible. It handles all interrupts, data transmissions, keyboard definition, error detection, and disc storage retrieval. The system operates with BASIC, COBOL, and FORTRAN. Circle 419 on Inquiry Card

Interface Products Are Aimed At Multibus Single-Board Computers

Two general purpose bus foundation modules and a universal wirewrap module are the first in a series of interface modules being marketed by MDB Systems, Inc, 1995 N Batavia St, Orange, CA 92665, for Intel Multibus computers. Each module takes only a single slot in the computer chassis.

Interfacing between 8- or 16-bit computers and peripherals, the bus foundation modules consist of basic Multibus logic elements plus wirewrap positions for up to 38 IC devices using low profile sockets or direct mounting of 14- to 40-pin ICs. Designer wired options permit multiple controller applications, address selection, and interrupt control. Containing wirewrap posts on the component side of the board, the modules also provide for three 50-pin ribbon cable connectors to external devices.

The wirewrap module provides for up to 60 low profile sockets or ICS chosen from 14- to 40-pin packages. Wirewrap posts on the component side achieve 0.5" (1.27-cm) spacing in a single chassis slot. Three 1/0 positions can be used with 16- to 50conductor ribbon cable edge connectors to external devices or modules. An extender board and 1/0 cable subassemblies complete the accessories for the computers.

Circle 420 on Inquiry Card

Memory System Supplies EXORciser With Hard Disc Expansion

STORAGE DEMON[™] is a disc controller. 10M-byte Winchester disc drive, and spos interrupt driven disc operating system that overcomes the limited disc storage of Motorola's 6800 EXORciser system. It is upward and downward compatible with the EXORCISET 1 and 11. The sealed media system from Software Dynamics, 2111 W Crescent Ave, Suite G, Anaheim, CA 92801, provides 19k 512-byte sectors for use under most environmental conditions. Latency times are 8.3 ms. Track to track seek time is 10 ms. while full seek takes 100 ms.

Support by the interrupt driven spos offers keyboard type ahead, automatic disc read ahead and disc sector pooling, dynamic files with random access to the byte, and device independence. Exordisk I, II, or III is supported by the operating system, permitting floppy disc drives to supply added disc storage or backup for the hard disc drive. spos accommodates the company's Business BASIC compiler, with 10-digit BCD arithmetic, long names, file 1/0, and error trapping.

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Commercial And Industrial Uses Are Served By Microcomputer

Total system performance is obtained from the 900 single-board computer packaged with quad-density flexible disc drives to provide a simple modular design. The 4-MHz, Z80 based model 90F microcomputer (see *Computer Design*, Feb 1979, p 146) used in the system is a member of the **OEM** board family manufactured by Quay Corp, PO Box 386, Freehold, NJ 07728; it contains the system's memory and peripheral controllers. The 48k bytes of dynamic RAM are expandable to 65k bytes.

All disc access is under DMA control for high speed data transfers and multitasking CPU operation. Two doublesided, double-density flexible disc drives from Control Data Corp are standard, with a formatted capacity exceeding 2.5M bytes. Track to track access time is 3 ms.

Automatic diskette type identification allows single-sided diskettes to be used also. Activity indicator, write protect, and transparent IBM 3740 format compatibility for loading or generating single-density diskettes are standard.

A disc expansion port can support up to four 2-sided flexible disc drives. Remaining system components include a parallel line printer port, Rs-232-C or 20-mA current loop serial port, dual power supplies with overvoltage protection, dual ac outlets for peripheral use, and a fan. The system requires 50 to 60 Hz for operation.

Optional features are an add-on dynamic RAM (to 65k bytes), add-on disc subsystem (for total of 5M bytes), rackmount enclosure, and P/ROM programmer for 2708 or 2716 EPROMS. Further expansion is possible with an S-100 bus adapter and two additional Rs-232-C ports with programmable baud rates, synchronous/ asynchronous operation, and modem control.

Enabling program construction with its context editor, assembler, and debugger, the CP/M disc operating system offers diskette initialization, absolute copy utility, and P/ROM resident bootstrap. For rapid access to programs, a file management package supports a named file structure, dynamic allocation of file space, and sequential and random file access. High level languages are BASIC, FORTRAN, and COBOL. Several business application packages are also available. Circle 418 on Inquiry Card

DS BRIEFS

Programmable Controller Offers Full Floppy Disc Mass Storage Capability-Compatible with IBM 3740 and TI disc formats, TM990/303 supports up to four double-sided drives. Texas Instruments, Inc, PO Box 1433, мs6404, Houston, тх 77001, has designed in soft sector compatibility, write precompensation, and 5 or 8" (13- or 20-cm) diskette compatibility for use of the controller board with the TM990 series of microcomputer products. . . . Flat Display Panel Interfaces Directly With Microprocessors -Lx140 is a 1-line, 40-char, alphanumeric, 5 x 10 dot matrix liquid crystal display system that interfaces via a 20-pin socket connector. Introduced by Kylex, Inc, 420 Bernardo Ave. Mountain View, cA 94043, the unit features integral drive, refresh, temperature compensation, and power supply electronics. It operates from a 5-V power supply with typ power drain of <400 mW. . . . Parallel Interface Provides 64 I/O Data Lines for LSI-11 Microcomputers-The 8.9 x 5.2" (22.6 x 13.2-cm) DRv11-J module for the LSI-11/23, -11/2, PDP-11/23, and -11/03 features programmable interrupt structure with bit interrupts on up to 16 lines. Digital Equipment Corp, Maynard, MA 01754, has organized the 64 lines into four ports; data line direction for each port is program selectable.

Z8000 Cross Assembler Programs Are Reproduced in P/ROM for Target Microprocessor Execution-Gen-Rad/Futuredata, 6151 W Century Blvd, Suite 1124, Los Angeles, CA 90045, claims that the Z8000 relocatable macro cross assembler is up to 10 times faster than other assemblers, because parts are written in assembly language to optimize speed and memory usage, the assembler program overlaps 1/0 operations, and all disc operations are handled by a disc controller. Operating with the 2300 series universal development system, the assembler contains macro facility, conditional assembly, and pseudo op, all compatible with 2300 series assemblers. . . . RAM Board for Multibus Units Holds 48k Bytes-Onboard LSI refresh for 16k dynamic RAMS, 8- or 16-bit mode, and 20 address bits for 1M-byte addressing are features of RAM-048. Reliability is assured by Electronic Solutions, Inc, 5780 Chesapeake Ct, San Diego, ca 92123, with a 168-h burn-in at 55 °C. Specs include 450-ns access time and 700-ns cycle time.

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CIRCLE 97 ON INQUIRY CARD

AROUND THE IC LOOP

MEMORY AND I/O IMPLEMENTATION IN 8-BIT SLICE ECL

Paul Chu

Fairchild Camera and Instrument Mountain View, California

• omputer systems utilizing large scale integrated emitter coupled logic components at the 8-bit slice level benefit from various advantages inherent in that advanced technology. Implementation of bit slice components reduces system complexity, component count, and costs. When specific capabilities such as error correction are built into the components, additional circuits normally provided by the system designer become superfluous. Simplifications of this kind, coupled with the high gate speeds, lead to more sophisticated capabilities in high speed microprogrammed system design.

Capabilities provided by ADIU and MFN components of the F100220 family, discussed in preceding columns, are essentially CPU-like, filling such roles as ALU, memory interface, bus multiplexer and demultiplexer, and Exclusiveor logic array. Here, the picture will be rounded out with the description of components of this family that provide capabilities oriented toward memory and I/o. These components (mentioned briefly in the earlier discussions) are the dual access stack (DAS) and the programmable interface unit (PIU). The combined capabilities of all four components provide diversified building blocks for digital systems requiring subnanosecond gates.

Dual Access Stack

Designed around a 32-register by 9-bit memory, the DAS (Fig 1) has a read access time of 14 ns (maximum) or 9 ns (typical) from addresse to data out on the bus.

The A and B buses are bidirectional and, although the inputs and outputs for each bus are illustrated separately in the figure, it should be noted that A "in" and A "out" are common and B "in" and B "out" are common. These ports are controlled by completely independent signals which may or may not be in synchronization externally. Thus, one port may be reading from or writing into one register, while the other may be reading from or writing into another register.

Each port has its own address lines, control lines, and error indicators via parity checking of both addresses and data. The address-equal output detects contention for possible error recovery or retry. Contention is flagged in the following situations: simultaneously writing to a common location via both ports, and writing to one location via one port while simultaneously reading the same location via the other port.

Programmable Interface Unit

The programmable interface unit (PIU) is designed to handle communications with a system element interface via the data access lines (DAL) bus and its associated controls, while communication between PIUS utilizes a common bus structure designated as A, B, and C buses. As shown in Fig 2(a), the DAL bus (eight data bits, one parity bit) allows bidirectional transfer into and out of the PIU. This path may be used by the controller to load the program information and data into the PIU registers.



The lines write address, address (3), write DAL, and read/write are used to control operations on that interface. Chip ID lines (4) are connected internally through a comparator to four bits of the B bus, allowing the PIUS to identify which PIU components should be active. Interrupt lines are used to signal the system element on the status of functions within the component.

Fig 2(b) illustrates the common buses connecting a multiplicity of PIUS. Data may be transmitted in a unidirectional or a bidirectional mode over buses A and B (nine bits each) and in some instances on bus C. In an automatic handshaking mode, bus C (eight bits) is utilized to communicate data service requests and acknowledgements.

PIU Registers

A more detailed block diagram of the PIU is presented in Fig 3. The registers in the PIU and their associated functions are

Register	Function					
DAL	Used for	data	and	for	loading	instructions
A Register	Used for	data				

B Register	Used for data and ID comparison			
C Register	Used for handshaking and, in some cases, for data transfer			
Interrupt Mask Register	Controls interrupt conditions in PIU			
Mode Register	Controls A bus and B bus input and out- put modes with and without automatic handshaking; and controls conditioning of interrupt A and interrupt B lines on DAL interface			
Bus Control Register	Indicates interrupt/service conditions on "priority request," "priority grant," and "busy" lines			
Address Register	Stores the address of internal register active during an operation			

A 9-bit bidirectional internal bus allows communication between these registers. Note that, as in other family members, parity is carried and checked in all appropriate operations. As bit patterns in appropriate registers are set from external sources (or from internal operations), mode of operation, interrupt conditions, data direction, and parity checking are program controlled.



PIU Transfer Operations

The PIU has three modes of transfer operations in which two groups of 13 lines may be individually programmed.

Mode 0: Bidirectional

- A (8 Bits + Parity) transferred in either direction.
- Two C bus lines perform automatic handshaking and two C bus lines for control signals may be defined by the user.
- B (8 Bits + Parity) and 4 bits of C (same operation as for A).

Mode 1: Unidirectional, Input or Output Latched

- A (8 Bits + Parity) transferred in one direction only, with two C bus lines doing automatic bidirectional handshaking and two (unidirectional) available for user definition.
- B (8 Bits + Parity) and 4 bits of C (same operations as for A).

Mode 2: Unidirectional Output Latched, Input Unlatched

A (8 Bits + Parity) and 4 bits of C with output data lines latched.

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- A (8 Bits + Parity) and 4 bits of C with input data lines unlatched.
- A (8 Bits + Parity) input data lines unlatched and any directional combination of remaining four C lines.
- A (8 Bits + Parity) output data lines latched and any directional combination of remaining four C lines.
- B (8 Bits + Parity) and 4 bits of C (same operations as for A).

PIU Compatibility and Standardization

TTL compatible inputs and outputs characterize the PIU, and the 3-state DAL lines also interface with commonly used TTL components. Level converters (F100124, F100125) must be used with the component when it is interfaced to the other ECL members of the family. The A, B, and C buses have high current sinking capability (48 mA) with open collector outputs and Schmitt triggered receivers providing built-in hysteresis for greater noise rejection. This component is currently a candidate for the ANSI small computer to peripheral bus interface (Committee X3T9) standard. It has also been submitted to the International Standards Organization (ISO) for possible approval as an international standard.

Summary

The 8-bit slice components described in this 3-part series supplement other subnanosecond ECL components, to provide designers of high speed systems with sophisticated system elements. In addition to the advantage of bidirectional architecture, the incorporation of parity checking and Hamming check and syndrome bit generation for error detection/correction vastly enhances system reliability. The computer system diagram in the first column of this series (see *Computer Design*, Dec 79, p 135), in light of the descriptions of the components, may now be reviewed with a better appreciation of the capabilities of this ECL family.



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32k-Bit EPROM Operates at 200-ns Maximum Access Time

Twice as fast as the present industry standard for high density erasable programmable read only memories (EPROMS), one version of the 32k-bit 2732A operates at a maximum access time of 200 ns. The ultraviolet erasable and electrically programmable devices were designed by Intel Corp. 3065 Bowers Ave, Santa Clara, CA 95051, to complement its concurrently introduced 8-MHz 8086-2 16-bit microprocessor (see p 182, this issue), as well as other very high performance microprocessors and microcomputers. However, the EPROM access speeds surpass even the companion microprocessor's typical 210-ns requirements and provide the backup speed that might be needed for very large system applications with up to 1M bytes of memory. In such systems, the microprocessor can operate without the addition of wait states for program store memory references. Except for programming, this 32kbit EPROM is a direct board replacement for the 450-ns 2732.

For use in multiple bus microprocessor systems, an output enable (\overline{OE}) control (see block diagram) separate from the chip enable (\overline{CE}) control eliminates bus contention. With this 2-line control, the \overline{CE} line selects a device, but device outputs cannot become active on the bus until an \overline{OE} pin receives a control signal from the microprocessor. When the microprocessor is ready to receive data from the EPROM, it sends the \overline{OE} signal. (In large systems, this is handled by a bus controller.)

Operating temperature range is 0 to 70 °C. Absolute maximum ratings are -10 to 80 °C temperature under bias and -65 to 125 °C storage. All input to output voltages with respect to ground must be in the 6 to -0.3 V range. V_{cc} power supply is 5 V ±5%. Maximum active current is 150 mA; in standby mode, achieved by applying a TTL-high signal to the CE input, the maximum current is reduced to 35 mA.

DC operating characteristics in read operation include $10-\mu A$ max input load and output leakage currents; -0.1-V min and 0.8-V max input low voltages; 2.0-V min and $(V_{cc} + 1)-V$



max input high voltages; 0.45-V max output low voltage; and 2.4-V min output high voltage. Ac characteristics, respectively, for three available versions (2732A, 2732A-2, and 2732A-3) are 250-, 200-, and 300-ns max access times; and 100-, 70-, and 150-ns max output enable to output delay as well as output enable high to output float.

Unlike earlier generation EPROMS produced by this company using PMOS and NMOS technologies, the 2732A is fabricated with HMOS-E, the company's patented process for manufacturing high performance NMOS devices. This silicon gate technology is credited with the device's capability for much faster access speeds.

Devices are now available in limited quantities for customer sampling. High volume deliveries are expected to begin in 1980. The high performance 2732A-2 200-ns max access time version and the 2732A-3 350-ns for less stringent applications will be available initially at single-unit prices of \$570 and \$475, respectively. Circle 350 on Inquiry Card

Multiplying DAC Provides High Accuracy

Maximum gain errors of $\pm \frac{1}{2}$ LSB at 25 °C and ± 1 LSB from -55 to 125 °C characterize a 4-quadrant, 12-bit multiplying digital to analog converter, the MN3412 from Micro Networks Corp, 324 Clark St, Worcester, MA 01606. Corresponding gain drift is 1 ppm/°C over the operating temperature range. Its manufacturer claims it to be the most accurate 12bit multiplying DAC on the market.

This converter finds use in high performance multiplying applications of computational and servo systems, and in high accuracy data conversion when used with a precision fixed reference. Additional applications include digital to synchro converters, programmable gain amplifiers, and ratiometric ADCS.

The device also features a low zero error, less than ± 5 mV at 25 °C with drift of only $\pm 5 \ \mu V/$ °C. Linearity is guaranteed to be better than $\pm \frac{1}{2}$ LSB over the full operating temperature range, insuring monotonicity. In addition, settling time is specified to be less than 20 μs , and feedthrough is 80 dB down at 400 Hz.

Available for operation over the full -55 to 125 °C military temperature range, the DAC can be processed to MIL-STD-883 for military/aerospace applications. It is packaged in a 32-pin minimodule that offers a low offboard height and has a standard dual-inline footprint.

Circle 351 on Inquiry Card



Programmable UART Uses 5-V Supply, Replaces 2-Supply Devices

Full- or half-duplex operation, TTL compatible 1/0, and a single 5-V power supply characterize the S1602, a completely programmable UART that generates start bits automatically. Produced by American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, cA 95051, the chip is a second source for the Fujitsu MB8868A and is a functional and pin compatible replacement for Western Digital's TR1602 A/B. The S1601 requires only a 5-Vdc supply instead of the 5- and -12-Vdc supplies needed by its predecessor, the 1602, and the Western Digital device.

This n-channel silicon gate device operates at up to 50k baud, full or half duplex. Additional features include the automatic synchronization of data and clock rates, a 3-state output capability, and completely static circuitry.

The UART transforms asynchronous serial data from terminals or other peripherals to parallel data for a microprocessor, computer, or other terminal. Parallel data are converted by the transmitter section of the UART into a serial word consisting of the data, plus start, parity, and stop bits. The receiver section converts serial data into parallel data and verifies correct code transmission by parity checking and receipt of a valid stop bit. The programmability of this chip allows options in accepting word lengths of 5, 6, 7, or 8 bits, setting even or odd parity, and inhibition of parity generation checking. The number of stop bits can be programmed for 1, 2, or 1½ during transmission of a 5-bit code.

Absolute maximum ratings require that $V_{\rm CC}$ relative to $V_{\rm SS}$ stays between -0.3 and 7.0 V. Input voltage is constrained to these same limits. Temperature must remain between 0 and 70 °C during operation and between -55 and 150 °C in storage. The device comes in a standard 40-pin DIP. Circle 352 on Inquiry Card

1k ECL RAMs Are Second Sourced

Applications for an ECL random access memory chip produced by Fujitsu America, 2945 Kifer Ave, Santa Clara, CA 95051, include high speed scratchpad, control, and buffer storage. Organized as 1024 x 1, the MBM 10415AH is completely compatible with industry standard 10k-series ECL families, and specifically with Fairchild's 20-ns ECL RAM, the F10415A, for which it is a second source. It is produced by means of proprietary DOPOS (doped polysilicon) and IOP (isolation by oxide and polysilicon) processes, which make possible small cell and chip sizes and fast access times. Address time is 12 ns (typ), and 20 ns (max); chip select time is 5 ns (max). Power dissipation is only 0.5 mW/bit.

Memory cell selection is achieved by means of a 10-bit address. Read and write operations are controlled by the state of the active low write enable (\overline{WE}) input. With \overline{WE} and chip select (\overline{CS}) held low, data at D_{IN} are written into the addressed location. To read, \overline{WE} is held high, while \overline{CS} is held low. Data at the addressed location are then transferred to D_{OUT} and read out noninverted. Open emitter outputs are provided to allow for maxi-



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mum flexibility in output wired-or connection.

The memory is provided in a fritsealed 16-pin DIP. It is specified over a temperature range of 0 to 75 °C. Circle 353 on Inquiry Card

Track/Hold Amplifier Meets Speed Requirements Of Flash A-D Converters

An acquisition time of 10 ns and an aperture uncertainty time (jitter) of 20 ps are typical performance characteristics of the DDC-8530 track and hold amplifier. It is designed primarily for use with parallel (flash) analog to digital converters and is said to be nearly twice as fast as comparable products on the market, as well as being the smallest T/H or S/H available in its speed range.

Flash converters with parallel input comparators as used in high speed A-D conversion applications have low input impedances. In order to utilize the full capability of these converters effectively, a high speed track/hold or sample/hold unit with buffered output is required at the ADC input. This amplifier from ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716, provides a 100-MHz bandwidth input, buffered output, and the speed necessary to fulfill this requirement. It is suited for applications in high speed radar pulse processing and in video data acquisition systems.

The typical acquisition time of 10 ns to within 0.1% of final value is for a 2-V input change. With a 0.2-V input change, the acquisition time falls to 5 ns (typ) and 8 ns (max). For improved droop rate, an optional external capacitor can be used to parallel the internal holding capacitor. This will reduce the specified droop rate of 1 mV/µs at 25 °C (typ) but will increase acquisition time.

Additional characteristics include a ±0.2% max linearity error at rated load, a linearity tempco of 5 ppm/°C (typ) and 15 ppm/°C (max), and a 400-V/ μ s min slew rate. Manufactured and processed to conform to MIL-STD-883 procedures, the amplifier is available in a 24-pin double DIP. Circle 354 on Inquiry Card

Charge-Coupled Devices Perform Digitization of Picture Elements

A charge-coupled imager from Hughes Aircraft Co, Industrial Products Div, 6155 El Camino Real, Carlsbad, CA 92008, converts picture elements (pixels) into a series of pulses, with the height of each pulse being the analog of the light incident on the associated pixel. With the addition of an analog to digital circuit, the image is converted into digital data compatible with digital computers. The HCCI 032A has a 32 x 32 array imaging section of 1024 pixels, and the HCCI 100A has a 100 x 100 array of 10^4 pixels, providing 32 and 100 stages of time delay and integration, respectively. Both are illuminated register frame transfer CCDs with a buried nchannel transparent polysilicon gate structure.

These devices, called Omneye[™] imagers, are designed for use in sizing, orienting, identification, and other control functions. They offer a number



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CIRCLE 103 ON INQUIRY CARD

AROUND THE IC LOOP

of advantages over vidicons, including the inherent reliability and ruggedness of a solid state device, together with low voltage and power consumption.

Operation occurs in either of two modes—as an imager, much like a camera, or as a line scanner with time delay and integration when images are moving and maximum response with low noise is necessary. The devices offer three modes of readout. There is a burst mode in which the section clocks are "frozen" for the integration period, after which the entire frame is read out one line at a time. In the strobe illumination mode, the imager section is continu-



ously clocked while the scene is illuminated by a strobe light at one flash/frame. Finally, in the TDI mode, the image is scanned across the array in synchronization with the motion of the charge packet.

The imagers use 4-phase clocking, and both input and output registers contain an onchip 2-stage output amplifier with a 3-MHz max output rate. Signal-noise ratio measures 150 at full well.

Circle 355 on Inquiry Card

Family of Programmable IIL Chips Generates Spectrum of Sounds

Combining logic functions and linear audio circuitry on single chips, a family of circuits based on integrated injection logic (IIL) provides complex sound generation capabilities. The sN76488N from Texas Instruments Inc, po Box 84, Sherman, TX 75090, includes a noise generator, a voltage controlled oscillator (vco), and a super low frequency oscillator (SLF), together with a noise filter, mixer, attach/decay circuitry, audio amplifier, and control circuitry to provide noise, tone, low frequency sounds, and any combinations of these. Programming is accomplished via control inputs and user defined external components, allowing a wide variety of sounds to be created and tailored for particular applications. It can produce simultaneous sounds, such as musical chords, without a multiplexer, since it has an internal clock. The device is provided in a 28-pin DIP. Direct pinouts from the oscillators and a 1-shot circuit provide added design flexibility.

This circuit operates from a 7.5to 10-V supply applied to a built-in voltage regulator through the V_{CC} terminal. A regulated 5 V is available from the V_{reg} terminal to power a small amount of external circuitry or to provide a high logic level voltage to logic inputs.

Another addition to this family of circuits is the sN76487N, which is a low cost version of the sN76477N, introduced in early 1978. Available in a 16-pin package, the new model is designed for high volume, low cost applications not requiring the outputs

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CIRCLE 105 ON INQUIRY CARD

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For Detailed Specifications Circle 107

AROUND THE IC LOOP



Complex sound generator. SN76487N is implemented on single chip in IIL technology. Produced by Texas Instruments, programmable device mixes noise, tone, and low frequency sounds

and controls offered by its predecessor or by the device detailed above. Both the -88N and the -87N are TTL and Mos compatible, enabling them to be used with microprocessor based systems, or they can act as standalone devices.

The sN76489AN sound generation controller is an IIL bipolar integrated circuit designed to interface with an 8- or 16-bit microprocessor system. It contains three programmable tone generators and a white noise generator, all controlled by internal registers. In addition, each tone generator and the noise generator are connected to programmable attenuators. The outputs of the attenuators are fed into an audio summer and output buffer, which, in turn, drive an external audio power stage to drive an $8-\Omega$ speaker. Unlike the two sound generators, which are available now, this chip is to be available in the second quarter of this year.

Circle 356 on Inquiry Card

Differential Input ADC Design Emphasizes uProcessor Compatibility

A family of 8-bit CMOS successive approximation analog to digital converters utilizing differential inputs has been designed to provide compatibil-

ity with a wide range of microprocessors while eliminating the need for external interface logic. These ADCS are configured to allow operation with the standard control bus of 8080 microprocessor derivatives, with TRI-STATE^R output latches directly driving the data bus. The devices appear to

MAKE THE CONNECTION WITH ICS



debugs the initial hookup and system program. It also acts as a manual controller, checkout device or field trouble-shooting aid.

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1450 Koll Circle, Suite 105 San Jose, CA 95112 (408) 298-4844 AROUND THE IC LOOP



Fig 1 National Semiconductor's ADC0801 analog to digital converter, also designated Naked-8[™]. On highto-low transition of WR input, internal successive approximation register latches and shift registers are reset. As long as CS and WR inputs remain low, ADC will stay in reset state. Conversion will start from one to eight clock periods after at least one of these inputs makes low-to-high transition

the processor as memory locations or I/O ports, accepting active low chip select (cs), write (wR), and read (RD) inputs, and outputting an active low interrupt (INTR) (Fig 1).

This series from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, includes four models. All provide 8-bit resolution, $100 \cdot \mu s$ conversion time, and 135-ns access time. However, they differ in max total error, which is $\pm \frac{1}{4}$ LSB with full-scale adjustment for the ADC0801, $\pm \frac{1}{2}$ LSB completely unadjusted for the ADC0802, $\pm \frac{1}{4}$ LSB with full-scale adjustment for the ADC0803, and ± 1

LSB completely unadjusted for the ADC0804. The monolithic converters are fabricated using a CMOS process that adds silicon-chromium (SiCr) thin film resistors to form the internal DAC ladder.

The internal DAC resembles that used in the standard potentiometric



8-bit approximation, via capacitor C2

approach. However, the standard approach would require a series ladder of 256 resistors (2n) and 510 analog decoding switches $(2^{n+1} - 2)$ for n = 8 bits of resolution. The DAC used in this ADC family requires only 7 series resistors and a tree decoder of 24 switches. This is accomplished through the use of different resistances in different stages of the series ladder. The first three resistors in series with the positive voltage reference are of equal resistance, R. The next four resistors (the last of which leads to ground) are of a lower resistance, R/4; this section of the ladder acts as a vernier scale in the successive approximation process.

Differential inputs to the comparator select tap locations along this ladder first utilizing the coarse scale that consists of the three larger re-

sistances for a 2-bit approximation. Additional 2-bit refinement of this approximation is provided by accessing locations in the vernier part of the ladder (See Fig 2). These two steps are accomplished by first selecting the negative input to tap the location between these two ladder sections, while the positive input tests locations in the more significant (coarse) section. Then the positive tap is left fixed while the negative tap explores locations in the less significant (vernier) section. The sequence described determines the four most significant bits of the input to the comparator-that is, the more significant half byte.

Differential voltages tapped from the same ladder are also switched through a network that diminishes their effects on the comparator by a factor of 2⁴. In this phase, too, the coarse section of the ladder is used to establish the two most significant bits of the less significant half byte, and the vernier section is used to establish the two least significant bits of the less significant half byte.

A fourth pair of differential inputs to the comparator (in addition to the analog and two 4-bit reference pairs) is provided as a ½-LSB offset, utilizing ground and the center point of the grounded resistor. The comparator can directly compare the sum total of the effects of all of the differential inputs. In a charge-balancing scheme, capacitors are used to convert voltages to charges, which are then algebraically summed. The net result of the design is that the 7-resistor, 24-switch circuit performs a successive approximation that is the equivalent of that performed by the 256-resistor, 510switch standard circuit, providing 8 bits of resolution at ½-LSB (or better) accuracy over the full dynamic range.

Conversion is initiated by the standard chip select, which is decoded from the address bus, and the write strobe. When the conversion is complete, an output pin of the converter asserts an interrupt. This replaces the conventional end of conversion signal. If the ADC is restarted or if the data are read, this interrupt will automatically be reset to remove the interrupting signal. Finally, to read the digital output from the converter, the microprocessor will issue a chip select and a read strobe, which is the same as a memory read cycle. This activates tristate output buffers on the ADC and places the digital data on the bus in time to be read by the microprocessor.

Additional features of the family include standalone capability, TTL compatible logic I/O, an onchip clock generator requiring only an external RC, external clock option, a 0- to 5-V analog input range with a single 5-V supply, and the capability to operate ratiometrically or with 2.5 Vdc, 5 Vdc, or analog span adjusted voltage reference. No additional hardware is needed in microprocessor applications.

The devices are provided in 20-pin DIPs and are available in three grades with respect to operating temperature: -55 to 125 °C, -40 to 85 °C, and 0 to 70 °C. Absolute maximum ratings limit supply voltage (V_{CC}) to 6.5 V, while voltage at any input must lie between -0.3 V and V_{CC} +0.3 V. The allowable storage temperature range is -65 to 150 °C. Package dissipation at T_A = 25 °C must not exceed 875 mW.



Personal Computer for Professionals Provides Powerful Computation for Dedicated Applications

Engineering, scientific, and business professionals who require powerful computational capability but who prefer not to timeshare a large computer are now offered the HP-85 standalone computer system. Manufactured by Hewlett-Packard's Corvallis Div, the self-contained system includes central processor, CRT display, keyboard, tape cartridge, and printer in a portable typewriter size package.

Because of English-like BASIC language programming, the system is said to be easy to use by even those without previous computer experience. In addition, data can be plotted on the CRT display to clarify complex information in pictorial form, further easing system operation. Built-in interactive graphics can display or plot data on a chart or curve, which then may be output as hard copy from the built-in printer. Capabilities include 16 graphics commands, independent x and y scaling, and labels.

Design Features

The system includes 16k bytes of read/write memory (14.5k bytes available to the user), expandable with an optional plug-in memory module to 32k bytes. A 32k ROM operating system in firmware leaves most of the RAM for the user.

Storage and retrieval of programs and data are handled by the tape drive; HP data cartridges have a capacity of 217k bytes, and operate at a read/write speed of 10 in (25 cm)/s and a search speed of 60 in (152 cm)/s. A tape directory is automatically set up at the beginning of each tape.

In alphanumeric mode, the 5-in (13-cm) black and white CRT displays up to 16 lines of data at 32 char/line. With scrolling, 64 lines may be reviewed. High resolution graphics are produced in a 256 x 192-dot plotting area. The computer stores the last alphanumeric and last graphics displays, permitting the user to switch between modes without losing data.

Four sets of keyboard functions are the typewriter keyboard of 128 ASCII characters plus underlining to enter alpha data; the 20-key numeric pad to enter numbers and perform addition, subtraction, multiplication, division, exponentiation, and integer division; eight soft keys that are user assigned during program development; and display, editing, and system control keys for user control of the CRT, operating system, tape drive, and printer.

The thermal printer prints two 32-char lines/s. A 128 ASCII character set, underlined, can be printed in alphanumeric mode. For graphics mode, any plot on the CRT can be reproduced under program control



A total system measures $16.5 ext{ x } 17.8 ext{ x } 6.3''$ (41.9 x 45.2 x 15.9 cm), and weighs under 20 lb (9 kg). No fan is required because of the low power consumption of 25 W—the printer and CRT cannot operate at the same time. Quartz crystal timer accuracy for the system clock and three timers is 1 s/h depending on the line voltage.

Four I/O ports permit optional interface modules, as well as plotters, impact printers, and 5" (13-cm) floppy disc drives, when available, to expand the system for data acquisition and control applications. I/O communications are HP-IB, serial, BCD, and bit-parallel GPIO.

Software

Based on the ANSI standard, the computer's BASIC interpretive language features 12-digit accuracy, versatile string operations, editing, 42 predefined functions, and four levels of program security. Flexible output formatting allows the user to include headings, columns, and spaces. Also included are a programmable tone, remarks after any statement for documentation, multistatement lines, and timers for branching at specific times. Programs of any size may be developed in segments and combined with the chain-common command.

Nine application packages on prerecorded cartridges include BASIC training for beginners, general statistics, finance, waveform analysis, math, circuit analysis, linear programming, text editing, and games. Additional packages are under development. Other written programs will be available for a user's library. BASIC programs developed for the company's desktop computer system can be adapted to this system, as can most BASIC software that complies with the ANSI standard.

Price and Delivery

Unit price of the HP-85 computer is \$3250, with applicable OEM discounts, and units are immediately available; each application package costs \$95. A 350-page owner's manual and standard applications package of 15 programs are standard accessories. Hewlett-Packard Co, 1000 Northeast Circle Blvd, Corvallis, OR 97330. Tel: 503/757-2000.

For additional information circle 199 on inquiry card.



Digests of the latest patents from the research labs where the transistor, the bubble memory and the solid state laser were invented, each book contains a complete set of full-size reprints ($8^{1/2''} \times 11''$) of the Title Pages of all U.S. Patents assigned to each company in 1979, arranged by class, with multiple indexes and bound in individual volumes for quick and easy reference.

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Data Acquisition Modules Provide Needed Precision for High Performance Applications



A series of modular devices intended to ease data acquisition interfacing problems have been introduced for system designers. One module, the A/D/A/M-724, combines a 6.8- μ s, 14-bit A-D converter with a low feedthrough sample/hold amplifier, a pin programmable differential amplifier, and a buffer amplifier, in a single 0.375" (9.525-cm) high package

that is shielded to eliminate interface problems and to guarantee end-to-end accuracy. Also included in each module are all signal conditioning and support circuitry. Throughput rates exceed 100k measurements/s, differential nonlinearity is $\pm \frac{1}{2}$ LSB max, and nonlinearity tempco is ± 3 ppm/°C FSR max. Computer bus lines are driven directly via byte selectable, latched, 3-state outputs.

True 17-bit resolution, integral linearity within ±0.00075% (7.5 ppm) FSR, and differential linearity of ±0.00025% (2.5 ppm) FSR enable the triple-slope integrating, TTL compatible MP8037 A-D converter to fit highly precise applications. Because it automatically zeros in standby mode, referenced conversions are always guaranteed. Other features include ±5-ppm/°C gain tempco, 50-nA input current at 100 conversions/s, 1-G Ω min input impedance, and the ability to make true ratiometric measurements. A 17-bit conversion requires 4 ms max.

MP260 and MP261 sample/hold amplifiers feature sampling nonlinearity of ±0.002% FSR max and support system throughput speeds of up to 100 kHz, in 1 x 2" (2.5 x 5-cm) packages. The 260 has a 3.5-µs acquisition time; the 261 has a 20-µV/ms max droop rate. Both have 0.001% offset pedestal nonlinearity, -100-dB typ hold mode voltage feedthrough attenuation, and user selectable input configurations. Analogic Corp, Audubon Rd, Wakefield, MA 01880.

Circle 200 on Inquiry Card

Full Function Video Display Terminal Isolates Errors with Self-Diagnosis Routines

A microprocessor based smart terminal with many features found on standard intelligent terminals, the ZMS-30 Zephyr is a plug compatible replacement for some video display terminals now in use. Extensive built-in diagnostic self-test routines isolate operator or equipment errors. A 12" (30.5cm) nonglare CRT provides 24 lines of 80 char each, plus another line that displays operator error messages and terminal status information.

Editing features include full cursor addressability as well as insert and delete line or character. A protected forms mode allows complete forms to be displayed on the screen; data entry or editing can be accomplished by filling in the blanks. The displayable character set is formed on a 7 x 9 dot matrix within a 10 x 10 cell and includes the 128-char ASCII set and all control codes. Screen areas may be highlighted under program control by dim, reverse background, blinking, and underlining. Two pages of 1920 char each can be stored; a blinking underline cursor may be positioned anywhere within either page display. An integral alphanumeric keyboard is combined with a separate keypad containing an industry standard numeric entry section, cursor control keys, 12 special purpose function keys, and 16 programmable function keys that may be used in both shifted and unshifted modes. An auto-repeat feature on most keys simplifies operator entry.

Both RS-232-C and 20-mA current loop interfaces are standard. The terminal can function in either conversational



TTY mode or blocked (buffered) communications mode. The communications interface operates in either full- or halfduplex asynchronous mode at switch selectable speeds of 110 to 19.2k baud. A special monitor mode for application program debugging displays all received characters on the screen, including control codes and escape sequences. An optional serial printer interface which functions at operator selectable speeds up to 9600 baud is available. Zentec Corp, 2400 Walsh Ave, Santa Clara, CA 95050. Circle 201 on Inquiry Card



You can bet "Decitek" earned its "glitchfree" disk drive reputation honestly. And, through long experience in manufacturing computer peripherals.

For example, Decitek Punched Tape Readers are considered the "recommended reading" of the industry.

The same goes for Decitek single-sided disk drives. Decitek believes "glitch-free" is just as imperative in disk drives as in tape readers.



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Here are some of the features that give Decitek Floppy Disk Drives fail-safe dependability plus long-life with minimum maintenance.

• direct linear head positioning • microprocessor controlled drive electronics • industry compatible formats • sealed front panel • jumper configurability.

If you need single-sided drives today, go glitch-free. Get Decitek. When Decitek announces its double-sided drive you can bet it will be glitch-free, too.

Write or telephone for complete information: Decitek, 129 Flanders Road, Westboro, Massachusetts 01581, (617) 366-8334.

> Decitek Standard Floppy Disk Drive uses 8" removable diskettes singlesided, single and double density recording. 48 TPI, industry compatible formats.

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SSR UPDATE

We put a generation of know-how into this industrial I/O system



We brought you the first solid state I/O Interface modules for computerized industrial controls. With 5 years of experience to guide us, our 2nd generation I/O system (Teledyne 673 Series) features significant refinements in both modules and mounting panels.

The modules are smaller and more efficient. Transient and noise immunity so critical in industrial control applications are exceptionally high. Thermal ratings have been substantially improved. And the price is lower.

An all new mounting track design combines convenience, safety, appearance, and economy. Modules snap in and out, requiring no mounting screws. No exposed PC boards. AC and DC line voltages are kept off the board. Up to 16 modules fit on the single panel, 32 on the dual. Logic connections are made via a 20-pin edge connector or a rear-facing D connector. And again, the price is lower.

If you want the best in I/O systems compatible with today's microprocessor-based single board computers, call on the folks who started it all — Teledyne Relays.

TELEDYNE RELAYS

12525 Daphne Avenue, Hawthorne, California 90250 • (213) 777-0077 CIRCLE 111 ON INQUIRY CARD



Single-Board SMD Controller Is Fully Compatible With PDP-11 Minicomputers



Packaged on a single standard hex board, the S33/A storage module disc (SMD) controller for Digital Equipment Corp's (DEC) PDP-11 series of minicomputers is completely software compatible with DEC's RM02 I/O driver and will operate with Control Data Corp's (CDC) 9762 SMD drive and equivalent SMD drives from Ampex, Ball, and Century Data Systems. It offers media compatibility with the RM02 SMD drive and its diagnostics, and operates with DEC's RSTS/E and RSX11-M operating systems. The controller emulates the functions and operations of the DEC RH11 Massbus controller and attached RM02 disc drives; when used with 1 to 4 80M-byte CDC 9762 or equivalent storage modules, it is functionally equivalent to an RM02 subsystem of the same configuration, for a maximum SMD storage capacity of 320M bytes, unformatted.

Dual-port capability enables two controllers to access one or more common discs equipped with a dual-port option. Using a std SMD 14" (36-cm) dia removable disc pack with 5 plotters, the controller provides a formatted disc capacity of 67M bytes/drive. Data are recorded on the discs in a format identical to that of the RM02. Internal self-test is a std feature.

Redundancy and reliability enhancement are provided by error detection and isolation operations performed on all information read from the disc. An RM02 compatible header block has provisions for accepting codes to indicate that the sector is unacceptable for data storage. A 2k-byte RAM provides a 4-sector data buffer to eliminate data late errors and to enable multiple sector cross track read or write operations. A 32-bit code allows correction of a single 11-bit error burst. Offset commands cause the heads to move off the track centerline to recover data that would otherwise be lost. **Dataram Corp**, Princeton-Hightstown Rd, Cranbury, NJ 08512. Circle 202 on Inquiry Card

UPS Maintains Full Power to Micro or Minicomputer During 5-Min Line Failure

Four dc voltage outputs required for micro and minicomputer systems with floppy or Winchester disc drives are provided during power outages of up to 5 min by the model AED 401 uninterruptible power supply, enabling an orderly data transfer back to disc without loss. Power outputs provided by the UPS are 5 Vdc, 12 A for logic; 12 Vdc, 0.7 A for memory; and -5 Vdc, 0.5 A and 24 Vdc, 3.5 A for a single- or dual-floppy disc drive.

Two logic signal lines provide handshaking between the UPS and the computer. Within 10 ms after a power outage occurs, an interrupt signal from the UPS to the CPU instructs it to secure all data. Once the system has stored the data on disc, the CPU sends a shutdown signal to the power supply. When line power is restored, the UPS waits 3 s and then signals the CPU that dc power is available. An integral circuit then recharges the battery. This circuit provides a 0.3-A charge current and is optimized for a 30-V, lead acid battery (1.5- to 5-Ah battery not supplied). The battery is maintained at a 35.2-Vdc, temperature compensated float voltage, corresponding to the optimal maximum charge at a given ambient temperature. A battery saver circuit prevents excessive battery discharge, disconnecting the battery



when the terminal voltage drops to 21 ± 1 Vdc. Following an outage, the battery recharge period is normally an hour for each minute of battery powered operation. However, in most cases, normal battery capacity will allow many repetitive power interruptions within a 5-h period.

The UPS can be powered from 100-, 110-, or 220-V, 50/60-Hz lines. Dimensions are $3.5 \times 11.0 \times 6.25''$ ($8.9 \times 28 \times 15.9$ cm); weight exclusive of battery is 11.5 lb (5.2 kg). Advanced Electronics Design, Inc, 440 Potrero Ave, Sunnyvale, CA 94086. Circle 203 on Inquiry Card



10M-BYTE CARTRIDGE DISC SYSTEM



High performance system interfaces to and is software compatible with PDP-11, LSI-11, Nova, and Interdata computer systems. Disc systems include series 6000 Western Dynex cartridge disc drive and imbedded controller compatible with chosen computer system. Each system is certified to meet published specs and to be fully interface compatible and software transparent to the applicable computer system. **Datrex**, **Inc**, 3101 W Thomas Rd, Suite 109, Phoenix, AZ 85017. Circle 204 on Inquiry Card

TRANSMISSION CONVERTER AND RECEIVER

Dual-line system functions either in an independent off line mode or as the interface for on line reception of terminal transmissions by a host computer. It can operate in either an attended or unattended mode. The MSI 2732 can output to its own 1- to 4-drive diskette subsystem, functioning as a 2-line standalone receiver. It can also reformat terminal inputs for output to a local bisync port. **MSI Data Corp.** 340 Fischer Ave, Costa Mesa, CA 92626. Circle 205 on Inquiry Card

VIDEO HARDCOPY UNIT FOR MINC SYSTEMS

High resolution hard copies from DEC MINC systems—the MINC, MiniMINC, and VT105 based DECLAB-11/MNC—are produced on the desktop 4632 Option 8, with the enhancement of a circuit board replacement. Both alphanumerics and graphics are copied simultaneously. Dry-process development on dry-silver paper takes 18 s to produce the first copy and 8 s for subsequent copies of the same display. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077. Circle 206 on Inquiry Card

IC SOCKETS WITH 4-TINE CONTACTS

Low profile DIP IC sockets feature Quad-Spring stamped contacts that wipe the IC lead on all 4 sides, making contact with the face and edge of the pins at the same time. Beryllium-copper contacts are available in a closed-entry model socket of either thermoplastic (GE Valox) or high temp diallyphthalate FS-10 material. Series QS520/QS530 are available with 8 to 24 contacts in std 0.3" (0.8-cm) spacing and 24 to 40 contacts in std 0.6" (1.5-cm) spacing. **Garry Manufacturing Co**, 1010 Jersey Ave, New Brunswick, NJ 08902.



Circle 207 on Inquiry Card



National helps DEC[®] users improve their memories.



Contrary to popular belief, all memories are not created equal. And if you're a DEC user, you should know that National's boards actually operate faster than DEC's. In fact, they run at UNIBUS® cache memory speed.

The truth is, National Semiconductor offers the highest quality add-in memories available for all QBUS and UNIBUS systems, including the newly-announced PDP-11/44. That's because National's boards offer faster throughput by making basic decisions earlier in the memory access cycle.

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National's UNIBUS product line features the fastest, densest production card around, not to mention the only ECC memory available for PDP-11s.

The high-speed NS11L memory offers 128K x 18 bits, including the parity controller. The NS11E memory corrects single-bit memory errors on the fly, and still runs faster than DEC. (Double bit errors are reported as parity errors.) And both cards require DEC, UNBUS, and QBUS are registered trademarks of Digital Equipment Corporation. only +5V power and function with any PDP-11 modified, standard, or special bus.

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CIRCLE 113 ON INQUIRY CARD



TRIPLE FLOPPY DISC DRIVE SUBSYSTEM

Providing instantaneous visual diagnostics for each drive, model 4400 features a realtime indicator control panel on each drive that verifies major disc functions to facilitate development, debugging, and operation of computer systems. Subsystem incorporates 3 8" (20cm) floppy disc drives for up to 1.5M bytes. An LED display panel indicates read, write, ready, load disc, in-use, and write protect. A write protect switch safeguards the system. **Innotronics Corp**, Brooks Rd, Lincoln, MA 01773.



Circle 208 on Inquiry Card

BELL COMPATIBLE MODEM WITH INTEGRAL MULTIPLEXER



Microprocessor based T209A transmits and receives synchronous serial binary data in half- or full-duplex mode over a 4-wire line at 9600 bits/s. Integral multiplexer multiplexes various input combinations into composite 9600-bit/s data stream. Front panel switches provide self-test plus analog and digital loopback in conjunction with 11 front panel lights for malfunction isolation. **Rixon Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904. Circle 209 on Inguiry Card

2-COLOR LED PANEL LIGHTS

Bi-Color panel lights package two colors of super-bright LEDs—red, amber, or green—in a single, panel mounting enclosure. Since the two LED circuits are electrically isolated in the 4-lead package, different resistor values may be chosen for different operating voltages. The lens permits light from either LED to be presented with little attenuation. Lenses may be clear or transparent; there is room for short legends. **Data Display Products**, 303 N Oak St, Inglewood, CA 90302. Circle 210 on Inguiry Card

RS-232 SWITCH AND LINE MONITOR

GRS 232-SM8, -SM16, and -SMC each consists of a std RS-232 line monitor plus a 3-way switching unit. Units can be cascaded, offering configuration flexibility. Model GRS 232-SM8 monitors 7 RS-232 signals and switches 8 EIA pins, model GRS 232-SM16 adds switching of 8 more EIA pins to the capabilities of the -SM8. The GRS 232-SMC adds several options to the -SM16. Giltronix, Inc, 450 San Antonio Ave, Suite 44, Palo Alto, CA 94306.



Circle 211 on Inquiry Card

6250 bpi is available today for DEC & DG users



Aviv's new GCR tape systems

AVIV is delivering GCR tape systems now for NOVA/Eclipse* and PDP-11/VAX** computers. Each offers ANSI/IBM media compatibility in 6250 and 1600 bpi modes, increased data capacity and speed four times over conventional 1600 bpi systems.

AVIV's tridensity 6250/1600/800 bpi tape systems are designed for flexible system configuration, high data integrity and the highest effective throughput in the industry.

•Large record capability. •Read/write "on the fly". •4k FIFO data buffer. •45, 75 or 125 ips drives. •Imbedded controller uses one host computer slot. •2 track error correction. •Software transparent to DEC and DG operating systems. •Comprehensive diagnostics. •From \$30,200.

Other AVIV mag tape products: PE and NRZI controllers and systems for NOVA/Eclipse, PDP-11/VAX and LSI-11/23** computers. From \$3,100, OEM discounts available.



Advanced GCR/minicomputer technology. 6 Cummings Park Woburn, Massachusetts 01801

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CIRCLE 114 ON INQUIRY CARD

COMPUTER DESIGN/FEBRUARY 1980



Actual 631 images on Polaroid instant 8x10 film.

Color hard copy is finally at hand!

Color hard copy: the luminescent electronic image, captured in the permanence of photographic prints and transparencies. Dunn Instruments makes it brilliant, accurate and effortless to obtain from an affordable system. At last you can hold the new computer graphics and digital images in your hands.

The source is the 631 Color Camera System. It packs a high resolution, high linearity CRT, sophisticated optics and microprocessor exposure control into a compact, fast and friendly unit. For instant hard copy for immediate analysis, use it with Polaroid Type 808 film to make stunning 8x10 color



prints. Add the optional motordriven 35mm system for beautiful color slides. Or load 8x10 transparency film and produce images you can project overhead.

The 631 economically records the data from any raster scan CRT, for presentation, reproduction, access and display. Applications range from management information graphics to satellite remote sensing. Call or write for more information. We'll arrange for you to get your hands on actual results from the 631 Color Camera System.

Dunn Instruments, Inc., 544 Second Street, P.O. Box 77172, San Francisco, CA 94107. 415/957-1600.

DUNN INSTRUMENTS

The 631

Polaroid" is a registered trademark of the Polaroid Corporation.

LANDSAT image courtesy NASA-Ames Research. Cartographic study courtesy Harvard Laboratory for Computer Graphics. Management information graphics courtesy ISSCO.



MODEM ELIMINATOR/DRIVER



For synchronous or asynchronous operation at distances up to 400 ft (122 m), the 300 allows direct connection between terminals and computers. Digital regeneration of signals from any terminal equipment to another achieves the increased operating distance and provides the necessary EIA signal interchange between the terminals. Internal crystal controlled oscillator provides operating speeds of 2.4k, 4.8k, 9.6k, and 19.2k bits/s. **Avanti Communications Corp**, Box 205, Broadway Sta, Newport, RI 02840. Circle 212 on Inquiry Card

LSI TESTING MODULE FOR IN-CIRCUIT TEST SYSTEMS

FF303 in-circuit test systems can accommodate LSI device populated boards using this LSI testing module. Functioning with the tester hardware and the system's minicomputer, a software program subjects devices under test to actual test instructions. The CHIPS test language compiler features a software testing technique, with each LSI testing algorithm contained in a macro assembly language module. Fairchild Camera and Instrument Corp, Subassembly Test Systems Div, 299 Old Niskayuna Rd, Latham, NY 12110. Circle 213 on Inquiry Card

DUAL-SPEED 212A COMPATIBLE MODEMS

Improved versions of the Western Electric 212A data set, P-212A and -212C provide full-duplex transmission of 300or 1200-bit/s serial binary data over 2-wire dial-up lines. Automatic speed selection in the answer mode allows adjusted operation to match the transmission rate of the originating modem. Self-test during idle periods on the C version provides a constant modem condition review. A selectable delayed busy-out feature is also included. **Prentice Corp**, 795 San Antonio Rd, Palo Alto, CA 94303. Circle 214 on Inquiry Card

CENTRIFUGAL BLOWERS FOR TIGHTLY PACKED PCBS

Each of 16 UL-approved, packaged centrifugal blowers features different exhaust configurations and is designed for limited space requirements. Units deliver 290 ft³/min (8.22 m³/min) to pressurize computers and other systems to prevent dust infiltration. Height and width of units is 3.5 x 19" (8.9 x 48.3 cm) or 5.25 x 19" (13.33 x 48.3 cm). Motors require 115 V, 50/60 Hz and can be furnished to commercial, military, or EMI shielding specs. McLean Engineering Laboratories, 70 Washington Rd, Princeton Junction, NJ 08850.



Circle 215 on Inquiry Card

THE UP MEMORY

- For program loading, diagnostics, PROM emulation
- Over 1 megabits, 2.4K Baud rate, 4.8K optional
- Includes all read/write and motion electronics
- Power 1 Watt @ 5VDC, TTL I/O

Model CM-600 Mini-Dek®



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The Paper Tiger has it all. Eight softwareselectable character sizes. 80 and 132 column formats. 96 upper/lower case characters. Continuous duty cycle operation. Stepper-motor tractor feed. Forms control. Multi-part forms. Re-inking ribbon system. Microprocessor electronics. Parallel/serial interface. Self diagnostics. Paper-out sensor. Uni-directional print speeds to 198 char/sec. DotPlot[™] graphics option, with 2K buffer. And more. For a free brochure or print sample, write or call. Integral Data Systems, 14 Tech Circle, Natick, Massachusetts 01760. (617) 237-7610.



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CIRCLE 117 ON INQUIRY CARD

440

The Paper Tiger. At \$995, why settle for less.



Teach us a thing or two.

You know things we don't know.

Okay, so we're the leader in MOS and bipolar VLSI circuitry, sonar, spreadspectrum TDMA digital communication, electronically quiet radar, and much more.

Still, we need your experience and skills to stay in front.

Sure, we're the world's foremost developer of high-technology data display consoles.

Nevertheless, we want people who can figure out how to make them better.

Here at Hughes Ground Systems in a quiet part of Southern California's Orange County, we have perhaps the best undersea lab in the world.

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In this company, with management by and for engineers, risk-taking is supported, not frowned on. So if you're a venturesome electronic engineer, computer science graduate, mechanical engineer, mathematician, or physicist, we'll give you all possible recognition and reward.

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Think about bringing your training and expertise to Hughes, the company with 1,500 high-technology projects to work on—a four-billion-dollar backlog that adds up to both variety and security.

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Ground Systems Group Professional Employment Dept. DC-2 1901 W. Malvern Ave. Fullerton, CA 92634 HUGHES AIRCRAFT COMPANY GROUND SYSTEMS U.S. citizenship required. Equal Opportunity M/F/HC Employer.

CIRCLE 133 ON INQUIRY CARD

FINANCIAL DATA ENTRY TERMINAL



The 90/12 teller terminal for window applications has a 5" (13-cm) CRT display screen and typewriter style keyboard. It also functions in a 3270 compatible mode for other data entry related tasks. Keyboard contains a 58-key format, 11-key numeric keypad, 4 adding machine keys, 24 function keys, plus clear and transmit kits. A magnetic stripe card reader is optional. CRT displays 6, 8, or 12 lines of 40 alphabetic and numeric char each. Bunker Ramo Corp, Information Systems Div, 35 Nutmeg Dr, Trumbull, CT 06609 CIRCLE 264 ON INQUIRY CARD

FLAT CABLE DIP CONNECTORS

Connecting flat cable to PC boards permanently by DIP soldering, mass terminating system terminates 1.27-mm center spaced flat cables of 10 to 60 conductors. U-shaped contacts, gold plated over phosphor bronze, ensure corrosionresistant gas tight connection. Manufactured with solvent-resistant resin, connectors mate with std IC sockets. Also featured are dual-inline terminals and low profile of 5.3 mm above the PC board. **Fujitsu America, Inc, Component Sales Div**, 910 Sherwood Dr, Lake Bluff, IL 60044.

CIRCLE 265 ON INQUIRY CARD

PORTABLE INTERFACE TESTER



Battery powered tester monitors and breaks out the RS-232/V.24 interface between a modem and a terminal. Datacheck-VF can also monitor audio signals found on dedicated or dial voice communications channels. An internal amplifier and speaker with level control provide signal monitoring over a 3- to -50-dBm range. Noise and crosstalk can be detected on the communications channel. Navtel Limited, 8481 Keele St, Concord, Ontario L4K 1B1, Canada. CIRCLE 266 ON INQUIRY CARD

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"NJE Power Supplies and Systems are THE BEST INVESTMENT in terms of watt hours per dollar of any available anywhere!"

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The same model can handle both 50Hz and 60Hz inputs. MTBF's in excess of 100,000 hrs. and efficiencies from 70% to 85%. Output power to 1000 watts. Densities up to 0.9 watts per cubic inch.

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High reliability, excellent line and load regulation, very low output ripple and noise, fast transient response, and remote control capability. Outputs available to 500 volts.

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POWER SYSTEMS



Incorporate up to eight modular supplies in one rack assembly. Systems may be tailored to your custom requirements by incorporating options from the extensive list available including panel metering, individual controls, test jacks, redundancy and load sharing. Combinations of ferroresonant and series regulated supplies may be accommodated.



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COLOR DISPLAY MONITORS



Offering 20-MHz (\pm 1 dB) bandwidth, switchable 4:3 and 1:1 aspect ratios, and improved convergence controls, CDCT 3 series monitors replace the CDCT 2 line. Models 3/37 and 3/51 are offered in both std and high resolution versions. All models are equipped with a 90° shadow mask CRT. High resolution versions incorporate a CRT with 4 times as many dots as the standard. **E & O Systems, Ltd**, 2998 Scott Blvd, Santa Clara, CA 95050. Circle 216 on Inquiry Card

RIBBON CABLE ASSEMBLIES

Preterminated assemblies with up to 28 conductors mate with 0.025" (0.064-cm) square inline posts on 0.100" (0.254-cm) centers mounted on PC laminates. For 0.045" (0.114-cm) square or round posts on 0.156" (0.396-cm) centers, up to 24 conductors are available. Styles include jumpers, daisy chain, and single-ended types. One end can be full or partially stripped. Connector housings are 94V-2 flame retardant thermoplastic and contacts are copper alloy with gold or tin plating. **AMP Inc**, Harrisburg, PA 17105. Circle 217 on Inquiry Card

PRECISION 3-TERMINAL FIXED VOLTAGE REGULATORS

MC7800A series 3-terminal fixed voltage regulators offer 2% output voltage tolerance. The devices employ internal current limiting, thermal shutdown, and safe-area compensation. With adequate heatsinking, they can deliver output currents in excess of 1 A. The devices are available in temperature ranges of 0 to 125 and -55 to 150 °C; case options are TO-220 plastic and TO-3 metal. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036. Circle 218 on Inquiry Card



PREASSEMBLED PRESS FIT CARD EDGE CONNECTOR



Connector consists of an insulator and contact assembly that is pressed into the motherboard by means of simple tooling. Insertion forces are low due to compliant press fit section on the pins; press fit joint makes both mechanical and electrical connections in one operation. Connectors are selfaligning with proven gas tight press fit joint insuring a reliable connection. **Elco Corp, Interconnect Systems Div,** 2250 Park PI, El Segundo, CA 90245. Circle 219 on Inquiry Card

MAGNETIC TAPE SYSTEM

MTS 1050-22 is an IBM/ANSI compatible 0.5" (1.3-cm) digital tape system. Designed to operate with Data General RTOS and RDOS software, the system requires one 15 x 15" (38 x 38-cm) PCB adapter to occupy one slot in the computer chassis. The system consists of TDI 1050 tape transport and TDF 4050 formatter. It provides dual-density, 9-track, 45 in(114 cm)/s, having both NRZI and PE recording/playback capability. **Innovative Data Technology**, 4060 Morena Blvd, San Diego, CA 92117. Circle 220 on Inquiry Card

PRECISION A-D CONVERTER

Converter combines 15-ms conversion time and $\pm 0.003\%$ accuracy with 16-bit binary or 2's complement resolution and a linearity of $\pm 0.0015\%$. Model ADC 1216 is a self-contained unit for digitizing high speed analog input signals. The converters are fully assembled, tested, and calibrated system ready modules. The only external requirement is a power supply input; no external voltage source or amplifiers are required. **Phoenix Data, Inc,** 3384 W Osborn Rd, Phoenix, AZ 85017.



COMPUTER DESIGN/FEBRUARY 1980

Circle 221 on Inquiry Card

6800 EXORciser Users...

YOUR DREAM OF MEMORY EXPANSION HAS JUST COME TRUE

The new STORAGE DEMON Memory System brings you high performance 10 Megabyte storage capabilities for your EXORcisor I, II, or III system. This high speed, high reliability Winchester technology system means virtually trouble-free operation in almost any environment.

> The STORAGE DEMON is fully supported by SOFTWARE DYNAMICS' new SDOS interruptdriven disk operating system. It features:

- □ Keyboard Typeahead
- Automatic Disk Readahead
- Automatic Disk Sector Pooling
- Dynamic Files With Random Access To Byte
- Complete Device Independence

CIRCLE 121 ON INQUIRY CARD

SDOS supports EXORdisk I, II, and III, and permits you to use your existing floppy disk drives for additional memory storage and/or as back-up for the Winchester hard disk. The STORAGE DEMON utilizes the field-proven, dependable LOBO DRIVES INTERNA-TIONAL 10 Megabyte hard disk and controller and comes with the famous LOBO DRIVES 1 year, 100% warranty.

33

Make your dream of expanded memory come true...Write, call or mail the coupon today.



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You've got my attention, DEMON Memory System	tell me more about: □ STORAGE 6800 Development Software or Pkg. □ BASIC Compiler
Name	Title
Company	
Address	and the second
City, State, Zip	
Phone	

225



80-COL OCR AND **BAR CODE PRINTER**



M80 MC, a 200-char/s matrix serial printer, features microprocessor controlled logic seeking bidirectional printing. Printheads allow choice of OCR A and OCR B, bar code, and upper/lower case (with descenders) char styles. Pitch is alterable for 10, 12, 14, or 16.5 char/in (4, 5, 5.5, or 6/cm); 3 matrix heads provide 7 x 7, 7 x 9, or 9 x 9. Printhead automatically adjusts itself to accommodate varying form thick-nesses. Tally Corp, 8301 S 180th St, Kent, WA 98031.

Circle 222 on Inquiry Card

10.4M-BYTE CARTRIDGE DISC DRIVE

Rackmountable, toploading RL02 employs the dual-density, 5440 type disc cartridge as storage medium. It operates on all PDP-11 based minicomputer systems, PDP-11/03L and -11/23 based microcomputer systems, and PDP-8/A systems. A subsystem configuration consists of a disc drive and controller. Up to 3 additional drives can be supported by the controller. With a max of 2 controllers per CPU, total storage capacity of max configuration is >83M bytes. Digital Equipment Corp, Maynard, MA 01754.

Circle 223 on Inquiry Card

SILICONE-POTTED LIGHTED **PUSHBUTTON SWITCHES**

Silicone-potted lamps in this series of pushbutton switches are said to result in fewer lamp failures in applications subject to shock and/or vibration. Ratings are up to 10 A, 125/150 Vac. Snap-in mounting and quick-connect or solder type terminals ease installation. Behind panel depth is 1" (2.54 cm). Oslo Controls Inc, 328 Industrial Ave, Cheshire, CT 06410.

Circle 224 on Inquiry Card

DUAL-OUTPUT DC POWER SUPPLY



Model HCC24-2.4 is another addition to the Hi-Vol series line. The unit outputs ±18 to ±24 V at 2.4 A, continuously variable. Std features include 115/ 230-Vac ±10% ac input capabilities, ±0.05% line and load regulation, and full protection against short circuit and overload. Max output ripple is 5 mV pk-pk while the full load operating temperature specs are 0 to 50 °C, derated to 71 °C. Power-One, Inc, Power One Dr, Camarillo, CA 93010. Circle 225 on Inquiry Card



New on the North Star Horizon: 18Mb Hard Disk Drive!



Horizon Computer with 64K RAM and dual quad capacity (720kb) floppy disks

Up to four 18Mb Winchestertype hard disk drives

Display terminal

Letter-quality or dot matrix printer

Horizon I/O flexibility allows expansion to meet your needs

Unsurpassed Performance and Capacity!

North Star now gives you hard disk capacity and processing performance never before possible at such a low price! Horizon is a proven, reliable, affordable computer system with unique hardware and software. Now the Horizon's capabilities are expanded to meet your growing system requirements. In addition to hard disk performance, the Horizon has I/O versatility and an optional hardware floating point board for high-performance number crunching. The North Star large disk is a Century Data Marksman, a Winchester-type drive that holds 18 million bytes of formatted data. The North Star controller interfaces the drive(s) to the Horizon and takes full advantage



North Star Computers Inc. 1440 Fourth St. Berkeley, CA 94710 (415) 527-6950 TWX/Telex 910-366-7001 of the high-performance characteristics of the drive. Our hard disk operating system implements a powerful file system as well as backup and recovery on floppy diskette.

Software Is The Key!

The Horizon's success to date has been built on the quality of its system software (BASIC, DOS, PASCAL) and the very broad range and availability of application software. This reputation continues with our new hard disk system. Existing software is upward compatible for use with the hard disk system. And, with the dramatic increase in on-line storage and speed, there will be a continually expanding library of readily available application software. For further information, contact the OEM sales department at North Star Computers Inc.

North Star OEM System Prices

HORIZON — HD-1 Horizon computer with 64K RAM, 2 quad capacity mini drives and one HD-18 hard disk drive \$5880* HD-18 Additional 18Mb hard disk drive for expansion of HD-1, or your present Horizon \$3150

*in OEM quantities

CIRCLE 124 ON INQUIRY CARD



DELAYED SWEEP OSCILLOSCOPE



Model 1530, a 30-MHz scope, uses delayed sweep to evaluate digital pulse trains and other complex waveforms. Min expansion at 30 MHz is five times. Features include variable hold-off, high triggering sensitivity, and flat response. Chop or alternate modes of dual-trace display are selectable. Five ranges of time base delay are from 1 μ s to 100 ms with vernier adjustment. Vertical input sensitivity is 2 mV/division. **B&K-Precision/Dynascan Corp**, 6460 W Cortland St, Chicago, IL 60635.

Circle 226 on Inquiry Card

IEEE 488 BUS INTERFACE MODULE

All handshake protocols for controlling and moving data between multiple instruments on the IEEE 488 instrument bus are automatically handled by this module. The MC68488 general purpose interface adapter performs talker and listener functions; these include primary address recognition, secondary address capability, and programmable interrupts. The software driver BUSCON performs system controller functions such as receive or pass control from or to another controller. **Wintek Corp**, 1801 S St, Lafayette, IN 47904. Circle 227 on Inquiry Card

100-W OPEN FRAME SINGLE-OUTPUT SWITCHER

Intended for OEMs, PD 100 100-W power supply features 115/230-Vac input voltage, 70 to 75% efficiency, with 30-ms typ holdup time. Designed to meet UL, VDE, and CSA specs, the unit's standard output voltages are from 2 to 48 Vdc. Temperature ranges are -40 to 85 °C storage, and 0 to 50 °C operating. 2.75 x 4 x 9.5" (6.99 x 10 x 24.1 cm) unit offers overvoltage and reverse voltage protection. **Power Dynamics Corp**, 9421 Telfair Ave, Sun Valley, CA 91352. Circle 228 on Inquiry Card

ELECTROSENSITIVE MATRIX PRINTER



power consumption, medium Low speed, and silent operation are achieved with the ESP40. Primarily used as a 40-char alphanumeric printer operating with 2 line shift increments, the device uses electrosensitive paper; 4 fonts are selectable. Operation is in local or online mode from a 12-V system. Print rate is 280 char/s sync for 80 char/line. Data line buffer is 320 char deep. Self-checking is optional. Rank Numbering Machines, Inc, Printer Div, 411 E Jarvis Ave, Des Plaines, IL 60018. Circle 229 on Inquiry Card



950 Dovlen Place, Suite B, Carson, Ca. 90746

(213) 538-2254



(213) 538-4251

Little Impact.

Meet the IMPs. A pair of stylish 3½ inch high impact printers that will look great on any desk.

Styled for desk top use, these sleek units stand just 3½ inches high, yet the unique fan-cooled printing system can knock out 80, 96 or 132 columns of crisp hardcopy with continuous throughput of one line per second.

A winning pair. IMP-1, with friction feed, can make multi-copies on plain 8½ inch wide paper, or on teletype rolls. In addition, IMP-2 has tractor feed and full forms control, with tractors adjustable from 1 inch to 9½ inches.

Interfaces abound. All IMPs have Centronics parallel and RS232C/20mA serial inputs as standard equipment. But if you need something different, then we make interfaces for just about any system — high speed serial, Apple, Pet, TRS-80, IEEE 488... **Versatile, too.** 96 ASCII character set is standard. And you can select 6 character sizes, even graphics, under software control. Options include 2K buffering and special character sets.

Service — a big difference. No other printer manufacturer offers Axiom's combination of low cost and nation-wide service and distribution — in the USA and eighteen overseas countries.

Pssst — the price!!! It's low. \$695 for IMP-1. \$795 for IMP-2. And that's the single unit price.

Better phone, write or mail the bingo card today!



5932 San Fernando Road, Glendale, CA 91202 Tel: (213) 245-9244 • TWX: 910-497-2283 CIRCLE 127 ON INQUIRY CARD



LOW PROFILE INDICATING FUSEHOLDERS



Two series of square cap fuseholders that light when the fuse blows snap into a 0.625" (1.588-cm) square mounting hole without mounting hardware. Available with 0.1875" (0.476-cm) combination quick-connect/solder terminals (344600 series) or 0.25" (0.635-cm) quick-connect/solder terminals (344800 series), devices may be ordered with 120- or 240-V neon lamps or with 6-, 14-, or 28-V incandescent lamps. They are rated at 15 A to the max voltage of the lamp. Littelfuse, Inc, 800 E Northwest Hwy, Des Plaines, IL 60016. Circle 230 on Inquiry Card

SERIAL PRINTER FOR 3270 SYSTEM

The 6541 printer directly replaces the IBM 3284 and 3286 printers used with the 3270 Information Display System. Performance is said to increase from 227 to 375%. Bidirectional printing produces 150 char/s along a print line of 132 columns. Individual char from a set of 64 are formed by a 9 x 7 dot matrix. **Decision Data Computer Corp**, 100 Witmer Rd, Horsham, PA 19044.



Circle 231 on Inquiry Card

12-BIT DAC

High output current capability of 50 mA, max glitch energy of 5000 mV-ns, and linearity error of only $\pm 0.0125\%$ are specs of the TTL compatible DAC-LGT. Settling time for 1-LSB input change is 50 ns typ and 400 ns typ for a full-scale input change. Unit has

a low skew digital input register and an internal reference. Pin programmable voltage ranges are ± 2.5 , ± 5 , ± 10 , 0 to -5, and 0 to -10 V. Coding is binary or offset binary; ± 15 - and 5-V power supplies are required. **ILC Data Device Corp**, Airport International Plaza, Bohemia, NY 11716. Circle 232 on Inquiry Card

LITHIUM CELLS FOR PERMANENT PCB MOUNTING



For permanent PCB mounting as long term (10+ yr) continuous or standby power sources for CMOS circuits, microprocessors, memories, sensor circuits, and emergency and unattended equipment, lithium thionyl chloride cells feature high energy density and cell voltage of 3.4 V. Discharge curves remain flat throughout cell life. Cells will not explode or release gases even if short-circuited. Op temp range, -55 to 75 °C. **Plainview Electronics Corp**, 8 Manetto Hill Rd, Plainview, NY 11803. Circle 233 on Inquiry Card

MARKETING CONSULTANTS We wish to retain marketing consultants to prepare market research reports analyzing and forecasting the market for the following: Security Equipment **Personal Identification Products Computer and Communications Security** Equipment All replies will be kept strictly confidential. Fees will be paid commensurate with qualifications. We are an internationally known firm and can provide continuous assignments. Magnetic Shielding by Eagle CUSTOM SHIELDS • STANDARD SHIELDS • FINISHING • DESIGN ENGINEERING • FOIL • HEAT TREATING • SHEET • TESTING • CONSULTING • FABRICATION Eagle can help improve your Choose from a wide selecproduct, and lower costs, by tion of sheet and foil, so you designing the right shield can form your own shields. for you. Take advantage For helpful design and of Eagle's vast backcost data, write or call. Offices worldwide. FROST & SULLIVAN ground in shield design and production. P.O. BOX 24283 . INDIANAPOLIS. INDIANA, 46224 . PHONE (317)297-103

CIRCLE 128 ON INQUIRY CARD



Meet the Mini Wini." The new 8" fixed disk drive that stores 20 megabytes.

It's the lowest-cost way of getting 20 megabytes in an 8" floppy slot. And with Winchester-type technology, to boot. So you can expand the on-line capacity of your present desk-top system without having to redesign one bit of your present chassis.

Interfacing?

It's a snap. The Mini-Wini (alias the PCC D8000 fixed disk) has a microprocessor-controlled interface, featuring a bidirectional command/status bus and serial data transfer. It's easier and simpler to design the CPU interface.

And maybe best of all, it's made by Pertec Computer Corporation. At PCC, we don't just innovate. We have the production capacity to supply those innovative products when we say we will. Which is reassuring.

The PCC Mini-Wini. Small size. Big capacity. Call us for details.



For further information, call toll-free 800-528-6050, Ext. 1323.



14-BIT DIGITAL TO SYNCHRO CONVERTER



14-bit resolution synchro driver series B1670 positions up to 3 size 11 torque receivers (TRs) with an accuracy of ± 4 arc min. Units will switch TRs through 180° step and are protected against shorts and synchro load malfunctions. Low power TTL input registers enable units to be paralleled and multiplexed. Internal damping prevents current surges for smooth rotation and oscillation-free settling. **Transmagnetics**, **Inc**, 210 Adams Blvd, Farmingdale, NY 11735. Circle 234 on Inquiry Card

FIBER OPTIC EMITTER AND DETECTOR

IRE-170 a visible LED coupled to 30 cm of DuPont PIR-40 step index fiber and terminated in an AMP #530530 F/O connector typ yields 5 μ W into the fiber at 100-mA dc drive. Peak wavelength is 670 nm with typ rise and fall time of 70 ns. DIR-170 high speed silicon PIN detector, similarly coupled and terminated, has responsivity of 0.2 A/W at 670 nm with good sensitivity from 350 to 1150 nm. Typ rise/fall times are 3 ns at 100 V bias. Laser Diode Laboratories, Inc, 1130 Somerset St, New Brunswick, NJ 08901.

Circle 235 on Inquiry Card

WAVE SOLDERABLE TOGGLE SWITCH

The E100 series blocks the 3 potential leakage paths for flux and solvents to prevent contamination from wave soldering during PC board assembly. Terminals are epoxy sealed to the case; the toggle is sealed by an internal Oring; and the top and bottom of the case are made from high temp thermoplastic and are ultrasonically bonded together. Available are 2 toggle lengths, 4 terminal lengths, 4 mounting versions, and 5 function options. **C&K Components, Inc,** 15 Riverdale Ave, Newton, MA 02158. Circle 236 on Inquiry Card

FLOPPY DISC MASS STORAGE SUBSYSTEM

A double-sided, single-density subsystem, the 3442 provides direct access at low cost. It stores approx 600k bytes/ diskette, with a transfer rate of 250k bits/s. As many as 4 floppy drives can be supported by a single microprocessor based controller, for over 2M formatted data bytes of storage capacity. The subsystem also includes automatic track verification and standard write protect. **General Automation**, **Inc**, 1055 S East St, Anaheim, CA 92803.



Circle 237 on Inquiry Card



CIRCLE 131 ON INQUIRY CARD

CIRCLE 132 ON INQUIRY CARD

Innovations are what make Control Data's new tape drive so exceptionally reliable.





Now with the introduction of our new 9214X tension arm tape transport, OEM's can incorporate exceptionally reliable tape capabilities into their design. And at low costs of acquisition and ownership.

Technical innovations like microprocessor

control, solid-state write enable sensing, and a design with fewer parts have brought 5000 hour MTBF reliability to half-inch tape.

Our optional *embedded* formatter simplifies interfacing and provides multiple-drive capability of up to four drives. The formatter can be moved from drive to drive quickly, if necessary.

Your customer will appreciate the easy tape loading and quiet operation. Low power consumption and a compact design save energy and space. And this newest member of Control Data's family of OEM tape equipment completes our line—now we can satisfy your requirements for high-speed, mediumspeed and low-speed tape peripherals.

Put quality behind your nameplate. For more information, call us at 612/853-3180. In Europe, contact one of our European representatives. Or return coupon to:

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Addressing society's major needs



LIGHTWEIGHT PORTABLE DATA ANALYZER



Microprocessor controlled Maxichek isolates faults in telecommunications networks either by simulating computer terminals or the CPU, or by performing bit or block error rate tests to check modems and phone lines. The 2.5 x 5.75 x 7.5" (6.4 x 14.61 x 19.1-cm) device connects with communications links using std EIA RS-232-C or CCITT interfaces. Speeds are 110 to 9600 bits/s (async) and up to 19.2k bits/s (sync). **Astrocom Corp**, 120 W Plato Blvd, St Paul, MN 55107. Circle 238 on Inquiry Card

VMOS FET FAMILIES

Additions to VMOS power FETs include the IVN5000 family and 30 direct replacements for Siliconix devices. Members of the IVN5000 family are proprietary n-channel, enhancement mode power FETs rated at 2.5 Ω on resistance and available in ultra-small TO-52 and TO-237 packages. The Siliconix compatible devices are function for function and pin for pin replacements for the VN30A, -35A, -46A, -66A, -67A, -88A, -90A, -98A, and -99A device families. Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014.

Circle 239 on Inquiry Card

SMALL SIZE HYBRID STEPPER MOTOR

50-mm long x 32-mm dia hybrid stepper motor in size 13 case develops holding torque of more than 600 g/cm and running torque greater than 500 g/cm. Resolution is 200 or 400 steps/r. Unit is designed to supplement existing ranges of size 23 and 34 hybrids, variable reluctance, and permanent magnet types. Motor can be used as drive or positioning device in instruments, process control, business machines, and opto-electronic systems. **Muirhead-Vactric Div, Muirhead, Inc,** 1101 Bristol Rd, Mountainside, NJ 07092. Circle 240 on Inquiry Card

LOW COST 35-MHz SCOPE

35-MHz, dual-channel, portable oscilloscope with chop frequency of 500 kHz and with alternate sweep and calibrated delay capabilities is comparable to the Tektronix T935A, but offers improved performance characteristics and specs. Horizontal axis sweep time for channel A (main sweep) and channel B (delayed sweep) is 0.1 μ s/div to 0.5 s/div in 21 steps. A 10X magnification can accelerate the sweep time to 10 ns/div to 50 ms/div. **Kikusui International Corp**, 17121 S Central Ave, Unit #2M, Carson, CA 90746.



Circle 241 on Inquiry Card

Girl-meets-flat-cable and lives happily ever after.

See page 46

19" RACKMOUNT TERMINAL



Requiring only 7" (18 cm) of panel space, the R301 19" (48-cm) rackmount computer terminal includes a 6" (15-cm) diagonal display monitor, alphanumeric keyboard, logic, and power supply. The ruggedized unit features full/half-duplex, RS-232/20-mA loop interfacing, and transmission rates from 110 to 9600 baud. Std display format is 32 columns by 16 lines, with 64 columns by 16 lines optional. Three-quarter size keyboard can be removed from the panel and used up to 8' (2.4 m) away. **Informer, Inc**, 8332 Osage Ave, Los Angeles, CA 90045.

Circle 242 on Inquiry Card

WIDE INPUT VOLTAGE RANGE DC-DC CONVERTERS

Hi-power series converters operate with typ efficiency of 65% over input ranges of 4.5 to 6.5, 9 to 18, 18 to 36, and 36 to 54 Vdc; within each input range 5-, 12-, 15-, ±12-, and ±15-Vdc output voltage models are available. All units employ an input filter to minimize emi/rfi reflected ripple current and are fully isolated with continuous short circuit protection. **Calex Manufacturing Co, Inc**, 3355 Vincent Rd, Pleasant Hill, CA 94523. Circle 243 on Inquiry Card

QUAD SIZE MAGNETIC-TAPE COUPLER

Intelligent magnetic tape coupler includes TM-11 emulation circuitry plus circuitry to handle streamer mode operation. Model DQ130 interfaces most industry compatible imbedded formatter, dual-density (NRZI/PE) magnetic tape drives to a CPU. Self-contained single quad size module requires only 3.5 A from the CPU. The unit physically couples up to 2 formatted tape drives, with 3 slave units each, for a total of 8 drives from an LSI-11 Q-bus slot. **Distributed Logic Corp**, 12800-G Garden Grove Blvd, Garden Grove, CA 92643.



Circle 244 on Inquiry Card

Introducing the new BASF 6170 Series 210mm Fixed Disk Drives.

High Performance. Perfect for multi-user multi-tasking applications, the BASF 6170 Series drives give you an average time-to-data of 50 milliseconds...four to seven times faster than standard 8" floppy drives.

Capacity. The BASF Model 6171 provides 8 megabytes and the Model 6172 provides 24 megabytes of fully usable unformatted capacity. Unique BASF circuitry eliminates user mapping.

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Invitations are available from participating companies or the ICC sponsor. For further information contact: B.J. Johnson & Associates, 2503 Eastbluff Drive, No. 203, Newport Beach, CA 92660. (714) 644-6037



DUAL-PLANE DRAWER



Model LPD-11 holds 4 full panels, 16pin pattern or universal dual-contact (D/C) pin socket panels, and provides from 30 to 720 IC positions with up to 1200 I/O connections. D/C interconnect panels allow either facewipe or edgewipe interface between wirewrap pin socket and IC lead frame. I/O panels are provided with cutouts for 1 to 10 connectors; covers are provided over these cutouts if connectors are not supplied. **Scanbe Div of Zero Corp**, 3445 Fletcher Ave, El Monte, CA 91731. Circle 245 on Inquiry Card

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DIP NON-NOBLE RESISTOR NETWORKS

Epoxy transfer-molded series 500 networks in 14- and 16-pin packages are suited for machine insertion. Schematics include N-1 with common lead, and N/2 isolated resistors. Patented nonnoble resistive materials such as TanTin[™] are fired in inert nitrogen gas at 1000 °C. Conductors are compatible thick film copper, also fired at high temps. Over 50 std resistances are available from 33 to 1M Ω in either ± 2 or $\pm 5\%$ tolerance. Power ratings at 25 °C range from 1.625 to 2.0 W/package, or 0.125 to 0.25 W/resistor. TRW/IRC Resistors, PO Box 1860, Boone, NC 28607. Circle 246 on Inquiry Card

900-CHAR/S MATRIX PRINTER



Designated model 600C, this enhanced model 600A offers compressed print of 900 char/s in 15-pitch font. Also featured are 600-char/s printing in a 10pitch font and selectable 6- or 8-line/ in (2 or 3/cm) formats. Full 96-char set, 894-char buffer, adjustable tractors, elongated char, and multipart forms are std. Print speed results in throughput capabilities that are better than those of 600-line/min printers. Florida Data Corp, 3308 New Haven Ave, West Melbourne, FL 32901. Circle 247 on Inguiry Card

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LOW SPEED OEM TAPE TRANSPORTS

Tension arm magnetic tape transports that operate at speeds ranging from 18.75 to 45 in (47.62 to 114.3 cm)/s, 92140 series single capstan drives read and write std 9-track data in densities of 800 and 1600 bits/in (314 and 629/cm) using NRZI and PE modes, respectively. All transports provide microprocessor based control logic, and microdiagnostic aids to simplify maintenance. An optional embedded formatter is available with dual recording modes and is contained on a single PC board, enabling the unit to be switched from 1 transport to another. Daisy chain connection of up to 4 tape transports is also optional. **Control Data Corp**, PO Box O, Minneapolis, MN 55440. Circle 250 on Inquiry Card

VOICE DIGITIZER

Microprocessor based Digi-phoneTM converts voice into a 2400-bit/s digital signal that can be multiplexed with data and other digital voice signals to greatly reduce communications costs. A dial option is also available for digitizing



conventional dial and tone signaling to establish std telephone access to the user's networks. Other advantages include increased network flexibility, and elimination of separate voice and data transmission

facilities. A commercial encryption unit may be added to provide max security of voice communications. **Codex Corp**, 20 Cabot Blvd, Mansfield, MA 02048. Circle 251 on Inquiry Card
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8-bit parallel STR-110 allows memory dumps or program loading up to 125 characters per second. \$1328 in single quantity.

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STR-810 digital cartridge recorder, designed for use with 3M DC-300A tape cartridge, allows OEMs designers to do their own formatting, select tape speeds, and choose read/write heads with from 1 to 4 tracks for remote data logging, data



acquisition, and disc backup systems. Data rate, packing density, and formats can also be selected. Optional ANSI X3.56 formatter turns the unit into a plug-in component. There are no moving parts except the car-

tridge engagement cam. An LED is used to sense EOT/BOT, and the drive meets ANSI specs for cartridge to head positioning. Under microprocessor control, the recorder monitors its own tape movement. Fault indications are provided for tape underspeed, acceleration, time out, and position. **Electronic Processors, Inc,** 1265 W Dartmouth Ave, Englewood, CO 80110. Circle 252 on Inquiry Card

LSI-11 COMPATIBLE ANALOG INPUT BOARD

Two 32-channel, plug-in compatible analog input systems interface directly with DEC's LSI-11, LSI-11/2, LSI-11/23, PDP-11/03, and PDP-11/23 microcomputers, accept inputs ranging from 10 mV to 10 V, and offer 12-bit resolution. MP1216-PGA includes an onboard amplifier that is software programmable allowing the host computer to select gains from 1 to 1024 V/V. An onboard RAM stores each channel's gain level and automatically sets gain (without software or operator involvement) when a channel is addressed. MP1216, with a resistor programmed amplifier, offers gains to 1000. It also features a unique software selectable delay/no-delay feature. Delay time from 18 to 70 μ s is hardwired on the board to allow for settling time at various gains. **Burr-Brown Research Corp**, International Airport Industrial Pk, Tucson, AZ 85734.

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WIDE LOAD RANGE SWITCHING POWER SUPPLIES



XL series models can handle a wide load range on all outputs while providing tight regulation, and maintaining compatibility with ac line voltages and frequencies in use worldwide. To do this, the series uses an output regulation technique that maintains good regulation on both secondary and primary outputs at up to 5 times the load range of previous standardized switching supplies. 25-W XL25, 75-W XL75, and 130-W XL130 have user selectable ac power line voltage ranges of 90 to 130 and 180 to 265 V; ac frequencies can vary from 47 to 440 Hz on either range. All have a 5-V primary output with \pm 1% regulation over a 5:1 load change; and -5-, 12-, and -12-V secondary outputs with \pm 3% regulation over a 10:1 load change. **Boschert Inc**, 384 Santa Trinita, Sunnyvale, CA 94086. Circle 254 on Inquiry Card

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For all the facts on these exciting new open-chassis monitors, contact your local Sanyo sales representative listed below.



Contact your nearest Sanyo rep: AKRON: Avcom, Inc. (216) 777-2060 ATLANTA: Len Elliott Company (404) 875-9701 ATLANTIC CITY: Austin Associates (609) 871-9290 BALTIMORE: David H. Brothers, Inc. (301) 764-7189 BOSTON: Piper Associates (617) 449-1144 CHICAGO: George Petit Company, Inc. (312) 261-0342 DALLAS: The Crockett Sales Co. (214) 748-8209 DENVER: Mile-High Marketing (303) 457-2058 DETROIT: Burcaw Co. & Associates (313) 533-7700 INDIANAPOLIS: Midwest Rep. & Assoc., Inc. (317) 844-4555 KANSAS CITY: Pacer Sales Corporation (816) 358-6610 SA DESCORDER (816) 358-650 LOS ANGELES: Marketing Specialists (213) 341-1471 MIAMI: L. Haas Company (305) 945-6544 PORTLAND: Eart & Brown Co., Inc. (503) 245-2283 SAN FRANCISCO: Tech-Rep Associates (415) 785-4531 SEATTLE: Eart & Brown Co., Inc. (206) 284-1121 ST. PAUL: Skor, Inc. (612) 645-6461 WHITE PLAINS: Irving Langbaum Assoc., Inc. (914) 634-1141 © 1979 Sanyo Electric Inc., Compton, CA 90220



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20M-BYTE 8" WINCHESTER DISC DRIVE



Series 7000 drives have unformatted capacities of 4M bytes in the single-disc version, 12M bytes in the double-platter model, and 20M bytes in the 3-disc unit. Two drives mount side by side in a std 18" (46cm) rack. Data transfer rates

are 5.5M bits/s. Using Winchester technique, an ironless rotary actuator accurately positions the read/write heads in response to prerecorded servo tracks on the lower side of the bottom disc. Lightly loaded (9.5 g) heads fly at 10 μ in (0.025 μ m) above the recording surface and land in lubricated areas adjacent to the tracks, preventing head damage or lost data. Recoverable read errors are 1 in 10¹⁰ bits transferred. Track to track time is 12 ms, while avg head movement time is 50 ms, with 100-ms worst case max. **Kennedy Co**, 1600 S Shamrock Ave, Monrovia, CA 91001. Circle 255 on Inquiry Card

MINIATURE ALPHANUMERIC THERMAL PRINTER

A miniature 20-col panel-mount printer weighing 4.25 lb (1.9 kg) uses only 2 input data wires to simplify user interfacing. Internal microprocessor and serial port reduce circuit complexity so that all electronics are contained inside the printer housing. APP-20A2 prints up to 96 ASCII alphanumeric char at up to 1.2 lines/s (24 char/s) at high baud rates. Basic print and advance period is 720 ms/line with the rest consumed by data char input buffer loading. Printer life is 30M lines (600M char) typ. Optional OEM pin functions are included on the rear connector, including pin selection of isolated TTY current loop input or std data terminal RS-232-C connections. Data rate is settable from 50 to 9600 baud. **Datel-Intersil**, 11 Cabot Blvd, Mansfield, MA 02048. Circle 256 on Inquiry Card

136-COL, 9 x 9 DOT MATRIX SERIAL IMPACT PRINTER

Series 6000 is microprocessor controlled to provide bidirectional, logic seeking printing at 150 char/s. Char are formed into a 9 x 9 dot matrix, allowing true lower case descenders, and are spaced at 10/in (3.9/cm) with selectable line spacing of 6 or 8 lines/in (2.3 or 3.1/cm). Unit can accommodate paper widths from 2 to 17.5" (5 to 44 cm) from single-part to multipart forms of 6 parts. Vertical forms control is produced via microprocessor control and a top form button on the control panel. The printer includes a 96-char ASCII set with either an RS-232 serial interface or a Centronics compatible parallel interface. Other features include a 240-char buffer and out of paper sensor. **Qantex Div, North Atlantic Industries, Inc,** 60 Plant Ave, Hauppauge, NY 11787.



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HP 2100

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For more information on these products, contact: Digital Pathways Inc. 4151 Middlefield Road Palo Alto, CA 94306 Phone: (415) 493-5544

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MODEM TEST SET



Self-contained MTS-1 tests asynchronous modems from 300 to 19.2k bits/s and internally timing synchronous modems up to 76.8k bits/s. An internal crystal controlled clock used for timing allows end to end testing of data lines with two separate test sets. The unit generates and receives 4 different patterns: all spaces, all marks, alternating marks and

spaces, and CCITT 511-bit pseudorandom pattern. Errors are detected and counted on all patterns and displayed on a 3-digit display. Indicators show when the error count has exceeded 999 and when the receiver has established synchronization with the incoming pattern. Using wire jumpers provided, the device can perform a complete self-test function. **Electrodata, Inc,** PO Box 46130, Bedford, OH 44146. Circle 258 on Inquiry Card

DISC SUBSYSTEM

Connected to Control Data's 3300 and 3500 computers via CDC communications channels, subsystem interfaces with the Master operating system through a supplied driver. The unit consists of 1 or more controllers, each capable of handling up to 16 disc drives. Each drive may contain more than 320M char, providing large online capacity and fast access for user data. Designed to replace the controllers and disc drives of host computer systems by emulating the basic characteristics of units normally supported by the Master operating system, the subsystem will emulate basic characteristics of the CDC 844-44 while providing more capacity per drive. Subsystem controller performs necessary mapping to the physical device. Advanced Computer Techniques Corp, 222 N Central Ave, Phoenix, AZ 85004. Circle 259 on Inquiry Card

CHARACTER GRAPHICS COLOR VIDEO DISPLAY CONTROLLER



Microprocessor based graphics system features an easily programmable display of 254 char and 64 foreground/background color combinations or 8 levels of gray scale. FS 2500 color video display controller consists of rackmountable display generator unit plus optional freestanding desktop keyboard with full u/lc tri-mode and numeric/control pad, and optional 13 or 19" (33- or 48-cm) color monitors. Char include 64 ASCII upper and 31 lower case in an effective 10 x 8 matrix and effective 12 x 9 field. Semigraphics sets include 2 x 3 element symbols, 64 in an effective 12 x 9 matrix and 31 which replace the lower case char set. The system displays 32 lines of 80 char each at 60-Hz refresh rate. Ramtek Corp, 2211 Lawson Lane, Santa Clara, CA 95050. Circle 260 on Inquiry Card

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- Large scrolling text memory
- Programmable function keys

Multiple character sets

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DELTA DATA SYSTEMS CORPORATION Woodhaven Industrial Park Cornwells Heights, PA 19020 (215) 639-9400

CIRCLE 147 ON INQUIRY CARD

The Associated Press Mighty Mouse System is the most advanced wire service copy processing network in the world. Over one hundred DELTA 7000 Series terminals are used in this system.

Courtesy Associated Press

U.K. Subsidiary: DELTA DATA SYSTEMS LTD. Welwyn Garden (07073) 33833 Service in over 150 locations in the U.S., and 10 European Countries and Canada.

UNIVERSAL FLOPPY DISC DRIVE EXERCISER



With model 108, singleor double-sided, singleor double-density minifloppy and std floppy disc drives can be tested and aligned in the field, lab, or incoming inspection. The unit can also be used

for testing and alignment of most top or front loading cartridge disc drives such as the Diablo series 30/40, CDC Hawk, and others. The exerciser simplifies head alignment, index detector adjustment, track 0 adjustment, and other normal maintenance procedures. It is compatible with all floppy drives using std Shugart interface; 2 connectors are provided, one 34-pin for minifloppy drives and one 50-pin for std drives. Other features include manual or alternate seek (with track 0) to any track address, and manual or automatic restore/recalibrate function. **Ava Instrumentation**, **Inc**, 9672 Manzanita Ave, Ben Lomond, CA 95005. Circle 261 on Inquiry Card

IN-CIRCUIT/CONTINUITY TEST SYSTEM

Combining in-circuit features for testing resistance with connectivity features for testing shorts and opens on both loaded and bare PC boards, the 2245 pinpoints a range of process errors like under- or over-etch, poor wash, and uneven cladding. The Z80 microprocessor based system prescreens loaded boards to measure resistance values from 10 to 10k Ω . It also allows testing of pull-up, pull-down, and ECL resistors. Bed of nails fixturing is identical to that of the 2270 analog/ digital in-circuit test system, equipping users with a dualpurpose fixture. Typ board test times are 1 to 2 s. Diagnostic messages are reported at 1 s/fault. A built-in 20-col printer provides diagnostic information; cassette tape cartridge stores multiple test programs for fast program loading. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742. Circle 262 on Inquiry Card

DISCRETE SEMICONDUCTOR TEST SYSTEM



An easy to use system with the same high throughput as the company's discrete test systems, the T347 provides datalogging capability and menu programming. The menu programmed software is versatile and easy to use. A prompting sequence leads users through the steps necessary to structure or create test plans of a test bin scheme. Datalogged results and summary information are available on a CRT screen, a thermal printer, or optional line printer for hard copy, and floppy discs can record information for permanent storage. The system can accommodate more than 6 different jobs at once. High voltage and high current options extend the current range from 16 to 50 A and voltage range from 400 V (600 V pulsed) to 2 kV. **Teradyne, Inc,** 183 Essex St, Boston, MA 02111. Circle 263 on Inquiry Card Now, X-10, AI-250, and AI-400 piezo audio indicators from Projects Unlimited come with PC pins making mounting fast and simple.

Get great features, too! Continuous tone. Wave solderable. 2.7-4.0 KHz frequency range. -50° to $+80^{\circ}$ C operating range. 84-98 dbA at 1 foot. Minimum 1000 hours design life. And more.

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ndau, Dayton, onio 43414. Phone: (513) 890-1918. TWX: 810-450-2523. A Singer State State



*KYNAR is a registered trademark of Pennwalt Corporation for its polyvinylidene fluoride.



Programmable Digital Switches

Checklist details P/ROM vs RAM program storage, individual station billing, reliability, and toll-cost management for PBX equipment. Digital Telephone Systems, Novato, Calif.

Circle 300 on Inquiry Card

Solid State Capacitive Keyboards

Brochure contains specs, block diagrams, and schematics plus flowchart to aid in customizing keyboards. Cherry Electrical Products Corp, Waukegan, Ill. Circle 301 on Inquiry Card

Industrial Microcomputers

Family of RacPac computers and accessories, including software packages, is outlined in illustrated brochure. Process Computer Systems, Inc, Saline, Mich. Circle 302 on Inquiry Card

Socket and Terminal Strips

Dimensional drawings and descriptions of sockets and terminal strips for DIP and SIP devices are cited in catalog. Samtec Inc, New Albany, Ind. Circle 303 on Inquiry Card

Microcomputer Analog I/O Systems

Selection guide details applications, specs, and user instructions for 80 analog 1/0 families; application article guides in selection of analog 1/0 system. Data Translation, Natick, Mass. Circle 304 on Inquiry Card

Short Haul Modems

Data sheet gives general description and lists transmission characteristics, terminal interface, transmission range, and dimensions of 410 asynchronous line driver. Micom Systems, Inc, Chatsworth, Calif. Circle 305 on Inquiry Card

Switching Power Supplies

The 30- to 300-W single-output high efficiency (68 to 80% typ) TDK series supplies are profiled with specs, dimensions, and characteristics in brochure. Kepco, Inc, Flushing, NY.

Circle 306 on Inquiry Card

Data Converters

Question and answer format of pocket sized guide addresses considerations in selecting a converter, including definitions of performance specs, state of the art advances, and performance tradeoffs. ILC Data Device Corp, Bohemia, NY. Circle 307 on Inquiry Card

Telecommunications Equipment

Sections in catalog briefly describe telecommunications products including microwave radio, FDM cable, n-type repeatered line, and PCM equipment. GTE Lenkurt Inc., San Carlos, Calif. Circle 308 on Inquiry Card



Small Business Computers

Audio-tutorial program consisting of three cassettes and illustrated workbook describes memory, compares storage media and 1/0, discusses software, and covers personnel needed for using a computer in business. Price is \$49.95. Heath Co, Benton Harbor. Mich.

Circle 309 on Inquiry Card

Delay Lines and Transformers

Lumped constant delay lines and digital delay modules are profiled with photos, operating characteristics, specs, and performance graphs in catalog. Rhombus Industries, Huntington Beach, Calif. Circle 310 on Inquiry Card

Custom Integrated Circuits

Reference guide describes radiation hardened, dielectric isolated digital circuits; radiation hardened IIL processes; MIL-STD interface technology; and custom bipolar JI P/ROMS. Request on company letterhead from Harris Semiconductor Programs Div, po Box 883, Melbourne, FL 32901.



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Data Communications Diagnostic System

Outlining system capability, operation, and flexibility, brochure provides specs for the Encore 100 and compares it with the earlier Pacer. Digitech Data Industries, Inc, Ridgefield, Conn. Circle 311 on Inquiry Card

Bipolar Memories

Cross reference guide classifies the company's P/ROMS and RAMS by size, organization, output, pins, and competitive manufacturer. Advanced Micro Devices, Inc, Sunnyvale, Calif.

Circle 312 on Inquiry Card

High Technology Courses

Facilities and course offerings at the company's Technology Center are described in brochure. Texas Instruments, Inc, Arlington Heights, Ill. Circle 313 on Inquiry Card

Cables and Connectors

Photos, descriptions, and dimensional data for planar cables, mass termination connectors, and cable assemblies are provided in catalog. Spectra-Strip, Garden Grove, Calif Circle 314 on Inquiry Card

Microcircuit Packages

Case and cover styles, plating and construction features, and dimensional data for standard platform plug-in metal packages for integrated and hybrid microcircuits are presented in catalog. Tekform, Anaheim, Calif. Circle 315 on Inquiry Card

Breadboards and Accessories

General purpose breadboards, card racks, connectors, IC sockets, and minicomputer compatible interface breadboards are featured in catalog. Douglas Electronics, Inc, San Leandro, Calif. Circle 316 on Inquiry Card

Portable and Desktop Terminals

Brochure compares Miniterm^R KSR and ASR printers' features with those of Texas Instruments' Silent 700 series models. Computer Devices, Inc, Burlington, Mass. Circle 317 on Inquiry Card

Digital Image Analysis

Implementation of the color display and capabilities of VIEWS, a standalone system designed for image analysis, are described in illustrated brochure. Interpretation Systems Inc, Overland Park, Kans. Circle 318 on Inquiry Card

Resistors, Delay Lines, Switches, and Networks

Catalog/engineering handbook includes dimensional drawings, electrical features, and engineering data for rotary switches, precision and power resistors, and delay lines. Electro-Components Div, AMF Inc, Manchester, NH. Circle 319 on Inquiry Card

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CIRCLE 153 ON INQUIRY CARD



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spark from body to computer cabinet is all it takes to produce a charge as high as 30,000 volts. And, if the cabinet and/or components are poorly grounded, the charge can be transmitted to components causing overloading and circuit malfunction.

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CRT Monitors

Brochures outline monochrome 5-, 7-, 9-, and 12" BHD series TV monitors, designed to be mechanically and electrically compatible in std data terminals. Bell & Howell Display Devices, Newport Beach, Calif.

Circle 320 on Inquiry Card

Alphanumeric Dot Matrix Printers

Brochure contains photos, specs, characteristics and options for 2-station bior unidirectional printer and for singlestation slip printer. Sweda International, Inc, OEM Products, Pine Brook, NJ. Circle 321 on Inquiry Card

Absolute and Incremental Optical Encoders

Separate data sheets detail electrical, mechanical, and military specs; and provide outline drawings for each optical encoder. **Itek Measurement Systems Div**, Newton, Mass.

Circle 322 on Inquiry Card

Manufacturing and Process Control

Brochure gives an overview of computers in warehousing and distribution, in materials handling, and on the factory floor, with the focus on problem solving applications. **Digital Equipment Corp**, Maynard, Mass.

Circle 323 on Inquiry Card

Custom Display Terminals

Foldout brochure describes how 5100S and 5100E terminals, featuring dual intensity characters, underscore, reverse video, and blink, can be tailored to specific requirements. **Data General Corp**, Westboro, Mass. Circle 324 on Inquiry Card

Magnetic Particle Clutch/Brake

Specs, operating and performance information, plus dimensional drawings for $FASTEP^{R}$ -SOFSTEPTM line of clutches and brakes are supplied in catalog. Simplatrol-Dana Industrial, Webster, Mass. Circle 325 on Inquiry Card

Data Communications

"Sherry Says" calendar lists dates of major trade shows and conferences, plus historical events relating to communications. **Racal-Milgo, Inc,** Miami, Fla. Circle 326 on Inquiry Card

Miniaturized Switching Supplies

Catalog describes high reliability ac-dc and dc-dc supplies and provides mechanical specs and reliability data. Arnold Magnetics Corp, Culver City, Calif. Circle 327 on Inquiry Card

when we introduced the SMC11 back in 1978, we caused something of a sensation. We'd just given DEC PDP-11 users the first disk controller ever to offer all the features of expensive multi-board controllers in a single hex-wide card. Suddenly it was possible to have sophisticated capabilities like multiple-sector transfer and hardware ECC without wasting space and money on extra fans, power supplies, rack mounts, and cabinets.

Now, after more than a year and hundreds of installations, we have another announcement: The SMC11 has proven itself to be the most capable and reliable storage module disk controller made. Which is an even better reason to get in touch with us if you happen to be in the market. After all, in 1978 we were asking you to try something new. Now we're asking you to buy something tried.

SMC11. The first single card SMD controller for DEC is still the best.



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Just what the doctor ordered for mass termination.

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The SMC12 is an intelligent single card disk controller that will interface any Nova or Eclipse compatible minicomputer with up to four storage module compatible disk drives. It has dual full-sector RAM buffers, which allow contiguous sector transfers of up to 64K words at a single command. It has hardware ECC which permits detection and correction of data error bursts of up to eleven bits long. It also has microprogrammed TTL logic, dual access support, and sector flagging. And the SMC12 comes with a no-nonsense guarantee of reliability. That's the latest statement of the disk controller art for Data General. Get in touch with us for a surprising statement of the price.

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For more information on how you can participate as a vendor contact: Hank Cronan at Robert T. Kenworthy Inc. 866 United Nations Plaza New York, New York 10017 (212) 752-0911



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 A simple concept. Not everybody with a computer and a disk drive needs or even wants a controller with all the ultra-sophistication that can be built into one today. There isn't much point in out-performing the purpose of a system. Especially when that over-performance can cost a lot of money.
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