COMPUTER DESIGN MAGAZINE OF DIGITAL EL RONICS F

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MARCH 1977

DESIGNING A MICROPROCESSOR-BASED TERMINAL FOR FACTORY DATA COLLECTION

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LETTERS TO THE EDITOR

To the Editor:

There are several inaccuracies in Jerry Washburn's article, "Low Power Computers: A Make or Buy Decision" (Computer Design, Nov 1976, pp 120-124). I would like to comment on those which are particularly misleading with regard to Intersil's IM6100 microprocessor. The CMOS IM6100 and its family of compatible CMOS RAMs, ROMs, UARTs, and PIEs are ideally suited for many low power applications and should have been more carefully researched.

The following quoted material was taken from Mr Washburn's article.

1. "Microprocessors generally are not I/O oriented \ldots "

The IM6100 devotes a class of instructions to I/O operations and supports DMA on a handshaking basis.

2. "Microprocessor chip interrupt capabilities are minimal . . .

Not with the IM6101 Parallel Interface Element (PIE), which provides a Vectored Priority Interrupt capability along with its sophisticated I/O functions.

3. "Minicomputer manufacturers offer a complete line of time-tested . . . software packages . . . '

Right! And since the IM6100 is PDP-8/E minicomputer compatible, this time-tested software support is available; shouldn't it have been mentioned?

4. "Most (of the high level languages available for microprocessors) are limited and inefficient.'

Not true for the IM6100! Excellent high level language compilers and interpreters are available, including FORTRAN (8k and 16k), BASIC, FOCAL, SNOBOL, LISP, ALGOL, DIBOL, etc.

In System Hardware (Table 2), 5. Mr Washburn completely neglected Intersil's extensive hardware support of the IM6100: chip family, PC cards, and partial, as well as complete, systems.

Chip Family

Intersil supports the IM6100 CMOS 12-bit microprocessor with a family of compatible CMOS parts (all second sourced):

M6100	CMOS Microprocessor
M6101	CMOS Parallel Interface
	Element (PIE)
M6402	CMOS UART
M6508/18	CMOS 1024-bit RAM
M6551/61	CMOS 256-word x 4-bit RAM

Soon to be released members of the family include:

IM6102	CMOS Memory Extender, Simul- taneous DMA, Programmable Real-Time Clock, Dynamic Mem-
IM6404	ory Refresh Controller Hex Bus Element/Interface
IM6512	CMOS 64-word x 12-bit RAM
IM6603	CMOS 512-word x 12-bit EPROM
IM6504	CMOS 4096-bit RAM

PC Cards and Partial Systems (Intercept and Intercept Jr components)

6900-CONTRL	Control Panel Module
6901-M4KX12	CMOS 4K-Word Nonvolatile Mem-
6902-CPUTTY	IM6100 Microprocessor/Tele-
6904-INTBUS	Universal Bus Expander
6905-WIREWP	Universal Wirewrap Module
6906-EXTEND	Extender Module
6907-EMC	Extended Memory Controller
6951-M1KX12	CMOS 1K-Word Nonvolatile RAM Module
6952-P2KX12	2K x 12 Programmable ROM
6953-PIEART	RS-232 or 20-mA Serial I/O
6960-SAMPLR	CMOS Family Sampler Module

Complete Systems

Intercept Prototyping System Intercept Jr Tutorial System IFDOS Dual Floppy Disc System

As Mr Washburn requires, for the IM6100 "the software tools, CPUs, and system hardware are all reliable, field proven, and readily available."

Stephen L. Diamond Intersil Cupertino, Calif

Letters to the Editor should be addressed:

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MAR 28-30—Data Communications INTER-FACE '77, Fifth Annual Nat'l Conf and Exposition, Georgia World Congress Center, Atlanta, Ga. INFORMATION: DataComm INTERFACE, Inc, 160 Speen St, Framingham, MA 01701. Tel: (617) 879-4502

MAR 28-31—IEEE Internat'I Semiconductor Power Converter Conf, Orlando, Fla. IN-FORMATION: Eberhart Reimers, Gen'I Conf Chm, USAMERDC, AMXFB-EA, Electrical Equipment Div, Fort Belvoir, VA 22060. Tel: (703) 664-5596

MAR 29-31—Computer Systems and Technology Conf, U of Sussex, England. INFOR-MATION: Conf Dept, Institution of Electronic and Radio Engineers, 8-9 Bedford Sq, London WC1B 3RG England

MAR 29-31, APR 5-7, APR 19-21, APR 26-28, and MAY 3-5—Computer Caravan, San Francisco, Calif; Los Angeles, Calif; Cleveland, Ohio; Minneapolis/St Paul, Minn; and Chicago, III. INFORMATION: John C. Forbes & Associates, One Hilltop Rd, Winchester, MA 01890. Tel: (617) 729-9244

APR 6-8—**Microcomputer '77 Conf and Exposition**, Oklahoma City, Okla. INFORMA-TION: Dr S. C. Lee, School of Electrical Engineering, U of Oklahoma, Norman, OK 73019

APR 6-8—Digital Processing of Signals in Communication, Loughborough, UK. INFOR-MATION: Institution of Electronic and Radio Engineers, 8-9 Bedford Sq, London WC1B 3RG England

APR 12-14—Internat'l Reliability Physics Sym, Caesars Palace, Las Vegas, Nev. IN-FORMATION: George Ebel, Singer Co, Kearfott Div, 150 Totowa Rd, Wayne, NJ 07470. Tel: (201) 256-4000

APR 13-15—Interactive Design Systems Conf, Stratford-upon-Avon, England. INFORMA-TION: Computer Aided Design Centre, Madingley Rd, Cambridge CB3 OHB England

APR 13-15—Sym on High Speed Computer and Algorithm Organization, U of Illinois, Urbana, III. INFORMATION: Prof E. C. Kalb, Office of Continuing Education and Public Service, 116 Illini Hall, U of Illinois, Champaign, IL 61820

APR 15-17—First West Coast Computer Faire, Civic Auditorium, San Francisco, Calif. INFORMATION: Jim Warren, Faire Chairperson, Star Route Box 111, Woodside, CA 94062. Tel: (415) 851-7075 APR 18-21—American Regional Meeting of Internat'l Purdue Workshop on Industrial Computer Systems, Purdue U, West Lafayette, Ind. INFORMATION: Dr T. J. Williams, Workshop Gen'l Chm, 102 Michael Golden, Purdue U, West Lafayette, IN 47907. Tel: (317) 494-8425

APR 19-21—SID Internat'I Symposia, Sheraton-Boston Hotel, Boston, Mass. INFOR-MATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

APR 19-21—Electro/77, The Internat'l Electronics Convention, New York Coliseum/ Hotel Americana, New York, NY. INFORMA-TION: William C. Weber, Jr, Gen'l Mgr, Electro/77, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

APR 21-22—Eighth Annual Pittsburgh Conf on Modeling and Simulation, Pittsburgh, Pa. INFORMATION: William G. Vogt, Modeling and Simulation Conf, 348 Benedum Engineering Hall, U of Pittsburgh, Pittsburgh, PA 15261

APR 25-27—IEEE Internat'I Sym on Circuits and Systems, Phoenix, Ariz. INFORMATION: Gen'I Chm, W. G. Howard, Jr, Motorola Corp, PO Box 20906, Phoenix, AZ 85036. Tel: (602) 962-3026

APR 26-27—The 25th Annual National Relay Conf, Oklahoma State U, Stillwater, Okla. INFORMATION: Dr D. D. Lingelbach, School of Electrical Engineering, 202 Engineering S, Oklahoma State U, Stillwater, OK 74074

APR 26 and APR 28—Invitational Computer Conf, Hempstead, NY and Philadelphia, Pa. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

MAY 2-5—ISA/77 Conf and Exhibit, Anaheim, Calif. INFORMATION: Anaheim/77, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

MAY 3-5—ECOMA-3 (European Computer Measurement Association), Hamburg, Germany. INFORMATION: Scott N. Yasler, ECOMA President, c/o Union Bank of Switzerland, Bahnhofstrasse 45, CH-8021 Zurich, Switzerland

MAY 3-6—EUROCON '77, Venice, Italy. IN-FORMATION: EUROCON '77, c/o AEI, Viale Monza 259, 1-20126 Milan, Italy

MAY 7-8 and JUNE 18-19—Personal Computing Show, Philadelphia, Pa and Boston, Mass. INFORMATION: Personal Computing, Conf and Exposition Management Co, Box 844, Greenwich, CT 06830 MAY 10-14—Minicomputer, Periheral, and Data Communications Exhibition, U.S. Trade Center, Milan, Italy. INFORMATION: Mike Springmann, Office of Internat'I Marketing, Rm 1014, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-4270

MAY 18-22—Hobby Electronics Fair, Philadelphia, Pa. INFORMATION: Aaron Kozlov, Project Manager, ISCM, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

MAY 24-26—Sixth Annual Sym of Incremental Motion Control Systems and Devices, Urbana, III. INFORMATION: Dr B. C. Kuo, University of Illinois, Dept of Electrical Engineering, Urbana, IL 61801. Tel: (217) 333-4341

MAY 24-26—Internat'l Exposition of Mini/ Micro Computers and Microprocessors, Palais de Exhibitions, Geneva, Switzerland. IN-FORMATION: Joseph C. Maurer, Industrial & Scientific Conference Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

MAY 24-27—PICA-77 (Power Industry Computer Application Conf), Toronto, Canada. INFORMATION: IEEE, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

MAY 24-27—Seventh International Sym on Multiple-Valued Logic, Charlotte, NC. IN-FORMATION: Dr C. M. Allen, Sym Chm, Engineering Analysis and Design Dept, U of North Carolina at Charlotte, Charlotte, NC 28223. Tel: (704) 597-2302

JUNE 20-22—IFAC/IFIP Real-Time Programming Workshop, Eindhoven, The Netherlands. INFORMATION: C. H. Smedema, Philips Research Laboratories, Eindhoven, Netherlands



APR 19-21—CAM-I '77—Getting CAD/CAM Together, Arlington, Tex. INFORMATION: C. H. Link, Executive Secretary and Gen'I Mgr, Computer Aided Manufacturing-Internat'I, Inc, Suite 1107, 611 Ryan Plaza Dr, Arlington, TX 76011. Tel: (817) 265-5328



APR 30—Introduction to Microprocessors, U of Alabama, Huntsville, Ala. INFORMA-TION: Dr Pei Hsia, U of Alabama, PO Box 1247, Huntsville, AL 35807

MAY 10-12, MAY 24-26, JUNE 7-9, and JUNE 21-23—Hands-on Microprocessor Short Course With Free Take-Home Microcomputer, Lafayette, Ind; Cleveland, Ohio; Syracuse, NY; and Hackensack, NJ. INFORMA-TION: Jerilyn Williams, Wintek Corp, 902 N 9th St, Lafayette, IN 47904 Tel: (317) 742-6802

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COMMUNICATION CHANNEL

by John E. Buckley Telecommunications Management Corp Cornwells Heights, Pa.

Possible 1977 WATS

Last month the background and present status of the Wide Area Telecommunications Service (WATS) were discussed and analyzed. The primary purpose of that dissertation was to establish a uniform basis of understanding for this month's topic—the possible structure of a new WATS tariff.

When major tariff revisions and rate restructurings are to be announced by the common carrier, it is imperative that the current or anticipated users of those services be aware of the redefinitions and new rates as soon as possible—for two major purposes. The first is so that users can convey to the proper regulatory agency (ie, FCC), the impact of any redefinition or rate restructuring on their existing or planned communication systems; and secondly, so that those users of the service can reanalyze and redesign their communication methods in anticipation of the implementation of a redefined communication service with new rates.

Two aspects of the 1977 WATS rates can be identified with a high degree of confidence at this time. Based on information obtained prior to the November 4, 1976 aborted filing, the new WATS tariff will reflect a complete restructuring of the previous geographic areas of the various bands. The anticipated WATS filing is expected to divide the Continental U.S. into three WATS bands rather than five, while maintaining the concentric circle arrangement of the previous WATS tariffs. In addition, a fourth band will be identified, encompassing Hawaii, Alaska, the Virgin Islands, and Puerto Rico. It is expected that this new band 4 will also be inclusive of the new bands 1, 2, and 3. A band 5 also is expected that will permit locations in the U.S. to place calls to Canada and Mexico. This U.S./International WATS band is expected to be provided only as an Out-WATS service and not have the corresponding In-WATS.

The anticipated band 3 is expected to be comprised of the present band 4 and 5 geographic areas; the new band 2 is expected to comprise the existing band 2 and 3 areas; and the new band 1 is expected to correspond essentially to the existing band 1 areas.

Both the physical redefinition of a geographic area comprising a WATS band and a probable return to the 1974 rate ratios are the basis of the rates that will typically be associated with the new WATS tariff. In the spring of 1976 the FCC had found that the short distance WATS user was essentially being overcharged with respect to associated costs, while the longer distance user was being undercharged. In effect, the FCC was suggesting that present band 1 and 2 users were subsidizing rates for band 4 and 5 users. A comparative analysis of present WATS rates with the 1974 rates clearly indicates that the recent trend has been toward establishing a uniform time charge for all WATS calls. If carried to its natural conclusions, the trend would eventually result in a single WATS band for the entire U.S. with a uniform time-related WATS charge.

The present band 1 full business day (FBD) WATS charge is typically \$900 if the WATS location is New York City. A band 5 FBD WATS charge for a New York City location is \$1675. In effect, the band 5 charge is only 86% more than the band 1 charge. In 1974, the difference between the two for a full time WATS line was 270%. This comparative analysis clearly indicates that the WATS charge trend has been towards a uniform WATS rate, regardless of the geographic distance of the calling and called locations. It has been suggested that a number of alternatives for new WATS charges are possible. These alternatives consist of the following:

1. The WATS rate ratio will be returned to the 1974 ratio which would be approximately 270% between the closest and the furthest band service.

2. It also has been predicted that two complete separate rate structures will be provided for In-WATS and Out-WATS services. At the present time, a band 5 In-WATS and band 5 Out-WATS service have exactly the same monthly charge whether full time or measured.

3. The entire WATS tariff concept will be discarded and a bulk discount rate schedule will be established, based on the accumulated volume of calls and the specific geographic area or bands.

4. A bulk discount rate schedule will be implemented regardless of the geographic area called and will be

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strictly determined by the total accumulated volume of all calling activity from a designated customer location.

If either of the last two possibilities should become a reality, the existence of WATS as a separate service would end. At the present time, an organization utilizing a WATS service is provided with a specific dial access line or trunk, designated as a WATS line to a specified band. Charges rendered by the telephone company are with respect to activity generated on each WATS line or trunk. In order for a user to achieve any significant economic advantage from this WATS service, he must place long distance calls over that WATS line. This requirement imposes the burden of sharing a line or trunk among those individuals in the customer's location, which typically places a constraint condition so that users experience busy conditions and delays in achieving access to the WATS line. The objective in designing a WATS network is to return genuine value for the customer's costs by balancing the accessability of the WATS line(s) for the proper grade of service, while generating a total WATS charge less than the corresponding toll charge for the same calls. If a bulk discount rate is implemented, use of specific WATS lines can be expected to be discontinued. Users subscribing to such a "bulk WATS" service may merely be committed to a minimum long distance charge per month and any long distance charges beyond that amount will be discounted according to an established schedule.

It is interesting to note that if the bulk discount concept should be implemented, a severe impact will be felt by manufacturers and suppliers of computerized call routing devices. Having recently found a significant market, these devices automatically route and control administrative voice calls among a limited number of WATS lines. Under such a bulk discount tariff there would be no limit to the number of dial access lines and hence no need to route or queue such calls.

Admittedly, these observations are predictive and speculative in nature. It can be established with a high degree of certainty, however, that a major revision in the WATS concept can be expected during the first half of 1977. The nature of these anticipated changes can only be more accurately established by tracking the developments and information available prior to the actual filing.

Once the filing takes place, it will typically be effective within 90 days. Such a period allows time for meaningful responses from the user community to the appropriate regulatory agency. It is important therefore that information system designers and users who anticipate or are presently using the WATS tariff as a major arrangement in their data communication network evaluate these possible alternatives and begin to compile their preferences and positions prior to the actual filings. It is hoped that the actual filing and resulting FCC approval will be fully cognizant of the large number of systems that are totally dependent at the present time on the economies that can be realized from the proper use of the WATS tariffs. It would be most unfortunate if repercussions similar to those that existed during the mid 60s with the revision of the TelPak tariff were allowed to occur with this pending revision of the WATS tariff. This column will address further developments in this important matter as they become clarified.

CONRAC

Production economics was only one of the factors that had to be considered in the selection of material for the cabinet of the new Conrac model 480/25 CRT terminal. Design, engineering, performance and appearance considerations also figured strongly in the eventual choice of molded Baydur urethane structural foam for this demanding application.

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the first and 16K RAMs.

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2104A-3	4K	250	375	30
2104A-4	4K	300	425	30
2116-2	16K	200	350	69
2116-3	16K	250	375	68
2116-4	16K	300	425	65

For Data Sheets and our 16-page Application Note, use the reader service card or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.



Glass Fiber Lightguides To Be Evaluated For Data Signal Transmission

Online evaluation of a lightwave transmission system that will carry voice, data, and video signals over a cable of glass fiber lightguides could result in expanded telecommunications capabilities. Tests will begin in Chicago, Ill by mid-1977 under the direction of Bell Laboratories and AT&T, in cooperation with Illinois Bell and Western Electric.

Light pulse signals will be carried for about a half mile between the Brunswick building in Chicago's Loop and an Illinois Bell central office (Franklin); and then between the Franklin office and a second central office (Wabash) about a mile away. Total transmission distance will be about 1½ miles (approximately 1 km). This evaluation will be a follow-up of tests on an experimental system conducted at the joint Bell Labs-Western Electric facility in Atlanta, Ga (see *Computer Design*, Mar 1976, pp 30, 34).

The planned system evaluation should be completed in 1978. If determined to be economically feasible and to provide operational advantages, lightwave systems could be in use by the early 1980s between telephone switching centers in metropolitan areas. Later, the systems might be expanded for long distance data transmission.

A single half-inch diameter cable containing 24 low-loss silica lightguides will be installed in standard telephone company ducts and manholes. Each lightguide will be connected at one end to a transmitter module containing either semiconductor laser or LED light source. The other end of each lightguide will be connected to a receiver module containing a photodetector device that converts light pulses to electrical signals compatible with those transmitted within the telecommunications network.

A single pair of lightguides in the cable will be able to carry 576 simultaneous conversations or an equivalent mix of voice and various types of data signals. Separate pairs of lightguides in the same cable will be used to carry Picturephone^R meeting service video signals. No amplifiers will be needed to boost signals along the route. Gallium-aluminum-arsenide (GaAl-As) lasers will produce infrared light signals at a wavelength of $0.82 \ \mu m$ at about 0.5 mW average power output. Accelerated aging tests conducted at Bell Labs suggest that this type of laser could operate continuously for more than 100,000 hours at room temperatures.

A transmitter module modulator circuit will turn the laser on and off 44.7 million times/s. Laser power will be maintained at a constant level over temperature variations normally encountered in telephone company use.

Lightguides will be coated to protect against humidity, abrasion, and losses due to bending, and will be combined into two flat ribbons, each containing 12 fibers. The ribbons will be enclosed in a cable that cushions and protects individual fibers against damage in field use, and helps minimize transmission losses. Average signal loss in the encabled fibers is expected to be 6 dB/km (10 dB/ mi). Laser light pulses could therefore be transmitted for at least 7 km (4 mi) without regeneration. A silicon "avalanche" photodetector will convert the light pulses to electrical signals at the receiving end of each lightguide.

Of related interest is an announcement that Bell Laboratories researchers in Murray Hill, NJ have demonstrated methods for making 1-km long glass fibers that are stronger than stainless steel wires of the same diameter. In tests the fibers have withstood pulling forces of more than 600,000 lb/in² before breaking. Accelerated testing has shown that high strengths can be maintained for many years.

In the past, only specially prepared glass fibers in relatively flawfree lengths of an inch or two exhibited such a high tensile strength. Even then, the fibers had to be kept in controlled environments, and when exposed to the atmosphere—or to handling of any kind—their strength deteriorated rapidly.

High tensile strength could reduce the cost of producing lightguides and further improve resistance to deterioration after prolonged use. Long lengths of communications-quality lightguides likely could be manufactured reliably with a very low probability of breakage.

During fabrication a rod of synthetic silica is "fire-polished" with an oxyhydrogen torch to remove surface defects and is then softened by heating in a focused laser beam that provides an extremely clean environment for processing. As the rod is softened, a continuous length of hair-thin fiber is drawn away and immediately coated with an organic resin. The resin and the technique for applying it give the fiber a highly durable protective coating without causing damage to the glass surface.

FCC Decision to Permit Refiling of Dataspeed 40/4 Tariff Challenged

Overturning a previous staff rejection, a Federal Communications Commission order released on Jan 5 authorized AT&T to refile a tariff for the interstate use of its Dataspeed 40/4 data communications service. Although the terminal equipment has been offered by many Bell System companies for intrastate use for several months, the refiled tariff, to become effective on Jan 19, will now clear the way for interstate use of the system.

The equipment includes a TV-like screen and printer to display information and a typewriter keyboard for entry of data. It provides high speed facilities for entering, storing, displaying, editing, printing, sending, and receiving large amounts of information.

However, in a motion filed on Jan 11 before the FCC, the Computer & Communications Industry Association (CCIA) asked the Commission to reconsider and stay the effect of its order permitting the interstate tariffing pending the outcome of the Commission's Computer Inquiry II (FCC Docket #20828). CCIA moved alternatively for a stay pending an appeal to Federal Court.

CCIA's motion asserts "that there is a strong likelihood of success in reversing the decision on its merits." Some of the key arguments presented are that:

"1. The FCC has violated its own rules formulated in Computer Inquiry I by admitting in its order that the Dataspeed 40/4 does, in fact, perform data processing functions, yet it fails to prohibit AT&T from offering the Dataspeed 40/4 as required by those rules. Further, even if one



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were to assume for the sake of argument that the offering does perform some message switching, the fact that it also performs data processing requires the Commission, again by its own rules, to determine whether the offering is a 'hybrid communications service' or a 'hybrid data processing service,' which the FCC has also failed to do.

"2. The Commission has misread its own findings of fact in Computer Inquiry I in that the order states that the original Computer Inquiry does not address the distribution of data processing among devices other than the central computer and that Chairman Wiley's concurrence states that the first Computer Inquiry did not purport to prescribe rules and definitions for terminals. CCIA alleges that such a reading is clearly in error, arguing that one of the FCC's Computer Inquiry I Rules deals exclusively with remote data processing services, ie, with terminals.

"3. The Commission has ruled arbitrarily by making its order contingent upon the outcome of Docket #20828 already in progress. The CCIA motion states that the Commission has engaged in what amounts to regulatory coin-flipping and that the order has the effect of preordaining the outcome of Computer Inquiry II in violation of its General Rules of Practice and Procedure required in such regulatory matters."

Editor's Note: Obstacles to the service offering were cleared when the U.S. Court of Appeals in New York City declined to issue a stay of an FCC order approving Dataspeed 40/4. The tariff, therefore, went into effect on Jan 26.

Communications Systems Are Cost-Effective In Network Applications

Higher level languages and compilers oriented to communications applications are included in two system and communications processors announced by Burroughs Corp, Detroit, Mich. B 870 and B 860 are said to be cost-effective in implementing communications network systems, particularly those involving distributed processing and control. They can control terminals locally or remotely while concurrently accessing their own data files and/or communicating with one or more central computer systems. In addition, they can communicate with all Burroughs terminal systems and Burroughs computers in a communications network, as well as with computer systems made by other manufacturers.

Models include three generalpurpose systems-the B 876, B 866-2, and B 866-1-each with a high speed control memory that houses system interpreters and master control program (MCP). The company's computer management system includes a network definition language and a message processing language for communications application programming. The MCP provides multiprogramming, virtual memory, iob scheduling, system and communication reconfiguration, and other system software features. COBOL and RPG compilers are provided with the computer management system for local programming and for applications that are not oriented to data communications.

B 876 and 866-2 processors operate at up to 2 MHz; that of the 866-1 operates at 1 MHz. B 876 has up to 147,456 bytes of main memory: 866-2 and 866-1 have 114,688 bytes. B 876 and 866-2 have 24,576-byte (expandable to 32,768 bytes) MOS and 16,384-byte bipolar control memories; the 866-1's 32,768-byte MOS control memory is expandable to 49,152 bytes. MOS memory has 632ns access time; that of bipolar memory is 70 ns for two bytes of data.

The systems can have nine (B 876) or five (B 866) channels for I/O devices and subsystems. All I/O is fully buffered and controls may be added or changed on site.

A separate microprocessor called a direct memory access control allows the disc I/O control and the data communications processor(s) to share memory cycles with the main system processor. It controls the priority of access for the three sources and prohibits any of them from preempting memory to the detriment of the other two.

Peripherals and subsystems include 60-char/s printer; 1960-char CRT display; 85-, 160-, 250-, 400-, and 750-line/min printers; 10-in/s tape cassette drives; 9-channel, 10k-byte/s magnetic tape drives; 1M-byte, 266ms access time super mini-discs; 243kbyte, 343-ms access time mini-discs; and 300-, 600-, and 800-card/min readers. Three removable disc cartridge drives have 4.6M-byte capacity and 80-ms access time, 9.2M-byte capacity and 100-ms access time, and 4.5M-byte capacity and 145-ms access time.

Disc pack drives have 65.2M- and 130.4M-byte capacities and 33.3-ms access time. Attaching multiple disc storage subsystems enables data storage of 521.6M bytes.

A B 876 system may be attached to one or two data communications processors, each able to service up to 16 lines concurrently in the fullor half-duplex mode in a multipoint and/or point-to-point network. B 866-2 and B866-1 systems can accommodate one data communication processor with up to seven lines.

The data communications processor is a microprocessor with its own standard memory of 6k 12-bit words. This memory houses the network definition language (NDL) interpreter, which is used to execute NDL object code. The NDL interpreter resides on disc and is loaded into the data communications processor memory under control of the master control program. Communication with the main memory is via the direct memory access control at a speed of up to 2M bytes/s.

Data communications processors are 10-MHz bit-oriented, and operate concurrently with the main system processor. They handle all processing associated with the various line procedures and managing of the communications lines. Hardware calculation of cyclic redundancy checks is included in the data communications processor to facilitate the handling of data link control, bisynchronous, and other transparent line procedures.

Messages are taken from, and placed into, queues in main memory without placing a burden on the main system processor. The main system processor becomes involved only when a complete message has been assembled and is made available to it for application processing. This asynchronous processing by the data communications processor provides the user with more efficient line utilization and increased message throughput.

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Data communications line characteristics are controlled by the data communications processor and are fully programmable for each line through the network definition language. Characteristics include odd, even, or no parity; 5-, 6-, 7-, or 8-bit characters; asynchronous, synchronous, or direct connect line types; full- or half-duplex line modes; and line speeds of 1800-bit/s asynchronous, 9600-bit/s synchronous transmission, 9600- and 19,200-bit/s direct connect, and 64,000-bit/s broadband transmission. Circle 400 on Inquiry Card

Contract Awarded For Satellite Communications

Under a contract awarded by the National Aeronautics and Space Administration (NASA), Western Union Upper Saddle River, NJ will provide the agency with satellite communications services over a 10-year period beginning in 1980. Instead of using ground stations as at present, the tracking and data relay satellite system (TDRSS) will provide tracking and communications for earth orbiting satellites, increased communications capacity, and low-orbit flight coverage.

1000

TDRSS is designed to consist of four identical satellites in orbit. Two, in-orbit satellites for NASA use are scheduled to start service by 1980, with an in-orbit spare to be available a few months later. The fourth satellite will be launched when Advanced Westar service is inaugurated in the early 1980s. Each satellite will have both analog and digital transmission capability.

A ground complex for NASA TDRSS services will be built and operated by Western Union on Government property in New Mexico. Advanced Westar services will be provided from separate ground facilities.

Options Expand System Diagnostic Capabilities

Two features-floppy disc memory and hardcopy printer-added to the System 180 network diagnostic controller by International Communications Corp of Miami, Fla provide extended capabilities. Both are options to the system.

The memory expands the systems network data base information storage and increases its network diagnostic scanning capability. It can be used by the operator to create and maintain data base information describing the characteristics of the data line as well as remote site modems, power, or terminal controllers. The additional data base expands the number of automatic testing sequences, and provides the operator with extensive network information.

The printer can be added for record keeping purposes. Online printing provides hardcopy records of data base information, allowing management reporting of system event data such as alarms and testing results. Expanded keyboard capability allows increased operator interaction with the video screen display. Circle 401 on Inquiry Card

Digital Facsimile Speeds Up Transmission **Of Graphic Documents**

High speed computer transmission of graphic documents was demonstrated at its Washington, DC headquarters late in November by the Defense Communications Agency. Further demonstrations were held in Germany and Hawaii early in December. Capable of transmitting maps, sketches, and handwritten documents, the system interfaces a 412 Securefax digital facsimile unit, made by Dacom, Inc, Santa Clara, Calif, to the Government's Autodin network via an Anacomm TLC-100 controller.

Either classified or clear messages on a store-and-forward basis can be transmitted on single- or multipleaddress distribution. Because preparation phases are shorter, the overall system is said to be much faster than current traffic methods. Circle 402 on Inquiry Card

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If yours is a multiprocessing or distributed processing network application, our new V77-400 just might be "the tie that binds."

Because on top of all its standard big machine features, there's an incredibly flexible dual port memory. (With up to 256K/16-bit words of 660ns MOS memory in a single, standard chassis.)

The V77-400's dual port memory, working with its unique direct memory access system, functions as a bridge when linked to other V77 Family computers in closely coupled, shared memory multiprocessor arrangements.

> An optional Writable Control Store is also available. Letting you expand the V77-400's instruction set to further improve the speed of both programming and program execution.

Top-of-the-line performance for almost any application. Our new V77-600.

Varian's new V77-600 sets new standards for all would-be high-performance mini's.

First, with a long list of standard big machine features. Second, with up to 1024K/16-bit words of 660ns MOS memory. And third, with a host of performance enhancing options. Including Writable Control Store, a floating point processor, and special scientific and commercial firmware.

For the ultimate in performance enhancement, an optional high-speed cache memory is also offered – cutting the V77-600's average execution time in half.

How our mini's speak fluent mainframe.

You won't waste any time or money training our new V77 Family how to communicate with your mainframe. Or developing your own control programs.

Because all V77 Family members utilize Varian's VORTEX (or VORTEX II) operating system – two of the world's best real-time systems.

Both systems permit concurrent job execution by allocating priorities. And help tailor other subsystems to fit scientific to commercial, real-time to batch, and stand-alone to data communications environments.

TOTAL, a highly efficient, network-type data base management system, is now available as a VORTEX II subsystem.



Usually found on only larger computers, TOTAL allows you to define and access your data base with powerful, high-level language processors like COBOL, FOR-

TRAN IV Level G, and RPG-II. Opening the door to large libraries of already developed applications programs.

The benefits of a well-structured family.

Our new V77 Family represents more than just a continuing commitment to total hardware and software compatibility. Because it's a commitment to solving basic price/performance needs on several different levels.

For those needing more computing power, there's a V77 that's an affordable, highperformance solution.

For those wanting less wasted overhead, there's a less expensive, high-performance alternative.

Plus an attractive new V77 discount plan designed to give even modest-volume OEM buyers a big break. Finally, for those

with special multiprocessing or distributed data processing requirements, there's an entire V77 Family. Specifically engineered to work well

together — through shared memories, intercomputer I/O bus lines, and shared communications channels — as new cost-effective replacements for typical "patchwork" systems.

Varian. A commitment to innovation.

Varian Data Machines has played a significant role in the evolution of digital minicomputers for almost a decade now.

Consistently producing innovations not only meaningful to the industry, but to the end-user as well. A look at just the last five years tells the story...

In 1972, VDM developed the first minicomputer operating system with all the multi-task and file handling capabilities of a large computer.

A year later, VDM created the first microprogrammed minicomputer with a 64-bit Writable Control Store. In 1975, two VDM



firsts: a minicomputer

with a data base management

system equivalent to those for large computers, and, the first 64K word semiconductor memory package on a single board.

Today, it's the whole new V77 Family. Well-structured and ready. Breaking new ground in terms of Varian size, compatibility, and price/performance. Three new mini's that really do think like mainframes.

For additional V77 Family planning literature, contact any of the 38 Varian offices listed below, or Varian Data Machines, 2722 Michelson Drive, P.O. Box C-19504, Irvine, California 92713, (714) 833-2400. In Europe, contact Varian

Associates Ltd., Molesey Road, Walton-on-Thames, Surrey, England, Telephone 28971.



Mini's that think like mainframes.

U.S. OFFICES: Los Angeles (213) 598-4438, San Diego (714) 276-9462, San Francisco (408) 736-5630, San Fernando Valley (213) 990-6042, Seattle (206) 641-4500, Denver (303) 770-2151, Dallas (214) 231-5145, Houston (713) 781-0105, St. Louis (314) 739-6433, Chicago (312) 692-7184, Detroit (313) 645-9550, Cleveland (216) 238-6960, Dayton (513) 258-1458, Orlando (305) 299-1592, Atlanta (404) 252-0047, Washington, D.C. (301) 773-6770, Philadelphia (215) 643-2355, Englewood Cliffs (201) 569-2323, New York City (212) 826-1010, Rochester (716) 586-3273, Boston (617) 890-6072. INTERNATIONAL OFFICES: Brussels (02) 4662000, Darmstat (0615) 7031, Munchen (089) 8126093, Bensberg (02204) 61066, Amsterdam (020) 15 94 10, Stockholm (08) 820030, Zug (042) 23 25 75, Surrey 093 22 28971, Toronto (416) 457-4130, Montreal (514) 332-2840, Vancouver (604) 736-5621, Ottowa (613) 224-6521, Calgary (403) 276-4456, Melbourne 560-7133, Sydney 43-0673, Sao Paulo (011) 240-3449, Singapore 379-239, Tokyo 403-7101, New Zealand 697-099, Taipei 58158-9.

CIRCLE 18 ON INQUIRY CARD

New from Centralab... IMPS PUSHBUTTON SWITCHES

A new miniature modular building block system that offers microprocessor control designers more of what they need.

To meet the special digital and analog needs of today's µP-based controls, Centralab offers design engineers a whole new system of modular pushbutton switch building blocks. We call it IMPS - Integrated Modular Panel System. IMPS saves PC board and panel area and simplifies front panel design, cuts assembly costs, reduces back-panel space requirements, and meets the digital-analog needs of µP-based controls. Check these space saving, cost-cutting features.

Simplify front panel interface.

All IMPS switches regardless of function, are uniform in size, simplifying design and selection of front panel hardware. They have high volumetric effi-ciency, occupying .505" x .388" PC board area and require only.608" of space between PC board and front panel.



Cut assembly costs.

IMPS switches may be mounted on the front panel, and are designed for automatic wave soldering installation and PC board cleaning. Insert molded terminals prevent flux and solder wicking and contact contamination. Integral PC board stand-offs provide for efficient board cleaning.

Meet analog and digital needs.

IMPS switches are available with momentary, push-push and interlocking actions, with a long-life contact system that switches both digital and analog signals. To accommodate critical signal requirements, housings are highinsulation molded plastic with UL 94V-0 rating.

Available options.

Optional installations include ganged assemblies, front-panel mounting and wire-wrapping.



All IMPS pushbutton switches are built to Centralab's highest quality standards (see specifications at right). They're priced as low as 41 cents in 1,000 quantity. For full technical details, samples and quotation, call (515) 955-3770, or write to the address below.



CIRCLE 19 ON INQUIRY CARD



Quality Specs.

IMPS Pushbutton Switches combine compact size, low cost and highest quality throughout.

• Silver or gold inlay wiping contacts for long-life and lowcontact resistance.

- Less than 2 milliseconds contact bounce.
- SPST, SPDT, DPST, and DPDT switch contacts.
- Printed circuit, DIL socket or wire-wrap terminations available.
- 2.5 to 3.5 oz. actuation force (momentary).
- Choice of button interface square or blade shaft (shown) -permits use of a variety of Centralab and industry standard buttons and keycaps.
- 10, 15, 20 or 25mm center-tocenter spacing.

DIGITAL TECHNOLOGY REVIEW

Core-Based Mass Storage System Replaces Discs, Lowers Access Time

Industry planners have speculated for years about the possibility of mass storage with an access time in the low microsecond range and inexpensive enough to use in quantity. Such storage would ideally be all electronic to minimize maintenance cost and reduce the time to repair.

To fill this long existing need at a minimal premium in initial cost, Ampex Corp, Memory Products Div, 200 N Nash St, El Segundo, CA 90245 designed the Megastore 1223 which stores 512k to 4096k bytes of information with data access within 2.5 μ s, and has a data transfer rate of 400k bytes/s. This improvement in data access speed and transfer rate should provide a 20 to 30% improvement in throughput in systems requiring large numbers of accesses to stored data. Modification of the operating system to take advantage of subsector addressing should provide a 50% improvement.

Targeted at the "access gap" that exists between the 300- to 600-ns range of main memory and the 10-ms range of direct access storage devices, the family of high performance alternatives to fixed-head disc devices are designed around 13-mil UnibitTM cores. The basic storage elements are ceramic devices made from a ferrite material having well-defined magnetic characteristics and an essentially flat temperature coefficient. To



Core-based mass memory from Ampex consists of controller, card rack, power supply, and up to eight logical modules each with capacity for 512k bytes of data





improve reliability, the memories use fewer components than traditional core memories and contain no electromechanical components or flying heads as are needed in rotating memories. In addition, the package's modular construction facilitates online repair should a failure occur. Increased system availability, increased system throughput, and negligible maintenance costs should result in a lower cost to the user over the lifetime of the system.

First product in the family, the 1223 serves as an alternative or replacement for fixed head discs on Nova[™] 2, 3, and 1200 computers. Each unit consists of controller, card rack, power supply, and up to eight logical modules, each storing 262,144 16-bit words. The controller is functionally equivalent to and physically replaces the Data General 4019 control card within the CPU, and contains all necessary logic to interface between the CPU and external memory. This logic responds to standard CPU commands for accessing a disc system and adds subsector addressing capability.

Data stored within the memory are accessed within 2.5 μ s compared with the 8.4 ms average access time for Novadiscs. Transfer rate is adjustable from 125k to 200k words/s to accommodate user program requirements.

Other units planned in the family are the 11 for plug-compatibility with the DEC RJ S03/S04 discs used on the PDP-11 computers; and the 4666 which is designed to provide the OEM multiple-unit buyer with a unit that is capable of accepting his own interface controller. Circle 140 on Inquiry Card

Modular Minicomputer Addresses 1M Bytes, Needs Little Space

A low cost, modular system with minimal space and power requirements, the 6/43 combines TTL logic, MSI and LSI circuitry, firmware driven microprocessor, semiconductor memory, etched wire connections, plug-in modules, and no backplane wiring to provide capability for performance in batch processing, real time applications, and distributed sys-

Here's how Data General's microNOVA system stacks up against the competition.

microNOVA Processor: Fully packaged 9-slot microcomputer, 16K words MOS memory, 2.4-microsecond arithmetic operations, hardware stack facility, multiply/divide, DMA capability. Includes RTC, PF/AR and APL. Supports up to 32K words RAM/PROM memory.

Dual-diskette subsystem: Integral DMA controller, compact 630KB capacity.

Cabinet: 37 inches high, holds all rack mounted components.



DASHER

terminal printer: 30 cps, 132-columns, typewriter keyboard, upper/lower case.

Systems Software: Multitasking Disc Operating System, Real-Time Operating System, FORTRAN IV, Extended BASIC, Macro Assembler, Utilities.

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The facts speak for themselves. For \$10,970, Data General's new microNOVA gives you more system, software and support than any other comparable computer. And we deliver in 60 days.

Any way you look at it, it all stacks up in your favor. For more information and our brochure, call our toll free number, 800-225-9497, or, fill out and return the coupon. *Quantity and OEM discounts available.

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CIRCLE 17 ON INQUIRY CARD

Here's how Data General's NOVA 3/D system stacks up against the competition.

Systems Software: Multitasking real-time disc operating system, FORTRAN IV, Extended BASIC, ALGOL, SORT/MERGE, and Utilities.

NOVA 3/D Processor: Hardware-protected dual partitions, 700-nanosecond arithmetic operations, 48K-word MOS memory with parity, RTC, and APL.

Video Display:

1920-character screen, upper/lower case characters, detached keyboard, numeric keypad, programmable function keys and character highlighting, display rotates on two axis.

Cabinet: 72-inch high, holds all rack mounted components.

60/30 cps; 132-columns; typewriter keyboard, upper/lower case. Diskette Subsystem: 315KB for program/data interchange, diagnostics and software distribution: convenient, industrystandard offline storage.

DASHER

Terminal Printer:

Cartridge Disc Subsystem: 10 megabytes (5 fixed, 5 removable); 50 ms. average access time, shares controller with diskette.

The facts speak for themselves. For \$37,610, Data General's new NOVA 3/D gives you more system, software and support than any comparable computer. And we deliver in 60 days.

Any way you look at it, it all stacks up in your favor. For more information and our brochure, call or fill out and return the coupon.

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tems. The processor is available in two versions from Honeywell Information Systems, Small/Medium Information Systems Div, 200 Smith St, MS 486, Waltham, MA 02154.

The series 60 level 6 processor is 30% faster than the 6/36; when combined with an optional doubleword access memory, performance is 60% better. A scientific instruction processor when added to the machine permits FORTRAN programs to run three times faster than on the 6/36.

The 6/43's central processor is packaged on a $15 \times 15''$ board. Other system elements are contained on similar boards, allowing a multifunctional, compact system of five boards and power supply to fit into a drawer only $5\frac{4''}{10}$ high.

Based on Schottky TTL technology, the processor is open-ended, powerful, and flexible. The firmware-driven processor enables multiple vectored interrupts to 64 levels, provides multiple vectored trap structure, and automatically saves and restores vital information in case of interrupts and traps. Bit, byte, word, and multiple word addressing is provided.

In addition to the CPU, the 6/43 includes Megabus, basic or full control panel, 5- or 10-slot chassis, power supply, multiply/divide, realtime clock, ROM bootstrap loader, and watchdog timer. System memory uses 4096-bit n-channel MOS dynamic RAMs as the storage media. The memory is a bus-compatible subsystem that communicates directly with the bus. Either parity or error detection and correction (EDAC) memory is available. EDAC memory includes six additional bits of code per word, which are derived from data bits and allow any internally caused single bit data error to be corrected when the 22-bit word is read. Both memories may be operated with either a standard single-fetch memory controller or with a doublefetch controller.

All system elements attach to the Megabus and all transfers (memory, interrupts, and instructions) between elements occur on it. Communication between elements is asynchronous, permitting efficient operation of elements having different speeds. The bus offers a transfer rate of 6M bytes/s. All transfers are direct memory access, each device controller maintains its own information about the location in memory and accesses that location directly.

System elements include multiple device controller (MDC), multiline communications processor (MLCP), mass storage controller (MSC), magnetic tape controller (MTC), and general purpose DMA interface. Device Pacs handle a variety of peripherals, while MLCP Communication Pacs control two full-duplex lines each, synchronous or asynchronous, in any combination. The MSC handles up to four cartridge disc units and the MTC handles up to four magnetic tape units.

A scientific instruction processor (SIP) introduced for 6/40 systems is a single-board processor which

operates on a set of 30 scientific instructions that includes arithmetic, operations on single- and doubleprecision floating point operands, and single and double word integer operands. The processor has three variable-length scientific accumulators that may contain floating point values of two or four words. Operands are stored internally in floating point format; 32- or 64-bit formats provide accuracy of six or 14 hexadecimal characters. The unit also provides automatic round/truncate for operations requiring right scaling, mixed-mode precision arithmetic, three scientific control registers, scientific traps, and firmware for a hardware verification routine that tests basic data paths. Circle 141 on Inquiry Card

OCR Reader and Transport Offers Flexibility With No Loss In Speed

Refuting the widely held belief that a sacrifice in speed is necessary to use an OCR unit with flexible recognition logic, Key Tronic Corp, PO Box 14687, Spokane, WA 99214 announced the Datareader, a low cost OCR document transport and reader. When used with the company's M9 electronics module, the Datareader offers multifont, alphanumeric character recognition combined with prac-



Alumax Mic-6 cast aluminum plate. All it needs are your finishing touches.

By the time our Mic-6 cast plate reaches you, the tough work has already been done. It's been stress-relieved, precision-machined and cut to size. All you do is finish it.

What can you do with it? Almost anything. Mic-6 can be sawed, drilled, tapped or milled. And it can be welded or anodized. All at speeds compatible with today's processing equipment.

Mic-6 is held to exceedingly close tolerances. Plate thickness is \pm .005". And its fine, precision-machined surface finish (typically 25 micro-inch) eliminates the high costs of in-plant surface machining.

All in all, it's the "answer material" for computers, printing systems, instrumentation, electronics and other high-spec OEM industries. It saves you the costs of permanent mold castings. And frees you from the eccentricities of wrought plate.

See your nearby Alumax distributor. Or write for the Mic-6 brochure that gives you complete information and specs.

Mic-6 cast aluminum plate from Alumax. We started it, you finish it.



A subsidiary of Alumax Inc. 5555 E. Highway 6, Morris, III. 60450 West Coast office: 1495 Columbia Avenue, Riverside, California 92507 CIRCLE 21 ON INQUIRY CARD



Because of an LSI-11 microcomputer, when this woman speaks, her computer listens.

Since Threshold Technology's introduction of the voice-input computer terminal, man and computer have begun a totally new relationship. A speaking one.

Their Threshold 500 terminal actually allows people to talk to their computers just like they talk to their other co-workers.

At the heart of the Threshold 500 is the highest performance, most software-supported microcomputer on the market. The LSI-11.

For Bob Cox, Chief Engineer at Threshold, anything less just wouldn't have been enough.

"At first we offered our voice-input terminal using a mini. But that put the price of the system at \$18,000 – a price that was way out of line with a lot of applications. So to cut costs, we developed our own micro from chips. Then the

Since Threshold Technology's LSI-11 came out. Right off, we troduction of the voice-input knew it was the answer.

"By incorporating the LSI-11 into our system, a lot of good things started happening.

"First, the price was reduced to about \$10,000. That's a 45% cut in cost. We were also spared the time and capital investment involved with setting up manufacturing facilities for a micro, as well as all the testing and support services we would have to provide. The fact was



Bob Cox, Chief Engineer at Threshold Technology, Delran, New Jersey

digital

COMPONENTS GROUP that the LSI-11 cost no more than the micro we had designed ourselves. Best of all, we were getting a computer that performed just as effectively as the mini we had used before. Solutions don't come much better than that."

For a lot of applications – like Threshold's and perhaps your own – anything less than the LSI-11 isn't really enough. Why not ask us more about it.

We're as easy to talk to as our computer.

For 600 pages of solid technical information, plus our new brochure of microcomputer case histories, "Why Anything Less than the LSI-11 Wasn't Enough for Me," just call toll free 800-225-9480 (in Mass. 617-481-7400 ext. 6819), or write Digital Equipment Corp., One Iron Way, Marlborough, Massachusetts 01752.



DIGITAL TECHNOLOGY REVIEW

ticality, reliability, and accuracy. It can read and process up to 3900 documents/hr.

Using microprocessor technology, the M9 alphanumeric recognition module has a software controlled electronics recognition unit that offers high level character resolution. Sensitivity adjustments located on the front panel allow the operator to fine tune or detune the recognition circuits to expand the range of character recognition.

Read heads have vertical adjustment to accommodate variations in form sizes ranging from a minimum of 1" in height by 2½" in length to a maximum of 6" in height by 8¼" in length. The unit can read and process OCR-A numeric and alphanumeric, Farrington 7B and 12F, MICR print, handprint, OCR-B, 407, 1428, and subsets of OCR-A numeric, OCR-B, and handprint.

The unit incorporates a jam detection device. If an irregular (in size, shape, or thickness) document causes a paper jam, a sensor in the transport detects the condition and causes the unit to shut down. After the jam has been cleared, the unit is restarted by depressing the start button either manually or by a foot control. The autofeed mechanism can be adjusted for document thickness to ensure single document selection. A control knob on the front of the unit lets the operator set the mechanism for the particular weight of document being processed. A multidocument detector shuts down the transport automatically if the thickness control has not been set correctly.

Circle 142 on Inquiry Card

Replacement Disc System Increases Throughput, Lowers Cost

A completely compatible replacement for IBM 3350 disc drive units, the STC 8350 disc subsystem features two disc storage spindles and can be operated in native mode with 317.5M bytes/spindle to provide 635M bytes/unit. The units incorporate rotational position sensing to increase system throughput by disconnecting the disc drive from the control unit during rotational delay times.



Storage Technology's 3350-compatible disc subsystem model 8350 operates with 635M bytes/ unit and 25-ms average access time to provide cost-effective storage for IBM System/370 users

Available from Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027, the unit connects directly to the integrated storage control (ISC) in System/370 models 145, 148, 158, and 168, or to an STC 8000 control unit. Formats include 3330 model 1 compatibility, emulating two spindles of the 3330-1 (using 200M bytes of the 317.5M bytes available on each spindle); and 3330 model 11 compatibility, emulating one spindle of the 3330-11 (using 200M bytes of the 317.5M bytes available).

The unit is available in three models, each with two spindles of 3350-compatible storage. A2 contains control functions to operate a string of up to eight spindles; the B2 contains no control function, but up to three units can be connected to an A2 for a maximum of eight spindles. The C2 may be substituted for one B2 in a string to provide an alternate backup control function to the A2 in the string.

When operated in native mode, each spindle has capacity for 317.5M

bytes or 635M bytes/unit. Data transfer rate is 1198k bytes/s. Average access is 25 ms with an average latency of 8.4 ms. There are 15 recording surfaces/spindle with two read/write heads/surface. Track density is 480 tracks/in and data are recorded at 6425 bits/in.

Standard features include an operator panel control switch to prevent accidental erasure of recorded data and full track read to significantly improve disc dump operation by allowing a full track to be read with a single channel command. A high speed dump/restore software program improves dump/restore performance while going to or from magnetic tape. A write format release disconnects the disc drive from the control unit during completion of the last formatted write on a track, allowing the control unit to perform other operations while the disc drive pads zeros to the end of the track.

Circle 143 on Inquiry Card

Computer System Understands and Acts on Verbal Commands

A computer system which can understand and act on human speech, Harpy has demonstrated that it is technically possible to communicate man to machine using natural language. Although not capable of carrying on a conversation, the system recognizes a 1000-word vocabulary with high accuracy.

Representing successful completion of a project funded by the Advanced Research Projects Agency (ARPA) of the Dept of Defense and conducted at five universities and research institutes, Harpy was developed at Carnegie-Mellon University, Schenley Park, Pittsburgh, PA 15213 by Drs Raj Reddy and
Choosing Systems or Components: Know your weapons.

Developed by Zilog. Manufactured by Zilog. Supported by Zilog. Here are the most powerful weapons on the microcomputer battlefield. Together or separately they herald victory over sluggish speeds and villanish inefficiencies.

Manufactured by Zilog.

Whether you need one or a million and one, Zilog's new facility can deliver. All of our production equipment is state-of-theart (4" wafers) — the most modern microcomputer manufacturing in the world. You order. We'll deliver, plastic or ceramic. Your choice!



Masterminded by the Z80-CPU.

A single chip, N-channel processor arms you with a super-set of 158 instructions that include all 78 of the 8080A's and the 8085 instructions with total software compatibility. The new instructions include 1, 4, 8 and 16-bit operations, such as, memory-tomemory or memory-to-I/O block transfers and searches, 16-bit arithmetic, 9 types of rotates and shifts, bit manipulation and a legion of addressing modes. And that means less programming time, and less end user costs. With these features, the Z80-CPU generally requires approximately 50% less memory space for program storage yet provides up to 500% more throughput than the 8080A or the 8085. Powerful ammunition at a surprisingly low cost (less than \$10 each in large quantities) and ready for immediate shipment.



Deploy the Z80 peripheral devices:

Z80-PIO—Parallel I/O Interface Controller. Two (2) ports for fast I/O transfer under full interrupt control.

280-SIO—Serial I/O Interface Controller. Two (2) fully independent full duplex channels that can be programmed to operate in any asynchronous or synchronous modes including Bi-Sync and HDLC/SDLC.

Z80-CTC—Counter Timer Circuit. Four (4) independent channels that can be used to count external events or to generate interrupts at programmable intervals.

Z80-DMA—Direct Memory Access. Programmable circuit that transfers data between memory and peripheral devices at up to 1.2 megabytes per second. The DMA can operate in a transparent mode without slowing the CPU.

Deploy the Z80 software:

Resident Macro Assemblers. With crossreference and conditional assembly, also relocatable assembler with linking loader. PLZ Resident Compiler. Most powerful microcomputer compiler available today.

Text Editor and File Maintenance. Basic Interpreter. For writing programs in Basic

Cross Software. Available from NCSS.



Made for the Military.

You can get Zilog components to meet MIL Spec 883B with extended temperature range of -55°C to +125°C. The Z80 component family operates with less power in MIL Temp environments.

For victory over obsolesence:

Deploy these strong components from the leader in microprocessors. We are bound by our pledge to stay a generation ahead and determined to make your components and systems the most powerful in the field. We're ready to dispatch help immediately.

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Mostek SDB-80. Z80 Power and

CONTROL

PANEL

The solution for OEM applications.

For OEM applications the

 (MK3882), serial ASCII interface
 (110—9600 baud) sockets for up to
 5K bytes of PROM or 20K bytes of
 ROM, plus a fully buffered and highly
 sophisticated system bus for
 complete expandability (including multi-processor applications).

These features are not only important in the user's final system, but also permit the SDB-80 to be used as an extremely powerful software development station, providing even greater savings.

X-Y

PLOTTER

LASER

High level languages such as BASIC are also easily supported with the SDB-80 by loading either Z80 or 8080A based interpreters/compilers into the 16K bytes of on-board RAM.

The solution for software development.

For software development, the SDB-80 is available with a complete package of software development

aids in ROM. This optional 10K byte firmware package may be located in sockets on the board to provide the ability to generate, edit, assemble, execute, and debug programs for all types of Z80 applications. Other features include channeled I/O for user-defined peripheral

MODEM

SDB-80 is one of the most powerful, yet low cost microcomputers available in the industry today. For \$995 (single unit quantities) the SDB-80 single board microcomputer includes Mostek's Z80 CPU (MK 3880), eight MK 4116 16K RAM memories, two PIO's (MK 3881), one CTC SIGNAL GENERATOR

> A/D CONVERTER

FILTER

UNDER

TEST



The \$995* solution. 16K Bytes of RAM.

drivers, relocatable object module generation with a corresponding linking loader, a complete set of console routines for examining and/or modifying memory and port locations, and a set of driver routines for various standard peripheral devices.

For users requiring even greater system capabilities, the SDB-80 is fully expandable through the use of optional add-on boards. In this way the user may configure his system to include whatever amount of PROM, ROM, RAM or I/O desired, plus add

CARD

READER

LINE

such features as in-circuit emulation floppy disk interfaces, and PROM programming capability.

Non-resident software development is also supported through the use of Z80 Cross Assemblers which are available for both Fortran IV and 8080A systems. The resultant object code can then be loaded into the SDB-80 for

> PER TAPE READER/ PUNCH

For more information on the SDB-80 and the complete range of optional support boards, software, and boxes, contact your local Mostek sales office or representative.

MOSTEK

1215 West Crosby Road Carrollton, Texas 75006 (214) 242-0444 In Europe, contact: MOSTEK GmBH W. Germany Telephone: (0711) 701096 MOSTEK ASIA Hongkong Telex: 85148MKA H X

CIRCLE 24 ON INQUIRY CARD

One piece quantities. Prices apply within the U.S. and Canada, Eurocard version available, Contact Mostek GmBH



DIGITAL TECHNOLOGY REVIEW

Bruce Lowerre of the Computer Science Dept. Other systems developed at CMU; Bolt, Beranek and Newman; and Systems Development Corp, while not meeting specific performance goals, have contributed significantly to the understanding of the speech decoding process.

Basic goal of the ARPA project, begun in 1971, was to determine whether it was scientifically and technically possible to develop a system that would enable people to communicate directly with a computer through a microphone. The real measure of how well the machine understands connected speech is how well it is able to execute the verbal commands that it receives. In designing speech-understanding systems, the elements of characteristics of speech sounds (phonetics), variability in pronounciations (phonology), stress and intonation patterns of speech (prosadics), sound patterns of words (lexicon), grammatical structure of language (syntax), meanings of words (semantics), and context of conversation (pragmatics) must all be accounted for.

In demonstrations on an information retrieval task, Harpy can be asked, via microphone, to search a computerized data file for abstracts and citations of scientific articles on a desired topic-or to conduct other types of searches that might now be instituted on a keyboard terminal. The system's answer appears as a printout or visual display on a terminal. Questions like "What is the title of that paper? Who wrote it? Is heuristic programming mentioned?" are asked one at a time. As soon as Harpy understands the speech, it responds to the questions, maintaining a knowledge of what was previously asked and referring to it as necessary.

Questions to Harpy must be on the topic, and must be phrased fairly precisely. Even so, acceptable speech is much less rigid in format then most other means of addressing the computer. Usually, instructions typed into a terminal, for example, must be entered as key words and symbols that are allowed by a programming language, and often even the smallest deviation—a comma out of place, a space between symbols where one is not allowed—results in an instruction that can not be processed by machine. Harpy has been "trained" to recognize the voice patterns of five operators, three males and two females, using normal speech into a headset microphone. It understands 97% of the words, and 91% of the sentences exactly as spoken. More important, it has a 95% semantic accuracy, a measure of how often it is able to complete the requested task.

A one-of-a-kind research modelwhich requires the resources of a major PDP-10 computer system for test runs-Harpy is not feasible for wide scale application. However, Dr Reddy believes that by using currently available technology the system could be re-engineered to run on a minicomputer, dropping processing costs from the current \$5 per second of speech to about \$0.05. The second constraint is processing time; it currently takes Harpy up to 4 min to understand 3 s of speech. However, Drs Reddy and Lowerre think that reasonable engineering and research efforts will be able to bring speeds up to those used by humans in conversation.

The researchers believe that the real scientific achievement in their work on connected speech understanding systems has to do with the idea of machines that can operate in "errorful domains." In the systems, as speech is analyzed, every decision made in the process of interpretation has some probability of being wrong. So the systems continually look for the best match of patterns, or the most likely, logical choice of words. Thus, each system is more reliable than any of its components. The researchers cite significant progress in machine recognition of acoustic phonetics-developing systems that can recognize and differentiate among sounds-and believe that Harpy has demonstrated the feasibility of speech as a form of man-machine communication. Circle 144 on Inquiry Card

Federal Standard Proposed For Computer I/O Interface

First of a planned family of computer peripheral interface standards, the Draft Proposed American National Standard Specification for Input/Output Channel Interface defines functional, electrical, and mechanical parameters for attaching peripheral controllers to a computing system. Proposed by the National Bureau of Standards Institute for Computer Sciences and Technology, as a Federal Information Processing Standard (FIPS), the standard's technical specifications were developed by the American National Standards Institute (ANSI) Technical Subcommittee X3T9.

When fully implemented, the proposed standard will help ensure economical procurement and effective utilization of Federal automatic data processing systems by enabling them to be configured with components procured from multiple competitive sources and drawn from the Federal inventory.

A copy of the proposed standard may be obtained from the NBS Office of ADP Standards Management, Washington, DC 20234. Comments regarding it should be sent to the same address before March 31, 1977.

Circle 145 on Inquiry Card

Reliable, Low Cost Cassette Transport Uses Molded Plastic Parts

The model 250B digital cassette recorder, manufactured by MFE Corp, Keywaydin Dr, Salem, NH, represents a breakthrough in cassette tape transport design. There are no capstans, solenoids, pinch rollers, clutches, belts, pulleys, or other mechanical elements involved to lower performance and reliability. This, plus the use of integrated circuits throughout, provides maximum dependability and performance at minimum cost.

All precision hardware in each transport—motors, recording head, and cassette locators—are secured to a single steel plate. Because there are no capstans, the cassette is "front loaded" into the head (the head never moves), and the same precise headto-tape relationship is maintained every time a tape is loaded on every single tape transport. This guarantees cassette interchangeability from transport to transport.

In addition, key subassemblies associated with mechanical positioning of the cassette shell and head-to-tape alignment—formerly machined and aligned with jigs and fixtures—have been replaced with precision injection molded plastic parts. After an exhaustive search, fiberglass loaded LEXAN



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(TMGE) was chosen as the appropriate material to be hard-tool injection molded. MFE worked in conjunction with Hy-Ten Dye and Development Corp, Power Street Extension, Milford, NH 03056, to design the tooling and to mass produce these parts.

Combination of the hard-tooled steel plate and the precision molded parts allows the unit to be assembled without any mechanical adjustments and, at the same time, guarantees a much more accurate manufacturing tolerance repeatability than is achievable via jig and fixture alignment as used in other transports.

One of the major concerns of digital cassette users is the ability to interchange tapes between different transports. The critical relationship that exists between the head assembly and the cassette tape must be maintained to achieve proper tape tracking every time that a cassette is removed and reinserted between transports. The 250B incorporates fixed head assemblies which minimize mistracking when the cassette is inserted or removed. The critical alignment between the cassette and the head is assured by the two guide block assemblies which position and ensure that the cassette shell is maintained at the proper height with respect to the precision head assembly. In addition, these assemblies not only assure that head penetration into the cassette is maintained to tight tolerances, but guarantee user repeatability each time the cassette is removed or reinserted. Parallelism between the plate and cassette shell is further ensured by a single rear precision reference surface, which is part of the cassette loaded switch assembly, and thereby provides a true three-point suspension for the cassette shell.

Another major achievement in the lack of mechanical adjustment comes from the "write permit" switch assembly which is so precisely designed that it will work with any ANSI/ ECMA compatible shell without requiring any adjustments or realignment. End result is that the transport does not require a single mechanical adjustment during its manufacturing process, or any mechanical maintenance by the customer in the field, other than head cleaning.

By eliminating moving parts, maintenance is eliminated. Occasional cleaning of the recording head is all that is required to keep the transport in perfect operating condition. Under continuous 100% operation, the unit has an MTBF of greater than 15,000 h; MTTR (mean time to repair) is less than 30 min.

The unique tape handling system results in constant tape speed, low bit-to-bit jitter $(\pm 3\%)$ and extremely gentle tape treatment even under the most severe start and stop operating conditions. Users can choose any tape speed from 2 to 120 in/s and any recording density up to 800 bits/in without factory modification or adjustment. For complex applications, any bit rate may be selected by simply changing the tape speed, allowing data to be collected at low speed and transmitted over communication lines at high speed. The 250B is fully bidirectional and operates in a continuous or incremental mode. Character blocking can be arranged to fit application needs.

Circle 146 on Inquiry Card

Multimodular Core Memory Lowers Space and Power Requirements

A fully compatible multimodular core memory for Univac computers, the T-70005 occupies 32% of the

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DIGITAL TECHNOLOGY REVIEW

floor space, runs on 70% less power, and costs less than half of that built by the original equipment manufacturer. Storage capacity begins at 65,536 40-bit words, and can grow in 32,768-word increments.

Developed by Telefile Computer Products, Inc, 17131 Daimler St, Irvine, CA 92714 as plug-compatible direct replacement for multimodular memory on Univac 494, 1106, 1108, and 1110 computers, the system meets or exceeds all speed, performance, and interface requirements of the equivalent Univac memory. It is software transparent and no programming changes are required. Data are retained in the event of power interruption, allowing the host to proceed with data save operations when power failures occur.

A single cabinet houses one or two 32,768-word memory chassis assemblies together with modular power sections. The pluggable dc power drawer can be replaced by maintenance service personnel. Only two other replaceable circuit modules-interface and memory-are necessary to maintain the unit. Connection to the processor is accomplished with a single cable to an interface module for each 32,768 word memory chassis. Multiple cabinets may be used in configurations requiring more than 65,536 words. Memory units may be located anywhere within a 10' radius of the rear of the Univac processor.

Access to memory may be interleaved between 32,768 word increments, effectively doubling the memory's standard 750-ns cycle time. Cycle time can be matched to system cycle times of 875, 1000, or 1500 ns. Priority circuits are included in the interface module to ensure proper access priority definition in a multiprocessor configuration.

Miniature LED indicators on each interface module enable service personnel to pinpoint faults in data, address, and control lines. Each unit contains indicator lights for determining parity errors in any of the four memory modules that it contains. Mean time to repair is estimated at a maximum of 30 min. Circle 147 on Inquiry Card

Visual Display System Allows Concurrent Entry, Batch, and Inquiry

A multifunction visual display capability that can be configured to provide concurrent data entry, remote batch, and online inquiry functions, the model 82 remote display system is compatible with mainframes using IBM 3271 protocol. Emulation capability will be offered on appropriately configured existing model 78 remote processing systems and model 74 Keybatch systems. In multiprocessor configurations, this will provide a concurrent multifunction system featuring shared display and full backup capability.

Announced by Data 100 Corp, 6110 Blue Circle Dr, Minneapolis, MN 55435, the unit consists of a processor, video controller, and diskette storage device for loading control programs and system diagnostics, and accommodates up to 16 1920char or 32 480-char display stations



An IBM 3271-compatible online inquiry system, Data 100's model 82 remote display system allows up to 32 stations to perform inquiry, data entry/capture/collection, or other CPU-accessing functions concurrently

located up to 2000' from the controller. Stations operate interactively on a real-time basis with host-based programs and files. Data can be added, modified, or deleted, and then sent back to the computer for storage or further processing under control of the host-resident application programs.

An operator-controlled display station switch allows users to operate each station as if it were two separate units. In dedicated systems, a single station can appear to the computer as two separate stations, each performing a different application. When configured with two controllers, each station can be alternately used for offline data entry and online inquiry communications with one or more mainframe computers.

Serving as the interface between operator, communications line, display stations, system line printers, and other control units, the control unit contains processor, memory, operator control panel, communica-tions interface, and diskette storage unit for use during normal operations for loading control programs and system diagnostics. Its communications interface operates with any RS-232 data set at speeds from 2000 to 9600 bits/s on dialup or dedicated multipoint, 2- or 4-wire lines. Line protocol is compatible with the IBM 3271 information display system controller and uses the standard EBCDIC code set.

Connecting directly to the system controller, system line printers range in speed from 62 to 300 lines/min. They are standard full character belt printers with interchangeable character clips. A 12-channel vertical format control allows efficient vertical spacing with 6 or 8 lines/in vertical line density; also provided are line advance suppression capability, 132-col print lines, and 63-char EBCDIC print set. Up to eight printers can be used as local or station printers and can be located up to 2000' from the system. Circle 148 on Inquiry Card

Computerized System Speeds Production of Graphic Hardcopy

Producing high quality graphic hardcopy 50 times faster than is possible with pen-plotter systems, the Plotmaster[™] system links to any IBM System 360/370 computer, reducing both plotting time and internal storage requirements. The flexible sys-



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Additionally, you can use block or character editing combined with high-speed tape duplicating and fast file search.

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To arrange a demonstration with your system call your nearest TI office listed below. Or write Texas Instruments Incorporated, P. O. Box 1444, M/S 784, Houston, Texas 77001. Or call Terminal Marketing at (713) 494-5115, extension 2124.

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GSA Contract Group 66



DIGITAL TECHNOLOGY REVIEW

tem, developed by Gould Inc, Instrument Systems Div, 3631 Perkins Ave, Cleveland, OH 44114, consists of an electrostatic printer/plotter, diversified graphics software, and a hardware interface between the printer/plotter and the software. Interface may be an online controller or a tape drive for offline operation, or may combine the two for either mode of operation.

Sharp, high resolution (up to 200 dots/in) hardcopy is produced at rates 50 to 400 times faster than incremental pen-plotters. Since no film processing and enlargements to hardcopy are involved, drawings are available faster than with microfilm systems. Resolution can be modified by software to produce "halftone" effects, useful in applications involving continuous tone copy, such as X-ray negatives, photographs, and brainwave scans. "Staggered head" electrostatic imaging techniques yield high contrast.

Standard plot package for the system is a set of FORTRAN-callable routines which use CalComp-compatible names and calling sequences. The packages can be used to generate any geometric construction complete with desired annotation. Subroutines can be used as building blocks to form complex routines for specific applications. Among the special features are selection of several standard background grids, capability of merging with user-designed grids, variation in line weight, automatic stripping, scaling of character height, and erasure of previously generated lines.

Link between the plotter and software is performed by an interface housed in a separate console that can provide online or offline operation, or a combination of the two. For online operation, the controller uses either the IBM selector, a selector subchannel, byte multiplexer, or a block multiplexer control. For offline use the controller includes a 9-track, 800- or 1600-char/in readonly tape drive for System 360/370 input.

Circle 149 on Inquiry Card

Multiprocessor Computer Based on Bidirectional Data Communication Bus

A multibus, multiprocessor computer system, ModulexTM offers expandability and performance using a building block approach. Basis of the system, introduced by Artronix, Inc, 1314 Hanley Industrial Court, St Louis, MO 63144, is a bidirectional data communication bus—a multilayer PC board that allows communication between connected system modules at rates up to 10M bytes/s. Priorities are resolved and accesses granted by a bus control unit which monitors data transfers between system modules.

Configured as a dual-slot module, the standard minicomputer is a full 16-bit processor which includes seven general-purpose registers and 98 instructions with seven addressing modes. MOS random-access memory with a cycle time of 480 ns is supplied in 16k-byte single-slot modules. Up to 64k bytes are directly addressable on the bus, or up to 1M byte with each memory management unit (MMU) used.

Control between multiprocessor buses is attained through the use of asynchronous real-time link (RTL) modules, while data transfers between buses are made through the MMU modules, providing either centralized or distributed memory management capabilities. Monitoring system modules on the bus using a unit other than the processor permits flexible configuration. Typically, four processors may be attached to a bus and may perform independent or related functions without conflict.

The system is completed by a range of peripherals including array processors, digital video graphic system, and mass storage devices that range from a floppy disc to a large high speed mass storage module. MX/OS, the operating system software, is as modular as the hardware. It is divided into a series of semiindependent modules, each performing a certain class of functions. A multiterminal, multiprogramming environment is supported with up to 255 active partitions. The virtual memory scheme supports contiguous, chained or hierarchical file structures. The system presently supports the MUMPS and FORTRAN IV application languages.

Circle 150 on Inquiry Card



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The SEL 32 family of high performance 32-bit computing systems offers a balance between big computer performance and minicomputer prices. Microprogrammable input/output processors, compatible central processing units, high-speed memory systems, and efficient data processing peripherals make up the hardware elements. On the software side, operating systems, language processors, libraries, application packages, and interactive terminal support balance the scales. Together, SEL 32 hardware and software provide a cost-effective solution to your current requirements, with expansion capability to meet your growth needs.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Computerized Ripple Control Eliminates Excessive Drain On Electric Utility Supply

Demand for electric power, as with similar demands for fuel supplies, has been continually expanding. Because the cost of finding and developing new sources of energy, or even of increasing available supplies of present fuels, are almost prohibitively high, steps have been taken to reduce—or at least control—the consumption of fuel.

One procedure that evolved from the attempts to control use of energy is "ripple control," an electric power load management system that automatically shuts off selected appliances or equipment in homes, offices, and industrial plants for brief periods of time to flatten out peaks in power consumption. Such regulation can be provided from a central location—under computer control, for instance—or locally in small installations.

In all cases, control signals are transmitted from the controller in the form of coded audio frequency pulses which are injected into the utility power grid. Dual-channel solid-state relays (receivers) mounted on the appliances or equipment being controlled decode specific signals which contain the on/off signals.

Ripple Control

Cumulative power consumption is normally dependent on the various whims of all consumers: turning equipment on or off, lowering or raising cooling demands of air conditioners, or deciding to use or not use certain appliances. As a result, load curves exhibit numerous peaks and valleys. Smoothing out those curves by removing the causes of the peaks and valleys is the purpose of "ripple control."

One type of such control, called Rythmatic^R, enables daily load curves to be "smoothed" and thereby provides economic use of generating capacity and distribution networks. Plessey Inc, 20245 Sunburst St, Chatsworth, CA 91311 has recently installed its first system in the United States, but other systems—some under computer control—have been installed by The Plessey Co Ltd in England, New Zealand, and other countries, resulting in claims for "10% discount on new power generation costs."

Direct control of switching devices from remote locations under the Rythmatic system is accomplished using standard high voltage power lines as the transmission medium. Coded audio frequency signals superimposed onto those lines are decoded by receivers in applicable locations within the low voltage distribution network.

Control signals, therefore, require no added transmission medium. In practice, an audio frequency between 300 and 1000 Hz is assigned to each distribution authority. Although in centralized systems the same coding system will be used by each authority operating on that system, the available range permits assignments of frequencies that will eliminate interference between neighboring authorities. Also, the superimposed voltage is too small to cause interference with the normal distribution network.

Rythmatic coding varies the pulse repetition rate (rhythm) of the carrier frequency within a range of 50 control codes from 1 to 10 pulses/s. Each receiving device will respond only to commands given at that device's particular rhythm.

Pulse trains are transmitted for 10 s and operating relays must receive a continuous train of at least 5 s before they will accept a command. Interference problems from harmonics and other ripple control systems are therefore practically eliminated.

The solid-state receiving relay, located on the consumer's equipment low voltage line, has two decoding modules: one to switch a device on, and one to switch it off. Therefore, 50 rhythms provide 25 separate control commands or channels. This capacity can be extended, however, by multiple coding techniques or by using three rhythms to control two channels with one rhythm as a common off signal.

Ripple signal injection points generally range from 400 V to 69 kV, dependent on a number of factors. Most commonly, a method known as parallel injection is used in which the signal frequency is in parallel with the high voltage link at the supply substation. Circuits are tuned to the ripple frequency for maximum transfer of energy.

Computerized Central Control

When ripple control signals are injected onto the network from a central controller, remote injection plants can be operated individually, simultaneously, or sequentially. The central controller can be either an extension of local control or a computer.

Signals can be initiated manually, automatically by program, automatically by load control, or by time switch. Pulses injected onto the network are controlled by the central rhythm generator. A further audio frequency pulse train is transmitted from the control room as a synchronizing control when a number of plants are under ripple control simultaneously.

Under computer control, the load dispatch system functions under either a dedicated computer, such as a DEC PDP-11, or in timeshare with an existing plant

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A UNIT OF PERKIN ELMER DATA SYSTEMS CIRCLE 35 ON INQUIRY CARD



DIGITAL CONTROL AND AUTOMATION SYSTEMS

computer. In one such configuration, the Auckland Electric Power Board in Auckland, New Zealand bases its master control on dual Honeywell 316 computers. That system is used to reduce peak load and improve the daily load factor, and has resulted in reduced reserve capacity requirements as well as less need for higher priced peak energy.

For the most part, customers are not deprived of the electrical power needed to operate water heaters, to heat plants, or to light streets. Except for street lights, where use is limited in any case to nights, the computer predicts when a peak is to occur and trims power usage to avert excessive energy drain. Power is restored for heating when the overall usage levels off or starts to form a valley.

The power board services a 935-km² area made up of 3250 km of overhead and 2650 km of underground circuits. Customers are densely populated city areas, heavy and light industry, suburban housing, and semirural areas. Distribution is via 36 main and 4400 secondary substations.

Control is primarily of a range of water and space heating units, but secondary functions include street lighting. A total of 130,000 solid-state receiving switches, with a maximum switchable load of 150 MW, are controlled from 12 injection points.

Load shaving and restoration are controlled by a standard control algorithm on the basis of anticipated consumption in time periods selectable at 0.25, 0.5, or 1 hour. Consumption for a current time period is predicted by analysis of consumption at given points in the period, the instantaneous load at the time of prediction, and the mean rate at which the load is changing.

Sufficient flexibility is maintained to permit the algorithm to be changed readily to provide load control on any other basis: eg, instantaneous, daily, or weekly loads; ambient temperature, length of time equipment has been on or off, or a combination of these. Although acceptance of control is optional for the consumer, the rate paid by the consumer to the power board for non-controlled use of energy is twice that of controlled power.

Information transfer between control computer and remote plants is handled via telephone communication lines, either a dedicated circuit or the switched network. An interface unit accepts synchronous serial



under ripple control. When predetermined level is reached, potential peak load is shaved in three stages; then portions are restored to main level demand



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CIRCLE 37 ON INQUIRY CARD

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command codes from central control and initiates transmission of control signals to the plants. It also queries the channels to determine that the signals have been received and reports to the computer that correct signals have been sent.

Modem interface meets CCITT V24 or EIA RS-232-C specifications. Configuration can be direct, multidrop, or dial up. Transmission speeds are 75, 110, 150, 300, 600, 1200, 2400, 4800, or 9600 baud. Operation can be either continuous or polled. Message lengths typically are two words control to plant, five words plant to control. Word format is one start bit; five, six, seven, or eight data bits; odd, even, or no parity bit; one or two stop bits.

Other Installations

Among diverse other applications in New Zealand are one in use by the Hawkes Bay Farmers Meat Co which uses only a single injection plant under local control, and one at the Namoi Valley County Council Supply authority that has three automatically controlled injection plants. Both function basically the same as the Auckland Electric Power Board installation except that no computers are involved.

The meat company deals mainly with the killing, processing, and freezing of cattle, sheep, and lambs for both local and overseas markets. Reducing peak load and improving daily load factor involves freezers, dryers, boilers, and rendering units plus heating and lighting. It is estimated that under present cost conditions, the plant would pay for itself in two years.

Control of the power supply authority is maintained by a programmed clock which sends out on/off commands at preselected times. An automatic load leveler monitors the system load—water heating, night store heating, and irrigation pumps—and sends appropriate override commands when necessary to keep the load as close as possible to a present optimum level.

In the U.S. the first installation is at the Southwest Public Power District of Palisade, Neb. This system controls 15% of the summer irrigation load in the area by stopping and starting the irrigation drive motors. A somewhat similar system is being installed in Wisconsin. Both systems use central control but neither is computerized.

Circle 160 on Inquiry Card

DC&AS BRIEF

Minicomputers Assist in Hospital Laboratory Test Analysis

Several hospitals in England are now using minicomputer-based systems for analysis of tests. In one case a Nova^R 1220 computer assists in the analysis of biochemical samples from patients at hospitals in the Kensington and Chelsea areas of London. At the North

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Staffordshire Health District in the North Staffordshire Health Center, Stoke-On-Trent, one of the country's largest hospitals, a Nova/830 checks and analyzes the results of tests carried out in the hospital's pathology laboratories. Both computers are manufactured by Data General Corp, Southboro, Mass.

The 1220 computer is used to speed up the computations involved in analyzing patients' samples and in checking that the results fall within prescribed limits of accuracy. It is also used to print the results of the analyses and to provide a number of reports for use by the hospitals' consultants.

About 1000 samples a day are processed in the laboratories from the hospitals, which have a total of about 1700 beds. Each sample is identified by a test code which, together with information about the patient and the sample batch number, is input to the computer from a visual display unit when the sample is received.

An auto-analyzer produces a graphic analysis of the substances in the sample. Peaks on the graphs indicate the concentrations of the constituent substances in the sample; values are read and are recorded on paper tape for subsequent input to the computer which performs the necessary calculations.

The 830 computer, part of the hospital's main information processing network, has functions beyond those common to a normal pathology laboratory environment. Four visual display terminals and four teletypewriter terminals are connected to the computer which, in turn, is directly connected to the hospital's main computer. This allows information from the hospital's data base to be updated and acquired where necessary. (The data base also can be accessed from some 90 other terminals.)

Three visual display terminals are installed in specimen reception areas in the City General Hospital, the North Staffs Royal Infirmary, and the Central Outpatients Department. The fourth visual display terminal and one of the teletypewriter terminals are directly associated with the minicomputer. The remainder of the teletypewriter terminals are installed in the hematology, microbiology, and autobiochemistry laboratories.

Full configuration includes, in addition to the terminals, 48k-word central processor, 10M-byte disc unit, magnetic tape drive, paper tape reader, 300-line/min and 165-char/s printers, and mark sense card reader to deal with results produced by manual tests.

The majority of requests for tests to be carried out will be initiated from the wards through terminals connected to the main computer. Before being dispatched to the laboratories, samples from the wards will be checked, using a terminal, against the request to ensure that the correct type of specimen has been submitted for the required tests, that there is sufficient material to carry out tests, and that all the specimens expected have arrived. The minicomputer will produce batch lists for the specimens and work schedules for each machine. \Box Amphenol® 17-Series rear-release connectors, contacts, and crimpers.

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CIRCLE 42 ON INQUIRY CARD



This year, New York City will be the location of ELECTRO77. Formed in the merger of the IEEE INTER-CON and the Northeast Research and Engineering Meeting (NEREM), the show is sponsored by New York area and New England elements of the Institute of Electrical and Electronics Engineers and the Electronic Representatives Association.

The Professional Program Committee, under the direction of Chairman Dr John Golembeski, Bell Laboratories, Holmdel, NJ, has put together a program that includes sessions focusing on advances in microcomputer hardware and software; semiconductor, CCD, and bubble memory technology; communications; computer-aided design; and techniques for testing complex digital assemblies. Seven sessions, from the planned 42 half-day sessions and an evening "special" on U.S. and Soviet Psychic Research, will be held concurrently at 10 am and 2 pm on Tuesday, Wednesday, and Thursday at the Hotel Americana.

Preceding the convention opening, the Electro Keynote Luncheon, to be held at the Americana Hotel on Monday April 18, will feature an address by Isaac Asimov, nationally known science writer and academician. The Luncheon Program also features the presentation of the IEEE Medal of Honor.

Manufacturers product exhibits and demonstrations will occupy two floors of the Coliseum. Of special interest is a display on "Energy Conservation" which will contain examples of the work being done in developing energy alternatives. A Film Theater will screen a program of selected engineering and scientific films daily in the Coliseum. Exhibit hours are 9:30 am to 6:30 pm on Tuesday, 9:30 am to 9 pm on Wednesday, and 9:30 am to 5:30 pm on Thursday. The registration fee of \$6 for IEEE members (\$9 for others) covers all three days of the exhibit and convention sessions.

Only sessions of particular interest to readers of *Computer Design* are covered in the following excerpts from the convention program. Information is limited to that available at press time.

Professional Program Excerpts

Tuesday Morning

Session I IO am-12:30 pm Royal Ballroom A

Switching Power Supplies

Organizer/Chairman: Robert H. Okada, R O Associates, Menlo Park, Calif

Panelists Mel Kravitz, Switching Power; Tom Ingman, Alpha Power; Walter Hirshberg, ACDC Electronics; and Derek Chambers, Raytheon/Sorenson will discuss the case for switching power supplies together with switching vs linear techniques, advantages and disadvantages of various switching techniques, available components, and the importance of accurate efficiency measurements.

Session 3 10 am-12:30 pm Imperial Ballroom A Microcomputers for Fun and Profit

Organizer/Chairman: Frank J. Burge, Regis McKenna Advertising, Palo Alto, Calif

Taking a look at the hobby and personal computer market, this session discusses how the trend started and where it's heading, what people are doing with microcomputers and what a personal computer is like, and attempts a customer profile.

"The Hobby Computer Market: Its History, Size, and Where It's Headed," Bob Wickham, Vantage Research

"Characteristics of the Ideal Personal Computer and Uses," Carl Helmers, Byte magazine

"The Neighborhood Computer Store and Its Customers," Paul Terrell, The Byte Shop Session 5 10 am-12:30 pm Imperial Ballroom B

The Semiconductor Memory Revolution

Organizer/Chairman: Paul Franklin, Monolithic Memories, Sunnyvale, Calif

The continuing revolution in semiconductor memories has radically changed the electronics industry, specifically computers and their associated peripherals. The technology's rapid pace since 1970 has perplexed and overwhelmed users with a variety of products. This session attempts to clarify state-of-the-art semiconductor memory trends.

"Advances and Recent Trends in EPROMs," Jim Oliphant and Bob Greene, Intel

"Registered p/ROMs Impact Computer Architecture," John Birkner, Monolithic Memories

"16k RAMs—A New Generation of Memory Products," Derrell Coker, Mostek

"Future Directions in 4k Static RAMs," Stephen K. Campbell and Joe Kroeger, Advanced Micro Devices

"Applications-Oriented Soft, Low Cost I²L Dynamic RAMs," Tom Longo, W. Sanders, J. Early, Fairchild Semiconductor

Session 6 10 am-12:30 pm Georgian Ballroom B

CCD Imaging

Organizer/Chairman: Dean Collins, Texas Instruments, Central Research Labs, Dallas, Texas

Session reviews current CCD imagers in commercial and low light level military applications.



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Circle 43 for technical information. Circle 115 for technical information and a demonstration. "A Cost-Effective 512 x 320 CCD Image Sensor," Robert L. Rodgers III and E. D. Savoye, RCA

"CCDs in Industrial Camera Applications," Will Steffe, Fairchild Camera & Instrument

"Comparison of Line Scan and Area Images," G. A. Antcliffe, Xerox MEC

"A Comparison of Photon-In vs Intensified CCD Imagers," Dean Collins, Texas Instruments

2-4:30 pm

Tuesday Afternoon

Session 8

Versailles Ballroom

Military and Aerospace Systems

Organizer: Dr Leo Young, Naval Research Lab, Washington, DC Chairman: Robert Hill, Naval Sea Systems Command, Washington, DC

Large electronic systems are entering a new era. NAVSTAR will provide accurate worldwide navigation capability to U.S. and Foreign users. AWACS will provide early warning against lowflying attackers and AECIS is an integrated fleet defense radar system

"NAVSTAR Global Positioning System—User Applications," Edward Martin, Magnavox Research Lab

"AEGIS—The Record," Rear Adm Wayne E. Meyer, Naval Sea Systems Command

"AWACS Radar Concept," Hank Airth, Westinghouse Electric

Session 10 2-4:30 pm Imperial Ballroom A

Home and Hobby Computers

Organizer/Chairman: Frank J. Burge, Regis McKenna Advertising, Palo Alto, Calif

Inevitably the hobby microcomputer will move out of the garage and into the kitchen and other parts of the home. This session attempts to predict the steps it will take in the transition, what home systems to expect, and what new products are on the horizon that will add to its momentum.

"Amateur Computer Clubs-Now and Future," Sol Libes, Amateur Computer Group of New Jersey

"The Need for Personal Computer Hardware/Software Standards," Mike Lipschutz, Byte Inc

"1977—Year of Transition—Hobby to Home Computer," Steve Jobs, Apple Computer

"Control Computers for the Home—How Far Away?" Gordon French, Processor Technology

Session 11 2-4:30 pm Georgian Ballroom A Serviceability and Maintainability in the Design Equation

Organizer/Chairman: Steve Swerling, Tektronix, Beaverton, Ore

Service costs and problems are being recognized as a major cost element in corporate operation, making the traditional approach to product service invalid. Speakers will cover key issues which impact design and maintainability trade-offs, giving specific approaches and examples.

"Designing Microcomputer-Based Systems for Reliability, Serviceability, and Maintainability," Charles A. Christy and Jane G. Morse, Arthur D. Little

"The Impact of a New Tool on Design and Service," Rod Bristol, Tektronix

"The Service Economic Model for Support (SEMS)," Roy Pierce, Xerox OSD

"Signature Analysis as a Field Service Solution," Hans-Jurg Nadig, Hewlett-Packard, Santa Clara

Session 12 2-4:30 pm Imperial Ballroom B

Update on Bubble Memories

Organizer/Chairman: J. E. Geusic, Bell Laboratories, Murray Hill, NJ

Current developments in bubble memories are reviewed and their possible use in telephone, military, and commercial applications are discussed. "The Development of Bubble Memory Devices," A. H. Bobeck, Bell Laboratories

"Survey of Possible Applications of Bubble Memories for Military and Government Sponsored Systems," S. E. Cummings and Mrs A. Buvinger, Wright-Patterson AFB Avionics Laboratory

"Bubble Memories in Telephone System Applications," J. E. Williams, Bell Laboratories

"Bubble Memory System Applications," W. C. Mavity, Rockwell International

"Bubble Memory as Small Mass Storage," J. E. Juliussen, Texas Instruments

Session 13 2-4:30 pm Georgian Ballroom B New CCD Signal Processing Applications

Organizer/Chairman: C. R. Robinson, Bell-Northern Research, Ottawa, Ontario, Canada

The number of applications for charge-coupled devices grows as more design engineers become familiar with the physics of the device. This session presents recent work utilizing CCDs in ultrasonic lenses, signal averaging systems, and data processing applications.

"Performance of CCD Transversal Filters in Digitone Receiver Applications," A. Ibrahim, L. Sellars, D. Rittenhouse, D. Ramsaran, Bell-Northern Research, Ottawa, Canada

"System Applications of Ultrasonic Lenses," R. D. Melen, J. D. Shott, J. D. Meindl, Stanford Electronics Lab, Stanford University

"A Charge-Coupled Device Used in a Signal Averaging Mode," R. D. Baertsch, W. E. Engeler, J. J. Tiemen, H. S. Goldberg, General Electric Corporate R&D Center

"CCD Real-Time Multispectral Feature Classification," H. F. Benz, C. Husson, NASA Langley Research Center

"Integrated Charge-Coupled Split Electrode Transversal Filter," P. I. Siciu, C. H. Sequin, M. S. Tomsett, P. M. Ryan, E. J. Zimany, Bell Laboratories

Wednesday Morning

Session 15 10 am-12:30 pm Royal Ballroom A

Advances in Digital Communications Methods

Organizer/Chairman: Richard C. Levine, Information Engineering Inc, Plainfield, NJ

Recent advances in IC technology make digital transmission from end-to-end of the network economically feasible. An overview of digital techniques, which discusses relevant aspects of telephone and data switching, is provided in this session, along with discussion of practical techniques for digitizing speech, and details of the engineering design of a highly sophisticated alldigital exchange.

"Digital Switching in the Local Network," Donald W. Glover, Bell Canada, Toronto, Ontario

"Total Network Switching by Digital Technique," Ed Jungerman, Danray

"Trends in Digital Coding of Speech Signals," David J. Goodman, Acoustics Research, Bell Laboratories

Session 16 10 am-12:30 pm Imperial Ballroom B Software Strategies for

Successful Microcomputer Programming

Organizer/Chairman: L. A. Solomon, RCA Solid-State Div, Somerville, NJ

The spectrum of microprocessor design tool alternatives available to the application software designer makes choice of a particular tool into a cost- and performance-based decision. Alternatives and their impact upon the application development are covered.

"The Role of Timesharing in Microprocessor Support," Roger E. Brady, National CSS

"Microprocessor Selection, Development, and Programming for a New Concept in Surveying Instrumentation—A Case History," Gary C. Rowe, Keuffel and Essen


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"An Integrated Approach to Microcomputer Support Tools," Ivan Cermack, Bell Laboratories

"Trends in Microprocessor Software," Edward O'Neil, Intel

Session 17 10 am-12:30 pm Imperial Ballroom A Designing With the New Single-Chip Microcomputers

Organizer/Chairman: Alan J. Weissberger, Signetics, Sunnyvale, Calif

Advances in semiconductor device technology have enabled the integration of CPU, ROM, RAM, clock, and I/O on a single IC. These devices promise to extend the pervasiveness of LSI micro-processors into the cost-sensitive controller and consumer markets, for use as standalone controllers or with other processors in a distributed system configuration. Application examples illustrate characteristics of 1-chip micros and compatible ROM/RAM and I/O chips.

"An Intelligent Peripheral Controller," Don Phillips, Intel

"F8 Micro-Machines," Van Lewing, Fairchild Micro Systems

"Applications of Dedicated Microcontrollers," Jerry Larkin, National Semiconductor

"A Versatile Single-Chip Microcomputer," Alex Goldberger, Signetics

"TMS 99-40 Single-Chip Microcomputers," John Bryant, Texas Instruments

Session 18 10 am-12:30 pm Georgian Ballroom A Predicting Test Effectiveness On Assembled PCBs

Organizer/Chairman: Raymond P. Oberly, IBM, Kingston, NY

Predicting and measuring the effectiveness of testing assembled PC boards is important to both designers and board and system manufacturers. This session emphasizes the users' experiences with the prediction and/or measurement of testing effectiveness using various testing approaches.

"In-Circuit Component Test," David Fucci and H. Whittemore, Data General

"Printed Circuit Board Testing," William Wolfson, Hamilton Standard Electronic Systems

"More Board Test Coverage, Please!" Joseph Strenk and Raymond P. Oberly, IBM

"The Life Cycle of Electronic Circuit Boards," Kilian To, Western Electric Engineering Research Center

Session 19 10 am-12:30 pm Georgian Ballroom B CCD Memories: The "Takeoff" Year

Organizer/Chairman: R. A. Minet, RCA, Lancaster, Pa

1977 is shaping up as the year when CCD digital memories will become truly cost-effective. Current status and coming major technical and commercial impact will be examined from both the device and systems standpoints.

"A Cost-Effective 64k CCD Memory," J. Brock Barton, A. F. Tasch, Turner E. Hasty, Texas Instruments Semiconductor R & D Lab

"CCD Memories-1977 and Future Projections," David L. House, Intel

"CCD Memory Applications and Their Impact on Computer Systems," Arthur V. Pohm, Iowa State University

Session 20 10 am-12:30 pm Royal Ballroom B Update on Computer-Aided Circuit Design

and Analysis

Organizer: Dr G. W. Zobrist, University of Toledo, Ohio

Chairman: J. C. Bowers, University of Southern Florida, Tampa, Fla

This state-of-the-art discussion presents the viewpoints of industrial user, program developer, theoretician, and educator, and develops the topics of present status and future directions; innovations; small dedicated programs vs larger general programs; modeling; buy, rent, or lease decisions; and program availability. "A Theoretician's Point-of-View," Frank Branin, IBM

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CIRCLE 46 ON INQUIRY CARD

"A Developer's Point-of-View," Sergio Bernstein, Berne Electronics

"A User's Point-of-View," John Trudel, Tektronix

"An Educator's Point-of-View," John Staudhammer, U.S. Army Computer Systems Command

Wednesday Afternoon

Session 24 2-4:30 pm Imperial Ballroom A

High Level Languages: Microprocessor Spoken Here

Organizer/Chairman: Ivan Cermak, Bell Laboratories, Holmdel, NJ

Sampling the spectrum of high level languages in use or under development today, this session reports on studies that show that programmer productivity is constant with respect to the number of lines of code produced, regardless of language; thus, productivity is higher with a language that accomplishes more in each program statement.

"TIML—High Level Language and Control Applications," Edward Hassler, Texas Instruments

"Using the C Language for Microprocessors," Helen D. Rozegno, Bell Laboratories

"Using APL for Programming Microcomputers," William Marr, IBM

"Domain-Specific Languages for Microprocessor-Based Systems, Stephen Ward, Massachusetts Institute of Technology

Session 25 2-4:30 pm Georgian Ballroom A Testing Microprocessors on Boards

Organizer/Chairman: Donald P. Allen, Fluke Trendar, Mountain View, Calif

With the increasing use of microprocessors, electronics manufacturers are finding that testing MPU board assemblies repre-

sents a quantum jump beyond present test methods. An accepted testing philosophy and equipment that reflects it have not yet emerged. This session attempts to define what progress is being made toward a clearly accepted testing philosophy and the equipment to carry it out.

"Microprocessor Testing—A Manufacturer's Overview," Mitchell Gooze, Motorola Semiconductor

"Adapting PCB Testing to the World of Microprocessors," Lew Olender, NCR

"New Tester Criteria for Handling MPU Boards," Noel Lyons, Fluke Trendar

"Hardware and Software Considerations for MPU Board Testing," John Turino, Instrumentation Engineering

"Problems Associated with User Testing of Microprocessors," W. Luciw, Sperry Univac

Session 27 2-4:30 pm Royal Ballroom B

What's New In Design Automation

Organizer/Chairman: Dr Harry Taxin, Hughes Aircraft Co, Los Angeles, Calif

Now an integral part of the design-to manufacturing process within the electronics industry, computer-aided design systems will be described by users who will focus on specific features which impact design and manufacturing costs and procedures. Panelists include Jon S. Squire, Westinghouse Defense and Electronic Systems Center, John L. Cairns, TRW; Edward Vrablik, Digital Equipment; and Larry O'Neill, Bell Laboratories

Thursday Morning

Session 29 10 am-12:30 pm Imperial Ballroom B Progress Report in Fiber Optic Transmission

Organizer/Chairman: Tingye Li, Bell Laboratories, Holmdel, NJ



Cold switching technology enables all the functions of a dual timebase oscilloscope, plus all the associated controls, to be included in a portable instrument that is designed for the user. Four channel display, plus A \pm B and C \pm D, with all the triggering facilities needed to display just what you're looking for in data measurements.

A full 8×10 cm, 10kV CRT brightly displays the most difficult data streams. And, the total 29 watt power consumption allows for long operating time from an optional battery pack.

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Developments in the field of optical fiber transmission have pushed the technology from research to field experiments. Four papers report on experimental fiber systems that have been implemented and evaluated under field environments.

"Lightwave Communications-Progress and Potential for Telephone Plant," Joe H. Mullins, Bell Laboratories

"An Experimental 100M-Bit/s Optical Guided Wave Communication System," S. M. Stone and G. J. Meslener, GTE Laboratories

"Naval Aircraft Fiber Optics Communication System," G. Holma, and T. Meador, Naval Electronics Laboratory Center

"Connectorized Optical Cables," M. I. Schwartz, Bell Laboratories

Session 31 2-4:30 pm Imperial Ballroom A Microprocessor Emulation: Software and Hardware Choices

Organizer/Chairman: Dave Bursky, *Electronic Design* magazine, Rochelle Park, NJ

When designing a microprocessor-based system, the designer who finds that the chosen processor cannot fill all his requirements can take another route. One alternative is to copy the processor's performance in bit-slice elements by microprogramming the same instructions. In-circuit microprocessor replacements such as emulation boxes permit examination of all internal registers to detect programming or hardware bugs. An alternative is to use a large computer which can completely simulate processor operation, making every software instruction available for examination. These approaches are among those covered by the papers presented.

"In-Circuit Emulation Using the Target Microprocessor," Stephen Dum, Tektronix

"Using M6800 Instructions on the 10800 Bit Slices," Tom Balph, Motorola Integrated Circuits

"Using the 3000 Series of Bit Slices to Emulate an 8080," Stephen Lau, Signetics

"Using Software to Emulate Microprocessors," Michael Rooney, The Boston Systems Office

Session 32 10 am-12:30 pm Royal Ballroom B Testing Complex Digital Assemblies

Organizer/Chairman: James Skilling, GenRad Inc, Concord, Mass

Challenging issues of complex digital assembly testing discussed during this session will focus on changes in technique and scope mandated by the introduction of large scale integrated circuits with their extreme functional density.

"Testing Circuit Packs," John Grason, Bell Laboratories

"Flexibility For Testing Boards Containing LSI," S. R. Purks, GenRad

"Impact of LSI On Complex Digital Circuit Board Testing," E. I. Muehldorf, IBM SPD

(Title to be announced) Larry Meyers, Texas Instruments

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Session 34 10 am-12:30 pm Versailles Ballroom The Future of Computer-Based Instruction

Organizer/Chairman: Charlé R. Rupp, General Electric Electronic Systems Div, Pittsfield, Mass

Introduction," Charlé R. Rupp, General Electric

"Instructional Science and the Evolution of Computer-Assisted Instructional Systems," G. W. Faust and A. F. O'Neal, Courseware

"A CBI System for Skill Training," P. L. Williams and C. R. Rupp, General Electric

"Optional Configurations for Everyman's Automatic Portable Tutor," D. M. Towne and J. W. Rigney, University of Southern California Behavioral Technology Labs

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Thursday Afternoon

Session 37 2-4:30 pm Georgian Ballroom A

A-D and D-A Converter Applications

Organizer/Chairman: Michael T. Timko, Analog Devices, Wilmington, Mass

While not as ubiquitous as operational amplifiers, converters are rapidly becoming popular building blocks in communications, industrial, computer, medical, and other applications. Speakers describe several applications and the components that have made them possible.

"Applications of High-Precision Signal A-D and D-A Converters," Bernie Gordon, Analogic

"Applications for a New Class of Nonlinear Conversion Circuits," D. J. Dooley, Pacific Monolithics

"Performance Applications of New Monolithic D-A," Peter Holloway, Analog Devices

"Application of A-D and D-A Converters in Automatic Testing," K. George Balekvjian, GenRad

"Applications for Very-High-Speed A-Ds," Phil Crosby, Tektronix

Session 38 2-4:30 pm Imperial Ballroom B Applications of Bit-Sliced Microprocessors

Organizer/Chairman: Dr Peter Jessel, Massachusetts Institute of Technology, Cambridge, Mass

Bipolar bit-sliced microprocessors are finding increasing use in applications where speed requirements exclude traditional microprocessors. Typical applications include high speed data collection, interface design, and special-purpose processors. Papers presented at this session attempt to describe available bipolar devices and illustrate the potential and problems associated with their use through several applications.

"Bipolar Microprocessors: Present Chips and Future Trends," Peter Jessel, Massachusetts Institute of Technology

"Design of a High Speed Logic Analyzer," Bernard Robinson, Western Electric Engineering Research Center

"Design of a High Speed Disc Controller," Harold Cohen, GTE Sylvania

"A Special-Purpose Processor for Speech Analysis," Dr John Allen, Massachusetts Institute of Technology

Session 39 2-4:30 pm Royal Ballroom A

The New ATLAS Standard Test Language

Organizer/Chairman: Chuck Evans, GenRad Inc, Concord, Mass

Reviewing the problems of language standardization from the user's and the supplier's viewpoints, this session will present an overview of ATLAS, and attempt to define its relation to languages in use in ATE and the impact that standardization will have.

"The Evolution, Definition, and Status of IEEE Standard 416-1976," Ivan G. Easton, IEEE

"User Looks at ATLAS," Robert Kurkjian, Hughes Aircraft

"A Commercial ATLAS Compiler," Herbert Pardula, Hewlett-Packard Automatic Measurement

"How ATLAS Solves Support Problems," Squadron Leader, David P. Fuller, RAF, London, England

Session 42 2-4:30 pm Georgian Ballroom B The Engineer Over 40

Organizer/Chairman: Dr Harold S. Goldberg, Data Precision Corp, Wakefield, Mass

Problems that have been encountered in the electrical engineering profession have been widely documented. This panel looks at the positive aspects, and will attempt first-pass details of what the engineer can do to build a career that will last a lifetime. To do this will require new thinking on the part of engineers, technical education systems, and industry and professional societies. Panel members are Dr James Mulligan, Dean, University of California School of Engineering; Irving Schwartz, Bernard Haldane Associates; and Dr James J. Rago, Jr, Cleveland State University, School of Business Administration



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CIRCLE 52 ON INQUIRY CARD



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The architecture of the terminal

embodies a micro-processor driven by micro-programs contained in read-only memories. A serial interface connecting the detached keyboard to the CRT display eliminates restrictions imposed by parallel interfaces used in other models.

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You can extend the C-9's capability even further with options like enhanced graphic hardware package with rotations, reflections, and line-texturing features or programmable gray levels for graphics (16 levels) and digital raster continuous tone images (256 levels). We also offer parallel interfaces for a variety of minicomputers and interfaces to popular digitizers for local data input and control of the interactive CRT cursor.

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Smoother curves and lower costs The patented Conographic[™] generator, using conic curves to plot curvilinear information, produces smoother curves from much less data, thus requiring less computer memory, simpler software, less computer or telecommunications time. Result: The lowest total cost of ownership of any graphic terminal available today.

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A better way to collect production-related data using a microprocessor controlled terminal may be the key which is being sought to manufacturing, thereby permitting low cost, adaptable system designs

Designing a Microprocessor-Based Terminal for Factory Data Collection

William S. Holderby

Modular Computer Systems Incorporated Fort Lauderdale, Florida

Profound changes in the distribution of intelligence in system design have resulted from the advent of microprocessors. In particular, a microprocessor-based factory data collection terminal can distribute a small part of the intelligence of the central system, which interconnects all portions of the factory data collection system (Fig 1). With today's technology, microprocessor control represents the "better way" that everybody is always looking for. It permits modifications to the basic terminal to be made in software, rather than hardware; it can check incoming data for accuracy; it can be more readily designed with human engineering factors taken into account. Among the last are visual prompters, such as field specification, detection of incorrect characters, and editing functions, all utilized to reduce human error. These are all expensive in hardware, but of minimal cost when relegated to software.

An unusually high level of intelligence is appropriate in remote factory data collection terminals (FDCTs), because their operators are factory personnel, not skilled in electronic data processing arts. Therefore, tedious and dilatory chores of presenting, retrieving, and checking bidirectional information from FDCTs is overhead, either included in the software which controls the entire system or delegated to smart terminals at the user's location. Factory automation concepts currently revolve around a central macrocomputer or computers. In a multifactory environment, an automation system employs miniprocessor concentrators with direct interfaces to data collection terminals. The FDCTs form a satellite system to the miniconcentrators, which prepare incoming data in a preselected format, to transmit to the macro system. Error checking, logging, and data base updating are confined to the macro system. Therefore, to the FDCT network, the concentrators are transparent. Only rarely do the concentrators, under failsafe conditions, store incoming information when, and as long as, the central system is under repair.

At any given time, the macro system contains the location and quantities of men and materials within the factory. Management uses this information to schedule and direct factory output; factory workers use the automating system to obtain parts, locate major items within the factory, and obtain vendor delivery dates, without excessive paperwork. A single 80-column card tracks a part from the receiving docks to the shipping docks.

The FDCT is the focal point of this system. It must be virtually all things to all people within the factory environment. It can be approximately so if it has been designed with a high degree of functional versatility.



Fig 1 Inter-factory processing system. Macro system contains controlling data base for entire factory data collection system, and is repository for all information gathered throughout network. Concentrators gather local information from satellite FDCTs, as does mini, which also backs up macro when system malfunctions. FDCTs, at local work stations, directly link factory worker to central processing system



Fig 2 Basic terminal functions. FDCT must provide five services to user: display incoming data to operator, accept input data to central system, identify operator or item, make hardcopy record of transactions, and select type of transaction to be made

What is a Factory Data Collection Terminal?

The factory data collection terminal, which is at the critical point of the man-machine interface, requires facilities for five functions: manual data entry, fixed data entry (as from a badge or card), data display, hardcopy printing, and functional selection (Fig 2). A keyboard for manual data entry allows operator input of alphanumeric data, such as part numbers and identity labels; a badge/card reader enables the operator to identify himself and/or parts he is using or working on; an alphanumeric display gives the operator machine instructions and lets him correct errors in data entered; a line printer makes hardcopy records of transactions taking place at the terminal; and with the function selector, the operator tells the supervisory computer that he requires a predefined terminal function.

At least some of these five facilities are found in virtually all data collection terminals. Various differences in design arise from requirements of specific applications. The fundamental task in designing the FDCT lies in the interface between the necessary facilities and the central system, rather than in determining what the machine must do.

Three alternatives are definable at this stage. The first is to connect a video display terminal directly to a standalone badge/card reader and standalone line printer. This is straightforward, but it is also expensive, and so powerful that factory personnel would derive little or no benefit from its capabilities.

Second alternative is to design one model of an FDCT, incorporating all five necessary facilities, and implementing it with conventional hardware. Such a terminal would require a redesign for any and all changes in requirements of use, and would force a potential customer either to absorb a large nonrecurring cost, or to buy the standard FDCT whether or not he required more or less capability. Five years ago this would have been the only feasible alternative.

Third alternative, which is the basis for this article, is to distribute a small part of the central system's intelligence by designing a microprocessor-based FDCT. In addition to permitting low cost special designs, the microprocessor-based FDCT may contain as little or as much power as the application requires.

Many of the fundamental problems in man-machine interfaces stem from man's imperfections. These imperfections manifest themselves as frequent erroneous information entered through such terminals. If the central system checks incoming data, the task is software overhead, but if a small part of the system's intelligence is distributed to the terminals, much of that overhead is reduced.

Which Microprocessor?

First lesson to be learned in dealing with microprocessors is: there are no absolutes. That is, no micro is absolutely perfect, in all respects, for every application. However, every manufacturer believes that his product is superior in all respects to the rest. The decision as to which manufacturer provides a superior product for a specific application must be individually made.

In the case of the FDCT, the requirements are a byte-oriented microprocessor with 4k to 10k bytes of semiconductor memory, consisting of both read-write and read-only forms. Speed is not critical because data input is relatively slow; the pace is set by the serial link to the master computer. This runs at 9600 baud, corresponding to a character in either direction approximately every millisecond. Speed of metal-oxide semiconductor (MOS) technology is adequate.

Power dissipation, although always a design factor, is not of prime importance here. An n-channel MOS microprocessor may be used without generating enough heat to necessitate a fan.

To permit both parallel and serial interfacing to the peripherals, the microprocessor should have a family of interfacing chips, thus reducing the amount of interface design. Family compatibility also reduces timing constraints and buffering requirements, and permits additional chip selection without the expense of discrete decoders.

A powerful instruction set reduces the recurring cost of read-only memory (ROM). A continuing savings may be obtained with a microprocessor that has a specialized instruction set oriented toward the application. In the FDCT, interrupt processing must be rapid; instructions that facilitate interrupt handling and buffer manipulation are desirable. Selection of a particular microprocessor will be based on application-dictated requirements, component cost, and number of sources.

The selection for the FDCT in this article is the Motorola 6800, also made by American Microsystems Inc and by Hitachi. This microprocessor is a 40-pin n-MOS device with an instruction set of 72 variablelength directives. It is byte-oriented with an 8-bit data bus, 16-bit address bus, and up to 65k bytes of memory with a 2- μ s cycle time. It is part of a family that includes a 6820 peripheral interface adapter (PIA), which is a 40-pin n-MOS chip that connects the 6800 with two byte-oriented parallel devices. The PIA can interrupt the 6800 and provides the necessary sequence of handshake signals for input and output operations. Also included in the family is a 6850 asynchronous communications interface adapter (ACIA), which connects the 6800 family to serial communication devices. This chip includes circuits for parity check and for detecting data and framing errors, overruns, and false starts. In addition, it connects the family to external modems or to integrated modems such as the 6860 digital modem. This chip gives the 6800 microsystem the capability of transmitting over voice-grade serial communication links at any rate from 0 to 600 bits/s. In addition, the family contains a 6810 random-access memory, which is a static 128 by 8 device; a 6830 ROM, which is an n-channel MOS mask-programmed chip for nonvolatile firmware storage; and a 6870 microprocessor clock, which generates all the necessary microprocessor and bus clocking pulses to effect stable system timing.

Matching Functions to Circuits

These integrated circuits (ICs) have the necessary parallel and serial interfacing capabilities required by an FDCT (Fig 3). These include:

Serial interface, which links the FDCT and the central factory system at baud rates of 9600 or more, and which checks data and informs the controller of any error detected during either transmission or reception. *Keyboard interface*, which transfers eight bits in parallel and requires handshaking logic to coordinate unidirectional transfer of data between the 6800 and the FDCT keyboard. The "A" side of the PIA (6820) No 1 provides the necessary data bus and control signals. The "A" side of the 6820 is designed for a read operation. This is augmented in the control signals accompanying the eight data bits.

Alphanumeric display interface is similar to that of the keyboard, but it transfers data outward instead of inward. Its destination is either an optional 32character memory, contained on a control board mounted behind the character generator board, or the character generator itself. The latter translates character codes received from the central processor into 5-by-7 dot matrices, and drives a gas discharge display on which these matrices appear.

Data and control signals for both the keyboard and alphanumeric display are generated and processed by a single IC, the PIA, which is divided into two parts. While either part can be used for reading or writing, in practice one part is used for reading and the other for writing; the distinction is established by control signals that accompany the command from the CPU. To use one part in both directions requires extra firmware overhead.

Badge- and card-reader interface, like the keyboard interface, transmits data to the microprocessor, and therefore responds to a read instruction. Since the reader is a parallel device, one side of a second PIA chip can implement the interface. The reader is capable of reading both 22-column badges and the first 22 columns of an 80-column standard punched card. Both carry data in 12-bit Hollerith format; when read eight bits at a time, the card image is stored in the FDCT and transmitted to the central system, which converts the image to its own code.

Functional switches transmit eight data bits in a 2out-of-8 code, which, arranged in an X-Y matrix, determines which of 16 switches is selected. Function selection notifies the central system of the task a particular FDCT is to perform. On this basis, the central system prepares the tables and software required by terminal and data base for that task. However, the particular 16 functions of a terminal are not a tight constraint on performance, because the terminal is microprocessor controlled and its functions are defined in software. The interface is implemented by the other side of the second PIA.

The line printer associated with the FDCT may be required to accept more than one paper form, and can be either built into the terminal or in a separate enclosure linked by a serial interface—a second 6850 ACIA, for example. The latter is preferable, because line printers are notorious noise generators and take up a lot of space.

The FDCT incorporates two separate buses: "A" for the read-write and read-only memory, and "B" for the necessary address, data, and control lines to the various PIAs and ACIAs. This dual bus arrangement allows a basic terminal to be expanded with additional memory and peripherals, if and when the FDCT must take on extra tasks.

How Big a Memory?

The designer's next step is to determine the quantity and type of memory. The size of the read-write memory is reasonably easy to determine. It need be only as large as the summation of the worst-case storage buffers for each of the peripherals and the worst-case limit of the software stack; 1k byte is adequate.

ROM size is more difficult to establish. It stores the firmware control program, so its size cannot be accurately determined until the control program has been written. However, at this point the designer should have enough confidence in the system's architecture to make a flowchart of the main portions of the firmware.

In doing so, he makes a principal decision: hardware versus software tradeoffs in each interface. One of the basic reasons for using a microprocessor is to replace former hardware functions with software. This replacement is based on a solid economic foundation as well as a versatile design concept. The major cost of software lies in the non-recurring costs of initial development, but it also has a recurring cost—the price of the ROMs to store it. This is usually much smaller than the recurring cost of a hardware-imple-



mented function. However, hardware is usually faster. The tradeoff is in determining which approach is best, considering both cost and capabilities. Memory sizing time is the best possible point in the design cycle at which to determine these tradeoffs.

Another important decision is in choosing the type of ROM. The choice is among three types—masked, programmable, and erasable ROMs—any of which is usable with the 6800 microsystem.

Masked ROM is programmed during manufacture, using a program furnished by the terminal designer and a mask designed and built by the manufacturer in accordance with the program. This mask controls a deposition stage in manufacture, and adds a masking charge to the purchaser's cost. The charge, spread over the entire quantity of ROMs purchased, becomes negligible for a large quantity of ROMs; but for applications where large quantities with the same firmware are not feasible, the masking charge becomes predominant. This is a basic disadvantage, particularly since changes in firmware require additional masking charges.

Programmable ROM (p/ROM) lets the user do his own programming. However, programs, once installed, cannot be changed; if changes are necessary, the programmed devices must be scrapped and new chips substituted in their place. This is the p/ROM's main disadvantage. Secondary disadvantages are the larger power dissipation and smaller available storage sizes; however, these are usually more than offset by the low cost and high speeds made possible by bipolar technology.

Erasable p/ROMs (EPROMs) cannot only be programmed by the user, using conventional equipment, but can also be erased and reprogrammed. Thus the designer enjoys a cost saving on firmware updating and error correction by using the same hardware over and over again. The EPROM is the most versatile of the three choices, but is also the most expensive—as much as three times the cost of p/ROMs. The decision to use it must anticipate a great deal of reprogramming to offset the extra initial cost. The FDCT firmware memory is composed of bipolar ROMs because they were the most cost-effective.

How to Get At the Memory

Memory addressing is the next order of priority. In the 6800, all elements, whether peripherals or memory, are treated as memory; all peripheral addresses are incorporated in its 65k-byte range of addressing—0 to 65k bytes (Fig 4). Specifically, all peripheral addresses are located between 8000 and 9000 hexadecimal. This address space allows the number and complexity of the peripherals to be expanded if needed.

Read/write memory is addressed between 0000-037F hexadecimal, wherein information is buffered enroute to or from the peripheral network. An additional 128 bytes of read/write memory between A000 and A07F make up the microprocessing unit's last in first out software stack in its worst-case extension. This stack is usable by both the programmer and the microprocessor for temporary storage and in responding to interrupts.



Fig 4 Memory map. FDCT's memory has six segments, as shown. Software stack temporarily stores program information when MPU must interrupt normal program sequence. Controlling program, or microprogram, contains detailed instructions for internal operation. Minibug II is fast diagnostic program in ROM. Interrupt vectors direct MPU when requested to service peripheral or perform some other infrequent task

FDCT ROM, containing the firmware, is addressed between B000 and BFD0. This memory addressing arrangement is not inconsistent with the dual bus structure mentioned previously, although at first glance it may seem to be so. On the contrary, the dual buses merely offer a convenient means of physically connecting the peripherals and memory modules; all addresses generated by the microprocessor go out on both buses, but only the addressed unit responds, whichever bus it is on.

Firmware

Firmware within the FDCT controls the terminal by performing two basic functions (Fig 5). When power is turned on, a vectored interrupt starts a sequence of instructions that insure that the peripheral network is in the proper state for terminal operation. To do this, the sequence initializes each PIA by setting the 16 data lines to either read or write status. Each ACIA is master reset individually so that erroneous line transitions are not transmitted to either the concentrator or the line printer over the serial links. Finally, the terminal reports its status to the concentrator, which logs the terminal online and functioning.

The firmware's other major function is to provide an interface between the operator and the central system, which requires the terminal to operate in various modes in reporting diverse transactions. Function selection by the operator defines the terminal mode. One of 16 modes is selected by depressing a suitable function switch; the FDCT transmits the selection to the concentrator. In reply, the concentrator returns video prompting and formatting information to insure correct input from the operator. This information is stored by the FDCT. It checks incoming data from the operator against the stored format for length, numeric limits, and line placement; displays it to the operator on the alphanumeric display for visual feedback and correction if necessary; prepares a hard copy, if required; and transmits the complete repertoire of gathered information to the concentrator. It then returns to a standby mode awaiting a new operation. If the concentrator detects a transmission error, the FDCT still contains the information and can retransmit any or all of it.

Dynamic redirection of the FDCT's sequence of operations allows the terminal to operate in any number of modes. Thus the terminal may be placed anywhere in the factory to perform different functions without changing either the terminal hardware or firmware. The central system's software determines the specific functions and sequences for each terminal. Because the system has distributed intelligence, any operation requires only two block transmissions—one from the concentrator to the terminal to set up the FDCT to work with the operator in the appropriate mode, and one from the FDCT to the concentrator transmitting the data gathered in the proper format and sequence.

If the level of terminal intelligence were reduced, transmissions between terminal and concentrator would increase. In the extreme case, each individual keystroke would be reported when it occurred. This would require the concentrator to receive, check, and store each portion of each transaction from each terminal asynchronously, at a cost in software overhead far in excess of that required by the block transmission scheme. In addition, if 60 to 100 terminals were transmitting randomly, there would be frequent interference and loss of data. A high level of terminal intelligence makes the block transmission scheme practical; it requires only one asynchronous transmission of one 8-bit mode character to initiate the sequence. Once the FDCT has transmitted the mode character, it accepts no further inputs from the operator before receiving the first block transmission or before a 2-minute timeout has expired. The timeout indicates a link failure between terminal and concentrator, and allows concentrator software to respond to the terminal even during periods of intense link activity.

The 6800 has 72 instructions, five addressing modes, two levels of interrupt, and an automatic stack. The power of the instruction set and the interrupt capability enable the programmer to establish certain peripherals as interrupters. These will be serviced only by interrupt routines.

Of the two interrupts, one is maskable and one is nonmaskable. For example, the line printer adapter is attached to the maskable interrupt line, so that the programmer can mask this interrupt during critical





activities. On the other hand, the serial link adapter is attached to the nonmaskable interrupt line, so that its interrupt will be serviced immediately. Thus the serial link maintains the highest priority. The keyboard, alphanumeric display, card reader, and function selector do not interrupt the microprocessor; instead, they are serviced in the test and transfer mode—that is, the respective PIAs are interrogated for a data ready signal caused by an incoming peripheral interface signal transition. If the signal is present, the peripheral is serviced and the signal reset.

Hardware-Software Integration

Integrating the software and hardware is the principal problem of designing with microprocessors. It is usually



Fig 6 Hardware-software design paths. Two paths converge where hardware and software combine for final checkout, when terminal first functions as unit and responds to operator commands. At end of this phase, hardware ROMs are programmed by melting away appropriate fusible elements

encountered when the designer has established the microsystem's architecture, and the firmware programmer has made flowcharts of his routines and designed a trial coded program to run in the terminal's environment. Now three utility programs are required to pass this point: an editor, assembler, and debugger.

The editor allows the user to write his code in an understandable format, to modify the code at any time in the process, and to store the code for input to the assembler. In turn, the assembler converts the output from the editor to machine language instructions. It generates two outputs: an object module and an assembly listing. The object module is the machine language instructions to be loaded into the terminal for checkout. The assembly listing tells the programmer what this object module contains, in both the programmer's code and the assembled machine instructions, and serves as a troubleshooting aid to the programmer.

Last of the three, the debugger is a software aid that loads a program into the terminal, steps through it to assure that it works, and verifies the correct transfer of data among memory, registers, stacks, and accumulators. Of the three utilities, the debugger is the most critical, because it directly aids the programmer in the most time-consuming phase of his task—that of checking out the code (Fig 6). The hardware at this time has undergone only preliminary testing; therefore, the designer has to determine whether the problems that he finds arise from software or hardware. Well-designed debugging software helps this determination.

The FDCT contains its own debug program, the Motorola Minibug II. This program is mask-programmed on a ROM card. When the Minibug is required, the card is simply plugged into a spare socket; it carries the necessary address and data bus interface circuits along with the ROM chips. When both the debug and main ROM card with the corresponding addresses are plugged in, mechanical switches on both cards are set to give the debug program control over the interrupts and terminal program and to remove control from the main ROM. The Minibug II lets the programmer connect an I/O device such as a terminal through the ACIA serial link. The debugger's stack is the same one used by the main terminal's program; the debugger also defines a software stack and an I/O port at specific addresses.

To include this capability in a design requires a modest effort, which rewards the designer with greatly decreased program development time. The debugger is also a practical aid in diagnosing hardware failures after program development has been completed.

Exact form of the editor and assembler depends on the terminal development system, which gives the hardware and firmware designers the ability to test and modify their designs rapidly and efficiently (Fig 7). Its principal requirement is the capability to modify, reassemble, and reload the terminal's software as rapidly as possible.

The FDCT development system is based on a minicomputer containing a ROM simulator, into which the mini loads the terminal's development firmware. Also, the mini controls a serial communications link through which it collects data sent from the terminal. A logic analyzer attached to the terminal's micro-system bus determines what addresses and data are present at any time, allowing the programmer to analyze "runaways" in his program.

In addition to specialized hardware, the mini also has a console device, with which the programmer controls the mini's operating system containing the editor and assembler.

To write programs coded in 6800 assembly language, the programmer commands the operating system to produce the editor, usually a basic utility feature of the operating system. He then enters his program using the console. Upon completion of this input, he calls



the assembler, the input of which is the output of the editor. The assembler's output is loaded into the RAM memory, and the program is run in conjunction with the debugger.

At any time during the checkout, usually after having made several changes, the programmer may wish to reassemble his terminal program. To do this he first uses the editor to change his initial assembly code; then he calls the assembler again. Through successive approximation, the entire task is eventually completed.

Many forms of development systems are available either from vendors or by individual design. Their principal goal is always to provide the capability of rapid reassembly and checkout.

Summary

Microprocessors have contributed greatly to the ability of ever smaller machinery to perform ever larger tasks. Design engineer's systems, from calculators to highly intelligent test equipment, now encompass far larger capabilities than could be achieved with random logic. This greatly increased ability to package a programmable computer within a small enclosure has rendered obsolete many of the previous concepts of man-machine interfaces and has led to the appearance of increasing numbers of microprocessor-based terminals.

With the proper control microprocessor, a terminal can provide better factory data collection; small portions of the central system's intelligence can be distributed, providing maximum versatility for users. Resulting low cost system designs are adaptable and allow expansion. Most importantly, this technology permits many functions, traditionally accomplished in hardware, to be relegated to software. The advantages achieved include savings in costs and a reduction in human errors.

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Model 70	PDP-11/45	
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An understanding of the basics of switching power supply operation coupled with an awareness of the essentials of writing a specification for such a device should prevent the engineer from being trapped with an inadequate supply

Switching Power Supplies: Specification Criteria

James H. Burens

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Switching power supplies have found their way into many new applications, and continue to do so at an accelerating rate. Where size, weight, and efficiency are prime requisites, these supplies are rapidly becoming the standard. Unfortunately, certain areas of their specifications have not kept pace with switching technology.

Quite often, a person encounters difficulty when writing specifications for a switching power supply because adequate information is not available to do it properly, or that information is not sufficiently accurate. Some engineers who are knowledgeable in linear power supplies assume that their expertise automatically

Linear	Switching
0.5 W/in ³	2 W/in ³
10 W/Ib	50 W/Ib
30%	80%
1.0 mV	50 mV 10 mV
25 µs	500 μs
2 ms	20 ms
±10%	±20%
0.1%	0.1%
	Linear 0.5 W/in ³ 10 W/lb 30% 1.0 mV 25 μs 2 ms ±10% 0.1%

carries over into the switching supply. In fact, the smaller, more efficient switcher requires a completely different set of specifications (see Table).

Although a number of different switching techniques are employed by manufacturers, the specifications are frequently independent of these differences, even when the circuitry varies considerably. Many key specifications are determined by the passive components which are usually fairly standard regardless of the type of circuitry. Since the power supply manufacturer normally has a limited choice of passive components, the several different types of switching supplies, in some respects, are nearly identical.

What to Look For

A switching power supply transforms line voltage, usually at 60 Hz, to an isolated and regulated dc voltage. Inversion is efficient and the unit is small because it contains a high frequency switching power stage built with one or more semiconductor switches and operated cyclically at cut-off and saturation, which applies high voltage pulses to a transformer. Many units regulate the filtered (averaged) output by varying the duration of the pulse as load and line changes occur.

The power stage commonly takes one of three forms: a full bridge, a half bridge, or a flyback. Coupled with this is a modulation method, of which four forms are widely used: pulse-width modulation, pulse-time modulation, frequency modulation, and pulse-frequency modulation. Modulation is applied to the time relationships—both duration and frequency—of the volt-







(b) Half bridge with pulse-time modulation. Transistors 1 and 2 conduct alternately for fixed time periods. Time between pulses varies to compensate for line and load conditions



(c) Full bridge with frequency modulation. Transistor pair 1 and 4 conduct alternately with pair 2 and 3, applying a square wave to power transformer. Frequency of operation varies in accordance with line and load conditions



(d) Flyback with pulse-frequency modulation. Transistor conducts for variable durations, storing energy in power transformer via primary winding. When transistor turns off, stored energy is delivered to load via secondary winding. Both duration and period of power pulse depend on load and line conditions

Fig 1 Power stage configurations. Power stage of switching power supply, in form of full bridge, half bridge, or flyback, is coupled with pulse-width, pulse-time, frequency, or pulse-frequency modulation applied to time relationships of voltage pulses applied to transformer

age pulses that are applied to the transformer. What power stage configuration and modulation technique are used depends on the manufacturer's technology, output voltage and power required, and input line range (Fig 1).

A switching specification (or any other) could be 40 to 400 pages long and still not guarantee reliable performance. For example, it cannot assure dependable vendor back-up or suitable factory service if the unit falls short of claims. Since it is not the quantity of specifications that is important, but rather the quality, the following discussion is a "bare-bones" approach to switcher specifications. By being aware of these essentials and by gaining insight into what constitutes meaningful specifications, the engineer will be much less likely to fall prey to copious, but inadequate, specifications.

Transient Response

Behavior of the power supply when its load changes suddenly is determined by the output filter impedance and the supply's feedback response. The key here is not only how long the voltage deviates from its static value, but how far it deviates. For example, during a load application, a supply that deviates 50 mV on a 5-V output for 5 ms might be much more acceptable for a transistor-transistor logic (TTL) system load than one that deviates 750 mV for 0.5 ms. While the latter's duration is considerably shorter, its extreme voltage dip would be harmful to the system.

Transient deviation is determined primarily by passive components, ie, the output filter capacitors. Their equivalent series resistance (ESR) and equivalent series inductance (ESL) can determine the extent of supply output changes during a load application or removal. Voltage deviation can be expressed as change in current times ESR, plus rate of change of current times ESL; or

 $\Delta \mathbf{V} = \Delta \mathbf{I} \times \mathbf{ESR} + \Delta \mathbf{I} / \Delta \mathbf{T} \times \mathbf{ESL}$

However, the deviation is modified by the closed-loop response, which is a function of the output choke size (inductance) and output capacitance as well as pulsewidth variation.

In addition, lead length between the supply and load introduces a resistive and inductive drop, which must be included when determining voltage deviation and load capacity.

Stability is another important criterion; prospective buyers should insist on adequate margin to assure stability. One of the most convenient and best understood representations of stability data is a Bode plot (Fig 2) based on measurements of the unit, not just an analysis of its design. A Bode plot is a graph of loop gain and phase shift versus frequency: The relative values indicate system stability. Often a peak in the gain curve indicates reduced stability margins.

Another helpful plot is a root locus (Fig 3). Drawn in the plane of the Laplace operator $s = \sigma + j\omega$, the plot shows the relative placement of poles and zeros. The location of the poles relative to the σ axis defines an angle which directly reflects system stability. The larger the angle, the lower the stability of the supply. Margin should be allowed to provide for changes in pole location due to supply gain variations.

Input Voltage

Most often specified input voltages are 115, 208, 220, and 230 Vac rms, and 115/230 V dual input. The voltage used by the supply's input circuit is the peak voltage, not the rms voltage. If the peak is clipped, as can happen if the source is ferroresonant or if the power line has a high impedance (as it might in a remote location), the effective input line range is altered and additional input tolerance may be required. In any case, the nominal value should be specified and used elsewhere within the specification as a reference. Tolerance on this nominal voltage is important, whether caused by clipping or otherwise. Many users require continuous operation in the presence of line voltage 20% below normal, which is difficult to achieve in a linear supply because it becomes less efficient and may have to be derated.

Input frequency also should be specified. Although switching power supplies are more tolerant of fre-







Fig 3 Root locus. Location of open loop poles varies with system gain. The larger the angle Θ , the lower the supply stability

General Switching Power Supply Specification Summary

The following four parameters apply to all sections of this specification unless noted otherwise:

Line:	[x]	Vac, [x] Hz (nominal)
Output voltage:	[X]	Vdc (nominal)
Output current:	[x]	Adc (full load)

Temperature: [x] °C (nominal ambient)

[Brackets] enclose items that must be added to complete a specification; {braces} indicate supplementary information that need not be included.

1.0 INPUT

1.1 *Range:* The input voltage shall have a nominal value of [x] Vac rms and [x] V peak-to-peak with a continuously operating range of [10 to -20%] of this value.

1.2 Fusing: An input fuse shall be provided of a capacity adequate to protect the power supply and the input wiring. {Underwriters' Laboratories UL478 does not require the power supply to have fuses (the line must be fused and proper size wiring provided) but a fuse can be more protective to a power supply in case the primary power line has a circuit breaker, which may be slow in reacting to an overload.}

1.3 Current Limiting on Turn-On: Maximum input ac current shall be limited to [an 8-A pk/100-W of output] for two cycles or less for all conditions of paragraphs 1.0, 2.0, 3.0, and 4.0. Interruption of input voltage for a duration sufficient to cause output voltage to drop below regulation setting shall cause reactivation of inrush limiting circuitry.

1.4 Input Common-Mode and Differential Noise (Conducted) and Unit Radiated Noise: {A ruling of the Federal Communications Commission is pending, which will specify limits on electromagnetic interference that will be more than enough for most usages.}

1.5 *Frequency:* The input frequency shall be [60 Hz] nominal with a continuous operating range of [47 to 63 Hz]. All static output specifications shall apply within this range.

2.0 OUTPUT VOLTAGE

2.1 Range: The output voltage shall have a nominal value of [x] Vdc with $[\pm 10\%]$ adjustment range. This paragraph shall be applicable to all conditions of paragraphs 1.1 and 3.1.

2.2 Regulation: The output voltage shall be statically regulated within [\pm 0.2%] for all combinations of conditions specified in paragraphs 1.1, 2.1, and 3.1. Temperature coefficient of output voltage shall be less than or equal to [\pm 0.02%/°C] over the range specified in paragraph 4.1. {The three paragraphs cited together specify input voltage, output voltage, and output current, respectively, thus covering both line and load regulation at once. On the other hand, temperature coefficient is cited separately, because it can be significant when taken into account over the entire temperature range.} 2.3 Differential Ripple and Noise: Ripple and noise at the output shall be equal to or less than [50 mV peak-to-peak] when measured under constant load with an oscilloscope with a bandwidth of 50 MHz or more.

2.4 Common-Mode Noise (Conducted): The common-mode noise shall be less than [200 mV peak-to-peak] when measured across a [5 μ H] choke connected between the chassis and the output with an oscilloscope with a bandwidth of 50 MHz or more, for all conditions specified in paragraphs 1.1, 2.1, 3.1, and 4.1. Common-mode output impedance to chassis shall be through a capacitor of less than 0.01 μ F and shall be at least 159 Ω at 100 kHz.

2.5 Transient Response and Deviation: The output voltage change for an increase or decrease in the load of up to [50%] of rated load at $[5 \text{ A}/\mu\text{s}]$, occurring entirely within the rated load band shall be less than $[\pm 5\%]$. Recovery of

the output to within [\pm 0.1%] of the adjusted nominal voltage shall occur within [0.5 to 1.0 ms]. {"Rated load band" is usually defined as 20 to 100% of rated load, instead of 0 to 100%. At light loads an output choke will not carry continuous current. The size of the choke inductance determines at what load the choke current becomes discontinuous; ie, a small choke allowing fast system response due to its low value of inductance will cease continuous conduction at a higher load current. Once the choke current is discontinuous, the system response to a step load addition will be longer than if the step load addition occurred when choke current was continuous.}

2.6 *Closed-Loop Stability:* The supply vendor shall provide proof of unit closed-loop stability with local sensing by submitting Bode plots and/or root locus analysis.

2.7 *Turn-On Delay:* The output voltage shall reach the setting specified in paragraph 2.1 within [500 ms] after application of nominal input voltage specified in paragraph 1.1 while loaded as specified in paragraph 3.1.

2.8 Overshoot on Turn-On and Turn-Off. Less than [2%] above output voltage setting shall be allowed for application or removal of input voltage for any combination of conditions specified in paragraphs 1.1, 2.1, 3.1, and 4.1.

2.9 *Carryover:* The supply shall maintain output regulation per paragraph 2.2 with loss of input for [20 ms] from nominal line, full load. The measurement shall be made from the point at which conduction of input current would normally begin until output voltage falls below the static regulating band. After loss of input, the supply shall recover to normal operation with the return of the input voltage to the operating range.

2.10 Ac Output Current: If an alternating component is superimposed on the power supply's direct current output by a fluctuating load, its rms value shall not exceed [20%] of full load direct current, and its peak value plus the direct current shall not exceed the full load rating. {This means that if an ac component is present with an rms value approaching the limit of 20% or whatever is specified, the dc components must be substantially less than the other 80% to prevent the sum of the dc component and the peak of the ac component from exceeding the 100% level. Just how much less than 80% can be tolerated depends on the waveshape of the alternating component; the familiar rms/ peak ratio of 0.707 = $\sqrt{2}/2$ applies only to sine waves and certain other shapes. Fluctuating loads are often presented by digital systems, which may contain large numbers of transistors that turn on and off in unison. This condition imposes a ripple on the power supply output, which is independent of the ripple of paragraph 2.3 (in which a constant load is specified). The fluctuating-load ripple must be kept within bounds to avoid overloading the power supply's output capacitor. If the load is known to be virtually constant, this paragraph can be omitted from the specification. 2.11 Remote Output Voltage Sensing {Optional}: Remote sensing shall assure that the adjusted nominal voltage is present at the load and shall compensate for up to [0.5 V] drop in each output lead. The output voltage at the power supply will not be required to exceed that specified in paragraph 2.1, either under normal conditions or in the event that either or both remote sense connections are lost. {Remote sensing can create many problems and is not recommended.

2.12 Output Voltage Margining (Optional): Provisions shall be made for connection of an external potentiometer for voltage margining of up to $[\pm 10\%]$ about the nominal of paragraph 2.1. {Margining is used to test the systems capability of operating at the minimum and maximum adjustment ($\pm 10\%$) of the supply output by the addition of an external potentiometer that can vary the output voltage to these extremes.}

2.13 Output Voltage Inhibit {Optional}: A terminal shall be provided to inhibit the output voltage if a TTL logic [low]

signal is applied. Removal of the signal shall allow output voltage to return to setting with less than [2%] overshoot within the time specified in paragraph 2.7. {This paragraph is required when a system is to contain several power supplies that are to be turned on in a prescribed sequence under automatic control.}

2.14 Output Fail Signal {Optional}: A [low] output signal, TTL compatible, shall indicate imminent power failure a minimum of [2 ms] before the output drops below 90% of setting.

3.0 OUTPUT CURRENT

3.1 Range: The output current shall be variable from 0 to [x] Adc. Full load current shall be [x] A.

3.2 Current Sharing: Paralleling of up to four supply outputs shall be possible with master/slave paralleling such that each output current does not differ from another by more than [$\pm 10\%$] of the average of each output. {Master/slave paralleling implies an active control of each slave such that no supply will become overloaded. Good practice would then dictate a supply rating such that no supply would be required to carry more than full load; ie, the average load is not more than 90% of the unit's full load rating. As an alternative, a wire-OR output could be specified (outputs tied to a common output bus) without master/slave sharing, but additional specifications for stability and over-current would be required.}

4.0 AMBIENT CONDITIONS

4.1 *Temperature:* The power supply shall meet all parameters specified in paragraphs 1.0, 2.0, and 3.0 for operating ambient temperatures of [10 to 40° C] and shall be proportionally derated for higher temperatures to [50%] of full load current at [70°C]. Nonoperating storage temperatures shall be between [-55 to 85° C].

4.2 Altitude and Humidity: {This specification is standard for most electronic devices.}

5.0 SIZE

As required. Presently available convection-cooled supplies are as dense as 1.4 W output/in³; forced air supplies attain 2.0 W/in³ (including connectors) for outputs of greater than 250 W.

6.0 WEIGHT

{As required. Presently available power supplies produce 30 to 60 W/lb.}

7.0 EFFICIENCY

The efficiency (W output \div W input) shall be [60 to 80%] under all conditions specified in paragraphs 1.1 and 2.1 and at the full load setting of paragraph 3.1.

8.0 PROTECTION

8.1 General: The power supply shall be self-protecting under internally and externally caused abnormal conditions, for all operating conditions specified in paragraphs 1.1, 2.1, 3.1, and 4.1, and/or as specified in paragraphs 8.2 to 8.6 inclusive.

8.2 Output Current Limit: The maximum static output current shall be set between [105 to 120%] of full load for all conditions of paragraphs 1.1, 2.1, 3.1, and 4.1. Overload conditions shall cause both the output current and the output voltage to decrease; short-circuit current shall be limited to [25% typical] of full load. Removal of an output overload condition shall permit automatic recovery of output voltage to the previous setting with less than [2%] overshoot. {This behavior of current and voltage under overload is often called "foldback"; it reduces the possibility of damage if, for example, a fault could develop on a branch load, the capacity of which was significantly less than the full-load current rating. If only a current limit was specified, without foldback, then the fault might overstress system wiring and/or printed circuit board traces.}

8.3 Output Overvoltage Protection {Optional}: The power

supply shall shut down if the output voltage exceeds [130 $\pm 5\%$] of the nominal value as specified in paragraph 2.1 for any condition of paragraphs 1.1, 3.1, or 4.1. Interruption of the input shall be required for resumption of operation. {This paragraph does not imply crowbar protection, which is necessary in linear supplies if the pass transistor fails short; switching supplies can be totally self-protecting without it.}

8.4 Overtemperature Protection {Optional}: The power supply shall shut down for ambient temperatures and loads that exceed those specified in paragraph 4.1 and shall automatically resume operation when safe ambient temperature is restored.

8.5 Low Input Voltage Protection {Optional}: The power supply shall be self-protecting for any static or dynamic variation of the input voltage below the ratings specified in paragraph 1.1.

8.6 *High Input Voltage Protection* {Optional}: The power supply, whether operating or not, shall not be damaged by differential input transients of (1) [1 kV with an energy of 2.5 J], or (2) [125% of nominal line voltage for 60 ms]. {These transients are caused, for example, by lightning or the operation of large power equipment on the same bus. Limits imposed by paragraph 1.0 may be relaxed for conditions of this paragraph.}

9.0 UL RECOGNITION

The power supply shall conform to Underwriters' Laboratories Standard No. 478 for component recognition (EDP) [or UL 114 if the power supply will be used in office equipment]. {Allow time for formal recognition to be received from UL—it may take 6 mo.}

10.0 RELIABILITY

All components are to be operated within ratings—that is, semiconductors shall be operated below maximum voltage, current, and junction temperature ratings, and all passive components at less than maximum wattage rating, and where applicable, within maximum hotspot rating. Derating for power components shall be of prime consideration because of their large effect on overall supply reliability.

The vendor shall provide suitable life test data indicating a mean time between failures of [25,000] h.

11.0 MECHANICAL

{Details of mechanical specifications are not included here, beyond the following listing of major sections. If required, details should be the same as those in most electronic procurements.}

11.1 Audible Noise: Operation of the supply shall produce no noise below [20 kHz]. {If a fan is used for cooling, allow for its noise.}

- 11.2 Outline Drawings {I/O connections defined}
- 11.3 Mounting Surfaces/Mounting Pattern
- 11.4 Finishes
- 11.5 Materials
- 11.6 Marking {User's Part Number}
- 12.0 QUALITY CONTROL/QUALITY ASSURANCE
- 12.1 Documentation
- 12.2 Workmanship

12.3 Test Data Recording {Certificates of Compliance}

12.4 Burn-In: A 24-h operating burn-in at [40°C] under full load shall be performed on all power supplies.

12.5 *Maintenance/Repair:* {Factory repair is suggested unless customer technicians are trained and qualified by the vendor.}

- 12.6 User Manuals
- 12.7 Facilities Inspection
- 13.0 WARRANTY

A 1-yr warranty to cover all labor and materials shall be provided.



Fig 4 Carryover measurement. Carryover should be measured from point at which conduction of input current would normally begin after loss of input



Fig 5 Common-mode noise sources. Shunting commonmode noise to chassis will reduce input and output common-mode noise but can lead to other problems

Fig 6 Common ground for loads. If all loads are connected to single ground point, there can be two paths for signal returns. If paths have different impedances, their existence can cause errors in one or more of loads

quency variations than some other types of equipment, restrictions on such variations may be necessary because the power supply derives bias voltages for internal use directly from the line by an ac (60 Hz) transformer that may require narrower frequency control than does the power stage.

LOOP 2

Many applications require the output to be maintained for a specific length of time after the ac input disappears. This is called carryover; it is a sort of poor man's uninterruptible power supply (UPS), insuring that power remains available to the load during a short interruption of the primary—a matter of milliseconds. The extent of carryover that can be incorporated in the design is a function of the input capacitor in the primary circuit, and of the peak current that the high-frequency switching devices can carry. A loss of line voltage occurring after an input current pulse ceases should not be used as a starting point for determining the carryover duration (Fig 4). The supply must be capable of carryover from this time to the next input current pulse under normal operation. The time at which the carryover measurement should begin, and the worst-case time of power loss, is at the point when the missing pulse would normally begin input current conduction.

Switching Noise

Although common-mode noise is often ignored in switching specifications, it is, nevertheless, a problem, especially in large computer systems. This noise, which is common to both input or both output leads, is generated through stray capacitances within the supply and is difficult to eliminate after other design aspects are complete.

Some manufacturers try to eliminate common-mode noise with relatively large capacitors between line and chassis and output and chassis; however, this often makes system grounding more difficult. Suppose that the output of a switching power supply is connected to chassis ground through a capacitor to shunt common-mode noise (Fig 5). Suppose also that all the loads share a common ground connection, established to eliminate or at least to minimize problems associated with "ground-loop" currents (Fig 6). A data line connects two of these loads, A and B, and the return for the data line is necessarily through the common ground line. However, another path is present through the chassis to the power supply and back along the voltage line to the originating circuit. If these paths have different impedances, they can cause errors in power supply load B (here assumed to be also the signal load for A). To avoid such problems, either the common-mode shunt should not be used on the power supply, or it should be made with the smallest possible capacitance.

Differential noise, like transient response, is a function of passive components: the output filter capacitors and filter chokes. The filter choke determines capacitor ripple current which, in turn, determines ripple voltage generated by the capacitor ESR, ESL, and, to a lesser degree, capacitance.

Switching noise should be defined over a wide frequency range, beginning at 47 Hz, which is 20% below nominal in the U.S., and going up to 10 or 50 MHz, depending on system sensitivity. It is reasonable to ask for ripple and noise of less than 50 mV peak-to-peak for any voltage from 2.0 to 60.0 V. While this may seem excessive compared with a linear (non-switching) supply, which generates less than 5 mV ripple and noise, the noise actually is attenuated with distance from the supply and is greatly reduced at the load. Noise spikes usually have a very high peak-to-average ratio, and are of fairly short duration. A fixed frequency of operation helps avoid potential interaction with noise sources in the load.

Reliability

Common sense plays a leading role in assuring that the chosen supply will perform reliably to specification. First and foremost, the manufacturer's field record in switching technology should be closely examined. How many units have actually been sold? Is each one thoroughly tested before shipment? Are all units burned in—that is, operated in a variety of worstcase conditions for some period of time prior to shipment? Where are they being used? What are the users' major complaints? Will the manufacturer supply life test data? Life test data and the answers to these other questions can substitute for calculations of mean time between failures. Many components frequently used in switching supplies do not have the history to make a calculation valid.

Finally, reliability is principally a matter of operating all components within their rating for all supply conditions. This can be difficult for a user to check, but not an unreasonable specification.

Insist on listing by Underwriters' Laboratories. Some vendors proclaim that their products meet U.L. standards, but that formal approval is not worth the time, money, and effort; in effect, they are confessing that certain of their components and dimensions will not make the grade. Although U.L. approval literally certifies only an insurable risk, it is a substantial help in ascertaining that a power supply is in fact reliable, and that its materials function within their ratings.

Specification Format

Unfortunately, there is no established standard or even an accepted universal format for specifications. Most specifications are generated to cover what each individual considers important—this may be nothing more than a copy of someone else's parameters with different values applied. So it is expedient to recognize and understand what constitutes a good specification or a bad one.

The sample specification presented on pages 94 and 95 of this article sets forth the minimum recommendations of what items to include in a specification and in what order. Its internal organization groups similar items; items that are referred to throughout the specification appear as near the beginning as possible. An example is the nominal input line voltage, which is referred to throughout for transient response, carryover, and other parameters. Generally, we have tried to avoid ambiguity. [Brackets] enclose items that must be added to complete a specification; {braces} indicate supplementary information that need not be included.

Summary

A switching power supply specification inherently requires details on more items than does an equivalent linear supply specification. This, coupled with the newness and complexity of switching technology, makes specifying the best possible unit for a given application a difficult task.

One rule that has proved beneficial: Keep it easy to achieve. Never specify a range that is unnecessarily broad for the application, such as meeting transient response under all input conditions, when it really is not needed. These overly strict requirements can drastically increase unit cost and frequently lower the supply's reliability.

Finally, a good interplay with the vendor is of paramount importance. Sit down and talk together. Discuss your specification in great detail. Do not consider any agreement firm until and unless it is in writing. If the company that you are dealing with does not operate in this manner, find one that does. It is the only way to get a switching supply that gives full and lasting value.



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The Remex RFS7500 is a better system at lower cost than the OEM can build himself or buy from a minicomputer manufacturer or second level supplier. Don't go to pieces, go to Remex, 1733 E. Alton St., P.O. Box C19533, Irvine, CA 92713 (714) 557-6860. Servo information contained in the intersector gap is more accurate and efficient than dedication of one disc surface to servo data; the concept also enhances interchangeability of discs

Servo Control Technique Enhances Performance of Disc Storage Units

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An innovative technique of servo design applied to magnetic disc storage units achieves increased capacity and high performance at low cost. The technique relies on servo information embedded in the data storage tracks, instead of setting aside a separate disc surface for the servo signals. It is called interspersed servo track following and, in the opinion of many, is the first-choice technology for all future highcapacity drives.

The method depends on prerecorded servo data embedded in the sector overhead area, and makes each head operate in a closed-loop servo on the track it is seeking. The result is higher positioning accuracy, greater utilization of disc surfaces, and disc pack interchangeability over a wide temperature range, completely eliminating the need to use so-called "customer engineer" disc packs to align the mechanism and ensure interchangeability.

Interspersed servo track following (ISTF) is a fourth-generation technology. If the original, mechanically positioned, moving-head disc drives were the first generation, second-generation machines had inductive or optical transducers that controlled linear motors (voice coils) via powerful servo amplifiers. The prime advantage of the second generation was the fast maximum and average access times, although positional accuracy still depended upon a transducer mounted on the body of the disc drive. Thus, the servo system positioned the heads relative to the drive body, rather than relative to the disc in its cartridge or pack. System accuracy was therefore limited by tolerances in the transducer, chassis, drive spindle and cartridge/ pack assembly, and by the effect of temperature on these tolerances. The only mechanical solution to this problem is to place the head carriage, data heads, and positional transducer within the disc pack or cartridge—an approach used in several machines announced in recent months.

Third generation alternative was to provide a reference on the pack itself for accurate head-to-track positioning. This reference took the form of a servo surface, which consists of one prewritten clock track on each cylinder. This track positions the heads during the last half of one track pitch of the seek operation [Fig 1(a)]. However, as head and media designers achieve increasing track densities, the half-track accuracy rapidly becomes insufficient, and heads are mispositioned by integral numbers of track pitches. The problem occurs during the transition from coarse addressing by the transducer on the drive to fine addressing following the on-pack reference. The capture or seek range of the on-pack reference must be



Fig 1 With and without ISTF. Third-generation disc drives have error-prone seek mechanisms (a) that attempt to bring head to within half track pitch of desired track, then depend on a servo with narrow capture range A-A to complete movement. With ISTF (b), capture and seek range A-A is much wider than coarse positional error B-B worst case; therefore coarse adjustment need not be so precise. Result is much less expensive, yet more accurate mechanism

wide enough to ensure that the coarse addressing system always positions the heads within this range, before the transition.

Servo Seeking Methods

ISTF has this facility [Fig 1(b)]; its servo seeks track groups, and precisely positions heads to within 5% of the data track width, with a coarse positioning seek range of ± 4 tracks. In contrast, the third-generation "storage module" disc drive seeks single tracks with a range of only $\pm \frac{1}{2}$ track; its head-positioning accuracy is determined by the precision of head alignment and disc pack assembly, not the servo system.

Some current coarse addressing systems use optical scales (reticules) with photocells, or detent racks with variable reluctance transducers. Both types require 2-part transducers, with one component fixed to the head carriage, the other to the body of the drive. These components must be aligned with each other and with the servo tracks during manufacture and, inevitably, during repair in the field. Although elements of human error and mechanical accuracy are therefore involved, the larger the seek range for the fine addressing system, the less serious these elements become.

An alternative coarse addressing system counts the servo tracks as they pass under the head during a seek operation. However, because the head is flying above the disc surface, and the signal levels are much lower than those in the other coarse addressing systems, the probability is high that a counting error will cause the head to address the wrong track. Such errors can also arise from disc wobble or from overshoot during coarse positioning.

The ISTF method positions the head by a conventional optical transducer, to within ± 4 tracks of the addressed track, and then switches to track following (Fig 2). This alleviates all problems described previously and



Fig 2 Four-track margin. When servo signal crosses zero, head is in its correct position. Range of single null is eight times as wide with ISTF (b) as with conventional mechanism (a)



Fig 3 Standard disc format. Servo signal is in gap between records, just before record address

makes possible reliable seeking at track densities far higher than 500 tracks/in. Furthermore, the method does not require a dedicated surface for servo data, giving a further increase in total data storage capacity.

Interspersion and Dedication Compared

Third-generation drives use a complete surface for servo tracks, which are also used for synchronizing write data and rotational position sensing. Major weakness of the dedicated servo surface drive is the accuracy with which packs must be assembled and initialized, and multiple heads aligned. Only the five surfaces adjacent to the servo surface are safely usable; heads at greater distances cannot maintain such accuracy. Thus, although the storage module drive (SMD) pack is five platters high, only the center three are used, leaving just five data surfaces from a possible eight (the outer surfaces are protective only). This method has been reasonably successful at a track density of up to 370/in, however, any further increase with interchangeable pack or cartridge systems is unlikely. It requires alignment accuracies between 20 and 200 μ in (0.5 to 5 μ m), which present a variety of temperature-related problems.

ISTF does not have a dedicated surface. Instead, the servo signal is incorporated in all data tracks. The method eliminates precision head alignments and temperature dependencies. Maximum track density is limited only by the signal-to-noise ratio of the data signal. At present, ISTF drives utilize only a standard IBM-compatible disc with 500 tracks/in, storing data at an average 4300 bits/in on each track. However, the components have been improved considerably since the ISTF disc drive system was introduced, and much greater storage capacity is feasible.

This standard format divides each track into 50 sectors, each storing 256 bytes (2048 bits) of data in a single block. Each block of data is preceded by 148 bits of synchronizing and identifying information, and is followed by error correction codes (Fig 3). Be-

tween successive sectors in a single track is a gap, in part of which servo signals are recorded. The presence of these signals requires a recovery period at the beginning of the gap or equivalently at the end of the record, during which the electronic circuits are reset following a write operation, to permit the servo signals and the subsequent sector address to be read. (A similar zone, called a splice, lies between the end of the address information and the beginning of the data, to permit new data to be written after reading the address.) An additional optional facility is hardware marking of sector condition; it identifies a sector that has been the source of repeated errors and, therefore, presumably lies in a defective area of the recording surface, and prevents further writing in that sector.

Servo signals occupy a space equivalent to 54 clock pulses and the recovery zone occupies an additional 41. Space for nine pulses is set aside as "spare," to ensure that one sector repeatedly written never drifts far enough to overlap the preceding or following sector. This adds up to 104 pulses; the sector condition, another 26 bits, makes the total 130. With 10 bits/byte in 5/4 code (a group-coded recording technique), this corresponds to 13 bytes overhead per track sector. Overhead per full track is $13 \times 50 = 650$ bytes. Each sector contains a total of 277 bytes, including all address and correction data, so that unformatted user data equals $277 \times 50 = 13,850$ bytes. Total overhead per track is thus 650/(13.850 + 650) =4.5%, a ratio that persists for all tracks on a surface and all surfaces in a disc pack.

A similar calculation for the dedicated servo surface drive is simpler, but the result is quite different: the number of bytes is not needed, because one whole surface out of the six available is reserved for servo signals. Overhead is therefore ½, or 16.67%. Thus the ISTF system is more economical by a factor of 3.7 than systems based on a separate servo surface.

Eccentricity, or runout, of the cartridge or pack, when mounted on a different drive, is a significant problem at high track densities. It can destroy the horizontal and vertical accuracy essential for good



Fig 4 Runout compensation. Feedback reduces effective wobble of eccentric disc to one-fifth of its open-loop amplitude

servo/data correlation. For the pack, the only solution is extremely accurate assembly, to minimize disc wobble.

On the other hand, the ISTF cartridge is immune to runout amplitudes far higher than those that occur in practice, because the servo sample rate is high enough that the head can follow the track eccentricity. This immunity was demonstrated in an experiment with a special disc pack, purposely built with a runout of $\pm 500 \ \mu$ in. The open loop servo signal (Fig 4) displays this amount of runout. When the servo loop was closed, the servo signal dropped to $\frac{1}{5}$ of the open loop signal or approximately $\pm 100 \ \mu$ in, with appropriate gain adjustment. Since runout on the standard disc

	VRC	VRC CDC	Ampex	Calcomp	
	5017-3	9762	980	T-50	T-80
Capacity (Mbyte)	56.7	82.0	82.0	54.7	82.1
Data Surfaces	4	5	5	5	5
Tracks/Surface	1024	800	800	800	800
Total Tracks	4096	4000	4000	4000	4000
Tracks/in	500	384	384	370	370
Bits/in	4000	6038	6038	4040	6060
Overhead/Sector (bytes)	21	73	73	66	96
Formatted Capacity (256-byte sector)	52.4	65.6	65.6	42	58.4
Avg Seek Time (ms)	40	30	30	30	30
Avg Latency (ms)	9.5	8.3	8.3	8.3	12.5
Transfer Rate (Mbits/s)	6.11	9.67	9.67	6.44	6.44
Configuration	1 over 1	5 high	5 high	5 high	5 high
Code Recorded	5/4 mod	MFM	MFM	MFM	MFM
I/O Code	NRZ	NRZ	NRZ	NRZ	NRZ
MTBF (hours)	4000	1600/1900		2500	2500

drive of this type does not exceed $\pm 250 \ \mu in$, the track-following accuracy will always be within $\pm 50 \ \mu in$.

Advantages

Marked reduction in cost per bit is the immediate and obvious advantage of the high areal storage density offered by ISTF technology. Together with low unit cost of the media and small physical size of the drive, this makes the technology also suitable for cartridge drives or combination fixed disc/removable cartridge drives.

An independent survey by the Datapro Research Corp, published in March 1976, reviewed 27 drives of this type. Its report showed that the ISTF drive had the lowest cost per bit, less than half that of its nearest rival. In 10 cases the ISTF drive cost was equal to, or less than, the cost of drives with less than one-quarter of its formatted capacity. The ISTF drive competes well with storage module drives and, in addition, because of its high capacity and fixed/ removable format, makes possible sophisticated systems with a single drive. General characteristics of several drives are compared in the table.

A second advantage of the ISTF initialized cartridge is its use of an IBM 3336 disc in an IBM 5440 plastic cartridge. The disc is initialized with servo zones during manufacture, instead of servo surface initialization for the SMD pack. Thus, the ISTF cartridge is composed of standard IBM parts, assembled in a slightly different way.

Still another advantage, rather obscure but nonetheless important, is the stability of the error rate of ISTF in a changing temperature. All third-generation drives use a head positioning correction facility that, under certain circumstances, makes nonsense of their specified access times, and can greatly increase users' hardware, firmware, and/or software overhead. This positioning technique, using the separate servo disc, may malfunction whenever a significant temperature change occurs between seek operations, even though the change remains within the specification for the device. The change is most likely to be encountered when a disc pack is replaced. The replacement pack is likely to have been sitting on a storage shelf at room temperature, while the mechanical and electrical energy expended by the drive make it substantially warmer. Until it reaches drive temperature, therefore, the replacement pack may be subject to numerous seek malfunctions.

This malfunction, which is effectively a misalignment of the head with the track, manifests itself in the form of a read error. Most systems attempt to recover data in error by rereading several times, manipulating the timing of various command pulses in the interface; every reread requires a full revolution of the disc, a delay of several milliseconds. If a record must be reread once a day, it is a minor nuisance; but if a malfunctioning mechanism requires one record in ten to be reread, perhaps several times, the reduction in throughput is very costly.

Sooner or later, of course, if an error persists through enough rereads, it graduates from "soft" to "hard"; different manufacturers specify different numbers of rereads before reaching this point of capitulation, sometimes with various other conditions imposed. Ampex and Control Data, for example, specify that an error becomes "firm" if it survives three retries and "hard" if it outlasts 27; Calcomp drives go directly from soft to hard after 19 retries. But errors in Vermont Research drives with ISTF can be adjudged hard after only three retries, without any manipulation of command pulses. Thus the effect of occasional errors on throughput is minimal. In all cases, of course, the specified frequency of error at various levels is less by factors of 10 to 1000 as the errors become more solid.

Third-generation drives are vulnerable in that every servo track is effectively a clock track; it contains revolution and sector markers as well as servo signals. This means that if a servo track is corrupted, a complete cylinder of five tracks is lost. With ISTF, if the user should lose a sector pulse, or grossly damage the track, he loses only that one, rather than five tracks.

The ISTF drive has fewer heads to align than do third-generation drives; and alignment is made to a lower mechanical accuracy and without a customer engineer pack. With the ISTF system, every cartridge can be used to align heads.

Medium to large original equipment manufacturers can reduce their cost by purchasing uninitialized disc packs and doing their own initialization and certification. Initialization equipment for the 5-high SMD pack is very expensive, because it requires very high accuracy.

As a general rule, the ISTF approach requires fewer organization or housekeeping bits per sector than thirdgeneration techniques do. This in turn tends to reduce the linear bit density in each track. Controller designers should keep this simpler overhead in mind; it can affect their choice of format.

Interspersed servo track following is a field-proven technology. Pilot "end-user" installations in the USA and Europe have been running for over a year, with a realized MTBF in excess of 4000 hours. All of the design problems normally associated with new generation disc drives have been resolved.



Terry W. Wright, as Vermont Research's engineering manager for Europe, is responsible for applications engineering, documentation, and product development. He holds the Full Technological Certificate of the City and Guilds of London in telecommunications engineering, digital computers, and digital switching systems.

DESIGN NOTE

Electrical Scanning Reduces Back-Panel Testing Time

Michael Karr

Massachusetts Computer Associates, Incorporated Wakefield, Massachusetts

Instead of testing for a connection between pins, a much faster testing method scans the panel looking for pins that either are or are not connected to a previously checked pin, recording their addresses as it goes

Industrial continuity testers contain cards that are inserted into the sockets of the panel in place of the logic cards that ordinarily go there. Test cards may or may not themselves contain circuitry; in any case they are connected to a minicomputer or paper tape controller, which is responsible for performing the test.

A suggested alternative procedure follows this same approach, but permits the construction of a tester which can check out large backpanels in a small fraction of the time required by present designs. The innovation is in the design of the test cards, which comes from reconsidering the nature of continuity testers.

What Testers Can and Cannot Do

A little thought shows that a continuity tester, whether it is a battery, two probes, and a light bulb or several hundred thousand dollars worth of minicomputer and test cards, can test only continuity—not wiring. For example, it cannot dis-



Although these two sets. Although these two sets of pins are wired differently, they are electrically identical—or would seem so to a continuity tester criminate between the two different wirings of Fig 1. The most that it can do is to partition pins into maximal electrically connected sets. In other words, it can group the pins into subsets, such that any two pins in the same subset are connected, and any two pins in different subsets are not connected. Many different wirings can lead to the same grouping.

Thus the testing of back-panel wiring may be divided into two parts: first, determine the subsets; then analyze the wiring errors by comparing subsets that result from the actual pin connections with those that would result from the desired pin connections.

At present, the minicomputer in the tester does these two tasks in immediate succession—at almost the same time. In large scale industrial practice, it is advantageous to establish the subsets first, and then do

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a very powerful error analysis on a high speed computer. For example, most wiring mistakes are made when a wire is put on an incorrect pin. This creates two apparent errors a missing connection and an extra connection. In both human and machine wiring, the incorrect pin is usually near the correct pin, so that, from the geometry of the pin layout, the computer can produce much more specific error reports than would otherwise be possible.

However, algorithms for generating such error reports are valueless without information about the subsets. This article describes the design of a device that rapidly determines the subsets.

How Not To Design a Tester

When the activity of a technician with a battery, two probes, and a light bulb was automated, the basic command to the tester naturally seemed to be, "Find out if there is a connection between pin X and pin Y." Most present-day testers are designed around this basic idea, though some have variants, such as: "Is there some pin in set U connected to some pin in set V?" (Never mind how these sets are specified.)

The problem with this approach, and all minor variants of it, is that the basic command (in the worst case) must be issued a number of times that grows in proportion to the square of the number of pins. This can be proved mathematically; we shall not demonstrate the proof, but the reader is invited to explore various strategies, which will reveal the difficulties.

In practice, test times need not actually grow as the square of the number of pins because, generally, few departures from the correct wiring are found. Desired connections may be fed to the tester as a "hint"; then the closer the wiring is to being correct, the more nearly linear is the ratio of test time to the pin count. However, the time may still increase in proportion to the square of the number of errors. A ratio of 7:1 has been observed between two test times on a back-panel tested first with many wiring errors, and again with few errors. Thus, the limitation of this design approach is felt in practice as well as in theory.



Searching With Electricity

The proposed design uses electricity to search directly for connected pins. To illustrate this idea, suppose that a light bulb is connected to each pin [Fig 2(a)]. Power is supplied to the left-most pin. Then all pins in the connected subset light up [Fig 2(b)]. Thus, the first subset is very quickly identified electrically.

However, all pins in the subset must be individually identified. The first such pin is one whose light is on, but which is not externally connected to power; we call this a rogue pin. To identify the next pin in the subset, the first rogue pin must be checked off. The easiest way to do this is essentially to connect the rogue pin directly to the power source in addition to connecting it through the left-most pin [Fig 2(c)]. Any pin can be so connected; connecting the left-most rogue pin identifies it, and the second left-most lit pin becomes the rogue. This is the next pin in line, but not necessarily the next pin in wiring order. After two more such connections, there are no more rogue pins. Thus, the first subset has been gathered in four steps, independently of the size of the back-panel.

At this juncture, it would be desirable to identify a pin whose light bulb is not on—we call this an untested pin. As good a place as any to start is at the left-most untested pin. A command to connect the leftmost pin starts the identification of the next subset (which in our example consists of only one pin). It is necessary, at the end of the test, to detect that there are no more untested pins.

In summary, then, the algorithm for testing is:
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1. Disconnect all pins from power, and initialize the output device.

2. If there are no more untested pins, the test is finished. Otherwise, find the first pin of a new subset, send the pin's address to the output device, and connect it to power.

 If there are no more rogue pins, repeat step 2. Otherwise find the nearest rogue pin, send its address to the output device and connect it to power.
 Repeat step 3.

Connection of Cards to Minicomputer

In most commercially available testers, the test cards carry direct connections from each contact of the back-panel socket to a cable that leads to a central switching matrix, under control of the minicomputer. This design is straightforward, but it is expensive and physically unwieldy, because it may require hundreds of heavy cables containing many individual wires leading to the main switching matrix.

Rather than connect each test card directly to a switching matrix, one commercially available tester connects each test card to the next in a row, and couples the minicomputer to the first and last test cards, to form what amounts to a ring. Electronic switching circuitry on the test cards, under control of the minicomputer, connects specified pins to one of two buses running through the ring; the minicomputer then determines continuity. This ring concept greatly reduces the bulk and cost of large testers; it would be highly desirable to implement the algorithm of the previous section using this connection discipline.

An important aspect of this design is that all the test cards are identical. Therefore they can be efficiently manufactured, and are rather simple to set up for the test. A particular card does not have to go in a particular slot—all that matters is that cards are connected in the proper order. This is to be compared with setting up for a test using a central switching matrix, when each card must be plugged into a specific socket.

Design of the Test Card

Design of the test card that implements the algorithm is based on the connection of the test cards in a ring and on the interchangeability of all the test cards. Three kinds of information pass through the cable from the last card in the ring to the minicomputer: the address of a pin, the presence or absence of more rogue pins, and the presence or absence of more untested pins. Similarly, three commands pass through the cable from the minicomputer to the first card in the chain: disconnect all pins from power, connect left-most untested pin, and connect left-most rogue pin.

If there are N pins, a pin address can be encoded in $\log_2 N$ wires or the next larger integer number. These signals thus require a total of $(\log_2 N) + 5$ wires, plus one for ground. A practical cable size is 24 wires; if 18 are address lines, they can reach $2^{18} > 250,000$ pins much larger than any panel of practical size.

On the card itself (Fig 3), power and ground lines go straight through the card, as do the two "connect" lines—though in large rings an amplifier may be desirable on each line to reshape the signal. The "untested line," which reports when the test is over, works through more complicated input/output logic. The "untested line out" is true if the "untested line in" is true, or the card has an untested pin. The "rogue line out" is controlled by similar logic. It is easy to verify that the "rogue line out" from the last card is true if and only if at least one card has one or more rogue pins; the same applies to the "untested line out."

The only unobvious aspect of the design is the control of the address lines. If there is a rogue pin anywhere, its address must come out of the last card. At most one card in the entire ring has both a false "rogue line in" and a true "rogue line out." This is the card with the left-most rogue pin. If this is the last card, it encodes on its address lines the card-relative address of the left-most rogue pin; the proper address appears in the minicomputer, provided the pins are numbered from right to left. Integrated circuits are available off the shelf to do this encoding.

If the first rogue pin is not on the last card, the correct address still appears at the end of the ring, as the result of a simple trick: If a "rogue line in" is true, the card adds the number encoded in its "address lines in" and the number of pins to which it connects on the





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back-panel, and puts the sum on the "address lines out."

If there are no rogue pins, the address of the first untested pin is produced at the last card in essentially the same way—except that the address of the untested pin is always overridden by that of a rogue pin.

In summary, the address lines logic for a card is as follows: "address lines out" carry the card-relative pin address of the first rogue pin on the card, if "rogue line in" is false and "rogue line out" is true. However, if both these lines and "untested line in" are false, and "untested line out" is true, "address lines out" carry the card-relative pin address of the first untested pin on card. Under all other conditions, the "address lines out" carry the sum of the number on the "address lines in" and the number of local pins.

Since a pin is identified as the left-most rogue or untested pin if power has not been applied locally and if the corresponding input line is false, when the respective command is issued it may be connected locally to power. Some care must be taken so that at most one untested pin is connected to power per command issued, but this is a detail of circuit design. The "disconnect" command may consist of simultaneous signals on both "connect" lines, an otherwise unused possibility, detected by the logical AND of these lines.

Characteristics of the Design

Main factor limiting the speed of this tester is the propagation time of address information from one card to the next. This involves a choice between an internally generated address, and the sum of the incoming address and a constant. With today's electronics, a reasonable estimate of the time for this choice is 1 μ s. Therefore a command can propagate through a ring of 1000 cards in 1 ms. Only one command per pin is required; if the cards have 80 pins apiece, the 80,000 pins can be analyzed in less than a minute and one-half. This compares with a time of several hours on existing testers to check out the same amount of wiring in the absence of any errors.

The proposed design, of course, has no concept of "error"; it merely reports on the existing wiring. Thus to compare several hours to one minute is somewhat unfair. An upper-bound estimate of how long error analysis would take a large machine, based on algorithms that have been sketched out but not vet implemented, is 10 minutes for a large back-panel with a typical number of errors. The fact that this 10-minute time is spent on a more expensive machine is balanced by the fact that its error reports are much more informative than those produced on a minicomputer.

In addition to this rather dramatic increase in speed, the design drastically reduces requirements on the minicomputer, because the only software needed are the test algorithm and I/O routines-to run a tape drive for recording the subsets. These requirements are so minimal that conceivably an economic alternative would eliminate the minicomputer altogether, in favor of a black box containing the algorithm in hardware or firmware. With a data link, the tester can be an input device to the large machine used for error analysis. These requirements are to be compared with the moderatesized minicomputer with peripherals that are typically associated with a tester capable of handling backpanels of about 100,000 pins.

Conclusions

The design is an example of the principle that the automation of human activities is often best done quite differently from the activity it replaces. In this particular case, the different approach was inspired by the realization that algorithm times are not linearly related to the size of the test when they are based on the elementary commands of existing testers. Once this was observed, clearly the basic commands had to be changed.

Acknowledgements

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APPLICATION NOTE

Low Cost A-to-D Conversion During Microcomputer Idle Time

Howard A. Raphael

Intel Corporation Santa Clara, California

When a microcomputer is not fully utilized, it can perform analog-to-digital conversions using either of two techniques, with a minimum of additional hardware

Many microcomputer applications call for a simple, low cost technique for converting analog signals to digital form. Since the microcomputer should do as many of the ancillary input/output (I/O) functions as possible, the least expensive means of interfacing an analog source is required at a given level of performance and accuracy. The microcomputer itself can convert one or several multiplexed analog sources using digital techniques. The technique is not necessarily accurate, and it does not filter out common-mode noise, but it is easy, requires very little extra hardware, and is useful in an application where the microprocessor is not kept busy. In addition, the microprocessor can do comparisons on the digital output of the conversion, whereas a conventional A-D converter cannot.

All microcomputers can measure time by executing a particular string of instructions a prescribed number of times. This string requires a fixed amount of time to execute and is called a delay routine; its resolution is the execution time of a single instruction. An example of a delay routine appears at the end of this article. Timing can be adjusted by adding NOP (no-operation) instructions as the final value of time is approached. NOPs take only enough time to be fetched from memory; they do nothing, therefore they take no execution time. The computer immediately fetches the next instruction.

VCO Technique

One method of A-D conversion (Fig 1) uses an analog sensor such as a strain gauge, thermocouple, or positional inductive transducer, and a voltage-controlled oscillator (VCO), the output frequency of which is proportional to variations in the analog source. The resulting frequency drives a digital counter for a fixed interval of time as determined by the microcomputer. The microcomputer samples the resulting Final Value Count (FVC) after the end of the fixed interval. Since the sample rate is fixed, changes result in the VCO frequency brought about by changes in the analog source. Count is converted to a display character or decimal value through a table look-up.

Length of the counter and frequency variation of the VCO determine the resolution of the A-D conversion. From time to time, a reference frequency may be applied to the counter, perhaps by multiplexing a known analog source to the VCO, and comparing the resulting FVC to a preprogrammed value. Any differences in the measured FVC and that expected from the reference disclose a drift or other error, which ordinarily is limited to about 0.5% using standard digital elements.

To use the implementation, the designer must determine three variables: range of the VCO for a given

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Fig 1 VCO method. Analog source controlling frequency of oscillator also controls total accumulated in counter during fixed time interval. Counter contents therefore reflect digitally the magnitude of the analog signal





sensor, number of counter stages (typically eight), and microcomputer-generated time interval. These variables are related in that the VCO frequency should not overflow the counter during the measuring interval, but should register enough counts to provide good resolution. A specific implementation is based on the Intel MCS-40, a self-contained 3-chip microcomputer. One of the three integrated circuits, the 4308 read-only memory, also contains I/O facilities. Other components such as communication devices and keyboard/displays can be added to the system bus. The VCO is free running. When a conversion is desired, the computer enters the conversion routine, clears the counter, then activates the count enable line. This line is held active for the predetermined fixed interval, while the counter accumulates the equivalent voltage measurement. At the completion of the fixed interval the counter is disabled, and the FVC is read into the MCS-40 system via the 4308 I/O lines.

Pulse Width Technique

Another approach to the poor man's A-D conversion uses a monostable multivibrator (one-shot), with a timing circuit which includes the variable analog source (Fig 2). The multivibrator is non-retriggerable—that is, once timing is initiated, the device produces a full-width output pulse, independent of additional trigger inputs.

The one-shot receives a trigger signal from the microcomputer, and its output controls the count-enable input of the counter. This input is any suitable frequency source, such as the system clock. When the computer triggers the one-shot, the variable analog source determines the time-out period, during which the counter counts the number of pulses generated by the frequency source. When the one-shot turns off, the number in the counter is proportional to the level of the analog signal.

Availability of the conversion is communicated to the microcomputer by testing the one-shot output or by receiving an interrupt when it turns off. The interrupt allows the central processing unit (CPU) to perform other tasks during the conversion; the repeated test does not.

In the MCS-40 system, for example, the one-shot controls an 8-bit binary counter incremented by the system clock at intervals of $1.35 \ \mu s$. If the counter is used for its full range of 255 steps, the range of the one-shot must be correspondingly wide, from 1.35 to 344.25 μs . This is a large order for a single timing circuit; alternatively, since the MCS-40 can work in binary-coded decimal (BCD) as well as pure binary, a 2-digit BCD counter may be substituted for the binary counter. Now the full range is only 99 steps, and

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Delay Routine

In the MCS-40 a delay routine can be built around an instruction called Increment Skip if Zero (ISZ). In this instruction, the content of a selected internal register is incremented by 1. If the result equals 0000, program execution continues in sequence; if the result does not equal 0000, program execution continues at the location specified by an 8-bit address which accompanies the instruction. This is an example of an instruction with which the programmer creates loops that, among other things, can measure time.

For example, a 4-instruction routine steps off a 5.14-ms delay:

	FIM 0,32
ELAY	ISZ 0,DELAY
	ISZ 1,DELAY
	JUN OUT

FIM is a Fetch Immediate which loads the number 32 into register pair 0, consisting of single registers 0 and 1, four bits each. Decimal 32 is binary 0010 0000, which means that register 0 now contains 0000 and register 1 contains 0010. The first ISZ then executes 16 times, repeating itself over and over; the first execution changes 0000 to 0001, the "next" instruction is itself. When register 0 comes up 0000 again, the next instruction in sequence is the second ISZ, which executes once and jumps back to the first ISZ. This continues— 16 executions of the first ISZ followed by one of the second—until register 1 comes up with 0000, which takes 14 times, since register 1 began with 0010. An unconditional jump (JUN) then takes the program out of the loop.

Total number of executions in the loop is 14 (16 + 1) = 238. Each ISZ requires two cycles at 10.8 μ s each, or 21.6 μ s; total elapsed time, therefore, is 238 x 21.6 = 5.14 ms.

the one-shot must have a range of 1.35 to $133.65 \ \mu s$.

Conclusion

Both VCO and one-shot methods of A-D conversion are simple, low cost techniques. The VCO method varies the clock rate during a fixed time interval; the one-shot method varies the time interval of counting at a fixed rate. The VCO technique is self-clocking and can track changes in the analog signal during conversion, but requires the CPU to turn it both on and off; whereas the oneshot, once started, turns itself off but depends on the system clock or other oscillator to drive the counter. Both methods thus have their advantages and disadvantages, but both work well.

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TECH BRIEF

Computer/Computer Interface

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A computer/computer interface synchronizes data transfer between two computers by generating data strobe pulses when the computers are ready for data transfer. In addition, the interface filters noise by sampling.

The system incorporates eight bidirectional data lines connecting the two computers. There are also four timing control lines: two are request lines which are unidirectional, and the other two are bidirectional response and ready lines. Time sequence of the control lines is described in the following steps. The operation is repeated for each linear bit or parallel byte. The request line is asserted (turned on); assertion of the request line is sampled and synchronized; the synchronized request signal allows assertion of the return response line; the return response line is synchronized and allows assertion of the ready line; the ready signal is sampled and synchronized and can be used to form a data strobe pulse for sampling the received data; upon sampling the received data, the ready signal can be used to turn off the response line; turnoff of the response line allows turnoff of the ready line; turnoff of the ready line again allows the response line to be turned on, which is conditional on

the request line being on; at the end of a block transmission the request line is turned off simultaneously with the ready line for the last character being turned off.

The interface is structured to recognize a signal change only when the signal remains in its new state for two consecutive clock periods after it has remained in its prior state for at least two clock periods. Thus, a noise pulse of either polarity of a duration less than two clock periods occurring at any time will not be the cause of a double data strobe pulse, nor will it interrupt the forming of a data pulse or the subsequent report level indicating that a data strobe is formed.

Note

Requests for further information may be directed to: Technology Utilization Officer, NASA Pasadena Office, 4800 Oak Grove Dr, Pasadena, CA 91103. Reference: TSP75-10326.

Patent status

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to: Patent Counsel, NASA Pasadena Office, 4800 Oak Grove Dr, Pasadena, CA 91103. Source: Tage O. Anderson of Caltech/JPL (NPO-13428). This document was prepared under the sponsorship of the National Aeronautics and Space Administration. Neither the United States Government nor any person acting on behalf of the United States Government assumes any liability resulting from the use of the information contained in this document, or warrants that such use will be free from privately owned rights.



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MICRO PROCESSOR DATA STACK

Microcomputer Interfacing: Register Pair Instructions

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Last month we discussed the single-byte data transfer instructions, MOV D,S and MVI $\langle B2 \rangle$, in the 8080 microprocessor instruction set. Significant points of the column are summarized in Fig 1, which indicates that for the MVI r $\langle B2 \rangle$ instruction, the data byte that is transferred to a register comes from the instruction itself, whereas for the MOV D,S instruction, the data byte is copied into destination register D from source register S.

Since the 8080 chip has a 16-bit address bus, both a 16-bit program counter and 16-bit stack pointer¹ exist within the chip. As a consequence of this architecture, it would be very convenient to be able to manipulate full 16-bit address words internally within the chip. This is done through the use of register pair operations, which treat the six general-purpose registers as three sets of register pairs, B and C, D and E, and H and L. Each register pair has associated with it a unique 2-bit register pair code,

Program to Transfer Data From Memory Location

Instruction Code	Mnemonic	Comments	
041	LXI H	Load register pair H with following LO and HI ad- dress bytes	
123	1.23	L register byte	
030	030	H register byte	
126	MOV D,M	Move data from the mem- ory location addressed by register pair H to register D	





Register Pair	HI Byte	LO Byte	2-Bit Register Pair Code
В	В	С	00
D	D	E	01
Н	н	L	10

The final 2-bit register pair code, 11, is reserved either for the stack pointer (SP) or the program status word (PSW), which consists of the contents of the accumulator and flag bits. In register pair operations, the HI byte is always the most significant eight bits in the 16-bit memory address; the LO byte is the least significant eight bits. Registers B, D, and H function as HI address bytes; C, E, and L, as LO address bytes.

As one example of a register pair operation, consider the 3-byte load register pair immediate instructions,

LAI IP	
<b2></b2>	(LO byte)
<b3></b3>	(HI byte)

TVI

which permit the data bytes contained within the second and third bytes of the instruction to be moved to the register pair, rp. General format of the instruction is,

0 0	R P O	001
Instruction	2-bit code	
class	for register	
	mair	

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Listing of Additional Register Pair Operations

legister Pair Operation	Octal Instruction Code	Comments
XCHG	353	Exchange contents of register pair H with contents of register pair D. HI bytes, H and D, exchange with each other and LO bytes, L and E, exchange with each other
SPHL	371	Load contents of register pair H into the stack pointer
PCHL	351	Load contents of register pair H into the program counter
LXI SP <b2> <b3></b3></b2>	061 <b2> <b3></b3></b2>	Move instruction bytes $<\!\!B2\!\!>$ and $<\!\!B3\!\!>$ into the stack pointer. $<\!\!B2\!\!>$ is the LO byte and $<\!\!B3\!\!>$ is the HI byte

Supplementary Listing of Register Pair Operations

Register Pair Operation	Octal Instruction Code	Comments
XTHL	343	Exchange the top of the stack with the con- tents of register pair H
DAD rp	011,031,051, or 071	Add contents of register pair rp to register pair H. Only the carry flag is affected
PUSH rp	305,325,345, or 365	Push register pair rp on stack
POP rp	301,321,341, or 361	Pop register pair rp off stack
SHLD <b2> <b3></b3></b2>	042 <b2> <b3></b3></b2>	Move contents of register L to memory lo- cation specified in instruction bytes <b2> and <b3>. Move contents of register to the succeeding memory location</b3></b2>
LHLD <b2> <b3></b3></b2>	052 <b2> <b3></b3></b2>	Load register L with contents of memory lo- cation specified in instruction bytes $\langle B2 \rangle$ and $\langle B3 \rangle$. Load register H with the con- tents of the succeeding memory location

Some examples include:

Data Transfer Operation	Mnemonic	Octal Instruction Code
$\langle B2 \rangle \rightarrow C$	LXI B	001
	< <u>B2</u> >	< <u>B</u> 2>
$\langle B3 \rangle \rightarrow B$	<b3></b3>	<b3></b3>
<b2> → E</b2>	LXI D	021
	<b2></b2>	<b2></b2>
<b3> → D</b3>	<b3></b3>	<b3></b3>
<b2> → L</b2>	LXI H	041
	<b2></b2>	< B 2>
$\langle B3 \rangle \rightarrow H$	< <u>B</u> 3>	<b3></b3>

It should be noted that the accumulator and "memory register" are not used as a register pair. To transfer data from memory location HI = 030 and LO = 123 (discussed in last month's column), the simplified Program (shown in the panel) is executed.

Fig 2 summarizes the four LXI rp instructions. Keep in mind that individual registers cannot arbitrarily be paired. For example, to load registers C and D with data for an operation, you will not be able to use an LXI rp instruction; use MVI C and MVI D instead. To substitute register E for register C, an LXI D instruction can then be used to load both register bytes into the indicated registers.

Other useful register pair operations are shown in the Listing. Since the program counter always contains the address of the next instruction to be executed, the register pair instruction PCHL is actually a jump instruction.

Two useful instructions for manipulating 16-bit memory address words are the increment register pair, INX rp, and decrement register pair, DCX rp, instructions,

0 0	R P O	011
Instruction class	2-bit code for register pair	Increment operation
0 0	RP1	011
Instruction class	2-bit code for register	Decrement operation

With these instructions, the 16-bit contents of the register pair are either incremented or decremented as a single 16-bit word. However, no condition flags are affected by the INX rp or DCX rp instructions. You do not get a carry out of the most significant bit; the zero flag is not set when the register pair contents are zero; etc. It should be clear that the INX rp and DCX rp instructions are designed for 16-bit address operations, not for multiprecision arithmetic.

Other register pair operations are covered in the Supplementary Listing, together with codes and comments. SHLD and LHLD instructions can be used as 16-bit I/O instructions if the I/O devices are addressed as memory

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locations.^{2.3} The above instructions will be discussed in subsequent columns.

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This article is based, with permission, on a column appearing in American Laboratory magazine.

Note: Dr Peter Rony, Dr Paul Field, and David Larsen will direct workshops to be held at the Virginia Polytechnic Institute and State University. The first, "Digital Electronics for Automation Workshop," June 7 and 8, is a 2-day workshop based on small- and mediumscale TTL ICs. Laboratory time with individual breadboarding stations will be provided along with in-depth lectures. "Microcomputer Interfacing Workshop," June 9, 10, and 11, is a 3-day workshop based on the popular 8080 microprocessor, with over 20 operating 8080 computers available for participant use. More information on these workshops is available from Dr Norris Bell, VPI and SU Continuing Education Center, Blacksburg, VA 24061, Tel: (703) 951-6328.

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The 8048, 8748 (a reprogrammable version), and the 8035 (an alternate design for additional system expansion) are all fully programmable systems designed to perform I/O control and processing tasks at rates up to 400k operations/s typical. I/O functions can be modified with system software, and, in addition, the system can operate as an I/O processor.

Basic processing and control subsystems of the three devices are alike—an 8-bit general-purpose CPU, 64-byte read/write memory, three programmable 8-bit I/O ports and eight other control and timing lines, programmable interval timer/event counter, priority interrupt controls, system clock generator, and a set of generally required system controls and utilities.

The CPU has a 96-instruction set; the register and stack array are located in a part of the data memory to permit expansion. CPU can operate as an 8-bit parallel binary processor, 4-bit binary processor, or BCD arithmetic processor. It can also address on-chip memory and/or peripheral memory; on-chip memory can be expanded if necessary.

All three are plug-compatible, 40-pin devices that operate on a single 5-V power supply. The 8048 operates as a standalone single-chip system with programs stored in 1kbyte masked ROM on the chip. The 8748, an interchangeable single-chip system, contains a 1k-byte EPROM for program storage. Memory is erasable with a beam of ultraviolet light through a transparent window on the package. It is then electrically reprogrammed. After programs are developed on the 8748, the device can be used in a new product design or can be replaced with an 8048. Equivalent to the 8048/8748 microcomputers without a program memory, the 8035 provides peripheral program storage.

MCS-48 expansion peripherals include a 24-pin I/O expander with 16 I/O lines that attach to one of the I/O ports; a 2k RAM, I/O, and timer which add 256 bytes of static RAM, 22 programmable I/O lines, and a programmable interval timer/ event counter to the microcomputer; 16k EPROM and I/O which adds 2k bytes of EPROM and two programmable 8-bit I/O ports; and 16k ROM and I/O, a mask-programmed ROM unit with two 8-bit programmable I/O ports.

The systems can also be expanded with MCS-80 components which provide a series of programmable LSI peripheral and I/O devices for complex interfaces (see *Computer Design*, Feb 1976, p 132).

The Intellec Microcomputer Development System (*Computer Design*, Aug 1975, pp 94-95) supports the 8048 system, as does the Intellec PROMPT 48 Personal Programming tool, a low cost tool for direct development of programs on the 8748.

8048 development enhancements include a resident macro assembler, ICE-48 in-circuit emulation module for software/hardware integration and debugging, and personality cards for the Intellec Universal p/ROM programmer to permit developmental programs to be stored in the 8748 microcomputer or 16k EPROM and I/O peripheral.

Deliveries of 8048 system components and support products, which are now being made in evaluation quantities, are planned to begin during the spring of 1977. Circle 170 on Inquiry Card

Family of Low Cost Microcontroller ICs Fits Dedicated Control Needs

To fill the gap between generalpurpose microprocessors that often are too powerful, and dedicated custom LSI circuits that take too long to develop, National Semiconductor Corp. 2900 Semiconductor Dr. Santa Clara, CA 95051 has designed a series of calculator-oriented processor systems (COPS). The three microcontrollers comprising the family include the MM5781 and 5782 set, the single-chip MM5799 controllers, and the simplified MM57140, each containing everything necessary to implement most dedicated control applications for less than \$10.

Sharing the same basic architecture, each controller includes a clock generator, CPU, control ROM, read/ write memory, parallel inputs, programmable outputs, and a variety of single-bit I/O ports under program control. Each can be connected directly to keyboards, displays, and similar devices through a buffer.

Differences are in the amount of ROM and RAM, and number and type of I/O ports. The 5799 contains 1536 8-bit instructions in its ROM. and its RAM can store 96 BCD digits of 4 bits each. The microcontroller also contains the RAM address register, address decode logic, an accumulator, a temporary register for intermediate results, an adder and carry latch, and a programmable logic array for converting BCD inputs to 7-segment outputs. Eight parallel latched outputs are available as binary, BCD, or 7-segmentplus-decimal-point output that is kept under program control.

In the control ROM section, there are four parallel inputs, a testable sense input, three bidirectional control flags for use as inputs or outputs, a program counter, a 2-word stack for nested subroutine calls, and an instruction-decode programmable logic array. RAM can be expanded for general-purpose usage or for key sequence storage in programmable calculator-type systems by adding the MM57126 lk-bit RAM; it connects directly to the 5799 or the 5782 without requiring interface circuits.

For more powerful systems, the MM5781/5782 2-chip set contains more internal ROM and RAM. The 5781 program chip contains the control ROM which holds 2k 8-bit instructions, the ROM address registers, control logic, and various I/O functions. The 5782 memory and processor element contains the ALU, instruction decode PLA, 160 x 4 bits

YOU WERE HIRED FOR YOUR BRAINS, NOT YOUR BODY.

It's not as silly as it sounds. Because many bright engineers and technicians are still spending their time soldering, desoldering and resoldering. Instead of designing

Which is pretty silly, considering the waste of talent. Especially when there's a better alternative.

With CSC Proto-Board* solderless breadboards, assembling a circuit is practically as fast as designing one. No

special jumpers or patch cords required - all types of components-from complex microprocessors to

resistors, capacitors and LED's-connect and interconnect as simply as pushing in a lead ... or short lengths of

#22-30 solid hookup wire. And circuit changes are done with the same

Manufacturer's suggested list Prices and specifications subje to change without notice

MODEL	NO. OF TIE-POINTS	14-PIN DIP CAPACITY	MFR'S SUGGEST LIST	OTHER FEATURES
PB-6	630	6	\$15.95	Kit – 10-minute assembly
PB-100	760	10	19.95	Kit - with larger capacity
PB-101	940	10	29.95	8 distribution buses. higher capacity
PB-102	1240	12	39.95	Large capacity, moderate price
PB-103	2250	24	59.95	Even larger capacity: only 2.7¢ per tie-point
PB-104	3060	32	79.95	Largest capacity: lowest price per tie-point
PB-203	2250	24	75.00	Built-in 1%-regulated 5V. 1A low-ripple power supply
PB-203A	2250	24	120.00	As above plus separate ¹ 2-amp +15V and -15V internally adjustable regulated outputs

plug-out, plug-in ease. All thanks to rugged, nickel-silver contacts and CSC's superior use-tested design

Proto-Board breadboards are available in a variety of sizes. from 630 to 3060 solderless tiepoints (six to thirty-two 14-pin DIP capacity), at prices from \$15.95* (kit) to \$79.95. And if you'd like built-in regulated supplies, they're available too, in models priced at \$75 and \$120.

Before you start your next project, put down your soldering iron and call 203-624-3103 (East Coast) or 415-421-8872 (West Coast)

amn

for full specifications and ordering information. Once you do, you'll find yourself soldering less ... and more than likely, earning more.



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CIRCLE 75 ON INQUIRY CARD

MICRO PROCESSOR DATA STACK



of RAM for data storage, a RAM address register, and a serial I/O port. ROM storage can be expanded to 16k bytes in the system by adding more 5781 ROM chips.

For systems that require less than what the 5799 provides, there is the MM57140-the simplest controller in the family and the lowest cost processor chip. Containing all of the functions needed for many controller and calculator applications, its ROM contains 630 instruction bytes; RAM is $55 \ge 4$ bits.

If the amount of on-chip RAM of each of the circuits is not sufficient, an interface circuit (MM5785) allows standard 1k x 1-bit RAMs to be added. All of the microcontrollers use the company's p-channel MOS process. All can be battery operated supply voltage range is 8 to 9.5 V, and power consumption is a nominal 135 mW (for the 5799).

The new generation of Diskette Drives is here and under control.

PerSci has it—a family of diskette drives "design-years" ahead of competitive drives—now available in complete low cost subsystems for interface to 8080, 6800 and other major microprocessors.

The Highest Performance Diskette Drives:

PerSci diskette drives, both single and dual head units, offer a combination of performance features unique in the marketplace while still maintaining compatibility in existing systems:

- Voice coil positioning for access speeds seven times faster than competitive drives (76 tracks in 100 ms)
- A low power all DC system reduces cost and assures high reliability
- Automatic electric loading simplifies operation and protects media
- □ Small size permits 5 single drives or 4 dual drives to be mounted vertically in a 19 in. rack

The Most Powerful Diskette Drive Controller

The PerSci Model 1070 Diskette Drive Controller puts the advanced performance of PerSci drives to work in microprocessor based systems. An IBM format compatible, "intelligent" controller, the Model 1070 will handle from 1-4 drives with minimum demand on the host system. In fact, with addition of a power supply and keyboard to the PerSci subsystem, the user can

perform many floppy disk routines without additional hardware or software. Controller features include: ☐ Interface to most microprocessors including 8080, 6800 & Z80

 Internal disk operating software including IBM formatting

RS232 interface option Rom options allowing copy data transfer between diskettes and data transfer between RS232 interface and diskette

An Economical Diskette Drive Subsystem

A complete subsystem including a single diskette drive (Model 70), the Model 1070 controller with interface and a controller-to-disk-drive cable is available in single units for \$1,195. For double capacity, a dual diskette drive (Model 270) subsystem is available for \$1,495. OEM discounts available. Don't settle for yesterday's diskette drive. Get the new generation under control from PerSci, 4087 Glencoe Avenue, Marina Del Rey, CA 90291 (213) 822-7545.



Peripherals a Generation Ahead.

32k ROM Reduces Costs and Components for Microprocessor Systems

Further reducing costs of complex 4- and 8-bit microprocessor systems, the 32k ROM (4k x 8), which features dynamic address decoding and device select circuitry, also reduces the number of required components. Rockwell International, Microelectronic Device Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803 has added this ROM, which is believed to be the largest one in the industry, to its grouping of more than 40 LSI circuits organized into five parallel processing system microprocessor families.

Up to 16 ROM circuits can be directly selected with the device's 12 address and four chip select inputs, and memory can be easily expanded through normal or "virtual" bank switching. The virtual mode permits simple switching command arrangements.

The ROM (part number A66XX) consists of over 18k transistors and elements on a 156 x 242-mil chip contained in the company's standard 42-pin plastic package. It is designed as a direct replacement for the smaller capacity A52XX and A05XX ROMs.

Circle 171 on Inquiry Card

dc/dc Converter Powers 8080 Microprocessor Plus Four RAMs or ROMs

Model 1200 microcomputer power supply is a dc/dc converter containing all the necessary outputs to power an 8080 microprocessor in addition to four 2107A RAMs or four 1702A ROMs. It is designed for local circuit board transformation of 5-Vdc logic power into well-regulated and isolated triple output voltages of 12, -5, and -9 Vdc. Other features include line and load regulation of 0.05%, maximum output ripple of 1 mV rms, and maximum transient recovery time of 50 μ s.

The isolator/regulator uses high frequency switching with transformer isolation to achieve efficient conversion in a rugged 2.0 x 2.0 x 2.75" ($5.08 \times 5.08 \times 6.99$ -cm) module. Full output power is 12 Vdc at 160

mA, -9 Vdc at 300 mA, and -5 Vdc at 2 mA with maximum tempco of 0.02% °C. Supply operates with full load efficiency of 48% and has output current limiting protection.

Available from Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021, the device is encapsulated in a diallyl phthalate case and weighs only 4.5 oz. Operating temperature range is -25 to 71°C; storage temperature range is -55 to 85°C. Circle 172 on Inquiry Card

Microprocessor Simulator Available on APL-Based Timesharing Service

As a development and debugging aid to system programmers working with microprocessors such as the Intel 8080, the interactive software simulator is offered as a public library program on PCS/Computernet[™], and APL-based timesharing service. Provided by Proprietary Computer Systems, Inc, 16625 Saticoy St, Van Nuys, CA 91406, the program provides the means of creating and managing files of assembly language source programs; assembling and loading programs into a simulated microprocessor; running programs on the microprocessor; and displaying the status of the microprocessor memory, flags, and registers. Circle 173 on Inquiry Card

Large Scale System Uses 6800 Microprocessor

Based on the flexible 6800 microprocessor, the Micro-68b is a complete microcomputer system supplied with a 13-slot motherboard and 20-A,



5-V supply in a ruggedized aluminum cabinet, measuring $10.5 \times 17 \times 18.5''$ $(26.67 \times 43.18 \times 46.99 \text{ cm})$. The computer accommodates up to 64k of RAM and accepts the full line of the company's boards including general-purpose 8k static RAM; IMP-1 printer interface; general-purpose I/O; 16k p/ROM; CRT/TTY/audio cassette interface adapter; and floppy disc interface boards.

Unit contains 8k RAM, 16-key hexadecimal keyboard, 6-digit hexadecimal LED display, 512-word keyboard monitor, and Motorola MIK-BUG lk teletypewriter monitor ROM. Bus is compatible with Motorola EXORCISER cards.

The microprocessor has a 72-instruction repertoire and includes binary and decimal arithmetic, logical, shift, rotate, load, store, branch, and interrupt. Other features include seven addressing modes, two accumulators, stack pointer and variable length stack, interrupt vectoring, and a separate nonmaskable interrupt.

Two models are available from Electronic Product Associates, Inc, 1157 Vega St, San Diego, CA 92110. The commercial version (M68bc) has all I/O [two 36-pin x 0.156" (0.39 cm) edge connectors] and bus connections [86-pin x 0.156" (0.39 cm) edge connectors] available at the rear edge connectors. Engineering model (M68be) has these connections at both the front panel and rear. All lines are fully buffered. Circle 174 on Inquiry Card

High Reliability Microprocessor Prevents Control Systems Failures

Based on the Intel MCS[™]-4 microcomputer set, these completely functional Q-series microprocessor packages include all supplementary equipment such as power supply input and output interfacing, and p/ROMs with 1536 8-bit words maximum. The basic microprocessor is built on a set of small, plug-in circuit cards. A versatile backplane/motherboard configuration allows a variety of customized system hardware design at low cost.

The microprocessor from Digital Dynamics, Inc, 830 E Evelyn, Sunnyvale, CA 94086 is expandable to read or provide 16 analog input signals, 24 digital input signals, six analog outputs, and 24 digital outputs. Digital input detects presence of 120-Vac signal, requires 1 W, and is opto-isolated. Digital output is

THAT'S WHAT MAKES OUR FLEXIFILE 10 THE SIMPLEST, MOST COST-EFFICIENT HIGH-SPEED PROGRAM LOADER MONEY CAN BUY

Flexibility in design. Flexibility in media. Flexibility in use. That's why our FlexiFile 10 flexible disk paper tape emulator offers you faster program

loading, quicker data access . . . less expensively. It's compact, portable, and plug compatible with most current readers and punches ... so you have greater field-loading capability, with no software changes required.

Utilizing its read/write capability, the FlexiFile 10 lets you upgrade from slow, hard-to-handle paper tape to high-density flexible disks. With its effective thruput rate of 1700 characters per second and its storage capacity of over 98K bytes per disk, the FlexiFile 10 enables you to transfer over 800

feet of paper tape data onto a single, removable flexible disk in less than one minute. And because each of the 32 tracks is individually selectable, you have access to more data, more easily.

The compact FlexiFile 10 is lightweight, too (just 18 lbs.). And it can be ordered with its own durable carrying case, so you can take it anywhere, for any program loading application. For high-speed loading of longer programs on computers or other peripherals. For quickly accessible, offline storage. For just about any fast, reliable field-programming function you require.

When you consider that you get all this program loading performance in a single, portable package for just \$1410,* it's easy to see why the FlexiFile 10 is the most cost-efficient, high-speed program loader money can buy. But you be the judge. Write today for our free product information package.

> *Single quantity price includes internal interface. Carrying case extra. OEM discounts are available.

stand alone or rackmount options are

FlexiFile 10 uses standard flexible disk media. including new flippy disks

FlexiFile 10 Paper Tape Emulator FlexiFie 10

CIRCLE 77 ON INQUIRY CARD







120 Vac at 1 A. Two lines function as single form A solid-state relays. The six remaining relays have one terminal common with the ac input (hot) line.

Analog input has 8-bit resolution, eight total inputs per card. Four inputs are 0 to 5 V, 0 to 20 mA, 0 to 50 mA (with each channel individually switch selectable), and four inputs 0 to 5 V only; or four inputs of 1 to 5 V, 4 to 20 mA, 10 to 50 mA (each channel individually switch selectable), and four inputs of 1 to 5 V only. Analog output is 0 to 10 Vdc or 4 to 20 mA (customer specified). Operating temperature limits are 0 to 120° F (-18 to 49°C). Power requirements are 120 Vac, 60 Hz, 100 W. Circle 175 on Inquiry Card

Inexpensive µComputer Hobby Kits Are High Performance Systems

The S6800 microprocessor kit offers personal computer builders a powerful naked system and custom design for system growth. The kits are also used as evaluation boards by OEMs of processing and manufacturing equipment. American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 offers three kits the EVK 99, 100, and 200—and an assembled version (300). All are packaged on $10.5 \times 12''$ (26.7 x 3 cm) PC boards with two 86-pin edge connectors, one for the microprocessing unit bus lines and one for I/O. Finished board thickness is approx 0.625'' (1.59 cm).

The CPU is the company's S6800 8-bit chip, with a $2-\mu s$ instruction execution time and memory access time of 575 ns maximum. Memory in the top-of-the-line 200 kit includes 2k bytes of dedicated ROM containing software pertinent to the system monitor, 1k bytes of RAM, and 2k bytes of EPROM.

System includes a programmer on the board for the S6834 512-byte (8-bit) EPROM. An adapter plug is available to program the S5204 EPROM. I/O consists of 48 lines through three parallel S6820 peripheral interface adapter chips and one S6850 asynchronous communications interface adapter. A 20-mA current loop and an RS-232 interface are available at the edge connector for serial or parallel interface peripherals. Baud rates, selectable by switch on the PC board, range from 0 to 9600. Interface bus and parallel I/O are TTL compatible.

The 200 kit provides four available interrupt vectors. Interrupt request, reset, and software interrupt are used by the board; the nonmaskable interrupt is for the user.

Three types of switch-selectable DMA are halt processor mode, cycle steal mode, and multiplex mode.

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Worldwide increases in both material and labor costs within the electro-mechanical industry have fostered a dangerous trend toward buying OEM components on the basis of price alone. But the fact is that the need for quality components has never been more critical. Loss of **your** product reliability for the sake of lower component costs can only result in substantially higher **life cycle costs** due to premature field failure. And that's a sure-fire way of increasing your product cost! That's struction result why most cost-conscious manufacturers SPECIFY escap[®] miniature dc servomotors. They know that the escap[®] line reflects the highest level of engineering skills and Swiss precision manufacturing... and the best performance-to-cost ratio available. struction result no cogging, sr efficiency, an volume ratio. T combination of our commutato sures high relifree operation. So, if reduced

escap[®] motors feature a permanent magnet stator and a selfsupporting skew wound ironless rotor. This unique low inertia con-

struction results in: fast response, no cogging, smooth torque, high efficiency, and high power-tovolume ratio. The use of a unique combination of precious metals in our commutator and brushes ensures high reliability and troublefree operation.

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Member of the Portescap Group 730 Fifth Avenue New York, New York 10019 Call for additional information and applications assistance: In New York: (212) 245-7715 In San Francisco: (415) 886-1618 Four kilobytes of software are allocated from addresses E800 and F7F for the system ROM.

Typical power supply requirements are 5 Vdc at 3.5 A and -12 V at 150 mA for EPROMs and RS-232 peripherals. For the p/ROM programmer, -50 Vdc at 40 mA are required, but only during p/ROM programming. A 1-MHz clock provides a 100- μ s and 1-ms timer.

Low end kit 99 consists of a PC board with two edge connectors, one MPU which can address up to 65k bytes of memory, four 128 x 8 RAMs, one peripheral interface adapter, one 2k x 8 ROM, and one asynchronous communications interface adapter. Board can be enhanced to include the interval timer, selectable DMA mode, restart address selection, variable speed or crystal controlled clock, and totally buffered MPU lines. Price is \$133.

The 100 kit contains the same parts plus enough TTL logic for simple communication with a terminal. Price is \$295. I/O interfaces, memory, a single EPROM device, onboard EPROM programmer, and a crystal clock are the additional features of the 200, which is priced at \$495. Available at \$765, a fully assembled and tested version, the 300, includes Tiny BASIC tape which may be programmed into the four EPROM chips.

Circle 176 on Inquiry Card

I/O Interface Controllers Provide Microcomputer System Support

A family of more than 100 I/O interface controllers are offered by General Automation, Inc, 1055 S East St, Anaheim, CA 92805 for use on their -16/220 and /330 16-bit microcomputers. Devices are packaged to plug into any I/O slot in the chassis of either microcomputer. This support supplies off-the-shelf controllers for many classes of peripheral, communications protocol, and analog or digital signals. The controllers themselves are supported with a powerful device-independent software package.

Family includes floppy discs, high performance moving arm discs to 300M bytes, head-per-track discs to 2M bytes, magnetic tape drives, line printers to 1250 lines/min, card readers to 1000 cards/min, teleprinters, character printers, paper tape readers and punches, plotters, keyboards, and CRTs.

For data acquisition and process control, a line of optically isolated input and output controllers for TTL digital signals, variable threshold dc or ac signals, and a family of A-D and D-A converters and multiplexers for analog signals is offered.

Available for communications is a full line of asynchronous and synchronous controllers, multiplexers, and line adapters to handle current loop, differential, RS-232, and SDLC protocols up to 2.5M baud. Circle 177 on Inquiry Card

Versatile Microprocessor Operates as Controller and Tutorial Card

Available in either tutorial or populated configurations, the 1000 card is an adaptable microprocessor designed with capability for full expansion, and for populating to a lesser degree for use as a controller. The tutorial form features the MOS Technology 6502 microprocessor chip; one page of RAM (256 bytes); 1-bit output latch; eight data, eight address, and nine control touch pads for data entry; eight data and eight address LEDs; and single-cycle operation.

In the fully populated form, the computer features full 16-bit addressing; 1k bytes of RAM (8 x 2111); sockets for 2k of UV ROM (2 x 2708) for use as a dedicated controller; MOS Technology 6530-004 teletypewriter I/O monitor (in ROM), 64 bytes of RAM, and an 8-bit I/O port; complete interface to teletypewriter current loop or EIA RS-232; high speed cassette interface using the MC6850 ACIA for storing programs; 6820/6520 PIA providing two 8-bit parallel I/O ports; fully buffered 3-state buses; power-on reset or restart; onboard address decoding for expansion; ribbon connector for I/O; and edge connector for expansion.

Model 1000 T, called the "tutorial board with a future," can be expanded from a completely self-contained learning tool to a powerful standalone controller or a standalone computer with 1k of RAM and 2k of EPROM, simply by adding chips to the board. A fully buffered bus on a 72-pin edge connector permits further expansion with the addition of other boards.

The fully expanded version, 1000 E, has the powerful TIM monitor which, when connected to a terminal via its RS-232, current loop, or TTL interface, allows complete control from the terminal over loading, running, and debugging programs. An onboard PIA chip provides interface to the outside world; a cassette interface for use with standard audio recorders is provided for offline program storage.

The board from Datac Engineering, PO Box 406, Southampton, PA 18966 includes a single-cycle function for learning machine operations as well as for debugging programs. A self-contained 5-V regulator operates from raw dc inputs. Circle 178 on Inquiry Card

Low Cost Single-Chip Microcomputer Is Compatible with the F8

Designed as a cost-effective solution to a wide range of control and logic replacement applications, the MK 3870 n-MOS single-chip microcomputer offers complete F8 software and hardware compatibility, 2k x 8 of mask programmable ROM, and a single 5-V power source requirement rated at $\pm 10\%$ tolerance. Fully compatible with the existing F8 multichip family and any standard TTL logic environment, the microcomputer can execute the complete F8 instruction set of more than 70 commands. Systems implemented with this microcomputer which eventually require more memory or I/O can simply upgrade to the expandable MK 3850 (F8 CPU) without major redesign or software development.

Features include 64 bytes of scratchpad RAM, a modulo "N" binary timer, multiple clock modes, four modes of vectored interrupts, and a versatile 4-MHz single-phase clock. Power dissipation is typically 300 mW.

Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 supports the microcomputer with a complete line of developmental tools—software de-



Our 100/200 megabyte OEM disk drives. Best for you. Best for your customers.

The new ISS 733-10/11 disk drives are the most advanced random access storage devices ever designed for the OEM market. With features that benefit you *and* your customers.

For example, exceptional speed in head positioning and start/stop times. Compactness. Quietness. Easy waist-high pack loading.

The big news, however, is their fieldupgrade capabilities. The 100-megabyte 733-10 can be easily field-upgraded to 200 megabytes. Or you can have 200 megabytes immediately with ISS 733-11. And both can be ordered with, or field-upgraded to, dual port.

Advanced interface design

Our interface permits functional compatibility between ISS 733-10/11 and most current 40, 80, 100, 150, 200, and 300-megabyte drives. This means minimal controller modifications, if any.

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Integral power supply. Tolerates wide power variations, reduces susceptibility to cycle sags and brown-outs.

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Data separation and write data

precompensation. All data encoding/ decoding is performed in the drive.

Absolute cylinder addressing. Disk addressing done in the drive, not the controller. Simplifies programming. Industry standard media. 3336-1 and

3336-11 or equivalent disk packs. Programmable sector mark. Allows user to

Rotational position sensing. Signals the system when the desired sector is approaching the read/write heads. Increases system throughput.

Daisy chaining. Greatly reduces cabling.

Important options

Dual port. ISS 733-10/11 can be upgraded from single to dual port in the field. Or dual port can be installed prior to delivery. Address mark format. Permits variable record lengths.

Round-the-clock ISS support

ISS maintains a complete support facility. Not just spares, but also technical assistance is available round-the-clock. Just call. We'll be glad to send more information about the ISS 733-10/11. Write or call ISS Marketing, 10435 N. Tantau Ave., Cupertino, CA 95014, (408) 257-6220. ISS is an operating unit of Sperry Univac.



Sperry Univac is a division of Sperry Rand Corporation



binary timer, 64 bytes of scratchpad RAM, four modes of vectored interrupts, and 4-MHz single-phase clock

velopment board (SBD-50/70), application interface module (AIM-70), and the Emulator-70 for field prototyping. SDB/AIM allows the user to create and edit source listings using the "resident text editor" and assemble into object code using the "resident assembler." The object code can then be copied to the interface module for listing.

Features available with this system include real-time execution of the target system code, breakpoint insertion, and single-step. Upon com-

Software Packages for Altair 8800 Meet Small Business Needs

Designed to provide software support for the Altair 8800 computer, the Altair Business System is a comprehensive set of software packages designed for the small business system market. System hardware may be individually configured for each installation and typically includes a CRT terminal, typewriter-quality precision printer, and one or more diskettes. pletion of software development and debugging, prototypes can be emulated for field testing and evaluation with the p/ROM-based Emulator-70. This allows exact verification of code prior to committing to mask programmed MK 3870s.

The single-chip microcomputer, which will be available in 40-pin plastic or ceramic DIPs during the first quarter of 1977, costs under \$10 for plastic devices in production (1000) quantities.

Circle 179 on Inquiry Card

The Altair Software Distribution Co, Suite 343, 3330 Peachtree Rd NE, Atlanta, GA 30326, a subsidiary of MITS, Inc, announced the system which includes complete software packages for accounting, word processing, and inventory management. Software is packaged in modules which allow the purchaser to select system components that most closely fit his needs.

The accounting package is comprised of four modules—general ledger (currently available), receivables, payables, and payroll (which will all be available during the first quarter of 1977). The word processing package (also available during the first quarter of 1977) is a flexible text editor system that allows large volume text material to be stored, edited, and printed. A flexible data base management system, the inventory management package allows a business to keep complete inventory records online.

Software may be licensed for use in individual packages to accommodate specific needs. Component packages are available under a one-time fee licensing arrangement which includes three years of software maintenance.

Circle 180 on Inquiry Card

Six Devices Added to Bipolar Microprocessor Family

Six device types have been added to the 2900 family of bipolar microprocessor components which are available from Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040. As with two previous parts, the devices are fabricated using the company's standard low power Schottky technology.

The Am2902 high speed lookahead carry generator is a 16-pin device which provides lookahead carries across a group of four Am2901 microprocessor ALUs with a typical propagation delay of 6 μ s. Three of the devices are open-collector quad bus transceivers-the Am2905, 2906, and 2907. Each features a quad D-type register on the driver side and a quad output latch on the receiver side for pipeline operation. Driver outputs can sink up to 100 mA at 0.8 V, while the receiver outputs sink up to 12 mA. The 24-pin 2905 and 2906 feature dual-driver inputs as opposed to the 20-pin 2907 which has only single-driver inputs. The difference between the two 24-pin devices is that the 2905 features 3state receiver capability, while the 2906 has odd-parity output. The 2907 features both.

Enabling reductions in both board space and cost, the Am2911 microprogram sequencer functions essentially the same as the 28-pin 2909 sequencer except that eight input lines are eliminated to accommodate its smaller 20-pin package. In the 2911, four direct inputs and register inputs are internally connected; the 2909 has eight separate pins for these signals. Four other pins are saved by eliminating the four on inputs.

The last device is the Am2918 quad D register which features two sets of outputs: four standard totem pole types and four 3-state types. These 16-pin devices can be used in microprocessor designs as address, status, and instruction registers.

All devices, available in both commercial and military versions, are currently provided in hermetic DIPs, with flat packs and plastic packages anticipated in the first quarter of 1977.

Circle 181 on Inquiry Card

Microprogram Assembler Assists Programming of 2900 Systems

A software system to generate microinstructions for use with the Am2900 (AMDASM) system has been developed by Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086, and is now available worldwide through Computer Science Corp's Infonet timesharing service. With AMDASM it is possible to microprogram all control signals and memory in order to reduce prototype and develop time for 2900 systems, and to reduce cost of writing microcode.

With the use of variable instruction set microprogramming, field service and enhancements to systems are easy; they require only additional data in the microprogram memory. Documentation for program changes is automatic.

The microprogram assembler provides software assistance and documentation for writing and modifying microprograms and generating tapes for p/ROM programmers. AMDASM includes a framework for a common language, automatic accounting information, and billing control. Budget limits, character rate options, and batch rates are claimed to make it cost competitive with in-house versions.

Circle 182 on Inquiry Card



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Another New Series of Microcomputer dedicated models from Power-One.

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dels designed to power	CP-205	1.7A	1A	0.5A	\$69.95	
ually any Floppy system	CP-206	3.4A	2.5A	0.5A	91.95	
the market today.	CP-162	6A	3A	0.6A	120.00	

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AROUND THE IC LOOP

Sample-and-Hold IC Interfaces to Nearly Any Logic Family

Combining bipolar and p-channel field-effect transistors on the same silicon chip through use of the company's BFET process results in a monolithic sample-and-hold IC with a speed of 6 μ s and accuracy within 0.01%. Basically, a circuit of this type is used in A-D conversion where it is desirable to make a measurement of a signal and to know precisely when the input signal corresponds to the results of the measurement. In some applications, it is also used to increase the duration of a signal.

The LF198 device has complete buffering for input and output and fully differential logic inputs, and can operate from a wide range of power supplies. Low current logic inputs will operate from TTL levels up to 15 V, permitting direct interface to nearly any logic family. Operating power supply range is ± 5 to ± 18 V.

Referring to the diagram, output buffer A_2 has p-channel FET inputs with typical input currents of 30 pA, giving a low droop rate while holding. Input amplifier A_1 has npn bipolar inputs for the lowest possible offset voltage and drift in the sample mode. In addition, A_1 is designed to have high common-mode rejection to achieve a gain accuracy of 0.002%. Input current is 20 nA, permitting use with high-impedance sources.

 R_1 and the two clamp diodes keep A_1 active during the hold mode. This keeps the input impedance high and eliminates the input loading problems encountered in other designs where the input impedance changes with sample or hold commands.

 A_3 is a differential logic comparator with a 1.2-V threshold. The differential capability allows the logic to be referenced to a separate ground from analog ground, minimizing noise. Either logic input can be driven, allowing the device to "hold" on either a high or a low logic signal.

Some other operational characteristics include offset voltage, 1 mV; input current, 20 nA; gain accuracy, 0.002%; hold step ($C_h = 0.01 \ \mu$ F), $0.5 \ mV$; input impedance, 20 G Ω ; power supply rejection, 100 dB; droop rate ($C_h = 0.01$) 3 mV/s; and input to output coupling (with 1000-pF hold capacitor), 0.1 pF. The LF198 is available from National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 in an 8-pin TO-5 package and is specified over the -55 to 125° C military temperature range; the LF298 and LF398 are rated over -25to 85° C and 0 to 70° C, respectively. Availability is from stock. When purchased in lots of 100, the LF398 sells for \$3.65 each.

Plug-In Memory System Expands PDP-11 Capacity

Any DEC PDP-11 computer can be provided with expanded memory capacity through use of plug-in memory systems from Motorola Semiconductor Products Inc, Integrated Circuits Div, 3501 Ed Bluestein Blvd, Austin, TX 78721.

The MMS1116 is a 16k-word x 16-bit system that plugs directly into the MM11-L memory slot of the computer and is both hardware- and software-compatible with it. Address and select changes are made via onboard DIP switches and jumper wires. 8k- and 12k-word versions are available for smaller memory expansion requirements.

Access time is 400 ns max, read cycle time is 460 ns max, and write cycle time is 500 ns max. Maximum active power requirement is 14.84 W; standby is 8.43 W. Short-circuit protection is provided on the board. Circle 350 on Inquiry Card

OFFSET INPUT INPUT

Static Buffer Memory Interfaces Systems With Different Data Rates

A universal Schottky-clamped 16word 5-bit TTL buffer memory, the SN74S225 interfaces directly between two digital systems or subsystems that operate at different data rates, such as keyboard-to-disc, CPU-tomemory, or peripherals. The static bipolar first in/first out memory, produced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222, has independent synchronous inputs and

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routining, absolute and relative vectors, ASCII keyboard and data desk is fine, but that's not enough. MEGATEK offers interactive devices such as data tablets and joysticks, floppy disc up through 10 Megabytes of dual disc storage, line printers and terminals, special interfaces, hard copy and more. Our mini can be expanded to 128K 16-bit words of memory.

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The Refreshing Alternative

14, rue de l'Ancien Port 1201 Geneva, Switzerland Telephone: (021) 32.97.20 Telex: 23343 outputs, dc to 10-MHz input or output data rates, 3-state data outputs, and two independent clock circuits.

Once stored, data are rippled through the memory by on-chip control logic. A separate clock permits outputting the stored data, as desired. Input and output clocks implement the basic buffer memory function. On-chip control logic provides status lines to indicate when the memory is full and when the output is ready.

The device is supplied in a high density 20-pin DIP with pin rows on 300-mil centers. In plastic with a temperature rating of from 0 to 70°C, the SN74S225N sells for \$4.50 in 100 quantities; in a ceramic package, the SN74S225J sells for \$5.63 in 100-piece quantities. Circle 351 on Inquiry Card

Up/Down Counter Has Infinite Rise/Fall Time

A synchronous, dual 3- or 6-decade up/down counter with all BCD data available in parallel, the LS7040 operates from dc to 350 kHz, is equipped with output latches, and provides a carry/borrow output for synchronous or asynchronous cascading with a like device. Its data format enables off-chip comparisons to be made with as many predetermined values as desired with a minimum of hardware.

Count input of the device made by LSI Computer Systems, Inc, 1235 Walt Whitman Rd, Melville, NY 11746 may have infinite rise and fall times. All inputs are CMOS-, TTL-, and DTL-compatible at 5-V operation and all I/O are CMOS-compatible over the entire voltage range. All inputs have CMOS-type noise immunity.

Other features include separate low current drain power supply for counter stages permitting battery standby operation, power-on-reset, and count enable inputs. The circuit can operate from either a single power supply between 5 and 15 Vdc, or from two supplies for battery standby operation, and is supplied in a 40-pin DIP.

Circle 352 on Inquiry Card

3-State Decoders Added To Schottky Family

Three 3-state decoders for use in bus-oriented systems have been added by Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086 to its proprietary low power Schottky family. All feature buffered common polarity control, which permits the outputs to be selected mutually exclusive active/low or active/high under control of the POL input.

The Am25LS2537, a 1-of-10 decoder/demultiplexer, accepts four active high BCD inputs and selects 1-of-10 mutually exclusive outputs. The Am25LS2538 is a 3-line to 8-line decoder/demultiplexer that has three buffered select inputs that are decoded to 1-of-8 outputs. The Am25LS2539 is a dual 2-line to 4-line decoder/demultiplexer with two buffered select inputs that are decoded to 1-of-4 outputs for each of the decoders.

All three circuits are available in molded and ceramic hermetic or ceramic flat 20-pin DIL packages. They meet all requirements of MIL-STD-883.

Circle 353 on Inquiry Card

Low Distortion Quad Oscillator Resistor Programmable to 20 kHz

A 0.002-Hz to 20-kHz precision quadrature oscillator (simultaneous sine and cosine outputs) is claimed to be the first to be resistor programmable over its entire range, the first to be offered in a DIP, and the first to include an uncommitted op amp; yet it is less than one-fifth the price of comparable units. The 14-pin DIP package occupies only 0.1 in³ compared to nearly 4 in³ for modular devices.

It is resistor programmable over its entire range, permitting the designer to meet varying needs with one device. The uncommitted op amp adds flexibility by providing a buffer, a level shifter, or an independent op amp.

Performance of the hybrid 4423 from Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734 is said to be comparable with that of more expensive, modular quadrature oscillators. Frequency stability is better than ± 100 ppm/°C and quadrature accuracy is better than $\pm 0.01\%$ °C. Sine output distortion is <0.2%, 0.002 Hz to 5 kHz, and <0.5%, 5 to 20 kHz.

The device, as supplied, can be used as a self-contained 20-kHz oscillator, requiring no external components and no adjustment. For the range of 2 to 20 kHz, only two external resistors are needed to program the oscillator frequency. From 0.002 Hz to 2 kHz, two resistors and two capacitors are needed to program the frequency.

Typical specs for the uncommitted op amp are 1.5-mV input offset voltage, 275-nA input bias current, 1-M Ω input impedance, 108-dB openloop gain, and 5-mA output current.

Prices are \$16.00 (1-24), \$12.00 (25-99), and \$9.85 (100-999). Delivery is stock to four weeks ARO. Circle 354 on Inquiry Card

Precision Decade Timer Counts in Seconds, Minutes, or Hours

The ICM 7045A, a CMOS precision decade timer with the oscillator, divider, and decoder drivers integrated on a single chip, is intended for use as a decimal timer. Selection of the oscillator frequency alone determines whether the timer is used for counting seconds (1.31072 MHz), minutes (2.184533 MHz), or hours (3.640889 MHz).

Introduced by Intersil, Inc, 10900 North Tantau Ave, Cupertino, CA 95014, the timer operates with a 3.6-V supply and is guaranteed to operate over a range of 2.5 to 4.5 V using nominal input and output tuning capacitances of 40 pF, depending on characteristics of crystals used. Output current drive is rated at 18 mA peak segment, with 12.5% duty cycle.

Prices for industrial-grade 28-pin epoxy DIPs rated for -20 to 70° C are \$29.75 for 1 to 24 pieces; \$23.80 for 25 to 99; and \$19.85 for 100 to 999. Delivery is from stock. Circle 355 on Inquiry Card
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3541

Compact TTY replacement. Solid-state uppercase keyboard. \$1200 purchase/\$52-mo. lease.*

3741

Upper/lower case typewriter style keyboard. Backspace TAB. \$1300 purchase/\$57-mo. lease.*

3841

Full cursor control, absolute X-Y addressing. Upper/lower case typewriter keyboard. Clear total screen, to end of line and screen. \$1450 purchase/\$63-mo. lease.



3931

APL and full ASCII character sets. Dual APL/ASCII keyboard. Overstrike Capability. High resolution 15-inch tube. \$2000 purchase/\$87-mo. lease.*

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CIRCLE 83 ON INQUIRY CARD

Telerav

Voltage Regulators Has Improved Current Levels

Easily adjustable over the range of 5 to 20 V, the 78HGKC hybrid voltage regulator subsystem provides a full 5 A of regulated power with built-in short-circuit and safe area protection. It offers all the advantages of a monolithic regulator at current levels that were previously unavailable.

Desired voltage rating of the device, introduced by Fairchild Camera and Instrument Corp, Analog Products Div, 464 Ellis St, Mountain View, CA 94042, is easily adjustable by means of two external resistors or by a single external potentiometer.

Hybrid circuit design limits maximum junction temperature of the power output transistor to provide full automatic thermal overload protection. If the safe operating area is ever exceeded, the device simply shuts down, rather than failing or damaging other components.

Circle 356 on Inquiry Card

Reference Books List U.S.S.R. Semiconductors

Current information on selected Soviet manufactured semiconductors is now available in three books published by D.A.T.A., Inc, of 45 U.S. Highway 46, Pine Brook, NJ 07058 under authorization by the Soviet Foreign Trade Organization. Electrical and physical parameters of the Soviet devices appear in several D.A.T.A.Book titles.

Featured in the Transistor D.A.T.A. Book are U.S.S.R. produced low power germanium and silicon transistors, field effect devices, and high power silicon type transistors. The Semiconductor Diode D.A.T.A.Book includes Soviet made switching diodes, rectifiers, and several categories of microwave types. References to U.S.S.R. produced light- and infraredemitting diodes and associated LED displays are found in the Optoelectronics D.A.T.A.Book.

In 1975, the U.S.S.R. exported approximately \$100 million in semiconductor devices to eastern and western European countries. Eastern Bloc countries use Soviet semiconductors in both industrial and military equipment. In 1976, the Soviets had a worldwide export goal of \$190 million. They claim competitive pricing in the international market place despite the U.S. import duty of 35 to 45% on Soviet manufactured electronic components and equipment.

Circle 357 on Inquiry Card

Matched Transistors Are Second Sourced

Its MAT-01 ultra-matched npn transistor pair can be directly substituted for the National LM114, LM114A, LM115, and LM115A; Analog Devices AD810, AD811, AD812, AD813, and AD818; and at least 17 standard "2N" numbers with greatly improved performance, according to Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050. Improvements of a factor of 10 or more in offset voltage, offset current, and temperature coefficients of offset voltage and current are claimed. Accuracy is achieved by using a thermally balanced IC layout with a triple passivation low noise process, rather than two discrete chips.

The device is available in four electrical grades in a 6-lead TO-78 can. All grades are specified and tested over the full -55 to 125°C temperature range. Parts processed and certified to Class B of MIL-STD-883A are also available. Circle 358 on Inquiry Card

Quad Op Amp Has Improved Ac Response

A quad operational amplifier, the RC/RM4156 features guaranteed minimums on slew rate and unitgain bandwidth. Circuit design retains the general-purpose capabilities of 741-type op amps (unity-gain stability, output short-circuit protection, low offsets), yet provides improved ac response over the audio range. Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040 designed and characterized this device specifically for use in active filter circuits.

Power supply drain is a max of ± 7 mA for the commercial units (RC) and ± 5 mA for the military unit (RM). Min slew rate is 1.3 $V/\mu s$, which provides a full-power response of 20 kHz. Min unity-gainbandwidth is 2.8 MHz. Input noise voltage is $<2 \mu$ Vrms over the audio band of 20 Hz to 20 kHz.

The 14-pin DIP is offered in either plastic or ceramic, with probed wafers or chips also available. It is produced in three temperature ranges: 0 to 70° C, -40 to 85° C, and -55 to 125°C. Circle 359 on Inquiry Card

SIL Resistor Packages **Permit High Density PC Board Mounting**

A series of low profile single inline packaged resistor networks, type 256C, have a maximum seated height of 0.250" (6.35 mm), permitting close mounting on PC boards. Announced by Sprague Electric Co, N Adams, MA 01247, the units are made up of seven resistors with one common terminal and are available in 72 standard values ranging from 50 Ω to 100 kΩ.

Circle 360 on Inquiry Card

NEW BURROUGHS' 480-CHARACTER GAS PLASMA DISPLAY:





Burroughs low-cost 40, 240 and 480 character SELF-SCAN[®] II panel displays can help you reduce the size and weight of your data terminals by more

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line is compatible with popular software.

Other significant advantages include direct digital address, easy interface to microprocessors, thin crosssection and rugged construction for long service life under all operating conditions. Give your data terminals a bright new

outlook; call or write for complete information. Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Plainfield, New Jersey 07061. Telephone (201) 757-5000. SELF-SCAN® displays are available nationwide through our distributors, Hamilton/Avnet and Cramer Electronics.





PRODUCT FEATURE

Complete Microcomputer Control System Develops and Debugs Programs Online in High Level Language



Procom II microcomputer system components (clockwise from bottom left): Procom II, CRT/keyboard terminal, dual mini-cartridge tape deck (top) and Composer, line printer, and RTP universal controller

Unquestionably, microcomputers have had a distinct influence upon today's technotronic society, particularly for industrial measurement and control. In theory they have solved many problems and been excellent elements for design engineers to incorporate into their systems. However, in practice the required programming can be so expensive as to negate the advantages of the low cost hardware unless the final design will be incorporated in a large number of systems where software costs can be spread out.

A microcomputer system introduced by Computer Products, Inc is aimed at systems designers developing small numbers (1 to 24) of identical control devices. Procom II is a complete microcomputer system including development and front-end subsystems. Primary use will be for real-time measurement and control applications in which the cost and power of a microcomputer can solve design problems—and for which designers will perform their own application engineering and programming with purchased subsystems. Programs can be both written and debugged online, interactively in a high level language.

Description

As a self-contained system, Procom II is made up of microcomputer, development subsystem, and input/output (I/O) subsystem for interfacing to sensor based signals. It operates

either in a standalone configuration or as a satellite to a larger host computer in a distributed concept. Its system software allows generation and checkout of an application program in an English-like language. After being written and debugged the program is stored with system software in programmable read-only memory (p/ROM).

The basic Procom II microcomputer is supplied in a rack-mountable package. It consists of an Intel 8080A-based microprocessor as CPU, memory, dual serial communication ports, and RTP I/O interface port. Memory can be divided into a mixture of up to 24k bytes each of p/ROM or random-access memory (RAM), depending on the nature of the program task, but to a total of not over 32k bytes. A typical system would use only 8k to 10k bytes of p/ROM and 4k to 8k bytes of RAM, allowing adequate room for expansion to a larger configuration.

Dual serial ports are included in anticipation of use for process operator I/O devices such as a teletypewriter or for connection to a host computer. The RTP I/O port is the main measurement and control interface and supports up to eight RTP controllers.

Specifically designed to provide the facilities needed to write and debug programs to be run on Procom II, the development system, called the Composer, is, in itself, a selfcontained microcomputer system. It includes an Intel 8080A-based microprocessor; 64k bytes of RAM; 24-line by 80-character, 12" CRT

epic data: simple, practical, flexible terminals and network controllers for data collection applications.

The EPIC DATA Model 1647 data collection terminals and 1648 system control units (SCUs) are designed to help the OEM quickly provide systems for such data collection applications as time and attendance recording, library circulation control, inventory reporting, access control, job costing and maintenance management. And to allow the OEM to market systems at prices considerably below those of competitors.

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flexible. Choose the terminal and options which best meet your application. EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

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Options. All terminals may optionally scan bar codes and magnetic stripes or accommodate through the RS232 ports other peripherals. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. A low-speed modem and serial asynchronous or synchronous communications ports with either RS232 or line driver I/O may be added. Both PROM and RAM memories are expandable.

SCUs. Each Series 1648 SCU polls up to 100 terminals, assembles transactions, formats data, appends time and date, and stores and forwards collected data to the host.

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CIRCLE 85 ON INQUIRY CARD

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terminal with keyboard; dual 3M minicartridge tape deck; 60-line/min printer; and automatic p/ROM programmer. It contains all peripherals and software required to compose, execute, and checkout real-time programs. Once a program development task is complete, the Composer is disconnected.

RTP measurement and control products provide the I/O interface to signals from various process sensors. These are standard products in the company line and eliminate the need for custom circuit design. Although a designer would choose the exact products to meet the requirements of his system, a typical RTP subsystem consists of a universal controller chassis and I/O cards.

Procom BASIC, the interpreter, is a totally interactive high level language for real-time applications that does not suffer the speed penalties imposed by classical interpreter design. The source language is highly compressed and pre-digested by the Composer for efficient high speed interpretation by Procom II, yet is always displayed to the user in his original form on the Composer CRT terminal. The resident system retains desirable real-time compiler features while affording advantages of an interactive interpreter during program development, debugging, and real-time operational checkout.

Debugging and Final Setup

All debugging is accomplished in both Composer and Procom II by working with the original Englishlike program statements. Any incorrect statements will be caught at program entry; program logic and process control logic may contain errors that will be discovered only during run time. However, the user never sees machine language or object code.

Debugging is performed concurrently by the Composer through its access to the shared memory and its control over Procom II. Any or all procedures can be used. For instance, entering a break command on the Composer allows the user to debug in short segments, checking operation of one segment at a time. Entering a trace command permits debugging at each statement that results in a program branch, or following execution of each program statement.

Dynamics of both process and program can be analyzed by an audit capability. This command allows the user to request a continuous display of selected variables based upon specific conditions while the application program is being run. The effect is to provide an instantaneous view of the selected variables. An expanded form of this command also debugs the intermittent glitches that can occur in real-time systems.

Any of the debug commands can be executed immediately upon entry from the keyboard. In addition, the user can write special analysis programs embodying those commands.

In the edit and correct procedures necessitated by the results of the debugging process, the user can recall program statements from memory, modify them selectively, and re-insert them. Statements can be cleared or inserted. Program changes are automatically checked for errors as they are entered and placed in their proper sequence. The program stops during insertion of corrected steps but can be started immediately after the changes are entered.

Once the program is debugged and system operation is thoroughly tested, a command entered at the keyboard causes the application program to be transferred to p/ROM. Chips are programmed in place without handling of individual chips. Another command results in comparison of p/ROM bit by bit with memory in the Composer.

The p/ROM resident application program is in permanent, non-destructive form. To effect future program changes, p/ROM is erased by using an ultraviolet eraser.

Price and Delivery

For a "typical" Procom II configuration with 8k p/ROM and 4k RAM, the price is \$2950. Costs of RTP units will vary dependent on the system chosen. The Composer sells for \$14,500 (or can be rented for \$145.00/month since many users will have only a one-time requirement). First deliveries will begin in May. After that, all deliveries will be 90 to 120 days ARO. Computer Products, Inc, 1400 NW 70th St, Ft Lauderdale, FL 33309. Tel: (305) 974-5500.

For additional information circle 199 on inquiry card.

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RAYMOND

Raycorder

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two sizes



Mini-Raycorder

With the advent of the microprocessor has come the need for even smaller tape transports — in test equipment, in desk-top calculators, in portable battery-operated terminals and in scores of other applications. Once again, Raymond is ready. The new Mini-Raycorder, completely compatible with the Information Terminals MI-50 MiniData Cassette and the proposed ANSI standard, brings to subminiature

recording the same standards of reliability and performance which have long been the hallmarks of the original Raycorder. Size: 3.0" x 3.0" x 1.8"

Weight: 16 ounces, including electronics Data Transfer Rate: 2,400 BPS Data Capacity: (single-track) 128K bytes

Complete specifications are available for the asking. Contact "Bud" Gould.

Raymond Engineering Inc.

A Subsidiary of Raymond Precision Industries Inc. 217 Smith Street, Middletown, Connecticut 06457 Phone: (203) 632-1000 Telex 9-8394

CIRCLE 86 ON INQUIRY CARD

PRODUCTS

Data Couplers Have FCC Registration for Communications Network Interface

FCC registration received for three data couplers allows individual data communications users to connect their terminals, modems, and like equipment to a switched telephone network via registered data access arrangements. It also permits EDP and computer equipment manufacturers to design the data couplers into their products. Model EDC 1000A, a manual device, isolates hazardous voltages, provides a longitudinal balance, provides automatic limiting on signal power, and provides a 2-way transmission path between modems and network. EDC 1001A, in addition, has interface control leads in accordance with EIA RS-232. It detects incoming ringing and features switch hook control and indicator, call delay timer, internal power supply, control lead for key telephone equipment, and capability for use with automatic calling unit. 1001D has contact type leads and no power supply. Elgin Electronics Inc, 802 Walnut St, Waterford, PA 16441.

Circle 200 on Inquiry Card





Printers Meet Special User Requirements

A 180-char/s, bidirectional, 132-col, logic seeking, serial printer, the model 703 is microprocessor-controlled and achieves throughput rates of from 90 to 375 lines/min. It has 15-in/s slew rate and can accommodate 6-part forms. Models 780 and 781 are smaller, 80-col, 60-char/s models for use in systems with space limitations. Throughput rates are 90 and 120 lines/min, respectively. They can produce 132-col forms by using the condensed print feature. The 781 prints bidirectionally and attains its throughput by logically seeking out the shortest path to the next line. Optional features include 5×7 , 7×7 , 7×9 , and 9×9 dot matrix printheads; choice of pinch roll, tractor feed, or pin feed platen; condensed print and single or full line character elongation; choice of 60 character sets; and mechanical and electronic VFU units. **Centronics Data Computer Corp**, Hudson NH 03051.

Circle 201 on Inquiry Card

Desktop Computer is Compatible with Tested Special Application Software

HP 9831A, a medium-priced desktop computer, can be used either as a standalone BASIC language machine or linked with peripherals to form a system. Its 8k bytes of internal read/write memory can be expanded to 32k bytes in 8k-byte increments and front slots are provided for four optional plug-in ROMs. A built-in bidirectional tape drive has an avg access time of 6 s, with 90-in/s search and rewind and 22-in/s read/write speeds. The computer can work with master and slave floppy discs for additional memory and can interface to plotters, printers, and CRT terminals. BASIC commands are built in for string variables, I/O, and advanced programming operations. Most tested software pacs available for the 9830 are compatible with this machine. Fixed- and floating-point formats can be set from the keyboard which has 12 special keys that can handle 24 different operations. Hewlett-Packard, Calculator Products Div, 1501 Page Mill Rd, Palo Alto, CA 94304. Circle 202 on Inquiry Card



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She smiles like that whenever they give her a lot of general data about only buying her peripherals from the mainframe manufacturer. But she's never decked by it because she knows about buying tape and disk systems. She knows that, at DATUM, she can get immediate delivery of controllers for a wider variety of peripherals... and save a lot of money, too.

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Datum also manufacturers cassette and rotating memories, data acquisition systems and timing instrumentation.

Peripheral Products Division

1363 S. State College Blvd., Anaheim, CA 928O6 • 714/533-6333 EUROPE: Datum House, Cranford Lane, Harlington, Middlesex, UK • O1-897-O456



PRODUCTS

FLOPPY DISC POWER SUPPLIES



Series of power supplies power almost all floppy disc memory systems available. All models have efficient open frame construction utilizing standard submodules for high reliability. Units have three outputs ± 5 Vdc at 3.0 A and any of the following ratings: 24 Vdc at 1.2, 2.4, 3.3, 4.8, or 7.2 A. Line and load regulation is 0.10%. Ripple/noise is 1 mV rms. All outputs are fully protected against overloads and short circuits. Overvoltage protection is optional. **Deltron, Inc,** Wissahickon Ave, North Wales, PA 19454. Circle 203 on Inquiry Card

SWITCHING RELAY

Modified to meet low cost, low level needs in simplified data acquisition systems, the D2A Multireed^R relay includes two Form A normally-open contacts. This configuration makes the relay suitable for applications where the Form C transfer mode or double-throw action of the std unit is not required. Other specs, identical to the std type D2C relay, include low noise generation, low thermal EMF, high speed, and reliability. **Thermosen, Inc.** 375 Fairfield Ave, Stamford, CT 06904. Circle 204 on Inquiry Card





Low cost time code generator/translator/ tape search unit features true automatic search along with simultaneous generation and translation of IRIG "B" serial modulated time code. Fully self-contained, model 544 includes controls and readouts for simple front panel operation and control. The desired mode of operation is selected; simultaneous operation of another mode may also be initiated. Std features include preset of time switches, reading data in forward or reverse, and error by-pass. **Moxon Inc**, 2222 Michelson Dr, Irvine, CA 92715. Circle 205 on Inquiry Card

TUBE-AXIAL FAN

Housed in a 1-piece zinc die casting, the TA600 cooling fan is claimed to offer superior (ft³/min)/W performance. Outside dimensions are 6.75 x 5.91" (17.15 x 15.01 cm); its axial depth is 1.5" (3.81 cm). The 5-bladed impeller is 1piece molded black thermoplastic polyester, meeting UL spec 94V-0. Integral motor is a permanent split capacitor type. Operating temp range is -40 to 60° C; normal life expectancy for nom indoor ambient conditions is at least 20 kh. The unit may be mounted directly from either face on 6.375" (16.19-cm) centers. Torin Corp. Torrington, CT 60790. Circle 206 on Inquiry Card

PROGRAMMABLE DATA TERMINAL



Allowing untrained personnel to use a complex computer system, the expanded, inline system 700/TS utilizes a full-scale 12-bit internal MOS LSI MSI processor. Up to 1920 chars can be shown on the 15" diag display area. Touch screen operation is performed via the "display surface wave reflection" process. Two rows of piezoelectric transducers are pulsed with a 4-MHz signal, propagating a wave front across the CRT faceplate. Megadata Computer and Communications Corp, 35 Orville Dr, Bohemia, NY 11716. Circle 207 on Inquiry Card

COMPUTER TERMINAL

Allowing 2-way computer data communication between a person and any RS-232 interface device, KDM/1 uses advanced semiconductor devices to provide reliable performance with digital computer systems, computer-controlled test equipment, and special-purpose devices. It combines, in a single compact unit, a full ASCII keyboard, 32-char alphanumeric LED display, ac power supply, and RS-232 interface. Display capacity up to 1920 char is optional. **Micon Industries**, 252 Oak St, Oakland, CA 94607.



Circle 208 on Inquiry Card

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

PC BOARD

PLATEN

PRINTER RIBBON



Downtime frays nerves. It costs money, too. But take heart. You'll see a lot less of it with a Printronix 300. That's assured by its elegantly simple mechanism based on a flat strip of spring steel with a hardened tip, pictured below. Forty-four springs, or hammers, are mounted to a hammer bank. Each is fastened at one end and normally held .retracted by a permanent magnet. (See the diagram.) A pulse of current thru a coil at the tip end of the hammer releases it to print a dot. The hammer bank is shuttled horizontally 0.3", enabling each hammer to cover the space between its tip and the tip of the next one, so that the total field covered is 132 columns. Aside from paper and ribbon feed, that is the only mechanical motion in the printer.

Since the Printronix 300 has 50% fewer components than mechanical font printers ... a head life 4 to 8 times longer than serial printers ... and never needs adjustments of hammer flight time or character alignment as drum/chain/belt printers do, you can see why it has a longer MTBF, and why we've felt comfortable offering a one-year warranty from the beginning.

> Send for our brochure. You'll discover why it produces 300 lpm print quality others can't match, has a shorter MTTR, and can give you full plotting capability . . . at no extra cost! Printronix, Inc., 17421 Derian, Irvine, CA 92714. (714) 549-8272.



PRINTRONIX 300 It's your best buy!

ACTUAL SIZE

CIRCLE 91 ON INQUIRY CARD



OPEN FRAME POWER SUPPLIES



Supplies that maintain regulation at 0.1%; hold ripple to 2 mV rms max, 20 mV pkpk max; and return output voltage to within regulation limits within 50 μ s in response to a 50% load step, have been added to the EC line. Single output EC5N40 provides a 5-V, 40-A output for for driving large TTL arrays. Triple output ET 301 and 302 offer outputs of 5 V at 3 A and ± 12 V at 0.5 A and ± 15 V, 0.5 Å, respectively. All units operate off 105 to 125 or 210/250 Vac inputs, 47 to 63 Hz. ACDC Electronics, 401 Jones Rd, Oceanside, CA 92054. Circle 209 on Inquiry Card

COMPACT S/D CONVERTER

Short enough to fit in one slot of a std $\frac{1}{2}$ " (1.27 cm) card cage, the SD402 offers 12-bit resolution at a 10-bit price, and works off a single 5-V power supply. It features an accuracy of ± 15 arc-min, and a tracking rate of 10,800 deg/s. Either 3-wire synchro plus reference, or resolver plus reference input signals are accepted. Reference frequency is 400 Hz; reference and stator inputs are transformer isolated. Unit is insensitive to line variations of voltage and frequency of up to 15%. Natel Engineering Co, Inc, 8954 Mason Ave, Canoga Park, CA 91306. Circle 210 on Inquiry Card

MINIATURE TOGGLE/ PUSHBUTTON SWITCH KIT

A 286-piece kit of switches gives engineers a complete selection for use in designing circuits and systems. Kit comprises 1-, 2-, 3-, and 4-pole switches with a variety of toggle and pushbutton actuators. The inside top cover of the case contains a chart showing how to specify the type of pole configuration, switching function, actuator and terminal style, contact material, bushing, finish, mounting nut, and cap desired. All switches are rated 6 A at 125 Vac and come with solid silver contacts. **Oak Industries Inc, Switch Div**, Crystal Lake, IL 60014.

Circle 211 on Inquiry Card



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9700-В PALMER HWY. ● LANHAM, MARYLAND 20801 USA (301) 459-2100 ● TELEX 89-8327

Performance Value

JOYSTICK CONSOLE



Including a speaker and amplifier in the same housing with the 2-axis joystick, the console can be used to provide sound effects for computer and other games, or to supply acoustic warnings. Four pushbutton switches on the console can be used for cursor positioning on a color graphics terminal where they can select desired colors. A 7-channel analog-to-digital I/O card directly interfaces two of the consoles to microcomputers. **Cromemco**, **Inc**, 2432 Charleston Rd, Mountain View, CA 94043.

Circle 212 on Inquiry Card

LARGE DIGITIZER

A 42 x 60" (106.7 x 152.4 cm) intelligent digitizer, with an accuracy of ± 0.004 ± 1 LSB, model ID-60 is a microprocessorbased unit. It offers firmware features for calculating area and perimeter, and for performing scaling and skew correction. resolution is 100 or 200 lines/in (40 or 80/cm). Available interfaces include RS-232, TTY, DEC PDP-11. Data General Nova, Hewlett-Packard 9800 series calculators, IBM 029 keypunch, and others. **Summagraphics Corp**, Box 781, Fairfield, CT 06430.

Circle 213 on Inquiry Card

PLOTTER CONTROLLER



The microprocessor-based 50 series of plotter controllers, using Graphic Machine Language (GML) software, are utilized with the company's high speed 12" (30.48 cm) or 36" (91.44 cm) plotter to provide a drum plotter system. GML relative vector commands provide for transmission of only significant digits; GML annotation vectors offer 128 chars which may be plotted at virtually every size and angle. Plotter speed is up to 3000 steps/s [7.5 in/s (19 cm/s) axially]. Zeta Research, div of Nicolet Instrument Corp, 1043 Stuart St, Lafayette, CA 94549. Circle 214 on Inquiry Card

CIRCLE 90 ON INQUIRY CARD



Very little stands between your mini and the disk drives of your choice.

Just Telefile's little Matchmaker disk controller. With it, we can put your minicomputer together with *any* of the latest 3330-type disk drives: Ampex, Memorex, CalComp, Control Data, or Diablo. You'll have a system no one else can match. **Greater flexibility.**

Special tailor-made, compatible interface modules make changing minicomputers a snap.

To change drives, simply switch circuit boards. Capacity can grow from 13.3 million to 1.2 *billion* bytes per system.

Interface software included.

Telefile even provides handlers

that make the Matchmaker software transparent to the operating systems of most major minicomputers. **Unmatched features.**

Telefile's Matchmaker controller brings to minicomputer users the latest large mainframe disk technology with such features as: Search and read command to help you with data base management. Write protection to the sector level. And Advanced error recovery techniques.

The Matchmaker even comes with a separate maintenance module for offline disk pack formatting and test exercising.

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100 fact-filled pages on the universal Matchmaker concept including operation, functional specs, features, diagnostics, installation, and maintenance. Get it free by writing: Telefile Computer Products, Inc., 17131 Daimler St., Irvine, CA 92714. Or call toll-free (800) 854-3128. In Calif., (714) 557-6660.





ELECTRONIC DISCHARGE PRINTER



The high speed model DC4004A has 48col capacity for hardcopy recording applications. It prints all letters of the alphabet, digits 0 through 9, and a variety of symbols at 3 lines (144 char)/s. $5 \ge 7$ or 7 ≥ 9 dot matrix characters are printed by current passing from the electrodes in the printhead to a std 4.75" (12.06 cm) wide roll of aluminum coated paper. The current exposes the characters on a high contrasting, permanent black undercoat. 9-dot writing allows full use of the $5 \ge 7$ ASCII set or other special symbols. **Hycom, Inc,** 16841 Armstrong Ave, Irvine, CA 92714.

Circle 215 on Inquiry Card

TEST GENERATION STATION

Enabling users to assemble, edit, and debug logic board test programs online using a modified 500-series tester and a std teletypewriter, the 550 uses the same mainframe and PCB assemblies as the tester and provides all testing functions. Programs can be developed offline by another 550, a 600-series programming station, or the user's own computer. A builtin computer allows users to prepare new test programs or modify existing programs without use of computer time. **Mirco Systems Inc**, 2106 W Peoria Ave, Phoenix, AZ 85029.

Circle 216 on Inquiry Card

REMOTE PRINTER ADAPTER

The printer communications adapter (PCA) option accepts voice-grade telecommunications between a system 99 CPU and a remote printer, providing complete forms handling capability. It can be used in conjunction with a remote video terminal and a remote printer which share a single modem and a single communication line, or alone with a remote printer. All data accepted by the PCA are buffered and sent in parallel form. Device handles full-duplex, serial asynchronous data at rates up to 1200 baud. **GRI Computer Corp**, 870 Georges Rd, North Brunswick, NJ 08902.

Circle 217 on Inquiry Card

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DISKETTE STORAGE SYSTEM



DataMaster II is a flexible disc I/O data recorder and editing system intended for plug-compatible attachment between ASCH printer/display terminals and their RS-232 modems. As a result of access speed and powerful text editor, the system in effect adds 311k chars to "working storage." Features include random access to any of 2k 128-char records in 0.3 s avg, and search command to initiate a scan for data or file locaters of up to 128 chars in length at a speed of 12 s/disc avg. Western Telematic Inc, 3001 Red Hill, Bldg 5-107, Costa Mesa, CA 92626.

Circle 218 on Inquiry Card

SOLID-STATE RELAYS

Series of relays with an ac control signal is designed with a built-in current transformer so that no external shunt is required for sensing currents as high as 20 A rms. They allow solid-state zero voltage switching of motor start windings with no additional circuitry. Relays are available in 120-, 240-, 480-, and 600-V ratings with ac and dc voltage control. Std line of the company's SSRs can be supplied with this ac control. **Opto 22**, 5842 Research Dr, Huntington Beach, CA 92649. Circle 219 on Inquiry Card

SMALL CODED DIP SWITCH



"Micro-Dip," a 10-position coded switch, occupies one-half of a 14-pin DIP socket and can be mounted/connected directly to circuit boards by hand or flow soldering. Switch settings can be made in either direction with a screwdriver; numbers on top indicate detent positions. The device can handle loads up to 100 mA at 5 Vdc and operate in a temperature range of -10 to 60°C. Contacts are gold-plated. Codes include BCD, with BCD-complement, 1- or 2-pole 2-throw and 1-pole 5position repeating in design. **EECO**, 1441 E Chestnut Ave, Santa Ana, CA 92701. Circle 220 on Inquiry Card

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–June 7–9

3 Circle those dates on your business calendar. Then show up and register! As a qualified professional, that's all you need to do to take part in the varied exhibits, demonstrations and exhibitor seminars.

- SEE: Live Demonstrations and Displays of new computer products and services, including Minicomputers, Printers, Microcomputers, Microprocessors, Printer Terminals, ROM's and RAM's, Flexible Disk Drives, Power Supplies, Keyboards, Modems, Readouts and Displays, Cassette Systems, Magnetic Tape Transports, Core Memories, Graphics Systems, Miniperipherals, Small Business Computers, Software, Data Communications Equipment, and much more! Every day from 10 AM to 5 PM.
- VISIT: Free Exhibitor Seminars covering the selection and use of these products and services. These free seminars will be held every day.

ENROLL: Designer Forums * will be conducted in five cities by leading designers and independent experts. Topics are Evaluating and Using Microprocessors (Tuesday) • Evaluating Peripherals for Mini- or Microcomputers (Wednesday) • Evaluating Memory and Storage Devices (Thursday) • (Designer Forums are scheduled in San Francisco, Los Angeles, Chicago, New York and Boston.)

NOTE: Case Study User Forums* are scheduled in all nine cities. Topics are: Applying Minicomputers (Tuesday) • Managing Terminal Networks (Wednesday) • Improving Software Productivity (Thursday)

* The Forums are held in conjunction with COMPUTER EXPO and require separate registration and fees. They are held each day from 9 AM to 1 PM. One day's admission fee is only \$45; additional days are \$35. Advance registration is recommended. Call (800) 225-3080 to reserve your space and get complete registration materials.

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INTELLIGENT SYSTEMS PRINTER



A programmable printer for data-recording applications provides print speed of 1.25 lines/s with 40 alphanumeric char/31/3" (8.46 cm) line and 3-copy capability, with optional automatic take-up for duplicate copy. Char height is 0.122" (0.31 cm). User-definable program options include printed format and interface variations, alarm setpoints, and engineering computations. Six card slots are available for system expansion. Hardware options include display, keyboard, A-D, D-A, V-F, and F-V conversions, clock/calendar/timer, and data memory with battery backup. Automation Designs, Inc, PO Box 281, Sebastopol, CA 95472. Circle 221 on Inquiry Card

OPTICALLY ISOLATED SOLID-STATE RELAY

Units feature TTL-compatible inputs, no contact bounce, DIL packaging, no moving parts, and solid-state speed and reliability. They have 1500-Vac I/O isolation over an operating range of -55 to 100°C. Model 750-A typically delivers 0.5-A dc load current with control current of 15 mA at 2.7 Vdc. Off-state breakdown voltage across the output is >60 Vdc. Hybrid thick film technology insures an I/O isolation resistance of $>10^{10}\Omega$. International Sensor Systems, Inc, PO Box 345, Aurora, NE 68818. Circle 222 on Inquiry Card

MICROPROCESSOR-BASED MULTIPLEXER

A time-division multiplexer that accommodates up to 16 asynchronous or synchronous digital data channels or any mixture of both types, M1318 MultitranTM can be used in point-to-point multiplexing between terminal clusters and central computers and is fully compatible with the company's M3200 network switching and management system. The device supports mixes of remote job entry terminals, synchronous video terminal controllers, and interactive asynchronous terminals over a single voice-grade telephone line. Computer Transmission Corp, 2352 Utah Ave, El Segundo, CA 90245. Circle 223 on Inquiry Card

ANALOG/HYBRID TEST SYSTEMS

Adding capability for automatic analog and hybrid circuit board testing to the CAPABLE 4000 series of computer-controlled test systems, model 4707 is a generalpurpose combination of hardware and software options in one add-on package. The package consists of an IEEE-compatible bus for interfacing analog instrumentation; a 4- or 5-bus by 32-pin switching matrix module; an instrumentation matrix (connecting up to 10 instruments to the analog bus); and software to control applying analog stimulus and performing analog measurement. Computer Automation, Industrial Products Div, 18651 Von Karman, Irvine, CA 92713. Circle 224 on Inquiry Card

PROPORTIONAL **DC/DC POWER SUPPLIES**

Series H dc/dc high voltage power supplies come in several output voltages (dc), load currents, and input currents (at 12 Vdc). They are small size (90 g), low cost devices. Supplies drive PMTs and other HV circuits and devices. Specs include input voltage of 4 to 12 Vdc, isolation of 3500 V (input to output), efficiency of 60% typ, and encapsulation of 100%. Mounting is accomplished with two through holes using PC pins as terminals. Wall Industries, Inc, 175 Middlesex Tpk, Bedford, MA 01730.

Circle 225 on Inquiry Card

1702A MANUAL EPROM PROGRAMMER

Features hex keypad, two digit hex address and two digit hex data display. Controls include load, clear, go! (step), key/copy, data in/ data out, and counter up/ down. Profile card includes high voltage pulse regulator, timing, 8 bit address and 8



bit data drivers/receivers. Two 61/2" x 9" stacked cards with spacers. Allows programming in 20 minutes - copying in 5 minutes. Requires +5, -9, and +80 volts. \$299.95

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IMSAI/ALTAIR computer interface (requires 3 output ports, +1 input port) and software \$49.95 Briefcase unit with power supplies and interface connectors (assembled and tested only) \$599.95

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- 111: MICROPROCESSOR PROJECT MANAGEMENT: Design, Manufacturing, QA and Field Service (220 pages/ 5 hours)
- 102: MICROPROCESSORS/MICROCOMPUTERS: A Comprehensive Technical Introduction and Survey (420 pages/9 hours)
- 156: SOFTWARE DEVELOPMENT: TOOLS AND TECH-NIQUES FOR MICROCOMPUTERS (320 pages/9 hours)
- 187: BIT-SLICE MICROPROCESSORS, PLA'S AND MICRO-PROGRAMMING (310 pages/9 hours)
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This new ICS Hands-On Training System is the first and only HARDWARE/SOFTWARE SELF-STUDY COURSE. The ICS Training System includes a fully-assembled 8080 microcomputer and built-in educational monitor program together with a coor-Jinated 400-page workbook/text. The System is ready to use in your office or home (with its built-in keyboard/display, no expensive teletype or CRT terminal is required)! You will learn the details of both programming and interfacing by actually per forming scores of exercises on your own microcomputer - at your own pace, in your office or at home.



The Training Computer itself includes: the 8080 microprocessor, .5K CMOS RAM, 1K PROM, three parallel I/O ports, two serial ports, one DMA channel, and the on-board 8-digit display and 25-key keyboard.

The ICS Monitor program is stored in the PROM memory and is specifically designed to be easy to use. It provides many unique functions essential to efficient learning. Furthermore, many monitor routines are available for use in your own programs, including display and keyboard I/O, timing, cassette interfaces, etc.

Using the ICS Training System, you will first learn each 8080 instruction through simple exercises which illustrate its effective use. These exercises, which also teach you basic programming, then progress to more and more advanced techniques. Other exercises specifically teach how to debug your programs quickly and effectively. Furthermore, throughout the course, hardware interface design and implementation projects are coordinated with programming problems. (For example, as your first project you will build a simple interface to an audio-cassette recorder.) Thus, you will learn both hardware and software design techniques and how to make HW/SW tradeoffs by actual hands-on

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TO ORDER Please Write:



Integrated Computer Systems, Inc. Self-Study Training Dept. 4445 Overland Avenue Culver City, Calif. 90230

Or Call: (213) 559-9265

Please Contact: Integrated Computer Systems, Inc. Boulevard Louis Schmidt 84, Bte 6 B-1040 Brussels, Belgium (02) 735 6003



ACOUSTIC COUPLER



The dual 300- and 1200-baud acoustic coupler, intended for use with remote data entry and retrieval systems, allows a terminal to be used with a single coupler at data rates of 110, 150, 300, 600, and 1200 baud. 103/202 protocol is readily accessable via an external switch. Bell-compatible 5-baud reverse channel is std with the unit; 150-baud FSK is optional. "The Switchable" is completely field programmable. Std RS-232-C digital interface is provided for transparency with all data terminals. **Omnitec Data Corp**, 2405 S 20th St, Phoenix, AZ 85034. **Circle 226 on Inquiry Card**

MATRIX PRINTER

Model 3510 is a 300-line/min matrix printer with a std 96-char u/lc capability for use where large volumes of forms and reports are required or graph-plotting capability is needed. Features include simplified operating controls, including a switch for selecting either 6 or 8 lines/in. Double height characters can be produced for report titles on forms up to 16" (40.6 cm) wide. The unit has few moving parts and seldom requires mechanical adjustments. An enclosure reduces noise, and a paper stacker gathers printed documents. **Basic/Four Corp**, PO Box C19550, Irvine, CA 92713.

Circle 227 on Inquiry Card

PHOTOHEADS

Compact solid-state series RPX photoheads measure $3.938 \times 3 \times 1.063''$ (10.003 x 7.62 x 2.70 cm) and have a Nema 12 rating. Std unit can focus at 10 ft (3 m) to a 4'' (10 cm) spot, not affected by normal ambient light because of a pulsed LED source. Effective range is up to >20 ft (6 m). Using a controller, unit responds to light interruption within 0.05 s. Model RPX is easily modified. Devices are available with or without controller, and with controller built in as an integrated unit. **Photobell Co, Inc,** 12 E 22nd St, New York, NY 10010.

Circle 228 on Inquiry Card



MICROPROGRAMMABLE VIDEO DISPLAY TERMINAL



The 4050 is a standalone display terminal designed for multidrop data communications networks that incorporate Burroughs, Honeywell, Univac, or other computers. The terminal can interconnect many terminals on the same communications line to a central computer for random or sequential polling. Display features include a 14" (35.6 cm) diag screen with 80 columns x 25 lines of u/lc chars, full- or half-duplex, synchronous or asynchronous data transmission at rates up to 9600 baud, and an online printing feature. Delta Data Systems Corp, Woodhaven Industrial Park, Cornwells Heights, PA 19020. Circle 229 on Inquiry Card

DIP OSCILLATOR

Model ZY-7410 provides an ECL-compatible output at any customer-specified frequency in the range of 25 to 100 MHz. Its crystal controlled output provides $\pm 0.005\%$ over an operating temperature range of 0 to 70°C. Self-contained in an all metal package measuring 0.87 x 0.50 x 0.36" (2.21 x 1.27 x 0.91 cm), the device plugs into a standard 14-pin DIP socket and operates from -5.2 Vdc. Greenray Industries, Inc, 840 W Church Rd, Mechanicsburg, PA 17055. Circle 230 on Inquiry Card

PRIVATE LINE TEST SYSTEM



For testing private lines and toll circuits in small rural and suburban offices, the 1400 requires 7" (18 cm) of rack space to perform primary tests on 2-, 4-, and 6wire circuits, in addition to accessing, communicating, signaling, and supervising. It can be expanded to 12.25" (31.12 cm) to include a transmission measuring set, a 1911 signal test set, or a cord reel, writing shelf, and jackfield. Available are five communications, two signaling, two supervision, an access, and primary test modules. **ADC Telecommunications, a div of Magnetic Controls Co,** 4900 W 78th St, Minneapolis, MN 55435. **Circle 231 on Inquiry Card**

The '77 National Computer Conference: a unique learning experience

For the individual with a need to know, the 1977 National Computer Conference, June 13-16 in Dallas, offers a wealth of information on computer technology and data processing applications. It's all available at one time, in one place — a recordbreaking exhibit of more than 1,100 booths; an extensive conference program covering the latest in technology, cost-effective computer usage, management concerns, and public policy issues.

You can also select from a wide range of special conference features, including eleven professional seminars on topics of critical importance to EDP management and technical specialists; indepth coverage of microprocessor technology and personal computing; plus a series of featured addresses by such leading authorities as Mark Shepherd, Jr., chairman of Texas Instruments Incorporated, and AFIPS president Dr. Theodore J. Williams. It all adds up to a unique learning experience keyed to your professional activities and career development.

At the '77 NCC exhibits, you'll obtain firsthand information on the latest hardware, software, systems, and services offered by more than 250 organizations, with industry representatives and technical experts on hand to assist you in meeting your data processing needs.

The conference program will include more than 300 presentations by leading experts designed to educate, stimulate, and promote the exchange of views among computer specialists, EDP managers, corporate executives, users, educators, and government officials. In addition, each of the professional seminars will provide an indepth, full-day presentation conducted by a nationally recognized authority on topics ranging from distributed database networks to long-range planning.

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PRODUCTS

DIGITAL RASTER GRAPHICS DISPLAY SYSTEM

A 1024 x 1024 display system, the GCT-1024 has ultra-high resolution to take the "stair-step" appearance out of raster displays to minimize distortion and provide greater density detail. The system includes a proprietary discrete microprocessor that provides instruction times as fast as 150 ns and 51 mnemonic instructions for increased user programming flexibility. Options include a table-mount "joystick" assembly, 64-function keyboard units, and graphic tablets and cursors. Genisco Computers, a div of Genisco Technology Corp, 17805-D Sky Park Circle Dr, Irvine, CA 92714.

Circle 232 on Inquiry Card

RF PROBE



Converting dc voltmeters into high frequency ac voltmeters by producing a dc output voltage equal to the rms value of a sine wave input, P6420 rf probe measures ac voltage from 10 kHz to 1 GHz. Designed to be used with digital multimeters which have $10-M\Omega$ inputs, the device is compatible with the company's DM 44, DM 501, DM 502, and 7D12/M1. When used with oscilloscopes with $1-M\Omega$ inputs and instruments with input resistance other than 10 M Ω , the dc reading will be directly proportional to the sine wave input but not equal to the rms value. Tektronix, Inc, PO Box 500, Beaverton, OR 97077. Circle 233 on Inquiry Card

SOLDER-TO-BOARD CONNECTOR

A PCB connector for the mass termination of "Quickie" round-conductor flat cable in solder-to-board applications, before or after wave-soldering, is available in gold or solder plating. It is available in 10, 20, 26, 34, 40, or 50 contact configurations. Connectors are supplied in through covers (suitable for daisy-chain applications). The askewed tines of the contact in the connector enhance the device's insulationstripping action. Berg Electronics Div, Du Pont Co, Interstate 83, New Cumberland, PA 17070. Circle 234 on Inquiry Card

GPIB/RS-232-C ADAPTER



Housed as a separate systems component, the model 111 adapter permits the use of any existing serially-communicating EIA RS-232-C terminal, instrument, or other digital device with control systems utilizing the parallel format of the IEEE 488-1975 general-purpose interface bus. Allowing for 2-way transmission of data, the device can be used to adapt older instruments and terminals which have been designed to RS-232-C standards to control and processing systems using the GPIB parallel format. Systems Consultants, Inc, 410 Jericho Tpk, Jericho, NY 11753. Circle 235 on Inquiry Card

PROGRAMMABLE SONIC DIGITIZER

Model NT-501 automatically performs mathematical functions which previously required hand calculation or external data processing equipment. Only two point sensors are required above the work area, allowing interaction with a variety of inputs. Points on the plane to be digitized, which can measure up to 36 x 48" (91.4 x 121.9 cm), are located by triangulation. Digitizer converts triangular coordinates into Cartesian (X,Y) coordinates when desired. Science Accessories Corp, 970 Kings Highway W, Southport, CT 06490. Circle 236 on Inquiry Card

RECTANGULAR INDICATOR LIGHT



Redesigned 3100 rectangular indicator features a nonconducting molded plastic bezel with snap-in ears for mounting in a std 1.281 x 0.395" (3.254 x 1.003 cm) hole. Panels 0.062 to 0.100" (0.157 to 0.254 cm) thick can be accommodated. Series is available with wire leads or 0.250" (0.635 cm) tab terminals. High voltage (125 to 250 V) neon or low voltage incandescent lamps are supplied. Units are UL listed. Red, green, amber, or white lens colors are std. Leecraft Manufacturing Co, Inc, 21-16 44th Rd, Long Island City, NY 11101. Circle 237 on Inquiry Card

PC CONNECTOR SERIES

High density, 2-piece metal-to-metal connector series 8223 includes a longer contact length for applications requiring 3/32" (0.24 cm) or 1/8" (0.32 cm) PC cards. Connectors are qualified to MIL-C-55302 in its entirety with Mil plating. With 0.100" (0.254 cm) contact spacing, the device is available with 24 to 96 contacts in a variety of sizes with 17 different terminations. The hermaphroditic VariconTM contacts are spring-loaded and interlocking to assure low contact resistance, high current capacity, and a positive gas-tight connection. Elco Corp, a Gulf + Western Mfg Co, 2250 Park Pl, El Segundo, CA 90245.

Circle 238 on Inquiry Card

VIDEO DISPLAY TERMINAL



Highly visible 12" (30.48 cm) monitor and hardcopy capability are features of the IQ 120 remote display terminal. Basic unit offers switch-selectable transmission rates from 110 to 19,200 bits/s, cursor control, current loop interface, addressable cursor, and erase mode. CRT format is 12 lines of display (24 lines optional) at 80 char/line. Total page memory is 160 chars with an optional 1920-char capability. Expansion options include formatting, and u/lc chars. **SOROC Technology, Inc**, 3074 E Miraloma Ave, Anaheim, CA 92806. Circle 239 on Inquiry Card

ULTRA LOW PROFILE KEYBOARDS

In single-pole or Touch $Tone^{TM}$ encoding, models FF and FR, claimed to be the thinnest keyboards available, are made by laminating folded, 1-piece flexible circuits and key legends. Both have 12 or 16 keys in calculator or Touch Tone format. FF has a slight movement of the key pad which closes an electrical circuit; FR uses



the company's patented "bubble" to provide key travel and tactile feedback. Contact rating is 20 mA at 30 V. Keyboards' life span is 10M operations. Chomerics, Inc, 77 Dragon Ct, Woburn, MA 01801. Circle 240 on Inquiry Card

FLEXIBLE DISC UNIT



Available in single- or dual-drive configurations, model 7500 Dynaterm flexible disc unit is compatible with industry std dual cassette units, and features asynchronous serial interface communications (RS-232-C) with terminal and line ports. Variable length records and all but two codes of the 128 ASCII character set may be stored. Units operate locally with any ASCII terminal or online with terminal or host computer providing control codes. **Bedford Computer Systems, Inc,** 3 Preston Ct, Bedford, MA 01730. Circle 241 on Inquiry Card

TAPE DATA TRANSMISSION SYSTEM

Series 7300 offline system provides for high speed transmission of IBM-compatible digital mag tape data via DDD, WATS, leased or private line links. It is fully compatible with terrestrial and satellite channels provided by domestic and international common carriers. All formatting, error protocol, modem signaling, and tape transport control is directed by a single chip LSI microprocessor. Tape transport can connect to many data terminals via an EIA RS-232-C compatible I/O port. **Quad Systems, Inc,** 11900 Parklawn Dr, Rockville, MD 20852.

Circle 242 on Inquiry Card

DUAL POWER SUPPLIES

This short-circuit protected series, noted for high performance and low cost, is designated P34C and P34C-12, delivering ± 15 and ± 12 Vdc at 200 mA, respectively. Epoxy encapsulated modules are constructed to isolate heat sensitive from heat generating components. Series can be supplied with fixed voltage from ± 5 to ± 24 Vdc and is available in both chassis and PC mounting. Other features include input, 105 to 125 Vac; ripple and noise, 1.0 mV rms; line regulation, 0.05%; and load regulation, 0.1%. **Polytron Devices, Inc,** PO Box 398, River St Station, Paterson, NJ 07524.

Circle 243 on Inquiry Card

DOUBLE DENSITY FLOPPY OS for HP21MX, RTE-II

... also OS/8, RT-11, RDOS, DOS, OS 16MT2, CP/M, RSX 11M, IRIS and many more. AED's new 6200 Series double-density diskette systems allow random access storage at a fraction of the cost of big disks. And in addition to DEC, DG and Interdata operating systems, the AED 6200 now operates as LU#2 or LU#3 under HP RTE-II, with a driver from AED that will run all RTE-II functions. This versatile MFM subsystem maintains the RTE-II on a single drive, allowing the other drives to be used for auxiliary storage or peripheral disks. AED's 3100 Series subsystems with IBM-compatible media are also available for use with RTE-II. All systems can be provided with choice of standard or low-profile cabinets. See below for our low prices.



Compare these features

	Double Density IE AED 6200	AED 3100
Number of Tracks	77	77
Transfer Rate	500K bps	250K bps
Storage on Both Sides	yes	yes
Programmable Formatter	yes	Yes
Typical Record Sizes per side • 128 bytes/sector • 256 bytes/sector • 512 bytes/sector	542,080 bytes 670,208 bytes 670,208 bytes	256,256 bytes 315,392 bytes 315,392 bytes
IPL, Drive Select, Write Protei	ct yes	yes
LED Status & Error Indication	yes	yes
Vertical Rack Space • 2 drives • 4 drives	5.25" 10.5"	5.25" 10.5"
Price: Quantity 25 (DMA 1/F)	\$2.060 88	\$1.930 ee.

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MICROCOMPUTER SYSTEM FLOPPY DISC

PRODUCTS

PRESSURE TRANSDUCERS WITH BUILT-IN DC-DC CONVERSION CIRCUITRY



Developed to eliminate the extra cost of the amplifiers that are required to boost the low level output signal from straintype pressure transducers, GS series feature built-in solid-state dc-dc conversion circuitry to produce an infinite resolution high level output signal. By coupling an LVDT type electrical position sensor to a stainless steel pressure sensing capsule and including dc-dc conversion circuitry that permits direct connection to dc power sources between 9 and 15 Vdc, the transducers provide several advantages. Full

scale output signal amplitude is 0 to 5 Vdc; temperature sensitive amplifiers are eliminated; and complete electrical isolation is provided between input and output. Response to step input is 15 ms max. Gulton Industries, Inc, S-C Div, 1644 Whittier Ave, Costa Mesa, CA 92627. Circle 244 on Inquiry Card

16-SEGMENT ALPHANUMERIC READOUT

Pinlite model 0-43, a 16-segment, 0.25'' (0.635 cm) directly viewed incandescent display, provides a sharp, high brightness image. For operation in either dc or multiplex mode, the low voltage device uses rugged single-plane unit construction and conforms to military spec. Brightness is adjustable with simple voltage control from zero to a level that is easily viewed even under high ambient light conditions. Character display measures $0.375 \times 0.335 \times 0.312''$ (0.953 $\times 0.851 \times 0.792$ cm) deep, and is rated at 100-kh life/segment at 3 Vdc with a brightness of 1400 ft-L. Patented cross-over filament design eliminates the dark spots sometimes found in the corners of similar displays, and the 120-deg viewing angle and high brightness make it easy to read. Microminiature size allows high density packaging. **Refac Electronics Corp**, PO Box 809, Winsted, CT 06098. Circle 245 on Inquiry Card

MULTICOPY PRINTER



A 150-char/s, 132-col printer, the 810 provides microprocessor control of printing functions, programmable forms control, and a buffered communications interface. Increased throughput results from having the microprocessor control select the next line of data to be printed and direct the printhead either forward or reverse to achieve the shortest time to move to the print positions. A wire-matrix printhead produces up to six permanent copies with a minimum of sound. Std char set is 64 ASCII char in a 9 x 7 dot pattern. Standard features include a 256-char communications line buffer, a self-test feature and an adjustable tractor drive for form widths of 3 to 147/8'' (7.62 to 37.8 cm). Texas Instruments Inc, Digital Systems Div, PO Box 1444, M/S 784, Houston, TX 77001.

Circle 246 on Inquiry Card



Interfacing to an 8-bit microcomputer system via a single PIA chip, the FD-8 uses GSI disc drives, with each housed in its own cabinet complete with power supply. Disc controller board is contained in the same cabinet with drive 1 and communicates with the microcomputer system by means of a small ribbon cable. Up to four drives connect to drive 1 by means of a parallel cable. System controller board contains a sector buffer; a 3k RAM on the board allows information to be transferred from controller to disc completely independent of processor speed. Approximately 512 bytes of memory in the microcomputer system house disc drive and FDOS bootstrap routine; disc driver subroutines occupy approx 1k of memory and are loaded by the bootstrap. Midwest Scientific Instruments, Inc, 220 W Cedar, Olathe, KS 66061. Circle 247 on Inquiry Card

IMAGE DISPLAY SYSTEM

Offering theoretically unlimited spatial resolution, series 200 system eliminates previous limitations of system performance imposed by the spatial resolution of CRT monitors. Spatial resolution of the large data base can be any array of X by Y picture elements (pixels) and up to 16 bits of intensity/pixel. Operator console, monitor type A has 512 x 512 resolution, and presents the entire data base reduced in spatial resolution to match that of the monitor. A square outline, indicating the 512 x 512 region which is displayed on the B type monitor, will be displayed on its reduced resolution presentation of the entire data base. Type B, with 512 x 512 resolution, displays in full resolution that section indicated by the square outline on the type A monitor. Type C has 1024 x 1024 resolution and can display any 1024 x 1024 region of the refresh data base in full spatial resolution. Comtal Corp, 169 N Halstead St, Pasadena, CA 91107. Circle 248 on Inquiry Card

INTELLIGENT DISC CONTROLLER

A microprocessor-based controller that supports storage module devices with capacities from 25M to 300M bytes/spindle, MSC-1000 attaches to one to four (optionally eight) drives of one type and capacity. Std features include overlapped seeks; auto-



matic track seek and verification; automatic head and cylinder switching; and multiple-sector transfer of adjacent sectors, tracks, and cylinders. The controller also contains a set of resident microdiagnostics. Its micropro-

grammed design permits it to respond as an RK11 or RP11 for bootstrapping purposes, allowing use of DEC's std switch or nonswitch register bootstrap ROMs. Memory reference requests can be issued on the PDP-11's Unibus, allowing commands to be fetched directly. **Microcomputer Systems Corp**, 440 Oakmead Pkwy, Sunnyvale, CA 94086. Circle 249 on Inquiry Card

PROGRAMMABLE LIMIT SWITCHES

Solid-state switches provide precise mechanical position programming and control without the use of cams, followers, or mechanical switches. Switches consist of high reliability magnetic position sensing device and electronics package which provides control signals at precisely selectable rotary positions. Coded key or thumbwheel switch programming changes settings. Transducers are supplied in miniature, Nema 12, and waterproof configurations. Astrosystems, Inc, 6 Nevada Dr, Lake Success, NY 11040.

Circle 250 on Inquiry Card

DRIVE AND STEPPING MOTORS

Designed for floppy disc drive applications, the 1/100 hp ac drive motor has precise repeatable speeds and output speeds of 1500 rpm at 50 Hz or 1800 rpm at 60 Hz. Unit is a permanent-split-capacitor reluctance synchronous motor with automatic reset thermal overload protector. Stepping motors are size 18 and 20, with single or multiple start lead screw. Available in 3or 4-phase, with 15-deg step angle, these variable reluctance motors are precision bidirectional devices. Eastern Air Devices, Holtzer-Cabot Motors, Dover, NH 03820.

Circle 251 on Inquiry Card

WIREWRAP SOCKET BOARD

The 6000 series of pluggable PC boards complements the company's 4000 series in size and configuration, but is designed to accommodate pin and socket style I/O connectors rather than fingers for card edge connectors. Onboard male connector with three rows of 40 pins is std. The female connector, with wirewrap pins or solder tails, is supplied separately if required. DIPs with legs spaced on 0.300, 0.400, and 0.600" (0.762, 1.016, and 1.524 cm) can be accommodated any place on the board. Excel Products Co, Inc, 401 Joyce Kilmer Ave, PO Box 168. New Brunswick, NJ 08903. Circle 252 on Inquiry Card

PROGRAMMING MATRIX KIT

The 10 x 10 mini p/ROM matrix offers a method of manual programming for prototyping of solid-state sequential control applications. TTL- and CMOS-compatible, the kit comes with 10 diode holders, 10 shorting pins, and 20 terminations. Binary information is programmed by the insertion of diode pins into the matrix board. Word capacity is ten 10-bit words. Additional matrices can be linked together for added memory capacity. Custom configurations of 8, 16, or 32 bits can also be obtained. **Programming Devices Div, Sealectro Corp,** Mamaroneck, NY 10543. **Circle 253 on Inquiry Card**

MONITOR ALARM



A 100-input alarm for data communications circuits can be programmed to monitor normally open or normally closed contacts or current loops. An audible alarm and a flashing LED indicate when a monitored circuit has failed. All contact circuits monitored are isolated from the monitor via reed relays, all current loops via optical isolators. Model AL-25-4 incorporates debounce and delay circuits to eliminate false alarms. Contacts are included for remote alarms. **Dataprobe, Inc,** 254 Green St, South Hackensack, NJ 07606. Circle 254 on Inquiry Card

DIP SWITCHES

The JS-8722 series features sealed construction utilizing a thermosetting plastic material to prevent flux contamination during wave soldering. A clip-type wiper design assures positive 2-sided contact to provide good shock and vibration characteristics. Switches range from one to ten positions. Available in spst configurations, switches are rated 500 mA at 50 Vdc nonswitching and 24 Vdc at 300 mA switching, resistive load, and operate from -20 to 60°C. SMK Electronics Corp of America, 118 E Savarona Way, Carson, CA 90746.

Circle 255 on Inquiry Card

DIP SOCKETS



Lower sidewall construction of the socket leaves a device body exposed for better heat dissipation and more uniform airflow during extended tests at elevated temperatures. The sidewall is high enough, however, to act as a guide to the tapered contact entry designed to accept devices with bent or distorted leads. Requiring up to 15% less PC board area than similar sockets, the device combines a minimum profile with low insertion force contacts. Models are available in 14- or 16-pin versions in materials capable of 300°C operation. Textool Products, Inc, 1410 W Pioneer Dr, Irving, TX 75061. Circle 256 on Inquiry Card

RK-II/RK-05 MEDIA CARTRIDGE fully DEC compatible

The AED 2200 hard disk subsystem offers complete compatibility with all RK-11/RK-05, and associated DEC software. Plugging directly onto the PDP-11 Unibus[®] the 2200 Controller can handle up to 4 drives, providing 4,915,200 16-bit words of economical storage. The AED 2200 subsystem is supplied with Diablo Series 30 or similar type disk drives, and is available immediately on a 30-60 day delivery basis. Check our competitive prices below.



Compare these features

- Direct substitute for RK-11/RK-05 System
- · Complete DEC media/software compatibility
- · A 2-drive power supply is included with controller
- · Complete with Unibus® and controller-to-drive cables
- ® Reg. Trademark of Digital Equipment Corp.

Compare these prices

Quantity 11 with 1 drive unit: \$6,255 ea. Quantity 11 with 4 drive units: \$14,190 ea.

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PRODUCTS

PORTABLE OSCILLOSCOPE



Featuring A + B and A - B capability, the dual-trace PM 3226P is a 15-MHz oscilloscope with 2-mV sensitivity and comprehensive triggering facilities. The 9.5-lb (4.3-kg) unit measures 4.72 x 10.8 x 12.5" (12 x 27.4 x 31.8 cm) and features adjustable level, automatic, line, automatic TV-line, and frame-sync-pulse triggering. External triggering is also possible. Input impedance of vertical and horizontal channels is 1 MΩ/25 pF, and rise time is 25 ns. Dynamic range is 24 div for sine wave signals up to 1 MHz. 18 sweep speeds from 500 ns to 0.2 s are available with chopped and alternate display possible for all time base settings, with a 400-kHz chopping frequency. Power can be 110, 127, 220, or 240 V ±10% at 46 to 440 Hz. Philips Test & Measuring Instruments, Inc, 85 McKee Dr, Mahwah, NJ 07430. Circle 257 on Inquiry Card

DUAL CASSETTE/TERMINAL INTERFACE CARD

The dual-function CI-812, an Imsai/Altair S-100 bus-compatible card, combines interfacing functions normally requiring two or three PC cards. Cassette interface phase encodes (Manchester/ biphase) at the std rate of 30 bytes/s, and at 60, 120, or 240 bytes/s for rapid loading of frequently used programs. Selfclocking encoding offers high reliability at fast data rates using inexpensive audio cassette recorders. Interface record and playback circuits are completely independent, and the card is patterned to include optional DIP reed relays for program control of two recorder/players, permitting operations such as crossfiling. A companion circuit, the RS-232 terminal interface is full duplex and provides for data exchange at 300 to 9600 baud. **PerCom Data Co, Inc,** 4021 Windsor, Garland, TX 75042. Circle 258 on Inquiry Card

MICROPROCESSOR-CONTROLLED PRINTERS

Dot-matrix printers that feature bidirectional printing under microprocessor control at speeds of 70 to 200 lines/min, 9317 and 9318 can be used with various minicomputers and terminal system configurations. Each is controlled by an Intel 8080A microprocessor that is common to both units. 9317, a single printhead unit that prints at 70 lines/min over the full 132char line, achieves a rate of 200

lines/min when printing lines of 33 contiguous columns or less. Its microprocessor computes the closest position on the next line to start printing, and directs the printhead movement either left or right. The 9318 includes two printheads, each covering up to 66 col of the full 132-char line, and achieves full line print speed of 125 lines/min for char formed in a 7 x 7 dot matrix pattern. **Control Data Corp.** Box O, Minneapolis, MN 55440. Circle 259 on Inquiry Card

HOOK-MOUNT SUBMINIATURE

For use with subminiature wedge-base lamps, the Tiny-Mite 4150 series has an integral hook designed for simple, 1-hole mounting. The 1-piece white nylon housing is available with or without light shield/reflector on either side of the hook. Socket accommodates T-1¾ subminiature wedge-base lamps rated at 6.3, 14, or 28 V. Construction provides reliable contact with the lamp regardless of lead position. Lamp is held securely and cannot "float." Industrial Devices, Inc, 7 Hudson Ave, Edgewater, NJ 07020.

Circle 260 on Inquiry Card

LOW COST STEPPER MOTOR

A 7 deg 30 min step angle bidirectional unipolar driven logic stepper motor, series 82700 features small package size. 5- and 12-Vdc models are available. Power consumption is 8 W; start speeds run to 375 r/min and max developed torque is 8.0 oz-in (0.056 N*m). Large bearing surfaces, straight-through rotor shaft, and rugged mechanical construction allow good gearing support and assure precise operation. **North American Philips Controls Corp**, Cheshire Industrial Pk, Cheshire, CT 06410.

Circle 261 on Inquiry Card

MIDGET FLANGED-BASE LEDS

Replacing incandescent bulbs at the same brightness but with 10 times the lifetime and using half the current, MF200 series LEDs are available in red, amber, and green. At a drive current of 20 mA the lamps put out 50 mcd (red), 35 mcd (amber), and 24 mcd (green), with a clear tinted encapsulation. Also available with diffusive encapsulation, they are immune to pulses of current. All have builtin resistors for voltages ranging from 3.6 to 28 Vdc. Units are also available for ac operation. **Data Display Products**, 5428 W 104th St, Los Angeles, CA 90045. **Circle 262 on Inquiry Card**

LOW PROFILE TOGGLE SWITCH

A short flatted actuator available as an option on any of the company's spdt, dpdt, and 4pdt models, P4 is a contemporarystyled toggle measuring 0.320" (8.13 mm) high, by 0.165" (4.19 mm) dia. Anti-rotation pivot pin secures the toggle to the bushing, assuring true linear motion of the toggle and preventing a circular switching effect. Actuator is brass with a chromeplated finish, or an optional satin-chrome finish. C&K Components, Inc, 103 Morse St, Watertown, MA 02172. Circle 263 on Inquiry Card

PROGRAMMABLE CMOS PULSE DRIVER

Combining flexible 50-MHz timing circuits with a programmable 20-V output amp to cover the high voltages required for MOS device testing, the 1504's output is $50-\Omega$ backmatched source which delivers 10 V into a 50- Ω terminated line or 20 V into higher impedances. Backmatch can be switched out to drive 20 V pulses into a 50- Ω load to accommodate most system and fixture testing requirements. Specifications include: frequency, 0.5 Hz to 50 MHz; delay/width, 10 ns to 1 s: and rise/fall times, 3 ns to 800 µs. EH Research Laboratories, Inc, 515 11th St, Box 1289, Oakland, CA 94604. Circle 264 on Inquiry Card

IMPROVED FLOPPY DISC SYSTEM

Model 423 provides seven times the performance of the model 422, achieving a significant increase in throughput on systems where contiguous information has wide track separations over the 77 available tracks. Max track access time is <100 ms. Software operating systems and hardware interface exist for both HP series 21XX and DEC PDP-8/E minicomputers. Basic dual diskette drive module accommodates two diskettes with a separate head for each. The unit is available in one or two dual diskette drive module configurations. **Dicom Industries, Inc,** 715 N Pastoria Ave, Sunnyvale, CA 94086.

Circle 265 on Inquiry Card

8-BIG DISK,4-CPU *L* CONTROLLER for DEC/DGC software

The new AED 8000 mass storage system with microprogrammable controller can be completely integrated into your DEC or Data General system. You can now enjoy patch-free use of any OS changes generated by the mainframe manufacturer, because AED's emulation capability ensures continuous compatibility to standard software. Add to this AED 8000's unique ability to serve up to 4 CPUs per controller at the same time, its built-in Error Correction System, and a multiple-register scroll that displays mainframe register information plus valuable diagnostic data, and you'll see why the AED 8000 is way ahead of the competition. AED's field-proven reliability and fast 45-60 day delivery make the AED 8000 mass storage system a serious contender for your disk dollars.

Compare these features

	AED 8000	DEC DGC
Megabytes per drive	67.4→250	40 92
No. of drives per controller	1→8	84
Megabytes per controller	540-→2,000	320 368
No. of CPU's per controller	4	12
16-bit transfer rate	1.6 µs	6.4 μs 2.5 μs
16-bit buffer	256	6
Error Correction Code	by controller	none
Bootstrap	IPL in controller	CPU ROM
Micro-processor	40 ns. 24 bits	none
Emulates DEC/DGC controller	Yes	
Macro Instruction Code	Yes	none
Data Scanning & Management	in controller	in CPU
Variable Sector Length	Ves	none
CPU to CPU transfers	bypass the disk	none via disk

Price: Quantity 1-\$18,200 incl. 67.4 Mbyte drive

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CIRCLE 102 ON INQUIRY CARD

TRANSMISSION TEST SET

PTS-107 is a complete generator, receiver, and error rate measurement system, which covers data rates from 1k to 55M bits/s for testing communication channels, twisted-pair wires, coaxial cables, and other communication systems. Three internal crystal

oscillators (T1, T2, and T3 rates std) serve as clock source for the generator section. Generator produces a choice of four pseudorandom code lengths from 63 to 1M bits in length, or a switch-programmable fixed pattern. Zeros, errors, or preamble may be inserted into the pattern; an exter-

nal control signal allows TDM patterns to be simulated. Receiver section features clock recovery; automatic clock data phasing, and automatic synchronization. The 4-digit counter measures generator and receiver clock frequency, bit error rate, and code violations on bipolar inputs. **Tau-Tron**, **Inc**, 11 Esquire Rd, North Billerica, MA 01862.

Circle 266 on Inquiry Card

GRID OR TABLET DIGITIZERS

DatatizerTM uses a clock-generated electromagnetic wave in conjunction with a free cursor. DTHR is a 0.001" (0.0254 mm) resolution, high performance series; DTLR is a 0.010" (0.254 mm) resolution, lower performance unit. Both allow digitizing through a thickness exceeding 1" (25.4 mm) and require no user adjustment. X and Y cursor or stylus position is determined by measuring the time required for the clock-generated electromagnetic wave to pass the cursor center. Since the system operates on an electromagnetic principle, it is immune to normally detrimental environmental factors. Using a scanning technique, X and Y coordinates are determined many times each second, thereby allowing the operator to lift the cursor from the surface when moving from point to point. Configuration includes grid or tablet digitizer, cursor and grid or tablet controller with all necessary power supplies, and a parallel BCD or binary output. GTCO Corp, 1055 First St, Rockville, MD 20850. Circle 267 on Inquiry Card

TAPE CARTRIDGE CAROUSEL

Resembling a 35-mm circular slide projector, model 5200 holds 16 ¹/₄" (0.635 cm) cartridges (ANSI std X3.55-1976) in a removable pack. A dual-microprocessor formatter simplifies interfacing, handles routine housekeeping functions, and reduces

ng functions, and reduces user-programming requirements. Designed for unattended operation, cartridges are indexed, loaded, processed, and unloaded automatically. Data can be copied, files sorted, information updated, and reports spooled without intervention. The pack mounts on a drive unit containing one to four read/write stations, logic circuitry, and oper-

ating mechanism. A cartridge is automatically loaded, processed, and unloaded at the nearest available station. Four stations can be operated simultaneously. **National Computer Systems**, 4401 W 76th St, Minneapolis, MN 55435. Circle 268 on Inquiry Card

PRINTHEAD CONTROL INTERFACES

Providing input controls for print commands, red/blue printing, and doublespace printing, interfaces for Precisa 388 series printheads generate status signals, such as printer busy and data stable, in control electronics. They work in conjunction with the power supply to apply power to the head at the beginning of the print cycle and remove power at the end. Model 388E-14-01, a general 14-col BCD interface on a 4.5 x 8" (11.4 x 20.3 cm) PC board, is DTL/TTL compatible and uses low power Schottky ICs, requiring <500 mA of 5 V power. Master Digital Corp, 1308-F Logan Ave, Costa Mesa, CA 92626.

Circle 269 on Inquiry Card

LINE PRINTER CONTROLLER

A DMA controller brings CDC, Centronics, and Dataproducts printer capabilities to Data General Novaⁿ and Eclipseⁿ users. The controller occupies a single CPU slot and interfaces the Control Data 300-, 600-, or 900-line/min band printer; Dataproducts 2230 or 2260; and the Centronics product line. All cables and diagnostics are provided. **Tri-Star Computer Systems, Inc,** 304 Harper Dr, Moorestown, NJ 08057.

Circle 270 on Inquiry Card

REMOTE CONTROL PANEL

Model 8931, added to the 8900 series "Minitest" line, switches individual channels and also provides a master which will switch all channels to A or B. Unit allows individual remote control of 16 channels of A,B switching, when used with the 8962 controller and power module. LEDs, which indicate the status of each channel master in full-duplex mode, are paralleled with LEDs on the master unit. Panel always has priority over the master unit. International Data Sciences, Inc, 100 Nashua St, Providence, RI 02904. Circle 271 on Inquiry Card

PUSHBUTTON SWITCH WITH PC TERMINALS

The Hi-D^R switch, a miniaturized momentary action pushbutton switch with molded box construction and PC terminals for high density mounting on PCBs or flat, flexible cable, can be specified with 1-A, 1-B, or 1-C circuitry. Switch body has a 1-piece unitized construction of molded nylon, which provides min electrical leakage, low stable capacity between springs, positive internal spring positioning, and positive 'make-break'' switch contacts. Contact springs are precision formed of a special nickel-silver alloy. **Switchcraft, Inc**, 5555 N Elston Ave, Chicago, IL 60630.

Circle 272 on Inquiry Card

MINIATURE FLOPPY DISC

One-half the size of the standard floppy disc and providing one-third the storage capacity, MD 525 stores the equivalent of 25 typed pages of data, yet is compatible with small disc drive systems like those available from Shugart Associates. It is manufactured using proven floppy disc media formulations, and is functional in such applications as power typing systems, editing systems, word processing, and the microcomputer hobby market. **Information Terminals Corp**, 323 Soquel Way, Sunnyvale, CA 94086. Circle 273 on Inquiry Card

LIGHT PENS

With sensitivities that range from 2 ft-L to 0.2 ft-L with <200-ns response time, FP-110P and -120F incorporate a lens system in the nose piece for high character discrimination. All processing circuitry is enclosed within the pen housing and no external adjustments are necessary. Signals interface directly with TTL logic. Spectral response is from 4200 to 10,000 Å with high background tolerance. The selection switch provides tactile feedback to the operator. Fuller Engineering & Manufacturing, 149 San Lazaro Ave, Sunnyvale, CA 95050. Circle 274 on Inquiry Card

MINIATURE SWITCHING POWER SUPPLIES

With efficiencies from 75 to 85%, MMG switching power supplies provide low ripple, regulated dc output voltages for operation of electronic circuits. Units operate from 110/120 V or 220/240 V \pm 10%, 50 or 60 Hz, and use optical coupling to provide 4-kV rms isolation (5.7 kV peak) between input and output. Four models provide dc outputs of 5, 12, 15, or 24 V at currents from 1.4 to 5 A. Voltage regulation is 0.1% max for worst case combination of 0 to 100% load change and \pm 10% line change. **Gould Inc**, 3631 Perkins Ave, Cleveland, OH 44114. Circle 275 on Inquiry Card

... and look at all the other design advantages our 28H Series relay offers.

Our 28H Series SPDT relay has so much going for it, it's hard to know where to begin. First, it's mini-sized —occupies only .92 sq. in. board area x 1.188" high. Second, it comes with a dust cover as standard and is available with a choice of enclosure styles and terminals to suit your application. It's also sensitive... 176 mw pick-up. Best of all, its low cost meets or beats competitive prices. U/L recognized. 10 amp 0.8 PF 120V 60Hz or 28V dc resistive. 3 amp models also available.

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DOUBLE DENSITY DISKETTE SYSTEM

PRODUCTS

PDP-8 users may now operate OS-8 from a diskette system using a DMA-type interface which allows attachment of the 6200LP system and an OS-8 version 3 driver which allows the disc system to serve as the system residence device. Users can operate under OS-8 with the floppy disc as the only system storage device. HP2100 users of the RTEII or III operating system can use the 6200 which allows the operating system to reside on diskette drive 0, with data and other programs on drives 1, 2, or 3. The diskette system serves either as the system residence device or as auxiliary storage. Space required for the operating system without compilers is less than 250k bytes. A dual-drive 6200LP provides approx 1.25M bytes of data storage; a 4-drive 6200P is also available. Advanced Electronics Design, Inc, 754 N Pastoria, Sunnyvale, CA 94086.

Circle 276 on Inquiry Card

LIGHT PEN

The RALTEC^R 285 is designed for use with the view mode of Tektronix storage displays 603, 611, and 613, and terminals 4006, 4010, 4012, 4013, 4014, and 4015. It works with most storage and nonstorage displays having P1 phosphor at a 10-kHz rate, or P2 and P31 phosphors up to 80 kHz with light-detect times as short as 2 μ s depending on the phosphor. For control purposes, a touch-detect channel is activated when the operator's finger contacts a resistance-sensing area on the probe barrel. Both light-detect and touch-detect channels operate independently, but their normally low, open-collector outputs may be wired together. The unit runs off ± 12 or ± 15 Vdc and is compatible with DTL, TTL, and CMOS. Lake Electronics Co, 25884 High-land Rd, Cleveland, OH 44143.

Circle 277 on Inquiry Card

RECESSED-ROCKER DIP SWITCHES

Featuring a rocker actuator that is recessed below the top surface of the switch to permit tape to be used as a seal for the top of the switch during the solder cleaning operation, and prevent accidental operation of the switch, the recessed-rocker DIP switch stands 0.275" (0.698 cm) above the PC board. This version is available with spst circuitry in two through 10 stations. Con-

tact design features a spring-loaded, sliding ball which provides wiping action and positive positioning of the actuator, making the switch less susceptible to normal shock and vibration than more conventional designs. Contacts are gold-plated and have 50,000-operation life at logic loads. Grayhill, Inc, 561 Hillgrove Ave, La Grange, IL 60525. Circle 278 on Inquiry Card

LITERATURE

Heat Sinks

A supplement to the general catalog and a performance guide containing scale drawings and tabulated performance data are available for expanded line of natural convection heat sinks. Astrodyne, Inc, Wilmington, Mass.

Circle 300 on Inquiry Card

Electro-Optics Devices

Operating parameters, physical descriptions, and optical and electrical characteristics of Sharp electro-optic products are covered by catalog which includes photodiodes, phototransistors, and IR LEDs. Quantrad Corp, El Segundo, Calif. Circle 301 on Inquiry Card

LED Panel Lamps

Electrical and mechanical data, as well as ordering information for P405 and PR405 snap-in lights, are detailed in the data sheet. Data Display Products, Los Angeles, Calif.

Circle 302 on Inquiry Card

Intelligent Terminals

Foldout brochure with system diagrams describes the intelligent terminal systems used in five applications, and the approaches taken to solve data communication problems. Incoterm Corp, Wellesley Hills, Mass.

Circle 303 on Inquiry Card

Frequency Synthesizer

Describing the model 5600 programmable frequency synthesizer, bulletin lists applications and specs, and includes curves and oscillograms. Rockland Systems Corp, West Nyack, NY. Circle 304 on Inquiry Card

Buffered Data Terminal

Brochure on the model 500 intelligent microprocessor-controlled data terminal discusses its advantages, operation, specs, options, and application. MFE Corp, Salem, NH.

Circle 305 on Inquiry Card

Line Printers

Brochure furnishes specs on range of line printers-from 100 to 1200 lines/minand on 300- to 1200-card/min card reader, and 100- to 1500-line/min interfaces. Digital Associates Corp, Stamford, Conn. Circle 306 on Inquiry Card

Computer Systems

"Computers in Engineering" discusses the use of computers in various fields of technical analysis and design, and their value in data acquisition, reduction, and processing. Digital Equipment Corp, Northboro, Mass.

Circle 307 on Inquiry Card

LSI Tester

Complete with photos, illustrations, and block diagram, brochure provides general description, operational performance characteristics, specs, and options of the low cost, benchtop tester. Macrodata Corp, Woodland Hills, Calif. Circle 308 on Inquiry Card

Solid-State Relays

Applications handbook, complete with block diagrams, schematics, performance graphs, charts, and specs, covers relays for a wide range of commercial/industrial and military/aerospace uses. Teledyne Relays, Hawthorne, Calif. Circle 309 on Inquiry Card

Word Processors

Illustrated brochure highlights features of word processors 10, 20, and 30, which are built around work, storage, and daisy wheel printer stations. Wang Laboratories, Inc, Lowell, Mass. Circle 310 on Inquiry Card

Printers

Application note covers system and time implications of printers utilized with microprocessor software development systems, and alludes to effects of program size on selection. Houston Instrument, Austin, Tex. Circle 311 on Inquiry Card

System Software

Divided into six sections, brochure presents systems software capabilities, languages, and special purpose utilities to help users get applications online quickly. Data General Corp, Southboro, Mass. Circle 312 on Inquiry Card

COSMAC Microprocessor

Basic users' manual, complete with detailed examples, is a guide to the application and programming of the CPD1802 microprocessor, a 1-chip CMOS 8-bit register-oriented CPU. Send \$5 to RCA Solid State Div, Box 3200, Somerville, NJ 08876.

Array Programming

Brochure explains an array programming approach to digital system design that allows LSI logic to be specified at the semiconductor chip level without the cost penalties of custom design. Stewart-Warner Microcircuits Div, Stewart-Warner Corp, Sunnyvale, Calif. Circle 313 on Inquiry Card

Power Supplies

Specs, principles, practices, and terminology for modular; high voltage modular; miniature; high power, open frame; and microcomputer supplies, and dc/dc converters are given in catalog. Datel Systems, Inc, Canton, Mass. Circle 314 on Inquiry Card

Electronic Wires/Cables

Data package includes technical data, application information, product selection guide, and samples of various electronic wires, coaxial and multiconductor cables, and cable assemblies. Essex Electronic Wire Products, Fort Wayne, Ind. Circle 315 on Inquiry Card

FSK Multiplex Equipment

Brochure provides information on equipment design and operation, and lists specs for basic transmitter and receiver modules in the Q-70 series crystal-controlled FSK multiplex equipment. QEI, Inc, Springfield, NJ.

Circle 316 on Inquiry Card

Memory Refresh Principles

Simple refresh circuitry is outlined in application summary bulletin which provides block diagrams along with a review of refresh principles and their implementation for 4k dynamic RAMs. Texas Instruments Inc, Dallas, Tex. Circle 317 on Inquiry Card

Amplifiers/Encoders

Line of 2SD405/412 npn silicon epitaxial mesa darlingtons are examined in data sheets which outline features, ratings, dimensions, and typ and electrical characteristics. Write on company letterhead to NEC America, Inc, Electron Device Div, 3070 Lawrence Expwy, Santa Clara, CA 95051.

Fast Fourier Transform

The FFT: Fundamentals and Concepts introduces basics of time and frequency measurements, along with an illustrated discussion of classical Fourier analysis and the FFT. Price is \$25. Order part number 070-1754-00 from a local Tektronix field office, or from Tektronix, Inc, PO Box 500, Beaverton, OR 97077.

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