

DESIGN NOTE

Choosing the Correct Flat Cable for High Speed Logic Circuits

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Before choosing a flat cable for a specific application, a designer should be aware of the standard designs' different characteristics; then, he may decide which best suits his needs

Flat cables have three common design configurations, offering different characteristics. While their differences may not be critical in many applications, in high speed logic circuits, several factors must be evaluated before making the necessary tradeoff to suit the particular circuit design needs. Principal factors are crosstalk, attenuation, and impedance.

The three designs (with arbitrary A, B, C designations for later reference) are:

- A Several twisted-pair lines, laced together to form a flat ribbon
- B A parallel "lay-flat" cable, with all lines enclosed within the same dielectric material
- C Same as B, with a controlled-impedance ground plane added

These designs were evaluated on the basis of tests made with one wire of each pair grounded, so that characteristic differences would clearly be

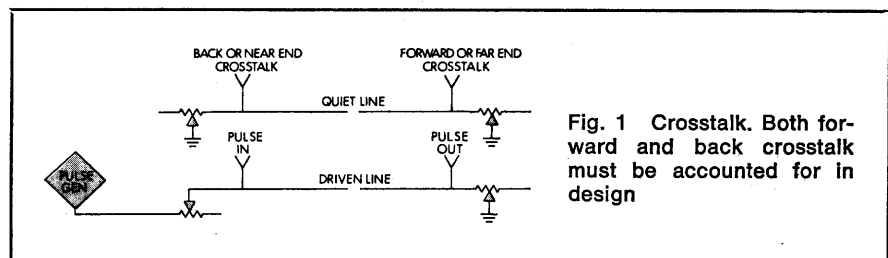


Fig. 1 Crosstalk. Both forward and back crosstalk must be accounted for in design

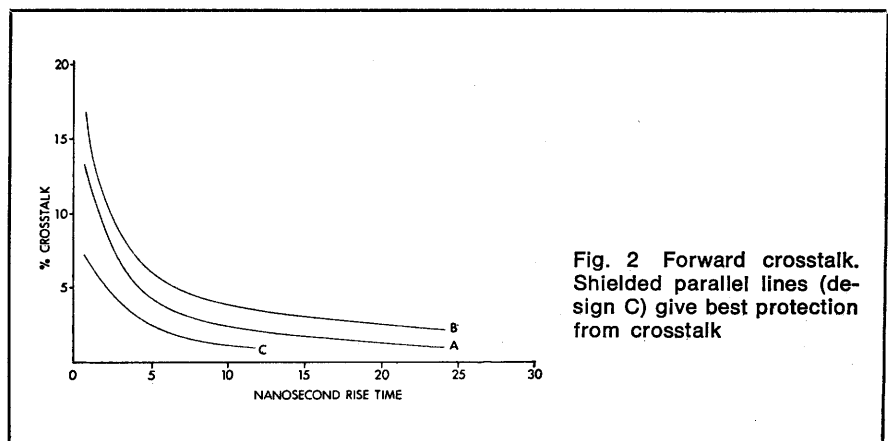
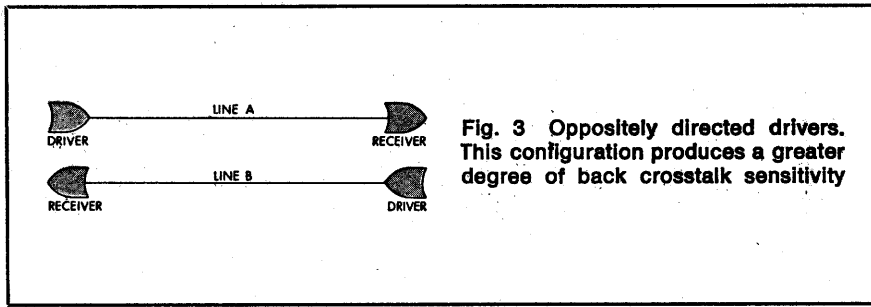


Fig. 2 Forward crosstalk. Shielded parallel lines (design C) give best protection from crosstalk



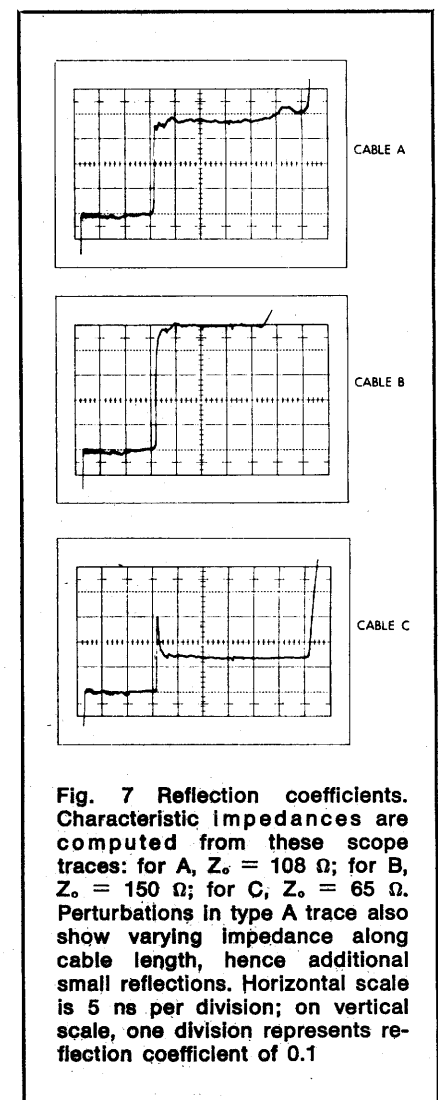
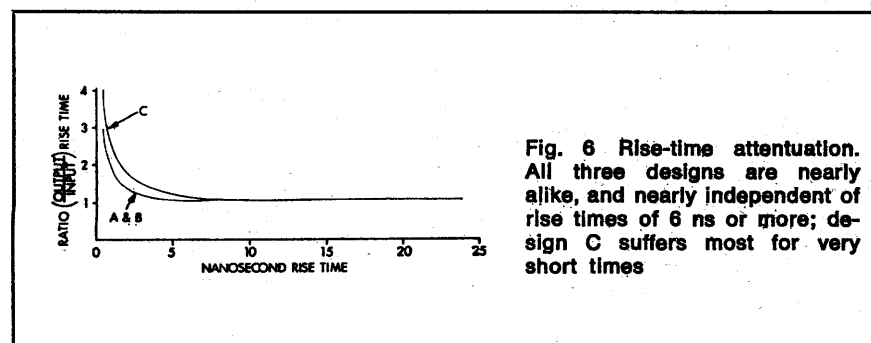
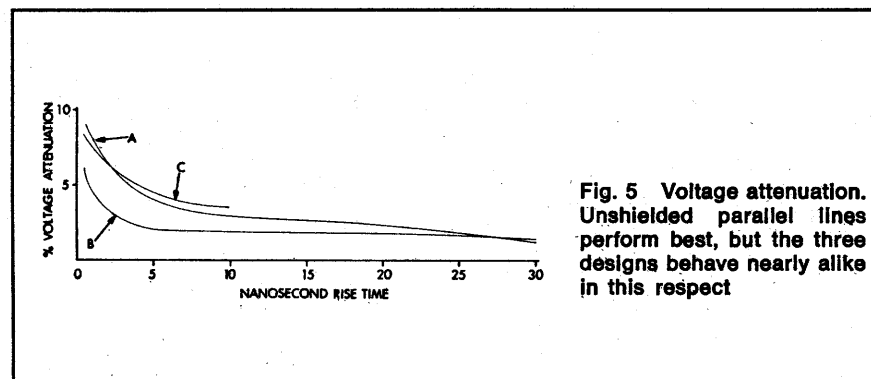
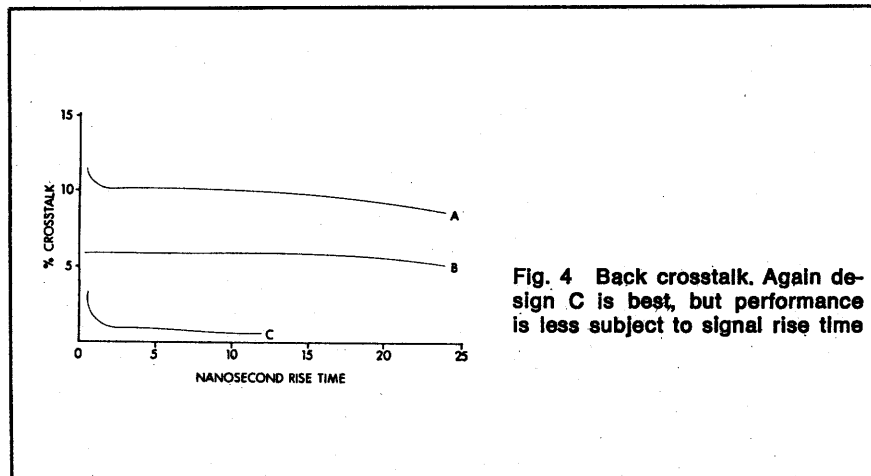
the result of design variations, not of common-mode noise or of circuit imbalance.

Although each electrical parameter is discussed separately, all are interdependent. Tradeoffs are important; an attempt to improve one characteristic by circuit or component design may degrade another characteristic.

Crosstalk

Originally, twisted-pair cables were used primarily to minimize crosstalk; however, alternative possibilities should be considered.

Crosstalk is voltage induced in a line adjacent to one being driven. It may be defined as either "forward" or "back" (Fig. 1).



Forward crosstalk should generally be no greater than 10%; otherwise, unwanted switching may occur in the quiet line. The shorter the rise time of the logic circuits, the higher the probability of crosstalk. Curves in Fig. 2 show that design C produces only 6.5% crosstalk even at 1-ns rise times, while A and B must be driven by slower signals to achieve that same protection. A further consideration is the logic-circuit choice; emitter-coupled logic can produce rise times of 1.5 ns, tending to limit the cable choice to C. When using transistor-to-transistor logic, however, which has a general minimum rise time of 5 ns, any of the three designs could be safe.

Back crosstalk becomes a special problem when adjacent lines are driven from opposite ends (Fig. 3). Back crosstalk is read at the receiver end of the quiet line, which is the most critical point in the possibility of producing unwanted switching in a receiver. Quite often, driven ends of the lines are connected directly to the driver, with no impedance-matching circuit, and thus have a reflection coefficient of 0.8 or more. Therefore, during the time the gate on the quiet line is turned off, 80% or more of the back-crosstalk signal can be reflected to the forward end of the driven line. This reflection from back crosstalk is another factor that affects the overall forward crosstalk. Some typical back-crosstalk curves are shown in Fig. 4.

Attenuation

Attenuation has two components: voltage attenuation and rise time attenuation. Our tests do not give absolute values, but they do show trends.

Voltage attenuation (in percent) is the ratio of the voltage drop between input and output to the input voltage:

$$100(E_{in} - E_{out})/E_{in} = \text{percent voltage attenuation}$$

Again, short rise times are associated with high voltage attenuation; for this parameter, design B appears to be the best (Fig. 5). However, the three curves are similar, and since

digital logic depends more on timing than on power transfer, none of the designs should be eliminated from consideration merely because of design B's relatively low voltage attenuation.

Rise-time attenuation is a simple ratio of output rise time to input rise time. Design C has the sharpest attenuation, but with circuit designs having rise times of 6 ns or greater, all three cable designs are comparable (Fig. 6).

Impedance

Characteristic impedance of the three designs (measured to ground reference) varies from 65 to 150 Ω (Fig. 7). Impedance was measured with a time-domain reflectometer, a plug-in for a standard oscilloscope. In each trace, the base line at the left results from a 50- Ω air line connected to the reflectometer; the height of the step is a measure of the reflection coefficient, ρ ; and characteristic impedance is determined with the relation

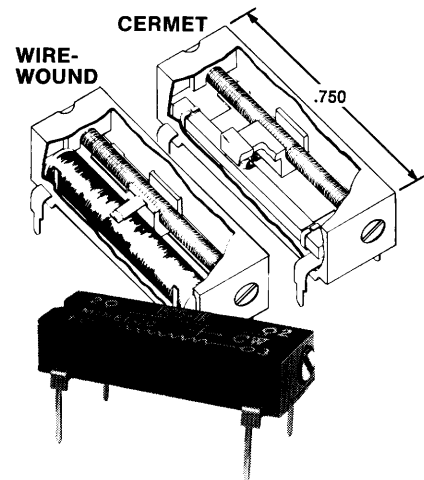
$$Z_0 = 50(1 + \rho)/(1 - \rho)$$

If lines are properly terminated externally, line impedance may not be a problem. On the other hand, if proper termination is not possible, the cable design that has the impedance closest to that of the driven circuit can be selected; it may be the best choice to minimize reflections.

Twisted-pair cables (design A) are subject to another potential difficulty. The scope trace shows perturbations in the magnitude of the reflection coefficient, corresponding to a varying characteristic impedance along the length of the cable. These variations are caused by nonconstant spacing of wires in the twisted pair. Although they are not severe in this case, the perturbations do show that small reflections occur at points where the impedance changes; these would make proper termination more difficult.

Flat cables may be the most practical, economical, and easy to install, particularly in the design of mass-produced equipment. However, a careful evaluation of their high speed logic characteristics is extremely important. □

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