XC4000 Series
Technical Information

June 1, 1996 (Version 1.0) Application Note

**Summary**

This Application Note contains additional information that may be of use when designing with XC4000 Series devices. This information supplements the product descriptions and specifications, and is provided for guidance only.

**Xilinx Family**

XC4000/XC4000A/XC4000H/XC4000E/XC4000L

# Introduction

This application note describes the electrical characteristics of the output drivers, their static output characteristics or I/V curves, the additional delay caused by capacitive loading, and the ground bounce created when many outputs switch simultaneously.

# Voltage/Current Characteristics of XC4000-Family Outputs

Figures 1 and 2 show the output source and sink currents, both drawn as absolute values. Note that the XC4000E/EX families offer a configuration choice between an n-channel only, totem-pole like output structure that pulls a High output to a voltage level that is one threshold drop lower than $V_{CC}$, and a conventional complementary output with a p-channel transistor pulling to the positive supply rail. When driving inputs that have a 1.4-V threshold, the lower $V_{OH}$ of the totem-pole (“TTL”) output offers faster speed and more symmetrical switching delays.

These curves represent typical devices. Measurements were taken at $V_{CC}$= 5 V, T = 25°C. These characteristics vary by manufacturing lot, and will be affected by future changes in minimum device geometries. These characteristics are not production-tested as part of the normal device test procedure; they can, therefore, not be guaranteed. Although these measurements show that the output sink and source capability far exceeds the guaranteed data sheet limits, continuous high-current operation beyond the data sheet limits can cause metal migration of the on-chip metal traces, permanently damaging the device. Output currents in excess of the data-sheet limits are, therefore, not recommended for continuous operation. These output characteristics can, however, be used to calculate or model output transient behavior, especially when driving transmission lines or large capacitive loads.

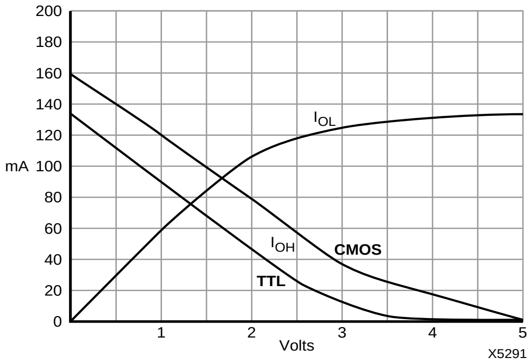


**Figure 1: Output Voltage/Current Characteristics for XC4000E**

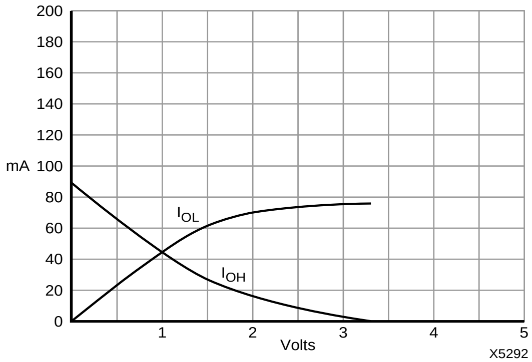


**Figure 2: Output Voltage/Current Characteristics for XC4000L**

## Additional Output Delays When Driving Capacitive Load

Xilinx Product Specifications in chapter 4 give guaranteed worst-case output delays with a 50-pF load.

The values below are based on actual measurements on a small number of mid-93 production XC4005-5, all in PQ208 packages, measured at room temperature and $V_{CC}$ = 5.5 V. Listed is the additional output delay, measured crossing 1.5 V, relative to the delays specified in this Data Book.

These parameters are not part of the normal production test flow, and can, therefore, not be guaranteed.

**Table 1: Increase in Output Delay When Driving Light Capacitive Loads (<150 pF)**

| | | High-to-Low | | | Low-to-High | | | |
|---|---|---|---|---|---|---|---|---|
| | **Slew Mode** | **10** | **50** | **100** | **10** | **50** | **100** | **pF** |
| XC4000 | Slow | -1.6 | 0* | 1.4 | -1.4 | 0* | 1.4 | ns |
| | Fast | -1.6 | 0* | 1.2 | -1.2 | 0* | 1.1 | ns |

Note: *Zero by definition

**Table 2: Increase in Output Delay When Driving Heavy Capacitive Loads (>150 pF)**

| | Slew Mode | High-to-Low | Low-to-High | |
|---|---|---|---|---|
| XC4000 | Slow | 1.7 | 1.2 | ns/100 pF |
| | Fast | 1.5 | 1.2 | ns/100 pF |

Example:

$\Delta$T High-to-Low for XC4005-5 with Fast-mode output driving 250 pF:

1.2 ns (from Table 1) plus (250-100) pF • 1.5 ns/100 pF = 1.2 ns + 2.25 ns = 3.45 ns

Total propagation delay, clock to pad:

$T_{OKPOF}$ + 3.45 ns = 7.0 ns + 3.45 ns = 10.45 ns

## Ground Bounce in XC4000 Devices

Ground-bounce is a problem with high-speed digital ICs, when multiple outputs change state simultaneously causing undesired transient behavior on an output, or in the internal logic. This is also referred to as the Simultaneous Switching Output (SSO) problem. Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC-internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously. Ground bounce affects outputs that are supposed to be stable Low, and it also affects all inputs since they interpret the incoming level by referencing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input will be interpreted as a short pulse with a polarity opposite to the ground bounce.

$V_{CC}$ bounce is not as important as ground bounce, because it is of lower magnitude due to the weaker pull-up transistors. Also, the noise immunity in the High state is usually better than in the Low state, and input levels are referenced to ground, not $V_{CC}$. All this is the result of our industry's TTL heritage.

### Test Method

Data was taken on XC4005-5, devices in the PQ208 package, soldered to the Xilinx Ground Bounce Test Board. Pin 82, two pins away from the nearest ground pin, was configured as a permanently Low output driver, effectively monitoring the internal ground level. The simultaneously switching outputs were on pins 80 and 83, for two outputs switching; additionally, pins 80 and 86 were used for four outputs switching. The closest ground pins are 79 and 90.

Four ground-bounce parameters were measured at room temperature, with Vcc set at 5.5 V as shown in Figure 3.

- $V_{OLP\text{-}HL}$ Peak ground noise when switching High-to-Low
- $V_{OLV\text{-}HL}$ Valley ground noise when switching High-to-Low
- $V_{OLP\text{-}LH}$ Peak ground noise switching Low-to-High
- $V_{OLV\text{-}LH}$ Valley ground noise switching Low-to-High

All four parameters can affect system reliability.

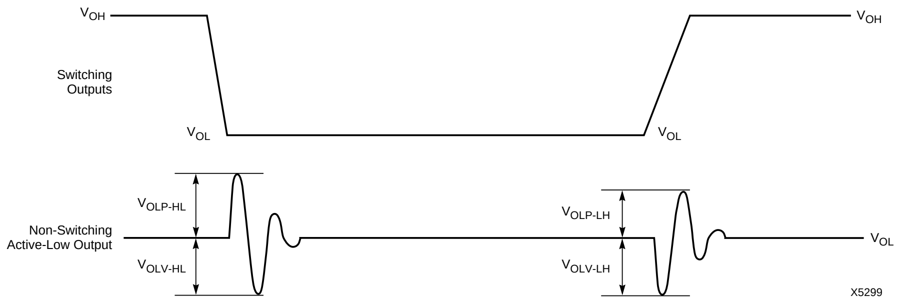


**Figure 3: Ground Bounce**

The two positive peak values can cause problems with a signal leaving the ground bounce chip, driving another chip. The positive ground bounce voltage is added to the $V_{OL}$, and may exceed the receiving input's noise margin. A continuously logic Low input may thus be interpreted as a short-duration High pulse.

The two negative valley parameters can cause problems with a signal arriving at the ground-bounce chip, reducing the Low-level noise immunity. The incoming voltage may not be Low enough, and may, therefore, be interpreted as a short-duration High input pulse.

**Table 3: Ground Bounce, 16 Outputs Switching, Each With 50 or 150 pF Load, $V_{CC}$ = 5.5 V**

| Load | Slew Rate | High-to-Low | | Low-to-High | | Unit |
|---|---|---|---|---|---|---|
| | | $V_{OLP}$ | $V_{OLV}$ | $V_{OLP}$ | $V_{OLV}$ | |
| 16 x 50 pF | Slow | 670 | 480 | 240 | 240 | mV |
| | Fast | 1,170 | 710 | 480 | 660 | mV |
| 16 x 150 pF | Slow | 740 | 330 | 210 | 280 | mV |
| | Fast | 1,180 | 420 | 350 | 710 | mV |

## Interpretation of the Results

Ground bounce is a linear phenomenon. When multiple outputs switch, the total ground bounce is the sum of the ground-bounce values caused by individual outputs switching. Since the actual switching of multiple outputs is usually not quite simultaneous, small timing differences between the switching outputs, caused by routing delays, can indirectly affect the amplitude. With low capacitive loading, < 50 pF, the peaks and valleys might even partially cancel each other. With larger capacitive loads, the tendency is for valleys to combine with valleys and peaks to combine with peaks.

In most devices tested, the load capacitance does not directly affect the ground-bounce **amplitude**, but it does affect the **duration** of the ground-bounce signals.

On the fastest outputs, minimal load capacitance created a ground-bounce resonant frequency of 340 MHz, with a half-cycle time of 1.5 ns. Such a signal exceeds 90% of its peak amplitude for about 0.4 ns.

With a 50 pF load on the switching outputs, the ground bounce resonant frequency is 90 MHz, with a half-cycle time of 5 ns, staying 1.7 ns above 90% of peak amplitude.

With a 150 pF load on the switching outputs, the ground bounce resonant frequency is 40 to 60 MHz, with a half-cycle time of 8 to 12 ns, staying 3 ns above 90% of peak amplitude.

The main problem with large load capacitances is not an increase in amplitude, but rather an increase in duration of the ground-bounce signal. The amplitude is mainly affected by the number of outputs switching simultaneously, and by the slew-rate mode of these outputs. Switching outputs closer to the monitoring output also cause larger peaks and valleys than outputs further away.

## Guidelines for Reducing Ground-Bounce Effects

- Minimize the impedance of the system ground distribution network and its connection to the IC pins. PQFPs are best suited, PGAs are worst, and PLCCs are in-between.
- Use PC-boards with ground- and $V_{CC}$-planes, connected directly to the ICs' supply pins. Place decoupling capacitors very close to these ground and $V_{CC}$ pins.
- Keep the ground plane as undisturbed as possible. A row of vias can easily cause a dynamic ground-voltage drop.
- Keep the clock inputs physically away from the outputs that create ground bounce, and connect clocks to input pins that are close to a ground pin. Make sure that all clock and asynchronous inputs have ample noise margin, especially in the Low state.
- If possible, avoid simultaneous switching by staggering output delays, e.g. through additional local routing of signals or clocks.
- Spread simultaneously switching outputs around the IC periphery. For a 16-bit bus, use two outputs each on either side of four ground pins.

# Ground-Bounce vs Delay Trade-Off

After the external sources of ground bounce have been reduced or eliminated. the designer can trade reduced ground bounce for additional delay by selecting between families and slew-rate options. Figure 4 shows the trade-off for 16 outputs switching simultaneously High-to-Low.

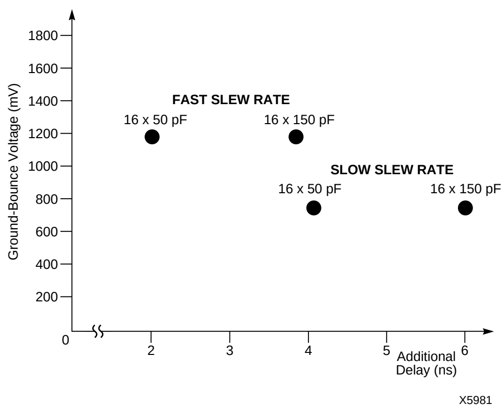


**Figure 4: Ground-Bounce vs. Delay Trade-off for 16 Outputs Switching 50 and 150 pF Each**

# XC4000 and XC4000E Power Consumption

Below are the dynamic power consumption values for typical design elements in XC4000 and XC4000E.

The differences between XC4000 and XC4000E are too small to be statistically relevant:

Global clocks in XC4000E are 3% higher, and Longlines and unloaded outputs in XC4000E are 5 to 10% lower than in XC4000.

Power consumption is given at nominal 5.0-V supply and 25˚C.

Power is proportional to the square of the supply voltage, but is almost constant over temperature changes. Power is given as “mW per million transitions per second”, since the more commonly used “MHz” can be ambiguous. When a 10-MHz clock toggles a flip-flop, the clock line obviously makes 20 MTps, the flip-flop output only 10 MTps.

The first six elements are device-size independent, i.e. they are applicable to all XC4000 or XC4000E devices operating at 5-V Vcc.

- One CLB flip-flop driving nothing but a neighboring flip-flop in the same or adjacent CLB (a typical shift register design):
  0.1 mW per million transitions per second =
  0.1 mW/MTps

- One CLB flip-flop driving its neighbor plus 9 lines of interconnect:
  0.2 mW per million transitions per second =
  0.2 mW/MTps

- One unloaded or unbonded TTL-level output:
  0.25 mW per million transitions per second =
  0.25 mW/MTps

- 50 pF on a TTL-level output: add 0.5 mW/MTps = 1.0 mW/MHz

- One unloaded or unbonded XC4000E CMOS-level output:
  0.31 mW per million transitions per second =
  0.31 mW/MTps

- 50 pF on a CMOS-level output: add 0.625 mW/MTps = 1.25 mW/MHz

The following elements are obviously device-size dependent:

- One Global Clock driving all CLB flip-flops, but no flip-flop changing:
  in XC4005: 4 mW/MTps = 8 mW/MHz
  in XC4010: 8 mW/MTps = 16 mW/MHz
  in XC4013: 12 mW/MTps = 24 mW/MHz
  in XC4020: 16 mW/MTps = 32 mW/MHz
  in XC4025: 20 mW/MTps = 40 mW/MHz

- One full-length horizontal or vertical Longline with one driving CLB source and one driven CLB load:
  in XC4005: 0.10 mW/MHz = 0.20 mW/MHz
  in XC4010: 0.15 mW/MTps = 0.30 mW/MHz
  in XC4013: 0.18 mW/MTps = 0.36 mW/MHz
  in XC4020: 0.20 mW/MTps = 0.40 mW/MHz
  in XC4025: 0.24 mW/MTps = 0.48 mW/MHz

These numbers do not account for the 10 mA of static power consumption when all device inputs are configured in TTL mode, which is always the default mode, and in XC4000 is actually the only user-accessible mode.

These numbers assume short rise and fall times on all inputs, avoiding the cross-current when both the n-channel pull-down and the p-channel pull-up transistor in the input buffer might conduct simultaneously.

**Tutorial Comments:**

In its pure form, a CMOS output driving a capacitive load has a power consumption that is independent of drive impedance or rise and fall time. For a full-swing signal, the power consumed when charging the capacitor is $C \times V^2 \times f$ where f is the frequency of charge operations. In each charge operation, half the total energy consumed ends up on the capacitor, and the other half of the energy is dissipated in the current-limiting resistor or transistor, whatever its value may be.

The subsequent discharge cycle does not take any new energy from the power supply, but dissipates in the current-limiting resistor/transistor all the energy that was formerly stored in the capacitor.

It is assumed here that the frequency is low enough so that the capacitors are completely charged and discharged in each half-cycle.