

W83194BR-250



STEPLESS CLOCK FOR VIA PRO266 CHIPSET

1.0 GENERAL DESCRIPTION

The W83194BR-250 is a Clock Synthesizer for VIA Pro266 chipset. W83194BR-250 provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, PCI, AGP, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

The W83194BR-250 provides I²C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.25% and 0.5% center type spread spectrum to reduce EMI.

The W83194BR-250 provides stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio. Also the skew of CPU and AGP clock outputs are programmable. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

The W83194BR-250 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50±5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

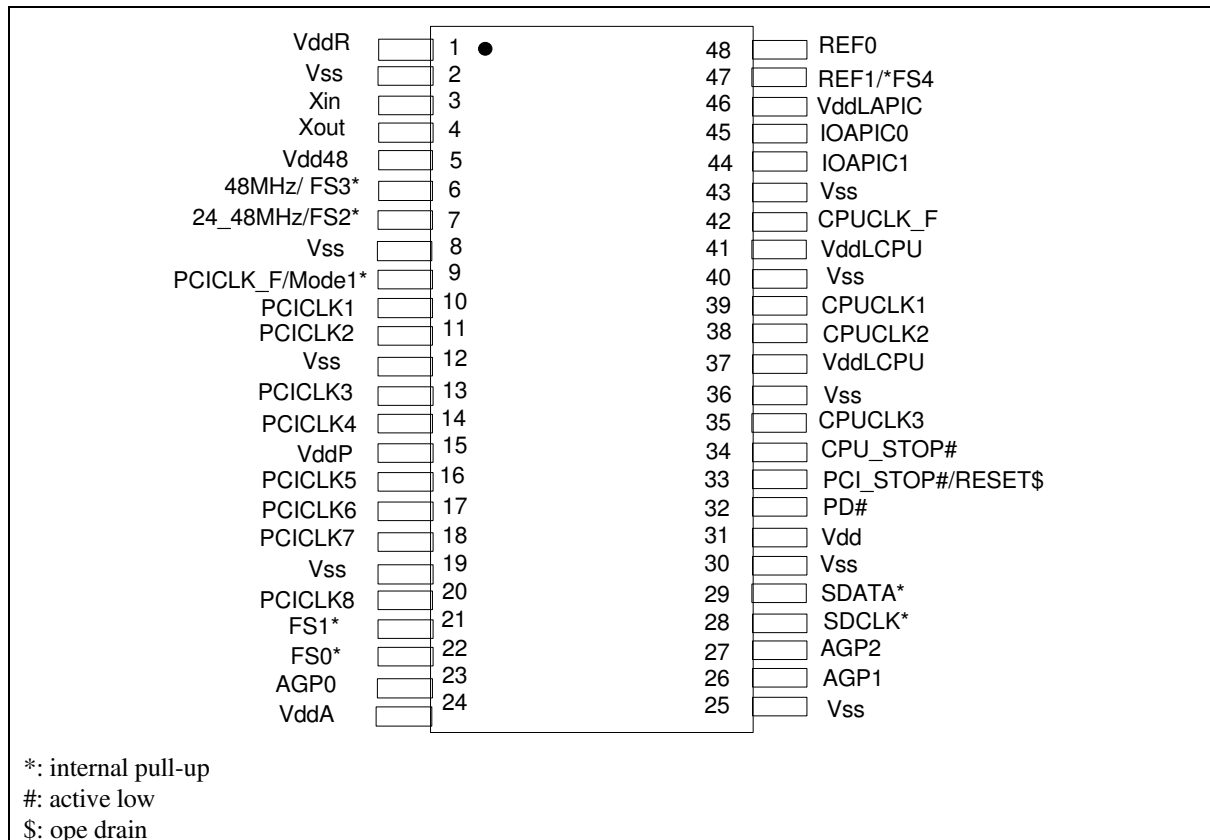
2.0 PRODUCT FEATURES

- 4 CPU clocks
- 3 AGP for chipset and AGP clocks
- 9 PCI synchronous clocks.
- Optional single or mixed supply:
(VddR = VddP= Vdd48 = VddA =Vdd = 3.3V, VddLAPIC=VddLCPU=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200 MHz
- I²C 2-Wire serial interface and I²C read back
- 0.25% and 0.5% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
- 48 MHz for USB
- 24 MHz for super I/O
- 48-pin SSOP package



PRELIMINARY

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up



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4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	3	IN	Crystal input with internal loading capacitors(36pF) and feedback resistors.
Xout	4	OUT	Crystal output at 14.318MHz nominally with internal loading capacitors(36pF).

4.2 CPU, AGP,PCI,IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F , [1:3]	42,39,38,35	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset. CPUCLK_F is the free running pin and does not affect by CPU_STOP#
CPU_STOP#	34	IN	CPU_STOP# when driven low.
PCI_STOP#/RESET\$	33	I/O	Pin9 *Mode1=1, PCI_STOP# when driven low. Pin9 *Mode1=0, RESET# output (4ms low active pulse when Watch Dog time out)
PD#	32	IN	Power Down mode when driven low.
IOAPIC[0:1]	45,44	OUT	Clock outputs synchronous with PCI clock and powered by VddLAPIC.
PCICLK_F/Mode1*	9	I/O	3.3V 33MHz free running PCI clock during normal operation. Latched input for Mode1* at initial power up for pin34 selection. *Mode1=1, pin 34 =CPU_STOP# when driven low. *Mode1=0, pin 34 = RESET# output (4ms low active pulse when Watch Dog time out)
PCICLK[1:8]	10,11,12,13,14,16,17,18,20	OUT	Low skew (< 250ps) PCI clock outputs.
AGP [0:2]	23,26,27	OUT	3.3V output clocks for the chipset.
*FS[1:0]	21,22	IN	H/W selecting the output frequency of CPU, AGP and PCI clocks (Default=1).



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4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
SDATA*	29	I/O	Serial data of I ² C 2-wire control interface
SDCLK*	28	IN	Serial clock of I ² C 2-wire control interface

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0	48	OUT	3.3V 14.318MHz reference clock.
REF1 / *FS4	47	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Latched input for FS4 at initial power up for H/W selecting the output frequency of CPU, AGP and PCI clocks (Default=1).
24_48MHz/FS2*	7	I/O	24MHz or 48MHz output clock. Latched input for FS42at initial power up for H/W selecting the output frequency of CPU, AGP and PCI clocks (Default=1).
48MHz_1/ FS3*	6	I/O	48MHz / Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, AGP and PCI clocks (Default=1).

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddLCPU,VddLAPIC	37,41,46	Power supply for CPU & IOAPIC, 2.5V or 3.3V.
Vdd48	5	Power supply for 48MHz output,3.3V.
VddA	24	Power supply for 3V_66 output, 3.3V.
VddP	15	Power supply for PCICLK, 3.3V.
VddR	1	Power supply for REFX2, 3.3V.
Vdd	31	Power for I2C CLK and DATA.
Vss	2,8,12,19,25,30,36,40,43	Circuit Ground.



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5.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU(MHz)	AGP(MHZ)	PCI(MHz)	IOAPIC
0	0	0	0	0	200.0	66.7	33.3	16.7
0	0	0	0	1	190.0	63.3	31.7	15.85
0	0	0	1	0	180.0	60.0	30.0	15
0	0	0	1	1	170.0	68	34	17
0	0	1	0	0	166.0	66.4	33.2	16.6
0	0	1	0	1	160.0	64.0	32.0	16
0	0	1	1	0	150.0	75.0	37.5	18.75
0	0	1	1	1	145.0	72.5	36.3	18.15
0	1	0	0	0	140.0	70.0	35.0	17.5
0	1	0	0	1	136.0	68.0	34.0	17
0	1	0	1	0	130.0	65.0	32.5	16.25
0	1	0	1	1	124.0	62.0	31.0	15.5
0	1	1	0	0	66.8	66.8	33.4	16.7
0	1	1	0	1	100.2	66.8	33.4	16.7
0	1	1	1	0	118.0	78.7	39.3	19.6
0	1	1	1	1	133.4	66.7	33.4	16.7
1	0	0	0	0	66.8	66.8	33.4	16.7
1	0	0	0	1	100.2	66.8	33.4	16.7
1	0	0	1	0	115.0	76.7	38.3	19.15
1	0	0	1	1	133.4	66.7	33.4	16.7
1	0	1	0	0	66.8	66.8	33.4	16.7
1	0	1	0	1	100.2	66.8	33.4	16.7
1	0	1	1	0	110.0	73.3	36.7	18.35
1	0	1	1	1	133.4	66.7	33.4	16.7
1	1	0	0	0	105.0	70.0	35.0	17
1	1	0	0	1	90.0	60.0	30.0	15
1	1	0	1	0	85.0	56.7	28.4	14.2
1	1	0	1	1	78.0	78.0	39.0	19.5
1	1	1	0	0	66.8	66.8	33.4	16.7
1	1	1	0	1	100.2	66.8	33.4	16.7
1	1	1	1	0	75.0	75.0	37.5	18.75
1	1	1	1	1	133.4	66.7	33.4	16.7

6.2.1 Register 0 : Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	0 = Normal 1 = Spread Spectrum enabled
6	0	-	SSEL2 (for frequency table selection by software via I ² C)
5	0	-	SSEL1 (for frequency table selection by software via I ² C)
4	0	-	SSEL0 (for frequency table selection by software via I ² C)
3	0	-	0 = Selection by hardware 1 = Selection by software I ² C - Bit 6:4, Bit2
2	0	-	SSEL4 (for frequency table selection by software via I ² C)
1	0	-	SSEL3 (for frequency table selection by software via I ² C)
0	0	-	0 = Running 1 = Tristate all outputs

6.2.2 Register 1 : CPU Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	44	IOAPIC1 (Active / Inactive)
6	1	45	IOAPIC0 (Active / Inactive)
5	1	47	REF1 (Active / Inactive)
4	1	48	REF0 (Active / Inactive)
3	1	35	CPUCLK3 (Active / Inactive)
2	1	38	CPUCLK2 (Active / Inactive)
1	1	39	CPUCLK1 (Active / Inactive)
0	1	42	CPUCLK_F (Active / Inactive)

6.2.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	20	PCICLK8 (Active / Inactive)
6	1	18	PCICLK7 (Active / Inactive)
5	1	17	PCICLK6 (Active / Inactive)
4	1	16	PCICLK5 (Active / Inactive)
3	1	14	PCICLK4 (Active / Inactive)
2	1	13	PCICLK3 (Active / Inactive)
1	1	11	PCICLK2 (Active / Inactive)
0	1	10	PCICLK1 (Active / Inactive)



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6.2.4 Register 3: 24MHz, 48MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	0	-	1 = $\pm 0.25\%$,0= $\pm 0.5\%$ Spread Spectrum Modulation
6	0	-	SEL24_48 (0=24Mhz, 1=48MHz)
5	1	6	48MHz (Active / Inactive)
4	1	7	24_48MHz (Active / Inactive)
3	1	9	PCICLK_F (Active / Inactive)
2	1	27	AGP2 (Active / Inactive)
1	1	26	AGP1 (Active / Inactive)
0	1	23	AGP0 (Active / Inactive)

6.2.5 Register 4: Buffer Chip Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	-	-	Reserved for W83176R-251
6	-	-	Reserved for W83176R-251
5	-	-	Reserved for W83176R-251
4	-	-	Reserved for W83176R-251
3	-	-	Reserved for W83176R-251
2	-	-	Reserved for W83176R-251
1	-	-	Reserved for W83176R-251
0	-	-	Reserved for W83176R-251

6.2.6 Register 5: Buffer Chip Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	-	-	Reserved for W83176R-251
6	-	-	Reserved for W83176R-251
5	-	-	Reserved for W83176R-251
4	-	-	Reserved for W83176R-251
3	-	-	Reserved for W83176R-251
2	-	-	Reserved for W83176R-251
1	-	-	Reserved for W83176R-251
0	-	-	Reserved for W83176R-251

6.2.7 Register 6: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	X	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

6.2.8 Register 7: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	0	-	Test 1 (Please do not modify)
5	1	-	Test 0 (Please do not modify)
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

6.2.9 Register 8: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

6.2.10 Register 9: Spread Spectrum Programming Register

Bit	@PowerUp	Pin	Description
7	0	-	Spread spectrum up count 3
6	0	-	Spread spectrum up count 2
5	0	-	Spread spectrum up count 1
4	0	-	Spread spectrum up count 0
3	0	-	Spread spectrum down count 3
2	0	-	Spread spectrum down count 2
1	0	-	Spread spectrum down count 1
0	0	-	Spread spectrum down count 0

6.2.11 Register 10: Divisor and Step-less Enable Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register to program frequency The equation is VCO freq. = 14.318MHz * (N+4)/ M
6	0	-	Reserved
5	X	-	Ratio SEL2
4	X	-	Ratio SEL1
3	X	-	Ratio SEL 0
2	1	-	CPU to AGP Skew 2
1	0	-	CPU to AGP Skew 1
0	0	-	CPU to AGP Skew 0

6.2.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	1	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	1	-	Winbond Chip ID
0	0	-	Winbond Chip ID



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6.2.13 Register 12: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	0	-	Winbond Chip ID
3	0	-	Winbond Version ID
2	0	-	Winbond Version ID
1	0	-	Winbond Version ID
0	1	-	Winbond Version ID

Reg10 Bit5	Reg10 bit4	Reg10 bit3	VCO/ CPU	VCO/ AGP	VCO/ PCI
SEL2	SEL1	SEL0	ratio	ratio	ratio
0	0	0	2	4	4
0	0	1	2	5	5
0	1	0	2	6	6
0	1	1	3	6	4
1	0	0	4	4	2
1	0	1	4	6	3
1	1	0	6	6	2
1	1	1	X	X	X

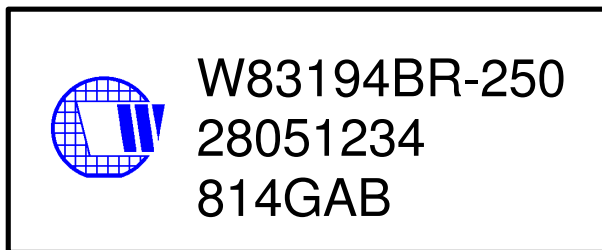


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7.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-250	48 PIN SSOP	Commercial, 0°C to +70°C

8.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-250

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

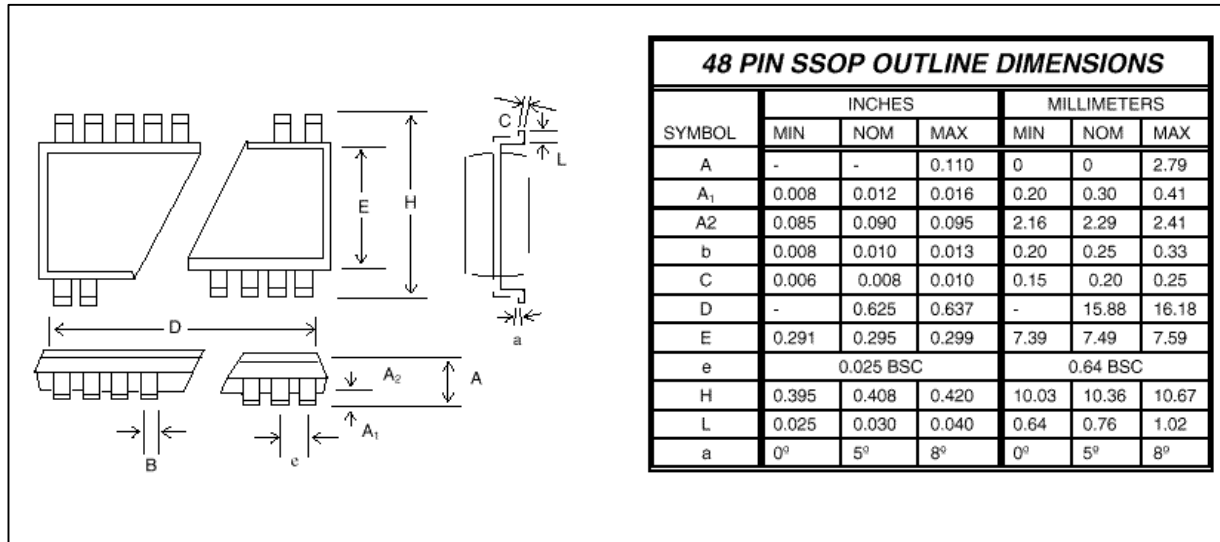
G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

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9.0 PACKAGE DRAWING AND DIMENSIONS



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