WD37C65C

Floppy Disk Subsystem Controller Device

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

The WD37C65C Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "superchip" integrates the following functions: formatter/controller, data separation, write precompensation, data rate selection (to a maximum of 1Mbit per second), and clock generation. It also provides interface drivers and receivers for the floppy drive.

The WD37C65C is functionally compatible pin-for-pin with the WD37C65A/B. In addition the WD37C65C supports a power down mode for laptop and portable systems. Refer to Table 16-6 for a descripion of functional differences between the WD37C65A/B and the WD37C65C.

On the disk drive interface, the WD37C65C includes data separation designed to address high performance error rates on floppy disk drives. It contains all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Write precompensation is included, in addition to the usual formatting, encoding/decoding, stepper motor control, and status sensing functions. All inputs are TTL compatible Schmitt Trigger line receivers, and outputs are high current, open drain, with 48 mA drivers which meet the ANSI specification.

The host interface supports an 8 or 12 MHz, 286 microprocessor bus without the use of wait states. The inputs are Schmitt Triggers. Output drive capability is 20 LSTTL loads, allowing direct interconnection to bus structures without the use of buffers or transceivers. For PC, PC AT and EISA applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and stepper motor control have been output ports of the host processor architecture. In the WD37C65C, these functions are latched into registers addressed within the I/O mapping of the system. The WD37C65C has eight internal registers. The eight bit main status register contains status information about the WD37C65C and may be accessed any time. Another four status registers under system control also give various status and error information. The Control Register provides support logic that latches the two LSBs used to select the desired data rate that controls internal clock generation. The Operations Register replaces the standard latched port used in floppy subsystems. These registers are incorporated into the WD37C65C.

All Clock Generation: SCLK - Sampling Clock, WCLK-Write Clock, and MCLK - Master Clock, are included in the WD37C65C. XTAL oscillator circuits provide the necessary signals for internal timing when using the 44-pin PLCC. If the 40-pin DIP is used, the TTL level clock inputs must be provided. There are two oscillator inputs to the WD37C65C. The first at 32 MHz that handles all standard data rates (1 MB/s, 500, 250, and 125 kb/s or 16 MHz to handle 500, 250, and 125 Kb/s). The second oscillator is at 9.6 MHz to support the 300 kb/sec data rate used in PC AT designs.

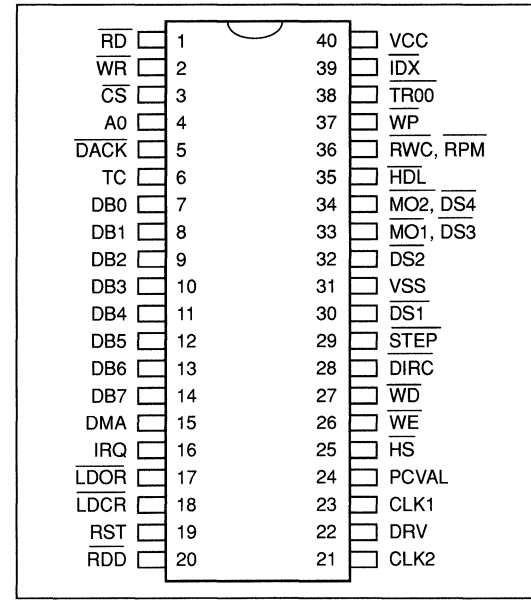
Some AT compatibles use two-speed disk drives. If a two-speed disk drive is used, the DRV input should be grounded along with the CLK2 input.

1.1 FEATURES

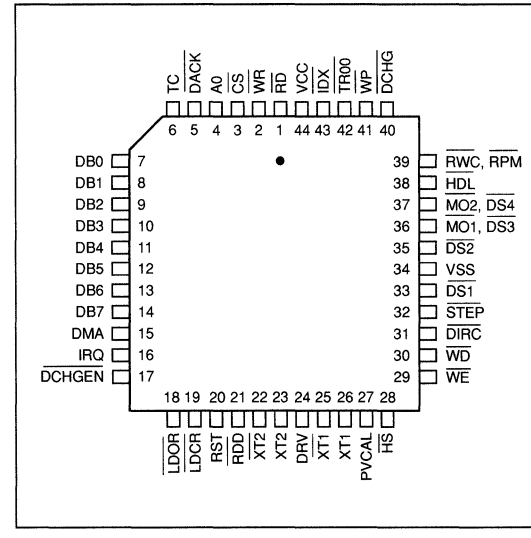
- IBM PC AT compatible format (single and double density)
  - —Provides "on chip" floppy control and operations
  - —Provides required signal qualification to DMA channel when in PC AT mode
  - —BIOS compatible
  - —Supports dual speed spindle drives
- CMOS low power consumption (typically 300 mW at 32 MHz)
- Power down mode with low standby current (ICC = 100 µA maximum)
- Address mark detection circuitry (internal to floppy disk controller)
- Multi-sector and multi-track transfer capability
- Direct floppy disk drive interface (no buffers needed)
  - —48 mA sink output drivers
  - —Schmitt Trigger line receivers

26

- Compatible with PD8080/85, PD8086, 8088, 80286, 80386SX, 80386, and PD780 (Z80) microprocessors
- On chip clock generation
- Two TTL clock inputs for 40-pin DIP
- Two XTAL oscillator circuits for 44-pin PLCC
- Automatic write precompensation
  - —Disable option
  - —Pin selectable inner track values of 125 or 187 nanoseconds
- Integrated high-performance DPLL data separator
  - —Industry standard error rates of 10<E-9
  - —Data rates of 125, 250, 300, 500 Kbits/second and 1Mbit/second
  - —Option to select 150 Kbits/second FM and 300 Kbits/second MFM data rates only
- Enhanced host interface
  - —20 LSTTL output drive capability
  - —TTL Schmitt trigger inputs
- User programmable track stepping rate and head load/unload times
- Supports four floppy or Micro Floppydisk drives with external decode logic
- Data transfer in DMA or non-DMA mode
- Parallel seek operation on a maximum of four drives
- Internal power up reset circuitry
- Single +5V DC power supply



40 PIN DIP



44 PIN PLCC

2.0 SIGNAL DESCRIPTIONS

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1 /1	$\overline{RD}$	$\overline{READ}$	I	Control signal for transfer of data or status onto the data bus by the WD37C65C.
2/2	$\overline{WR}$	$\overline{WRITE}$	I	Control signal for latching data from the bus into the WD37C65C Buffer Register.
3/3	$\overline{CS}$	$\overline{CHIP\ SELECT}$	I	Selected when 0 (low) allowing $\overline{RD}$ or $\overline{WR}$ operation from the host.
4/4	A0	ADDRESS LINE	I	Address line selecting data (=1) or status (=0) information. (A0 = logic 0 during $\overline{WR}$ is illegal except in Power Down mode.)
5/5	$\overline{DACK}$	$\overline{DMA\ ACKNOWLEDGE}$	I	Used by the DMA controller to transfer data from the WD37C65C onto the bus. Logical equivalent to $\overline{CS}$ and A0=1. In Special or AT/EISA mode, this signal is qualified by DMAEN from the Operations Register.
6/6	TC	TERMINAL-COUNT	I	This signal indicates to WD37C65C that data transfer is complete. If DMA operational mode is selected for command execution, TC will be qualified by $\overline{DACK}$, but not in the programmed I/O execution. In AT/EISA or Special mode, qualification by $\overline{DACK}$ requires the Operations Register signal DMAEN to be logically true. Note also that in AT/EISA mode, TC will be qualified by $\overline{DACK}$, whether in DMA or non-DMA host operation. Programmed I/O in AT/EISA mode will cause an abnormal termination error at the completion of a command.
7-14/ 7-14	DB0 thru DB7	DATA BUS 0 thru DATA BUS 7	I/O	8-Bit, bi-directional, tristate, data bus. D0 is the least significant bit (LSB). D7 is the most significant bit (MSB).
15/15	DMA	DIRECT MEMORY ACCESS	O	DMA request for byte transfers of data. In Special or AT/EISA mode, this pin is tristated, enabled by the DMAEN signal from the Operations Register. This pin is driven in the Base mode.
16/16	IRQ	INTERRUPT	O	Interrupt request indicating the completion of command execution or data transfer requests (in non-DMA mode). Normally driven in base mode. In Special or AT/EISA mode, this pin is tristated, enabled by the DMAEN signal from the Operations Register.

TABLE 2-1. SIGNAL DESCRIPTION

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

26

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
/17	DCHGEN*	DISK CHANGE ENABLE	I	This input must be at Logic = 0 to enable DCHG input status at pin 40 to be placed on bit 7 of the data bus during a RD = 0 of LDCR = 0. It has Internal pull-up.
17/18	LDOR	LOAD OPERATIONS REGISTER	I	Address decode which enables the loading of the Operations Register. Internally gated with WR creates the strobe which latches the data bus into the Operations Register.
18/19	LDCR	LOAD CONTROL REGISTER	I	Address decode which enables loading of the Control Register. Internally gated with WR creates the strobe which latches the two LSBs from the data bus into the Control Register.
19/20	RST	RESET	I	Resets controller, placing microsequencer in idle. Resets device outputs. Puts device in Base mode, not PC AT or Special mode.
20/21	RDD	READ DISK DATA	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
21/	CLK2	CLOCK2	I	TTL level clock input used for non-standard data rates; is 9.6 MHz for 300 kb/s, and can only be selected from the Control Register.
/22	XT2	XTAL2	0	XTAL oscillator drive output for 44-pin PLCC (See Figure 6). Should be left floating if TTL inputs used at pin 23.
/23	XT2	XTAL2	I	XTAL oscillator input used for non-standard data rates. It may be driven with a TTL level signal.
22/24	DRV	DRIVE TYPE	I	Drive type input indicates to the device that a twospeed spindle motor is used if logic is 0. In that case, the second clock input will never be selected and must be grounded.
23/	CLK1	CLOCK1	I	TTL level clock input is used to generate all internal timings for standard data rates. Frequency must be 16MHz ± 0.1% or 32MHz ± 0.1%, and may have 40/60 or 60/40 duty cycle.
/25	XT1	XTAL1	0	XTAL oscillator drive output for 44-pin PLCC (See Figure 6). Should be left floating if TTL inputs are used at pin 26.
/26	XT1	XTAL1	I	XTAL oscillator input requiring 16 MHz or 32 MHz crystal. This oscillator is used for all standard data rates, and may be driven with a TTL level signal.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
24/27	PCVAL	PRECOMPENSATIONVALUE	I	Precompensation value select input. This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125 ns, Logic 0 = 187 ns. If the defeat option is used, PCVAL is unimportant and precompensation is disabled.
25/28	$\overline{HS}$	$\overline{HEAD\ SELECT}$	O	High current driver (HCD) output selects the head (side) of the floppy disk that is being read or written. Logic 1 = side 0. Logic 0 = side 1.
26/29	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
27/30	$\overline{WD}$	$\overline{WRITE\ DATA}$	O	This HCD output is $\overline{WRITE\ DATA}$. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
28/31	$\overline{DIRC}$	$\overline{DIRECTION}$	O	This HCD output determines the direction of the head stepper motor. Logic 1 = outward motion. Logic 0 = inward motion.
29/32	$\overline{STEP}$	$\overline{STEP\ PULSE}$	O	This HCD output issues an active low pulse for each track to track movement of the head.
30/33	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	This HCD output, when active low, is $\overline{DRIVE\ SELECT\ 1}$ in AT/EISA mode. It enables the interface to this disk drive. This signal comes from the Operations Register. In Base, or Special mode, this output is #1 of the four decoded Unit Selects, as specified in the device command syntax.
31/34	VSS	GROUND	--	Ground.
32/35	$\overline{DS2}$	$\overline{DRIVE\ SELECT\ 2}$	0	This HCD output, when active low, is $\overline{DRIVE\ SELECT\ 2}$ in AT/EISA mode, enables the interface to this disk drive. This signal comes from the Operations Register. In Base or the Special mode, this output is #2 of the four decoded Unit Selects as specified in the device command syntax.
33/36	$\overline{MO1}$, $\overline{DS3}$	$\overline{MOTOR\ ON\ 1}$, $\overline{DRIVE\ SELECT\ 3}$	0	This HCD output, when active low, is MOTOR ON enable for disk drive #1, in AT/EISA mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #3 of the four decoded Unit Selects as specified in the device command syntax.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
34/37	$\overline{MO2}$, $\overline{DS4}$	$\overline{MOTOR\ ON\ 2}$, $\overline{DRIVE\ SELECT\ 4}$	0	This HCD output, when active low, is MOTOR ON enable for disk drive #2, in AT/EISA mode. This signal comes from the Operations Register. In the Base or Special mode, this output is #4 of the four decoded Unit Selects as specified in the device command syntax.
35/38	$\overline{HDL}$	$\overline{HEAD\ LOADED}$	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
36/39	$\overline{RWC}$, $\overline{RPM}$	$\overline{REDUCED\ WRITE\ CURRENT}$, $\overline{REVOLUTIONS\ PER\ MINUTE}$	O	This HCD output, when active low, causes a REDUCED WRITE CURRENT, when bit density is increased toward the inner tracks, becoming active when tracks >28 are accessed. This condition is valid for Base or Special mode, and is indicative of when write precompensation is necessary. In the AT/EISA mode, this signal will be active when CR0=1.
/40	$\overline{DCHG}$*	$\overline{DISK\ CHANGE}$	I	This Schmitt Trigger (ST) input senses status from the drive. Active low indicates that drive door is open or that the diskette has possibly changed since the last drive selection. It has internal pull-up.
37/41	$\overline{WP}$	$\overline{WRITE\ PROTECTED}$	I	This ST input senses status from the disk drive indicating active low when a diskette is WRITE PROTECTED.
38/42	$\overline{TR00}$	$\overline{TRACK\ 00}$	I	This ST input senses status from disk drive, indicating active low when the head is positioned over the outermost track, TRACK 00.
39/43	$\overline{IDX}$	$\overline{INDEX}$	I	This ST input senses status from the disk drive, indicating active low when the head is positioned over the beginning of a track marked by an index hole.
40/44	VCC	+5VDC	--	Input power supply.

TABLE 2-1. SIGNAL DESCRIPTION (CONTINUED)

*Only in the PLCC version of the WD37C65C. Not connected in the DIP package.

3.0 ARCHITECTURE

The WD37C65C Floppy Disk Subsystem Controller is an LSI device that provides all the needed functionality between the host processor and the floppy disk drive. This "superchip" integrates: formatter/controller, data separation, write precompensation, data rate selection, clock generation, drive interface drivers and receivers.

Figure 3-1 illustrates a block diagram of the WD37C65C Floppy Disk Subsystem Controller.

Figure 3-2 illustrates a typical WD37C65C system.

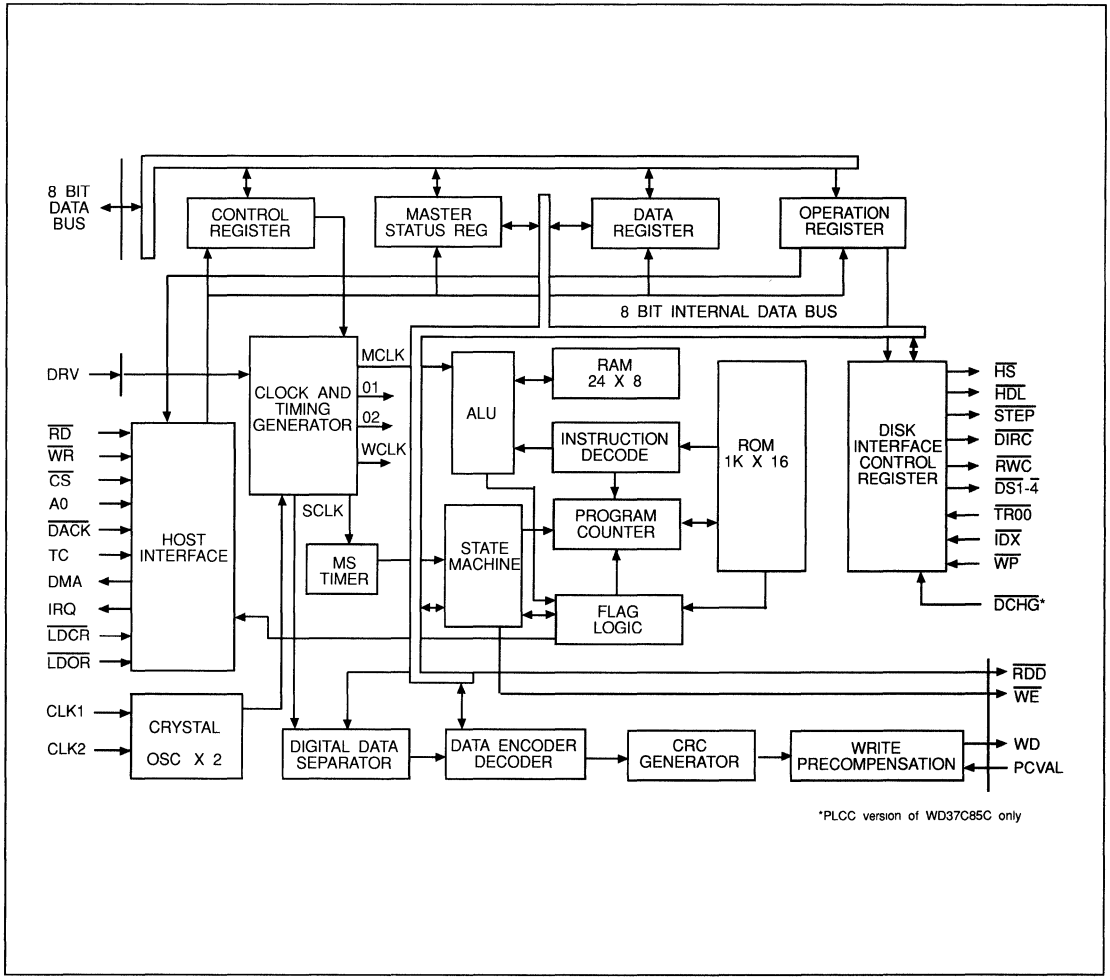


FIGURE 3-1. WD37C65C BLOCK DIAGRAM

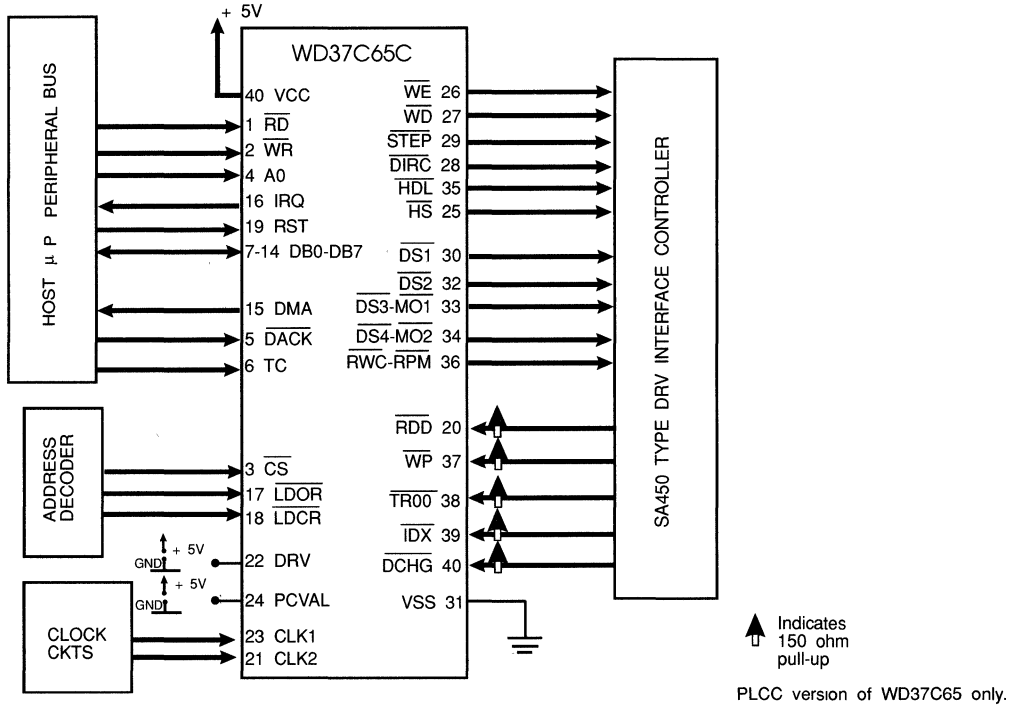


FIGURE 3-2. TYPICAL WD37C65 SYSTEM

4.0 HOST INTERFACE

The host interface is the Host Microprocessor Peripheral Bus. This bus is composed of eight control signals and eight data signals. In the Special or AT/EISA modes, IRQ and DMA request are tri-stated and qualified by DMA enable which is provided by the Operations Register. The data bus, DMA, and IRQ outputs are designed to handle 20 LSTTL loading. Inputs are Schmitt Trigger receivers and can be hooked up to a bus or backplane without any additional buffering.

During the Command or Result phases, the Main Status Register must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data is read from or written into the Data Register, the CPU waits for 12 µs before reading the Main Status Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the WD37C65C. Many of the commands require multiple bytes. As a result, the Main Status Register must be read prior to each byte transfer to the WD37C65C. During the Result phase, Bits D6 and D7 in the Main Status Register must both be 1's (D6=1 and D7=1) before reading each byte from the Data Register. Note that this reading of the Main Status Register before each byte transfer to the WD37C65C is required only in the Command and Result phases, and not during the Execution phase. Note also that DB6 and DB7 in the MSR can be polled instead of waiting 12 µs.

During the Execution phase, the Main Status Register need not be read. If the WD37C65C is in the non-DMA Mode, then the receipt of each data byte (WD37C65C is reading data from the FDD) is indicated by an interrupt signal on pin 16 (IRQ=1). The generation of a Read signal ($\overline{RD}$ = 0) clears the interrupt and sends the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13 µs for the MFM mode and 27 µs for the FM mode), then it may poll the Main Status Register and bit D7 (RQM) functions as the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

All timings mentioned above double for mini floppy data rates.

Note that in the non-DMA mode it is necessary to examine the Main Status Register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the WD37C65C is in the DMA mode, no interrupt signals are generated during the Execution phase. The WD37C65C generates DMA's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both $\overline{DACK}$=0 (DMA Acknowledge) and an $\overline{RD}$=0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$=0), the DMA Request is cleared (DMA= 0) If a Write Command has been issued, then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution phase has been completed (Terminal Count has occurred) or the EOT sector read/written, then an Interrupt will occur (IRQ = 1). This signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (IRQ = 0).

Note that in PC AT usage, non-DMA Host transfers are not the normal procedure. If the user chooses to do so, the WD37C65C will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive $\overline{DACK}$.

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect durinq DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to Vcc. Note that during the Result phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has several bytes of data in the Result phase. All seven bytes must be read in order to successfully complete the Read Data command. The WD37C65C will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result phase. The WD37C65C contains five Status Registers. The Main Status Register mentioned may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and may be read only afler completing a command. The particular command that has been executed

determines how many of the Status Registers will be read.

The bytes of data which are sent to the WD37C65C to form the Command phase, and are read out of the WD37C65C in the Result phase, must occur in the order shown in the Command Table. The command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the WD37C65C, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the WD37C65C is ready for a new command.

5.0 CONTROL REGISTER

The Control Register is a write only register that is used to set the data transfer rate and disable write precompensation. It provides support logic that latches the two LSBs of the data bus upon receiving LDCR and WR. CS should not be active when this happens. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally "deglitched," allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock or crystal. The frequency must be 64 times the desired MFM data rate. This implies a maximum data rate of 250 kb/s for a frequency of 16 MHz or a maximum data rate of 500 Kb/s for a frequency of 32 MHz, unless the Control Register is used. Switching of this clock must be "glitchless" or the device will need to be reset. Table 5-1 and Table 5-2 present the Control Register configuration for 16 MHz and 32 MHz frequencies, respectively.

The WD37C65C optionally supports 150 kb/s FM data transfer rate. The Control Register configuration is shown in Table 5-3. The 150 kb/s data rate can be selected by using a 9.6 MHz XTAL or TTL level clock input on pin 26 (44-pin PLCC) or pin 23 (40-pin DIP). Only two data transfer rates can be selected with this configuration: 150 kb/s FM and 300 kb/s MFM.

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA MODE)
0	0	x	500 K	MFM	1
0	0	x	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM,(9.6 MHz XTAL)	0
1	0	x	250 K	MFM, RST Default	1
1	0	x	125 K	FM, RST Default	1

TABLE 5-1. CONTROL REGISTER CONFIGURATION - 16 MHZ

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISAMODE)
0	0	x	1 M	MFM	1
0	0	x	500 K	FM	1
0	1	0	500 K	MFM	0
0	1	1	300 K	MFM,(9.6 MHz XTAL)	0
1	0	x	500 K	MFM, RST Default	1

TABLE 5-2. CONTROL REGISTER CONFIGURATION - 32 MHz

In AT/EISA mode, write precompensation can be disabled by a logic high on bit 2 of the Control Register. (See Table 5-4).

CR1	CR0	DRV	DATA RATE	COMMENTS	RPM (AT/EISA MODE)
0	0	x	300 K	MFM	1
0	0	x	150 K	FM	1

TABLE 5-3. CONTROL REGISTER CONFIGURATION - OPTIONS

Bit	SIGNAL NAME AND FUNCTION	RESET CONDITION	CLOCK QUALIFIER
0	Data Rate	0	None
1	Data Rate	0	None
2	No Write Precompensation	0	None
3-7	Reserved	None	None

TABLE 5-4. CONTROL REGISTER CONFIGURATION - AT/EISA MODE

6.0 MASTER STATUS REGISTER

The Master Status Register is an eight-bit, read/write register that contains the status information of the FDC. It can be accessed at any time. The WD35C65C provides a write only register, called Master Status Register 1 (MSR1) which is used only to select power down mode. In power down mode the XTAL oscillator, controller circuitry and all linear circuitry are turned off so that the controller draws very low current. Normal operation is restored by asserting reset to the WD37C65C. See Master Status Register 1.

Only the Master Status Register may be read and used to facilitate the transfer of data between the processor and WD37C65C. The DIO and RQM bits in the Master Status Register indicate when data is ready and in which direction data will be transferred on the data bus. The maximum time between the last RD or WR during a Command or Result phase and the setting of DIO and RQM is 12 µs if 500 kb/s MFM data rate is selected. (If 250 kb/s MFM is selected, the delay is 24 µs. If 1 Mb/s is selected, the delay is 6 µs.) For this reason, everytime the Master Status Register is read, the CPU should wait 12 µs. The maximum time from the trailing edge of the last RD in the result phase to when DB4 (FDC busy) goes low is 12 µs.

The bits in the Master Status Register are listed in Table 6-1. The bits in Status Register 0 are listed in Table 6-2.The bits in Status Register 1 are listed in Table 6-3.The bits in Status Register 2 are listed in Table 6-4.The bits in Status Register 3 are listed in Table 6-5.

6.1 MASTER STATUS REGISTER 1 (MSR1--WRITE ONLY)

The WD37C65C will enter power down mode, when bit 0 of MSR1 is set to logical "1" and the following conditions are met:

1. The RST pin to the FDC is inactive.

2. Bit 2 in the Operations Register is "SRST/= 1".

3. The WD37C65C is awaiting a command from the host.

The WD37C65C can also be programmed with external logic to automatically enter power down mode a few milliseconds after the beginning of idle mode.

Normal operation is restored when the RST pin to the FDC is active and the FDC is reset. This in turn resets bit 0 of MSR1 register to logic 0.
The bits in the Master Status Register are listed in Table 6-2.

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION	CLOCK QUALIFIER
0	Power down mode (PDM)	0	None
1-7	Reserved	None	None

TABLE 6-1. AT/EISA MODE. MASTER STATUS REGISTER 1 CONFIG.

BIT NO.	NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number is 0 in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in the Seek Mode. If any of the bits is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to the processor. If DIO=0, then transfer is from the processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and '"direction" to the processor.

TABLE 6-2. STATUS REGISTER 0 BITS

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
D7	INTERRUPT CODE	IC	D7=0 and D6=0. Normal termination of command was completed and properly executed. D7=0 and D6=1. Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
D6	---	---	D7=1 and D6=0. Invalid command issue, (IC). Command which was issued was never started.
D5	SEEK END	SE	When the FDC completes the SEEK command, this flag is set to 1 (high).
†D4	EQUIPMENT CHECK	EC	If the Track 0 signal fails to occur after 77 step pulses per Recalibrate Command, then this flag is set.
†D3	NOT READY	NR	Since drive Ready is always presumed true, this will always be a logic 0.
D2	HEAD SELECT	HS	This flag is used to indicate the state of the head at interrupt.
D1	UNIT SELECT 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
D0	UNIT SELECT 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.

TABLE 6-3. STATUS REGISTER 1 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	END OF CYLINDER	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D6	---	---	Not used. This bit is always 0 (low).
D5	DATA ERROR	DE	When the FDC detects a *CRC error in either the ID field or the data field, this flag is set.
D4	OVERRUN	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D3	---	---	Not used. This bit is always 0 (low).
D2	NO DATA	ND	During execution of READ DATA, WRITE DELETED DATA, or SCAN command, if the FDC cannot find the sector specified in the **IDR Register, this flag is set. During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set. During execution of the READ A TRACK command, if the starting sector cannot be found, then this flag is set.
D1	NOT WRITEABLE	NW	During execution of WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK commands, if the FDC detects a $\overline{WP}$ signal from the FDD, then this flag is set.
D0	MISSING ADDRESS MARK	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. At the same time the MD (Missing Address Mark in data field) of Status Register 2 is set.

TABLE 6-4. STATUS REGISTER 2 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
D7	---	---	Not Used. This bit is always 0 (low).
D6	CONTROL MARK	CM	During execution of the READ DATA or SCAN Command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D5	DATA ERROR	DD	If the FDC detects a CRC error in the data field, then this flag is set.
D4	WRONG CYLINDER	WC	This bit is related to the ND bit, and when the contents of * * *C on the medium is different from that stored in the IDR, this flag is set.
D3	SCAN EQUAL	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D2	SCAN NOT	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D1	BAD CYLINDER	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF, then this flag is set.
D0	MISSING ADDRESS MARK IN DATA FIELD	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.

TABLE 6-5. STATUS REGISTER 3 BITS

BIT NO.	NAME	SYMBOL	DESCRIPTION
†D7	---	---	Not used. Will always be logic 0.
D6	WRITE PROTECTED	$\overline{WP}$	This bit is used to indicate the status of the WRITE PROTECTED signal from the FDD.
†D5	READY	RY	This bit will always be a logic 1. Drive is presumed to be ready.
D4	TRACK 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
†D3	WRITE PROTECTED	$\overline{WP}$	This bit is used by the WD37C65C to indicate the status of the WRITE PROTECTED signal from the FDD.
D2	HEAD SELECT	HS	This bit is used to indicate the status of the Side Select signal to the FDD.
D1	UNIT SELECT 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D0	UNIT SELECT 2	US0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

TABLE 6-6. MASTER STATUS REGISTER BITS

* CRC - Cyclic Redundancy Check

* * IDR - Internal Data Register

* * * C - Cylinder

† - Different from NEC765

7.0 DATA REGISTER

The eight-bit Data Register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command.

The relationship between the Master Status Register and the Data Register and the signals RD, WR, and A0 are shown in Table 7-1.

A0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

TABLE 7-1. MASTER STATUS AND DATA REGISTERS RELATIONSHIPS

8.0 OPERATIONS REGISTER

The Operations Register provides support logic that latches the data bus upon receiving LDOR and WR. CS should not be active when this happens. The Operations Register replaces the typical latched port found in floppy subsystems used to control disk drive spindle motors and to select the desired disk drive. Table 8-1 represents the Operations Register.

NO.	SYMBOL	DESCRIPTION
OR0	DSEL	Drive Select, if low and MOEN1 = 1, then DS1 is active. If high and MOEN2 = 1, then DS2 is active, but only in the AT/EISA mode.
OR1	(x)	This must be a logic O for DS1 and DS2 to become active.
OR2	SRST	Soft reset, active low.
OR3	DMAEN	DMA enable, active in Special and AT/EISA modes. Qualifies DMA and IRQ outputs and DACK input.
OR4	MOEN1	Motor On enable, inverted output M01 is active only in AT/EISA mode.
OR5	MOEN2	Motor On enable, inverted output M02 is active only in AT/EISA mode.
OR6	(X)	Has no defined function. A spare.
OR7	(MSEL)	Mode Select. During a soft reset condition, may be used to select between Special mode (1) and AT/EISA mode (0).

TABLE 8-1. OPERATIONS REGISTER

9.0 BASE, SPECIAL, AND AT/EISA MODES

Base, Special, PC AT and EISA modes allow subtle differences which the user may find desirable. The Control Register may be used in any mode without altering functionality.

9.1 BASE MODE

After a hardware reset, RST active, the WD37C65C will be held in soft reset, SRST active, with the normally driven signals, DMA request and IRQ request outputs tristated. Base mode may be initiated at this time by a chip access by the host. Although this may be any read or write, it is strongly recommended that the Base mode user's first chip access be a read of the Master Status Register. Once Base mode is entered, the soft reset is released, and IRQ and DMA are driven. Base mode prohibits the use of the Operations Register, hence there can be no qualifying by DMAEN and no soft resets. The Drive Select outputs, DS1 to DS4, offer a 1 of 4 decoding of the Unit Select bits resident in the command structure. Pin RWC represents Reduce Write Current and is indicative of when write precompensation is necessary.

9.2 SPECIAL MODE

Special mode allows use of the Operations Register for the DMAEN signal as a qualifier and to do a software driven device reset, SRST. To enter Special mode, the Operations Register is loaded with (1 X 0 0 X 0 X X), setting mode Select to a logic 1 disabling MOEN1 and MOEN2 and causing SRST to be active. Then a read of the Control Register address, LDCR and RD, places the device in Special mode. The DS1 through DS4 is again offered in this mode, as is RWC.

9.3 AT/EISA MODES

For AT/EISA compatibility, users write to the Operations Register, LDOR and WR; this action, performed after a hardware reset, or in the Base mode, initiates AT/EISA mode. AT/EISA mode can also be entered from Special mode by loading the Operations Register with (0 X 0 0 X 0 X X), setting Mode Select to a logic 0, disabling MOEN1 and MOEN2, and causing SRST to be active. Then a read of the Control Register address sets the device into AT/EISA mode. The DS outputs are replaced with the DSEL and MOEN signals buffered from the Operations Register. DMAEN and SRST are supported and compatible with the current BIOS. RWC pin function is now RPM so that users with two-speed drives may reduce spindle speed from a nominal 360 revolutions per minute to 300 revolutions per minute when active low. It can also be used to reduce write current when a slower data rate is selected for a given drive. Figure 9-1 illustrates the relationship among the three modes.

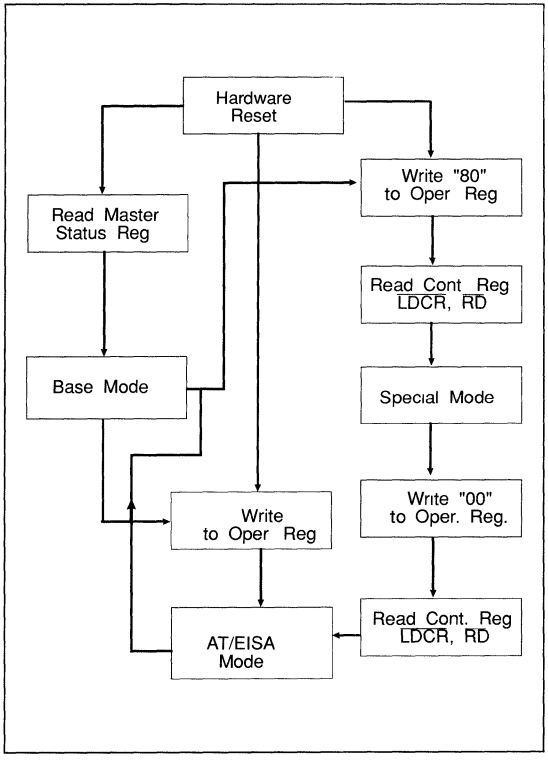


FIGURE 9-1. FLOW DIAGRAM BASE, SPECIAL & AT/EISA MODES

26

10.0 POLLING ROUTINE

After any reset the WD37C65C, (a hard RST or soft SRST), will automatically go into a Polling routine. In between commands (and between step pulses in the SEEK Command), the WD37C65C polls all four FDDs looking for a change in the Ready line from any of the drives. Since the drive is always presumed Ready, an interrupt will only be generated following a reset. This occurs because a reset forces Not Ready status, which then promptly becomes Ready. Note that in Special, AT/EISA modes, if DMAEN is not valid 1 ms after reset goes inactive, then IRQ may be already set and pending when finally enabled onto the bus. The polling of the Ready line by the WD37C65C occurs continuously between commands. Each drive is polled every 1.024 ms, except during the READ/WRITE commands. For mini-floppies, the polling rate is 2.048 ms. The drive polling sequence is 1-2-4-3. Note that in the AT/EISA mode, the user will not see the polling at the Drive Select signals. Figure 10-1 illustrates the Drive Select Polling Timing.

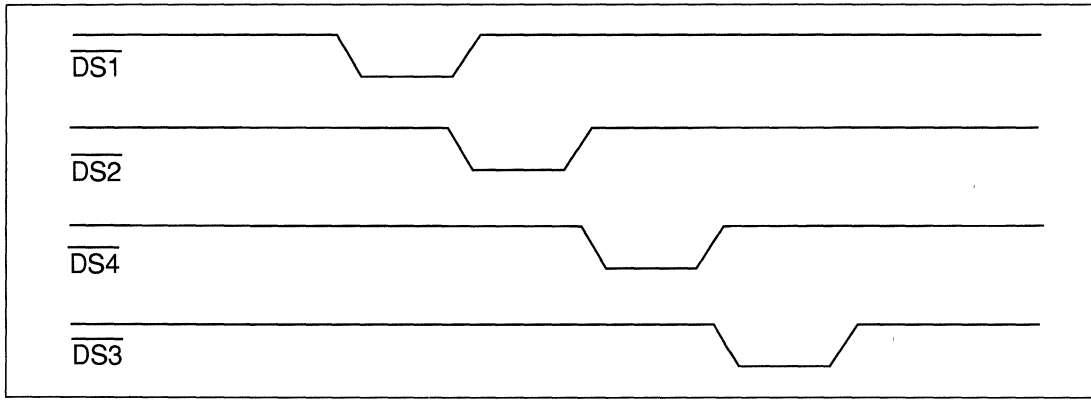


FIGURE 10-1. DRIVE SELECT POLLING TIMING

11.0 DEVICE RESETS

The WD37C65C supports both hardware reset (RST) pin (19) and a software reset (SRST) through use of the Operations Register. The RST pin will cause a device reset for the active duration. RST causes a default to Base mode, and selects 250 Kb MFM (or 125 Kb FM, code dependent) as the data rate (16 MHz input clock). The default data rate for a 32 MHz input clock is 500 Kb MFM. SRST will reset the microcontroller as did the RST, but will not affect the current data rate selection or the mode. RST, when active, will disable the high current driver outputs to the disk drive. RST and SRST will not affect the values set for the internal timers - HUT, HTL, and SRT.

If the XTAL oscillators are used, instead of the TTL driven clock inputs, the hardware RST active time requirement will be extended. The oscillator circuit is designed so that RST will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

12.0 DATA SEPARATOR

The Data Separator is a WD92C32 Digital Phase Lock Loop Floppy Disk Data Separator (DPLL). It was designed to address high performance error rates on floppy disk drives, and to provide superior performance in terms of available bit jitter tolerance. It contains the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Figure 3-1 illustrates the WD92C32 used as the Data Separator in the WD37C65C system. Figure 13-1 illustrates the WD92C32 simplified block diagram. The bit jitter tolerance for the data separator is 60%, which guarantees an error rate of <10E-9.

13.0 WRITE PRECOMPENSATION

The WD37C65C maintains the standard first level algorithm to determine when write precompensation should be applied. The EARLY and LATE signals are used internally to select the appropriate delay in the write data pulse stream. The encoded WRITE DATA signal is synchronized to the 16 MHz or 32 MHz clock if this is the frequency on CLK1 pin (23), and clocked through a shift register. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has a 25% duty cycle, i.e., one fourth of the bit cell period, and equal to one half the WCLK period.

When PCVAL pin (24) = 1, all data will be precompensated by ± 125 ns, regardless of track number and data rate. However, this is only for MFM encoding. There is no write precompensation for FM. If PCVAL = 0, and if a track inside number 28 is accessed, then ± 187 ns precompensation will be generated. For frequencies other than 16 MHz or 32 MHz on the CLK1 pin, the precompensation values will be two and three clock cycles respectively.

When the non-standard 300 Kb/s data rate using CLK2 is chosen, the MFM precompensation will always be two clock cycles. For 9.6 MHz, this is ± 208 ns. In this case, the PCVAL function is disabled.

Write precompensation can be disabled by bit 2 of the Control Register for the AT/EISA. The PCVAL input to WD37C65C is ignored if there is no write precompensation.

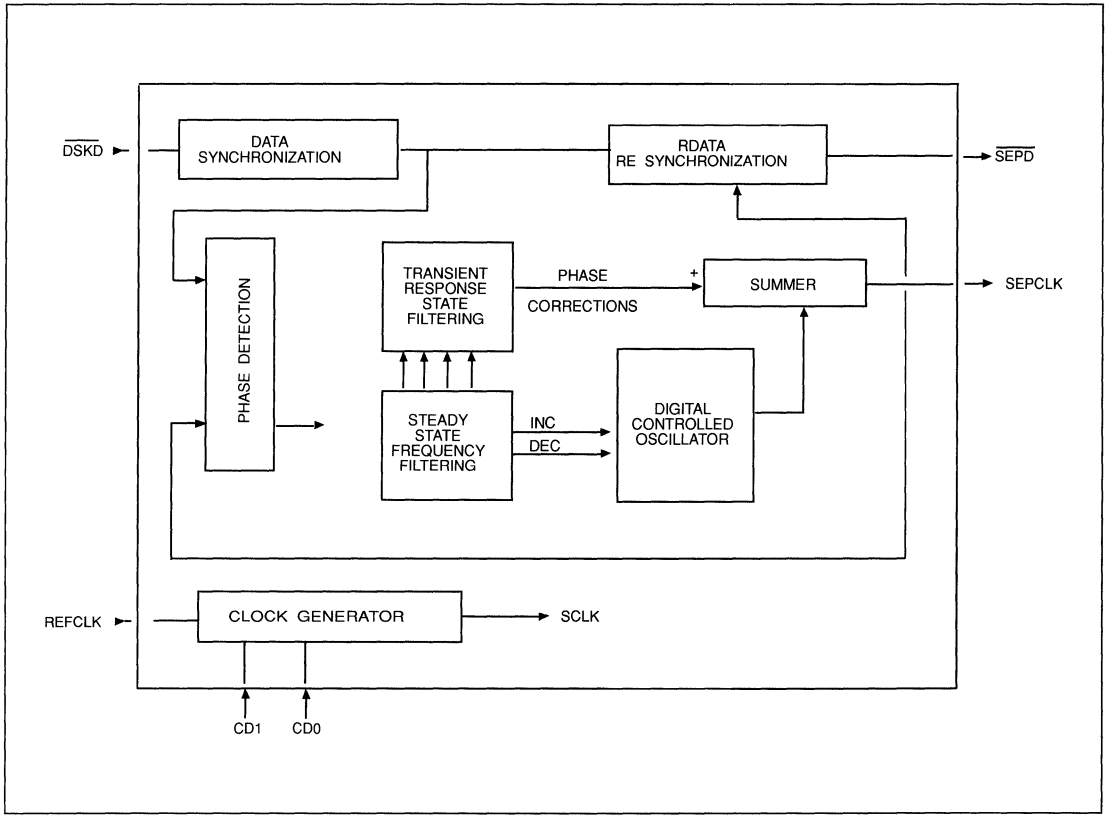


FIGURE 13-1. WD92C32 SIMPLIFIED BLOCK DIAGRAM

26

14.0 CLOCK GENERATION

This logical block provides all the clocks needed by the WD37C65C. They are: Sampling Clock (SCLK), Write Clock (WCLK), and the Master Clock (MCLK).

SCLK drives the WD92C32 Data Separator used during data recovery. This clock's frequency is always 32 times the selected data rate.

WCLK is used by the encoder logic to place MFM or FM on the serial WD-stream to the disk. WCLK always has a frequency two times the selected data rate.

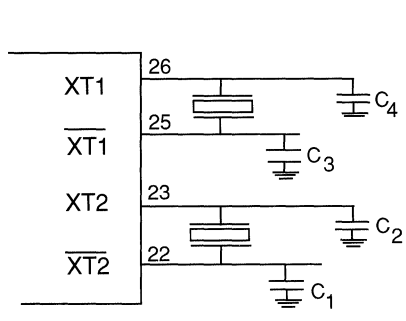
MCLK is used by the microsequencer. MCLK and MCLK clock all latches in a two-phase scheme. One microinstruction cycle is four MCLK cycles. MCLK has a frequency equal to eight times the selected MFM data rate or 16 times the FM data rate. Table 14-1 presents the Clock Data Rate.

Figure 14-1 illustrates the XTAL oscillator circuits for the 44-pin PLCC configuration.

In power down mode the XTAL oscillator and the clock circuitry are turned off.

DATA RATE	CODE	SCLK MHz	MCLK MHz	WCLK
1 Mb/s	MFM	32.0	8.0	2.0 MHz
500 kb/s	MFM	16.0	4.0	1.0 MHz
500 kb/s	FM	16.0	8.0	1.0 MHz
250 kb/s	FM	8.0	4.0	500 KHz
250 kb/s	MFM	8.0	2.0	500 KHz
125 kb/s	FM	4.0	2.0	250KHz
300 kb/s	MFM	9.6	2.4	600 KHz

TABLE 14-1. CLOCK DATA RATE



SERIES RESONANT
XT2

9.6 MHz ± 100 ppm
R series = 30 ohm max
C shunt = 10 pf max
C1 = 68 pf 5% mica
C2 = 56 pf 5% mica

SERIES RESONANT
XT1

16.0 MHz ± 100 ppm
R series = 30 ohm max
C shunt = 10 pf max
C3 = 47 pf 5% mica
C4 = 15 pf 5% mica

32 MHz ± ppm
R series = 47.2 ohm
C shunt = 2 pf max
C3 = 30 pf 5% mica
C4 = 30 pf 5% mica

FIGURE 14-1. CRYSTAL OSCILLATOR CIRCUITS FOR 44-PIN PLCC

15.0 COMMAND PARAMETERS

The WD37C65C is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor. The results after execution of the command may also be a multibyte transfer back to the processor. The commands consist of three phases: Command phase, Execution phase, and the Result phase.

Command phase - The Floppy Disk Controller (FDC) receives all information required to perform a particular operation from the processor

Execution phase - The FDC performs the operation it was instructed to do.

Result phase - After completion of the operation, status and other housekeeping information are made available to the processor.

Table 15-1 lists the 15 WD37C65C commands.

READ DATA
READ DELETED DATA
WRITE DATA
WRITE DELETED DATA
READ A TRACK
READ ID
FORMAT A TRACK
SCAN EQUAL
SCAN LOW OR EQUAL
SCAN HIGH OR EQUAL
RECALIBRATE
SENSE INTERRUPT STATUS
SPECIFY
SENSE DRIVE STATUS
SEEK

TABLE 15-1. WD37C65C COMMANDS

Tables 15-1 through 15-16 are presented to show the required parameters and results for each command. Most commands require nine command bytes and return seven bytes during the result phase. The "W" to the left of each byte indicates a command phase byte to be written. An "R" indicates a result byte.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to
	W	H	H	H	H	H	H	H	H	command execution. The four
	W	R	R	R	R	R	R	R	R	bytes are compared against
	W	N	N	N	N	N	N	N	N	header on floppy disk.
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after com-
	R	R	R	R	R	R	R	R	R	mand execution.
	R	N	N	N	N	N	N	N	N	

TABLE 15-2. READ DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-3. READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-4. WRITE DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-5. WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US1	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	DTL	DTL	DTL	DTL	DTL	DTL	DTL	DTL	
EXECUTION										Data transfer between FDD and main system. FDD reads all data fields from index hole to EOT.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-6. READ A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
EXECUTION										The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information read during
	R	R	R	R	R	R	R	R	R	Execution Phase from floppy
	R	N	N	N	N	N	N	N	N	disk.

TABLE 15-7. READ ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	N	N	N	N	N	N	N	N	Bytes/Sector
	W	SC	SC	SC	SC	SC	SC	SC	SC	Sectors/Track
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	Gap 3
	W	D	D	D	D	D	D	D	D	Filler Byte
EXECUTION										Floppy Disk Controller (FDC) formats an entire track.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after com-
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	mand execution.
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	In this case, the ID information
	R	R	R	R	R	R	R	R	R	has no meaning.
	R	N	N	N	N	N	N	N	N	

TABLE 15-8. FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-9. SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-10. SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HS	US1	US0	
	W	C	C	C	C	C	C	C	C	Sector ID information prior to command execution.
	W	H	H	H	H	H	H	H	H	
	W	R	R	R	R	R	R	R	R	
	W	N	N	N	N	N	N	N	N	
	W	EOT	EOT	EOT	EOT	EOT	EOT	EOT	EOT	
	W	GPL	GPL	GPL	GPL	GPL	GPL	GPL	GPL	
	W	STP	STP	STP	STP	STP	STP	STP	STP	
EXECUTION										Data compared between FDD and main system.
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information after command execution.
	R	ST1	ST1	ST1	ST1	ST1	ST1	ST1	ST1	
	R	ST2	ST2	ST2	ST2	ST2	ST2	ST2	ST2	
	R	C	C	C	C	C	C	C	C	
	R	H	H	H	H	H	H	H	H	Sector ID information after command execution.
	R	R	R	R	R	R	R	R	R	
	R	N	N	N	N	N	N	N	N	

TABLE 15-11. SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
EXECUTION										Head retracted to Track zero.

TABLE 15-12. RECALIBRATE

The WD37C65C issues 77 step pulses, the same as the NEC765.

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
RESULTS	R	ST0	ST0	ST0	ST0	ST0	ST0	ST0	ST0	Status information about the FDC at the end of seek operation
	R	PCN	PCN	PCN	PCN	PCN	PCN	PCN	PCN	

TABLE 15-13. SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W W	0 SRT HLT	0 SRT HLT	0 SRT HLT	0 SRT HLT	0 HUT HLT	0 HUT HLT	1 HUT HLT	1 HUT ND	Command Codes

TABLE 15-14. SPECIFY

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W	0 X	0 X	0 X	0 X	0 X	0 HS	0 US1	0 US0	Command Codes
RESULTS	R	ST3	ST3	ST3	ST3	ST3	ST3	ST3	ST3	Status information about the FDC.

TABLE 15-15.SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W W W	0 X NCN	0 X NCN	0 X NCN	0 X NCN	1 X NCN	1 HS NCN	1 US1 NCN	1 US0 NCN	Command Codes
EXECUTION										Head is positioned over proper cylinder on the diskette.

TABLE 15-16. SEEK

26

Table 15-17 defines, in alphabetical order, the symbols used in Command Tables 15-1 through 15-16.

SYMBOL	NAME	DESCRIPTION
A0	ADDRESS LINE 0	A0 controls selection of Main Status Register (A0=0) or Data Register (A0=1).
C	CYLINDER NUMBER	C stands for the current/selected cylinder (track) numbers 0 through 255 of the medium.
D	DATA	D stands for the data pattern which is going to be written into a sector.
D7 - D0	DATA BUS	8-bit DATA BUS, where D7 stands for a most significant bit, and D0 stands for a least significant bit.
DTL	DATA LENGTH	When N is defined as 00, DTL stands for the DATA LENGTH which users are going to read out or write into the sector.
EOT	END OF TRACK	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	GAP LENGTH	GPL stands for the length of Gap 3. During the FORMAT Command, it determines the size of Gap 3.
H	HEAD ADDRESS	H stands for head number 0 or 1 as specified in the ID field.
HLT	HEAD LOAD TIME	HLT stands for the HEAD LOAD TIME in FDD (2 to 254 ms in 2 ms increments).
HS	HEAD SELECT	HS stands for a selected head number 0 or 1 and controls the polarity of pin 25 (in 40-pin DIP) or pin 28 (in 44-pin PLCC).
HUT	HEAD UNLOAD TIME	HUT stands for the HEAD UNLOAD TIME after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM	If MF is low, FM mode is selected. If it is high, MFM mode is selected.
MT	MULTITRACK	If MT is high, a MULITRACK operation is performed. If MT=1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 on side 1.
N	NUMBER	N stands for the NUMBER of data bytes written in a sector.
NCN	NEW CYLINDER NUMBER	NCN stands for a NEW CYLINDER NUMBER which is going to be reached as a result of the Seek operation. Desired position of head.
ND	NON-DMA MODE	ND stands for operation in the NON-DMA MODE.
PCN	PRESENT CYLINDER	PCN stands for the cylinder number at the completion of the SENSE INTERRUPT STATUS Command. Position of head at present time.

TABLE 15-17. COMMAND SYMBOL DESCRIPTIONS

SYMBOL	NAME	DESCRIPTION
R	RECORD	R stands for the sector number which will be read or written.
R/W	READ/WRITE	R/W stands for either READ or WRITE signal.
SC	SECTOR	SC indicates the number of sectors per cylinder.
SK	SKIP	SK stands for SKIP Deleted Data Address mark.
SRT	STEP RATE TIME	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives. In 2's complement format, F(Hex)=1 ms, E(Hex)=2 ms, etc.
ST0 ST1 ST2 ST3	STATUS 0 STATUS 1 STATUS 2 STATUS 3	ST0-3 stands for one of four registers which store the STATUS information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the Main Status Register (selected by A0=0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	---	During a SCAN operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP=2, then alternate sectors are read and compared.
US0,US1	UNIT SELECT	US stands for a selected drive; binary encoded, 1 of 4.

TABLE 15-17. COMMAND SYMBOL DESCRIPTIONS (CONTINUED)

16.0 COMMAND DESCRIPTIONS

16.1 READ DATA

A set of nine byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT (multitrack), MF (MFM/FM), and N (number of bytes/sector). Table 31 lists the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sect or N	Maximum Transfer Capacity (Bytes/Sector) Number of Sectors	Final Sector Read From Diskettes
0 0	0 1	00 01	(128)(26)=3,328 (256)(26)=6,656	26 at Side 0 or 26 at Side 1
1 1	0 1	00 01	(128)(52)=6,656 (256)(52)=13,312	26 at Side 1
0 0	0 1	01 02	(256)(15)=3,840 (512)(15)=7,680	15 at Side 0
1 1	0 1	01 02	(256)(30)=7,680 (512)(15)=15,360	15 at Side 1
0 0	0 1	02 03	(512)(8)=4,096 (1024)(8)=8,192	8 at Side 1 or 8 at Side 1
1 1	0 1	02 03	(512)(16)=8,192 (1024)(16)=16,384	8 at Side 1

TABLE 16-1. TRANSFER CAPACITY

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the Data Bus. The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read operation. When N is non-zero, then DTL has no meaning and should be set to FF hexadecimal.

At the completion of the Read Data command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in 'R'), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to 1 (high). If a CRC error occurs in the Data Field, the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 µs in the FM mode, and every 13 µs in the MFM mode, or the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high), and terminates the Read Data command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result phase is dependent upon the state of the MT bit and EOT byte. Table 16-2 shows the values for C, H, R, and N, when the processor terminates the command.

MT	HD	Final Sector Transferred to Procesor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
0	0	Equal to EOT	C+1	NC	R=0	NC
0	1	Less than EOT	NC	NC	R+1	NC
0	1	Equal to EOT	C+1	NC	R=0	NC
1	0	Less than EOT	NC	NC	R+1	NC
1	0	Equal to EOT	NC	LSB	R=0	NC
1	1	Less than EOT	NC	NC	R+1	NC
1	1	Equal to EOT	C+1	LSB	R=0	NC

TABLE 16-2. C, H, R, AND N VALUES

Notes
NC (No Change) The same value as the one at the beginning of command execution
LSB (Least Significant bit) The least significant bit of H is complemented

16.2 WRITE DATA

A set of nine bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in 'R' is incremented by one, and the next data field is written into. The FDC continues this 'Multisector Write Operation' until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write command operates in much the same manner as the Read command. The following items are the same, and one should refer to the Read Data command for details:

- Transfer capacity
- EN (End of Cylinder) flag
- ND (No Data) flag
- Head Unload Time interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠0

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27 µs in the FM mode and every 13 µs in the MFM mode. If the time interval between data transfers is longer than this, then the FDC sets the OR (Overrun) flag in Status Register 1 to a 1 (high) and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

16.3 WRITE DELETED DATA

This command is the same as the Write Data command except a Deleted Data Address mark is written at the beginning of the data field instead of the normal Data Address mark.

16.4 READ DELETED DATA

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field (and SK = 0 [low]), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

16.5 READ A TRACK

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hold for the second time, it sets the MA (Missing Address mark) flag in Status Register 1 to a 1 (high) and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

16.6 READ ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, then the MA (Missing Address mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

16.7 FORMAT A TRACK

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM System 34 (double density) or System 3740 (single density) format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (gap length), and D (data pattern) which are supplied by the processor during the Command phase. The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (cylinder number), H (head number), R (sector number) and N (number of bytes/sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the WD37C65C for each sector on the track. If FDC is set for the DMA mode, it will issue four DMA requests per sector. If it is set for the Interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formaning continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

Table 16-3 shows the relationship between N, SC, and GPL for various sector sizes.

Format	Sector Size Bytes/sector	N	SC	GPL 1	GPL 2,3
8" Standard Floppy					
FM Mode	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5 1/4" Minifloppy					
FM Mode	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3 1/2" Sony Microfloppy					
FM Mode	128	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

TABLE 16-3. N, SC AND GPL RELATIONSHIP

Notes:
1. Suggested values of GPL in Read 0, Write commands to avoid splice point between data field and ID field of contiguous sections
2. Suggested values of GPL in format command
3. All values except sector size are hexadecimal.
4 In MFM mode FDC cannot perform a Read/Write/format operation with 126 bytes/sector (N=00)

16.8 SCAN COMMANDS

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP -8 R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high) and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high) and terminates the Scan command. The receipt of a Terminal Count signal from the processor or DMA controller durring the scan operation will cause the FDC to complete the comparison of the particular byte which is in process and then to terminate the command. Table 16-4 shows the status of bits SH and SN under various conditions of Scan.

26

Command	Status Register 2 Bit 2=SN	Bit 3=SH	Comments
Scan Equal	0	1	$D_{FFD}=D$ Processor
Scan Equal	1	0	$D_{FFD}\neq D$ Processor
Scan Low or Equal	0	1	$D_{FFD}=D$ Processor
Scan Low or Equal	0	0	$D_{FFD}<D$ Processor
Scan Low or Equal	1	0	$D_{FFD}>D$ Processor
Scan Low or Equal	0	1	$D_{FFD}=D$ Processor
Scan High or Equal	0	0	$D_{FFD}>D$ Processor
Scan High or Equal	1	0	$D_{FFD}<D$ Processor

TABLE 16-4. STATUS OF BITS SH AND SN

If the FDC encounters a Deleted Data Address mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control mark) flag of Status Register 2 to a 1 (high) in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read or the MT (Multitrack) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following will happen: sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the index hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA controller for comparison against the data read from the diskette. In order to avoid having the OR (Overrun) flag set in Status Register 1, it is necessary to have the data available in less than 27 µs (FM mode) or 13 µs (MFM mode). If an Overrun occurs, the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

16.9 SEEK

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. FDC has four independent Present Cylinder Registers for each drive. They are cleared only after the Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to a 1 (high), and step pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD set to a 0 (low), and step pulses are issued. (Step Out)

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued NCN is compared against PCN, and when NCN = PCN, the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits D_0B-D_3B in the Main Status Register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state; but during the Execution phase, it is in the non-busy state. While the FDC is in the non-busy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150 µs, the timing between the first two step pulses may be shorter than that set in the Specify command by as much as 1ms.

16.10 RECALIBRATE

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is

low, the Direction signal remains 0 (low) and step pulses are issued. When the Track 0 signal goes high, the SE (Seek End) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 255 step pulses have been issued, (for the WD37C65 and the WD37C65A) or 77 step pulses (WD37C65B/C), the FDC sets the SE (Seek End) and EC (Equipment Check) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command.

16.11 SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Cylinder command
   g. Write Deleted Data command
   h. Scan commands

2. Ready Line of FDD changes state

3. End of Seek or Recalibrate command

4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an Execution phase in non-DMA mode, DB5 in the Main Status Register is high. Upon entering the Result phase, this bit gets cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command. This command, when issued, resets the Interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Seek End Bit 5	Interrupt Code Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

TABLE 16-5. INTERRUPT CAUSE

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no Result phase. When the disk drive has reached the desired head position, the WD37C65C will set the Interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. See Figure 16-1.

The Specify command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 =32 ms . . . $0F_{16}$ = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 23). Times indicated above are for a 16 MHz clock; if the clock was reduced to 8 MHz, then all time intervals are increased by a factor of 2. If the clock was increased to 32 MHz, then all time intervals are decreased by half.

The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1), the Non-DMA mode is selected; and when ND = 0, the DMA mode is selected.

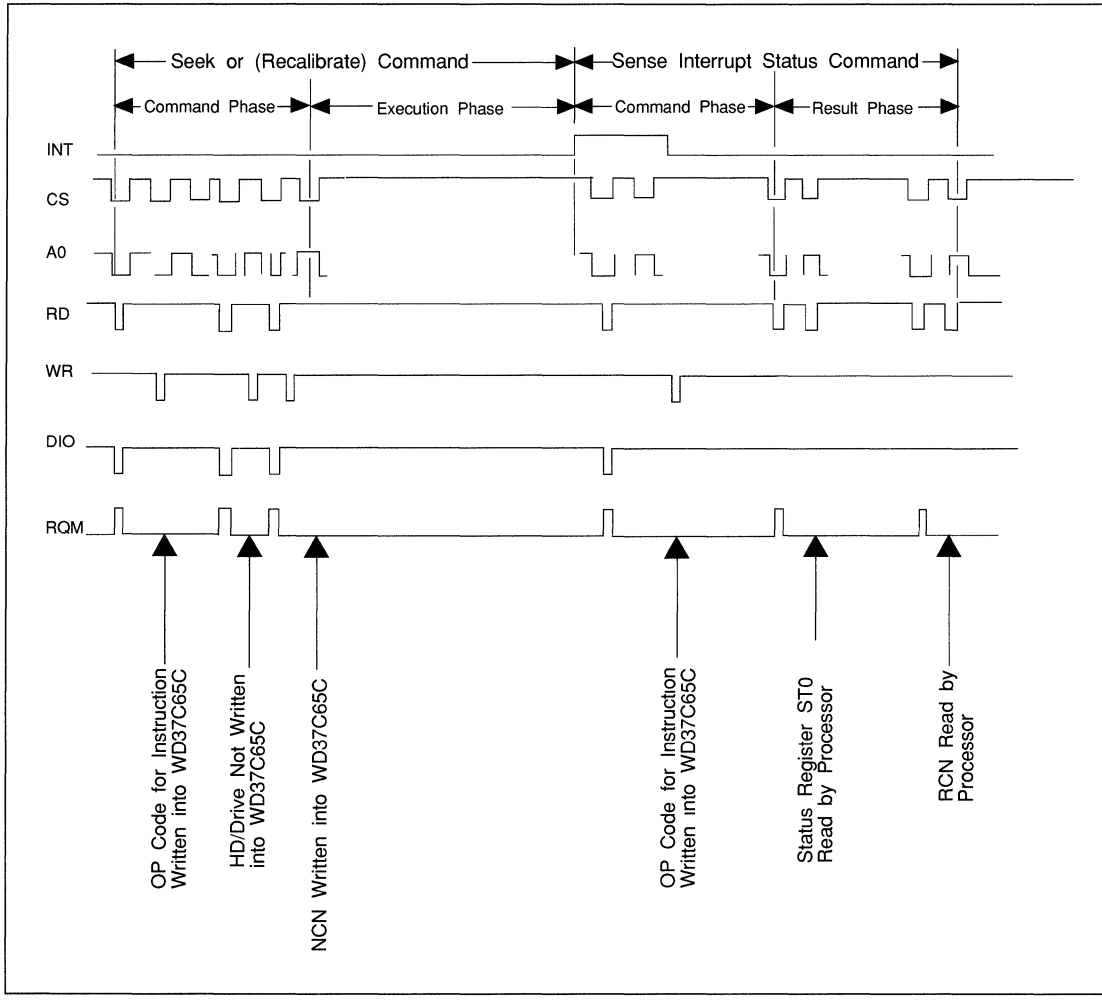


FIGURE 16-1. SEEK, RECALIBRATE, AND SENSE INTERRUPT

16.12 SENSE DRIVE STATUS

This command may be used by the processor to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

16.13 INVALID

If an Invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both high (1), indicating to the processor that the WD37C65C is in the Result phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0, it will find an 80 hex, indicating an Invalid command was received.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt; otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

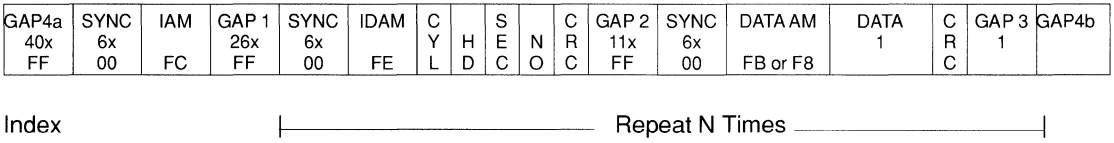


FIGURE 16-2. WD37C65C FM MODE FORMAT

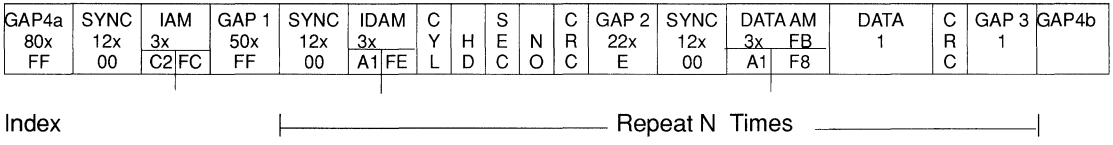


FIGURE 16-3. WD37C65C MFM MODE FORMAT

No.	WD37C65/A/B	WD37C65/C
1.	2 XTAL oscillators. - 16 MHz for standard data rate (up to 500 kb/s MFM). - 9.6 MHz for non-standard rate. (300 kb/s PCAT)	2 XTAL oscillators. - 32 MHz for standard data rate (up to 1 Mb/s MFM) or 16 MHz for standard data rate (up to 500 kb/s MFM). - 9.6 MHz for non-standard rate. (300 kb/s AT/EISA)
2.	Supports data rate up to 500 Kb/s.	Supports data rate up to 1 Mb/s
3.	Does not support power down mode.	Supports power down mode feature, standby ICC = 100 µA max.
4.	PCVAL pin for selecting the precomp values.	PCVAL pin for selecting the precomp values and a feature to disable write precomp.

TABLE 16-6. DIFFERENCES BETWEEN WD37C65/A/B AND WD37C65C

17.0 DC ELECTRICAL SPECIFICATIONS

17.1 MAXIMUM RATINGS

Operating Temperature	0°C (32°F) to 70°C (158°F)
Storage Temperature	-55°C (-67°F) to +125°C (257°F)
Voltage on any pin with respect to ground	-0.3V to VCC +0.3V
Supply Voltage with respect to ground	7V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

17.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to ground.

Operating temperature range (TA)	0°C (32°F) to 70°C (158F)
Power supply voltage (VCC)	+5V ± 10%

17.3 DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS
VCC	+5VDC Power Supply	4.5	5.5	V
VIL	Input Low Voltage - Data Bus & XTOSC	---	0.8	V
VIH	Input High Volt - Data Bus & XTOSC	2.0	---	V
VILT	Input Low Threshold - Schmitt Trigger	0.8	1.1	V
VIHT	Input High Threshold - Schmitt Trigger	1.7	2.0	V
VHYS	Schmitt Trigger Hysterisis	0.45	---	V
VOL	Output Low- DBx,IRQ,DMA,; Io = 24.0 mA	---	0.4	V
VOH	Output High - DBx,IRa,DMA,; Io = -5.0 mA	2.8	---	V
VOLHC	Output Low - High Current; Io = 48.0 mA	---	0.4	V
ILUL	Latch Up Current Low	40.0	---	mA

SYMBOL	PARAMETER	MIN	MAX	UNITS
ILUH	Latch Up Current High	-40.0	---	mA
ILL	Leakage Current Low	---	10.0	µA
ILH	Leakage Current High	---	-10.0	µA
ICC	Supply Current - 100 µA Source Loads	---	60.0	mA
ICCHL	Supply Current - 5.0 mA Source Loads	---	120.0	mA
ICCPDM	Supply Current in Power Down Mode	---	100.0	µA[1]
PD	Power Dissipation- ICC Max	---	600.0	mW[3]
PDHL	Power Dissipation - ICCHL Max	---	750.0	mW[2,3]
VPQR	Power Qualified Reset Threshold	2.8	4.35	V

Note 1. Vin = VCC or GND, Io = O mA.

Note 2. Includes DBx, IRQ and DMA; Io = -5.0 mA source loads.

Note 3. Includes open drain high current drivers at Vol = 0.4V.

26

18.0 AC TIMING CHARACTERISTICS

The following notes apply to all parameters presented in this section:

1. TA = 0°C (32°F) to 70°C (158°F)
2. VCC = +5V ± 10%
3. CL = 100 pf
4. CY = CLK1 or XT1 period
5. MCY = MCLK period, dependent on selected data rate
6. WCY = WCLK period, dependent on selected data rate

SYMBOL	PARAMETER	MIN	MAX	UNITS
tCY	Clock Period	31	---	nS
tPH	Clock Active (High or Low)	13.5	---	nS
tR	Clock Rise Time (Vin 0.8 to 2.0)	---	2	nS
tF	Clock Fall Time (Vin 2.0 to 0.8)	---	2	nS
tAR	A0,$\overline{CS}$,$\overline{DACK}$ Set Up Time to $\overline{RD}$ Low	0	---	nS
tRA	A0,$\overline{CS}$,$\overline{DACK}$ Hold Time to RD High	0	---	nS
tRR	$\overline{RD}$ Width	90	---	nS
tRD	Data Access Time From $\overline{RD}$ Low	---	90	nS
tDF	DB To Float Delay From $\overline{RD}$ High	10	65	nS
tAW	A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Set Up Time To $\overline{WR}$ Low	0	---	nS
tWA	A0,$\overline{CS}$,$\overline{DACK}$,$\overline{LDCR}$,$\overline{LDOR}$, Hold Time From $\overline{WR}$ High	0	---	nS
tWW	$\overline{WR}$ Width	60	---	nS
tDW	Data Set Up Time To $\overline{WR}$ High	80	---	nS
tWD	Data Hold Time From $\overline{WR}$ High	0	---	nS
tRI	IRQ Reset Delay Time From $\overline{RD}$ High			1MCY +150nS
tWI	IRQ Reset Delay Time From $\overline{WR}$ High			1MCY +150nS
tMCY	DMA Cycle Time	52		MCY
tAM	DMA Reset Delay Time From $\overline{DACK}$ Low	---	140	nS
tMA	$\overline{DACK}$ Delay Time From DMA High	0	---	nS
tAA	$\overline{DACK}$ Width	90	---	nS
tTC	TC Width	60	---	nS
tRST	Reset Width - TTL Driven CLK1	60	---	nS
tSRST	Reset Width - Software Reset	5	---	MCY
tRDD	$\overline{RDD}$ Active Time Low	40	---	nS
tWDD	$\overline{WD}$ Write Data Width Low	1/2 (TYP)	---	WCY
tDST	$\overline{DIRC}$ Hold & Set Up To $\overline{STEP}$ Low	4	---	MCY
tSTU	$\overline{DSX}$ Hold Time From $\overline{STEP}$ Low	20	---	MCY
tSTP	$\overline{STEP}$ Active Time Low	24	---	MCY
tSC	$\overline{STEP}$ Cycle Time	132	---	MCY
tSTD	$\overline{DIRC}$ Hold Time After $\overline{STEP}$	96	---	MCY
tIDX	$\overline{IDX}$ Index Pulse Width	2	---	MCY
tMR	$\overline{RD}$ Delay From DMA	0	---	nS
tMW	$\overline{WR}$ Delay From DMA	0	---	nS

SYMBOL	PARAMETER	MIN	MAX	UNITS
tMRW	$\overline{RD}$ Or $\overline{WR}$ Response From DMA High	---	48	MCY
tCA	Chip Access Delay From RST Low - TTL	32	---	MCY
tCAS	Chip Access Delay From tSRST Low	40	---	MCY
tXCA	Chip Access Delay From RST-OSC XT1 at 16 MHz	500	---	µS
tXTS	XT2 Access Delay After RST 9.6 MHz	1000	---	µS
tTCR	TC Delay From Last DMA Or IRQ, $\overline{RD}$	0	192	MCY
tTCW	TC Delay From DMA Or IRQ, $\overline{WR}$	0	384	MCY
Tcycle	Clock Cycle	60	---	nS
Tp-high	Clock High	25	---	nS
Tp-low	Clock Low	25	---	nS
Trise	Rise Time	---	5	nS; Vin .8 to 2.0
Tfall	Fall Time	---	5	nS; Vin 2.0 to .8

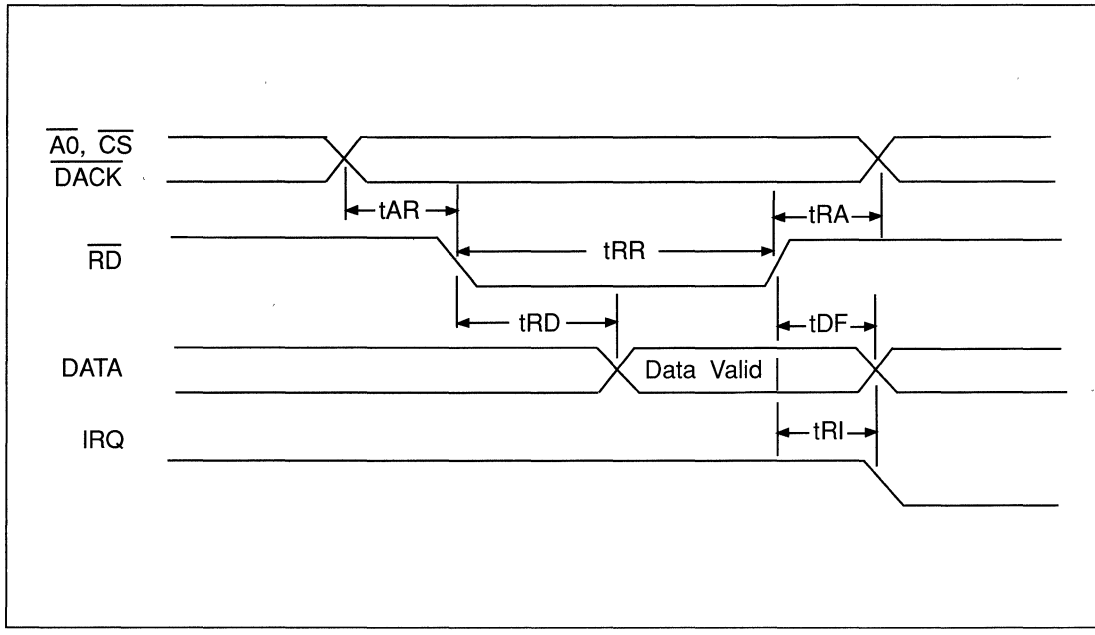


FIGURE 18-1. READ TIMING

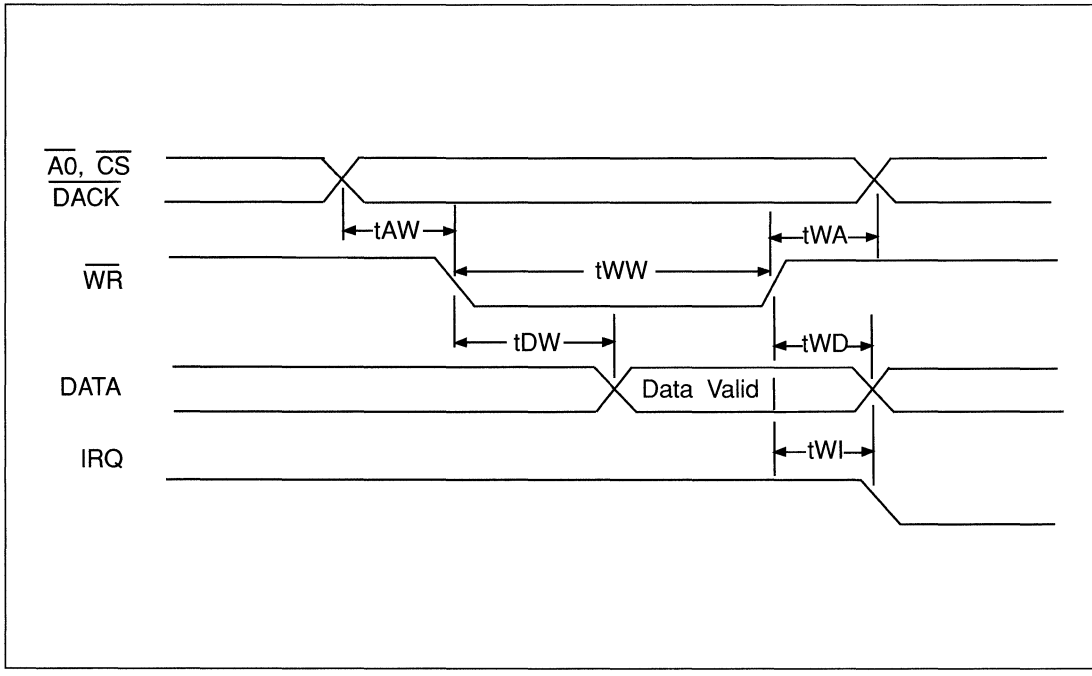


FIGURE 18-2. WRITE TIMING

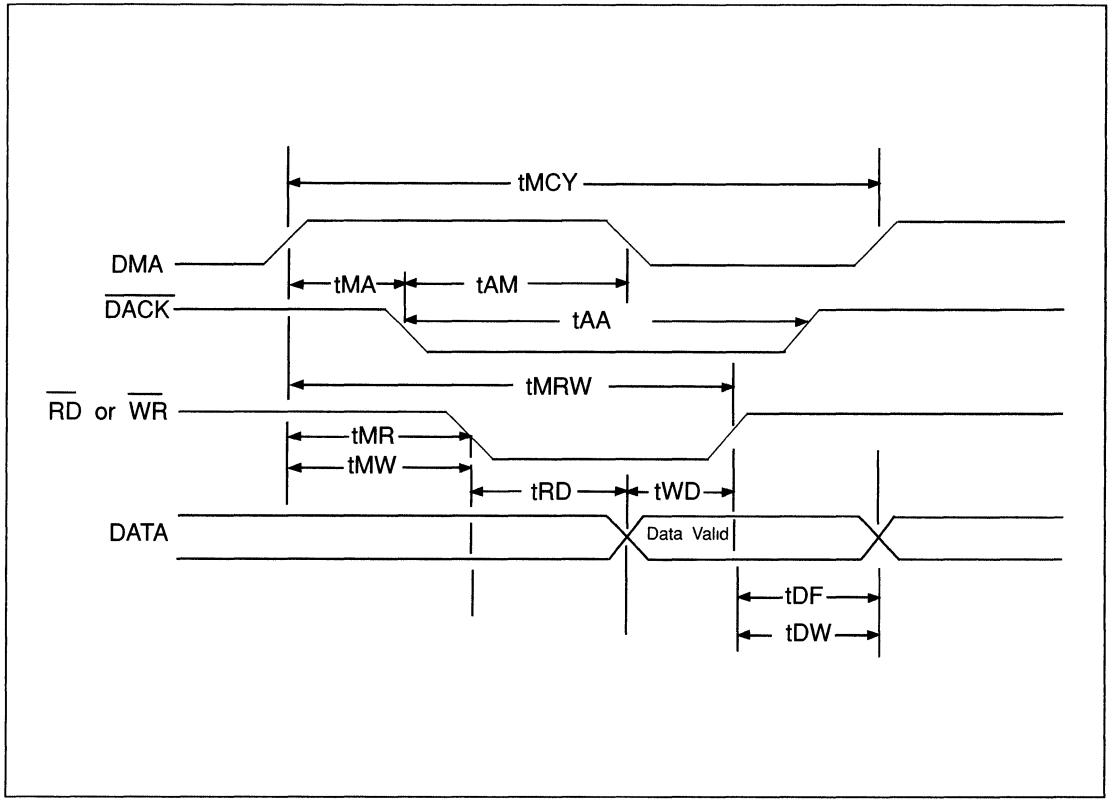


FIGURE 18-3. DMA TIMING

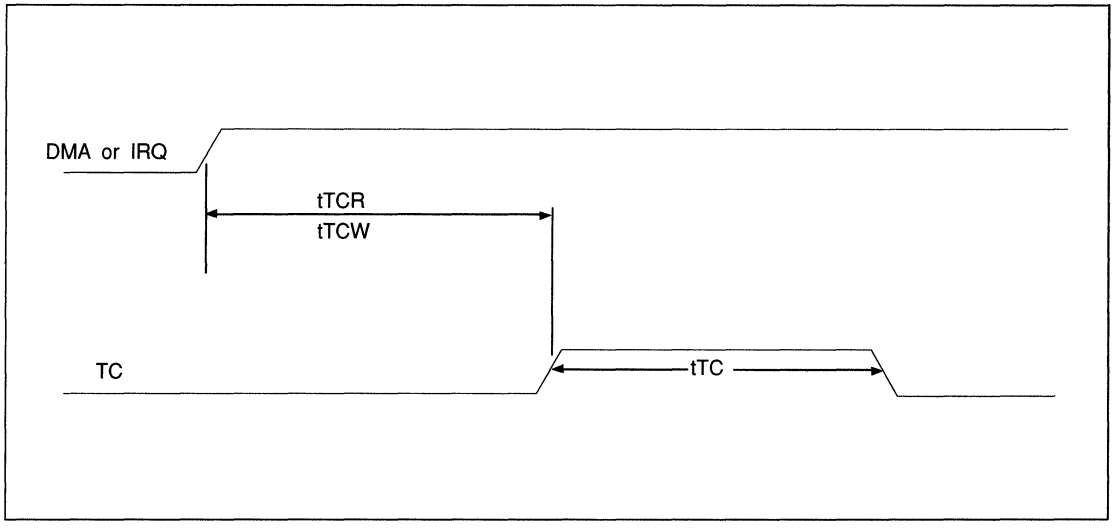


FIGURE 18-4. TERMINAL COUNT TIMING

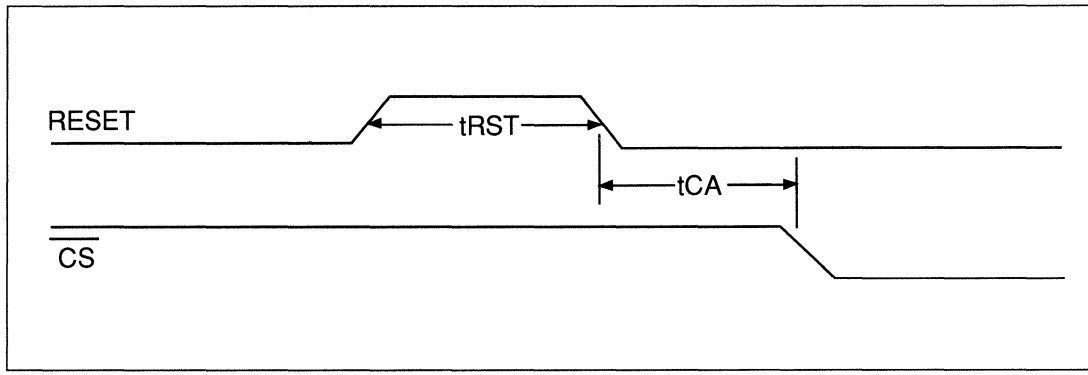


FIGURE 18-5. RESET TIMING

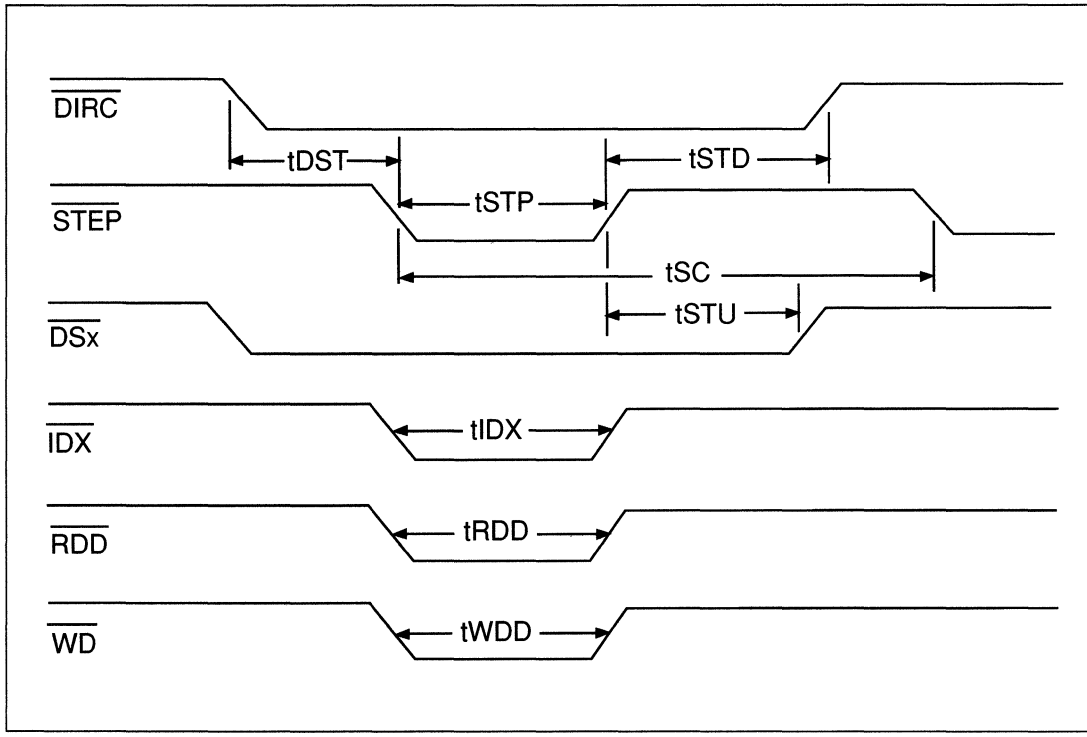


FIGURE 18-6. DISK DRIVE TIMING

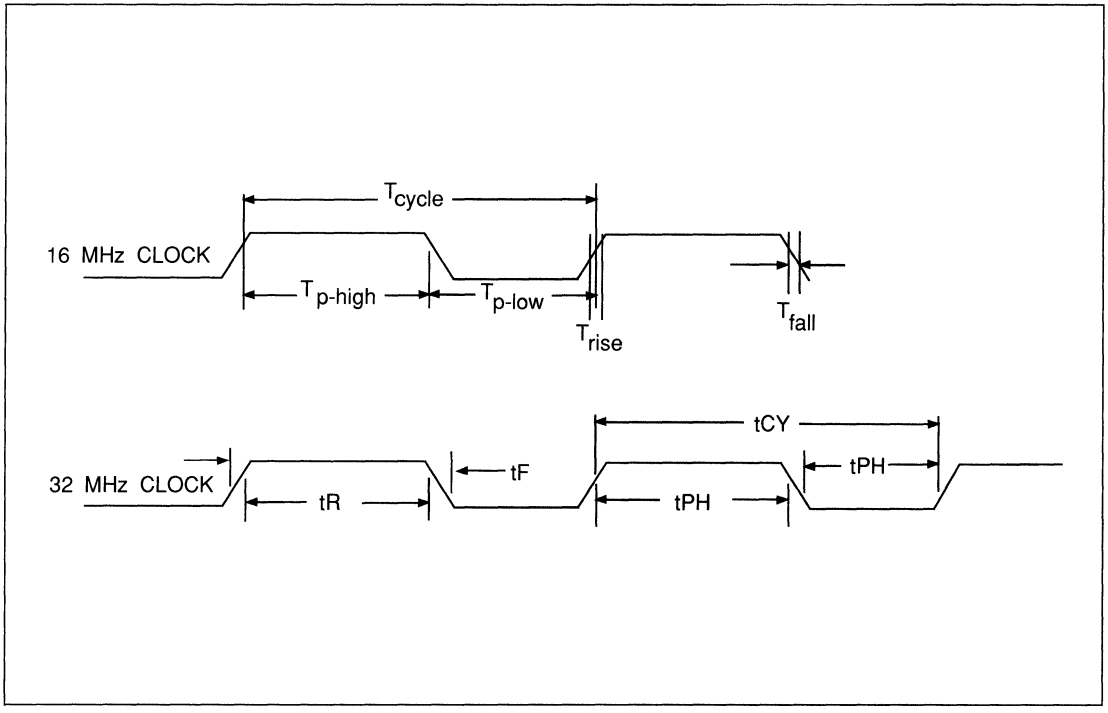


FIGURE 18-7. CLOCK TIMING