System Programming Manual

VX900 Series

All-in-One
System Processor

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VIA TECHNOLOGIES, INC.

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1.0	9/10/10	Initial public release	JW
1.01	11/25/10	Updated the base address in the descripton of “Bus Master IDE I/O Space”	JW
1.1	3/9/11	Updated bit descriptions of: SATA_EPHY index Rx24[7:5], Rx34[7:5]; D16F4 Rx5B-5A[15:12]; D17F0 Rx94[1:0], Rx97[2] and Rx9F[7]; PMIO Rx26[2], Rx6F[4]	JW
1.2	3/14/11	Updated D17F0 Rx46[7] and Rx47[7]	EY
1.3	4/18/11	Updated FSB support up to 1066Mhz for VX900 Updated D0F7 Rx76[7]	EY
1.4	8/4/11	Modify D17F0 Rx95[0] and PMIO Rx20[14]	DA
1.41	10/4/11	Updated D20F0 Rx3D description	JW

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

REGISTER OVERVIEW

Register Document Introduction

This document includes the registers for VIA VX900 Series. Please refer to Table 1 for the specification differences of VX900 Series products.

VX900 Series is an all-in-one system processor that integrates functional modules of the traditional North Module and South Module, plus 3D/2D and Video Processors, Video Decoding Accelerator and controller for external display interface. The register set is partitioned into two blocks: System Processor and Graphics and Video Module; of which, processor related registers are described in this **System Programming Manual** while graphics and video registers are described in the **Graphics Programming Guide**.

Table 1. VX900M and VX900 Feature Comparison Table

Product Model	VX900M VX900MH *	VX900 VX900H *
FSB Speed (MHz)	400-800	400-1066
Memory Type	Single channel DDR2 667 DDR3 800	Single channel DDR2 800 DDR3 1066
PCI Express	3 ports: 3*1 Gen1 (1.1)	4 ports: 1*8 + 3*1 Gen2 (1.1 / 2.0)
Video Interface	LVDS – single channel	
	HDMI – 1 port	
	Display Port – 2 ports	
Video Decoding	HD capable	BD capable
Core Voltage	1.0V	1.2V

Note: VX900H and VX900MH are with HDCP capability supported, while VX900 and VX900M are not.

Module and Register Scope Definitions

Module Name Abbreviations

NM: North Module. It contains functional modules of the traditional North Bridge chip.
SM: South Module. It contains functional modules of the traditional South Bridge chip.
NSMIC: North-South Module Interface Control
SNMIC: South-North Module Interface Control
PM: Power Management
HDAC: High Definition Audio Controller

Register Scope Map Within Modules

To specifically identify every function, the following abbreviations will be applied in subsequent sections.

Abbreviation of Register Space / Module Name	Register Space	Function
North Module		
D0F0	PCI Device 0, Function 0	GFX Access and Debugging Control
D0F1	PCI Device 0, Function 1	Error Reporting
D0F2	PCI Device 0, Function 2	Host Bus Control
D0F3	PCI Device 0, Function 3	DRAM Bus Control
D0F4	PCI Device 0, Function 4	Power Management and Chip Testing Control
D0F5	PCI Device 0, Function 5	Central Traffic Control and APIC
D0F6	PCI Device 0, Function 6	Scratch Registers
D0F7	PCI Device 0, Function 7	North-South Module Interface Control **<NSMIC>**
D3F0	PCI Device 3, Function 0	PCI Express Root Port 0 – x8, x4, x2, x1
D3F1	PCI Device 3, Function 1	PCI Express Root Port 1 – x2,x1
D3F2	PCI Device 3, Function 2	PCI Express Root Port 2 – x1
D3F3	PCI Device 3, Function 3	PCI Express Root Port 3 – x1
D3F4	PCI Device 3, Function 4	PCI Express EPHY Block
RCRBH	Memory Space	PCI Express Root Complex Register Block for Host

Abbreviation of Register Space / Module Name	Register Space	Function
South Module		
D10F0~F3	PCI Device 10, Function 0~3	PCI UART Ports 0-3 Registers
D11F0	PCI Device 11, Function 0	USB Mass Storage Device
USBD-MMIO	Memory Space	USB Device Memory Mapped I/O Space Registers
D12F0	PCI Device 12, Function 0	SDIO Host Controller
SDIO-MMIO	Memory Space	SDIO Memory Mapped I/O Space Registers
D13F0	PCI Device 13, Function 0	Card Reader Controller
xDC-MMIO	Memory Space	Extreme Digital-Picture Controller Memory Mapped I/O
SDC-MMIO	Memory Space	Security Digital Controller Memory Mapped I/O Space
Data DMA-MMIO	Memory Space	Data DMA Memory Mapped I/O Space Registers
CICH DMA-MMIO	Memory Space	CICH DMA Memory Mapped I/O Space Registers
PCI Control-MMIO	Memory Space	PCI Control Memory Mapped I/O Space Registers
D15F0	PCI Device 15, Function 0	Serial ATA Controller
D16F0	PCI Device 16, Function 0	USB 1.1 UHCI Ports 0-1
D16F1	PCI Device 16, Function 1	USB 1.1 UHCI Ports 2-3
D16F2	PCI Device 16, Function 2	USB 1.1 UHCI Ports 4-5
D16F3	PCI Device 16, Function 3	USB 1.1 UHCI Ports 6-7
USB 1.1-IO	IO Space	USB 1.1 I/O Space Registers
D16F4	PCI Device 16, Function 4	USB 2.0 EHCI Controller, Ports 0-5
USB 2.0-MMIO	Memory Space	EHCI USB 2.0 Memory Mapped I/O Space Registers
D17F0	PCI Device 17, Function 0	Bus and Power Management Control
PMIO	IO Space	ACPI I/O Registers
PM-MMIO	Memory Space	Power Management Memory Mapped I/O Space
SMIO	IO Space	System Management Bus I/O Space Registers
CEC	MMIO Space	Consumer Electronics Controller
HPET	Memory Space	HPET Memory Mapped I/O Space Registers
SPI-MMIO	Memory Space	Special Peripheral Interface Memory Mapped I/O Space
SPI0-MMIO	Memory Space	SPI Bus 0 Memory Mapped I/O Space Registers
D17F7	PCI Device 17, Function 7	South-North Module Interface Control **<SNMIC>**
D19F0	PCI Device 19, Function 0	PCI-to-PCI Bridge
D20F0 / HDAC	PCI Device 20, Function 0	High Definition Audio Controller
HDAC-MMIO	Memory Space	HDAC Memory Mapped I/O Space Registers

Register Table Format

In the register descriptions, column "Default" indicates the power-on default value of register bit(s), while column "Attribute" indicates access type of register bit.

Attribute Definition

Basic Attributes

RO:	Read Only.
WO:	Write Only. (register value can not be read by the software)
RW:	Read / Write.
RW1:	Write Once then Read Only after that.
RW1C:	Read / Write of "1" clears bit to zero.

***Sticky Attributes*:** adding a "S" in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.

ROS:	Sticky-Read-Only.
WOS:	Sticky-Write-Only.
RWS:	Sticky-Read/Write.
RW1S:	Sticky-Write-Once.
RW1CS:	Sticky-Write-1-to-Clear.

Special Default Value Definitions

Dip:	means the default value is set by dip switch or strapping.
HwInit:	Hardware initialized; bit default value is set by hardware.
ROMSIP:	The default value with ROMSIP attribute is loaded from preset ROM when chipset resets.

PCI Configuration Space I/O

All north bridge's PCI space registers are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: CFB-CF8h

PCI Configuration Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** (always reads 0)
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** (always reads 0)

I/O Port Address: CFF-CFCh

PCI Configuration Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note: Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

NORTH MODULE IRQ AND APIC CONTROL

PCIE Link Declaration Description

	PE0(D3F0)	PE1(D3F1)	PE2(D3F2)	PE3(D3F3)
Device number	03	03	03	03
Component ID	01	01	01	01
Function number	0	1	2	3
Port number	1	2	3	4

IRQ and Interrupt Assignment Table

Internal IRQ#	Device Interrupt
IRQ0	INTA_PE0
IRQ1	INTB_PE0
IRQ2	INTC_PE0
IRQ3	INTD_PE0 or MSGC_INT_PE0
IRQ4	INTA_PE1
IRQ5	INTB_PE1
IRQ6	INTC_PE1
IRQ7	INTD_PE1 or MSGC_INT_PE1
IRQ8	INTA_PE2
IRQ9	INTB_PE2
IRQ10	INTC_PE2
IRQ11	INTD_PE2 or MSGC_INT_PE2
IRQ12	INTA_PE3
IRQ13	INTB_PE3
IRQ14	INTC_PE3
IRQ15	INTD_PE3 or MSGC_INT_PE3
IRQ16	USINTA
IRQ17	USINTB
IRQ18	Reserved
IRQ19	Reserved
IRQ20	Reserved
IRQ21	Reserved
IRQ22	Reserved
IRQ23	Reserved

APIC Register I/O

Memory Mapped I/O APIC Registers

The IO APIC registers are accessed by an indirect addressing scheme using Index Registers and Data Registers that are mapped into memory space.

Table 2. Memory Mapped I/O APIC Registers Summary Table

Memory Address	Function	Size
FECxyz00	**APIC Index**	8 bit
FECxyz10	**APIC Data**	32 bit
FECxyz20	**APIC IRQ Pin Assertion**	8 bit
FECxyz40	**APIC EOI**	8 bit

Please reference D0F5 Rx40[3:0] and Rx41[7:0] for the control x, y, z

Memory Address: FECxyz00h

APIC Index **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	0	**I/O APIC Index** 8-bit pointer to the I/O APIC register.

Memory Address: FECxyz10h

APIC Data **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	RW	0	**I/O APIC Data** This is a 32-bit register for the data to be read or written to the I/O APIC indirect register pointed by the Index Register.

Memory Address: FECxyz20h

APIC IRQ Pin Assertion **Default Value: nnh**

Bit	Attribut	Default	Description
7:5	RO	0	**Reserved**
4:0	WO	nnh	**IRQ Number** Bit[4:0] written to this register contain the IRQ number for this interrupt. The only valid values are 0-23.

Memory Address: FECxyz40h

APIC EOI **Default Value: nnh**

Bit	Attribut	Default	Description
7:0	WO	nnh	**Redirection Entry Clear** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the "Remote_IRR" bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC Registers

For index registers setting, please refer to Memory Address FECxyz00h (APIC Index) and FECxyz10 (APIC Data).

Index: 00h

I/O APIC Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RW	0	**I/O APIC Identification** Software must program this value before using the I/O APIC.
23:0	RO	0	**Reserved**

Index: 01h

I/O APIC Version **Default Value: 0017 8003h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RO	17h	**Maximum Redirection Entry** This value is equal to the number of interrupt input pins for the I/O APIC minus one. For this I/O APIC, the value is 17h.
15	RO	1b	**PCI IRQ** This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and that PCI devices are allowed to write to it to cause interrupt.
14:8	RO	0	**Reserved**
7:0	RO	03h	**APIC Version** The implementation version for this I/O APIC is 03h.

Index: 02h

I/O APIC Arbitration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RO	0	**I/O APIC Arbitration ID**
23:0	RO	0	**Reserved**

Index: 03h

Boot Configuration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Delivery Type** 0: Interrupt Delivery Mechanism is via the APIC Serial Bus. 1: Interrupt Delivery Mechanism is a Front-side Bus Message.

Index: 10-3Fh

I/O Redirection Table

There are 24 64-bit I/O Redirection Table entry registers. Each register is a dedicated entry for each interrupt input signal.

Table 3. I/O Redirection Table

Index	Function
11-10h	I/O APIC Redirection – APIC IRQ0
13-12h	I/O APIC Redirection – APIC IRQ1
15-14h	I/O APIC Redirection – APIC IRQ2
17-16h	I/O APIC Redirection – APIC IRQ3
19-18h	I/O APIC Redirection – APIC IRQ4
1B-1Ah	I/O APIC Redirection – APIC IRQ5
1C-1Dh	I/O APIC Redirection – APIC IRQ6
1E-1Fh	I/O APIC Redirection – APIC IRQ7
21-20h	I/O APIC Redirection – APIC IRQ8
23-22h	I/O APIC Redirection – APIC IRQ9
25-24h	I/O APIC Redirection – APIC IRQ10
27-26h	I/O APIC Redirection – APIC IRQ11
29-28h	I/O APIC Redirection – APIC IRQ12
2B-2Ah	I/O APIC Redirection – APIC IRQ13
2D-2Ch	I/O APIC Redirection – APIC IRQ14
2F-2Eh	I/O APIC Redirection – APIC IRQ15
31-30h	I/O APIC Redirection – APIC IRQ16
33-32h	I/O APIC Redirection – APIC IRQ17
35-34h	I/O APIC Redirection – APIC IRQ18
37-36h	I/O APIC Redirection – APIC IRQ19
39-38h	I/O APIC Redirection – APIC IRQ20
3B-3Ah	I/O APIC Redirection – APIC IRQ21
3D-3Ch	I/O APIC Redirection – APIC IRQ22
3F-3Eh	I/O APIC Redirection – APIC IRQ23

I/O Redirection Entry **Default Value: nnn1 nnnn nnnn nnnnh**

Bit	Attribut	Default	Description
63:56	RW	nnh	**Destination Field** In Physical Mode (bit-11=0), bits [59:56] contain an APIC ID. In Logical Mode (bit-11=1), bits [63:56] of the Destination Field specify the logical destination address. **Destination Mode IOREDTBLx[11]** — **Logical Destination Address** 0: Physical Mode — IOREDTBLx[59:56] = APIC ID 1: Logical Mode — IOREDTBLx[63:56] = Set of processors
55:17	RO	0	**Reserved**
16	RW	0	**Interrupt Mask** 0: Not Mask 1: Masked
15	RW	0	**Trigger Mode** Indicates the type of signal on the interrupt pin that triggers an interrupt. 0: Edge Sensitive 1: Level Sensitive
14	RO	0	**Remote Interrupt Request Register (IRR)** This bit is used for level triggered interrupts. Its meaning is undefined for edge triggered interrupts. For level triggered interrupts, this bit is set to 1 when local APIC(s) accept the level interrupt sent by the IOAPIC. 0: EOI message with a matching interrupt vector is received from a local APIC 1: Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)
13	RW	0	**Interrupt Input Pin Polarity** Specifies the polarity of the interrupt signal. 0: High active 1:Low active
12	RO	0	**Delivery Status** Contains the current status of the delivery of this interrupt. 0: Idle (there is currently no activity for this interrupt.) 1: Send Pending (the interrupt has been injected but its delivery is temporarily held either because the APIC bus is busy or because the receiving APIC unit can not currently accept the interrupt.)
11	RW	0	**Destination Mode** Determines the interpretation of the Destination field. 0: Physical Mode 1: Logical Mode
10:8	RW	000b	**Delivery Mode** Specify how the APICs listed in the destination field should act upon reception of this signal. 000: Fixed 001: Lowest Priority 010: SMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	RW	nnh	**Interrupt Vector** Contain the interrupt vector for this interrupt. Vector values range from 10h to FEh.

DEVICE 0 FUNCTION 0 (D0F0): HOST CONTROLLER

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 1 below.

Device 0 Function 0 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 0. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**000**	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

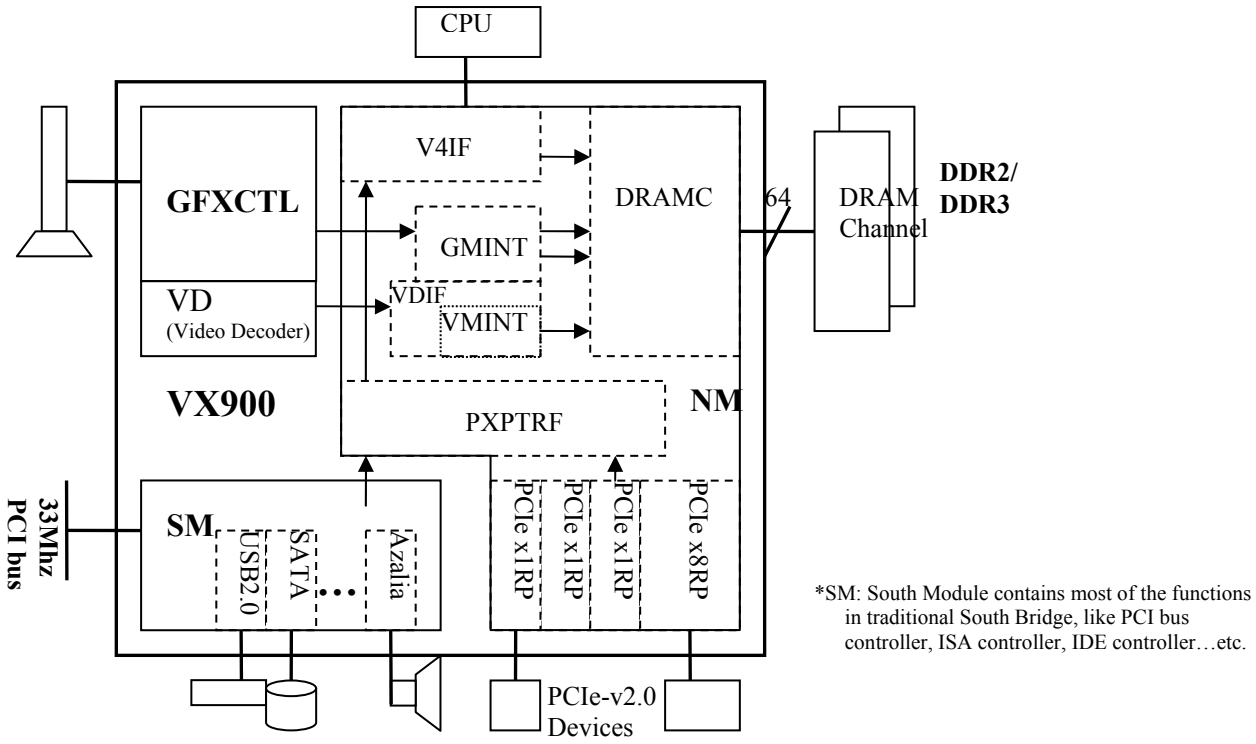


Figure 1. System Block Diagram for D0F0

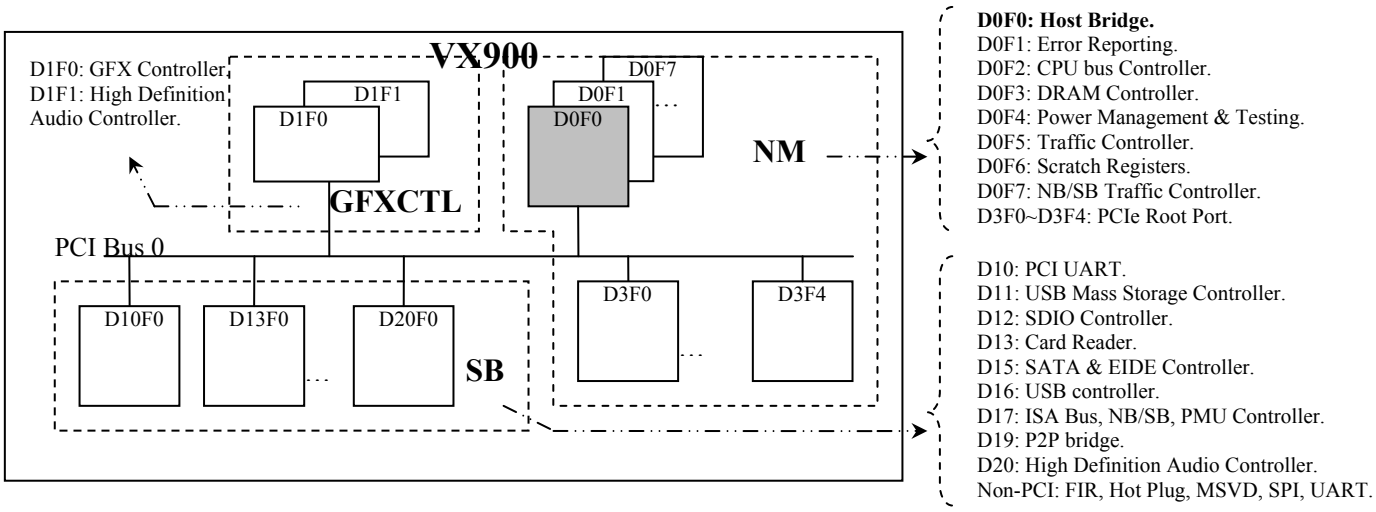


Figure 2. Register Level Block Diagram for D0F0

The registers in this function are accessibility control for internal modules, debugging selections, and other miscellaneous controls. Please refer to the shadow block in Figure 2 for the register level location of this function in the whole chip.

Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F0)

Device ID **Default Value:0410h**

Bit	Attribute	Default	Description
15:0	RO	0410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F0)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RW	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F0)

PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RW1C	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RW1C	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	01b	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus.
8	RW1C	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F0)

Revision ID **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Chip Revision Code** They are the revision ID of this chip.

Offset Address: 0B-09h (D0F0)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F0)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Maximum Time Slice for CPU as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. Programming to any values to these bits does not change any behaviors of this chip.
2:0	RO	0	**Bit[2:0] of the Maximum Time Slice For CPU as a Master on the PCI Bus** These bits are bit[2:0] for the maximum time slice of the PCI bus controller.

Offset Address: 0Eh (D0F0)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. When Rx4F[0] = 1, the value of these bits are 80h. When Rx4F[0] = 0, the value of these bits are 00h, and the accessing to D0F1, D0F2, .. and D0F7 will not be available. i.e. a configuration read cycle to function other than this function will have data FFFF_FFFFh returned.

Offset Address: 0Fh (D0F0)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F0)

Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address Registers 0** This function does not claim base address.

Offset Address: 17-14h (D0F0)
Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address Registers 1** This function does not claim base address.

Offset Address: 1B-18h (D0F0)
Base Address Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address Registers 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F0)
Base Address Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address Registers 3** This function does not claim base address.

Offset Address: 23-20h (D0F0)
Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address Registers 4** This function does not claim base address.

Offset Address: 27-24h (D0F0)
Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address Registers 5** This function does not claim base address.

Offset Address: 2B-28h (D0F0)
CardBus CIS Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 33-30h (D0F0)
Expansion ROM Base Address **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Expansion ROM Base Address** Bits [31:11] defined the accessing address[31:11] for the expansion ROM. Bit-0 is the enable bit for the ROM accessing. It is not supported by this function.

Offset Address: 34h (D0F0)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F0) – Reserved

Offset Address: 3D-3Ch (D0F0)
Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F0)
Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

Multiple Function and Legacy Space Access Control (40-AFh)

Offset Address: 40-4Dh (D0F0) – Reserved

Offset Address: 4Eh (D0F0)

Legacy Space Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**VGA I/O 16 Bits Access Decode** VGA I/O cycles are with address 3B0h-3BBh, and 3C0-3DF. This bit is to enable a full 16 bits address decoding for the VGA I/O cycles. The conventional decoding is only to decode bit[9:0]. As for the forwarding of such cycles, it depends on the setting of D0F3 RxA1[7]. If it is 0, the chip will forward VGA cycles to PCI bus. If it is 1, the chip will forward such VGA cycles to internal Graphic Controller (GFXCTL). 0: 10 bits I/O address decoding. i.e. All VGA aliased (e.g. 13B0h, 23B0h..F3B0h) cycles will be forwarded. 1: Full 16 bits I/O address decoding. Only base VGA cycle, i.e., bits [15:10]=000000b, will be forwarded.
3:2	RW	0	**Reserved**
1	RW	0	**MDA Resource Location** MDA (Monochrome Display Adapter) cycles are memory with address B_0000h - B_7FFFh and I/O with address 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh. This bits determined the destination this chip will forward such MDA cycles to. It also had to work with D0F3 RxA1[7]: **{D0F3 RxA1[7], Bit-1}:** 0x: 33Mhz PCI Bus. 10: Internal Graphic Controller (GFXCTL). 11: 33Mhz PCI Bus.
0	RW	0	**Reserved**

Offset Address: 4Fh (D0F0)

Multiple Function Control **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	1b	**Multi-Function Support** This bit determines if this device (Device 0) is a multi-function device or not. The status of this bit will be reflected on Rx0E[7]. Please refer to register descriptions on Rx0E. 0: Disabled. Registers of functions 1-7 of this device cannot be accessed, and the value returned will be 0FFFFFFFFh when accessed. 1: Enabled. This device is a multi-function device, and all the other functions D0F1, D0F2,…D0F7 can be accessed.

Offset Address: 50-AFh (D0F0) – Reserved

Access Capability for GFXCTL, VD, and HDAC (B0-BFh)

Offset Address: B0h (D0F0)

Access Capability for GFXCTL, VD, and HDAC **Default Value: nBh**

Bit	Attribute	Default	Description
7:6	RO	HwInit	**NB Bonding Option**
5	RW	0	**64-bit Memory Base2 (SL) Support** This bit should be programmed with the same value of D1F0 RxB0[7]. 0: Disable, 32-bit mode, D0F0 RxCC is read only and always read as 0 regardless of programming value of D1F0 Rx1C[3:0]. 1: Enable, 64-bit mode, D0F0 RxCC reflect the bits at D1F0 Rx1C[3:0]
4	RW	1b	**HDAC Memory Base0 Access Capability** For supporting HDMI, internal GFX controller incorporated with an HDAC (High Definition Audio Controller) in D1F1. The address range of this HDAC is defined by base registers at D1F1 Rx13~Rx10 and size registers at D0F3 RxAC[2:0] (Note 1). This bit enables the downstream memory cycles to this HDAC controller. 0: Disabled, the downstream memory cycles with address falling in this HDAC MMIO range will be forwarded to 33Mhz PCI bus. 1: Enabled, the downstream memory cycles with address falling in this HDAC MMIO range will be forwarded to the internal HDAC which controlled by D1F1. When D0F3 RxA1[7] = 0 or D1F1 Rx04[1]=0, the function of this bit will be considered as disabled.
3	RW	1b	**GFXCTL Memory Base0 (Video Decoder) Access Capability** Video Decoder (VD) had its accessed memory range defined by base registers at D1F0 Rx13~Rx10 with a size of 32K (i.e. address decoding using Address[31:15]). This bit enables the downstream memory cycles to the internal Video Decoder. 0: Disabled, the downstream memory cycles with address falling in this VD MMIO range will be forwarded to 33Mhz PCI bus. 1: Enabled, the downstream memory cycles with address falling in this VD MMIO range will be forwarded to the internal Video Decoder. When D0F3 RxA1[7] =0 or D1F0 Rx04[1]=0, the function of this bit will be considered as disabled.
2	RO	0	**Reserved**
1	RW	1b	**GFXCTL Memory Base1 (MMIO) Access Capability** Internal Graphic controller (GFXCTL) had memory mapped I/O using memory address range defined by base registers at D1F0 Rx17~Rx14 and size registers at D0F3 RxAC[5:3] (Note 2). This bit enables the downstream memory access for GFXCTL MMIO accessing. 0: Disabled, the downstream memory cycles with address falling in this GFXCTL MMIO range will be forwarded to 33Mhz PCI bus. 1: Enabled, the downstream memory cycles with address falling in this GFXCTL MMIO range will be forwarded to GFXCTL. When D0F3 RxA1[7] =0 or D1F0 Rx04[1]=0, the function of this bit will be considered as disabled.
0	RW	1b	**GFXCTL Memory Base2 (SL) Access Capability** Internal Graphic controller (GFXCTL) had memory addressing mapped to System Local frame buffer (SL) defined by base registers at D1F0 Rx1B~Rx18 and size registers at D0F3 RxA1[6:4] (Note 3). This bit enables the downstream memory access for the SL accessing. 0: Disabled, the downstream memory cycles with address falling in this SL accessing range will be forwarded to 33Mhz PCI bus. 1: Enabled, the downstream memory cycles with address falling in this SL accessing range will be forwarded to GFXCTL. When D0F3 RxA1[7] =0 or D1F0 Rx04[1]=0, the function of this bit will be considered as disabled.

Notes:
1. The size for this HDAC MMIO defined at D0F3 RxAC[2:0] is ranged from 8K to 32K.
2. The size for this GFX MMIO defined at D0F3 RxAC[5:3] is ranged from 8M to 512M.
3. The size for this SL accessing defined at D0F3 RxA1[6:4] is ranged from 8M to 512M.

Offset Address: B1-BFh (D0F0) – Reserved

Shadow Registers for Integrated Graphics Controller and Video Processor (C0-FFh)

Offset Address: C0h (D0F0)

Shadow Register for D1F0 (GFXCTL) Rx04 – PCI Command Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	0	**Shadow Register for Memory Space Access of D1F0** This register completely reflects the status of D1F0 Rx04[1]. 0: Internal Graphic Controller (GFXCTL) does not respond to those downstream cycles targeted to it. Those cycles will be forwarded to 33Mhz PCI bus. 1: GFXCTL will accept downstream cycles targeted to its MMIO range, SL accessing range, and Video Decoder's MMIO range. Please refer to RxB0[3,1,0] for more information.
0	RO	0	**Shadow Register for I/O Space Access of D1F0** This register completely reflects the status of D1F0 Rx04[0]. The IO address ranges defined for GFXCTL are 3B0h~3B7h, 3B8h~3BBh and 3C0h~3DFh. 0: GFXCTL does not respond to I/O space access. I/O downstream cycles will be forwarded to 33Mhz PCI bus. 1: GFXCTL will respond to the I/O access for those addresses mentioned.

Offset Address: C1-C3h (D0F0) – Reserved

Offset Address: C4h (D0F0)

Shadow Registers for D1F0 (GFXCTL) Rx64 – GFX Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RO	0	**Shadow Registers for Device Power State of D1F0** These registers completely reflect the status of D1F0 Rx64[1:0] which are the ACPI device power management status registers. They indicate which device power state the GFXCTL is in. 00: D0 State. 01: D1 State. 10: D2 State. 11: D3 State. When the power state is not in D0 state, the chip will forward all cycles targeted to GFXCTL to 33Mhz PCI bus.

Offset Address: C5-C7h (D0F0) – Reserved

Offset Address: CB-C8h (D0F0)

Shadow Registers for D1F0 (GFXCTL) Rx1B~Rx18 – Memory Base2 **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:0	RO	FFF00000h	**Shadow Registers for Memory Base2 Bit[31:0] – SL** These registers completely reflect the bits at D1F0 Rx1B~18. They are the memory base2 of the GFXCTL. These memory base is defined for the accessing range of "System Local frame buffer" (SL). Please refer to RxB0[0] for more information.

Offset Address: CF-CCh (D0F0)

Shadow Registers for D1F0 (GFXCTL) Rx1F~Rx1C – Memory Base2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RO	0	**Shadow Registers for Memory Base2 Bit[35:32] – SL** These registers completely reflect the bits at D1F0 Rx1C[3:0]. They are the high bits of memory base2 (RxCB~C8). When RxC8[2:1] = 10b, it indicates this memory base2 is 64 bits addressing. In such case, these four bits become valid.

Offset Address: D3-D0h (D0F0)

Shadow Registers for D1F0 (GFXCTL) Rx17~Rx14 - Memory Base1 **Default Value: F800 0000h**

Bit	Attribute	Default	Description
31:0	RO	F8000000h	**Shadow Registers for Memory Base1 Bit[31:0] - MMIO** These registers completely reflect the bits at D1F0 Rx17~14. They are the memory base1 of the GFXCTL. This memory base is defined for the MMIO accessing for GFXCTL. Please refer to RxB0[1] for more information.

Offset Address: D4-DFh (D0F0) – Reserved

Offset Address: E0h (D0F0)

Shadow Registers for D1F1 (HD-Audio Controller) Rx04 – PCI Command Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	0	**Shadow Register for Memory Space Access of D1F1** This register completely reflects the status of D1F1 Rx04[1]. 0: Integrated High Definition Audio Controller (HDAC) does not respond to those downstream cycles targeted to it. Those cycles will be forwarded to 33Mhz PCI bus. 1: HDAC will accept downstream cycles targeted to the range defined by its base address register at D1F1 Rx13~Rx10. Please refer to RxB0[4] for more information.
0	RO	0	**Shadow Registers for I/O Space Access of D1F1** This register completely reflects the status of D1F1 Rx04[0]. However, no matter what the status of this bit is, HDAC won't respond to any I/O access targeted to it.

Offset Address: E1-E3h (D0F0) – Reserved

Offset Address: E4h (D0F0)

Shadow Registers for D1F1 (HDAC) RxE0[1:0] - HDAC Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RO	0	**Shadow Registers for Device Power State of D1F1** These registers completely reflect the status of D1F1 RxE0[1:0] which are the ACPI device power management status registers. They indicate which device power state the HDAC is in. 00: D0 State. 01: D1 State. 10: D2 State. 11: D3 Hot State. When the power state is not in D0 state, the chip will forward all cycles targeted to HDAC to 33Mhz PCI bus.

Offset Address: E5-E7h (D0F0) – Reserved

Offset Address: EB-E8h (D0F0)

Shadow Registers for D1F1 (HDAC) Rx13~Rx10 – Memory Base0 **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:0	RO	FFF00000h	**Shadow Registers for Memory Base0 Bit[31:0] – HDAC** These registers completely reflect the bits at D1F1 Rx13~10. They are the memory base0 of HDAC. These memory base is defined for the MMIO accessing for HDAC. Please refer to RxB0[4] for more information.

Offset Address: EF-ECh (D0F0)

Shadow Registers for D1F1 (HDAC) Rx17~Rx14 – Memory Base0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RO	0	**Shadow Registers for Memory Base0 Bit[35:32] – HDAC** These registers completely reflect the bits at D1F1 Rx14[3:0]. They are the high bits of memory base0 (RxEB~E8). When RxE8[2:1] = 10b, it indicates this memory base0 is 64 bits addressing. In such case, these four bits become valid.

Offset Address: F0-F3h (D0F0) – Reserved

Offset Address: F7-F4h (D0F0)

Shadow Registers for D1F0 (GFXCTL) Rx13~Rx10 – Memory Base0 **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:0	RO	FFF0 0000h	**Shadow Registers for Memory Base0 Bit[31:0] – Video Decoder** These registers completely reflect the bits at D1F0 Rx13~10. They are the memory base0 of the GFXCTL. These memory base is defined for the MMIO accessing for Video Decoder (VD). Please refer to RxB0[3] for more information.

Offset Address: F8-FFh (D0F0) – Reserved

DEVICE 0 FUNCTION 1 (D0F1): ERROR REPORTING

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 3 below.

Device 0 Function 1 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 1. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**001**	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

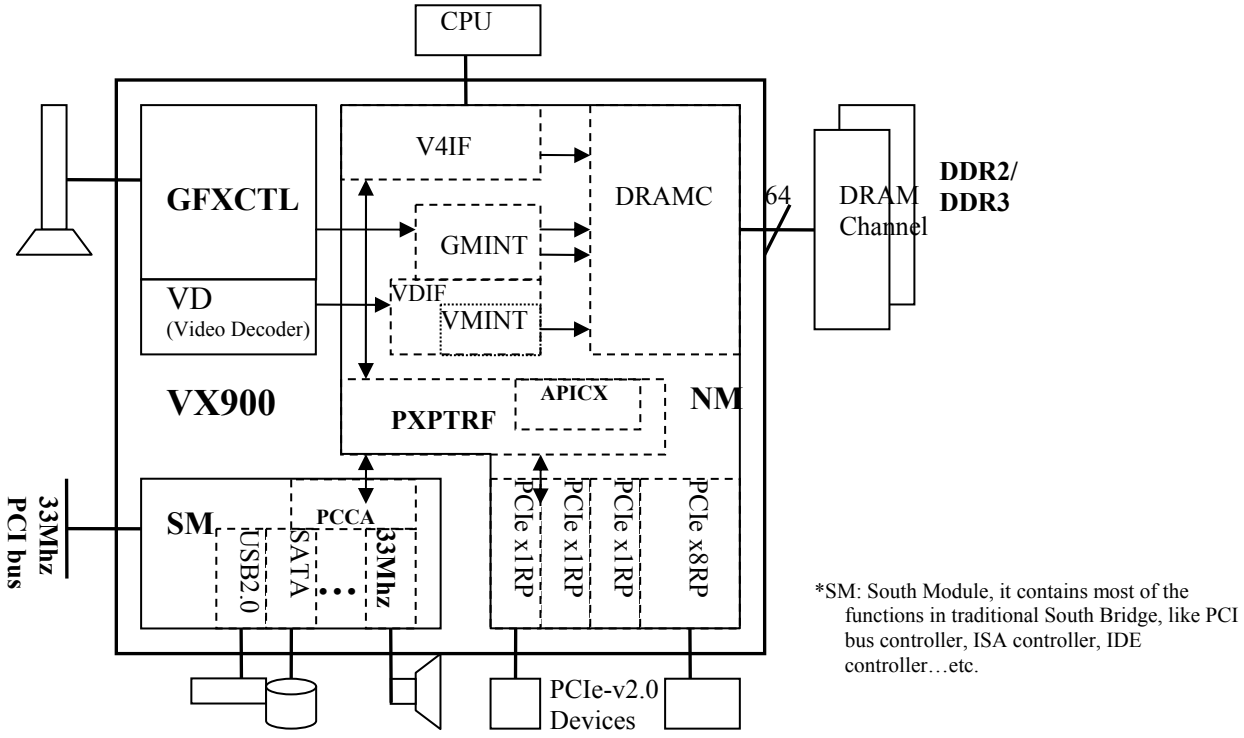


Figure 3. System Block Diagram for D0F1

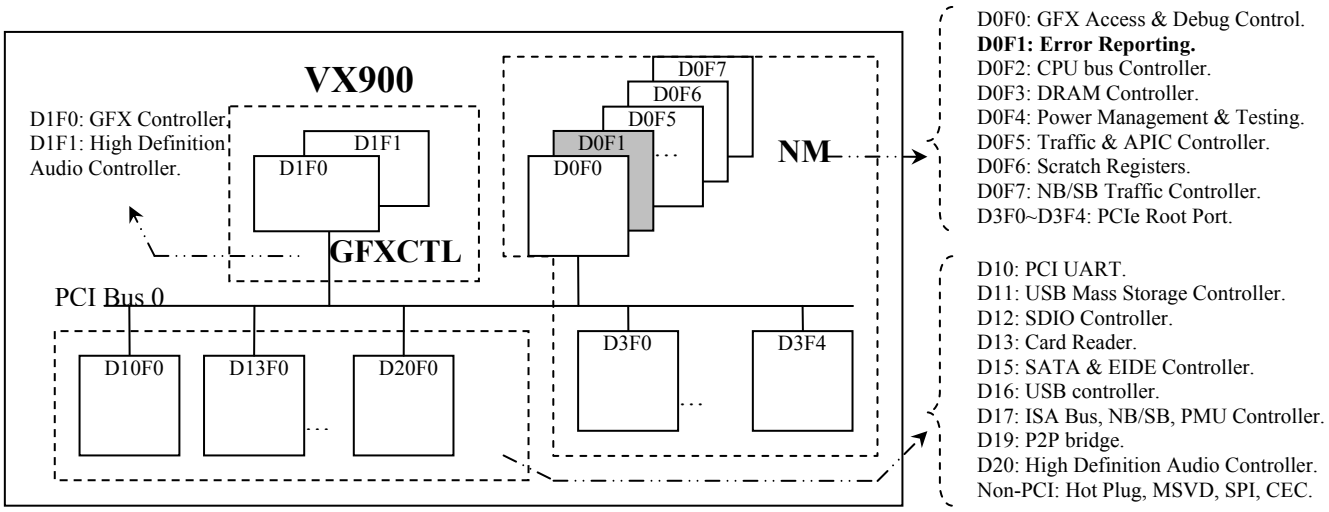


Figure 4. Register Level Block Diagram for D0F1

The registers in this function are error reporting for the functions in NB. A software programming view for this register space D0F1 is as shown in the shaded block in Figure 4.

Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F1)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F1)

Device ID **Default Value: 1410h**

Bit	Attribute	Default	Description
15:0	RO	1410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F1)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** This is a PCI header register. It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** This is a PCI header register. It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RO	0	**Parity Error Response** This is a PCI header register. It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** This is a PCI header register. It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** This is a PCI header register. It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** This is a PCI header register. It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** This is a PCI header register. It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** This is a PCI header register. It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** This is a PCI header register. It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F1)

PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RO	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RO	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	01b	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus*1.
8	RO	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F1)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** These bits are PCI header registers. They are the revision ID of this function.

Offset Address: 0B-09h (D0F1)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F1)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F1)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F1)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value of these bits are 80h. It indicates this is a multi-function device.

Offset Address: 0Fh (D0F1)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 10-27h (D0F1) – Reserved

Offset Address: 2B-28h (D0F1)
CardBus CIS Pointer **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F1)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F1)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F1) – Reserved

Offset Address: 34h (D0F1)
Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F1) – Reserved

Offset Address: 3D-3Ch (D0F1)
Interrupt Line and Interrupt Pin **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F1)
Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

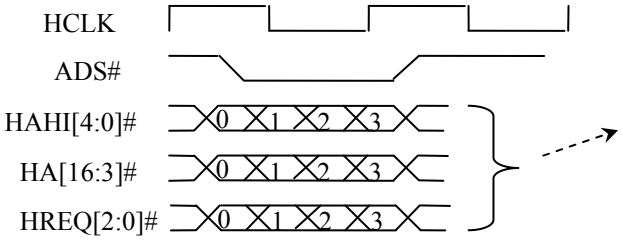
Host Bus Error Report (40-6Fh)

Offset Address: 40-5Fh (D0F1) – Reserved

Offset Address: 60h (D0F1)

CPU Bus Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**CPU Bus Address Parity Error Detected** Refer to Figure 5, the address parity bits on the V4 bus are the signal HAPa# and HAPb#. They are actually the signal status of HA16# at beat time 1 and 3 respectively. Internally, an address parity (AP0) for beat time 0 and 1 is generated and checked against inversion of HAPa# (note that the signals in V4 bus are inverted before the internal logic uses it). That parity is generated by the exclusive-OR function of inversion of {HAa[39:3]#, HREQa[4:0]#} (HREQa[5]# is excluded) which conveyed at the beat 0 and 1 on the V4 bus. i.e. HAPa# will be 0 when the number of 0 in {HAa[39:3]#, HREQa[4:0]#} is an odd number. The address parity (AP1) for beat time 2 and 3 had the same function as those for beat time 0 and 1, only that its source is {HAb[39:3]#, HREQb[4:0]#} which conveyed at the beat 2 and 3 on the V4 bus. This register bit will be set to 1 if either AP0 or AP1 can not reflect the correct address parity. Rx68[7] must be set to 1 to enable this parity check function. i.e. if the Rx68[7] is disabled, this bit should be always 0. 0: Not detected. 1: Detected. Once this bit is set, it will remain at 1 until a 1 is written to this bit to clear it.
6	RW1C	0	**Reserved** This bit will be always 0.
5	RO	0	**Reserved**
4	RW1C	0	**CPU Downstream LOCK Cycle Detected** This bit will be set to 1 if there is a CPU downstream lock cycle to a non-DRAM target (e.g. PCIe RP0~RP3, GFXCTL or some devices on the SB block). 0: Not detected. 1: Detected. Once this bit is set, it will remain at 1 until a 1 is written to this bit to clear it.
3:0	RO	0	**Reserved**



V4 bus's signal definition can be mapped to signal definitions of P4 bus:

Beat	AHI[4:0]#, HA[16:3]#	HREQ[2:0]#
0	HAa[37:36,33:32,30,16:3]#	HREQa[2:0]#
1	HAa[39:38,35:34,31]#, HAPa#, HAa[29:17]#	HREQa[5:3]#
2	HAb[37:36,33:32,30,16:3]#	HREQb[2:0]#
3	HAb[39:38,35:34,31]#, HAPb#, HAb[29:17]#	HREQb[5:3]#

V4 bus evolved from Intel's P4 bus. Where the suffix a# and b# are referred to as P4 bus's signal package a and b respectively.

Figure 5. Rx60.1 VIA's V4 Bus Address Conveying Mechanism – 4X Sampling

Offset Address: 61-67h (D0F1) – Reserved

Offset Address: 68h (D0F1)

CPU Bus Parity Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU Bus Address Parity Check** This bit is used to enable the CPU address bus parity check. When this bit is enabled, if the address parity error happened, the error bit in Rx60[7] will be set. Note that no matter what the status of this bit is, the address parity driven by this chip during an upstream cycle should be always correct. 0: Disabled. 1: Enabled.
6:4	RW	0	**Reserved**
3	RW	0	**Parity Test for CPU Bus Address** This bit is to invert the status of the coming in address parity (i.e. inverted the HAPa# and HAPb#, refer to Figure 5). The purpose of this bit is to test the system at the case when CPU bus parity error happened. 0: Disabled. For a normal system, this bit should be stayed at 0. 1: Enabled, the address parity coming in to this chip will be inverted.
2:0	RW	0	**Reserved**

Offset Address: 69-6Fh (D0F1) – Reserved

DEVICE 0 FUNCTION 2 (D0F2): CPU BUS CONTROLLER (V4IF)

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 6 below.

Device 0 Function 2 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 2. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**010**	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

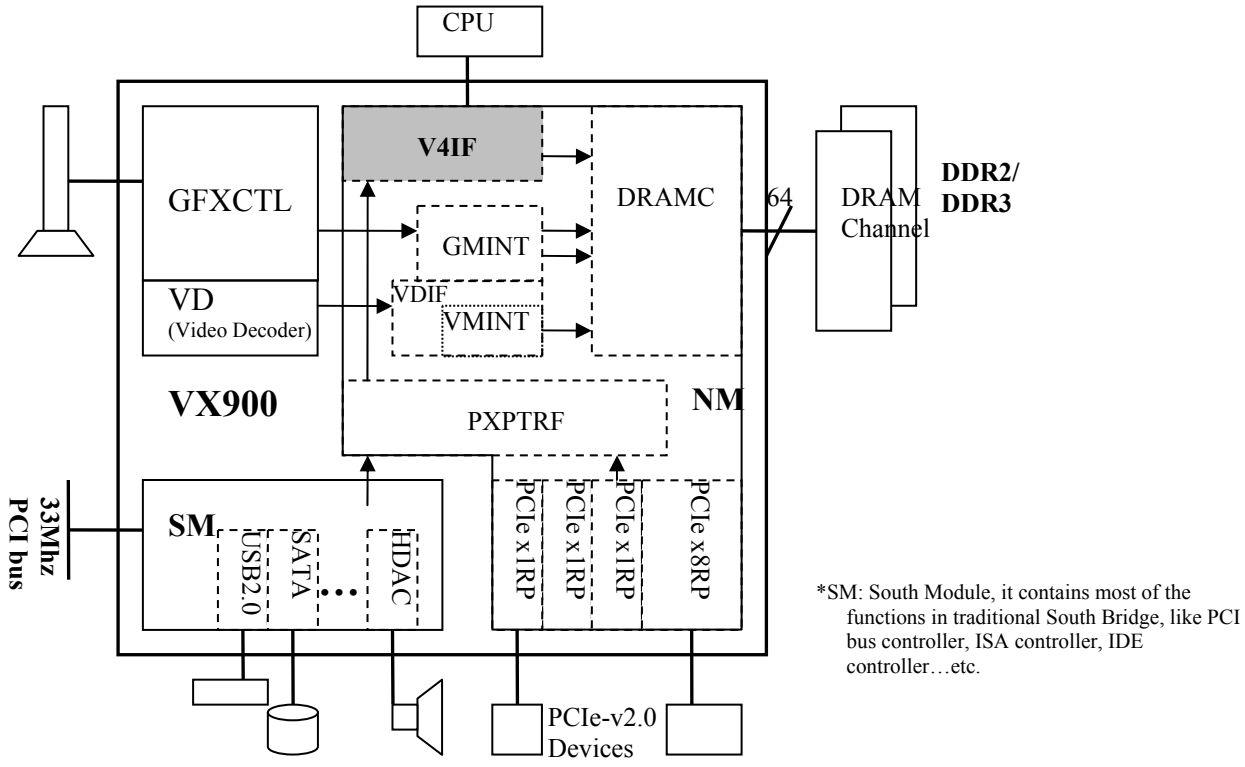


Figure 6. System Block Diagram for D0F2

The registers in this function (D0F2) control most of the logics in the shadow block named as V4IF which is the CPU bus controller (also known as "host controller" in the previous versions of VIA's chipsets) of this chip. CPU bus controller handles cycles (memory, I/O and special) from CPU to DRAM, PCIe devices, internal integrated graphic device (GFX) and other devices in the South Module. It also handles upstream cycles (memory) from PCIe devices and other devices in SM.

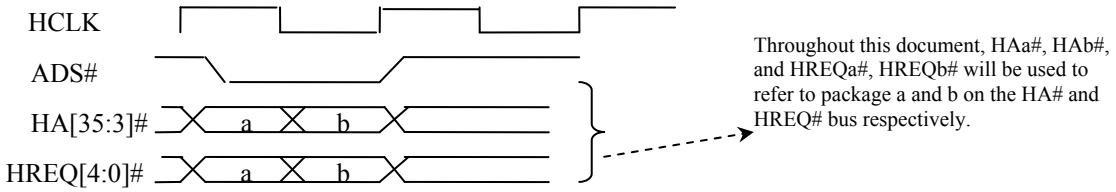


Figure 7. Intel's P4 Bus Address Conveying Mechanism – 2X Sampling

Conventional X2 Sampling Mechanism

This chip supports bus protocol for VIA – C7/CN series CPU in the CPU bus. The figure above shows the P4 Bus X2 sampling protocol. Throughout this document, HAa#, HAb#, HREQa# and HREQb# will be used to refer to the package a and b of HA# and HREQ# pins. For example, HAa[35:3]# from the package a of the HA[35;3]# is referred to the address of the current cycle. HBE[7:0]# (or HAb[15:8]#) from the package b of the HA[15:8]# is the byte enable of the current cycle. For details of HAa#, HAb# definition, please refer to Table 4.

Table 4. Definitions of Request Signals for P4 Bus Protocol

Pin Name	Pin Mnemonic	Signal Name	Signal Mnemonic	Number of Pins
Request Command	HREQ[4:0]#	Request	HREQa[4:0]#	5
		Extended Request	HREQb[4:0]#	
Address	HA[35:3]#	Address	HAa[35:3]#	33
		Debug	HAb[35:32]#	
		Attributes	ATTR[7:0]# or HAb[31:24]#	
		Deferred ID	DID[7:0]# or HAb[23:16]#	
		Byte Enables	HBE[7:0]# or HAb[15:8]#	
		Extended Functions	EXF[4:0]# or HAb[7:3]#	

When mentioning commands (I/O, MEMR, MEMW, special cycles), it is actually referring to the command decoded from the combination of HREQa[4:0]# and HREQb[4:0]#. For example, MEMR (Memory data/code Read) is composed by {HREQa[2]#=1, HREQa[1]#=1/0, HREQa[0]#=0}. I/O Write is composed by {HREQa[4:0]#=11h}. Table 5 gives the details of the commands. Those ASZ# notation in the table indicates address bus size. Those LEN# notation in the table indicates the length of the data which is going to be transferred. For VIA C7 series CPU, DSZ# = 00b means that the current cycle is 8QW cycle and each bit of {HAb[31:24]#,HBE[7:0]#} indicating the active DW in the 8QW data transfer phase. DSZ# = 11b means an interleaved burst order is given in the data transfer phase. Cycles with DSZ# = 10b or 01b are not supported by this chipset.

Table 5. Transaction Types Defined by HREQa# and HREQb# Signals

Transaction	HREQa[4:0]#					HREQb[4:0]#				
	4	3	2	1	0	4	3	2	1	0
Deferred Reply	0	0	0	0	0	x	x	x	x	x
Reserved	0	0	0	0	1	x	x	x	x	x
Interrupt Acknowledge	0	1	0	0	0	DSZ#		x	0	0
Special Transactions	0	1	0	0	0	DSZ#		x	0	1
Reserved	0	1	0	0	0	DSZ#		x	1	x
Branch Trace Message	0	1	0	0	1	DSZ#		x	0	0
Reserved	0	1	0	0	1	DSZ#		x	0	1
Reserved	0	1	0	0	1	DSZ#		x	1	x
I/O Read	1	0	0	0	0	DSZ#		x	LEN#	
I/O Write	1	0	0	0	1	DSZ#		x	LEN#	
Reserved	1	1	0	0	x	DSZ#		x	x	x
Memory Read & Invalidate	ASZ#		0	1	0	DSZ#		x	LEN#	
Reserved	ASZ#		0	1	1	DSZ#		x	LEN#	
Memory Code Read	ASZ#		1	D/C#=0	0	DSZ#		x	LEN#	
Memory Data Read	ASZ#		1	D/C#=1	0	DSZ#		x	LEN#	
Memory Write (may not be retried)	ASZ#		1	W/WB#=0	1	DSZ#		x	LEN#	
Memory Write (may be retried)	ASZ#		1	W/WB#=1	1	DSZ#		x	LEN#	

Where

LEN[1:0]#		Length of Data Transfer
0	0	0-8 bytes
0	1	16 bytes
1	0	32 bytes
1	1	Reserved

ASZ[1:0]#		Memory Address Space
0	0	32 bit
0	1	36 bit
1	x	Reserved

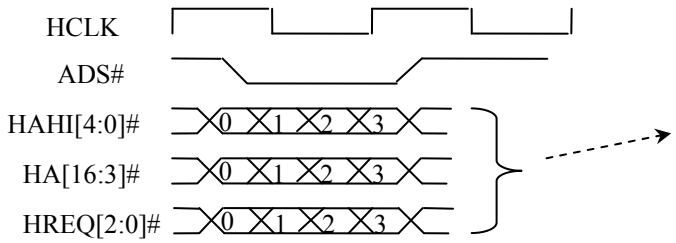
DSZ[1:0]#		BE# and Data Burst Order
0	0	Write combining for 8QW
0	1	Invalid
1	0	Invalid
1	1	Interleaved burst order

Table 6. Data Transfer Burst Order

Linear	Interleaved
0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

VIA V4 Bus - Innovative X4 Sampling Mechanism

Instead of having HA[35:3]# and HREQ[4:0]#, VIA's C7/CN series CPU used X4 sampling at address phase on the CPU bus. This CPU bus with X4 sampling capability on request phase defined by VIA's C7/CN series CPU is called the "V4 bus". The X4 sampling means there are four beats of information in the request phase where the ADS# is asserted. VIA's CN series CPU have pins address A[16:3]#, AHI[4:0]# (in VX900 Series, only HAHI[1:0]# signals are available since this chip supports address up to A33.) and REQ[2:0]#. All the information we needed in the address phase can be gotten from the table in Figure 8.



V4 bus's signal definition can be mapped to signal definitions of P4 bus:

Beat	AHI[4:0]#, A[16:3]#	REQ[2:0]#
0	HAa[37:36,33:32,30,16:3]#	HREQa[2:0]#
1	HAa[39:38,35:34,31]#, HAPa#, HAa[29:17]#	HREQa[5:3]#
2	HAb[37:36,33:32,30,16:3]#	HREQb[2:0]#
3	HAb[39:38,35:34,31]#, HAPb#, HAb[29:17]#	HREQb[5:3]#

Where the suffix a# and b# are referred to as P4 bus's signal package a and b respectively.

Figure 8. VIA's V4 Bus Address Conveying Mechanism – 4X Sampling

In the document following, for the convenience on the address notation, we still use X2 sampling terminologies like HAa#, HAb#, HREQa# to represent the information got in the address phase. We need to refer to the table in Figure 8 later to know the notation meaning for those X2 naming. Thus, even there is no HA[17]# in the pin definition for VIA's CPU, for example, HAa[17]# is the status of HA[3]# in the beat 1.

Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F2)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** Used to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F2)

Device ID **Default Value: 2410h**

Bit	Attribute	Default	Description
15:0	RO	2410h	**Device ID** Used to identify this function.

Offset Address: 05-04h (D0F2)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RO	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F2)

PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RO	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RO	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	01b	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast 01: Medium 10: Slow 11: Reserved These bits won't affect the DEVSEL# timing on the PCI bus.
8	RO	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserts PERR# on a read cycle or observes the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encounters error upon the cycle it initiates. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F2)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** Indicates the revision ID of this function.

Offset Address: 0B-09h (D0F2)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F2)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F2)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The unit is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F2)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If bit 7 = 0, the device is single function. If bit 7 = 1, the device is multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value 80h indicates that this is a multi-function device.

Offset Address: 0Fh (D0F2)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F2)
Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D0F2)
Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 1B-18h (D0F2)
Base Address Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F2)
Base Address Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 3** This function does not claim base address.

Offset Address: 23-20h (D0F2)
Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 4** This function does not claim base address.

Offset Address: 27-24h (D0F2)
Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 5** This function does not claim base address.

Offset Address: 2B-28h (D0F2)
CardBus CIS Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F2)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F2)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F2) – Reserved

Offset Address: 34h (D0F2)

Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F2) – Reserved

Offset Address: 3D-3Ch (D0F2)

Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F2)

Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

Reserved Registers (40-4Fh)

Offset Address: 40-4Fh (D0F2) – Reserved

CPU Bus Interface Control (50-52h)

Offset Address: 50h (D0F2)

CPU Interface Control - Request Phase **Default Value: n0h**

Bit	Attribute	Default	Description
7	RO	dip	**IOQ (In-Order Queue) Depth** This bit works with Rx55[7] to determine the internal IO Queue depth of CPU bus (host) controller. **Rx50[7] / Rx55[7] / Description** 0 / x / 1 level 1 / 0 / 16 levels 1 / 1 / 12 levels This bit comes from the strapping value of Pin GPO39 during the hardware reset: L: This bit will be 1. H: This bit will be 0.
6	RO	0	**Reserved**
5	RW	0	**Faster CPU to DRAM Cycle** This bit is to reduce the latency for 1T for CPU to DRAM cycles. 0: Disable 1: Enable
4:0	RW	0	**Dynamic Defer Snoop Stall Count** These registers defined the expiration count for the Defer Snoop Stall timer. The timer starts counting at the beginning of the snoop phase of a cycle which is not directed to DRAM; it increases one for every 2 controller's clocks (same as CPU clock). Before the timer expires, the controller will use Snoop Stall protocol to extend the snoop phase. When the timer expires, if that cycle is not finished and the IOQ of this controller has been queued more cycles (could be from CPU before the snoop phase of the current request or from upstream masters), a Defer/Retry response will be replied to the CPU bus for that cycle. How the controller will do on the response phase will depend on the register setting on Rx51[4,1,0]. Please refer to Table 8. 00h: timer count is 0 clocks, i.e., the CPU bus controller goes to the response phase immediately. 01h: timer count is 2 clocks. …. 0Fh: timer count is 30 clocks. 10h: timer count is 32 clocks. …. 1Fh: timer count is 62 clocks. Note: Please refer to Table 7 Rx50 below for the response of the CPU bus controller at different situations.

Table 7. Rx50 Dynamic Defer Snoop Stall Table

Timer is Expired?	IOQ has more requests followed the current downstream cycles?	The current downstream cycles - Completion?	The action of the CPU bus controller of this chip does on the CPU bus upon the conditions on the left column:
No	-	No	Snoop Stall to extend the snoop phase.
No	-	Yes	Go to response phase and do Normal Data Response.
Yes	No	No	Snoop Stall to extend the snoop phase.
Yes	No	Yes	Go to response phase and do Normal Data Response
Yes	Yes	No	Go to response phase and do Defer/Retry Response
Yes	Yes	Yes	Go to response phase and do Normal Data Response

Offset Address: 51h (D0F2)

CPU Interface Control – Basic Option **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**Fast Cycle Control for CPU-to-DRAM Read Cycle** CPU bus controller finishes the CPU-to-DRAM read cycle earlier. These bits work with Rx54[3], Rx55[1] and Rx90[1:0] to have appropriate timing for CPU to DRAM read latency. 0: Disabled. This CPU bus controller will wait for all data (e.g. 8QW) coming back from the DRAM controller to finish its CPU-to-DRAM read cycle. i.e. the CPU bus controller won't get into the data phase on the CPU bus until all the data has returned from the DRAM controller. 1: Enabled. This CPU bus controller will finish its CPU-to-DRAM read cycle before all read data returned from the DRAM controller. This is for better CPU-to-DRAM read performance.
6	RW	0	**Read Around Write** This bit is for the feature that the CPU read command can bypass the queued CPU write command to let DRAM controller process the read first. 0: Disabled. 1: Enabled. Note: When this bit is enabled, the policy of CPU-to-DRAM write retire become critical for the entire system performance. Please refer to Table 9 & Table 11 for more details.
5	RW	0	**CPU-to-Memory Request Queue Control** This bit is the request pipelining for CPU bus controller to DRAM controller. The requests could be from CPU or upstream masters. 0: Disable. There will be at least 1T for consecutive requests being accepted by DRAM controller. 1: Enable. The requests from the CPU bus controller to DRAM controller can be consecutive, i.e., 1-1-1-1.
4	RW	1b	**Defer Response Control** This bit works for CPU memory Read cycles targeted to non-DRAM agents, some other memory cycles and CPU IOR cycles. Please refer to Table 8 Rx51 for details [Note 1]. 0: Disable. For the cycles listed above, CPU bus controller will do retry on the CPU bus until the cycle is complete. 1: Enable. For the cycles listed above, CPU bus controller will do defer on the CPU bus.
3	RW	0	**Defer / Retry Queue Entries** This bit specified the number of defer/retry queue entries for CPU memory read cycles targeted to non-DRAM agents and CPU IOR cycles. 0: 1 entry. 1: 2 entries
2	RW	0	**Defer / Retry Queue Sharing Policy** This bit only works with bit 3 = 1. The sharing policy for the two entries of the Defer/Retry Queue. 0: One entry for each processor in a dual processor situation. 1: Each entry is shared by the two CPUs in a dual processor situation.
1	RW	0	**Special Cycle Handling** This bit defines the handling behavior for special cycles from CPU. Please refer to Table 8 Rx51 for details [Note 1]. 0: CPU bus controller will treat the special cycle as a posted write cycle. A "Retry response" will be returned to CPU bus. 1: CPU bus controller will treat the special cycle as a non-posted write cycle. A "Defer response" will be returned to CPU bus.
0	RW	0	**Defer Response Control for I/O Write and Some Memory Write Cycles** This bit defines the chip's behavior during response phase for I/O write and some memory write cycles. Please refer to Table 8 Rx51 for details [Note 1]. 0: CPU bus controller will do defer response on the CPU bus for some cycles. 1: CPU bus controller will always do retry on the CPU bus for the some cycles until those cycles are complete.

Note 1: For different downstream cycles on the CPU side, with different registers setting at Rx51[4], Rx51[1] and Rx51[0], the CPU bus controller's response are shown in the Table 8 Rx51.

Table 8. Rx51 The CPU Bus Controller's Response for Different Cycles at Different Register Settings

	RX51[4]	0	0	0	0	1	1	1	1
	RX51[1]	0	0	1	1	0	0	1	1
	RX51[0]	0	1	0	1	0	1	0	1
Cycles	**Target**	**Response Phase Action**							
CPU Memory Read, CPU Lock Read	DRAM	vcc	vcc	vcc	vcc	vcc	vcc	vcc	vcc
	RCRB, Extended configuration, others (PCIe, GFX, or SB devices) *	R	R	R	R	D	D	D	D
CPU I/O Read	Internal configuration space, Others (PCIe, GFX, or SB devices)	R	R	R	R	D	D	D	D
CPU Memory Write	DRAM	vcc	vcc	vcc	vcc	vcc	vcc	vcc	vcc
	RCRB, Extended configuration *	R	R	R	R	R	D	R	D
	Others (PCIe, GFX, or SB devices)	vcc	vcc	vcc	vcc	vcc	vcc	vcc	vcc
CPU Lock Write	DRAM	vcc	vcc	vcc	vcc	vcc	vcc	vcc	vcc
	Others (PCIe, GFX, or SB devices)	R	R	R	R	R	D	R	D
CPU IO Write	Internal configuration space, Others (PCIe, GFX, or SB devices)	R	R	R	R	R	D	R	D
Special Cycle	SB devices	R	R	R	R	R	R	R	D

vcc stands for Normal; **D** stands for Defer; **R** stands for Retry
*RCRB, extended configuration space are internal register spaces. Please refer to D0F5 for more information.

Table 9. DRAM Write Retire Policy

RX51[6]	RX52[3]	RX55[2]	RX56[7:4]	RX5D[7:4]	RX5D[3:0]	Write Policy* for write requests which might come from CPU or upstream masters.
0	-	-	----	----	----	CPU bus controller will issue read or write cycles to the DRAM controller in the order of their coming in sequence. These include upstream cycles.
1	0	-	----	----	----	If the DRAM bus is idle (i.e. all the DRAM read cycles are finished), the CPU bus controller will of course start to flush all DRAM write requests out. However, if the DRAM bus is busy (i.e. DRAM read cycles are on going), the CPU bus controller will start to flush those write requests only when the write queue is full. It will stop flushing when the write queue is not full.
1	1	0	----	x	y	If the DRAM bus is idle (i.e. all the DRAM read cycles are finished), the CPU bus controller will of course start to flush all DRAM write requests out. However, if the DRAM bus is busy (i.e. DRAM read cycles are on going), CPU bus controller will start to flush the write requests out to the DRAM controller when the request count in the write queue accumulates to x, and it will stop flushing those write requests when the request count in the write queue lowers to y. where x= 0000b means count is 1, x=1111b means count is 16; y= 0000b means count is 1, y=1111b means count is 16; and since the write queue in this chip is only 12 levels, so: (a) x must be in between 0000b and 1011b (b) y must be in between 0000b and 1011b (c) x must be >= y.
1	1	1	z	x	y	If the DRAM bus is idle (i.e. all the DRAM read cycles are finished), the CPU bus controller will of course start to flush all DRAM write requests out. However, if the DRAM bus is busy (i.e. DRAM read cycles are on going), CPU bus controller will start to flush the write requests out to the DRAM controller when the request count in the write queue accumulates to z, and it will stop flushing those write requests when the request count in the write queue lowers to y. where z= 0000b means count is 1, z=1111b means count is 16; y= 0000b means count is 1, y=1111b means count is 16; and since the write queue in this chip is only 12 levels, so: (a) z must be in between 0000b and 1011b (b) y must be in between 0000b and 1011b (c) z must be >= y. (d) z must be <= x.

Note: In addition to what listed in this table, there are extra adjustments in Table 11. Please also refer to register Rx5E, Rx5F[2], Rx5F[1] for more information.

Offset Address: 52h (D0F2)

CPU Interface Control – Advanced Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**RS Response Phase Pipeline Control** This bit defines the interval in between two response phases of CPU write and CPU read (including upstream read cycles). 0: 1T. The interval between two response phases is at least 1T. 1: 0T. The pins HRS[2:0]# can be continuously asserted.
6	RW	0	**High Priority Request to DRAM controller** This bit defines the priority of the requests to DRAM controller for efficient DRAM usage. 0: Disable. All the cycles to DRAM controller will be treated as normal priority. 1: Enable. Requests to DRAM controller will have high priority when a.) The CPU write request queue is full, or b.) The upstream cycles which target to DRAM controller have high priority entity (this can be done by programming corresponding register bits on the register space of different devices connected to the system).
5	RO	0	**Reserved**
4	RW	0	**Reserved**
3	RW	0	**DRAM Write Retire Policy – 1** Used to control DRAM write retire policy with high and low threshold on the request counts in the write queues for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 9 for detailed operations. 0: Disable. 1: Enable
2	RW	0	**Defer Policy With Lock Cycle** For two consecutive CPU to non DRAM agents read cycles, when the first lock read cycle is deferred, this bit provides what the CPU bus controller will respond for the second normal read cycle before the first lock read cycle is finished. 0: Defer response. 1: Retry response.
1	RW	0	**Speculative Read Policy** Speculative read refers to the case that the CPU bus controller issues read request to the DRAM controller prior to knowing the result of the snoop of a read request which originates from the CPU or an upstream device. However, if the read cycle does hit the cache inside another CPU (for multi-CPU's case) or inside the single CPU (i.e. for upstream read cycle's case), the speculative read which had just been executed will need to be discarded. This bit control the speculative read behavior of this chip. This bit will co-work with Rx52[0]. x0: Speculative read is disabled, i.e., CPU bus controller only issues read to DRAM controller after it gets to know the snoop result of that read cycle. 01: Speculative read applied only when the read request queue in the CPU bus controller before this in coming read request is empty, i.e., the speculative read only happened for the first read in a bunch of consecutive reads. 11: Speculative read applied to every read request.
0	RW	0	**Speculative Read Policy** Speculative read refers to the case that the CPU bus controller issues read request to the DRAM controller prior to knowing the result of the snoop of a read request which originates from the CPU or an upstream device. However, if the read cycle does hit the cache inside another CPU (for multi-CPU's case) or inside the single CPU (i.e. for upstream read cycle's case), the speculative read which had just been executed will need to be discarded. This bit control the speculative read behavior of this chip. This bit will co-work with Rx52[1]. x0: Speculative read is disabled, i.e., CPU bus controller only issues read to DRAM controller after it gets to know the snoop result of that read cycle. 01: Speculative read applied only when the read request queue in the CPU bus controller before this in coming read request is empty, i.e., the speculative read only happened for the first read in a bunch of consecutive reads. 11: Speculative read applied to every read request.

DRAMC Interface Control (53-56h)

Offset Address: 53h (D0F2)

DRAMC Interface Control - Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CPU Occupancy Timer** In arbitration for the read/write requests to DRAM controller from the CPU or the upstream master devices, this timer guarantees a period of time counted by the number of CPU clocks (in unit of 4) that the requests from the CPU can be serviced as long as there are continuous requests from the CPU. 0000: Infinite. i.e. as long as there are requests from the CPU, the arbiter will serve those requests from CPU before it switches to serve for the requests from upstream masters. 0001: 1 x 4 clocks. 0010: 2 x 4 clocks. … 1111: 15 x 4 clocks.
3:0	RW	0	**Master Occupancy Timer** In arbitration for the read/write requests to DRAM controller from the CPU or the upstream master devices, this timer guarantees a period of time counted by the number of clocks (in unit of 4) that the requests from the upstream masters can be serviced as long as there are continuous requests from the upstream master devices. 0000: Infinite. i.e. as long as there are requests from the upstream masters, the arbiter will serve those requests from upstream masters before it switches to serve for the requests from CPU. 0001: 1 x 4 clocks. 0010: 2 x 4 clocks. … 1111: 15 x 4 clocks.

Note: The CPU bus controller arbitrates the requests from the CPU and upstream masters guarded by these two occupancy timers. When two requests coming in from CPU and the upstream master at the same time, the controller will serve the one which had been serviced last time.

Offset Address: 54h (D0F2)

DRAMC Interface Control – Miscellaneous 1 **Default Value: n0h**

Bit	Attribute	Default	Description
7:5	RO	dip	**CPU Front Side Bus (FSB) Frequency** These bits indicated the internal HCLK (CPU bus controller's main clock) frequency of this chip. 000: 100Mhz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: Reserved 110: Reserved 111: Reserved
4	RW	1b	**8QW Burst Memory Access** CPU bus controller takes 8QW read/write cycles from either CPU or upstream masters and sends them to DRAM controller. This bit is to control the way this controller handles those 8QW cycles. 0: Disable. CPU bus controller splits the 8QW R/W requests into two 4QW cycles. 1: Enable. CPU bus controller will forward the 8QW R/W requests to DRAM controller. Note: This bit needs to be set to 0 in DRAM 32bit mode (D0F3, Rx6C[3] = 1).
3	RW	0	**CPU Bus Controller to DRAM Read Cycle Control – 1** This bit is the read cycle control for requests from either CPU or upstream masters to DRAM controller. This bit works with other registers (Rx51[7], Rx54[1], Rx55[1], Rx90[1:0]) in different conditions for the DRAM read cycle. 0: Normal mode. 1: Special mode. The controller will use Rx90[1:0] to determine the DRDY timing.
2	RW	0	**Merge 4QW to 8QW Burst Memory Access for Upstream Cycles.** The bit is the option for CPU bus controller to merge two 4QW upstream master read or write cycles into one 8QW cycle and send it to DRAM controller. 0: Disable 1: Enable When bit 4 = 0, the 8QW cycles will be split into 4QW cycle, it is thus meaningless to enable this bit. In such case, it is suggested to set this bit to 0.
1	RW	0	**Memory to CPU Bus Controller Conversion Mode** This register option affects the timing of CPU bus controller to DRAM controller accessing. 0: Transparent mode. It is 1T faster for some control signals in between DRAMC and CPU bus controller than those in synchronous mode. 1: Synchronous mode. Some control signals will be synchronized 1T in between DRAMC and CPU bus controller.
0	RW	0	**Reserved** Writing 0 or 1 to this bit does not have any impact to this chip.

Offset Address: 55h (D0F2)

DRAMC Interface Control – Miscellaneous 2 **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**CPU Bus Interface IOQ (In-Order Queue) Size** This bit works with Rx50[7] to determine the internal IO Queue depth of this CPU bus controller. **Rx50[7]** / **Rx55[7]** / **Description** 0 / x / 1 level 1 / 0 / 16 levels 1 / 1 / 12 levels
6	RW	0	**Reserved** This bit must be always set to 0.
5	RW	1b	**Reserved** This bit must be always set to 1.
4:3	RW	0	**Reserved**
2	RW	0	**DRAM Write Retire Policy – 2** In addition to write queue threshold registers in Rx5D[7:4] and Rx5D[3:0], this register is an extra option for write retire policy with medium threshold on the request counts in the write queues for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 9 for detail operation. 0: Disable 1: Enable
1	RW	0	**CPU Bus Controller to DRAM Read Cycle Control – 2** This bit is the read cycle control for requests from either CPU or upstream masters to DRAM controller. 0: Several T faster 1: 2T slower Note: This bit works with other registers (Rx54[1], Rx55[3], Rx90[1:0]) in different conditions for the DRAM read cycle.
0	RW	0	**Reserved**

Offset Address: 56h (D0F2)

DRAMC Interface Control - Write Policy 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Medium Threshold for Write Retire Policy** These registers indicate the request count in the write queue as the medium threshold for flushing write. They work with Rx55[2] for extra write retire policy for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 9 for details. 0000: 1 write request. 0001: 2 write requests. … 1011: 12 write requests. 11xx: Invalid setting.
3	RW	0	**Reserved**
2	RW	0	**Upstream Request 3T Rate** This bit is the request queuing rate for CPU bus controller to accept upstream requests from PCIe devices or other master devices (i.e. SATA, USB ..). 0: Disable. 2T request rate 1: Enable. 3T request rate Note: It is suggested to set this bit to 1 when HCLK (main clock of the CPU bus controller) is faster than 266Mhz.
1	RW	0	**Flushing Write Requests Upon Snoop Requests from GFXCTL** Internal integrated GFX controller - GFXCTL snoops the post write buffers. And if there is a hit, with this bit is enabled, this CPU bus controller will flush write requests out to the DRAM with the highest priority. i.e. These flushed write requests will pass all read requests queued. When this bit is disabled, the snoop result is ignored, the write requests in the post write buffers will follow other rules waiting to be put to the DRAM bus. 0: Disable 1: Enable
0	RW	0	**High Priority Upstream Requests** Enabling of this bits gives higher priority for the upstream masters when CPU bus controller arbitrates in between CPU and upstream masters for obtaining the CPU (V4) bus. The priority of the requests also depends on the priority setting of each master devices. i.e. Even with this bit being enabled, if the corresponding priority bit of the master device had not been set, the priority of the request won't be raised. 0: Disable 1: Enable Note: The high priority attribute comes with the request from the traffic controller module (shown as PXPTRF in Figure 6). Please refer to RCRB register sets Rx200~Rx255, Rx234[7] is an example of setting the priority to high for requests from conventional master devices in the SB.

CPU Bus Interface Control (57-5Ch)

Offset Address: 57h (D0F2)

CPU Bus Interface - V4 Bus Features **Default Value: nnh**

Bit	Attribute	Default	Description
7:1	RW	HwInit	**Reserved**
0	RW	0 ROMSIP	**CPU Bus HREQ5 Support** Unlike Intel's P4, VIA's C7/CN series CPUs only have three HREQ pins: HREQ0#, HREQ1# and HREQ2#. By using 4X sampling, we have information at beat 1 of HREQ[2:0]# (please refer to Figure 8) for HREQa[3]#, HREQa[4]# (which P4 had as pins) and HREQa[5]#. VIA's C7 source-2 CPU (and CN series followed) introduced to use the extra information – HREQa[5]# which indicates the processor may assert DBSY# for adding wait states at the data phase of the current write cycle. In this case, the fast TRDY feature (this chip accepts the write data earlier, please refer to Rx96[3]) cannot work. Thus, the chip must dynamically turn the fast TRDY feature off when it detects HREQa[5]# is asserted. 0: CPU bus controller will never activate the fast TRDY feature. 1: CPU bus controller will detect the de-assertion of HREQa[5]# to activate the fast TRDY feature for the current downstream write cycles. Note: 1. This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST# (Assertion of PCIRST# is also called the hardware initialization period). The corresponding programming bit is at the secondary QW, byte 0, bit[0] in the initialization ROM. 2. Fast TRDY feature is an enhanced protocol introduced after VIA's C7 source-1 CPU. This feature is also controlled by register Rx96[3] and Rx9E[7]. For details on the enabling of the fast TRDY feature, please refer to the Table 10 below.

Table 10. Enabling of Fast TRDY Feature

CPU	RX57[0]	RX96[3]	RX9E[7]	Request # in the internal downstream queue	Dynamic Fast TRDY feature	Comment
C7 Source-1	0	-	-	-	off	
	1	0	-	-	off	
	1	1	-	-	n/a	Invalid setting, system cannot work normally.
C7 Source-2 or CN	0	-	-	-	off	
	1	0	-	-	off	
	1	1	0	-	on	CPU bus controller will detect the status of HREQa[5]# to enable the fast TRDY feature
			1	> 1	on	
			1	1 or 0	off	

Offset Address: 58h (D0F2) – Reserved

Offset Address: 59h (D0F2)

CPU Interface Control – CPURST# **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved** This bit should be always set to 0.
6	RW	0	**Reserved**
5:4	RW	0	**Warm CPU Reset (CPURST#) Duration Control** These two bits defined the active duration of the CPURST# when bit 3 is programmed to 1. 00: 2us 01: 10us 10: 15us 11: 16us Note: 1. The internal design uses the HCLK to count; however, the chip will adjust the clock counts to meet the time programmed here. 2. VIA's CPU required at least 15us assertion time for the CPURST#, these bits should be set at either 10b or 11b for most of the cases.
3	RW	1b	**Warm CPU Reset (CPURST#) Trigger** A 0 to 1 transition of this bit will trigger warm reset, i.e. CPURST# will be driven low for a certain period of time. The active duration of the CPURST# is defined at bits [5:4]. Software will have to write this bit to "0" before writing "1" to trigger another CPURST#.
2	RW	0	**CPU-to-DRAM Access Control** This bit is to delay one T for the request from CPU bus controller to DRAM controller. 0: Disable 1: Enable Note: It is suggested to set this bit to 1 when DCLK (DRAM main clock) is faster than 533Mhz.
1	RW	0	**Reserved**
0	RW	0	**MSI Cycle IPI (Inter-Processor Interrupt) Flat Model Support** While working with multiple CPUs, this bit is to let the CPU bus controller take the Message Interrupt cycle (downstream from one CPU) and re-direct that Message Interrupt cycle to the local APIC controller inside those CPU cores with least task priority. The address bit AHa[3:2]# of this coming in MSI cycle equals to 11b. 0: Disable 1: Enable

Offset Address: 58-5Bh (D0F2) – Reserved

Offset Address: 5Ch (D0F2)

CPU Bus Interface Control – APIC & MSI **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Data Bit 11 Mask for Redirected MSI Cycle** Used for the IPI (Inter-Processor Interrupt) support, the chipset takes the MSI cycle (downstream cycle from one CPU) whose redirection hint bit (address bit Aha[3]#) is set to 1 and redirect that MSI cycle to proper CPU cores. Rx59[0] is the enable bit for the IPI support. However, for proper operation, this bit should always be set to 1. 0: Data bit[11] of the redirected MSI cycle uses the ICR (Interrupt Command Register) bit[11] from CPU. 1: Data bit[11] of the redirected MSI cycle is 1.
3:0	RW	0	**Reserved**

DRAMC Interface Control (5D-5Fh)

Offset Address: 5Dh (D0F2)

DRAMC Interface Control - Write Policy 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**High Threshold for Write Retire Policy** These registers indicate the request count in the write queue as the high threshold for flushing write. They work with Rx52[3] for write retire policy for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 9 for details. 0000: 1 write request 0001: 2 write requests … 1011: 12 write requests 11xx: Invalid setting
3:0	RW	0	**Low Threshold for Write Retire Policy** These registers indicate the request count in the write queue as the low threshold for flushing write. They work with Rx52[3] for write retire policy for CPU or upstream memory write cycles to DRAM controller. Please refer to Table 9 for details. 0000: 1 write request 0001: 2 write requests … 1011: 12 write requests 11xx: Invalid setting

Offset Address: 5Eh (D0F2)

DRAMC Interface Control - Bandwidth Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Preset Counts For Host Bandwidth Counter** A counter called Host (CPU bus) Bandwidth Counter is used to direct this chip to a period called HOSTBW period when Rx5F[2] is 1. In this HOSTBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 11 for details. The counter is loaded with the programmed value after the reset or when the chip is going to enter the DRAMBW period (please refer to Rx5E[3:0]). The counter decreases by one whenever a non-DRAM cycle is issued by the CPU. Before the counter counts down to zero, if there is a cycle targeted to DRAM coming in, the counter will also be reloaded. Working with DRAM Bandwidth counter (Rx5E[3:0]), when the counter counts down to zero, it gives an indication that the past several cycles are not targeted to DRAM. The chip enters the HOSTBW period to handle the write cycles to DRAM in an appropriate way. Basically, under normal operation, the chip should be running in between HOSTBW and DRAMBW period. Thus, the write policy to DRAM is changing dynamically. 0000: Immediately. It means the chip is always running at HOSTBW period. 0001: If 1 CPU cycle not targeted to DRAM comes, the chip goes into HOSTBW period. 0010: If 2 consecutive CPU cycles not targeted to DRAM come, the chip goes into HOSTBW period. … 1111: If 15 consecutive CPU cycles not targeted to DRAM come, the chip goes into HOSTBW period.
3:0	RW	0	**Preset Counts For DRAM Bandwidth Counter** A counter called DRAM Bandwidth Counter is used to direct this chip to a period called DRAMBW period when Rx5F[1], RDRAMBW is 1. In this DRAMBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 11 for details. The counter is loaded with the programmed value after the reset or when the chip is going to enter the HOSTBW period (please refer to Rx5E[7:4]). The counter decreases by one whenever a DRAM cycle is issued by CPU or other masters (upstream cycles go through CPU bus too). Before the counter is counted down to zero, if there is cycle not targeted to DRAM coming in, the counter will also be reloaded. Working with HOST Bandwidth counter (Rx5E[7:4]), when the counter counts down to zero, it gives an indication that the past several cycles are all targeted to DRAM. The chip enters the DRAMBW period to handle the write cycles to DRAM in an appropriate way. Basically, under normal operation, the chip should be running in between HOSTBW and DRAMBW period. Thus, the write policy to DRAM is changing dynamically. 0000: Immediately. It means the chip is always running at DRAMBW period. 0001: If 1 CPU cycle targeted to DRAM comes, the chip goes into DRAMBW period. 0010: If 2 consecutive CPU cycles targeted to DRAM come, the chip goes into DRAMBW period. … 1111: If 15 consecutive CPU cycles targeted to DRAM come, the chip goes into DRAMBW period.

Table 11. DRAM Write Retire Policy Adjustments in HOSTBW Period and DRAMBW Period

HOSTBW Period	DRAMBW Period	DRAM write policy adjustments* besides those shown in Table 9
0	0	When the chip is in neither HOSTBW period nor DRAMBW period (Rx5F[2] = 0 and Rx5F[1] = 0), the write to DRAM policy followed what Table 9 described.
1	0	This case happened when Host Bandwidth Period (Rx5F[2]) is 1 and Host Bandwidth counter (Rx5E[7:4]) counted down to zero; The DRAM write policy described in Table 9 will be adjusted to: a. When the DRAM bus is idle, as long as there is write request queued, as described in Table 9, the CPU bus controller should flush the write right away. However, in this case, the CPU bus controller won't start the DRAM write unless there is no DRAM read from the CPU or upstream masters in the coming up consecutive 8T. i.e. the CPU bus controller will delay 8T to make decision of flushing the writes out. Within this 8T, if there is any DRAM read cycle comes in, the CPU bus controller won't flush the write. b. When the DRAM bus is not idle, and when the write requests in the write queue accumulated over the high (or medium, when Rx55[2] = 1) threshold, as described in Table 9, the CPU bus controller should flush the write. However, in this case, if there is DRAM read coming in from the CPU or upstream masters, it won't start the DRAM write unless the write queue is currently full.
0	1	This case happened when DRAM Bandwidth period (Rx5F[1]) is 1 and DRAM Bandwidth counter (Rx5E[3:0]) counted down to zero; The DRAM write policy described in Table 9 will be adjusted to: a. When the DRAM bus is idle, as long as there is write request queued, as described in Table 9, the CPU bus controller should flush the write right away. However, in this case, the CPU bus controller won't start the DRAM write unless there is no DRAM read from the CPU or upstream masters at the current moment. i.e. the CPU bus controller will start to flush the write as long as there is no DRAM read request coming in. b. When the DRAM bus is not idle, and when the write requests in the write queue accumulated over the high (or medium, when RX55[2] = 1) threshold, as described in Table 9, the CPU bus controller should flush the write. However, in this case, if there is DRAM read coming in from the CPU or upstream masters, it won't start the DRAM write unless the write queue is currently full. (This b operating condition is the same as that described in last row, case b of HOSTBW period =1.)
1	1	This case only happened when 1. Both Host Bandwidth period (Rx5F[2]) and DRAM Bandwidth period (Rx5F[1]) are enabled and 2. The Host bandwidth counter (Rx5E[7:4]) and the DRAM bandwidth counter (Rx5E[3:0]) are both programmed to 00h. In a normal operation, such programming (2. above) is abnormal. Even so, the DRAM write policy described in Table 9 will be adjusted to: a. As described in Table 9, no matter whether there is DRAM read coming in or not, the CPU bus controller won't issue write until the write requests accumulated over the high (or medium) threshold. In this case, if there is no DRAM read request coming in, CPU bus controller will flush the write requests as long as it accumulated the write requests to two. b. As described in Table 9, the CPU bus controller won't issue write until the write requests accumulated over the high (or medium) threshold. In this case, if any one of the writes in the write queue has the same memory page as the one on processing to DRAM controller, the CPU bus controller will start flush the write out to DRAM controller even that the write request number in the write queue is only larger than the low threshold.

Note: These adjustments only apply to the third and fourth rows in the Table 9, where the Rx51[6] and Rx52[3] are both 1.

A typical HOSTBW and DRAMBW operating behavior is shown in Figure 6 below. During HOSTBW period and DRAMBW period, the DRAM write retire policy will be a slight different. Please refer to the case a on the second row and third row on the Table 11 above. To summarize, when DRAM bus is idle, during HOSTBW period, we did give CPU bus side a little bit more time (8T) to see if there is DRAM read needed to be serviced before we serve the DRAM write. i.e. During HOSTBW period, the chip gives DRAM read cycle more priority. When DRAM bus is not idle, during these two periods, the chip gives DRAM read cycle the highest priority, those DRAM write cycles only can be flushed out when the write queue is full.

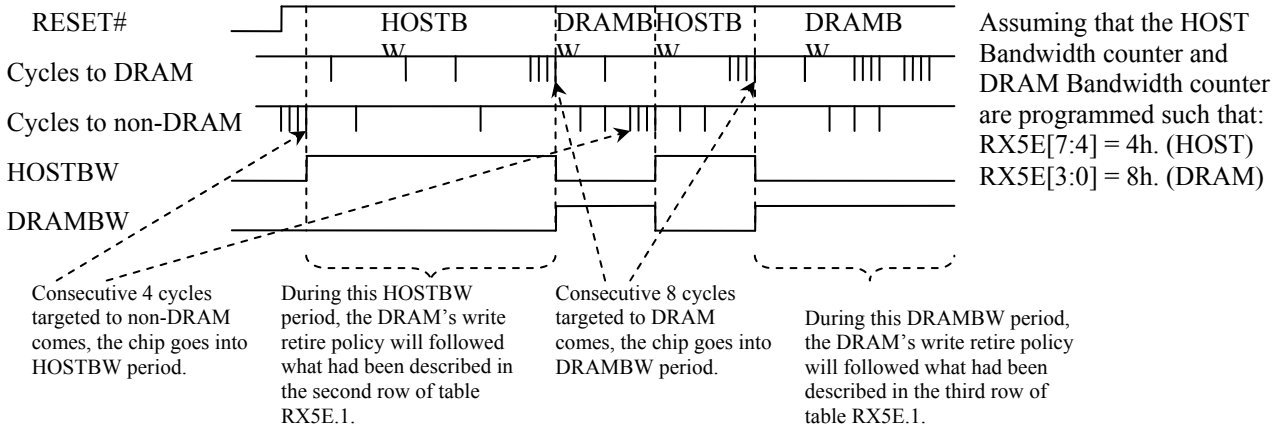


Figure 9. A Typical Behavior of HOSTBW and DRAMBW when Rx5F[2] and Rx5F[1] Are Both Programmed to 1

Offset Address: 5Fh (D0F2)

DRAMC Interface Control – Bandwidth Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Retry Queue Reordering** For CPU downstream cycles, this bit is to control the behavior of the retired cycles for the CPU requests queued in the Retry Queue. 0: Retried CPU transactions always complete in order. 1: Allow the second retired transaction (IOW/MEMW) to complete before the previous retried transaction. Note that this chip has only two levels of retry queue for the transactions on the CPU bus.
5:4	RW	0	**Reserved**
3	RO	0	**Reserved**
2	RW	0	**Host Bandwidth Period** This bit works with Host Bandwidth Counter, Rx5E[7:4]. In the HOSTBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 11. 0: Disable. The chip will never go to HOSTBW period. 1: Enable. The chip will go to HOSTBW period when Host Bandwidth Counter is counted down to zero.
1	RW	0	**DRAM Bandwidth Period** This bit works with DRAM Bandwidth Counter, Rx5E[3:0]. In the DRAMBW period, the policy for write cycles (from either CPU or upstream devices) to DRAM will be slightly adjusted to have the best system performance. Please refer to Table 11. 0: Disable. The chip will never go to DRAMBW period. 1: Enable. The chip will go to DRAMBW period when the DRAM Bandwidth Counter is counted down to zero.
0	RW	0	**Reserved**

Data Return Timing Control For CPU-To-DRAM Read Cycle (60-67h)

DRDY (Data Ready) is a control signal to indicate the read data is ready between CPU bus controller and DRAM controller inside the chip. The timing of DRDY will affect the accessing time of the read cycle for CPU-to-DRAM because the controller has to make sure that the timing of the read data retuned to CPU bus is consistent with the timing of DRDY. The register settings at Rx51[7], Rx54[1], Rx54[3], Rx55[1] and Rx90[1:0] will affect the DRDY timing. Control registers in Rx60[4:0] are detail timing control for the read data returning to the CPU bus. They need to be programmed to certain values when the chip is operated in different CPU/DRAM frequency with different register setting at those DRDY timing related registers.

Offset Address: 60h (D0F2)

DRAMC Interface Control - DRDY Timing **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Auto Mode for the Data Return Timing Adjustment** According to DRDY timing, the Data Return Timing (of a CPU-to-DRAM read cycle) can be determined automatically by frequency combinations of CPU bus controller and DRAM controller. 0: Manual Mode. Data Return Timing is determined by bits [4:0]. 1: Auto Mode. Data Return Timing is automatically set based on DRDY timing and CPU/DRAM working frequency.
4	RW	0	**Manual Adjustment for the Data Return Timing – 3** This bit determines the wait state timing of the second 4QW data phase in a Line Read cycle (CPU-to-DRAM 8QW read cycle). 0: No wait state. 1: 1T wait state. Note: This bit works only when bit 5 = 0.
3:2	RW	0	**Manual Adjustment for the Data Return Timing – 2** These bits determine the wait state timing of the first 4QW data phase in a line read cycle (CPU-to-DRAM 8QW read cycle). 00: No wait state 01: 1T wait state 10: 2T wait state 11: 3T wait state Note: These bits work only when bit [5] = 0.
1:0	RW	0	**Manual Adjustment for the Data Return Timing – 1** These bits determine the wait state timing of the data phase in a QW (1, 2, 4QW) read cycle (There is only 1QW read request from the VIA's CPU). 00: No wait state. 01: 1T wait state. 10: 2T wait state. 11: 3T wait state. Note: These bits work only when bit 5 = 0.

Offset Address: 61-67h (D0F2) – Reserved

APIC Logic Control (68-6Fh)

Offset Address: 68h (D0F2)
APIC CPU Priority 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 00h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_0qq0h. This register will be updated with qqh.

Offset Address: 69h (D0F2)
APIC CPU Priority 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 01h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_1qq0h. This register will be updated with qqh.

Offset Address: 6Ah (D0F2)
APIC CPU Priority 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 02h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_2qq0h. This register will be updated with qqh.

Offset Address: 6Bh (D0F2)
APIC CPU Priority 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 03h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_3qq0h. This register will be updated with qqh.

Offset Address: 6Ch (D0F2)
APIC CPU Priority 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 04h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_4qq0h. This register will be updated with qqh.

Offset Address: 6Dh (D0F2)
APIC CPU Priority 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 05h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_5qq0h. This register will be updated with qqh.

Offset Address: 6Eh (D0F2)

APIC CPU Priority 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 06h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_6qq0h. This register will be updated with qqh.

Offset Address: 6Fh (D0F2)

APIC CPU Priority 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Logical APIC ID of APIC Which Has Physical Local APIC ID = 07h** The value is updated when the CPU bus controller decoded a special cycle with HREQa# = 08h, HREQb# = 19h, and HAa# = FEE0_7qq0h. This register will be updated with qqh.

CPU Bus AGTL+ I/O Driving Control (70–7Dh)

In manual mode (when Rx7A[7] is set to 0), the register setting on the Rx70~Rx73 provides the driving setting for those pull-up and pull-down resistance on the AGTL+ I/O. In Auto-Compensation mode (when Rx7A[7] is set to 1), the register setting on Rx70~Rx73 becomes an offset to be added to the compensation result (RxA2) provided by the AGTL+ Auto compensation circuitry in the chip. Figure 10 provides an illustration of the driving setting scheme. This chip needs to work on a lot of different scenarios. Ideally, those register setting should be provided by a self-adjusted way – the Auto-Compensation mode. However, manual mode is designed to provide more flexibility.

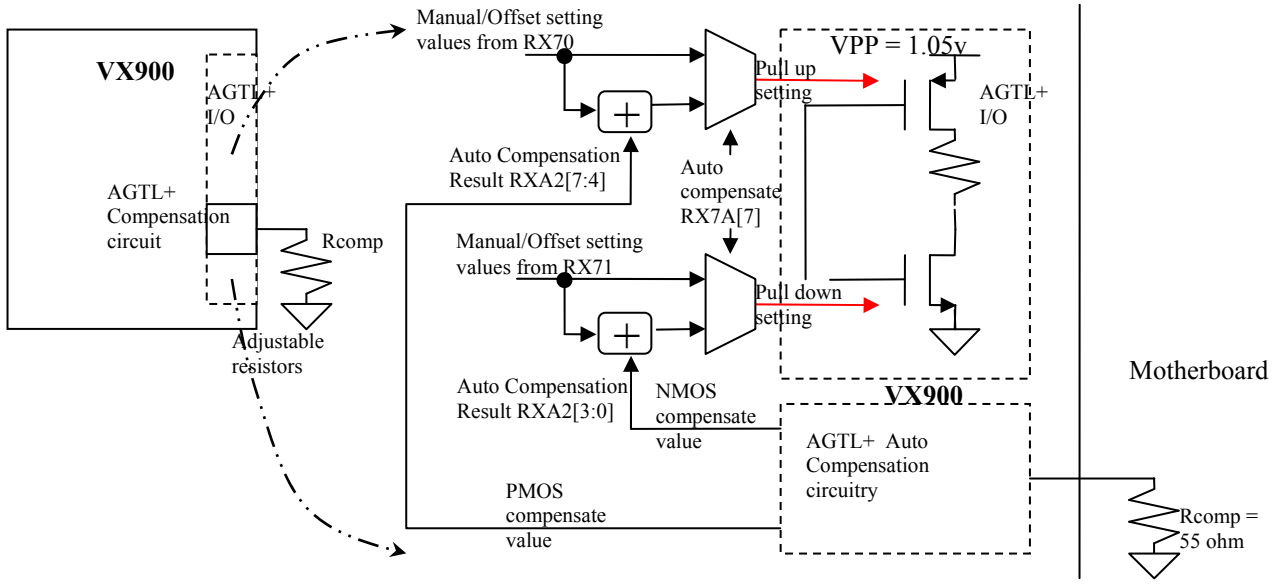


Figure 10. Pull Up and Pull Down Resistance Register Control on the AGTL+ I/O – Use HA as An Example

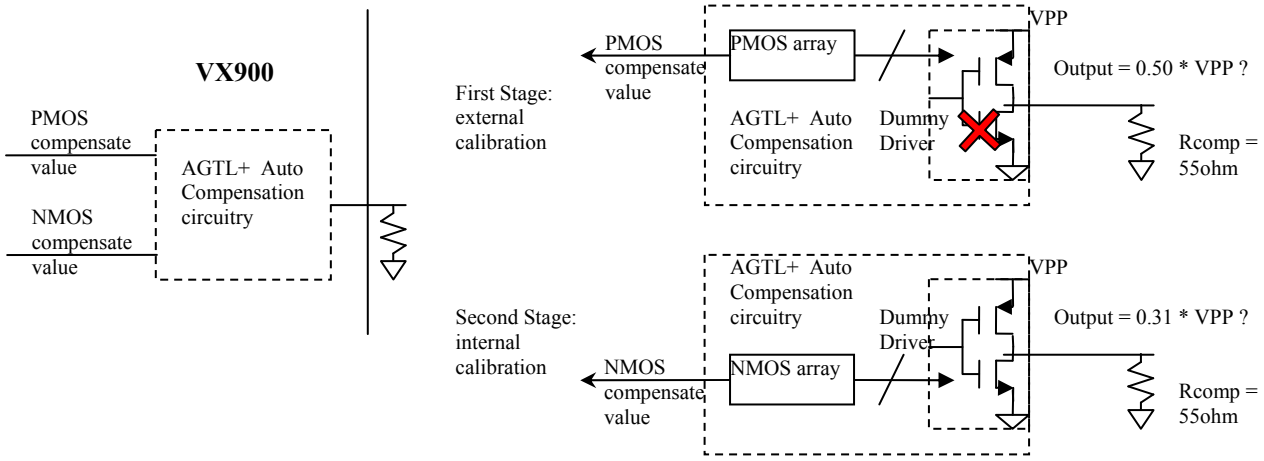


Figure 11. Calibration Process for the AGTL+ Auto Compensation Circuitry

This chip builds a circuit inside trying to detect the situations on the motherboard and to provide appropriate driving setting for those high speed AGTL+ I/O. As illustrated in the Figure 11 above, after the power is applied (or the chip resumes from C3, C4, C5 or S1 power state depending on the register setting at RxBE[4]), the calibration process starts trying to have the PMOS/NMOS compensate value. This process consists of two calibration stages. During external calibration, with the NMOS transistor shutting off, PMOS array of external dummy driver is calibrated against the external resistor (Rcomp = 55 ohm) until the output is tracked at around 0.5 VPP (Please refer to register setting at RxBE[3:2]). Then compensation circuit switches to internal calibration stage. During internal calibration, NMOS array of the internal dummy driver is calibrated with respect to the selected PMOS transistor (determined at the first stage – external calibration) in series with a poly resistor until the output reaches 0.31 VPP (Please refer to register setting at RxBE[3:2]). When two calibration stages are completed, auto compensation circuit comes up with a setting so that the effective resistance on the AGTL+ I/O can match that on the other end of the GTL bus.

Offset Address: 70h (D0F2)

Pull Up Driving CPU Bus Address **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Pull-Up Resistance for Address Strobe – HADSTB0P#, HADSTB0N#** The HADSTB0N# and HADSTB0P# are the differential pair for the strobe used to latch address information at the request phase for VIA's C7/ CN series CPU. These bits are for the pull-up resistance for the driving setting of HADSTB0N# and HADSTB0P#. Please refer to Figure 10 for the driving setting structure. ***For Manual Mode:*** When *auto compensation mode is disabled* (Rx7A[7] = 0), the driving setting is in manual mode, the corresponding pull-up resistance values are: 0000: 105 ohm 0001: 90 ohm 0010: 80 ohm 0011: 73 ohm 0100: 68 ohm 0101: 63 ohm 0110: 60 ohm 0111: 57 ohm 1000: 55 ohm 1001: 53 ohm 1010: 51 ohm 1011: 50 ohm 1100: 49 ohm 1101: 48 ohm 1110: 47 ohm 1111: 46 ohm Note: 1. The values of pull-up effective resistor value are as listed. They are based on typical case, a -38% to +43% of variance may need to be applied. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the first QW, byte 0, bits[7:4] in the initialization ROM. ***For Auto Mode:*** When *auto compensation mode is enabled* (Rx7A[7] =1), the driving setting is in auto compensate mode, these bits are acting as an offset to the PMOS compensate value (RxA2[3:0]) resulting from the calibration at the auto compensation circuitry. The pull-up setting is obtained as shown: 0000: Pull-up setting = RxA2[3:0] 0001: Pull-up setting = RxA2[3:0] + 1 0010: Pull-up setting = RxA2[3:0] + 2 0011: Pull-up setting = RxA2[3:0] + 3 0100: Pull-up setting = RxA2[3:0] + 4 0101: Pull-up setting = RxA2[3:0] + 5 0110: Pull-up setting = RxA2[3:0] + 6 0111: Pull-up setting = RxA2[3:0] + 7 1000: Pull-up setting = RxA2[3:0] – 8 1001: Pull-up setting = RxA2[3:0] – 7 1010: Pull-up setting = RxA2[3:0] – 6 1011: Pull-up setting = RxA2[3:0] – 5 1100: Pull-up setting = RxA2[3:0] – 4 1101: Pull-up setting = RxA2[3:0] – 3 1110: Pull-up setting = RxA2[3:0] – 2 1111: Pull-up setting = RxA2[3:0] – 1 Note: 3. The effective resistance values are provided on the description for the manual mode above. 4. If the pull-up setting above is greater than 1111b, the final pull-up setting will be 1111b. If the pull-up setting above is less than 0000b, the final pull-up setting will be 0000b.
3:0	RW	1000b ROMSIP	**Pull-Up Resistance for Address – HAHI[1:0]#, HA[16:3]#, HREQ[2:0]#, HABI#** These bits are for the pull-up resistance for the driving setting of HAHI[1:0]#, HA[16:3]#, HREQ[2:0]#, and HABI#. Please refer to Figure 10 for the driving setting structure. The operation of these bits is as those described in Rx70[7:4]. When in manual mode (auto compensation mode is disabled), these registers defined the same pull-up resistance value for signals mentioned above as those presented in the Rx70[7:4]. When in auto compensation mode, these registers also act as an offset to be added to the PMOS compensate value in RxA2[3:0] as shown in Rx70[7:4]. The only difference is the ROMSIP location, they are at the first QW, byte 0, bits[3:0] in the initialization ROM.

Offset Address: 71h (D0F2)

Pull Down Driving CPU Bus Address **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Pull-Down Resistance for Address Strobe – HADSTB0P#, HADSTB0N#** The HADSTB0N# and HADSTB0P# are the differential pair for the strobe used to latch address information at the request phase for the VIA's C7/ CN series CPU. These bits are for the pull-down resistance for the driving setting of HADSTB0N# and HADSTB0P#. Please refer to Figure 10 for the driving setting structure. When *auto compensation mode is disabled* (Rx7A[7] = 0), the driving setting is in manual mode, the corresponding pull-down resistance are: 0000: 51 ohm 0001: 43 ohm 0010: 38 ohm 0011: 34 ohm 0100: 32 ohm 0101: 29 ohm 0110: 28 ohm 0111: 26 ohm 1000: 25 ohm 1001: 24 ohm 1010: 23 ohm 1011: 22 ohm 1100: 22 ohm 1101: 21 ohm 1110: 21 ohm 1111: 20 ohm Note: 1. The pull-down effective resistor value is as listed. They are based on typical case, a -45% to +43% of variance may need to be applied. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the first QW, byte1, bit[7:4] in the initialization ROM. When *auto compensation mode is enabled* (Rx7A[7] =1), the driving setting is in auto compensate mode, these bits are acting as an offset to the NMOS compensate value (RxA2[7:4]) resulting from the calibration at the auto compensation circuitry. The pull-down setting is obtained as shown: 0000: Pull-down setting = RxA2[7:4] 0001: Pull-down setting = RxA2[7:4] + 1 0010: Pull-down setting = RxA2[7:4] + 2 0011: Pull-down setting = RxA2[7:4] + 3 0100: Pull-down setting = RxA2[7:4] + 4 0101: Pull-down setting = RxA2[7:4] + 5 0110: Pull-down setting = RxA2[7:4] + 6 0111: Pull-down setting = RxA2[7:4] + 7 1000: Pull-down setting = RxA2[7:4] – 8 1001: Pull-down setting = RxA2[7:4] – 7 1010: Pull-down setting = RxA2[7:4] – 6 1011: Pull-down setting = RxA2[7:4] – 5 1100: Pull-down setting = RxA2[7:4] – 4 1101: Pull-down setting = RxA2[7:4] – 3 1110: Pull-down setting = RxA2[7:4] – 2 1111: Pull-down setting = RxA2[7:4] – 1 Note: 3. The effective resistance value are provided on the description for the manual mode above. 4. If the pull-down setting above is greater than 1111b, the final pull-down setting will be 1111b. If the pull-down setting above is less than 0000b, the final pull-down setting will be 0000b.
3:0	RW	1000b ROMSIP	**Pull-Down Resistance for Address – HAHI[1:0]#, HA[16:3]#, HREQ[2:0]#, HABI#** These bits are for the pull-down resistance for the driving setting of HAHI[1:0]#, HA[16:3]#, HREQ[2:0]#, and HABI#. Please refer to Figure 10 for the driving setting structure. The operation of these bits is as those described in Rx71[7:4]. When in manual mode (auto compensation mode is disabled), these registers defined the same pull-down resistance value for signals mentioned above as those presented in the Rx71[7:4]. When in auto compensation mode, these registers also act as an offset to be added to the NMOS compensate value in RxA2[7:4] as shown in Rx71[7:4]. The only difference is the ROMSIP location, they are at the first QW, byte 1, bits[3:0] in the initialization ROM.

Offset Address: 72h (D0F2)

Pull Up Driving CPU Bus Data **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Pull-Up Resistance for Data Strobe – HDSTB[3:0]vcc#, HDSTB[3:0]P#** These bits are for the pull-up resistance for the driving setting of HDSTB[3:0]vcc# and HDSTB[3:0]P#. Please refer to Figure 10 for the driving setting structure. When *auto compensation mode is disabled* (Rx7A[7] = 0), the driving setting is in manual mode, the corresponding pull-up resistance are: 0000: 105 ohm 0001: 90 ohm 0010: 80 ohm 0011: 73 ohm 0100: 68 ohm 0101: 63 ohm 0110: 60 ohm 0111: 57 ohm 1000: 55 ohm 1001: 53 ohm 1010: 51 ohm 1011: 50 ohm 1100: 49 ohm 1101: 48 ohm 1110: 47 ohm 1111: 46 ohm Note: 1. The pull-up effective resistor value is as listed. They are based on typical case, a -38% to +43% of variance may need to be applied. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the first QW, byte 2, bits[7:4] in the initialization ROM. When *auto compensation mode is enabled* (Rx7A[7] =1), the driving setting is in auto compensate mode, these bits are acting as an offset to the PMOS compensate value (RxA2[3:0]) resulting from the calibration at the auto compensation circuitry. The pull-up setting is obtained as shown: 0000: Pull up setting = RxA2[3:0]. 0001: Pull up setting = RxA2[3:0] + 1 0010: Pull up setting = RxA2[3:0] + 2 0011: Pull up setting = RxA2[3:0] + 3 0100: Pull up setting = RxA2[3:0] + 4 0101: Pull up setting = RxA2[3:0] + 5 0110: Pull up setting = RxA2[3:0] + 6 0111: Pull up setting = RxA2[3:0] + 7 1000: Pull up setting = RxA2[3:0] – 8 1001: Pull up setting = RxA2[3:0] – 7 1010: Pull up setting = RxA2[3:0] – 6 1011: Pull up setting = RxA2[3:0] – 5 1100: Pull up setting = RxA2[3:0] – 4 1101: Pull up setting = RxA2[3:0] – 3 1110: Pull up setting = RxA2[3:0] – 2 1111: Pull up setting = RxA2[3:0] – 1 Note: 3. The effective resistance value are provided on the description for the manual mode above. 4. If the pull-up setting above is greater than 1111b, the final pull-up setting will be 1111b. If the pull-up setting above is less than 0000b, the final pul-up setting will be 0000b.
3:0	RW	1000b ROMSIP	**Pull-Up Resistance for Data – HD[63:0]#, HDBI[3:0]#** These bits are for the pull-up resistance for the driving setting of HD[63:0]# and HDBI[3:0]#. Please refer to Figure 10 for the driving setting structure. The operation of these bits is as those described in Rx72[7:4]. When in manual mode (auto compensation mode is disabled), these registers defined the same pull-up resistance value for signals mentioned above as those presented in the Rx72[7:4]. When in auto compensation mode, these registers also act as an offset to be added to the PMOS compensate value in RxA2[3:0] as shown in Rx72[7:4]. The only difference is the ROMSIP location, they are at the first QW, byte 2, bits[3:0] in the initialization ROM.

Offset Address: 73h (D0F2)

Pull Down Driving CPU Bus Data **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Pull-Down Resistance for Data Strobe– HDSTB[3:0]vcc#, HDSTB[3:0]P#** These bits are for the pull-down resistance for the driving setting of HDSTB[3:0]vcc# and HDSTB[3:0]P#. Please refer to Figure 10 for the driving setting structure. When *auto compensation mode is disabled* (Rx7A[7] = 0), the driving setting is in manual mode, the corresponding pull-down resistance are: 0000: 51 ohm 0001: 43 ohm 0010: 38 ohm 0011: 34 ohm 0100: 32 ohm 0101: 29 ohm 0110: 28 ohm 0111: 26 ohm 1000: 25 ohm 1001: 24 ohm 1010: 23 ohm 1011: 22 ohm 1100: 22 ohm 1101: 21 ohm 1110: 21 ohm 1111: 20 ohm Note: 1. The pull-down effective resistor value is as listed. They are based on typical case, a -45% to +43% of variance may need to be applied. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the first QW, byte 3, bits[7:4] in the initialization ROM. When *auto compensation mode is enabled* (Rx7A[7] =1), the driving setting is in auto compensate mode, these bits are acting as an offset to the NMOS compensate value (RxA2[7:4]) resulting from the calibration at the auto compensation circuitry. The pull-down setting is obtained as shown: 0000: Pull-down setting = RxA2[7:4] 0001: Pull-down setting = RxA2[7:4] + 1 0010: Pull-down setting = RxA2[7:4] + 2 0011: Pull-down setting = RxA2[7:4] + 3 0100: Pull-down setting = RxA2[7:4] + 4 0101: Pull-down setting = RxA2[7:4] + 5 0110: Pull-down setting = RxA2[7:4] + 6 0111: Pull-down setting = RxA2[7:4] + 7 1000: Pull-down setting = RxA2[7:4] – 8 1001: Pull-down setting = RxA2[7:4] – 7 1010: Pull-down setting = RxA2[7:4] – 6 1011: Pull-down setting = RxA2[7:4] – 5 1100: Pull-down setting = RxA2[7:4] – 4 1101: Pull-down setting = RxA2[7:4] – 3 1110: Pull-down setting = RxA2[7:4] – 2 1111: Pull-down setting = RxA2[7:4] – 1 Note: 3.The effective resistance value are provided on the description for the manual mode above. 4. If the pull-down setting above is greater than 1111b, the final pull-down setting will be 1111b. If the pull-down setting above is less than 0000b, the final pull-down setting will be 0000b.
3:0	RW	1000b ROMSIP	**Pull-Down Resistance for Data – HD[63:0]#, HDBI[3:0]#** These bits are for the pull-down resistance for the driving setting of HD[63:0]# and HDBI[3:0]#. Please refer to Figure 10 for the driving setting structure. The operation of these bits is as those described in Rx73[7:4]. When in manual mode (auto compensation mode is disabled), these registers defined the same pull-down resistance value for signals mentioned above as those presented in the Rx73[7:4]. When in auto compensation mode, these registers also act as an offset to be added to the NMOS compensate value in RxA2[7:4] as shown in Rx73[7:4]. The only difference is the ROMSIP location, they are at the first QW, byte 3, bits[3:0] in the initialization ROM.

Offset Address: 74-75h (D0F2) – Reserved

Offset Address: 76h (D0F2)
CPU Interface Control - DBI **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RW	HwInit	**Reserved**
4	RW	1b ROMSIP	**6bit/7bit VID VRM Strapping Selection** 0: chipset drive HA13_high in address strapping to inform processor 6bit VID VRM selection 1: Chipset drive HA13_low in address strapping to inform processor 7bit VID VRM selection
3	RW	0 ROMSIP	**Power Down Input Comparators of AGTL+ IO Buffers When in S3 State** When the chip is in S3 state (Suspend-to-DRAM state, the system suspends and stores all of the system information to DRAM) where most of the logic core in the chip is powered down. However, if the external power source is not able to be powered off, this option shuts off the power of the input buffer of the AGTL+ I/O to have more power conservation on the AGTL+ bus. 0: Disable 1: Enable Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the first QW, byte 5, bit[6] in the initialization ROM.
2	RO	1b	**Reserved**
1	RW	0 ROMSIP	**DBI Function on the CPU Bus** HDBI[3:0]# are valid only when the HD[63:0]# are valid. When HDBI[3:0]# are low, it indicates the data bits of the corresponding data group are inverted. The HDBI[3:0]# and the data bus group are related as: HDBI3# goes with HD[63:48]# ; HDBI2# goes with HD[47:32]#; HDBI1# goes with HD[31:16]#; HDBI0# goes with HD[15:0]# 0: Enable. When this chip is in output mode, HDBI[3:0]# will be driven low to indicate that the data bits are inverted on the corresponding data bus group. 1: Disable. When this chip is in output mode, HDBI[3:0]# will always stay at high. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the first QW, byte 4, bit[7] in the initialization ROM.
0	RW	0 ROMSIP	**DBI Functional Mode** This register bit defined the generation method of HDBI[3:0]#. 0: DBI signals HDBI[3:0]# are generated to minimize the number of changes on the data bits. i.e. The HDBI[3:0]# are asserted if the number of data bits changed (0->1 or 1-> 0) on its corresponding data group from the previous clock cycle to the current clock cycle are equal to or greater than 8. 1: DBI signals HDBI[3:0]# are generated to minimize the AGTL+ pull-down count. i.e. The HDBI[3:0]# are asserted if the number of "low" on the data bits on its corresponding data group for the current clock cycle are equal to or greater than 8. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the first QW, byte 4, bit[6] in the initialization ROM.

Offset Address: 77-79h (D0F2) – Reserved

Offset Address: 7Ah (D0F2)

AGTL Auto Compensation **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	0 ROMSIP	**Auto-Compensation Mode** Auto compensation mode for those pull-up and pull-down setting for high speed AGTL+ I/O control. These I/O are HADSTB0N#, HADSTB0P#, HAHI[1:0]#, HA[16:3]#, HREQ[2:0]#, HDSTB[3:0]vcc#, HDSTB[3:0]P#, HD[63:0]#, HDBI[3:0]# and other 1X I/O signals like HADS#.. Please refer to Figure 10 for more information. 0: Disable. The pull-up / pull-down setting for high speed AGTL+ I/O will be provided by those in Rx70~ Rx73 and RxA1. 1: Enable. The pull-up / pull-down setting for high speed AGTL+ I/O will use the addition of compensation result and the offset provided by Rx70~Rx73 and RxA1. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit are at the first QW, byte 4, bit[7] in the initialization ROM.
6:0	RW	HwInit	**Reserved**

Offset Address: 7B-7Dh (D0F2) – Reserved

Output Beat Time Control for HA and HD (7E-8Fh)

Offset Address: 7Eh (D0F2)

Beat Time Control for CPU Bus Address **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Beat Time Adjustment Enable for Even/Odd Beat of Address Signals** This bit controls the Beat Time adjustment for the 4X address phase signals: HREQ[2:0]#, HA[16:0]#, HABI# and HAHI[1:0]#. 0: Enable. The adjustment is based on the value specified at bits[6:5]. 1: Disable. The even/odd beat time is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 4, bit[5] in the initialization ROM.
6:5	RW	0 ROMSIP	**Beat Time Adjustment Value for Address Signals** These bits adjust the beat time of the even/odd beats of the 4X address phase signals: HREQ[2:0]#, HA[16:0]#, HABI#, and HAHI[1:0]#. These bits become valid only when bit 7 = 0. 00: Beat time of even beat is increased by 35ps. 01: Beat time of even beat is increased by 57ps. 10: Beat time of even beat is decreased by 26ps. 11: Beat time of even beat is decreased by 51ps. Note: 1. In a 0-1-2-3 address sequence, 0, 2 are referred as the even beat, 1, 3 are referred as the odd beat. These bits control the duty cycle of the internal clock. Thus, when beat time of even beat is increased by 40ps, it also means that of odd beat is decreased by 40ps, and vice versa. 2. The delay is measured at typical case, it can vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 4, bits[4:3] in the initialization ROM.
4:2	RW	0 ROMSIP	**Output Delay for Address Signals** These bits indicates the delay of the first (or fifth) beat for the 4X address phase signals: HREQ[2:0]#, HA[16:0]#, HABI#, and HAHI[1:0]# with respect to the controller's internal clock which is supposed to be aligned with the clock fed to CPU - HCLK. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 4, bits[2:0] in the initialization ROM.
1:0	RW	HwInit	**Reserved**

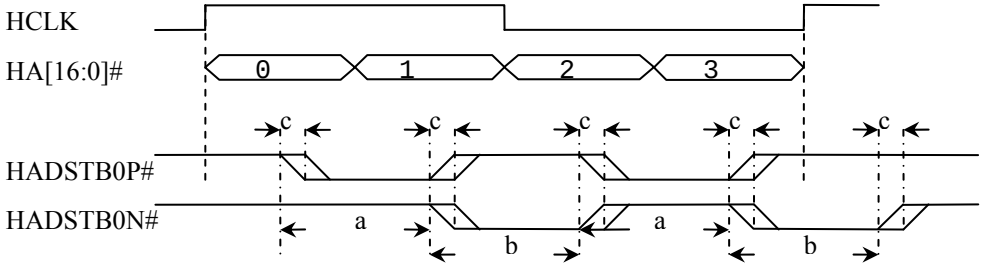


Figure 12. Timing Relationship for the Address and Address Strobe on the V4 Bus

Offset Address: 7Fh (D0F2)

Timing Control for CPU Bus Address Strobe **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Timing Adjustment Enable for Address Strobe** This bit controls the timing adjustment for the 4X address strobe signals: HADSTB0P#, HADSTB0N#. 0: Enable. The adjustment is based on the that value specified at bits[6:5]. 1: Disable. The timing of the address strobe is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 5, bit[5] in the initialization ROM.
6:5	RW	0 ROMSIP	**Timing Adjustment Value for Address Strobe** These bits determine the assertion/de-assertion time of the HADSTB0P# / HADSTB0N#. These bits become valid only when bit 7 = 0. 00: Assertion time of HADSTB0P# (a in Figure 12) is increased by 35ps. 01: Assertion time of HADSTB0P# is increased by 57ps. 10: Assertion time of HADSTB0P# is decreased by 26ps. 11: Assertion time of HADSTB0P# is decreased by 51ps. Note: 1. These bits control the duty cycle of the internal clock. Thus, when assertion time of HADSTB0P# (a in Figure 12) is increased, the assertion time of HADSTB0N# (b in Figure 12) will be decreased. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 5, bits[4:3] in the initialization ROM.
4:2	RW	0 ROMSIP	**Output Delay for Address Strobe** These bits indicates the delay for the 4X address strobe: HADSTB0P# and HADSTB0N# with respect to a clock which is 1/8T delay of controller's internal main clock. This internal main clock is supposed to be aligned with the clock fed to CPU - HCLK. Please refer to "c" in Figure 12. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 5, bits[2:0] in the initialization ROM.
1:0	RW	HwInit	**Reserved**

Offset Address: 80-83h (D0F2) – Reserved

Offset Address: 84h (D0F2)

Beat Time Control for CPU Bus Data – Group 0 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Beat Time Adjustment Enable for Even/Odd Beat of Data Signals (Group 0)** This bit controls the Beat Time adjustment for the 4X data phase signals: HD[15:0] and HDBI0. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The even/odd beat time is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 6, bit[5] in the initialization ROM.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Beat Time Adjustment Value for Data Signals (Group 0)** These bits adjust the beat time of the even/odd beats of the 4X data phase signals: HD[15:0] and HDBI0. These bits become valid only when bit 7 = 0. 00: Beat time of even beat is increased by 35ps. 01: Beat time of even beat is increased by 57ps. 10: Beat time of even beat is decreased by 26ps. 11: Beat time of even beat is decreased by 51ps. Note: 1. In a 0-1-2-3 data sequence, 0, 2 are referred as the even beat, 1, 3 are referred as the odd beat. These bits control the duty cycle of the internal clock. Thus, when beat time of even beat is increased by 40ps, it also means that of odd beat is decreased by 40ps, and vice versa. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[4:3] in the initialization ROM.
2:0	RW	0 ROMSIP	**Output Delay for Data Signals (Group 0)** These bits indicates the delay of the first (or fifth) beat for the 4X data phase signals: HD[15:0] and HDBI0 with respect to the controller's internal clock which is supposed to be aligned with the clock fed to CPU - HCLK. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[2:0] in the initialization ROM.

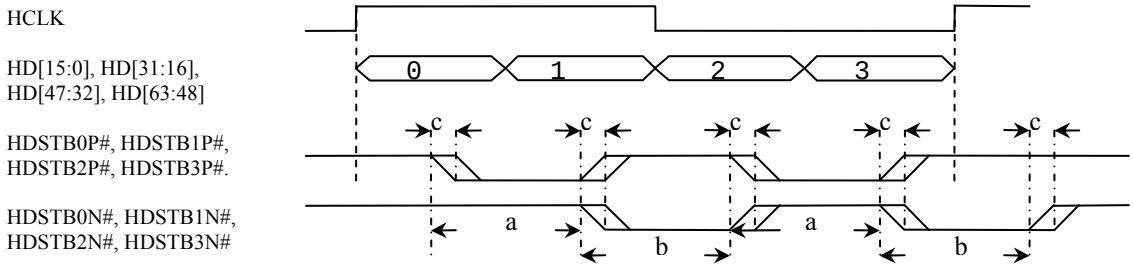


Figure 13. Timing Relationship for the Data and Data Strobe on the V4 Bus

Offset Address: 85h (D0F2)

Timing Control for CPU Bus Data Strobe – Group 0 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Timing Adjustment Enable for Data Strobe (Group 0)** This bit controls the timing adjustment for the 4X data strobe signals: HDSTB0P#, HDSTB0N#. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The timing of the address strobe is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 7, bit[5] in the initialization ROM.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Timing Adjustment Value for Data Strobe (Group 0)** These bits determine the assertion/de-assertion time of the HDSTB0P#/HDSTB0N#. These bits become valid only when bit 7 = 0. 00: Assertion time of HDSTB0P# (a in Figure 13) is increased by 35ps. 01: Assertion time of HDSTB0P# is increased by 57ps. 10: Assertion time of HDSTB0P# is decreased by 26ps. 11: Assertion time of HDSTB0P# is decreased by 51ps. Note: 1. These bits control the duty cycle of the internal clock. Thus, when assertion time of HDSTB0P# (a in Figure 13) is increased, the assertion time of HDSTB0N# (b in Figure 13) will be decreased. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[4:3] in the initialization ROM.
2:0	RW	0 ROMSIP	**Output Delay for Data Strobe (Group 0)** These bits indicates the delay for the 4X data strobe: HDSTB0P# and HDSTB0N# with respect to a clock which is 1/8T delay of controller's internal main clock. This internal main clock is supposed to be aligned with the clock fed to CPU – HCLK. Please refer to "c" in Figure 13. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[2:0] in the initialization ROM.

Offset Address: 86h (D0F2)

Beat Time Control for CPU Bus Data – Group 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Beat Time Adjustment Enable for Even/Odd Beat of Data Signals (Group 1)** This bit controls the Beat Time adjustment for the 4X data phase signals: HD[31:16] and HDBI1. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The even/odd beat time is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 6, bit[5] in the initialization ROM. Note that the ROMSIP bit is the same as that for Rx84[7] which is for Data Group 0.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Beat Time Adjustment Value for Data Signals (Group 1)** These bits adjust the beat time of the even/odd beats of the 4X data phase signals: HD[31:16] and HDBI1. These bits become valid only when bit 7 = 0. 00: Beat time of even beat is increased by 35ps. 01: Beat time of even beat is increased by 57ps 10: Beat time of even beat is decreased by 26ps 11: Beat time of even beat is decreased by 51ps Note: 1. In a 0-1-2-3 data sequence, 0, 2 are referred as the even beat, 1, 3 are referred as the odd beat. These bits control the duty cycle of the internal clock. Thus, when beat time of even beat is increased by 40ps, it also means that of odd beat is decreased by 40ps, and vice versa. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[4:3] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx84[4:3] which are for Data Group 0.
2:0	RW	0 ROMSIP	**Output Delay for Data Signals (Group 1)** These bits indicates the delay of the first (or fifth) beat for the 4X data phase signals: HD[31:16] and HDBI1 with respect to the controller's internal clock which is supposed to be aligned with the clock fed to CPU - HCLK. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[2:0] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx84[2:0] which are for Data Group 0.

Offset Address: 87h (D0F2)

Timing Control for CPU Bus Data Strobe – Group 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Timing Adjustment Enable for Data Strobe (Group 1)** This bit controls the timing adjustment for the 4X data strobe signals: HDSTB1P#, HDSTB1N#. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The timing of the address strobe is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 7, bit[5] in the initialization ROM. Note that the ROMSIP bit is the same as that for Rx85[7] which is for Data Group 0.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Timing Adjustment Value for Data Strobe (Group 1)** These bits determine the assertion/de-assertion time of the HDSTB1P#/HDSTB1N#. These bits become valid only when bit 7 = 0. 00: Assertion time of HDSTB1P# (a in Figure 13) is increased by 35ps. 01: Assertion time of HDSTB1P# is increased by 57ps. 10: Assertion time of HDSTB1P# is decreased by 26ps. 11: Assertion time of HDSTB1P# is decreased by 51ps. Note: 1. These bits control the duty cycle of the internal clock. Thus, when assertion time of HDSTB1P# (a in Figure 13) is increased, the assertion time of HDSTB1N# (b in Figure 13) will be decreased. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[4:3] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx85[4:3] which are for Data Group 0.
2:0	RW	0 ROMSIP	**Output Delay for Data Strobe (Group 1)** These bits indicates the delay for the 4X data strobe: HDSTB1P# and HDSTB1N# with respect to a clock which is 1/8T delay of controller's internal main clock. This internal main clock is supposed to be aligned with the clock fed to CPU – HCLK. Please refer to "c" in Figure 13. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[2:0] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx85[2:0] which are for Data Group 0.

Offset Address: 88h (D0F2)

Beat Time Control for CPU Bus Data – Group 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Beat Time Adjustment Enable for Even/Odd Beat of Data Signals (Group 2)** This bit controls the Beat Time adjustment for the 4X data phase signals: HD[47:32] and HDBI2. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The even/odd beat time is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 6, bit[5] in the initialization ROM. Note that the ROMSIP bit is the same as that for Rx84[7] which is for Data Group 0.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Beat Time Adjustment Value for Data Signals (Group 2)** These bits adjust the beat time of the even/odd beats of the 4X data phase signals: HD[47:32] and HDBI2. These bits become valid only when bit 7 = 0. 00: Beat time of even beat is increased by 35ps. 01: Beat time of even beat is increased by 57ps. 10: Beat time of even beat is decreased by 26ps. 11: Beat time of even beat is decreased by 51ps. Note: 1. In a 0-1-2-3 data sequence, 0, 2 are referred as the even beat, 1, 3 are referred as the odd beat. These bits control the duty cycle of the internal clock. Thus, when beat time of even beat is increased by 40ps, it also means that of odd beat is decreased by 40ps, and vice versa. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[4:3] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx84[4:3] which are for Data Group 0.
2:0	RW	0 ROMSIP	**Output Delay for Data Signals (Group 2)** These bits indicates the delay of the first (or fifth) beat for the 4X data phase signals: HD[47:32] and HDBI2 with respect to the controller's internal clock which is supposed to be aligned with the clock fed to CPU - HCLK. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[2:0] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx84[2:0] which are for Data Group 0.

Offset Address: 89h (D0F2)

Timing Control for CPU Bus Data Strobe – Group 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Timing Adjustment Enable for Data Strobe (Group 2)** This bit controls the timing adjustment for the 4X data strobe signals: HDSTB2P#, HDSTB2N#. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The timing of the address strobe is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 7, bit[5] in the initialization ROM. Note that the ROMSIP bit is the same as that for Rx85[7] which is for Data Group 0.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Timing Adjustment Value for Data Strobe (Group 2)** These bits determine the assertion/de-assertion time of the HDSTB2P#/HDSTB2N#. These bits become valid only when bit 7 = 0. 00: Assertion time of HDSTB1P# (a in Figure 13) is increased by 35ps. 01: Assertion time of HDSTB1P# is increased by 57ps. 10: Assertion time of HDSTB1P# is decreased by 26ps. 11: Assertion time of HDSTB1P# is decreased by 51ps. Note: 1.These bits control the duty cycle of the internal clock. Thus, when assertion time of HDSTB2P# (a in Figure 13) is increased, the assertion time of HDSTB2N# (b in Figure 13) will be decreased. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[4:3] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx85[4:3] which are for Data Group 0.
2:0	RW	0 ROMSIP	**Output Delay for Data Strobe (Group 2)** These bits indicates the delay for the 4X data strobe: HDSTB2P# and HDSTB2N# with respect to a clock which is 1/8T delay of controller's internal main clock. This internal main clock is supposed to be aligned with the clock fed to CPU – HCLK. Please refer to "c" in Figure 13. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[2:0] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx85[2:0] which are for Data Group 0.

Offset Address: 8Ah (D0F2)

Beat Time Control for CPU Bus Data – Group 3 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Beat Time Adjustment Enable for Even/Odd Beat of Data Signals (Group 3)** This bit controls the Beat Time adjustment for the 4X data phase signals: HD[63:48] and HDBI3. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The even/odd beat time is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 6, bit[5] in the initialization ROM. Note that the ROMSIP bit is the same as that for Rx84[7] which is for Data Group 0.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Beat Time Adjustment Value for Data Signals (Group 3)** These bits adjust the beat time of the even/odd beats of the 4X data phase signals: HD[63:48] and HDBI3. These bits become valid only when bit 7 = 0. 00: Beat time of even beat is increased by 35ps. 01: Beat time of even beat is increased by 57ps. 10: Beat time of even beat is decreased by 26ps. 11: Beat time of even beat is decreased by 51ps. Note: 1. In a 0-1-2-3 data sequence, 0, 2 are referred as the even beat, 1, 3 are referred as the odd beat. These bits control the duty cycle of the internal clock. Thus, when beat time of even beat is increased by 40ps, it also means that of odd beat is decreased by 40ps, and vice versa. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[4:3] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx84[4:3] which are for Data Group 0.
2:0	RW	0 ROMSIP	**Output Delay for Data Signals (Group 3)** These bits indicates the delay of the first (or fifth) beat for the 4X data phase signals: HD[63:48] and HDBI3 with respect to the controller's internal clock which is supposed to be aligned with the clock fed to CPU - HCLK. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 6, bits[2:0] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx84[2:0] which are for Data Group 0.

Offset Address: 8Bh (D0F2)

Timing Control for CPU Bus Data Strobe – Group 3 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	1b ROMSIP	**Timing Adjustment Enable for Data Strobe (Group 3)** This bit enables the timing adjustment for the 4X data strobe signals: HDSTB3P#, HDSTB3N#. 0: Enable. The adjustment is based on the value specified at bits[4:3]. 1: Disable. The timing of the address strobe is determined by the duty cycle of internal clock. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the first QW, byte 7, bit[5] in the initialization ROM. Note that the ROMSIP bit is the same as that for Rx85[7] which is for Data Group 0.
6:5	RW	HwInit	**Reserved**
4:3	RW	0 ROMSIP	**Timing Adjustment Value for Data Strobe (Group 3)** These bits determine the assertion/de-assertion time of the HDSTB3P#/HDSTB3N#. These bits become valid only when bit 7 = 0. 00: Assertion time of HDSTB1P# (a in Figure 13) is increased by 35ps. 01: Assertion time of HDSTB1P# is increased by 57ps. 10: Assertion time of HDSTB1P# is decreased by 26ps. 11: Assertion time of HDSTB1P# is decreased by 51ps. Note: 1. These bits control the duty cycle of the internal clock. Thus, when assertion time of HDSTB3P# (a in Figure 13) is increased, the assertion time of HDSTB3N# (b in Figure 13) will be decreased. 2. The delay is measured at typical case, it could vary from -58% to +58%. 3. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[4:3] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx85[4:3] which are for Data Group 0.
2:0	RW	0 ROMSIP	**Output Delay for Data Strobe (Group 3)** These bits indicates the delay for the 4X data strobe: HDSTB3P# and HDSTB3N# with respect to a clock which is 1/8T delay of controller's internal main clock. This internal main clock is supposed to be aligned with the clock fed to CPU – HCLK. Please refer to "c" in Figure 13. 000: 118ps 001: 170ps 010: 222ps 011: 274ps 100: 326ps 101: 378ps 110: 430ps 111: 482ps Note: 1. The delay is measured at typical case, it could vary from -27% to +37%. 2. These bits will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits at the ROMSIP sequence are at the first QW, byte 7, bits[2:0] in the initialization ROM. Note that the ROMSIP bits are the same as that for Rx85[2:0] which are for Data Group 0.

Offset Address: 8C-8Fh (D0F2) – Reserved

DRAM Interface Control (90–91h)

Offset Address: 90h (D0F2)

DRAMC Interface Control – Read/Write Cycle **Default Value: 48h**

Bit	Attribute	Default	Description
7	RW	0	**Condition to Resume DCLK for CPU to DRAM Request** When D0F4 RxA2[6] is set to 1, DCLK which is the DRAM controller's main clock can be stopped when there is no active cycle. This bit determines which active pins at CPU side to resume the DCLK for a CPU to DRAM request. 0: Use BREQ0 to resume the DCLK. 1: Use ADS to resume the DCLK. Noted that when D0F4 RxA2[6] is set to 0, setting this bit to either 0 or 1 does not have any effect. The DCLK is always running freely in that case.
6	RW	1b	**CPU-to-DRAM Read Cycle Reorder Control** This bit controls the reordering of the read requests. i.e. When enabled, the controller will have to deal with the reordering for those read cycles that could be out of order returned from the DRAM controller. Note that the CPU always has to get the data in its requested order. 0: Disable. The controller will treat the data returned from DRAM controller as all in-ordered. Thus, the data will need to be in-ordered. This can be done by programming the registers in DRAM controller – D0F3: Rx6A[7:4] = 0h and Rx6D = 1b. If those registers are not programmed right, the system won't be able to work. 1: Enable. The controller always treats those data from DRAM controller as out-of-order and a corresponding reordering mechanism will be applied to those data before they are sent to CPU.
5:4	RW	0	**Reserved**
3	RO	1b	**Reserved** This bit must always be set to 1.
2	RW	0	**Reserved**
1:0	RW	0	**CPU Bus Controller to DRAM Read Cycle Control – 3** This bit provides the fast timing for DRDY. DRDY is an internal signal for CPU-to-DRAM read cycle control. 00: 2T faster 01: 3T faster 10: 4T faster 11: 5T faster Note: These bits work with Rx54[3], Rx55[1] for different CPU-to-DRAM read cycle timing.

Offset Address: 91h (D0F2) – Reserved

Power Management Related Control (92-95h)

Offset Address: 92h (D0F2)

PMU Control - ACPI IO Base Address – 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**ACPI IO Base Address – 2** These bits define the IO base address [15:8] for ACPI (Advanced Configuration and Power Interface). They work with Rx93[7:5] to form the IO base address[15:0] = {Rx92[7:0], Rx93[7:5], 1b, ----b}. i.e. set Rx92[7:0] = xyh, {Rx93[7:5],1} = zh. And the controller will respond the following IOR read cycles with: IOR with address {xyz0h ~ xyz3h} : this chip will do nothing. IOR with address {xyz4h or xyzCh} : an IOR command to ACPI defined register P_LVL2 is decoded, this chip's C-state state machine will go to C2 state. IOR with address {xyz5h or xyzDh} : an IOR command to ACPI defined register P_LVL3 is decoded, this chip's C-state state machine will go to C3 state. IOR with address {xyz6h or xyzEh} : an IOR command to ACPI defined register P_LVL3 is decoded, this chip's C-state state machine will go to C4 state. IOR with address {xyz7h or xyzFh} : an IOR command to ACPI defined register P_LVL3 is decoded, this chip's C-state state machine will go to C5 state [Note 1]. IOR with address {xyz8h ~ xyzBh} : this chip will do nothing. Note: When the chip detects the command to go to C5 (with Rx9F[6] set to 1), the chip will be able to direct upstream cycles directly to DRAM without snooping CPU bus. However, this re-direction only works when the registers Rx98[0] and D0F4, Rx8F[2] are both set to 1.

Offset Address: 93h (D0F2)

PMU Control - ACPI IO Base Address - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**ACPI IO Base Address – 1** These bits define the IO base address [7:5] for ACPI (Advanced Configuration and Power Interface). They work with Rx92[7:0] to form the IO base address[15:0] = {Rx92[7:0], Rx93[7:5], 1b, ----b}. The chip decode the IOR with the IO base address and go to corresponding C states. Please refer to the descriptions of Rx92[7:0].
4:0	RW	0	**Reserved**

Offset Address: 94-95h (D0F2) – Reserved

CPU Bus Interface Control (96-9Fh)

Offset Address: 96h (D0F2)

CPU Interface Control – V4 Bus Protocol **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**V4 Bus Fast TRDY** VIA's C7/CN series CPUs have a fast TRDY feature which has higher throughput for CPU downstream write cycles. This enhanced protocol basically allows this chip to assert HTRDY# at a faster rate. Besides this register bit, Rx57[0] must also be set to let the feature work. Please refer to Table 10 for details. 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	0	**HDPWR# Assertion Enable** HDPWR# is connected to VIA's C7/CN series CPU. When it is asserted, the chip tells the CPU to provide power to the HD bus. When it is de-asserted, the CPU can shut down the power of the HD bus. 0: HDPWR# is always asserted by this chip. 1: HDPWR# is dynamically asserted by this chip. With this feature, VIA's C7/CN series CPU can dynamically shut off the power of HD I/O when there is no data transfer. It gives better CPU power saving.
0	RW	0	**HDPWR# Assertion Policy** This bit works only when bit 1 is 1. 0: The chip asserts HDPWR# at the data phase for a.) CPU downstream read cycles b.) Upstream APIC write cycles and c.) CPU downstream write cycles (including snoop write back data phase of upstream DRAM read and write cycles). 1: The chip asserts HDPWR# at the data phase for a.) CPU downstream read cycles and b.) Upstream APIC write cycles This one gives more power saving.

Offset Address: 97h (D0F2)

APIC Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Redirect Lowest Priority MSI Requests to APIC with Physical ID = 00h** For supporting the IPI cycle (Inter-Processor Interrupt), the chip is able to redirect the coming in MSI cycle to the CPU with least task priority. Please refer to Rx59[0] for the enabling of this IPI cycle support. This register is used to redirect the IPI cycle to the CPU with APIC physical ID = 00h (CPU0 is treated as the lowest priority processor). 0: Disable. No redirection is done, the content of the MSI cycle will not be altered, the chip will put it on to the CPU bus as it was. 1: Enable. The content of the MSI cycle could be altered. i.e. the redirected cycle would have format as: address= 'hFEE0_000y, data= 'h0000_zwvv.

Offset Address: 98h (D0F2)

CPU Interface Control - V4 Protocol **Default Value: 0nh**

Bit	Attribute	Default	Description
7	RW	0	**Retry Response 2T Delay** Giving HADS# asserted at the end of the T1, this chip should assert HDEFER# at the end of T3 to let CPU know (sampled at the end of T4) if the chip is going to do defer or retry for cycles not targeted to DRAM. This bit gives the option to delay the assertion of HDEFER# for 2T. 0: Disable. This chip always asserts the HDEFER# at the end of T3 if the cycle is going to be retried. 1: Enable. When the defer/retry queue is empty, upon seeing the cycle needed to be retried, this chip asserts the HDEFER# at the end of T3. When the defer/retry queue is not empty, i.e. there is at least one previous request queued, upon seeing the cycle needed to be retried, this chip asserts both HHITM# and HHIT# at the end of T3 to stall the CPU bus and asserts HDEFER# later at the end of T5. Note: This register option is to ease the timing for decoding of the incoming request against the request queued in the retry queue. It is suggested to set this bit to 1 when HCLK (CPU bus clock) is >= 333Mhz.
6	RW	0	**Flushing DRAM Write Requests for CPU to Internal GFX Cycles** When cycles of CPU accessing GFXCTL (internal graphic controller) come, these bits provide the strategy of how the CPU bus controller handles the write requests queued in the CPU to Memory write FIFO. This bit will co-work with Rx98[5]. 0x: Disable. No flushing action is taken. 10: Either read or write cycles of CPU to GFXCTL will flush the CPU-to-Memory write FIFO. 11: Only Write cycle of CPU to GFXCTL will flush the CPU-to-Memory write FIFO.
5	RW	0	**Flushing DRAM Write Requests for CPU to Internal GFX Cycles** When cycles of CPU accessing GFXCTL (internal graphic controller) come, these bits provide the strategy of how the CPU bus controller handles the write requests queued in the CPU to Memory write FIFO. This bit will co-work with Rx98[6]. 0x: Disable. No flushing action is taken. 10: Either read or write cycles of CPU to GFXCTL will flush the CPU-to-Memory write FIFO. 11: Only Write cycle of CPU to GFXCTL will flush the CPU-to-Memory write FIFO.
4	RW	0	**Acceptance of Cycles When Retry Queue Is Not Empty** Although there is register to control the entry size of defer/retry queue at Rx51[3], this bit is to control if the controller takes more downstream read cycles targeted to non-DRAM agents when there is another downstream retry read cycle ongoing inside the retry queue. 0: Enable. This chip can take another downstream read cycle targeted to non-DRAM agent while there is a retry cycle ongoing inside the chip. 1: Disable. This chip cannot take another downstream read cycle targeted to non-DRAM agent when there is already a retry cycle ongoing inside the chip, even entry size of defer/retry Rx51[3] is set to 1b for 2 entries.
3	RW	1b	**BPRI Assertion condition for Redirected Upstream Cycles** When D0F4 Rx8F[3] is set as 1, NB exits C5 state by STPCLK de-assertion. During C5 status transition, if CPU issues request during master request re-direction, it might mess up V4IF internal IOQ and cause system hang-up. This register is used to assert BPRI in this scenario for CPU issuing request prevention. 0: The chip asserts BPRI upstream cycles are forwarding to DRAMC after STPCLK de-assertion. 1: The chip won't assert BPRI when upstream cycles are forwarding to DRAMC
2	RW	1b	**Reserved**
1	RW	1b ROMSIP	**Dynamic FSB Protocol Support** This bit is enabled to support the Dynamic FSB protocol. For system with VIA's CN series CPU, this bit should be always set at 1. 0: Disable 1: Enable Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the second QW, byte 7, bit[4] in the initialization ROM.
0	RW	0	**Redirection of Upstream Cycles During C5 State** This register is used to redirect the upstream cycles directly to DRAM controller to access DRAM without snoop the CPU during C5 state. Please refer to Rx92 for more information. 0: Disable. The chip will always forward upstream cycles to CPU bus to do snoop even the system is in C5 state. 1: Enable. The chip will forward upstream cycles to DRAM controller without snooping the CPU when the system is in C5 state.

Offset Address: 99-9Dh (D0F2) – Reserved

Offset Address: 9Eh (D0F2)

Chip Internal Operation Control – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	0	**Turning Off Dynamic Fast TRDY When Less Requests is Pending** Dynamic Fast TRDY features are listed in register Rx57[0] and Table 10. This register is to enhance the function of Dynamic Fast TRDY. 0: Dynamic Fast TRDY features are always on. 1: Dynamic Fast TRDY features will be turned off when there is only one or none request queued in the internal downstream queue.
6	RW	0	**Extending CPU Bus Occupied Time for Master Cycles** When the Master Occupancy Timer (Rx53[3:0]) is expired, the chip should give the ownership of the V4 bus back to the CPU(s) by de-asserting the HBPRI# pin. This register is to extend the ownership of V4 bus for upstream master cycles if the next upstream requests had the address to be within the same cache-line as the last upstream cycle's. It helps to improve performance for consecutive upstream 2/4 QW requests. 0: Disable 1: Enable
5	RW	0	**Retry Address Comparison Control for Internal GFX Cycles** When "Tile Mode Address Windows" is not supported (Rx9E[1]=0), setting this bit to 0 provides better timing margin for retried cycles to be directed to internal GFX. When "Tile Mode Address Windows" is supported (Rx9E[1]=1), this bit must be set to 0. 0: The address source to be compared against those in the retry queue is those after DFA addressing conversion. 1: The address source to be compared against those in the retry queue is those coming directly from CPU bus. Note: This bit only needs to be set to 1 when "Tile Mode Address Windows" is not supported and the frequency of this CPU bus controller is at or over 333Mhz.
4	RW	0 ROMSIP	**Turning Off Pull-up Driving During Auto De-skew Process** When VIA's CPU and this chip work together in the GTL trace compensation mode, since CPU will toggle all the source-synchronous signals, this register is to turn off pull-up driving for the signals in inactive sub-groups during the auto de-skew process. The main purpose of doing that (turning off some pull-up driving) is to prevent power bounce resulted by simultaneous switching on large number of signals. 0: During auto de-skew process, the pull-up driving of those active I/O are turned on and those inactive I/O are turned off. 1: During auto de-skew process, all the pull-up driving of the I/O of this chip are turned on. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the second QW, byte 0, bit[3] in the initialization ROM.
3	RW	1b ROMSIP	**1T Delay for Receiving Data on the CPU Bus** This bit is to add 1T delay for the data (HD[63:0]) receiving path from the circuit macro on the chip boundary to the internal data buffer. The related bus control logic is also changed accordingly. 0: Disable. The data to the internal data buffer comes directly from the circuit macro on the chip boundary. 1: Enable. 1T delay is added to the internal data receiving path in between the internal data buffer and the circuit macro on the chip boundary. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the second QW, byte 0, bit[2] in the initialization ROM.
2	RW	1b ROMSIP	**1T Delay for Transmitting Data on the CPU Bus** This bit is to add 1T delay for the data (HD[63:0]) transmitting path from the internal data buffer to the circuit macro on the chip boundary. The related bus control logic is also changed accordingly. 0: Disable. The data to the circuit macro on the chip boundary comes directly from the internal data buffer. 1: Enable. 1T delay is added to the internal data transmitting path in between the circuit macro on the chip boundary and the internal data buffer. Note: This bit will be programmed during ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit at the ROMSIP sequence is at the second QW, byte 0, bit[1] in the initialization ROM.
1	RW	0	**Tile Mode Address Windows Support** This is the enabling bit for supporting "Tile Mode Address Windows". Under DFA (Direct Frame Buffer Access) mode, DFA address range can be divided into several (16) windows. Each window has an "Tile mode accessible" attribute associated with it. The controller directs the cycles with address falling into windows having "Tile mode accessible" attribute being set to internal GFX controller (GFXCTL) and those not being set to DRAM. 0: Disable. All frame buffer access using DFA address will be sent to DRAM. 1: Enable. Frame buffer access using DFA address will be directed to either DRAM or GFXCTL depending on the "tile mode accessible" attribute associated with each address window.
0	RW	0	**Reserved**

Offset Address: 9Fh (D0F2)

DRAMC Interface Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Requests to DRAM Controller** This bit is to let the CPU bus controller to issue controller's request status to get the ownership of DRAM controller earlier. 0: Disable. This CPU bus controller asserts request to DRAM controller only when the request is already in the queue. 1: Enable. The CPU bus controller asserts request to DRAM controller whenever the it predicts there is requests going to be sent to DRAM controller. This option helps to arbitrate the ownership of DRAM controller a few cycles earlier.
6	RW	1b	**C5 Command Decoding** CPU issues IOR command with specific address assigned to let the C-state state machine which works for the CPU power management to go to C5 state. This bit enables the logic for the C5 command decoding, please refer to Rx92 and Rx93 for more information. 0: Disable. Controller will not respond the C5 command, i.e. the CPU bus controller just returns a dummy data for the corresponding IOR cycle. 1: Enable. The controller responds the C5 command with the handling of forwarding later upstream cycles to DRAM controller directly, without going to CPU bus to snoop when Rx98[0] is set to 1.
5:0	RW	0	**Reserved**

AGTL Physical Control (A0–A2h)

Offset Address: A0h (D0F2)

Slew Rate Control of AGTL+ I/O **Default Value: 0nh**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0 ROMSIP	**Slew Rate Control of the AGTL+ I/O Pad** These bits control the slew rate of the rising and falling for all the AGTL+ I/O (Address, Data and 1X signals; please refer to note *1, *2 and *3 below the register descriptions of RxA2) when the signals are in output mode. These registers affect both the rising and falling of the signals. This will co-work with RxA0[0]. **RxA0[1:0]** / **Rising** / **Falling** 00 / 9.01 mv/ps / 15.23 mv/ps 01 / 9.11 mv/ps / 15.41 mv/ps 10 / 9.01 mv/ps / 15.22 mv/ps 11 / 9.11 mv/ps / 15.41 mv/ps Note: 1. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at second QW, byte 1, bits [1:0] in the initialization ROM. 2. The number given by mv/ps above are at typical case, a -13% ~ +21% variation for the rising and a -19% ~ +9% variation for the falling will need to be applied in the real system.
0	RW	0 ROMSIP	**Slew Rate Control of the AGTL+ I/O Pad** These bits control the slew rate of the rising and falling for all the AGTL+ I/O (Address, Data and 1X signals; please refer to note *1, *2 and *3 below the register descriptions of RxA2) when the signals are in output mode. These registers affect both the rising and falling of the signals. This will co-work with RxA0[1]. **RxA0[1:0]** / **Rising** / **Falling** 00 / 9.01 mv/ps / 15.23 mv/ps 01 / 9.11 mv/ps / 15.41 mv/ps 10 / 9.01 mv/ps / 15.22 mv/ps 11 / 9.11 mv/ps / 15.41 mv/ps Note: 1. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at second QW, byte 1, bits [1:0] in the initialization ROM. 2. The number given by mv/ps above are at typical case, a -13% ~ +21% variation for the rising and a -19% ~ +9% variation for the falling will need to be applied in the real system.

Offset Address: A1h (D0F2)

CPU Bus AGTL+ 1X Signals Pull Down/Up Driving **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	1000b ROMSIP	**Pull-Down Resistance for AGTL+ 1X Signals** These bits are pull-down resistance setting for the driving of AGTL+ 1X signals: CPURST#, HDPWR#, HLOCK#, HRS[2:0]#, HDRDY#, HBNR#, HHITM#, HHIT#, HADS#, HBPRI#, HDBSY#, HDEFER#, HTRDY#, HALF#, HBREQ0#. Please refer to Figure 10 for the driving setting structure. The operation of these bits is as those described in Rx71[7:4]. When in manual mode (Rx7A[7] =0), these registers define the same pull-down resistance value for signals mentioned above as those presented in the Rx71[7:4]. When in auto compensation mode(Rx7A[7] =1), these registers also act as an offset to be added to the NMOS compensate value in RxA2[7:4] as shown in Rx71[7:4]. The only difference is the ROMSIP location, they are at the second QW, byte 2, bits[7:4] in the initialization ROM.
3:0	RW	1000b ROMSIP	**Pull Up Resistance for AGTL+ 1X Signals** These bits are pull-up resistance setting for the driving of AGTL+ 1X signals: CPURST#, HDPWR#, HLOCK#, HRS[2:0]#, HDRDY#, HBNR#, HHITM#, HHIT#, HADS#, HBPRI#, HDBSY#, HDEFER#, HTRDY#, HALF#, HBREQ0#. Please refer to Figure 10 for the driving setting structure. The operation of these bits is as those described in Rx70[7:4]. When in manual mode (Rx7A[7] =0), these registers defined the same pull-up resistance value for signals mentioned above as those presented in the Rx70[7:4]. When in auto compensation mode(Rx7A[7] =1), these registers also act as an offset to be added to the PMOS compensate value in RxA2[3:0] as shown in Rx70[7:4]. The only difference is the ROMSIP location, they are at the second QW, byte 2, bits[3:0] in the initialization ROM.

Offset Address: A2h (D0F2)

Auto Compensation Value for the Driving of AGTL+ I/O **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**AGTL+ Auto Compensation Result for Pull Down (NMOS) Driving** These four bits are the NMOS compensate results*4 from the auto compensation circuitry for address signals*1, data signals*2 and other 1X AGTL+ signals*3. They are used to set the pull-down driving for AGTL+ I/O when auto compensation mode is enabled (Rx7A[7]=1). Please refer to Figure 10 for the driving setting structure. Please also refer to the register descriptions of Rx70~Rx73 and RxA1.
3:0	RO	0	**AGTL+ Auto Compensation Results for Pull Up (PMOS) Driving** These four bits are the PMOS compensate results*4 from the auto compensation circuitry for address signals*1, data signals*2 and other 1X AGTL+ signals*3. They are used to set the pull-up driving for AGTL+ I/O when auto compensation mode is enabled (Rx7A[7]=1). Please refer to Figure 10 for the driving setting structure. Please also refer to the register descriptions of Rx70~Rx73 and RxA1.

Note:

*1: Address signals: HADSTB0N#, HADSTB0#, HADSTB1#, HA[32:3]# and HREQ[2:0]#.

*2: Data signals: HDSTB[3:0]vcc#, HDSTB[3:0]P#, HD[63:0]# and HDBI[3:0]#.

*3: 1X AGTL+ Signals: CPURST#, HDPWR#, HLOCK#, HRS[2:0]#, HDRDY#, HBNR#, HHITM#, HHIT#, HADS#, HBPRI#, HDBSY#, HDEFER#, HTRDY#, HALF# and HBREQ0#.

*4: Note the value are updated when the power is first applied or when the chip is resumed from power-down state, please refer to RXBE[4] for more information.

Output and Input Timing Adjustment for AGTL+ I/O Trace Delay (A3-FFh)

AGTL+ I/O 4X Signals Timing Delay Adjustment

For high speed signals, either data or strobe which runs at 4X speed on the V4 bus, to be sensed correctly, Fine-tuning is required on the transmitting and receiving paths. Not only Rx7E and Rx7F are adjusted to tune the duty cycle and delay for odd/even beat time, but also there is extra delay in the macro circuit (GTLPHY) besides the I/O buffers. Auto De-skew process is a process this chip will do after the de-assertion of CPURST# to detect the possible trace delay difference. The delay adjustment registers beginning from RxA3 are control bits for those delay adjustment for different signal groups. Figure 14 is an example using HREQ1# and HADSTB0P/vcc# to illustrate this auto de-skew delay adjustment structure.

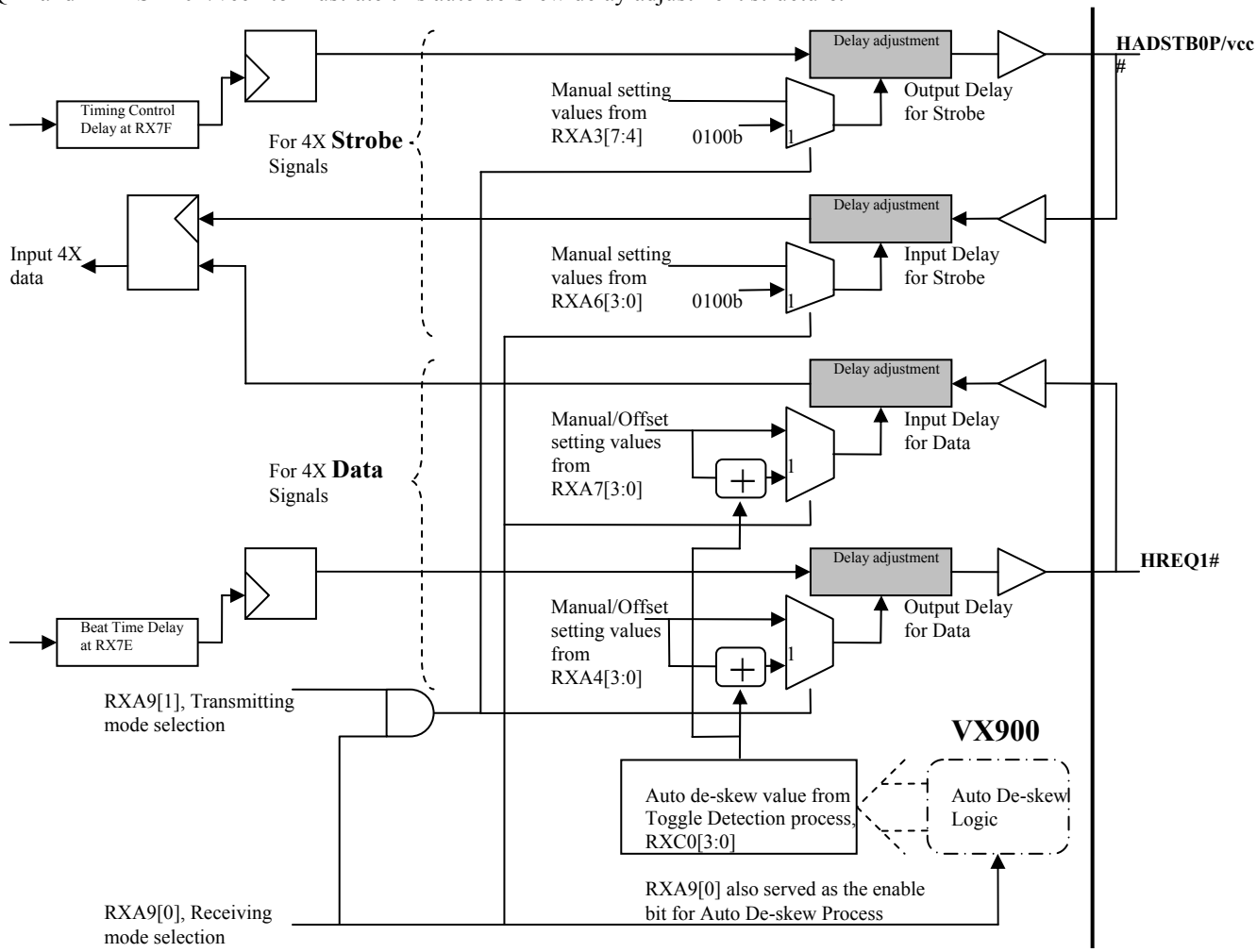


Figure 14. Structure of Output and Input Delay Adjustment for Strobe and HA/HD Signals

Offset Address: A3h (D0F2)

Output Delay Adjustment for HA Strobe **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Output Delay Setting for HA Strobe** These bits set extra delay for the HADSTB0P/vcc# before they toggled on the V4 bus. Please refer to Figure 14 for the delay adjustment structure. ***When in Manual mode (RxA9[1:0]=-0b) or RX Auto De-skew mode(RxA9[1:0]=01b)***, the corresponding output delay for those strobe signals are: 0000: 153ps 0001: 182ps 0010: 211ps 0011: 240ps 0100: 269ps 0101: 298ps 0110: 327ps 0111: 356ps 1000: 385ps 1001: 414ps 1010: 443ps 1011: 472ps 1100: 501ps 1101: 530ps 1110: 559ps 1111: 588ps ***When in Auto De-skew mode (RxA9[1:0]=11b),*** the output delays are: xxxx: 269ps. The output delay setting of HADSTB0P/vcc# will be fixed to 0100b which allow the output delay = 269ps at typical case. Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 4, bits[3:0] in the initialization ROM.
3:1	RW	0	**Reserved**
0	RW	0 ROMSIP	**Reserved**

Offset Address: A4h (D0F2)

Output Delay Adjustment for HA Group - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HA Group – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#1 of HA signals: HABI#, HA13#, HA5#, HA4# and HA7#. Please refer to register descriptions at RxA4[3:0]. The bit description is similar to RxA4[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC0[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HA Group – Subgroup#0** Refer to Figure 14, these bits are output delay adjustment for subgroup#0 of HA signals: HREQ0#, HREQ1#, HA3#, HA6# and HREQ2#. ***When in Manual mode (RxA9[1:0]= -0b) or RX Auto De-skew mode (RxA9[1:0]=01b):*** The delay adjustment to the output paths of the signals mentioned above are: 0000: 153ps 0001: 182ps 0010: 211ps 0011: 240ps 0100: 269ps 0101: 298ps 0110: 327ps 0111: 356ps 1000: 385ps 1001: 414ps 1010: 443ps 1011: 472ps 1100: 501ps 1101: 530ps 1110: 559ps 1111: 588ps Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte3, bit[3:0] in the initialization ROM. ***When in Auto De-skew mode (RxA9[1:0] =11b):*** These bits are actually the offset value to be added to the results of Auto De-skew process at RxC0[3:0]. The delay adjustment setting to the delay paths is actually listed as: 0000: Delay setting = RXC0[3:0] 1000: Delay setting = RXC0[3:0] – 8 0001: Delay setting = RXC0[3:0] + 1 1001: Delay setting = RXC0[3:0] – 7 0010: Delay setting = RXC0[3:0] + 2 1010: Delay setting = RXC0[3:0] – 6 0011: Delay setting = RXC0[3:0] + 3 1011: Delay setting = RXC0[3:0] – 5 0100: Delay setting = RXC0[3:0] + 4 1100: Delay setting = RXC0[3:0] – 4 0101: Delay setting = RXC0[3:0] + 5 1101: Delay setting = RXC0[3:0] – 3 0110: Delay setting = RXC0[3:0] + 6 1110: Delay setting = RXC0[3:0] – 2 0111: Delay setting = RXC0[3:0] + 7 1111: Delay setting = RXC0[3:0] – 1 Note: 1. The effective delay values to the transmitting paths are provided on the description for the manual mode above. 2. If the calculation above is greater than 1111b, the final delay setting would be at 1111b. If it is less than 0000b, the final delay setting would be 0000b.

Offset Address: A5h (D0F2)

Output Delay Adjustment for HA Group - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HA Group – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#3 of HA signals: HA10#, HA8#, HA14#, HA16# and HA12#. Please refer to register descriptions at RxA4[3:0]. The bit description is similar to RxA4[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC1[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HA Group – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#2 of HA signals: HA9#, HA11#, HA15#, HAHI1# and HAHI0#. Please refer to register descriptions at RxA4[3:0]. The bit description is similar to RxA4[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC1[3:0]**.

Offset Address: A6h (D0F2)

Input Delay Adjustment for HA Strobe **Default Value: 0nh**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0111b ROMSIP	**Manual Input Delay Setting for HA Strobe** These bits set internal input delay for strobe signals – HADSTB0P/vcc# which are used to latch the signals in HA group after they coming in through chip's pad. Please refer to Figure 14 for the delay adjustment structure. ***When in Manual mode (RxA9[1:0]=-0b):*** The corresponding input delay for those strobe signals are: 0000: 153ps 0001: 182ps 0010: 211ps 0011: 240ps 0100: 269ps 0101: 298ps 0110: 327ps 0111: 356ps 1000: 385ps 1001: 414ps 1010: 443ps 1011: 472ps 1100: 501ps 1101: 530ps 1110: 559ps 1111: 588ps ***When in RX Auto De-skew mode (RxA9[1:0]=01b) or Auto De-skew mode (RxA9[1:0]=11b),*** the input delays are: xxxx: 269ps. The input delay setting of HADSTB0P/vcc# will be fixed to 0100b which allow the input delay = 269ps at typical case. Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 4, bits[7:4] in the initialization ROM.

Offset Address: A7h (D0F2)

Input Delay Adjustment for HA Group - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HA Group – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#1 of HA signals: HABI#, HA13#, HA5#, HA4# and HA7#. Please refer to register descriptions at RxA7[3:0]. The bit description is similar to RxA7[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC0[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HA Group – Subgroup#0** Refer to Figure 14, these bits are input delay adjustment for subgroup#0 of HA signals: HREQ0#, HREQ1#, HA3#, HA6# and HREQ2#. ***When in Manual mode (RxA9[1:0]=-0b:*** The delay adjustments to the input path of the signals mentioned above are: 0000: 153ps 0001: 182ps 0010: 211ps 0011: 240ps 0100: 269ps 0101: 298ps 0110: 327ps 0111: 356ps 1000: 385ps 1001: 414ps 1010: 443ps 1011: 472ps 1100: 501ps 1101: 530ps 1110: 559ps 1111: 588ps Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 3, bits[7:4] in the initialization ROM. ***When in RX Auto De-skew mode (RxA9[1:0]=01b) or Auto De-skew mode (RxA9[1:0]=11b):*** These bits are actually the offset value to be added to the results of Auto De-skew process at RxC0[3:0]. The delay adjustment setting to the delay paths is actually listed as: 0000: Delay setting = RXC0[3:0] 1000: Delay setting = RXC0[3:0] – 8 0001: Delay setting = RXC0[3:0] + 1 1001: Delay setting = RXC0[3:0] – 7 0010: Delay setting = RXC0[3:0] + 2 1010: Delay setting = RXC0[3:0] – 6 0011: Delay setting = RXC0[3:0] + 3 1011: Delay setting = RXC0[3:0] – 5 0100: Delay setting = RXC0[3:0] + 4 1100: Delay setting = RXC0[3:0] – 4 0101: Delay setting = RXC0[3:0] + 5 1101: Delay setting = RXC0[3:0] – 3 0110: Delay setting = RXC0[3:0] + 6 1110: Delay setting = RXC0[3:0] – 2 0111: Delay setting = RXC0[3:0] + 7 1111: Delay setting = RXC0[3:0] – 1 Note: 1. The effective delay values to the receiving paths are provided on the description for the manual mode above. 2. If the calculation above is greater than 1111b, the final delay setting would be at 1111b. If it is less than 0000b, the final delay setting would be 0000b.

Offset Address: A8h (D0F2)

Input Delay Adjustment for HA Group - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HA Group – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#3 of HA signals: HA10#, HA8#, HA14#, HA16# and HA12#. Please refer to register descriptions at RxA7[3:0]. The bit description is similar to RxA7[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC1[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HA Group – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#2 of HA signals: HA9#, HA11#, HA15#, HAHI1# and HAHI0#. Please refer to register descriptions at RxA7[3:0]. The bit description is similar to RxA7[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC1[3:0].**

Offset Address: A9h (D0F2)

Auto De-skew Control **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0 ROMSIP	**AGTL+ I/O Loopback** This bit is the loop back control in the circuit macro – GTLPHY for all the signals at AGTL+ I/O. When this bit is enabled, the signals transmitted to the output buffer will be redirected to the input buffer of the I/O pads. It should be set to 0 for normal operation. The only situation that this bit can be set to 1 is for the speed mode testing. Special vectors need to be applied to the chip to achieve a complete speed mode test. 0: Disable 1: Enable Note: These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 7, bit[0] in the initialization ROM.
3:2	RW	01b ROMSIP	**Threshold Setting for Signal Detection at Auto De-skew Process** These bits define the times the high/low status of the signals being detected to be stable at the Auto De-skew process. i.e. when Auto De-skew process is on going, the controller detects the signal coming in from CPU as low/high for this programmed number of times before it delays the signal for another step to continue the process. 00: 3 times 01: 4 times 10: 5 times 11: 6 times Note: These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 0, bits[7:6] in the initialization ROM.
1	RW	1b ROMSIP	**Mode Selections for Output/Input Delay of HA & HD Signals** These bits determine the way the adjustment applied on the delay paths for Output and Input of HA and HD Signals on the V4 bus. For clearer illustration, please refer to Figure 14. Please also refer to RxA3~RxA8, RxAA~RxBD for more information. This bit will co-work with RxA9[0]. x0: Manual mode. The registers at RxA3~RxA8, RxAA~RxBD will be in manual mode. i.e. the register setting would be the delay setting for the delay elements in the signal input/output paths. 01: RX Auto De-skew mode. The Auto De-skew process of this chip is enabled, the corresponding detected trace delay stored in RxC0~RxC9 would be used as the main delay for the delay elements in the signal input paths. Note that in this RX Auto De-skew mode, the delay setting in the signal output paths is in manual mode. 11: Auto De-skew mode. The Auto De-skew process of this chip is enabled, the corresponding detected trace delay stored in RxC0~RxC9 would be used as the main delay for both the delay elements in the signal input and output paths. Note: These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at second QW, byte 0, bits [5:4] in the initialization ROM.
0	RW	1b ROMSIP	**Mode Selections for Output/Input Delay of HA & HD Signals** These bits determine the way the adjustment applied on the delay paths for Output and Input of HA and HD Signals on the V4 bus. For clearer illustration, please refer to Figure 14. Please also refer to RxA3~RxA8, RxAA~RxBD for more information. This bit will co-work with RxA9[1]. x0: Manual mode. The registers at RxA3~RxA8, RxAA~RxBD will be in manual mode. i.e. the register setting would be the delay setting for the delay elements in the signal input/output paths. 01: RX Auto De-skew mode. The Auto De-skew process of this chip is enabled, the corresponding detected trace delay stored in RxC0~RxC9 would be used as the main delay for the delay elements in the signal input paths. Note that in this RX Auto De-skew mode, the delay setting in the signal output paths is in manual mode. 11: Auto De-skew mode. The Auto De-skew process of this chip is enabled, the corresponding detected trace delay stored in RxC0~RxC9 would be used as the main delay for both the delay elements in the signal input and output paths. Note: These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at second QW, byte 0, bits [5:4] in the initialization ROM.

Offset Address: AAh (D0F2)

Output Delay Adjustment for HD Strobe - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Output Delay Setting for HD Strobe – HDSTB1P/vcc#** These bits set extra delay for the HDSTB1P/vcc# before they toggled on the V4 bus. Please refer to register descriptions at RxAA[3:0]. The statement in RxAA [3:0] can all be applied here including the ROMSIP setting.
3:0	RW	0111b ROMSIP	**Manual Output Delay Setting for HD Strobe – HDSTB0P/vcc#** These bits set extra delay for the HDSTB0P/vcc# before they toggled on the V4 bus. Please refer to similar structure as shown in Figure 14. ***When in Manual mode (RxA9[1:0]=-0b) or RX Auto De-skew mode (RxA9[1:0]=01b):*** The corresponding output delay for those strobe signals are: 0000: 153ps 0001: 182ps 0010: 211ps 0011: 240ps 0100: 269ps 0101: 298ps 0110: 327ps 0111: 356ps 1000: 385ps 1001: 414ps 1010: 443ps 1011: 472ps 1100: 501ps 1101: 530ps 1110: 559ps 1111: 588ps ***When in Auto De-skew mode (RXA9[1:0]=11b),*** the output delays are: xxxx: 269ps. The output delay setting of HADSTB0P/vcc# will be fixed to 0100b which allow the output delay = 269ps at typical case. Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 5, bits[3:0] in the initialization ROM.

Offset Address: ABh (D0F2)

Output Delay Adjustment for HD Strobe - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Output Delay Setting for HD Strobe – HDSTB3P/vcc#** These bits set extra delay for the HDSTB3P/vcc# before they toggled on the V4 bus. Please refer to register descriptions at RxAA[3:0]. The statement in RxAA [3:0] can all be applied here including the ROMSIP setting.
3:0	RW	0111b ROMSIP	**Manual Output Delay Setting for HD Strobe – HDSTB2P/vcc#** These bits set extra delay for the HDSTB2P/vcc# before they toggled on the V4 bus. Please refer to register descriptions at RxAA[3:0]. The statement in RxAA[3:0] can all be applied here including the ROMSIP setting.

Offset Address: ACh (D0F2)

Output Delay Adjustment for HD Group 0 - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 0 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#1 of HD Group 0 signals: HD14#, HD11#, HD1#, HDBI0# and HD13#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC2[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 0 – Subgroup#0** Refer to Figure 14, these bits are output delay adjustment for subgroup#0 of HD Group 0 signals: HD12#, HD5#, HD15# and HD10#. ***When in Manual mode (RxA9[1:0]= -0b) or RX Auto De-skew mode (RxA9[1:0]=01b):*** The delay adjustment to the output paths of the signals mentioned above are: 0000: 153ps 0001: 182ps 0010: 211ps 0011: 240ps 0100: 269ps 0101: 298ps 0110: 327ps 0111: 356ps 1000: 385ps 1001: 414ps 1010: 443ps 1011: 472ps 1100: 501ps 1101: 530ps 1110: 559ps 1111: 588ps Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 6, bits[3:0] in the initialization ROM. ***When in Auto De-skew mode (RxA9[1:0] =11b):*** These bits are actually the offset value to be added to the results of Auto De-skew process at RxC2[3:0]. The delay adjustment setting to the delay paths is actually listed as: 0000: Delay setting = RXC2[3:0] 0001: Delay setting = RXC2[3:0] + 1 0010: Delay setting = RXC2[3:0] + 2 0011: Delay setting = RXC2[3:0] + 3 0100: Delay setting = RXC2[3:0] + 4 0101: Delay setting = RXC2[3:0] + 5 0110: Delay setting = RXC2[3:0] + 6 0111: Delay setting = RXC2[3:0] + 7 1000: Delay setting = RXC2[3:0] – 8 1001: Delay setting = RXC2[3:0] – 7 1010: Delay setting = RXC2[3:0] – 6 1011: Delay setting = RXC2[3:0] – 5 1100: Delay setting = RXC2[3:0] – 4 1101: Delay setting = RXC2[3:0] – 3 1110: Delay setting = RXC2[3:0] – 2 1111: Delay setting = RXC2[3:0] – 1

Offset Address: ADh (D0F2)

Output Delay Adjustment for HD Group 0 - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 0 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#3 of HD Group 0 signals: HD4#, HD6#, HD3# and HD8#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC3[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 0 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#2 of HD Group 0 signals: HD0#, HD9#, HD2# and HD7#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC3[3:0]**.

Offset Address: AEh (D0F2)

Output Delay Adjustment for HD Group 1 - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 1 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#1 of HD Group 1 signals: HD31#, HD18#, HD24#, HD26# and HDBI1#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC4[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 1 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#0 of HD Group 1 signals: HD28#, HD19#, HD27# and HD30#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC4[3:0]**.

Offset Address: AFh (D0F2)

Output Delay Adjustment for HD Group 1 - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 1 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#3 of HD Group 1 signals: HD23#, HD20#, HD22# and HD21#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC5[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 1 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#2 of HD Group 1 signals: HD25#, HD29#, HD17# and HD16#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC5[3:0]**.

Offset Address: B0h (D0F2)

Output Delay Adjustment for HD Group 2 - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 2 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#1 of HD Group 2 signals: HD33#, HD43#, HD47#, HDBI2# and HD39#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC6[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 2 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#0 of HD Group 2 signals: HD32#, HD42#, HD36# and HD41#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC6[3:0]**.

Offset Address: B1h (D0F2)

Output Delay Adjustment for HD Group 2 - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 2 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#3 of HD Group 2 signals: HD38#, HD35#, HD40# and HD45#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC7[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 2 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#2 of HD Group 2 signals: HD34#, HD44#, HD37# and HD46#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC7[3:0]**.

Offset Address: B2h (D0F2)

Output Delay Adjustment for HD Group 3 - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 3 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#1 of HD Group 3 signals: HD62#, HD51#, HD59#, HD58# and HDBI3#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC8[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 3 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#0 of HD Group 3 signals: HD61#, HD52#, HD56# and HD60#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC8[3:0]**.

Offset Address: B3h (D0F2)

Output Delay Adjustment for HD Group 3 - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 3 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#3 of HD Group 3 signals: HD50#, HD57#, HD63# and HD55#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC9[7:4]**.
3:0	RW	0111b ROMSIP	**Output Delay Adjustment for HD Group 3 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are output delay adjustment for subgroup#2 of HD Group 3 signals: HD49#, HD54#, HD53# and HD48#. Please refer to register descriptions at RxAC[3:0]. The bit description is similar to RxAC[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC9[3:0]**.

Offset Address: B4h (D0F2)

Input Delay Adjustment for HD Strobe - 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Input Delay Setting for HD Strobe – HDSTB1P/vcc#** These bits set internal input delay for strobe signals – HDSTB1P/vcc# which are used to latch the signals in HD group 1 after they coming in through chip's pad. Please refer to register descriptions at RxB4[3:0]. The statement in RxB4[3:0] can all be applied here including the ROMSIP setting.
3:0	RW	0111b ROMSIP	**Manual Input Delay Setting for HD Strobe – HDSTB0P/vcc#** These bits set internal input delay for strobe signals – HDSTB0P/vcc# which are used to latch the signals in HD group 0 after they coming in through chip's pad. Please refer to similar structure as shown in Figure 14. ***When in Manual mode (RxA9[1:0]=-0b),*** the corresponding input delay for those strobe signals are: 0000: 153ps. 0001: 182ps. 0010: 211ps. 0011: 240ps. 0100: 269ps. 0101: 298ps. 0110: 327ps. 0111: 356ps. 1000: 385ps. 1001: 414ps. 1010: 443ps. 1011: 472ps. 1100: 501ps. 1101: 530ps. 1110: 559ps. 1111: 588ps. ***When in RX Auto De-skew mode (RxA9[1:0]=01b) or Auto De-skew mode (RxA9[1:0]=11b),*** the input delays are: xxxx: 269ps. The input delay setting of HDSTB0P/vcc# will be fixed to 0100b which allow the input delay = 269ps at typical case. Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 5, bits[7:4] in the initialization ROM.

Offset Address: B5h (D0F2)

Input Delay Adjustment for HD Strobe - 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Manual Input Delay Setting for HD Strobe – HDSTB3P/vcc#** These bits set internal input delay for strobe signals – HDSTB3P/vcc# which are used to latch the signals in HD group 3 after they coming in through chip's pad. Please refer to register descriptions at RxB4[3:0]. The statement in RxB4[3:0] can all be applied here including the ROMSIP setting.
3:0	RW	0111b ROMSIP	**Manual Input Delay Setting for HD Strobe – HDSTB2P/vcc#** These bits set internal input delay for strobe signals – HDSTB2P/vcc# which are used to latch the signals in HD group 2 after they coming in through chip's pad. Please refer to register descriptions at RxB4[3:0]. The statement in RxB4[3:0] can all be applied here including the ROMSIP setting.

Offset Address: B6h (D0F2)

Input Delay Adjustment for HD Group 0 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 0 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#1 of HD Group 0 signals: HD14#, HD11#, HD1#, HDBI0# and HD13#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC2[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 0 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#0 of HD Group 0 signals: HD12#, HD5#, HD15# and HD10#. ***When in Manual mode (RxA9[1:0]=-0b:*** The delay adjustments to the input path of the signals mentioned above are: 0000: 153ps. 0001: 182ps. 0010: 211ps. 0011: 240ps. 0100: 269ps. 0101: 298ps 0110: 327ps. 0111: 356ps. 1000: 385ps. 1001: 414ps. 1010: 443ps. 1011: 472ps. 1100: 501ps. 1101: 530ps. 1110: 559ps. 1111: 588ps. Note: 1. The values provided are based on typical case, they could vary from -32% to +49% in real system. 2. These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 6, bits[7:4] in the initialization ROM. ***When in RX Auto De-skew mode (RXA9[1:0]=01b) or Auto De-skew mode (RxA9[1:0]=11b):*** These bits are actually the offset value to be added to the results of Auto De-skew process at RxC2[3:0]. The delay adjustment setting to the delay paths is actually listed as: 0000: Delay setting = RXC2[3:0] 0001: Delay setting = RXC2[3:0] + 1 0010: Delay setting = RXC2[3:0] + 2 0011: Delay setting = RXC2[3:0] + 3 0100: Delay setting = RXC2[3:0] + 4 0101: Delay setting = RXC2[3:0] + 5 0110: Delay setting = RXC2[3:0] + 6 0111: Delay setting = RXC2[3:0] + 7 1000: Delay setting = RXC2[3:0] – 8 1001: Delay setting = RXC2[3:0] – 7 1010: Delay setting = RXC2[3:0] – 6 1011: Delay setting = RXC2[3:0] – 5 1100: Delay setting = RXC2[3:0] – 4 1101: Delay setting = RXC2[3:0] – 3 1110: Delay setting = RXC2[3:0] – 2 1111: Delay setting = RXC2[3:0] – 1 Note: 3. The effective delay values to the transmit paths are provided on the description for the manual mode above. 4. If the calculation above is greater than 1111b, the final delay setting would be at 1111b. If it is less than 0000b, the final delay setting would be 0000b.

Offset Address: B7h (D0F2)

Input Delay Adjustment for HD Group 0 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 0 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#3 of HD Group 0 signals: HD4#, HD6#, HD3# and HD8#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC3[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 0 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#2 of HD Group 0 signals: HD14#, HD11#, HD1#, HDBI0# and HD13#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC3[3:0]**.

Offset Address: B8h (D0F2)
Input Delay Adjustment for HD Group 1 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 1 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#1 of HD Group 1 signals: HD31#, HD18#, HD24#, HD26# and HDBI1#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC4[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 1 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#0 of HD Group 1 signals: HD28#, HD19#, HD27# and HD30#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC4[3:0]**.

Offset Address: B9h (D0F2)
Input Delay Adjustment for HD Group 1 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 1 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#3 of HD Group 1 signals: HD23#, HD20#, HD22# and HD21#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC5[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 1 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#2 of HD Group 1 signals: HD25#, HD29#, HD17# and HD16#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC5[3:0]**.

Offset Address: BAh (D0F2)
Input Delay Adjustment for HD Group 2 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 2 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#1 of HD Group 2 signals: HD33#, HD43#, HD47#, HDBI2# and HD39#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC6[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 2 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#0 of HD Group 2 signals: HD32#, HD42#, HD36# and HD41#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC6[3:0]**.

Offset Address: BBh (D0F2)
Input Delay Adjustment for HD Group 2 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 2 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#3 of HD Group 2 signals: HD38#, HD35#, HD40# and HD45#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC7[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 2 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#2 of HD Group 2 signals: HD34#, HD44#, HD37# and HD46#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC7[3:0]**.

Offset Address: BCh (D0F2)
Input Delay Adjustment for HD Group 3 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 3 – Subgroup#1** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#1 of HD Group 3 signals: HD62#, HD51#, HD59#, HD58# and HDBI3#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC8[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 3 – Subgroup#0** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#0 of HD Group 3 signals: HD61#, HD52#, HD56# and HD60#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC8[3:0]**.

Offset Address: BDh (D0F2)

Input Delay Adjustment for HD Group 3 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 3 – Subgroup#3** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#3 of HD Group 3 signals: HD50#, HD57#, HD63# and HD55#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC9[7:4]**.
3:0	RW	0111b ROMSIP	**Input Delay Adjustment for HD Group 3 – Subgroup#2** Refer to similar structure as shown in Figure 14, these bits are input delay adjustment for subgroup#2 of HD Group 3 signals: HD49#, HD54#, HD53# and HD48#. Please refer to register descriptions at RxB6[3:0]. The bit description is similar to RxB6[3:0] including the ROMSIP location., except that the Auto De-skew process is controlled by **RxC9[3:0]**.

Offset Address: BEh (D0F2)

Auto Compensation Process for Driving Setting **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0 ROMSIP	**Auto Compensation Operating Mode for AGTL+ Driving Setting** This bit defines the mode for the Auto Compensation process (calibration for AGTL+ driving, please refer to Figure 11) to work on this chip. Please also refer to RxA2. 0: Single-shot mode. The Auto Compensation process only occurs when the power is applied to the chip. 1: Continuous-update mode. The Auto Compensation process not only occurs when the power is applied, it also occurs after the chip resumes from the some power management states (e.g. C3, C4, C5, or S1). Note: These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 1, bit[7] in the initialization ROM.
3:2	RW	11b ROMSIP	**Threshold Setting for Voltage Detection at Auto Compensation Process** Please refer to Figure 11. These bits define the times the voltage level of the output of the AGTL PMOS/NMOS dummy driver inside the circuit macro being detected to be stable at the Auto Compensation process. i.e. when Auto Compensation process is on going, the controller detects the signal to reach certain voltage level for this programmed number of times before it latches its final compensation driving setting. 00: 1 times 01: 2 times 10: 3 times 11: 4 times Note: These bits will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are at the second QW, byte 1, bits[6:5] in the initialization ROM.
1	RW	0 ROMSIP	**Operating Mode of Generating Address Bus Inversion** This register bit defined the generation method for HABI#. It is meaningful only when bit 0 is set to 1. 0: ABI (Address Bus Inversion) signal HABI# is generated to minimize the number of changes on the address bus. i.e. The HABI# are asserted if the number of address bits changed (0->1 or 1-> 0) from the previous clock cycle to the current clock cycle are equal to or greater than 9. 1: ABI signal HABI# is generated to minimize the AGTL+ pull-down count. i.e. The HABI# are asserted if the number of "low" on the address bits for the current clock cycle are equal to or greater than 9. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the second QW, byte 1, bit[4] in the initialization ROM.
0	RW	1b ROMSIP	**Address Bus Inversion** HABI# on the V4 bus are valid only when the HAHI[1:0]#, HA[16:3]#, HREQ[2:0]# are valid. When HABI# are low, it indicates the address bus are inverted. 0: Disable. When those address signals are to be driven out on the V4 bus, HABI# is always driven high (de-asserted). 1: Enable. When the address signals are to be driven out on the V4 bus, this chip will drive HABI# low (asserted) based on the operating mode set on bit 1 at the same time while the address signals (HAHI[1:0]#, HA[16:3]#, and HREQ[2:0]#) are inverted. Note: This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the second QW, byte 1, bit[3] in the initialization ROM.

Offset Address: BFh (D0F2) – Reserved

Offset Address: C0h (D0F2)

Auto De-skew Delay Setting – HA Group – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HA Group – Subgroup #1** These bits store the results of the Auto De-skew Process for signals of subgroup#1 for HA group: HABI#, HA13#, HA5#, HA4# and HA7#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXA4[7:4] and RXA7[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HA Group – Subgroup #0** These bits store the results of the Auto De-skew Process for signals of subgroup#0 for HA group: HREQ0#, HREQ1#, HA3#, HA6# and HREQ2#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXA4[3:0] and RXA7[3:0].

Offset Address: C1h (D0F2)

Auto De-skew Delay Setting – HA Group – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HA Group – Subgroup #3** These bits store the results of the Auto De-skew Process for signals of subgroup#3 for HA group: HA10#, HA8#, HA14#, HA16# and HA12#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXA5[7:4] and RXA8[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HA Group – Subgroup #2** These bits store the results of the Auto De-skew Process for signals of subgroup#2 for HA group: HA9#, HA11#, HA15#, HAHI1# and HAHI0#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXA5[3:0] and RXA8[3:0].

Offset Address: C2h (D0F2)

Auto De-skew Delay Setting – HD Group 0 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 0 – Subgroup #1** These bits store the results of the Auto De-skew Process for signals of subgroup#1 for HD group 0: HD14#, HD11#, HD1#, HDBI0# and HD13#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAC[7:4] and RXB6[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 0 – Subgroup #0** These bits store the results of the Auto De-skew Process for signals of subgroup#0 for HD group 0: HD12#, HD5#, HD15# and HD10#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAC[3:0] and RXB6[3:0].

Offset Address: C3h (D0F2)

Auto De-skew Delay Setting – HD Group 0 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 0 – Subgroup #3** These bits store the results of the Auto De-skew Process for signals of subgroup#3 for HD group 0: HD4#, HD6#, HD3# and HD8#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAD[7:4] and RXB7[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 0 – Subgroup #2** These bits store the results of the Auto De-skew Process for signals of subgroup#2 for HD group 0: HD0#, HD9#, HD2# and HD7#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAD[3:0] and RXB7[3:0].

Offset Address: C4h (D0F2)

Auto De-skew Delay Setting – HD Group 1 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 1 – Subgroup #1** These bits store the results of the Auto De-skew Process for signals of subgroup#1 for HD group 0: HD31#, HD18#, HD24#, HD26# and HDBI1#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAE[7:4] and RXB8[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 1 – Subgroup #0** These bits store the results of the Auto De-skew Process for signals of subgroup#0 for HD group 0: HD28#, HD19#, HD27# and HD30#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAE[3:0] and RXB8[3:0].

Offset Address: C5h (D0F2)

Auto De-skew Delay Setting – HD Group 1 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 1 – Subgroup #3** These bits store the results of the Auto De-skew Process for signals of subgroup#3 for HD group 1: HD23#, HD20#, HD22# and HD21#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAF[7:4] and RXB9[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 1 – Subgroup #2** These bits store the results of the Auto De-skew Process for signals of subgroup#2 for HD group 1: HD25#, HD29#, HD17#, and HD16#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXAF[3:0] and RXB9[3:0].

Offset Address: C6h (D0F2)

Auto De-skew Delay Setting – HD Group 2 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 2 – Subgroup #1** These bits store the results of the Auto De-skew Process for signals of subgroup#1 for HD group 2: HD33#, HD43#, HD47#, HDBI2# and HD39#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB0[7:4] and RXBA[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 2 – Subgroup #0** These bits store the results of the Auto De-skew Process for signals of subgroup#0 for HD group 2: HD32#, HD42#, HD36# and HD41#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are used as the input delay setting for signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are used as the output and input delay setting for signals mentioned above. Please refer to the register descriptions at RXB0[3:0] and RXBA[3:0].

Offset Address: C7h (D0F2)

Auto De-skew Delay Setting – HD Group 2 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 2 – Subgroup #3** These bits store the results of the Auto De-skew Process for signals of subgroup#3 for HD group 2: HD38#, HD35#, HD40# and HD45#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB1[7:4] and RXBB[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 2 – Subgroup #2** These bits store the results of the Auto De-skew Process for signals of subgroup#2 for HD group 2: HD34#, HD44#, HD37# and HD46#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB1[3:0] and RXBB[3:0].

Offset Address: C8h (D0F2)

Auto De-skew Delay Setting – HD Group 3 – 1 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 3 – Subgroup #1** These bits store the results of the Auto De-skew Process for signals of subgroup#1 for HD group 3: HD62#, HD51#, HD59#, HD58# and HDBI3#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB2[7:4] and RXBC[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 3 – Subgroup #0** These bits store the results of the Auto De-skew Process for signals of subgroup#0 for HD group 3: HD61#, HD52#, HD56# and HD60#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB2[3:0] and RXBC[3:0].

Offset Address: C9h (D0F2)

Auto De-skew Delay Setting – HD Group 3 – 2 **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Auto De-skew Delay Setting for HD Group 3 – Subgroup #3** These bits store the results of the Auto De-skew Process for signals of subgroup#3 for HD group 3: HD50#, HD57#, HD63# and HD55#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. **When in RX Auto De-skew mode (RXA9[1:0]=01b):** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB3[7:4] and RXBD[7:4].
3:0	RO	HwInit	**Auto De-skew Delay Setting for HD Group 3 – Subgroup #2** These bits store the results of the Auto De-skew Process for signals of subgroup#2 for HD group 3: HD49#, HD54#, HD53# and HD48#. ***When in Manual mode (RXA9[1:0]=-0b):*** These bits does not have any impact to the driving of signals mentioned above. ***When in RX Auto De-skew mode (RXA9[1:0]=01b):*** These bits are the main delay for the input delay setting of signals mentioned above. ***When in Auto De-skew mode (RXA9[1:0]=11b):*** These bits are the main delay for the output and input delay setting of signals mentioned above. Please refer to the register descriptions at RXB3[3:0] and RXBD[3:0].

Offset Address: CA-FFh (D0F2) – Reserved

DEVICE 0 FUNCTION 3 (D0F3): DRAM BUS CONTROL

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 15 below.

Device 0 Function 3 is a Host Bridge and in order to access this function D0F0 Rx4F[0] must be set to 1. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 3. i.e.: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**011**	RX value with bit[1:0] = 00b		

All registers in Device 0 Function 3 DRAM Controller are implemented in the area of the chip which is powered by suspend power on the motherboard. During suspend power mode all register values would be retained and all the power in the system would be shut off except for the suspend power. When the system DRAM and the DRAM controller related registers are powered by the suspend power, the system will retain the system information in the DRAM, while most of the system power for the chip is shut off. Comparing with the case in which the whole system is powered off, suspend mode allows the system to easily and efficiently return to the normal operating mode whenever the system is required to.

Besides the registers for the DRAM controller, D0F3 also contains registers for the GMINT (GFX Controller) and VMINT (GFX Controller and Video decoder) interfaces. Please refer to the shaded blocks Figure 15 below for details.

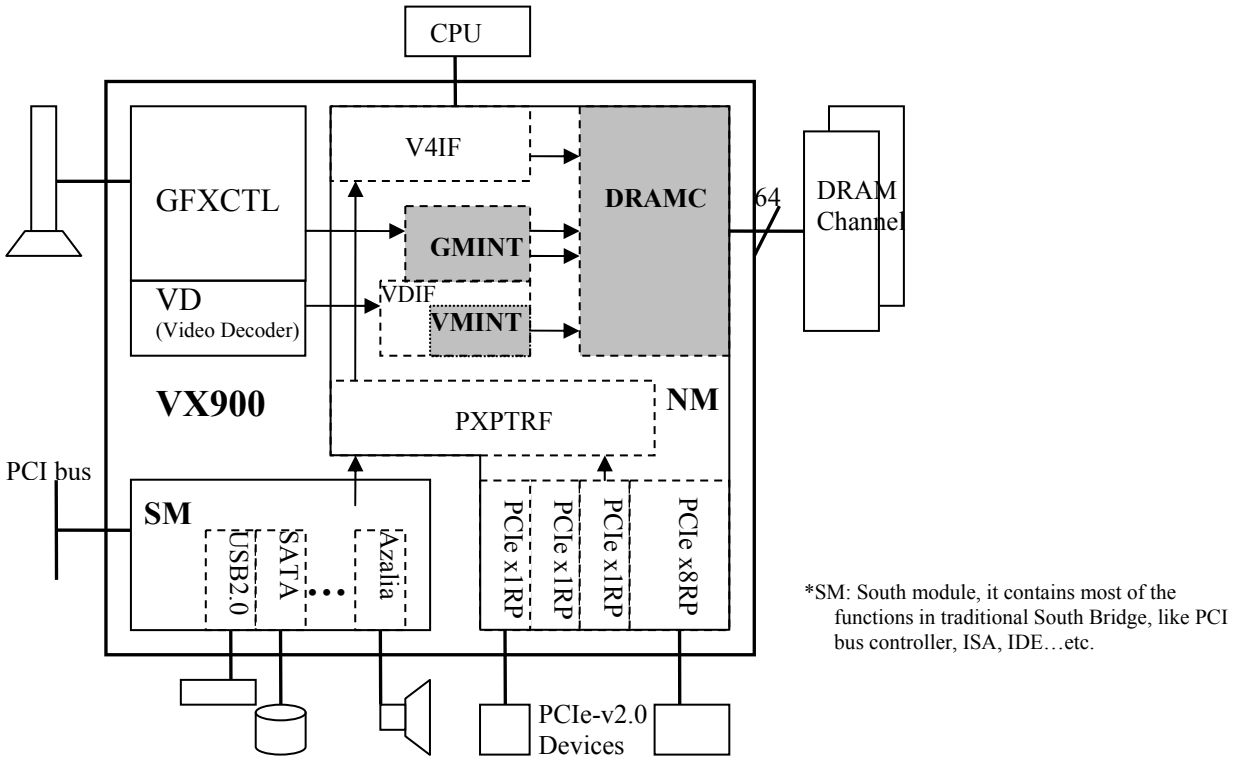


Figure 15. System Block Diagram for D0F3

DRAM Controller Overview

VX900 Series is a chip which integrated the original chipset functions of North Bridge (NB), South Bridge (SB) and a graphic controller (GFXCTL). DRAM controller (DRAMC) is one of the major functions in the NB, which interfaced with host controller to communicate with the CPU. It also communicates with the Graphic controller and Video Decoder via two modules: GMINT and VDIF (with major block VMINT). These upstream cycles requested by PXPTRF are cycles from PCIe controller and other controllers in the SB and they would go to host controller to perform cache snooping and eventually go to DRAMC.

VX900 Series DRAM controller supports DDR2 533 - 800 MHz and DDR3 800 - 1066 MHz. Note that the VX900 Series system board with is capable of supporting either DDR2 or DDR3, but not both. The registers within this IRS are applied to both DDR2 and DDR3. If the registers are applied to only one of them, special notation will be stated in the descriptions. The maximum DRAM bus width is 64 bits. This DRAM is used for the main memory and the frame buffers (memory used for Graphic controller). It can be configured either at 64 bits or 32 bits as shown in the table below:

Table 12. Complete DRAM Supporting Mode

DRAM Supporting Mode	DRAM Mode Related Registers	DRAM Bus Data Bits	
	Rx6C[3]	High 32-Bits	Low 32-Bits
M64	0	Activated	Activated
M32	1	Float	Activated

M32 mode is mostly used for debugging and the high 32 bits of data in this mode are either floating or de-activated. When this mode is used the system board will need to be configured so the high 32 bits of data bus (MD[63:32]) won't be connected to any other signals on the motherboard. Also be noted that the internal Video Decoder (VD) worked only at 64 bit mode. So if the M32 working mode is desired, VD function will not be available.

DRAMC Architecture

VX900 Series can work with two DIMM sockets on the motherboard. Refer to Figure 16 below, each DIMM can have two ranks of DRAM. The term "Rank" refers to a group of DRAM chip on the DIMM module which have their CS (chip select) and CMD (command signals) connected together. Therefore, the command pins of different ranks might be connected together, and use MCS# pins to differentiate them.

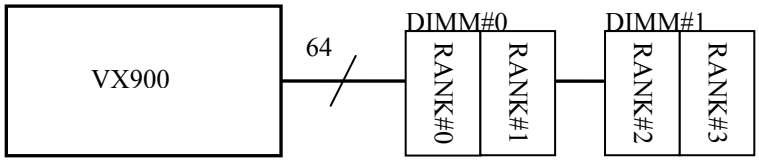


Figure 16. VX900 Series DRAM Supporting Schemes

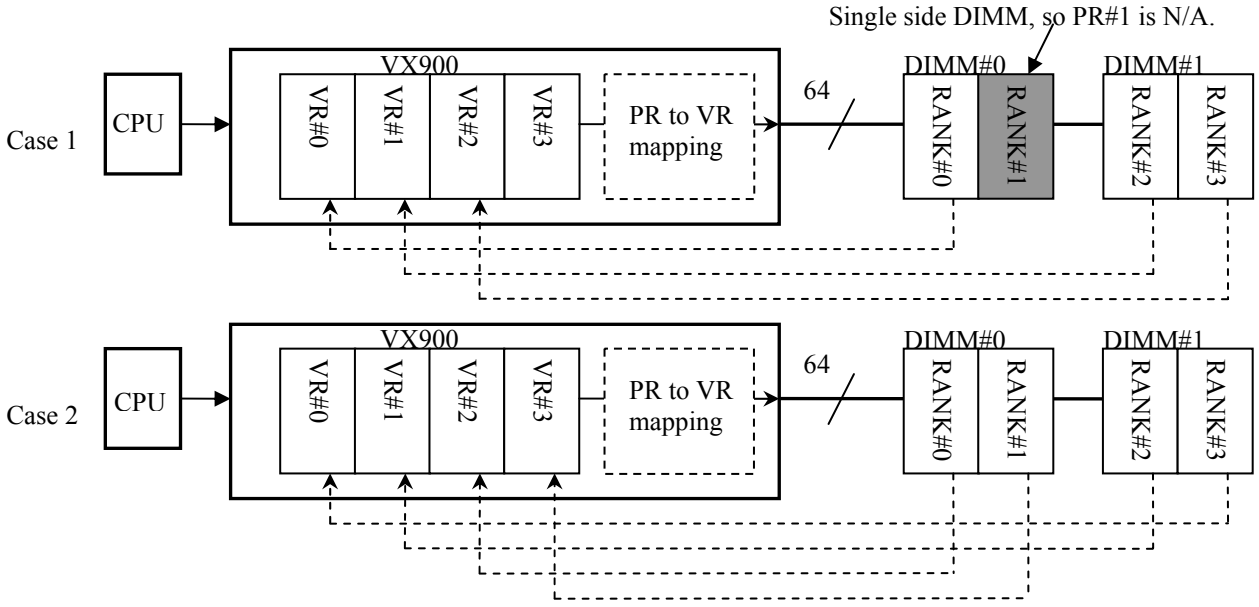


Figure 17. Examples of Physical Rank (PR) to Virtual Rank (VR) Mapping

Virtual Rank to Physical Rank Mapping

DRAMC decodes cycles which directed to memory locations on the DIMM sockets. As shown in Figure 17, it uses Virtual Rank (VR) structure to access to the Physical Rank (PR) on the DIMM. PR can be mapped to any VR through register setting at Rx54~Rx55. The virtual rank mapping architecture here is originally built so that at most two PRs can be mapped to the same VR. For example, PR0 → VR0, PR1 → VR0 for 128 bits DRAM bus supports. However, VX900 Series only supports one-to-one mapping, , in another word, only 64 bits DRAM accessing is supported in this chip. So when the registers for PR-to-VR mapping at Rx54~Rx55 are programmed, users should be aware that one-to-one PR-to-VR mapping is being taking care of.

VR are defined by the beginning and the ending address (Rx40~Rx43, Rx48~Rx4B). Cycles from CPU, Graphic controller or other master devices from module PXPTRF (refer to Figure 15) with address falling into the starting address and ending address (i.e. starting <= Address < ending) of a specific range will be directed to that VR. And the cycle will also be directed to the PR through the PR to VR mapping, please refer to Figure 17 for more details.

The ending address of a system looks like to be the ending address of the last VR, e.g., the ending address of VR#2 in case 1 of Figure 17 or the ending address of VR#3 in case 2 of Figure 17. However, the predefined addressing allocation for the fundamental PC architecture occupied some space on the 4G boundary, and there are also frame buffer memory and SMM (System Memory Management) memory used by the system. Please be noted the real memory can be used by the users are different in different situations.

Bank Interleave

As shown in Figure 18, the "Banks" are referred as the memory allocations within the Rank on a DIMM. The bank interleave is an architecture to access two banks of memory alternatively. What the DRAM controller should do is to assign proper address bits as the bank addresses so the performance of certain applications can be maximized.

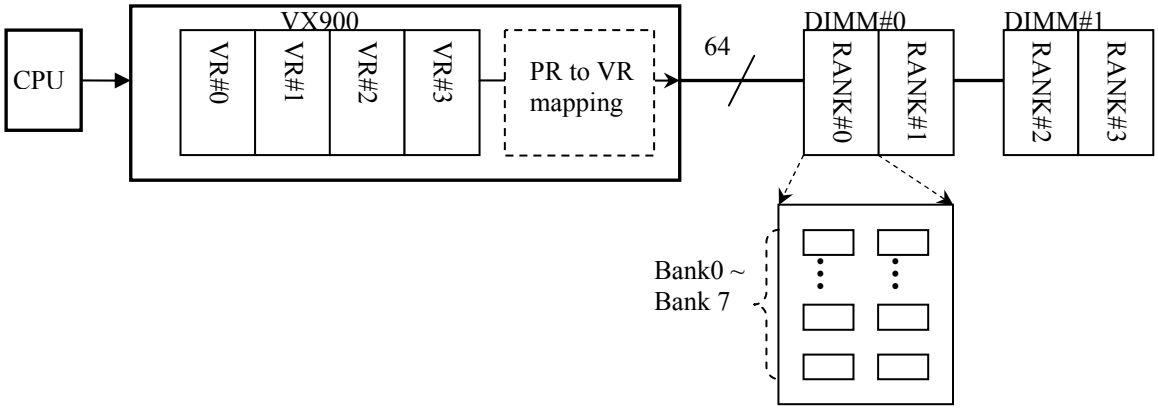


Figure 18. Bank Structure in the DRAM DIMM

Header Registers (00–3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-0h (D0F3)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F3)

Device ID **Default Value: 3410h**

Bit	Attribute	Default	Description
15:0	RO	3410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F3)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RO	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F3)
PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RO	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RO	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	0	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus.
8	RO	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F3)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** These bits are PCI header registers. They are the revision ID of this function.

Offset Address: 0B-09h (D0F3)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	06 0000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F3)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F3)
PCI Master Latency Timer — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F3)
Header Type — **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value of these bits are 80h. It indicates this is a multi-function device.

Offset Address: 0Fh (D0F3)
Built In Self Test (BIST) — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F3)
Base Address Registers 0 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D0F3)
Base Address Registers 1 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 1B-18h (D0F3)
Base Address Registers 2 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F3)
Base Address Registers 3 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 3** This function does not claim base address.

Offset Address: 23-20h (D0F3)
Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 4** This function does not claim base address.

Offset Address: 27-24h (D0F3)
Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 5** This function does not claim base address.

Offset Address: 2B-28h (D0F3)
CardBus CIS Pointer **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F3)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F3)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F3)-Reserved

Offset Address: 34h (D0F3)
Capability Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F3)-Reserved

Offset Address: 3D-3Ch (D0F3)

Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F3)

Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

DRAM Rank (Row) Beginning / Ending Address (40–4Fh)

The actual DRAM ending address of the system with the DRAM usage is quite different depending on the system application and available register options presented in this document. Note the integrated graphic controller might request some chunk of memory as its frame buffer, also need to note that there is system required address which had to be reserved for specific use.

Offset Address: 40h (D0F3)

DRAM Rank Ending Address 0 **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RWS	01h	**Virtual Rank 0 Ending Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 0 when the address meets the following condition: Rx48 <= A[33:26]< Rx40

Offset Address: 41h (D0F3)

DRAM Rank Ending Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 1 Ending Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 1 when the Address meets the following condition: Rx49 <= A[33:26]< Rx41

Offset Address: 42h (D0F3)

DRAM Rank Ending Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 2 Ending Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 2 when the Address meets the following condition: Rx4A <= A[33:26]< Rx42

Offset Address: 43h (D0F3)

DRAM Rank Ending Address 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 3 Ending Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 3 when the Address meets the following condition: Rx4B <= A[33:26]< Rx43

Offset Address: 47-44h (D0F3)

Reserved **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**Reserved for Further DRAM Rank Supports**

Offset Address: 48h (D0F3)

DRAM Rank Beginning Address 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 0 Beginning Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 0 when the Address meets the following condition: Rx48 <= A[33:26]< Rx40

Offset Address: 49h (D0F3)

DRAM Rank Beginning Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 1 Beginning Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 1 when the Address meets the following condition: Rx49 <= A[33:26]< Rx41

Offset Address: 4Ah (D0F3)

DRAM Rank Beginning Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 2 Beginning Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 2 when the Address meets the following condition: Rx4A <= A[33:26]< Rx42

Offset Address: 4Bh (D0F3)

DRAM Rank Beginning Address 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**Virtual Rank 3 Beginning Address** DRAM controller will direct cycles (either from CPU or other master devices) to Virtual Rank 3 when the Address meets the following condition: Rx4B <= A[33:26]< Rx43

Offset Address: 4F-4Ch (D0F3)

Reserved **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**Reserved for Further DRAM Rank Supports**

MA Map / Command Rate (50–53h)

Offset Address: 51-50h (D0F3)

DRAM MA Map Type **Default Value: 2424h**

Bit	Attribute	Default	Description
15:13	RWS	001b	**Reserved**
12:10	RWS	001b	**Reserved**
9	RWS	0	**Reserved**
8	RWS	0	**1T Command/MA Rate** Continuous DRAM commands issued on the DRAM bus by this chip. 0: Disable (2T command), the fastest DRAM command rate on the DRAM bus is every other T. 1: 1T command, i.e. every T on the DRAM bus could have a valid DRAM command. Please refer to Rx9E[6] for more information.
7:5	RWS	001b	**Rank 2/3 MA Map Type** Table 13 below showed the address bits arrangement of Bank / Row / Column address for Rank 2 and Rank 3. If the DRAM plugged in is DDR3, MA map type 011b and 111b should not be selected.
4:2	RWS	001b	**Rank 0/1 MA Map Type** Table 13 below showed the address bits arrangement of Bank / Row / Column address for Rank 0 and Rank 1. If the DRAM plugged in is DDR3, MA map type 011b and 111b should not be selected.
1:0	RWS	0	**Reserved**

Table 13. Rx50 Number of Bits for Bank / Row / Column Address Supported for Different MA Map Type

Rank MA Map Type	000	001	010	011	100	101	110	111
# of Bank Address Bits	2	2	2	2	Reserved	3	3	3
# of Row Address Bits (*1)	13-12	14-12	16-12	16-13		16-12	16-12	16-13
# of Column Address Bits (*2)	9	10	11	12		10	11	12
DRAM Size (Byte)	128M-64M	512M-128M	2G-256M	4G-1G		2G-256M	4G-512M	8G-2G

Notes:
1. One MA Map type can support several DRAM types which have different number of Row address. Those high row address bits could be mapped from high system address bits.
2. Column address bit A10 is always used as the “Auto-Precharge” bit. For DDR3, A12 is also used as the “Burst-Chop” bit. Thus, when working with DDR3, MA map type 011b and 111b cannot be selected.

Offset Address: 53-52h (D0F3)

Bank / Rank Interleave Address Select **Default Value: 0111h**

Bit	Attribute	Default	Description
15:14	RWS	0	**Rank Interleave Address Bit 1 (RA1) Selection** Address bit that Rank Address bit 1 is mapped to. 00: A14 01: A16 10: A18 11: A20 For more detail of how to set this bits, please refer to Table 15 below. Also note that the Address being mapped by the Bank Address: MBA2, MBA1, MBA0 and the internal Rank Address: RA1, RA0 cannot be the conflict. *1
13:12	RWS	0	**Rank Interleave Address Bit 0 (RA0) Selection** Address bit that Rank Address bit 1 is mapped to. 00: A15 01: A17 10: A19 11: A21 For more detail of how to set this bits, please refer to Table 15 below. Also note that the Address being mapped by the Bank Address: MBA2, MBA1, MBA0 and the internal Rank Address: RA1, RA0 cannot be the conflict. *1
11	RWS	0	**BA2 Support Enable** This bit needs to be turn on if 8 bank DRAM is detected in the system. 0: Disable BA2 support 1: Enable BA2 support
10:8	RWS	001b	**Pin MBA2 Bank Address Bit 2 Select** Address bit that pin MBA2 is mapped to: x00: A14 x01: A15 x10: A18 x11: A19 IF Rx53[3] is 0, these bits are meaningless. For more detail of how to set these bits, please refer to Table 14 below. Also note that the address being mapped by the Bank Address: MBA2, MBA1, MBA0 and the internal Rank Address: RA1, RA0 cannot be the conflict (Note).
7	RWS	0	**Reserved** Writing 1or 0 to this bit does not have any impact to this chip.
6:4	RWS	001b	**Pin MBA1 Bank Address Bit 1 Select** Address bit that pin MBA1 is mapped to: 000: A12 001: A14 010: A16 011: A18 1xx: A20 For more detail of how to set these bits, please refer to Table 14 below. Also note that the Address being mapped by the Bank Address: MBA2, MBA1, MBA0 and the internal Rank Address: RA1, RA0 cannot be the conflict (Note).
3	RWS	0	**Reserved** Writing 1 or 0 to this bit does not have any impact to this chip.
2:0	RWS	001b	**Pin MBA0 Bank Address Bit 0 Select** Address bit that pin MBA0 is mapped to: 000: A11 001: A13 010: A15 011: A17 1xx: A19 For more detail of how to set these bits, please refer to Table 14 below. Also note that the Address being mapped by the Bank Address: MBA2, MBA1, MBA0 and the internal Rank Address: RA1, RA0 cannot be the conflict (Note).

Note: What the address being selected by MBA2, MBA1, MBA0, RA1, RA0 should be different. i.e. when Rx53[7:6] is programmed to 01, which select A16 as the RA1; Rx52[6:4] should not be programmed to 010, which also select A16 as the MBA1.

Table 14. Rx52 Bank Address Selections

Rx53[2:0]	Rx52[6:4]	Rx52[2:0]	Rx69[5]	Rx53[3]	MBA2	MBA1	MBA0	Comment
---	---	---	-	0	0	-	-	
-00	---	---	0	1	A14	-	-	
-01	---	---	0	1	A15	-	-	
-10	---	---	0	1	A18	-	-	
-11	---	---	0	1	A19	-	-	
-00 or -11	---	---	1	1	A18^A15	-	-	Invalid (*1)
-01 or -10	---	---	1	1	A18^A15	-	-	
---	000	---	0	-	-	A12	-	
---	001	---	0	-	-	A14	-	
---	010	---	0	-	-	A16	-	
---	011	---	0	-	-	A18	-	
---	1--	---	0	-	-	A20	-	
---	000	---	1	0	-	A20^A18^A16^A14	-	Invalid (*2)
---	Other than 000	---	1	0	-	A20^A18^A16^A14	-	
---	000 or 011	---	1	1	-	A20^A16^A14	-	Invalid (*2)
---	other than 000 and 011	---	1	1	-	A20^A16^A14	-	
---	---	000	0	-	-	-	A11	Invalid (*3)
---	---	001	0	-	-	-	A13	
---	---	010	0	-	-	-	A15	
---	---	011	0	-	-	-	A17	
---	---	1--	0	-	-	-	A19	
---	---	000	1	0	-	-	A19^A17^A15^A13	Invalid (*4)
---	---	Other than 000	1	0	-	-	A19^A17^A15^A13	
---	---	000 or 010	1	1	-	-	A19^A17^A13	Invalid (*4)
---	---	other than 000 and 010	1	1	-	-	A19^A17^A13	

Notes:
1. When Rx69[5] = 1, the MBA2 would be the exclusive-or function of A18 and A15. In this case, Rx53[2:0] must be programmed to select either A15 or A18 for the system to work properly.
2. When Rx69[5] = 1, the MBA1 would be the exclusive-or function of A20, A18, A16, and A14 depending on the Rx53[3]. In this case, Rx52[6:4] must be programmed to select one of the elements in the exclusive-or function (A20, A18, A16, or A14) for the system to work properly.
3. Rx52[2:0] selected as 000, which assigned A11 to MBA0. However, A11 had been assigned as the Column Address in all of the current MA type, which make the selection invalid.
4. When Rx69[5] = 1, the MBA0 would be the exclusive-or function of A19, A17, A15, and A13 depending on the Rx53[3]. In this case, Rx52[2:0] must be programmed to select one of the elements in the exclusive-or function (A19, A17, A16, or A13) for the system to work properly.

Table 15. Rx53 Bank Address Selections

Rx53[7:6]	Rx53[5:4]	RA2 (Note)	RA1	RA0
00	--	A6	A14	-
01	--	A6	A16	-
10	--	A6	A18	-
11	--	A6	A20	-
--	00	A6	-	A15
--	01	A6	-	A17
--	10	A6	-	A19
--	11	A6	-	A21

Note: RA2 mapping is not used for this chip.

There are three Rank Address bits for the DRAM controller, RA2, RA1, and RA0. These three bits are internal to the chip to select address bits for Rank decoding. But since there are at most 4 ranks are supported, RA2 mapping is not used for this chip. RA1 and RA0 can be mapped from A14 to A21 depending on how the register Rx53[7:6] and Rx53[5:4] are programmed. Their setting mainly depends on what kind of application software that this chip is used for.

Physical-to-Virtual Rank Mapping (54–57h)

Offset Address: 57-54h (D0F3)

Physical-to-Virtual Rank Mapping **Default Value: 765C 3218h**

Bit	Attribute	Default	Description
31:28	RWS	7h	**Reserved**
27:24	RWS	6h	**Reserved**
23:20	RWS	5h	**Reserved**
19:16	RWS	Ch	**Reserved**
15	RWS	0	**Enable Physical Rank 3** 0: Disable Physical Rank (PR) 3 by de-asserting the Pin MCS3_. 1: Enable Physical Rank 3 by allowing MCS3_ be activated when the cycles are directed to.
14	RWS	0	**Reserved**
13:12	RWS	11b	**Virtual Rank Number of Physical Rank 3** The Virtual Rank (VR) # that the Physical Rank (PR) 3 is mapped to (Note). 00: VR0, Cycles with address decoded to go to VR 0 will be directed to PR 3. 01: VR1, Cycles with address decoded to go to VR 1 will be directed to PR 3. 10: VR2, Cycles with address decoded to go to VR 2 will be directed to PR 3. 11: VR3, Cycles with address decoded to go to VR 3 will be directed to PR 3.
11	RWS	0	**Enable Physical Rank 2** 0: Disable Physical Rank (PR) 2 by de-asserting the Pin MCS2_. 1: Enable Physical Rank 2 by allowing MCS2_ be activated when the cycles are directed to.
10	RWS	0	**Reserved**
9:8	RWS	10b	**Virtual Rank Number of Physical Rank 2** The Virtual Rank (VR) # that the Physical Rank (PR) 2 is mapped to (Note). 00: VR0, Cycles with address decoded to go to VR 0 will be directed to PR 2. 01: VR1, Cycles with address decoded to go to VR 1 will be directed to PR 2. 10: VR2, Cycles with address decoded to go to VR 2 will be directed to PR 2. 11: VR3, Cycles with address decoded to go to VR 3 will be directed to PR 2.
7	RWS	0	**Enable Physical Rank 1** 0: Disable Physical Rank (PR) 1 by de-asserting the Pin MCS1_. 1: Enable Physical Rank 1 by allowing MCS1_ be activated when the cycles are directed to.
6	RWS	0	**Reserved**
5:4	RWS	01b	**Virtual Rank Number of Physical Rank 1** The Virtual Rank (VR) # that the Physical Rank (PR) 1 is mapped to (Note). 00: VR0, Cycles with address decoded to go to VR 0 will be directed to PR 1. 01: VR1, Cycles with address decoded to go to VR 1 will be directed to PR 1. 10: VR2, Cycles with address decoded to go to VR 2 will be directed to PR 1. 11: VR3, Cycles with address decoded to go to VR 3 will be directed to PR 1.
3	RWS	1b	**Enable Physical Rank 0** 0: Disable Physical Rank (PR) 0 by de-asserting the Pin MCS0_. 1: Enable Physical Rank 0 by allowing MCS0_ be activated when the cycles are directed to.
2	RWS	0	**Reserved**
1:0	RWS	0	**Virtual Rank Number of Physical Rank 0** The Virtual Rank (VR) # that the Physical Rank (PR) 0 is mapped to (Note). 00: VR0, Cycles with address decoded to go to VR 0 will be directed to PR 0. 01: VR1, Cycles with address decoded to go to VR 1 will be directed to PR 0. 10: VR2, Cycles with address decoded to go to VR 2 will be directed to PR 0. 11: VR3, Cycles with address decoded to go to VR 3 will be directed to PR 0.

Note: Rx54[1:0], Rx54[5:4], Rx55[1:0] and Rx55[5:4] have to have different programming. i.e. those PR # to VR# mapping are one to one mapping.

Virtual Rank Interleave Address Select / Enable (58–5Fh)

Offset Address: 58h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6:4	RWS	0	**Rank #0 Interleave Address Select** This 3-bit field determines the decoding of the internal Rank Interleave Address (RA[2:0]) for Virtual Rank (VR) 0. The corresponding address bits of the Rank Address (RA[1:0]) are defined at Rx53[7:6] and Rx53[5:4]. RA2 is always mapped from A6 in the chip. **When bits [2:0] are set to 000b:** xxx: Rank Interleave of VR 0 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 0. **When bits [2:0] are set to 001b:** xx0: The decoding of RA0 for VR 0 is 0. RA2, RA1 are ignored. xx1: The decoding of RA0 for VR 0 is 1. RA2, RA1 are ignored. **When bits [2:0], RINVL0AEN[2:0] are set to 010b:** x0x: The decoding of RA1 for VR 0 is 0. RA2, RA0 are ignored. x1x: The decoding of RA1 for VR 0 is 1. RA2, RA0 are ignored. **When bits [2:0] are set to 011b:** x00: The decoding of the {RA1, RA0} for VR 0 is 00. RA2 is ignored. x01: The decoding of the {RA1, RA0} for VR 0 is 01. RA2 is ignored. x10: The decoding of the {RA1, RA0} for VR 0 is 10. RA2 is ignored. x11: The decoding of the {RA1, RA0} for VR 0 is 11. RA2 is ignored. **When bits [2:0] are set to 1xx:** xxx: Invalid setting, VX900 Series only supports 4 Ranks, RA2 is never needed to be used.
3	RWS	0	**Reserved**
2:0	RWS	0	**Rank #0 Interleave Address Enable** 000: The Rank Interleave address decoding for VR 0 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 0. 001: Only RA0 is used for Rank Interleave address decoding for VR 0. 010: Only RA1 is used for Rank Interleave address decoding for VR 0. 011: RA1 and RA0 are both used for Rank Interleave address decoding for VR 0. 1xx: Invalid, VX900 Series only supports 4 Ranks. RA2 is never needed to be used. Please refer to the register description of bits [6:4] for more details.

Offset Address: 59h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6:4	RWS	0	**Rank #1 Interleave Address Select** This 3-bit field determines the decoding of the internal Rank Interleave Address (RA[2:0]) for Virtual Rank (VR) 1. The corresponding address bits of the Rank Address (RA[1:0]) are defined at Rx53[7:6] and Rx53[5:4]. RA2 is always mapped from A6 in the chip. **When bits [2:0] are set to 000b:** xxx: Rank Interleave of VR 1 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 1. **When bits [2:0] are set to 001b:** xx0: The decoding of RA0 for VR 1 is 0. RA2, RA1 are ignored. xx1: The decoding of RA0 for VR 1 is 1. RA2, RA1 are ignored. **When bits [2:0] are set to 010b:** x0x: The decoding of RA1 for VR 1 is 0. RA2, RA0 are ignored. x1x: The decoding of RA1 for VR 1 is 1. RA2, RA0 are ignored. **When bits [2:0] are set to 011b:** x00: The decoding of the {RA1, RA0} for VR 1 is 00. RA2 is ignored. x01: The decoding of the {RA1, RA0} for VR 1 is 01. RA2 is ignored. x10: The decoding of the {RA1, RA0} for VR 1 is 10. RA2 is ignored. x11: The decoding of the {RA1, RA0} for VR 1 is 11. RA2 is ignored. **When Rx58[2:0] are set to 1xx:** xxx: Invalid setting, X900 only supports 4 Ranks, RA2 is never needed to be used.
3	RWS	0	**Reserved**
2:0	RWS	0	**Rank #1 Interleave Address Enable** 000: The Rank Interleave address decoding for VR 1 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 1. 001: Only RA0 is used for Rank Interleave address decoding for VR 1. 010: Only RA1 is used for Rank Interleave address decoding for VR 1. 011: RA1 and RA0 are both used for Rank Interleave address decoding for VR 1. 1xx: Invalid setting, VX900 Series only supports 4 Ranks. RA2 is never needed to be used. Please refer to the register description of bits [6:4] for more details.

Offset Address: 5Ah (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6:4	RWS	0	**Rank #2 Interleave Address Select** This 3-bits field determines the decoding of the internal Rank Interleave Address (RA[2:0]) for Virtual Rank (VR) 2. The corresponding address bits of the Rank Address (RA[1:0]) are defined at Rx53[7:6] and Rx53[5:4]. RA2 is always mapped from A6 in the chip. **When bits [2:0] are set to 000b:** xxx: Rank Interleave of VR 2 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 2. **When bits [2:0] are set to 001b:** xx0: The decoding of RA0 for VR 2 is 0. RA2, RA1 are ignored. xx1: The decoding of RA0 for VR 2 is 1. RA2, RA1 are ignored. **When bits [2:0] are set to 010b:** x0x: The decoding of RA1 for VR 2 is 0. RA2, RA0 are ignored. x1x: The decoding of RA1 for VR 2 is 1. RA2, RA0 are ignored. **When bits [2:0] are set to 011b:** x00: The decoding of the {RA1, RA0} for VR 2 is 00. RA2 is ignored. x01: The decoding of the {RA1, RA0} for VR 2 is 01. RA2 is ignored. x10: The decoding of the {RA1, RA0} for VR 2 is 10. RA2 is ignored. x11: The decoding of the {RA1, RA0} for VR 2 is 11. RA2 is ignored. **When Rx58[2:0] are set to 1xx:** xxx: Invalid setting, VX900 Series only supports 4 Ranks, RA2 is never needed to be used.
3	RWS	0	**Reserved**
2:0	RWS	0	**Rank #2 Interleave Address Enable** 000: The Rank Interleave address decoding for VR 2 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 2. 001: Only RA0 is used for Rank Interleave address decoding for VR 2. 010: Only RA1 is used for Rank Interleave address decoding for VR 2. 011: RA1 and RA0 are both used for Rank Interleave address decoding for VR 2. 1xx: Invalid setting, VX900 Series only supports 4 Ranks. RA2 is never needed to be used. Please refer to the register description of bits [6:4] for more details.

Offset Address: 5Bh (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6:4	RWS	0	**Rank #3 Interleave Address Select** This 3-bit field determines the decoding of the internal Rank Interleave Address (RA[2:0]) for Virtual Rank (VR) 3. The corresponding address bits of the Rank Address (RA[1:0]) are defined at Rx53[7:6] and Rx53[5:4]. RA2 is always mapped from A6 in the chip. **When bits [2:0] are set to 000b:** xxx: Rank Interleave of VR 3 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 3. **When bits [2:0] are set to 001b:** xx0: The decoding of RA0 for VR 3 is 0. RA2, RA1 are ignored. xx1: The decoding of RA0 for VR 3 is 1. RA2, RA1 are ignored. **When bits [2:0] are set to 010b:** x0x: The decoding of RA1 for VR 3 is 0. RA2, RA0 are ignored. x1x: The decoding of RA1 for VR 3 is 1. RA2, RA0 are ignored. **When bits [2:0] are set to 011b:** x00: The decoding of the {RA1, RA0} for VR 3 is 00. RA2 is ignored. x01: The decoding of the {RA1, RA0} for VR 3 is 01. RA2 is ignored. x10: The decoding of the {RA1, RA0} for VR 3 is 10. RA2 is ignored. x11: The decoding of the {RA1, RA0} for VR 3 is 11. RA2 is ignored. **When Rx58[2:0] are set to 1xx:** xxx: Invalid setting, VX900 Series only supports 4 Ranks, RA2 is never needed to be used.
3	RWS	0	**Reserved**
2:0	RWS	0	**Rank #3 Interleave Address Enable** 000: The Rank Interleave address decoding for VR 3 is disabled, i.e. this chip will use the decoding of the highest address bits of the system to select VR 3. 001: Only RA0 is used for Rank Interleave address decoding for VR 3. 010: Only RA1 is used for Rank Interleave address decoding for VR 3. 011: RA1 and RA0 are both used for Rank Interleave address decoding for VR 3. 1xx: Invalid setting, VX900 Series only supports 4 Ranks. RA2 is never needed to be used. Please refer to the register description of bits [6:4] for more details.

Offset Address: 5Ch (D0F3) – Reserved

Offset Address: 5Dh (D0F3)

8Gb Support **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RWS	0	**Reserved**
0	RWS	0	**Enable 8Gb DRAM Device Support** 0: Disable 1: Enable Only set this bit to 1 when using 8Gb device. When set to 1, address bit A16 can not map to row address bits.

Offset Address: 5Eh (D0F3) – Reserved

Offset Address: 5Fh (D0F3)

4Gb Support **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RWS	0	**Reserved**
0	RWS	0	**Enable 4Gb DRAM Device Support** 0: Disable 1: Enable Only set this bit to 1 when using 4Gb device. When set to 1, address bit A13 must map to one of the bank address bits.

DRAMC Pipeline Control (60–64h)

Offset Address: 60h (D0F3)

DRAM Pipeline Turn-Around Setting **Default Value: 04h**

Bit	Attribute	Default	Description
7	RWS	0	**Back-to-Back Write to Different Ranks (0 Wait State Write)** This register applies to commands to different ranks only. 0: Disabled, there is at least one Turn-Around cycle in between the data phase of two write operations on the DRAM bus. 1: Enabled, the seamless write operation is supported.
6	RWS	0	**Fast Read-to-Read Turn Around for Different Ranks** This register applies to commands to different ranks only. 0: Disabled, there is at least one Turn-Around cycle in between the data phase of two read operations on the DRAM bus. 1: Enabled, the seamless read operation is supported.
5	RWS	0	**Fast Read-to-Write Turn Around** This register applies to commands to different ranks or the same ranks. 0: Disabled. 1: Enabled, this option reduced 1 Turn Around cycle on the MD bus when Read operation is followed by Write operation.
4	RWS	0	**Fast Write-to-Read Turn Around** This register applies to commands to different ranks only. 0: Disabled. 1: Enabled, this option reduced 1 Turn Around cycle on the MD bus when Write operation is followed by Read operation.
3	RWS	0	**Reserved**
2	RWS	1b	**Write Merging Disable for 8QW Write Request.** This bit worked with Rx61[1], Rx62[7:4] and Rx62[3:0], please refer to Table 16 and Figure 19 for details regarding to write merging behavior. 0: Multiple write requests, either 4QW or 8QW, will be merged into one as needed. 1:8QW write request will not be merged.
1:0	RWS	0	**Reserved**

Table 16. Rx61 Write Merging Options with Rx62[7:4] =a and Rx62[3:0] =b

Rx61[1]	Rx60[2]	The current write cycle's data size	# of write requests accumulated in front of the current write in the queue	How many write requests comes in after the current write	Being able to do Write Merging? (For requests just coming in or those already in and doing shifting in the queue.)
0	-	-	-	-	No (*1)
1	0	-	< a + 1	-	No (*1)
1	0	-	>= a + 1	< b	Yes (*2)
1	0	-	>= a + 1	>= b	No (*3)
1	1	8QW	-	-	No (*1)
1	1	4, 2, 1 QW	< a + 1	-	No (*1)
1	1	4, 2, 1 QW	>= a + 1	< b	Yes (*2)
1	1	4, 2, 1 QW	>= a + 1	>= b	No (*3)

Notes:
1. The DRAM controller will send the current write requests to the DRAM bus. No Write Merging will be happen to this write request.
2. The current write request will be kept in the queue waiting for merging. i.e. any further write requests with the same address coming in will be merged into this request in the queue. For example, if a is programmed as 0010b, that means the safety window for not merging is a+1, 3 requests. Thus, if there is 3 requests in front of current write, this write is merge-able.
3. The write stayed in the queue, either waiting for merging or having been merged, is eligible to go out to DRAM bus. There will be no merging happened to this request any more.

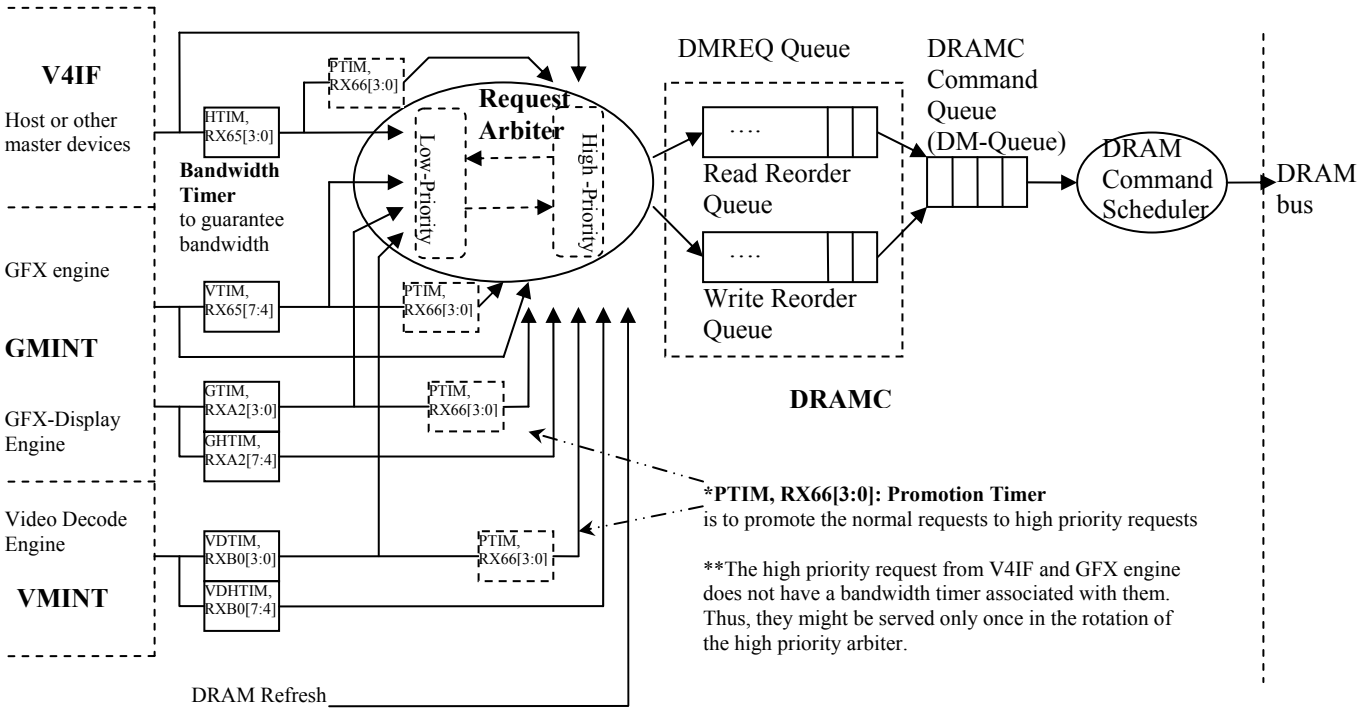


Figure 19. Rx61.1 The Structure of the Request Arbiter, Request Queues and the Command Scheduler in DRAMC

Offset Address: 61h (D0F3)
DRAMC Pipeline Control **Default Value: 04h**

Bit	Attribute	Default	Description
7	RWS	0	**Reorder Queue Size** This bit applied to both Read Reorder Queue and Write Reorder Queue. Please refer to Figure 19. 0: 16 levels. 1: 8 levels.
6	RWS	0	**Reserved**
5	RWS	0	**2T Command Scheduling** This bit controls the internal command request throughput to the command scheduler. Registers bits at RxC4[5:4] and RxC6[2:0] are affected by this bit. 0: 1T 1: 2T
4	RWS	0	**Reserved**
3	RWS	0	**2T Command Scheduling for Non-valid Request Queue** This bit is to improve DRAMC internal timing for DDR2-1066 and above, but may affect performance.
2	RWS	1b	**DRAM Command Path 1T Delay.** This bit adds one T for DRAM command (CS/SCMD/MA) coming out of the DRAM command scheduler to DRAM bus. 0: Disabled. 1: Enabled.
1	RWS	0	**Write Merging for Write Requests.** Write merging had to work with Rx60[2], Rx62[7:4] and Rx62[3:0], please refer to Table 16 for details regarding to write merging behavior. 0: Disabled. 1: Enabled.
0	RWS	0	**Reserved**

Offset Address: 62h (D0F3)
DRAMC Write Merger Control **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RWS	1000b	**Threshold Window to Disable the Write Merging** In order to prevent the consistency problem on Write Reorder Queue and DM-Queue (Figure 19), these bits define a safety window which won't allow write merging to occur at the output end of the Write Reorder Queue. i.e. If there is only a few write requests left in the very front of the Write Reorder Queue, controller might like to let those requests be not merge-able since these writes could anytime be moved to DM-Queue. When a write request comes in or shifts in the Write Reorder Queue, the controller calculates the number of requests already accumulated in front of it and marks it as Merge-able if the number of write in front of it is larger than the number presented by these registers. For detail write merging behavior, please refer to Table 16. 0000: 1 request. 0001: 2 requests. 0010: 3 requests. 0011: 4 requests. …. 1111: 16 requests, i.e. Write Merging won't happen at all.
3:0	RWS	1000b	**Threshold to Stop Write Merging** After being marked as Merge-able, the write request in the Write Reorder Queue can be merged with further coming in write requests if they have the same address. However, if the controller had processed this programmed number of write requests after this write being put to the Write Reorder Queue, this write will be marked as Non-Merge-able. And that write won't be merged again afterwards. For detail write merging behavior, please refer to Table 16. 0000: 0 requests. i.e. No Write Merging will be performed. 0001: 1 requests. 0010: 2 requests. 0011: 3 requests. …. 1111: 15 requests.

Offset Address: 64-63h (D0F3)

DRAMC Reorder Control and Dynamic Clock Control **Default Value: FFFFh**

Bit	Attribute	Default	Description
15:13	RWS	111b	**Maximum Number of Bypass in the Command Queue (DM-Queue)** Please refer to Figure 19, when Rx6D[3] is 0, the requests in the DM-Queue is allowed to be passed. In order to prevent from endless waiting, these bits limit the number of bypasses for the request in the DM-Queue. 000: 0 bypass. i.e. no bypass is allowed. 001: 1 bypass. 010: 2 bypasses. … 111: 7 bypasses. Note: This register particularly applies to the cases when different ranks of accessing happened at the same time. E.g. The request to the second rank could wait forever if there are a bunch of requests to the first rank coming in. This register prevent a potential starvation for this case, it allows the request to the second rank to go out if certain of bypasses happens to it.
12	RWS	1b	**Dynamical Clock Enable for the Control Block for the Refresh Functions** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
11	RWS	1b	**Dynamical Clock Enable for the Clock of the RX Path for the Circuit Macro Besides the IO Pad of MDQS[7:0]P, MDQS[7:0]N, and MD[63:0]** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
10	RWS	1b	**Dynamical Clock Enable for the control block for the MCKE[3:0] and MODT[3:0].** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
9	RWS	1b	**Dynamical Clock Enable for the Control Block for the DRAM Read Cycle** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
8	RWS	1b	**Dynamical Clock Enable for the Control Block for the DRAM Write Cycle** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
7	RWS	1b	**Dynamical Clock Enable for the Control Block for the MCS[3:0]#** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
6	RWS	1b	**Dynamical Clock Enable for the Control Block for MSRAS#, MSCAS#, MSWE#, MBA[2:0] and MA[15:0]** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
5	RWS	1b	**Dynamical Clock Enable for the Read Reorder Queue and Write Reorder Queue** For the Read Reorder Queue and Write Reorder Queue, please refer to Figure 19. 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
4	RWS	1b	**Dynamical Clock Enable for the Input Side of the Data FIFO Associated with Write Reorder Queue** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
3	RWS	1b	**Dynamical Clock Enable for the Output Side of the Data FIFO Associated with Write Reorder Queue** 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
2	RWS	1b	**Dynamical Clock Enable for the DM- Queue** For the DM-Queue, please refer to Figure 19. 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
1	RWS	1b	**Dynamical Clock Enable for the Control Block for the Page Management** There are 32 page tables in the chip, i.e. this chip can support at most 32 opened pages for the DRAM on the DIMM. This register is to control the clock for the controls of these page management. 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).
0	RWS	1b	**Dynamical Clock Enable for the Control Block for the Page Timer** Each Page table (32 tables in all) had a page timer associated with it. The timer expired (expiration time is defined by Rx72[3:0]) to tell the controller to close that opened DRAM page. This register is to control the clock for the logic needed to manage the page timer function. 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be started and stopped automatically (Note).

Note: The clock will be enabled to run (toggle) whenever the control logic detects there are functions needing that clock controlled block to be activated. And the control logic will also let the clock stop (stayed at low) when the related function is finished for that clock controlled block.

DRAM Queue / Arbitration (65–67h)

Offset Address: 65h (D0F3)

DRAM Arbitration Bandwidth Timer - I **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RWS	0	**GFX Bandwidth Timer** Indicates the Time slot allocated for DRAM controller to accept request from internal GFX engine. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the Graphic Engine of the integrated graphic controller can be continuously served for that much of time. Please refer to Figure 19 for the logic location for the bandwidth timer. 0000: 0 DCLK, i.e. if there are other requests in the system, only one request from the GFX can be served before DRAM controller switch to serve others. 0001: 1 x 4 DCLKs. 0010: 2 x 4 DCLKs. … 1111: 15 x 4 DCLKs.
3:0	RWS	0	**Host Bandwidth Timer** Indicates the Time slot allocated for DRAM controller to accept requests from host controller. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the host controller can be continuously served for that much of time. Note that the requests in the host controller include requests from the CPU and other master devices in the system. Please refer to Figure 19 for the logic location for the bandwidth timer. 0000: 0 DCLK, i.e. if there are other requests in the system, only one request from the host controller can be served before DRAM controller switch to serve others. 0001: 1 x 4 DCLKs. 0010: 2 x 4 DCLKs. … 1111: 15 x 4 DCLKs.

Offset Address: 66h (D0F3)

DRAM Queue / Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**DRAMC Command Queue Size Bit 1** This bit sets the size of the DRAMC Command Queue (DM-Queue) for pipelining. **Bits [7:6]:** 0x: 2 levels. 10: 4 levels. 11: 3 levels.
6	RWS	0	**DRAMC Command Queue Size Bit 0** Refer to bit-7 for descriptions.
5:4	RWS	0	**Reserved**
3:0	RWS	0	**Priority Promotion Timer** The DRAM request from Host (or other masters), GFX, GFX-Display, or Video Decoder is promoted to become a high priority request when it is pending over this programmed time. 0000: Promotion Timer is disabled. i.e. No promotion will be done for the reqeusts. 0001: 1 x 4 DCLKs. 0010: 2 x 4 DCLKs. … 1111: 15 x 4 DCLKs. Please refer to Figure 19, note that the request arbiter can arbitrate requests coming in from a lot of sources. It won't process the low priority requests until all the high requests have all been processed. With this priority promotion timer, a normal request from Host, GFX, GFX-Display or Video Decoder can become high priority so that it can be serviced before it is too late. The corresponding normal request timers are at Rx65[7:4], Rx65[3:0], RxA2[3:0] and RxB0[3:0].

Offset Address: 67h (D0F3)

DIMM Command / Address Selection **Default Value: 50h**

Bit	Attribute	Default	Description
7:6	RWS	01b	**Reserved**
5:4	RWS	01b	**Reserved**
3:2	RWS	00b	**DIMM 1 Command / Address Selection** Indicates what command pins for SRAM command (MSRAS#, MSCAS#, MSWE#) and MA are used for the DIMM selected by MCS2# and MCS3#. 00: MSRAS#, MSCAS#, MSWE#, MA[15:0]. 01: Invalid selections. 10: Invalid selections. 11: Invalid selections. This chip had only one set of command pins and MA pins, thus 00B is the only valid selection.
1:0	RWS	00b	**DIMM 0 Command / Address Selection** What command pins for SRAM command (MSRAS#, MSCAS#, MSWE#) and MA are used for the DIMM selected by MCS0# and MCS1#. 00: MSRAS#, MSCAS#, MSWE#, MA[15:0]. 01: Invalid selections. 10: Invalid selections. 11: Invalid selections. This chip had only one set of command pins and MA pins, thus 00b is the only valid selection.

DRAM Page Control (68–69h)

Offset Address: 68h (D0F3)

Write Expiration Timer **Default Value: 3fh**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5:0	RWS	3Fh	**Write Expiration Timer for Write Reorder Queue** Please refer to Figure 19. The DRAM controller always processes the read requests in the Read Reorder Queue first. Once the read request is all served, it will come to serve the write requests in the Write Reorder Queue. When write requests in the Write Reorder Queue being served for more than this number of clocks, the controller will shift to serve the requests in the Read Reorder Queue if there is read request pending. Note that if the system satisfied the condition described at Rx6A[3:0] earlier than this timer expired, the controller will also shift the service to read if there is read pending. Also noted that a DRAM read snoop cycle will force those write requests being hit all flushed out. However, during those time doing write flushing, the expiration timer being programmed with expiration time indicated by these registers is stopped. 00h: 0 DCLK, i.e. the controller will go back to serve read requests, only at most one write request is served. 01h: 1 DCLK. 02h: 2 DCLKs. 03h: 3 DCLKs. …. 3Fh: 63 DCLKs.

Offset Address: 69h (D0F3)

Bank Interleave Control **Default Value: 82h**

Bit	Attribute	Default	Description
7:6	RWS	10b	**Page Number Supported for the Rank.** This bit indicates the most opened pages for one rank. Note that the page table structure of this chip is 8 page registers per rank for 4 ranks. And each page register is used for one bank. Thus, 8 bank device is supported. If there are 8 banks device on the DIMM, and these registers are set as 10b, only 4 of the 8 page registers are used. The other 4 pages (e.g. MBA2=1) are always closed after the accessing. However, if the DIMM only had 4 banks, this register cannot be programmed as 11b. An overwritten of data could happen. i.e. the supported number of banks programmed here must be less or equal to the number of banks supported by the physical DRAM on the DIMM. 00: All the page registers are not used. 01: 2 page registers for each rank are used. Those cycles with {MBA2, MBA1} != 00b will be processed as non-page mode cycles. 10: 4 page registers for each rank are used. Those cycle with MAB2 != 0 will be processed as non-page mode cycles. 11: 8 page registers for each rank are all used. Rx53[3] must be set to 1 in this case.
5	RWS	0	**Bank Address Scramble** Instead of mapping to specific address bits, MBA2, MBA1, MBA0 will be mapped to the Exclusive-OR function of certain address bits of the requesters. Please refer to table Rx52 for more details. 0: Disabled 1: Enabled
4	RWS	0	**Auto-Precharge for CPU Write-Back** This feature enables DRAM controller to close the DRAM page when the request is CPU Write-Back. A CPU write back cycle implies this page won't be accessed too soon. This bit must be 0. 0: Disabled 1: Enabled
3	RWS	0	**Reserved**
2	RWS	0	**High Priority Refresh Request** This bit set the priority of the internal refresh requests. 0: Disabled, Refresh requests will be promoted to high priority only if refresh requests accumulated to 8. 1: Enabled, Refresh requests are always treated as high priority
1	RWS	1b	**Reserved**
0	RWS	0	**Multiple Page Mode** 0: Disabled, DRAM controller and the DRAM DIMM will work in Non-Page mode, i.e. every access of DRAM followed by a pre-charge command. By doing this, it saves DRAM power on the DIMM but degrades the DRAM performance. 1: Enabled, DRAM controller will maintain at most 32 active pages in several banks.

DRAM Miscellaneous Control (6A–6Fh)

Offset Address: 6Ah (D0F3)

DRAMC Request Reorder Control **Default Value: 40h**

Bit	Attribute	Default	Description
7:4	RWS	4h	**Maximum Number of Bypassing Read Requests in Read Reorder Queue** The read request in the Read Reorder Queue can be bypassed in order to achieve maximum DRAM performance. The bypassing criteria could be consideration of Rank, Bank, Page, Priority, etc. This number is the maximum number of bypassing requests can be allowed for a single read in the queue. 0h: 0, i.e. no bypassing is allowed. 1h: 1 read request. 2h: 2 read requests. … Fh: 15 read requests.
3:0	RWS	0h	**Number of Write Requests Left in the Write Reorder Queue** Please refer to Figure 19. The DRAM controller always processes the read requests in the Read Reorder Queue first. Once the read request is all served, it will come to serve the write requests in the Write Reorder Queue. The controller will continue serving the write requests until the request # of writes in the Write Reorder Queue is equal or less than the # indicated by these registers. Note that if the system satisfied the condition described at Rx68[5:0] earlier than the time this chip needed to process the necessary write requests, the controller will also shift the service to read if there is read pending. Also noted that a DRAM read snoop cycle will force those write requests being hit all flushed. 0h: 0 write request. i.e. All the write requests will be flushed. 1h: 1 write request. 2h: 2 write requests. …. Fh: 15 write requests. i.e. Only at most 1 write request is served since there is at most 16 write requests pending in the system.

Offset Address: 6Bh (D0F3)

DRAM Initialization Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RWS	0	**DLL Adjustment for DQS Input** This bit is used to calibrate the chip internal DLL for 1/4T delay on pin MDQS[3:0]N/P. This 1/4 T delay is the timing margin to latch the MD[63:0] when a DRAM read is performed on the DRAM bus. Software sets 1 to this bit to start the calibration, and sets 0 to finish the calibration. 0: Finish the calibration with current adjustment on the DLL. 1: Enable the calibration of the DLL.
6	RWS	0	**Reserved**
5	RWS	0	**DDR3 Memory Reset** Software programs this bit to set the status of MEMRESET# pin. 0: Chip pin MEMRESET# will become low. 1: Chip pin MEMRESET# will become high. For a DDR3 DIMM connected to this chip to work normally, this bit should be programmed to 1 right after the system reset. And the system should not access to the DDR3 within a period of time which is defined by the DDR3 specification.
4	RWS	1b	**DLL Manual Reset** For the DLL used for the 1/4T delay for the MDQS[3:0]N/P, this bit is used to reset that DLL. 0: Reset the DLL. 1: Enable the DLL to work normally. For a manual calibration after the system reset, a possible procedure is as following: a. {Bits [7:4]} = 00 → Reset the DLL. b. {Bits [7:4]} = 01 → Enable the DLL. c. {Bits [7:4]} = 11 → Enable the DQS calibration. d. {Bits [7:4]} = 01 → Finish the calibration.
3	RWS	0	**Enable Memory Size Detection, A32/A16 Swap** When doing the memory size detection, BIOS will need to go beyond 4G boundary when the plugged in DIMM had MA map type being 011b, 110b, and 111b. In order to let the BIOS's accessing stay within 4G for easy detection, this register is used to swap the host address bit 32 and 16. There is bit 33 used for Ma map type = 111b. However, since VX900 Series only supports address up to A32, if there is such case, only half of memory on the DIMM is used. 0: Disabled, A32 and A16 stay at the predefined MA location in the MA tables. 1: Enabled. A32 and A16 swapped their MA location in the MA table when doing memory sizing.
2:0	RWS	000b	**Operation Mode for Software DDR Initialization** When BIOS does DDR initialization, it issues a memory read cycle to each ranks on the DIMM. This bit defines what type of memory command cycle it will appear on the DRAM bus for that read cycle. 000: Read Command, this is the Normal Mode, i.e., after the initialization, BIOS should set these registers to this value for the system to work normally. 001: NOP Command. 010: All-Banks-Precharge Command. 011: MRS (Mode Register Set) Command. (Note) 100: CBR (CAS-before-RAS refresh) Command. 101: NOP Command. 110: Long ZQ Calibration Command. 111: NOP Command. Besides this software based DDR initialization, this chip provides another hardware initialization mechanism. Please refer to RxCC for more details.

Note: For the MRS command, Bank Address and MA Address are needed as the following table shown: MA Address A10 in the design is fixed at A20. BIOS can use the other address bits to do the right configuration for the MRS command. BA[2:0] can be set through programming 011b to Rx53[2:0], 011b to Rx52[6:4] and 011b to Rx52[2:0]. And noted that the MA type (Rx50[7:5], Rx50[4:2]) needed to be programmed as 111b. It is shown on Table 17 below for convenience.

Table 17. Rx6B A Typical MA Mapping for a MRS Command

	BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
MRS Address	19	18	17				14	13	20	12	11	10	9	8	7	6	5	4	3

Offset Address: 6Ch (D0F3)

DRAM Type **Default Value: n0h**

Bit	Attribute	Default	Description
7	RWS	0	**DDR Type Support Bit 1** The corresponding controlling logic of this chip (e.g. burst length) will be adjusted according to the setting of these registers. **Bits [7:6]** 00: Illegal setting. 01: DDR2. 10: DDR3. 11: Illegal setting.
6	RWS	0	**DDR Type Support Bit 0** Refer to bit-7 for descriptions.
5	ROS	dip	**DRAM Pad I/O Voltage** This bit reflect the status of the pin MEMDET. 0: MEMDET is pulled low. It indicates the Memory I/O should be supplied with 1.8V. 1: MEMDET is pulled high. It indicates the Memory I/O should be supplied with 1.5V. For working with DDR3 DRAM, those I/O are mostly operated at Low voltage I/O – 1.5v. For working with DDR2 DRAM, those I/O could be operated at either High voltage I/O (1.8v) or Low voltage I/O (1.5v) I/O.
4	RWS	0	**Reserved**
3	RWS	0	**32 Bit DRAM Data Bus Support** This register is to define the MD bus width. When in 32 bit mode, high 32 bits of the DRAM data could be used for debugging purpose. 0: 64 bit. 1: 32 bit, MD[63:32], MDQS[7:4]P, MDQS[7:4]N, MDQM[7:4] will output some chip internal status.
2:1	RWS	0	**Reserved**
0	RWS	0	**Registered DIMM Support** When this bit is enabled, one more T delay will be expected on the MD bus. 0: Disabled (i.e. supports un-buffered DIMM). 1: Enabled.

Offset Address: 6Dh (D0F3)

In Order Service Control **Default Value: C0h**

Bit	Attribute	Default	Description
7	RWS	1b	**Reserved (Do Not Program)**
6	RWS	1b	**Reserved (Do Not Program)**
5:4	RWS	0	**Reserved (Do Not Program)**
3	RWS	0	**In Order Service for the Requests in the Command Queue** Please refer to Figure 19, this bit is to determine the service order of the requests in the Command Queue (DM-Queue). 0: Disabled, the requests can be served in different order. e.g. Read request could be treated as higher priority and then pass those write requests in front of it. 1: Enabled, the requests will be served in their coming in order.
2	RWS	0	**In Order Service for the Write Request in the Write Reorder Queue.** Please refer to Figure 19, this bit is to determine the service order of the requests in the Write Reorder Queue. 0:Disabled, the write requests in the Write Reorder Queue can be passed. 1:Enabled, the write requests in the Write Reorder Queue will be served in their coming in order.
1:0	RWS	0	**Reserved**

Offset Address: 6Eh (D0F3)

DRAM Data Burst Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RWS	0	**SDRAM Effective Burst Length** This bit indicates how many effective data cycles in the DRAM access. For a 64 bit MD bus, the effective burst length is 1QW * (number of T indicated by this bit) * 2 (double edges for DDR operations). When doing the hardware MRS (RxCC[0]) for the DDR2* (Rx6C[7] =0) initialization, this bit will be read and put to the MA bus for the MRS command. So, before doing the MRS initialization, this bit has to be set. For detail bursting order, please refer to Table 18 and Table 19. 0: The DRAM data occupied 2T. For a 64 bit MD bus, the effective burst length in this case is 4QW. For 32 bit mode (Rx6C[3] = 1), the effective burst length is 2QW. During hardware MRS for DDR2 device, the burst length field for the MR will be filled with 010b. 1: The DRAM data occupied 4T. For a 64 bit MD bus, the effective burst length in this case is 8QW. For 32 bit mode (Rx6C[3]), the effective burst length is 4QW. During hardware MRS for DDR2 device, the burst length field for the MR will be filled with 011b. When working with DDR3 DRAM (Rx6C[7]=1), this bit has to be set to 1.
4	RWS	0	**DDR3 Burst Chop On-The-Fly** Burst Chop is indicated by setting column address MA12 to 0 by this chip when issuing cycles to DRAM on the DIMM. Only DDR3 DIMM supports this feature. When this chip issued a Burst Chop cycle, the second half of the data phase will be removed. For example, for a normal burst write cycle, the data phase could be 4T, however, when MA12 is 0 in the column address, the data phase become only 2T. When doing MRS (RxCC[0]) for the DDR3* (Rx6C[7] =1) initialization, this bit will be read and put to the MA bus for the MRS command. So, before doing the MRS initialization, thib bit has to be set. For detail bursting order, please refer to Table 18 and Table 19. 0: Disabled. No Burst Chop cycle on the DRAM bus. During hardware MRS for DDR3 device, the burst length field for the MR0 will be filled with 00b. 1: Enabled. There will be Burst Chop cycles on the DRAM bus. During hardware MRS for the DDR3 device, the burst length field for the MR0 will be filled with 01b. When working with DDR2 DRAM (Rx6C[7]=0), this bit has to be set to 0.
3	RWS	0	**Write Burst Reordering** This bit defined the data burst ordering for the DRAM cycles. For detail bursting order, please refer to Table 18 and Table 19. 0: Disabled, the burst order of the data depends on the requesters' address[5:3]. 1: Enabled, the burst order would be always linear. When working with DDR2 DRAM (Rx6C[7]=0), this bit has to be 0; When working with DDR3 DRAM (Rx6C[7]=1), this bit has to be 1.
2:0	RWS	0	**Reserved**

Table 18. Rx6E.1 DRAM Data Burst Order for DDR2 (Rx6C[7] = 0)

Rx6E[5] Effective Burst Length	Rx6E[4] Burst Chop On the Fly	Rx6E[3] Write Burst Reordering	R/W	Request Address [5:3]	Data Burst Order on the DRAM bus	Comment
0	-	1	-	---	x,x,x,x	Invalid setting.
0	1	0	-	---	x,x,x,x	Invalid setting.
1	-	1	-	---	x,x,x,x,x,x,x,x	Invalid setting.
1	1	0	-	---	x,x,x,x,x,x,x,x	Invalid setting.
0	0	0	-	-00	0,1,2,3	
0	0	0	-	-01	1,0,3,2	
0	0	0	-	-10	2,3,0,1	
0	0	0	-	-11	3,2,1,0	
1	0	0	-	000	0,1,2,3,4,5,6,7	
1	0	0	-	001	1,0,3,2,5,4,7,6	
1	0	0	-	010	2,3,0,1,6,7,4,5	
1	0	0	-	011	3,2,1,0,7,6,5,4	
1	0	0	-	100	4,5,6,7,0,1,2,3	
1	0	0	-	101	5,4,7,5,1,0,3,2	
1	0	0	-	110	6,7,4,5,2,3,0,1	
1	0	0	-	111	7,6,5,4,3,2,1,0	

Table 19. Rx6E.2 DRAM Data Burst Order for DDR3 (Rx6C[7] = 1)

Rx6E[5] Effective Burst Length	Rx6E[4] Burst Chop On the Fly	Rx6E[3] Write Burst Reordering	R/W	Request Address [5:3]	Data Burst Order on the DRAM bus	Comment
0	-	-	-	---	x,x,x,x,x,x,x,x	Invalid setting.
1	-	0	-	---	x,x,x,x,x,x,x,x	Invalid setting.
1	0	1	W	---	0,1,2,3,4,5,6,7	
1	0	1	R	000	0,1,2,3,4,5,6,7	
1	0	1	R	001	1,2,3,4,5,6,7,0	
1	0	1	R	010	2,3,4,5,6,7,0,1	
1	0	1	R	011	3,4,5,6,7,0,1,2	
1	0	1	R	100	4,5,6,7,0,1,2,3	
1	0	1	R	101	5,6,7,0,1,2,3,4	
1	0	1	R	110	6,7,0,1,2,3,4,5	
1	0	1	R	111	7,0,1,2,3,4,5,6	
1	1	1	W	0--	0,1,2,3,z,z,z,z	
1	1	1	W	1--	4,5,6,7,z,z,z,z	
1	1	1	R	-00	0,1,2,3,x,x,x,x	
1	1	1	R	-01	1,0,3,2,x,x,x,x	
1	1	1	R	-10	2,3,0,1,x,x,x,x	
1	1	1	R	-11	3,2,1,0,x,x,x,x	

Offset Address: 6Fh (D0F3)

Miscellaneous Control **Default Value: 42h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6	RWS	1b	**DRAM Side Input Pointer Non-Return-Zero Mode** This bit should be enabled to avoid from overwritten for the data. Only when chip is doing internal testing, this bit can be set to 0. It should be always set at 1 for normal operation. 0: Disabled. 1: Enabled.
4:2	RWS	0	**Reserved**
1	RWS	1b	**Compact Refresh Mode** This bit is to de-assert MCS[3:0]# for their corresponding ranks without physical DRAM when this chip is doing the DRAM refresh. 0: Disabled. 1: Enabled.
0	RWS	0	**Burst Refresh** There is a refresh timer for DRAM refresh control. This timer starts counting using DCLK whenever the Refresh Counter (defined by RxC7) is programmed to a value other than 0. When the timer expired with the counts defined by Refresh Counter, it issues an internal refresh request. 0: Disabled, the controller will generate refresh request to the DRAM bus for every internal refresh request. 1: Enabled, the controller will accumulate the internal refresh requests to 4 before issuing refresh command on the DRAM bus. i.e. the interval between two refresh commands could be as long as 4 times the time defined by the Refresh Counter.

DRAM Signal Timing Control (70–7Fh)

As shown in the Figure 20 below, those blocks highlighted with grey are the DRAM signal timing control for the receiving and transmitting of DDR2/DDR3 DRAM. There are four of them:

RX Capture Range: 8 register bits are used to control it. It is to control to have an appropriate timing widow to receive the data from the DRAM.

RX DQS Delay: 6 register bits are used to control it. It is to control the delay of the MDQS input which is used to latch the correct MD input into the internal receiving buffers.

TX DQ Delay: 7 register bits are used to control it. It is to control the output delay of the MD.

TX DQS Delay: 7 register bits are used to control it. It is to control the output delay of the MDQS.

The register setting in Rx78~Rx7F in the following section are the settings for these four delay adjustments. Those calibration inherited in the circuits related to these register settings are for DDR3 DRAM. For working with DDR2 DRAM, we used manual setting based on the experience in the system.

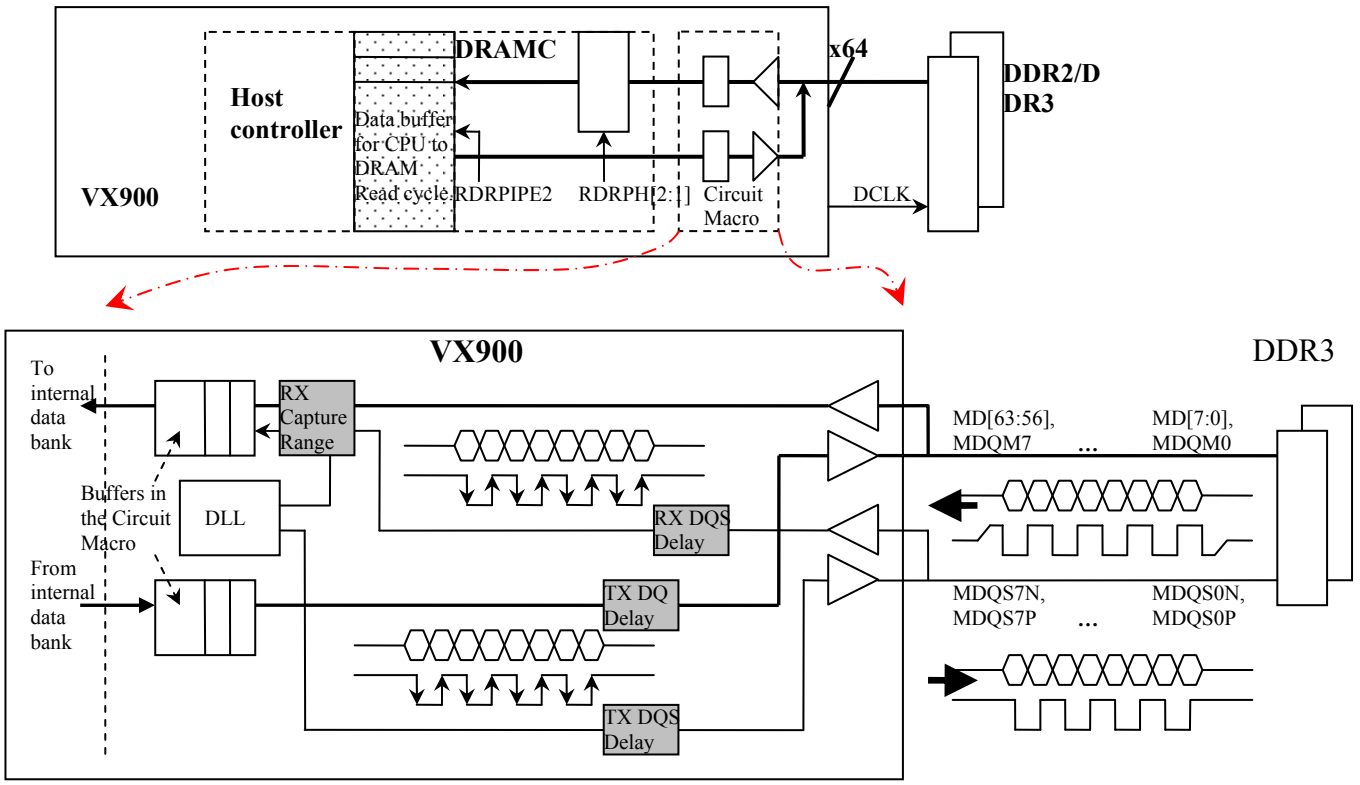


Figure 20. Rx70.1 Timing Control for the DDR3 I/O Receiving and Transmitting

There are 8 sets of such controlling units in the chip, each set is used to control a byte. Rx78 ~ Rx7F are allocated for byte {MD[7:0], MDQM0, MDQS0N/P} ~ {MD[63:56], MDQM7, MDQS7N/P}. Since there are four sets of control bits, to save the register space, this chip implemented a hierarchical register programming scheme to adapt all these four sets of control within a 8 bits register space. Figure 21 to Figure 24 used Rx78 (for MDQ[7:0], MDQM0, and MDQS0N/P) as an example to illustrate this scheme.

In the following few paragraphs, when DRAM read cycles are involved during the calibration, we need to program appropriate value on the Rx74[2:1] to adjust the read latency in order to have the calibration engine to check data at the right time. Noted that the calibration is done on those timing path delay within the circuit macro. But unfortunately, we still need to have the right latency to let the reading scheme to work.

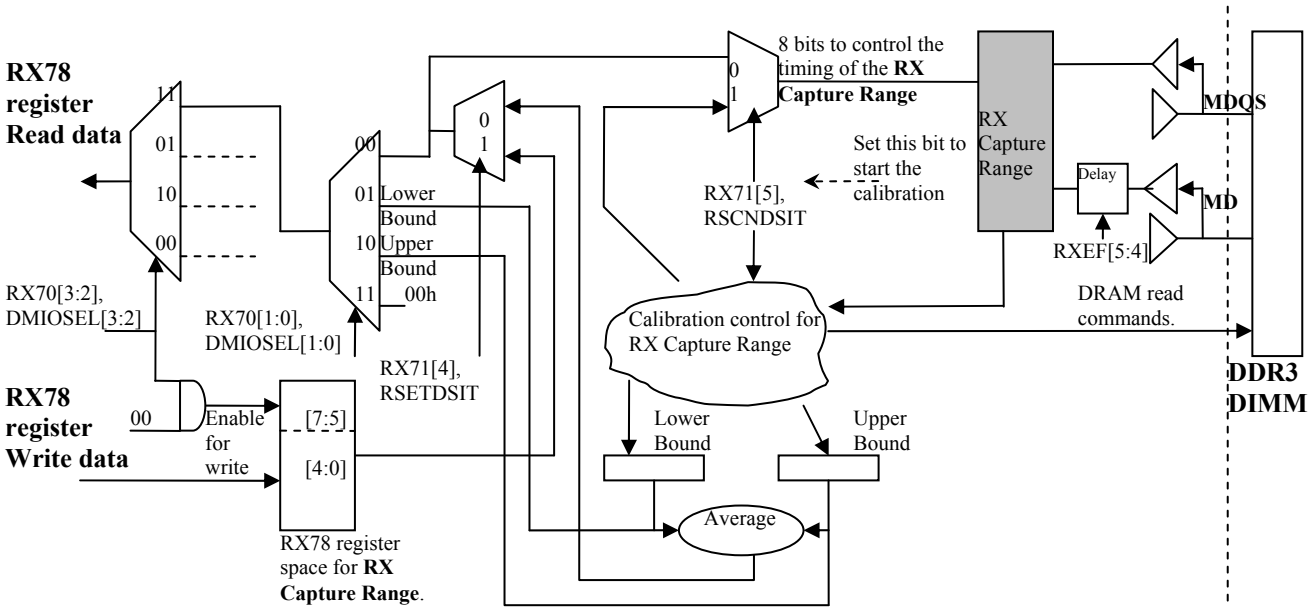


Figure 21. Rx70.2 and Rx78 Related Structure when Rx70[3:2] = 11b, which is to control the setting of RX Capture Range

As shown in the Figure 21, not only manual setting is available, calibration of RX Capture Range can be triggered by setting Rx71[5] to 1. The process started by sending a series of read commands on the DRAM bus with different setting for the RX Capture Range. After a MRS (Mode Register Set) command to put DDR3 in a mode called “Read Leveling Mode”, DDR3 returned the read command with a predefined data pattern either “00h-01h-00h-01h” or “00h-FFh-00h-FFh”. There is no specific definition in the current DDR3 specification for this pattern. So, the working software might need to do the calibration twice. It could triggered the scanning with Rx71[6] set to 1 first. If nothing can be working right, the software trigger the scanning again with Rx71[6] set to 0. The controller thus can check those pattern to verify if the data from DDR3 DIMM is correct or not. The calibration will work from the lowest limit of the setting for the RX Capture Range, it marked the setting for its lower bound when checking is correct. It increased the setting and issued read cycle again and again until checking of the data is incorrect. It then marked the last working setting as the upper bound. Controller also calculated the average of the lower bound and upper bound to have the center of the setting, which presumably the most stable one. Besides this capture range setting, there is another set of delay control for internal MD paths at RxEF[5:4]. However, that one is independent of the calibration mechanism here.

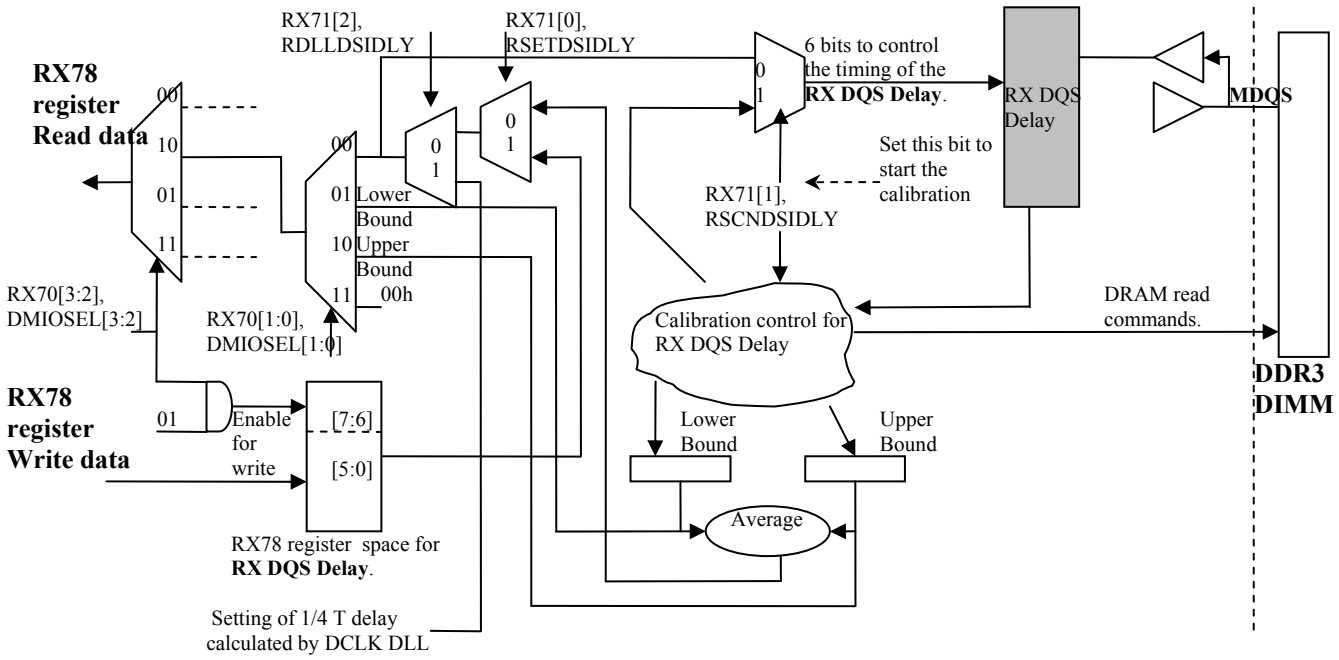


Figure 22. Rx70.3 and Rx78 Related Structure when Rx70[3:2] = 10b, which is to control the setting of RX DQS Delay

The same process is done by setting Rx71[1] to 1 to start the calibration for RX DQS Delay. Besides the manual setting, there is also a setting which is calculated by using internal DCLK DLL to have a 1/4T delay for DQS. Noted that when this option is set (Rx71[2] =1), the DQS of all the bytes (MDQS[7:0]P/N) will use this self-calculated 1/4 delay setting.

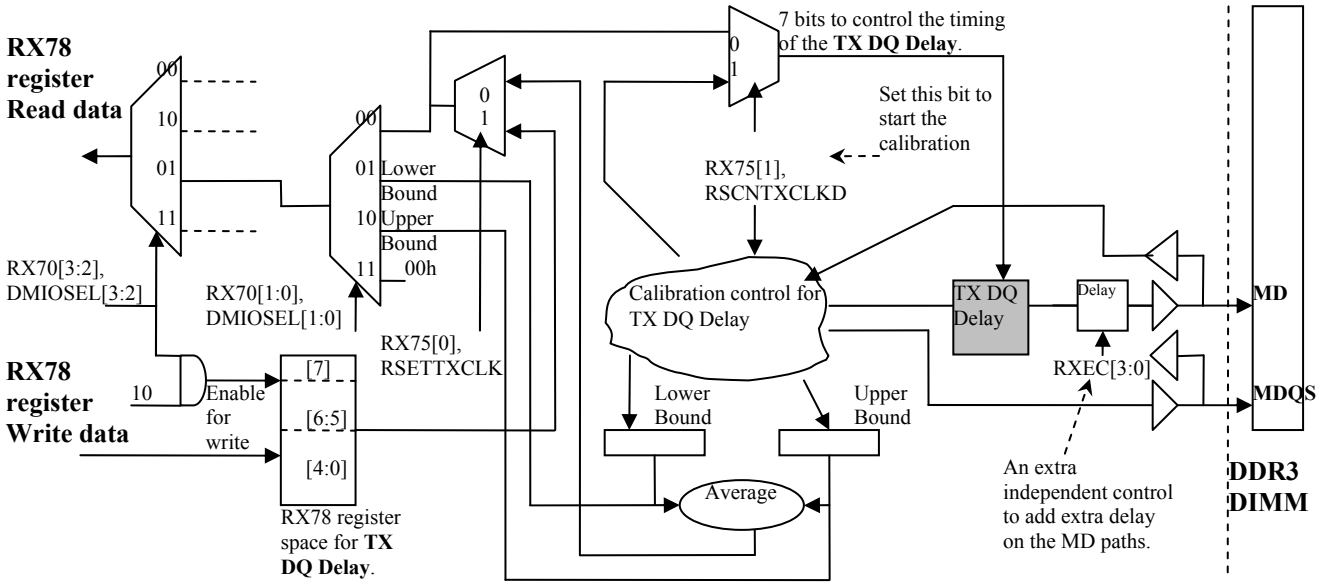


Figure 23. Rx70.4 and Rx78 Related Structure when Rx70[3:2] = 01b, which is to control the setting of TX DQ Delay

The register structure for setting TX DQ Delay is shown on Figure 23. The calibration for TX DQ Delay is started once Rx75[1] is set to 1. That process is to issue a write with data defined by Rx8E[7:0] and to issue a read command right after it to do the checking. Before issuing the write command, the calibration controller will set the setting of TX DQ Delay. It started with the smallest setting, and it will mark the one as lower bound when the corresponding checking is right. It continue with the write + read + checking processes and see if it started to fail. The last working setting is the upper bound. This process will not stop until all the upper bound are found for all the bytes.

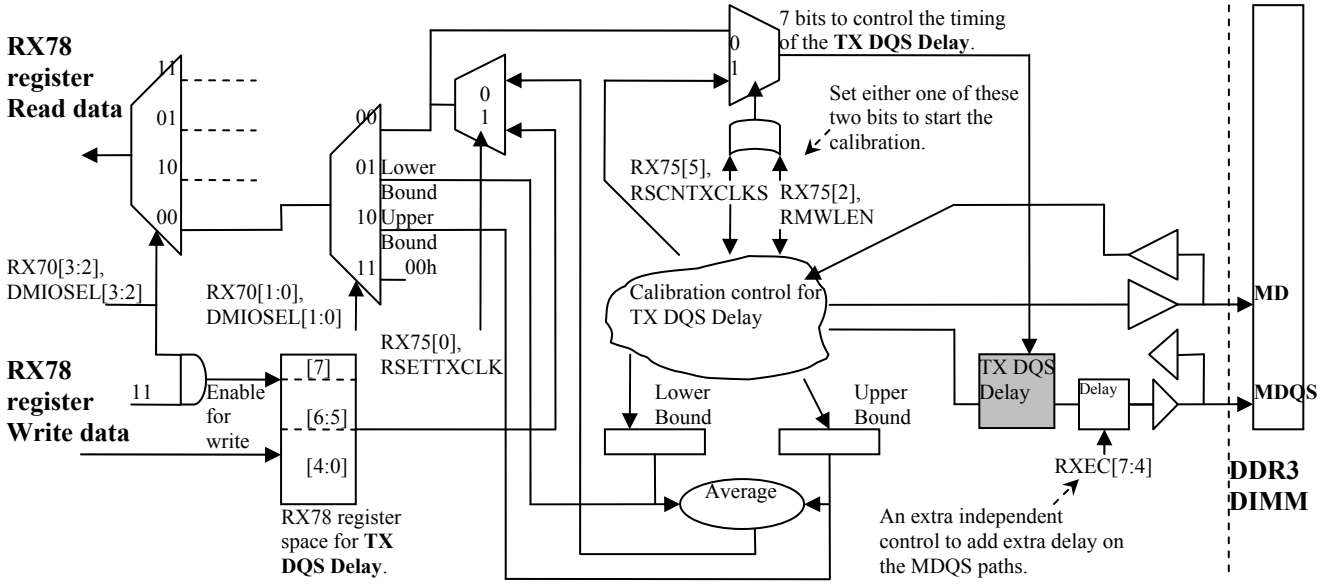


Figure 24. Rx70.5 and Rx78 Related Structure when Rx70[3:2] = 00b, which is to control the setting of TX DQS Delay

The register structure for setting TX DQS Delay is shown on Figure 24. Noted that there are two types of calibration for the TX DQS Delay. Setting Rx75[5] to 1, the calibration process will go as that of TX DQ Delay. Only that the adjustment made is on the TX DQS output path not the TX DQ output path. There is another way of calibration worked with DDR3 DRAM called “Write Leveling”. The procedure would be

1) Set Rx9E[3:2] to select which Rank to do write leveling.
2) Issue MRS commands to each Rank of DRAM to let them know which one is enabled for Write leveling.
3) Set Rx75[2] to 1 to trigger the operation.

After step 3, the controller will adjust the TX DQS delay by one step and send a pulse of DQS out to DRAM. The bit0 of MD of a byte (MD0, MD8, MD16, .. MD57) will return the status (“high” or “low”) of DCLK the selected Rank sensed. The controller will continue adjusting the delay and sending a pulse of MDQS out. This scheme is to detect the MDQS delay against the DCLK’s rising and falling edge. Thus we can know where the lower bound of the TX DQS setting is when the falling edge of DCLK is found, and where the upper bound of the TX DQS setting is when the rising edge of DCLK is found by the DRAM. With the upper bound and lower bound, we can choose the middle point as the setting for the calibration (scan) result.

Offset Address: 70h (D0F3)

IO Timing Control Mode Select **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RWS	0	**Reserved**
3:2	RWS	0	**Content Selection Among Different Delay Paths for Rx78~Rx7F** These two bits determine what the content read from and write to Rx78 ~ Rx7F represents. 00: Setting to control TX DQS Delay. 01: Setting to control TX DQ Delay. 10: Setting to control RX DQS Delay. 11: Setting to control RX Capture Range.
1:0	RWS	0	**Content Selection Among Different Setting for Rx78~Rx7F** These two bits determine what the content read from Rx78~Rx7F represents. Please refer from Figure 21 to Figure 24 for more information on the selections of these bits. 00: Manual setting or average setting of lower and upper bound depending on other register setting for different delay paths. 01: Setting of the lower bound resulted from the calibration. 10: Setting of the upper bound resulted from the calibration. 11: Reserved. The return value of reads to Rx78~Rx7F will always be 00h.

Offset Address: 71h (D0F3)

MD/MDQS Input Timing Control **Default Value: 11h**

Bit	Attribute	Default	Description
7	RWS	0	**DDR3 Read Leveling Enable** When this chip is triggered to do the calibrations for bit-5 (RX Capture Range) and bit-1 (RX DQS Delay) for DDR3 DRAM, this bit is needed to be set to 1 to avoid from dealing with on/off-page, pre-charge, and refresh related logic which is needed for normal DRAM cycles. Please refer to Figure 21 and Figure 22. 0: Disabled. 1: Enabled.
6	RWS	0	**Expected Returned Data Format for Calibration** When this chip is triggered to do the calibrations for bit-5 (RX Capture Range) and bit-1 (RX DQS Delay), or the I/O calibration Rx8C[0], this bit defined the data pattern returned from the DRAM. 0: The controller would expect DQ bytes returned from the DRAM will be in a sequence that a) The first byte (even byte) is from Rx8E[7:0]. b) The odd byte is always the bit-to-bit inversion of the byte in front of it. c) The even byte is one bit shifted to the right of the previous even byte. e.g. 00h-FFh-00h-FFh…. , or 5A-A5-2D-D2-16-E9-0B-F4… 1: The controller would expect DQ bytes returned from the DRAM will be in a sequence of 00h-01h-00h-01h….. When worked with DDR3 DRAM in the Read Leveling mode (RX Capture Range or RX DQS Delay), this bit should be set to 1 for DRAM output DQ1~7 low . For DRAM output DQ1~7 the same value as DQ0 when read leveling mode, set this bit to 0 and Rx8E[7:0] to 0.
5	RW1C	0	**Trigger of Calibration for the RX Capture Range** Set this bit to 1 to start the calibration for RX Capture Range. Please refer to Figure 21 and the paragraph beneath it for more information. 0: Disabled. 1: Enabled.
4	RWS	1b	**Setting for RX Capture Range** Selection of the control bits of RX Capture Range. 0: Use the result of calibration (scan). 1: Use the manual setting on Rx78~Rx7F. Noted that the value in Rx78~Rx7F reflect the setting for RX Capture Range only when Rx70[3:2] is set to 11b. For more information regarding to the setting of RX Capture Range, please refer to Figure 21.
3	RWS	0	**Reserved**
2	RWS	0	**Auto Setting for RX DQS Delay** Internal DLL will automatically generated a setting for a 1/4 T delay for RX DQS Delay. Please refer to bit-0 for more details. 0: Calibration/Manual. 1: DLL 1/4 T delay setting.
1	RW1C	0	**Trigger of Calibration for the RX DQS Delay** Set this bit to 1 to start the calibration for RX DQS Delay. Please refer to Figure 22 and the paragraph beneath it for more information. 0: Disabled. 1: Enabled.
0	RWS	1b	**Setting for RX DQS Delay** Selection of the control bits of RX DQS Delay, it has to work with bit-2: **Bits [2,0]** 00: Use the result of calibration. 01: Use the manual setting on Rx78~Rx7F. Noted that the value in Rx78~Rx7F reflect the setting for RX DQS Delay only when bits[3:2] is set to 10b. 1x: Use the 1/4 T delay DLL calibration result. For more information regarding to the setting of RX DQS Delay, please refer to Figure 22.

Offset Address: 72h (D0F3)

Page Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RWS	0	**Reserved**
3:0	RWS	0	**Expiration Time for the Page Register Life Timer** Each rank of DRAM are associated with 8 page registers, there are total 32 page registers in the design. And each page register is associated with one Page Register Life Timer. Each time a DRAM page is opened, the page is marked as opened. There are at most 8 pages can be opened for one rank. Page is thus closed when it is replaced by other page. This Life Timer is programmed to prevent a page being opened for too long. The setting of these bit represents the time that a page is allowed to remain opened at most. The controller will issue "Pre-charge" command on the DRAM bus to close the DRAM page after the expiration of the Life Timer. 0000: 0 x 16 DCLKs, i.e. the page closed right after it is opened for accessing. 0001: 1 x 16 DCLKs. 0010: 2 x 16 DCLKs. …. 1111: 15 x 16 DCLKs.

Offset Address: 73h (D0F3)

Close All Pages Threshold **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RWS	0	**Reserved**
4:0	RWS	0	**DRAM Expired Page Threshold** The controller will issue "Pre-charge All" command to close all of the pages when the number of expired pages (pages whose associated Life Timer is expired) exceeds this value. Please refer to the register description of Rx72[3:0] for the Page Register Life Timer. 00h: 0 expired page, i.e. whenever there is a expired page, the controller will issue pre-charge all command to close the page. 01h: 1 expired page. 02h: 2 expired pages. … 1Fh: 31 expired pages.

Offset Address: 74h (D0F3)

Read Data Phase Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RWS	1b	**Extend Internal Signals for RX Capture Range (DQS Input Enable)** When set to 1, this bit extend the RX capture range by 1 more T. 0: Disabled. 1: Enabled.
6	RWS	0	**Reserved**
5	RWS	0	**1 More Pipelined Stage on Read Data Path** This bit adds one more T in the path from circuit macro to the internal data buffers for the read data at DRAM read cycles. 0: Disabled. 1: Enabled.
4:3	RWS	0	**Reserved**
2:1	RWS	0	**MD Input Data Push Timing Control** These two bits determine the timing the controller get the first data out of circuit macro and put to the internal read buffers. 00: 1T after the first data coming in. 01: 2T after the first data coming in. 10: 3T after the first data coming in. 11: 4T after the first data coming in. It is suggested to program these two bits as shown in the following table when working with different DCLK's frequency:
0	RWS	0	**Reserved**

Bits [2:1]	DCLK's Frequency
00	200Mhz
01	266Mhz or 333Mhz
10	400Mhz or 533Mhz
11	n/a

Offset Address: 75h (D0F3)
MD/MDQS output Timing Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RW1C	0	**Trigger of Calibration for TX DQS Delay** Set this bit to 1 to start the calibration for TX DQS Delay. Note that there are two types of calibration for TX DQS Delay. This one triggered the calibration using normal write command followed by read command to DRAM bus. Please refer Figure 24 and the paragraph beneath it for more information. 0: Disabled. 1: Enabled.
4	RWS	1b	**Reserved**
3	RWS	0	**Reserved**
2	RW1C	0	**Trigger of Calibration for TX DQS Delay Using Write Leveling** Set this bit to 1 to start the calibration for TX DQS Delay. Note that there are two types of calibration for TX DQS Delay. This one triggered the calibration using DDR3 specific "Write Leveling" method. Please refer to Figure 24 and the paragraph beneath it for more information. 0: Disabled. 1: Enabled.
1	RW1C	0	**Trigger of Calibration for TX DQ Delay.** Set this bit to 1 to start the calibration for TX DQ Delay. Please refer to Figure 23 and the paragraph beneath it for more information. 0: Disabled. 1: Enabled.
0	RWS	1b	**Setting for TX DQS Delay and TX DQ Delay.** Selection of the control bits for both TX DQS Delay and TX DQ Delay. 0: Use the result of calibration. 1: Use the manual setting on Rx78~Rx7F. For TX DQ Delay value, they can be read from Rx78~Rx7F by setting Rx70[3:2] to 01b. For TX DQS Delay value, they can be read from Rx78~Rx7F by setting Rx70[3:2] to 00b. For more information regarding to the setting of TX DQ Delay, please refer to Figure 23; for more information regarding to the setting of TX DQS Delay, please refer to Figure 24.

Offset Address: 76h (D0F3)
Write Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6	RWS	0	**1 More Pipeline for write data between DBX and DRAMC SRAM** This bit adds one more T in write data path between DBX and DRAMC SRAM. 0: Disabled. 1: Enabled.
5	RWS	0	**1 More Pipelined Stage on Write Data Path** This bit adds one more T in the path from internal data buffers to circuit macro for DRAM Write cycles. 0: Disabled. 1: Enabled.
4	RWS	0	**Reserved** Must be set to 0.
3:2	RWS	0	**Early DQ/DQS Output for Write Cycles** This register is for logic core to provide early signals of MD/MDQS transmitted to Circuit Macro to compensate the long delay on the Circuit Macro besides the chip boundary. 00: Normal mode. 01: 1 cycle earlier. 10: 2 cycles earlier. 11: 3 cycles earlier. Since this register is used to compensate the delay in the Circuit Macro, they should be set to the same value as bit[6:5] at Rx78~Rx7F for TX DQ Delay (while Rx70[3:2] = 10b) and for TX DQS Delay (while Rx70[3:2]=11b). Please refer to Figure 23 and Figure 24 for more information. Noted for timing concerned, it should be set 01 or 10 when working with DDR2-667 and above.
1:0	RWS	0	**Reserved**

Offset Address: 77h (D0F3)

MDQS Output Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RWS	0	**Reserved**
4	RWS	0	**DDR3 MDQS Output Preamble** This bit control the behavior of the MDQS[7:0]P/N for the time 1T right before the first strobe of a write cycle. 0: Disabled, the behavior of MDQS[7:0]P/N will be always low/high right before the first strobe. 1: Enabled, the MDQS[7:0]P/N will output to high/low and swing to low/high then go back to high/low for the first effective MDQS for a DDR write cycle. For DDR2, this bit should be always set to 0.
3	RWS	0	**MDQS Earlier Output Enable** This bit is the control bit to enable the MDQS[7:0]P/N output earlier for write cycles. Bits [1:0] defined how much earlier the output enable will be. 0: Disabled. 1: Enabled.
2	RWS	0	**MD 1/2T Earlier Output Enable** This bit enable the output of the MD[63:0] for write cycles by 1/2T earlier. 0: Disabled. 1: Enabled. When this bit is set to 1, register bits[6:5] of Rx78~Rx7F for TX DQ Delay (while Rx70[3:2] is set to 10b) will need to be set as 01b, 10b, or 11b.
1:0	RWS	0	**MDQS Earlier Output Enable Selections** This two bits defined how much earlier the output enable of MDQS[7:0]P/N will be when bit 3 is set to 1. 00: 1/4T earlier 01: 1/2T earlier 10: 3/4T earlier 11: 1T earlier When these bits set to value other than 00b, bits [6:5] at Rx78~Rx7F for TX DQS Delay (while Rx70[3:2] is set to 11b) will need to be set as the following table shown :

Bits [1:0]	Bits [6:5] for TX DQS Delay
00	00 or 01 or 10 or 11
01	01 or 10 or 11
10	01 or 10 or 11
11	10 or 11

Offset Address: 78h (D0F3)

DQ Group 0 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 0 IO Timing Control** Under a hierarchy register structure, this register contained register setting to control RX Capture Range, RX DQS Delay, TX DQ Delay and TX DQS Delay for DQ Group 0: MD[7:0], MDQM0, MDQS0P and MDQS0N. Noted that the internal corresponding registers are allowed to be written only when Rx70[3:2] were programmed to their designated value. Please refer from Figure 20 to Figure 24 for more information. The definition of these bits can be seen in Table 20 below.

Table 20. Rx78.1: Detail Register Descriptions for Rx78

Rx70[3:2]	Definition of Register Rx78
00	The register is to indicate the settings for TX DQS Delay: ***Bit [7]***: Reserved, writing anything to this bit had no effect. ***Bits [6:5]***: The delay of TX DQS. 00: 0T. 01: 1T. 10: 2T. 11: 3T. When this chip worked with 667Mhz or higher frequency DDR2/DDR3, these two bits should be 01b, 10b, or 11b. Rx76[3:2] should be equal to these two bits. ***Bits [4:0]***: Adding 1/32T delay to the timing defined by bit[6:5]. 00h: 0 x 1/32 T. 01h: 1 x 1/32 T. 02h: 2 x 1/32 T. … 1Fh: 31 x 1/32 T. When this register is read back, it could be the manual setting described above, the lower bound, the upper bound, or the average of calibration's result depending on the register setting on Rx70[1:0], please refer to Figure 24 for details.
01	The register is to indicate the setting for TX DQ Delay: ***Bit [7]***: Reserved, writing anything to this bit had no effect. ***Bits [6:5]*:** The delay of TX DQ. 00: 0T. 01: 1T. 10: 2T. 11: 3T. When this chip worked with 667Mhz or higher frequency DDR2/DDR3, these two bits should be 01b, 10b, or 11b. Rx76[3:2] should be equal to these two bits. ***Bits [4:0]***: Adding 1/32T delay to the timing defined by bit[6:5]. 00h: 0 x 1/32 T. 01h: 1 x 1/32 T. 02h: 2 x 1/32 T. … 1Fh: 31 x 1/32 T. When this register is read back, it could be the manual setting described above, the lower bound, the upper bound, or the average of calibration's result depending on the register setting on Rx70[1:0]], please refer to Figure 23 for details.
10	The register is to indicate the setting for RX DQS Delay: ***Bits [7:6]***: Reserved, writing anything to these bits had no effect. ***Bits [5:0]***: adding delay to the receiving DQS paths by: 00h: 450ps delay. 01h: 450ps + 1x30 ps delay. 02h: 450ps + 2x30 ps delay. … 3Fh: 450ps + 63x30 ps delay. *The number is based on worst case, it could be 50% at best case. When this register is read back, it could be the manual setting described above, the lower bound, the upper bound, or the average of calibration's result depending on the register setting on Rx70[1:0], please refer to Figure 22 for details.

11	The register is to indicate the setting for RX Capture Range: ***Bits [7:5]***: Capturing of the receiving signals (MD/MDQS) started from: 000: 1T prior to 1st rising edge of MDQS0P. 001: 1st rising edge of MDQS0P. 010: 1T after the 1st rising edge of MDQS0P. 011: 2T after the 1st rising edge of MDQS0P. 100: 3T after the 1st rising edge of MDQS0P. 101: 4T after the 1st rising edge of MDQS0P. 110: 5T after the 1st rising edge of MDQS0P. 111: 6T after the 1st rising edge of MDQS0P. ***Bits [4:0]***: Adding 1/32T delay to the timing defined by bits [7:5]. 00h: 0 x 1/32 T delay. 01h: 1 x 1/32 T delay. 02h: 2 x 1/32 T delay. … 1Fh: 31 x 1/32 T delay. When this register is read back, it could be the manual setting described above, the lower bound, the upper bound, or the average of calibration's result depending on the register setting on Rx70[1:0], please refer to Figure 21 for details.

Offset Address: 79h (D0F3)
DQ Group 1 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 1 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 1: MD[15:8], MDQM1, MDQS1P and MDQS1N. Please refer to Rx78 for register descriptions.

Offset Address: 7Ah (D0F3)
DQ Group 2 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 2 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 2: MD[23:16], MDQM2, MDQS2P and MDQS2N. Please refer to Rx78 for register descriptions.

Offset Address: 7Bh (D0F3)
DQ Group 3 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 3 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 3: MD[31:24], MDQM3, MDQS3P and MDQS3N. Please refer to Rx78 for register descriptions.

Offset Address: 7Ch (D0F3)
DQ Group 4 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 4 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 4: MD[39:32], MDQM4, MDQS4P and MDQS4N. Please refer to Rx78 for register descriptions.

Offset Address: 7Dh (D0F3)
DQ Group 5 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 5 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 5: MD[47:40], MDQM5, MDQS5P and MDQS5N. Please refer to Rx78 for register descriptions.

Offset Address: 7Eh (D0F3)
DQ Group 6 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 6 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 6: MD[55:48], MDQM6, MDQS6P and MDQS6N. Please refer to Rx78 for register descriptions.

Offset Address: 7Fh (D0F3)
DQ Group 7 IO Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/RW	0	**DQ Group 7 IO Timing Control** These registers have the same meaning as those at Rx78. Only that these registers defined those for DQ Group 7: MD[63:56], MDQM7, MDQS7P and MDQS7N. Please refer to Rx78 for register descriptions.

Shadow RAM Control (80–83h)

Offset Address: 80h (D0F3)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	00b	**CC000-CFFFFh Memory Space Access Control** When enabled, the cycles with address CC000~CFFFFh coming from the host side or other master devices will be forwarded to DRAM. When disabled, the cycles will be forwarded to 33Mhz PCI bus and then to the ROM on the LPC bus. 00: Read and Write access are both disabled. I.e. Both read and write cycles are directed to LPC ROM. 01: Read is disabled and Write is Enabled. I.e. Read cycles are directed to LPC ROM, and write cycles are directed to DRAM. 10: Read is enabled and Write is disabled. I.e. Read cycles are directed to DRAM, and write cycles are directed to LPC ROM. 11: Read and Write accesses are both enabled. I.e. Both read and write cycles are directed to DRAM.
5:4	RWS	00b	**C8000-CBFFFh Memory Space Access Control** The meaning of these bits have the same function as those described at bits [7:6], only that they are applied to cycles with address C8000~CBFFFh.
3:2	RWS	00b	**C4000-C7FFFh Memory Space Access Control** The meaning of these bits have the same function as those described at bits [7:6], only that they are applied to cycles with address C4000~C7FFFh.
1:0	RWS	00b	**C0000-C3FFFh Memory Space Access Control** The meaning of these bits have the same function as those described at bits [7:6], only that they are applied to cycles with address C0000~C3FFFh.

Offset Address: 81h (D0F3)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	00b	**DC000-DFFFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address DC000~DFFFFh.
5:4	RWS	00b	**D8000-DBFFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address D8000~DBFFFh.
3:2	RWS	00b	**D4000-D7FFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address D4000~D7FFFh.
1:0	RWS	00b	**D0000-D3FFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address D0000~D3FFFh.

Offset Address: 82h (D0F3)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	00b	**EC000-EFFFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address EC000~EFFFFh.
5:4	RWS	00b	**E8000-EBFFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address E8000~EBFFFh.
3:2	RWS	00b	**E4000-E7FFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address E4000~E7FFFh.
1:0	RWS	00b	**E0000-E3FFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address E0000~E3FFFh.

Offset Address: 83h (D0F3)

Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5:4	RWS	00b	**F0000-FFFFFh Memory Space Access Control** The meaning of these bits have the same function as those described at Rx80[7:6], only that they are applied to cycles with address F0000~FFFFFh.
3:2	RWS	00b	**Memory Hole** These bits define an address space so that cycles with address targeted to this space will not be forwarded to DRAM, instead, they will be forwarded to PCI bus or LPC bus. 00: None. Cycles with address range at either 80000h~9FFFFh or E0_0000h~FF_FFFFh will be forwarded to DRAM. 01: 512K – 640K, Cycles with address range at 80000h~9FFFFh will be forwarded to PCI or LPC bus. Those at E0_0000h~FF_FFFFh will be forwarded to DRAM. 10: 15M – 16M (1M), Cycles with address range at either 80000h~9FFFFh or E0_0000h~EF_FFFFh will be forwarded to DRAM. Those at F0_0000h~FF_FFFFh will be forwarded to PCI or LPC bus. 11: 14M – 16M (2M), Cycles with address range at 80000h~9FFFFh will be forwarded to DRAM. Those at E0_0000h~FF_FFFFh will be forwarded to PCI or LPC bus.
1	RWS	0	**SMRAM (A0000~BFFFFh) Data Cycles Access in SM Mode** This bit defined the destination of the CPU cycles with data read/write accessing A0000~BFFFFh in SM mode (System Management Mode). 0: Cycles are forwarded to the DRAM. 1: Cycles are forwarded to the PCI bus or other devices in the system. This bit is effective when bit-0 is set to 0. i.e. if bit-0 is 1, all the accessing are forwarded to DRAM. SMRAM Code R/W cycles are always forwarded to DRAM.
0	RWS	0	**SMRAM (A0000~BFFFFh) Cycles Access in Normal Mode** This bit defined the destination of CPU cycles with address accessing to A0000~BFFFFh in normal mode (not in SMM). 0: Cycles could be forwarded to DRAM, PCI bus or other devices in the system depending on the setting of bit-1, the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycles. 1: Cycles (Code and Data) are always forwarded to DRAM.

DRAM Above 4G Support (84-8Bh)

Offset Address: 85-84h (D0F3)

Low Top Address **Default Value: FF01h**

Bit	Attribute	Default	Description
15:4	RWS	FF0h	**Low Top Address - A[31:20]** No matter whether DRAM's size is larger than 4G or not, these bits defined the upper limit of the address space under 4G that the system can use as the system memory. i.e. If the highest address under 4G that the cycles from CPU or other master devices in the system can be directed to DRAM is HIGH_A[31:20], these bits defined the Low Top Address = HIGH_A[31:20] +1. Noted that Low Top Address can be lower than or equal to the real physical DRAM top which defined by Ending Address (Rx48~Rx4F). It cannot be larger than the Ending Address. 000h~3FFh: Invalid setting, the system cannot work with this setting. 400h: This defined 1G bytes of DRAM under 4G as the system memory. 401h: This defined 1G + 1 bytes of DRAM under 4G as the system memory. … 800h: This defined 2G bytes of DRAM under 4G as the system memory. 801h: This defined 2G + 1 bytes of DRAM under 4G as the system memory. … C00h: This defined 3G bytes of DRAM under 4G as the system memory. C01h: This defined 3G + 1 bytes of DRAM under 4G as the system memory. … FC0h: This defined 4G – 64M of DRAM space under 4G to be used as the system memory. FC1h ~ FFFh: Invalid setting. The address in between FF00_0000h and FFFF_FFFFh are reserved for System Hardware Address Space which is address space right under 4G. And the address FC10_0000h ~ FEFF_FFFFh are reserved for some system hardware to use.
3:1	RWS	0	**Reserved**
0	RWS	1b	**On Board Decode Method Selection** This bit determines the method used in the host controller to decode the addressing for DRAM cycles. It becomes valid only when the ending address of the system is larger than 4G. For the system to work correctly, this bit should be set to 1. 0: The host controller will direct cycles to DRAM if the address is lower than the Low Top Address[31:20] which is defined in bits [15:4]. 1: The host controller will direct cycles to DRAM if the address is lower than ({Low Top Address[31:20]} – {Frame buffer size, RxA1[6:4]})

Table 21. Rx84.1 On Board Decoding for Rx84[0]

CPU's Coming Address, X	System Memory Size, Rx89-88[10:0]	Rx84[0]	Chipset Decode for DRAM Cycles
<= 4G (FFFF_FFFFh)	> 4G	0	If X >= Rx84[15:4], then send to PCI If X < RLOWTOPA then send to DRAM
<= 4G (FFFF_FFFFh)	> 4G	1	If X >= (Rx84[15:4] - FB_size (*1)) then send to PCI If X < (Rx84[15:4] - FB_size) then send to DRAM
<= 4G (FFFF_FFFFh)	<=4G (1_00h)	-	If X >= (REND7 - FB_size) then send to PCI If X < (REND7 - FB_size) then send to DRAM
> 4G	> 4G	-	If X >= REND7 then send to PCI If X < REND7 then send to DRAM
> 4G	<=4G (1_00h)	-	send to PCI

Note: FB_size is provided in RxA1[6:4].

Offset Address: 86h (D0F3)
SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Top SM Memory Size** For SM mode, these two bits defined the size of the memory at the top of the memory. They are activated only when bit-2 is 1. 00: 1M. 01: 2M. 10: 4M. 11: 8M.
5	RWS	0	**APIC Lowest Interrupt Arbitration** With the destination redirection mechanism, host controller is able to redirect the MSI requests to the CPU with lowest task priority. When the requested MSI had Destination Mode = 1 (logical) and Delivery Mode = 001 (Lowest Priority), with the enable of this bit, this chip is able to change the destination ID to the CPU with lowest priority. 0: Disabled, MSI cycle is directed with the original assigned CPU. 1: Enabled, MSI cycle can be redirected to the CPU with lowest priority.
4:3	RWS	0	**Reserved**
2	RWS	0	**Top SM Memory Enable** This bit is the enable bit for the SM Memory at the top of the memory to be activated. When this bit is enabled, the memory with size defined by bits [7:6] will be deducted from the top of the system memory and be used for SM mode. 0: Disabled. 1: Enabled.
1	RWS	0	**Reserved**
0	RWS	1b	**Compatible SMM Enable** Conventional SM Memory (rather than the Top SMM defined at bits [7:6]) are defined at A_0000h ~ B_FFFFh. If this bit is enabled, cycles within that address can be directed to DRAM. There are also other register options at Rx83[1] and Rx83[0] needed to work together. 0: Disabled. 1: Enabled.

Offset Address: 87h (D0F3) – Reserved

Offset Address: 89-88h (D0F3)
DRAM Ending Address **Default Value:0nnnh**

Bit	Attribute	Default	Description
15:11	RWS	0	**Reserved**
10:0	RO	HwInit	**The Address Next to the Last Valid DRAM Address** These registers report the maximum of Rx40 ~ Rx43. It indicates the upper bound of the physical DRAM the chip connected. Bits [10,1:0] are all 0. 0_00: N/A. 0_04: 64 M. 0_08: 128 M. 0_0C: 192 M. 0_10: 256M. … 1_00: 4G. 1_04: 4G + 64M. … 2_00: 8G. 2_04 ~ 7_FC: Invalid, This chip had address bits up to A32, only 8G of memory can be supported.

Offset Address: 8A-8Bh (D0F3) – Reserved

DRAM Test Pattern Control (8C-8Fh)

Offset Address: 8D-8Ch (D0F3)

Address for I/O Calibration **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RWS	0	**Address of I/O Calibration** These register bits store the Address[31:20] used for IO timing calibration when triggered by Rx75[5], Rx75[1], bit-1 or bit-0. Note that when this I/O calibration is triggered, eight consecutive 8 QW cycles are issued.
3	RWS	0	**Reserved**
2	RWS	0	**MDQM toggle on Memory Write for I/O Calibration** This bit determines the behavior of MDQM[7:0] on the write cycles at the I/O timing calibration cycles. 0: When bit-1 is triggered, the MDQM[7:0] for the write cycles will all be de-asserted, 00h. 1: When bit-1 is triggered, the MDQM[7:0] for the write cycles will be asserted on odd QW. i.e. the MDQM[7:0] for that 8 QW cycles would be like 00-FF-00-FF-00-FF-00-FF.
1	RWS	0	**Trigger Memory Write Cycle** This bit triggered the I/O timing calibration (Note) for write cycles. When this bit is programmed to 1, eight consecutive 8 QW write cycles are issued with starting address set at bits [15:4]. And the write data pattern is constructed with the following rules: a) The first byte (even byte) is from Rx8E[7:0]. b) The odd byte is always the bit-to-bit inversion of the bytes in front of it. c) The even byte is one bit shifted to the right from the previous even byte. E.g. If the data in Rx8E is 5Ah, those data this chip output to the bus would be 5A-A5-2D-D2-16-E9-0B-F4 for every bytes. Software need to program this bit to 0 and 1 again to trigger another eight consecutive 8 QW write cycles. 0: Disabled. 1: Enabled.
0	RWS	0	**Trigger Memory Read Cycle** This bit triggered the I/O timing calibration*1 for read cycles. When this bit is programmed to 1, eight consecutive 8 QW read cycles are issued with starting address set at bits [15:4]. The read back data is checked against with those programmed at Rx8E[7:0]. Note that the data pattern expected to be check against with is in a fashion that a) The first byte (even byte) is from Rx8E[7:0]. b) The odd byte is always the bit-to-bit inversion of the bytes in front of it. c) The even byte is one bit shifted to the right from the previous even byte. Software need to program this bit to 0 and 1 again to trigger another eight consecutive 8 QW read cycles. 0: Disabled. 1: Enabled.

Note: After setting internal ODT (RxD0) driving, output (RxE0~RxE8) driving, and timing at RxEC~RxEE, one can trigger this register to observe the performance of the I/O timing for DRAM write/read cycles.

Offset Address: 8Eh (D0F3)

DQ Data Pattern for I/O Calibration **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RWS	0	**I/O Calibration Data Pattern** These register bits store the data pattern used for I/O timing calibration when triggered by Rx71[5], Rx71[1], Rx75[5], Rx75[1], Rx8C[0], or Rx8C[1]. When it is a read cycle, this data byte provided the first data pattern to be checked against. When it is a write cycle, this data byte provided the first data pattern to be put on the MD bus. When Rx71[7] is programmed to 1, this chip is in "Read Leveling Mode". The controller would expect the data pattern returned from DDR3 could be 00-01-00-01.. or 00-FF-00-FF.. For chip doing the calibration for DDR3 using read leveling, it is necessary to try both pattern. Rx71[6] needed to be set as 1 to define the data pattern as "00-01-00-01.." and set as 0 to define the data pattern as "00-FF-00-FF..". In either case, these register bits must be programmed as 00h.

Offset Address: 8Fh (D0F3) – Reserved

DRAM Clocking Control (90-9Bh)

Offset Address: 90h (D0F3)

DRAM Clock Operation Mode and Frequency **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RWS	0	**DRAM PLL Output Clock/VCO Control** 0: PLL output clock is divided by 2 from VCO, output clock duty may be better. 1: PLL output clock frequency is the same as VCO.
4	RWS	0	**Reserved**
3:0	RWS	0000b	**DRAM Operating Frequency** These bits define the operation frequency of this DRAM controller or the frequency of DCLK. This chip uses Rx6C[5] to decide if the Memory I/O of this chip is operating at 1.8V or 1.5V. ***If it is 1.8V, Rx6C[5]=0***: 0000: 266 MHz. 0001: Illegal Setting. 0010: Illegal Setting. 0011: Illegal Setting. 0100: 266 MHz. 0101: 333 Mhz. 0110: 400 MHz. 0111: 533 Mhz. 1000: Illegal Setting. 1001: Illegal Setting. 1010: Illegal Setting. 1011: Illegal Setting. 1100: Illegal Setting. 1101: Illegal Setting. 1110: Illegal Setting. 1111: 0 Mhz, PLL Resetted. ***If it is 1.5V, Rx6C[5]=1***: 0000: 400 MHz. 0001: Illegal Setting. 0010: Illegal Setting. 0011: Illegal Setting. 0100: 266 MHz. 0101: 333 Mhz. 0110: 400 MHz. 0111: 533 Mhz. 1000: Illegal Setting. 1001: Illegal Setting. 1010: Illegal Setting. 1011: Illegal Setting. 1100: Illegal Setting. 1101: Illegal Setting. 1110: Illegal Setting. 1111: 0 Mhz, PLL Resetted. To change the DRAM frequency, it is required to set this bits to 1111b to reset the PLL first and set to the target value then. Minimum assertion time for the PLL Reset is 10ns.

Offset Address: 91h (D0F3)

MCLKO Output Phase Delay - I **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RWS	0	**Reserved**
4:0	RWS	0	**MCLKO Phase Select for DIMM0** These registers determine the delay of DRAM clock pin pairs MCLKO[2:0]P/N against the internal DCLK whose frequency is determined at Rx90[3:0]. 00h: No delay, i.e. MCLKO[2:0]P/N are synchronous to internal DCLK. 01h: 1 x 1/32 T of DCLK. 02h: 2 x 1/32 T of DCLK. .. 1Fh: 31 x 1/32 T of DCLK. Note that the synchronization is done within the chip, there could be I/O delay needed to be added on the MCLKO[2:0]P/N pins.

Offset Address: 92h (D0F3)
MCLKO Output Phase Delay - II **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RWS	0	**Reserved**
4:0	RWS	0	**MCLKO Phase Select for DIMM1** These registers determine the delay of DRAM clock pin pairs MCLKO[5:3]P/N against the internal DCLK whose frequency is determined at Rx90[3:0]. 00h: No delay, i.e. MCLKO[5:3]P/N are synchronous to internal DCLK. 01h: 1 x 1/32 T of DCLK. 02h: 2 x 1/32 T of DCLK. … 1Fh: 31 x 1/32 T of DCLK. Note that the synchronization is done within the chip, there could be I/O delay needed to be added on the MCLKO[2:0]P/N pins.

Offset Address: 94-93h (D0F3)
CS/CKE Output Phase Delay **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RWS	0	**Reserved**
4:0	RWS	0	**Phase Select for CS/CKE** These registers determine the delay of MCS[3:0]#, MCKE[3:0] against the internal DRAM Controller's clock - DCLK. 00h: No delay, i.e. the signal mentioned are synchronous to internal DCLK. 01h: 1 x 1/32 T of DCLK. 02h: 2 x 1/32 T of DCLK. … 1Fh: 31 x 1/32 T of DCLK. Note that the synchronization is done within the chip, there could be I/O delay needed to be added on the MCS[3:0]# and MCKE[3:0] pins.

Offset Address: 96-95h (D0F3)
SCMD/MA Output Phase Delay **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RWS	0	**Reserved**
4:0	RWS	0	**Phase Select for SCMD/MA** These registers determine the delay of MSCAS#, MSRAS#, MSWE#, MA[15:0], MBA[2:0] against the internal DRAM Controller's clock - DCLK. 00h: No delay, i.e. the signals mentioned are synchronous to internal DCLK. 01h: 1 x 1/32 T of DCLK. 02h: 2 x 1/32 T of DCLK. … 1Fh: 31 x 1/32 T of DCLK. *Note that the synchronization is done within the chip, there could be I/O delay needed to be added on the pins mentioned above.

Offset Address: 97h (D0F3)

By-Rank Self Refresh Related Registers - I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**MODT Constraint for Entering and Exiting By-Rank Self Refresh** When By-Rank Self Refresh is enabled (bits [3:0]), the DRAM in that Rank is allowed to go to Self Refresh mode as long as the conditions given by the registers (bits [6:4] and Rx98) are met. With this bit turned on, the system will also check the setting for the MODT assignment (programmed at Rx9C) when entering or exiting the self refresh mode. For example, if Rx9C[7:6] = 00b, the MODT0 provides the termination for accessing Rank3. Thus, even if the condition for Rank0 to go to self-refresh is met, the controller will need to wait for Rank3 to be idle to let both Rank0 and Rank3 enter Self Refresh mode. When exiting Self Refresh mode with the accessing to Rank3, Rank0 is also needed to be waken (exiting Self Refresh mode) since MODT0 is needed to provide the termination for accessing Rank3. If Rx9C[5:4] is also programmed as 00b, the controller will also need to wait for Rank2 to be idle to let Rank0, Rank2, and Rank3 to go to Self Refresh mode at the same time. There is another bit at Rx9A[7], when activated, is allowed only to check the pairing relationship when exiting the self refresh mode. We will put them together here: **{Bit[7], Rx9A[7]}** 00: Disabled, the controller gives self refresh commands to individual Rank on conditions given by bits [6:4] and Rx98. 01: Enabled for exiting Self Refresh mode together. Not only the conditions given by bits [6:4] and Rx98, the idle condition of Ranks indicated by MODT assignment programmed at Rx9C had to be met in order for this controller to give commands to let Ranks to exit Self Refresh mode. 1x : Enabled for entering and exiting Self Refresh mode together. Not only the conditions given by bits [6:4] and Rx98, the idle condition of Ranks indicated by MODT assignment programmed at Rx9C had to be met in order for this controller to give commands to let Ranks to enter and exit Self Refresh mode. For best signal integrity concern, when working at DDR3 system (Rx6C[7] = 1), it is recommended to set these bits either at 01 or 1x. When working at DDR2 system (Rx6C[7] = 0), it is recommended to set these bits either at 01 or 1x if the operating frequency is 800Mhz (400Mhz DCLK) and above.
6:4	RWS	0	**The Number of Auto-Refresh while Rank is Idle to Trigger Self Refresh** Auto-Refresh commands were sent to DRAM when chip internal refresh request is generated (counted by RxC7) to tell DDR to do refresh. A Self Refresh Command to DRAM will put DDR DRAM into a mode that the DDR can do the refresh by itself (without auto-refresh command from controller). In self refresh mode, DDR even does not need the clock MCLKO to toggle such that more power saving can be achieved. These bits defined the number of auto-refresh during which the corresponding Rank had been always idle. If the number of auto-refresh happened in such a long period that the rank has been always idle, this chip is able to let the associated ranks to go into Self Refresh mode. The rank enable bit to do the self refresh is defined at bits [3:0]. Besides this auto refresh condition, Rx98 is also defined another two conditions to let the rank to go into self refresh mode. 000: 1 auto refresh. 100: 5 auto refreshes. 001: 2 auto refreshes. 101: 6 auto refreshes. 010: 3 auto refreshes. 110: 7 auto refreshes. 011: 4 auto refreshes. 111: 8 auto refreshes.
3	RWS	0	**By-Rank Self Refresh for Rank 3** If this bit is 1, this chip is allowed to issue Self Refresh command to Rank 3. The condition of doing self refresh for Rank 3 depends on the idle period measured by the happening of internal refresh requests (bits [6:4]), the vertical blank period from GFX(Rx98[7]), and the idle condition determined by the Power Management Unit (Rx98[6]) in the chip. 0: Disabled. 1: Enabled.
2	RWS	0	**By-Rank Self Refresh for Rank 2** If this bit is 1, this chip is allowed to issue Self Refresh command to Rank 2. The condition of doing self refresh for Rank 2 depends on the idle period measured by the happening of internal refresh requests (bits [6:4]), the vertical blank period from GFX(Rx98[5]), and the idle condition determined by the Power Management Unit (Rx98[4]) in the chip. 0: Disabled. 1: Enabled.
1	RWS	0	**By-Rank Self Refresh for Rank 1** If this bit is 1, this chip is allowed to issue Self Refresh command to Rank 1. The condition of doing self refresh for Rank 1 depends on the idle period measured by the happening of internal refresh requests (bits [6:4]), the vertical blank period from GFX(Rx98[3]), and the idle condition determined by the Power Management Unit (Rx98[2]) in the chip. 0: Disabled. 1: Enabled.
0	RWS	0	**By-Rank Self Refresh for Rank 0** If this bit is 1, this chip is allowed to issue Self Refresh command to Rank 0. The condition of doing self refresh for Rank 0 depends on the idle period measured by the happening of internal refresh requests (bits [6:4]), the vertical blank period from GFX(Rx98[1]), and the idle condition determined by the Power Management Unit (Rx98[0]) in the chip. 0: Disabled. 1: Enabled.

Offset Address: 98h (D0F3)

By-Rank Self Refresh Related Registers - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Check Vertical Blank of GFX for Rank3 to do By-Rank Self Refresh** When Rx97[3] =1, this chip is allowed to send self refresh command to Rank3 to let it do the self refresh. Besides the idle time defined by Rx97[6:4] and the C3/C4 status defined by bit-6, an extra condition is defined in this bit: 0: The controller is allowed to send the self refresh command to Rank3 regardless if it is the time of vertical blanking (Note) in the GFX (Graphic Controller). 1: The controller will need to check if it is the time that vertical blanking is occurring on the GFX. If it is not the vertical blanking period (Note), the chip won't allowed the Rank3 of DRAM to go into self refresh mode; It is very possible that the GFX will need data from DRAM soon. If it is vertical blanking period, it is safe to enter the self refresh since there will be a significant of time that the system probably won't need data.
6	RWS	0	**Check C3/C4 State of PMU for Rank3 to do By-Rank Self Refresh** When Rx97[3] =1, this chip is allowed to send self refresh command to Rank3 to let it do the self refresh. Besides the idle time defined by Rx97[6:4] and the vertical blanking period defined by bit-7, an extra condition is defined in this bit: 0: The controller is allowed to send the self refresh command to Rank3 regardless if it is the time of C3/C4/C4P states in the PMU (Power Management Unit). 1: The controller will need to check if it is the C3/C4/C4P states in the PMU. If it is in neither C3 nor C4(C4P) state, the chip won't allowed the Rank3 of DRAM to go into self refresh mode; If it is in C3, C4 or C4P state, it is safe to let the DRAM to enter the self refresh since there will be a significant of time that the system probably won't need data.
5	RWS	0	**Check Vertical Blank of GFX for Rank2 to do By-Rank Self Refresh** Check the Vertical Blank status to determine if the chip is allowed to issue command to let Rank2 of DRAM to do self refresh. Please refer to bit-7 for more information only that it is applies to Rank2 instead of Rank3. 0: Not check. 1: Check.
4	RWS	0	**Check C3/C4 State of PMU for Rank3 to do By-Rank Self Refresh** Check the C3/C4 state to determine if the chip is allowed to issue command to let Rank2 of DRAM to do self refresh. Please refer to bit-6 for more information only that it is applies to Rank2 instead of Rank3. 0: Not check. 1: Check.
3	RWS	0	**Check Vertical Blank of GFX for Rank1 to do By-Rank Self Refresh** Check the Vertical Blank status to determine if the chip is allowed to issue command to let Rank1 of DRAM to do self refresh. Please refer to bit-7 for more information only that it is applies to Rank1 instead of Rank3. 0: Not check. 1: Check.
2	RWS	0	**Check C3/C4 State of PMU for Rank1 to do By-Rank Self Refresh** Check the C3/C4 state to determine if the chip is allowed to issue command to let Rank1 of DRAM to do self refresh. Please refer to bit-6 for more information only that it is applies to Rank1 instead of Rank3. 0: Not check. 1: Check.
1	RWS	0	**Check Vertical Blank of GFX for Rank0 to do By-Rank Self Refresh** Check the Vertical Blank status to determine if the chip is allowed to issue command to let Rank0 of DRAM to do self refresh. Please refer to bit-7 for more information only that it is applies to Rank0 instead of Rank3. 0: Not check. 1: Check.
0	RWS	0	**Check C3/C4 State of PMU for Rank0 to do By-Rank Self Refresh** Check the C3/C4 state to determine if the chip is allowed to issue command to let Rank0 of DRAM to do self refresh. Please refer to bit-6 for more information only that it is applies to Rank0 instead of Rank3. 0: Not check. 1: Check.

Note: Vertical Blanking: For a 30 Frame/ps screen, vertical blanking happened every other 33.33 ms. The duration of the vertical blanking period varies for configuration with different pixel resolutions. For example, for a 1920 x 1080 resolution screen, the duration could be as long as 596us. And for a 1600 x 1200 resolution screen, the duration could be 604us.

Offset Address: 99h (D0F3)

Power Management and Bypass Reorder Queue **Default Value: 10h**

Bit	Attribute	Default	Description
7	RWS	0	**1T Delay for DRAM Write Data Pointer Control** This register is to add one more internal cycle for data path at DRAM write cycle. 0: Disabled. It is recommended to set to 0 when the controller worked with DDR2/DDR3-800 and below. 1: Enabled. It should be set at 1 when the controller worked with DDR2/DDR3-1066 and above.
6	RWS	0	**Internal Control for DRAM Write Cycle** Adding one more cycle for an internal signal for the write cycle in the DRAM controller. 0: Disabled. It is recommended when the controller worked with DDR2/DDR3-800 and below. 1: Enabled. It should be set to 1 when the controller worked with DDR2/DDR3-1066 and above.
5	RWS	0	**1T Delay for DRAM Read Data Pointer Control** This register is to add one more internal cycle for data path at DRAM read cycle. 0: Disabled. It is recommended to set to 0 when the controller worked with DDR2/DDR3-533 and below. 1: Enabled. It should be set at 1 when the controller worked with DDR2/DDR3-800 and above.
4	RWS	1b	**Dynamical Clock Enable for the Clock of the TX path** This bit is to control the dynamical clock enable for the clock on the TX paths for the Circuit Macro besides the IO Pad of MDQS[7:0]P, MDQS[7:0]N, MD[63:0], and MDQM[7:0]. 0: Disabled, i.e. the clock is freely running. 1: Enabled, i.e. the clock will be running and stopped automatically.
3	RWS	0	**Behavior Control for MCS3#** This bit is to control the behavior of Rank Select Pin MCS3# when Rank 3 is in Self Refresh Mode. 0: MCS3# is driven high. 1: MCS3# is tri-stated.
2	RWS	0	**Behavior Control for MCS2#** This bit is to control the behavior of Rank Select Pin MCS2# when Rank 2 is in Self Refresh Mode. 0: MCS2# is driven high. 1: MCS2# is tri-stated.
1	RWS	0	**Behavior Control for MCS1#** This bit is to control the behavior of Rank Select Pin MCS1# when Rank 1 is in Self Refresh Mode. 0: MCS1# is driven high. 1: MCS1# is tri-stated.
0	RWS	0	**Behavior Control for MCS0#** This bit is to control the behavior of Rank Select Pin MCS0# when Rank 0 is in Self Refresh Mode. 0: MCS0# is driven high. 1: MCS0# is tri-stated.

Offset Address: 9Ah (D0F3)

By-Rank Self Refresh Related Registers - III **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**MODT Constraint for Exiting By-Rank Self Refresh** This bit works with Rx97[7] for the By-Rank Self Refresh mode on the DRAM DIMMs when MODT is needed to assert to provide termination for data integrity. Please refer to the register descriptions for Rx97[7]. **{Rx97[7] , Bit [7]}** 00: Disabled, the controller gives self refresh commands to individual Rank on conditions given by Rx97[6:4] and Rx98. 01: Enabled for exiting Self Refresh mode together. Not only the conditions given by Rx97[6:4] and Rx98, the idle condition of Ranks indicated by MODT assignment programmed at Rx9C had to be met in order for this controller to give commands to let Ranks to exit Self Refresh mode. 1x : Enabled for entering and exiting Self Refresh mode together. Not only the conditions given by Rx97[6:4] and Rx98, the idle condition of Ranks indicated by MODT assignment programmed at Rx9C had to be met in order for this controller to give commands to let Ranks to enter and exit Self Refresh mode. For best signal integrity concern, when working at DDR3 system (Rx6C[7] = 1), it is recommended to set these bits either at 01 or 1x. When working at DDR2 system (Rx6C[7] = 0), it is recommended to set these bits either at 01 or 1x if the operating frequency is 800Mhz (400Mhz DCLK) and above.
6:0	RWS	0	**Reserved**

Offset Address: 9Bh (D0F3)

Memory Clock Output Enable **Default Value: 3Fh**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RWS	1b	**Output Enable for Memory Clock Pin – MCLKO5P, MCLKO5N** This bit controls the behavior of memory clock pins – MCLKO5P/N. 0: Disabled, i.e. the pins MCLKO5P/N are tri-stated. 1: Enabled. MCLKO5P/N toggled at a clock rate the same as the internal DRAM controller's main clock.
4	RWS	1b	**Output Enable for Memory Clock Pin – MCLKO4P, MCLKO4N** This bit controls the behavior of memory clock pins – MCLKO4P/N. 0: Disabled, i.e. the pins MCLKO4P/N are tri-stated. 1: Enabled. MCLKO4P/N toggled at a clock rate the same as the internal DRAM controller's main clock.
3	RWS	1b	**Output Enable for Memory Clock Pin – MCLKO3P, MCLKO3N** This bit controls the behavior of memory clock pins – MCLKO3P/N. 0: Disabled, i.e. the pins MCLKO3P/N are tri-stated. 1: Enabled. MCLKO3P/N toggled at a clock rate the same as the internal DRAM controller's main clock.
2	RWS	1b	**Output Enable for Memory Clock Pin – MCLKO2P, MCLKO2N** This bit controls the behavior of memory clock pins – MCLKO2P/N. 0: Disabled, i.e. the pins MCLKO2P/N are tri-stated. 1: Enabled. MCLKO2P/N toggled at a clock rate the same as the internal DRAM controller's main clock.
1	RWS	1b	**Output Enable for Memory Clock Pin – MCLKO1P, MCLKO1N** This bit controls the behavior of memory clock pins – MCLKO1P/N. 0: Disabled, i.e. the pins MCLKO1P/N are tri-stated. 1: Enabled. MCLKO1P/N toggled at a clock rate the same as the internal DRAM controller's main clock.
0	RWS	1b	**Output Enable for Memory Clock Pin – MCLKO0P, MCLKO0N** This bit controls the behavior of memory clock pins – MCLKO0P/N. 0: Disabled, i.e. the pins MCLKO0P/N are tri-stated. 1: Enabled. MCLKO0P/N toggled at a clock rate the same as the internal DRAM controller's main clock.

DRAM ODT Control (9C-9Fh)

ODT (On Die Termination) is needed to provide resistance so that the signal integrity on a high speed bus can be maintained. For high speed signals of this chip like MD[63:0], MDQM[7:0], MDQS[7:0]P/N, when operating at DDR2-800, DDR3-800 or higher frequency, ODT on this chip and on the DRAM chips (controlled by the MODT[3:0] pin provided by this chip) will need to be turn on/off in an appropriate fashion. The basic idea is to turn on the ODT during the data phase of the read/write cycles on the MD, MDQM, MDQS bus so that the equivalent resistance on the bus is provided to ensure signal quality on those high speed signals. The controller's ODT enable control is at RxD4[7,1]. The main enable control for MODT[3:0] is at Rx9E[7]. The control for MODT[3:0] is complicate.

Offset Address: 9Ch (D0F3)

DRAM ODT Lookup Table **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**MODT Signal Active Selections When Accessing Rank 3** MODT[3:0] is allowed to assert when Rx9E[7] is 1. These registers specify which MODT pin will be asserted during the data phase when the controller accesses Rank3 (MCS3# asserted). 00: MODT0 01: MODT1 10: MODT2 11: MODT3
5:4	RWS	0	**MODT Signal Active Selections When Accessing Rank 2** MODT[3:0] is allowed to assert when Rx9E[7] is 1. These registers specify which MODT pin will be asserted during the data phase when the controller accesses Rank2 (MCS2# asserted). 00: MODT0 01: MODT1 10: MODT2 11: MODT3
3:2	RWS	0	**MODT Signal Active Selections When Accessing Rank 1** MODT[3:0] is allowed to assert when Rx9E[7] is 1. These registers specify which MODT pin will be asserted during the data phase when the controller accesses Rank1 (MCS1# asserted). 00: MODT0 01: MODT1 10: MODT2 11: MODT3
1:0	RWS	0	**MODT Signal Active Selections When Accessing Rank 0** MODT[3:0] is allowed to assert when Rx9E[7] is 1. These registers specify which MODT pin will be asserted during the data phase when the controller accesses Rank0 (MCS0# asserted). 00: MODT0 01: MODT1 10: MODT2 11: MODT3

Note: Besides the programming on these registers, MODT assertion also comes from other cases. Please refer to Table 22 below for detail information.

Table 22. Rx9C.1 MODT0 Assertion Logic for DDR3 and DDR2 System

DDR3 or DDR2 (Rx6C[7:6] = 10b or 01b)	Rank the cycle is accessing?	Read/Write Cycle?	DRAM Existed on Another DIMM (DIMM1)	Which Rank accessing would activate MODT0? As programmed in Rx9C (*1)	MODT0 (*2) status during the data phase cycle
DDR3	Rank 0	Read	-	--	0
		Write	-	--	1
	Rank A (other than Rank 0)	Read	No	--	0
		Read	Yes	Rank A	1
		Read	Yes	Not Rank A	0
		Write	-	Rank A	1
		Write	-	Not Rank A	0
DDR2	Rank 0	Read	-	--	0
		Write	-	Rank 0	1
		Write	-	Not Rank 0	0
	Rank A (other than Rank 0)	Read	No	--	0
		Read	Yes	Rank A	1
		Read	Yes	Not Rank A	0
		Write	-	Rank A	1
		Write	-	Not Rank A	0

Notes:
1: MODT0 could be programmed so that it's assertion comes from a lot of sources, e.g. when Rx9C is 00h, it means that the MODT0 will be asserted when accessing Rank0, Rank1, Rank2, and Rank3.
2: For the Assertion Logic for MODT1, it will have the same table only that we should change the "MODT0" to "MODT1", and "Rank 0" to "Rank1". As that for MODT2 and MODT3, besides the number switches to 2 and 3 for MODT and Rank, we also need to change the "DIMM1" to "DIMM0" for the header of the fourth column.

Offset Address: 9Dh (D0F3) – Reserved

Offset Address: 9Eh (D0F3)

DDR2/DDR3 DRAM ODT and Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**MODT Main Control** This bit is the enable bit for the assertion of MODT[3:0]. 0: Disabled, MODT[3:0] will always be de-asserted. 1: Enabled, MODT[3:0] will be asserted in an appropriate fashion.
6	RWS	0	**Idle Cycle before Write Command** This bit works with Rx51[0] to provide the timing for the case that any valid DDR commands followed by a write command. **{Rx51[0], Bit-6}** 0x: 2T command, there is always at least 1T of idle cycle in between two DRAM commands. 10: 1T command, there could be consecutive DRAM commands. 11: 2T write command, for the write command in the Command Queue, controller will always make sure there is always at least 1T of idle before the write being put to the DRAM bus.
5:4	RWS	0	**Extra MD Bus Turn Around Cycles for MODT Assertion** When adding extensions for the assertion of MODT[3:0] (Rx9F), the DRAM controller has to make sure that no data phase of the write cycle comes in after the data phase of a read cycle. When doing MD bus turn around for high speed, the assertion of MODT needs to be extended to make sure the data is correctly transferred. These bits tells the controller how many turn around cycles is needed to be added. 00: No extra cycle. 01: 1 extra cycle. 10: 2 extra cycles. 11: 3 extra cycles. *To make sure these bits are programmed correctly, two general rules as shown below must both be met: (1) Bits [5:4] >= Rx9F[1:0] + Rx9F[7:6] (2) Bits [5:4]) >= Rx9F[1:0] + Rx9F[5:4] For working with DDR3 system, these bits are suggested to be set at 01b, 10b or 11b. Please refer to Table 23 for more suggested value.
3:2	RWS	0	**DRAM Ranks for returning DQ0 when in write leveling mode** When preparing to go to write leveling mode (please refer to Figure 24 and the paragraph beneath it), chipset issues MRS commands to DRAM rank to let DRAM know which ranks are going to respond. Those MRS commands are done by CPU issuing DRAM read command with Rx6B[2:0] = 011b. When issuing MRS to different ranks, the write leveling enable bit in the MRS command bit is determined by the registers programmed here. 00: Rank0, the write leveling enable bit of the MRS to Rank0 is enabled. That of the MRS to other ranks are disabled. 01: Rank1, the write leveling enable bit of the MRS to Rank1 is enabled. That of the MRS to other ranks are disabled. 10: Rank2, the write leveling enable bit of the MRS to Rank2 is enabled. That of the MRS to other ranks are disabled. 11: Rank3, the write leveling enable bit of the MRS to Rank3 is enabled. That of the MRS to other ranks are disabled.
1	RWS	0	**Reserved**
0	RWS	0	**Differential DQS Input** This bit determine whether the internal strobe (latch) for MD[63:0] at DRAM read cycle is from MDQS pair MDQS[7:0]P/MDQS[7:0]N or MDQS[7:0]P only. 0: Disabled, MDQS[7:0]N are ignored. 1: Enabled, MDQS[7:0]P and MDQS[7:0]N are used as differential pairs.

Table 23. Rx9E.1 Suggested Setting for Rx9E[5:4], Rx9F[1:0,5:4,7:6] for DDR2/DDR3 at Different Frequency

DDR Type	Frequency	*Extra MD Bus Turn around for MODT Assertion:* 00: No 01: 1T extra 10: 2T extra 11: 3T extra	*Head extension of MODT Assertion for R/W cycles:* 00: No 01:1T ahead 10: 2T ahead 11: 3T ahead;	*Tail extension of MODT assertion for Write cycles:* 00: No 01: 1T extended 10: 2T extended 11: 3T extended	*Tail extension of MODT assertion for Read cycles:* 00: No 01: 1T extended 10: 2T extended 11: 3T extended
		Rx9E[5:4]	Rx9F[1:0]	Rx9F[7:6]	Rx9F[5:4]
DDR2	533	01	00	01	01
	667	01	00	01	01
	800	01	00	01	01
DDR3	800	10	01	01	01
	1066	10	01	01	01

Offset Address: 9Fh (D0F3)

DDR2/DDR3 DRAM ODT Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Tail Extension of MODT Assertion for Write Cycles** These bits define the extension of the assertion of pins MODT[3:0] at the end of a DRAM write cycle. Note that the MODT [3:0] is enabled when Rx9E[7] is 1 and the active selection at Rx9C is programmed. e.g. MODT3 could be asserted at the data phase when accessing Rank0 if Rx9C[1:0] is programmed as 11b. 00: No extension, i.e. the assertion of the MODT[3:0] goes with the data phase of the write cycle.. 01: 1T extension, i.e. the assertion of the MODT[3:0] extends 1T after the data phase of the write cycle. 10: 2T extension, i.e. the assertion of the MODT[3:0] extends 2T after the data phase of the write cycle. 11: 3T extension. i.e. the assertion of the MODT[3:0] extends 3T after the data phase of the write cycle. The idle cycle added for the DRAM controller when MD bus turn around happened have to be larger than the extra T added by programming to these registers. Please refer to Table 23 and Rx9E[5:4] for more information.
5:4	RWS	0	**Tail Extension of MODT Assertion for Read Cycles** These bits define the extension of the assertion of pins MODT[3:0] at the end of a DRAM read cycle. Note that the MODT [3:0] is enabled when Rx9E[7] is 1 and the active selection at Rx9C is programmed. e.g. MODT3 could be asserted at the data phase when accessing Rank0 if Rx9C[1:0] is programmed as 11b. 00: No extension, i.e. the assertion of the MODT[3:0] goes with the data phase of the read cycle.. 01: 1T extension, i.e. the assertion of the MODT[3:0] extends 1T after the data phase of the read cycle. 10: 2T extension, i.e. the assertion of the MODT[3:0] extends 2T after the data phase of the read cycle. 11: 3T extension. i.e. the assertion of the MODT[3:0] extends 3T after the data phase of the read cycle. The idle cycle added for the DRAM controller when MD bus turn around happened have to be larger than the extra T added by programming to these registers. Please refer to Table 23 and Rx9E[5:4] for more information.
3:2	RWS	0	**Reserved**
1:0	RWS	0	**Head Extension of MODT Assertion for Read/Write Cycles.** The time the pins MODT[3:0] asserted before the beginning of a DRAM read/write cycle. Note that the MODT[3:0] is enabled when Rx9E[7] is 1 and the active selection at Rx9C is programmed. e.g. MODT3 could be asserted at the data phase when accessing Rank0 if Rx9C[1:0] is programmed as 11b. 00: 0T, i.e. the assertion of MODT[3:0] starts with the data phase of the DRAM cycles. 01: 1T ahead, i.e. the assertion of MODT[3:0] starts 1T before the data phase of the DRAM cycles. 10: 2T ahead, i.e. the assertion of MODT[3:0] starts 2T before the data phase of the DRAM cycles. 11: 3T ahead, i.e. the assertion of MODT[3:0] starts 3T before the data phase of the DRAM cycles. The idle cycle added for the DRAM controller when MD bus turn around happened have to be larger than the extra T added by programming to these registers. Please refer to Table 23 and Rx9E[5:4] for more information. For working with DDR3 system, these bits are suggested to be set at 01b, 10b or 11b.

UMA/GMINT Registers (A0–AFh)

Offset Address: A1-A0h (D0F3)

CPU Direct Access Frame Buffer Control **Default Value: 8000h**

Bit	Attribute	Default	Description
15	RWS	1b	**Internal Graphic Controller Enabling** This chip integrated an internal Graphic Controller device at PCI configuration address:{B0D1F0}, this bit is to enable that Graphic function. 0: Internal Graphic Device is disabled. 1: Internal Graphic Device is enabled and can be seen at B0D1F0.
14:12	RWS	000b	**Frame Buffer Size Selection** When bit-15 is set to 1, the internal Graphic controller is enabled. These bits defined the size of the Frame buffer memories used by the internal Graphic controller. When these bits were programmed a value other than 000b, this chip will define the very top of the physical memory with the size defined by these bits as the frame buffer memory used for Graphic controller. The base address of this area is defined by D1F0 Rx18~Rx1B. Cycles from any devices in the system with the address targeted to these Frame Buffer area will be forwarded to internal Graphic controller to let it issue cycles to DRAM controller to access DRAM. Besides bit-15, another control bit D0F0 RxB0[0] is used for Frame Buffer accessing, and needed to be programmed to 1. 000: 0 Mega, i.e. no Frame Buffer is defined, this option is valid only when bit-15 is 0. 001: 8M 010: 16M 011: 32M 100: 64M 101: 128M 110: 256M 111: 512M
11:3	RWS	0	**Base Address [31:23] for Direct Frame Buffer Access** In a conventional system, when CPU needs to access Frame Buffer, it issues r/w cycles to Graphic controller. Then, Graphic controller issues cycles to its Frame Buffer memory. In a system with integrated Graphic controller, since the Graphic controller uses part of the memory as its Frame Buffer, chipset could arrange to access Frame Buffer directly from CPU. Only that software might need to program this base address in a non-memory mapped area such that no memory space will be wasted. When Direct Frame Buffer Access is enabled (D1F0 RxB9[1] =1), the CPU issues cycles in the range of {RDFBA+Frame Buffer size: RDFBA} (where RDFBA is defined here at this register space), the host controller of this chip will translate these cycles to the real address of the Frame Buffer defined at the top of the memory below 4G and send requests to DRAM controller to complete the accessing. Note that Direct Frame Buffer Access is available only when internal Graphic controller is enabled, i.e. Bit-15 = 1.
2	RWS	0	**Base Address [32] for Direct Frame Buffer Access** Bit[32] is defined here for the Address of Direct Frame Buffer accessing when address space is over 4G. Please refer to bits [11:3] for more information about the Direct Frame Buffer Access.
1	RWS	0	**Direct Frame Buffer Base Address Selection** In the Direct Frame Buffer Access mode, the controller had two sources of Base address[32:23] can be used. One of them is in this Function at{Bit [2], Bits[11:3]}, the other is in D0F0 {RxCC[0], RxCB, RxCA[7]}. Noted that the registers in D0F0 RxC8~RxCF are shadow registers of D1F0 Rx18~Rx1F, which also stored another Direct Frame Buffer Base Address other than {Bit [2], Bits [11:3]}.This bit is used to select which one to be used. 0: Use {Bit [2], Bits [11:3]} as the base address[32:23] for Direct Frame Buffer Access. 1: Use D0F0{RxCC[0], RxCB, RxCA[7]}as the base address[32:23] for Direct Frame Buffer Access.
0	RWS	0	**Reserved**

Offset Address: A2h (D0F3)

DRAM Arbitration Bandwidth Timer - II **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RWS	0	**GFX Display High Priority Bandwidth Timer** Time slot allocated for DRAM controller to accept high priority requests from internal GFX-Display engine. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the high priority requests from GFX Display engine can be continuously served for that much of time. Please refer to Figure 19 for the illustration of the arbiter's structure. 0000: 0 DCLK, i.e. if there are other requests in the system, only one high priority request from the GFX-Display engine can be served before DRAM controller switch to serve others. 0001: 1 x 16 DCLKs. 0010: 2 x 16 DCLKs. … 1111: 15 x 16 DCLKs.
3:0	RWS	0	**GFX Display Bandwidth Timer** Time slot allocated for DRAM controller to accept normal priority requests from internal GFX-Display engine. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the normal priority requests from GFX-Display engine can be continuously served for that much of time. Please refer to Figure 19 for the illustration of the arbiter's structure. 0000: 0 DCLK, i.e. if there are other requests in the system, only one normal priority request from the GFX-Display engine can be served before DRAM controller switch to serve others. 0001: 1 x 16 DCLKs. 0010: 2 x 16 DCLKs. … 1111: 15 x 16 DCLKs.

Request Queues and Data Dispatcher for GMINT

GMINT is a unit resided in between the Graphic Controller (GFXCTL) and DRAM Controller (DRAMC). It handled the requests from GFX and GFX-Display engines and passed the requests to DRAMC. Since the data coming back from the DRAMC will be out of order, GMINT also needs to pack and reorder those data before it passed them to the requesters inside the GFXCTL. An simple illustration is provided on Figure 25 below.

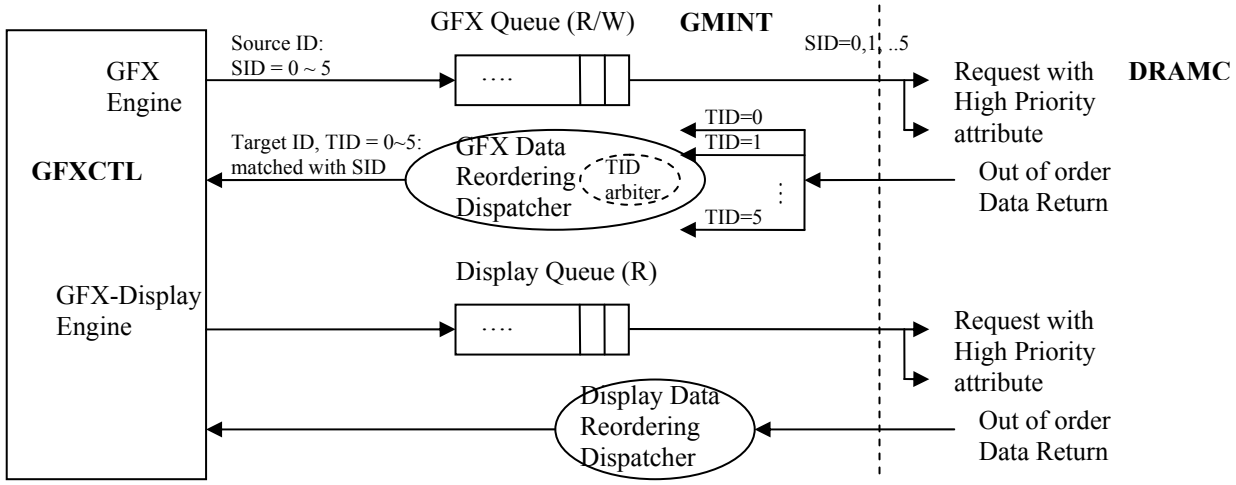


Figure 25. RxA3.1 Structure of Requests and Data return handling units of the GMINT

There are 6 different sources of requests (read and write, thus, there are 6 SID in the interface of GFXCTL and GMINT.) from GFX Engine. GMINT will put them into the GFX Queue which worked at the first-in and first-out fashion. However, if any of the requests from the GFX engine indicating it is a high priority event, a high priority attribute will be marked while GMINT is requesting service to the DRAMC. The data return from DRAMC could be out of order. Thus, GMINT does have a data dispatcher unit to handle the data reordering. Since the coming back data could be for different sources, an arbitration unit within the dispatcher called TID arbiter is also needed. The same structure is also provided for requests from GFX-Display Engine. But, noted that there is only one source of request from GFX-Display Engine. Thus, the data dispatcher for Display request handling is simpler (no TID arbiter), however, the dispatcher for the display data still have to handle the data reordering.

Offset Address: A3h (D0F3)

GMINT Miscellaneous Control - I **Default Value: 28h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RWS	1b	**1T Latency for 8QW Merging.** In order to determine if the internal multiple requests from GFX engine can be merged into one 8QW request for the GFX Queue within the GMINT (please refer to Figure 25), 1T latency is added before entering the GFX Queue. 0: Normal latency. 1: 1T extra latency is added.
4	RWS	0	**Reserved**
3	RWS	1b	**Write Merging Depends on Request Attribute of GFX Engine** For the write requests from the GFX engine, there is a request attribute "VMERGE" comes with the request to indicate if the write request can be merged (Note) with other write requests queued or coming in later on. When this bit is enabled, the write merging attribute "VMERGE" is ignored by the DRAMC. 0: DRAMC will do write merging depends on the "VMERGE" attribute of the write requests from GFX engine. VMERGE = 0: DRAMC will not do write merging for that request. VMERGE = 1: DRAMC will do write merging for that request if the write merging condition is met. 1:DRAMC will ignore the status of VMERGE from GFX engine, all write cycles can be merged if the write merging condition is met. For the write merging condition, please refer to Table 16 for complete information.
2	RWS	0	**Disable Option to Check GFXCTL Request Behavior** 0: GPRI will be 1 when there is a higher priority GADS pending regardless the status of GFX request. 1: GPRI may be 0 in some special cases when there is still a higher priority GADS pending but no GFX request.
1:0	RWS	0	**Reserved**

Note: VMERGE: When GFX engine requests write cycles for 3D engine's Z data or color data, this signal will be asserted.

Offset Address: A4h (D0F3)

GMINT Miscellaneous Control - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Conventional VGA Paths for Internal Integrated GFX** With RxA1[7] being 1, this bit is to enable conventional VGA cycles for the internal integrated graphic controller. The so-called conventional VGA cycles are memory cycles with range {A0000h~BFFFFh} and I/O cycles with range {3B0h~3BBh, 3C0h~3DFh}. 0: The chip will forward the conventional VGA cycles to other GFX related buses. 1: The chip will forward the conventional VGA cycles to internal GFX controller.
6	RWS	0	**Reserved** Programming 1 or 0 to this bit does not change any chip behavior.
5	RWS	0	**Disabling of the PCIe Physical Macro - PCIE_EPHY** This bit is to control the PLL of the PCIe physical macro: PCIE_EPHY. 0: PCIE_EPHY is enabled. 1: PCIE_EPHY is disabled, i.e. the PLL inside the PCIE_PHY is reset.
4:0	RWS	0	**Reserved**

Offset Address: A5h (D0F3)

GMINT Miscellaneous Control - III **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RWS	0	**Reset of Internal Integrated Graphic Controller (GFXCTL)** This bit is to reset the internal integrated graphic controller. 0: The GFXCTL will be in normal State. 1: The GFXCTL will be in Reset State. *To complete a reset to the GFX, this bit has to be programmed to 1 and to 0 again.
4:0	RWS	0	**Reserved**

Offset Address: A7-A6h (D0F3)

GMINT – Data Reordering Dispatcher Arbitration – GFX Engine - I **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 0** Please refer to Figure 25, when TID arbiter in the GFX Data Reordering Dispatcher arbitrates data streams returned from DRAMC, it will try to balance the data stream for every requests with different Source ID (SID, 0~5 , refer to note below). These two bits defined the maximum number of consecutive data can be served for requests with SID=0 when there are other data for requests with different SID are ready to be passed back to the GFX engine. However, if there is no other returned data needed to be served. The bandwidth of data for requests with SID=0 won't be constrained by these registers. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
13:12	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 1** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 1. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
11:10	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 2** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 2. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
9:8	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 3** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 3. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
7:6	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 4** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 4. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
5:4	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 5** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 5. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
3	RWS	0	**Reserved**
2	RWS	0	**Test Mode for Holding Requests from GFX engine** This bit is for test mode used only. When this bit is enabled, the test general I/O pin TP1will be used to hold (TP1=0) the requests from GFX engine. In a normal system, this bit should be always 0. 0: Disabled. 1: Enabled.
1	RWS	0	**Request Priority Handling from GFX Engine to DRAMC** For those high priority requests from the GFX engine, with this bit turn on, the high priority attribute which goes along with the requests to DRAMC will be masked. i.e. All requests from GFX engine will be treated as normal priority by DRAMC. 0: The requests from GMINT to DRAMC will have the priority as indicated by the GFX engine. 1: The requests from GMINT to DRAMC will always be treated as normal priority.
0	RWS	0	**8QW Requests Merging** Requests (4QW, 2QW) from the GFX engine can be merged into one single 8QW request if this bit is enabled. 0: Disabled, the requests to the DRAMC will follow what comes in from the GFX engine. 1: Enabled, multiple requests may be merged into one single 8QW request.

Note: There are programmable Sequence (or Source) ID defined by the GFX's IO register 3C5.7E ~ 3C5.A7 (These registers are accessed through IOW 3C4h, index#; IOW 3C5h, byte_value; where index# is from 90h to A7h) to assign SID for the requests from each engines (e.g. Command Bus Unit(CBU), Command Regulator (CR), Table Lookaside Buffer (TLB), Display engine, 2D engine, MPEG engine, 3D engine, and DMA engine). However, only SID=0~5 are valid setting, and only SID=0 can be assigned to multiple engines. SID=1..5 must be assigned to one single engine.

Offset Address: A9-A8h (D0F3)

GMINT – Data Reordering Dispatcher Arbitration – GFX Engine - II **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RWS	0	**Reserved**
13:12	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 0** Please refer to Figure 25. For data stream returned from the DRAMC, the TID arbiter within the GFX Data Reordering Dispatcher will arbitrate in between data streams with different Source ID (SID, 0~5, refer to note below). TID arbiter had normal and high priority arbitration engine inside. When data stream comes back from the DRAMC, they should be all queued in the normal priority engine waiting for being dispatched. These two bits defined the time the data stream with SID = 0 will wait for service in the normal priority engine before the TID arbiter raises its priority. Once the data stream with SID = 0 had been raised to high priority, it will push the TID arbiter to serve for it in a shorter latency. However, if there are also data streams with different SID waiting in the high priority engine. It will follow the round robin scheme and wait to be served. And once it is served by the high priority engine, it will be served for the maximum bandwidth programmed at RxA7[7:6] as long as it had that many of requests. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
11:10	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 1** Please refer to the register descriptions of bits [13:12]. The only difference is that these registers defined the promotion timer for the data streams with SID = 1. And the maximum bandwidth registers for SID=1 is at RxA7[5:4]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
9:8	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 2** Please refer to the register descriptions of bits [13:12]. The only difference is that these registers defined the promotion timer for the data streams with SID = 2. And the maximum bandwidth registers for SID=2 is at RxA7[3:2]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
7:6	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 3** Please refer to the register descriptions of bits [13:12]. The only difference is that these registers defined the promotion timer for the data streams with SID = 3. And the maximum bandwidth registers for SID=3 is at RxA7[1:0]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
5:4	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 4** Please refer to the register descriptions of bits [13:12]. The only difference is that these registers defined the promotion timer for the data streams with SID = 4. And the maximum bandwidth registers for SID=4 is at RxA6[7:6]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
3:2	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 5** Please refer to the register descriptions of bits [13:12]. The only difference is that these registers defined the promotion timer for the data streams with SID = 5. And the maximum bandwidth registers for SID=5 is at RxA6[5:4]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
1	RWS	0	**1 More Pipelined Stage for Signals from GFX Engine** Those signals from GFX engine to GMINT will be added one T in the path from GFX core to GMINT control logic. 0: One more T of pipelined stage is added. 1: No pipelined stage is added, i.e. signals of GFX engine from GFX core directly drive to GMINT controller.
0	RWS	0	**1 More Pipelined Stage for Signals from GFX Display Engine** Those signals from GFX Display engine to GMINT will be added one T in the path from GFX core to GMINT control logic. 0: One more T of pipelined stage is added. 1: No pipelined stage is added, i.e. signals of Display engine from GFX core directly drive to GMINT controller.

Note: There are programmable Sequence ID defined by the GFX's IO register 3C5.7E ~ 3C5.A7 (These registers are accessed through IOW 3C4h, index#; IOW 3C5h, byte_value; where index# is from 90h to A7h) to assign SID to each engines (e.g. Command Bus Unit(CBU), Command Regulator (CR), Table Lookaside Buffer (TLB), Display engine, 2D engine, MPEG engine, 3D engine, and DMA engine). However, only SID=0~5 are valid setting, and only SID=0 can be assigned to multiple engines. SID=1..5 must be assigned to one single engine.

Offset Address: AA-ABh (D0F3) – Reserved

Offset Address: ACh (D0F3)

GMINT – Space Size Selections for HDMI/HD Audio **Default Value:12h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5:3	RWS	010b	**Graphic Core/HDMI MMIO Space Size Selection** When RxA1[7] is set to 1, the internal Graphic controller is enabled. These bits defined the size of the MMIO space for the HDMI engine in the GFX Core. The base address of this space is defined by D1F0 Rx14~Rx17. Cycles from any devices in the system (especially from CPU) with the address targeted to this HDMI MMIO space will be forwarded to internal graphic controller. PCI standard memory accessing enable bit at D1F0 Rx04[1], and another control bit at D0F0 RxB0[1], are needed to be programmed to 1 to enable the accessing to this space. 000:Illegal. 001:8M 010:16M. 011:32M 100:64M. 101:128M 110:256M. 111:512M
2:0	RWS	010b	**HD Audio MMIO Space Size Selection** When RxA1[7] is set to 1, the internal Graphic Controller is enabled. These bits defined the size of the MMIO space for the HD Audio Controller inside the GFX core. The base address of this space is defined by D1F1 Rx10~Rx13. Cycles from any devices in the system (especially from CPU) with the address targeted to this HD Audio MMIO space will be forwarded to internal graphic controller. PCI standard memory accessing enable bit at D1F1 Rx04[1] and another control bit at D0F0 RxB0[4], are needed to be set to 1 to enable the accessing to this space. 000: Illegal. 001: 8K 010:16K. 011: 24K. 100:32K. 101~111: 16K

Offset Address: AD-AFh (D0F3) – Reserved

VDIF/VMINT Registers (B0–BFh)

VDIF is just a wrapper outside of VMINT for interface connections. VMINT is the major block in between Video Decoder and the DRAM controller. Figure 26 below provides illustrations for the major functions of VMINT.

Offset Address: B0h (D0F3)

DRAM Arbitration Bandwidth Timer - III **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RWS	0	**Video Decoder High Priority Bandwidth Timer** Time slot allocated for DRAM controller to accept high priority requests from internal Video Decoder engine. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the high priority requests from Video Decoder engine can be continuously served for that much of time. Please refer to Figure 19 for the illustration of the arbiter's structure. 0000: 0 DCLK, i.e. if there are other requests in the system, only one high priority request from the Video Decoder engine can be served before DRAM controller switch to serve others. 0001: 1 x 16 DCLKs. 0010: 2 x 16 DCLKs. … 1111: 15 x 16 DCLKs.
3:0	RWS	0	**Video Decoder Bandwidth Timer** Time slot allocated fro DRAM controller to accept normal priority requests from internal Video Decoder engine. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the normal priority requests from Video Decoder engine can be continuously served for that much of time. Please refer to Figure 19 for the illustration of the arbiter's structure. 0000: 0 DCLK, i.e. if there are other requests in the system, only one normal priority request from the Video Decoder engine can be served before DRAM controller switch to serve others. 0001: 1 x 16 DCLKs. 0010: 2 x 16 DCLKs. … 1111: 15 x 16 DCLKs.

Request Queues and Data Dispatcher for VMINT

VMINT is the major unit resided in between Video Decoder (VD) and DRAM Controller (DRAMC). It handled the requests from Video Decoder engine and passed the requests to DRAMC. Since the data coming back from the DRAMC will be out of order, VMINT also needs to pack and reorder those data before it passed them to the requesters inside the VD. An simple illustration is provided in Figure 26 below.

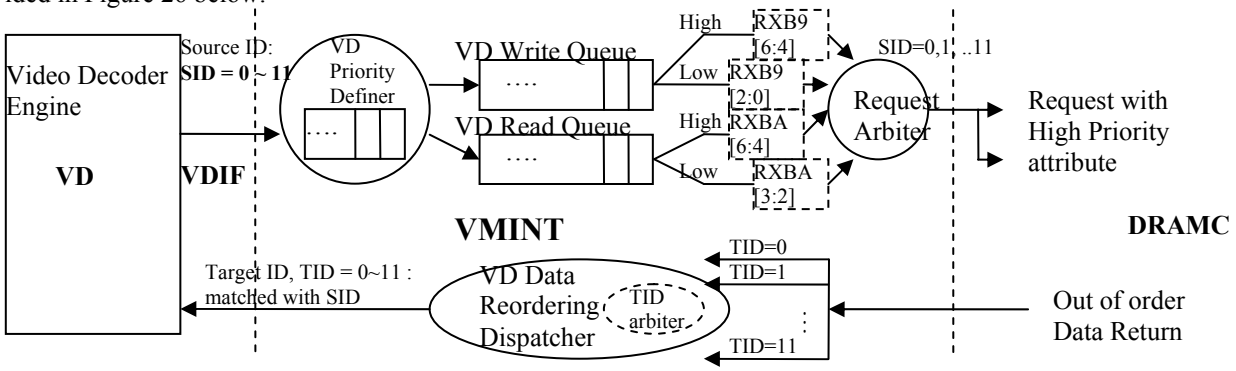


Figure 26. RxB1.1 Structure of Requests and Data Return Handling Units of the VMINT

There are 12 different sources of requests (read and write) from Video Decoder Engine. VMINT will put them into the VD Write Queue and VD Read Queue which worked at the first-in and first-out fashion. Before VMINT pushed the requests into the VD R/W Queues, it defined the attributes for each of the requests. The control logic "VD Priority Definer" is designed so that VMINT is able to dynamically change the priority to high/low for each requests when the controller predicts the bandwidth is less/more than enough (RxB8). There are also arbitration unit before VMINT sending request out to DRAMC. For high/low priority read/write requests, there are bandwidth timer associated with them. VMINT provided flexibility for users to adjust the bandwidth for high/low priority on read/write requests. However, since the VD W/R Queue are working at the first-in and first-out fashion, once there are high priority requests queued in, the high priority indicator to the Request Arbiter will be asserted. The real priority in the request arbiter to the DRAMC are "High priority Write" > "High Priority Read" > "Low Priority Write" > "Low Priority

Read". i.e. Although there are bandwidth timer associated with Low Write requests, the arbiter could shift the ownership to High Read immediately if there are High Priority Read coming in. A more clear illustration is given below by walking through an example. Let's define some terminologies here first:
Write High Priority Bandwidth Timer (Bandwidth time slot can be programmed at RxB9[6:4]): WH_Timer;
Write Low Priority Bandwidth Timer (Bandwidth time slot can be programmed at RxB9[2:0]): WL_Timer;
Read High Priority Bandwidth Timer (Bandwidth time slot can be programmed at RxBA[6:4]): RH_Timer;
Read Low Priority Bandwidth Timer (Bandwidth time slot can be programmed at RxBA[2:0]): RL_Timer;
A simple diagram below can be given to have a simple idea regarding the arbitration for the high/low priority r/w requests:

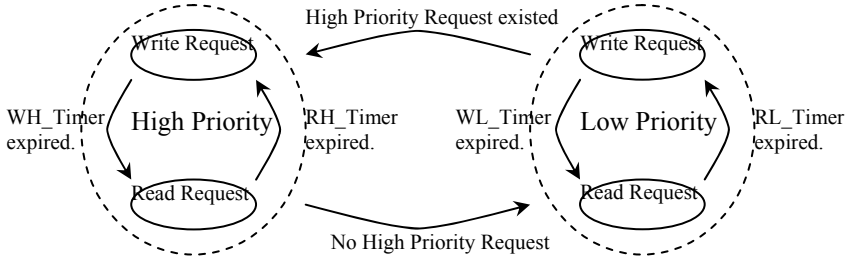


Figure 27. RxB1.2. The Ownership Shifting for the Request Arbiter

A bunch of requests come in from the VD, and the processing of the request could be as described in the following steps:

1) Low Priority Write requests queued in from VD: WL0, WL1, WL2. And we had the queue status as:

VD Queue	Tail							Head
Write						WL2	WL1	WL0
Read								

2) Arbiter serves WL0.
3) Low Priority Read requests queued in from VD: RL0, RL1. And we had the queue status as:

VD Queue	Tail							Head
Write							WL2	WL1
Read							RL1	RL0

4) Arbiter served WL1, and High Priority Write requests queued in from VD: WH0, WH1, WH2, WH3. Queue status is:

VD Queue	Tail							Head
Write			WH3	WH2	WH1	WH0	WL2	WL1
Read							RL1	RL0

5) Although the WL_Timer is still counting, arbiter shift to count WH_Timer and continue serving WL2, then WH0. Note that although WL2 is low priority, but since it is in front of the WH0 in a single write queue. It got to be served as the high priority request.
6) High Priority Read requests come in from VD: RH0, RH1. And Low Priority Write requests comes in from VD: WL3, WL4, WL5, WL6, WL7. Queue status is:

VD Queue	Tail							Head
Write	WL7	WL6	WL5	WL4	WL3	WH3	WH2	WH1
Read					RH1	RH0	RL1	RL0

7) WH_Timer counts to its programmed time while serving WH2, and since there are high request in the Read Queue. The arbiter shifts to serve high priority read and counting RH_Timer. The Queue status is:

VD Queue	Tail							Head
Write			WL7	WL6	WL5	WL4	WL3	WH3
Read					RH1	RH0	RL1	RL0

8) Low Priority Read come in while arbiter is serving read queue using RH_Timer. Noted that the arbiter is actually serving RL0 which is intrinsically a low priority request. The Queue status is:

VD Queue	Tail							Head
Write			WL7	WL6	WL5	WL4	WL3	WH3
Read			RL4	RL3	RL2	RH1	RH0	RL1

9) RH_Timer counts to its programmed time while serving RH1. It shifted to serve to WH3 and start to count WH_Timer. While serving the WH3, the high priority signal is de-asserted since there is no more high priority requests in the Write Queue. Queue status is:

VD Queue	Tail							Head
Write				WL7	WL6	WL5	WL4	WL3
Read						RL4	RL3	RL2

10) Arbiter continue serving WL3 and start to count WL_Timer. WL_Timer counts to its programmed time while serving WL6. It will shift to serve Read Queue. Queue status is:

VD Queue	Tail							Head
Write								WL7
Read						RL4	RL3	RL2

11) Arbiter now serves RL2, RL3 and start to count RL_Timer. Read Queue is empty before the expiration of RL_Timer. And thus, the arbiter can shift back to serve WL7.

Again, the principle is: “High priority Write” > “High Priority Read” > “Low Priority Write” > “Low Priority Read”. As long as there is high priority (read or write), the arbiter would go serve high priority requests. The WH_Timer or RH_Timer will work for shifting between High Priority writes and reads. And the WL_Timer and RL_Timer will work for shifting between Low priority writes and reads.

The data return from DRAMC could be out of order. Thus, VMINT does have a data dispatcher unit to handle the data reordering. Since the coming back data could be for different sources, an arbitration unit within the dispatcher called TID arbiter is also needed.

Offset Address: B1h (D0F3)

VMINT Miscellaneous Control - I **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5	RWS	1b	**1T Latency for 8QW Merging** In order to determine if the internal multiple requests from VD engine can be merged into one 8QW request for the VD Queue within the VMINT (please refer to Figure 26), 1T latency is added before entering the VD Queue. 0: Normal latency. 1: 1T extra latency is added.
4:3	RWS	0	**Reserved**
2	RWS	0	**Request Priority Handling from VD Engine to DRAMC** For those high priority requests from the VD engine, with this bit turn on, the high priority attribute which goes along with the requests to DRAMC will be masked. i.e. All requests from VD engine will be treated as normal priority by DRAMC. 0: The requests from VMINT to DRAMC will have the priority as indicated by the VD engine. 1: The requests from VMINT to DRAMC will always be treated as normal priority.
1	RWS	0	**8QW Requests Merging** Requests (4QW, 2QW) from the VD engine can be merged into one single 8QW request if this bit is enabled. 0: Disabled, the requests to the DRAMC will follow what comes in from the VD engine. 1: Enabled, multiple requests may be merged into one single 8QW request.
0	RWS	0	**Reserved**

Offset Address: B3-B2h (D0F3)

VMINT – Data Reordering Dispatcher Arbitration – VD Engine - I **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 0** Please refer to Figure 26, When TID arbiter in the VD Data Reordering Dispatcher arbitrates data streams returned from DRAMC, it will try to balance the data stream for every requests with different Source ID (SID, 0~11). These two bits defined the maximum number of consecutive data can be served for requests with SID=0 when there are other data for requests with different SID are ready to be passed back to the VD engine. However, if there is no other returned data needed to be served. The bandwidth of data for requests with SID=0 won't be constrained by these registers. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
13:12	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 1** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 1. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
11:10	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 2** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 2. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
9:8	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 3** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 3. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
7:6	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 4** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 4. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
5:4	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 5** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 5. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
3:2	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 6** Please refer to the register descriptions of bits [15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 6. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
1:0	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 7** Please refer to the register descriptions of bits[15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 7. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.

Offset Address: B4h (D0F3)

VMINT – Data Reordering Dispatcher Arbitration – VD Engine - II **Default Value: 0000h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 0** Please refer to Figure 26. For data stream returned from the DRAMC, the TID arbiter within the VD Data Reordering Dispatcher will arbitrate in between data streams with different Source ID (SID, 0~11). TID arbiter had normal and high priority arbitration engine inside. When data stream comes back from the DRAMC, they should be all queued in the normal priority engine waiting for being dispatched. These two bits defined the time the data stream with SID = 0 will wait for service in the normal priority engine before the TID arbiter raises its priority. Once the data stream with SID = 0 had been raised to high priority, it will push the TID arbiter to serve for it in a shorter latency. However, if there are also data streams with different SID waiting in the high priority engine. It will follow the round robin scheme and wait to be served. And once it is served by the high priority engine, it will be served for the maximum bandwidth programmed at RxB3[7:6] as long as it had that many of requests. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
5:4	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 1** Please refer to the register descriptions of bits [7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 1. And the maximum bandwidth registers for SID=1 is at RxB3[5:4]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
3:2	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 2** Please refer to the register descriptions of bits [7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 2. And the maximum bandwidth registers for SID=2 is at RxB3[3:2]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
1:0	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 3** Please refer to the register descriptions of bits [7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 3. And the maximum bandwidth registers for SID=3 is at RxB3[1:0]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.

Offset Address: B5h (D0F3)

VMINT – Data Reordering Dispatcher Arbitration – VD Engine - III **Default Value: 0000h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 8** Please refer to the register descriptions of RxB2[15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 8. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
5:4	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 9** Please refer to the register descriptions of RxB2[15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 9. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
3:2	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 10** Please refer to the register descriptions of RxB2[15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 10. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.
1:0	RWS	0	**Maximum Bandwidth for Data Stream with Source ID = 11** Please refer to the register descriptions of RxB2[15:14]. The only difference is that these registers defined the maximum bandwidth for the data streams with SID = 11. 00: 8 cycles, i.e. 8 x 2QW. 01: 16 cycles, i.e. 16 x 2QW. 10: 24 cycles, i.e. 24 x 2QW. 11: 32 cycles, i.e. 32 x 2QW.

Offset Address: B7-B6h (D0F3)

VMINT – Data Reordering Dispatcher Arbitration – VD Engine - IV **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 4** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 4. And the maximum bandwidth registers for SID=4 is at RxB2[7:6]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
13:12	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 5** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 5. And the maximum bandwidth registers for SID=5 is at RxB2[5:4]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
11:10	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 6** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 6. And the maximum bandwidth registers for SID=6 is at RxB2[3:2]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
9:8	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 7** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 7. And the maximum bandwidth registers for SID=7 is at RxB2[1:0]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
7:6	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 8** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 8. And the maximum bandwidth registers for SID=8 is at RxB5[7:6]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
5:4	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 9** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 9. And the maximum bandwidth registers for SID=9 is at RxB5[5:4]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
3:2	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 10** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 10. And the maximum bandwidth registers for SID=10 is at RxB5[3:2]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.
1:0	RWS	0	**Promotion Timer to Raise Priority for Data Stream with Source ID = 11** Please refer to the register descriptions of RxB4[7:6]. The only difference is that these registers defined the promotion timer for the data streams with SID = 11. And the maximum bandwidth registers for SID=11 is at RxB5[1:0]. 00: 8 DCLKs. 01: 16 DCLKs. 10: 24 DCLKs. 11: 32 DCLKs.

Offset Address: B8h (D0F3)

VMINT – Priority Adjustment **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RWS	0	**Reserved**
5:4	RWS	0	**Priority Adjustment Window for VD Write Requests** Those write requests from VD (Video Decoder engine) does not have priority attribute associated with them. However, since there is some latency requirement needed to be satisfied for a correct video decode processing, the "Priority Definer" in the VMINT (please refer to Figure 26) did have a scheme to append a high priority attribute to its write requests. This priority adjustment scheme is to adjust the priority attribute which associated with the write requests sent to the DRAM eventually. Within a period of time (Priority Adjustment Window) defined by these two bits, the inherent priority will be raised to high if the number of the requests queued in the Priority Definer at the beginning of this period is greater than the number of requests being processed to the Write VD Queue. And it will be changed to low priority if the number of the requests queued in the Priority Definer at the beginning of this period is less than the number of requests being processed to Write VD Queue. This priority adjustment scheme continuously works at the end of each Priority Adjustment Window. Thus, the priority attribute associated with the requests coming in from the VD could be changed at the end of each period defined by this Priority Adjustment Window. 00: 32 DCLKs. 01: 64 DCLKs. 10: 96 DCLKs. 11: 128 DCLKs.
3:2	RWS	0	**Reserved**
1:0	RWS	0	**Priority Adjustment Window for VD Read Requests** Those read requests from VD (Video Decoder engine) does not have priority attribute associated with them. However, since there is some latency requirement needed to be satisfied for a correct video decode processing, the "Priority Definer" in the VMINT (please refer to Figure 26) did have a scheme to append a high priority attribute to its read requests. This priority adjustment scheme is to adjust the priority attribute which associated with the read requests sent to the DRAM eventually. Within a period of time (Priority Adjustment Window) defined by these two bits, the inherent priority will be raised to high if the number of the requests queued in the Priority Definer at the beginning of this period is greater than the number of requests being processed to the Read VD Queue. And it will be changed to low priority if the number of the requests queued in the Priority Definer at the beginning of this period is less than the number of requests being processed to Read VD Queue. This priority adjustment scheme continuously works at the end of each Priority Adjustment Window. Thus, the priority attribute associated with the requests coming in from the VD could be changed at the end of each period defined by this Priority Adjustment Window. 00: 32 DCLKs. 01: 64 DCLKs. 10: 96 DCLKs. 11: 128 DCLKs.

Offset Address: B9h (D0F3)

VMINT Arbitration Bandwidth Timer - I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6:4	RWS	0	**VD Write Queue High Priority Bandwidth Timer** Time slot allocated for VMINT arbiter to accept high priority requests from VD Write Queue. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the high priority requests from VD Write Queue can be continuously served for that much of time. Please refer to Figure 26 for the illustration of the arbiter's structure. 000: Infinite, If granted, high priority requests in the VD Write Queue will be served as long as there is request. However, if other requests did have their bandwidth timers (Bits [2:0], RxBA[6:4], RxBA[2:0]) be programmed as 000b and all requests come in at the same time, a priority scheme with "high write" > "high read" > "low write" > "low read" is applied. 001: 4 DCLKs. 010: 8 DCLKs. 011: 16 DCLKs. 1xx: 32 DCLKs.
3	RWS	0	**Reserved**
2:0	RWS	0	**VD Write Queue Low Priority Bandwidth Timer** Time slot allocated for VMINT arbiter to accept low priority requests from VD Write Queue. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the low priority requests from VD Write Queue can be continuously served for that much of time. Please refer to Figure 26 for the illustration of the arbiter's structure. 000: Infinite, If granted, low priority requests in the VD Write Queue will be served as long as there is request. However, if high priority requests comes in, arbiter will shift to serve high priority requests. If only low priority read requests come in at the same time, the arbiter won't shift to others until all the requests in the low priority write queues are served. 001: 4 DCLKs. 010: 8 DCLKs. 011: 16 DCLKs. 1xx: 32 DCLKs.

Offset Address: BAh (D0F3)

VMINT Arbitration Bandwidth Timer - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**Reserved**
6:4	RWS	0	**VD Read Queue High Priority Bandwidth Timer** Time slot allocated for VMINT arbiter to accept high priority requests from VD Read Queue. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the high priority requests from VD Read Queue can be continuously served for that much of time. Please refer to Figure 26 for the illustration of the arbiter's structure. 000: Infinite, If granted, high priority requests in the VD Read Queue will be served as long as there is request. However, if other requests did have their bandwidth timers (RxB9[6:4], RxB9[2:0]), Bits [2:0]) be programmed as 000b and all requests come in at the same time, a priority scheme with "high write" > "high read" > "low write" > "low read" is applied. 001: 4 DCLKs. 010: 8 DCLKs. 011: 16 DCLKs. 1xx: 32 DCLKs.
3	RWS	0	**Reserved**
2:0	RWS	0	**VD Read Queue Low Priority Bandwidth Timer** Time slot allocated for VMINT arbiter to accept low priority requests from VD Read Queue. This time slot calculated by DCLK (DRAM controller's main clock) is to guarantee that the low priority requests from VD Read Queue can be continuously served for that much of time. Please refer to Figure 26 for the illustration of the arbiter's structure. 000: Infinite, If granted, low priority requests in the VD Read Queue will be served as long as there is request. However, if high priority requests comes in, arbiter will shift to serve high priority requests. If only low priority write requests come in at the same time, the arbiter won't shift to others until all the requests in the low priority read queues are served. 001: 4 DCLKs. 010: 8 DCLKs. 011: 16 DCLKs. 1xx: 32 DCLKs.

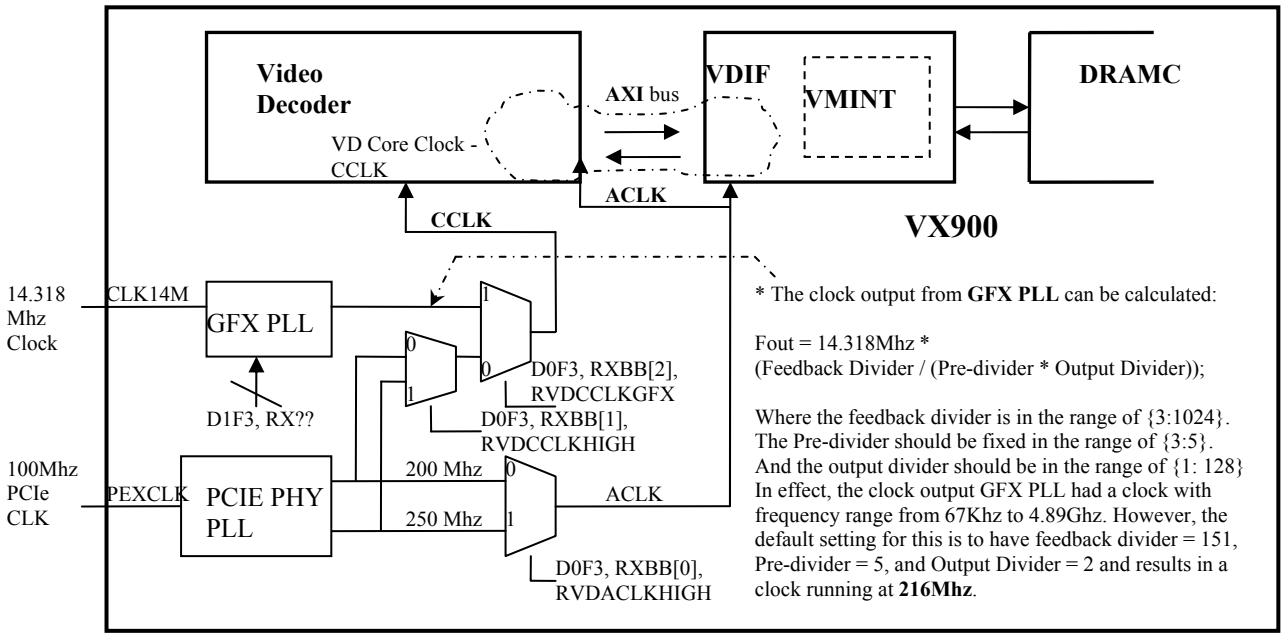


Figure 28. RxBB.1 Clocking Scheme Options Used for Video Decoder

Offset Address: BBh (D0F3)

VD Clocking **Default Value: 01h**

Bit	Attribute	HW Reset	Default	Description	Mnemonic	ChipRev	PwrDm	S	P	E
7:3	RWS	RO	0	**Reserved**	**RXBB[7:3]**		VSUS	x	x	x
2	RWS	RO	0	**VD IP Core Clock Selection Bit-1** These bits select the clock source for the VD's core clock- CCLK. **Bits [2:1]:** 00: CCLK is driven by 200Mhz clock from PCIe's PLL 01: CCLK is driven by 250Mhz clock from PCIe's PLL 1x: CCLK is driven by the output from the GFX PLL. Please refer to Figure 28 for more detail descriptions for this clock output from GFX PLL.	**RVDCCLKGFX**		VSUS	0	0	0
1	RWS	RO	0	**VD IP Core Clock Selection Bit-0** See description for bit-2.	**RVDCCLKHIGH**		VSUS	0	1	0
0	RWS	RO	1b	**Clock Selections for Interface Between VD and VDIF** This bit select the clock source for the clock between VD and VDIF – ACLK. 0: ACLK is driven by 200Mhz clock from PCIe's PLL. 1: ACLK is driven by 250Mhz clock from PCIe's PLL.	**RVDACLKHIGH**		VSUS	0	1	0

Offset Address: BCh (D0F3)

DRAM Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RWS	0	**Reserved**
2:0	RWS	0	**Arbitration Parking Policy** These bits defined the default agent who has the right to access the DRAM immediately. If there is no other requests outstanding, even the requester did not have the ownership right away, it will be granted at the next cycle. An illustration of the request arbiter is shown in Figure 19. 000: The last bus owner 001: V4IF (CPU). 010: GFX Display Engine. 011: GFX Engine. 1xx: VD (Video Decoder).

Offset Address: BD-BFh (D0F3) – Reserved

DRAM Timing Parameters (C0-CBh)

The register values at RxC0 ~ RxC8 defined the controller's behavior when accessing DRAM. The values have different meaning for DDR2 (Rx6C[7] = 0) and DDR3 (Rx6C[7] = 1) system.

Offset Address: C0h (D0F3)

DRAM Timing for All Ranks - I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	0	**CAS Latency for Write cycle – Only for DDR3** These bits defined the CAS latency for the write cycle in a DDR3 system. They are meaningless when in DDR2 system 000: 4T 001: 5T 010: 6T 011: 7T 100: 8T 101: 9T 110: 10T 111: 11T
3	RW	0	**Reserved**
2:0	RW	0	**CAS Latency** *For DDR2 System (Rx6C[7:6]=01b)*: These bits defined the CAS latency for the read/write cycles. 000: Invalid setting. 001: 3T 010: 4T 011: 5T 100: 6T 101: 7T 110: 8T 111: 9T *For DDR3 System (Rx6C[7:6]=10b)*: These bits defined the CAS latency for the read cycles. 000: 4T 001: 5T 010: 6T 011: 7T 100: 8T 101: 9T 110: 10T 111: 11T

Offset Address: C1h (D0F3)

DRAM Timing for All Ranks - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	0	**Active to Read/Write Delay (tRCD)** These bits defined the minimum latency from an Active command to a Read/Write command. *For DDR2 System (Rx6C[7:6]=01b)*: 000: 2T. 001: 3T 010: 4T 011: 5T 100: 6T 101: 7T 110: 8T 111: 9T *For DDR3 System (Rx6C[7:6]=10b)*: 000: 4T 001: 5T 010: 6T 011: 7T 100: 8T 101: 9T 110: 10T 111: 11T
3	RW	0	**Reserved**
2:0	RW	0	**Pre-charge Period (tRP)** These bits defined the minimum latency from a Pre-charge command to an Active command. *For DDR2 System (Rx6C[7:6]=01b)*: 000: 2T. 001: 3T 010: 4T 011: 5T 100: 6T 101: 7T 110: 8T 111: 9T *For DDR 3 System (Rx6C[7:6]=10b)*: 000: 4T 001: 5T 010: 6T 011: 7T 100: 8T 101: 9T 110: 10T 111: 11T

Offset Address: C2h (D0F3)

DRAM Timing for All Ranks - III **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Active to Pre-charge (tRAS)** These bits defined the minimum latency from an Active command to a pre-charge command. *For DDR2 System (Rx6C[7:6]=01b)*: 0000: 5T 0001: 6T 0010: 7T 0011: 8T 0100: 9T 0101: 10T 0110: 11T 0111: 12T 1000: 13T 1001: 14T 1010: 15T 1011: 16T 1100: 17T 1101: 18T 1110: 19T 1111: 20T *For DDR3 System (Rx6C[7:6]=10b)*: 0000: 15T 0001: 16T 0010: 17T 0011: 18T 0100: 19T 0101: 20T 0110: 21T 0111: 22T 1000: 23T 1001: 24T 1010: 25T 1011: 26T 1100: 27T 1101: 28T 1110: 29T 1111: 30T
3	RW	0	**Reserved**
2:0	RW	0	**Write Recovery Time (tWR)** These bits defined the minimum latency from a Read command to a Write command. *For DDR2 System (Rx6C[7:6]=01b)*: 000: 2T. 001: 3T 010: 4T 011: 5T 100: 6T 101: 7T 110: 8T 111: 9T *For DDR3 System (Rx6C[7:6]=10b)*: 000: 4T 001: 5T 010: 6T 011: 7T 100: 8T 101: 9T 110: 10T 111: 11T

Offset Address: C3h (D0F3)

DRAM Timing for All Ranks - IV **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Bias of Four Activate Window (tFAW)** When continuously opening DRAM pages by issuing Active commands to the same Ranks, it is required by the DRAM device (8 and more banks devices) that the fifth Active command cannot be issued until a time tFAW is met. This tFAW defined the time from the first active command to the fifth active command. These bits defined the minimum latency of (tFAW – 4 * tRRD), where rRRD is defined at Bits [2:0]. i.e. These bits defined how many extra T on top of four consecutive Active-to-Active period is required to issue the fifth Active command. This requirement is not maintained unless the RxC4[7] is enabled. *For DDR3 and DDR2 System*: 0000: 0T 0001: 1T 0010: 2T 0011: 3T 0100: 4T 0101: 5T 0110: 6T 0111: 7T 1000: 8T 1001: 9T 1010: 10T 1011: 11T 1100: 12T 1101: 13T 1110: 14T 1111: 15T
3	RW	0	**Reserved**
2:0	RW	0	**Active-to-Active Period (tRRD)** These bits defined the minimum latency from an Active command to an Active command. They applied to both DDR2 and DDR3 system: *For DDR3 and DDR2 System*: 000: 2T. 001: 3T 010: 4T 011: 5T 100: 6T 101: 7T 110: 8T 111: 9T

Offset Address: C4h (D0F3)

DRAM Timing for All Ranks - V **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**8-Bank Device Timing Constraint** For supporting 8 Banks DRAM, there are some timing constraints might need to be added to the timing parameters for 4 banks (or less) device. This bit enabled the support for this extra timing constraints. It affects the timing requirement on RxC3[7:4], RxC5[5:0], and RxC8[1:0]. 0: Disabled. 1: Enabled.
6	RW	0	**Reserved**
5:4	RW	0	**Read to Pre-charge Delay (tRTP)** These bits defined the minimum latency from a Read command to a Pre-charge command. *For DDR2 System (Rx6C[7:6]=01b)*: 00: 2T. 01: 3T 10: 4T 11: 5T *For DDR3 System (Rx6C[7:6]=10b)*: 00: 3T. 01: 4T 10: 5T 11: 6T When Rx61[5] is 1, one more T will be added for this latency.
3	RW	0	**Reserved**
2:0	RW	0	**Write to Read Command Delay (tWTR)** These bits defined the minimum latency from a Write command to a Pre-charge command. When worked with DDR3 memory, 000b is an invalid setting. *For DDR3 and DDR2 System*: 000: 2T. 001: 3T 010: 4T 011: 5T 100: 6T 101: 7T 110: 8T 111: 9T

Offset Address: C5h (D0F3)

DRAM Timing for All Ranks - VI **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**CKE Assertion Minimum Pulse Width** These bits defined the minimum assertion pulse width of the MCKE[3:0]. They applied to both DDR2 and DDR3 system (Rx6C[7] = 0 or 1). 00: 1T 01: 2T 10: 3T 11: 4T When D0F4 RxA1[6] = 0, except entering the Self-Refresh (the controller de-asserts MCKE[3:0] after it program the DRAM to enter self-refresh), the MCKE[3:0] will be always asserted. And thus, these two bits become meaningless.
5:0	RW	0	**Refresh-to-Active or Refresh-to-Refresh (tRFC)** These bits defined the minimum latency from an Auto-Refresh command to an Active command and/or from an Auto-Refresh command to an Auto-Refresh command. They applied to both DDR2 and DDR3 system (Rx6C[7] =0 or 1). This number changes when 8 bank device timing constraint is enabled: ***RxC4[7] = 0*:** 00h: 10T 01h: 11T 02h: 12T 03h: 13T … mnh: (10+m*16+n)T 3Eh: 72T 3Fh: 73T ***RxC4[7] = 1*:** 00: 30T 01h: 32T 02h: 34T 03h: 36T ... mnh: (30+2*m*16+2*n)T 3Eh: 154T 3Fh: 156T

Offset Address: C6h (D0F3)

DRAM Timing for All Ranks -VII **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Minimum Latency from the Exiting of Self Refresh to Any Command** After programming the DRAM rank to enter Self Refresh, the controller de-assert MCKE[3:0] to enter Self Refresh mode. It asserts the MCKE[3:0] to notify DRAM to exit Self Refresh. These bits defined the minimum latency from the assertion of MCKE[3:0] to any commands when the controller directs the DRAM to exit Self Refresh. It applied to both DDR2 and DDR3 system (Rx6C[7] =0 or 1). 0: 200T 1: 512T For working properly with DDR3 (Rx6C[7]=1) system, this bit has to be set at 1.
6:3	RW	0	**Reserved**
2:0	RW	0	**Minimum Latency from Power Down Exit to Any Command** MCKE[3:0] de-assertion is the way to enter the Power Down mode. It is OK for DRAM to be in either Active (any bank opened) or Pre-charged (all banks pre-charged) state when MCKE[3:0] is de-asserted. When exiting power down mode, the controller asserts the MCKE[3:0] again. These two bits define the minimum latency from the assertion of MCKE[3:0] to the first command to the DRAM bus when exiting power down mode. They applied to both DDR2 and DDR3 system (Rx6C[7] =0 or 1). 000: 1T 001: 2T 010: 3T 011: 4T 100: 5T 101: 6T 11x: 7T When Rx61[5] is 1, one more T will be added for this latency. When D0F4 RxA1[6] = 0, except entering the Self-Refresh (the controller de-asserts MCKE[3:0] after it program the DRAM to enter self-refresh), the MCKE[3:0] will be always asserted.

Offset Address: C7h (D0F3)

Refresh Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Refresh Counter** There is a refresh timer for DRAM refresh control. This timer starts counting using DCLK whenever this Refresh Counter is programmed to a value other than 0. When the timer expired with the counts defined by Refresh Counter, it issues an internal refresh request. *For DDR2 System (Rx6C[7:6] =0)*: 00h: refresh counter is disabled. 01h: 1 x 16 DCLKs. 02h: 2 x 16 DCLKs. … FFh: 255 x 16 DCLKs. *For DDR2 System (Rx6C[7:6] =1)*: 00h: refresh counter is disabled. 01h: 1 x 32 DCLKs. 02h: 2 x 32 DCLKs. … FFh: 255 x 32 DCLKs.

Offset Address: C8h (D0F3)

DRAM Timing for All Ranks - VIII **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Short ZQ Calibration** The ZQ calibration in DDR3 is used both for the adjustment of the output driver and the ODT on the DRAM devices. There are two types of ZQ calibration – long and short. When a ZQ calibration command (long or short) is put to the DRAM bus, the DRAM device would do the self adjustment on the strength of its driver and ODT in order to maintain the high quality on its bussed signals. Long ZQ calibration always goes with the initialization sequence -- note that there are two kinds of initialization – Software based (Rx6B[2:0]) and Hardware based (RxCC[0]). This bit is to enable the Short ZQ calibration. When this bit is 1, every 16 * 1024 internal refresh requests (programmed at RxC7, refer to note) will trigger the controller to issue a Short ZQ calibration command to DRAM to let the DDR3 device do short ZQ calibration. 0: Disabled. 1: Enabled. If it is a DDR2 system (Rx6C[7] =0), this bit must be set to 0.
6:2	RW	0	**Reserved**
1:0	RW	0	**Pre-charge All period (Especially for 8-bank Devices)** These bits defined the minimum latency from a pre-charge all command to an active command. For 4 (or 2) bank devices, the pre-charge all period could be the same as pre-charge period (defined in RxC1[2:0]). Thus, the minimum latency of pre-charge all period in the controller depends on RxC4[7]: These bits applied to both DDR2 and DDR3 system (Rx6C[7] = 0 or 1). ***RxC4[7] = 0*:** xx: The minimum latency = what defined by RxC1[2:0]. ***RxC4[7] =1***: 00: The minimum latency = what defined by RxC1[2:0]. 01: The minimum latency = what defined by RxC1[2:0] +1T. 10: The minimum latency = what defined by RxC1[2:0] +2T. 11: The minimum latency = what defined by RxC1[2:0] +3T.

Note: The time interval in between two Short ZQ Calibrations for a typical DDR3 system with different setting on RxC7 could be listed as:

DDR3	DRAM Clock period (ns)	RxC7 (hex)	RxC7 (decimal)	Short Term ZQ period (ms) =RxC7*32*DRAM_Clock_Period*16*1024*10^-9
DDR3-800	2.5	60	96	125.83
		80	128	167.77
DDR3-1066	1.875	60	96	94.37
		80	128	125.83

Offset Address: CB-C9h (D0F3) – Reserved

DRAM MRS for Initialization (CC-CFh)

Offset Address: CCh (D0F3)

DRAM Mode Register Sets (MRS) Hardware Based Programming for Initialization -I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	0	**ODT Strength Bits for MRS Hardware Programming.** These bits defined ODT strength bits of EMR (MA6, MA2 in the Enhanced Mode Register of the Mode Registers) for DDR2 and MR1 (MA9, MA6, MA2 in the MR1 of the Mode Registers) for DDR3 during MRS hardware programming (when bit-0 set to 1) . They are used to set the ODT strength for the DDR2/DDR3 devices. *For DDR2 System (Rx6C[7] =0)*: x00: ODT Rtt is disabled. x01: ODT Rtt is 75 ohm. x10: ODT Rtt is 150 ohm. x11: ODT Rtt is 50 ohm. *For DDR2 System (Rx6C[7] =1)*: 000: ODT Rtt is disabled. 001: ODT Rtt is 60 ohm. 010: ODT Rtt is 120 ohm. 011: ODT Rtt is 40 ohm. 100: ODT Rtt is 20 ohm. 101: ODT Rtt is 30 ohm. 11x: Reserved. Note that option 100 and 101 are restricted to be used.
3:2	RW	0	**Output Drive Strength Bits for MRS Hardware Programming** *For DDR2 System (Rx6C[7] =0)*: Bit[3] is meaningless. Bit[2] defined the bits of (MA1) for EMR (Enhanced Mode Register of the Mode Registers of DDR2 device) when entering MRS hardware programming (when bit-0 set to 1). They are used to set the output driving strength for the DDR2 device. x0: Full strength. x1: 45% ~ 60% of the Full strength. *For DDR3 System (Rx6C[7] =1)*: They defined the bits of (MA5, MA1) for MR1 (Mode Register 1 of the Mode Registers of DDR3 device) when entering MRS hardware programming (when bit-0 set to 1). They are used to set the output driving strength for the DDR3 device. 00: RZQ/6, 40 ohm at typical case. 01: RZQ/7, 34 ohm at typical case. 1x: Reserved. Noted that the nominal value of RZQ is 240 ohm +/- 1%. RZQ is an external precision resistor connected between the ZQ ball and VSS on the DRAM DIMM. It is used for DRAM to calibrate in order to have appropriate driving strength.
1	RW	0	**MA SWAP for MRS Programming** This bit is to swap the pins {MA3, MA5, MA7, BA0} with {MA4, MA6, MA8, BA1}. When this bit is enabled, the chip internal {MA3, MA5, MA7, BA0} will be routed to pins{MA4, MA6, MA8, BA1}, and the internal {MA4, MA6, MA8, BA1} will be routed to pins {MA3, MA5, MA7, BA0}. It is used for some of the motherboard that are hard to route with the bad locations of those pins on the DIMM. Note that the MA pins swapping does not impact the normal DRAM operations, but they do affect the MRS operations. This function only worked when in DDR3 system (Rx6C[7] = 1). 0: Disabled. 1: Enabled.
0	RW1C	0	**DRAM MRS Hardware Programming Trigger** This bit is the enable bit to enter the hardware based MRS programming. 0: After the MRS hardware programming sequence is done, this bit will be reset to 0. 1: Write 1 to this bit will trigger the start of DRAM MRS hardware programming sequence.

Offset Address: CDh (D0F3)

DRAM Mode Register Sets (MRS) Hardware Based Programming for Initialization - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**This bit is used for by rank HW initialization. When enable this bit, all the CS to DRAM will be driven no matter what (Rx54-55) is. When finish HW init set this bit to 0.**
5:4	RW	0	**Dynamic ODT Bits for MRS Hardware Programming** These bits defined the Dynamic ODT bits of MR2 (MA10, MA9 in the Mode Register 2of the Mode Registers) for DDR3 during MRS hardware programming (when RxCC[0] is set to 1). They are used to set the strength of the Dynamic ODT for the DDR3 device. Note that this bit is only meaningful for DDR3 system. 00: Dynamic ODT is disabled. 01: RZQ/4, 60 ohm at typical case. 10: RZQ/2, 120 ohm at typical case. 11: Reserved. For details of the MRS structures of DDR2 and DDR3.
3:2	RW	0	**Reserved**
1	RW	0	**Refresh Rate Bit for MRS Hardware Programming** This bit defined the Refresh Rate bit of EMR2 (MA7 in the Enhanced Mode Register 2 of the Mode Registers) for DDR2 and MR2 (MA7 in the Mode Register 2 of the Mode Registers) for DDR3 during MRS hardware programming (when RxCC[0] is set to 1). They are used to set the refresh rate for the DDR2/DDR3 device. *For DDR2 System (Rx6C[7] =0)*: 0: 1X refresh rate. 1: 2X refresh rate. *For DDR3 System (Rx6C[7] =1)*: 0: 1X refresh rate (Normal, for 0 to 85 C) 1: 2X refresh rate (Extended, for 0 to 95 C)
0	RW	0	**Auto Self Refresh Bit for MRS Hardware Programming** This bit defined the Auto Self Refresh (ASR) bit of MR2 (MA6 in the Mode Register 2 of the Mode Registers) for DDR3 during MRS hardware programming (when RxCC[0] is set to 1). They are used to set the ASR features on the DDR3 device. 0: ASR is disabled. 1: ASR is enabled.

Offset Address: CE-CFh (D0F3) – Reserved

Driving Control Architecture

Registers in RxD0~RxEB are control bits for the I/O Pad driving strength and the chip's internal ODT termination strength. Since the motherboard made by different vendors could have different quality, it is better to control those driving strength using automatically adjusted method. However, in the design, we also reserved the capability to set those driving manually so that we have rooms to play with for all of the applications under different situations.

For the strength control of the chip's internal ODT which resided in the Circuit Macro for the I/O of MD[63:0], MDQM[7:0], and MDQS[3:0]P/N, there are three kinds of operating modes for their termination strength control:
{RxD3[1], RxE1[0]}:
10: Manual mode.
11: Auto Compensation Offset mode.
0x: Auto Compensation mode.

Please also refer to Figure 29 where we illustrate the control for chip's internal termination strength setting.

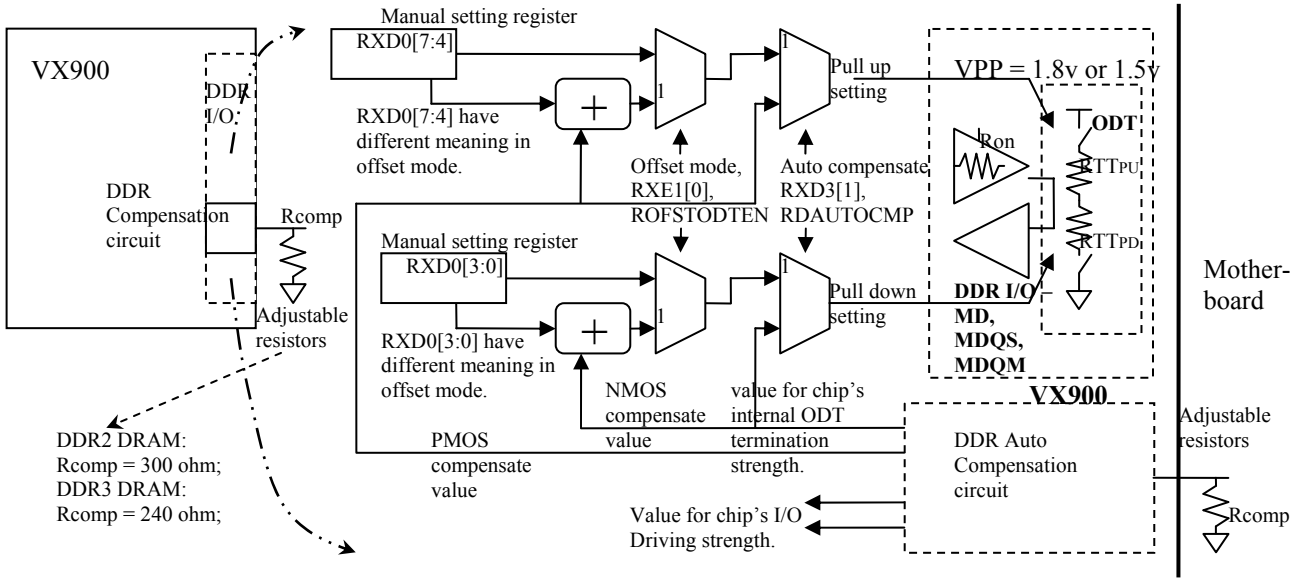


Figure 29. RxD0.1 Pull-up and Pull-down Resistance Register Control for Internal ODT Termination Strength

In **Manual mode**, the strength of the internal ODT are given directly by the manual setting register (e.g. RxD0).
In **Auto Compensation Offset mode**, the setting which send to the DDR circuit macro for the ODT strength is actually the values from the DDR Auto-compensation circuit plus/minus the value in manual setting register (RxD0). Noted that in this mode, the definition of manual setting register is different. It is now an offset to the value provided by the DDR Auto-compensation circuit. When bit[3] of the manual setting is 0, the final value to the DDR circuit macro for the internal ODT is the compensated value provided by the DDR Auto-compensation circuit plus bit[2:0] of the manual setting register with the maximum set at 1111b. When bit[3] of the manual setting is 1, the final value to the DDR circuit macro for the internal ODT is the compensated value provided by the DDR Auto-compensation circuit minus (8 – bits [2:0]) of the manual setting register with the minimum set at 0000b.
In **Auto Compensation mode**, the strength of the internal ODT are given directly by the compensated values provided from the DDR Auto-compensation Circuit.

For I/O pins MD[63:0]/MDQM[7:0], MDQS[3:0]P/N, MCS[3:0]#, MCKE[3:0], MODT[3:0], MCLKO[5:0]P/N, MA[15:0], MBA[2:0], MSCAS#, MSRAS#, MSWE#, there are two kinds of operating modes for their driving strength control:
For example, for MCS[3:0]#, RxE1[3]:

0: Manual mode.

1: Auto Compensation Offset mode.

The control bits for Auto Compensation Offset mode for those pins mentioned above can be divided into several groups:
RxE1[1], the offset mode control for MD[63:0]/MDQM[7:0];
RxE1[2], the offset mode control for MDQS[3:0]P/N;
RxE1[3], the offset mode control for MCS[3:0]#, MCKE[3:0], MODT[3:0] (as shown in Figure 30);
RxE1[4], the offset mode control for MCLKO[2:0]P/N;
RxE1[5], the offset mode control for MCLKO[5:3]P/N;
RxE1[6], the offset mode control for MA[15:0], MBA[2:0], MSCAS#, MSRAS#, MSWE#.

Please refer to the Figure 6, where MCS[3:0]# is used as an example.

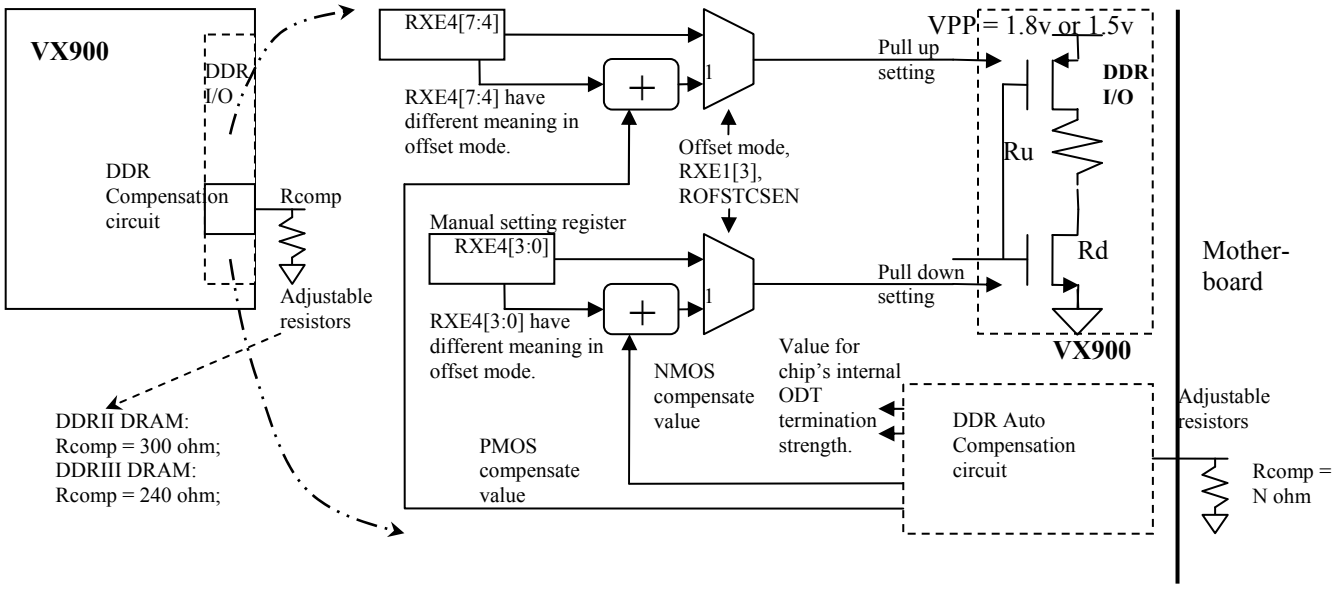


Figure 30. RxD0.2 Pull-up and Pull-down Resistance Register Control for Driving Strength of MCS[3:0]#

In **Manual mode**, the driving strength of the I/O are given directly by the manual setting register (e.g. RxE4 for MCS[3:0]#).
In **Auto Compensation Offset mode**, the setting which send to the I/O is actually the values from the DDR Auto-compensation circuit plus/minus the value in manual setting register. Noted that in this mode, the definition of manual setting register is different. It is now an offset to the value provided by the DDR Auto-compensation circuit. When bit[3] of the manual setting is 0, the final value to the I/O pad is the compensated value plus bit[2:0] of the manual setting register with the maximum set at 1111b. When bit[3] of the manual setting is 1, the final value to the I/O pad is the compensated value minus (8 – bits [2:0]) of the manual setting register with the minimum set at 0000b.

DDR2/DDR3 – I/O Pad Termination and Driving Control (D0–DFh)

Offset Address: D0h (D0F3)

Manual Control for On Die Termination (ODT) Strength **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up ODT Strength Manual Setting** These registers are the pull-up strength setting for the chip's internal ODT. Please refer to the Figure 29 and the paragraph beneath it. ***Manual Mode*:** {RxD3[1], RxE1[0]} = 10b: These register bits define the pull-up driving of the chip's internal ODT: a) When the system is working with high voltage I/O DRAM (1.8V, Rx6C[5] = 0): 0000: 248ohm 0001: 229 ohm 0010: 213 ohm 0011: 199 ohm 0100: 187 ohm 0101: 176 ohm 0110: 166 ohm 0111: 157 ohm 1000: 149 ohm 1001: 142ohm 1010: 136 ohm 1011: 130 ohm 1100: 125 ohm 1101: 120 ohm 1110: 115 ohm 1111: 110 ohm b) When the system is working with low voltage I/O DRAM (1.5V, Rx6C[5] = 1): 0000: 193 ohm 0001: 182 ohm 0010: 172 ohm 0011: 163 ohm 0100: 141 ohm 0101: 135 ohm 0110: 129 ohm 0111: 124 ohm 1000: 111 ohm 1001: 107 ohm 1010: 103 ohm 1011: 100 ohm 1100: 91 ohm 1101: 89 ohm 1110: 86 ohm 1111: 84 ohm Note the value is based on a typical case, it might vary from -25% to 30%. Also noted that the strength value is obtained when RxD5[3:2] is 00b. When RxD5[3:2] = 01b, the value above becomes one half of its current value. When RxD5[3:2]=1-b, the value above will drop to only 1/3. ***Auto Compensation Offset Mode*:** {RxD3[1], RxE1[0]} = 11b: These register bits define an offset value to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of the chip's internal ODT = RxD1[7:4] + bits [2:0] of this bits with a maximum value set at 1111b; 1xxx: The pull-up driving setting of the chip's internal ODT = RxD1[7:4] – (8 – bits [2:0]) of this bits with a minimum value set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0. ***Auto Compensation Mode*:** {RxD3[1], RxE1[0]} = 0-b: These register bits do not have impact to the pull-up ODT driving.
3:0	RW	0	**Pull-Down ODT Strength Manual Setting** These registers are the pull-down strength setting for the chip's internal ODT. Please refer to the Figure 29 and the paragraph beneath it.. ***Manual Mode*:** {RxD3[1], RxE1[0]} = 10b: These register bits define the pull-down driving of the chip's internal ODT: a) When the system is working with high voltage I/O DRAM (1.8V, Rx6C[5] = 0): 0000: 245 ohm 0001: 227 ohm 0010: 210 ohm 0011: 197 ohm 0100: 184 ohm 0101: 174 ohm 0110: 164 ohm 0111: 155 ohm 1000: 148 ohm 1001: 141 ohm 1010: 134 ohm 1011: 129 ohm 1100: 123 ohm 1101: 118 ohm 1110: 114 ohm 1111: 110 ohm b) When the system is working with low voltage I/O DRAM (1.8V, Rx6C[5] = 1): 0000: 191 ohm 0001: 180 ohm 0010: 170 ohm 0011: 161 ohm 0100: 139 ohm 0101: 133 ohm 0110: 128 ohm 0111: 123 ohm 1000: 110 ohm 1001: 106 ohm

			1010: 102 ohm 1011: 99 ohm 1100: 91 ohm 1101: 88 ohm 1110: 86 ohm 1111: 83 ohm Note the value is based on a typical case, it might vary from -25% to 30%. Also noted that the strength value is obtained when RxD5[3:2] is 00b. When RxD5[3:2] = 01b, the value above becomes one half of its current value. When RxD5[3:2]=1-b, the value above will drop to only 1/3. ***Auto Compensation Offset Mode*:** {RxD3[1], RxE1[0]} = 11b: These register bits define an offset value to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-down driving setting of the chip's internal ODT = RxD1[3:0] + bits [2:0] of this bits with a maximum value set at 1111b; 1xxx: The pull-down driving setting of the chip's internal ODT = RxD1[3:0] – (8 – bits [2:0]) of this bits with a minimum value set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0. ***Auto Compensation Mode*:** {RxD3[1], RxE1[0]} = 0-b: These register bits do not have impact to the pull-down ODT driving.

Offset Address: D1h (D0F3)

On Die Termination (ODT) Strength from DDR Auto-Compensation Circuit **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Pull-Up ODT Strength from DDR Auto-Compensation Circuit** These bits comes from the DDR Auto-Compensation circuit. It indicates the pull-up ODT strength suggested by that circuitry. The values of these 4 bits depends on the setting on RxD3[1:0]: 1x: 1111b. 00: 1111b. 01: These four bits reflect the pull-up driving setting of the internal ODT provided by the DDR Auto-Compensation Circuit. As for how these register bits apply to the pull-up driving of the internal ODT, please refer to the register descriptions of RxD0[7:4].
3:0	RO	HwInit	**Pull-Down ODT Strength from DDR Auto-Compensation Circuit** These bits comes from the DDR Auto-Compensation circuit. It indicates the pull-down ODT strength suggested by that circuitry. The values of these 4 bits depends on the setting on RxD3[1:0]: 1x: 0000b. 00: 0000b. 01:These four bits reflect the pull-down driving setting of the internal ODT provided by the DDR Auto-Compensation Circuit. As for how these register bits apply to the pull-down driving of the internal ODT, please refer to the register descriptions of RxD0[3:0].

Offset Address: D2h (D0F3)

I/O Driving Strength from DDR Auto-Compensation Circuit **Default Value: nnh**

Bit	Attribute	Default	Description
7:4	RO	HwInit	**Pull-Up I/O Driving Strength from DDR Auto-Compensation Circuit** These bits comes from the DDR Auto-Compensation circuit. It indicates the pull-up I/O Driving strength for MD, MDQS, MDQM, MCS#, MCKE, MODT, MCLKO, MA, MBA, MSCAS#, MSRAS#, and MSWE# suggested by that circuitry. The values of these 4 bits depends on the setting on RxD3[1:0]: 1x: 1111b. 00: 1111b. 01: These four bits reflect the pull-up driving setting of the I/O pins provided by the DDR Auto-Compensation Circuit. As for how these register bits apply to the pull-up driving of the I/O pins, please refer to Figure 30 and the paragraph beneath it. Register descriptions on RxE0~RxEA also shows the usages of these bits.
3:0	RO	HwInit	**Pull-Down I/O Driving Strength from DDR Auto-Compensation Circuit** These bits comes from the DDR Auto-Compensation circuit. It indicates the pull-down I/O Driving strength for MD, MDQS, MDQM, MCS#, MCKE, MODT, MCLKO, MA, MBA, MSCAS#, MSRAS#, and MSWE# suggested by that circuitry. The values of these 4 bits depends on the setting on RxD3[1:0]: 1x: 0000b. 00: 0000b. 01: These four bits reflect the pull-down driving setting of the I/O pins provided by the DDR Auto-Compensation Circuit. As for how these register bits apply to the pull-up driving of the I/O pins, please refer to Figure 30 and the paragraph beneath it. Register descriptions on RxE0~RxEA also shows the usages of these bits.

Offset Address: D3h (D0F3)

DDR Auto Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Auto Compensation Mode for ODT Strength Setting.** This bit work with RxE1[0] to control the ODT strength setting mode. Please refer to Figure 29 and the paragraph beneath it. Please also refer to the descriptions of RxD0 for more information. 0: ODT Auto Compensation Mode is enabled. 1: ODT Auto Compensation Mode is disabled.
0	RW	0	**Auto Compensation Circuit Function Enable** Disabling DDR Auto Compensation circuit by setting this bit to 0 provides better power saving; However, the values of RxD1 and RxD2 should be ignored since the PMOS setting will be set to 1111b and the NMOS setting will be set to 0000b. Please refer to register descriptions of RxD1 and RxD2 for more information. 0: Disabled. 1: Enabled.

Offset Address: D4h (D0F3)

Internal ODT Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Chip Internal ODT Dynamic On/Off Enable** This bit enables the dynamic on/off function for internal ODT which works with pins MD[63:0], MDQM[7:0], and MDQS[7:0]P/N for data integrity at high speed. It works with bit-1 to control the on/off for the ODT. **{Bit [7], Bit [1]}** x1: Internal ODT is always turned on. 00: Internal ODT is always turned off. 10: Internal ODT is dynamically turned on and off depends on the current DRAM cycles.
6:2	RW	0	**Reserved**
1	RW	0	**Chip Internal ODT On/Off Switch** This bit turn on the internal ODT for MD[63:0], MDQM[7:0], and MDQS[7:0]P/N. It works with bit-7 to control the on/off for the ODT. **{Bit [7], Bit [1]}** x1: Internal ODT is always turned on. 00: Internal ODT is always turned off. 10: Internal ODT is dynamically turned on and off depends on the current DRAM cycles.
0	RW	0	**Reserved**

Offset Address: D5h (D0F3)

MD / MDQM / MDQS Driving Selection and ODT Range Selection **Default Value: 00h**

<table>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>7</td><td>RW</td><td>0</td><td>Driving Selection for MD/MDQM/MDQS
This bit select the driving strength for pins MD[63:0], MDQM[7:0], MDQS[7:0]P/N. Under the same driving bits setting, the driving strength of the pins with Strong driving setting is about 30% ~ 60% stronger (less resistance) than that with Weak driving setting. Please refer to the driving setting bits at RxE0, RxE2.

0: Weak driving. 1: Strong driving.

Note that when working with low voltage I/O DRAM (Rx6C[5] = 1), it is recommended to set this bit to 0. Under normal situation for these low voltage I/O DRAM, the driving selection in RxE0 and RxE2 should be sufficient enough to cover all cases with this bit set to 0.</td></tr>
<tr><td>6:4</td><td>RW</td><td>0</td><td>Reserved</td></tr>
<tr><td>3:2</td><td>RW</td><td>0</td><td>ODT Range Selection
These bits control how many ODT blocks in the MD[63:0], MDQM[7:0], and MDQS[7:0]P/N are enabled. Two sets of ODT enabled had an effective 1/2 resistance as that of only one set of ODT enabled. Three sets of ODT enabled had an effective 1/3 resistance than that of only one set of ODT enabled. For working with 1.8V and 1.5V I/O DRAM, the controller will have different ODT range. The status of pin MEMDET during the reset determines which system (High I/O -1.8V or low I/O - 1.5V*1) it will be. Please refer to register descriptions of Rx6C[5] for more information.
00 : Only on set of ODT block enabled. The typical effective resistance for the ODT is150 ohm (High I/O - 1.8V) / 120 ohm (Low I/O – 1.5V).
01 : Two sets of ODT blocks enabled. The typical effective resistance for the ODT is 75 ohm (High I/O - 1.8V) / 60 ohm (Low I/O – 1.5V).
1x : Three sets of ODT blocks enabled. The typical effective resistance for the ODT is 50 ohm (High I/O - 1.8V) / 40 ohm (Low I/O – 1.5V).
It is suggested to program as the following table shown on different system:
<table>
<tr><th>Suggested value</th><th>DRAM existed only on 1 DIMM</th><th>DRAM existed on 2 DIMMs</th></tr>
<tr><td>High I/O – 1.8v system</td><td>01</td><td>00</td></tr>
<tr><td>Low I/O – 1.5v system</td><td>01</td><td>00</td></tr>
</table>
</td></tr>
<tr><td>1:0</td><td>RW</td><td>0</td><td>Reserved</td></tr>
</table>

*1: For DDR3 DRAM, they are mostly operated at Low I/O – 1.5v. For DDR2 DRAM, they could be operated at High (1.8v) or Low (1.5v) I/O mode.

Offset Address: D6h (D0F3)

MCLK / MA / MCS Driving Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Driving Selection for MCLKO to DIMM0** This bit select the driving strength for pins MCLKO[2:0]P/N. Under the same driving bits setting, the driving strength of the pins with Strong driving setting is about 30% ~ 60% stronger (less resistance) than that with Weak driving setting. Please refer to the driving setting bits at RxE6. 0: Weak driving 1: Strong driving Note that when worked with low voltage I/O DRAM (Rx6C[5] = 1) , it is recommended to set this bit to 0. Under normal situation for these low voltage I/O DRAM, the driving selection in RxE6 should be sufficient enough to cover all cases with this bit set to 0. Also note that in a system with high voltage I/O DRAM (DDR2), it is recommended to set this bit to 0/1 for motherboard without/with serial resistance on the MCLKO path.
6	RW	0	**Driving Selection for MCLKO to DIMM1** This bit select the driving strength for pins MCLKO[5:3]P/N. Under the same driving bits setting, the driving strength of the pins with Strong driving setting is about 30% ~ 60% stronger (less resistance) than that with Weak driving setting. Please refer to the driving setting bits at RxE7. 0: Weak driving 1: Strong driving Note that when worked with low voltage I/O DRAM (Rx6C[5] = 1) , it is recommended to set this bit to 0. Under normal situation for these low voltage I/O DRAM, the driving selection in RxE7 should be sufficient enough to cover all cases with this bit set to 0. Also note that in a system with high voltage I/O DRAM (DDR2), it is recommended to set this bit to 0/1 for motherboard without/with serial resistance on the MCLKO path..
5	RW	0	**Driving Selection for MA and DRAM commands** This bit select the driving strength for pins MA[15:0], MBA[2:0], MSRAS#, MSCAS# and MSWE#. Under the same driving bits setting, the driving strength of the pins with Strong driving setting is about 30% ~ 60% stronger (less resistance) than that with Weak driving setting. Please refer to the driving setting bits at RxE8. 0: Weak driving 1: Strong driving Note that when worked with low voltage I/O DRAM (Rx6C[5] = 1) , it is recommended to set this bit to 0. Under normal situation for these low voltage I/O DRAM, the driving selection in RxE8 should be sufficient enough to cover all cases with this bit set to 0.
4	RW	0	**Reserved**
3	RW	0	**Driving Selection for MCS/MCKE/ MODT** This bit select the driving strength for pins MCS[3:0]#, MCKE[3:0], and MODT[3:0]. Under the same driving bits setting, the driving strength of the pins with Strong driving setting is about 30% ~ 60% stronger (less resistance) than that with Weak driving setting. Please refer to the driving setting bits at RxE4. 0: Weak driving 1: Strong driving Note that when worked with low voltage I/O DRAM (Rx6C[5] = 1) , it is recommended to set this bit to 0. Under normal situation for these low voltage I/O DRAM, the driving selection in RxE4 should be sufficient enough to cover all cases with this bit set to 0.
2:0	RW	0	**Reserved**

Offset Address: D7-D9h (D0F3) – Reserved

Offset Address: DAh (D0F3)

NB POWER STATE **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RO	0	**Chip Internal POWER States** These three bits indicate what power states the internal state machines are at, please refer below table for details.

Bits [2:0]	C-state State Machine	S-state State Machine
000	C0 (Fully on) state	S0 (Fully on) state.
001	C2 (CPU Clock Stop) state	S0 (Fully on) state
010	C4 (CPU Deep Sleep) state	S0 (Fully on) state
011	C3 (CPU Sleep) state	S0 (Fully on) state
100	N/A (C-state had no power)	S3 (Suspend to DRAM) state
101	C5 (CPU Deepest Sleep) state	S0 (Fully on) state
110	C4P (CPU Deeper Sleep) state	S0 (Fully on) state
111	Reserved	It should never be at this state.

Offset Address: DB-DFh (D0F3) – Reserved

DRAM Driving Control (E0–EBh)

Offset Address: E0h (D0F3)

DRAM Driving – Group DQS (MDQS) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up Driving Strength Manual Setting for MDQS** These registers are the pull-up (PMOS) driving setting for the MDQS[7:0]P/N. Please refer to Figure 30 and paragraph beneath it for driving setting structure. ***Manual Mode (RxE1[2])= 0*:** a) when the system is working with high voltage I/O DRAM (1.8V, Rx6C[5] =0) a.1) with RxD5[7] = 0 for Weak driving, the driving strength are: (in ohm) 0000: 70.1 0001: 60.2 0010: 52.9 0011: 47.1 0100: 42.5 0101: 38.8 0110: 35.6 0111: 32.9 1000: 30.6 1001: 28.7 1010: 27.0 1011: 25.4 1100: 24.1 1101: 22.9 1110: 21.8 1111: 21.8 a.2) with RxD5[7] = 1 for Strong driving, the driving strength are: (in ohm) 0000: 28.8 0001: 27.0 0010: 25.5 0011: 24.2 0100: 23.0 0101: 21.9 0110: 20.9 0111: 20.0 1000: 19.1 1001: 18.4 1010: 17.7 1011: 17.1 1100: 16.5 1101: 15.9 1110: 15.4 1111: 14.9 b) when the system is working with low voltage I/O DRAM (1.5V, Rx6C[5]=1), RxD5[7] must be set to 0 for Weak driving, the driving strength are: (in ohm) 0000: 90.9 0001: 75.9 0010: 65.2 0011: 57.2 0100: 51.0 0101: 46.0 0110: 41.9 0111: 38.5 1000: 35.6 1001: 33.1 1010: 31.0 1011: 29.1 1100: 27.5 1101: 26.0 1110: 24.7 1111: 23.5 Note the value is based on a typical case, it might vary from -30% to 35%. ***Auto Compensation Mode (RxE1[2])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of MDQS[7:0]P/N = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-up driving setting of MDQS[7:0]P/N = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.
3:0	RW	0	**Pull-Down Driving Strength Manual Setting for MDQS** These registers are the pull-down (NMOS) driving setting for the MDQS[7:0]P/N. Please refer to Figure 30 and paragraph beneath it for driving setting structure. ***Manual Mode (RxE1[2])= 0*:** a) when the system is working with high voltage I/O DRAM (1.8V, Rx6C[5] =0) a.1) with RxD5[7] = 0 for Weak driving, the driving strength are: (in ohm) 0000: 71.2 0001: 61.1 0010: 53.5 0011: 47.6 0100: 42.9 0101: 39.1 0110: 35.9 0111: 33.3 1000: 30.9 1001: 28.9 1010: 27.1 1011: 25.6 1100: 24.2 1101: 22.9 1110: 21.8 1111: 21.8 a.2) with RxD5[7] = 1 for Strong driving, the driving strength are: (in ohm) 0000: 28.9 0001: 27.1 0010: 25.5 0011: 24.1 0100: 22.9 0101: 21.8 0110: 20.8 0111: 19.9 1000: 19.1 1001: 18.3 1010: 17.6 1011: 16.9 1100: 16.3 1101: 15.8 1110: 15.2 1111: 14.8 b) when the system is working with low voltage I/O DRAM (1.5V, Rx6C[5]=1), RxD5[7] must be set to 0 for Weak driving, the driving strength are: (in ohm) 0000: 91.6 0001: 76.4 0010: 65.6 0011: 57.4 0100: 51.1 0101: 46.1 0110: 41.9 0111: 38.5 1000: 35.7 1001: 33.2 1010: 31.0 1011: 29.1 1100: 27.4 1101: 25.9 1110: 24.6 1111: 23.4 Note the value is based on a typical case, it might vary from -30% to 38%. ***Auto Compensation Mode (RxE1[2])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of MDQS[7:0]P/N = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-down driving setting of MDQS[7:0]P/N = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.

Offset Address: E1h (D0F3)

Auto Compensation Offset Mode for Driving Strength Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Auto Compensation Offset Mode for Driving Strength of MA and DRAM Command.** Please refer to Figure 30. The Auto Compensation Offset mode is one of the modes for the driving setting of MA[15:0], MBA[2:0], MSRAS#, MSCAS#, and MSWE#. 0: Disabled. 1: Enabled.
5	RW	0	**Auto Compensation Offset Mode for Driving Strength of DIMM1's Clock** Please refer to Figure 30. The Auto Compensation Offset mode is one of the modes for the driving setting of MCLK[5:3]P/N. 0: Disabled. 1: Enabled.
4	RW	0	**Auto Compensation Offset Mode for Driving Strength of DIMM0's Clock** Please refer to Figure 30. The Auto Compensation Offset mode is one of the modes for the driving setting of MCLK[2:0]P/N. 0: Disabled. 1: Enabled.
3	RW	0	**Auto Compensation Offset Mode for Driving Strength of MCS#/MCKE/MODT** Please refer to Figure 30. The Auto Compensation Offset mode is one of the modes for the driving setting of MCS[3:0]#, MCKE[3:0], and MODT[3:0]. 0: Disabled. 1: Enabled.
2	RW	0	**Auto Compensation Offset Mode for Driving Strength of MDQS** Please refer to Figure 30. The Auto Compensation Offset mode is one of the modes for the driving setting of MDQS[7:0]P/N. 0: Disabled. 1: Enabled.
1	RW	0	**Auto Compensation Offset Mode for Driving Strength of MD/MDQM** Please refer to Figure 30. The Auto Compensation Offset mode is one of the modes for the driving setting of MD[63:0] and MDQM[7:0]. 0: Disabled. 1: Enabled.
0	RW	0	**Auto Compensation Offset Mode for Strength Control of Internal ODT** Please refer to Figure 29. The Auto Compensation Offset mode is one of the modes for the driving setting of chip's internal ODT for MD[63:0], MDQM[7:0] and MDQS[7:0]P/N. 0: Disabled. 1: Enabled.

Offset Address: E2h (D0F3)

DRAM Driving – Group DQ (MD, MDQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up Driving Strength Manual Setting for MD & MDQM** These registers are the pull-up (PMOS) driving setting for the MD[63:0] and MDQM[7:0]. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[1])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[7:4]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[1])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of {MD[63:0], MDQM[7:0]} = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-up driving setting of {MD[63:0], MDQM[7:0]} = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.
3:0	RW	0	**Pull-Down Driving Strength Manual Setting for MD & MDQM** These registers are the pull-down (NMOS) driving setting for the MD[63:0] and MDQM[7:0]. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[1])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[3:0]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[1])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-down driving setting of {MD[63:0], MDQM[7:0]} = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-down driving setting of {MD[63:0], MDQM[7:0]} = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.

Offset Address: E3h (D0F3) – Reserved

Offset Address: E4h (D0F3)

DRAM Driving – Group CSA (MCS, MCKE, MODT) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up Driving Strength Manual Setting for MCS/MCKE/MODT** These registers are the pull-up (PMOS) driving setting for the MCS[3:0]#, MCKE[3:0], and MODT[3:0]. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[3])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[7:4]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[3])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of {MCS[3:0]#, MCKE[3:0], MODT[3:0]} = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-up driving setting of {MCS[3:0]#, MCKE[3:0], MODT[3:0]} = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.
3:0	RW	0	**Pull-Down Driving Strength Manual Setting for MCS/MCKE/MODT** These registers are the pull-down (NMOS) driving setting for the MCS[3:0]#, MCKE[3:0], and MODT[3:0]. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[3])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[3:0]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[3])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-down driving setting of {MCS[3:0]#, MCKE[3:0], MODT[3:0]} = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-down driving setting of {MCS[3:0]#, MCKE[3:0], MODT[3:0]} = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.

Offset Address: E5h (D0F3) – Reserved

Offset Address: E6h (D0F3)

DRAM Driving – Group DCLK0 (DCLK[2:0] for DIMM0) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up Driving Strength Manual Setting for MCLKO[2:0]P/N** These registers are the pull-up (PMOS) driving setting for the MCLKO[2:0]P/N. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[4])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[7:4]. Please refer to them for the exact value. ***Auto Compensation Mode(RxE1[4])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of MCLKO[2:0]P/N = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-up driving setting of MCLKO[2:0]P/N = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.
3:0	RW	0	**Pull-Down Driving Strength Manual Setting for MCLKO[2:0]P/N** These registers are the pull-down (NMOS) driving setting for the MCLKO[2:0]P/N. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[4])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[3:0]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[4])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-down driving setting of MCLKO[2:0]P/N = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-down driving setting of MCLKO[2:0]P/N = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.

Offset Address: E7h (D0F3)

DRAM Driving – Group DCLK1 (DCLK[5:3] for DIMM1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up Driving Strength Manual Setting for MCLKO[5:3]P/N** These registers are the pull-up (PMOS) driving setting for the MCLKO[5:3]P/N. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[5])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[7:4]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[5])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of MCLKO[5:3]P/N = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-up driving setting of MCLKO[5:3]P/N = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.
3:0	RW	0	**Pull-Down Driving Strength Manual Setting for MCLKO[5:3]P/N** These registers are the pull-down (NMOS) driving setting for the MCLKO[5:3]P/N. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[5])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[3:0]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[5])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-down driving setting of MCLKO[5:3]P/N = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-down driving setting of MCLKO[5:3]P/N = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.

Offset Address: E8h (D0F3)

DRAM Driving – Group MA (MA, MBA, MSRAS, MSCAS, MSWE) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Pull-Up Driving Strength Manual Setting for MA/MBA/Commands** These registers are the pull-up (PMOS) driving setting for the MA[15:0], MBA[2:0], MSRAS#, MSCAS#, and MSWE#. Please refer to Figure 30 and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[6])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[7:4]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[6])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-up driving setting of {MA, MBA, MSRAS#, MSCAS#, MSWE#} = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-up driving setting of {MA, MBA, MSRAS#, MSCAS#, MSWE#} = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.
3:0	RW	0	**Pull-Down Driving Strength Manual Setting for MA/MBA/Commands** These registers are the pull-down (NMOS) driving setting for the MA[15:0], MBA[2:0], MSRAS#, MSCAS#, and MSWE#. Please refer to Figure 30and the paragraph beneath it for the driving setting structure. ***Manual Mode (RxE1[6])= 0*:** The driving strength indicated by these four bits are the same as those stated in the descriptions for Manual mode of RxE0[3:0]. Please refer to them for the exact value. ***Auto Compensation Mode (RxE1[6])= 1*:** These register bits define an offset to the value provided by the DDR Auto-Compensation Circuit. 0xxx: The pull-down driving setting of {MA, MBA, MSRAS#, MSCAS#, MSWE#} = (RxD2[7:4] + bits [2:0] of these bits) with a maximum set at 1111b. 1xxx: The pull-down driving setting of {MA, MBA, MSRAS#, MSCAS#, MSWE#} = (RxD2[7:4] – (8 – bits [2:0]) of these bits) with a minimum set at 0000b. When it is 1000b, the final value is to minus 8 instead of 0.

Offset Address: E9h (D0F3)

DQ/DQM Duty Control Byte 0/1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MD/MDQM Output Even Beats Delay Byte 1** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 1** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MD/MDQM Output Even Beats Delay Byte 0** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 0** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Offset Address: EAh (D0F3)

DQ/DQM Duty Control Byte 2/3 **Default Value: 00h**

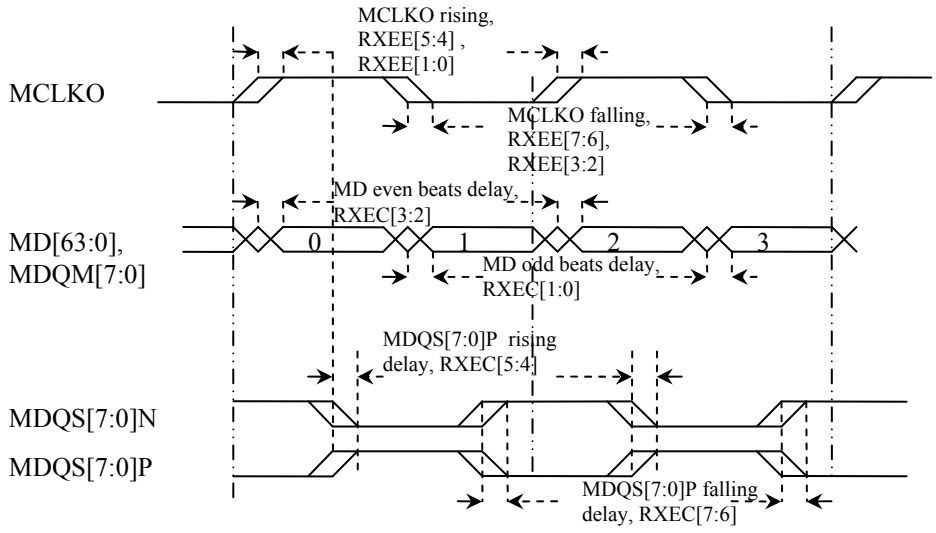
Bit	Attribute	Default	Description
7:6	RW	00b	**MD/MDQM Output Even Beats Delay Byte 3** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 3** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MD/MDQM Output Even Beats Delay Byte 2** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 2** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Offset Address: EBh (D0F3)

DQ/DQM Duty Control Byte 4/5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MD/MDQM Output Even Beats Delay Byte 5** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 5** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MD/MDQM Output Even Beats Delay Byte 4** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 4** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Output Timing Control



Output delay for some DRAM related signals are defined at RxEC~RxEE. Their related timing are illustrated in Figure 31 below.

Figure 31. RxEC.1 Output Delay Timing Control for MD, MDQM, MDQS and MCLKO

DRAM Signal Timing Control (EC–EFh)

Offset Address: ECh (D0F3)

MDQS / MD Output Delay Duty Control Byte 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 7** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 7** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MD/MDQM Output Even Beats Delay Byte 7** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 7** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Offset Address: EDh (D0F3)

DQ/DQM Duty Control Byte 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MD/MDQM Output Even Beats Delay Byte 6** These two bits control the delay of the even beats data with respect to the rising edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MD/MDQM Output Odd Beats Delay Byte 6** These two bits control the delay of the odd beats data with respect to the falling edge of internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:0	RW	0	**Reserved**

Offset Address: EEh (D0F3)

MCLK Output Duty Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Falling Edge Output Delay for MCLK of DIMM0** These bits control the delay of the falling edge of MCLKO[2:0]P (or said, the rising edge of MCLKO[2:0]N) with respect to the chip internal MCLK. 00: The delay is 0 ps. 01: The delay is 100 ps. 10: The delay is 200 ps. 11: The delay is 300 ps. The number is based on typical case, it could vary from -25% to +25%.
5:4	RW	00b	**Rising Edge Output Delay for MCLK of DIMM0** These bits control the delay of the rising edge of MCLKO[2:0]P (or said, the falling edge of MDCLKO[2:0]N) with respect to the chip internal MCLK. 00: The delay is 0 ps. 01: The delay is 100 ps. 10: The delay is 200 ps. 11: The delay is 300 ps. The number is based on typical case, it could vary from -25% to +25%.
3:2	RW	00b	**Falling Edge Output Delay for MCLK of DIMM1** These bits control the delay of the falling edge of MCLKO[5:3]P (or said, the rising edge of MCLKO[5:3]N) with respect to the chip internal MCLK. 00: The delay is 0 ps. 01: The delay is 100 ps. 10: The delay is 200 ps. 11: The delay is 300 ps. The number is based on typical case, it could vary from -25% to +25%.
1:0	RW	00b	**Rising Edge Output Delay for MCLK of DIMM1** These bits control the delay of the rising edge of MCLKO[5:3]P (or said, the falling edge of MDCLKO[5:3]N) with respect to the chip internal MCLK. 00: The delay is 0 ps. 01: The delay is 100 ps. 10: The delay is 200 ps. 11: The delay is 300 ps. The number is based on typical case, it could vary from -25% to +25%.

Input Timing Control

As mentioned in the paragraph before Rx70, there are calibrations to determine the delay for RX capture range and delay of internal RX DQS. Besides those mentioned for the calibration, this chip also provided an extra delay control for the internal MD. The related timing is illustrated in Figure 32 below.

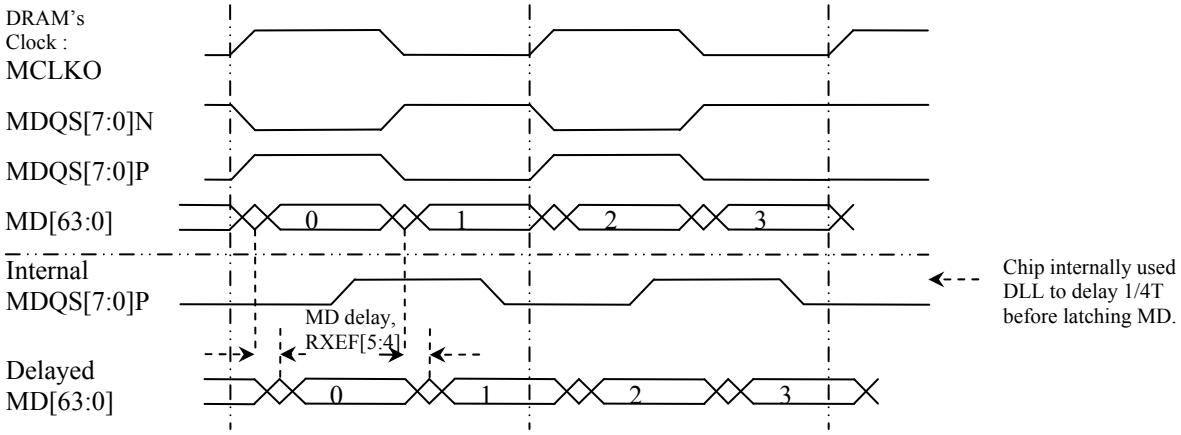


Figure 32. RxEF.1 Input Delay Timing Control for MD

Offset Address: EFh (D0F3)

MD Input Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	00b	**MD Input Delay** These bits add extra delay in the chip's internal paths of MD[63:0] for DRAM read cycles. Please refer Figure 32 for clearer timing. Chip internally latched MD with MDQS input. There are calibration mechanism for the receiving paths of this chip, please refer to Figure 21and Figure 22 for more information. 00: The delay is 200 ps. 01: The delay is 280 ps. 10: The delay is 340 ps. 11: The delay is 400 ps. The number is based on worst case, it could reduced to 50% at best case.
3:0	RW	0	**Reserved**

DRAM Memory Remap (F0–FFh)

Offset Address: F0-F7h (D0F3)-Reserved

Offset Address: FB-F8h (D0F3)

Memory Remapping **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:24	RWS	0	**Reserved**
23:14	RWS	0	**Ending Address of the Memory Remapping Range** These bits defined the ending address of the system address range defined by the Memory Remapping scheme. It's granularity is 64M bytes. Please refer to bit-0 for more details.
13:12	RWS	0	**Reserved**
11:2	RWS	0	**Beginning Address of the Memory Remapping Range** These bits defined the beginning address of the system address range defined by the Memory Remapping scheme. It's granularity is 64M bytes. Please refer to bit-0 for more details.
1	RWS	0	**Reserved**
0	RWS	0	**Memory Remapping Scheme** When this option is enabled, this chip will convert the cycles with address Addr[35:26] which addressed to the range defined by "Bits [11:2] =< Addr[35:26] < Bits [23:14]" to DRAM where used to be addressed by system hardware address space right beneath 4G. Note that it does have limitation for the programming for Ending Address (Bits [23:14]) and Beginning Address (Bits [11:2]) of the Memory Remapping Range. Ideally, considering the system application, the size of (Bits [23:14]-Bits [11:2])*64M should be larger than or equal to 64M and less than or equal to 3G (For a typical operating system to work normally, an 1G of memory under 4G is suggested by software specialist.). 0: Disabled. 1: Enabled.

Offset Address: FCh (D0F3)

DQS Output Duty Control Byte 0/1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 1** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 1** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 0** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 0** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Offset Address: FDh (D0F3)

DQS Output Duty Control Byte 2/3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 3** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 3** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 2** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 2** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Offset Address: FEh (D0F3)

DQS Output Duty Control Byte 4/5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 5** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
5:4	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 5** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
3:2	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 4** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 4** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

Offset Address: FFh (D0F3)

DQS Output Duty Control Byte 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:2	RW	00b	**MDQS[7:0]P Output Falling Edge Delay Byte 6** These two bits control the delay of the falling edge of MDQS[7:0]P (or said, the rising edge of MDQS[7:0]N) with respect to the 1/4 T delayed falling edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.
1:0	RW	00b	**MDQS[7:0]P Output Rising Edge Delay Byte 6** These two bits control the delay of the rising edge of MDQS[7:0]P (or said, the falling edge of MDQS[7:0]N) with respect to the 1/4 T delayed rising edge of the internal MCLK. Please refer to Figure 31 for clearer timing relationship. There are calibration mechanism for the transmitting paths of this chip, please refer to Figure 23 and Figure 24 for more information. 00: The delay is 0 ps. 01: The delay is 50 ps. 10: The delay is 100 ps. 11: The delay is 150 ps. The number is based on worst case, it could reduce to 50% at best case.

DEVICE 0 FUNCTION 4 (D0F4): POWER MANAGEMENT AND CHIP TESTING CONTROL

PCI Configurations

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 33 below.

Device 0 Function 4 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 4. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**100**	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

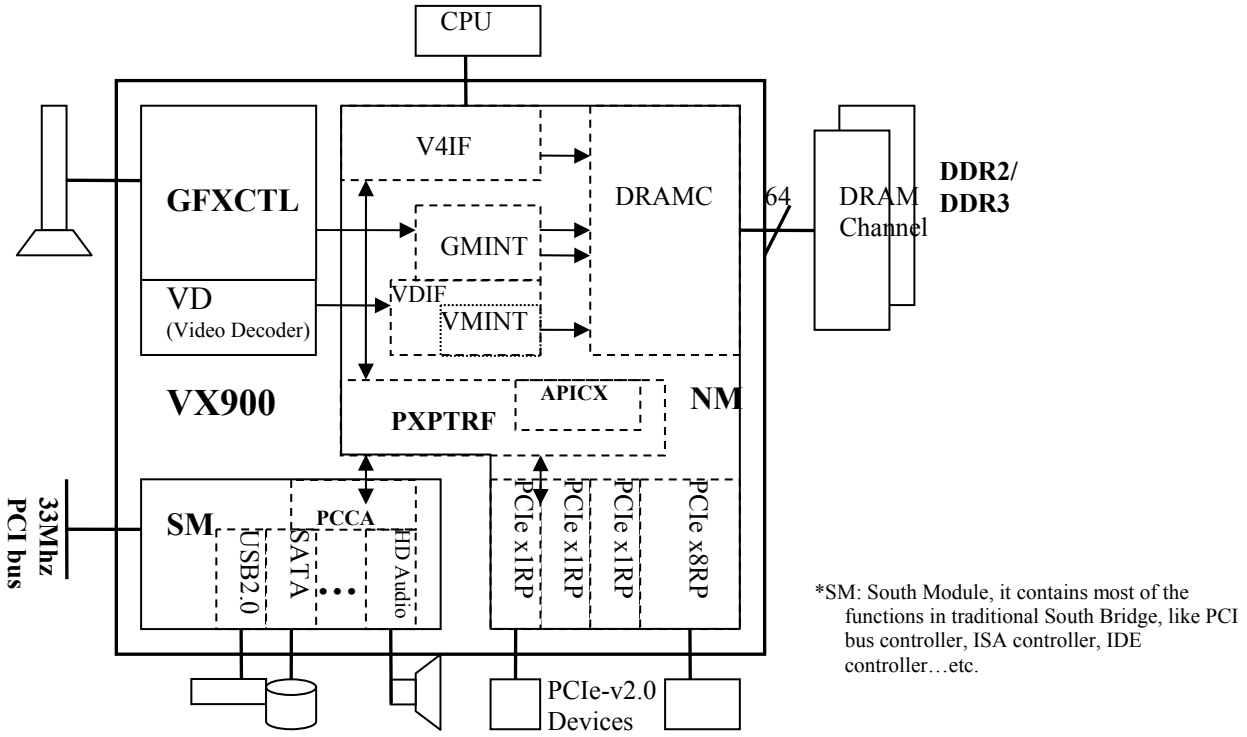


Figure 33. System Block Diagram for D0F4

The registers in this function are control registers for the power management in the NB block and testing options for PCIe module and chip top design. A software programming view for this register space D0F4 is as shown in the shaded block in Figure 34 below.

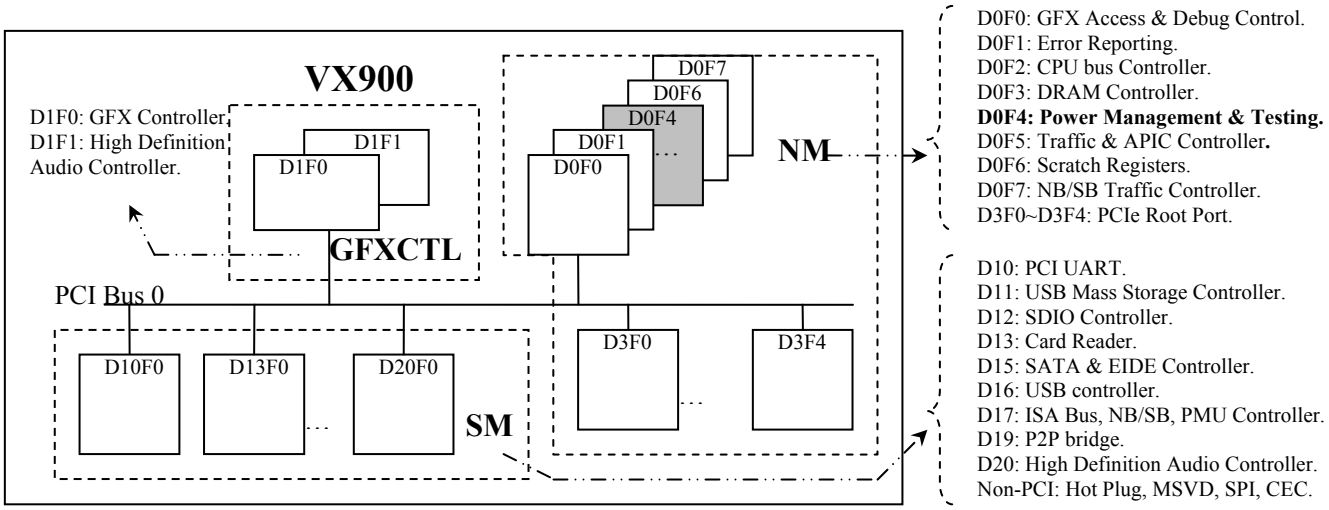


Figure 34. Register Level Block Diagram for D0F4

Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F4)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F4)

Device ID **Default Value: 4410h**

Bit	Attribute	Default	Description
15:0	RO	4410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F4)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RO	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F4)

PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RO	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RO	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	01b	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus.
8	RO	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F4)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** These bits are PCI header registers..

Offset Address: 0B-09h (D0F4)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F4)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F4)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F4)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value of these bits are 80h. It indicates this is a multi-function device.

Offset Address: 0Fh (D0F4)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F4)
Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D0F4)
Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 1B-18h (D0F4)
Base Address Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F4)
Base Address Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 3** This function does not claim base address.

Offset Address: 23-20h (D0F4)
Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 4** This function does not claim base address.

Offset Address: 27-24h (D0F4)
Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 5** This function does not claim base address.

Offset Address: 2B-28h (D0F4)
CardBus CIS Pointer **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F4)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F4)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F4) – Reserved

Offset Address: 34h (D0F4)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F4) – Reserved

Offset Address: 3D-3Ch (D0F4)
Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F4)
Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

Test Mode Registers (40-7Fh)

Offset Address: 40h (D0F4)

Test Mode Register 1 **Default Value: n0h**

Bit	Attribute	Default	Description
7	RW	0	**Core Clock for PCIe Module** This bit sets the core clock of PCIe module (PEXC). i.e. although the PCIe Link at root port 3~0 (RP0 ~ RP3) of this chip runs at either PCIe-v1.1 (2.5G) or PCIe-v2.0 (5G), the internal core clock can be running at either 250Mhz or 500Mhz. 0: 250MHz 1: 500MHz
6	RW	0 ROMSIP	**Downstream Set Slot Power Limit Message Control for PCIe Root Ports** This bit determined if the PCIe Link at root port 3~0 (RP3~RP0) sends the Set_Slot_Power_Limit messages to the device through the corresponding PCIe Link after the device detects a Link transitions from a non-DL_Up (Note 1) status to a DL_Up status. The contents in Slot Capability registers (Rx54[16:7]) of D3F0~D3F3 will be sent as message data[9:0] followed the Set_Slot_Power_Limit message for the slot power limit value. 0: Enabled, the Set_Slot_Power_Limit message will be sent 1: Disabled, the Set_Slot_Power_Limit will never be sent Notes: 1. DL_Up is a status indicating the PCIe Link is active when it is 1. Please refer to PCIe Link document. 2. This bit will be programmed during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bit is at the second QW, byte 7, bit 1 in the initialization ROM.
5	RW	0	**Reserved**
4	RW	0	**Register File BIST Mode** This BIST mode is mainly for chip testing on the testers. This bit is to turn on a feature to see if the internal register files are working properly. 0: Disabled 1: Enabled
3:2	RW	0	**Reserved**
1	RW	0	**PHYES Pattern Sequence Generation Mode** PHYES is the Circuit Macro of the PCIe Physical Electrical Sub-layer which connects to the PCIe pads (PEXTX[10:0]P/N, REXRX[10:0]P/N). This bit is to enable the RPHYEST mode to observe the pattern sending out by this chip. It is most likely used for the observation of the electrical behavior on the PCIe pins which is controlled by PHYES. 0: Disabled 1: Enabled, this chip will enter RPHYEST mode
0	RW	0	**Chip Production Test Mode for PCIe Design** This bit is for production test mode used only. When this bit is enabled, the interface in between Logic Sub-layer (LS) and Electrical Sub-Layer (ES) of the PCIe physical blocks will be pulled to the chip pins. Note that this mode is used to test on one root port only. Programmed to Rx41[1:0] to select which root port to do the this test mode. 0: Disabled. 1: Enabled.

Offset Address: 41h (D0F4)

Test Mode Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Debugging Signal Output Pad Selection** This bit is to direct some internal signals to the boundary of the chip. The signals from internal modules can be put to DRAM's MD[63:32] and GFX's Pins {VCPD[15:0], DVP1D[15:0]} to be observed when doing system debugging. GFX accessing & debugging control) for more details. 0: Internal signals directed to MD[63:32]. Noted that D0F3 Rx6C[3] is also needed to be set to 1. 1: Internal signals directed to {VCPD[15:0], DVP1D[15:0]}. Noted that D1F0 RxB9[0] is also needed to be set to 1.
4:2	RW	0	**Reserved**
1:0	RW	00b	**Root Port Selection for Chip Production Test Mode for PCIe Design** These bits are to select which root port to be selected to do the RPHYTST Test mode (Rx40[0]). 00: Root Port 0. 01: Root Port 1. 10: Root Port 2. 11: Root Port 3.

Offset Address: 42-43h (D0F4) – Reserved

Asynchronous Circuit and the Bypassing Logic for Chip Production Test Mode

Modules in this chip are running at different clocks, those clocks are basically irrelevant to each other. In order to let them normally operate, there are a lot of synchronization logic in between two modules which operated at different clock. This synchronization logic or said conversion logic guarantee the integrity of the protocol, however, it did create possible latency. An uncertainty is existed when two clocks do not have any relationship. This uncertainty in delay does not effect the normal operation – it only gives the operation one cycle of time ahead or none. However, when the chip is in production speed test mode, even we put all the clock at the same speed, we will still have timing issues due to the nature of the synchronization logic. For being able to do the high speed test on this chip, a multiplexer is added in the paths so that a bypassing path is formed which provides the stability of the production test. The registers followed at the section below are all related to these logic, only being applied to different interface in the chip.

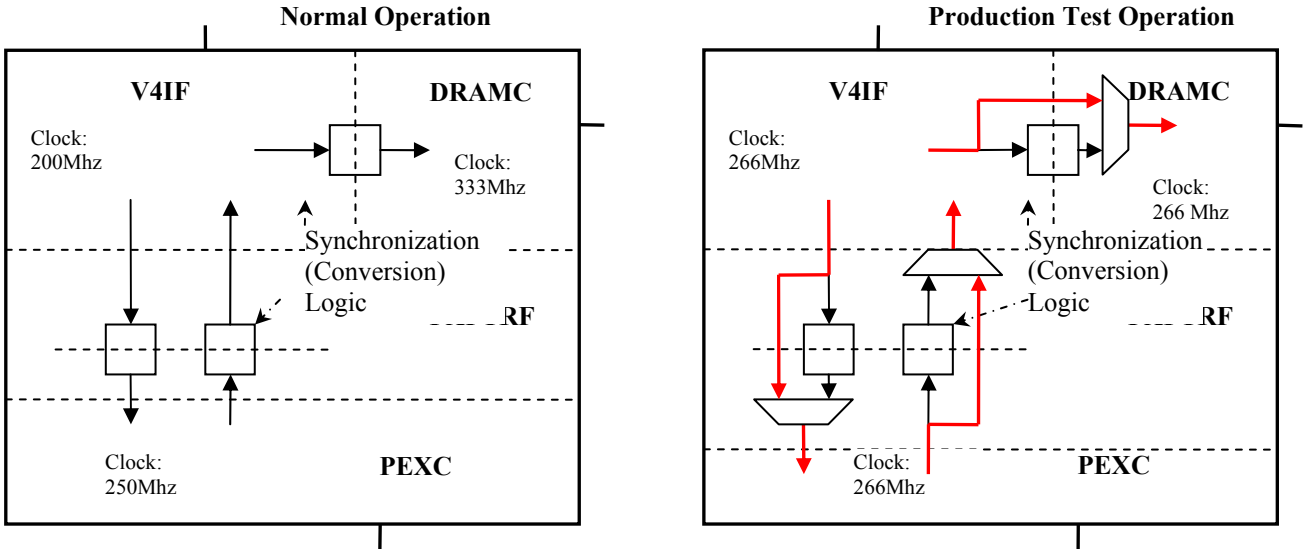


Figure 35. Rx44.1 Asynchronous Circuit & Bypassing Logic for Chip Production Test Mode

Offset Address: 44h (D0F4)

Asynchronous Circuit Testing Mode 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Bypassing Synchronization Logic for V4IF to DRAMC** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from V4IF (CPU bus controller) to DRAMC (DRAM controller) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
6	RW	0	**Bypassing Synchronization Logic for DRAMC to V4IF** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from DRAMC (DRAM controller) to V4IF (CPU bus controller) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
5	RW	0	**Reserved**
4	RW	0	**Bypassing Synchronization Logic for NBPMU to V4IF** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from NBPMU (NB's PMU controller) to V4IF (CPU bus controller) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
3	RW	0	**Bypassing Synchronization Logic for V4IF to SB** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from V4IF (CPU bus controller) to SB (Conventional SB block) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
2	RW	0	**Bypassing Synchronization Logic for SB to V4IF** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from SB (Conventional SB block) to V4IF (CPU bus controller) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
1:0	RW	0	**Reserved**

Offset Address: 45h (D0F4)

Asynchronous Circuit Testing Mode 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Bypassing Synchronization Logic for V4IF to PEXC** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from V4IF (CPU bus controller) to PEXC (PCIe Root Ports, RP3 ~ RP0) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
2	RW	0	**Bypassing Synchronization Logic for PEXC to V4IF** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from PEXC (PCIe Root Ports, RP3 ~ RP0) to V4IF (CPU bus controller) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
1:0	RW	0	**Reserved**

Offset Address: 46h (D0F4)

Asynchronous Circuit Testing Mode 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Bypassing Synchronization Logic for VD to DRAMC** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from VD (Video Decoder) to DRAMC (DRAM controller) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
6	RW	0	**Bypassing Synchronization Logic for DRAMC to VD** Please refer to Figure 35. This bit is to enable the bypassing logic which is built around the synchronization logic for signals traveling from DRAMC (DRAM controller) to VD (Video Decoder) of this chip. This bit should be enabled when generating production test vector. 0: Disabled 1: Enabled
5:0	RW	0	**Reserved**

Offset Address: 47-7Fh (D0F4) – Reserved

Power Management Control (80–FFh)

The Power Management control in the north bridge includes 1) Power management state control within NB for CPU C-states. 2) Reduction of I/O power. 3) Dynamic clock stop for clocks within the NB blocks.

Dynamic Clock Stop is the main focus in the registers following this section for the NB in terms of power saving. Please refer to Figure 33 to know which blocks are involved in the NB. With the dynamic clock stop feature, this chip detects the activities and enables the local clock in a pre-defined logic scope to maintain the integrity of the function. Thus, the normal function is maintained while the toggling of the internal clocks can be limited to some local area, which lowers the power consumption generated by the clock toggling.

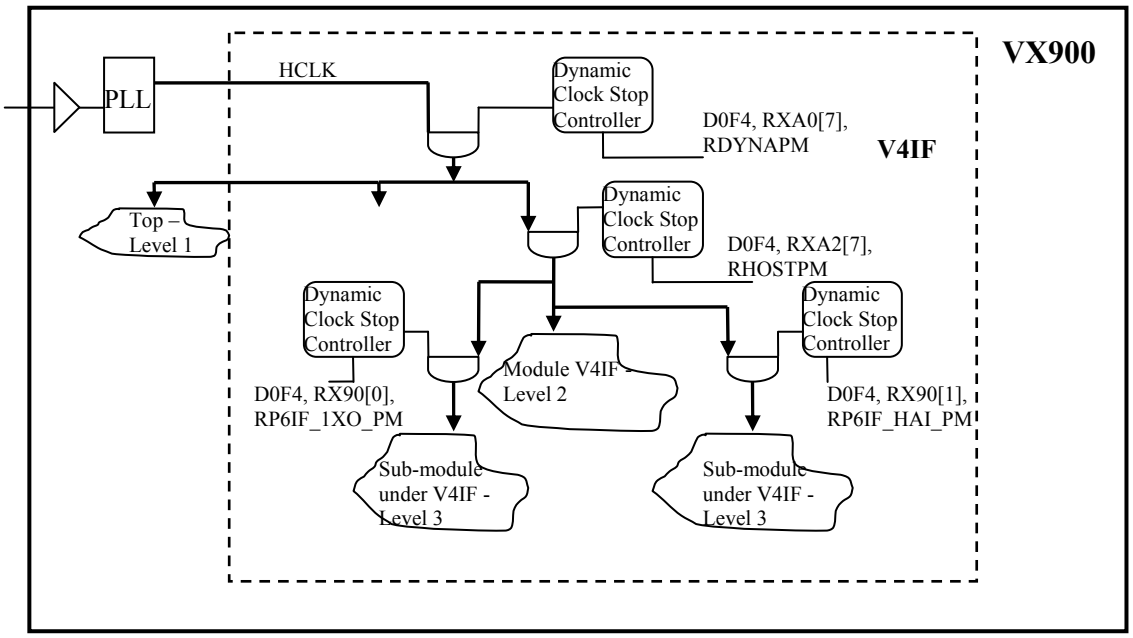


Figure 36. Rx80.1 Dynamic Clock Stop Feature - Use V4IF as An Example

In order to reduce the most power consumption, this chip divided the clock trees into several regions. Please refer to Figure 36 where we used the CPU bus controller – V4IF as an example. We had the main control of this Dynamic Clock Stop feature of this chip at D0F4 RxA0[7]. Then we had the main control for V4IF module at D0F4 RxA2[7]. Furthermore, we had D0F4 Rx90[0] and Rx90[1] for different logics for same clock source – HCLK. Thus, if there is a cycle coming from CPU to DRAM, the chip will only need to enable those clocks governed the logic of CPU accessing DRAM. Those HCLKs used for interface between V4IF and other modules will remain at low and saves power.

HCLK is only one of the clock trunks in this chip, there are many more clocks in different modules. In the following sections, there are registers to control the dynamic clock stop feature for each levels of different clocks. They had the same structure as it described here.

Offset Address: 80-83h (D0F4) – Reserved

Offset Address: 84h (D0F4)

Dynamic Clock Stop for Central Traffic Controller (PXPTRF) - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for HCLK at PXPTRF module** HCLK is the main clock for the CPU bus controller – V4IF. This bit is the level 2 control bit to enable the dynamic stop feature for the HCLK within PXPTRF module to interface with V4IF. Level 1 enabling bits for this dynamic stop feature includes RxA0[7], RxA8[6], and RxA2[7]. Register bits at Bits [4,1] are the level 3 enabling bits to control the dynamic stop feature of HCLK in the sub-functions. Please refer to bits [4,1] for more details. **{RxA0[7], RxA8[6], RxA2[7], Bit-7}:** 0xxx, 1000, 1100 or 1110: HCLK within PXPTRF toggled freely. 1111: HCLK within PXPTRF will stop toggling when there is no cycle coming from or going to V4IF existed in PXPTRF. To encourage more power saving, it is suggested to program this bit to 1.
6	RW	0	**Dynamic Stop for GCLK at PXPTRF module** GCLK is the internal 66Mhz clock to interface with SB block within PXPTRF in the chip. This bit is the level 2 control bit to enable the dynamic stop feature for the GCLK within PXPTRF module. Level1 enabling bits for this dynamic stop feature are at RxA0[7], RxA8[6]. Register bits at bits [3,0] are the level 3 enabling bits to control the dynamic stop feature of GCLK in the sub-functions. Please refer to bits [3,0] for more details. **{RxA0[7], RxA8[6], Bit-7}:** 0xx, 100, or 110: GCLK within PXPTRF toggled freely. 111: GCLK within PXPTRF will stop toggling when there is no cycles coming from or going to SB block existed in PXPTRF. To encourage more power saving, it is suggested to program this bit to 1.
5	RW	0	**Reserved**
4	RW	0	**Dynamic Stop for Downstream HCLK at PXPTRF module** Refer to the descriptions at bit-7. This bit is the dynamic stop control bit for the HCLK related to downstream cycles within PXPTRF. It works with bit-7 to control the dynamic stopping for downstream HCLK within PXPTRF. **{RxA0[7], RxA8[6], RxA2[7], Bit-7, Bit-4}:** 0xxxx, 10xxx, 110xx, or 1110x: HCLK for downstream cycles within PXPTRF toggled freely. 11110: HCLK for downstream cycles within PXPTRF will stop toggling when there is neither downstream cycle (from V4IF) nor upstream cycle (to V4IF) existed. 11111: HCLK for downstream cycles within PXPTRF will stop toggling when there is no downstream cycle coming (from V4IF) existed.
3	RW	0	**Dynamic Stop for Downstream GCLK at PXPTRF module** Refer to the descriptions at bit-6. This bit is the dynamic stop control bit for the GCLK related to downstream cycles within PXPTRF. It works with bit-6 to control the dynamic stopping for downstream GCLK within PXPTRF. **{RxA0[7], RxA8[6], Rx84[6], Bit-3}:** 0xxx, 10xx, or 110x: GCLK for downstream cycles within PXPTRF toggled freely. 1110: GCLK for downstream cycles within PXPTRF will stop toggling when there is neither downstream cycle (to devices in SM block) nor upstream cycle (from devices in SM block) existed. 1111: GCLK for downstream cycles within PXPTRF will stop toggling when there is no downstream cycle going (to devices in SM block) existed.
2	RW	0	**Dynamic Stop for APBCLK at PXPTRF Module** APBCLK is the internal 133Mhz clock to interface with VD (Video Decoder) block within PXPTRF in the chip. This bit is the level 2 control bit for the dynamic stop feature for the APBCLK. Level 1 control bits are at RxA0[7] and RxA8[6]. And the control bits for level1 & level2 combines to work here: **{RxA0[7], RxA8[6], Bit-2}:** 0xx, 10x, or 110: APBCLK within PXPTRF toggled freely. 111: APBCLK within PXPTRF will stop toggling when there is no cycle going to the VD existed.
1	RW	0	**Dynamic Stop for Upstream HCLK at PXPTRF module** Refer to the descriptions at bit-7. This bit is the dynamic stop control bit for the HCLK related to upstream cycles within PXPTRF. It works with bit-7 to control the dynamic stopping for upstream HCLK within PXPTRF. **{RxA0[7], RxA8[6], RxA2[7], Rx84[7], Bit-1}:** 0xxxx, 10xxx, 110xx,or 1110x: HCLK for upstream cycles within PXPTRF toggled freely. 11110: HCLK for upstream cycles within PXPTRF will stop toggling when there is neither downstream cycle (from V4IF) nor upstream cycle (to V4IF) existed. 11111: HCLK for upstream cycles within PXPTRF will stop toggling when there is no upstream cycle (to V4IF) existed.

0	RW	0	**Dynamic Stop for Upstream GCLK at PXPTRF module** Refer to the descriptions at bit-6. This bit is the dynamic stop control bit for the GCLK related to upstream cycles within PXPTRF. It works with bit-6 to control the dynamic stopping for upstream GCLK within PXPTRF. **{RxA0[7], RxA8[6], Rx84[6], Bit-0}:** 0xxx, 10xx, or 110x: GCLK for upstream cycles within PXPTRF toggled freely. 1110: GCLK for upstream cycles within PXPTRF will stop toggling when there is neither downstream cycles (to devices in SM block) nor upstream cycles (from devices in SM block) existed. 1111: GCLK for upstream cycles within PXPTRF will stop toggling when there is no upstream cycle (from devices in SM block) existed.

Offset Address: 85h (D0F4)

Dynamic Clock Stop for Central Traffic Controller (PXPTRF) - 2

Default Value: 00h

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Dynamic Stop for CFGCLK at PXPTRF module** CFGCLK is a 66Mhz clock and is the internal clock for the register files of the NM (North Module). This bit is the level 2 enabling bit to control the dynamic stop feature for CFGCLK. Level 1 enabling bits are at RxA0[7] and RxA2[1]. This bit works with the level 1 bits to control the CFGCLK: **{RxA0[7], RxA2[1], Bit-2}:** 0xx, 10-, or 110: CFGCLK toggled freely. 111: CFGCLK will stop toggling when there is no cycle coming from CPU existed.
1	RW	0	**Dynamic Stop for APICCLK at PXPTRF module** APICCLK is a 66Mhz clock and is the internal clock for the APIC controller in the NM (North Module). This bit is the level 2 enabling bit to control the dynamic stop feature for APICCLK. Level 1 enabling bits are at RxA0[7], RxA8[6]. This bit works with the level 1 bits to control the APICCLK: **{RxA0[7], RxA8[6], Bit-1}:** 0xx, 10x, or 110: APICCLK within PXPTRF toggled freely. 111: APICCLK within PXPTRF will stop toggling when there is no cycle coming from CPU or any interrupt events coming from PCIe RP0~RP3 or GFXCTL (Integrated Graphic Controller) existed.
0	RW	0	**Reserved**

Offset Address: 86h (D0F4)

Dynamic Clock Stop for Central Traffic Controller (PXPTRF) - 3

Default Value: 00h

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Dynamic Stop for ECLK of PCIe Downstream at PXPTRF Module** ECLK is a 250Mhz clock and is the internal clock for the PCIe root port controller. This bit is the level 2 enabling bit to control the dynamic stop feature for the ECLK used for downstream controller interfaced with all PCIe Root Port (RP0 ~ RP3) within PXPTRF module. Level 1 control bits are at RxA0[7], and RxA8[6]. This bit works with those level 1 bits to control the ECLK for PCIe downstream: **{RxA0[7], RxA8[6], Bit-0}:** 0xx, 10x, or 110x: ECLK for downstream controller to interface PCIe root ports within PXPTRF toggled freely. 1111: ECLK for downstream controller to interface PCIe root ports within PXPTRF will stop toggling when there is no downstream cycle coming from CPU or other upstream masters targeted to any root port (RP0 ~ RP3) existed.

Offset Address: 87h (D0F4)

Dynamic Clock Stop for Central Traffic Controller (PXPTRF) - 4 **Default Value: 00h**

Bit	Attribut	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Dynamic Stop for ECLK of Upstream RP3 at PXPTRF Module** ECLK is a 250Mhz clock and is the internal clock for the PCIe root port controller. This bit is the level 2 enabling bit to control the dynamic stop feature for the ECLK used for upstream controller interfaced with the Root Port3 (RP3) within PXPTRF module. Level 1 control bits are at RxA0[7] and RxA8[6]. This bit works with those level 1 bits to control the ECLK for RP3 upstream: **{RxA0[7], RxA8[6], Bit-3}:** 0xx, 10x, or 110: ECLK for upstream controller to interface RP3 within PXPTRF toggled freely. 111: ECLK for upstream controller to interface RP3 within PXPTRF will stop toggling when there is no upstream cycle coming from PCIe device connected to RP3 existed.
2	RW	0	**Dynamic Stop for ECLK of Upstream RP2 at PXPTRF Module** As described in bit-3, only that this bit is for RP2 instead of RP3. **{RxA0[7], RxA8[6], Bit-2}:** 0xx, 10x, or 110: ECLK for upstream controller to interface RP2 within PXPTRF toggled freely. 111: ECLK for upstream controller to interface RP2 within PXPTRF will stop toggling when there is no upstream cycle coming from PCIe device connected to RP2 existed.
1	RW	0	**Dynamic Stop for ECLK of Upstream RP1 at PXPTRF Module** As described in bit-3, only that this bit is for RP1 instead of RP3. **{RxA0[7], RxA8[6], Bit-1}:** 0xx, 10x, or 110: ECLK for upstream controller to interface RP1 within PXPTRF toggled freely. 111: ECLK for upstream controller to interface RP1 within PXPTRF will stop toggling when there is no upstream cycle coming from PCIe device connected to RP1 existed.
0	RW	0	**Dynamic Stop for ECLK of Upstream RP0 at PXPTRF Module** As described in bit-3, only that this bit is for RP0 instead of RP3. **{RxA0[7], RxA8[6], Bit-0}:** 0xx, 10x, or 110: ECLK for upstream controller to interface RP0 within PXPTRF toggled freely. 111: ECLK for upstream controller to interface RP0 within PXPTRF will stop toggling when there is no upstream cycle coming from PCIe device connected to RP0 existed.

Offset Address: 88h (D0F4)

Dynamic Clock Stop for APIC Controller (APICX) in NB **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for ECLK at APICX module** ECLK is a 250Mhz clock and is also the internal clock for the APICX (APIC controller in NB) to deal with signals coming from PCIe root ports (RP0 ~ RP3). This bit is the level 2 enabling bit to control the dynamic stop feature for the ECLK used for APICX. Level 1 enabling bits are at RxA0[7] and RxA2[3]. This bit works with those level 1 bits to control the ECLK within APICX: **{RxA0[7], RxA2[3], Bit-1}:** 0xx, 10x, or 110: ECLK within APICX toggled freely. 111: ECLK within APICX will stop toggling when there is no interrupt events coming from PCIe root ports existed.
0	RW	0	**Dynamic Stop for GCLK at APICX module** GCLK is a 66Mhz clock and is the main clock for the APICX (APIC controller in NB). This bit is the level 2 enabling bit to control the dynamic stop feature for the GCLK used for APICX. Level 1 enabling bits are at RxA0[7] and RxA2[3]. This bit works with those level 1 bits to control the GCLK within APICX: **{RxA0[7], RxA2[3], Bit-0}:** 0xx, 10x, or 110: GCLK within APICX toggled freely. 111: GCLK within APICX will stop toggling when there is no event needed to be handled or pending downstream command cycle existed.

Offset Address: 89h (D0F4) – Reserved

Offset Address: 8Ah (D0F4)

Dynamic Clock Stop for Graphics-Memory Interface (GMINT) - 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for DCLK of Typical Requests at GMINT Module** DCLK is the main clock used for DRAM controller (DRAMC). It is also used in the Graphic-Memory Interface (GMINT), an interface in between internal integrated graphic controller (GFXCTL) and DRAMC. This bit is the level 2 enabling bit to control the dynamic stop feature for the DCLK used for the Typical Request control logic within GMINT. Level 1 enabling bits are at RxA0[7] and RxA2[2]. This bit works with the level 1 bits to control the DCLK as: **{RxA0[7], RxA2[2], Bit-7}:** 0xx, 10x, or 110: DCLK for Typical Request Control within GMINT toggled freely. 111: DCLK for Typical Request Control within GMINT will stop toggling when there is no typical requests from GFXCTL existed.
6	RW	0	**Dynamic Stop for DCLK of Priority Requests at GMINT module** DCLK is the main clock used for DRAM controller (DRAMC). It is also used in the Graphic-Memory Interface (GMINT), an interface in between internal integrated graphic controller (GFXCTL) and DRAMC. This bit is the level 2 enabling bit to control the dynamic stop feature for the DCLK used for the Priority Request control logic within GMINT. Level 1 enabling bits are at RxA0[7] and RxA2[2]. This bit works with the level 1 bits to control the DCLK as: **{RxA0[7], RxA2[2], Bit-6}:** 0xx, 10x, or 110: DCLK for Priority Request Control within GMINT toggled freely. 111: DCLK for Priority Request Control within GMINT will stop toggling when there is no priority requests from GFXCTL existed.
5	RW	0	**Dynamic Stop for DCLK of Read Data Control at GMINT module** DCLK is the main clock used for DRAM controller (DRAMC). It is also used in the Graphic-Memory Interface (GMINT), an interface in between internal integrated graphic controller (GFXCTL) and DRAMC. This bit is the level 2 enabling bit to control the dynamic stop feature for the DCLK used in the logic of Read Data coming back from DRAMC within GMINT. Level 1 enabling bits are at RxA0[7] and RxA2[2]. This bit works with the level 1 bits to enable the DCLK as: **{RxA0[7], RxA2[2], Bit-5}:** 0xx, 10x, or 110: DCLK for Read Data Control within GMINT toggled freely. 111: DCLK for Read Data Control within GMINT will stop toggling when there is no read data coming back from DRAMC.
4:0	RW	0	**Reserved**

Offset Address: 8Bh (D0F4)

Dynamic Clock Stop for Data Path **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Dynamic Stop for DBXCLK at CMFIFO** DBX is a module handling data paths in between CPU, DRAM, and other peripheral devices. CMFIFO is a data path handling the data written from CPU to DRAM. DBXCLK is the main clock for the CMFIFO and clocked at the speed of HCLK (CPU bus' main clock) . This bit is the level 2 enabling bit to control the dynamic stop feature for the DBXCLK used for CMFIFO. Level 1 enabling bits are RxA0[7], RxA2[7], RxA8[6], and RxA2[4]. This bit works with level 1 bits to control the DBXCLK as: **{RxA0[7], RxA2[7], RxA8[6], RxA2[4], Bit-5}:** 0xxxx-, 10xxx, 110xx, 1110x, or 11110: DBXCLK for CMFIFO toggled freely. 11111: DBXCLK for CMFIFO will stop toggling when there is no write data remained in the CMFIFO or no CPU to DRAM write requests coming in.
4	RW	0	**Dynamic Stop for DBXCLK at MCFIFO** DBX is a module handling data paths in between CPU, DRAM, and other peripheral devices. MCFIFO is a data path handling the data read from DRAM to CPU. DBXCLK is the main clock for the MCFIFO and clocked at the speed of HCLK (CPU bus' main clock) . This bit is the level 2 enabling bit to control the dynamic stop feature for the DBXCLK used for MCFIFO. Level 1 enabling bits are RxA0[7], RxA2[7], RxA8[6], and RxA2[4]. This bit works with level 1 bits to control the DBXCLK as: **{RxA0[7], RxA2[7], RxA8[6], RxA2[4], Bit-4}:** 0xxxx, 10xxx, 110xx, 1110x, or 11110: DBXCLK for MCFIFO toggled freely. 11111: DBXCLK for MCFIFO will stop toggling when there is no read data remained in the MCFIFO or no CPU to DRAM read requests coming in.
3	RW	0	**Dynamic Stop for DBXCLK at CPWFIFO** DBX is a module handling data paths in between CPU, DRAM, and other peripheral devices. CPWFIFO is a data path handling the data written from CPU to peripheral devices which could be either PCIe Root ports or devices on the SB block in a downstream write cycle. DBXCLK is the main clock for the CPWFIFO and clocked at the speed of HCLK (CPU bus' main clock) . This bit is the level 2 enabling bit to control the dynamic stop feature for the DBXCLK used for CPWFIFO. Level 1 enabling bits are RxA0[7], RxA2[7], RxA8[6], and RxA2[4]. This bit works with level 1 bits to control the DBXCLK as: **{RxA0[7], RxA2[7], RxA8[6], RxA2[4], Bit-3}:** 0xxxxx, 10xxx, 110xx, 1110x, or 11110: DBXCLK for CPWFIFO toggled freely. 11111: DBXCLK for CPWFIFO will stop toggling when there is no write data remained in the CPWFIFO or no CPU to peripheral write requests coming in.
2	RW	0	**Dynamic Stop for DBXCLK at CPRFIFO** DBX is a module handling data paths in between CPU, DRAM, and other peripheral devices. CPRFIFO is a data path handling the data read from peripheral devices which could be either PCIe Root ports or devices on the SB block to CPU in a downstream read cycle. DBXCLK is the main clock for the CPRFIFO and clocked at the speed of HCLK (CPU bus' main clock) . This bit is the level 2 enabling bit to control the dynamic stop feature for the DBXCLK used for CPRFIFO. Level 1 enabling bits are RxA0[7], RxA2[7], RxA8[6], and RxA2[4]. This bit works with level 1 bits to control the DBXCLK as: **{RxA0[7], RxA2[7], RxA8[6], RxA2[4], Bit-2}:** 0xxxx, 10xxx, 110xx, 1110x, or 11110: DBXCLK for CPRFIFO toggled freely. 11111: DBXCLK for CPRFIFO will stop toggling when there is no read data remained in the CPRFIFO or no CPU to peripheral read requests coming in.
1	RW	0	**Dynamic Stop for DBXCLK at PMWFIFO** DBX is a module handling data paths in between CPU, DRAM, and other peripheral devices. PMWFIFO is a data path handling the data written from peripheral devices which could be either PCIe Root ports or devices on the SB block to CPU in an upstream write cycle. DBXCLK is the main clock for the PMWFIFO and clocked at the speed of HCLK (CPU bus' main clock) . This bit is the level 2 enabling bit to control the dynamic stop feature for the DBXCLK used for PMWFIFO. Level 1 enabling bits are RxA0[7], RxA2[7], RxA8[6], and RxA2[4]. This bit works with level 1 bits to control the DBXCLK as: **{RxA0[7], RxA2[7], RxA8[6], RxA2[4], Bit-1}:** 0xxxx, 10xxx, 110xx, 1110x, or 11110: DBXCLK for PMWFIFO toggled freely. 11111: DBXCLK for PMWFIFO will stop toggling when there is no write data remained in the PMWFIFO or no upstream write requests coming in.
0	RW	0	**Dynamic Stop for DBXCLK at PMRFIFO** DBX is a module handling data paths in between CPU, DRAM, and other peripheral devices. PMRFIFO is a data path handling the data read from CPU to peripheral devices which could be either PCIe Root ports or devices on the SB block in a upstream read cycle. DBXCLK is the main clock for the PMRFIFO and clocked at the speed of HCLK (CPU bus' main clock) . This bit is the level 2 enabling bit to control the dynamic stop feature for the DBXCLK used for PMRFIFO. Level 1 enabling bits are RxA0[7], RxA2[7], RxA8[6], and RxA2[4]. This bit works with level 1 bits to control the DBXCLK as: **{RxA0[7], RxA2[7], RxA8[6], RxA2[4], Bit-0}:** 0xxxx, 10xxx, 110xx, 1110x, or 11110: DBXCLK for PMRFIFO toggled freely. 11111: DBXCLK for PMRFIFO will stop toggling when there is no read data remained in the PMRFIFO or no upstream read requests coming in.

Offset Address: 8Ch (D0F4)

Dynamic Clock Stop for Video Decoder Interface (VDIF) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for DCLK of Write Request Control at VDIF** VDIF is the interface module in between Video Decoder (VD) and DRAM controller. It used the DRAM's DCLK as the clock. This bit is the level 2 enabling bit to control the dynamic stop feature for the DCLK used for VDIF's write control block in a VDIF write request cycle. The level 1 enabling bits are RxA0[7] and bit-0. This bit works with level 1 bits to control the DCLK in VDIF's write block as: **{RxA0[7], Bit-0, Bit-7}:** 0xx, 10x, or 110: DCLK for write (to DRAM) request in VDIF toggled freely. 111: DCLK for write request in VDIF will stop toggling when there is no write request in service or coming in within the VDIF.
6	RW	0	**Dynamic Stop for DCLK of Read Reqeust Control at VDIF** VDIF is the interface module in between Video Decoder (VD) and DRAM controller. It used the DRAM's DCLK as the clock. This bit is the level 2 enabling bit to control the dynamic stop feature for the DCLK used for VDIF's read control block in a VDIF read request cycle. The level 1 enabling bits are RxA0[7] and bit-0. This bit works with level 1 bits to control the DCLK in VDIF's read block as: **{RxA0[7], Bit-0, Bit-7}:** 0xx, 10x, or 110: DCLK for write (to DRAM) request in VDIF toggled freely. 111: DCLK for read request in VDIF will stop toggling when there is no read request in service or coming in within the VDIF.
5	RW	0	**Dynamic Stop for DCLK of Read Data Control at VDIF** VDIF is the interface module in between Video Decoder (VD) and DRAM controller. It used the DRAM's DCLK as the clock. This bit is the level 2 enabling bit to control the dynamic stop feature for the DCLK used for VDIF's read data returning block in a VDIF read request cycle. The level 1 enabling bits are RxA0[7] and bit-0. This bit works with level 1 bits to control the DCLK in VDIF's read data returning block as: **{RxA0[7], Bit-0, Bit-7}:** 0xx, 10x, or 110: DCLK for write (to DRAM) request in VDIF toggled freely. 111: DCLK for read's data returning in VDIF will stop toggling when there is no outstanding read request cycle or no data returned from DRAM needed to be processed to return to VD within the VDIF.
4:1	RW	0	**Reserved**
0	RW	0	**Dynamic Stop for DCLK at VDIF module** VDIF is the interface module in between Video Decoder (VD) and DRAM controller. It used the DRAM's DCLK as the clock. This bit along with the RxA0[7] are the level 1 enabling bits to control the dynamic stop feature for the DCLK used in VDIF. **{RxA0[7], Bit-0}:** 0x or 10: DCLK within VDIF toggled freely. 11: DCLK within VDIF will top toggling when there is no outstanding VD related cycles. Please refer to bits [7:5] for more information.

Offset Address: 8Dh (D0F4)

North Bridge Power Management Related Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Self Refresh Mode in C3 State** This bit is to enable the request to set the DRAM in self refresh mode. When this bit is set to 1, power management unit in NB block will issue request to DRAM controller to let it issue self refresh command to DRAM when this chip goes to C3 state. Please refer to register descriptions at D0F3 Rx98[6,4,2,0] for more details. 0: Disabled, DRAM won't be able to go to self refresh mode due to this chip's CPU power state changed to C3. 1: Enabled, DRAM connected to this chip is allowed to go to self refresh mode when this chip's CPU power state goes to C3.
4	RW	0	**Self Refresh Mode in C4 State** This bit is to enable the request to set the DRAM in self refresh mode. When this bit is set to 1, power management unit in NB block will issue request to DRAM controller to let it issue self refresh command to DRAM when this chip goes to C4 state. Please refer to register descriptions at D0F3 Rx98[6,4,2,0] for more details. 0: Disabled, DRAM won't be able to go to self refresh mode due to this chip's CPU power state changed to C4. 1: Enabled, DRAM connected to this chip is allowed to go to self refresh mode when this chip's CPU power state goes to C4.
3:0	RO	0	**Reserved**

Offset Address: 8Eh (D0F4)

North Bridge Power Management Related Registers 2 **Default Value: 50h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	1b	**Reserved**
5	RW	0	**Reserved**
4	RW	1b	**PLL Enabling Option** There are PLLs in this chip. PLL generates clocks which drive the chip to work. However, PLL outputs unstable clocks right after it is powered. This bit is to disable the output of the clocks from the PLL for 20us more after the power is up (assertion of PWRGD), so that the clocks output from the PLL can be guaranteed stable. 0: Disabled, PLLs drive clock right after the power is applied to this chip (the assertion of PWRGD). 1: Enabled, PLLs drive the clock 20us (at least) after the assertion of PWRGD.
3	RO	0	**Reserved**
2:1	RW	0	**Reserved**
0	RO	0	**Reserved**

Offset Address: 8Fh (D0F4)

North Bridge Power Management Related Registers 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Acknowledge PCIe L1 Request with the Downstream Completion** L1 is the low power standby state of the Link power management state machine in each PCIe root ports (RP0 ~ RP3). When PCIe device connected to the root ports is programmed to D state (ACPI device state) other than D0 state, the device might issue "PM_Enter_L1" DLLP (Note 1) to request to go to L1 state. The PCIe link on the device can go to L1 state when it received the acknowledge (PM_Request_Ack) from the root ports. This bit is used to control the returning of PM_Request_Ack. 0: The root ports of this chip will return the PM_Request_Ack to the device as soon as it received the PM_Enter_L1 request. It ignored any possible unfinished downstream cycles. i.e. There could be possible downstream requests waiting for the return of CPL TLP (Note 2) for previous downstream cycles. 1: The root ports of this chip will return the PM_Request_Ack only when the CPL TLP (Note 2) of previous downstream cycles are all returned from the device connected to the root port. Notes: 1. DLLP: Data Link Layer Packet, packets transferred on PCIe bus. 2. CPL TLP: Completion Transaction Layer Packet, packets transferred on PCIe bus.
6:4	RW	0	**Reserved**
3	RW	0	**Signal to Enter and Exit C5** This bit determines the signal to enter and exit C5 as described in bits [1:0] of this register. 0: This chip uses SLP# to enter and exit C5 as described in bits [1:0]. 1: This chip uses STPCLK# to enter and exit C5 as described in bits [1:0].
2	RW	0	**C5 State Enabling in NB block** During C5 state, CPU's caches will be all cleared and all the upstream cycles should be directed to DRAM without snooping to the internal cache inside CPU. This bit enable the C5 state for NB block of this chip. 0: Disabled, the NB block of this chip will never go to C5 state. 1: Enabled, the NB block of this chip is able to go to C5 state.
1	RW	0	**Exiting C5 Condition for NB block** This bit determines the way to exit C5 for NB block. When bit-2 is set to 0, this bit becomes meaningless since NB block will never go to C5 state. 0: NB block exit C5 state when SLP# (or STPCLK# when bit[3] of this register is 1), which is connected to CPU is de-asserted. 1: NB block exit C5 state when another CPU downstream command which is not a STPGNT (stop grant special cycle) cycle is detected (Note). Note: SLP# de-assertion usually happened earlier than any CPU downstream commands. i.e. when this bit is set to 1, the NB block gets out of C5 later than the case this bit set to 0.
0	RW	0	**Entering C5 Condition for NB block** This bit determines the way to enter C5 for NB block. When bit-2 is set to 0, this bit becomes meaningless since NB block will never go to C5 state. 0: NB block enters C5 state when entering C5 downstream command from CPU is detected. 1: NB block enters C5 state when SLP# (or STPCLK# when bit[3] of this register is 1), which is connected to CPU is asserted (Note). Note: SLP# assertion is usually much late than C5 downstream command is detected. i.e. when this bit set to 1, the NB block gets into the C5 later than the case this bit set to 0.

Offset Address: 90h (D0F4)

Dynamic Clock Stop for CPU Bus Controller (V4IF) - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for HCLK for CPURST# Related Logic** HCLK is the main clock for the CPU bus controller (VDIF) of this chip. This register is the level 2 enabling bit to control the dynamic stop feature for the HCLK used for CPURST# related logic. Level 1 enabling bits are RxA0[7] and RxA2[7]. This bit works with level 1 bits to control the HCLK for CPURST# related logic as: **{RxA0[7], RxA2[7], Bit-7}:** 0xx, 10x, or 110: HCLK for CPURST# related logic toggled freely. 111: HCLK for CPURST# related logic will only toggle during the assertion of CPURST#.
6	RW	0	**Dynamic Stop for HCLK for AGTL+ & AGTL+ Compensation Pads** This bit works as those described at bit-7, only that it is for the logic of AGTL+ & AGTL+ compensation pads. AGTL+ is the electrical specification for the signals traveled on V4 CPU bus. **{RxA0[7], RxA2[7], Bit-6}:** 0xx, 10x, or 110: HCLK for AGTL+ & AGTL+ compensation pads toggled freely. 111: HCLK for AGTL+ & AGTL+ compensation pads will only toggle during the auto-compensation process (Note) or AGTL+ pads. The power of the AGTL+ compensation circuitry will also be shut off after the process. Note: This auto-compensation process is a calibration process for the driving of AGTL+ pads of this chip. This process begins after the power is firstly applied to this chip or resumed from C3/C4/C5 or S1 state. Please refer to D0F2's diagram named "Calibration Process for the AGTL+ Auto Compensation Circuitry" and the paragraph besides it for more information.
5	RW	0	**Dynamic Stop for HCLK for Snoop Cycles on the CPU bus.** This bit works as those described at bit-7, only that it is for the logic of the snoop cycles on the CPU bus. **{RxA0[7], RxA2[7], Bit-5}:** 0xx, 10x, or 110: HCLK for the snoop cycles toggled freely. 111: HCLK for the snoop cycles toggled only at the Snoop phase of the host bus.
4	RW	0	**Dynamic Stop for HCLK for ROMSIP cycle** This bit works as those described at bit-7, only that it is for the logic of the ROMSIP (Note) cycles at the initialization of this chip. **{RxA0[7], RxA2[7], Bit-4}:** 0xx, 10x, or 110: HCLK for the ROMSIP cycle toggled freely. 111: HCLK for the ROMSIP cycle toggled only when ROMSIP cycles are in process. Note: ROMSIP is short for "ROM Serial In Programming". It is a process of reading in some predefined value of the registers of this chip. These predefined values are stored at somewhere of the ROM connected to this chip.
3	RW	0	**Dynamic Stop for HCLK for Transmitting Data on HD# bus** This bit works as those described at bit-7, only that it is for the logic of transmitting data on the HD[63:0]#. **{RxA0[7], RxA2[7], Bit-3}:** 0xx, 10x, or 110: HCLK for transmitting data on HD# toggled freely. 111: HCLK for transmitting data on HD# toggled only when data is transmitting on the HD# bus.
2	RW	0	**Dynamic Stop for HCLK for Transmitting Requests on HA# & HREQ#** This bit works as those described at bit-7, only that it is for the logic of transmitting requests on the HA[16:3]# and HREQ[2:0]# bus. **{RxA0[7], RxA2[7], Bit-2}**:: 0xx, 10x, or 110: HCLK for transmitting requests on HA# & HREQ# toggled freely. 111: HCLK for transmitting requests on HA# & HREQ# toggled only when request is transmitting on the HA# & HREQ# bus.
1	RW	0	**Dynamic Stop for HCLK for Receiving Requests on HA# & HREQ#** This bit works as those described at bit-7, only that it is for the logic of receiving requests on the HA[16:3]# and HREQ[2:0]# bus. **{RxA0[7], RxA2[7], Bit-1}**:: 0xx, 10x, or 110: HCLK for receiving requests on HA# & HREQ# toggled freely. 111: HCLK for receiving requests on HA# & HREQ# toggled only when request is receiving on the HA# & HREQ# bus.
0	RW	0	**Dynamic Stop for HCLK for Driving of 1X Signals** This bit works as those described at bit-7, only that it is for the logic of driving 1X signals. These 1X signals are CPURST#, HDPWR#, HLOCK#, HRS[2:0]#, HDRDY#, HBNR#, HHTIM#, HHIT#, HADS#, HBPRI#, HDBSY#, HDEFER#, HTRDY#, HALF#, HBREQ0#. **{RxA0[7], RxA2[7], Bit-0}:** 0xx, 10- or 110: HCLK for driving of those 1X signals on the CPU bus toggled freely. 111: HCLK for driving of those 1X signals on the CPU bus toggled only when these 1X signals are designated to drive.

Offset Address: 91h (D0F4)

Dynamic Clock Stop for CPU Bus Controller (V4IF) - 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Input Buffer Disabling Options for HA#, HREQ#, and 1X Signals on CPU Bus** This bit works with Rx92[6] to dynamically turn off the internal input buffers for AGTL+ signals like HA[16:3]#, HREQ[2:0]#, HADSTB[1:0]P/N#, and other 1X Signals (all 1X signals described at Rx90[0] except HADS# and HBREQ0#). **{RxA0[7], Bit-7}:** 0x: Chip internal input buffers for those signals mentioned are always on. 10: Chip internal input buffers for those signals mentioned will be turn on when HBREQ0# is activated and will be kept on when there are requests in the IO Queues of the CPU bus controller (V4IF) waiting to be served. 11: Chip internal input buffers for those signals mentioned will be turn on when HADS# is activated and will be kept on when there are requests in the IO Queues of V4IF waiting to be served.
6	RW	0	**Dynamic Stop for HCLK for Downstream Non-DRAM Cycle** This bit works as those described at Rx90[7], only that it is for the logic controlling downstream cycles targeted to non-DRAM agents, i.e. PCIe devices, internal Graphic controller, or devices in SB blocks. **{RxA0[7], RxA2[7], Bit-6}:** 0xx, 10x or 110: HCLK for downstream non-DRAM cycle toggled freely. 111: HCLK for downstream non-DRAM cycle only toggled when there are downstream cycles targeted to non-DRAM agents.
5	RW	0	**Dynamic Stop for HCLK for Defer Queue Control** This bit works as those described at Rx90[7], only that it is for the defer queue logic within CPU bus controller (V4IF). **{RxA0[7], RxA2[7], Bit-5}:** 0xx, 10x, or 110: HCLK for defer queue logic toggled freely. 111: HCLK for defer queue logic only toggled when this chip is writing requests to defer queue.
4	RW	0	**Dynamic Stop for HCLK for CPU to DRAM write cycle** This bit works as those described at Rx90[7], only that it is for the logic dealing with CPU to DRAM write cycle. **{RxA0[7], RxA2[7], Bit-4}:** 0xx, 10x, or 110: HCLK for the logic of CPU to DRAM write cycle toggled freely. 111: HCLK for the logic of CPU to DRAM write cycle only toggled when this chip is dealing with CPU to DRAM write cycle.
3	RW	0	**Dynamic Stop for Clock used to Receive Requests on CPU Bus** The clock used to receive requests on the CPU bus and put to the IO Queue (IOQ) within the CPU bus controller (V4IF) is the internal version of HADSTB[1:0]P/N#. This bit is to enable the dynamic stop feature for this clock. It is also worked with the level 1 signals as those described in Rx90[7]: **{RxA0[7], RxA2[7], Bit-3}:** 0xx, 10x, or 110: The clock to write requests into IOQ within the CPU bus controller toggled freely. 111: The clock to write requests into IOQ within the CPU bus controller only toggled 1 cycle which is right after the assertion of HADS#.
2	RW	0	**Dynamic Stop for HCLK for Requests of Downstream Non-DRAM Cycle** This bit works as those described at Rx90[7], only that it is for the logic controlling downstream requests targeted to non-DRAM agents, i.e. PCIe devices, internal Graphic controller, or devices in SB blocks. **{RxA0[7], RxA2[7], Bit-2}:** 0xx, 10x, or 110: HCLK for requests of downstream non-DRAM cycle toggled freely. 111: HCLK for requests of downstream non-DRAM cycle only toggled at the time when requests are pushed into internal request FIFO.
1	RW	0	**Dynamic Stop for HCLK for Requests of Downstream Posted DRAM Write Cycle** This bit works as those described at Rx90[7], only that it is for the logic controlling downstream posted write requests targeted to DRAM. **{RxA0[7], RxA2[7], Bit-1}:** 0xx, 10x, or 110: HCLK for data writing for downstream posted write to DRAM toggled freely. 111: HCLK for data writing for downstream posted write to DRAM only toggled when requests are pushed into internal request FIFO.
0	RW	0	**Dynamic Stop for HCLK used to Assert CPURST#** This bit works as those described at Rx90[7], only that it is for the assertion of CPU's RESET – CPURST# being generated from D0F2 Rx59[3]. Besides RxA0[7] and RxA2[7], Rx92[0] also affects the dynamic stop feature of this HCLK. **{RxA0[7], RxA2[7], Rx92[0], Bit-0}:** 0xxx, 10xx, 110x, or 1110: HCLK for CPURST# generation toggled freely. 1111: HCLK for CPURST# generation toggled only during the assertion of D0F2 Rx59[3].

Offset Address: 92h (D0F4)

Input Buffers Disabling for CPU Bus Controller (V4IF) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Input Buffer Disabling for HD#** This bit is to turn off the input buffers for more power saving. When it is enabled, the chip internal input buffers for AGTL+ HD[63:0]# & HDSTB[3:0]P/N# will be dynamically turn off. 0: Chip internal input buffers for signals mentioned are always on. 1: Chip internal input buffers for signals mentioned will be turn off and only be turn on when this chip is receiving data from the HD[63:0]# on the CPU bus.
6	RW	0	**Input Buffer Disabling for HA#, HREQ#, and 1X Signals on AGTL+ Bus** This bit is to turn off the input buffers for more power saving. When it is enabled, the chip internal input buffers of hose AGTL+ signals like HA[16:3]#, HADSTB[1:0]P/N#, HREQ[2:0]#, and those 1X signals (except HADS# & HBREQ0#) can be dynamically turn off. 0: Chip internal input buffers for those signals mentioned are always on. 1: Chip internal input buffers for those signals mentioned can be dynamically turn off. Please refer to Rx91[7] for options.
5:4	RW	0	**Reserved**
3	RW	0	**Input Buffer Disabling for Some AGTL+ Signals During C2** This bit is to turn off the internal input buffers for AGTL+ signals – HA[16:3]#, HREQ[2:0]#, HLOCK#, HBNR#, and HBREQ0# to save power during C2 power management state. 0: Internal input buffers for signals mentioned are always on. 1: Internal input buffers for signals mentioned will be turn off during C2 state.
2	RW	0	**Input Buffer Disabling for All AGTL+ Signals During C3/C4/S1** This bit is to turn off the internal input buffers for all AGTL+ Signals to save power during C3/C4/S1 power management state. 0: All internal input buffers of AGTL+ signals are always on. 1: All internal input buffers of AGTL+ signals will be turn off during C3, C4, or S1 state.
1	RW	0	**Reserved**
0	RW	1b	**Dynamic Stop for HCLK used to Control Miscellaneous Logic** This bit works as those described at Rx90[7], only that it is for the assertion of CPU's RESET (Please refer to Rx91[0]) and some other miscellaneous logic in V4IF. {**RxA0[7], RxA2[7], Bit-0**}: 0xx, 10x, or 110: HCLK for CPURST# generation & some miscellaneous logic toggled freely. 111: HCLK for CPURST# generation will toggle depends on the status of Rx91[0] (Please refer to Rx91[0]). And HCLK for some miscellaneous logic in V4IF will stop toggling when those miscellaneous logic is not functioned.

Offset Address: 93h (D0F4)

Dynamic Clock Stop for CPU Bus Controller (V4IF) - 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Dynamic Stop for HCLK for Receiving Data on HD# Bus** This bit works as those described at Rx90[7], only that it is for the logic within AGTL+ circuit macro to receive data from the HD[63:0]# on the CPU bus. **{RxA0[7], RxA2[7], Bit-0}:** 0xx, 10x, or 110: HCLK for data receiving on the HD[63:0]# toggled freely. 111: HCLK for data receiving on the HD[63:0]# only toggled when receiving data from the CPU bus.

Offset Address: 94-95h (D0F4) – Reserved

Offset Address: 96h (D0F4)

Dynamic Clock Stop for Clocks in Message Controller within PCIe Controller - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for Clocks for Stop Grant Cycle Handling in MSGC** MSGC is the PCIe message handling module for PCIe Root Ports (RP0 ~ RP3). This bit controls the dynamic stop feature for the clocks used for handling the logic to put the PCIe devices into power management L1 mode upon seeing stop grant cycle from CPU. It works with RxA0[7] as: **{RxA0[7], Bit-7}:** 0x or 10: Clocks for stop grant cycle handling in MSGC toggled freely. 11: Clocks for stop grant cycle handling in MSGC only toggled during the period from the detection of stop grant cycle to the L1 acknowledgement are all returned from all the devices connected to RP0 ~ RP3.
6:4	RW	0	**Reserved**
3	RW	0	**Dynamic Stop for ECLK_PE3 in MSGC for PCIe RP3** MSGC is the PCIe message handling module for PCIe Root Ports (RP0 ~ RP3). ECLK_PE3 in MSGC is the clock used to interface with the RP3 and is running at 250Mhz. This bit worked with RxA0[7] to control the dynamic stop features for the ECLK_PE3. **{RxA0[7], Bit-3}:** 0x or 10: ECLK_PE3 in MSGC toggled freely. 11: ECLK_PE3 in MSGC toggled only when there is PCIe message to be sent to device connected to RP3.
2	RW	0	**Dynamic Stop for ECLK_PE2 in MSGC for PCIe RP2** As those described in bit-3, only that this bit is for ECLK_PE2 which is used for the MSGC served for RP2. **{RxA0[7], Bit-2}:** 0x or 10: ECLK_PE2 in MSGC toggled freely. 11: ECLK_PE2 in MSGC toggled only when there is PCIe message to be sent to device connected to RP2.
1	RW	0	**Dynamic Stop for ECLK_PE1 in MSGC for PCIe RP1** As those described in bit-3, only that this bit is for ECLK_PE1 which is used for the MSGC served for RP1. **{RxA0[7], Bit-1}:** 0x or 10: ECLK_PE1 in MSGC toggled freely. 11: ECLK_PE1 in MSGC toggled only when there is PCIe message to be sent to device connected to RP1.
0	RW	0	**Dynamic Stop for ECLK_PE0 in MSGC for PCIe RP0** As those described in bit-3, only that this bit is for ECLK_PE0 which is used for the MSGC served for RP0. **{RxA0[7], Bit-0}:** 0x or 10: ECLK_PE0 in MSGC toggled freely. 11: ECLK_PE0 in MSGC toggled only when there is PCIe message to be sent to device connected to RP0.

Offset Address: 97h (D0F4)

Dynamic Clock Stop for Clocks in Message Controller within PCIe Controller - 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Dynamic Stop for GCLK_PE3 in MSGC for PCIe RP3** MSGC is the PCIe message handling module for PCIe Root Ports (RP0 ~ RP3). GCLK_PE3 is the main clock for MSGC to handle the messages for RP3 and is running at 66Mhz. This bit worked with RxA0[7] to control the dynamic stop features for the GCLK_PE3. **{RxA0[7], Bit-3}:** 0x or 10: GCLK_PE3 in MSGC toggled freely. 11: GCLK_PE3 in MSGC toggled only during the preparation of PCIe messages to be sent to RP3.
2	RW	0	**Dynamic Stop for GCLK_PE2 in MSGC for PCIe RP2** As those described in bit-3, only that this bit is for GCLK_PE2 which is used for the MSGC served for RP2. **{RxA0[7], Bit-2}:** 0x or 10: GCLK_PE2 in MSGC toggled freely. 11: GCLK_PE2 in MSGC toggled only when there is PCIe message to be sent to device connected to RP2.
1	RW	0	**Dynamic Stop for GCLK_PE1 in MSGC for PCIe RP1** As those described in bit-3, only that this bit is for GCLK_PE1 which is used for the MSGC served for RP1. **{RxA0[7], Bit-1}:** 0x or 10: GCLK_PE1 in MSGC toggled freely. 11: GCLK_PE1 in MSGC toggled only when there is PCIe message to be sent to device connected to RP1.
0	RW	0	**Dynamic Stop for GCLK_PE0 in MSGC for PCIe RP0** As those described in bit-3, only that this bit is for GCLK_PE0 which is used for the MSGC served for RP0. **{RxA0[7], Bit-0}:** 0x or 10: GCLK_PE0 in MSGC toggled freely. 11: GCLK_PE0 in MSGC toggled only when there is PCIe message to be sent to device connected to RP0.

Offset Address: 98-9Fh (D0F4) – Reserved

Offset Address: A0h (D0F4)

Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Clock Stop Feature for the Clocks in NB Block** Dynamic Clock Stop is a feature to stop the clocks of NB block of this chip dynamically. i.e. when this feature is enabled, the internal clocks of NB block will be forced to electrical low level when they are not needed. Those clocks will be recovered to toggle when the corresponding logic is required to for normal function. Please refer to Figure 36, this bit is the level 1 control bit to enable the dynamic stop feature for the clocks in NB block. 0: Disabled, all the clocks in NB will be toggle freely. 1: Enabled, this bit served as the level 1 signal to enable the clocks of NB dynamically. Note there are other level 1 (RxA2 and RxA8) and level 2 enable bits in Rx80 ~ RxFF to control all the clocks in each clock network.
6:0	RW	0	**Reserved**

Offset Address: A1h (D0F4)

DRAM Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Dynamic Assertion of MCKE** This bit is to enable the dynamic assertion for MCKE[3:0] of this chip. MCKE[3:0] are connected to the DRAM DIMM on the motherboard, when de-asserted, the internal clocks of the DIMM modules can be stopped which provides power saving on the DIMM modules. 0: MCKE[3:0] will always be asserted. 1: MCKE[3:0] will be only asserted when DRAM cycles are processing on the DRAM bus. Note that MCKE will be used to issue self refresh commands to the DIMM, it is a must to set this bit to 0 before this chip enters the STR (Suspend To RAM) mode.
5	RW	0	**Dynamic Output Enabling for DRAM I/O** This bit is to enable the dynamic output enabling on some DRAM balls: MA[15:0], MBA[2:0], MSRAS#, MSCAS#, and MSWE#. 0: Those DRAM balls mentioned will always be in output mode. 1: Those DRAM balls mentioned will be floated (Will not be driven) when there is no DRAM activity.
4:0	RW	0	**Reserved**

Offset Address: A2h (D0F4)

Dynamic Clock Stop Control - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Clock Stop Control for CPU Bus Controller** This bit is the enable bit for the dynamic stop feature for the clocks used in CPU bus controller (V4IF). This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature for the clocks used in V4IF. **{RxA0[7], Bit-7}:** 0x or 10: Clocks used in the V4IF toggled freely. 11: Clocks used in the V4IF will stop toggling (stay at low) when there is no activity involved in the logic within V4IF. Register bits at Rx90 ~ Rx93 are meaningful only when {RxA0[7], Bit-7} is 11b.
6	RW	0	**Dynamic Clock Stop Control for DRAM Controller** This bit is the enable bit for the dynamic stop feature for the clocks used in DRAM controller (DRAMC). This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature for the clocks used in DRAMC. **{RxA0[7], Bit-6}:** 0x or 10: Clocks used in DRAMC toggled freely. 11: Clocks used in DRAMC will stop toggling (stay at low) when there is no activity involved in the logic within DRAMC.
5	RW	0	**Reserved**
4	RW	0	**Dynamic Clock Stop Control for Data Paths** This bit is the enable bit for the dynamic stop feature for the clocks used in the chip internal data paths in between CPU bus controller (V4IF), DRAM controller (DRAMC), and central traffic controller (PXPTRF) which communicates to other peripherals in the chip. This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature for the clocks used in the internal data paths. **{RxA0[7], Bit-4}:** 0x or 10: Clocks used in data paths toggled freely. 11: Clocks used in data paths will stop toggling (stay at low) when there is no activity involved in the logic within data paths. Registers at Rx8B are meaningful only when {RxA0[7], Bit-4} is 11b.
3	RW	0	**Dynamic Clock Stop Control for APICX** APICX is the APIC Controller in NB block. This bit is the enable bit for the dynamic stop feature for the clocks used in the APICX. This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature for the clocks used in the APICX. **{RxA0[7], Bit-3}:** 0x or 10: Clocks used in APICX toggled freely. 11: Clocks used in APICX will stop toggling (stay at low) when there is no activity involved in the logic within APICX. Registers at Rx88 are meaningful only when {RxA0[7], Bit-3} is 11b.
2	RW	0	**Dynamic Clock Stop Control for GMINT** GMINT is the interface in between internal integrated graphic controller and DRAM controller. This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature for the clocks used in the GMINT. **{RxA0[7], Bit-2}:** 0x or 10: Clocks used in GMINT toggled freely. 11: Clocks used in GMINT will stop toggling (stay at low) when there is no activity involved in the logic within GMINT. Registers at Rx89 ~ Rx8A are meaningful only when {RxA0[7], Bit-2} is 11b.
1	RW	0	**Dynamic Clock Stop Control for Configuration Registers** This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the enabling bit for the dynamic stop feature for the clocks used in the register files (configuration space registers). **{RxA0[7], Bit-1}:** 0x or 10: Clocks used in register files toggled freely. 11: Clocks used in register files will only toggled when there is configuration cycle on going in the chip. Register at Rx85[2] is meaningful only when {RxA0[7], Bit-1} is 11b.
0	RW	0	**Reserved**

Offset Address: A3h (D0F4)

Power Reduction on DRAM I/O - 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Toggle Reduction for DRAM I/O** This bit is to hold the status (not toggle) of some DRAM signals during the idle period on the DRAM bus. These signals are MA[15:0], MBA[2:0], MSRAS#, MSCAS#, and MSWE#. 0: Those DRAM balls mentioned toggled to reflect the internal logic. 1: Those DRAM balls mentioned will maintain the status as it is in the last phase of previous DRAM cycle. They will not toggle when the DRAM bus is idle.
6:0	RW	0	**Reserved**

Offset Address: A4-A6h (D0F4) – Reserved

Offset Address: A7h (D0F4)

Dynamic Clock Stop for PCIe Physical Layer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Dynamic Stop for EPCLK_PE3 at PCIe Physical Layer** EPCLK_PE3 is the main clock used at the logic sub-layer of the PCIe physical layer (PHYLS) for root port 3 (RP3). This bit is the dynamic stop feature for the EPCLK_PE3. It works with RxA0[7] to control the EPCLK_PE3 as: **{RxA0[7], Bit-3}:** 0x or 10: EPCLK_PE3 always toggled freely. 11: EPCLK_PE3 only toggled when RP3's PHYLS is either receiving or transmitting PCIe packets. Register bits at RxAC are meaningful only when {RxA0[7], Bit-3} is 11b.
2	RW	0	**Dynamic Stop for EPCLK_PE2 at PCIe Physical Layer** As described in bit-3, only that this bit is for EPCLK_PE2 which is the clock used for RP2. **{RxA0[7], Bit-2}:** 0x or 10: EPCLK_PE2 always toggled freely. 11: EPCLK_PE2 only toggled when RP2's PHYLS is either receiving or transmitting PCIe packets. Register bits at RxAC are meaningful only when {RxA0[7], Bit-2} is 11b.
1	RW	0	**Dynamic Stop for EPCLK_PE1 at PCIe Physical Layer** As described in bit-3, only that this bit is for EPCLK_PE1 which is the clock used for RP1. **{RxA0[7], Bit-1}:** 0x or 10: EPCLK_PE1 always toggled freely. 11: EPCLK_PE1 only toggled when RP1's PHYLS is either receiving or transmitting PCIe packets. Register bits at RxAC are meaningful only when {RxA0[7], Bit-1} is 11b.
0	RW	0	**Dynamic Stop for EPCLK_PE0 at PCIe Physical Layer** As described in bit-3, only that this bit is for EPCLK_PE0 which is the clock used for RP0. **{RxA0[7], Bit-0}:** 0x or 10: EPCLK_PE0 always toggled freely. 11: EPCLK_PE0 only toggled when RP0's PHYLS is either receiving or transmitting PCIe packets. Register bits at RxAC are meaningful only when {RxA0[7], Bit-0} is 11b.

Offset Address: A8h (D0F4)

Dynamic Clock Stop Control - 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Dynamic Clock Stop Control for Central Traffic Controller** This bit is the enable bit for the dynamic stop feature for the clocks used in central traffic controller (PXPTRF). This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature for the clocks used in PXPTRF. **{RxA0[7], Bit-6}:** 0x or 10: Clocks used in PXPTRF toggled freely. 11: Clocks used in PXPTRF will stop toggling (stay at low) when there is no activity involved in the logic within PXPTRF. Register bits at Rx84 ~ Rx87 are meaningful only when {RxA0[7], Bit-6} is 11b.
5:4	RW	0	**Reserved**
3	RW	0	**Dynamic Clock Stop Control for ETCLK_PE3 at PCIe Root Port 3** ETCLK_PE3 is the main clock used at Transaction Layer & Data Link Layer of PCIe root port 3 (RP3). This bit is the enable bit for the dynamic stop feature for ETCLK_PE3. This bit works with the global control of dynamic clock stop feature, RxA0[7], to be the level 1 enabling bit for the dynamic stop feature of ETCLK_PE3. **{RxA0[7], Bit-3}:** 0x or 10: ETCLK_PE3 always toggled freely. 11: ETCLK_PE3 only toggled when RP3's Transaction Layer or Data Link Layer is processing the transmitting or receiving PCIe packets. Register bits at RxBD are meaningful only when {RxA0[7], Bit-3} is 11b.
2	RW	0	**Dynamic Clock Stop Control for ETCLK_PE2 at PCIe Root Port 2** As described in bit-3, only that this bit is for ETCLK_PE2 which is the clock used for RP2. **{RxA0[7], Bit-2}:** 0x or 10: ETCLK_PE2 always toggled freely. 11: ETCLK_PE2 only toggled when RP2's Transaction Layer or Data Link Layer is processing the transmitting or receiving PCIe packets. Register bits at RxBC are meaningful only when {RxA0[7], Bit-2} is 11b.
1	RW	0	**Dynamic Clock Stop Control for ETCLK_PE1 at PCIe Root Port 1** As described in bit-3, only that this bit is for ETCLK_PE1 which is the clock used for RP1. **{RxA0[7], Bit-1}:** 0x or 10: ETCLK_PE1 always toggled freely. 11: ETCLK_PE1 only toggled when RP1's Transaction Layer or Data Link Layer is processing the transmitting or receiving PCIe packets. Register bits at RxBB are meaningful only when {RxA0[7], Bit-1} is 11b.
0	RW	0	**Dynamic Clock Stop Control for ETCLK_PE0 at PCIe Root Port 0** As described in bit-3, only that this bit is for ETCLK_PE0 which is the clock used for RP0. **{RxA0[7], Bit-0}:** 0x or 10: ETCLK_PE0 always toggled freely. 11: ETCLK_PE0 only toggled when RP2's Transaction Layer or Data Link Layer is processing the transmitting or receiving PCIe packets. Register bits at RxBA are meaningful only when {RxA0[7], Bit-0} is 11b.

Offset Address: A9h (D0F4) – Reserved

Offset Address: AAh (D0F4)

PCIe Power Management Registers - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Clock Stop at L1 state for PCIe Root Port 3** This bit is to stop the toggling of PCIe main clock which provided by the PLL in PCIe physical circuit macro when PCIe root port3 (RP3) is in L1 (low power stand by) link power management state. 0: The clock provided by the PCIe PLL toggled freely. 1: When RP0, RP1, RP2, and RP3 are all in L1 state and bits [2:0] = 111, the clock provided by the PCIe PLL will stop toggling. Please refer to Table 24 for complete information on the clock behavior.
2	RW	0	**Clock Stop at L1 state for PCIe Root Port 2** This bit is to stop the toggling of PCIe main clock which provided by the PLL in PCIe physical circuit macro when PCIe root port2 (RP2) is in L1 (low power stand by) link power management state. 0: The clock provided by the PCIe PLL toggled freely. 1: When RP0, RP1, RP2, and RP3 are all in L1 state and bits [3, 1:0] = 111, the clock provided by the PCIe PLL will stop toggling. Please refer to Table 24 for complete information on the clock behavior.
1	RW	0	**Clock Stop at L1 state for PCIe Root Port 1** This bit is to stop the toggling of PCIe main clock which provided by the PLL in PCIe physical circuit macro when PCIe root port1 (RP1) is in L1 (low power stand by) link power management state. 0: The clock provided by the PCIe PLL toggled freely. 1: When RP0, RP1, RP2, and RP3 are all in L1 state and bits [3:2, 0] = 111, the clock provided by the PCIe PLL will stop toggling. Please refer to Table 24 for complete information on the clock behavior.
0	RW	0	**Clock Stop at L1 state for PCIe Root Port 0** This bit is to stop the toggling of PCIe main clock which provided by the PLL in PCIe physical circuit macro when PCIe root port0 (RP0) is in L1 (low power stand by) link power management state. 0: The clock provided by the PCIe PLL toggled freely. 1: When RP0, RP1, RP2, and RP3 are all in L1 state and bits [3:1] = 111, the clock provided by the PCIe PLL will stop toggling. Please refer to table Table 24 for complete information on the clock behavior.

Table 24. RxAA: The Clock Behavior of the PCIe's PLL on Different Registers Setting Specified at RxAA[3:0]

RxAA[3]	RxAA[2]	RxAA[1]	RxAA[0]	Link Power state				Clocks output from PLL within PCIe physical circuit macro
				RP3	RP2	RP1	RP0	
0	-	-	-	-	-	-	-	toggle normally
	0	-	-	-	-	-	-	
		0	-	-	-	-	-	
		-	0	-	-	-	-	
1	1	1	1	~L123 *	-	-	-	
1	1	1	1		~L123 *	-	-	
1	1	1	1			~L123 *	-	
1	1	1	1			-	~L123 *	
1	1	1	1	L123 *	L123 *	L123 *	L123 *	Stop toggling

*L123: L123 state means that the Link state machine is at L1, L2, or L3; ~L123 means that the Link state machine is at either L0 or L0S state.

Offset Address: ABh (D0F4)

PCIe Power Management Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Ignore Requests to Update FC When PCIe Link is not at L0/L0S** FC (Flow Control) in the PCIe bus is updated periodically. Root ports sends FC DLLP (Data Link Layer Packets) to devices every a few micro seconds. This bit is to ignore the internal requests to send FC to the PCIe devices connecting to RP0~RP3 of this chip when the link is at link states other than L0 or L0S. The purpose of this bit is to allow the PCIe's Data Link Layer (DLL) internal clock to stop when the dynamic clock stop features (please refer to register bit [1:0] of RxC2 ~ RxC5) are on. It applied to RP0, RP1, RP2, and RP3. 0: With dynamic clock stop feature being on, when the link is at link states other than L0/L0S, the internal clock of DLL won't stop if there is FC updates request pending. 1: With Dynamic clock stop feature being on, when the link is at link states other than L0/L0S, the internal clock of DLL will stop even if there is FC updates request pending.
3:0	RW	0	**Reserved**

Offset Address: ACh (D0F4)

Dynamic Clock Stop for Clocks in Physical Logic Sub-Layer within PCIe Controller **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Dynamic Stop for Clocks for Link Status Changes** This bit is the dynamic stop feature for the clocks dealing with Link Status changes within PHYLS (Physical Logic Sub-layer) of PCIe. It is the level 2 control signals for the dynamic stop feature. RxA0[7] & registers at RxA7[3:0] are the level 1 signals. It apples to all PCIe root ports (RP3 ~ RP0). **{RxA0[7], RxA7[3], Bit-6}:** 0xx, 10x, or 110: The clocks for link status changes within PHYLS of RP3 toggled freely. 111: The clocks for link status changes within PHYLS of RP3 toggled only when the RP3's Link change status (i.e. changes from L0 → L1, L0S → L0..). **{RxA0[7], RxA7[2], Bit-6}:** 0x, 10x, or 110: The clocks for link status changes within PHYLS of RP2 toggled freely. 111: The clocks for link status changes within PHYLS of RP2 toggled only when the RP2's Link change status (i.e. changes from L0 → L1, L0S → L0..). **{RxA0[7], RxA7[1], Bit-6}:** 0xx, 10x, or 110: The clocks for link status changes within PHYLS of RP1 toggled freely. 111: The clocks for link status changes within PHYLS of RP1 toggled only when the RP1's Link change status (i.e. changes from L0 → L1, L0S → L0..). **{RxA0[7], RxA7[0], Bit-6}:** 0xx, 10x, or 110: The clocks for link status changes within PHYLS of RP0 toggled freely. 111: The clocks for link status changes within PHYLS of RP0 toggled only when the RP0's Link change status (i.e. changes from L0 → L1, L0S → L0..).
5	RW	0	**Dynamic Stop for Clocks for Configuration Registers Updates** For reducing the long distance traveled from the register files, there are a lot of configuration registers fed built in the PCIe's Physical Logic Sub-layer. In order to save power, this bit is to enable the dynamic stop features for the clocks of these configuration registers. This bit acts as the level 2 enable bit for the dynamic stop feature. It works with level 1 enable bits at RxA0[7] and RxA7[3:0]. It applys to all PCIe root ports (RP0 ~ RP3). **{RxA0[7], RxA7[3], Bit-5}:** 0xx, 10x, or 110: The clocks for the configuration registers within PHYLS of RP3 toggled freely. 111: The clocks for the configuration registers within PHYLS of RP3 toggled only when the register changes its value. **{RxA0[7], RxA7[2], Bit-5}:** 0xx, 10x, or 110: The clocks for the configuration registers within PHYLS of RP2 toggled freely. 111: The clocks for the configuration registers within PHYLS of RP2 toggled only when the register changes its value. **{RxA0[7], RxA7[1], Bit-5}:** 0xx, 10x, or 110: The clocks for the configuration registers within PHYLS of RP1 toggled freely. 111: The clocks for the configuration registers within PHYLS of RP1 toggled only when the register changes its value. **{RxA0[7], RxA7[0], Bit-5}:** 0xx, 10x, or 110: The clocks for the configuration registers within PHYLS of RP0 toggled freely. 111: The clocks for the configuration registers within PHYLS of RP0 toggled only when the register changes its value.
4	RW	0	**Reserved**
3	RW	0	**Dynamic Stop for Clocks for Internal Counters** For counting the timing of the PCIe protocol, PCIe PHYLS (Physical Logic Sub-Layer) does have a lot of counters. These counters only works for a period of time on the PCIe bus (e.g. Training Sequence: TS1, TS2). This bit is the dynamic stop feature for the clocks used for these counters. RxA0[7] & registers at RxA7[3:0] are the level 1 signals. It apples to all PCIe root ports (RP3 ~ RP0). **{RxA0[7], RxA7[3], Bit-3}:** 0xx, 10x, or 110: The clocks for internal counters within PHYLS of RP3 toggled freely. 111: The clocks for internal counters within PHYLS of RP3 toggled only when the counters are needed to function. **{RxA0[7], RxA7[2], Bit-3}:** 0xx, 10x, or 110: The clocks for internal counters within PHYLS of RP2 toggled freely. 111: The clocks for internal counters within PHYLS of RP2 toggled only when the counters are needed to function. **{RxA0[7], RxA7[1], Bit-3}:** 0xx, 10x, or 110: The clocks for internal counters within PHYLS of RP1 toggled freely. 111: The clocks for internal counters within PHYLS of RP1 toggled only when the counters are needed to function. **{RxA0[7], RxA7[0], Bit-3}:** 0xx, 10x, or 110: The clocks for internal counters within PHYLS of RP0 toggled freely.

			111: The clocks for internal counters within PHYLS of RP0 toggled only when the counters are needed to function.
2:0	RW	0	**Reserved**

Offset Address: AD-AEh (D0F4) – Reserved

Offset Address: AFh (D0F4)

PCIe Power Management Registers 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Reset PCIe PLL** This bit is to reset the PLL within the PCIe physical circuit macro. When programmed to 1, the clocks used in root ports (RP0 ~ RP3) will be stopped right away. 0: Disabled, the clocks used for PCIe root ports toggled freely. 1: Enabled, the PLL of the PCIe macro will be reset, the clocks used for all root ports will be remained at low. It is recommended that this bit be programmed to 1 only when there is no PCIe devices connected to any root ports of this chip.
1:0	RW	0	**Reserved**

Offset Address: B0-B9h (D0F4) – Reserved

Offset Address: BAh (D0F4)

Dynamic Clock Stop for Clocks in Transaction Layer of PCIe Root Port 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for ETCLK_PE0 for Upstream Paths of RP0** ETCLK_PE0 is the main clock used at Transaction Layer of PCIe root port 0 (RP0). This bit is the level 2 enable bit for the dynamic stop feature for ETCLK_PE0 used in upstream requests related logics. It works with level 1 bits, RxA0[7] and RxA8[0], to control the dynamic stop feature of this ETCLK_PE0 for the RP0's upstream paths. **{RxA0[7], RxA8[0], Bit-7}:** 0xx, 10x, or 110: The ETCLK_PE0 for RP0's upstream paths toggled freely. 111: The ETCLK_PE0 for RP0's upstream paths toggled only when there are upstream requests on going in RP0.
6	RW	0	**Dynamic Stop for ETCLK_PE0 for Downstream Paths of RP0** As described in bit-7, only that this bit is for the ETCLK_PE0 used in RP0's downstream paths. **{RxA0[7], RxA8[0], Bit-6}:** 0xx, 10x, or 110: The ETCLK_PE0 for RP0's downstream paths toggled freely. 111: The ETCLK_PE0 for RP0's downstream paths toggled only when there are downstream requests on going in RP0.
5	RW	0	**Dynamic Stop for ETCLK_PE0 for Downstream Retry Path of RP0** As described in bit-7, only that this bit is for the ETCLK_PE0 used in RP0's downstream retry paths. Note that when downstream cycle could not get acknowledge from the device through PCIe bus, the root port will sent the transaction again through downstream retry controls. **{RxA0[7], RxA8[0], Bit-5}:** 0xx, 10x, or 110: The ETCLK_PE0 for RP0's downstream retry paths toggled freely. 111: The ETCLK_PE0 for RP0's downstream paths toggled only when there are downstream retry transactions needed to be processed in RP0.
4	RW	0	**Dynamic Stop for ETCLK_PE0 for Downstream Retry FIFO of RP0** As described in bit-7, only that this bit is for the ETCLK_PE0 used for clocking in the requests and data into the FIFO which is for downstream retry controls for RP0. **{RxA0[7], RxA8[0], Bit-4}:** 0--, 10-, or 110: The ETCLK_PE0 for RP0's downstream retry FIFO toggled freely. 111: The ETCLK_PE0 for RP0's downstream retry FIFO toggled only when the RP0 issued downstream cycle (directly from CPU's downstream cycle, not internally retried) to the device connected to the RP0.
3	RW	0	**Dynamic Stop for ETCLK_PE0 for Upstream Data Handling of RP0** As described in bit-7, only that this bit is for the ETCLK_PE0 used in RP0's upstream data handling controls. **{RxA0[7], RxA8[0], Bit-3}:** 0xx, 10x, or 110: The ETCLK_PE0 for RP0's upstream data handling paths toggled freely. 111: The ETCLK_PE0 for RP0's upstream data handling paths toggled only when there are upstream data phases on going in RP0.
2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for ETCLK_PE0 for Downstream Data FIFO of RP0** As described in bit-7, only that this bit is for the ETCLK_PE0 used for clocking in the data into the FIFO which is for downstream read/write for RP0. **{RxA0[7], RxA8[0], Bit-1}:** 0xx, 10x, or 110: The ETCLK_PE0 for RP0's downstream data FIFO toggled freely. 111: The ETCLK_PE0 for RP0's downstream data FIFO toggled only when the write data of the downstream write cycle were written into the FIFO or the read data returned from the device connected to the RP0 of the downstream read cycle were written into the FIFO.
0	RW	0	**Dynamic Stop for ETCLK_PE0 for Upstream Data FIFO of RP0** As described in bit-7, only that this bit is for the ETCLK_PE0 used for clocking in the data into the FIFO which is for upstream read/write for RP0. **{RxA0[7], RxA8[0], Bit-0}:** 0xx, 10x, or 110: The ETCLK_PE0 for RP0's upstream data FIFO toggled freely. 111: The ETCLK_PE0 for RP0's upstream data FIFO toggled only when the write data of the upstream write cycle were written into the FIFO or the read data returned from the DRAM (or other devices connected in the system for a peer-to-peer transfer, refer to Note) of the upstream read cycle were written into the FIFO. Note: Peer-to-peer cycle are those upstream requests (read or write from SB blocks or PCIe root ports) not targeted to CPU (which eventually to DRAM).

Offset Address: BBh (D0F4)

Dynamic Clock Stop for Clocks in Transaction Layer of PCIe Root Port 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for ETCLK_PE1 for Upstream Paths of RP1** As those described at RxBA[7], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-7}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's upstream paths toggled freely. 111: The ETCLK_PE1 for RP1's upstream paths toggled only when there are upstream requests on going in RP1.
6	RW	0	**Dynamic Stop for ETCLK_PE1 for Downstream Paths of RP1** As those described at RxBA[6], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-6}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's downstream paths toggled freely. 111: The ETCLK_PE1 for RP1's downstream paths toggled only when there are downstream requests on going in RP1.
5	RW	0	**Dynamic Stop for ETCLK_PE1 for Downstream Retry Path of RP1** As those described at RxBA[5], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-5}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's downstream retry paths toggled freely. 111: The ETCLK_PE1 for RP1's downstream paths toggled only when there are downstream retry transactions needed to be processed in RP1.
4	RW	0	**Dynamic Stop for ETCLK_PE1 for Downstream Retry FIFO of RP1** As those described at RxBA[4], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-4}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's downstream retry FIFO toggled freely. 111: The ETCLK_PE1 for RP1's downstream retry FIFO toggled only when the RP1 issued downstream cycle (directly from CPU's downstream cycle, not internally retried) to the device connected to the RP1.
3	RW	0	**Dynamic Stop for ETCLK_PE1 for Upstream Data Handling of RP1** As those described at RxBA[3], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-3}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's upstream data handling paths toggled freely. 111: The ETCLK_PE1 for RP1's upstream data handling paths toggled only when there are upstream data phases on going in RP1.
2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for ETCLK_PE1 for Downstream Data FIFO of RP1** As those described at RxBA[1], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-1}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's downstream data FIFO toggled freely. 111: The ETCLK_PE1 for RP1's downstream data FIFO toggled only when the write data of the downstream write cycle were written into the FIFO or the read data returned from the device connected to the RP1 of the downstream read cycle were written into the FIFO.
0	RW	0	**Dynamic Stop for ETCLK_PE1 for Upstream Data FIFO of RP1** As those described at RxBA[0], only that this bit is for ETCLK_PE1 which is in RP1. And the level 1 bits changed to RxA0[7] and RxA8[1]. **{RxA0[7], RxA8[1], Bit-0}:** 0xx, 10x, or 110: The ETCLK_PE1 for RP1's upstream data FIFO toggled freely. 111: The ETCLK_PE1 for RP1's upstream data FIFO toggled only when the write data of the upstream write cycle were written into the FIFO or the read data returned from the DRAM (or other devices connected in the system for a peer-to-peer transfer, refer to Note) of the upstream read cycle were written into the FIFO. Note: Peer-to-peer cycle are those upstream requests (read or write from SB blocks or PCIe root ports) not targeted to CPU (which eventually to DRAM).

Offset Address: BCh (D0F4)

Dynamic Clock Stop for Clocks in Transaction Layer of PCIe Root Port 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for ETCLK_PE2 for Upstream Paths of RP2** As those described at RxBA[7], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-7}:** 0xx, 10x, or 110: The ETCLK_PE2 for RP2's upstream paths toggled freely. 111: The ETCLK_PE2 for RP2's upstream paths toggled only when there are upstream requests on going in RP2.
6	RW	0	**Dynamic Stop for ETCLK_PE2 for Downstream Paths of RP2** As those described at RxBA[6], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-6}:** 0xx, 10x, or 110: The ETCLK_PE2 for RP2's downstream paths toggled freely. 111: The ETCLK_PE2 for RP2's downstream paths toggled only when there are downstream requests on going in RP2.
5	RW	0	**Dynamic Stop for ETCLK_PE2 for Downstream Retry Path of RP2** As those described at RxBA[5], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-5}:** 0xx, 10x, or 110: The ETCLK_PE2 for RP2's downstream retry paths toggled freely. 111: The ETCLK_PE2 for RP2's downstream paths toggled only when there are downstream retry transactions needed to be processed in RP2.
4	RW	0	**Dynamic Stop for ETCLK_PE2 for Downstream Retry FIFO of RP2** As those described at RxBA[4], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-4}:** 0xx, 10x, or 110: The ETCLK_PE2 for RP2's downstream retry FIFO toggled freely. 111: The ETCLK_PE2 for RP2's downstream retry FIFO toggled only when the RP2 issued downstream cycle (directly from CPU's downstream cycle, not internally retried) to the device connected to the RP2.
3	RW	0	**Dynamic Stop for ETCLK_PE2 for Upstream Data Handling of RP2** As those described at RxBA[3], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-3}:** 0xx, 10x, or 110: The ETCLK_PE2 for RP2's upstream data handling paths toggled freely. 111: The ETCLK_PE2 for RP2's upstream data handling paths toggled only when there are upstream data phases on going in RP2.
2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for ETCLK_PE2 for Downstream Data FIFO of RP2** As those described at RxBA[1], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-1}:** 0xx, 10x, or 110: The ETCLK_PE2 for RP2's downstream data FIFO toggled freely. 111: The ETCLK_PE2 for RP2's downstream data FIFO toggled only when the write data of the downstream write cycle were written into the FIFO or the read data returned from the device connected to the RP2 of the downstream read cycle were written into the FIFO.
0	RW	0	**Dynamic Stop for ETCLK_PE2 for Upstream Data FIFO of RP2** As those described at RxBA[0], only that this bit is for ETCLK_PE2 which is in RP2. And the level 1 bits changed to RxA0[7] and RxA8[2]. **{RxA0[7], RxA8[2], Bit-0}:** 0xx, 10-, or 110: The ETCLK_PE2 for RP2's upstream data FIFO toggled freely. 111: The ETCLK_PE2 for RP2's upstream data FIFO toggled only when the write data of the upstream write cycle were written into the FIFO or the read data returned from the DRAM (or other devices connected in the system for a peer-to-peer transfer, refer to Note) of the upstream read cycle were written into the FIFO. Note: Peer-to-peer cycle are those upstream requests (read or write from SB blocks or PCIe root ports) not targeted to CPU (which eventually to DRAM).

Offset Address: BDh (D0F4)

Dynamic Clock Stop for Clocks in Transaction Layer of PCIe Root Port 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Stop for ETCLK_PE3 for Upstream Paths of RP3** As those described at RxBA[7], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-7}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's upstream paths toggled freely. 111: The ETCLK_PE3 for RP3's upstream paths toggled only when there are upstream requests on going in RP3.
6	RW	0	**Dynamic Stop for ETCLK_PE3 for Downstream Paths of RP3** As those described at RxBA[6], RxBA[5], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-6}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's downstream paths toggled freely. 111: The ETCLK_PE3 for RP3's downstream paths toggled only when there are downstream requests on going in RP3.
5	RW	0	**Dynamic Stop for ETCLK_PE3 for Downstream Retry Path of RP3** As those described at RxBA[5], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-5}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's downstream retry paths toggled freely. 111: The ETCLK_PE3 for RP3's downstream paths toggled only when there are downstream retry transactions needed to be processed in RP3.
4	RW	0	**Dynamic Stop for ETCLK_PE3 for Downstream Retry FIFO of RP3** As those described at RxBA[4], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-4}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's downstream retry FIFO toggled freely. 111: The ETCLK_PE3 for RP3's downstream retry FIFO toggled only when the RP3 issued downstream cycle (directly from CPU's downstream cycle, not internally retried) to the device connected to the RP3.
3	RW	0	**Dynamic Stop for ETCLK_PE3 for Upstream Data Handling of RP3** As those described at RxBA[3], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-3}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's upstream data handling paths toggled freely. 111: The ETCLK_PE3 for RP3's upstream data handling paths toggled only when there are upstream data phases on going in RP3.
2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for ETCLK_PE3 for Downstream Data FIFO of RP3** As those described at RxBA[1], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-1}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's downstream data FIFO toggled freely. 111: The ETCLK_PE3 for RP3's downstream data FIFO toggled only when the write data of the downstream write cycle were written into the FIFO or the read data returned from the device connected to the RP3 of the downstream read cycle were written into the FIFO.
0	RW	0	**Dynamic Stop for ETCLK_PE3 for Upstream Data FIFO of RP3** As those described at RxBA[0], only that this bit is for ETCLK_PE3 which is in RP3. And the level 1 bits changed to RxA0[7] and RxA8[3]. **{RxA0[7], RxA8[3], Bit-0}:** 0xx, 10x, or 110: The ETCLK_PE3 for RP3's upstream data FIFO toggled freely. 111: The ETCLK_PE3 for RP3's upstream data FIFO toggled only when the write data of the upstream write cycle were written into the FIFO or the read data returned from the DRAM (or other devices connected in the system for a peer-to-peer transfer, refer to Note) of the upstream read cycle were written into the FIFO. Note: Peer-to-peer cycle are those upstream requests (read or write from SB blocks or PCIe root ports) not targeted to CPU (which eventually to DRAM).

Offset Address: BE-C1h (D0F4) – Reserved

Offset Address: C2h (D0F4)

Dynamic Clock Stop for Clocks in Data Link Layer & Link PMU within PCIe Root Port 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Dynamic Stop for EPCLK_PE0 for LPMU of RP0** Each root port of PCIe had one Link Power Management Unit (LPMU) associated with it. The EPCLK_PE0 is the main clock for the LPMU of root port 0 (RP0). This bit works with the level 1 bit, RxA0[7], to be the enable bit for the dynamic stop feature for the EPCLK_PE0. **{RxA0[7], Bit-4}:** 0x or 10: The EPCLK_PE0 toggled freely. 11: The EPCLK_PE0 toggled only when the PCIe link of RP0 changes its power management status.
3:2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for EDCLK_PE0 for Downstream Packets in DLL of RP0** EDCLK_PE0 is the main clock for the Data Link Layer (DLL) of PCIe root port 0 (RP0). This bit is the level 2 enable bit for the dynamic stop feature of the EDCLK_PE0 used for downstream (transmitting) packets handling of RP0. It works with level 1 bit, RxA0[7] and RxA8[0], to control the dynamic stop of EDCLK_PE0. **{RxA0[7], RxA8[0], Bit-1}:** 0xx, 10x, or 110: The EDCLK_PE0 for downstream packets handling in DLL of RP0 toggled freely. 111: The EDCLK_PE0 for downstream packets handling in DLL of RP0 toggled only when there are packets waited for transmitting to PCIe Physical Layer.
0	RW	0	**Dynamic Stop for EDCLK_PE0 for Upstream Packets in DLL of RP0** EDCLK_PE0 is the main clock for the Data Link Layer (DLL) of PCIe root port 0 (RP0). This bit is the level 2 enable bit for the dynamic stop feature of the EDCLK_PE0 used for upstream (receiving) packets handling of RP0. It works with level 1 bit, RxA0[7] and RxA8[0], to control the dynamic stop of EDCLK_PE0. **{RxA0[7], RxA8[0], Bit-0}:** 0xx, 10x, or 110: The EDCLK_PE0 for upstream packets handling in DLL of RP0 toggled freely. 111: The EDCLK_PE0 for upstream packets handling in DLL of RP0 toggled only when there are packets received from PCIe Physical Layer waited for processing.

Offset Address: C3h (D0F4)

Dynamic Clock Stop for Clocks in Data Link Layer & Link PMU within PCIe Root Port 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Dynamic Stop for EPCLK_PE1 for LPMU of RP1** As described in RxC2[4], only that this bit is for EPCLK_PE1 in RP1. **{RxA0[7], Bit-4}:** 0x or 10: The EPCLK_PE1 toggled freely. 11: The EPCLK_PE1 toggled only when the PCIe link of RP1 changes its power management status.
3:2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for EDCLK_PE1 for Downstream Packets in DLL of RP1** As described in RxC2[1], only that this bit is for EDCLK_PE1 in RP1. **{RxA0[7], RxA8[1], Bit-1}:** 0xx, 10x, or 110: The EDCLK_PE1 for downstream packets handling in DLL of RP1 toggled freely. 111: The EDCLK_PE1 for downstream packets handling in DLL of RP1 toggled only when there are packets waited for transmitting to PCIe Physical Layer.
0	RW	0	**Dynamic Stop for EDCLK_PE1 for Upstream Packets in DLL of RP1** As described in RxC2[0], only that this bit is for EDCLK_PE1 in RP1. **{RxA0[7], RxA8[1], Bit-0}:** 0xx, 10x, or 110: The EDCLK_PE1 for upstream packets handling in DLL of RP1 toggled freely. 111: The EDCLK_PE1 for upstream packets handling in DLL of RP1 toggled only when there are packets received from PCIe Physical Layer waited for processing.

Offset Address: C4h (D0F4)

Dynamic Clock Stop for Clocks in Data Link Layer & Link PMU within PCIe Root Port 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Dynamic Stop for EPCLK_PE2 for LPMU of RP2** As described in RxC2[4], only that this bit is for EPCLK_PE2 in RP2. **{RxA0[7], Bit-4}:** 0x or 10: The EPCLK_PE2 toggled freely. 11: The EPCLK_PE2 toggled only when the PCIe link of RP2 changes its power management status.
3:2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for EDCLK_PE2 for Downstream Packets in DLL of RP2** As described in RxC2[1], only that this bit is for EDCLK_PE2 in RP2. **{RxA0[7], RxA8[2], Bit-1}:** 0xx, 10x, or 110: The EDCLK_PE2 for downstream packets handling in DLL of RP2 toggled freely. 111: The EDCLK_PE2 for downstream packets handling in DLL of RP2 toggled only when there are packets waited for transmitting to PCIe Physical Layer.
0	RW	0	**Dynamic Stop for EDCLK_PE2 for Upstream Packets in DLL of RP2** As described in RxC2[0], only that this bit is for EDCLK_PE2 in RP2. **{RxA0[7], RxA8[2], Bit-0}:** 0xx, 10x, or 110: The EDCLK_PE2 for upstream packets handling in DLL of RP2 toggled freely. 111: The EDCLK_PE2 for upstream packets handling in DLL of RP2 toggled only when there are packets received from PCIe Physical Layer waited for processing.

Offset Address: C5h (D0F4)

Dynamic Clock Stop for Clocks in Data Link Layer & Link PMU within PCIe Root Port 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Dynamic Stop for EPCLK_PE3 for LPMU of RP3** As described in RxC2[4], only that this bit is for EPCLK_PE3 in RP3. **{RxA0[7], Bit-4}:** 0x or 10: The EPCLK_PE3 toggled freely. 11: The EPCLK_PE3 toggled only when the PCIe link of RP3 changes its power management status.
3:2	RW	0	**Reserved**
1	RW	0	**Dynamic Stop for EDCLK_PE3 for Downstream Packets in DLL of RP3** As described in RxC2[1], only that this bit is for EDCLK_PE3 in RP3. **{RxA0[7], RxA8[3], Bit-1}:** 0xx, 10x, or 110: The EDCLK_PE3 for downstream packets handling in DLL of RP3 toggled freely. 111: The EDCLK_PE3 for downstream packets handling in DLL of RP3 toggled only when there are packets waited for transmitting to PCIe Physical Layer.
0	RW	0	**Dynamic Stop for EDCLK_PE3 for Upstream Packets in DLL of RP3** As described in RxC2[0], only that this bit is for EDCLK_PE3 in RP3. **{RxA0[7], RxA8[3], Bit-0}:** 0xx, 10x, or 110: The EDCLK_PE3 for upstream packets handling in DLL of RP3 toggled freely. 111: The EDCLK_PE3 for upstream packets handling in DLL of RP3 toggled only when there are packets received from PCIe Physical Layer waited for processing.

Offset Address: C6-CFh (D0F4) – Reserved

Offset Address: D3-D0h (D0F4)
BIOS Extended Scratch Registers D - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers D – 1** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: D7-D4h (D0F4)
BIOS Extended Scratch Registers D - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers D – 2** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: DB-D8h (D0F4)
BIOS Extended Scratch Registers D - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers D – 3** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: DF-DCh (D0F4)
BIOS Extended Scratch Registers D - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers D – 4** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: E3-E0h (D0F4)
BIOS Extended Scratch Registers E - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers E – 1** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: E7-E4h (D0F4)
BIOS Extended Scratch Registers E - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers E – 2** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: EB-E8h (D0F4)
BIOS Extended Scratch Registers E - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers E – 3** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: EF-ECh (D0F4)
BIOS Extended Scratch Registers E - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**BIOS Extended Scratch Registers E – 4** This is a four bytes register space for BIOS or system software to store some temporary data.

Offset Address: F0h (D0F4)

Chip Miscellaneous Control -1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Resetting Registers to Default for North Bridge Registers** Programming 1 to this bit will reset the registers to hardware default value for North Bridge (NB) configuration registers. These includes functions at D0F0, D0F1, D0F2, D0F3, D0F4, D0F5, D0F6, D0F7, D3F0, D3F1, D3F2, D3F3, D3F4, and RCRB-H. 0: The NB's configuration registers maintained. 1: The NB's configuration registers as described above will all be reset to hardware default value.
3:0	RW	0	**Reserved**

Offset Address: F1h (D0F4) – Reserved

Offset Address: F2h (D0F4)

Chip Miscellaneous Control -2 **Default Value: 00h**

Bit	Attribut	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Forcing ASZ# at V4 CPU Bus for Upstream Cycle** Please refer to table 1.2 of D0F2. The ASZ[1:0]# field of the V4 CPU bus protocol defined as 00b/01b for a request under/above 4G. This bit is used to force the ASZ[1:0]# to 00 when the upstream cycles are driven on the V4 bus by the chip. 0: ASZ[1:0]# = 00b when address is less than 4G and ASZ[1:0]# = 01b when address is larger than or equal to 4G during an upstream request cycle. 1: ASZ[1:0]# will always be 00b during an upstream request cycle no matter whether the address of that requests is larger than 4G or not.
3	RW	0	**Reserved**
2	RW	0	**Disabling of the Assertion for Both HHIT#/HHITM#** This bit is to change the behavior of the HIT#/HITM# for non-posted downstream cycle targeted to non-DRAM agent. 0: HIT#/HITM# will both assert to stall the CPU bus when that downstream cycle cannot finish in no time. 1: Instead of asserting both HIT# and HITM# to stall the bus, the chip will do retry on the response phase.
1	RW	0	**Disabling of the Assertion of HBNR#** This bit is to change the behavior of the HBNR# for downstream cycles when the previous downstream cycles fill up the In Order Queues of the CPU bus controller. 0: When the In Order Queues are all occupied and left no room for more downstream cycles, the chip will assert HBNR# to block the next request coming from CPU. 1: When the In Order Queues are all occupied and left no room for more downstream cycles, the chip will assert HBPRI# to stop the CPU issuing cycles.
0	RW	0	**Eliminating tXSR time for Fast DRAM Access** A time call tXSR is required by DDR2 (200T) and DDR3 (500T) for accessing correctly after the CKE assertion. This bit is to eliminate this tXSR time for shortening the production testing vector size. 0: Normal DRAM accessing, i.e. DRAM controller will not issue the DRAM requests up to a tXSR time after the assertion of the MCKE[3:0] 1: Testing mode DRAM accessing, i.e. DRAM controller will issue the DRAM requests to DRAM no matter if the tXSR time is satisfied.

Offset Address: F3-FFh (D0F4) – Reserved

DEVICE 0 FUNCTION 5 (D0F5): APIC AND CENTRAL TRAFFIC CONTROL

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 37 below.

Device 0 Function 5 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 5. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**101**	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

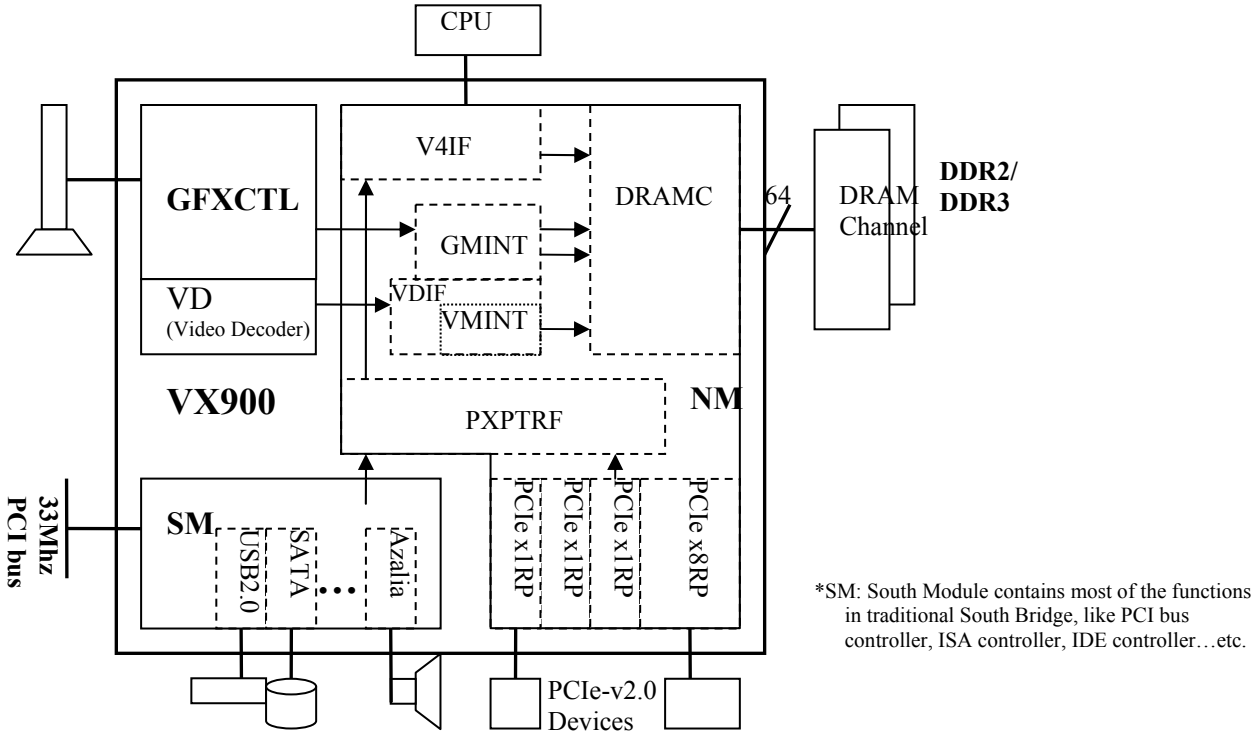


Figure 37. System Block Diagram for D0F5

The registers in this function are logic control for the central traffic controller module (PXPTRF) and an APIC controller (APICX). As shown in the shadow block in the block diagram provided in Figure 37, the central traffic controller handled the traffic in between CPU, PCIe root ports, graphic controller (GFXCTL), and other modules integrated in conventional SB (South Bridge). The APIC within the conventional NB (North Bridge) handled the interrupt requests from PCIe root ports.

A software programming view for this register space D0F5 is as shown in the shaded block in Figure 38 below.

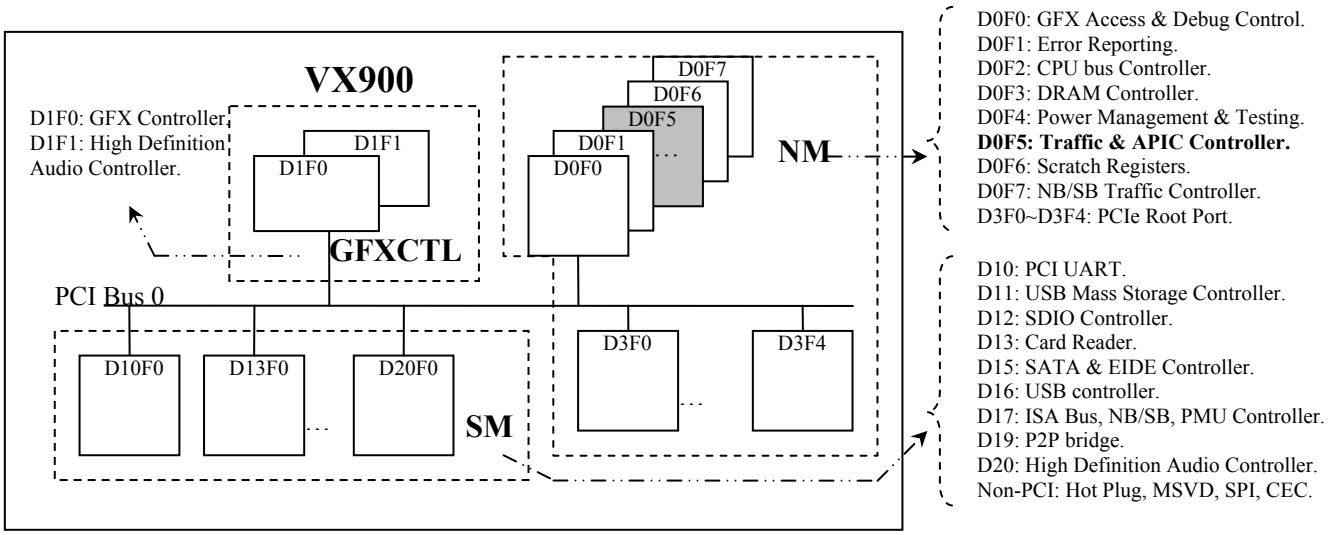


Figure 38. Register Level Block Diagram for D0F5

Header Registers (00–3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F5)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F5)

Device ID **Default Value: 5410h**

Bit	Attribute	Default	Description
15:0	RO	5410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F5)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RW	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F5)

PCI Status **Default Value: 0000h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RW1C	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RW1C	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	0	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus.
8	RW1C	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F5)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** They are the revision ID of this function.

Offset Address: 0B-09h (D0F5)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F5)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F5)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F5)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value of these bits are 80h. It indicates this is a multi-function device.

Offset Address: 0Fh (D0F5)
Build In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F5)
Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D0F5)
Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 1B-18h (D0F5)
Base Address Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F5)
Base Address Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 3** This function does not claim base address.

Offset Address: 23-20h (D0F5)
Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 4** This function does not claim base address.

Offset Address: 27-24h (D0F5)
Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 5** This function does not claim base address.

Offset Address: 2B-28h (D0F5)
CardBus CIS Pointer **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F5)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F5)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F5) – Reserved

Offset Address: 34h (D0F5)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F5) – Reserved

Offset Address: 3D-3Ch (D0F5)
Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F5)
Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

APIC Related Registers (40–5Fh)

Offset Address: 40h (D0F5)

APIC Access Control **Default Value: 4Ch**

Bit	Attribute	Default	Description
7	RW	0	**IO APIC Enable** An APIC (Advance Programmable Interrupt Controller) core is integrated in the conventional NB (North Bridge) block of this chip. This bit is the enabling switch for memory cycles with address APIC_addr where FECx_yzFFh >= APIC_addr >= FECx_yz00h to be forwarded to that APIC to do programming. Where x, y, and z are defined at bits [3:0] and Rx41[7:0]. 0: Disabled, the downstream memory cycles with address in the range described above will be forwarded to conventional SB module. They would end up appears on the 33Mhz PCI bus. 1: Enabled, the downstream memory cycles with address in the range described above will be forwarded to the internal APIC controller (APICX in Figure 37) in the NB block.
6	RW	1b	**Reserved**
5	RW	0	**Issuing MSI Cycles for the IRQ De-assertion** This bit is to control the occurring of MSI cycles for those IRQs connected to the APIC controller in the NB block. Those corresponding IRQs are from PCIe root port (0~3) and internal graphic controller (GFXCTL). 0: Disabled. Only the assertion of IRQs will trigger the MSI cycle be issued out. There will be no corresponding MSI cycles when IRQs de-asserted. 1: Enabled. IRQ assertion and de-assertion will both trigger the issuing of MSI cycles.
4	RW	0	**Reserved**
3:0	RW	Ch	**APIC Legacy Address Range – x** These bits are the 4 bits "x" for the APIC addressing FECx_yz--h defined by this chip. Value can be programmed are from 0h~Fh. Bit-7 is the enable bit for this APIC addressing decoding. Please refer to the description at bit-7 for more details.

Offset Address: 41h (D0F5)

APIC Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**APIC Legacy Address Range – y** These bits are the 4 bits "y" for the APIC addressing FECx_yz--h defined by this chip. Value can be programmed are from 0h~Fh. Rx40[7] is the enable bit for this APIC addressing decoding. Please refer to the description at Rx40[7] for more information.
3:0	RW	0	**APIC Legacy Address Range – z** These bits are the 4 bits "z" for the APIC addressing FECx_yz--h defined by this chip. Value can be programmed are from 0h~Fh. Rx40[7] is the enable bit for this APIC addressing decoding. Please refer to the description at Rx40[7] for more information.

Offset Address: 42h (D0F5)

APIC Interrupt Control - I **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**IRQ Transparent Mode** BT_INTR_ is an internal signal sending to the 8259 (Programmable Interrupt Controller or PIC) or wake up logic in the SB module. It is used as an IRQ signal to 8259 when the chip is in PIC mode (use 8259 as the interrupt handler) or as an wake up signal to wake the system up from C2 or C3 when the chip is in APIC mode (use APIC as the interrupt handler). BT_INTR_ is basically the result of logic OR of all IRQs existed in NB block. This bit is to determine if BT_INTR_ generation be blocked by the status of IRQ mask bit which is in the APIC controller in the NB block. 0: IRQ Transparent mode is enabled, i.e. BT_INTR_ will assert as long as there is IRQ active in the NB block. 1: IRQ Transparent mode is disabled, i.e. BT_INTR_ asserts only when there are IRQs asserted and the corresponding IRQ Mask bits are disabled. It is recommended to program this bit to 0 no matter what modes (PIC or APIC) the chip is in.
2:0	RW	0	**Reserved**

Offset Address: 43h (D0F5) – Reserved

Offset Address: 44h (D0F5)
APIC Interrupt Control - II **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**PCIe Device Uses MSI Cycle to Wake Up System from C3** PCIe Devices connected to Root Ports: RP0, RP1, RP2, or RP3 which might issues Message TLP (Transaction Layer Packets, please refer to PCIe base specification revision 1.0 or newer.) to this chip. The PCIe controller (please refer to D3F0~D3F3), translates that TLP to upstream memory write cycles. When this case happened, this bit is used to choose to assert BT_INTR_ to notify the wake up logic in SB module. Regarding to the BT_INTR_ function, please refer to the register descriptions at Rx42[3] for further information. 0: Disabled, BT_INTR_ won't be asserted when PCIe device issued MSI packets. 1: Enabled, BT_INTR_ will be asserted to wake up the system from C2 or C3 when PCIe device issued MSI packets. This bit should be programmed to 0/1 when this chip is operated at PIC/APIC mode. As for PIC/APIC mode .
0	RW	0	**Reserved**

Offset Address: 45-4Ch (D0F5) – Reserved

Offset Address: 4Dh (D0F5)
Backdoor register Control - I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Backdoor Revision ID and Device ID** This bit is to enable the backdoor revision ID and Device ID for this function, D0F5. 0: Disabled, issuing configuration read cycles to the Rx03~02 and Rx08 will have the default value at Rx03~02 and Rx08 be read back. 1: Enabled, in response to configuration read cycles to Rx03~Rx02/Rx08, this chip will return the value programmed at Rx4F~Rx4E/{0000, Bits [3:0]}.
6:4	RW	0	**Reserved**
3:0	RW	0	**Backdoor Revision ID** These bits are the backdoor registers for the revision ID bit[3:0]. When bit-7 = 1, the revision ID reported at Rx08 of this function will be {0000, Bits [3:0]}.

Offset Address: 4F-4Eh (D0F5)
Backdoor register Control - II **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Backdoor Device ID Back** These bits are the backdoor registers for the device ID. When Rx4D[7] = 1, the device ID reported at Rx03~02 of this function will be these 16 bits.

Offset Address: 50-5Fh (D0F5) – Reserved

Central Traffic - Downstream Control (60–7Fh)

Offset Address: 60h (D0F5)

Configuration Cycle Control - I **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**CF8/CFC Configuration Cycle Manner** This bit defined the PCI configuration manner using I/O cycles with address CF8h and CFCh. 0: Multiple I/O CFC cycles after one I/O CF8 write will all be considered as the PCI configuration cycles. 1: Configuration cycles happened in CF8 - CFC pairs. There must be an I/O CF8 write before an I/O CFC to be considered as a PCI configuration cycle. i.e. If a I/O CFC cycle comes in without an preceding I/O CF8 write, that I/O CFC will be treated as a normal I/O cycle and passed to PCI bus.
4	RW	0	**CF8 Byte Write Enable** In PCI defined configuration mechanism, the I/O CF8 write cycle must have Byte-Enable all (BE3~BE0) active This bit adds more flexibility. 0: I/O CF8 write cycles must have BE3~BE0 all active to be considered as a PCI configuration index write. Those CF8 cycle with partial BE active will be considered as a normal I/O cycle to be forwarded to PCI bus. 1: Even the I/O CF8 write with partial BE active, this chip still consider it is a valid PCI configuration index write cycle.
3	RW	0	**Configuration Cycles to the Secondary Bus behind the P2P Bridge** D3F0~D3F3 of this chip are PCIe Root Port (RP) which connected to PCIe devices. The configuration space structure for those RPs are P2P (PCI to PCI) bridges. According to the PCIe specification, there should be only one device behind this P2P bridge and it must be device 0. This bit provides more flexibility to this restriction for configuration cycles to those devices. 0: Type 1 Configuration cycles for all the devices will be passed through RP0~RP3 to the devices behind them. 1: Only type 1 configuration cycles for device 0 will be passed through RP0~RP3 to the devices behind them.
2	RW	0	**Reserved**
1:0	RW	0	**Extended Configuration Space Access** These two bits defined the access capability of the extended configuration space for this chip. 00: Extended Configuration Space is disabled, i.e. only 256 bytes of conventional PCI register space (offset 00~FFh) is available. 01: Reserved. 10: Extended Configuration Addressing mode is enabled. 11: Memory Mapped Configuration Access mode is enabled. Rx61[7:0] must also be programmed to a value other than 00h to have this mode work correctly.

Offset Address: 61h (D0F5)

Configuration Cycle Control - II **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Addressing for Memory Mapped Configuration Access** These bits defined the addressing for configuration space accessing when in Memory Mapped Configuration Access mode (Rx60[1:0] = 11b). 00h: Memory Mapped Configuration Access mode is disabled. Others: These register bits are the address bit[35:28] for the memory mapped configuration space.

Offset Address: 62-63h (D0F5) – Reserved

Offset Address: 64h (D0F5)

Traffic Flow Control – Downstream & Upstream - I **Default Value: F2h**

Bit	Attribute	Default	Description
7	RW	1b	**Blocking Peer-to-Peer Downstream Requests** When upstream arbiter in the PXPTRF is disabled (IOW 22h, 1h; I/O write 1 to I/O port 22 bit[0]) to block all the upstream requests, this bit is to block the downstream peer-to-peer (P2P) cycles. The so-called P2P cycles could be like upstream PCIe requests targeted to another PCIe device, or SB's devices, or even the internal GFX device. 0: Disabled, i.e. downstream P2P cycles are processed normally. 1: Enabled, i.e. downstream P2P requests will be held at the upstream queues till the arbiter in the PXPTRF is enabled (IOW 22h, 0h).
6	RW	1b	**Splitting Downstream QW Request to GFXCTL into DW Access** This bit is to split the downstream QW requests (either 1QW or 8QW) targeted to legacy VGA space (memory address = A_xxxxh, B_xxxxh) into several DW requests. Those cycles to PCI defined memory based ranges will always be at QW accessing no matter what the status of this bit is. 0: Disabled. 1: Enabled.
5	RW	1b	**Reserved**
4	RW	1b	**Downstream Cycles to Flush Upstream Write** When traffic controller (PXPTRF) received memory read, I/O read, or I/O write (non-posted) cycles from the V4IF (CPU bus controller), it processed one and only one of these cycles without accepting any further request until the cycle is finished with a response from the target. 0: Disabled, upon seeing the response from the target, PXPTRF immediately returns data ready signal to the V4IF to finish the current downstream cycle. 1: Enabled, upon seeing the response from the target, PXPTRF will flush those upstream write cycles currently queued in the PXPTRF upstream controller. It won't return the data ready signal to the V4IF to finish the current downstream cycle until those upstream write cycles (Note those upstream cycles come in after the response from the target is not included) are all flushed out.
3	RW	0	**Blocking Downstream Cycles to PCIe** This bit is enabled to block downstream cycles to PCIe root port when it is in L1 or L2 power state. 0: Disabled. 1: Enabled
2	RW	0	**Blocking Upstream PCIe Cycles** This bit is to block the upstream PCIe cycles when system is in non-S0 system state or C3/C4/C4P CPU power state. Note the main PLL of the NB block is reset or the clock output of the PLL is disabled when in those power states. 0: Disabled. 1: Enabled. For the chip to run normally when the power management is turn on, this bit should always be set to 1.
1	RW	1b	**Downstream Write Request Timing** Upon receiving memory write requests from the CPU, this bit is to control the request issuing of the downstream memory write cycles to their target agents. 0: PXPTRF will not issue the downstream write requests until the write data from the CPU bus are received completely. 1: PXPTRF will issue downstream write requests once the request from the CPU is received. The data can be arranged by another data flow control. It is suggested to set this bit to 1 so that the latency of the downstream write is shortened.
0	RW	0	**In Order Downstream Cycles** This bit is to control if the posted write transaction can pass the previous non-posted downstream cycles (memory read, I/O read, or I/O write cycles). 0: Disabled, Downstream post write transaction can be issued out to its target before the completion of the previous non-posted cycle. 1: Enable. Downstream post write transaction won't be issued out until the transaction of the previous non-posted cycle is finished.

Offset Address: 65-67h (D0F5) – Reserved

Offset Address: 6B-68h (D0F5)

RCRB-H Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RW	0	**Reserved**
23:0	RW	0	**Base Address[35:12] of RCRB-H** Root Complex Register Block (RCRB) is a register file for the root complex structure needed for a group of PCIe root ports. In this chip, RCRB-H is the RCRB associated with the root complex. RCRB-H has 4K bytes in size, and can be addressed using address bit[11:0]. These registers defined the base address bit[35:12] for the RCRB-H. 000000h: The accessing to the RCRB-H is disabled. Other values rather than 000000h, said abcdefh: Memory cycles with address [35:12] = abcdefh will be directed to the RCRB-H. And address [11:0] is the offset to the registers which user is intended to access.

Offset Address: 6C-7Fh (D0F5) – Reserved

Central Traffic - Upstream Control (80-9Fh)

Offset Address: 80h (D0F5)

Traffic Flow Control – Upstream - I **Default Value: 80h**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved**
6:4	RW	0	**Reserved**
3	RW	0	**Upstream Request 1T Earlier** This bit defined the upstream protocol for the request phase in between PXPTRF and V4IF (CPU bus controller). 0: Normal latency for upstream request. 1: 1T reduction for the latency of upstream request.
2	RW	0	**Reserved**
1	RW	0	**Upstream Read Data Returning Path** This bit controls the data return latency for the upstream read requests from PXPTRF to the V4IF (CPU bus controller). 0: 2-level synchronous FIFO for V4IF to PXPTRF. 1: 1-level synchronous FIFO for V4IF to PXPTRF.
0	RW	0	**Reserved**

Offset Address: 81h (D0F5)

Traffic Flow Control – Downstream & Upstream - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Reducing 1T Latency for Upstream Requests from SB module** This bit is to reduce the latency of the upstream requests from SB module to PXPTRF by 1T. 0: Disabled, normal latency for requests from SB to PXPTRF. 1: Enabled, latency is reduced by 1T for requests from SB to PXPTRF.
5	RW	0	**Reducing 1T Initial Latency for Downstream Write Data to PCIe** This bit is to reduce the initial latency of the write data for the downstream write cycles from PXPTRF to PCIe Root Port 0 ~ 3. 0: Disabled, normal latency. 1: Enabled, latency is reduced by 1T.
4	RW	0	**Peer-to-Peer 8QW Access Capability** Peer-to-peer (P2P) cycles are those upstream requests (read or write from SB module, or PCIe Root port 0~3) not targeted to CPU, i.e., Root Port 0~3, SB module, or internal Graphic Controller (GFXCTL). PXPTRF will put those requests into a P2P queue and issue requests to downstream controller which handles all the downstream cycles. This bit is an option to split those 4QW based P2P requests into 1QW request. 0: Disabled, PXPTRF will split 4QW/8QW requests to 1QW requests to downstream controller. 1: Enabled, PXPTRF will send those upstream P2P 4QW/8QW request cycles as 4QW/8QW request to downstream controller.
3	RW	0	**Reducing 1T Latency for PCIe Upstream Requests** This bit is to reduce the latency of the PCIe upstream requests for 1T. 0: Disabled, normal latency for requests from PCIe to PXPTRF. 1: Enabled, latency is reduced by 1T for requests from PCIe to PXPTRF.
2	RW	0	**Reducing 1T Latency for Upstream Read Data returned** This bit is to reduce 1T latency for the read data return for upstream read requests to V4IF (CPU bus controller). 0: Disabled, normal latency for read requests from PXPTRF to V4IF. 1: Enabled, latency is reduced by 1T for read requests from PXPTRF to V4IF
1	RW	0	**Upstream MSI Address FEEx_xxxxh Decoding** This traffic controller (PXPTRF) will decode the address of an upstream request and check them against those MSI address programmed at the MSI capability table reported at the capability lists of every root ports (RP0~RP3). When PXPTRF decode the MSI cycle, it will tell CPU bus controller (V4IF) to put those high DW data on to the low DW before that MSI cycle is put to the CPU bus. (No matter what the MSI's address is, the valid MSI data should be always on the low DW on the CPU bus) This bit tells the PXPTRF not just to check address matching with those programmed at MSI tables but also to check the conventional MSI address: FEEx_xxxxh. 0: Disabled, PXPTRF only decode MSI cycles against those programmed in the MSI capability table. 1: Enabled, PXPTRF not only decode MSI cycles against those programmed in the MSI capability table, but it also check the MSI cycle against the conventional MSI address: FEEx_xxxxh.
0	RW	0	**Peer-to-peer Read Cycle to Trigger AGPBUSY** An internal signal call AGPBUSY, which is used to be a signal pin connected from NB to SB back in time when NB and SB are separate two chips, will be asserted to wake up the system from sleeping power state. An downstream or upstream cycles should be able to make this signal asserted. This bit is to allow this chip keep this signal AGPBUSY de-asserted when a peer-to-peer (P2P, please refer to bit-4) read cycle comes in. 0: AGPBUSY will be asserted when a P2P read cycle comes. i.e. the system will wake up from the sleeping state. 1: AGPBUSY will not be asserted when a P2P read cycle comes. i.e. the system could remain staying at sleeping state.

Offset Address: 82h (D0F5) – Reserved

Offset Address: 83h (D0F5)

Downstream Arbitration – Occupancy Time - I **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**Minimum Occupancy Time for Peer-to-peer Downstream Write Request** PXPTRF(this traffic controller) had a downstream arbitration unit which arbitrates downstream requests between CPU, P2P(please refer to Rx81[4]) read request, and P2P write request. Each source did have an occupancy timer which is used to guarantee a minimum time slot for the downstream controller to process its requests once it is granted. These registers are to specify the expiration time for the occupancy timer for P2P downstream writes (please also refer to Rx84[3:0] and bits [3:0]). Of course, if the requests of P2P write does not have that many requests needed to be served, the arbiter is able to grant to others before the expiration of this occupancy time. 0000: Occupancy timer is off, i.e. the arbitration will be a Round Robin scheme, i.e. one request is served before the arbiter switch to other requests. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. The unit T is calculated using HCLK, CPU bus controller's main clock.
3:0	RW	0001b	**Minimum Occupancy Time for Peer-to-peer Downstream Read Request** PXPTRF(this traffic controller) had a downstream arbitration unit which arbitrates downstream requests between CPU, P2P(please refer to Rx81[4]) read request, and P2P write request. Each source did have an occupancy timer which is used to guarantee a minimum time slot for the downstream controller to process its requests once it is granted. These registers are to specify the expiration time for the occupancy timer for P2P downstream reads (please also refer to Rx84[3:0] and bits [3:0]). Of course, if the requests of P2P read does not have that many requests needed to be served, the arbiter is able to grant to others before the expiration of this occupancy time. 0000: Occupancy timer is off, i.e. the arbitration will be a Round Robin scheme, i.e. one request is served before the arbiter switch to other requests. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. The unit T is calculated using HCLK, CPU bus controller's main clock.

Offset Address: 84h (D0F5)

Downstream Arbitration – Occupancy Time - II **Default Value: 05h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0101b	**Minimum Occupancy Time for CPU Downstream Request** PXPTRF(this traffic controller) had a downstream arbitration unit which arbitrates downstream requests between CPU, P2P(please refer to Rx81[4]) read request, and P2P write request. Each source did have an occupancy timer which is used to guarantee a minimum time slot for the downstream controller to process its requests once it is granted. These registers are to specify the expiration time for the occupancy timer for CPU downstream requests (please also refer to Rx84[3:0] and bits [3:0]). Of course, if the requests of CPU downstream does not have that many requests needed to be served, the arbiter is able to grant to others before the expiration of this occupancy time. 0000: Occupancy timer is off, i.e. the arbitration will be a Round Robin scheme, i.e. one request is served before the arbiter switch to other requests. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. The unit T is calculated using HCLK, CPU bus controller's main clock.

Offset Address: 85h (D0F5)

Traffic Flow Control – Downstream & Upstream - III **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Abortion of Peer-to-peer Cycles Issued to SB Module** This bit is enabled to abort any Peer-to-peer (P2P, refer to Rx81[4]) cycles to SB modules. 0: Disabled, P2P cycles targeted to SB module are processed normally. 1: Enabled, P2P cycles targeted to SB module will be aborted. i.e. the P2P read cycle will be returned with data = FFFF_FFFFh, and the data for the P2P write cycle will be discarded. It is suggested to set this bit to 1.
6	RW	0	**Holding the Downstream Cycle on Non-posted Cycle to SB Module** PXPTRF(this traffic controller) is able to handle the downstream write cycles pass the previous downstream read cycles as long as these two downstream cycles are directed to different agents (i.e. for the same agents, the downstream cycles will always be in ordered). This bit is enabled to have PXPTRF to hold the read/write cycle following a downstream non-posted cycle to SB module till that cycle is finished. 0: Disabled. 1: Enabled.
5	RW	0	**Reserved**
4	RW	0	**Reducing 1T Latency for Upstream Requests** This bit reduced the latency of arbitration for the upstream requests from SB module, PCIe root ports, and GFXCTL. 0: Upstream arbiter of PXPTRF(this traffic controller) arbitrates when upstream request queue becomes non-empty. 1: Upstream arbiter of PXPTRF arbitrates while upstream queues are filling with requests, i.e. 1T earlier than the case when this bit is 0.
3	RW	0	**Ordering Rule for Upstream read from PCIe** For PCIe root ports (RP0~RP3), there are upstream read/write cycles to CPU, other PCIe root ports, SB modules, or GFXCTL. These upstream requests to different targets basically do not have ordering relationship. This bit provides an ordering rule to these cycles. 0: PCIe upstream read request to CPU won't be issued out until the previous P2P (please refer to Rx81[4]) read cycle is finished. 1: PCIe upstream read request to CPU will be issued out no matter if the previous P2P read cycle is finished or not.
2:0	RW	0	**Reserved**

Offset Address: 86h (D0F5)

Traffic Flow Control – Downstream & Upstream - IV **Default Value: 0Dh**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Blocking Upstream MSI When in C5 State** When this chip is in C5 state, the data inside the CPU's cache are all flushed out, upstream cycles could be directed to DRAM. This bit is to block the upstream MSI cycle until the system leaves C5 and goes back to C0 normal state. 0: MSI request is not blocked when in C5 state, and is sent to CPU bus. 1: MSI request is blocked when in C5 state. It can be sent to the CPU bus only when the chip goes back to C0 normal state. This bit should be set to 1 for normal operation.
3	RW	1b	**Flushing GFX Upstream for Dynamic FSB Process** Dynamic FSB is a feature of VIA's CN series CPU to change the frequency of the CPU's running clock dynamically. Before the chip goes into the process of clocking downshift or upshift, PXPTRF (this traffic controller) should block all the upstream cycles to the CPU bus. This register bit is enabled to flush all the upstream requests in the queues inside Graphic Controller (GFXCTL). 0: This chip goes into the clocking changing process without flushing all the upstream requests in the GFXCTL. 1: This chip won't go into the clocking changing process unless the upstream requests in the GFXCTL are all processed. This bit should be set to 1 for normal operation.
2	RW	1b	**Peer-to-Peer 4QW Write Cycle Support** For supporting Peer-to-peer transactions (please refer to Rx81[4]) PXPTRF (this traffic controller) could break 8QW cycles into 8 1QW cycles. This register bit provides the option to support 4QW cycles when the P2P write transaction is targeted to PCIe root ports (RP0~RP3) or GFXCTL. 0: Disabled, 4QW P2P write cycles will be split into 4 1QW cycles. 1: Enabled, 4QW P2P write cycles will be considered as one transaction to the target. It is suggested to set this bit to 1 for better performance.
1	RW	0	**Adding 1T latency for Upstream Request from GFXCTL** This bit is to add one T of latency for the upstream request signal from GFXCTL (graphic controller) to PXPTRF (this traffic controller). 0: Adding 1T latency for request signals from GFXCTL to PXPTRF. 1: PXPTRF will take the request signal directly from GFXCTL. It is suggested to set this bit to 0 for best timing margin.
0	RW	1b	**Merging for Upstream Write Requests from GFXCTL** This bit is enabled to merge the upstream 2QW write requests from GFXCTL into 4QW write requests. These cycles were sent to CPU bus and eventually to the DRAM bus. Consecutive merged 4QW cycles from GFXCTL will greatly increase the performance. 0: Disabled. 1: Enabled.

Offset Address: 87h (D0F5)

Traffic Flow Control – Downstream - I **Default Value: 02h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Block Null Write Cycle to GFX** This bit is to control the abort mechanism for downstream null write cycle to GFX. 0: Downstream null write cycle can be sent to GFX 1: Downstream null write cycle target to GFX will be aborted
2	RW	0	**Downstream Write Data Timing to GFXCTL** This bit controls the internal signal behavior for downstream write cycles to GFXCTL. 0: PXPTRF (the traffic controller) won't assert signal (*write data ready*) to GFXCTL unless the downstream request had been sent out to GFXCTL. 1: The PXPTRF asserts signal (*write data ready*) to GFXCTL based on the fact if the data is in the data buffer, regardless if the downstream request had been issued to GFXCTL or not. For normal operation, this bit should be always set to 0.
1	RW	1b	**Downstream Read Request Level** This bit is to adjust the levels of the downstream read request queues resided in between PXPTRF (this traffic controller) and the V4IF (CPU bus controller). 0: 1 level. 1: 2 levels.
0	RW	0	**Reserved**

APB Interface

Two modules inside the VD (Video Decoder) needs to be programmed for Video Data to be correctly transferred to display unit in the GFXCTL. Internal bus protocol in between PXPTRF and VD is APB interface defined by AMBA 3 protocol, please refer to Figure 39 below. Those two modules can be programmed from CPU or CR (Command Regulator) in GFXCTL. In order to make sure the bandwidth coming from CPU and GFXCTL being able to be adjusted. A few registers are added in Rx88 and Rx89.

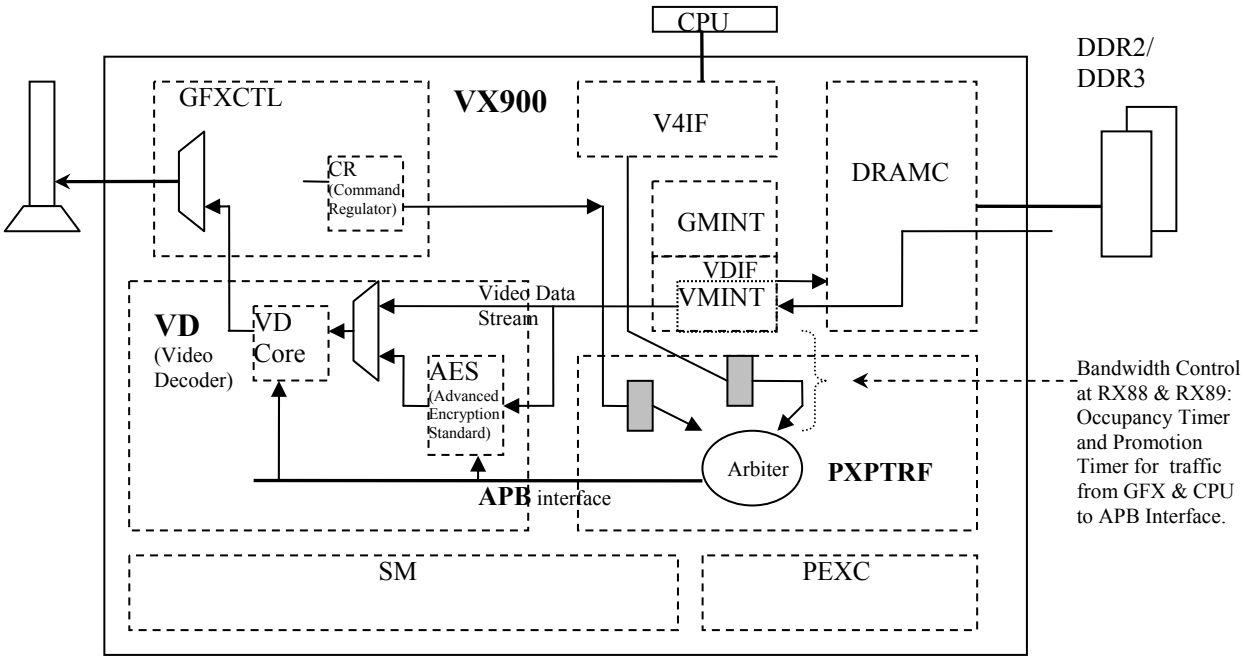


Figure 39. Rx88.1 Flow Control for Video Decoder's Data in between VD and PXPTRF

Offset Address: 88h (D0F5)

Occupancy Timer for Command Bandwidth to VD **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Maximum Occupancy Time for Commands from GFXCTL to VD** Please refer to Figure 39. There is a bandwidth timer for commands from GFXCTL to VD. These registers defined the expiration time for that bandwidth timer. When the arbiter in the PXPTRF processes consecutive commands from the GFXCTL and CPU to VD, it will continue serving the commands from GFXCTL for the time limited by these registers before it shifts to serve the commands from CPU. 0000: Occupancy timer is off, i.e. Once the arbiter serves the commands from GFXCTL, it won't switch to serve those commands from CPU until all the requests from GFXCTL had all been served. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. Note: This unit is one CPU bus controller's clock.
3:0	RW	0	**Maximum Occupancy Time for Commands from CPU to VD** Please refer to Figure 39. There is a bandwidth timer for commands from CPU to VD. These registers defined the expiration time for that bandwidth timer. When the arbiter in the PXPTRF processes consecutive commands from the GFXCTL and CPU to VD, it will continue serving the commands from CPU for the time limited by these registers before it shifts to serve the commands from GFXCTL. 0000: Occupancy timer is off, i.e. Once the arbiter serves the commands from CPU, it won't switch to serve those commands from GFXCTL until all the requests from CPU had all been served. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. Note: The unit is one CPU bus controller's clock.

Offset Address: 89h (D0F5)

Priority Promotion Timer for Command to VD **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**Priority Promotion Time for Commands from GFXCTL to VD** Please refer to Figure 39. Besides a bandwidth timer (Rx88[7:4]) to guarantee the bandwidth from GFXCTL to VD, there is also a priority promotion timer. This timer is to guarantee at least one request can be served within a particular time. These registers defined an expiration time for the commands from GFXCTL to be promoted as high priority. Initially, commands from either GFXCTL and CPU are treated as normal requests. The priority promotion timer started counting as long as there is request coming in. If this promotion timer expired before the arbiter is able to serve the commands from GFXCTL, those requests from GFXCTL will be treated as high priority and be served immediately. Note that once it is served, the priority timer resets, and it will start another run of counting if there are requests behind the one just served. 0000: Promote timer is off, i.e. the requests from GFXCTL will never be promoted to high priority. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. Note: The unit is one CPU bus controller's clock.
3:0	RW	0001b	**Priority Promotion Time for Commands from CPU to VD** Please refer to Figure 39. Besides a bandwidth timer (Rx88[3:0]) to guarantee the bandwidth from CPU to VD, there is also a priority promotion timer. This timer is to guarantee at least one request can be served within a particular time. These registers defined an expiration time for the commands from CPU to be promoted as high priority. Initially, commands from either GFXCTL and CPU are treated as normal requests. The priority promotion timer started counting as long as there is request coming in. If this promotion timer expired before the arbiter is able to serve the commands from CPU, those requests from CPU will be treated as high priority and be served immediately. Note that once it is served, the priority timer resets, and it will start another run of counting if there are requests behind the one just served. 0000: Promote timer is off, i.e. the requests from CPU will never be promoted to high priority. 0001: 1 x 4 T. 0010: 2 x 4 T. ….. 1111: 15 x 4 T. Note: The unit is one CPU bus controller's clock.

Offset Address: 8A-8Fh (D0F5) – Reserved

Offset Address: 91-90h (D0F5)

GFX ROMSIP 0 **Default Value: nnnnh**

Bit	Attribute	Default	Description
15:0	RW	0040h ROMSIP	**GFX ROMSIP Registers Group 0** These 16 bits registers are latched during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are the third QW, byte1 and byte0 – with bit[15] and bit[0] of this register mapped to byte1[7] and byte0[0] respectively. Note that these registers are provided for operating options provided to GFXCTL (internal integrated graphic controller). The meaning of each bits are listed in Table 25. Also note that these registers are also stored as EXSR registers in the VGA space which can be accessed through I/O write 3C4h and I/O read/write 3C5h.

Table 25. Rx90.1: Bits Definition for Rx91-90h

Bits at Rx91~Rx90	ROMSIP Location	EXSR_address *1 when EXSR_5A[0] = 0 *2	What are the registers' meaning?
[15]	Third QW, byte 1, bit[7:0]	EXSR_12[7]	Reserved
[14]		EXSR_13[7]	Reserved
[13:11]		EXSR_13[6,2:1]	DVP1 output port *3 selection: 00-: DVP-TV output. 01-: DVP-TV with alpha output. 100: Digital TV, Y/Cb/Cr 10 bit data output. 101: Digital TV, Y/Cb/Cr 8 bit data output. 110: Digital TV, Y/Cb/Cr 20 bit data output. 111: Digital TV, Y/Cb/Cr 16 bit data output.
[10]		EXSR_13[5]	Reserved
[9]		vcc/a	Reserved
[8]		EXSR_13[3]	Reserved, must be set to 0.
[7]	Third QW, byte 0, bit[7:0]	EXSR_13[0]	Reserved
[6]		EXSR_12[6]	Reserved, must be set to 0.
[5]		EXSR_12[5]	Reserved
[4]		EXSR_12[4]	Reserved
[3]		vcc/a	Reserved *4
[2:0]		vcc/a	Reserved

Notes:

1. This register can also be read from GFXCTL's register space using {IOW 3C4, EXSR_addr; IOR 3C5;} e.g. EXSR_13 can be accessed through {IOW 3C4, 13; IOR 3C5;}
2. When EXSR_5A[0] is programmed to 1, the result for {IOW 3C4, EXSR_addr; IOR 3C5;} will have different meaning defined by the GFXCTL.
3. DVP1 (Digital Visual Port 1) output port involved the following chip pins: DVP1D[15:0], DVP1DE, DVP1TVFLD, DVP1HS,DVP1VS, PVP1CLK, DVP1TVCLKR.
4. This bit is used to be bit[3] of the Panel type which works with the other three strapping pins to complete the selection. In VX900 Series, these four penal type selection pins are all from strapping pins, please refer to Table 26.

Table 26. Rx90.2: Panel Type Selection

Strapping Pins	EXSR_address when EXSR_5A[0] = 0	What do the registers mean?			
DVP1D[3:0]	EXSR_12[3:0]	EXSR_12[3:0]: Panel type in (# of Active Horizontal Pixels) x (# of Active Vertical Pixels)			
		0000: 640 x 480.	0001: 800 x 600.	0010: 1024 x 768.	0011: 1280 x 768.
		0100: 1280 x 1024.	0101: 1400 x 1050.	0110: 1440 x 900.	0111: 1280 x 800.
		1000: 800 x 480.	1001: 1024 x 600.	1010: 1366 x 768.	1011: 1600 x 1200.
		1100: 1600 x 1050.	1101: 1920 x 1200.	1110: 640 x 240.	1111: 1024 x 576.

Offset Address: 93-92h (D0F5)

GFX ROMSIP 1 **Default Value: nnnnh**

Bit	Attribute	Default	Description
15:0	RW	0 ROMSIP	**GFX ROMSIP Registers Group 1** These 16 bits registers are latched during the ROMSIP right after the de-assertion of PCIRST#. The corresponding programming bits are the third QW, byte3 and byte2 – with bit[15] and bit[0] of this register mapped to byte3[7] and byte2[0] respectively. Note that these registers are provided for operating options provided to GFXCTL (internal integrated graphic controller). The meaning of these bits are listed in Table 27. Also note that these registers are also stored as EXSR registers in the VGA space which can be accessed through I/O write 3C4h and I/O read/write 3C5h.

Table 27. Rx92.1: Bits Definition for Rx93-92h

Bits at Rx93~Rx92	ROMSIP location	EXSR_address *1 when EXSR_5A[0] = 1 *2	What the registers meaning?
[15:14]	Third QW, byte 3, bit[7:0]	EXSR_13[7:6]	Integrated LVDS/TMDS mode *3 selection: 00: LVDS 01: Reserved 10: Reserved 11: Reserved
[13:11]		EXSR_13[5:3]	Reserved
[10:8]		EXSR_13[2:0]	DAC (TV/CRT) output mode *4 selection: 0--: DAC A/B/C used for R/G/B for CRT. 100: DAC A/B/C used for C/Y/CVBS fro TV 101: DAC A/B/C used for C/Y/Y for TV 110: DAC A/B/C used for R/G/B for TV 111: DAC A/B/C used for Pr/Y/Pb for TV
[7:4]	Third QW, byte 2, bit[7:0]	EXSR_12[7:4]	Reserved
[3:0]		EXSR_12[3:0]	Capture Port *4 type selection: 0000: CAP 8 bit CCIR656. 0001: CAP 8 bit CCIR601. 0010: CAP 8 bit VIP 1.1. 0011: CAP 8 bit VIP 2.0. 0100: CAP 16 bit CCIR656. 0101: CAP 16 bit CCIR601. 0110: CAP 16 bit VIP 1.1. 0111: CAP 16 bit VIP 2.0. 1---: TS (Transfer Stream, Parallel and Serial) 8 bit.

Notes:

1. This register can also be read from GFXCTL's register space using {IOW 3C4, addr; IOR 3C5;} e.g. EXSR_13 can be accessed through {IOW 3C4, 13; IOR 3C5;}
2. When EXSR_5A[0] is programmed to 0, the result for {IOW 3C4, EXSR_addr; IOR 3C5} will have different meaning defined by the GFXCTL.
3. LVDS/TMDS uses the following pins: LVDSENVDD, LVDSENBL, LVDSPWM, LVDSD[3:0]P/VCC, LVDSCLKP/VCC, DVISWG_REXT.
4. Capture port use the following pins: VCPD[15:0], VCPHS, VCPVS, VCPCLK.

Offset Address: 94-9Fh (D0F5) – Reserved

PCIe Message Controller and Power Management (A0–FFh)

Offset Address: A0h (D0F5)

PCIe PMU Status - I **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCI Express Wake Activation** When the PCIe devices connected to the root port 0, 1, 2, and 3 sent PM_PME messages to this chip, registers at Rx62[0] of D3F0~3 are set. This register is enabled to allow the assertion of the status of Rx62[0] of D3F0~3 to wake up the power management unit in the SB block, which then wake up the system. 0: Disabled. 1: Enabled.
6:4	RW	0	**Reserved**
3	RW1C	0	**PME_TO_ACK Acknowledge Status for RP3** This bit is a PME status bit for the PCIe endpoint device connected on RP3 (Root Port 3). When RxF0[7] is programmed to 1, this chip will send PM_TRUN_OFF messages to the end point devices connected to RP0 ~ RP3 to notify that the system intends to put the PCIe Link to L2_L3_Ready State (Note). Upon receiving the PM_TURN_OFF message, endpoint device connected to RP3 will send back the message PME_TO_ACK when it is ready to go to L2_L3_Ready state. When this chip received the PME_TO_ACK from end pint device on RP3, this bit will be set to 1. 0: This chip did not receive PME_TO_ACK from the device connected to RP3. 1: This chip had received the PME_TO_ACK from the device connected to RP3. Writing 1 to this bit clears the register value back to 0.
2	RW1C	0	**PME_TO_ACK Acknowledge Status for RP2** This bit is a PME status bit for the PCIe endpoint device connected on RP2 (Root Port 2). When RxF0[7] is programmed to 1, this chip will send PM_TRUN_OFF messages to the end point devices connected to RP0 ~ RP3 to notify that the system intends to put the PCIe Link to L2_L3_Ready State (Note). Upon receiving the PM_TURN_OFF message, endpoint device connected to RP2 will send back the message PME_TO_ACK when it is ready to go to L2_L3_Ready state. When this chip received the PME_TO_ACK from end pint device on RP2, this bit will be set to 1. 0: This chip did not receive PME_TO_ACK from the device connected to RP2. 1: This chip had received the PME_TO_ACK from the device connected to RP2. Writing 1 to this bit clears the register value back to 0.
1	RW1C	0	**PME_TO_ACK Acknowledge Status for RP1** This bit is a PME status bit for the PCIe endpoint device connected on RP1 (Root Port 1). When RxF0[7] is programmed to 1, this chip will send PM_TRUN_OFF messages to the end point devices connected to RP0 ~ RP3 to notify that the system intends to put the PCIe Link to L2_L3_Ready State (Note). Upon receiving the PM_TURN_OFF message, endpoint device connected to RP1 will send back the message PME_TO_ACK when it is ready to go to L2_L3_Ready state. When this chip received the PME_TO_ACK from end pint device on RP1, this bit will be set to 1. 0: This chip did not receive PME_TO_ACK from the device connected to RP1. 1: This chip had received the PME_TO_ACK from the device connected to RP1. Writing 1 to this bit clears the register value back to 0.
0	RW1C	0	**PME_TO_ACK Acknowledge Status for RP0** This bit is a PME status bit for the PCIe endpoint device connected on RP0 (Root Port 0). When RxF0[7] is programmed to 1, this chip will send PM_TRUN_OFF messages to the end point devices connected to RP0 ~ RP3 to notify that the system intends to put the PCIe Link to L2_L3_Ready State (Note). Upon receiving the PM_TURN_OFF message, endpoint device connected to RP0 will send back the message PME_TO_ACK when it is ready to go to L2_L3_Ready state. When this chip received the PME_TO_ACK from end pint device on RP0, this bit will be set to 1. 0: This chip did not receive PME_TO_ACK from the device connected to RP0. 1: This chip had received the PME_TO_ACK from the device connected to RP0. Writing 1 to this bit clears the register value back to 0.

Note: Usually software should put the device in D3 state before the PM_TURN_OFF message is sent.

Offset Address: A1h (D0F5)
PCIe PMU Status - II **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PM_PME Message Status** When a PCIe endpoint device requests to wake up from the D1, D2 or D3 state, it will issue PM_PME message to the root port in this chip. The PM_PME messages combined with other hot plug signals defined for the PCIe root port will be stored in the Rx62[0] of D3F0~D3F3 (RP0 ~ RP3). This bit reflects the OR function of these signals. 0: No PM_PME message or equivalent hot plug event was recorded in either one of the root ports. 1: At least one PM_PME message or equivalent hog plug event was received at the PCIe root ports. The chip can wake up the system through appropriate programming at the PMU related logic, D17F0 RxE2[1].
6	RO	0	**Reserved**
5	RO	0	**Hot Plug Event Status** When a hot plug condition is detected in either one of the root ports (RP0 ~ RP3), this register will be set to 1. 0: No Hot Plug event was recorded in either one of the root ports. 1: At least one Hot Plug event is received at the PCIe root ports. The chip can wake up the system through appropriate programming at the PMU related logic, D17F0 RxE2[2].
4:0	RO	0	**Reserved**

Offset Address: A2h (D0F5)
ACPI Base Address – Bit[15:8] **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**ACPI Base Address - Bits [15:8]** The base address of the ACPI I/O space is defined at D17F0, Rx88[15:7]. However, for easy implementation of the "HOLD_STPGNT" feature as described at RxA3[0]. These registers are provided to let the NM block to decode the I/O cycles to put the system to STR (Suspend to RAM) or STD (Suspend to Disk) modes. Please refer to the register description at RxA3[0]. Software must copy the contents of D17F0 Rx88[15:8] to these registers before RxA3[0] is set to 1 to enable the "HOLD_STPGNT" feature.

Offset Address: A3h (D0F5)
STPGNT Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**ACPI Base Address – Bit[7]** This bit is the base address bit[7] of the ACPI I/O space. This bit concatenated with RxA2 to form a base address [15:7] for the ACPI I/O space. Please refer to the description at RxA2.
6:1	RW	0	**Reserved**
0	RW	0	**Holding STPGNT for Entering Sleeping Mode** This chip goes to sleep mode when CPU issues IO commands directed to offset 05h (Note1) in the ACPI space. The base address of the ACPI I/O space is defined at D17F0 Rx88[15:7]. However, for easy implementation, this chip uses the registers at{RxA2[7:0], Bit-7} of this function as the base address for decoding of accessing to ACPI I/O space. When this bit is enabled, the chip will monitor the CPU IO commands which intends to put the system to STR (Suspend to RAM) or STD (Suspend to Disk) modes. And once it decodes the commands (compared the address[15:7] against the registers programmed at {RxA2[7:0], Bit-7}, and data to be either 24h or 28h), the chip will do the "HOLD_STPGNT" as described following: (1) The controller starts to monitor the next STPGNT cycle from the CPU. (2) Once the controller detect the coming in of the STPGNT cycle, it won't issue to the SB block as usual (Note2). Instead, it will trigger MSGC (PCIe message controller) to issue PCIe message PME_Turn_Off to PCIe devices (connected to RP0~RP3). (3) The controller waits for the acknowledge PME_To_Ack returned from all the devices to issue the STPGNT cycle which is received in step 1 to SM's PMU unit. 0: Disabled. STPGNT cycles from CPU will be forwarded to SM. 1: Enabled. The chip will do "HOLD_STPGNT" to make sure all the PCIe devices are also ready to get into sleep mode (no clocks, or even no power). However, ONLY one STPGNT cycle is treated as those described at (1) ~ (3). This chip will need to detect another ACPI sleep enable command (STR or STD) to start another "HOLD_STPGNT" process .

Notes:
1. Offset 05h at ACPI space: Bit-5 is the enable bit to go to sleep mode with definition at bits [4:2].
2. Normally (When bit-0 = 0), STPGNT cycle will be forwarded to SB block to indicate an acknowledge from CPU in return of the requests (STPCLK#) to stop the CPU's clock which issued by SM's PMU unit.

Offset Address: A4-AFh (D0F5) – Reserved

Offset Address: B0h (D0F5)
PCIe Root Port Configuration **Default Value: n8h**

Bit	Attribute	Default	Description
7	RWS	dip	**PCIe Lane[3:0] Function Select** PCIe Lane3~Lane0 (PEXTX[3:0]P/VCC) can be used for internal graphic controller to output its display data. The PCIe compatible digital display interface DisplayPort is used to be connected to. 0: PCIe Lane3~Lane0 is used as the lanes for Root Port 0. 1: PCIe Lane3~Lane0 is used as the transmit data for DisplayPort interface. This bit is set to the strapping value of ball C4PSTOP# during the hardware reset: L: This bit will be 0. H: This bit will be 1.
6:4	RO	0	**Reserved**
3	RWS	1b	**Lane Width for Root Port 1** This register bit is to configure the lane width for the root port1 (RP1). 0: 2 lanes, PEXTX[9:8]P/VCC, and PEXRX[9:8]P/VCC are used for the RP1. RP2 is disabled. 1: 1 lanes, PEXTX8P/VCC, PEXRX8P/VCC will be used for RP1. PEXTX9P/VCC, PEXRX9P/VCC will be used for RP2.
2:0	RO	0	**Reserved**

Offset Address: B1-EFh (D0F5) – Reserved

Offset Address: F0h (D0F5)
PMU Control **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**Triggering Sending PME_TURN_OFF Messages** When this bit is programmed to 1, this chip will send PM_TURN_OFF messages to all the endpoints devices (connected to RP0~RP3) to let them know that the system is going to put all the PCIe Link of all devices in L2_L3_Ready state and to remove clocks and power on the devices. This bit has to be programmed to 0 before it can issue another PME_TURN_OFF message (writing 1) again. 0: Disabled. 1: Enabled.
6:2	RW	0	**Reserved**
1	RW	1b	**Reserved**
0	RW	0	**Reserved** This bit should be always set to 0.

Offset Address: F1h (D0F5)

PCIe Devices Register Space **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	1b	**Existence of PCI D3F3** PCI D3F3 (Device 3 Function 3) on the bus 0 for the system constructed by this chip is a PCIe Root Port (RP). This bit is to control the accessibility of its PCI register space. 0: D3F3 is absent, PCI configuration read to D3F3 will always get FFFF_FFFFh back. 1: D3F3 is existed, PCI configuration read to D3F3 will get the register value of RP3 back.
2	RW	1b	**Existence of PCI D3F2** PCI D3F2 (Device 3 Function 2) on the bus 0 for the system constructed by this chip is a PCIe Root Port (RP). This bit is to control the accessibility of its PCI register space. 0: D3F2 is absent, PCI configuration read to D3F2 will always get FFFF_FFFFh back. 1: D3F2 is existed, PCI configuration read to D3F2 will get the register value of RP2 back.
1	RW	1b	**Existence of PCI D3F1** PCI D3F1 (Device 3 Function 1) on the bus 0 for the system constructed by this chip is a PCIe Root Port (RP). This bit is to control the accessibility of its PCI register space. 0: D3F1 is absent, PCI configuration read to D3F1 will always get FFFF_FFFFh back. 1: D3F1 is existed, PCI configuration read to D3F1 will get the register value of RP1 back.
0	RW	1b	**Existence of PCI D3F0** PCI D3F0 (Device 3 Function 0) on the bus 0 for the system constructed by this chip is a PCIe Root Port (RP). This bit is to control the accessibility of its PCI register space. 0: D3F0 is absent, PCI configuration read to D3F0 will always get FFFF_FFFFh back. 1: D3F0 is existed, PCI configuration read to D3F0 will get the register value of RP0 back.

Offset Address: F2-FFh (D0F5) – Reserved

DEVICE 0 FUNCTION 6 (D0F6): SCRATCH REGISTERS

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 40 below.

Device 0 Function 6 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 6. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	**110**	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

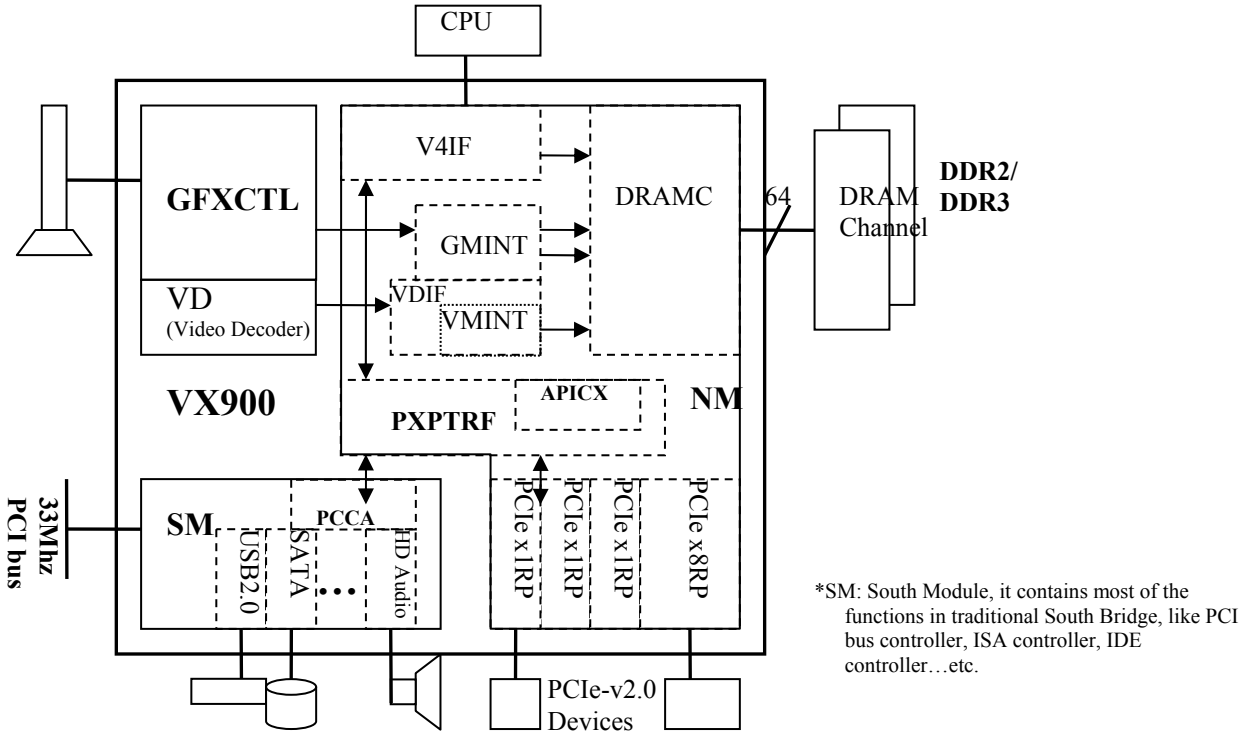


Figure 40. System Block Diagram for D0F6

The registers in this function are scratch registers for chip development. A software programming view for this register space D0F6 is as shown in the shaded block in Figure 41 below.

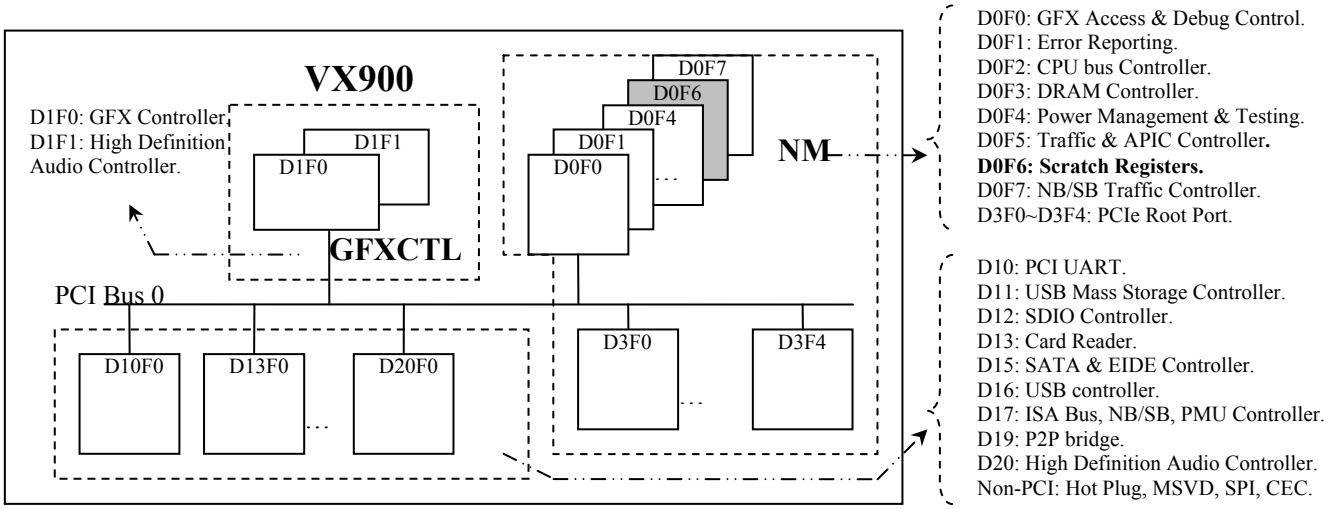


Figure 41. Register Level Block Diagram for D0F6

Header Registers (00–3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F6)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F6)

Device ID **Default Value: 6410h**

Bit	Attribute	Default	Description
15:0	RO	6410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F6)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RO	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F6)

PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RO	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RO	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	01b	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus.
8	RO	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F6)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** These bits are PCI header registers. They are the revision ID of this function.

Offset Address: 0B-09h (D0F6)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F6)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F6)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F6)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value of these bits are 80h. It indicates this is a multi-function device.

Offset Address: 0Fh (D0F6)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F6)

Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D0F6)

Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 1B-18h (D0F6)

Base Address Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F6)

Base Address Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 3** This function does not claim base address.

Offset Address: 23-20h (D0F6)

Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 4** This function does not claim base address.

Offset Address: 27-24h (D0F6)

Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 5** This function does not claim base address.

Offset Address: 2B-28h (D0F6)
CardBus CIS Pointer **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F6)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F6)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F6) - Reserved

Offset Address: 34h (D0F6)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F6) – Reserved

Offset Address: 3D-3Ch (D0F6)
Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F6)
Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

BIOS Scratch Registers (40-FFh)

Offset Address: 43-40h (D0F6)
BIOS Scratch Register 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 0** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 47-44h (D0F6)
BIOS Scratch Register 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 1** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 4B-48h (D0F6)
BIOS Scratch Register 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 2** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 4F-4Ch (D0F6)
BIOS Scratch Register 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 3** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 53-50h (D0F6)
BIOS Scratch Register 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 4** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 57-54h (D0F6)
BIOS Scratch Register 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 5** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 5B-58h (D0F6)
BIOS Scratch Register 6 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 6** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 5F-5Ch (D0F6)
BIOS Scratch Register 7 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 7** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 63-60h (D0F6)
BIOS Scratch Register 8 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 8** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 67-64h (D0F6)
BIOS Scratch Register 9 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 9** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 6B-68h (D0F6)
BIOS Scratch Register 10 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 10** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 6F-6Ch (D0F6)
BIOS Scratch Register 11 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 11** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 73-70h (D0F6)
BIOS Scratch Register 12 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 12** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 77-74h (D0F6)
BIOS Scratch Register 13 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 13** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 7B-78h (D0F6)
BIOS Scratch Register 14 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 14** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 7F-7Ch (D0F6)
BIOS Scratch Register 15 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RWS	0	**BIOS Scratch Register 15** These 32 bits register space is provided for temporary storage for BIOS or system software to work with.

Offset Address: 80-FFh (D0F6) – Reserved

DEVICE 0 FUNCTION 7 (D0F7): NORTH-SOUTH MODULE INTERFACE CONTROL

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 42 below.

Device 0 Function 7 is a Host Bridge. All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 7. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0000	111	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

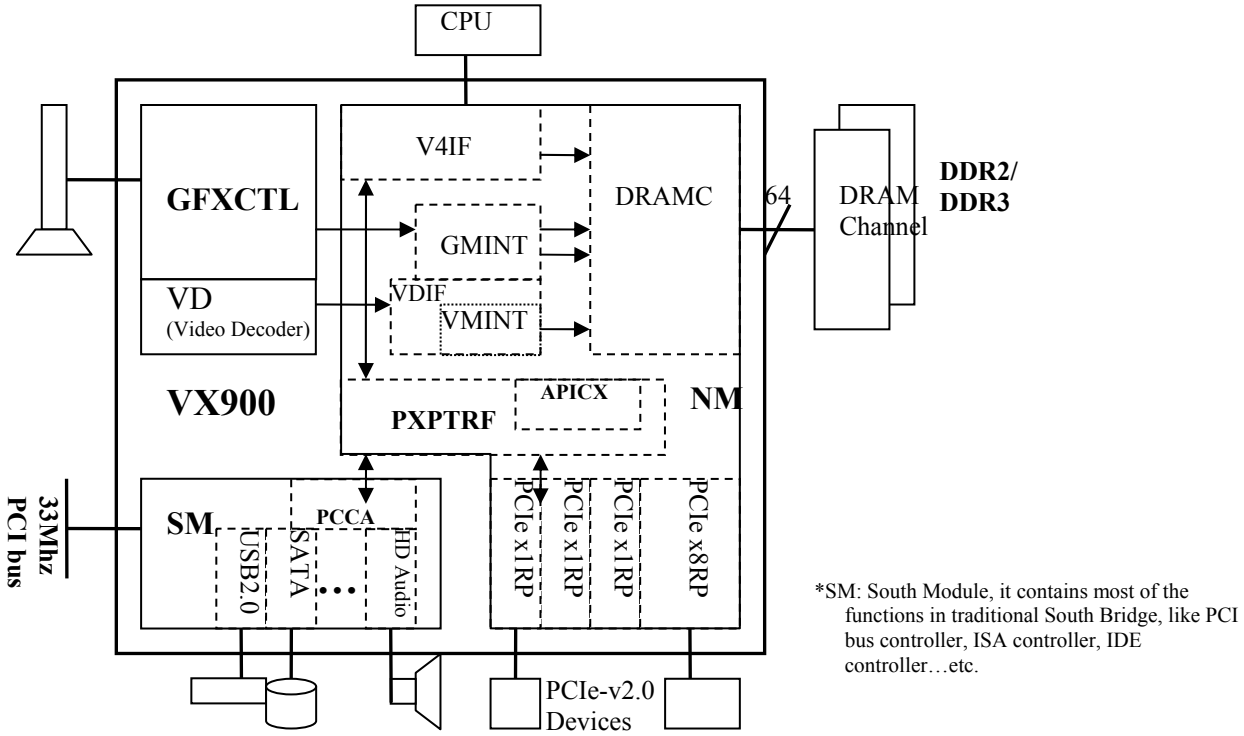


Figure 42. System Block Diagram for D0F7

The registers in this function are miscellaneous functions for traffic controls in between NM and SM. A software programming view for this register space D0F7 is as shown in the shaded block in Figure 43 below.

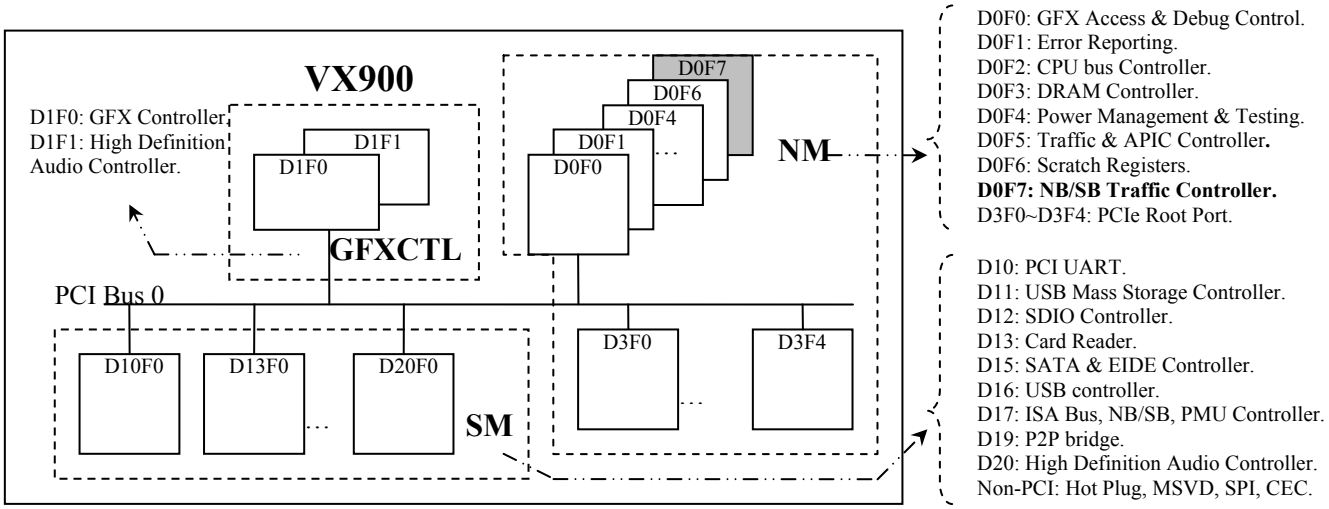


Figure 43. Register Level Block Diagram for D0F7

Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D0F7)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D0F7)

Device ID **Default Value: 7410h**

Bit	Attribute	Default	Description
15:0	RO	7410h	**Device ID** It is to identify this function.

Offset Address: 05-04h (D0F7)

PCI Command **Default Value: 0006h**

The bit values of this register are fixed and they do not affect any behavior on the PCI bus. The behavior of the PCI bus is controlled by the PCI command registers on D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** It is used to enable the Fast back-to-back capability on the PCI bus for the PCI bus controller.
8	RO	0	**SERR# Enable** It is used to enable the SERR# driver which assert SERR# signal on the PCI bus.
7	RO	0	**Address / Data Stepping** It is used to enable the address/data stepping for PCI bus controller to generate cycles on the PCI bus.
6	RO	0	**Parity Error Response** It is used to tell the PCI bus controller to perform the parity check on the PCI bus or not.
5	RO	0	**VGA Palette Snooping** It controls how VGA compatible Graphic devices handle accesses to VGA palette registers. This bit is fixed at 0.
4	RO	0	**Memory Write and Invalidate** It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus.
3	RO	0	**Respond To Special Cycle** It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus.
2	RO	1b	**PCI Master Function** It is used to enable the PCI bus controller to issue cycles to devices on the PCI bus.
1	RO	1b	**Memory Space Access** It is used to enable the PCI bus controller to accept the memory cycles from devices on the PCI bus.
0	RO	0	**I/O Space Access** It is used to enable the PCI bus controller to accept the I/O cycles from devices on the PCI bus.

Offset Address: 07-06h (D0F7)

PCI Status **Default Value: 0200h**

The value of this register won't reflect what happened on the PCI bus. The status of the PCI bus is reported to the PCI Status Register at D17F7 (when D17F7Rx4F[6] = 0) or D19F0 (when D17F7Rx4F[6] = 1).

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** It is used to indicate a parity error had been detected by the PCI bus controller.
14	RO	0	**Signaled System Error (SERR# Asserted)** It is used to indicate the PCI bus controller had asserted the SERR#.
13	RO	0	**Received Master-Abort (Except Special Cycle)** It is used to indicate the PCI bus controller encountered a cycle termination by master abort for its transaction.
12	RO	0	**Received Target-Abort** It is used to indicate the PCI bus controller encountered a cycle termination by target abort for its transaction.
11	RO	0	**Target-Abort Assertion** It is used to indicate the PCI bus controller issued a target abort termination for the cycle targeted to it.
10:9	RO	01b	**DEVSEL# Timing** It is used to indicate the response latency for the timing of PCI signal DEVSEL#. 00: Fast. 01: Medium. 10: Slow. 11: Reserved. These bits won't affect the DEVSEL# timing on the PCI bus.
8	RO	0	**Master Data Parity Error** It is used to tell that PERR# on the PCI bus is asserted to indicate a possible parity error happened. Three cases: 1) As a target, the PCI bus controller asserted PERR# on a read cycle or observed the assertion of PERR# on a write cycle. 2) As a initiator, the PCI bus controller encountered error upon the cycle it initiated. 3) Parity Error Response bit at Rx04[6] is set.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** It is used to indicate the capability of accepting fast back-to-back cycles.
6	RO	0	**User Definable Features** It is reserved for user to define.
5	RO	0	**66 MHz Capable** It is used to indicate the capability of supporting 66Mhz for the PCI bus controller.
4	RO	0	**Support New Capability List** It indicates whether or not this device implements the pointer for a New Capabilities linked list at offset 34h. 0: New capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of new capabilities, i.e., New capability linked list is supported.
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F7)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** These bits are PCI header registers. They are the revision ID of this function.

Offset Address: 0B-09h (D0F7)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code** 060000h indicates this function is a host bridge.

Offset Address: 0Ch (D0F7)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words.

Offset Address: 0Dh (D0F7)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Time Slice for this Function as a Master on the PCI Bus** It indicates how many PCI clocks of duration the PCI controller as a master can own the PCI bus. The units is 8 PCI Clocks. They do not have any impact to the behaviors of this chip.

Offset Address: 0Eh (D0F7)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 00h is the header type for this host bridge. The value of these bits are 80h. It indicates this is a multi-function device.

Offset Address: 0Fh (D0F7)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D0F7)
Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D0F7)
Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 1B-18h (D0F7)
Base Address Registers 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 2** This function does not claim base address.

Offset Address: 1F-1Ch (D0F7)
Base Address Registers 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 3** This function does not claim base address.

Offset Address: 23-20h (D0F7)
Base Address Registers 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 4** This function does not claim base address.

Offset Address: 27-24h (D0F7)
Base Address Registers 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 5** This function does not claim base address.

Offset Address: 2B-28h (D0F7)
CardBus CIS Pointer **Default Value: 00000000h**

Bit	Attribute	Default	Description
31:0	RO	0	**CardBus CIS Pointer** This field is used to point to the Card Information Structure (CIS) for the CardBus Card. It is not supported by this function.

Offset Address: 2D-2Ch (D0F7)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID** They are used to uniquely identify the manufacturer of the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 2F-2Eh (D0F7)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID** They are used to uniquely identify the expansion board or subsystem where the PCI device resides. These write once registers can be written once and only once after the de-assertion of PCIRST#.

Offset Address: 30-33h (D0F7) – Reserved

Offset Address: 34h (D0F7)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip does not have any capability needed to specify.

Offset Address: 35-3Bh (D0F7) – Reserved

Offset Address: 3D-3Ch (D0F7)
Interrupt Line and Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Interrupt Pin** It tells which interrupt pin the device uses. It is not applicable to this function.
7:0	RO	0	**Interrupt Line** It is used to communicate interrupt line routing information. It is not applicable to this function.

Offset Address: 3F-3Eh (D0F7)
Minimum Grant and Maximum Latency **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Maximum Latency** It is used to specify how often the device needs to gain access to the PCI bus in units of 1/4 microsecond. It is not applicable to this function.
7:0	RO	0	**Minimum Grant** It is used to specify how long a burst period this device needs in units of 1/4 microsecond. It is not applicable to this function.

North-South Module Interface Control (40–6Fh)

Offset Address: 40h (D0F7)

Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:1	RW	0	**Number of STPGNT Cycles for Assertion of SLP#** Working with the transition of C-state machine of this chip going to C3/C4/C5 states, CPU issues STPGNT cycles to the chipset (upon seeing assertion of STPCLK#) to let chipset drive SLP# to get into sleep state. However, when this chip works with CPU having multiple CPU cores, there could be STPGNT cycles from each CPU core when power states transitioned inside the CPU. These bits control the number of STPGNT cycles seen by this chip before this chip asserts SLP# when C-state machine is transitioning to C3/C4/C5. 00: 1 STPGNT cycle. 01: 2 STPGNT cycles. 10: 3 STPGNT cycles. 11: 4 STPGNT cycles.
0	RW	0	**Reserved**

Offset Address: 41-56h (D0F7) – Reserved

Offset Address: 57h (D0F7)

DRAM Bank Ending Address **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	HwInit	**The Address Next to the Last Valid DRAM Address** These bits are read only. The chip will return the value of D0F3, Rx88 when a read is issued to this register. Please refer to the register description of D0F3, Rx88. They are used to identify the address next to the last physical memory. However, the information is not complete, the valid ending address of this chip is up to bit[33].

Offset Address: 58-6Fh (D0F7) – Reserved

Host-PCI Bridge Control (70-FFh)

Offset Address: 70-75h (D0F7) – Reserved

Offset Address: 76h (D0F7)

IO Port 22 Enable (NM) **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**IO Port 22 Enable (NM)** 0: CPU access to IO address 22 is passed onto the PCI bus 1: CPU access to IO address 22 is processed internally IO This bit should be set as same as D17F7 Rx76[7]. When this bit is enabled, PXPTRF (traffic controller) could block peer-to-peer downstream requests before arbiter being disabled to prevent deadlock (please refer to D0F5 Rx64[7]).
6:0	RW	0	**Reserved**

Offset Address: 77-FFh (D0F7) – Reserved

DEVICE 3 FUNCTION 0-3 (D3F0-3): PCI EXPRESS ROOT PORT 0-3 (PCI-TO-PCI VIRTUAL BRIDGE)

PCI Configuration Space

The VX900 Series integrates the functions of conventional chipset North Bridge, South Bridge and the Graphics Controller (GFXCTL) into one single chip. The traditional functions of North Bridge is included in the North Module (NM) of this chip; while the functions of traditional South Bridge, like PCI bus controller and ISA controller, are included in the South Module (SM) of this chip, as shown in Figure 44 below.

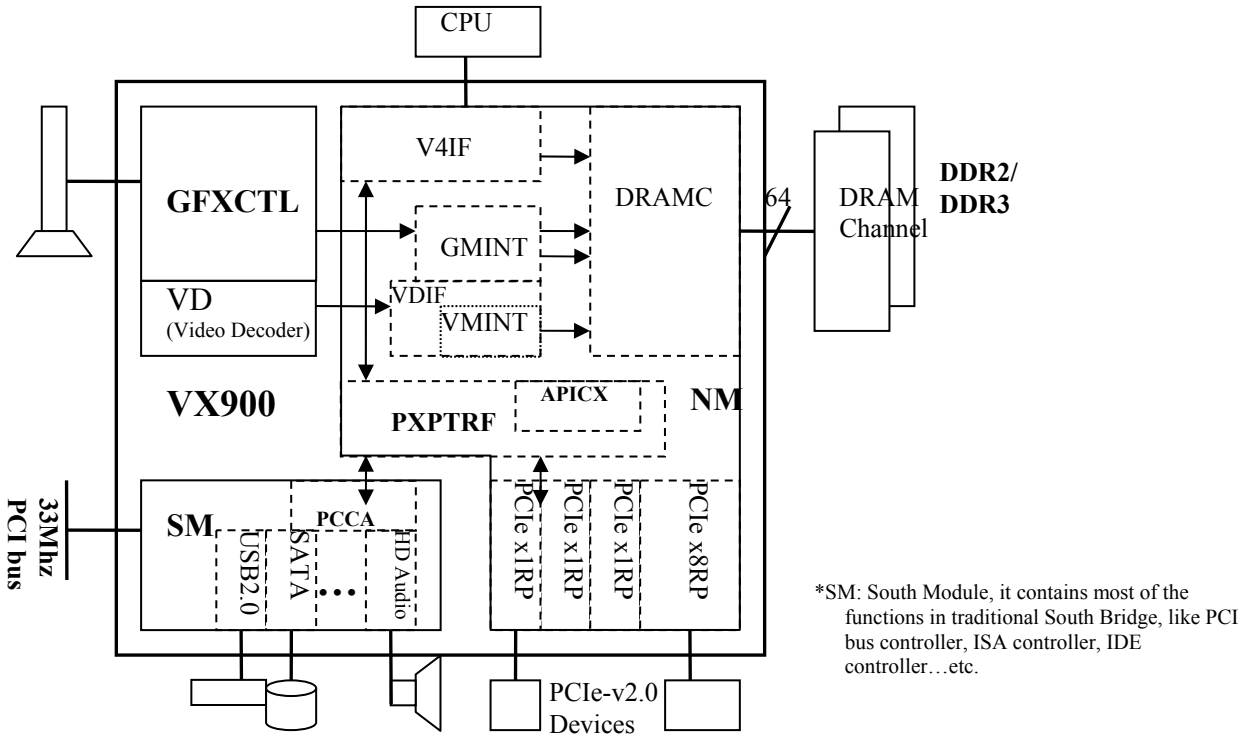


Figure 44. System Block Diagram for VX900 Series

The PCIe designs of this chip are 11 Lanes for at most 4 ports {8,1,1,and 1 lane(s) for Root Port (RP) 0, RP1, RP2, and RP3} with a configuration table as shown in Table 28 below. They operated at either 5GHz (for PCIe-v2.0) or 2.5GHz (for PCIe-v1.1).

Table 28. PCIe Lane Configuration of this chip

Lane configuration	RP0		RP1		RP2		RP3	
D0F5, RxB0[3] (ATMNCFG_PE1)	# of lanes	Pins used	# of lanes	Pins used	# of lanes	Pins used	# of lanes	Pins used
0	8	PEXTX[7:0]P/N, PEXRX[7:0]P/N	2	PEXTX[9:8]P/N, PEXRX[9:8]P/N	0	n/a	1	PEXTX10P/N, PEXRX10P/N
1			1	PEXTX8P/N, PEXRX8P/N	1	PEXTX9P/N, PEXRX9P/N		

Root port 0 (RP0) is an 8-Lane root port for high end graphics interface, which can be operated at x8, x4, x2 or x1 lane width. RP1 ~ RP3 are three 1-Lane root port for peripheral devices, which can be configured as 3 x 1-Lane or 1 x 2-Lane + 1 x 1-Lane as shown in Table 28 above.

This document contains PCI express registers for Device3 Function 0, 1, 2, and 3. They are control registers for those PCI Express root ports (RP0 ~ RP3) described above, with D3F0 for RP0, D3F1 for RP1, D3F2 for RP2, and D3F3 for RP3. Noted that most of the registers for RP0 are also existed and having the same functions for RP1, RP2, and RP3. In the document, unless there are significant differences (in which case, register descriptions for D3F1~D3F3 will be provided at the same register location), only descriptions for registers of D3F0 are provided. But, we will have to assume the same register existed for D3F1, D3F2, and D3F3.

All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 0-3. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0011	000 ~ 011	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

The above convention PCI configuration register accessing method can access registers with offset from 00h to FFh (register number RX is defined by 8 bits). For these PCIe root port controls, there are registers existed over FFh. And these registers can be accessed by using either **Extended Configuration Addressing Mode** or **Memory Mapped Configuration Access Mode**.

Extended Configuration Addressing Mode:

With D0F5, Rx60[1:0] programmed to 10b, the programming method is still using I/O write CF8 and I/O write/read CFC. Only that the data format presented above for the I/O write CF8h is then redefined as:

Bit-31	Bits [30:28]	Bits [27:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Extended Register Address bit[11:8]	Bus Number	Device Number	Function Number	Register Number	0	0
1	000	Rx value bit[11:8]	0000_0000	0_0011	000 ~ 011	RX value [7:0] with bit[1:0] = 00b		

Memory Mapped Configuration Access Mode:

With D0F5, Rx60[1:0] programmed to 11b, the programming method is changed to use Memory read & Memory write command with address defined below. The address bit[35:28] is the Memory Mapped configuration address defined at D0F5, Rx61[7:0]

Bits [35:28]	Bits [27:20]	Bits [19:15]	Bits [14:12]	Bit[11:8]	Bits [7: 2]	Bit-1	Bit-0
Memory Mapped Configuration Address [35:28]	Bus Number	Device Number	Function Number	Extended Register Address Bit[11:8]	Register Number	0	0
D0F5, Rx61[7:0]	0000_0000	0_0011	000 ~ 011	RX value [11:0] with bit[1:0] = 00b			

Memory command with the address defined above can also be used to get access to all the registers in D3F0~D3F3.

A software programming view for the register space D3F0~D3F3 is as shown in the shaded block in Figure 45 below.

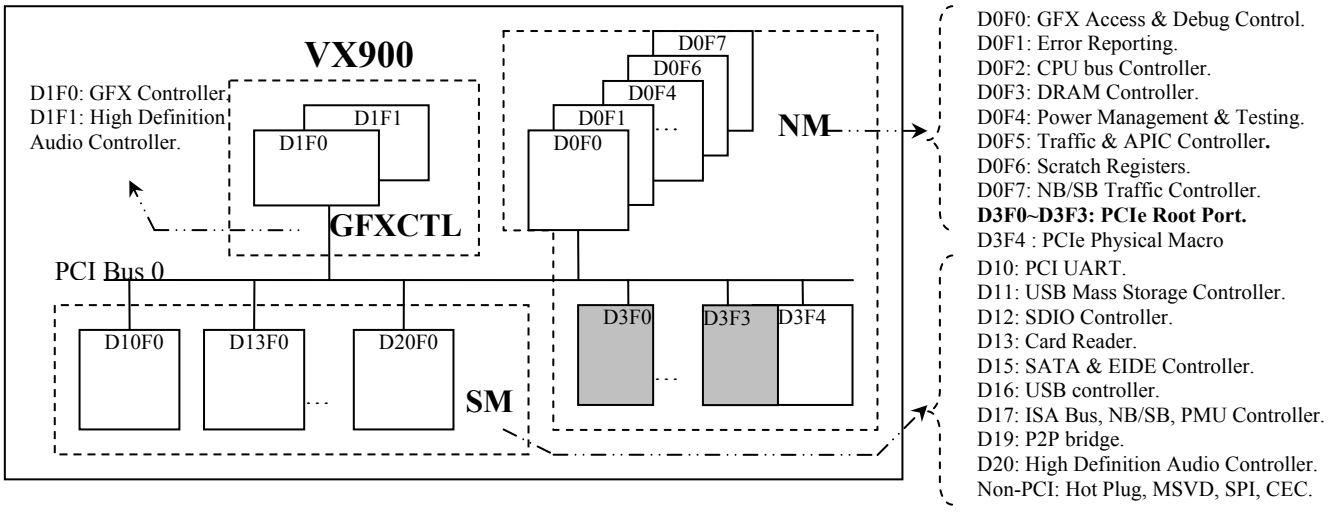


Figure 45. Register Level Block Diagram for D3F0~D3F3

Header Registers (00-3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D3F0-3)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID** It is to identify the manufacturer of this device. 1106h is the ID Code for VIA Technologies.

Offset Address: 03-02h (D3F0-3)

Device ID (D3F0) **Default Value: A410h**

Bit	Attribute	Default	Description
15:0	RO	A410h	**Device ID** It is to identify this function (D3F0).

Device ID (D3F1) **Default Value: B410h**

Bit	Attribute	Default	Description
15:0	RO	B410h	**Device ID** It is to identify this function (D3F1).

Device ID (D3F2) **Default Value: C410h**

Bit	Attribute	Default	Description
15:0	RO	C410h	**Device ID** It is to identify this function (D3F2).

Device ID (D3F3) **Default Value: D410h**

Bit	Attribute	Default	Description
15:0	RO	D410h	**Device ID** It is to identify this function (D3F3).

Offset Address: 05-04h (D3F0-3)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** This bit controls the ability of a PCIe device to generate INTx interrupt Messages. When set, devices are prevented from generating INTx interrupt Messages. MSI and INTx message generated by downstream devices are not controlled by this bit. For this root port 0 (RP0), this bit controls the generation of the interrupts induced by events like link width changes, hot plugging, PME assertion & de-assertion, and some error messages (Fatal Error, Non-fatal Error, Correctable Error) regarding to the links. 0: Upon the happening of the events mentioned, RP0 will generate interrupt *. 1: Upon the happening of the events mentioned, RP0 will not generate interrupt. This interrupt is connected to the IRQ3 (please refer to Appendix A.1 of IRS of D0F5, it will be IRQ7 for RP1, IRQ11 for RP2, IRQ15 for RP3) of the APIC in North Bridge Module. Programming to that APIC to determine either normal interrupt or MSI being performed in the system.
9	RO	0	**Fast Back-to-Back Transaction Enable** This bit is a PCI header register. It is used to enable the Fast back-to-back feature on the PCI bus. This bit does not apply to PCI Express. It is reserved.
8	RW	0	**SERR# Enable** When this bit is enabled, the Fatal Error & Non-Fatal Error Messages sent by the devices connected to root port 0 (RP0) will be reported to Rx07[6]. 0: Disabled. 1: Enabled.
7	RO	0	**Address / Data Stepping** This is a PCI header register. It is used to enable the address/data stepping for PCI bus controller. This bit does not apply to PCI Express. It is reserved.
6	RW	0	**Parity Error Response** This bit is a PCI header register. It is used to tell the PCI bus controller to perform the parity check on the PCI bus. It is reserved. Programming 1 or 0 to this bit does not change the behavior of this chip.
5	RO	0	**VGA Palette Snooping** This is a PCI header register. It controls how VGA compatible Graphic device handle accesses to the VGA palette registers. This bit does not apply to PCI Express. It is reserved.
4	RO	0	**Memory Write and Invalidate** This is a PCI header register. It is used to enable the PCI bus controller to issue Memory Write Invalidate command on the PCI bus. This bit does not apply to PCI Express. It is reserved.
3	RO	0	**Response to Special Cycle** This is a PCI header register. It is used to enable the PCI bus controller to take actions once it sees a special cycle on the PCI bus. This bit does not apply to PCI Express. It is reserved.
2	RW	0	**Bus Master Enable** This bit controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. 0: Disabled. Root port 0 will return Unsupported Requests (UR) or Completion with UR completion for the posted or non-posted requests from the devices connected on the root port 0 (RP0). The upstream MSI messages are also ignored. 1: Enabled. Upstream requests will be proceeded normally.
1	RW	0	**Memory Space** This is a PCI header register. It is used to enable the PCI controller to accept memory cycles from devices on the PCI bus. This bit is used to control the downstream memory cycles targeted to devices connected to the root port 0 (RP0). 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** This is a PCI header register. It is used to enable the PCI controller to accept the I/O cycles from devices on the PCI bus. This bit is used to control the downstream I/O cycles targeted to devices connected to the root port 0 (RP0). 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 07-06h (D3F0-3)

Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This is a PCI header register. This bit reports the detection of an address or data parity error by the bridge on its primary interface. This chip never sets this bit, it is always 0.
14	RW1C	0	**Signaled System Error** This is a PCI header register. This bit reports the assertion of SERR# by the bridge on the primary interface. For the root port 0, this bit is set when the following conditions occurs. 1. A device connected to root port 0 (RP0) sent an ERR_FATAL or ERR_NONFATAL message. 2. Error reported from Training Sequence, CRC errors, or unexpected TLP received by this root port. This chip sets this bit to 1 when Rx04[8] is set to 1 and either one of the above two conditions is met. i.e. when Rx04[8] is 0, this bit is always 0.
13	RW1C	0	**Received Master Abort** This is a PCI header register. This bit reports the detection of a Master-Abort termination by the bridge, when it is the master of a transaction on the primary interface. This chip never sets this bit, it is always 0.
12	RW1C	0	**Received Target Abort** This is a PCI header register. This bit reports the detection of a Target-Abort termination by the bridge when it is the master of a transaction on the primary interface. This chip never sets this bit, it is always 0.
11	RW1C	0	**Signaled Target Abort** This is a PCI header register. This bit reports the signaling of a Target-Abort termination by the bridge, when it responds as the target of a transaction on the primary interface. This chip never sets this bit, it is always 0.
10:9	RO	0	**DEVSEL# Timing** These are PCI header registers. It is used to indicate the response latency for the timing of PCI signals DEVSEL# on the primary interface. These bits do not apply to this chip. They are reserved.
8	RW1C	0	**Master Data Parity Error** This is a PCI header register. This bit is used to report the detection of a parity error by the bridge when it is the master of the transaction This bit is set if the following three conditions are all met: 1. The bridge is the bus master of the transaction on the primary interface. 2. The bridge asserted PERR# (read transaction) or detected PERR# asserted (write transaction). 3. The Parity Error Response bit (Rx04[6]) is set. This chip does not have the physical PCI compatible primary interface for this PCIe root port. It is reserved for this chip.
7	RO	0	**Capability of Accepting Fast Back-to-back as a Target** This is a PCI header register. It is used to indicate the capability of the PCI bus controller. This bit does not apply to this chip. It is reserved.
6	RO	0	**User Definable Features** This is a PCI header register. It is reserved for user to define. This bit is fixed at 0 at all times.
5	RO	0	**66 MHz capable** This bit is a PCI header register. It is used to indicate the capability of supporting 66Mhz for the PCI bus controller. This bit does not apply to this chip. It is reserved.
4	RO	1b	**Capabilities List** This bit is a PCI header register. It indicates whether or not this function implements the pointer for a capability linked list started at offset 34h. 0: Capability linked list is not available. 1: The value read at offset 34h is a pointer in configuration space to a linked list of capabilities.
3	RO	0	**Interrupt Status** A 1 of this bit indicates an INTx message is pending internally. Root port 0 (RP0) generates interrupts when events like link width changes, hot plugging, PME assertion & de-assertion, and some error messages (Fatal Error, Non-fatal Error, Correctable Error Messages from device connected on the RP0) received. This bit will be set when the above events happened and the event source is not cleared yet. Note that if Rx04[10] (RINTDIS_PE0) is 1, this bit will always be 0.
2:0	RO	0	**Reserved**

Offset Address: 08h (D3F0-3)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code** These bits are PCI header registers. They are the revision ID of this function.

Offset Address: 0B-09h (D3F0-3)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code** 060400h indicates this function is a PCI-PCI bridge.

Offset Address: 0Ch (D3F0-3)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** It indicates the cache-line size in a cache-line transaction in units of double words. For this chip, this bit has no impact on the functionality. It is reserved.

Offset Address: 0Dh (D3F0-3)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Primary Latency Timer** It indicates how many PCI clocks of duration the PCI-PCI bridge controller as a master can own the PCI bus on the primary side. The units is 8 PCI clocks. They do not have any impact to the behaviors of this chip. They are reserved.

Offset Address: 0Eh (D3F0-3)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	81h	**Header Type Code** Bit 7 in this register is used to identify a multifunction device. If that bit is 0, the device is single function. If that bit is 1, the device has multiple functions. Bits 6 through 0 identify the layout of the second part of the predefined header. 01h is the header type for this PCI-PCI bridge. 81h indicates that this is a multiple function PCI-PCI bridge device. The PCI header space are Rx00~Rx3F conforms to the PCI type 1 configuration space header which is defined for PCI-PCI bridge.

Offset Address: 0Fh (D3F0-3)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support** Bit 7 = 0 indicates that this function does not support BIST. Writing a 1 to bit 6 will invoke the BIST operation. The value of 0h on bit[3:0] means the device has passed its test. Non-zero values on bit[3:0] means the device failed. This chip does not support BIST through these registers.

Offset Address: 13-10h (D3F0-3)
Base Address Registers 0 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 0** This function does not claim base address.

Offset Address: 17-14h (D3F0-3)
Base Address Registers 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Base Address - 1** This function does not claim base address.

Offset Address: 18h (D3F0-3)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number** This is the standard PCI header for PCI-PCI bridge. These bits are used to record the bus number of the PCI bus segment to which the primary interface of the bridge is connected. PCI Express root port is a PCI-PCI bridge, this chip needs primary bus number to configure the PCI bus structure on the bus tree behind the root port.

Offset Address: 19h (D3F0-3)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number** This is the standard PCI header for PCI-PCI bridge. These bits are used to record the bus number of the PCI bus segment to which the secondary interface of the bridge is connected. PCI Express root port is a PCI-PCI bridge, this chip needs secondary bus number to configure the PCI bus structure on the bus tree behind the root port.

Offset Address: 1Ah (D3F0-3)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number** This is the standard PCI header for PCI-PCI bridge. These bits are used to record the bus number of the highest numbered PCI bus segment which is behind the bridge. PCI Express root port is a PCI-PCI bridge, this chip needs this subordinate bus number to configure the PCI bus structure on the bus tree behind the root port.

Offset Address: 1Bh (D3F0-3)
Secondary Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Secondary Latency Timer** This is the standard PCI header for PCI-PCI bridge. It indicates how many PCI clocks of duration the PCI-PCI bridge controller as a master can own the PCI bus on the secondary side. The units is 8 PCI clocks. For PCI Express root port, they do not have any impact to the behaviors of this chip. They are reserved.

Offset Address: 1Ch (D3F0-3)

I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Base (AD[15:12])** This is the standard PCI header for PCI-PCI bridge. This bridge will forward the cycles from primary interface to secondary interface if the I/O address AD[15:12] is between these 4 bits and I/O limit (D3F0 Rx1D[7:4]), inclusively.
3:0	RO	0	**I/O Addressing Capability** This is the standard PCI header for PCI-PCI bridge. 0h means I/O addressing is 16-bit only, the controller may only decode the I/O cycle without the higher 16 bit address (AD[31:16]). 1h means I/O addressing is 32-bit and the controller will have to decode the I/O address with the high 16 bits (AD[31:16]) equaled to 0000h. 2h~Fh are reserved.

Offset Address: 1Dh (D3F0-3)

I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12])** This is the standard PCI header for PCI-PCI bridge. This bridge will forward the cycles from primary interface to secondary interface if the I/O address AD[15:12] is between I/O base (Rx1C[7:4]) and these 4 bits, inclusively.
3:0	RO	0	**I/O Addressing Capability** This is the standard PCI header for PCI-PCI bridge. 0h means I/O addressing is 16-bit only, the controller may only decode the I/O cycle without the higher 16 bit address (AD[31:16]). 1h means I/O addressing is 32-bit and the controller will have to decode the I/O address with the high 16 bits (AD[31:16]) equaled to 0000h. 2h~Fh are reserved.

Offset Address: 1F-1Eh (D3F0-3)

Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when a PCIe poisoned TLP is received on the root port, regardless the status of Rx04[6].
14	RW1C	0	**Received System Error** This bit is set when the device connected to this root port sends a ERR_FATAL or ERR_NONFATAL Message to the root port, and the SERR Enable bit in the control register (Rx04[8]) is 1. Note that when this bit is set, the Rx06[14] is also set.
13	RW1C	0	**Received Master Abort** This bit is set when the root port receives a Completion with Unsupported Request Completion status.
12	RW1C	0	**Received Target Abort** This bit is set when the root port receives a Completion with Completer Abort Completion status.
11	RO	0	**Signaled Target Abort** This bit is set when the root port completes a Request using Completer Abort Completion status. This chip will never complete a request with Completer Abort Completion status. It is always 0.
10:9	RO	0	**DEVSEL Timing** They do not apply to PCI Express. They are reserved.
8	RW1C	0	**Master Data Parity Error** This bit is set by the root port if the Parity Error Response bit for the Bridge Control (Rx3E[0]) is set and either one of the following two conditions occurs: 1. Root port receives a Completion marked poisoned for its previous requests. 2. Root port poisons a write Request.
7	RO	0	**Fast Back-to-Back Capable** This bit indicates whether or not the secondary interface of the bridge is capable of decoding the fast back-to-back transactions. It does not apply to PCI Express. It is reserved.
6	RO	0	**Reserved**
5	RO	0	**66Mhz Capable** This bit indicates whether or not the secondary interface of the bridge is capable of operating at 66Mhz. It does not apply to PCI Express. It is reserved.
4:0	RO	0	**Reserved**

Offset Address: 21-20h (D3F0-3)

Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base** The Memory Base and Memory Limit (Rx22~Rx23) registers are both required registers that define a memory mapped I/O address range which is used by this bridge (root port) to determine when to forward memory transactions from upstream side (CPU side) of the root port to the PCIe bus. These 12 bits registers mapped to the upper 12 bits of the 32-bit base address. When this chip decodes cycles from the upstream side, the lower 20 address bits of this 32 bit base address will be assumed all 0 and the lower address bits of the 32 bit limit address will be assumed all 1. Thus, a memory cycle with address[31:0] such that{RMIBS_PE0[31:20], 0_0000h} <= address[31:0] <= {RM1LM_PE0[31:20], F_FFFFh} will be forwarded to the device connected on this root port.
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D3F0-3)

Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Limit** Please refer to the register descriptions of Rx20[15:4]. These 12 bits registers mapped to the address bit[31:20] of the upper limit for this root port to decode cycles to forward to the device connected on this root port.
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D3F0-3)

Prefetchable Memory Base **Default Value: FFF1h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base** The Prefetchable Memory Base and Prefetchable Memory Limit (Rx26~Rx27) registers define a prefetchable memory address range which is used by the bridge (root port) to determine when to forward memory transactions from upstream side (CPU side) of the root port to the PCIe bus. This Prefetchable Memory base & limit is defined for 64-bit addressing. These 12 bits registers mapped to the bit[31:20] of the 64-bit base address. When this chip decodes cycles from the upstream side, the lower 20 address bits of this 64 bit base address will be assumed all 0 and the lower address bits of the 64 bit limit address will be assumed all 1. Thus, a memory cycle with address[63:0] such that {0000_000h, RM3BS_PE0[35:32] (Rx28[3:0]), RM2BS_PE0[31:20], 0_0000h} <= address[63:0] <= {0000_000h, RM3LM_PE0[35:32] (Rx2C[3:0]), RM2BS_PE[31:20], F_FFFFh} will be forwarded to the device connected on this root port. Note that this chip only supports addressing upto 16G, thus, upper addressing above bit[35] of the prefetchable memory base & limit should be fixed at 0.
3:1	RO	0	**Reserved**
0	RO	1b	**64 Bits Addressing for Prefetchable Memory Base** This bit reports the support of 64 bit addressing for the Prefetchable Memory Base at Rx24[15:4]. 0: The prefetchable memory base are 32 bits with bit[31:20] defined at Rx24[15:4]. 1: The prefetchable memory base are 64 bits. Besides the lower bit[31:20] defined at Rx24[15:4], the upper 32 bits bit[63:32] are at Rx28[31:0].

Offset Address: 27-26h (D3F0-3)

Prefetchable Memory Limit **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**Prefetchable Memory Limit** Please refer to the descriptions of Rx24[15:4]. These 12 bits registers mapped to the address bit[31:20] of the upper limit for this root port to decode cycles to forward to the device connected on this root port. Note that this chip supports 64 bit addressing for the prefetchable memory range. The register at Rx2C[31:0] mapped to the address bit[63:32] of the upper limit.
3:1	RO	0	**Reserved**
0	RO	1b	**64 Bits Addressing for Prefetchable Memory Limit** This bit reports the support of 64 bit addressing for the Prefetchable Memory Limit at Rx26[15:4]. 0: The prefetchable memory limit are 32 bits with bit[31:20] defined at Rx26[15:4]. 1: The prefetchable memory limit are 64 bits. Besides the lower bit[31:20] defined at Rx26[15:4], the upper 32 bits bit[63:32] are at Rx2c[31:0].

Offset Address: 2B-28h (D3F0-3)

Prefetchable Memory Base Upper 32 bits **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Prefetchable Memory Base Upper bit[63:36]** Please refer to register descriptions at Rx24[15:4]. These bits mapped to the upper address bit[63:36] of the Prefetchable Memory Base. Since the chip only supports system address bit up to bit[35], these bits should always be programmed as 0000_000h in order for the system to work normally.
3:0	RW	0	**Prefetchable Memory Base Upper bit[35:32]** Please refer to register descriptions at Rx24[15:4]. These bits mapped to the upper address bit[35:32] of the Prefetchable Memory Base. This chip supports system address up to bit[35].

Offset Address: 2F-2Ch (D3F0-3)

Prefetchable Memory Limit Upper 32 Bits (D3F0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Prefetchable Memory Limit Upper Bits [63:36]** Please refer to register descriptions at Rx24[15:4]. These bits mapped to the upper address bits [63:36] of the Prefetchable Memory limit. Since the chpi only supports system address bit up to bit[35], these bits are read only and are 0000_000h.
3:0	RW	0	**Prefetchable Memory Limit Upper Bits [35:32]** Please refer to register descriptions at Rx24[15:4]. These bits mapped to the upper address bits [35:32] of the Prefetchable Memory Limit. This chip supports system address up to bit[35].

Prefetchable Memory Upper Limit (D3F1-F3) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RW	0	**Prefetchable Memory Limit Upper Bits [63:36]** Please refer to register descriptions at Rx24[15:4]. These bits mapped to the upper address bits [63:36] of the Prefetchable Memory limit. Since the chpi only supports system address bit up to bit[35], these bits are read only and are 0000_000h.
3:0	RW	0	**Prefetchable Memory Limit Upper Bits[35:32]** Please refer to register descriptions at Rx24[15:4]. These bits mapped to the upper address bits [35:32] of the Prefetchable Memory Limit. This chip supports system address up to bit[35].

Offset Address: 31-30h (D3F0-3)

I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Base Upper 16 bits Address** These registers work with Rx1C[7:4] to be the upper 16 bits of the I/O Base address. Since Rx1C[3:0] is 0h which means the I/O Base is 16 bits addressing, these bits are reserved.

Offset Address: 33-32h (D3F0-3)

I/O Base Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Limit Upper 16 bits Address** These registers work with Rx1D[7:4] to be the upper 16 bits of the I/O Limit address. Since Rx1D[3:0] is 0h which means the I/O limit is 16 bits addressing, these bits are reserved.

Offset Address: 34h (D3F0-3)

Capability Pointer **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability List Pointer** It indicates an offset address from the start of the configuration space. This pointer pointed to a linked list of new capabilities implemented by this device. A 0 indicates the end of the list. This function of this chip had the following capabilities started at Rx40, thus it is read as 40h. Capability Pointer link list: Rx40 (PCI Express capability) → RxA0 (PCI Power Management capability) → RxB0 (MSI capability) → RxE0 (Subsystem ID and Subsystem Vendor ID Capability) → NULL

Offset Address: 35-3Bh (D3F0-3) – Reserved

Offset Address: 3Ch (D3F0-3)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line** This register is used to communicate interrupt line routing information between initialization code and the device driver. 00h: IRQ0 01h: IRQ1 02h: IRQ2 03h: IRQ3 04h: IRQ4 05h: IRQ5 … 0Eh: IRQ14 0Fh: IRQ15 10h ~ FEh : Reserved FFh: No interrupt line is used.

Offset Address: 3Dh (D3F0-3)

Interrupt Pin (D3F0) **Default Value: 01h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	001b	**Interrupt Pin** This register adheres to the definition in the PCI Local Bus Specification. This Interrupt Pin register is used to indicate which interrupt pin the bridge uses. 000b: No interrupt pin is used. 001b: INTA#. 010b: INTB#. 011b: INTC#. 100b: INTD#. 101b ~ 111b: Reserved. This register is needed when the function connected to the PCI bus where four Interrupt Pins (INTA#, INTB#, INTC#, INTD#) are defined. This root port (RP0) connects the internal interrupt to IRQ3 of the APIC in the North Bridge module (APICX), please refer to Appendix A of IRS for D0F5 for more details.

Interrupt Pin (D3F1) **Default Value: 02h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	010b	**Interrupt Pin** Please refer to the Rx3D of D3F0 above. Only that the root port (RP1) connects the internal interrupt to IRQ7 of the APICX.

Interrupt Pin (D3F2) **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	011b	**Interrupt Pin** Please refer to the Rx3D of D3F0 above. Only that the root port (RP2) connects the internal interrupt to IRQ11 of the APICX.

Interrupt Pin (D3F3) **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	100b	**Interrupt Pin** Please refer to the Rx3D of D3F0 above. Only that the root port (RP3) connects the internal interrupt to IRQ15 of the APICX.

Offset Address: 3F-3Eh (D3F0-3)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11	RO	0	**Discard Timer SERR# Enable** When set to 1, this bit enables the bridge to assert SERR# on the primary interface when either the Primary Discard Timer or Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue in the bridge. This bit does not apply to this chip, it is reserved.
10	RO	0	**Discard Timer Status** This bit is set to 1 when either the Primary Discard Timer or Secondary Discard Timer expires and a Delayed Completion is discarded from a queue in the bridge. This bit does not apply to this chip, it is reserved.
9	RO	0	**Secondary Discard Timer** This bit selects the number of PCI clocks that the bridge will wait for a master on the secondary interface to repeat a Delayed Transaction request. 0: The Secondary Discard Timer counts 2^{15} PCI clock cycles. 1: The Secondary Discard Timer counts 2^{10} PCI clock cycles. This bit does not apply to this chip, it is reserved.
8	RO	0	**Primary Discard Timer** This bit selects the number of PCI clocks that the bridge will wait for a master on the primary interface to repeat a Delayed Transaction request. 0: The Primary Discard Timer counts 2^{15} PCI clock cycles. 1: The Primary Discard Timer counts 2^{10} PCI clock cycles. This bit does not apply to this chip, it is reserved.
7	RO	0	**Fast Back-to-Back Enable** This bit controls ability of the bridge to generate fast back-to-back transactions to different devices on the secondary interface. 0: Disabled. 1: Enabled. This bit does not apply to this chip, it is reserved.
6	RW	0	**Secondary Bus Reset** Writing this bit to 1 will reset the PCI Express bus on the root port. This bit must be written to 0 before another reset can be issued. The minimum interval between writing 1 and writing 0 to this bit is 2 ms. 0: The PCI Express bus will go to the Detect state to start a PCIe training sequence to begin the connection of the root port and the device. 1: The PCI Express bus will go to Recovery state and stay at hot reset state. During the hot reset state, the TX lanes (PEXTX[7:0]P/N for RP0, PEXTX[8]P/N for RP1, PEXTX[9]P/N for RP2, and PEXTX[10]P/N for RP3) will be in electrical idle condition.
5	RO	0	**Master Abort Mode** This bit controls the behavior of a bridge when a Master-Abort termination occurs on either interface while the bridge is the master of the transaction. This bit does not apply to this chip, it is reserved.
4	RW	0	**Base VGA 16 bits Decode** This bit determines the address width of the VGA compatible I/O and memory address which are described at Rx3E[3]. 0: When Rx3E[3] is 1, all downstream cycles with VGA alias range will be also forwarded to the PCIe bus. i.e. I/O address bit[15:10] and Memory address bit[31:20] won't be decoded. 1: When Rx3E[3] is 1, this chip only forward cycles with base VGA range, i.e. I/O address bit[15:10] = 000000b and Memory address bit[31:20]=000h, to the PCIe bus. Cycles with alias range, i.e., I/O address bit[15:10] != 000000b, Memory address bit[31:20] !=000h, will be forwarded to SB module.
3	RW	0	**VGA Compatible I/O and Memory Address Range** VGA I/O cycles are I/O with addresses 3B0-3BBh and 3C0-3DFh. VGA memory cycles are memory with addresses A0000-BFFFFh. This bit controls the destination of those downstream cycles with those VGA I/O and memory addresses. 0: Do not forward VGA compatible memory and I/O from primary side to secondary side. Those downstream cycles with VGA I/O and memory addresses mentioned will be forwarded to SB module. 1: Forward VGA compatible memory and I/O to the downstream side of this root port.
2	RW	0	**Block/Forward ISA I/O Cycles** This bit defined the I/O cycles type for those I/O cycles being forwarded to the downstream side of this root port. 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit. 1: Do not forward ISA I/Os that are in the top 768 bytes of each 1K byte block address range. i.e. only lower 256 bytes addressing will be forwarded to the downstream side of this root port, upper 768 bytes within the 1K will be forwarded to SB block even though the I/O address is claimed by the I/O base & I/O limit defined at Rx1C~Rx1D.
1	RW	0	**SERR Enable** This bit controls the forwarding of secondary interface SERR# assertions to the primary interface. The bridge will assert SERR# on the primary interface when 1) SERR# is asserted on the secondary interface 2) This bit is set. 3) The SERR# enable bit at Rx04[8] is set. This bit in this chip implemented as a mask for those correctable messages, non-fatal error messages, and fatal error messages sent by the device connected to this root port. 0: Disabled, messages mentioned will be blocked, i.e. there won't be error reporting. 1: Enabled, the fatal & non-fatal error will be reported to Rx1E[14] when Rx04[8] is enabled. The correctable error will be reported to Rx130[0], non-fatal error will be reported to Rx130[5], and fatal error will be reported to Rx130[6]. Regarding to the details of the error reporting, please refer to appendix A, figure A.1

0	RW	0	**Parity Error Response Enable** This bit determines if the Rx1E[8] can be set or not when there is either the root port received a completion masked as poisoned or the root port poisoned a write request. 0: Ignore the response to poisoned TLPs, i.e. Rx1E[8] won't be set. 1: Enable the response to poisoned TLPs, i.e. Rx1E[8] will be set if there is poisoned TLP.

PCI Express Capability Registers (40-9Fh)

PCI Express capability registers for this root port had the following structure started from Rx40.

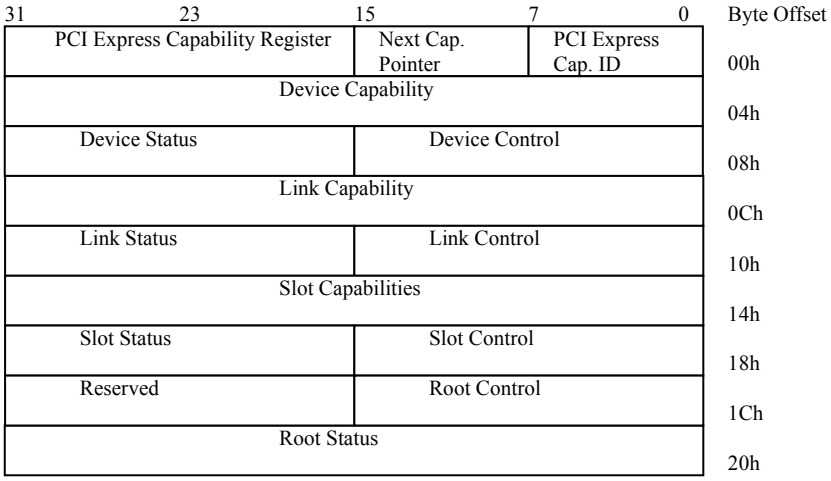


Figure 3. PCI Express Capability Structure

Offset Address: 41-40h (D3F0-3)

PCI Express List **Default Value: A010h**

Bit	Attribute	Default	Description
15:8	RO	A0h	**Next Capability Pointer** This 8 bits pointer pointed to the next capability this function had. Next capability is resided started from RxA0h.
7:0	RO	10h	**Capability ID** This byte is read as 10h indicating it is a PCI Express Capability structure.

Offset Address: 43-42h (D3F0-3)

PCI Express Capabilities **Default Value: 0n42h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**TCS Routing Supported** This bit is the support bit to support the TCS (Trusted Configuration Space). When this bit is 1, trusted configuration cycles (downstream MMIO cycles with specific address defined by the chipset) from the CPU will be routed to root port 0 (RP0). RP0 will translate that cycle to trusted configuration command on the PCIe bus to do trusted configuration on the device connected to RP0. This chip does not support this TCS routing capability.
13:9	RO	0	**Interrupt Message Number** This register indicates which MSI vector is used for the interrupt message generated when any of the status bits in either the slot status register or the root port status register of this capability structure is set. For example, the Multiple Message Enable bit in the MSI capability register (RxB0[22:20]) is set to 010b; It means there are 4 MSI messages (vectors) are allocated for this function. And if the bits here are set to 02h, it means the changes of the PCIe slot or root port status bits of this root port will trigger the third MSI messages (vectors). And if the Multiple Message Enable bit in the MSI capability register is 0h, it means this function had only one MSI message, thus, this bit must be 0 to indicate that message 0 is used for the MSI. This bit must always be 0 because this function had only one MSI message.
8	RO	1b	**Slot Implemented** This bit when set (to 1) indicates that the PCI Express Link associated with this port is connected to a slot (as compared to being connected to an integrated component or being disabled).
7:4	RO	0100b	**Device / Port Type** These bits indicates the type of PCI Express Logic device. 0100b: Root Port of PCI Express Root Complex.
3:0	RO	2h	**Capability Version** These bits indicates PcI-SIG defined PCI Express capability structure version number. 1h: Compliant to PCIe 1.0a and PCIe 1.1. 2h: Compliant to PCIe 2.0.

Offset Address: 47-44h (D3F0-3)

Device Capabilities **Default Value: 0000 8001h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28	RO	0	**Function Level Reset Capability** A value of 1 indicates this function supports the optional Function Level Reset (FLR) mechanism. This field applies to Endpoints only. It is reserved for this root port.
27:26	RO	00b	**Captured Slot Power Limit Scale** This field specifies the scale used for the Slot Power Limit Value (Rx44[25:18]), Range of Values: 00: 1.0x. 01: 0.1x. 10: 0.01x. 11: 0.001x. Upon receiving the Set_Slot_Power_Limit Message from the upper link, this field is set as the value specified in the message or is hardwired to 00b. This bit is for upstream port only, it is reserved and always read as 00b for this root port.
25:18	RO	0	**Captured Slot Power Limit Value** In combination with the Slot Power Limit Scale value (Rx44[27:26]), this field specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field (Rx44[27:26]). Upon receiving the Set_Slot_Power_Limit Message from the upper link, this field is set as the value specified in the message or is hardwired to 00h. This bit is for upstream port only, it is reserved and always read as 00h for this root port.
17:16	RO	0	**Reserved**
15	RO	1b	**Role-Based Error Reporting** When set to 1, this bit indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. The Role-based error reporting supporting in this chip is implemented such that some uncorrectable errors can be reported as correctable errors. Please refer to register descriptions at Rx104, Rx110[13], the Advisory Non-Fatal error status, and Rx130, the root error status. 0: Role-based error reporting is not supported. 1: Role-based error reporting is supported.
14	RO	0	**Power Indicator Present** When set to 1, this bit indicates that a Power Indicator is implemented on the adapter and is electrically controlled by the component on the adapter using the Power_Indicator_On, Power_Indicator_Blink, and Power_Indicator_Off Messages. It is reserved for root port.

13	RO	0	**Attention Indicator Present** When set to 1, this bit indicates that an Attention Indicator is implemented on the adapter and is electrically controlled by the component on the adapter using the Attention_Indicator_On, Attnetion_Indicator_Blink, and Attention_indicator_Off Messages. It is reserved for root port.
12	RO	0	**Attention Button Present** When set to 1, this bit indicates that an Attention Button is implemented on adapter and is electrically controlled by the component on the adapter. Attention Button press events are reported using the Attention_Button_Pressed Message. It is reserved for root port.
11:9	RO	000b	**Endpoint L1 Acceptable Latency** This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. 000: 1us. 001: 2us. 010: 4us. 011: 8us. 100: 16us 101: 32us. 110: 64us 111: no limit. It is reserved for Root Port.
8:6	RO	0	**Endpoint L0s Acceptable Latency** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition for L0s state to L0 State. 000: 64ns. 001: 128ns. 010: 256ns. 011: 512ns. 100: 1024ns. 101: 2us. 110: 4us. 111: no limit. It is reserved for Root Port.
5	RO	0	**Extended Tag Field Supported** This bit indicates the maximum supported size of the Tag field as a Requester. 0: 5-bit Tag field is supported for this root port. 1: 8-bit Tag field is supported for this root port. *This root port is able to support 8-bit Tag field.
4:3	RO	0	**Phantom Functions Supported** This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers (called Phantom Functions) with the Tag identifier. This field indicates the number of most significant bits of the function number portion of Requester ID that are logically combined with the Tag identifier. 00: Function number bit is not used for Phantom Functions. i.e. the Tag field of the requester remain at 8 bits. 01: First MSB of function number in Requester ID is used for Phantom Functions. i.e. MSB bit can be combined with the transaction Tag to form a 9 bits Tag to track the outstanding transactions. 10: First 2 MSB of function number in Requester ID are used for Phantom Functions. i.e. 2 MSB bits can be combined with the transaction Tag to form a 10 bits Tag to track the outstanding transactions. 11: All three bits of function number in Requester ID are used for Phantom Functions. i.e. All 3 function bits can be combined with the transaction Tag to form a 11 bits Tag to track the outstanding transactions. This chip does not support the Phantom Functions.
2:0	RO	001b	**Max Payload Size Supported** This field indicates the maximum payload size that this root port can support for the upstream write requests. 000: 128 bytes (16 QW). 001: 256 bytes (32 QW). 010: 512 bytes (64 QW). 011: 1024 bytes (128 QW). 100: 2048 bytes (256 QW). 101: 4096 bytes (512 QW). 110, 111: Reserved.

Offset Address: 49-48h (D3F0-3)

Device Control **Default Value: 0810h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	0	**Max Read Request Size** This field sets the maximum Read Request size for this root port as a Requestor (for a downstream cycle). 000: 128 bytes (16 QW). 001: 256 bytes (32 QW). 010: 512 bytes (64 QW). 011: 1024 bytes (128 QW). 100: 2048 bytes (256 QW). 101: 4096 bytes (512 QW). 110, 111: Reserved.
11	RW	1b	**Enable No Snoop** If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions to indicate that it does not require hardware enforced cache coherency. 0: Disabled 1: Enabled This root port controls the setting of the No Snoop bit (Attr[0]) for its downstream cycles at Rx1A0[6]. Writing 1 or 0 to this bit does not change the behavior of this chip.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power. 0: Disabled 1: Enabled This root port (RP0) does not support auxiliary power. Writing 1 or 0 to this bit does not change the behavior of this chip.
9	RO	0	**Phantom Functions Enable** This root port does not support Phantom Functions (Please refer to register descriptions at Rx44[4:3]). This bit is Read Only and always read as 0.
8	RO/RW	0	**Extended Tag Field Enable** This bit defines the bit size of the Tag field on a transaction generated by this root pot. 0: 5-bit Tag field is used. 1: 8-bit Tag field is used. When Rx44[5] is set to 0, this bit is RO. When Rx44[5] is set to 1, this bit is RW.
7:5	RW	0	**Max Payload Size** This field sets the maximum TLP payload size for this root port in a downstream posted write cycle or a completion return of a upstream read cycle. 000: 128 bytes. 001: 256 bytes. 010: 512 bytes. 011: 1024 bytes. 100: 2048 bytes. 101: Reserved, it is defined as 4096 bytes in PCIe spec, this root port (RP0) does not support this option. 110, 111: Reserved
4	RW	1b	**Enable Relaxed Ordering** If this bit is set to 1, the function is permitted to set the Relaxed Ordering bit in the Attributes field of the transactions it initiates that do not require strong write ordering. This root port controls the setting of the Relaxed Ordering bit (Attr[1]) for its downstream cycles at Rx1A0[5]. Writing 1 or 0 to this bit does not change the behavior of this chip. 0: Disabled 1: Enabled
3	RW	0	**Unsupported Request Reporting Enable** This bit is set to enable the report of an Unsupported Request error to Fatal Error Received bit (Rx130[6]), Non-Fatal Error Received bit (Rx130[5]) or Correctable Error Received bit (Rx130[0]). The Fatal, Non-Fatal, or Correctable error bits at Rx4A[2:0] won't be affected by the setting of this bit. 0: Disabled 1: Enabled
2	RW	0	**Fatal Error Reporting Enable** This bit is set to enable the setting of the Fatal Error Messages Received bit at Rx130[6]. i.e. if this bit is 0, Rx130[6] will always stay at 0. 0: Disabled 1: Enabled
1	RW	0	**Non-Fatal Error Reporting Enable** This bit is set to enable the setting of the Non-Fatal Error Messages Received bit at Rx130[5]. i.e. if this bit is 0, Rx130[5] will always stay at 0. 0: Disabled 1: Enabled

0	RW	0	**Correctable Error Reporting Enable** This bit is set to enable the setting of the ERR_COR Received bit at Rx130[0]. i.e. if this bit is 0, Rx130[0] will always stay at 0. 0: Disabled 1: Enabled

Offset Address: 4B-4Ah (D3F0-3)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:6	RW	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that this root port has issued Non-Posted Requests on its own behalf (using the Requestor ID of the Root Port) which have not been completed.
4	RO	1b	**AUX Power Detected** This bit is set to 1 when the function detects the Auxiliary power. Software may need this information to know if this root port is able to support the beacon wake up. 0: Auxiliary power has not been detected in this root port. 1: Auxiliary power has been detected in this root port.
3	RW1C	0	**Unsupported Request Detected (TL)** This bit is set to 1 when a completion is returned with completion status set at 100b for the downstream requests. Note that this bit differs from Rx104[20] in that this bit will not be affected by the mask bit at Rx108[20]. Writing 1 to this bit clear this bit to 0. 0: Unsupported request has not been detected in this root port. 1: Unsupported request has been detected in this root port.
2	RW1C	0	**Fatal Error Detected (TL)** This bit is set to 1 when one of the Uncorrectable Error Status bits at Rx104[31:0] is set *1 and their corresponding severity bits at Rx10C[31:0] is set. Writing 1 to this bit clear this bit to 0. 0: Fatal error has not been detected in this root port. 1: Fatal error has been detected in this root port.
1	RW1C	0	**Non-Fatal Error Detected (TL)** This bit is set to 1 when one of the Uncorrectable Error Status bits at Rx104[31:0] is set *1 and their corresponding severity bits at Rx10C[31:0] is not set. Writing 1 to this bit clear this bit to 0. 0: Non-fatal error has not been detected in this root port. 1: Non-fatal error has been detected in this root port.
0	RW1C	0	**Correctable Error Detected (TL)** This bit is set to 1 when one of the Correctable Error Status bits at Rx110[31:0] is set *1. It indicates a correctable error had happened in this root port. Writing 1 to this bit clear this bit to 0. 0: Correctable error has not been detected in this root port. 1: Correctable error has been detected in this root port.

*1: For some Uncorrectable Error in Rx104: Unsupported Request Error (Rx104[20]), ECRC Error (Rx104[19]), Unexpected Completion Error (Rx104[16]), Completion Timeout Error (Rx104[14]), and Poisoned TLP Error (Rx104[12]) can be reported to Fatal Error (Rx48[2]), Non-Fatal Error (Rx48[1]) or Correctable Error (Rx48[0]) depending on the corresponding severity bits at Rx10C, the Role-Based Error reporting (Rx44[15]). Please refer to the table below:

Corresponding Severity Bit	Role-Based Error Reporting bit	Fatal Error bit at Rx48[2], set or not set?	Non-Fatal Error bit at Rx48[1], set or Not Set?	Correctable Error bit at Rx48[0], set or not set?
Rx10C	Rx44[15]			
1	-	Set	Not Set	Not Set
0	0	Not Set	Set	Not Set
0	1	Not Set	Not Set	Set

Offset Address: 4F-4Ch (D3F0-3)

Link Capabilities **Default Value: nn3D Bnn2h**

Bit	Attribute	Default	Description
31:24	RO	*	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link. It is used as the Link Number during the training sequence of the PCIe Link on this root port. For the root port 0 (RP0) of this chip, its default value is 01h. ***For D3F1***, it is for the Port Number of RP1 and its default value is 02h. ***For D3F2***, it is for the Port Number of RP2 and its default value is 03h. ***For D3F3***, it is for the Port Number of RP3 and its default value is 04h.
23:22	RO	0	**Reserved**
21	RO	1b	**Link Bandwidth Notification Capability** This bit indicates support for the Link Bandwidth Notification status and interrupt mechanism. This root port does support the link bandwidth change notification. Please refer to link status, Rx52[15, 14].
20	RO	1b	**Data Link Layer Link Active Reporting Capable** This bit indicates support of reporting the DL_Active state of Data Link Control and Management State Machine (DLCMSM). 0: Not supported 1: Supported This root port does support this feature. When this bit is 1, the DL_Active state can be reported to Link status register, Rx52[13]. Note that DL_Active will become active before the completion of the configuration state of the LTSSM (Link Training & Status State Machine).
19	RO	1b	**Surprise Down Error Reporting Capable** When this bit is set, the Surprise down error is reported when the PCIe Link connected to this root port (RP0) is down (lost connection). 0: Not supported 1: Supported This root port reports the Surprise Down Error to the bit[5] of Uncorrectable Error Status of the Advanced Error Reporting Capability registers at Rx104[5]. Please refer to the descriptions there for the possible surprise down conditions.
18	RO	0	**Clock Power Management** For upstream ports, a value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) via the "clock request"(CLKREQ#) mechanism when the link is in the L1 and L2/L3 Ready Link sates. A value of 0b indicates the component does not have this capability and the reference clock(s) must not be removed in these link states. This root port is a downstream port, it is not supported.
17:15	RO	011b	**L1 Exit Latency** This field indicates the L1 exit latency (to L0) for the given PCIe Link. Defined encoding for this latency T_l_L1 are: 000: T_l_L1 < 1us. 001: 1us <= T_l_L1< 2us. 010: 2us <= T_l_L1 < 4us. 011: 4us <= T_l_L1 < 8us. 100: 8us <= T_l_L1 < 16us. 101: 16us <= T_l_L1 < 32us. 110: 32us <= T_l_L1 < 64us. 111: 64us <= T_l_L1
14:12	RO	101b	**L0s Exit Latency** This field indicates the L0s exit latency (to L0) for the given PCIe Link. Defined encoding for this latency T_l_L0s are: 000: T_l_L0s < 64ns. 001: 64ns <= T_l_L0s < 128ns. 010: 128ns <= T_l_L0s < 256ns. 011: 256ns <= T_l_L0s < 512ns. 100: 512ns <= T_l_L0s < 1us. 101: 1us <= T_l_L0s < 2us. 110: 2us <= T_l_L0s < 4us. 111: 4us <= T_l_L0s
11:10	RO	11b	**Active State Power Management (ASPM) Support** This field indicates the level of ASPM supported on the PCIe Link of this root port. 00: Reserved. 01: L0s Entry Supported. 10: Reserved. 11: L0s and L1 Supported. This root port (RP0) supports the capability of entering L0s and L1.
9:4	RO	HwInit	**Maximum Link Width** This field indicates the maximum link width implemented by this root port (RP0). 000000: Reserved. 000001: x1. 000010: x2. 000100: x4. 001000: x8. 001100: x12. 010000: x16. 100000: x32. Other: Reserved.

			The value of this register of this root port (RP0) depends on the value shown at D0F5, RxB0[7]: When D0F5, RxB0[7] = 0, PCIe Lane 0 ~ 3 (PEXTX[3:0]P/N, PEXRX[3:0]P/N) is used for PCIe, the default value of this field is 001000. When D0F5, RxB0[7] = 1, PCIe Lane 0 ~ 3 are used for the digital display interface, the default value of this field is thus 000100. Please refer to appendix G of D0F5 for more detail. ***For D3F1:*** When D0F5, RxB0[3] = 0, PCIe Lane 8, 9 (PEXTX[9:8]P/N, PEXRX[9:8]P/N) are both assigned for RP1. These field is thus 000010. When D0F5, RxB0[3] = 1, only PCIe Lane 8 (PEXTX[8]P/N, PEXRX[8]P/N) is assigned for RP1. This field is thus 000001. ***For D3F2:*** When D0F5, RxB0[3] = 0, PCIe Lane 8, 9 (PEXTX[9:8]P/N, PEXRX[9:8]P/N) are both assigned for RP1. This field is thus 000000. When D0F5, RxB0[3] = 1, PCIe Lane 9 (PEXTX[9]P/N, PEXRX[9]P/N) is assigned to RP2. This field is thus 000001. ***For D3F3:*** This field is always reported as 000001.
3:0	RO	0010b	**Supported Link Speed** This field indicates the supported Link speed of this root port. 0001b: 2.5GT/s. 0010b: 5.0GT/s and 2.5GT/s. Others: Reserved. This root port will use these bits in the Training Sequence to negotiate the link speed after the de-assertion of the PCIRST#

Offset Address: 51-50h (D3F0-3)

Link Control **Default Value: 00n0h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11	RW	0	**Enable Link Autonomous Bandwidth Interrupt** When Set, this bit enables the generation of an interrupt to indicate that the Link Autonomous Bandwidth Status bit (Rx53[7]) has been set. 0: Interrupt generation is disabled. 1: Enable the generation of an interrupt to indicate that the autonomous bandwidth status bit has been set.
10	RW	0	**Enable Link Bandwidth Management Interrupt** When Set, this bit enables the generation of an interrupt to indicate that the Link Bandwidth Management Status bit (Rx53[6]) has been set. 0: Interrupt generation is disabled. 1: Enable the generation of an interrupt to indicate that the link bandwidth management status bit has been set.
9	RW	0	**Hardware Autonomous Width Disable** When Set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. 0: The link width of this root port is allowed to change by the Hardware Autonomous Bandwidth Link management. 1: Other than the unreliable link induced width changing, the link width of this root port is not allowed to change.
8	RO	0	**Enable Clock Power Management** This bit is for upstream port that support the "Clock Request" (CLKREQ#) mechanism. 0: Clock power management is disabled and device must hold CLKREQ# low. 1: The device is permitted to use CLKREQ# signal to power manage link clock. This root port does not support this Features.
7	RW	0	**Extended Synch** When set, this bit force the transmission of additional Ordered Sets when exiting the L0s state and when in the Recovery State. This mode provides external devices (e.g. logic analyzers) monitoring the Link time to achieve bit and Symbol lock before the Link enters the L0 state and resumes communication. 0: This root port perform normally. 1) The Flow Control Update (FCU) timer limit is 30us. i.e. when the link is idle, the root port will perform FC updates every 30us. 2) Number of FTS Ordered Sets to be transmitted when the Link state changed from L0s to L0 is N_FTS which is sent by the device during TS1. Usually, 1 <= N_FTS <= 256. 3) Number of FTS Ordered Sets to be transmitted in Recovery.RcvrLock state is at least 8, and the root port won't stop transmitting until there is response from the device. 1: This root port will extend those values described in setting 0 above: 1) The FCU timer limit is 120us. 2) Number of FTS transmitted during L0s to L0 transition is 4096. 3) Number of FTS transmitted is at least 1024, and the root port won't stop transmitting until there is response from the device.
6	RW	1b	**Common Clock Configuration** When this root port and the device connected on it use two different clock sources (100Mhz), this bit should be set to 0; And if this root port and the device connected on it use the distributed common reference clock, this bit should be set to 1. The design should use this bit to report the correct L0s and L1 exit latency. 0: It should be set to this when asynchronous reference clocks are used for this root port and the device connected to it. 1: It should be set to this when a distributed common reference clock is used for this root port and the device connected to it. This root port did not implement any design according to the setting of this bit. Writing 1 or 0 to this bit does not change the behavior of this chip.
5	RW	0	**Retrain Link** Link retrain is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM (Link Training & Status State Machine) of this root port to the Recovery state to retrain the link. It will be cleared to 0 when the LTSSM get into the Recovery state.
4	RW	0 ROMSIP	**Link Disable** This bit disables the Link by directing the LTSSM (Link Training & Status State Machine) of this root port to Disabled State when it is set. 0: The link is enabled. 1: The link is disabled. ROMSIP cycle right after the de-assertion of PCIRST# will set this bit to an initial value. The corresponding programming bit is the third QW, byte 4, bit[0]. ***For D3F1:*** The ROMSIP bit is at 3rd QW, byte 5, bit[0]. ***For D3F2:*** The ROMSIP bit is at 3rd QW, byte 6, bit[0]. ***For D3F3:*** The ROMSIP bit is at 3rd QW, byte 7, bit[0].

3	RO	0	**Read Completion Boundary** This field indicates the Read Completion Boundary (RCB) value for this root port. It is to determine the data boundary for the read data returned from the devices for a read completion. 0: 64 bytes 1: 128 bytes
2	RO	0	**Reserved**
1:0	RW	00b	**Link Active State Power Management (ASPM) Control** This field controls the level of ASPM supported on this root port. It basically enables the link power management state machine of the transmitter of this root port to be able to enter the L0s or L1 state. 00: Disable 01: Enable L0s entry 10: Enable L1 entry 11: Enable L0s and L1 entry

Offset Address: 53-52h (D3F0-3)

Link Status **Default Value: nnnnh**

Bit	Attribute	Default	Description
15	RW1C	0	**Link Autonomous Bandwidth Status** This bit is set to 1b to indicate that hardware has autonomously changed link speed or width, without the port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable link operation.
14	RW1C	0	**Link Bandwidth Management Status** This bit is Set by hardware to indicate that either of the following case has occurred without the port transitioning through DL_Down state: 1. LTSSM transits from Recovery to L0 after the Link Retraining bit (Rx50[5]) being programmed to 1. 2. Either Link speed or Link width is changed due to either Unreliable Link Management or Autonomous Bandwidth Link Management mechanism. Interrupt can be generated if bit10 of the link control register (Rx50[10]) is set to 1.
13	RO	0	**Data Link Layer Link Active** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active State, 0b otherwise. 0: Data Link Layer is inactive 1: Data Link Layer is active Since the Data Link Active reporting capability bit is set at Rx4C[20], this bit is set to 1 after the completion of the configuration state of the LTSSM (Link Training & Status State Machine) to report the Data Link is at active state.
12	RO	1b	**Slot Clock Configuration** This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector. For this root port, this bit is read 1.
11	RO	HwInit	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit (Rx50[5]) but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	HwInit	**Training Error** Set when a Link training error occurred. Link training error is defined when the root port cannot receive correct training order set within 24ms after it sent out the training order set. When the training error happened, the LTSSM (Link Training and Status State Machine) in physical layer will go to Detect state to start link initialization over again. It is cleared by hardware upon successfully training of the Link when the link state goes to the L0 Link state.
9:4	RO	HwInit	**Negotiated Link Width** This field indicates the negotiated width of the link governed by this root port. These bits will be updated every time the link goes through link configuration and training. ***For D3F0:*** 000001: x1. 000010: x2. 000100: x4. 001000: x8. Others: Invalid. ***For D3F1:*** 000001: x1. 000010: x2. Others: Invalid. ***For D3F2:*** 000001: x1. Others: Invalid. ***For D3F3:*** 000001: x1. Others: Invalid.
3:0	RO	HwInit	**Current Link Speed** This field indicates the negotiated Link speed of the link governed by this root port. These bits will be updated every time the link goes through link training. 0001: 2.5GT/s (PCIe-I). 0010: 5.0 GT/s (PCIe-II).

Offset Address: 57-54h (D3F0-3)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO)	0	**Physical Slot Number** This field indicates the physical slot number attached to this root port. That number should be unique in the system. This field must be initialized to zero for ports connected to devices that are either integrated on the system board or integrated within the same silicon. This field did not specify at chip level, however, this bit becomes writable when D0F5, RxF0[0] is set to 1.
18	RO	0	**No Command Completed Support** When Set, this bit indicates that the slot connected to this root port does not generate software notification when an issued command is completed by the Hot-Plug Controller. This root port does not have Hot-Plug controller associated with it, however, command completed notification is supported as described at bit[4] of Slot Status register at Rx5A[4]. It should be always read 0.
17	RO	0	**Electromechanical Interlock Present** When Set, this bit indicates that an Electromechanical interlock is implemented for the slot connected to this root port. This root port does not support it. It should be always read 0.
16:15	RO	0	**Slot Power Limit Scale** This field specifies the scale used for the Slot Power Limit Value defined at bit[14:7] of this register. Range of the values: 00: 1.0 x. 01: 0.1 x. 10: 0.01 x. 11: 0.001 x. This root port will send Set_Slot_Power_Limit Message to the devices connected to it at certain condition, please refer to the descriptions at bit[14:7] of this register. This root port did not define the Slot Power Limit on the chip level, however, this field can be written when D0F5, RxF0[0] is set to 1.
14:7	RO	0	**Slot Power Limit Value** In combination with the Slot Power Limit Scale value (bit[16:15] of this register), these bits specifies the upper limit o power supplied by the slot connected to this root port. Power limit (in Watts) of the slot is calculated by: Power Limit = Slot Power Limit Value * Slot Power Limit Scale. 00h: Slot Power Limit = 0W. 01h: Slot Power Limit = 1W. 02h: Slot Power Limit = 2W. 03h: Slot Power Limit = 3W. …. EEh: Slot Power Limit = 238W. EFh: Slot Power Limit = 239W. Except when Slot Power Limit Value is over EFh, F0h: Slot Power Limit = 250W. F1h: Slot Power Limit = 275W. F2h: Slot Power Limit = 300W. F3h~FFh: Reserved. This root port will send Set_Slot_Power_Limit Message to the devices connected to it with the Slot Power Limit value defined by the Power Limit mentioned above when 1) the Data Link Layer becomes Active after the training sequence or 2) Slot Capability bytes (register bytes at Rx54, Rx55, or Rx56) are written. A register at D0F4, Rx40[6]can be set to 1 to disable this root port to send the Set_Slot_Power_Limit Message out. This root port did not define the Slot Power Limit on the chip level, however, this field can be written when D0F5, RxF0[0] is set to 1.
6	RO	1b	**Hot-plug Capable** When set, this bit indicates that this slot is capable of supporting hot-plug operations.
5	RO	1b	**Hot-Plug Surprise** When set, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow such removal without impact on successive software operation.
4	RO	0	**Power Indicator Present** When set, This bit indicates that a Power Indicator is electrically controlled by this root port. This root port does not have the control over the Power Indicator on the slot. It is always read 0.
3	RO	0	**Attention Indicator Present** When set, this bit indicates that an Attention Indicator is electrically controlled by this root port. This root port does not have the control over the Attention Indicator on the slot. It is always read 0.
2	RO	0	**MRL Sensor Present** When Set, this bit indicates that a MRL (Manually-operated Retention Latch) Sensor is implemented. This chip does not have MRL Sensor in it. It is always read 0.
1	RO	0	**Power Controller Present** When set, this bit indicates that a software programmable Power Controller is implemented for this slot. This chip does not have power controller in it. It is always read 0.
0	RO	0	**Attention Button Present** When set, this bit indicates that an Attention Button (for hot-plug) for this slot is electrically controlled by this root port. This root port does not have the control over the attention button on the slot. It is always read 0.

Offset Address: 59-58h (D3F0-3)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Data Link Layer State Changed Enable** When Set, this bit enables software notification (interrupt) when Data Link Layer Link Active reporting bit which reported at bit[8] of Slot Status register at Rx5A[8] is changed 0: Disabled 1: Enabled *1
11	RO	0	**Electromechanical Interlock Control** A write of 1 to this bit causes the state of the interlock to toggle. A write of 0 to this bit has no effect. This root port does not support the electromechanical interlock, this bit is read only, and always read 0.
10	RW	0	**Power Controller Control** This bit when written sets the power state of the slot per the defined encodings. 0: Power on 1: Power off This root port does not have power controller in it. Writing 1 or 0 to this bit does not change the behavior of this chip.
9:8	RW	0	**Power Indicator Control** Writes to this field set the Power Indicator to the Written state. This root port does not have direct control to the Power Indicator. Upon being written to these bits (this register byte, Rx59) with value other than 00, this root port will send a Message TLP out to the device connected to it. 00: Reserved 01: On. Power_Indicator_On Message (with Message code = 0100_0101b & Type sub-field, r[2:0] = 100b) will be sent 10: Blink. Power_Indicator_Blink Message (with Message code = 0100_0111b & Type sub-field, r[2:0] = 100b) will be sent 11: Off. Power_Indicator_Off Message (with Message code = 0100_0100b & Type sub-field, r[2:0] = 200b) will be sent
7:6	RW	0	**Attention Indicator Control** Writes to this field set the Attention Indicator to the states defined by these bits. This root port does not have direct control to the Attention Indicator. Upon being written to these bits (this register byte, Rx58) with value other than 00, this root port will send a Message TLP out to the device connected to it. 00: Reserved 01: On. Attention_Indicator_On Message (with Message code = 0100_0001b & Type sub-field, r[2:0]=100b) will be sent 10: Blink. Attention_Indicator_Blink Message (with Message code = 0100_0011b & Type sub-field, r[2:0] = 100b) will be sent 11: Off. Attention_Indicator_Off Message (with Message code = 0100_0000b & Type sub-field, r[2:0] = 100b) will be sent
5	RW	0	**Hot-Plug Interrupt Enable** When Set, this bit enables generation of an interrupt on enabled Hot-Plug events. For this root port, these events are Attention button pressed, Presence Detect changed, and Command competed. 0: Disabled 1: Enabled
4	RW	0	**Command Completed Interrupt Enable** When Set, this bit enables software notification (interrupt) when a Hot-Plug command is completed by the Hot-Plug Controller. This root port does not have Hot-Plug controller associated with it. However, please refer to bit[4] of Slot status register at Rx5A[4] for descriptions. This bit enables the interrupt generation when Rx5A[4] is set. 0: Disabled 1: Enabled*1
3	RW	0	**Presence Detect Changed Enable** When Set, this bit enables software notification (interrupt) on a presence detect changed which reported at bit[3] of Slot Status register at Rx5A[3]. 0: Disabled 1: Enabled*1
2	RO	0	**MRL Sensor Change Enable** When Set, this bit enables software notification (interrupt) on a MRL (Manually-Operated Retention Latch) sensor changed event. 0: Disabled 1: Enabled*1 This chip does not have MRL sensor associated with this root port. This bit cannot be set and will always be 0.
1	RO	0	**Power Fault Detected Enable** When Set, this bit enables software notification (interrupt) on a power fault event. 0: Disabled 1: Enabled*1 This chip does not have power controller and is not able to detect power fault. This bit cannot be set and will always be 0.

0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event which reported at bit[0] of Slot Status register at Rx5A[0]. 0: Disabled 1: Enabled*1

*1: Bit[5] of this register, Hot-Plug Interrupt Enable, will also need to be enabled to have the interrupt or MSI generated.

Offset Address: 5B-5Ah (D3F0-3)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW1C	0	**Data Link Layer State Changed** This bit is Set when the value reported in the Data Link Layer Link Active bit of the Link Status register is changed. 0: Data Link's state does not change. 1: Data Link's state changed. This bit is asserted when Rx53[5] is changed.
7	RO	0	**Electromechanical Interlock Status** This bit indicates the status of the Electromechanical interlock. 0: Electromechanical interlock disengaged. 1: Electromechanical interlock engaged. This root port does not support the Electromechanical Interlock, this bit is always read 0.
6	RO	0	**Presence Detect State** This bit indicates the presence of an adapter in the slot, reflected by the logic "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. 0: Slot empty 1: Card present in slot The root port of this chip only implement the in-band presence detect mechanism. i.e. this bit reflects the Physical Layer's detection results.
5	RO	0	**MRL Sensor State** This bit reports the status of the MRL (Manually-Operated Retention Latch) sensor. 0: MRL is closed 1: MRL is opened This root port does not have a MRL sensor associated with it. This bit is always read as 0.
4	RW1C	0	**Command Completed** This bit is Set when a hot-plug command has competed and the Hot-Plug Controller is ready to accept a subsequent command. 0: Not completed 1: Completed This root port does not have the hot-plug controller associated with it, however, this bit is set when bit[9:8] or bit[7:6] of slot control register (Rx58[9:8] and Rx58[7:6]) is set to one of ON, OFF, or Blink states.
3	RW1C	0	**Presence Detect Changed** This bit is set when the value reported in the Presence Detect State bit is changed. i.e. this root port detects the device connected to it become inactive or this root port detects a device connect to it and become active after the Presence Detect process. 0: Presence Detect in the Physical Layer of this root port is not changed. 1: Presence Detect in the Physical Layer of this root port is changed.
2	RO	0	**MRL Sensor Changed** This bit is Set when a MRL (Manually-Operated Retention Latch) Senor state change is detected. 0: MRL Senor state is not changed. 1: MRL Sensor state changed. This root port does not have MRL sensor associated with it, this bit is always read 0.
1	RO	0	**Power Fault Detected** This bit is Set when the Power Controller detects a power fault at this slot. 0: No power fault is detected. 1: A power fault is detected. This root port does not have power controller associated with it, this bit is always read 0.
0	RW1C	0	**Attention Button Pressed** This bit is Set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set. 0: Attention Button is not pressed. 1: Attention Button is pressed. This root port is implemented in a way that this bit is set whenever this root port received Attention_Button_Pressed Message (with message Code = 0100_1000b & Routing 2[2:0] = 100b) from the device.

Offset Address: 5D-5Ch (D3F0-3)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RO	0	**Reserved**
4	RW	0	**CRS Software Visibility Enable** When Set, this bit enables the root port to return Configuration Request Retry Status (CRS) Completion Status to software. This bit defined the behavior of the configuration read cycle which accesses offset 00-03h of the PCI configuration space on the device connected to it when received completion with CRS (completion status = 010b). 0: Disabled. Upon seeing the CRS completion, this root port will re-issue that configuration cycle to the device until the cycle is successfully completed. 1: Enabled. Upon seeing the CRS completion, this root port will not re-issue the configuration read cycle, instead, it returns data with Vendor ID field = 0001h, other bits = 1b to the CPU.
3	RW	0	**PME Interrupt Enable** When Set, this bit enables PME interrupt generation upon receipt of a PME Message as reflected in the PME Status bit at bit16 of the Root Status (Rx60[16]). A PME interrupt is also generated if the PME status register bit is set when this bit is set from clear state. 0: Disabled 1: Enabled
2	RW	0	**System Error on Fatal Error Enable** If Set, this bit indicates that a System Error (SERR#) should be generated if a non-fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with this root port, or by the root port itself. 0: Disabled 1: Enabled With this bit being set to 1, this root port should have generated the System Error upon seeing the assertion of fatal-error bit at Rx130[6]. But since this System Error did not pass to the NMI generation circuit in the SB block, the enabling of this bit does not really make any change to the behavior of this chip.
1	RW	0	**System Error on Non-Fatal Error Enable** If Set, this bit indicates that a System Error (SERR#) should be generated if a non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with this root port, or by the root port itself. 0: Disabled 1: Enabled With this bit being set to 1, this root port should have generated the System Error upon seeing the assertion of non-fatal error bit at Rx130[5]. But since this System Error did not pass to the NMI generation circuit in the SB block, the enabling of this bit does not really make any change to the behavior of this chip.
0	RW	0	**System Error on Correctable Error Enable** If Set, this bit indicates that a System Error (SERR#) should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with this root port, or by the root port itself. 0: Disabled 1: Enabled With this bit being set at 1, this root port should have generated the System Error upon seeing the assertion of correctable error bit at Rx130[0]. But since this System Error did not pass to the NMI generation circuit in the SB block, the enabling of this bit does not really make any change to the behavior of this chip.

Offset Address: 5F-5Eh (D3F0-3)

Root Capabilities **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**CRS Software Visibility** When Set, this bit indicates that this root port is capable of returning Configuration Request Retry Status (CRS) completion status to software – returning configuration data with Vendor ID = 0001h, and other bits = 1b to the CPU. 0: Not capable 1: Capable

Offset Address: 63-60h (D3F0-3)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**PME Pending** This bit indicates that another PME is pending when the PME status bit (bit[16] of this register) is set. 0: No pending PME. 1: Indicates another PME is pending when the PME Status (bit[16] of this register) is set. This root port keeps track only one PME pending event (including its PME requester ID), it will discard those coming in PME events after this bit is set. If this bit is set, the PME status (bit[16] of this register) will be set to 1 again when it is cleared by software. PME Requester ID (bit[15:0] of this register) will also be updated at the same time when PME status is set.
16	RW1C	0	**PME Status** When asserted, this bit indicates either one of the following cases happened: 1). The PME was asserted (received Power Management Message – PM_PME) by the PME Requester with Requester ID indicated at PME Requester ID file, Bits[15:0] of this registers. 2). PME enable bit (RxA4[8]) & Presence Detect Changed Enable bit (Rx58[3]) are both enabled, and Presence Detect Changed bit (Rx5A[3]) is also set. 3). PME enable bit (RxA4[8]) & Attention Button Pressed Enable bit (Rx58[0]) are both enabled, and Attention Button Pressed bit (Rx5A[0]) is also set. Writing 1 to this bit clears it to 0.
15:0	RO	0	**PME Requester ID** This field indicates the PCI Requester ID of the last PME Requester. It is only valid when bit[16] is set. Note that PME is sent through the Power Management Messages – PM_PME.

Offset Address: 67-64h (D3F0-3)

Device Capabilities 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:6	RO	0	**Reserved**
5	RO	0	**ARI Forwarding Supported** ARI (Alternative Routing ID) is the capability of treating the configuration cycle having 256 functions for the root port. i.e. the original device field (5 bits) of a configuration cycle will be ignored and considered part of the function bits. Thus, when decoding configuration cycle, this root port will always consider the device # is 00000b so that the configuration cycle can be forwarded to the device connected to it. Note that for those root port not supporting ARI, configuration cycle to be forwarded must have its device filed to be 00000b. 0: Not supported 1: Supported
4	RO	0	**Completion Timeout Disable Supported** A value of 1 indicates support for the Completion Timeout Disable Mechanism. 0: Not support Completion Timeout Disable. 1: Support Completion Timeout Disable. This root port did support Completion Timeout, but the timeout value is not as the range suggested by the PCIe specification defined at Device Capability 2 register bit[3:0] (Rx64[3:0]). Please refer to Rx68[4].
3:0	RO	0	**Completion Timeout Ranges Supported** This field indicates device Function support for the optional Completion Timeout Programmability mechanism. Four time value ranges are defined: Range A: 50us to 10ms. Range B: 10ms to 250ms. Range C: 250ms to 4s. Range D: 4s to 64s. And bits are set according to: 0000: Completion Timeout Programming not supported. 0001: Range A 0010: Range B 0011: Ranges A and B 0100, 0101: Reserved 0110: Ranges B and C 0111: Ranges A, B, and C 1000, 1001, … 1101: Reserved 1110: Ranges B, C, and D 1111: Ranges A, B, C, and D This root port does not support Completion Timeout Programming as PCIe specification suggested here. The Completion timeout value is defin-.

Offset Address: 69-68h (D3F0-3)

Device Control 2 **Default Value: 0000h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO/RW	0	**Enable ARI Forwarding** This bit is to enable the ARI (Alternative Routing ID) capability. Please refer to the register descriptions at Rx64[5]. 0: Disabled. When decode and forward downstream Type1 to Type 0 configuration cycle, this root port will check if the device field = 00000b. 1: Enabled. When decode and forward downstream Type1 to Type 0 configuration cycle, this root port will not check if the device field = 00000b.
4	RW	0	**Completion Timeout Disable** When Set, this bit disables the Completion Timeout mechanism. 0: Enable Completion Timeout function. 1: Disable Completion Timeout function. This root port did have Completion Timeout mechanism, but the timeout range is not as suggested by the PCIe defined at Bit[3:0] of this register. Instead, the timeout range defined at Rx1A1[2:0]. Setting this bit to 1 disables the Completion Timeout function defined by Rx1A1[2:0].
3:0	RO	0	**Completion Timeout Value** In device Functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. Timeout programmability must support the values given below corresponding to the programmability ranges indicated in bit[3:0] of Device Capability 2 register, Rx64[3:0]. Defined encodings: 0000: Default range, which is 50us to 50ms. Value available if Range A is supported: 0001: 50us to 100us. 0010: 1ms to 10ms. Value available if Range B is supported: 0101: 16ms to 55ms. 0110: 65ms to 210ms. Value available if Range C is supported: 1001: 260ms to 900ms. 1010: 1s to 3.5s. Value available if Range D is supported: 1101: 4s to 13s. 1110: 17s to 64s. Values not defined above are reserved. This root port does support Completion Timeout Programming. However, the timeout range is not defined by these bits but at Rx1A1[2:0].

Offset Address: 6A-6Fh (D3F0-3) – Reserved

Offset Address: 71-70h (D3F0-3)

Link Control 2 **Default Value: 00n2h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RWS	0	**Compliance De-emphasis** This bit sets the de-emphasis level in Polling.Compliance State if the entry occurred due to the Enter Compiance bit (Bit[4] of this register) being 1b. It depends the current link speed at the Rx52[3:0]: When Rx52[3:0] = 0001, this root port operated at PCIe-I: 0: -3.5db 1: -3.5db When Rx52[3:0] = 0010, this root port operated at PCIe-II: 0: -6db 1: -3.5db For the de-emphasis level setting at regular operation, please refer to bit[6] of this register.
11	RWS	0	**Compliance SOS** When Set to 1, the LTSSM of this root port is required to send SKP Ordered Sets (SOS) periodically in between the (modified) compliance patterns. 0: No SOS is sent in between the (modified) compliance patterns. 1: The LTSSM will send SOS periodically in between the (modified) compliance patterns. SOS can be sent to aligned patterns which travelled in the link for two devices used different clocks.
10	RWS	0	**Enter Modified Compliance** When this bit is set to 1, the device transmits Modified Compliance Pattern if the LTSSM enters Polling Compliance sub-state. 0: This root port transmits Modified Compliance Pattern if LTSSM of this root port enters Polling.Compliance state. 1: This root port transmits Normal Compliance Pattern if LTSSM of this root port enters Polling.Compliance state.
9:7	RWS	0	**Transmit Margin** This field controls the value of the voltage level (full swing [V_{TX-PP}] / de-emphasis level [$V_{TX-DE-EMPH}$] / low swing [$V_{TX-PP-LOW}$]) at the transmitting pins PEXTX[7:0]P/N. This field is reset to 000b on entry to the LTSSM Polling.Configuration substate of this root port. When Transmit Margin Manual set register D3F4, Rx50[4] is set to 0, this register associated with Rx1CE[2], Rx70[6] affect the voltage swing level on PEXTX[7:0]P/N. However, when D3F4, Rx50[4] is 1, registers at Rx50[7:5], Rx50[0], Rx50[1] of D3F4 take place to control. ***When {Rx1CE[2], Rx70[6]} = 00, primarily for PCIe-II:*** 000: Depending on the register setting on D3F4, Rx53-52. With the default, V_{TX-PP} / $V_{TX-DE-EMPH}$ is 1.02v/0.48v (-6.55db) for PCIe-II. 001: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 1.02v/0.48v (-6.55db). 010: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 0.68v/0.32v (-6.55db). 011: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 0.48v/0.22v (-6.78db). 100: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 0.27v/0.13v (-6.35db). 101 ~ 111: Invalid. ***When {Rx1CE[2], Rx70[6]} = 01, primarily for PCIe-I:*** 000: Depending on the register setting on D3F4, Rx53-52. With the default, V_{TX-PP} / $V_{TX-DE-EMPH}$ is 1.03v/0.67v (-3.74db) for PCIe-II. 001: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 1.03v/0.67v (-3.74db). 010: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 0.71v/0.49v (-3.22db). 011: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 0.50v/0.30v (-4.44db). 100: V_{TX-PP} / $V_{TX-DE-EMPH}$ is 0.30v/0.20v (-3.52db). 101 ~ 111: Invalid. ***When {Rx1CE[2], Rx70[6]} = 1-, Low Swing:*** 000: Depending on the register setting on D3F4, bit[2:0] of Rx53-52. With the default, $V_{TX-PP-LOW}$ is 0.5v for PCIe-II, and 0.6v for PCIe-I. 001: $V_{TX-PP-LOW}$ is 0.50v. 010: $V_{TX-PP-LOW}$ is 0.30v. 011: $V_{TX-PP-LOW}$ is 0.20v. 100: $V_{TX-PP-LOW}$ is 0.10v. 101 ~ 111: Invalid. ***For D3F1:*** When D0F5, RxB0[3] is 0, this bit is to control PEXTX[9:8]P/N. When D0F5, RxB0[3] is 1, this bit is to control PEXTX[8]P/N. ***For D3F2:*** This bit is to control PEXTX[9]P/N. ***For D3F3:*** This bit is to control PEXTX[10]P/N.
6	RO	HwInit	**Selectable De-emphasis** The de-emphasis level of the transmitting circuit comes from several sources as listed on the Table 28 below. This bit is one of the source when D3F4, Rx50[4] = 0 and Rx200[1] = 1. When the Link is operating at 5.0GT/s speed, the de-emphasis value works with bit[9:7], Rx1CE[2] to control the transmit voltage swing level. Please refer to register descriptions at

			bit[9:7] of this register for more information. 0: -6 db 1: -3.5db This bit is read only and will be set to 1 if either bit[1] or bit[0] of D3F4, Rx50 is set to 1.
5	RW	0	**Hardware Autonomous Speed Disable** When Set, this bit disables hardware from changing the Link speed for device-specific reasons other than attempting to correct unreliable Link operation by reducing Link speed. This chip implement a scheme called "Autonomous Bandwidth Link Management" for each root port. 0: Autonomous Bandwidth Link Management is enabled. 1: Autonomous Bandwidth Link Management is disabled.
4	RWS	0	**Enter Compliance** Software is permitted to force this link to enter Compliance mode at the speed indicated in the Target Link Speed field (Bit[3:0] of this register) by setting 1 to this bit. After setting this bit to 1, software should set Rx3E[6] to 1 then to 0 to start the Detect and Compliance process. And after the LTSSM of this root port goes to Compliance state, it will stay there unless this bit is set to 0. 0: Normal operation. 1: Entering Polling.Compliance state.
3:0	RWS	0010b	**Target Link Speed** The default value of this field is the highest Link speed supported by this root port. This field is used to set the target compliance mode speed when software is using the Enter Compliance bit (Bit[4] of this register) to force this Link into compliance mode. 0001: 2.5GT/s Target Link speed. 0010: 5.0GT/s Target Link speed. Others: Invalid.

Table 29. Rx70. De-emphasis Value for the Transmitting Circuit

D3F4	D3F0-3	De-emphasis value of Transmit circuit comes from?
Rx50[4]	Rx200[1]	
1	-	D3F4, Rx50[0]
0	0	Suggesting value got from Training Sequence
0	1	D3F0-3, Rx70[6]

Offset Address: 73-72h (D3F0-3)

Link Status 2 **Default Value: 000nh**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	HwInit	**Current Link De-emphasis Level** When the Link is operating at 5GT/s speed, this bit reflects the level of de-emphasis for the transmitting circuit. This root port may update this bit every time the LTSSM went in/out of Polling or Recovery state doing the speed negotiation when the de-emphasis level option is given by D3F4, Rx50[4]= 0, and Rx200[1] = 0. The de-emphasis level can also be determined by D3F4, Rx50[0] or Rx70[6], please refer to the Table 29 above. 0: -6 db 1: -3.5db

Offset Address: 74-9Fh (D3F0-3) – Reserved

PCI Power Management Capability Structure Registers (A0-AFh)

PCI Power Management Capability register for this root port had the following structure.

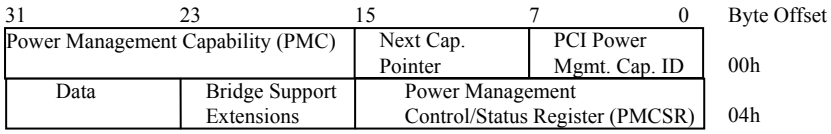


Figure 46. PCI Power Management Capability Structure

Offset Address: A1-A0h (D3F0-3)

Capabilities ID & Next Pointer **Default Value: B001h**

Bit	Attribute	Default	Description
15:8	RO	B0h	**Next Capability Pointer** Next capability started at RxB0.
7:0	RO	01h	**Capability ID** 01h indicates this capability is for PCI Power Management registers.

Offset Address: A3-A2h (D3F0-3)

Power Management Capabilities **Default Value: C822h**

Bit	Attribute	Default	Description
15: 11	RO	19h	**PME Support** This 5 bit field indicates the power states in which this function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signals while in that power state. i.e. xxxx1: PME# can be asserted from D0 power state. xxx1x: PME# can be asserted from D1 power state. xx1xx: PME# can be asserted from D2 power state. x1xxx: PME# can be asserted from D3 (Hot) power state. 1xxxx: PME# can be asserted from D3 (Cold) power state. This root port report 19h, means that this root port as a PCI-to-PCI bridge will forward the PME# from device connected to it when this root port's power state is at D0, D3 (Hot) or D3 (Cold).
10	RO	0	**D2 Support** This bit indicates the support of D2 power state for this root port. 0: Not supported 1: Supported This root port does not support D2 power state.
9	RO	0	**D1 Support** This bit indicates the support of D1 power state for this root port. 0: Not supported 1: Supported This root port does not support D1 power state.
8:6	RO	0	**AUX Current** This 3 bit field reports the 3.3Vaux auxiliary current requirements for this root port. 000: Self powered 001: 55 mA 010: 100 mA 011: 160 mA 100: 220 mA 101: 270 mA 110: 320 mA 111: 375 mA This root port does not need Aux power. It is read as 0.
5	RO	1b	**Device Specific Initialization** This bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. A "1" indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
4	RO	0	**Reserved**
3	RO	0	**PME Clock** This bit indicates if PCI clock is needed to generate PME#. 0: No PCI clock is needed 1: PCI clock is needed For this root port, this bit does not apply.
2:0	RO	010b	**Version** A value of 010b indicates that this root port implemented this power management complies with Revision 1.1 of the PCI Power Management Interface Specification.

Offset Address: A7-A4h (D3F0-3)

Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data** This register is used to report the state dependent data requested by the Data_Select field (bit[12:9] of this register). The value of this register is scaled by the value reported by the Data_Scale field (bit[14:13] of this register).
23	RO	0	**Bus Power / Clock Control Enable** This bit is to enable the Bus Power/clock control mechanism as described at section 4.7 of PCI Power Management specification rev 1.1 or above. Basically, when enabled, the D2 state will stop the clock on the bus. And the D3 state will shot the power off. 0: Disabled 1: Enabled This root port does not implement this power /clock control. This bit is read only and always read as 0.
22	RO	0	**B2 / B3 Support** The state of this bit determines the action that is to occur as a direct result of programming the power state (bit[1:0] of this register) to D3(Hot). 0: D3(Hot) state will have the power of the secondary bus removed. 1: D3(Hot) state will have the clock of the secondary bus stopped. This root port does not implement the power/control control. This bit is read only and always read as 0.
21:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit is set when this root port would normally assert the PME# signal independent of the state of the PME_EN bit (bit8 of this register). This root port will send PME as interrupt only when PME_EN bit is set. This bit is always read as 0.
14:13	RO	0	**Data Scale** This 2 bit field indicates the scaling factor to be used when interpreting the value of the Data register (bit[31:24] of this register). 00: Reserved 01: 0.1 x. (in Watt) 10: 0.01 x (in Watt) 11: 0.001 x (in Watt) This field is not applied to this root port.
12:9	RO	0	**Data Select** This 4 bit field is used to select which data is to be reported through Data register (bit[31:24] of this register). 0h: D0 Power Consumed. 1h: D1 Power Consumed. 2h: D2 Power Consumed. 3h: D3(Hot) Power Consumed. 4h: D0 Power Dissipated. 5h: D1 Power Dissipated. 6h: D2 Power Dissipated. 7h: D3(Hot) Power Dissipated. 8h: Common Logic Power Consumption for D3F0. Reserved for D3F1, D3F2, D3F3. Others: Reserved. This field is not applied to this root port.
8	RWS	0	**PME Enable** This field control the assertion of PME#. 0: Disabled 1: Enabled This root port implemented this bit to reflect the status of Attention Button Pressed (Rx5A[0]) & Presence Detect Changed (Rx5A[3]) to the assertion of PME Status bit (Rx60[16]). Please refer to the descriptions at Rx60[16] for more information.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State** This 2 bit field is used to determine the current power state of this root port. And writing a different value to this bits set this root port into a new power state. 00: D0 01: D1 10: D2 11: D3(Hot) This root port required this field to be 00. If this field is programmed to a value other than 00, the PCIe Link might not be able to go to L0s state.

Offset Address: A8-AFh (D3F0-3) – Reserved

PCI Message Signal Interrupt (MSI) Capability Structure Registers (B0-DFh)

PCI Message Signal Interrupt Capability register for this root port had the following structure.

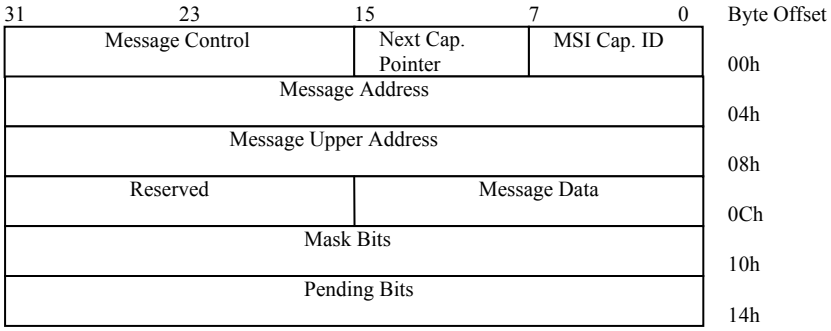


Figure 47. MSI Capability Structure

Offset Address: B1-B0h (D3F0-3)

Capability ID & Next Pointer **Default Value: E005h**

Bit	Attribute	Default	Description
15:8	RO	E0h	**Next Capability Pointer** This 8 bits register pointed to the next capability that this function claimed. Next capability is at RxE0 for this root port.
7:0	RO	05h	**Capability ID** 05h indicates this capability is a MSI capability register structure.

Offset Address: B3-B2h (D3F0-3)

MSI Capability Support **Default Value: 0180h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RO	1b	**Pre-vector Masking Capable** This bit indicates the support of MSI per-vector masking. 0: Not supported 1: Supported This root port supports the per-vector masking. Please refer to Message Mask Control register at RxC0.
7	RO	1b	**64-Bit Message Address Capable** This bit indicates the capability of generating MSI using 64 bits address. 0: Not supported 1: Supported This root port supports this 64 bit addressing. However, this chip only supports address up to A32. For normal MSI operation, bit[31:1] of System-Specified Message Address –High register at RxB8 must be 0.
6:4	RW	0	**Multiple Message Enable** System software writes to this field to indicate the number of allocated vectors. The number of allocated vectors is aligned to a power of two and must be less or equal to the values reported by the Multiple Message Capable registers (bit[3:1] of this register). 000: 1 vector allocated 001: 2 vectors allocated 010: 4 vectors allocated 011: 8 vectors allocated 100: 16 vectors allocated 101: 32 vectors allocated 11x: Reserved This root pot had only one vector, this field is thus always 000b.
3:1	RO	0	**Multiple Message Capable** System software reads this field to determine the number of vectors requested by this function. 000: 1 vector requested 001: 2 vectors requested 010: 4 vectors requested 011: 8 vectors requested 100: 16 vectors requested 101: 32 vectors requested 11x: Reserved This root pot had only one vector, this field is thus always 000b.
0	RW	0	**MSI Enable** This bit is to enable the MSI. Once set, this function is permitted to use MSI to request service and is prohibited from using its INTx# pin. 0: MSI is disabled 1: MSI is enabled

Offset Address: B7-B4h (D3F0-3)

Message Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Message Address** This field is the system-specified message address. If the Message Enable bit (RxB0[16]) is set, the contents of this register specify the DWORD assigned address (Addr[31:2]) for the MSI memory write transaction.
1:0	RO	0	**Reserved**

Offset Address: BB-B8h (D3F0-3)

Message Upper Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Message Upper Address** This field is the system-specified message upper address. If the Message enable bit (RxB0[16] is set, the contents of this register specify the upper 32 bits of a 64-bit message address (Addr[63:32]). This chip only supports 32 bits addressing. Bits [31:1] must be programmed to 0.

Offset Address: BD-BCh (D3F0-3)

Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** If the Message enable bit (RxB0[16] is set, the contents of this field will be put on bits [15:0] on the data bus for the MSI cycles. Note that the bits [31:16] of the data bus will be 0 during the MSI transaction.

Offset Address: BE-BFh (D3F0-3) – Reserved

Offset Address: C3-C0h (D3F0-3)

Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Mask Bits for Message Vector 31-1** For each mask bit that is set, this root port is prohibited from generating the associated message. This root port only supports 1 message vector. These bits had no function.
0	RW	0	**Mask Bit for Message Vector 0** For each mask bit that is set, this root port is prohibited from generating the associated message. 0: Message vector 0 is allowed to be generated. 1: Message vector 0 will not be generated.

Offset Address: C7-C4h (D3F0-3)

Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Pending Bits for Message Vector 31-1** For each Pending bit that is set, the function had a pending associated message. This root port only supports 1 message vector. These bits had no meaning and should always be 0.
0	RO	0	**Pending Bit for Message Vector 0** For each Pending bit that is set, the function had a pending associated message. 0: There is no message vector 0 pending. 1: There is at least one message vector 0 pending.

Offset Address: C8-DFh (D3F0-3) – Reserved

Subsystem ID and Subsystem Vendor ID Capability Structure Registers (E0-FFh)

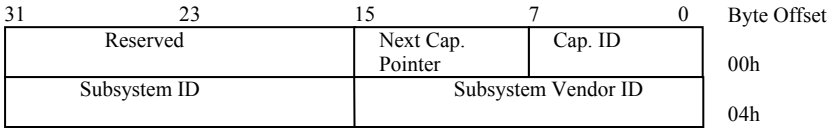


Figure 48. Subsystem Vendor ID & Subsystem ID Capability Structure

Offset Address: E1-E0h (D3F0-3)
Capability ID & Next Pointer **Default Value: 000Dh**

Bit	Attribute	Default	Description
15:8	RO	0	**Next Pointer** This 8 bits register pointed to the next capability that this function claimed. A 0 is the end of the capability list.
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for "Subsystem ID / Subsystem Vendor ID."

Offset Address: E2-E3h (D3F0-3) – Reserved

Offset Address: E5-E4h (D3F0-3)
Subsystem Vendor ID Control **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID** This field identifies the manufacturer of the add-in card or subsystem, it is assigned by PCI-SIG to insure uniqueness. For this chip, it is read only and read as 1106h which is the vendor ID for VIA technologies, Inc.

Offset Address: E7-E6h (D3F0-3)
Subsystem ID Control **Default Value: A410h**

Bit	Attribute	Default	Description
15:0	RO	A410h	**Subsystem ID** This field identifies the particular add-in card or subsystem and is assigned by the vendor. For this chip, it is read only and read as A410h. ***For D3F1:*** The default & the value at "S" field are both B410h. ***For D3F2:*** The default & the value at "S" field are both C410h. ***For D3F3:*** The default & the value at "S" field are both D410h.

Offset Address: E8-FFh (D3F0-3) – Reserved

Device 3 Function 0 (D3F0-3) – PCI Express Root Port Extended Space

Registers defined in this Extended Space are registers with PCI configuration register offset above FFh. Conventional PCI configuration cycles using I/O address CF8h and CFCh can only access up to register offset FFh. This chip implement two other register accessing method called "Extended Configuration Addressing" and "Memory Mapped Configuration Access". Extended Configuration Addressing used I/O address CF8h and CFCh to access, however, with different definition on the layout of the configuration addressing. Memory Mapped Configuration access used certain memory addressing defined in D0F5, Rx61[7:0]

Advanced Error Reporting Capability (100-137h)

Advanced Error Reporting (AER) had the following register structure.

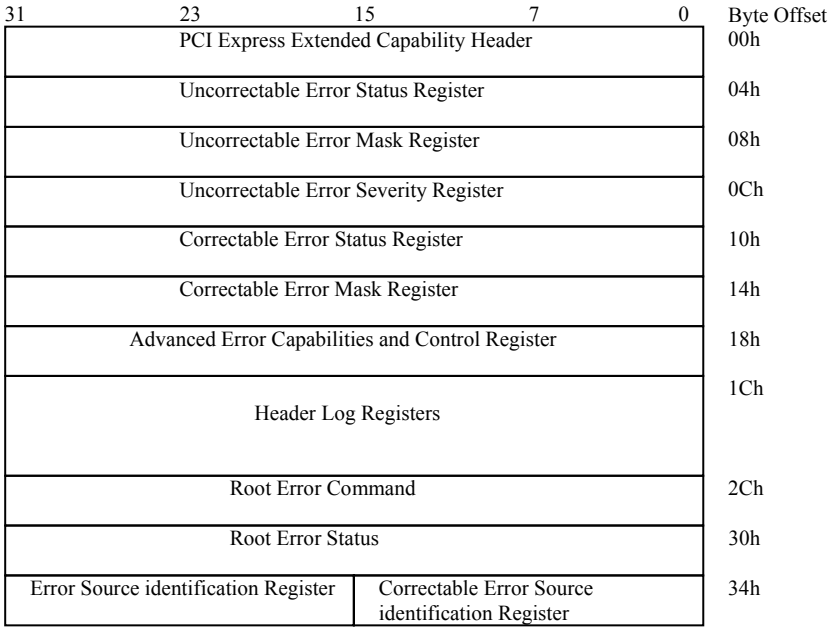


Figure 49. Advanced Error Reporting Register Structure

Offset Address: 103-100h (D3F0-3)

Advanced Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribut	Default	Description
31:20	RO	140h	**Next Capability Offset** These registers pointed to the next capability. This root port had the following capability list: Rx100 (Advanced Error Reporting Capability)->> Rx140 (Virtual Channel Capability) ->> Rx170 (PCI Express Root Complex Link Declaration Capability) ->> Rx190 (ACS [Access Control Service] Extended Capability) ->> Null (End of Capability)
19:16	RO	1h	**Capability Version** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. It must be 1h for this chip.
15:0	RO	0001h	**PCI Express Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. They are 0001h for this Advance Error Reporting (AER) capability.

Offset Address: 107-104h (D3F0-3)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RW1CS	0	**Unsupported Request Error Status (TL) *1** This root port set this bit to 1 when a completion is return with completion status set at 100b for the downstream requests. Writing 1 to this bit clears this bit to 0.
19	RW1CS	0	**ECRC Error Status (TL)** This root port does not support ECRC. This bit is always fixed at 0.
18	RW1CS	0	**Malformed TLP Status (TL)** This root port set this bit to 1 when a TLP received with wrong lengths of header or data payload, unexpected bits combination in the TLP header, or other cases that cannot be recognized as a valid TLP. Writing 1 to this bit clears this bit to 0.
17	RW1CS	0	**Receiver Overflow Status (TL)** When the device connected to this root port issues requests (Posted or Non-posted) over the pre-arranged outstanding number. i.e. the device issued the requests does not follow the Flow Control to keep track the request credits of this root port. Those overflow requests will be discarded. Writing 1 to this bit clears this bit to 0.
16	RW1CS	0	**Unexpected Completion Status (TL) *1** This root port set this bit to 1 when the completion returned for the downstream non-posted cycles with unmatched tag number or when an unexpected completion is received. Writing 1 to this bit clears this bit to 0.
15	RW1CS	0	**Completer Abort Status (TL)** This root port fixed this bit to 0. This root port does not return completion with "Completion Abort" for upstream requests.
14	RW1CS	0	**Completion Timeout Status (TL) *1** This root port set this bit to 1 when the time this root port waits for the completion return from the device for a downstream non-posted cycle exceeds the time defined in Rx1A1[2:0]. Writing 1 to this bit clears this bit to 0.
13	RW1CS	0	**Flow Control Protocol Error Status (TL)** This root port set this bit to 1 when the Flow Control (FC) number this root port kept track is out of synchronization upon the FC updates from the device connected on the root port.
12	RW1CS	0	**Poisoned TLP Status (TL) *1** This root port set this bit to 1 when EP bit in the received TLP header is set. Writing 1 to this bit clears this bit to 0.
11:6	RO	0	**Reserved**
5	RW1CS	0	**Surprise Down Error Status** This bit is set when Surprise Down Error Reporting Capable bit (Rx4C[19] is set and either of the following condition is happened: 1) Physical Layer goes down when the signals on PCIe links of this root port lost the connections. 2) The PCIe Link was programmed to go the L2 or L3 Link Power Management states. 3) Rx3E[6] is programmed to 1. 4) Link Disable bit (Rx50[4] is programmed to 1. 5) Rx1D0[1] is programmed to 1. 6) With Rx54[6] being 1, either Rx54[5] is set or Rx58[10] is programmed to 1. Writing 1 to this bit clears this bit to 0.
4	RW1CS	0	**Data Link Protocol Error Status (DLL)** This root port set this bit to 1 when a Data Link Protocol Error is detected.
3:1	RO	0	**Reserved**
0	RW1CS	0	**Training Error Status (PHY)** This bit is undefined in PCIe-v2.0. However, this root port set this bit to 1 when a Training Error reported from the physical layer. Writing 1 to this bit clears this bit to 0.

*1: Setting of this bit also depends on the corresponding Uncorrectable Error Severity bit (Rx10C), Role-Based Error Reporting bit (Rx44[15]), and Advisory Non-Fatal Error Mask bit (Rx114[13]). The true table is shown in below:

Corresponding Severity Bit	Role-Based Error Reporting bit	Advisory Non-Fatal Error Mask bit	Uncorrectable bit at Rx104, Set or Not Set?
Rx10C	Rx44[15]	Rx114[13]	
1	-	-	Set
0	0	-	Set
0	1	0	Set
0	1	1	Not Set

Offset Address: 10B-108h (D3F0-3)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Mask (TL)** This root port reported Unsupported Request Error to Uncorrectable Error Status register (Rx104) bit[20]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
19	RWS	0	**ECRC Error Mask (TL)** This root port will never report ECRC Error. Setting this bit to 1 will never change the behavior of this chip.
18	RWS	0	**Malformed TLP Mask (TL)** This root port reported Malformed TLP Error to Uncorrectable Error Status register (Rx104) bit[18]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
17	RWS	0	**Receiver Overflow Mask (TL)** This root port reported Receiver Overflow Error to Uncorrectable Error Status register (Rx104) bit[17]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
16	RWS	0	**Unexpected Completion Mask (TL)** This root port reported Unexpected Completion Error to Uncorrectable Error Status register (Rx104) bit[16]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
15	RWS	0	**Completer Abort Mask (TL)** This root port will never report Completer Abort Error. Setting this bit to 1 won't change any behavior of this chip.
14	RWS	0	**Completion Timeout Mask (TL)** This root port reported Completion Timeout Error to Uncorrectable Error Status register (Rx104) bit[14]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
13	RWS	0	**Flow Control Protocol Error Mask (TL)** This root port reported Flow Control Protocol Error to Uncorrectable Error Status register (Rx104) bit[13]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
12	RWS	0	**Poisoned TLP Mask (TL)** This root port reported Poisoned TLP Error to Uncorrectable Error Status register (Rx104) bit[12]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
11:6	RO	0	**Reserved**
5	RWS	0	**Surprise Down Error Mask** This root port reported Surprise Down Error to Uncorrectable Error Status register (Rx104) bit[5]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
4	RWS	0	**Data Link Protocol Error Mask (DLL)** This root port reported Data Link Protocol Error to Uncorrectable Error Status register (Rx104) bit[4]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
3:1	RO	0	**Reserved**
0	RWS	0	**Training Error Mask (PHY)** This bit is undefined in PCIe-v2.0. However, this root port reported Training Error to Uncorrectable Error Status register (Rx104) bit[0]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1

*1: Setting this bit to 1 will not affect the assertion on the corresponding status bit at Rx104, but it will mask the assertion so that the error reporting at Rx4A[2:1], Rx130[6:2], Rx1E[14], Rx06[14] won't reflect this error. Interrupt could be generated when Rx130[6:2] is set and Rx12C[2:1] are programmed to 1.

Offset Address: 10F-10Ch (D3F0-3)

Uncorrectable Error Severity **Default Value: 0006 2031h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Severity (TL)** This root port reported Unsupported Request Error to Uncorrectable Error Status register (Rx104) bit[20]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
19	RWS	0	**ECRC Error Severity (TL)** This bit is used to set the ECRC Error as fatal or non-fatal error. However, this root port will never report ECRC Error. Setting this bit to 1 or 0 will never change the behavior of this chip.
18	RWS	1b	**Malformed TLP Severity (TL)** This root port reported Malformed TLP Error to Uncorrectable Error Status register (Rx104) bit[18]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
17	RWS	1b	**Receiver Overflow Error Severity (TL)** This root port reported Receiver Overflow Error to Uncorrectable Error Status register (Rx104) bit[17]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
16	RWS	0	**Unexpected Completion Error Severity (TL)** This root port reported Unexpected Completion Error to Uncorrectable Error Status register (Rx104) bit[16]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
15	RWS	0	**Completed Abort Error Severity (TL)** This bit is used to set the Completed Abort Error as fatal or non-fatal error. However, this root port will never report Completed Abort Error. Setting this bit to 1 or 0 will never change the behavior of this chip.
14	RWS	0	**Completion Timeout Error Severity (TL)** This root port reported Completion Timeout Error to Uncorrectable Error Status register (Rx104) bit[14]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
13	RWS	1b	**Flow Control Protocol Error Severity (TL)** This root port reported Flow Control Protocol Error to Uncorrectable Error Status register (Rx104) bit[13]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
12	RWS	0	**Poisoned TLP Severity (TL)** This root port reported Poisoned TLP Error to Uncorrectable Error Status register (Rx104) bit[12]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
11:6	RO	0	**Reserved**
5	RWS	1b	**Surprise Down Error Severity** This root port reported Surprise Down Error to Uncorrectable Error Status register (Rx104) bit[5]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
4	RWS	1b	**Data Link Protocol Error Severity (DLL)** This root port reported Data Link Protocol Error to Uncorrectable Error Status register (Rx104) bit[4]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1
3:1	RO	0	**Reserved**
0	RWS	1b	**Training Error Severity (PHY)** This bit is undefined in PCIe-v2.0. However, this root port reported Training Error to Uncorrectable Error Status register (Rx104) bit[0]. Setting this bit to 1/0 will have this root port report this error as fatal/non-fatal error. *1

*1: The fatal or non-fatal errors report to Rx130[6:2], Rx1E[14], Rx06[14] and they could also trigger the generation of interrupt when Rx12C[2:1] is enabled.

Offset Address: 113-110h (D3F0-3)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	RW1CS	0	**Advisory Non-Fatal Error Status** This bit is set to 1 when Rx44[15] (Role-Based Error Reporting) is set 1, and one of the following errors took place: 1) Poisoned TLP 2) Unsupported Request 3) Unexpected Completion Error 4) Completion Timeout Error 5) ECRC Error (this chip does not support ECRC, thus it will never happen) Writing 1 to this bit to clear it to 0.
12	RW1CS	0	**Replay Timer Timeout Status (DLL)** After sending a TLP (Transaction Layer Packets) out, an internal replay timer counts to wait for the return of an ACK to track the TLP transmission. If a NAK is received or an ACK is not received within a certain period of time, the Replay Time, this root port will resend the TLP and set this bit to 1 to notify an acknowledge is lost. The Replay Time is defined as 1 x Replay Timer Limit when the Link of this root port is at L0 (normal) state, and as L0s Replay Count (defined in Rx1B3[2:0]) x Replay Timer Limit when the Link of this root port is at L0s state. The Replay Timer Limit is defined at Rx1BE or Rx1BF depending on the link width (Link Status register, Rx52[8:4]) of this root port. Writing 1 to this bit to clear it to 0.
11:9	RO	0	**Reserved**
8	RW1CS	0	**REPLAY_NUM Rollover Status (DLL)** Replay Timer Timeout status (Bit[12] of this register) is set when the waiting time of the return of an ACK for a TLP transmission exceeds the Replay Time defined in Bit[12] of this register. This root port resent the same TLP and reset its internal replay timer every time when Replay Time is expired or a NAK is received. However, if this root port continues to resend the same TLP for 4 times and still failed to receive the ACK, it will set this bit to 1 and goes into Link Re-train state in which the Link will go through the Link Training just like that had been done during the power on sequence. Writing 1 to this bit clear it to 0.
7	RW1CS	0	**Bad DLLP Status (DLL)** This bit is set when Data Link Layer detected CRC Error for a Data Link Layer Packet (DLLP).
6	RW1CS	0	**Bad TLP Status (DLL)** This bit is set when 1. Data Link Layer (DLL) received a TLP (TLP header + data payload) with CRC errors. 2. The DLLP sequence number precedent to the TLP is larger than this root port expected. In either case, a DLLP NAK is sent to notify for retransmission.
5:1	RO	0	**Reserved**
0	RW1CS	0	**Receiver Error Status (PHY)** This bit is set when Physical Layer 1) Detects an undefined 10 bits Symbol, 2) Elastic Buffers is overflowed (that Symbol caused overflow is discarded) and 3) De-skew mechanism in between different lanes having alignment problem.

Offset Address: 117-114h (D3F0-3)

Correctable Error Mask **Default Value: 0000 2000h**

Bit	Attribute	Default	Description
31:14	RO	0	**Reserved**
13	RWS	1b	**Advisory Non-Fatal Error Mask** This root port reported Advisory Non-Fatal Error to Correctable Error Status register (Rx110) bit[13]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
12	RWS	0	**Replay Timer Timeout Mask (DLL)** This root port reported Replay Timer Timeout Error to Correctable Error Status register (Rx110) bit[12]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
11:9	RO	0	**Reserved**
8	RWS	0	**REPLAY_NUM Rollover Mask (DLL)** This root port reported REPLAY_NUM Rollover Error to Correctable Error Status register (Rx110) bit[8]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
7	RWS	0	**Bad DLLP Mask (DLL)** This root port reported Bad DLLP Error to Correctable Error Status register (Rx110) bit[7]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
6	RWS	0	**Bad TLP Mask (DLL)** This root port reported Bad TLP Error to Correctable Error Status register (Rx110) bit[6]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1
5:1	RO	0	**Reserved**
0	RWS	0	**Receiver Error Mask (PHY)** This root port reported Receiver Error to Correctable Error Status register (Rx110) bit[0]. Setting this bit to 1 to disable the interrupt or error reporting caused by this error. *1

*1: Setting this bit to 1 will not affect the assertion on the corresponding status bit at Rx110, but it will mask the assertion so that the error reporting at Rx130[1:0], won't reflect this error. Interrupt could be generated when Rx130[1:0] is set and Rx12C[0] is programmed to 1.

Offset Address: 11B-118h (D3F0-3)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RO	0	**Reserved**
8	RWS	0	**ECRC Check Enable (TL)** This root port does not support ECRC checking, writing 1 or 0 to this bit does not change the behavior of this chip.
7	RO	0	**ECRC Check Capable (TL)** This root port does not support ECRC checking, this bit is always read 0.
6	RWS	0	**ECRC Generation Enable (TL)** This root port does not support ECRC generation, writing 1 or 0 to this bit does not change the behavior of this chip.
5	RO	0	**ECRC Generation Capable (TL)** This root port does not support ECRC generation, this bit is always read 0.
4:0	ROS	0	**First Error Pointer (TL)** These five bits pointer pointed to the bit in the 32 bits Uncorrectable Error Status (Rx104 ~ Rx107) registers indicating the first uncorrectable error case when there are error bits asserted in Uncorrectable Error status. 00h: The first uncorrectable error is Training Error. 01h~03h: Reserved. These combinations will never happen. 04h: The first uncorrectable error is Data Link Protocol Error. … 20h: The first uncorrectable error is Unsupported Request Error. 21h ~ 1Fh: Reserved. These combination will never happen. These bits will not be updated until the status bit it pointed to in the Uncorrectable Error Status registers (Rx104 ~ Rx107) is cleared.

Offset Address: 11F-11Ch (D3F0-3)
Header Log 1st Register DW **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	ROS	0	**Header Log Register - 1st DW** When the First Error Pointer is updated for logging the first uncorrectable error case happened to this root port, this register is also updated for the header information of the packet which caused the error. The header information is stored as bits [31:0] = {Header byte 0, Header type 1, Header type 2, Header byte 3}. This field will not be updated until the status bit pointed by First Error Pointer of the Uncorrectable Error Status register at Rx118[4:0] is cleared.

Offset Address: 123-120h (D3F0-3)
Header Log 2nd Register DW **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	ROS	0	**Header Log Register - 2nd DW** Please refer to the descriptions of Rx11C, these bits are for the second DW of the header information logged. The header information is stored as bits[31:0] = {Header byte 4, Header byte 5, Header byte 6, Header byte 7}.

Offset Address: 127-124h (D3F0-3)
Header Log 3rd Register DW **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	ROS	0	**Header Log Register - 3rd DW** Please refer to the descriptions of Rx11C, these bits are for the third DW of the header information logged. The header information is stored as bits [31:0] = {Header byte 8, Header byte 9, Header byte 10, Header byte 11}.

Offset Address: 12B-128h (D3F0-3)
Header Log 4th Register DW **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	ROS	0	**Header Log Register - 4th DW** Please refer to the descriptions of Rx11C, these bits are for the fourth DW of the header information logged. The header information is stored as bits[31:0] = {Header byte 12, Header byte 13, Header byte 14, Header byte 15}.

Offset Address: 12F-12Ch (D3F0-3)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable** This bit is set to 1 to enable the interrupt generation *1 when the Fatal Error Messages Received bit, bit[6] of Root Error Status register at Rx130 is set. 0: Disable 1: Enable
1	RW	0	**Non-Fatal Error Reporting Enable** This bit is set to 1 to enable the interrupt generation *1 when the Non-Fatal Error Messages Received bit, the bit[5] of Root Error Status register at Rx130 is set. 0: Disable 1: Enable
0	RW	0	**Correctable Error Reporting Enable** This bit is set to 1 to enable the interrupt generation *1 when either of the Correctable Error Received or Multiple Correctable Errors Received , bit[1:0] of Root Error Status register at Rx130 is set. 0: Disable 1: Enable

*1: The interrupt this root port (RP0) generated is guarded by MSI Enable bit at RxB0[16] and then connected to IRQ3 (IRQ7 for RP1, IRQ11 for RP2, and IRQ15 for RP3) of the APIC controller (APICX) in the NB Module.

Offset Address: 133-130h (D3F0-3)

Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Advanced Error Interrupt Message Number (TL)** These registers indicate which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this capability. For MSI, the value in this register indicates the offset between the base Message Data and the interrupt message that is generated. Please refer to PCIe specification rev2.0 for more details. This root port does not implemented multiple MSI, this field is always read as 0.
26:7	RO	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)** This bit is set when one or more ERR_FATAL (Fatal Error) Messages had been received or one or more errors defined at Rx104[31:0] *1 are set while their corresponding mask bits at Rx108[31:0] are not set, and their corresponding severity bit at Rx10C[31:0] is set. Writing 1 to clear this bit to 0.
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)** This bit is set when one or more ERR_NONFATAL (Non-Fatal Error) Messages had been received or one or more errors defined at Rx104[31:0] *1 are set while their corresponding mask bits at Rx108[31:0] are not set, and their corresponding severity bit at Rx10C[31:0] is not set. Writing 1 to clear this bit to 0.
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** This bit is set to 1 when the first Uncorrectable Error Message received is for a Fatal Error. Writing 1 to clear this bit to 0.
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)** This bit is set when another ERR_FATAL (Fatal Error) or ERR_NONFATAL (Non-Fatal Error) Message is received again or uncorrectable error events of this root port happened again before Uncorrectable Error Received bit at Bit2 of this register is cleared. Writing 1 to clear this bit to 0.
2	RW1CS	0	**ERR_FATAL/NONFATAL Received (TL)** This bit is set when either a ERR_FATAL (Fatal Error) or ERR_NONFATAL (Non-Fatal Error) Message is received or one of the bits in Uncorrectable Error Status register at Rx104[31:0] is set while its corresponding mask bit at Rx108[31:0] is not set. Writing 1 to clear this bit to 0.
1	RW1CS	0	**Multiple Correctable Error Message Received (TL)** This bit is set when another ERR_COR (Correctable Error) Message is received again or correctable error events of this root port happened again before Correctable Error Received bit at Bit0 of this register is cleared. Writing 1 to clear this bit to 0.
0	RW1CS	0	**Correctable Error Message Received (TL)** This bit is set when a ERR_COR (Correctable Error) Message is received or any of the bits in Correctable Error Status register at Rx110[31:0] is set while its corresponding mask bit at Rx114[31:0] is not set. Advisory Non-Fatal Error (Rx110[13]) *1 will also be reported to this bit when Role-Based Error reporting (Rx44[15]) is set to 1 and Advisory Non-Fatal Error Mask (Rx114[13]) is set to 0. Writing 1 to clear this bit to 0.

*1: Some Uncorrectable Error in Rx104: Unsupported Request Error (Rx104[20]), ECRC Error (Rx104[19]), Unexpected Completion Error (Rx104[16]), Completion Timeout Error (Rx104[14]), and Poisoned TLP Error (Rx104[12]) can be reported to Fatal Error (Rx130[6]), Non-Fatal Error (Rx130[5]) or Correctable Error (Rx130[0]) depending on the corresponding severity bits at Rx10C, the Role-Based Error reporting (Rx44[15]), and the advisory non-fatal error mask (Rx114[13]). Please refer to the table below:

Corresponding Severity Bit	Role-Based Error Reporting bit	Advisory Non-Fatal Error Mask bit	Fatal Error Received bit at Rx130[6] set or not set?	Non-Fatal Error Received bit at Rx130[5], Set or Not Set?	ERR_COR Received at Rx130[0] set or not set?
Rx10C	Rx44[15]	Rx114[13]			
1	-	-	Set	Not Set	Not Set
0	0	-	Not Set	Set	Not Set
0	1	0	Not Set	Not Set	Set
0	1	1	Not Set	Not Set	Not Set

Offset Address: 137-134h (D3F0-3)

Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	ROS	0	**ERR_FATAL / NONFATAL Source Identification (TL)** This field stored the 16 bits Request ID indicated in the received ERR_FATAL (Fatal Error) or ERR_NONFATAL (Non-Fatal Error) Message when bit2 of Root Error Status register is setting to 1. If the assertion of bit2 of the Root Error Status register at Rx130 is caused by the root port internal uncorrectable errors, this field is read as {Bus#, Device#, Function#} for this root port RP0 which is 0018h (0019h for RP1, 001Ah for RP2, 001Bh for RP3).
15:0	ROS	0	**ERR_COR Source Identification (TL)** This field stored the 16 bits Requester ID indicated in the received ERR_COR (Correctable Error) Message when bit0 of Root Error Status register is setting to 1. If the assertion of bit0 of the Root Error Status register at Rx130 is caused by the root port internal correctable errors, this field is read as {Bus#, Device#, Function#} for this root port RP0 which is 0018h (0019h for RP1, 001Ah for RP2, 001Bh for RP3)..

Offset Address: 13B-138h (D3F0-3)

Error DLLP Log **Default Value: 0000 0000h**

Bit	Attribut	Default	Description
31:0	ROS	0	This field logged the whole 32 bits DLLP (Data Link Layer Packet) when the Bad DLLP status bit (bit[7]) in Correctable Error Status (Rx110) register is set.

Offset Address: 13C-13Fh (D3F0-3) – Reserved

Virtual Channel Capability (140-167h)

Virtual Channel Capability is defined for Egress direction of the PCIe device. For Root Port, only VC0 is defined.

- VC0 mapping: TC0, TC1, TC2, TC3, TC4, TC5, TC6, TC7
- No VC arbitration table
- No port arbitration table

It thus has the following structure started from Rx140.

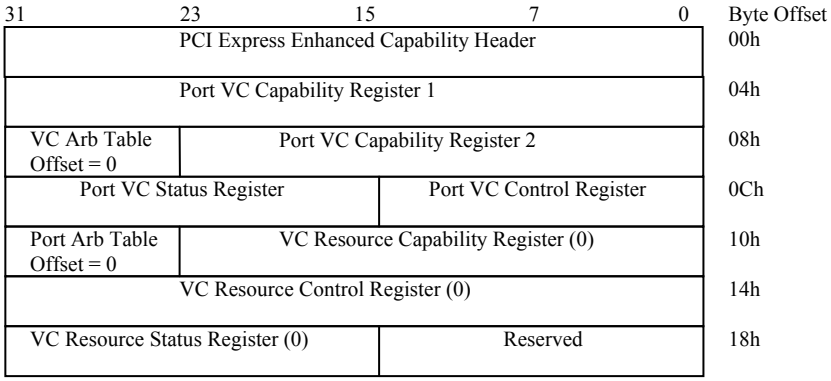


Figure 50. PCI Express Virtual Channel Capability Register Structure

Offset Address: 143-140h (D3F0-3)

Virtual Channel Enhanced Capability **Default Value: 1701 0002h**

Bit	Attribute	Default	Description
31:20	RO	170h	**Next Capability Offset** These registers pointed to the next capability. This root port had the following capability list: Rx100 (Advanced Error Reporting Capability)-> Rx140 (Virtual Channel Capability) -> Rx170 (PCI Express Root Complex Link Declaration Capability) -> Rx190 (ACS [Access Control Service] Extended Capability) -> Null (End of Capability)
19:16	RO	1h	**Capability Version** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. It must be 1h for this chip.
15:0	RO	0002h	**PCI Express Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. They are 0002h for his Virtual Channel Capability.

Offset Address: 147-144h (D3F0-3)
Port VC Capability 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** This field indicates the size (in bits) of Port Arbitration table entry in the function. This field is valid for root ports that support peer-to-peer traffic. 00: 1 bits 01: 2 bits 10: 4 bits 11: 8 bits This root port of this chip does support peer-to-peer traffic, but it does not use this field to do the port arbitration. The arbitration for peer-to-peer traffic in this chip is done by using Occupancy and Promote Timer for RP0, RP1, RP2, RP3, and conventional SB block. Please refer to register descriptions at RX270~RX27F for RCRB-H.
9:8	RO	0	**Reference Clock** This field indicates the reference clock for Virtual Channels that support time-based WRR (Weighted Round Robin) port arbitration. 00: 100ns reference clock 01,10, 11: Reserved This field is fixed at 00b for this root port.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count** This field indicates the number of extended Virtual Channels in addition to the default VC belonging to the low-priority VC group that has the lowest priority with respect to other VC resources in a strict priority VC arbitration. This root port does not support extended VC, only VC0 is supported.
3	RO	0	**Reserved**
2:0	RO	0	**Extended VC Count** This filed indicates the number of Extended Virtual Channels in addition to the default VC supported by the device. 000: No extended VC supported 001: 1 extended VC supported .. 111: 7 extended VC supported This root port does not support extended VC, only VC0 is supported.

Offset Address: 14B-148h (D3F0-3)
Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** This field indicates the location of the VC arbitration table. It contains the zero-based offset of the table in Double QW (16 bytes) from the base address of the Virtual Channel Capability structure. A value of 0 indicates that the table is not present. This root port only support VC0 egress (downstream traffic). This field is thus always 0.
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability** This field indicates the types of VC arbitration supported by this function. Each bits location within this field corresponds to a VC Arbitration Capability defined below. When more than 1 bit in this field is set, it indicates that the port can be configured to provide different VC arbitration services. Defined bit position are: Bit [0]: Hardware fixed arbitration scheme, e.g. Round Robin. Bit [1]: Weighted Round Robin (WRR) arbitration with 32 phases. Bit [2]: WRR arbitration with 64 phases. Bit [3]: WRR arbitration with 128 phases. Bits [4:7]: Reserved. This field is always fixed at 00h since this root port only support VC0 egress (downstream traffic). The extended VC count of this root port reported at Rx144[2:0] is 0.

Offset Address: 14D-14Ch (D3F0-3)

Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RW	0	**VC Arbitration Select** This filed is used for software to configure the VC arbitration by selecting one of the supported VC Arbitration schemes indicated by the VC Arbitration Capability field in the Port VC Capability Register 2. The value of this field is the number corresponding to one of the asserted bits in the VC Arbitration Capability field. i.e. 000: Hardware fixed arbitration scheme, e.g. Round Robin. 001: Weighted Round Robin (WRR) arbitration with 32 phases. 010: WRR arbitration with 64 phases. 011: WRR arbitration with 128 phases. 1xx : Reserved. This root port supports only VC0 egress (downstream traffic). No matter what value this field is programmed, the root port will have no impact on its egress traffic.
0	RO	0	**Load VC Arbitration Table** This bit is used by software to update the VC arbitration table. Software sets this bit to request hardware to apply new values programmed into VC Arbitration Table; clearing this bit has no effect. Software checks the VC Arbitration Table status bit (bit0 of Port VC status at Rx14E[0]) to confirm that new values stored in the VC Arbitration Table are latched by the VC arbitration logic. This root port does not have VC arbitration table, it is always 0.

Offset Address: 14F-14Eh (D3F0-3)

Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** This bit indicates the coherency status of the VC Arbitration Table. It is set by hardware when any entry of the VC Arbitration Table is written by software. This bit is cleared by hardware when hardware finishes loading values stored in the VC Arbitration Table after software sets the Load VC Arbitration Table field in the Port VC Control register (Rx14C[0]). This root port does not have VC arbitration table, it is always 0.

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F0-3)

VC0 Resource Capability **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset** This field indicates the location of the Port Arbitration Table associated with this VC resource (VC0). It contains the zero-based offset of the table in Double QW (16 bytes) from the base address of the Virtual Channel Capability structure. This root port's VC0 (the only VC of this root port) does not have a port arbitration associated with this field. A 00h is returned when a read is issued to this registers. Please refer to descriptions at bit[11:10] of the Port VC capability 1 (Rx144[11:10]) for more information.
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots** This field indicates the maximum number of time slots (minus one) that the this VC resource (VC0) is capable of supporting when it is configured for time-based WRR (Weighted Round Robin) Port Arbitration. 00h: Max. Time slot = 1 01h: Max. Time slot = 2 02h: Max. Time slot = 3 03h: Max. Time slot = 4 … 7Eh: Max. Time slot = 127 7Fh: Max. Time slot = 128 This root port does not have a port arbitration associated with this registers. It is always returned 00h when a read is issued to this registers.
15	RO	0	**Reject Snoop Transactions** This field is to indicate how the TLP request with "No Snoop" attribute being set is treated by this VC (VC0). 0: The transaction with or without the No Snoop bit set within the TLP header are allowed on this VC (VC0). 1: Any transaction for which the No Snoop attribute is applicable but is not set within the TLP header is permitted to be rejected as an Unsupported Request.
14	RO	0	**Undefined** In early versions (earlier than revision 1.1) of the PCIe specification, this bit is defined as Advanced Packet Switching (AS). When it is set, it was defined that this VC (VC0) only supports transactions optimized for Advanced Packet Switching. It is always read as 0.
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** This field indicates the types of Port Arbitration supported by this VC (VC0). Each bit location within this field corresponds to a Port Arbitration Capability defined below. When more than 1 bit in this field is set, it indicates that this VC (VC0) can be configured to provide different arbitration services. Software selects among these capabilities by writing to the Port Arbitration Select field (Rx154[19:17]). Defined bit positions are: Bit [0]: Hardware fixed arbitration scheme, e.g. Round Robin. Bit [1]: Weighted Round Robin (WRR) arbitration with 32 phases. Bit [2]: WRR arbitration with 64 phases. Bit [3]: WRR arbitration with 128 phases. Bit [4]: Time-based WRR with 128 phases. Bit [5]: WRR arbitration with 256 phases. Bits [6:7]: Reserved. This root port's VC0 (the only VC of this root port) does not have a port arbitration associated with this field. A 00h is returned when a read is issued to this registers. Please refer to descriptions at bit[11:10] of the Port VC capability 1 (Rx144[11:10]) for more information.

Offset Address: 157-154h (D3F0-3)

VC0 Resource Control **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable** This bit is to enable this VC (VC0). 0: Disabled 1: Enabled VC0 is the only VC this root port had. It is always enabled.
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID** This field is to assign a VC ID to this VC resource (VC0). Since this bits are for the first VC (the default VC), the VC0, this field is read-only and hardwired to 000b.
23:20	RO	0	**Reserved**
19:17	RW	0	**Port Arbitration Select** This field configures the VC resource to provide a particular Port Arbitration service. The permissible value of this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of this VC (VC0) resource (Rx150[7:0]). This root port's VC0 (the only VC of this root port) does not have a port arbitration associated with this field. Please refer to descriptions at bit[11:10] of the Port VC capability 1 (Rx144[11:10]) for more information. Writing anything to these bits does not change the behavior of this VC (VC0).
16	RO	0	**Load Port Arbitration Table** When set, this bit updates the Port Arbitration logic from the Port Arbitration Table for this VC resource (VC0). Software sets this bit to signal hardware to update Port Arbitration logic with new values stored in Port Arbitration Table (Bit[19:17] of this register). Software uses the Port Arbitration Status bit (Rx158[16]) to confirm whether the new values of Port Arbitration Table are completely latched by the arbitration logic. This root port's VC (VC0) does not implement Port Arbitration associated with this register. Please refer to descriptions at bit[11:10] of the Port VC capability 1 (Rx114[11:10]) for more information. This bit is Read Only and must return 0 when read.
15:8	RO	0	**Reserved**
7:1	RW	7Fh	**TC/VC Map** This field indicates the TCs (Traffic Class) that are mapped to this VC (VC0). Bit locations within this field correspond to TC values. E.g. when bit7 is set, TC7 is mapped to this VC (VC0). When more than 1 bit in this field is set, it indicates that multiple TCs are mapped to this VC (VC0). This root port only had one VC (this VC0). No matter what the values are set here, all the TCs will be mapped to VC0.
0	RO	1b	**TC/VC Mapping for TC0** As described in Bit[7:1], this bit indicates the mapping of TC0 to this VC (VC0). This bit for TC0 has to be set for this VC (VC0). This bit is read only and is read as 1.

Offset Address: 15B-158h (D3F0-3)

VC0 Resource Status **Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	HwInit	**VC Negotiation Pending** This bit indicates whether the Virtual Channel negotiation (initialization or disabling) for this VC (VC0) is in pending state. The value of this bit is defined only when the Link is in DL_Active state and the Virtual Channel is enabled (the VC enable bit, Rx154[31], is set). 0: Negotiation is complete 1: Negotiation is on-going The default value of this bit depends on the existence of the device connecting to this root port. This bit is 1 after the power is applied to this chip. And it will become 0 if the root port finished the VC0 credit initialization with the device connected to it. It will remain at 1 if there is no device connected to it, or the VC0 credit initialization cannot be finished successfully.
16	RO	0	**Port Arbitration Table Status** This bit indicates the coherency status of the Port Arbitration Table associated with this VC (VC0) resource. This bit is defined being set by hardware when any entry of the Port Arbitration Table is written to by software and being cleared by hardware when hardware finishes loading values stored in the Port Arbitration Table. This root port does not implement Port Arbitration mechanism associated with this registers. Instead, this chip uses another arbitration mechanism as described in Rx144[11:10]. This bit is always read as 0.
15:0	RO	0	**Reserved**

Offset Address: 15C-16Fh (D3F0-3) – Reserved

PCI Express Root Complex Link Declaration Capability (170-18Bh)

PCI express Root Complex Link Declaration capability has the following register structure. There are Root Complex Link Declaration Capabilities existed in D3F0, D3F1, D3F2, D3F3, D20F0, and RCRB-H. They are used to describe the Link topology within the chip

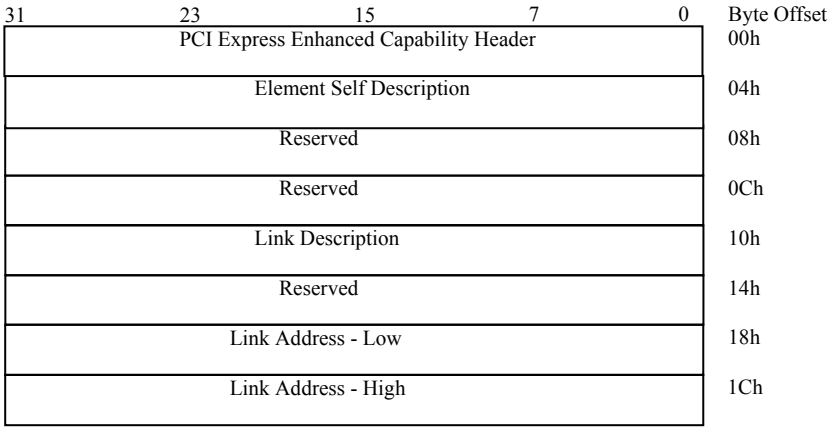


Figure 51. PCI Express Root Complex Link Declaration Capability

Offset Address: 173-170h (D3F0-3)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability Offset** These registers pointed to the next capability. This root port had the following capability list: Rx100 (Advanced Error Reporting Capability)->>br>Rx140 (Virtual Channel Capability) ->>br>Rx170 (PCI Express Root Complex Link Declaration Capability) ->>br>Rx190 (ACS [Access Control Service] Extended Capability) ->>br>Null (End of Capability)
19:16	RO	1h	**Capability Version** This field is a PCI-SIG defined version number that indicates the version of the Capability structure present. It must be 1h for this chip.
15:0	RO	0005h	**PCI Express Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the nature and format of the Extended Capability. They are 0005h for the Root Complex Link Declaration Capability.

Offset Address: 177-174h (D3F0-3)

Element Self Description **Default Value: 0101 0100h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Port Number** This field specifies the Port Number associated with this element with respect to the Root Complex Component that contains this element. An element with a Port Number of 00h indicates the default Egress Port to configuration software. This root port (RP0) declare itself the Port 01h of the Root Complex which is described at RCRB-H. ***For D3F1:*** The default value is 02h. RP1 is the Port 02h of the RCRB-H. ***For D3F2:*** The default value is 03h. RP2 is the Port 03h of the RCRB-H. ***For D3F3:*** The default value is 04h. RP3 is the Port 04h of the RCRB-H.
23:16	RO	01h	**Component ID** This field indentifies the Root Complex Component that contains this Root Complex Element. This root port (RP0) reports itself as the Root Complex Component which described at RCRB-H. ***For D3F1:*** This field is also 01h, RP1 also reports itself as the Root Complex which described at RCRB-H. ***For D3F2:*** This field is also 01h, RP2 also reports itself as the Root Complex which described at RCRB-H. ***For D3F3:*** This field is also 01h, RP3 also reports itself as the Root Complex which described at RCRB-H.
15:8	RO	01h	**Number of Link Entries** This field indicates the number of Link entries following the Element Self Description. 00h: Invalid 01h: 1 Link Entry 02h: 2 Link Entries … FFh: 255 Link Entries This root port (RP0) has one Link entry associated with this element. ***For D3F1:*** This field is also 01h. RP1 also has only one link entry. ***For D3F2:*** This field is also 01h. RP2 also has only one link entry. ***For D3F3:*** This field is also 01h. RP3 also has only one link entry.
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** This field indicates the type of the Root Complex Element. 0h: Configuration Space Element. 1h: System egress port or internal sink (memory). 2h: Internal Root Complex Link. 3-15h: Reserved. This root port (RP0) reports 0h and has a configuration space as the root complex element. ***For D3F1:*** This field is also 0h. RP1 also reports this element as a configuration space. ***For D3F2:*** This field is also 0h. RP2 also reports this element as a configuration space. ***For D3F3:*** This field is also 0h. RP3 also reports this element as a configuration space.

Offset Address: 178-17Fh (D3F0-3) – Reserved

Offset Address: 183-180h (D3F0-3)

Link Description **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO)	01h	**Target Port Number** This field specifies the Port Number associated with the element targeted by this link entry; the target Port Number is with respect to the Root Complex Component (identified by the Target Component ID) that contains the target element. It specifies the target port # of this root port in the Root Complex structure. It should be 00h for the Root Complex described at RCRB-H.
23:16	RO	01h	**Target Component ID** This field identifies the Root Complex Component that is targeted by this Link entry. Components IDs must start at 01h, as a value of 00h is reserved. The target component of this root port is the Root Complex described at RCRB-H. Thus, this field is 01h. ***For D3F1:*** This field is also 01h. The Root Complex described at RCRB-H is the target component for RP1. ***For D3F2:*** This field is also 01h. The Root Complex described at RCRB-H is the target component for RP2. ***For D3F3:*** This field is also 01h. The Root Complex described at RCRB-H is the target component for RP3.
15:3	RO	0	**Reserved**
2	RO	0	**Associate RCRB Header** When Set, this bit indicates that the Link Entry associates the declaring element with an RCRB Header Capability in the target RCRB. Link entries that do not have either this bit Set or the Link Valid bit Set (or both) are ignored by software. The Link Type bit must be Clear when this bit is Set. The RCRB-H (target RCRB of this root port (RP0)) does not have the "RCRB Header Capability. This bit is 0b. ***For D3F1:*** It is also 0b for the same reason above. ***For D3F2:*** It is also 0b for the same reason above. ***For D3F3:*** It is also 0b for the same reason above.
1	RO	0	**Link Type** This bit indicates the target type of the Link and defines the format of the Link address field (Rx188~Rx18F). 0: Link points to memory-mapped space (for RCRB). The Link address specifies the 64-bit base address of the target RCRB. 1: Link points to Configuration Space (for a root port or root complex integrated Endpoint). The Link address specifies the configuration address (PCI Segment Group, Bus, Device, Function) of the target element. This bit is 0. Root port (RP0) points to the RCRBH using memory mapped address A[35:12] which can be programmed at D0F5, Rx68[23:0]. ***For D3F1:*** This bit is also 0. RP1 points to the RCRBH using memory mapped address defined at D0F5, Rx68[23:0]. ***For D3F2:*** This bit is also 0. RP2 points to the RCRBH using memory mapped address defined at D0F5, Rx68[23:0]. ***For D3F3:*** This bit is also 0. RP3 points to the RCRBH using memory mapped address defined at D0F5, Rx68[23:0].
31:24	RO	0	**Target Port Number** This field specifies the Port Number associated with the element targeted by this link entry; the target Port Number is with respect to the Root Complex Component (identified by the Target Component ID) that contains the target element. It specifies the target port # of this root port in the Root Complex structure. It should be 00h for the Root Complex described at RCRB-H.

Offset Address: 184-187h (D3F0-3) – Reserved

Offset Address: 18B-188h (D3F0-3)

Lower Link Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Lower Link Address – Bits [31:12]** The Link Type of the Link specified by the Root Complex Capability register of this root port (RP0) is 0. Thus, the Link Address is a memory-mapped RCRB address. For this chip, the RCRB pointed by this Link can be addressed by the registers defined at D0F5, Rx68[23:0].
11:0	RO	0	**Lower Link Address – Bits [11:0]** As defined in bit[31:12], this chip's RCRB address bit[11:0] is fixed at 0.

Offset Address: 18F-18Ch (D3F0-3)

Upper Link Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Upper Link Address – Bits [63:36]**
3:0	RO	0	**Upper Link Address – Bits [35:32]** As described in Rx188[31:12], this field defined the upper address bit[35:32] of the RCRB of this chip. And they are defined at D0F5, Rx68[23:20].

Offset Address: 190-19Fh (D3F0-3) – Reserved

PCI Express Transaction Layer Registers (1A0-1A8h)

Offset Address: 1A0h (D3F0-3)

Downstream Control 1 **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command.
2:1	RW	0	**Reserved** Writing 1 or 0 to these bits does not change behaviors of this chip.
0	RW	1b	**Downstream Pipeline** 0: Disabled 1: Enabled

Offset Address: 1A1h (D3F0-3)

Downstream Control 2 **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW1C	0	**Reserved** Writing 1 or 0 to these bits does not change behaviors of this chip.
6	RW	0	**Reserved** Writing 1 or 0 to these bits does not change behaviors of this chip.
5	RW	0	**For the Data Return of Upstream Read Requests** 0: The chip always checks CPL credit unless the endpoint advertises infinite CPL credits. 1: The chip does not check CPL credit even when endpoint advertises finite CPL credits.
4	RW	1b	**Transaction Layer Downstream Does Not Check Downstream PH Credit for PME_TURN_OFF Message as the PCIe V1.1 Spec requirement** 0: Disable 1: Enable
3	RW	0	**Downstream Read Completion Timeout Period for Test Mode** This bit is enabled only at chip production test mode. It changed the downstream read completion timeout period defined at bits [2:0] of this register. 0: Disabled 1: Enabled
2:0	RW	010b	**Downstream Read Completion Timeout Period** These bits define the time limit for the completion returned from the device for a downstream read cycle. If this root port does not receive the completion packets from the device within the timeout period defined by these bits, it will return FFFF_FFFFh back to the CPU. However, if bit4 of the Device Control 2 register (Rx68[4]) is 1, this timeout feature is disabled, and the timeout period will become infinity. 000: 1ms. 001: 10ms. 010: 30ms. 011: 50ms. 100: 100ms. 101: 200ms. 110: 500ms. 111: 1s. PCIe specification suggested that the minimum timeout period is 10ms. When bit[3] of this register is set to 1, the timeout period defined above becomes: 000: 1us. 001: 3us. 010: 10us . 011: 20us. 100: 50us. 101: 100us. 110: 200us. 111: 500us.

Offset Address: 1A2h (D3F0-3)

Downstream Control 3 **Default Value: 38h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Ordering Queue Timing Option** 0: 1T setup time 1: 2T setup time If Root Complex is connected to PCIe Endpoint, there is no problem. Because PCIe spec requires Endpoint CPL credits to be infinite. But if Root Complex is connected to PCIe Switch, the CPL credits are finite. This may cause ERROR and need to change this bit to 1.
6:4	RW	011b	**Waiting for GNT Timer for Priority Arbitration Mode** 000: 1T 001: 4T 010: 8T 011: 16T 100: 24T 101: 32T 110: 64T 111: 128T If GNT timer of VC0/C2P request expires, VC0/C2P request will become higher priority. Priority VC1 > VC0 > C2P request when Rx1A0[3] = 0
3	RW	1b	**Enable Fast Reorder** 0: 2T latency 1: 1T latency that reordering buffer push/pop at the same time
2	RW	0	**Pending C2P NP Completion Cycle to Block L1 Entry** 0: Disable. L1 entry does not wait for C2P NP completion. 1: Enable. L1 entry waits for C2P NP completion.
1:0	RW	00b	**Downstream Arbitration Parking** 00: GNT parks on the last request source. 01: GNT parks on VC1 completion. If VC1 is not enabled (or no VC1), park on VC0 completion. 10: GNT parks on VC0 completion. 11: GNT parks on C2P request.

Offset Address: 1A3h (D3F0-3)

Downstream Control 4 (D3F0) **Default Value: F8h**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Retry Buffer Level** 0000: 2-level 0001: 4-level 0010: 6-level 0011: 8-level 0100: 10-level 0101: 12-level 0110: 14-level 0111: 16-level 1000: 18-level 1001: 20-level 1010: 22-level 1011: 24-level 1100: 26-level 1101: 28-level 1110: 30-level 1111: 32-level
3	RW	1b	**Downstream Read Retry Time Out Control in DL_Down State** 0: Disable downstream read retry time out. If bit 0 is set to 1, downstream read request will always wait for DL_DLUp assertion then retry. 1: Enable downstream read retry time out. The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion.
2:1	RW	0	**Reserved**
0	RW	0	**Downstream Read Cycle Retry** 0: When DL_DOWN is asserted, transaction layer returns "FF" to Central Traffic Controller for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle. This incompletes C2P read cycle will be retried when DL_UP is asserted.

Note:
DL_DLUp: Link layer signal which means PCIe link is OK for TLP transmission.
DL_DOWN: Link layer signal which means PCIe link is not ready for TLP transmission.
DL_UP: Link layer signal which means PCIe link is OK for TLP transmission.

Downstream Control 4 (D3F1,D3F2,D3F3) **Default Value: 78h**

The differences between D3F1-3 and D3F0 are the bit descriptions of bits [7:4, 1].

Bit	Attribute	Default	Description
7:4	RW	0111b	**Retry Buffer Level** Bit 7: Read only 0000: 1-level 0001: 2-level 0010: 3-level 0011: 4-level 0100: 5-level 0101: 6-level 0110: 7-level 0111: 8-level 1xxx: Reserved
3	RW	1b	**Downstream Read Retry Time Out Control in DL_Down State** 0: Disable downstream read retry time out. If bit 0 is set to 1, downstream read request will always wait for DL_DLUp assertion then retry. 1: Enable downstream read retry time out. The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion.
2:1	RW	0	**Reserved**
0	RW	0	**Downstream Read Cycle Retry** 0: When DL_DOWN is asserted, transaction layer returns "FF" to Central Traffic Controller for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle. This incompletes C2P read cycle will be retried when DL_UP is asserted.

Offset Address: 1A4h (D3F0-3)

Upstream Control **Default Value: 19h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35-A31 Forced to 0** 0: Disabled 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory.
6	RW	0	**Reserved**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" and "Over 4K Boundary Rule"** 0: Disable 1: Enable
4	RW	1b	**Downstream Read Wait till the Upstream Write Data Flushed** 0: Disable 1: Enable
3	RW	1b	**Infinite Flow Control** 0: Advertise credits 2, 4, 1 for CPLH, CPLD, NPD (4DWs as the units), update credits when device responds normally. 1: CPLH & CPLD & NPD become infinite mode.
2	RW	0	**Reserved**
1	RW	0	**VC1 Request Queue Usage** (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0) 0: Disable through VC1 Request Queue to the Central Traffic Controller. Note. Bit 0 has to be 0 when this bit is set.
0	RW	1b	**Reserved**

Offset Address: 1A5h (D3F0-3)

Credit Advertisement Control 1 (D3F0) **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Upstream Posted (Write) Data FIFO Size and the Initial PD Credit Value** 0000: 1-line upstream write FIFO size, and initial PD credit = 4h 0001: 2-line upstream write FIFO size, and initial PD credit = 8h 0010: 3-line upstream write FIFO size, and initial PD credit = Ch 0011: 4-line upstream write FIFO size, and initial PD credit = 10h 0100: 5-line upstream write FIFO size, and initial PD credit = 14h 0101: 6-line upstream write FIFO size, and initial PD credit = 18h 0110: 7-line upstream write FIFO size, and initial PD credit = 1Ch 0111: 8-line upstream write FIFO size, and initial PD credit = 20h 1000: 9-line upstream write FIFO size, and initial PD credit = 24h 1001: 10-line upstream write FIFO size, and initial PD credit = 28h 1010: 11-line upstream write FIFO size, and initial PD credit = 2Ch 1011: 12-line upstream write FIFO size, and initial PD credit = 30h 1100: 13-line upstream write FIFO size, and initial PD credit = 34h 1101: 14-line upstream write FIFO size, and initial PD credit = 38h 1110: 15-line upstream write FIFO size, and initial PD credit = 3Ch 1111: 16-line upstream write FIFO size, and initial PD credit = 40F
3:0	RW	1111b	**Upstream PH Header Queues Size and the Initial PH Credit** 0000: 1-level PH header queue, and initial PH credit = 2h 0001: 2-level PH header queue, and initial PH credit = 4h 0010: 4-level PH header queue, and initial PH credit = 6h 0011: 8-level PH header queue, and initial PH credit = 8h 0100: 10-level PH header queue, and initial PH credit = Ah 0101: 12-level PH header queue, and initial PH credit = Ch 0110: 14-level PH header queue, and initial PH credit = Eh 0111: 16-level PH header queue, and initial PH credit = 10h 1000: 18-level PH header queue, and initial PH credit = 12h 1001: 20-level PH header queue, and initial PH credit = 14h 1010: 22-level PH header queue, and initial PH credit = 16h 1011: 24-level PH header queue, and initial PH credit = 18h 1100: 26-level PH header queue, and initial PH credit = 1Ah 1101: 28-level PH header queue, and initial PH credit = 1Ch 1110: 30-level PH header queue, and initial PH credit = 1Eh 1111: 32-level PH header queue, and initial PH credit = 20h

Credit Advertisement Control 1 (D3F1-F3) **Default Value: 73h**

Bit	Attribute	Default	Description
7:4	RW	0111b	**Upstream Posted (Write) Data FIFO Size and the Initial PD Credit Value** Bit [7]: Read only 0000: 1-line upstream write FIFO size, and initial PD credit = 4h 0001: 2-line upstream write FIFO size, and initial PD credit = 8h 0010: 3-line upstream write FIFO size, and initial PD credit = Ch 0011: 4-line upstream write FIFO size, and initial PD credit = 10h 0100: 5-line upstream write FIFO size, and initial PD credit = 14h 0101: 6-line upstream write FIFO size, and initial PD credit = 18h 0110: 7-line upstream write FIFO size, and initial PD credit = 1Ch 0111: 8-line upstream write FIFO size, and initial PD credit = 20h 1xxx: Reserved
3:0	RW	0011b	**Upstream PH Header Queues Size and the Initial PH Credit** Bit [3:2]: Read only 0000: 1-level PH header queue, and initial PH credit = 1h 0001: 2-level PH header queue, and initial PH credit = 2h 0010: 4-level PH header queue, and initial PH credit = 4h 0011: 8-level PH header queue, and initial PH credit = 8h 01xx / 1xxx: Reserved

Offset Address: 1A6h (D3F0-3)

Credit Advertisement Control 2 (D3F0) **Default Value: 1Fh**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Non-Posted Header Credit Infinite Mode Control** 0: The non-posted header credit is finite and has to update NPH credits. 1: The non-posted header credit is infinite and not necessary to update NPH credits.
6:4	RW	001b	**Reserved**
3:0	RW	1111b	**Upstream Non-Posted Request Queue Size and Initial NPH Credit Value** 0000: 1-level NPH header queue, and initial NPH credit = 2h 0001: 2-level NPH header queue, and initial NPH credit = 4h 0010: 4-level NPH header queue, and initial NPH credit = 6h 0011: 8-level NPH header queue, and initial NPH credit = 8h 0100: 10-level NPH header queue, and initial NPH credit = Ah 0101: 12-level NPH header queue, and initial NPH credit = Ch 0110: 14-level NPH header queue, and initial NPH credit = Eh 0111: 16-level NPH header queue, and initial NPH credit = 10h 1000: 18-level NPH header queue, and initial NPH credit = 12h 1001: 20-level NPH header queue, and initial NPH credit = 14h 1010: 22-level NPH header queue, and initial NPH credit = 16h 1011: 24-level NPH header queue, and initial NPH credit = 18h 1100: 26-level NPH header queue, and initial NPH credit = 1Ah 1101: 28-level NPH header queue, and initial NPH credit = 1Ch 1110: 30-level NPH header queue, and initial NPH credit = 1Eh 1111: 32-level NPH header queue, and initial NPH credit = 20h

Credit Advertisement Control 2 (D3F1-F3) **Default Value: 13h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Non-Posted Header Credit Infinite Mode Control** 0: The non-posted header credit is finite and has to update NPH credits. 1: The non-posted header credit is infinite and not necessary to update NPH credits.
6:4	RW	001b	**Reserved**
3:0	RW	0011b	**Upstream Non-Posted Request Queue Size and Initial NPH Credit Value** Bit [3:2]: Read only 0000: 1-level NPH header queue, and initial NPH credit = 1h 0001: 2-level NPH header queue, and initial NPH credit = 2h 0010: 4-level NPH header queue, and initial NPH credit = 4h 0011: 8-level NPH header queue, and initial NPH credit = 8h 01xx / 1xxx: Reserved

Offset Address: 1A7h (D3F0-3)

Upstream Performance Control 1 **Default Value: C4h**

Bit	Attribute	Default	Description
7:6	RW	11b	**Reserved**
5	RW	0	**Reserved**
4	RW	0	**Upstream Read FIFO Entry Release Timing** 0: Release upstream read FIFO entry when the last data pop into retry data FIFO. 1: Release upstream read FIFO entry when the first data pop into retry data FIFO.
3	RW	0	**Downstream Read Data Wait for Previous Upstream Write Complete** 0: Disable 1: Enable
2	RW	1b	**Upstream Requests Read and Write Orders** 0: Upstream requests are served in order. 1: Upstream write always pass upstream read.
1	RO	0	**Reserved**
0	RW	0	**Reserved**

Offset Address: 1A8h (D3F0-3)

Completion Timeout Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**C2P Completion Timeout Method When PHY Retrains or Configures** 0: Keep the timeout value 1: Reset the timeout value
6	RW	0	**Reserved**
5:4	RW	01b	**Configuration Request Timeout Timer** 00: 100ms 01: 500ms 10: 1000ms 11: 1500ms
3:2	RW	0	**Reserved**
1:0	RW	0	**Downstream Configuration Retry Request Timing After Receiving CRS Completion** 00: assert 1T after CRS is received 01: assert 4T after CRS is received 10: assert 8T after CRS is received 11: assert 16T after CRS is received

Offset Address: 1A9h (D3F0-3)

CRS Retry Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Enable CRS Retry Mechanism** 0: No retry cycle for CRS regardless of Rx5C[4] setting and return FFFF FFFFh for read cycles. 1: Follow Rx5C[4] setting.

Offset Address: 1AAh (D3F0-3)

Upstream Performance Control 2 **Default Value: 16h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**UpdateFC-P Generation to The Endpoint for Upstream Write TLPs** 0: UpdateFC-P is generated only when PD update is requested. 1: UpdateFC-P is generated when PH or PD update is requested.
3:2	RW	01b	**Control of Completion Merge Function Referred to the Condition of the Retry Buffer Header Queue** 00: Completion Merge function is performed when there is at least 1 new TLP in the retry buffer header queue. 01: Completion Merge function is performed when there are at least 2 new TLPs in the retry buffer header queue. 10: Completion Merge function is performed when there are at least 3 new TLPs in the retry buffer header queue. 11: Completion Merge function is performed when there are at least 4 new TLPs in the retry buffer header queue.
1	RW	1b	**Enable of Completion Merge Function** 0: Disable, directly generate the P2C Read Completion TLP as long as the completion data is ready for transmission. 1: Enable, merge the 1st and 2nd P2C Read CompletionsTLPs when the heavy PCIe traffic is observed.
0	RW	0	**Upstream Read Path Timing Option** 0: Fast timing, better read performance 1: Moderate timing, medium read performance

Offset Address: 1AB-1AFh (D3F0-3) – Reserved

PCI Express Data Link Layer Registers (1B0-1B9h)

Offset Address: 1B0-1B1h (D3F0-3) – Reserved

Offset Address: 1B2h (D3F0-3)

FCU Control and Status (D3F0) **Default Value: 40h**

FCI: Flow Control Initialization. FCU: Flow Control Unit.

Bit	Attribute	Default	Description
7	RW1C	0	**FCI/FCU Timeout Status** 0: No time out 1 The FCI / FCU timeout has occurred
6	RW	1b	**FCI/FCU Receive Timer Enable Control** 0: Disable the timeout mechanism. 1: Enable the timeout mechanism.
5	RW	0	**FCI/FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCI/FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only. 1: Timer reset by any received DLLPs.
3:0	RW	0	**Reserved**

FCU Control and Status (D3F1,D3F2,D3F3) **Default Value: 40h**

FCI: Flow Control Initialization. FCU: Flow Control Unit.

Bit	Attribute	Default	Description
7	RW1C	0	**FCI/FCU Timeout Status** 0: No time out 1 The FCI / FCU timeout has occurred
6	RW	1b	**FCI/FCU Receive Timer Enable Control** 0: Disable the timeout mechanism. 1: Enable the timeout mechanism.
5	RW	0	**FCI/FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCI/FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only. 1: Timer reset by any received DLLPs.
3:2	RW	0	**Reserved**
1:0	RO	0	**Reserved**

Offset Address: 1B3h (D3F0-3)

Replay Timer Control **Default Value: 81h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Replay Timer Control During Rewind** This root port resends those TLPs which do not have corresponding ACK/NAK received within the Replay Time which is defined at bit[2:0] of this register or Correctable Error Status bit[12]. The Rewind is defined as the period of time that this root port prepares the previously sent TLP which stored at the TLP Retry Buffer to resend. These bits defined the behavior of the internal replay timer during the Rewind so that the root port would have more accurate time measures for the TLP replay. 00: During Rewind, the root port halt the Replay Timer. It starts to count after root port sends the TLP out. 01 or 10: During Rewind, the Replay Timer continues counting.. 11: Reserved.
5:3	RO	0	**Reserved**
2:0	RW	001b	**Replay Count in L0s** The root port replays the TLP every Replay Time which is Replay Count x Replay Timer Limit (defined at Rx1BE or Rx1BF depending on the link width of this root port) when the ACK/NAK is failed to appear. These bits define the Replay Count when the receiver of the Link of this root port is in L0s. Please refer to the descriptions of bit[13, 12] of Correctable Error Status (Rx110). Note that the Replay Count is always 1 when the link is at L0. These bits work with Rx50[7] to define the TLP Replay Count during L0s: **When Rx50[7] is set to 0:**: 000: indefinite, i.e. the root port will wait forever for the ACK/NAK returned from the device side. 001: 1, this root port resends the TLP every 1 x Replay Timer Limit. 010: 2, this root port resends the TLP every 2 x Replay Timer Limit. 011: 4, this root port resends the TLP every 4 x Replay Timer Limit. 100: 8, this root port resends the TLP every 8 x Replay Timer Limit. 101: 16, this root port resends the TLP every 16 x Replay Timer Limit. 110: 32, this root port resends the TLP every 32 x Replay Timer Limit. 111: 64, this root port resends the TLP every 64 x Replay Timer Limit. **When Rx50[7] is set to 1:**: 000: indefinite, i.e. the root port will wait forever for the ACK/NAK returned from the device side. 001: 16, this root port resends the TLP every 16 x Replay Timer Limit. 010: 32, this root port resends the TLP every 32 x Replay Timer Limit. 011: 64, this root port resends the TLP every 64 x Replay Timer Limit. 100: 128, this root port resends the TLP every 128 x Replay Timer Limit. 101: 256, this root port resends the TLP every 256 x Replay Timer Limit. 110: 512, this root port resends the TLP every 512 x Replay Timer Limit. 111: 1024, this root port resends the TLP every 1024 x Replay Timer Limit.

Offset Address: 1B4h (D3F0-3)

Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Data Link TX Packets Arbitration Scheme** 0: Strict priority: NAK > TLP > FCU > ACK 1: Strict priority: NAK > FCU > TLP > ACK

Offset Address: 1B5h (D3F0-3)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets is sent or when FCU timer expires. 1: Update flow control credit only when FCU timer expired.
5:4	RW	0	**ACK Minimum Latency Control** Usually ACK will be issued as long as transmit one symbol transmission time is available. 00: Send ACK when the latency timer Rx1BA, Rx1BB, Rx1BC expired. 01: Send ACK every 4 correct TLP has been received or when the latency timer Rx1BA, Rx1BB, Rx1BC expired. 10: Send ACK every 8 correct TLP has been received or when the latency timer Rx1BA, Rx1BB, Rx1BC expired. 11: Send ACK every 16 correct TLP has been received. or when the latency timer Rx1BA, Rx1BB, Rx1BC expired.
3:2	RW	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received. 1: Do not complete FCI process even when TLP/FCU has been received.
0	RW	0	**VC1 FCI Data Link Layer Packet (DLLP) Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired. 1: Transmit FCI DLLP continuously as long as the FCI process is not finished.

Offset Address: 1B6h (D3F0-3)

Transaction / Link Layer Checking Control **Default Value: A1h**

Bit	Attribute	Default	Description
7	RW	1b	**Nak_Scheduled Flag Control** 0: Disable Nak_Scheduled Flag. Schedule Nak regardless of Nak_Scheduled Flag. 1: Enable Nak_Scheduled Flag. Nak can only be scheduled when Nak_Scheduled Flag is cleared. Nak_Scheduled Flag is set after a Nak is scheduled by receiving a TLP with CRC or Seq_Num ERROR, and is cleared after receiving a new Ack.
6:5	RW	01b	**TLP Receiving Timer** When timeout, reset error-framing byte-counter. 00: Reset byte-counter when 1us after TLP header received. 01: Reset byte-counter when 2us after TLP header received. 10: Reset byte-counter when 3us after TLP header received. 11: Reset byte-counter when 4us after TLP header received.
4	RW	0	**The First Downstream TLP Is Popped Out from TL 1T Earlier** 0: Disable 1: Enable
3:1	RW	0	**Reserved**
0	RW	1b	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

Offset Address: 1B7h (D3F0-3)

Link Layer FCU(Flow Control Unit) Control **Default Value: 0Ah**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:2	RW	10b	**Control of Update_FC-P DLLP Transmission** 00: Update_FC-P DLLP is transmitted as long as the transaction layer would like to update PH/PD credits. 01: Update_FC-P DLLP is transmitted only when the number of PH/PD requests in PH/PD FIFO is larger than 1/4 of PH/PD FIFO size. 10: Update_FC-P DLLP is transmitted only when the number of PH/PD requests in PH/PD FIFO is larger than 1/2 of PH/PD FIFO size. 11: Update_FC-P DLLP is transmitted only when the number of PH/PD requests in PH/PD FIFO is larger than 3/4 of PH/PD FIFO size.
1:0	RW	10b	**Control of Update_FC-NP DLLP Transmission** 00: Update_FC-NP DLLP is transmitted as long as the transaction layer would like to update NPH credits. 01: Update_FC-NP DLLP is transmitted only when the number of NPH requests in NPH FIFO is larger than 1/4 of NPH FIFO size. 10: Update_FC-NP DLLP is transmitted only when the number of NPH requests in NPH FIFO is larger than 1/2 of NPH FIFO size. 11: Update_FC-NP DLLP is transmitted only when the number of NPH requests in NPH FIFO is larger than 3/4 of NPH FIFO size.

Offset Address: 1B8h (D3F0-3)

Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Reserved** **Data Link Layer Header Position** 0: SDP (Start DLLP) can be on Lane 0 / 4 / 8 / 12. 1: SDP (Start DLLP) is always on Lane 0.

Offset Address: 1B9h (D3F0-3)

Data Link Layer Miscellaneous Control (D3F0) **Default Value: 00h**

This register applies only to D3F0, for D3F1-F3 the register is reserved.

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Enable of RXBCTL RESET Scheme when PM_Request_Ack DLLP Sequences are Generated** 0: When PM_Request_Ack sequences are generated, RXBCTL will not be reset 1: When PM_Request_Ack sequences are generated, RXBCTL will be reset

Offset Address: 1BAh (D3F0-3)

Ack / Nak Latency Timer Limit for X16 (D3F0) **Default Value: 0Ch**

This register applies only to D3F0, for D3F1-F3 the register is reserved.

Bit	Attribute	Default	Description
7:0	RW	0Ch	**Timer Limit for Ack / Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz) for X16** 00h: 4 x 1 clocks 01h: 4 x 2 clocks 02h: 4 x 3 clocks 0nh: 4 x (n+1) clocks … FFh: 4 x 256 clocks

Offset Address: 1BBh (D3F0-3)

Ack / Nak Latency Timer Limit for X8 / X4 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Timer Limit for Ack / Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz) for X8/X4** 00h: 4 x 1 clocks 01h: 4 x 2 clocks 02h: 4 x 3 clocks 0nh: 4 x (n+1) clocks … FFh: 4 x 256 clocks

Offset Address: 1BCh (D3F0-3)

Ack / Nak Latency Timer Limit for X2 / X1 **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**Timer Limit for Ack / Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz) for X2 / X1** 00h: 4 x 1 clocks 01h: 4 x 2 clocks 02h: 4 x 3 clocks 0nh: 4 x (n+1) clocks … FFh: 4 x 256 clocks

Offset Address: 1BDh (D3F0-3)

Replay Timer Limit for X16 (D3F0) **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay Timer Limit for X16** This root port resend the TLP if it did not receive ACK or NAK within a certain period of time, the Replay Timer Limit. Link width (Link status register, Rx52[8:4]) of this root port will change where the Replay Timer Limit is referred to. It is defined at these bits when the lane width of this root port is x16, at Rx1BE when it is x8 or x4, or at Rx1BF when it is x2 or x1. This root port 0 (RP0) will never be configured as a x16 link. Thus, writing anything to these bits will not change the behavior of this chip. 00h: 8 x 1 clocks 01h: 8 x 2 clocks 02h: 8 x 3 clocks … mnh: 8 x (mn+1) clocks … FFh: 8 x 256 clocks The clock in this root port is running at 250Mhz.

Offset Address: 1BEh (D3F0-3)

Replay Timer Limit for X8 / X4 **Default Value: 1Bh**

Bit	Attribute	Default	Description
7:0	RW	1Bh	**Replay Timer Limit for X8 / X4** This root port resend the TLP if it did not receive ACK or NAK within a certain period of time, the Replay Timer Limit. Link width (Link status register, Rx52[8:4]) of this root port will change where the Replay Timer Limit is referred to. It is defined at Rx1BD when the lane width of this root port is x16, at these bits when it is x8 or x4, or at Rx1BF when it is x2 or x1. 00h: 8 x 1 clocks 01h: 8 x 2 clocks 02h: 8 x 3 clocks … mnh: 8 x (mn+1) clocks … FFh: 8 x 256 clocks The clock in this root port is running at 250Mhz.FFh: 8 x 256 clocks

Offset Address: 1BFh (D3F0-3)

Replay Timer Limit for X2 / X1 **Default Value: 58h**

Bit	Attribute	Default	Description
7:0	RW	58h	**Replay Timer Limit for X2 / X1** This root port resend the TLP if it did not receive ACK or NAK within a certain period of time, the Replay Timer Limit. Link width (Link status register, Rx52[8:4]) of this root port will change where the Replay Timer Limit is referred to. It is defined at Rx1BD when the lane width of this root port is x16, at Rx1BE when it is x8 or x4, or at these bits when it is x2 or x1. 00h: 8 x 1 clocks 01h: 8 x 2 clocks 02h: 8 x 3 clocks … mnh: 8 x (mn+1) clocks … FFh: 8 x 256 clocks The clock in this root port is running at 250Mhz.

PCI Express Physical Layer Logical Sub-Block Registers (1C0-1CFh)

Offset Address: 1C0h (D3F0-3)

General Control 1 (D3F0) **Default Value: n3h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0 ROMSIP	**Disable Data Scrambling / Descrambling** 0: Enable data scrambling / descrambling 1: Disable data scrambling / descrambling
5:3	RW	0	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See Figure 52 “Loop Back Mode Selections”.
2:0	RW	011b	**COMMA Detection Window** 0, 1: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

General Control 1 (D3F1) **Default Value: n3h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0 ROMSIP	**Disable Data Scrambling / Descrambling** 0: Enable data scrambling / descrambling 1: Disable data scrambling / descrambling
5:3	RW	0	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See Figure 52 “Loop Back Mode Selections”.
2:0	RW	011b	**COMMA Detection Window** 0, 1: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

General Control 1 (D3F2) **Default Value: n3h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0 ROMSIP	**Disable Data Scrambling / Descrambling** 0: Enable data scrambling / descrambling 1: Disable data scrambling / descrambling
5:3	RW	0	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See Figure 52 “Loop Back Mode Selections”.
2:0	RW	011b	**COMMA Detection Window** 0, 1: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

General Control 1 (D3F3) **Default Value: n3h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, the following timeout will be shorter: TIMEOUT_2MS → TIMEOUT_4US TIMEOUT_12MS → TIMEOUT_24US TIMEOUT_24MS → TIMEOUT_48US TIMEOUT_48MS → TIMEOUT_96US TIMEOUT_1024TS → TIMEOUT_32TS Receiver Detection: 15x1024ns → 1x1024ns
6	RW	0 ROMSIP	**Disable Data Scrambling / Descrambling** 0: Enable data scrambling / descrambling 1: Disable data scrambling / descrambling
5:3	RW	0	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See Figure 52 “Loop Back Mode Selections”.
2:0	RW	011b	**COMMA Detection Window** 0, 1: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

Offset Address: 1C1h (D3F0-3)

General Control 2 (D3F0) **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	0	**Enable Clock Gating on Unused Lanes in a Multilane Link** 0: Disable. The clock of the unused lanes is active 1: Enable. The clock of the unused lanes is gated.
6	RW	0	**Enable Power down on Unused Lanes in a Multilane Link** 0: Disable. The unused lanes are active. 1: Enable. The unused lanes are power-down.
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module (DLLM)** 0: Disable 1: Enable
4:0	RW	0 ROMSIP	**PHY Lane Configuration Setting** 00000: Use PHY negotiation. 00001: 1x with normal lane connection 00010: 2x with normal lane connection 00100: 4x with normal lane connection 10101: 8x with normal lane connection (valid for D0F5 RxB0[7]=0) 11000: Force into DETECT_QUIET state, for testing measurement used only. 11001: Force intor DETECT_ACTIVE state, for testing measurement used only. Other values are not allowed.

General Control 2 (D3F1) **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	0	**Enable Clock Gating on Unused Lanes in a Multilane Link** 0: Disable. The clock of the unused lanes is active 1: Enable. The clock of the unused lanes is gated.
6	RW	0	**Enable Power down on Unused Lanes in a Multilane Link** 0: Disable. The unused lanes are active. 1: Enable. The unused lanes are power-down.
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module (DLLM)** 0: Disable 1: Enable
4:0	RW	0 ROMSIP	**PHY Lane Configuration Setting** 00000: Use PHY negotiation. 00001: 1x with normal lane connection 00010: 2x with normal lane connection 00100: 4x with normal lane connection 10101: 8x with normal lane connection (valid for D0F5 RxB0[7]=0) 11000: Force into DETECT_QUIET state, for testing measurement used only. 11001: Force intor DETECT_ACTIVE state, for testing measurement used only. Other values are not allowed.

General Control 2 (D3F2) **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	0	**Enable Clock Gating on Unused Lanes in a Multilane Link** 0: Disable. The clock of the unused lanes is active 1: Enable. The clock of the unused lanes is gated.
6	RW	0	**Enable Power down on Unused Lanes in a Multilane Link** 0: Disable. The unused lanes are active. 1: Enable. The unused lanes are power-down.
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module (DLLM)** 0: Disable 1: Enable
4:0	RW	0 ROMSIP	**PHY Lane Configuration Setting** 00000: Use PHY negotiation. 00001: 1x with normal lane connection 00010: 2x with normal lane connection 00100: 4x with normal lane connection 10101: 8x with normal lane connection (valid for D0F5 RxB0[7]=0) 11000: Force into DETECT_QUIET state, for testing measurement used only. 11001: Force intor DETECT_ACTIVE state, for testing measurement used only. Other values are not allowed.

General Control 2 (D3F3) **Default Value: nnh**

Bit	Attribute	Default	Description
7	RW	0	**Enable Clock Gating on Unused Lanes in a Multilane Link** 0: Disable. The clock of the unused lanes is active 1: Enable. The clock of the unused lanes is gated.
6	RW	0	**Enable Power down on Unused Lanes in a Multilane Link** 0: Disable. The unused lanes are active. 1: Enable. The unused lanes are power-down.
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module (DLLM)** 0: Disable 1: Enable
4:0	RW	0 ROMSIP	**PHY Lane Configuration Setting** 00000: Use PHY negotiation. 00001: 1x with normal lane connection 00010: 2x with normal lane connection 00100: 4x with normal lane connection 10101: 8x with normal lane connection (valid for D0F5 RxB0[7]=0) 11000: Force into DETECT_QUIET state, for testing measurement used only. 11001: Force intor DETECT_ACTIVE state, for testing measurement used only. Other values are not allowed.

Offset Address: 1C2h (D3F0-3)

MAC and PCS **Default Value: A7h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Reset of Elastic Buffer When PHYLS Starts to Transmit TS2** 0: Disabled 1: Enabled
6	RW	0	**Reset Elastic Buffer** Initiate Reset of Elastic Buffer When Write 1. Always read 0.
5	RW	1b	**Lane Enable** 0: Enable lanes based on LTSSM negotiation results. 1: Enable lanes based on receiver detection's results.
4	RW	0	**Bypass PHYES Device Detection in Detect Phase of LTSSM** 0: Enable PHYES to actually perform receiver detection in Detect phase. 1: Bypass receiver detection, and assume device exist. Usually, only set to "1" for testing or debugging.
3	RW	0	**State Machine LTSSM Exit Polling Active** 0: LTSSM follows the normal state transition check 1: LTSSM always stays in Polling.Active in 24ms and then does the state transition check.
2	RW	1b	**Wait IDL Ordered Set or Electrical Idle When L1/L23 Entry** 0: Always wait IDL ordered set for L1/L23 entry. 1: Wait Electrical Idle and ignore IDL ordered set for L1/L23 entry.
1	RW	1b	**Running Disparity Check** 0: Disable 1: Enable
0	RW	1b	**State Machine "Link Training and Status State Machine (LTSSM)" Control** 0: Wait for the electrical idle signal from the PHYES or 12ms after RESET# become inactive. 1: Always wait for 12ms after the RESET# become inactive.

Offset Address: 1C3h (D3F0-3)

LTSSM State **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PHYLS LTSSM State** See Table 30 "PHYLS_STATE_PE0_[7:0] Mapping".

Offset Address: 1C4h (D3F0-3)

Elastic Buffer Base Registers for Lane 0 to 1 (D3F0) **Default Value: 44h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	100b	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.
3	RW	0	**Reserved**
2:0	RW	100b	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Elastic Buffer Base Registers for Lane 0 to 1 (D3F1) **Default Value: 44h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	100b	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.
3	RW	0	**Reserved**
2:0	RW	100b	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Elastic Buffer Base Registers for Lane 0 to 1 (D3F2,D3F3) **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RW	100b	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: 1C5h (D3F0-3)

Elastic Buffer Base Registers for Lane 2 to 3 (D3F0) **Default Value: 44h**

This register applies only to D3F0, for D3F1-F3 the register is reserved.

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	100b	**Elastic Buffer Base Register for Lane 3** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.
3	RW	0	**Reserved**
2:0	RW	100b	**Elastic Buffer Base Register for Lane 2** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: 1C6h (D3F0-3)

Elastic Buffer Base Registers for Lane 4 to 5 (D3F0) **Default Value: 44h**

This register applies only to D3F0, for D3F1-F3 the register is reserved.

Bit	Attribute	Default	Description
7	RW	0	**Reserved** Writing 1 or 0 to these bits does not change behaviors of this chip.
6:4	RW	100b	**Elastic Buffer Base Register for Lane 5** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.
3	RW	0	**Reserved** Writing 1 or 0 to these bits does not change behaviors of this chip.
2:0	RW	100b	**Elastic Buffer Base Register for Lane 4** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: 1C7h (D3F0-3)

Elastic Buffer Base Registers for Lane 6 to 7 (D3F0) **Default Value: 44h**

This register applies only to D3F0, for D3F1-F3 the register is reserved.

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	100b	**Elastic Buffer Base Register for Lane 7** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.
3	RW	0	**Reserved**
2:0	RW	100b	**Elastic Buffer Base Register for Lane 6** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: 1C8-1CCh (D3F0-3) – Reserved

Offset Address: 1CDh (D3F0-3)

PHYLS MAC II (D3F0) **Default Value: 5Eh**

Bit	Attribute	Default	Description
7:6	RW	01b	**Number of FTS Ordered Sent in L0s Exit Sequence with vcc_FTS in the Received Training Sequence** 00: vcc_FTS + 1 01: vcc_FTS 10: vcc_FTS – 2 11: vcc_FTS – 5 * ***FTS*** is "Fast Training Sequence" defined in PCIe spec. * ***vcc_FTS*** is the numbers of FTS required by the receiver when exiting L0s.
5	RW	0	**Skip Speed Negotiation and Get to Target Speed Directly** 0: Disable. Normal operation 1: Enable. Get to target speed directly
4	RW	1b	**Lane Reversal Support** 0: Disable of lane reversal support 1: Enable of lane reversal support
3	RW	1b	**Support Width Change in Configuration State During Run Time** 0: Not support 1: Support
2	RW	1b	**FTS Timeout Counter Start Condition** 0: Start from electrical idle exit 1: Start from first COMMA symbol detected
1	RW	1b	**Inferred Electrical Idle in GEN2 State Transition** 0: Disable. Use PCIEPHY electrical idle detection result 1: Enable. Inferred electrical idle in GEN2 state
0	RW	0	**Downstream Tx arbitration between DLLM and PHYLS** 0: Normal arbitration 1: Arbitration with lower latency

PHYLS MAC II (D3F1-F3) **Default Value: 4Eh**

Bit	Attribute	Default	Description
7:6	RW	01b	**Number of FTS Ordered Sent in L0s Exit Sequence with vcc_FTS in the Received Training Sequence** 00: vcc_FTS + 1 01: vcc_FTS 10: vcc_FTS – 2 11: vcc_FTS – 5 * ***FTS*** is "Fast Training Sequence" defined in PCIe spec. * ***vcc_FTS*** is the numbers of FTS required by the receiver when exiting L0s.
5	RW	0	**Skip Speed Negotiation and Get to Target Speed Directly** 0: Disable. Normal operation 1: Enable. Get to target speed directly
4	RW	0	**Lane Reversal Support** 0: Disable of lane reversal support 1: Enable of lane reversal support
3	RW	1b	**Support Width Change in Configuration State During Run Time** 0: Not support 1: Support
2	RW	1b	**FTS Timeout Counter Start Condition** 0: Start from electrical idle exit 1: Start from first COMMA symbol detected
1	RW	1b	**Inferred Electrical Idle in GEN2 State Transition** 0: Disable. Use PCIEPHY electrical idle detection result 1: Enable. Inferred electrical idle in GEN2 state
0	RW	0	**Downstream Tx arbitration between DLLM and PHYLS** 0: Normal arbitration 1: Arbitration with lower latency

Offset Address: 1CEh (D3F0-3)

PHYLS PCS and PMA I (D3F0) **Default Value: 1nh**

Bit	Attribute	Default	Description
7	RW	0	**Transmitter Power State Setting When Link Speed Is Changed** 0: The transmitter power state is P1. 1: The transmitter power state is P0.
6:4	RW	001b	**CDR VCO Stabilization Time** 000: 1us 001: 2us 010: 4us 011: 8us 100:12us Others: Reserved
3	RW	0	**Receiver Termination Disable** 0: Termination enable (50ohm) 1: Termination disable (Hi-Z)
2	RW	1b ROMSIP	**Enable Low Swing Mode** 0: Disable 1: Enable
1	RW	1b	**Quick Byte Alignment Support** 0: Disable 1: Enable
0	RW	0	**Quick Phase Conversion Support** 0: Disable 1: Enable

PHYLS PCS and PMA I (D3F1) **Default Value: 1nh**

Bit	Attribute	Default	Description
7	RW	0	**Transmitter Power State Setting When Link Speed Is Changed** 0: The transmitter power state is P1. 1: The transmitter power state is P0.
6:4	RW	001b	**CDR VCO Stabilization Time** 000: 1us 001: 2us 010: 4us 011: 8us 100:12us Others: Reserved
3	RW	0	**Receiver Termination Disable** 0: Termination enable (50ohm) 1: Termination disable (Hi-Z)
2	RW	1b ROMSIP	**Enable Low Swing Mode** 0: Disable 1: Enable
1	RW	1b	**Quick Byte Alignment Support** 0: Disable 1: Enable
0	RW	0	**Quick Phase Conversion Support** 0: Disable 1: Enable

PHYLS PCS and PMA I (D3F2) **Default Value: 1nh**

Bit	Attribute	Default	Description
7	RW	0	**Transmitter Power State Setting When Link Speed Is Changed** 0: The transmitter power state is P1. 1: The transmitter power state is P0.
6:4	RW	001b	**CDR VCO Stabilization Time** 000: 1us 001: 2us 010: 4us 011: 8us 100:12us Others: Reserved
3	RW	0	**Receiver Termination Disable** 0: Termination enable (50ohm) 1: Termination disable (Hi-Z)
2	RW	1b ROMSIP	**Enable Low Swing Mode** 0: Disable 1: Enable
1	RW	1b	**Quick Byte Alignment Support** 0: Disable 1: Enable
0	RW	0	**Quick Phase Conversion Support** 0: Disable 1: Enable

PHYLS PCS and PMA I (D3F3) **Default Value: 1nh**

Bit	Attribute	Default	Description
7	RW	0	**Transmitter Power State Setting When Link Speed Is Changed** 0: The transmitter power state is P1. 1: The transmitter power state is P0.
6:4	RW	001b	**CDR VCO Stabilization Time** 000: 1us 001: 2us 010: 4us 011: 8us 100:12us Others: Reserved
3	RW	0	**Receiver Termination Disable** 0: Termination enable (50ohm) 1: Termination disable (Hi-Z)
2	RW	1b ROMSIP	**Enable Low Swing Mode** 0: Disable 1: Enable
1	RW	1b	**Quick Byte Alignment Support** 0: Disable 1: Enable
0	RW	0	**Quick Phase Conversion Support** 0: Disable 1: Enable

Offset Address: 1CFh (D3F0-3)

SKP Ordered Set Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Enable SKP Ordered-set Scheduling of 4.72us or 6.12us** 0: SKP ordered-set is scheduled every 4.72us 1: SKP ordered-set is scheduled every 6.12us
0	RW	0	**Enable SKP Ordered-set Scheduling to Match the Clock Difference of 5600ppm** 0: Disable. Only match the clock difference of 600ppm 1: Enable

Table 30. PHYLS_STATE_PE0-3_[7:0] Mapping

LTSSM States	Binary Coding	Hexadecimal Coding
DETECT_QUIET	8'B0000_0000	8'H00
DETECT_ACTIVE	8'B0000_0001	8'H01
POLLING_ACTIVE	8'B0001_0000	8'H10
POLLING_CONFIGURATION	8'B0001_0001	8'H11
POLLING_SPEED	8'B0001_0010	8'H12
POLLING_COMPLIANCE	8'B0001_0100	8'H14
POLLING_COMPLIANCE_ENTRY	8'B0001_0101	8'H15
POLLING_COMPLIANCE_EXIT	8'B0001_0110	8'H16
CONFIGURATION_RCVRCFG_STEP_1	8'B0010_0001	8'H21
CONFIGURATION_RCVRCFG_STEP_2	8'B0010_0010	8'H22
CONFIGURATION_RCVRCFG_STEP_3	8'B0010_0011	8'H23
CONFIGURATION_RCVRCFG_STEP_4	8'B0010_0100	8'H24
CONFIGURATION_RCVRCFG_STEP_5	8'B0010_0101	8'H25
CONFIGURATION_RCVRCFG_STEP_6	8'B0010_0110	8'H26
CONFIGURATION_RCVRCFG_STEP_7	8'B0010_0111	8'H27
CONFIGURATION_IDLE	8'B0010_1000	8'H28
RECOVERY_RCVRLOCK	8'B0011_0000	8'H30
RECOVERY_RCVRCFG	8'B0011_0001	8'H31
RECOVERY_IDLE	8'B0011_0011	8'H33
RECOVERY_SPEED	8'B0011_0111	8'H37
LOOPBACK_MSTR_ENTRY	8'B0100_0000	8'H40
LOOPBACK_MSTR_ACTIVE	8'B0100_0001	8'H41
LOOPBACK_MSTR_EXIT	8'B0100_0011	8'H43
LOOPBACK_SLAV_ENTRY	8'B0100_0100	8'H44
LOOPBACK_SLAV_ACTIVE	8'B0100_0101	8'H45
LOOPBACK_SLAV_EXIT	8'B0100_0111	8'H47
LOOPBACK_MSTR_SPEED	8'B0100_1000	8'H48
LOOPBACK_SLAV_SPEED	8'B0100_1001	8'H49
DISABLED_ENTRY	8'B0101_0000	8'H50
DISABLED_DISABLED	8'B0101_0001	8'H51
HOTRESET_ACTIVE	8'B0110_0000	8'H60
L0L0_TXL0_RXL0	8'B1000_1010	8'H8A
L0L0S_TXL0_RXENTRY	8'B1001_1000	8'H98
L0L0S_TXL0_RXIDLE	8'B1001_1001	8'H99
L0L0S_TXL0_RXFTS	8'B1001_1011	8'H9B
L0SL0_TXENTRY_RXL0	8'B1010_0010	8'HA2
L0SL0_TXIDLE_RXL0	8'B1010_0110	8'HA6
L0SL0_TXFTS_RXL0	8'B1010_1110	8'HAE
L0SL0S_TXENTRY_RXENTRY	8'B1011_0000	8'HB0
L0SL0S_TXENTRY_RXIDLE	8'B1011_0001	8'HB1
L0SL0S_TXENTRY_RXFTS	8'B1011_0011	8'HB3
L0SL0S_TXIDLE_RXENTRY	8'B1011_0100	8'HB4
L0SL0S_TXIDLE_RXIDLE	8'B1011_0101	8'HB5
L0SL0S_TXIDLE_RXFTS	8'B1011_0111	8'HB7
L0SL0S_TXFTS_RXENTRY	8'B1011_1100	8'HBC
L0SL0S_TXFTS_RXIDLE	8'B1011_1101	8'HBD
L0SL0S_TXFTS_RXFTS	8'B1011_1111	8'HBF
L1_ENTRY	8'B1100_0000	8'HC0
L1_IDLE	8'B1100_0001	8'HC1
L23READY_ENTRY	8'B1101_0000	8'HD0
L23READY_IDLE	8'B1101_0001	8'HD1

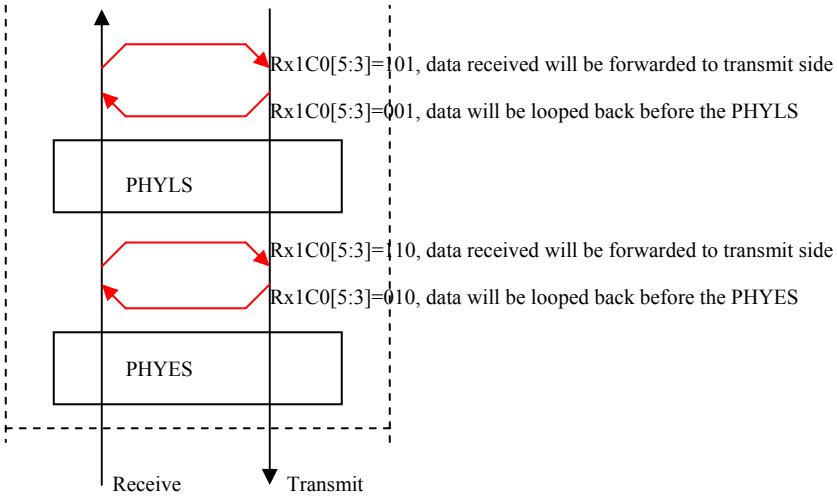


Figure 52. Loop Back Mode Selections

PCI Express Power Management Module Registers (1D0-1D7h)

Offset Address: 1D0h (D3F0-3)

PMU Control **Default Value: D8h**

Bit	Attribute	Default	Description
7	RW	1b	**Option to Let PMU Generate Link Retrain Command when PHYLS Requests to Change Link Bandwidth** 0: Disabled 1: Enabled
6:4	RW	101b	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	1b	**Enable Clearing the PM Cycles Requested by the Device in Speed Negotiation Process** 0: Disable 1: Enable
2	RW	0	**Link Retrain When Bad DLLP is Checked** 0: Disable 1: Enable
1	RW	0	**Link Loopback** 0: Normal operation. 1: Direct device to enter Loopback mode. Received data in the device will be sent to the transmission side.
0	RW	0	**Link Reconfigure Link Width** Link width reconfiguration is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state first, and then to the Configuration state. 0: When reconfigure link width, LTSSM must be in Detect state. 1: When reconfigure link width, LTSSM can go to Configuration state.

Offset Address: 1D1h (D3F0-3)

PMU (Power Management Unit) Timeout **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at bits [5:4] expired.
6	RW	0	**Reserved**
5:4	RW	10b	**Electrical Idle Waiting Period Before Moving to L1 State** After issue ACK to the L1 request from the device. 00: Always wait for electrical idle 01: Wait for 640 clocks 10: Wait for 1152 clocks 11: Wait for 2500 clocks in GEN1 and 5000 clocks in GEN2
3:2	RW	0	**Reserved**
1:0	RW	0	**Downstream Cycles Triggered C2P Cycles** Period of staying at L0 Before Returned to L1 for PHY (when PMU is not in D0 state) 00: Immediately 01: 1 cfgW or message + delay 10T 10: 1 32QW + 1 cfgW or message + delay 10T 11: 2 32QW + 1 cfgW or message + delay 10T

Offset Address: 1D2h (D3F0-3)

PMU L0s Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Idle Period to Enter L0s** When these bits are set to 00h, minimum time period is 128ns. 00: 128ns 01: 2x128ns 02: 3x128ns … FF: 256x128ns

Offset Address: 1D3h (D3F0-3)

PMU L1 Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Idle Period to Enter ASL1** Minimum time period is 128ns. 00: 128ns 01: 2x128ns 02: 3x128ns … FF: 256x128ns

Offset Address: 1D4-1D7h (D3F0-3) – Reserved

PCI Express Message Controller Related Registers (1D8-1DFh)

Offset Address: 1D8h (D3F0-3)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in The MSGC** 0: Normal operation. 1: There are errors not reported to the system.
6:0	RW	0	**Reserved**

Offset Address: 1D9-1DFh (D3F0-3) – Reserved

PCI Express Link Management Registers (1E0-1E9h)

Offset Address: 1E0h (D3F0-3)

Target Link Width (D3F0) **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4:0	RW	01000b	**Target Link Width** Allowable setting: D0F5 RxB0[7] = 0: x8/x4/x2/x1 D0F5 RxB0[7] = 1: x4/x2/x1

Target Link Width (D3F1) **Default Value: 02h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4:0	RW	00010b	**Target Link Width** Allowable setting: D0F5 RxB0[3] = 0: x2 D0F5 RxB0[3] = 1: x1

Target Link Width (D3F2) **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4:0	RW	00001b	**Target Link Width** Allowable setting: D0F5 RxB0[3] = 0: no lane D0F5 RxB0[3] = 1: x1

Target Link Width (D3F3) **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4:0	RW	00001b	**Target Link Width** Allowable setting: Fixed to x1.

Offset Address: 1E1h (D3F0-3)

Percentage of Non-Idle (PNI) Counter Setting **Default Value: 12h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**After Entering L0 State How Many Delay the PNI Counter Will Start** 0000: 32 T 0001: 64 T 0010: 128 T 0011: 256 T Others: Reserved
3:0	RW	0010b	**Evaluation Period of PNI Calculation** 0000: 16us 0001: 32us 0010: 64us 0011: 128us Others: Reserved

Note: For support Hardware-controlled autonomous power management minimizes power during full-on power States.
1. Rx1E1 control the start timing and duration of PNI counter.
2. Rx1E2 control the threshold to increase or reduce bandwidth.
3. Rx1E7[0] control the priority when hardware auto bandwidth change for power saving by change link width or speed.

Offset Address: 1E2h (D3F0-3)
PNI Algorithm Settings **Default Value: 22h**

Bit	Attribute	Default	Description
7:4	RW	0010b	**The Threshold of PNI to Increase Bandwidth** 0000: 75% 0001: 87.5% 0010: 93.75% 0011: 96.875% Others: Reserved
3:0	RW	0010b	**The Threshold of PNI to Reduce Bandwidth** 0000: 50% 0001: 25% 0010: 12.5% 0011: 6.25% Others: Reserved

Offset Address: 1E3h (D3F0-3)
GEN2 MAC Enhancement **Default Value: n1h**

Bit	Attribute	Default	Description
7	RW	0	**Set Compliance Receive Bit to 1b in Transmitting TS1 Ordered Sets** 0: Compliance Receive bit is 0b in transmitting TS1 ordered sets 1: Compliance Receive bit is 1b in transmitting TS1 ordered sets
6	RW	0	**If Hardware Automatically Upgrade Link Width to Increase Bandwidth, A Maximum Link Width Will be Selected** 0: If hardware automatically upgrades link width, a larger link width than current width is selected 1: If hardware automatically upgrades link width, a maximum link width will be selected
5:4	RW	10b ROMSIP	**Equalizer Tuning Timeout Setting** 00: 100us 01: 200us 10: 400us 11: 800us
3	RW	0	**Power Down Unintended TX to Down Configure Link Width When LTSSM is in Configuration State** 0: Unintended TX is power up and sends out TS1 with Lane number set to PAD. 1: Unintended TX is power down.
2	RW	0	**Electrical Idle Detection Behavior in Inactive Lanes When LTSSM Is in Configuration.Linkwidth.Start State** 0: Inactive lanes report electrical idle exit 1: Inactive lanes do not report electrical idle exit
1	RW	0	**Waiting Condition of Equalizer Tuning Timeout When LTSSM Is to Be Changed:** **1) From Polling.Active to Polling.Configuration** **2) From Recovery.Rcvrlock to Recovery .Rcvrcfg** 0: Always wait for equalizer tuning timeout 1: Do not wait for equalizer tuning timeout
0	RW	1b	**Enable of TXs in Inactive Lanes to Upconfigure Link Width When LTSSM Is in Configuration and Recovery State** 0: Disable. TXs in inactive lanes are enabled only when LTSSM is in Configuration state. 1: Enable. TXs in inactive lanes are enabled when LTSSM is in Configuration and Recovery state.

Offset Address: 1E4h (D3F0-3)
Speed Negotiation **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Write 1 to Clear the Internal Register "speed_fail_field"**
6:0	RW	0	**Number of Permitted Speed Negotiation** 00h: 1 01h: 2 02h: 4 03h: 8 04h: 16 05h: 32 06h: 64 07h: 128 08h: 256 09h: 512 0Ah: 1024 0Bh: 2048 0Ch: 4096 0Dh: 8192 0Eh: 16384 0Fh: 32768 Others: Reserved

Offset Address: 1E5h (D3F0-3)
Link Width Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Write 1 to clear the internal register "width_fail_field"**
6:0	RW	0	**Number of Permitted Link Width Negotiation** 00h: 1 01h: 2 02h: 4 03h: 8 04h: 16 05h: 32 06h: 64 07h: 128 08h: 256 09h: 512 0Ah: 1024 0Bh: 2048 0Ch: 4096 0Dh: 8192 0Eh: 16384 0Fh: 32768 Others: Reserved

Offset Address: 1E6h (D3F0-3)
Unreliable Link Management **Default Value: 43h**

Bit	Attribute	Default	Description
7	RW	0	**Write 1 to Clear the Internal Register "speed_unrl_field"**
6	RW	1b	**If GEN2 Link is More Unreliable Than GEN1 Link that Link Width is Larger Than x1** 0: No 1: Yes
5:4	RW	00b	**Limitation of Transmitter Replays the TLP with the Same Sequence Number** 00: 8 times 01: 16 times 10: 32 times 11: 64 times
3:2	RW	00b	**Limitation of Receiver Receives the TLP with the Same Sequence Number and LCRC Error** 00: 8 times 01: 16 times 10: 32 times 11: 64 times
1	RW	1b	**Enable of Receiver Link Unreliable Detection** 0: Disable. Not report Rx link unreliable status to PHYLS 1: Enable. Report Rx link unreliable status to PHYLS
0	RW	1b	**Enable of Transmitter Link Unreliable Detection** 0: Disable. Not report Tx link unreliable status to PHYLS 1: Enable. Report Tx link unreliable status to PHYLS

Offset Address: 1E7h (D3F0-3)
Bandwidth Power Arbitration **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	1b	**If GEN1 Link that Link Width is Larger Than x1 Consumes More Power Than GEN2 Link** 0: No 1: Yes

Offset Address: 1E8h (D3F0-3)
Aggressive Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Enable Aggressive Power Management When No Device Plug** 0: Disable 1: Enable
1	RW	0	**Enable PHYES Level-2 Power Down** 0: Disable 1: Enable
0	RW	0	**Enable of TPLL Turn Off When in L1 State** 0: Disable 1: Enable

Offset Address: 1E9-1EFh (D3F0-3) – Reserved

PCI Express Electrical PHY Test Registers (1F0-1F9h)

Offset Address: 1F0h (D3F0-3) – Reserved

Offset Address: 1F1h (D3F0-3)

Repeated Count of the Test Pattern (D3F0,D3F1,D3F3) **Default Value: 00h**

This register applies only to D3F0, for D3F1-F3 the register is reserved.

Bit	Attribute	Default	Description
7:0	RW	0	**Repeated Count of the Test Pattern** (as selected in Rx1F2[7:4]) When using loopback mode to test electrical PHY, the following should be satisfied: Rx1F1 x 8 > loopback latency/4ns 00-0Bh: Illegal value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times … FFh: Test pattern repeats 255 times

Offset Address: 1F2h (D3F0-3)

Test Pattern Selection 1 (D3F0) **Default Value: 20h**

For D3F2 this register is reserved.

Bit	Attribute	Default	Description
7:4	RW	0010b	**Test Pattern Select** 0000: SKP order-set 0001: User define SPTPTXD[39:0], combined from Rx1FC~Rx1FD[15:0] and Rx204~R207[23:0] 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Long bit pattern, from SATA spec 1110: Original RPAT random patter 1111: Compliance test bit sequence
3	RW	0	**Reserved**
2:0	RW	0	**Select Lane for Test** 000: Loop back test will be applied on lane 00, select EPHY lane00 signals for debugging. 001: Loop back test will be applied on lane 01, select EPHY lane01 signals for debugging. 010: Loop back test will be applied on lane 02, select EPHY lane02 signals for debugging. 011: Loop back test will be applied on lane 03, select EPHY lane03 signals for debugging. 100: Loop back test will be applied on lane 04, select EPHY lane04 signals for debugging. 101: Loop back test will be applied on lane 05, select EPHY lane05 signals for debugging. 110: Loop back test will be applied on lane 06, select EPHY lane06 signals for debugging. 111: Loop back test will be applied on lane 07, select EPHY lane07 signals for debugging.

Test Pattern Selection 1 (D3F1) — Default Value: 20h

The difference between D3F1 and D3F0 is in bits [3:0] bit descriptions.

Bit	Attribute	Default	Description
7:4	RW	0010b	**Test Pattern Select** 0000: SKP order-set 0001: User define SPTPTXD[39:0], combined from Rx1FC~Rx1FD[15:0] and Rx204~R207[23:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Long bit pattern, from SATA spec 1110: Original RPAT random patter 1111: Compliance test bit sequence
3:2	RW	0	**Reserved**
1:0	RW	00b	**Select Lane for Test and Debugging** 00: Loop back test will be applied on lane08, select EPHY lane08 signals for debugging. 01: Loop back test will be applied on lane09, select EPHY lane09 signals for debugging. 1x: Select EPHY lane09 signals for debugging.

Test Pattern Selection 1 (D3F3) — Default Value: 20h

The difference between D3F3 and D3F0 is in bits [3:0] bit descriptions.

Bit	Attribute	Default	Description
7:4	RW	0010b	**Test Pattern Select** 0000: SKP order-set 0001: User define SPTPTXD[39:0], combined from Rx1FC~Rx1FD[15:0] and Rx204~R207[23:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: Long bit pattern, from SATA spec 1110: Original RPAT random patter 1111: Compliance test bit sequence
3:0	RW	0	**Reserved**

Offset Address: 1F3h (D3F0-3)
Test Mode Control 1 (D3F0,D3F1,D3F3) **Default Value: 06h**

For D3F2 this register is reserved.

Bit	Attribute	Default	Description
7	RW	0	**Electrical PHY Test Mode Enable** Program this bit to 1 to start Electrical PHY test. 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3:0	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns. Suggested Value Settings: (Lane 0 for example) Rx1C0[5:3] = 001b: Rx1C4[2:0] + 2 Rx1C0[5:3] = 010b: Rx1C4[2:0] + 2 + (Loopback Path Latency/4ns)+1

Offset Address: 1F5-1F4h (D3F0-3)
BIST Status 1 (D3F0,D3F1,D3F3) **Default Value: 0nnnh**

For D3F2 this register is reserved.

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9:0	RO	HwInit	**Received Symbol When Rx1F3[7] is Set to 1** 00 when Rx1F3[7] is 0.

Offset Address: 1F7-1F6h (D3F0-3)
BIST Status 2 (D3F0,D3F1,D3F3) **Default Value: nnnnh**

For D3F2 this register is reserved.

Bit	Attribute	Default	Description
15	RO	HwInit	**Electrical PHY Test Error** 0: No error 1: Indicates that there is an error detected in the receiving side during the loop back test mode.
14	RO	HwInit	**Electrical PHY Built-In Self Test Error of Symbol Comparison** 0: No error detected 1: Indicates that some errors detected or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP.
13:10	RO	0	**Reserved**
9:0	RO	HwInit	**Transmitted Symbol When Rx1F3[7] is Set to 1** 00 when Rx1F3[7] is set to 0.

Offset Address: 1F9-1F8h (D3F0-3)
PHY BIST Counter Test Mode (D3F0,D3F1,D3F3) **Default Value: nnnnh**

For D3F2 this register is reserved.

Bit	Attribute	Default	Description
15:0	RO	HwInit	**PHY BIST Period Electrical PHY Test Error**

Offset Address: 1FB-1FAh (D3F0-3)

PHY Receiver Error Counter Control (D3F0) **Default Value: 00h**

Bit	Attribute	Default	Description
15:8	RO	0	**Error Count in Received Modified Compliance Pattern**
7	RW	0	**Enable of Receiver Error Counter** 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	0	**Receiver Error Counter Manual Start Control** 0: Receiver error counter cannot be manually started. 1: Receiver error counter can be manually started when bit 4 is set to 1.
4	RW	0	**Enable Receiver Error Counter Manual Start** 0: Receiver error counter starts when the receiver is valid. 1: Receiver error counter starts when bit 5 is set to 1.
3:2	RW	0	**Reserved**
1	RW	0	**Receiver Error Counter Manual End Control** 0: Receiver error counter cannot be manually ended. 1: Receiver error counter can be manually ended when bit 0 is set to 1.
0	RW	0	**Enable Receiver Error Counter Manual End** 0: Receiver error counter ends with 10us timeout. 1: Receiver error counter ends when bit 1 is set to 1.

PHY Receiver Error Counter Control (D3F1,D3F3) **Default Value: 00h**

The difference between D3F1,F3 and D3F0 is in bits [7:6] bit descriptions, and D3F2 is reserved.

Bit	Attribute	Default	Description
15:8	RO	0	**Error Count in Received Modified Compliance Pattern**
7:6	RW	0	**Reserved**
5	RW	0	**Receiver Error Counter Manual Start Control** 0: Receiver error counter cannot be manually started. 1: Receiver error counter can be manually started when bit 4 is set to 1.
4	RW	0	**Enable Receiver Error Counter Manual Start** 0: Receiver error counter starts when the receiver is valid. 1: Receiver error counter starts when bit 5 is set to 1.
3:2	RW	0	**Reserved**
1	RW	0	**Receiver Error Counter Manual End Control** 0: Receiver error counter cannot be manually ended. 1: Receiver error counter can be manually ended when bit 0 is set to 1.
0	RW	0	**Enable Receiver Error Counter Manual End** 0: Receiver error counter ends with 10us timeout. 1: Receiver error counter ends when bit 1 is set to 1.

Offset Address: 1FD-1FCh (D3F0-3)

User Defined Test Pattern (D3F0,D3F1,D3F3) **Default Value: 0000h**

For D3F2 this register is reserved.

Bit	Attribute	Default	Description
15:0	RW	0	**User Defined Test Pattern When Rx1F2[7:4] is Set to 0001b**

Offset Address: 1FEh (D3F0-3)

Loopback Latency Control 1 (D3F0) **Default Value: 00h**

For D3F1-F3 this register is reserved.

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Constant Loopback Latency Support** 0: Disable 1: Enable
4	RW	0	**Check If the Multi-lane Link Has Too Much Skew** 0: Lane-to-lane skew can be tolerated in any value of (0ns, 38ns) 1: Check lane-to-lane skew. All lanes in the link should be in a single latency group.
3:2	RW	0	**Reserved**
1:0	RW	0	**Loopback Latency Control for Lane 16, 17 and Lane 18** 00: Loopback latency range is (0ns, 14ns) 01: Loopback latency range is (14ns, 26ns) 10: Loopback latency range is (26ns, 38ns) 11: Reserved

Offset Address: 1FFh (D3F0-3)

Loopback Latency Control 2 (D3F0) **Default Value: 00h**

For D3F1-F3 this register is reserved.

Bit	Attribute	Default	Description
7:6	RW	0	**Loopback Latency Control for Lane 12 ~ Lane 15** 00: Loopback latency range is (0ns, 14ns) 01: Loopback latency range is (14ns, 26ns) 10: Loopback latency range is (26ns, 38ns) 11: Reserved
5:4	RW	0	**Loopback Latency Control Lane 8 ~ Lane 11** 00: Loopback latency range is (0ns, 14ns) 01: Loopback latency range is (14ns, 26ns) 10: Loopback latency range is (26ns, 38ns) 11: Reserved
3:2	RW	0	**Loopback Latency Control Lane 4 ~ Lane 7** 00: Loopback latency range is (0ns, 14ns) 01: Loopback latency range is (14ns, 26ns) 10: Loopback latency range is (26ns, 38ns) 11: Reserved
1:0	RW	0	**Loopback Latency Control Lane 0 ~ Lane 3** 00: Loopback latency range is (0ns, 14ns) 01: Loopback latency range is (14ns, 26ns) 10: Loopback latency range is (26ns, 38ns) 11: Reserved

Offset Address: 200h (D3F0-3)

PHYLS - PCS and PMA 2 **Default Value: 0nh**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Enforce De-emphasis Level with Selectable De-emphasis Value** This bit is used to select the De-emphasis level which sends to the transmitting circuit of this root port. Two more register affects the de-emphasis level, please refer to the register descriptions at Rx70[6]. 0: This root port uses the one advertised by downstream component as the De-emphasis level. 1: This root port uses the Selectable De-emphasis value at Rx70[6] as the De-emphasis level.
0	RW	1b ROMSIP	**Receive Low Swing Adjustment** The Swing mode for the receiving circuits is determined by this bit or D3F4, Rx50[3] when D3F4, Rx50[4] is 0/1. 0: Receiver voltage tuning circuits assumes the receiving signals on this root port is in normal swing mode, with de-emphasis. 1: Receiver voltage tuning circuits assumes the receiving signals on this root port is in low swing mode, without de-emphasis. This bit will be set to an initial value at the ROMSIP cycle after the de-assertion of PCIRST#. The corresponding programming bit in the ROMSIP is at 4th QW, byte 7, bit[0]. ***For D3F1:*** Tthe ROMSIP bit is at 4th QW, byte 7, bit[1]. ***For D3F2:*** The ROMSIP bit is at 4th QW, byte 7, bit[2]. ***For D3F3:*** The ROMSIP bit is at 4th QW, byte 7, bit[3].

Offset Address: 201h (D3F0-3)

PHY Transmit Error Counter Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Error Count in Transmitted Modified Compliance Pattern**

Offset Address: 202h (D3F0-3)

Test Pattern Selection 2 (D3F0,D3F1) **Default Value: 00h**

For D3F2-F3 this register is reserved.

Bit	Attribute	Default	Description
7:4	RW	0	**Difference Pattern Selection** Encoding is similar to Rx1F2[7:4] 0000: SKP order-set 0001: User define, use Rx1FC[9:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequencenn 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: D 10.2 test bit sequence 1110: D 24.3 test bit sequence 1111: Compliance test bit sequence
3:0	RW	0	**Reserved**

Offset Address: 203h (D3F0-3)

Test Pattern Selection 3 (D3F0) **Default Value: 00h**

The difference between D3F0 and D3F1 is in bits [7:2] bit descriptions. For D3F2 and D3F3 this register is reserved.

Bit	Attribute	Default	Description
7:0	RW	0	**Select Lanes with Different Pattern** When any of those bits are set to 1, different pattern is put into the according lanes. Else, test pattern is put into according lane. Bit m=0 : Rx1F2[7:4] test pattern is transmitted in m lane Bit m=1 : Rx206[7:4] difference pattern is transmitted in m lane (m= 0~ n-1) n=8 in this chip.

Test Pattern Selection 3 (D3F1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1:0	RW	0	**Select Lanes with Different Pattern** When any of those bits are set to 1, different pattern is put into the according lanes. Else, test pattern is put into according lane. Bit m=0 : Rx1F2[7:4] test pattern is transmitted in m lane Bit m=1 : Rx206[7:4] difference pattern is transmitted in m lane (m= 0~ n-1) n=2 in this chip.

Offset Address: 207-204h (D3F0-3)

Test Mode Control 2 (D3F0,D3F1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RW	0	**Reserved** Writing 1 or 0 to these bits does not change behaviors of this chip.
28	RW	0	**Control All Lanes in a Link Set to a Common Loopback Configuration Or Different Configurations** 0: All lanes in a link are set with a common loopback configuration. 1: Lanes in a link are set to different configurations.
27	RW	0	**Control SKP Ordered Set Insertion Control in EPHYTST Data Test Pattern** 0: No SKP Ordered set inserted In EPHYTST data pattern, 1: SKP ordered set inserted in EPHYTST data pattern. Apply to all PCIe ports (Lane 0 ~ 10)
26	RW	0	**The Option to Control Error Count Counts Data Mismatch Result or RXSTATUS Result** 0: Error count counts RXSTATUS. 1: Error count counts data mismatch result. Apply to all PCIe ports (Lane 0 ~ 10)
25:24	RW	0	**Transmit and Receiver Power State Setting Options** To generate maximum power ground noise or VCO interference, set TX/RX power state with following coding By default, transmit and receiver power state is set according to PHYLS state machine result. However, the power state can be manually set according to D3F4 Rx60~Rx6A[5:4, 1:0] settings based on below encoding table 00: Do not set Tx / Rx power state according to the manual setting. 01: Set Rx power state according to Rx manual setting. 10: Set Tx power state according to Tx manual setting. 11: Set both Tx and Rx with their manual setting respectively. The Tx and Rx power state manual settings are programmed from D3F4 Rx60~73[5:4, 1:0] respectively.
23:0	RW	0	**User Defined Test Pattern When Rx1F2[7:4] is Set to 0001b**

Test Mode Control 2 (D3F2) **Default Value: 0000 0000h**

The difference between D3F2 and D3F0-1 is in bits [31:26] bit descriptions.

Bit	Attribute	Default	Description
31:26	RO	0	**Reserved**
25:24	RW	0	**Transmit and Receiver Power State Setting Options** To generate maximum power ground noise or VCO interference, set TX/RX power state with following coding 00: Do not set Tx / Rx power state according to the manual setting. 01: Set Rx power state according to Rx manual setting. 10: Set Tx power state according to Tx manual setting. 11: Set both Tx and Rx with their manual setting respectively. The Tx and Rx power state manual settings are programmed from D3F4 Rx60~73[5:4, 1:0] respectively.
23:0	RO	0	**Reserved**

Test Mode Control 2 (D3F3) **Default Value: 0000 0000h**

The difference between D3F3 and D3F0-1 is in bits [31:28] bit descriptions.

Bit	Attribute	Default	Description
31:28	RW	0	**Reserved**
27	RW	0	**Control SKP Ordered Set Insertion Control in EPHYTST Data Test Pattern** 0: No SKP Ordered set inserted In EPHYTST data pattern, 1: SKP ordered set inserted in EPHYTST data pattern. Apply to all PCIe ports (Lane 0 ~ 10)
26	RW	0	**The Option to Control Error Count Counts Data Mismatch Result or RXSTATUS Result** 0: Error count counts RXSTATUS. 1: Error count counts data mismatch result. Apply to all PCIe ports (Lane 0 ~ 10)
25:24	RW	0	**Transmit and Receiver Power State Setting Options** To generate maximum power ground noise or VCO interference, set TX/RX power state with following coding 00: Do not set Tx / Rx power state according to the manual setting. 01: Set Rx power state according to Rx manual setting. 10: Set Tx power state according to Tx manual setting. 11: Set both Tx and Rx with their manual setting respectively. The Tx and Rx power state manual settings are programmed from D3F4 Rx60~73[5:4, 1:0] respectively.
23:0	RW	0	**User Defined Test Pattern When Rx1F2[7:4] is Set to 0001b**

Offset Address: 208-20Fh (D3F0-3) – Reserved

DEVICE 3 FUNCTION 4 (D3F4) – PCI EXPRESS PHYSICAL LAYER ELECTRICAL SUB-BLOCK

PCI Configuration Space

All registers in this function are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 3 and function number 4. For example: I/O write CF8h, with the data having the following format.

Bit-31	Bits [30:24]	Bits [23:16]	Bits [15:11]	Bits [10:8]	Bits [7: 2]	Bit-1	Bit-0
Enable	Reserved	Bus Number	Device Number	Function Number	Register Number	0	0
1	000_0000	0000_0000	0_0011	100	RX value with bit[1:0] = 00b		

And then I/O read CFCh, to get the data or I/O write CFCh, written_data (32 bits).

Header Registers (00–3Fh)

Rx00-Rx3F are PCI header registers. Please refer to PCI specification for more information.

Offset Address: 01-00h (D3F4)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D3F4)
Device ID **Default Value: E410h**

Bit	Attribute	Default	Description
15:0	RO	E410h	**Device ID**

Offset Address: 05-04h (D3F4)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RO	0	**Interrupt Disable** This bit only effects the interrupts generated by Root Port (PME and Hot plug event). MSI and INTx message generated by downstream devices are not controlled by this bit. 0: This Root Port is allowed to generate INTx message. 1: This Root Port is prevented from generating INTx messages.
9	RO	0	**Reserved**
8	RO	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors
7	RO	0	**Reserved**
6	RO	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors
5:3	RO	0	**Reserved**
2	RO	1b	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Set this bit to 0 will disable MSI messages.
1	RO	1b	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RO	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 07-06h (D3F4)

PCI Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error**
14	RO	0	**Signaled System Error**
13	RO	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status.
12	RO	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status.
11	RO	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status.
10:9	RO	0	**Reserved**
8	RO	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request.
7:5	RO	0	**Reserved**
4	RO	0	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device.
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally (TL).
2:0	RO	0	**Reserved**

Offset Address: 08h (D3F4)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision Code**

Offset Address: 0B-09h (D3F4)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D3F4)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** Reserved

Offset Address: 0Dh (D3F4)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer** Reserved

Offset Address: 0Eh (D3F4)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h indicates that this is a multiple function device.

Offset Address: 0Fh (D3F4)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 13-10h (D3F4)
Lower Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Lower Base Address**

Offset Address: 17-14h (D3F4)
Upper Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Upper Base Address**

Offset Address: 18h (D3F4)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Primary Bus Number

Offset Address: 19h (D3F4)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Secondary Bus Number

Offset Address: 1Ah (D3F4)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Subordinate Bus Number

Offset Address: 1Bh (D3F4) – Reserved

Offset Address: 1Ch (D3F4)
I/O Base **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	I/O Base
3:0	RO	0	I/O Addressing Capability

Offset Address: 1Dh (D3F4)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	I/O Limit
3:0	RO	0	I/O Addressing Capability

Offset Address: 1F-1Eh (D3F4)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	Detected Parity Error
14	RO	0	Received System Error
13	RO	0	Received Master Abort
12	RO	0	Received Target Abort
11	RO	0	Signaled Target Abort
10:9	RO	0	Reserved
8	RO	0	Master Data Parity Error
7:0	RO	0	Reserved

Offset Address: 21-20h (D3F4)
Memory Base **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Memory Base**
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D3F4)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Memory Limit**
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D3F4)
Prefetchable Memory Base **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Prefetchable Memory Base AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	0	**Report Support of Prefetchable 64 Bits Memory Addressing**

Offset Address: 27-26h (D3F4)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Prefetchable Memory Limit AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	0	**Report Support of Prefetchable 64 Bits Memory Addressing**

Offset Address: 2B-28h (D3F4)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RO	0	**AD[35:32]**

Offset Address: 2F-2Ch (D3F4)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RO	0	**AD[35:32]**

Offset Address: 31-30h (D3F4)

I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Base Upper 16 Bits Address for PCI**

Offset Address: 33-32h (D3F4)

I/O Limit Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**I/O Limit Upper 16 Bits Address for PCI**

Offset Address: 34h (D3F4)

Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer** Contains an offset from the start of configuration space.

Offset Address: 35-3Bh (D3F4) – Reserved

Offset Address: 3Ch (D3F4)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**INT Line**

Offset Address: 3Dh (D3F4)

Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**INT Pin** 0 indicates using INTA# as interrupt pin

Offset Address: 3F-3Eh (D3F4)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RO	0	**Secondary Bus Reset**
5	RO	0	**Reserved**
4	RO	0	**Base VGA 16 Bits Decode**
3	RO	0	**VGA Compatible I/O and Memory Address Range**
2	RO	0	**Block/Forward ISA I/O Cycles**
1	RO	0	**SERR Enable**
0	RO	0	**Parity Error Response Enable**

PCI Express Physical Layer Electrical Sub-block Registers (40-FFh)

Offset Address: 40h (D3F4)

PCIe PLL Settings **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	000b	**Set Voltage Control Oscillator (VCO) in Free Running Mode** x00: PLL locking mode x01: 1.25V x10: 1.50V x11: 1.75V
3:2	RW	00b	**Built-In Self Test Mode for Resistance Tuning** 00: BIST disable 01: BIST down 10: BIST up 11: BIST free running
1	RW	0	**Feedback Clock Ratio for Testing** 0: REFCLK is 100MHz 1: REFCLK is 125MHz
0	RW	0	**Enable All Functions in Master Block When Doing EPHY Testing** 0: Disable 1: Enable

Offset Address: 41h (D3F4)

Resistance Tuning - Tx Enable Settings **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Enable Tx Resistance for Set 2** 0: Disable 1: Enable
1	RW	0	**Enable Tx Resistance for Set 1** 0: Disable 1: Enable
0	RW	0	**Enable Tx Resistance for Set 0** 0: Disable 1: Enable

Offset Address: 42h (D3F4)

Resistance Tuning - Rx Enable Settings **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Enable Rx Resistance for Set 2** 0: Disable 1: Enable
1	RW	0	**Enable Rx Resistance for Set 1** 0: Disable 1: Enable
0	RW	0	**Enable Rx Resistance for Set 0** 0: Disable 1: Enable

Offset Address: 43h (D3F4)

Resistance Tuning Value for Set 0 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**Tx Resistance Value for Set 0** 0h: 73.5 1h: 69.4 2h: 65.8 3h: 62.5 4h: 59.5 5h: 56.8 6h: 54.3 7h: 52.1 8h: 50.0 9h: 48.1 Ah: 46.3 Bh: 44.6 Ch: 43.1 Dh: 41.7 Eh: 40.3 Fh: 39.1
3:0	RW	8h	**Rx Resistance Value for Set 0** 0h: 73.5 1h: 69.4 2h: 65.8 3h: 62.5 4h: 59.5 5h: 56.8 6h: 54.3 7h: 52.1 8h: 50.0 9h: 48.1 Ah: 46.3 Bh: 44.6 Ch: 43.1 Dh: 41.7 Eh: 40.3 Fh: 39.1

Offset Address: 44h (D3F4)

Resistance Tuning Value for Set 1 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**Tx Resistance Value for Set 1** 0h: 73.5 1h: 69.4 2h: 65.8 3h: 62.5 4h: 59.5 5h: 56.8 6h: 54.3 7h: 52.1 8h: 50.0 9h: 48.1 Ah: 46.3 Bh: 44.6 Ch: 43.1 Dh: 41.7 Eh: 40.3 Fh: 39.1
3:0	RW	8h	**Rx Resistance Value for Set 1** 0h: 73.5 1h: 69.4 2h: 65.8 3h: 62.5 4h: 59.5 5h: 56.8 6h: 54.3 7h: 52.1 8h: 50.0 9h: 48.1 Ah: 46.3 Bh: 44.6 Ch: 43.1 Dh: 41.7 Eh: 40.3 Fh: 39.1

Offset Address: 45h (D3F4)

Resistance Tuning Value for Set 2 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**Tx Resistance Value for Set 2** 0h: 73.5 1h: 69.4 2h: 65.8 3h: 62.5 4h: 59.5 5h: 56.8 6h: 54.3 7h: 52.1 8h: 50.0 9h: 48.1 Ah: 46.3 Bh:44.6 Ch: 43.1 Dh: 41.7 Eh: 40.3 Fh: 39.1
3:0	RW	8h	**Rx Resistance Value for Set 2** 0h: 73.5 1h: 69.4 2h: 65.8 3h: 62.5 4h: 59.5 5h: 56.8 6h: 54.3 7h: 52.1 8h: 50.0 9h: 48.1 Ah: 46.3 Bh: 44.6 Ch: 43.1 Dh: 41.7 Eh: 40.3 Fh: 39.1

Offset Address: 46h (D3F4)
Resistance Tuning Value for Set 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

Offset Address: 47h (D3F4)
Resistance Tuning Value for Set 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

Offset Address: 48h (D3F4)
Electrical Idle Detection Threshold Value for Set 0 **Default Value: 1nh**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	01b	**Beacon Detection Threshold Select** 00: 85mV 01: 114mV 10: 128mV 11: 135mV
3	RW	0	**Reserved**
2:0	RW	010b ROMSIP	**Electrical Idle Detection Threshold Value for Set 0** 000: 47mV 001: 70mV 010: 107mV 011: 130mV 100 ~ 111: Reserved

Offset Address: 49h (D3F4)
Electrical Idle Detection Threshold Value for Set 1 **Default Value: 1nh**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	01b	**Beacon Detection Threshold Select** 00: 85mV 01: 114mV 10: 128mV 11: 135mV
3	RW	0	**Reserved**
2:0	RW	010b ROMSIP	**Electrical Idle Detection Threshold Value for Set 1** 000: 47mV 001: 70mV 010: 107mV 011: 130mV 100 ~ 111: Reserved

Offset Address: 4Ah (D3F4)
Electrical Idle Detection Threshold Value for Set 2 **Default Value: 1nh**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	01b	**Beacon Detection Threshold Select** 00: 85mV 01: 114mV 10: 128mV 11: 135mV
3	RW	0	**Reserved**
2:0	RW	010b ROMSIP	**Electrical Idle Detection Threshold Value for Set 2** 000: 47mV 001: 70mV 010: 107mV 011: 130mV 100 ~ 111: Reserved

Offset Address: 4B-4Dh (D3F4) – Reserved

Offset Address: 4Eh (D3F4)

TPLL Power Down Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**TPLL2 Power Down Control** 0: TPLL2 power down behavior is the same as MPLL 1: TPLL2 power down is directly forced.
1	RW	0	**TPLL1 Power Down Control** 0: TPLL1 power down behavior is the same as MPLL 1: TPLL1 power down is directly forced.
0	RW	0	**TPLL0 Power Down Control** 0: TPLL0 power down behavior is the same as MPLL 1: TPLL0 power down is directly forced.

Offset Address: 4Fh (D3F4) – Reserved

Offset Address: 50h (D3F4)

Tx Swing Level Setting **Default Value: 0Ah**

Bit	Attribute	Default	Description
7:5	RW	000b	**Near-end Tx Margin Manual Set** Unit: V (full / low swing) 000: Normal 001: 0.8~1.2 / 0.4~0.7 010: 0.6~0.8 / 0.3~0.4 011: 0.4~0.6 / 0.2~0.3 100: 0.2~0.4 / 0.1~0.2 Others: Reserved
4	RW	0	**Tx Swing Level Enable** 0: Disable 1: Enable
3:2	RW	10b	**Far-end Tx Swing De-emphasis Manual Set** 00: Gen1 3.5dB, Gen2 6dB 01: Gen1 3.5dB, Gen2 3.5dB 10: Low swing, no de-emphasis 11: Reserved
1:0	RW	10b	**Near-end Tx Swing De-emphasis Manual Set** 00: Gen1 3.5dB, Gen2 6dB 01: Gen1 3.5dB, Gen2 3.5dB 10: Low swing, no de-emphasis 11: Reserved

Offset Address: 52-51h (D3F4)

De-emphasis and Bias Current Settings for Set 0 **Default Value: DD95h**

Bit	Attribute	Default	Description
15:11	RW	1Bh	**PCIe GEN2 De-emphasis Manual Setting for Set 0** 00h: 0mA 01h: 0.1mA 02h: 0.2mA 03h: 0.3 mA 04h: 0.4 mA 05h: 0.5 mA 06h: 0.6 mA 07h: 0.7 mA 08h: 0.8 mA 09h: 0.9 mA 0Ah: 1.0 mA 0Bh: 1.1 mA 0Ch: 1.2 mA 0Dh: 1.3 mA 0Eh: 1.4 mA 0Fh: 1.5 mA 10h: 1.6 mA 11h: 1.7 mA 12h: 1.8 mA 13h: 1.9 mA 14h: 2.0 mA 15h: 2.1 mA 16h: 2.2 mA 17h: 2.3mA 18h: 2.4 mA 19h: 2.5 mA 1Ah: 2.6 mA 1Bh: 2.7 mA 1Ch: 2.8 mA 1Dh: 2.9 mA 1Eh: 3.0 mA 1Fh: 3.1 mA
10:8	RW	101b	**PCIe GEN2 Bias Current Manual Setting for Set 0** Full swing: 000 (6+0mA) ~ 111 (6+3.5mA) Low swing: 000 (3.5+0mA) ~ 111(3.5+3.5mA) Default 101: +2.5mA
7:3	RW	12h	**PCIe GEN1 De-emphasis Manual Setting for Set 0** 00h: 0mA 01h: 0.1mA 02h: 0.2mA 03h: 0.3 mA 04h: 0.4 mA 05h: 0.5 mA 06h: 0.6 mA 07h: 0.7 mA 08h: 0.8 mA 09h: 0.9 mA 0Ah: 1.0 mA 0Bh: 1.1 mA 0Ch: 1.2 mA 0Dh: 1.3 mA 0Eh: 1.4 mA 0Fh: 1.5 mA 10h: 1.6 mA 11h: 1.7 mA 12h: 1.8 mA 13h: 1.9 mA 14h: 2.0 mA 15h: 2.1 mA 16h: 2.2 mA 17h: 2.3mA 18h: 2.4 mA 19h: 2.5 mA 1Ah: 2.6 mA 1Bh: 2.7 mA 1Ch: 2.8 mA 1Dh: 2.9 mA 1Eh: 3.0 mA 1Fh: 3.1 mA
2:0	RW	101b	**PCIe GEN1 Bias Current Manual Setting for Set 0** Full swing: 000 (6+0mA) ~ 111 (6+3.5mA) Low swing: 000 (3.5+0mA) ~ 111(3.5+3.5mA) Default 101: +2.5mA

Offset Address: 53h (D3F4)

De-emphasis and Bias Current Settings for Set 1 - I **Default Value: 95h**

Bit	Attribute	Default	Description
7:3	RW	12h	**PCIe GEN1 De-emphasis Manual Setting for Set 1** 00h: 0mA 01h: 0.1mA 02h: 0.2mA 03h: 0.3 mA 04h: 0.4 mA 05h: 0.5 mA 06h: 0.6 mA 07h: 0.7 mA 08h: 0.8 mA 09h: 0.9 mA 0Ah: 1.0 mA 0Bh: 1.1 mA 0Ch: 1.2 mA 0Dh: 1.3 mA 0Eh: 1.4 mA 0Fh: 1.5 mA 10h: 1.6 mA 11h: 1.7 mA 12h: 1.8 mA 13h: 1.9 mA 14h: 2.0 mA 15h: 2.1 mA 16h: 2.2 mA 17h: 2.3mA 18h: 2.4 mA 19h: 2.5 mA 1Ah: 2.6 mA 1Bh: 2.7 mA 1Ch: 2.8 mA 1Dh: 2.9 mA 1Eh: 3.0 mA 1Fh: 3.1 mA
2:0	RW	101b	**PCIe GEN1 Bias Current Manual Setting for Set 1** Full swing: 000 (6+0mA) ~ 111 (6+3.5mA) Low swing: 000 (3.5+0mA) ~ 111 (3.5+3.5mA) Default 101: +2.5mA

Offset Address: 54h (D3F4)

De-emphasis and Bias Current Settings for Set 1 - II **Default Value: DDh**

Bit	Attribute	Default	Description
7:3	RW	1Bh	**PCIe GEN2 De-emphasis Manual Setting for Set 1** 00h: 0mA 01h: 0.1mA 02h: 0.2mA 03h: 0.3 mA 04h: 0.4 mA 05h: 0.5 mA 06h: 0.6 mA 07h: 0.7 mA 08h: 0.8 mA 09h: 0.9 mA 0Ah: 1.0 mA 0Bh: 1.1 mA 0Ch: 1.2 mA 0Dh: 1.3 mA 0Eh: 1.4 mA 0Fh: 1.5 mA 10h: 1.6 mA 11h: 1.7 mA 12h: 1.8 mA 13h: 1.9 mA 14h: 2.0 mA 15h: 2.1 mA 16h: 2.2 mA 17h: 2.3mA 18h: 2.4 mA 19h: 2.5 mA 1Ah: 2.6 mA 1Bh: 2.7 mA 1Ch: 2.8 mA 1Dh: 2.9 mA 1Eh: 3.0 mA 1Fh: 3.1 mA
2:0	RW	101b	**PCIe GEN2 Bias Current Manual Setting for Set 1** Full swing: 000 (6+0mA)~111 (6+3.5mA) Low swing: 000 (3.5+0mA)~111(3.5+3.5mA) Default 101: +2.5mA

Offset Address: 55h (D3F4)

De-emphasis and Bias Current Settings for Set 2 - I **Default Value: 95h**

Bit	Attribute	Default	Description
7:3	RW	12h	**PCIe GEN1 De-emphasis Manual Setting for Set 2** 00h: 0mA 01h: 0.1mA 02h: 0.2mA 03h: 0.3 mA 04h: 0.4 mA 05h: 0.5 mA 06h: 0.6 mA 07h: 0.7 mA 08h: 0.8 mA 09h: 0.9 mA 0Ah: 1.0 mA 0Bh: 1.1 mA 0Ch: 1.2 mA 0Dh: 1.3 mA 0Eh: 1.4 mA 0Fh: 1.5 mA 10h: 1.6 mA 11h: 1.7 mA 12h: 1.8 mA 13h: 1.9 mA 14h: 2.0 mA 15h: 2.1 mA 16h: 2.2 mA 17h: 2.3mA 18h: 2.4 mA 19h: 2.5 mA 1Ah: 2.6 mA 1Bh: 2.7 mA 1Ch: 2.8 mA 1Dh: 2.9 mA 1Eh: 3.0 mA 1Fh: 3.1 mA
2:0	RW	101b	**PCIe GEN1 Bias Current Manual Setting for Set 2** Full swing: 000 (6+0mA) ~ 111 (6+3.5mA) Low swing: 000 (3.5+0mA) ~ 111 (3.5+3.5mA) Default 101: +2.5mA

Offset Address: 56h (D3F4)

De-emphasis and Bias Current Settings for Set 2 - II **Default Value: DDh**

Bit	Attribute	Default	Description
7:3	RW	1Bh	**PCIe GEN2 De-emphasis Manual Setting for Set 2** 00h: 0mA 01h: 0.1mA 02h: 0.2mA 03h: 0.3 mA 04h: 0.4 mA 05h: 0.5 mA 06h: 0.6 mA 07h: 0.7 mA 08h: 0.8 mA 09h: 0.9 mA 0Ah: 1.0 mA 0Bh: 1.1 mA 0Ch: 1.2 mA 0Dh: 1.3 mA 0Eh: 1.4 mA 0Fh: 1.5 mA 10h: 1.6 mA 11h: 1.7 mA 12h: 1.8 mA 13h: 1.9 mA 14h: 2.0 mA 15h: 2.1 mA 16h: 2.2 mA 17h: 2.3mA 18h: 2.4 mA 19h: 2.5 mA 1Ah: 2.6 mA 1Bh: 2.7 mA 1Ch: 2.8 mA 1Dh: 2.9 mA 1Eh: 3.0 mA 1Fh: 3.1 mA
2:0	RW	101b	**PCIe GEN2 Bias Current Manual Setting for Set 2** Full swing: 000 (6+0mA) ~ 111 (6+3.5mA) Low swing: 000 (3.5+0mA) ~ 111 (3.5+3.5mA) Default 101: +2.5mA

Offset Address: 57h (D3F4)

De-emphasis and Bias Current Settings for Set 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

Offset Address: 5A-58h (D3F4)

De-emphasis and Bias Current Settings for Set 4 **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:0	RO	0	**Reserved**

Offset Address: 5B-5Fh (D3F4) – Reserved

Offset Address: 60h (D3F4)

Power Status Manual Settings - Lane 0 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 0** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 0** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 0** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 0** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 61h (D3F4)

Power Status Manual Settings - Lane 1 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 1** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 1** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 1** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 1** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 62h (D3F4)

Power Status Manual Settings - Lane 2 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 2** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 2** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 2** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 2** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 63h (D3F4)

Power Status Manual Settings - Lane 3 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 3** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 3** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 3** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 3** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 64h (D3F4)

Power Status Manual Settings for Lane 4 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 4** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 4** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 4** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 4** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 65h (D3F4)

Power Status Manual Settings - Lane 5 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 5** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 5** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 5** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 5** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 66h (D3F4)

Power Status Manual Settings - Lane 6 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 6** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 6** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 6** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 6** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 67h (D3F4)

Power Status Manual Settings - Lane 7 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 7** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 7** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 7** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 7** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 68h (D3F4)

Power Status Manual Settings - Lane 8 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 8** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 8** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 8** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 8** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 69h (D3F4)

Power Status Manual Settings - Lane 9 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 9** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 9** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 9** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 9** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 6Ah (D3F4)

Power Status Manual Settings - Lane 10 **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Tx Power Status Manual Setting Enable for Lane 10** 0: Disable 1: Enable
6	RW	0	**Reserved**
5:4	RW	10b	**Tx Power Status Manual Setting Value for Lane 10** 00: P0 01: P0s 10: P1 11: P2
3	RW	0	**Rx Power Status Manual Setting Enable for Lane 10** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	10b	**Rx Power Status Manual Setting Value for Lane 10** 00: P0 01: P0s 10: P1 11: P2

Offset Address: 6B-73h (D3F4) – Reserved

Offset Address: 74h (D3F4)

Tx Electrical Idle and Speed Setting - Lane 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 0 Tx Electrical Idle Setting Enable** (See Note below) 0: Disable 1: Enable
3	RW	0	**Lane 0 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 0 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Note : The Tx Electrical Idle Setting Enable bit is effective only when the Tx Power Status Manual Setting Enable bit is set to 1. When the Tx Power Status Manual Setting Enable bit = 1 and Tx Electrical Idle Setting Enable bit = 0, lane n will be in electrical idle.

Offset Address: 75h (D3F4)

Tx Electrical Idle and Speed Setting - Lane 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 1 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 1 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 1 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 76h (D3F4)

Tx Electrical Idle and Speed Setting - Lane 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 2 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 2 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 02 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 77h (D3F4)

Tx Electrical Idle and Speed Setting - Lane 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 3 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 3 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 3 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 78h (D3F4)

Tx Electrical Idle and Speed Setting - Lane 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 4 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 4 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 4 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 79h (D3F4)

Tx Electrical Idle and Speed Setting - Lane 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 5 Tx Electrical Idle Setting Enable** 0: Disable 1b: Enable
3	RW	0	**Lane 5 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 5 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 7Ah (D3F4)

Tx Electrical Idle and Speed Setting - Lane 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 6 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 6 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 6 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 7Bh (D3F4)

Tx Electrical Idle and Speed Setting - Lane 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 7 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 7 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 7 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 7Ch (D3F4)

Tx Electrical Idle and Speed Setting - Lane 8 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 8 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 8 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 8 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 7Dh (D3F4)

Tx Electrical Idle and Speed Setting - Lane 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 9 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 9 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 9 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 7Eh (D3F4)

Tx Electrical Idle and Speed Setting - Lane 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Lane 10 Tx Electrical Idle Setting Enable** 0: Disable 1: Enable
3	RW	0	**Lane 10 GEN1 / GEN2 Manual Setting Enable** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**Lane 10 GEN1 / GEN2 Manual Setting Value** 0: GEN1 (2.5GHz) 1: GEN2 (5.0GHz)

Offset Address: 7F-8Bh (D3F4) – Reserved

Offset Address: 8Ch (D3F4)

PCIe MPLL0 Control **Default Value: 04h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Set0/Set1 Band Gap Power Down Selection** 0: Set0/Set1 Band Gap can be optionally power down by setting D3F0 Rx1E8[1] and D3F4 Rx4E[1:0] to 1. 1: Set0/Set1 Band Gap power down only when PCIE is power off or disabled.
3:0	RW	4h	**Reserved**

Offset Address: 8D-8Fh (D3F4) – Reserved

Offset Address: 90h (D3F4)

Receiving Clock Settings 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	000b ROMSIP	**Rx CLK Phase Selection** 0xx: No offset 100: + 0.2 period 110: + 0.4 period 101: + 0.6 period 111: + 0.8 period Others: Reserved
3	RW	0	**Reserved**
2:0	RW	000b	**IV Mode Selection** 000: CP1:x1 CP2x1 001: CP1:x1.25 CP2x1 010: CP1:x1 CP2x1.25 011: CP1:x1.25 CP2x1.25 100: CP1:x1 CP2x1 101: CP1:x1.5 CP2x1 110: CP1:x1 CP2x1.5 111: CP1:x1.5 CP2x1.5

Offset Address: 91h (D3F4)

Receiving Clock Settings 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**VCO Power Off Method When in P1 State** 0: VCO fully power off 1: VCO oscillates at lower frequency
3:1	RW	0	**Reserved**
0	RW	0	**RCV Power Off Method** 0: RCV power off at P0s/P1/P2 1: RCV power off at P1/P2

Offset Address: 92-93h (D3F4) – Reserved

Offset Address: 94h (D3F4)

Equalizer Tuning General Settings **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Tuning Function BIST Setting Enable** 0: Disable 1: Enable
6:4	RW	0	**Tuning Function BIST Event Selection** See Table 31 Tuning Function BIST Event Selection For GEN 1and Table 32 Tuning Function BIST Event Selection For GEN 2 below for detail.
3:0	RW	0 ROMSIP	**Equalizer Tuning Mode Selection**

Table 31. Tuning Function BIST Event Selection For GEN 1

	EPn_DCOUT Value 1/ Value 2	EPn_HFOUT Value 1 / Value2	EPn_OSOUT Value 1 / Value 2	EPn_W1OUT Value 1 / Value 2	EPn_W2OUT Value 1 / Value 2
000	00000 / 11111	Any value	01111 / 11111	Any value	11000 / 00000
001	Any value	Any value	01111 / 11111	Any value	11000 / 00000
010	00000 / 11111	Any value	01111 / 11111	Any value	11000 / 00000
011	11111 / 00000	Any value	01111 / 11111	Any value	00000 / 11000
100	11111 / 00000	Any value	11111 / 01111	Any value	00000 / 11000
101	Any value	00000	11111 / 01111	Any value	00000 / 11000
110	11111 / 00000	Any value	11111 / 01111	Any value	00000 / 11000
111	00000 / 11111	Any value	11111 / 01111	Any value	11000 / 00000

Table 32. Tuning Function BIST Event Selection For GEN 2

	EPn_DCOUT Value 1/ Value 2	EPn_HFOUT Value 1 / Value2	EPn_OSOUT Value 1 / Value 2	EPn_W1OUT Value 1 / Value 2	EPn_W2OUT Value 1 / Value 2
000	00000 / 11111	Any value	01111 / 11111	11111 / 00000	01100 / 00000
001	Any value	Any value	01111 / 11111	Any value	Any value
010	00000 / 11111	11111	01111 / 11111	11111 / 00000	01100 / 00000
011	11111 / 00000	00000	01111 / 11111	00000 / 11111	00000 / 01100
100	Any value	Any value	Any value	Any value	01100 / 00000
101	Any value	00000	Any value	00000 / 11111	Any value
110	11111 / 00000	11111	Any value	Any value	01100 / 00000
111	00000 / 11111	00000	Any value	Any value	00000 / 01100

Offset Address: 95h (D3F4)

Equalizer Tuning Bandwidth Settings 1 **Default Value: 71h**

Bit	Attribute	Default	Description
7:4	RW	7h ROMSIP	**LEQ HF Gain Tuning Bandwidth Setting** 0h: 1/2 1h: ¼ 2h: 1/6 3h: 1/8 4h: 1/10 5h: 1/12 6h: 1/14 7h: 1/16 8h: 1/18 9h: 1/20 Ah: 1/22 Bh: 1/24 Ch: 1/26 Dh: 1/28 Eh: 1/30 Fh: 1/32
3:0	RW	1h ROMSIP	**LEQ DC Gain Tuning Bandwidth Setting** 0h: 1 1h: ½ 2h: 1/3 3h: 1/4 4h: 1/5 5h: 1/6 6h: 1/7 7h: 1/8 8h: 1/9 9h: 1/10 Ah: 1/11 Bh: 1/12 Ch: 1/13 Dh: 1/14 Eh: 1/15 Fh: 1/16

Offset Address: 96h (D3F4)

Equalizer Tuning Bandwidth Settings 2 **Default Value: 71h**

Bit	Attribute	Default	Description
7:4	RW	7h ROMSIP	**Decision Feedback Equalizer (DFE) Weight Tuning Bandwidth Setting** 0h: 1/2 1h: ¼ 2h: 1/6 3h: 1/8 4h: 1/10 5h: 1/12 6h: 1/14 7h: 1/16 8h: 1/18 9h: 1/20 Ah: 1/22 Bh: 1/24 Ch: 1/26 Dh: 1/28 Eh: 1/30 Fh: 1/32
3:0	RW	1h ROMSIP	**LEQ Offset Tuning Bandwidth Setting** 0h: 1/2 1h: ¼ 2h: 1/6 3h: 1/8 4h: 1/10 5h: 1/12 6h: 1/14 7h: 1/16 8h: 1/18 9h: 1/20 Ah: 1/22 Bh: 1/24 Ch: 1/26 Dh: 1/28 Eh: 1/30 Fh: 1/32

Offset Address: 97-99h (D3F4) – Reserved

Offset Address: 9Ah (D3F4)

Equalizer Tuning Mode Settings - Set 0 **Default Value: 92h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable DFE in Training Mode** 0: Disable 1: Enable
6:4	RW	001b ROMSIP	**Equalizer Tuning Threshold Voltage for Set 0** x00: 400 mV x01: 450 mV x10: 500 mV x11: 550 mV
3	RW	0	**Enable Low Speed Mode After First Tuning Finished When Bit [2] = 1** 0: Disable 1: Enable
2	RW	0 ROMSIP	**Equalizer Always In Tuning Mode Enable for Set 0** 0: Disable 1: Enable
1:0	RW	10b ROMSIP	**Equalizer DFE Tap Selection for Set 0** 00: 0 tap (DFE off) 01: 0 tap for GEN1, 1 tap for GEN2 10: 1 tap for GEN1, 2 taps for GEN2 11: Reserved

Offset Address: 9Bh (D3F4)

Equalizer Tuning Mode Settings for Set 1 **Default Value: 92h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable DFE in Training Mode** 0: Disable 1: Enable
6:4	RW	001b ROMSIP	**Equalizer Tuning Threshold Voltage for Set 1** x00: 400 mV x01: 450 mV x10: 500 mV x11: 550 mV
3	RW	0	**Enable Low Speed Mode After First Tuning Finished When Bit 2 = 1** 0: Disable 1: Enable
2	RW	0 ROMSIP	**Equalizer Always In Tuning Mode Enable for Set 1** 0: Disable 1: Enable
1:0	RW	10b ROMSIP	**Equalizer DFE Tap Selection for Set 1** 00: 0 tap (DFE off) 01: 0 tap for GEN1, 1 tap for GEN2 10: 1 tap for GEN1, 2 taps for GEN2 11: Reserved

Offset Address: 9Ch (D3F4)

Equalizer Tuning Mode Settings for Set 2 **Default Value: 92h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable DFE in Training Mode** 0: Disable 1: Enable
6:4	RW	001b ROMSIP	**Equalizer Tuning Threshold Voltage for Set 2** x00: 300 x01: 350 x10: 400 x11: 450
3	RW	0	**Enable Low Speed Mode After First Tuning Finished When Bit 2 = 1** 0: Disable 1: Enable
2	RW	0 ROMSIP	**Equalizer Always In Tuning Mode Enable for Set 2** 0: Disable 1: Enable
1:0	RW	10b ROMSIP	**Equalizer DFE Tap Selection for Set 2** 00: 0 tap (DFE off) 01: 0 tap for GEN1, 1 tap for GEN2 10: 1 tap for GEN1, 2 taps for GEN2 11: Reserved

Offset Address: 9Dh (D3F4)

Equalizer Tuning Mode Settings for Set 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

Offset Address: 9Eh (D3F4)

Equalizer Tuning Mode Settings for Set 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Reserved**

Offset Address: 9Fh (D3F4) – Reserved

Offset Address: A3-A0h (D3F4)

Equalizer LEQ / DFE Settings for Set 0 **Default Value: FFC0 0000h**

Bit	Attribute	Default	Description
31:27	RW	1Fh	**LEQ DC Gain Manual Setting Value for Set 0** Min gain ~ Max gain
26:22	RW	1Fh	**LEQ HF Gain Manual Setting Value for Set 0** Min boost ~ Max boost
21:17	RW	0	**LEQ Offset Manual Setting Value for Set 0** 1Fh (-15 units) ~ 0Fh (15 units) sign magnitude 0000: 0 unit 00001: 1 unit 00010: 2 units 00011: 3 units 00100: 4 units ….. 01110: 14 units 01111: 15 units 10000: 0 unit 10001: -1 unit 10010: -2 units 10011: -3 units 10100: -4 units ….. 11110: -14 units 11111: -15 units
16:12	RW	0	**LEQ Weight 1 Manual Setting Value for Set 0** 0 (1 unit) ~ 1Fh (32 units)
11:7	RW	0	**DFE Weight 2 Manual Setting Value for Set 0** 0 (1 unit) ~ 1Fh (32 units)
6:5	RW	0	**Reserved**
4	RW	0	**LEQ DC Gain Manual Setting Enable for Set 0** 0: Disable 1: Enable
3	RW	0	**LEQ HF Gain Manual Setting Enable for Set 0** 0: Disable 1: Enable
2	RW	0	**LEQ Offset Manual Setting Enable for Set 0** 0: Disable 1: Enable
1	RW	0	**DFE Weight 1 Manual Setting Enable for Set 0** 0: Disable 1: Enable
0	RW	0	**DEF Weight 2 Manual Setting Enable for Set 0** 0: Disable 1: Enable

Offset Address: A7-A4h (D3F4)

Equalizer LEQ / DFE Settings for Set 1 **Default Value: FFC0 0000h**

Bit	Attribute	Default	Description
31:27	RW	11111b	**LEQ DC Gain Manual Setting Value for Set 1** Min gain ~ Max gain
26:22	RW	11111b	**LEQ HF Gain Manual Setting Value for Set 1** Min boost ~ Max boost
21:17	RW	0	**LEQ Offset Manual Setting Value for Set 1** 1Fh (-15 units) ~ 0Fh (15 units) sign magnitude See RxA3-A0 for detail.
16:12	RW	0	**LEQ Weight 1 Manual Setting Value for Set 1** 0 (1 unit) ~ 1Fh (32 units)
11:7	RW	0	**DFE Weight 2 Manual Setting Value for Set 1** 0 (1 unit) ~ 1Fh (32 units)
6:5	RW	0	**Reserved**
4	RW	0	**LEQ DC Gain Manual Setting Enable for Set 1** 0: Disable 1: Enable
3	RW	0	**LEQ HF Gain Manual Setting Enable for Set 1** 0: Disable 1: Enable
2	RW	0	**LEQ Offset Manual Setting Enable for Set 1** 0: Disable 1: Enable
1	RW	0	**DFE Weight 1 Manual Setting Enable for Set 1** 0: Disable 1: Enable
0	RW	0	**DEF Weight 2 Manual Setting Enable for Set 1** 0: Disable 1: Enable

Offset Address: AB-A8h (D3F4)

Equalizer LEQ / DFE Settings for Set 2 **Default Value: FFC0 0000h**

Bit	Attribute	Default	Description
31:27	RW	11111b	**LEQ DC Gain Manual Setting Value for Set 2** Min gain ~ Max gain
26:22	RW	11111b	**LEQ HF Gain Manual Setting Value for Set 2** Min boost ~ Max boost
21:17	RW	0	**LEQ Offset Manual Setting Value for Set 2** 1Fh (-15 units) ~ 0Fh (15 units) sign magnitude See RxA3-A0 for detail.
16:12	RW	0	**LEQ Weight 1 Manual Setting Value for Set 2** 0 (1 unit) ~ 1Fh (32 units)
11:7	RW	0	**DFE Weight 2 Manual Setting Value for Set 2** 0 (1 unit) ~ 1Fh (32 units)
6:5	RW	0	**Reserved**
4	RW	0	**LEQ DC Gain Manual Setting Enable for Set 2** 0: Disable 1: Enable
3	RW	0	**LEQ HF Gain Manual Setting Enable for Set 2** 0: Disable 1: Enable
2	RW	0	**LEQ Offset Manual Setting Enable for Set 2** 0: Disable 1: Enable
1	RW	0	**DFE Weight 1 Manual Setting Enable for Set 2** 0: Disable 1: Enable
0	RW	0	**DEF Weight 2 Manual Setting Enable for Set 2** 0: Disable 1: Enable

Offset Address: AF-ACh (D3F4)

Equalizer LEQ / DFE Settings for Set 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Offset Address: B3-B0h (D3F4)

Equalizer LEQ / DFE Settings for Set 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Offset Address: B4-BFh (D3F4) – Reserved

Offset Address: C0h (D3F4)

CDR Ratio Settings for Set 0 **Default Value: 24h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	010b	**FD Mode Ratio from P1 to P0 for Set 0** 000: 4/16 001: 5/16 010: 6/16 011: 7/16 100: 8/16 101: 9/16 110: 10/16 111: 11/16
3	RW	0	**Reserved**
2:0	RW	100b	**PD Training Mode Ratio from P0s to P0 for Set 0** 000: 6/16 001: 7/16 010: 8/16 011: 9/16 100: 10/16 101: 11/16 110: 12/16 111: 13/16

Offset Address: C1h (D3F4)

GEN1 Equalizer Exit Latency Settings for Set 0 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	001b	**GEN1 P1 Exit Latency for Set 0** 000: 1us 001: 2us 010: 4us 011: 8u 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Reserved**
2:0	RW	100b	**GEN1 P0s Exit Latency for Set 0** 000: 256ns 001: 256ns 010: 256ns 011: 512ns 100: 1us 101: 2us 110: 4us 111: 8us

Offset Address: C2h (D3F4)

GEN2 Equalizer Exit Latency Settings for Set 0 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	001b	**GEN2 P1 Exit Latency for Set 0** 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Reserved**
2:0	RW	100b	**GEN2 P0s Exit Latency for Set 0** 000: 256ns 001: 256ns 010: 256ns 011: 512ns 100: 1us 101: 2us 110: 4us 111: 8us

Offset Address: C3h (D3F4) – Reserved

Offset Address: C4h (D3F4)

GEN1 CDR Training Mode Settings for Set 0 **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**GEN1 Update Time During Training Mode for Set 0** 0: x1 1: x2
5:4	RW	10b	**GEN1 Gain 1 During Training Mode for Set 0** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	01b	**GEN1 Gain 2 During Training Mode for Set 0** 00: 1x 01: 2x 10: 4x 11: 8x
1:0	RW	01b	**GEN1 LF Select During Training Mode for Set 0** 00: 4 01: 8 10: 12 11: 16

Offset Address: C5h (D3F4)

GEN1 CDR Tracking Mode Settings for Set 0 **Default Value: 13h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**GEN1 Update Time During Tracking Mode for Set 0** 0: x1 1: x2
5:4	RW	01b	**GEN1 Gain 1 During Tracking Mode for Set 0** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	0	**GEN1 Gain 2 During Tracking Mode for Set 0** 00: 256ns 01: 256ns 10: 1us 11: 2us
1:0	RW	11b	**GEN1 LF Select During Tracking Mode for Set 0** 00: 4 01: 8 10: 12 11: 16

Offset Address: C6h (D3F4)

GEN2 CDR Training Mode Settings for Set 0 **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**GEN2 Update Time During Training Mode for Set 0** 0: x1 1: x2
5:4	RW	10b	**GEN2 Gain 1 During Training Mode for Set 0** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	01b	**GEN2 Gain 2 During Training Mode for Set 0** 00: 1x 01: 2x 10: 4x 11: 8x
1:0	RW	01b	**GEN2 LF Select During Training Mode for Set 0** 00: 4 01: 8 10: 12 11: 16

Offset Address: C7h (D3F4)

GEN2 CDR Tracking Mode Settings for Set 0 **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**GEN2 Update Time During Tracking Mode for Set 0** 0: x1 1: x2
5:4	RW	0	**GEN2 Gain 1 During Tracking Mode for Set 0** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	0	**GEN2 Gain 2 During Tracking Mode for Set 0** 00: 256ns 01: 256ns 10: 1us 11: 2us
1:0	RW	11b	**GEN2 LF Select During Tracking Mode for Set 0** 00: 4 01: 8 10: 12 11: 16

Offset Address: C8h (D3F4)

CDR Ratio Settings for Set 1 **Default Value: 24h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	010b	**FD Mode Ratio from P1 to P0 for Set 1** 000: 4/16 001: 5/16 010: 6/16 011: 7/16 100: 8/16 101: 9/16 110: 10/16 111: 11/16
3	RW	0	**Reserved**
2:0	RW	100b	**PD Training Mode Ratio from P0s to P0 for Set 1** 000: 6/16 001: 7/16 010: 8/16 011: 9/16 100: 10/16 101: 11/16 110: 12/16 111: 13/16

Offset Address: C9h (D3F4)

GEN1 Equalizer Exit Latency Settings for Set 1 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	001b	**GEN1 P1 Exit Latency for Set 1** 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Reserved**
2:0	RW	100b	**GEN1 P0s Exit Latency for Set 1** 000: 256ns 001: 256ns 010: 256ns 011: 512ns 100: 1us 101: 2us 110: 4us 111: 8us

Offset Address: CAh (D3F4)

GEN2 Equalizer Exit Latency Settings for Set 1 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	001b	**GEN2 P1 Exit Latency for Set 1** 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Reserved**
2:0	RW	100b	**GEN2 P0s Exit Latency for Set 1** 000: 256ns 001: 256ns 010: 256ns 011: 512ns 100: 1us 101: 2us 110: 4us 111: 8us

Offset Address: CBh (D3F4) – Reserved

Offset Address: CCh (D3F4)

GEN1 CDR Training Mode Settings for Set 1 **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**GEN1 Update Time During Training Mode for Set 1** 0: x1 1: x2
5:4	RW	10b	**GEN1 Gain 1 During Training Mode for Set 1** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	01b	**GEN1 Gain 2 During Training Mode for Set 1** 00: 1x 01: 2x 10: 4x 11: 8x
1:0	RW	01b	**GEN1 LF Select During Training Mode for Set 1** 00: 4 01: 8 10: 12 11: 16

Offset Address: CDh (D3F4)

GEN1 CDR Tracking Mode Settings for Set 1 **Default Value: 13h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**GEN1 Update Time During Tracking Mode for Set 1** 0: x1 1: x2
5:4	RW	01b	**GEN1 Gain 1 During Tracking Mode for Set 1** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	0	**GEN1 Gain 2 During Tracking Mode for Set 1** 00: 256ns 01: 256ns 10: 1us 11: 2us
1:0	RW	11b	**GEN1 LF Select During Tracking Mode for Set 1** 00: 4 01: 8 10: 12 11: 16

Offset Address: CEh (D3F4)

GEN2 CDR Training Mode Settings for Set 1 **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**GEN2 Update Time During Training Mode for Set 1** 0b: x1 1b: x2
5:4	RW	10b	**GEN2 Gain 1 During Training Mode for Set 1** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	01b	**GEN2 Gain 2 During Training Mode for Set 1** 00: 1x 01: 2x 10: 4x 11: 8x
1:0	RW	01b	**GEN2 LF Select During Training Mode for Set 1** 00: 4 01: 8 10: 12 11: 16

Offset Address: CFh (D3F4)

GEN2 CDR Tracking Mode Settings for Set 1 **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**GEN2 Update Time During Tracking Mode for Set 1** 0: x1 1: x2
5:4	RW	0	**GEN2 Gain 1 During Tracking Mode for Set 1** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	0	**GEN2 Gain 2 During Tracking Mode for Set 1** 00: 256ns 01: 256ns 10: 1us 11: 2us
1:0	RW	11b	**GEN2 LF Select During Tracking Mode for Set 1** 00: 4 01: 8 10: 12 11: 16

Offset Address: D0h (D3F4)

CDR Ratio Settings for Set 2 **Default Value: 24h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	010b	**FD Mode Ratio from P1 to P0 for Set 2** 000: 4/16 001: 5/16 010: 6/16 011: 7/16 100: 8/16 101: 9/16 110: 10/16 111: 11/16
3	RW	0	**Reserved**
2:0	RW	100b	**PD Training Mode Ratio from P0s to P0 for Set 2** 000: 6/16 001: 7/16 010: 8/16 011: 9/16 100: 10/16 101: 11/16 110: 12/16 111: 13/16

Offset Address: D1h (D3F4)

GEN1 Equalizer Exit Latency Settings for Set 2 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	001b	**GEN1 P1 Exit Latency for Set 2** 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Reserved**
2:0	RW	100b	**GEN1 P0s Exit Latency for Set 2** 000: 256ns 001: 256ns 010: 256ns 011: 512ns 100: 1us 101: 2us 110: 4us 111: 8us

Offset Address: D2h (D3F4)

GEN2 Equalizer Exit Latency Settings for Set 0 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	001b	**GEN2 P1 Exit Latency for Set 2** 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3	RW	0	**Reserved**
2:0	RW	100b	**GEN2 P0s Exit Latency for Set 2** 000: 256ns 001: 256ns 010: 256ns 011: 512ns 100: 1us 101: 2us 110: 4us 111: 8us

Offset Address: D3h (D3F4) – Reserved

Offset Address: D4h (D3F4)

GEN1 CDR Training Mode Settings for Set 2 **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**GEN1 Update Time During Training Mode for Set 2** 0: x1 1: x2
5:4	RW	10b	**GEN1 Gain 1 During Training Mode for Set 2** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	01b	**GEN1 Gain 2 During Training Mode for Set 2** 00: 1x 01: 2x 10: 4x 11: 8x
1:0	RW	01b	**GEN1 LF Select During Training Mode for Set 2** 00: 4 01: 8 10: 12 11: 16

Offset Address: D5h (D3F4)

GEN1 CDR Tracking Mode Settings for Set 2 **Default Value: 13h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**GEN1 Update Time During Tracking Mode for Set 2** 0: x1 1: x2
5:4	RW	01b	**GEN1 Gain 1 During Tracking Mode for Set 2** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	0	**GEN1 Gain 2 During Tracking Mode for Set 2** 00: 256ns 01: 256ns 10: 1us 11: 2us
1:0	RW	11b	**GEN1 LF Select During Tracking Mode for Set 2** 00: 4 01: 8 10: 12 11: 16

Offset Address: D6h (D3F4)

GEN2 CDR Training Mode Settings for Set 2 **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**GEN2 Update Time During Training Mode for Set 2** 0b: x1 1: x2
5:4	RW	10b	**GEN2 Gain 1 During Training Mode for Set 2** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	01b	**GEN2 Gain 2 During Training Mode for Set 2** 00: 1x 01: 2x 10: 4x 11: 8x
1:0	RW	01b	**GEN2 LF Select During Training Mode for Set 2** 00: 4 01: 8 10: 12 11: 16

Offset Address: D7h (D3F4)

GEN2 CDR Tracking Mode Settings for Set 2 **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**GEN2 Update Time During Tracking Mode for Set 2** 0: x1 1: x2
5:4	RW	0	**GEN2 Gain 1 During Tracking Mode for Set 2** 00: 1x 01: 2x 10: 4x 11: 8x
3:2	RW	0	**GEN2 Gain 2 During Tracking Mode for Set 2** 00: 256ns 01: 256ns 10: 1us 11: 2us
1:0	RW	11b	**GEN2 LF Select During Tracking Mode for Set 2** 00: 4 01: 8 10: 12 11: 16

Offset Address: D8-FFh (D3F4) – Reserved

PCI EXPRESS ROOT COMPLEX REGISTER BLOCK

RCRB-H MMIO

RCRB-H is the Root Complex Register Block for Host interface in memory-mapped IO space. The MMIO base address is defined in D0F5 Rx6B-68.

Virtual Channel (VC) Capability (000-03Fh)

Offset Address: 003-000h (RCRB-H)
Virtual Channel Enhanced Capability Header **Default Value: 0401 0002h**

Bit	Attribute	Default	Description
31:20	RO	040h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 007-004h (RCRB-H)
Port VC Capability 1 **Default Value: 0000 0800h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	10b	**Port Arbitration Table Entry Size** The upstream arbitration unit of this chip supports up to 6 ports. 10b indicates the size of port arbitration table entry is 4 bits.
9:8	RO	0	**Reference Clock** Reserved.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 00B-008h (RCRB-H)
Port VC Capability 2 **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**VC Arbitration Table** 00: Table is not present.
23:8	RO	0	**Reserved**
7:0	RO	01h	**VC Arbitration Capability** Fixed at hardware fixed arbitration support.

Offset Address: 00D-00Ch (RCRB-H)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RO	0	**VC Arbitration Select**
0	RO	0	**Load VC Arbitration Table** Reserved

Offset Address: 00F-00Eh (RCRB-H)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

Offset Address: 013-010h (RCRB-H)
VC Resource Capability (VC0) **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table (VC0)** Reserved
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions** Reserved
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	01h	**Port Arbitration Capability** Time-based Weighted Round Robin (T_WRR) 128 phase

Offset Address: 017-014h (RCRB-H)
VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RW	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RO	0	**Port Arbitration Select**
16	RO	0	**Load Port Arbitration Table** Reserved
15:8	RO	0	**Reserved**
7:1	RW	7Fh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0.
0	RO	1b	**TC/VC Mapping** The bit definition is the same as bits [7:1]. However this bit is hardwired to 1 (TC0 is always mapped to VC0).

Offset Address: 01B-018h (RCRB-H)
VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved
15:0	RO	0	**Reserved**

Offset Address: 01C-03Fh (RCRB-H) – Reserved

Root Complex Link Declaration Enhanced Capability (040-04Fh)

Offset Address: 043-040h (RCRB-H)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**PCI Express Extended Capability ID**

Offset Address: 047-044h (RCRB-H)

Element Self Description **Default Value: 0001 0501h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Number** 0: Egress port
23:16	RO	01h	**Component ID**
15:8	RO	05h	**Number of Link Entries** 5 Links.
7:4	RO	0	**Reserved**
3:0	RO	1h	**Element Type** 0h: Configuration space element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 048-04Fh (RCRB-H) – Reserved

Link Entry for PE0 (050-05Fh)

PE0 is for D3F0, PE1 for D3F1, PE2 for D3F2 and PE3 for D3F3.

Offset Address: 053-050h (RCRB-H)

PE0 Link Description **Default Value: 0101 0003h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:8	RW	0	**Reserved**
7:2	RO	0	**Reserved** Total 2VC. RW is set by D0F5 RxF0[0].))
1	RO	1b	**Link Type** Points to PE0.
0	RO	1b	**Link Valid**

Offset Address: 054-057h (RCRB-H) – Reserved

Offset Address: 05B-058h (RCRB-H)

PE0 Lower Base Address **Default Value: 0001 8000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 05C-05Fh (RCRB-H) – Reserved

Link Entry for PE1 (060-06Fh)

Offset Address: 063-060h (RCRB-H)

PE1 Link Description **Default Value: 0201 0003h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:8	RW	0	**Reserved**
7:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Points to PE1.
0	RO	1b	**Link Valid**

Offset Address: 064-067h (RCRB-H) – Reserved

Offset Address: 06B-068h (RCRB-H)

PE1 Lower Base Address **Default Value: 0001 9000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	001b	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 06C-06Fh (RCRB-H) – Reserved

Link Entry for PE2 (070-07Fh)

Offset Address: 073-070h (RCRB-H)

PE2 Link Description **Default Value: 0301 0003h**

Bit	Attribute	Default	Description
31:24	RO	03h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:8	RW	0	**Reserved**
7:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Points to PE2
0	RO	1b	**Link Valid**

Offset Address: 074-077h (RCRB-H) – Reserved

Offset Address: 07B-078h (RCRB-H)

PE2 Lower Base Address **Default Value: 0001 A000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	010b	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 07C-07Fh (RCRB-H) – Reserved

Link Entry for PE3 (080-08Fh)

Offset Address: 083-080h (RCRB-H)

PE3 Link Description **Default Value: 0401 0003h**

Bit	Attribute	Default	Description
31:24	RO	04h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:8	RW	0	**Reserved**
7:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Points to PE3.
0	RO	1b	**Link Valid**

Offset Address: 084-087h (RCRB-H) – Reserved

Offset Address: 08B-088h (RCRB-H)

PE3 Lower Base Address **Default Value: 0001 B000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	011b	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 08C-08Fh (RCRB-H) – Reserved

Link Entry for HDAC (090-1FFh)

Offset Address: 093-090h (RCRB-H)

HDAC Link Description **Default Value: 0501 0003h**

Bit	Attribute	Default	Description
31:24	RO	05h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:8	RW	0	**Reserved**
7:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Point to HDAC.
0	RO	1b	**Link Valid**

Offset Address: 094-097h (RCRB-H) – Reserved

Offset Address: 09B-098h (RCRB-H)

HDAC Lower Base Address **Default Value: 000A 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:20	RO	0	**Bus Number**
19:15	RO	14h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 09C-1FFh (RCRB-H) – Reserved

VC Arbitration Timer (200-20Fh) – Not Support

Offset Address: 200-20Fh (RCRB-H) – Reserved

Port Arbitration Timer for VC0 (210-21Fh)

Offset Address: 210h (RCRB-H)

PE0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 211h (RCRB-H)

PE0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 212h (RCRB-H)

PE1 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 213h (RCRB-H)

PE1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 214h (RCRB-H)

PE2 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 215h (RCRB-H)

PE2 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 216h (RCRB-H)

PE3 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 217h (RCRB-H)

PE3 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of 125MHz)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 218-21Fh (RCRB-H) – Reserved

Port Arbitration Timer for VC1 (220-22Fh) – Not support

Offset Address: 220-22Fh (RCRB-H) – Reserved

Host Side Upstream Arbitration Timers (230-23Fh)

A fair arbitration timer is designed for the upstream traffic, which provides a fair arbitration between PCI express devices and other devices like AGP, PCI2 master, I/O APIC and V-Link. The arbitration scheme is the same with the one currently implemented in the DRAMC.

Offset Address: 230h (RCRB-H)

PCIe VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 231h (RCRB-H)

PCIe VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 232-233h (RCRB-H) – Reserved

Offset Address: 234h (RCRB-H)

PCCA VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Priority to SM (South Module) Request** 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3:0	RW	0	**VC0 Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 235h (RCRB-H)

PCCA VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**VC0 Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 236-237h (RCRB-H) – Reserved

Offset Address: 238h (RCRB-H)

GFX Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GADS from IGFX** 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3:0	RW	0	**GFX Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 239h (RCRB-H)

GFX Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**GFX Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23A-23Bh (RCRB-H) – Reserved

Offset Address: 23Ch (RCRB-H)

IO APIC Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23Dh (RCRB-H)

IO APIC Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23E-23Fh (RCRB-H) – Reserved

DRAM Side Upstream Arbitration Timers (240-25Fh)

This fair arbitration timer is for upstream traffic to do a fair arbitration between all of the VC1 PCI Express devices.

Offset Address: 240-245h (RCRB-H) – Reserved

Offset Address: 246h (RCRB-H)

IPI Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 247h (RCRB-H)

IPI Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 248-25Fh (RCRB-H) – Reserved

SLI / Host Arbitration Timers (260-26Fh) - Not support

Offset Address: 260-26Fh (RCRB-H) – Reserved

P2P Arbitration Timer of PCIe (270-27Fh)

Offset Address: 270h (RCRB-H)
PE0 - P2P Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 271h (RCRB-H)
PE0- P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 272h (RCRB-H)
PE1 - P2P Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 273h (RCRB-H)
PE1 - P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 274h (RCRB-H)
PE2 - P2P Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 275h (RCRB-H)
PE2 - P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 276h (RCRB-H)

PE3 - P2P Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 277h (RCRB-H)

PE3 - P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 278-27Dh (RCRB-H) – Reserved

Offset Address: 27Eh (RCRB-H)

PCCA P2P Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**P2P Occupancy Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 27Fh (RCRB-H)

PCCA P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0	**P2P Promote Timer (In Unit of Host Frequency)** 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

SOUTH MODULE LEGACY CONTROL

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented by using discrete logic on original PC/AT motherboards. All the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All the registers reside in I/O space.

Table 33. System I/O Ports Map

Port	Function
00-1Fh	**Master DMA Controller**
20-3Fh	**Master Interrupt Controller**
40-5Fh	**Timer / Counter**
60-6Fh	**Keyboard Controller**
(60h)	**KBC Data**
(61h)	**Misc Functions & Speaker Control**
(64h)	**KBC Command / Status**
70-77h	**RTC/CMOS/NMI-Disable**
78-7Fh	**-available for system use**
80h	**-reserved- (debug port)**
81-8Fh	**DMA Page Registers**
90-91h	**-available for system use**
92h	**System Control**
93-9Fh	**-available for system use**
A0-BFh	**Slave Interrupt Controller**
C0-DFh	**Slave DMA Controller**
E0-FFh	**-available for system use**
100-CF7h	**-available for system use**
CF8-CFBh	**PCI Configuration Address**
CFC-CFFh	**PCI Configuration Data**
D00-FFFFh	**-available for system use**

I/O Port Address: 61h

Miscellaneous Functions & Speaker Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**SERR# Status** 0: SERR# has not been asserted 1: SERR# was asserted by a PCI agent This bit is set when the PCI bus SERR# signal is asserted. Once set, this bit may be cleared by setting bit-2 of this register. Bit-2 should be cleared to enable recording of the next SERR# (i.e., bit-2 must be set to 0 to enable this bit to be set).
6	RO	0	**IOCHK# Status** 0: IOCHK# has not been asserted 1: IOCHK # was asserted by an ISA agent This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK# (i.e., bit-3 must be set to 0 to enable this bit to be set). IOCHCK# generates NMI to the CPU if NMI is enabled.
5	RO	0	**Timer/Counter 2 Output** This bit reflects the output of Timer/Counter 2 without any synchronization.
4	RO	0	**Refresh Detected** This bit toggles to reflect timer update on every rising edge of the ISA bus REFRESH# signal.
3	RW	0	**IOCHK# Control** 0: Enable (see bit-6 above) 1: Disable (force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6)
2	RW	0	**SERR# Control** 0: Enable (see bit-7 above) 1: Disable (force SERR# inactive and clear any "SERR# Active" condition in bit-7)
1	RW	0	**Speaker Control** 0: Disable 1: Enable Timer/Counter 2 output to drive SPKR pin
0	RW	0	**Timer/Counter 2 Enable** 0: Disable 1: Enable Timer/Counter 2

I/O Port Address: 92h

System Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**A20 Address Line Enable** 0: A20 disabled / forced 0 (real mode) 1: A20 address line enabled
0	RW	0	**High Speed Reset** 0: Normal 1: Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller I/O Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60h.

A "Control" register is also available. It is accessible by writing commands 20h / 60h to the command port (port 64h); the control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" that control pins dedicated to specific functions. These ports are defined as follows:

Bit	**Input Port**
0	Keyboard Data In
1	Mouse Data In

Bit	**Output Port**
0	System Reset (1 = Execute Reset)
1	Gate A20 (1 = A20 Enabled)
2	Mouse Data Out
3	Mouse Clock Out
6	Keyboard Clock Out
7	Keyboard Data Out

Bit	**Test Port**
0	Keyboard Clock In
1	Mouse Clock In

The above definitions are provided for reference only as actual keyboard and mouse control is no longer performed bit by bit using the above ports but controlled directly by keyboard / mouse controller internal logic. Data is sent and received using the command codes listed on the following page.

I/O Port Address: 60h

Keyboard Controller Input / Output Buffer

Bit	Attribute	Default	Description
7:0	RW	0	When Write: Keyboard Controller Input Buffer Only write to port 60h if port 64h bit-1 = 0 (1=full). When Read: Keyboard Controller Output Buffer Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Only write to port 60h if port 64h bit-1 = 0 (1=full).

I/O Port Address: 64h (When Read)

Keyboard / Mouse Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Parity Error** 0: No parity error (odd parity received) 1: Even parity occurred on last byte received from keyboard / mouse
6	RO	0	**General Receive / Transmit Timeout** 0: No Error 1: Error
5	RO	0	**Mouse Output Buffer Full** 0: Mouse output buffer empty 1: Mouse output buffer holds mouse data
4	RO	0	**Keylock Status** 0: Locked 1: Free
3	RO	0	**Command / Data** 0: Last write was data write 1: Last write was command write
2	RO	0	**System Flag** 0: Power-On default 1: Self test successful
1	RO	0	**Input Buffer Full** 0: Input buffer empty 1: Input buffer full
0	RO	0	**Keyboard Output Buffer Full** 0: Keyboard output buffer empty 1: Keyboard output buffer full

I/O Port Address: 64h (When Write)
Keyboard / Mouse Command

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by this chip are listed in the table below.

Table 34. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) Value: 00h = OK, 01h = clock stuck low, 02h=clock stuck high, 03h = data stuck low, 04h = data stuck high, FFh = general error
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
C0h	Read Input Port (read input data to output buffer)
C1h	Poll Input Port (read Mouse Data In continuously to status bit 5)
C8h	Unblock Mouse Output (use before D1 to change active mode)
C9h	Reblock Mouse Output (protection mechanism for D1)
CAh	Read Mode (output KBC mode info to port 60 output buffer: bit 0 = 0 if ISA, bit 0 = 1 if PS/2)
D0h	Read Output Port (copy output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit 5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit 5 (write following byte to mouse; put value in mouse input buffer so it appears to have action from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read Keyboard Clock In and Mouse Clock In (return in bits 0-1 respectively of response byte)
Exh	Set Mouse Clock Out per command bit 3 Set Mouse Data Out per command bit 2 Set Gate A20 per command bit 1
Fxh	Pulse Mouse Clock Out low for 6 us per command bit 3 Pulse Mouse Data Out low for 6 us per command bit 2 Pulse Gate A20 low for 6 us per command bit 1 Pulse System Reset low for 6 us per command bit 0

All other codes not listed are undefined.

KBC Control Register (R/W via Commands 20h/60h)

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	1b	**PC Compatibility** 0: Disable scan conversion 1: Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes.
5	RW	0	**Mouse Interface** 0: Enable 1: Disable
4	RW	0	**Keyboard Interface** 0: Enable 1: Disable
3	RO	0	**Reserved**
2	RO	0	**System Flag** This bit may be read back as status register bit-2.
1	RW	0	**Mouse Interrupts** 0: Disable 1: Enable. Generate interrupt on IRQ12 when mouse data comes into output buffer.
0	RW	0	**Keyboard Interrupts** 0: Disable 1: Enable. Generate interrupt on IRQ1 when output buffer has been written.

DMA Controller I/O Registers

I/O Ports Address: 00-0Fh
Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 000x 0000	RW	**Channel 0 Base / Current Address**
0000 0000 000x 0001	RW	**Channel 0 Base / Current Count**
0000 0000 000x 0010	RW	**Channel 1 Base / Current Address**
0000 0000 000x 0011	RW	**Channel 1 Base / Current Count**
0000 0000 000x 0100	RW	**Channel 2 Base / Current Address**
0000 0000 000x 0101	RW	**Channel 2 Base / Current Count**
0000 0000 000x 0110	RW	**Channel 3 Base / Current Address**
0000 0000 000x 0111	RW	**Channel 3 Base / Current Count**
0000 0000 000x 1000	RW	**Status / Command**
0000 0000 000x 1001	WO	**Write Request**
0000 0000 000x 1010	WO	**Write Single Mask**
0000 0000 000x 1011	WO	**Write Mode**
0000 0000 000x 1100	WO	**Clear Byte Pointer**
0000 0000 000x 1101	WO	**Master Clear**
0000 0000 000x 1110	WO	**Clear Mask**
0000 0000 000x 1111	RW	**Read/Write All Mask Bits**

I/O Ports Address: C0-DFh
Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1100 000x	RW	**Channel 4 Base / Current Address**
0000 0000 1100 001x	RW	**Channel 4 Base / Current Count**
0000 0000 1100 010x	RW	**Channel 5 Base / Current Address**
0000 0000 1100 011x	RW	**Channel 5 Base / Current Count**
0000 0000 1100 100x	RW	**Channel 6 Base / Current Address**
0000 0000 1100 101x	RW	**Channel 6 Base / Current Count**
0000 0000 1100 110x	RW	**Channel 7 Base / Current Address**
0000 0000 1100 111x	RW	**Channel 7 Base / Current Count**
0000 0000 1101 000x	RW	**Status / Command**
0000 0000 1101 001x	WO	**Write Request**
0000 0000 1101 010x	WO	**Write Single Mask**
0000 0000 1101 011x	WO	**Write Mode**
0000 0000 1101 100x	WO	**Clear Byte Pointer F/F**
0000 0000 1101 101x	WO	**Master Clear**
0000 0000 1101 110x	WO	**Clear Mask**
0000 0000 1101 111x	WO	**Read/Write All Mask Bits**

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 80-8Fh

DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (address bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1000 0111	RW	**Channel 0 DMA Page (M-0)**
0000 0000 1000 0011	RW	**Channel 1 DMA Page (M-1)**
0000 0000 1000 0001	RW	**Channel 2 DMA Page (M-2)**
0000 0000 1000 0010	RW	**Channel 3 DMA Page (M-3)**
0000 0000 1000 1111	RW	**Channel 4 DMA Page (S-0)**
0000 0000 1000 1011	RW	**Channel 5 DMA Page (S-1)**
0000 0000 1000 1001	RW	**Channel 6 DMA Page (S-2)**
0000 0000 1000 1010	RW	**Channel 7 DMA Page (S-3)**

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting D17F0 Rx40 bit[1]. If the shadow registers are enabled, DMA control registers' contents could be read back from the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port Address	Attribute	Description
Port 0	RO	**Channel 0 Base Address**
Port 1	RO	**Channel 0 Byte Count**
Port 2	RO	**Channel 1 Base Address**
Port 3	RO	**Channel 1 Byte Count**
Port 4	RO	**Channel 2 Base Address**
Port 5	RO	**Channel 2 Byte Count**
Port 6	RO	**Channel 3 Base Address**
Port 7	RO	**Channel 3 Byte Count**
Port 8	RO	**1st Read Channel 0-3 Command Register**
Port 8	RO	**2nd Read Channel 0-3 Request Register**
Port 8	RO	**3rd Read Channel 0 Mode Register**
Port 8	RO	**4th Read Channel 1 Mode Register**
Port 8	RO	**5th Read Channel 2 Mode Register**
Port 8	RO	**6th Read Channel 3 Mode Register**
Port F	RO	**Channel 0-3 Read All Mask**
Port C4	RO	**Channel 5 Base Address**
Port C6	RO	**Channel 5 Byte Count**
Port C8	RO	**Channel 6 Base Address**
Port CA	RO	**Channel 6 Byte Count**
Port CC	RO	**Channel 7 Base Address**
Port CE	RO	**Channel 7 Byte Count**
Port D0	RO	**1st Read Channel 4-7 Command Register**
Port D0	RO	**2nd Read Channel 4-7 Request Register**
Port D0	RO	**3rd Read Channel 4 Mode Register**
Port D0	RO	**4th Read Channel 5 Mode Register**
Port D0	RO	**5th Read Channel 6 Mode Register**
Port D0	RO	**6th Read Channel 7 Mode Register**
Port DE	RO	**Channel 4-7 Read All Mask**

Interrupt Controller I/O Registers

This chip integrates two Interrupt Controllers, Master and Slave Interrupt Controllers, either one is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 21-20h
Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7 and occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 001x xxx0	RW	**Master Interrupt Control**
0000 0000 001x xxx1	RW	**Master Interrupt Mask**

Note that not all bits of the address are decoded.

I/O Ports Address: A1-A0h
Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 101x xxx0	RW	**Slave Interrupt Control**
0000 0000 101x xxx1	RW	**Slave Interrupt Mask**

Note that not all address bits are decoded.

Interrupt Controller I/O Shadow Registers

The following shadow registers are enabled by setting D17F0 Rx40[1]. If the shadow registers are enabled, Interrupt Controller control registers' contents could be read back from the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

I/O Ports Address: 20h
Master Interrupt Control Shadow

Bit	Attribut	Default	Description
7	RO	-	Reserved
6	RO	-	OCW3 bit 2 for Poll Mode (POLL)
5	RO	-	OCW3 bit 0 for Read IS Register (RIS)
4	RO	-	OCW3 bit 5 for Special Mask Mode (SMM)
3	RO	-	OCW2 bit 7 for Rotation (R)
2	RO	-	ICW4 bit 4 for Special Fully Nest Mode (SFNM)
1	RO	-	ICW4 bit 1 for Automatic End of Interrupt (AEOI)
0	RO	-	ICW1 bit 3 for Level Trigger Mode (LTIM)

Note: OCW: Operation Command Word; ICW: Initialization Command Word.

I/O Ports Address: A0h
Slave Interrupt Control Shadow

Bit	Attribut	Default	Description
7	RO	-	Reserved
6	RO	-	OCW3 bit 2 for Poll Mode (POLL)
5	RO	-	OCW3 bit 0 for Read IS Register (RIS)
4	RO	-	OCW3 bit 5 for Special Mask Mode (SMM)
3	RO	-	OCW2 bit 7 for Rotation (R)
2	RO	-	ICW4 bit 4 for Special Fully Nest Mode (SFNM)
1	RO	-	ICW4 bit 1 for Automatic End of Interrupt (AEOI)
0	RO	-	ICW1 bit 3 for Level Trigger Mode (LTIM)

Note: OCW: Operation Command Word; ICW: Initialization Command Word.

I/O Ports Address: 21h
Master Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	—	**T7-T3 of Interrupt Vector Address**

I/O Ports Address: A1h
Slave Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	—	**T7-T3 of Interrupt Vector Address**

Timer / Counter I/O Registers

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 010x xx00	RW	**Timer / Counter 0 Count**
0000 0000 010x xx01	RW	**Timer / Counter 1 Count**
0000 0000 010x xx10	RW	**Timer / Counter 2 Count**
0000 0000 010x xx11	WO	**Timer / Counter Command Mode**

Note that not all bits of the address are decoded.

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting D17F0 Rx40[1]. If the shadow registers are enabled, Timer / Counter registers are read back from the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port Address	Attribute	Description
Port 40	RO	**Counter 0 Base Count Value (LSB 1st MSB 2nd)**
Port 41	RO	**Counter 1 Base Count Value (LSB 1st MSB 2nd)**
Port 42	RO	**Counter 2 Base Count Value (LSB 1st MSB 2nd)**

CMOS / RTC I/O Registers

I/O Ports Address: 70h
CMOS Address

Bit	Attribute	Default	Description
7	RW	1b	**NMI Disable** 0: Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus. 1: Disable NMI Generation
6:0	RW	–	**CMOS Address** (lower 128 bytes of the CMOS memory)

I/O Ports Address: 71h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Data** (128 bytes of the CMOS memory)

Ports 70-71 may be accessed if D17F0 Rx51[3] is set to one to select the internal RTC. If Rx51[3] is set to zero, accesses to ports 70-71 will be directed to an external RTC.

I/O Ports Address: 74h
CMOS Address

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Address** (256 bytes of the CMOS memory)

I/O Ports Address: 75h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Data** (256 bytes of the CMOS memory)

Ports 74-75 may be accessed only if D17F0 Rx4E[3] (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the “CMOS” block. The RTC control registers are located at specific offsets in the CMOS data area (00-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Table 35. CMOS Register Summary

Offset	Description		
	Register Function	Binary Range	Decimal Range
00	Seconds	00-3Bh	00-59
01	Seconds Alarm	00-3Bh	00-59
02	Minutes	00-3Bh	00-59
03	Minutes Alarm	00-3Bh	00-59
04	Hours	am 12hr: 01-0Ch	01-12
		pm 12hr: 81-8Ch	129-140
		24hr: 00-17h	00-23
05	Hours Alarm	am 12hr: 01-0Ch	01-12
		pm 12hr: 81-8Ch	129-140
		24hr: 00-17h	00-23
06	Day of the Week	Sun=1: 01-07h	01-07
07	Day of the Month	01-1Fh	01-31
08	Month	01-0Ch	01-12
09	Year	00-63h	00-99

Offset	Description			
	Register Function	Bit Description		
0A	Register A	7:	UIP	Update In Progress
		6:4:	DV2-0	Divide (010=Enable oscillator & keep time)
		3:0:	RS3-0	Rate Select for Periodic Interrupt
0B	Register B	7:	SET	Inhibit Update Transfers
		6:	PIE	Periodic Interrupt Enable
		5:	AIE	Alarm Interrupt Enable
		4:	UIE	Update Ended Interrupt Enable
		3:	SQWE	No function (read/write bit)
		2:	DM	Data Mode (0= BCD; 1= Binary)
		1:	24/12	Hours Byte Format
		0:	DSE	Daylight Savings Enable
0C	Register C	7:	IRQF	Interrupt Request Flag
		6:	PF	Periodic Interrupt Flag
		5:	AF	Alarm Interrupt Flag
		4:	UF	Update Ended Flag
		3:0		Unused (always read 0)
0D	Register D	7:	VRT	Reads 1 if VBAT voltage is OK
		6:0		Unused (always read 0)
0E-7C	Software-Defined Storage Registers			
Offset	**Extended Function**	**Binary Range**		**Decimal Range**
7D	Date Alarm	01-1Fh		01-31
7E	Month Alarm	01-0Ch		01-12
7F	Century Field	13-14h		19-20

Keyboard / Mouse Wakeup Index / Data Registers

The Keyboard / Mouse Wakeup registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 2Eh and 2Fh. The registers accessed using this mechanism are used to initialize Keyboard / Mouse Wakeup functions at index values in the range of E0-EFh.

Keyboard / Mouse Wakeup initialization is accomplished in three steps:

Step 1) Enter KBC initialization mode (set D17F0 Rx51[1] = 1)

Step 2) Initialize the chip

- a) Write index to port 2Eh
- b) Read / write data from / to port 2Fh
- c) Repeat a and b for all desired registers

Step 3) Exit KBC initialization mode (set D17F0 Rx51[1] = 0)

I/O Ports Address: 2Eh
Keyboard Wakeup Index

Bit	Attribute	Default	Description
7:0	RW	0	**Index Value** D17F0 PCI configuration space register Rx51[1] must be set to 1 to enable access to the configuration registers.

I/O Ports Address: 2Fh
Keyboard Wakeup Data

Bit	Attribute	Default	Description
7:0	RW	0	**Data Value**

Keyboard / Mouse Wakeup Registers

These registers are accessed via the port 2E / 2F index / data register paired with D17F0 Rx51[1] = 1 using the indicated index values below.

Index: E0h

Keyboard / Mouse Wakeup Enable **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved** Always reads 0.
4	RO	0	**Reserved**
3	RW	1b	**Win98 Keyboard Power Key Wakeup** 0: Disable 1: Enable
2	RW	0	**Password Wakeup** 0: Disable 1: Enable
1	RW	0	**PS/2 Mouse Wakeup** 0: Disable 1: Enable
0	RW	0	**Keyboard Wakeup** 0: Disable 1: Enable

Index: E1h

Keyboard Wakeup Scan Code Set 0 **Default Value: F0h**

Bit	Attribute	Default	Description
7:0	RW	F0h	**Keyboard Wakeup First Reference Scan Code** Write 00 means that keyboard supports any key wake up.

Index: E2h

Keyboard Wakeup Scan Code Set 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Second Reference Scan Code** Write 00 means that PS/2 mouse supports any key wake up.

Index: E3h

Keyboard Wakeup Scan Code Set 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Third Reference Scan Code**

Index: E4h

Keyboard Wakeup Scan Code Set 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Fourth Reference Scan Code**

Index: E5h

Keyboard Wakeup Scan Code Set 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Fifth Reference Scan Code**

Index: E6h

Keyboard Wakeup Scan Code Set 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Sixth Reference Scan Code**

Index: E7h

Keyboard Wakeup Scan Code Set 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Seventh Reference Scan Code**

Index: E8h

Keyboard Wakeup Scan Code Set 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Keyboard Wakeup Eighth Reference Scan Code**

Index: E9h

Mouse Wakeup Scan Code Set 1 **Default Value: 09h**

Bit	Attribute	Default	Description
7:0	RW	09h	**Mouse Wakeup Scan Code Set 1**

Index: EAh

Mouse Wakeup Scan Code Set 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mouse Wakeup Scan Code Set 2**

Index: EBh

Mouse Wakeup Scan Code Mask **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Mouse Wakeup Scan Code Mask**

Memory Mapped I/O APIC Registers

The IO APIC registers are accessed by an indirect addressing scheme using Index Registers and Data Registers that are mapped into memory space.

Memory Address: FEC00000h

APIC Index **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	0	**I/O APIC Index** 8-bit pointer to the I/O APIC register.

Memory Address: FEC00010h

APIC Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**I/O APIC Data** This is a 32-bit register for the data to be read or written to the I/O APIC indirect register pointed by the Index Register.

Memory Address: FEC00020h

APIC IRQ Pin Assertion **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	WO	nnh	**IRQ Number** Bit[4:0] written to this register contain the IRQ number for this interrupt. The only valid values are 0-23.

Memory Address: FEC00040h

APIC EOI **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	WO	nnh	**Redirection Entry Clear** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the "Remote_IRR" bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC Registers

For index registers setting, please refer to Memory Address FEC00000h (APIC Index) and FEC00010 (APIC Data).

Index: 00h

I/O APIC Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RW	0	**I/O APIC Identification** Software must program this value before using the I/O APIC.
23:0	RO	0	**Reserved**

Index: 01h

I/O APIC Version **Default Value: 0017 8003h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RO	17h	**Maximum Redirection Entry** This value is equal to the number of interrupt input pins for the I/O APIC minus one. For this I/O APIC, the value is 17h.
15	RO	1b	**PCI IRQ** This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and that PCI devices are allowed to write to it to cause interrupt.
14:8	RO	0	**Reserved**
7:0	RO	03h	**APIC Version** The implementation version for this I/O APIC is 03h.

Index: 02h

I/O APIC Arbitration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RO	0	**I/O APIC Arbitration ID**
23:0	RO	0	**Reserved**

Index: 03h

Boot Configuration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Delivery Type** 0: Interrupt Delivery Mechanism is via the APIC Serial Bus. 1: Interrupt Delivery Mechanism is a Front-side Bus Message.

There are 24 64-bit I/O Redirection Table entry registers. Each register is a dedicated entry for each interrupt input signal.

Table 36. I/O Redirection Table

Index	Function	Mnemonic
11-10h	I/O APIC Redirection – APIC IRQ0	IOREDTBL0
13-12h	I/O APIC Redirection – APIC IRQ1	IOREDTBL1
15-14h	I/O APIC Redirection – APIC IRQ2	IOREDTBL2
17-16h	I/O APIC Redirection – APIC IRQ3	IOREDTBL3
19-18h	I/O APIC Redirection – APIC IRQ4	IOREDTBL4
1B-1Ah	I/O APIC Redirection – APIC IRQ5	IOREDTBL5
1C-1Dh	I/O APIC Redirection – APIC IRQ6	IOREDTBL6
1E-1Fh	I/O APIC Redirection – APIC IRQ7	IOREDTBL7
21-20h	I/O APIC Redirection – APIC IRQ8	IOREDTBL8
23-22h	I/O APIC Redirection – APIC IRQ9	IOREDTBL9
25-24h	I/O APIC Redirection – APIC IRQ10	IOREDTBL10
27-26h	I/O APIC Redirection – APIC IRQ11	IOREDTBL11
29-28h	I/O APIC Redirection – APIC IRQ12	IOREDTBL12
2B-2Ah	I/O APIC Redirection – APIC IRQ13	IOREDTBL13
2D-2Ch	I/O APIC Redirection – APIC IRQ14	IOREDTBL14
2F-2Eh	I/O APIC Redirection – APIC IRQ15	IOREDTBL15
31-30h	I/O APIC Redirection – APIC IRQ16	IOREDTBL16
33-32h	I/O APIC Redirection – APIC IRQ17	IOREDTBL17
35-34h	I/O APIC Redirection – APIC IRQ18	IOREDTBL18
37-36h	I/O APIC Redirection – APIC IRQ19	IOREDTBL19
39-38h	I/O APIC Redirection – APIC IRQ20	IOREDTBL20
3B-3Ah	I/O APIC Redirection – APIC IRQ21	IOREDTBL21
3D-3Ch	I/O APIC Redirection – APIC IRQ22	IOREDTBL22
3F-3Eh	I/O APIC Redirection – APIC IRQ23	IOREDTBL23

I/O Redirection Entry **Default Value: nnn1 nnnn nnnn nnnnh**

Bit	Attribute	Default	Description
63:56	RW	nnh	**Destination Field** In Physical Mode (bit-11=0), bits [59:56] contain an APIC ID. In Logical Mode (bit-11=1), bits [63:56] of the Destination Field specify the logical destination address. **Destination Mode IOREDTBLx[11]** — **Logical Destination Address** 0: Physical Mode — IOREDTBLx[59:56] = APIC ID 1: Logical Mode — IOREDTBLx[63:56] = Set of processors
55:17	RO	0	**Reserved**
16	RW	0	**Interrupt Mask** 0: Not Mask 1: Masked
15	RW	0	**Trigger Mode** Indicates the type of signal on the interrupt pin that triggers an interrupt. 0: Edge Sensitive 1: Level Sensitive
14	RO	0	**Remote Interrupt Request Register (IRR)** This bit is used for level triggered interrupts. Its meaning is undefined for edge triggered interrupts. For level triggered interrupts, this bit is set to 1 when local APIC(s) accept the level interrupt sent by the IOAPIC. 0: EOI message with a matching interrupt vector is received from a local APIC 1: Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)
13	RW	0	**Interrupt Input Pin Polarity** Specifies the polarity of the interrupt signal. 0: High active 1:Low active
12	RO	0	**Delivery Status** Contains the current status of the delivery of this interrupt. 0: Idle (there is currently no activity for this interrupt.) 1: Send Pending (the interrupt has been injected but its delivery is temporarily held either because the APIC bus is busy or because the receiving APIC unit can not currently accept the interrupt.)
11	RW	0	**Destination Mode** Determines the interpretation of the Destination field. 0: Physical Mode 1: Logical Mode
10:8	RW	000b	**Delivery Mode** Specify how the APICs listed in the destination field should act upon reception of this signal. 000: Fixed 001: Lowest Priority 010: SMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	RW	nnh	**Interrupt Vector** Contain the interrupt vector for this interrupt. Vector values range from 10h to FEh.

DEVICE 10 FUNCTION 0-3 (D10F0-F3): PCI UART PORT 0-3

PCI UART PCI Configuration Space

All registers in D10F0~3 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 10 and function number 0~3. All registers in this chapter are for PCI UART control.

Header Registers (00-3Fh)

Offset Address: 01-00h (D10F0-F3)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D10F0-F3)

Device ID **Default Value: F410h**

Bit	Attribute	Default	Description
15:0	RO	F410h	**Device ID Code**

Offset Address: 05-04h (D10F0-F3)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** 0: Enable interrupt 1: Disable interrupt
9	RO	0	**Fast Back to Back** Hardwired to 0. (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0. (Not supported)
7	RO	0	**Address Stepping** Hardwired to 0. (Not supported)
6	RO	0	**Parity Error Response** Hardwired to 0. 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0. (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0. (Not supported)
3	RO	0	**Respond to Special Cycle** Hardwired to 0. (Not supported)
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D10F0-F3)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase Hardwired to 0. (Not supported)
14	RW1C	0	**Signaled System Error (SERR#)** This bit must be set whenever the device asserts SERR#.
13	RW1C	0	**Received Master Abort** 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Signaled Target Abort** 0: No abort signaled 1: Transaction aborted by this chip. Hardwired to 0. (Not supported)
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Data Parity Detected** This bit only implemented by bus masters. Hardwired to 0. (Not supported)
7	RO	0	**Fast Back-to-Back Capability** 0: Device can't accept fast back-to-back transactions 1: Device can accept fast back-to-back transactions Hardwired to 0. (Not supported)
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List** 0 :No new capabilities linked list 1: Available to implement the pointer for a new capabilities linked list at Rx34 Hardwired to 1.
3	RO	0	**Interrupt Status** This read-only bit reflects the state of the interrupt in the device/function.
2:0	RO	0	**Reserved**

Note: Please refer to the PCI Local Bus Specification Revision 3.0 Chapter 6.2 for more detailed information on the PCI Commad & Status registers.

Offset Address: 08h (D10F0-F3)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-09h (D10F0-F3)

Class Code **Default Value: 07 0002h**

Bit	Attribute	Default	Description
23:0	RO	070002h	**Class Code**

Offset Address: 0Ch (D10F0-F3)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D10F0-F3)
Latency Timer **Default Value: 16h**

Bit	Attribute	Default	Description
7:0	RW	16h	**Latency Timer**

Offset Address: 0Eh (D10F0-F3)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h indicates a multi-function device.

Offset Address: 0Fh (D10F0-F3)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**BIST** Fixed at 0.

Offset Address: 13-10h (D10F0-F3)
PCI UART MMIO Register Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**PCI UART MMIO Register Base Address [31:8]**
7:0	RO	0	**Reserved**

Offset Address: 17-14h (D10F0-F3)
PCI UART IO Register Base Address **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:3	RW	0	**PCI UART IO Register Base Address [31:3]**
2:0	RO	001b	**Reserved**

Offset Address: 18-2Bh (D10F0-F3) – Reserved

Offset Address: 2D-2Ch (D10F0-F3)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor**

Offset Address: 2F-2Eh (D10F0-F3)
Subsystem ID **Default Value: F410h**

Bit	Attribute	Default	Description
15:0	RO	F410h	**Subsystem ID**

Offset Address: 30-33h (D10F0-F3) – Reserved

Offset Address: 34h (D10F0-F3)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability List Pointer**

Offset Address: 35-3Bh (D10F0-F3) – Reserved

Offset Address: 3Ch (D10F0-F3)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Interrupt Line Selection** 0000: Disable 0001: IRQ1 0010: Reserve 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Disable 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Disable 1110: IRQ14 1111: IRQ15

Offset Address: 3Dh (D10F0-3)

Interrupt Pin (D10F0) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Interrupt Pin (D10F1) **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Interrupt Pin** Fixed at 02h (INTB#).

Interrupt Pin (D10F2) **Default Value: 03h**

Bit	Attribute	Default	Description
7:0	RO	03h	**Interrupt Pin** Fixed at 03h (INTC#).

Interrupt Pin (D10F3) **Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	**Interrupt Pin** Fixed at 04h (INTD#).

Offset Address: 3E-3Fh (D10F0-F3) – Reserved

PCI UART Control Registers (40-FFh)

Offset Address: 40-6Fh (D10F0-F3) – Reserved

Offset Address: 73-70h (D10F0-F3)

UARTCFG Bakup Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:25	RW	0	**Reserved**
24	RW	0	**Function Swap Enable** Set any of D10F0~3 Rx73[0] to 1, PCI UART F0&F1 will swap with F2&F3: 0: D10F0 (UART0) will connect to UART device port 0 D10F1 (UART1) will connect to UART device port 1 D10F2 (UART2) will connect to UART device port 2 D10F3 (UART3) will connect to UART device port 3 1: D10F0 (UART0) will connect to UART device port 2 D10F1 (UART1) will connect to UART device port 3 D10F2 (UART2) will connect to UART device port 0 D10F3 (UART3) will connect to UART device port 1
23:17	RW	0	**Reserved**
16	RW	0	**Interrupt Type Select** 0: Low active 1: High active
15:1	RW	0	**Reserved**
0	RW	0	**PCI Compatible Mode Enable** When PCI UART in a PCI device, this bit will be PCI UART Compatible Control register: 0: Disable, in this case,PCI UART will in PCI DMA mode. 1: Enable, PCI UART will be in PCI compatible mode.

Table 37. PCI UART Debug Pin Selection Scheme

D10F3Rx71[0]	D10F2Rx71[0]	D10F1Rx71[0]	D10F0Rx71[0]	Debug Pin Selection	Function
0	0	0	0	DMA_DBGPIN	DMA Top signals
0	0	0	1	U0_DBGPIN	UART0 debug signals
0	0	1	0	U1_DBGPIN	UART1 debug signals
0	1	0	0	U2_DBGPIN	UART2 debug signals
1	0	0	0	U3_DBGPIN	UART3 debug signals
0	0	1	1	DBG_CCAIN	DMA CCA interface debug signals
0	1	1	1	DBG_RXDMA	DMA receiving part debug signals
1	1	1	1	DBG_TXDMA	DMA transmitting part debug signals

Offset Address: 74-7Fh (D10F0-F3) – Reserved

Offset Address: 80h (D10F0-F3)

Power Management Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D10F0-F3)

Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer: Null** 0 indicates there is no next item.

Offset Address: 83-82h (D10F0-F3)

Power Management Capability **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME# Support** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. xxxx1: PME# can be asserted from D0 xxx1x: PME# can be asserted from D1 xx1xx: PME# can be asserted from D2 x1xxx: PME# can be asserted from D3 hot 1xxxx: PME# can be asserted from D3 cold
10	RO	1b	**D2 Support** 0: Not supported 1: Supported
9	RO	1b	**D1 Support** 0: Not supported 1: Supported
8:6	RO	111b	**Aux Current (Maximum Current Required)** 111b: 375 mA
5	RO	0	**Device Specific Initialization <DSI>** 1 indicates that beyond the standard PCI configuration header, the function requires a device specific initialization sequence following transition to the D0 uninitialized state, which is before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, the driver's capabilities is used to determine this.
4	RO	0	**Reserved**
3	RO	0	**PME# Clock** 0: No PCI clock is required for the function to generate PME#. 1: The function relies on the presence of the PCI clock for PME# operation.
2:0	RO	010b	**Version** 010b: Complies with Revision 1.1 of the PCI Power Management Interface Specification.

Offset Address: 85-84h (D10F0-F3)

Power Management Capability Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME# Status**
14:9	RO	0	**Reserved**
8	RW	0	**PME# Assertion** 0: Disable PME# assertion 1: Enable PME# assertion
7:2	RO	0	**Reserved**
1:0	RW	00b	**Device Status Control** 00: D0 01: D1 10: D2 11: D3 hot

Offset Address: 86-EFh (D10F0-F3) – Reserved

Offset Address: F3-F0h (D10F0-F3)

Back Door Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RO	0	**Reserved**
1	RW	0	**Subsystem ID Register RW Control Backdoor** 0 : Subsystem ID register is RO register 1 : Subsystem ID register is RW register
0	RW	0	**Subsystem VendorID Register RW Control Backdoor** 0 : Subsystem VendorID register is RO register 1 : Subsystem VendorID register is RW register

Offset Address: F4-FFh (D10F0-F3) – Reserved

PCI UART Host Controller MMIO Registers (PCI UART-MMIO)

This section describes memory mapped I/O registers of PCI-UART. Legacy UART Registers(Rx00- 07) are also I/O registers which should be accessed through legacy mode or PCI compatible mode. The legacy registers function are the same in both modes. In this section only legacy registers of Rx00-07 are included in the MMIO descriptions.

PCI UART Base Address Register:
In legacy mode, the location is at D17F0 RxB3-B6. In PCI compatible mode, the location is at D10F0-F3 Rx14. In PCI HP/DMA mode, the location is at D10F0-F3 Rx10.

PCI UART Host Controller Legacy Registers (00-0Fh)

Offset Address: 00h (PCI UART-MMIO)

Receiver Buffer (RBUF) – For Read When DLAB (Rx03[7]) = 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Receiver Buffer** When FIFO is enabled, reading this register will retrieve data from Rx FIFO; when FIFO is disabled, the data is from the receiver buffer.

Transmitter Buffer (RBUF) – For Write When DLAB = 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	WO	0	**Transmitter Buffer** When FIFO is enabled, a write to this register will put data to Tx FIFO; when FIFO is disabled, the data will be written to transmitter buffer.

Divisor Latch Low Byte (DLLB) – When DLAB = 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Divisor Latch Low Byte**

Offset Address: 01h (PCI UART-MMIO)

Interrupt Enable Register (IER) – When DLAB = 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Modem Status Interrupt Enable** The UART will generate interrupt when modem status changes. 0: Disable 1: Enable
2	RW	0	**Receiver Line Status Interrupt Enable** The UART will generate interrupt when the receiver line status changes. 0: Disable 1: Enable
1	RW	0	**Transmitter Holding Register Empty Interrupt Enable** When set, interrupt will be generated when the transmitter buffer is empty. 0: Disable 1: Enable
0	RW	0	**Received Data Available Interrupt Enable** When set, interrupt will be generated when the receiving register/FIFO contains data ready to be read. 0: Disable 1: Enable

Divisor Latch High Byte (DLHB) – When DLAB = 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Divisor Latch High Byte**

Offset Address: 02h (PCI UART-MMIO)

Interrupt Identification Register (IIR) – When DLAB = 0 **Default Value: 01h**

Bit	Attribute	Default	Description
7:6	RO	0	**FIFO Buffer Status** 00: No FIFO 01: FIFO Enable but Unusable 10: Reserved 11: FIFO Enable
5:4	RO	0	**Reserved**
3	RO	0	**Time-out Interrupt Pending** 0: No time-out interrupt 1: 16550 time-out interrupt pending
2:1	RO	0	**Interrupt Occurred Status** 00: Modem Status Interrupt 01: Transmitter Holding Register Empty Interrupt 10: Received Data Available Interrupt 11: Receiver Line Status Interrupt When interrupt occurred, its status will be shown in bits 1 and 2. These interrupts work on a priority status. The Line Status Interrupt has the highest priority, followed by the Data Available Interrupt, then the Transmit Register Empty Interrupt and then the Modem Status Interrupt which has the lowest priority.
0	RO	1b	**Interrupt Pending Status** This bit shows whether an interrupt has occurred or not. 0: Interrupt pending 1: No interrupt pending

FIFO Control Register (FCR) – When DLAB = 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	WO	0	**Interrupt Trigger Level Control** 00: 1 Byte 01: 4 Bytes 10: 8 Bytes 11: 14 Bytes
5:3	WO	0	**Reserved**
2	WO	0	**Clear Transmit FIFO** Set to 1 will clear the content of the Transmot FIFO.
1	WO	0	**Clear Receive FIFO** Set to 1 will clear the contents of the Receive FIFO. Setting bit1 and bit 2 to 1 will only clear the content of the FIFO and the shift register won't be affected. These two bits are self resetting, thus there is no need to set the bits to '0' when finished.
0	WO	0	**Enable FIFOs** Bit 0 enables the operation of the receive and transmit FIFOs. Writing a '0' to this bit will disable the operation of receive and transmit FIFOs, thus all data stored in these FIFO buffers will be lost.

Offset Address: 03h (PCI UART-MMIO)

Line Control Register (LCR) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Divisor Latch Access Bit <DLAB> or Transceiver Buffer Control** 0: Access to Receiver buffer, Transmitter buffer & Interrupt Enable Register 1: Divisor Latch Access Bit If this bit is set, Transceiver Buffer and IER cab be accessed to set the Divisor Latch Access Bit (DLAB), by which we can get commonly used baud rate. If this bit is not set, the function of IER and Receiver Buffer or Transmitter Holding Buffer is used when respectively read or write.
6	RW	0	**Set Break Enable** This bit sets break enable. When active, the TD line goes into "Spacing" state, which causes a break in the receiving UART. 0: Disable 1: Enable
5:3	RW	0	**Parity Selection** xx0: No parity 001: Odd parity 011: Even parity 101: Space parity (sticky) 111: Mark parity (sticky) Others: Reserved
2	RW	0	**Stop Bit Length** 0: One stop bit 1: Two stop bits for word length of 6,7 or 8 bits or 1.5 stop bits for word length of 5 bits. Note that the receiver only checks the first stop bit.
1:0	RW	0	**Word Length** 00: 5 Bits 01: 6 Bits 10: 7 Bits 11: 8 Bits

Offset Address: 04h (PCI UART-MMIO)

Modem Control Register (MCR) **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Loopback Mode** In this mode any data which is placed in the transmitter registers for output is received by the receiver circuitry on the same chip and is available at the receiver buffer. This can be used to test the UART operation.
3	RW	0	**Aux Output 2** Aux Output 2 can be connected to external circuitry which controls the UART-CPU interrupt process.
2	RW	0	**Aux Output 1** Aux Output 1 is normally disconnected, but on some cards, it is used to switch between a 1.8432MHZ crystal to a 4MHZ crystal which is used for MIDI.
1	RW	0	**Force Request to Send** Setting this bit to 1 makes the Request To Send line active.
0	RW	0	**Force Data Terminal Ready** Setting this bit to 1 makes the Data Terminal Ready line active.

Offset Address: 05h (PCI UART-MMIO)

Line Status Register (LSR) **Default Value: 60h**

Bit	Attribute	Default	Description
7	RO	0	**Error in Receiver FIFO** This bit is high when at least one break, parity or framing error has occurred on a byte which is contained in the FIFO.
6	RO	1b	**Empty Data Holding Registers** When this bit is set, both the transmitter holding register and the shift register are empty. This indicates that no serial conversions are taking place so there should be no activity on the transmit data line.
5	RO	1b	**Empty Transmitter Holding Register** When this bit is set, the transmitter holding register is empty, thus another byte can be sent to the data port, but a serial conversion using the shift register may be taking place. The UART's holding register holds the next byte of data to be sent in parallel fashion. The shift register is used to convert the byte to serial, so that it can be transmitted over one line.
4	RO	0	**Break Interrupt** The break interrupt occurs when the received data line is held in a logic state '0' (Space) for more than the time it takes to send a full word. That includes the time for the start bit, data bits, parity bits and stop bits.
3	RO	0	**Framing Error** A framing error is set when the last bit is not a stop bit. This is commonly encountered while transfer data by null modem between two ports with different speed.
2	RO	0	**Parity Error** A Parity Error is set when the parity error has occurred.
1	RO	0	**Overrun Error** An Overrun Error is set when the overrun has occurred. An overrun error normally occurs when your program can't read from the port fast enough. If you don't get an incoming byte out of the register fast enough, and another byte just happens to be received, then the last byte will be lost and a overrun error will result.
0	RO	0	**Data Ready** Data Ready is set when a byte has been received by the UART and is at the receiver buffer ready to be read.

Offset Address: 06h (PCI UART-MMIO)

Modem Status Register (MSR) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Carrier Detect** This bit shows the current state of the data line DCD.
6	RO	0	**Ring Indicator** This bit shows the current state of the data line RI.
5	RO	0	**Data Set Ready** This bit shows the current state of the data line DSR.
4	RO	0	**Clear To Send** This bit shows the current state of the data line CTS.
3	RO	0	**Delta Data Carrier Detect** This bit shows a change in DCD line. Delta means that there was a change in the related lines, since the last read of this register.
2	RO	0	**Trailing Edge Ring Indicator** The assertion of bit2 indicates that there was a transformation from low to high state on the Ring Indicator line.
1	RO	0	**Delta Data Set Ready** This bit shows a change in DSR line.
0	RO	0	**Delta Clear to Send** This bit shows a change of CTS line.

Offset Address: 07h (PCI UART-MMIO)

Scratch Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Register** This register is not used for communications but rather used as a place to leave a byte of data. The only real use it has is to determine whether the UART is a 8250/8250B or a 8250A/16450 and even that is not very practical today as the 8250/8250B was never designed for AT's and can't hack the bus speed.

Offset Address: 08-0Fh(PCI UART-MMIO) – Reserved

PCI UART Host Controller HP/DMA Registers (10-7Fh)

Offset Address: 13-10h (PCI UART-MMIO)

PCI UART FIFO Write Access **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	WO	0	**PCI UART FIFO Write Access** Write data to FIFO directly when there is no DMA active in HP/DMA mode. When in PCI HP/DMA mode, the write buffer at I/O Base Address register offset 0 will be discarded. If CPU wants to do transaction by PIO, it can write data to UART Host controller FIFO directly by writing to this register.

Offset Address: 17-14h (PCI UART-MMIO)

PCI UART FIFO Read Access **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**PCI UART FIFO Read Access** Read data from FIFO directly when there is no DMA active in HP/DMA mode. When in PCI HP/DMA mode, the read buffer at I/O Base Address register offset 0 will be discarded. If CPU wants to do transaction by PIO, it can read data from UART Host controller FIFO directly by reading this register.

Offset Address: 1B-18h (PCI UART-MMIO)

PCI UART Received Data Length **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:20	RO	0	**Reserved**
19:16	RO	0	**PCI UART Receiver FIFO Length** Data length in Receiver FIFO. Software may use this register to know how many data remained in the Host Controller Receiver FIFO. In the PIO mode, software should use this value to decide how many data should be read.
15:0	RW1C	0	**PCI UART Received Data Length** Total received data length. Software may use this register to determine whether there is data remained in FIFO when using PIO mode. Writing any data to it will clear its value and FIFO pointer.

Offset Address: 1C-1Fh(PCI UART-MMIO) – Reserved

Offset Address: 23-20h (PCI UART-MMIO)

PCI UART DMA-A Address for Transmission **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI UART DMA-A Start Address for Transmission** DMA-A address for transmission while DMA in Ping-Pang mode. A write to this register will cause TX DMA-A be ready to transmit. If Transmission DMA Enable (Rx30[0]) is set, the data transfer will start. Under such condition, the UART slot will issue a request to DMA engine and then the transmitting will be triggered.

Offset Address: 27-24h (PCI UART-MMIO)

PCI UART DMA-A Data Length for Transmission **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**PCI UART DMA-A Data Length for TX** Indicates the data length for transmission while DMA-A in Ping-Pang mode.

Offset Address: 2B-28h (PCI UART-MMIO)

PCI UART DMA-B Address for Transmission **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI UART DMA-B Start Address for Transmission** DMA-B address for transmission while DMA in Ping-Pang mode. A write this register will cause TX DMA-B be ready to transmit. If Transmission DMA Enable (Rx30[0]) is set, the data transfer will start. Under such condition, the UART slot will issue a request to DMA engine and then the transmitting will be triggered.

Offset Address: 2F-2Ch (PCI UART-MMIO)

PCI UART DMA-B Data Length for Transmission **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**PCI UART DMA-B Data Length for Transmitter** Indicates the data length for transmission while DMA-B in Ping-Pang mode.

Note: When transmitting, software should configure one set of address and length register. Then enable Transmitter Control Register[0](Rx30). In theory, software can configure either DMA-A firstly or DMA-B firstly. If the address and length is not configured completed, DMA Enable (Transmitter Control Register[0]) cannot be asserted.

Offset Address: 33-30h (PCI UART-MMIO)

PCI UART Transmitter Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Transmitter DMA One-shot Timer Value** If TX One-shot Timer Enable and TX One-shot Interrupt Enable are set, an interrupt will be triggerd when the timer is matched to this value.
15:9	RW	0	**Reserved**
8	RW	0	**Transmitter DMA One-shot Timer Enable** 0: Disable 1: Enable
7:2	RW	0	**Reserved**
1	RW	0	**Transmitter Flow Control Enable** When enabled, TX flow control will be working. When CTS is inactive, transmitter will be halted. Unless reset, when CTS is active then, transmission will be resuming. 0: Disable 1: Enable
0	RW	0	**Transmitter DMA Enable** When enabled, transmitter DMA should be used. When disabled, if there is DMA transaction, TXDMA will discard request to memory and send data remained in PCI UART to device. 0: Disable 1: Enable

Offset Address: 34-3Fh(PCI UART-MMIO) – Reserved

Offset Address: 43-40h (PCI UART-MMIO)

PCI UART DMA-A Address for Receiving **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI UART DMA-A Start Address for Receiving** DMA-A address for receiving while DMA in Ping-Pang mode. A write to this register will cause RX DMA-A be ready to receive. If Receiver DMA Enable (Rx50[0]) is set, the data receiving will start. Under such condition, the UART slot will issue a request to DMA engine when the trigger level is arrived.

Offset Address: 47-44h (PCI UART-MMIO)

PCI UART DMA-A Data Length for Receiving **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**PCI UART DMA-A Data Length for Receiving** Indicates the data length for receiving while in DMA-A Ping-Pang mode.

Offset Address: 4B-48h (PCI UART-MMIO)

PCI UART DMA-B Address for Receiving **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI UART DMA-B Start Address for Receiving** DMA-B address for receiving while DMA in PingPang mode. A write to this register will cause RX DMA-A be ready. If Receiver DMA Enable (Rx50[0]) is set, the data receiving will start. Under such condition, the UART slot will issue a request to DMA engine when the trigger level is arrived.

Offset Address: 4F-4Ch (PCI UART-MMIO)

PCI UART DMA-B Data Length for Receiving **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**PCI UART DMA-B Data Length for Receiving** Indicates the data length for receiving while in DMA-B Ping-Pang mode.

Note: When receiving, software should configure one set of address and length register. Then enable RXDMA Control Register[0] (Rx50). In theory, software can configure either DMA-A firstly or DMA-B firstly. If the address and length is not configured completely, Receiver DMA Enable (Rx50[0]) cannot be asserted.

Offset Address: 53-50h (PCI UART-MMIO)

PCI UART Receiver DMA Control Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Receiver DMA One-shot Timer Value** The value will be programmed by software. If RX One-shot timer enable and RX One-shot interrupt enable are set, an interrupt will be triggerd when the timer is match to this value.
15:9	RW	0	**Reserved**
8	RW	0	**Receiver DMA One-shot Timer Enable** 0: Disable 1: Enable
7:2	RW	0	**Reserved**
1	RW	0	**Receiver Flow Control Enable** When enabled, RX flow control will be working and make RTS inactive when receiver FIFO is full or errors occurred. 0: Disable 1: Enable
0	RW	0	**Receiver DMA Enable** When enabled, receiver DMA should be used. When disabled, if there is DMA transaction, RXDMA will not accept data from slot and send current data in DMA engine to memory. 0: Disable 1: Enable

Offset Address: 57-54h (PCI UART-MMIO)

PCI UART Receiver DMA Control High **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:20	RW	FFFh	**DMA Timeout Value** The value means the period of times of one bit data in UART bus. If there is no new data coming to FIFO during receiving before timer reaches the value, the UART controller will send all received data to system memory without waiting.
19	RW	0	**DMA Timeout Event Enable** Refer to PCI UART Receiver DMA Control High[31:20] for DMA Timeout function details. Note: While in DMA mode, this bit should be always configured to 1'b1; otherwise, data transfer may be wrong. While in PCI-Compatible or HP PIO access, this function can be ignored. 0: Disable 1: Enable
18:13	RW	0	**Reserved**
12:9	RW	0	**Urgent DMA Request Level** If the number of the received data is more than this value, a DMA urgent request will be sent.
8	RW	0	**Urgent DMA Request Level Control** 0: Disable, determined by hardware automatically 1: Enable, configured by software
7:5	RW	0	**Reserved**
4:1	RW	0	**Normal DMA Request Level** If the number of the received data is more than its value, a DMA request will be sent.
0	RW	0	**Normal DMA Request Level Control** 0: Disable, determined by hardware automatically 1: Enable, configured by software

Offset Address: 5F-58h (PCI UART-MMIO)

PCI UART High Baud Rate Control Low **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:4	RW	0	**Reserved**
3:0	RW	0	**PCI UART Baud Rate Multiplier** This register value will control PCI UART high baud rate. It will be working together with Divisor Latch Bit. Details shows in below table.

Note: Baud rate generation by Divisor Latch Bit and Multiplier cooperation.

1. When in legacy mode or PCI compatible mode, PCI UART should be fully compatible with legacy UART(16550A). So PCI UART Baud rate Multiplier should be set to 0, which will indicate that PCI UART High Baud Rate Control disable. Then PCI UART can use baud rate by configuration of Divisor Latch Bit, just like legacy UART.

2. When in DMA mode, for baud rate lower than 115200bps, please disable PCI UART High Baud Rate Control and configure PCI UART Divisor Latch Bit, just like legacy mode. For high speed, please configure PCI UART High Baud Rate Control to special value. While Multiplier is not 0, Divisor Latch Bit will be ignored. The relationship between PCI UART High Baud Rate Control and baud rate is shown in Table 38 below.

Table 38. PCI UART High Baud Rate Control

Divisor	Multiplier	n	PCI UART Baud Rate (bps)
96	0	1/96	1200
48	0	1/48	2400
24	0	1/24	4800
12	0	1/12	9600
6	0	1/6	19200
3	0	1/3	38400
2	0	1/2	57600
1	0	1	115200
-	1	4	460800
-	2	8	921600
-	3	12	1382400
-	4	16	1843200
-	5	20	2304000
-	6	24	2764800
-	7	28	3225600
-	8	32	3686400
-	9	36	4147200
-	10	40	4608000
-	11	44	5068800

Offset Address: 63-60h (PCI UART-MMIO)

PCI UART TXDMA Current Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**PCI UART TXDMA Current Address** Current DMA transmitting address information. This address is the current address of transaction in DMA engine, if DMA transmission is done, the register will keep record of the last version address.

Offset Address: 67-64h (PCI UART-MMIO)

PCI UART TXDMA Current Length **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**PCI UART TXDMA A Current Length** Current DMA transmitting length information when DMA ends, which will always be the TX DMA _A length when the last DMA ends.
15:0	RO	0	**PCI UART TXDMA B Current Length** This register will show TXDMA B current remained data length. If TXDMA B transmission is done, it will always be the TX DMA B length when the last DMA ends.

Offset Address: 6B-68h (PCI UART-MMIO)

PCI UART RXDMA Current Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**PCI UART RXDMA Current Address** Current DMA receiving address information. This address is current address of transaction in DMA engine, not including receive data in uart slots.

Offset Address: 6F-6Ch (PCI UART-MMIO)

PCI UART RXDMA Current Length **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**PCI UART RXDMA_B Current Length** Current DMA receiving length information when DMA ends, which will always be the RX DMA_B length when the last DMA ends.
15:0	RO	0	**PCI UART RXDMA_A Current Length** Current DMA receiving length information, when DMA ends, which will always be the RX DMA_A length when the last DMA ends.

Offset Address: 73-70h (PCI UART-MMIO)

PCI UART DMA Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:2	RO	0	**RXDMA State** When PCI UART is in DMA transaction, RXDMA state will show Receiving DMA state when DMA ends. Software can know current RXDMA state via this register. 00: RX DMA is idle, no receiving via DMA 01: RX DMA is in DMA_A state, which address and length is set by Rx40 and Rx44 10: RX DMA is in DMA_B state, which address and length is set by Rx48 and Rx4C 11: Reserved
1:0	RO	0	**TXDMA State** When PCI UART is in DMA transaction, TXDMA state will show Transmitting DMA state when DMA ends. Software can know current TXDMA state via this register. 00: TX DMA is idle, no receiving via DMA 01: TX DMA is in DMA_A state, which address and length is set by Rx20 and Rx24 10: TX DMA is in DMA_B state, which address and length is set by Rx28 and Rx2C 11: Reserved

Offset Address: 74-77h(PCI UART-MMIO) – Reserved

Offset Address: 7B-78h (PCI UART-MMIO)

PCI UART Normal Interrupt Enable DMA Mode **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Reserved**
7	RW	0	**Receiver One-shot Interrupt Enable** 0: Disable 1: Enable
6	RW	0	**Transmitter One-shot Interrupt Enable** 0: Disable 1: Enable
5	RW	0	**Parity Check Error Interrupt Enable** 0: Disable 1: Enable
4	RW	0	**FIFO Overrun Interrupt Enable** 0: Disable 1: Enable
3	RW	0	**Data Receiving Complete Interrupt Enable** 0: Disable 1: Enable
2	RW	0	**DMA Receiving Interrupt Enable** 0: Disable 1: Enable
1	RW	0	**Data Transmission Complete Interrupt Enable** 0: Disable 1: Enable
0	RW	0	**DMA Transmission Interrupt Enable** 0: Disable 1: Enable

Offset Address: 7F-7Ch (PCI UART-MMIO)

PCI UART Normal Interrupt Status Under DMA **Default Value: 0000 00000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
9	RW1C	0	**FIFO Overrun Interrupt** It is set when there is no space to receiving data. The coming data will be lost.
8	RW1C	0	**Parity Check Error** It is set when parity check is wrong during receiving.
7	RW1C	0	**Receiver One-shot Interrupt** When receiver data length match value in Rx50[31:16] and Receiver One-shot interrupt enable set, interrupt will be generated.
6	RW1C	0	**Data Receiving Complete Interrupt** It is set when DMA FIFO empty, which means all data are transferred to system memory.
5	RW1C	0	**DMA-B Receiving Interrupt** It is set when PCI UART DMA-B data length for TX (Rx4C) reaches zero or timeout. If there is more data to be received, software should reconfigure DMA address and data length for receiving.
4	RW1C	0	**DMA-A Receiving Interrupt** It is set when PCI UART DMA-A data length for TX (Rx44) reaches zero or timeout. If there is more data to be received, software should reconfigure DMA address and data length for receiving.
3	RW1C	0	**Transmitter One-shot Interrupt** When transmitter send data length match value in Rx30[31:16] and Transmitter One-shot interrupt enable set, interrupt will be generated
2	RW1C	0	**Data Transmission Complete Interrupt** It is set when all data are transferred to UART bus.
1	RW1C	0	**DMA-B Transmission Interrupt** It is set when PCI UART DMA-B data length for RX (Rx2C) reaches zero. If there is more data to be transferred, software may reconfigure DMA address and data length for transmission.
0	RW1C	0	**DMA-A Transmission Interrupt** It is set when PCI UART DMA-A data length for RX (Rx24) reaches zero. If there is more data to be transferred, software may reconfigure DMA address and data length for transmission.

DEVICE 11 FUNCTION 0 (D11F0): USB DEVICE

This chip can work as a mass storage USB device. Four endpoints are supported, they are: Control endpoint, Bulk In endpoint, Bulk Out endpoint and Interrupt In endpoint.

PCI Configuration Space

All registers in D11F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 11 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D11F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D11F0)

Device ID **Default Value: A409h**

Bit	Attribute	Default	Description
15:0	RO	A409h	**Device ID Code** Fixed at A409h if Rx41[1] = 0.

Offset Address: 05-04h (D11F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidation Enable** 0: Disable 1: Enable
3	RO	0	**Reserved**
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D11F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8:0	RO	010h	**Fixed at 10h (for PCI PMI)**

Offset Address: 08h (D11F0)

Revision ID **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Revision ID**

Offset Address: 0B-09h (D11F0)

Class Code **Default Value: 02 8000h**

Bit	Attribute	Default	Description
23:0	RO	028000h	**Class Code** 028000h indicates the Network Controller.

Offset Address: 0Ch (D11F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D11F0)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Latency Timer**

Offset Address: 0Eh (D11F0)

Header Type Default **Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D11F0)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 0.

Offset Address: 13-10h (D11F0)
VIACOM MMIO Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RW	0	**Corresponding to AD[31:11]**
10:3	RO	0	**Reserved**
2:1	RO	0	**Memory Mapping** 00: 32-bit space 10: 64-bit space Others: Reserved
0	RO	0	**Reserved**

Offset Address: 14-2Bh (D11F0) – Reserved

Offset Address: 2D-2Ch (D11F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D11F0)
Subsystem ID **Default Value: A409h**

Bit	Attribute	Default	Description
15:0	RO	A409h	**Subsystem ID**

Offset Address: 30-33h (D11F0) – Reserved

Offset Address: 34h (D11F0)
Power Management Capability **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Power Management Capability** Fixed at 80h.

Offset Address: 35-3Bh (D11F0) – Reserved

Offset Address: 3Ch (D11F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**USB Interrupt Routing** The high 4 bits have no effect. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disabled

Offset Address: 3Dh (D11F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3E-3Fh (D11F0) – Reserved

USB PHY And MAC Control (40-7Fh)

Offset Address: 40h (D11F0)

Debug Signal Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:1	RW	000b	**Debug Signal Group Select** 000: Endpoint 0 DMA debug signal 001: Endpoint 1 DMA debug signal 010: Endpoint 2 DMA debug signal 011: Endpoint controller debug signal 100: PHY debug signal 101: HS MAC debug signal 110: FS MAC debug signal 111: Port state debug signal
0	RW	0	**Debug Signal Enable** 0: Disable 1: Enable

Offset Address: 41h (D11F0) – Reserved

Offset Address: 42h (D11F0)
Miscellaneous Control 1 **Default Value: 24h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:0	RW	24h	**USB 1.1 Full Speed (FS) Timeout Parameter** In FS mode, this register is used to control timeout period with the 80ns unit.

Offset Address: 43h (D11F0)
PHY Signal Monitoring 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**15K Pull-up Resistor Enable** This bit enables the connection of 15K pull-up resistor and is valid if bit 5 is set. 0: Disconnect 1: Connect
6	RW	0	**45-Ohm Termination Resistor Enable** This bit enables the connection of 45-ohm termination resistor and is valid if bit 5 is set. 0: Disconnect 1: Connect
5	RW	0	**PHY Resistor Manual Control Enable** This bit enables the control of 45-ohm termination resistor and 15K pull-up resistor via software instead of hardware. 0: Hardware auto mode 1: Manual mode
4	RW	0	**Enable Switch2 Pull-Up** 0: Disconnect switch2 pull-up resistor 1: Connect switch2 pull-up resistor
3:2	RW	00b	**PULL_ON_SW2 Type Select** 00: Connect switch2 pull-on resistor when bus signal changes from 1 to 0 01: When active (from 1 to 0 or 0 to 1) 10: Always disconnect 11: Always connect
1	RW	0	**Reserved**
0	RW	0	**Device Port PHY Signal Monitor Enable** 0: Disable 1: Enable

Offset Address: 44h (D11F0)
PHY Signal Monitoring 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**RxData** 0: RxData = 0 1: RxData = 1
2	RO	0	**Squelch Detection** 0: No squelch 1: Squelch detected
1	RO	0	**45-Ohm Termination Impedance Detection** 0: Not detected (connected as full/low speed) 1: Detected (connected as high speed)
0	RO	0	**USB Bus Line D+ Pull-up Detection** 0: Not detected 1: Detected

Offset Address: 45h (D11F0)
Miscellaneous Control 2 **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	1b	**USB 2.0 EOP Pattern/PHY Data Buffer Error Check Disable** 0: Enable check 1: Disable check
6	RW	0	**Reserved**
5	RW	1b	**Disable CCA Burst Access** 0: Enable burst 1: Disable burst
4	RW	0	**Sync-Fast Option** 0: Disable 1: Enable
3	RW	0	**Sync-Jend Option** 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 46h (D11F0)
Miscellaneous Control 3 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Clock Auto-Stop Enable** 0: Disable auto-stop 1: Enable auto-stop
6	RW	0	**CRC Received Token Check** 0: Enable check 1: Disable check
5	RW	0	**Hardware Auto-Reset Device Address on USB Reset** 0: Auto reset device address 1: Not reset
4:1	RW	0	**Reserved**
0	RW	0	**USB Transceiver Macrocell (UTM) Auto-Check Enable** 0: Disable 1: Enable

Offset Address: 47h (D11F0)
Miscellaneous Control Register 4 **Default Value: 38h**

Bit	Attribute	Default	Description
7:4	RW	3h	**Pull-up Resistor Fine Tune (No Effect)**
3:0	RW	8h	**Termination Resistor Fine Tune**

Offset Address: 48-49h (D11F0) – Reserved

Offset Address: 4Ah (D11F0)
MAC Turn Around Time **Default Value: 09h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	9h	**USB 2.0 MAC Transmit Turn Around Time** High Speed turn around time with the 16ns unit.

Offset Address: 4Bh (D11F0)
High Speed (HS) MAC Receiver Delay Control **Default Value: 61h**

Bit	Attribute	Default	Description
7:4	RW	6h	**Receiver Delay Time After TX Packet (Unit: 16ns)**
3:0	RW	1h	**Receiver Delay Time Between Two Consecutive Rx Packets (Unit: 16ns)**

Offset Address: 4Ch (D11F0)

Function Patch Enable **Default Value: 65h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**LS Packet Cause FS Packet Timeout Error Patch** 0: Disable 1: Enable
5	RW	1b	**Hardware Attach Process Evaluation Enable** 0: Disable 1: Enable
4	RW	0	**Bulk Endpoint NYET Response Enable** The NYET is a token defined by USB 2.0 spec to indicate device busy. 0: Disable 1: Enable
3	RW	0	**USB 1.1 EOP Issue Patch Disable** 0: Enable patch 1: Disable patch
2	RW	1b	**Force RXACTIVE to Deassert on BABBLE Occur to Prevent System Hang** 0: Disable 1: Enable
1	RW	0	**Disable Patch Unsafe BULK DMA Pause** 0: Enable 1: Disable
0	RW	1b	**CRC16 Even Data Toggle Mismatch Check Enable** 0: Disable 1: Enable

Offset Address: 4Dh (D11F0)

Test Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Enable Eye-Pattern Test Mode** Set this bit to generate continuously toggled pattern to FS test for eye-pattern characterization. 0: Disable 1: Enable
4	RO	0	**UTM Error Auto Check** This bit indicates UTM auto check in loop-back mode error status. 0: No error found 1: Data check error
3	RW	0	**HS Eye Test** 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 4Eh (D11F0)

USB 2.0 MAC Timeout **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RW	60h	**USB 2.0 Receive Timeout Parameter** The unit is byte time. According to the core spec, the host controller or a device expecting a response to a transmission must not timeout the transaction if the inter-packet delay is within 736 and 816 bit times. The worst round trip delay is 721 bit times.

Offset Address: 4Fh (D11F0)

PHY Control 1 **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RW	00b	**External Current Source Increment** 00: No increment 01: 1% 10: 2 % 11: 4%
5:4	RW	10b	**125mv Squelch Level Fine Tune** 00: 100mv 01: 112.5mv 10: 125mv 11: 137.5mv
3	RW	0	**PLLTEST Output** 0: 48MHz 1: 60MHz
2	RW	0	**HS Transmitter** Used for HS transmitter, no DPLL. 0: Normal 1: Rise / fall time increase 100ps
1:0	RW	00b	**DPLL Input Data Delay Select** 00: 0ps 01: -43~-135ps 10: 43~135ps 11: 86~270ps

Offset Address: 50h (D11F0)

PHY Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reset DPLL for BIST** 0: No work 1: Reset
6	RW	0	**Different Test Pattern for DPLL BIST** 0: Off 1: 1T pulse-shift
5	RW	0	**Different Test Pattern for DPLL BIST** 0: Off 1: 1T duty-offset
4	RW	0	**Different Test Pattern for DPLL BIST** 0: Off 1: 1T phase shift
3	RW	0	**DPLL Receive Data Out (RDOUT[4:0]) Output Enable** 0: Disable 1: Enable
2	RO	0	**DPLL BIST Pattern Match Flag** 0: Error 1: Success
1	RW	0	**FS Tx Test** 0: Disable 1: Enable
0	RO	0	**FS Rx Test** 0: Disable 1: Enable

Offset Address: 51h (D11F0)

PHY Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**DPLL Test Mode Observed Signals (RDOUT[4:0])**
2:0	RO	0	**Reserved**

Offset Address: 52h (D11F0)

PHY Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Device Suspend Disable** For test purpose. 0: Normal mode 1: Disable suspend
5:4	RW	0	**Reserved**
3	RW	0	**DPLL Loopback Enable** 0: Disable 1: Enable
2	RW	0	**HS Transmission Test**
1:0	RW	0	**Reserved**

Offset Address: 53h (D11F0)

PHY Control 5 **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**PHY Auto Power-down Disable** If this bit is asserted, and when the port is suspended, the port will auto power-down. 0: Auto power-down 1: Disable auto power-down
6:3	RW	0001b	**Reserved (Do Not Program)**
2	RW	0	**PHY APLL Auto Power Down Enable** 0: Disable 1: Enable
1:0	RW	00b	**DPLL Non-Squelch (NSQ) Offset Set Reg** 00: 0ps 01: -43~-135ps 10: 43~135ps 11: 86~270ps

Offset Address: 54h (D11F0)

PHY Control 6 **Default Value: 17h**

Bit	Attribute	Default	Description
7	RW	0	**Input Data Control (FASTSTART)** Set this bit 1 may cause HsRxAck HSRXACT_DEV (PHYUSB20DEV) assert later than PHY_RxData_o RXDATA_O (PHYUSB20DEV), so Rx valid will be lost (Drop DP). 0 Disable 1 Enable
6:5	RW	0	**Reserved**
4	RW	1b	**Fast Lock** 0: Disable 1: Enable
3:2	RW	01b	**DPLL Track Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)
1:0	RW	11b	**DPLL Lock Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)

Offset Address: 55h (D11F0)
New USB 1.1 and USB 2.0 PHY Test Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**HS Test Enable** 0: Disable 1: Enable
4	RW	0	**USB 2.0 Test Packet External Input Mode Enable** 0: Disable 1: Enable
3	RW	0	**USB 2.0 Test Packet Auto Compare Enable** 0: Disable 1: Enable
2:0	RW	000b	**Test Packet Mode** 000: Disable 100: USB 2.0 test packet mode 101: Incremental data of 16 bytes index starting from 0 110: Incremental data of 256 bytes index starting from 0 111: Incremental data of 1024 bytes index starting from 0

Offset Address: 56h (D11F0)
New USB 1.1 and USB 2.0 PHY Test Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**USB2.0 Auto Compare Data Detect Status** 0: No data 1: Data detected
2	RO	0	**USB2.0 Auto Compare Error Status** 0: No error 1: Rx/Tx data compare error
1	RO	0	**USB2.0 Auto Compare Timeout Error Status** 0: No error 1: Timeout error in receiving Rx data
0	RO	0	**USB2.0 Auto Compare EOP Error Status** 0: No error 1: Unable to detect Rx data EOP

Offset Address: 57-5Fh (D11F0) – Reserved

Offset Address: 61-60h (D11F0)
Subsystem ID Back Door **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	**Subsystem ID Back Door** When Rx41[3] is set to 1, the value of Rx2F-2E is from this register

Offset Address: 63-62h (D11F0)
Subsystem Vendor ID Backdoor **Default Value: A409h**

Bit	Attribute	Default	Description
15:0	RW	A409h	**Subsystem Vendor ID Back Door** When Rx41[3] is set to 1, the value of Rx2D-2C is from this register.

Offset Address: 64-7Fh (D11F0) – Reserved

USB Power Management (80-FFh)

Offset Address: 80h (D11F0)

USB Device Power Management Capabilities ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**USB Device Power Management Capabilities ID** The Capability Identifier, when read by system software as 01h, indicates that the data structure currently being pointed to is the PCI Power Management data structure.

Offset Address: 81h (D11F0)

Next Linked Item **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Linked Item**

Offset Address: 83-82h (D11F0)

Power Management Capabilities **Default Value: 7E02h**

Bit	Attribute	Default	Description
15:0	RO	7E02h	**Power Management Capabilities**

Offset Address: 85-84h (D11F0)

Power Management Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME Status** 0: De-active 1: Active
14:9	RO	0	**Reserved**
8	RW	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State** For PHY, D0~D3 states are the same. Power will shut down and be disconnected in D3 state. 00: D0 01: D1 10: D2 11: D3

Offset Address: 86-FFh (D11F0) – Reserved

VIA USB Device Memory-Mapped I/O Registers (USBD-MMIO)

VIA USB Communication Capability and Shadow Registers (00-0Fh)

Offset Address: 00h (USBD-MMIO)

Capability Register **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Capability Register Length**

Offset Address: 01h (USBD-MMIO)

Interface Version **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Interface Version Number**

Offset Address: 02-0Fh (USBD-MMIO) – Reserved

VIA USB Device Controller Operational Registers (10-1Fh)

Offset Address: 13-10h (USBD-MMIO)

Controller Register **Default Value: 0020 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Device Address Change** On change device address, this bit must be set for status phase decoding. This bit is cleared by hardware when next setup command is received. When this bit is 1, hardware will decode both old address and the newly changed address. Note that when modifying the device address, this bit must also be set.
30:24	RW	0	**Device Address** These bits specify the device address. Default value is 00h. These bits are reset to default value on receiving USB bus reset when D11F0 Rx46[5] is 0. This bit is also programmed by software after address setup procedure completes.
23	RW	0	**Manual Control for PHY Power** 0: Hardware control 1 Manual control
22	RW	0	**PHY Power On** This bit is valid only when bit-23 is 1b. 0: Power off 1: Power on
21	RO	1b	**Self-Powered Device** If the device is in self-powered configuration, set this bit to one for connection determination. 0: Bus-powered 1: Self-powered
20	RW	0	**HS / FS Support** This bit disables the device controller high-speed support, default is set to support high-speed. 0: HS supported 1: FS supported
19	RW	0	**Device Force Resume** This bit forces the suspended device port to issue resume signal to wakeup the host, and the hardware clears this bit automatically after software set this bit. Set this bit must check the suspension status first.
18	RW	0	**Software Ready** After USBD is plugged to the HOST, Software may need to do some operation. When software is ready, write this bit to 1. Then USBD will do attach operation. 0: Not ready 1: Ready
17	RW	0	**Controller Reset** Write a one to this bit resets device controller. This bit is set to zero by controller when reset process is complete.
16	RW	0	**Run/Stop** Set this bit enables device controller operation, including Host/Device negotiation and endpoint DMA. 0: Stop 1: Run
15	RW	0	**PIO Enable** 0: Disable 1: Enable
14	RW	0	**Prevent the System Entering from C1~C4 States** 0: Disable 1: Enable
13	RW	0	**CCA Interface Selection** 0: Select register out CCA interface 1: Select original CCA interface
12:0	RO	0	**Reserved**

Offset Address: 15-14h (USBD-MMIO)

Device Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RW1C	0	**Device Port Bus Resume Detected** This bit indicates that the controller has detected bus host resume status. 0: No resume detected 1: Host resume detected
6	RW1C	0	**Device Port Bus Suspend Detected** This bit indicates that the controller has detected bus suspend status. 0: No suspend detected 1: Bus suspend detected
5	RW1C	0	**Device Reset** This bit is set by the controller if the USB bus reset status is detected. 0: No reset 1: Reset
4	RO	0	**Reserved**
3	RW1C	0	**Controller System Error** The controller sets this bit to a one when a serious error occurs during a system access. If this bit is set, the controller also clears Run/Stop bit and sets halted bit. 0: No error 1: System error
2	RO	0	**Reserved**
1	RO	0	**FS Mode Status** This bit indicates if the device is in USB 1.1 FS mode. 0: Not in FS mode 1: FS mode
0	RO	0	**High-Speed Mode Status** This bit indicates if the device is in USB 2.0 High-Speed mode. 0: Not in High-Speed mode 1: High-Speed mode

Offset Address: 17-16h (USBD-MMIO)

Device Port Control / Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RW	000b	**Port Test Control – R/W** 000: Test mode not enabled 001: Test J_STATE 010: Test K_STATE 011: SE0_NAK 100: Test Packet 101: Test FORCE_ENABLE 110: Test Chirp J 111: Test Chirp K
12:10	RO	0	**Reserved**
9:8	RO	00b	**Bus Line Status** These bits correspond to USB bus signals [D+: D-] with bit [9:8].
7:2	RO	0	**Reserved**
1	RW1C	0	**Connection Change Status** This bit is set if bit 0 state changes. 0: No change 1: Status changed
0	RO	0	**Current Connection Status** This bit indicates current connection status. 0: No connect 1: Connected

Offset Address: 19-18h (USBD-MMIO)

Device Interrupt Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RO	0	**Descriptor Error Interrupt Enable Status** 0: Disable 1: Enable
2	RW1C	0	**Bus Activities Interrupt Status** The controller sets this bit when any USB bus activities interrupt is generated. The bus activities include bus reset, bus suspend and bus resume. 0: No bus activities events 1: Bus activities events occur
1	RO	0	**Babble Interrupt Status** The controller set this bit to a one when packet babble received. 0: No babble 1: Babble received
0	RO	0	**Complete Interrupt** The controller sets this bit on transfer completion. Software can clear the interrupts from all endpoints to clear this bit. 0: No interrupt 1: Transfer completed

Offset Address: 1B-1Ah (USBD-MMIO)

Device Interrupt Enable Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RW	0	**Descriptor Error Interrupt Enable**
2	RW	0	**Bus Activities Interrupt Enable** When this bit is set, controller will generate interrupt if any bus activities occur. 0: Disable 1: Enable
1	RW	0	**Babble Interrupt Enable** When this bit is set, controller will generate interrupt if packet babble error occurs. 0: Disable 1: Enable
0	RW	0	**Complete Interrupt Enable** When this bit is set, controller will generate interrupt on transfer completion. 0: Disable 1: Enable

Offset Address: 1D-1Ch (USBD-MMIO)

Force Interrupt Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW	0	**Force Bus Active Interrupt to be Asserted** 0: Disable 1: Enable
7	RW	0	**Force End Point 3 Interrupt of Complete (IOC)** 0: Disable 1: Enable
6	RW	0	**Force End Point 2 Descriptor Error** 0: Disable 1: Enable
5	RW	0	**Force End Point 2 Interrupt of Complete (IOC)** 0: Disable 1: Enable
4	RW	0	**Force End Point 1 Descriptor Error** 0: Disable 1: Enable
3	RW	0	**Force End Point 1 Babble Interrupt to be Asserted** 0: Disable 1: Enable
2	RW	0	**Force End Point 1 Interrupt of Complete (IOC)** 0: Disable 1: Enable
1	RW	0	**Force End Point 0 Babble** 0: Disable 1: Enable
0	RW	0	**Force End Point 0 Interrupt of Complete (IOC)** 0: Disable 1: Enable

Offset Address: 1E-1Fh (D11F0) – Reserved

VIA USB Device Endpoint Controller Operational Registers (20-2Fh)

Offset Address: 23-20h (USBD-MMIO)

Endpoint 0 Status and Control Register **Default Value: 0040 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Endpoint Number** This field stores this endpoint's ID number. Note that this field of the control endpoint is fixed to zero, and only the least two bits are writable since only four endpoints are implemented in this design.
27	RW	0	**DMA Reset** Set this bit to reset DMA to initial idle state. Once the reset is finished by hardware, this bit will be cleared to 0 automatically.
26:16	RW	040h	**Endpoint Max Packet Size (Bytes)** This field specifies the maximum packet size of this endpoint. This value must not exceed: 8: Interrupt endpoint and the attribute is RO 64: Control endpoint 512: Bulk endpoint
15	RW1C	0	**Endpoint Received an Error Descriptor Interrupt** Hardware sets this bit when it gets an error descriptor, also the controller will generate interrupt.
14	RW1C	0	**Endpoint Received Packet Babble Interrupt** Controller sets this bit when it receives packet babble if schedule has its IOC bit set. If interrupt is enabled, the controller will also generate interrupt. 0: No interrupt 1: Interrupt event
13	RW1C	0	**Endpoint Transfer Completion Interrupt** Controller sets this bit when it completes transfer if schedule has its IOC bit set. If interrupt is enabled, the controller will also generate interrupt. 0: No interrupt 1: Interrupt event
12	RO	0	**Endpoint DMA Engine Active Status** This bit is set by endpoint controller if it starts DMA engine including USB bus and PCI bus traffic and is cleared if DMA process completes. When this bit is set, software must not modify the pointed related data buffer.
11	RO	0	**DMA Need Reset** When meet complete interrupt, check this bit. If it is 1, issue a DMA reset for this endpoint. Other endpoint always 0 0: Control data DMA don't need reset 1: Control data DMA need reset
10	RO	0	**Reserved**
9:8	RO	0	**Index of the Next Descriptor the USB Device would Deal (NEXTDES)**
7:6	RO	0	**Index of the Last Descriptor the USB Device would Deal (ENDDES)**
5:4	RO	0	**Index of Current Descriptor the USB Device is Dealing (CURDES)**
3	RW	0	**Endpoint Stalled** This bit stalls this endpoint. If set this bit, the DMA engine may halt at once and will return STALL handshake to USB bus query. The endpoint controller also sets this bit if DMA engine encounters serious error. This endpoint should be active at runtime. It can not be set by MMIO Rx20[2] (Endpoint Light Reset) but only be reset by MMIO Rx10[17] (Controller Reset).
2	RW	0	**Endpoint Light Reset** If this bit is set, this endpoint will be reset to initial condition except the endpoint number and maximum packet size. Software should wait until this bit goes to zero before any further operations. 0: Not reset 1: Endpoint light reset
1	RW	0	**Endpoint DMA Engine Enable** Set this bit activates endpoint DMA engine. Software may disable DMA engine by clearing this bit to remove schedule. Software must ensure that DMA active status goes to zero before removing or modifying the schedule. 0: Disable 1: Enable
0	RW	0	**Endpoint Run/Stop** When set to 1, the endpoint controller starts executing the specified descriptor. If sets to zero, the controller will not respond to any USB host packets. If serious error occurs, the controller also clears this bit. 0: Stop 1: Run

Offset Address: 27-24h (USBD-MMIO)

Bulk Out Endpoint Control and Status **Default Value: 1200 0100h**

Bit	Attribute	Default	Description
31:28	RW	1h	**Endpoint Number** This field stores this endpoint's ID number. Note that this field of the control endpoint is fixed to zero, and only the least two bits are writable since only four endpoints are implemented in this design.
27	RW	0	**DMA Reset** Set this bit to reset DMA to initial idle state. Once the reset is finished by hardware, this bit will be cleared to 0 automatically.
26:16	RW	200h	**Endpoint Max Packet Size (Bytes)** This field specifies the maximum packet size of this endpoint. This value must not exceed: 8: Interrupt endpoint and the attribute is RO 64: Control endpoint 512: Bulk endpoint
15	RW1C	0	**Endpoint Received an Error Descriptor Interrupt** Hardware sets this bit when it gets an error descriptor, also the controller will generate interrupt.
14	RW1C	0	**Endpoint Received Packet Babble Interrupt** Controller sets this bit when it receives packet babble if schedule has its IOC bit set. If interrupt is enabled, controller will also generate interrupt. 0: No interrupt 1: Interrupt event
13	RW1C	0	**Endpoint Transfer Completion Interrupt** Controller sets this bit when it completes transfer if schedule has its IOC bit set. If interrupt is enabled, controller will also generate interrupt. 0: No interrupt 1: Interrupt event
12	RO	0	**Endpoint DMA Engine Active Status** This bit is set by endpoint controller if it starts DMA engine including USB bus and PCI bus traffic and is cleared if DMA process completes. When this bit is set, software must not modify the pointed related data buffer.
11	RO	0	**DMA Need Reset** When meet complete interrupt, check this bit, if it is 1, issue a DMA reset for this endpoint. Other endpoint always 0 0: Control data DMA don't need reset 1: Control data DMA need reset
10	RO	0	**Reserved**
9:8	RO	1	**Index of the Next Descriptor the USB Device would Deal (NEXTDES)**
7:6	RO	0	**Index of the Last Descriptor the USB Device would Deal (ENDDES)**
5:4	RO	0	**Index of Current Descriptor the USB Device is Dealing (CURDES)**
3	RW	0	**Endpoint Stalled** This bit stalls this endpoint. If set this bit, the DMA engine may halt at once and will return STALL handshake to USB bus query. The endpoint controller also sets this bit if DMA engine encounters serious error. It can be reset by MMIO Rx24[2] (Endpoint Light Reset).
2	RW	0	**Endpoint Light Reset** If this bit is set, this endpoint will be reset to initial condition except the endpoint number and maximum packet size. Software should wait until this bit goes to zero before any further operations. 0: Not reset 1: Endpoint light reset
1	RW	0	**Endpoint DMA Engine Enable** Set this bit activates endpoint DMA engine. Software may disable DMA engine by clearing this bit to remove schedule. Software must ensure that DMA active status goes to zero before removing or modifying the schedule. 0: Disable 1: Enable
0	RW	0	**Endpoint Run/Stop** When set to 1, the endpoint controller starts executing the specified descriptor. If sets to zero, the controller will not respond to any USB host packets. If serious error occurs, the controller also clears this bit. 0: Stop 1: Run

Offset Address: 2B-28h (USBD-MMIO)

Bulk In Endpoint Control and Status **Default Value: 2200 0100h**

Bit	Attribute	Default	Description
31:28	RW	2h	**Endpoint Number** This field stores this endpoint's ID number. Note that this field of the control endpoint is fixed to zero, and only the least two bits are writable since only four endpoints are implemented in this design.
27	RW	0	**DMA Reset** Set this bit to reset DMA to initial idle state. Once the reset is finished by hardware, this bit will be cleared to 0 automatically.
26:16	RW	200h	**Endpoint Max Packet Size (Bytes)** This field specifies the maximum packet size of this endpoint. This value must not exceed: 8: Interrupt endpoint and the attribute is RO 64: Control endpoint 512: Bulk endpoint
15	RW1C	0	**Endpoint Received an Error Descriptor Interrupt** Hardware sets this bit when it gets an error descriptor, also the controller will generate interrupt.
14	RW1C	0	**Endpoint Received Packet Babble Interrupt** Controller sets this bit when it receives packet babble if schedule has its IOC bit set. If interrupt is enabled, the controller will also generate interrupt. 0: No interrupt 1: Interrupt event
13	RW1C	0	**Endpoint Transfer Completion Interrupt** Controller sets this bit when it completes transfer if schedule has its IOC bit set. If interrupt is enabled, the controller will also generate interrupt. 0: No interrupt 1: Interrupt event
12	RO	0	**Endpoint DMA Engine Active Status** This bit is set by endpoint controller if it starts DMA engine including USB bus and PCI bus traffic and is cleared if DMA process completes. When this bit is set, software must not modify the pointed related data buffer.
11	RO	0	**DMA Need Reset** When meet complete interrupt, check this bit. If it is 1, issue a DMA reset for this endpoint. Other endpoint always 0. 0: Control data DMA don't need reset 1: Control data DMA need reset
10	RO	0	**Reserved**
9:8	RO	1	**Index of the Next Descriptor the USB Device would Deal (NEXTDES)**
7:6	RO	0	**Index of the Last Descriptor the USB Device would Deal (ENDDES)**
5:4	RO	0	**Index of Current Descriptor the USB Device is Dealing (CURDES)**
3	RW	0	**Endpoint Stalled** This bit stalls this endpoint. If set this bit, the DMA engine may halt at once and will return STALL handshake to USB bus query. The endpoint controller also sets this bit if DMA engine encounters serious error. It can be reset by MMIO Rx28[2] (Endpoint Light Reset).
2	RW	0	**Endpoint Light Reset** If this bit is set, this endpoint will be reset to initial condition except the endpoint number and maximum packet size. Software should wait until this bit goes to zero before any further operations. 0: Not reset 1: Endpoint light reset
1	RW	0	**Endpoint DMA Engine Enable** Set this bit activates endpoint DMA engine. Software may disable DMA engine by clearing this bit to remove schedule. Software must ensure that DMA active status goes to zero before removing or modifying the schedule. 0: Disable 1: Enable
0	RW	0	**Endpoint Run/Stop** When set to 1, the endpoint controller starts executing the specified descriptor. If sets to zero, the controller will not respond to any USB host packets. If serious error occurs, the controller also clears this bit. 0: Stop 1: Run

Offset Address: 2F-2Ch (USBD-MMIO)

Interrupt Endpoint Control and Status **Default Value: 3008 0000h**

Bit	Attribute	Default	Description
31:28	RW	3h	**Endpoint Number** This field stores this endpoint's ID number. Note that this field of the control endpoint is fixed to zero, and only the least two bits are writable since only four endpoints are implemented in this design.
27	RW	0	**DMA Reset** Set this bit to reset DMA to initial idle state. Once the reset is finished by hardware, this bit will be cleared to 0 automatically.
26:16	RO	8h	**Endpoint Max Packet Size (Bytes)** This field specifies the maximum packet size of this endpoint. This value must not exceed: 8: Interrupt endpoint and the attribute is RO 64: Control endpoint 512: Bulk endpoint
15	RW1C	0	**Endpoint Received an Error Descriptor Interrupt** Hardware sets this bit when it gets an error descriptor, also the controller will generate interrupt.
14	RW1C	0	**Endpoint Received Packet Babble Interrupt** Controller sets this bit when it receives packet babble if schedule has its IOC bit set. If interrupt is enabled, the controller will also generate interrupt. 0: No interrupt 1: Interrupt event
13	RW1C	0	**Endpoint Transfer Completion Interrupt** Controller sets this bit when it completes transfer if schedule has its IOC bit set. If interrupt is enabled, the controller will also generate interrupt. 0: No interrupt 1: Interrupt event
12	RO	0	**Endpoint DMA Engine Active Status** This bit is set by endpoint controller if it starts DMA engine including USB bus and PCI bus traffic and is cleared if DMA process completes. When this bit is set, software must not modify the pointed related data buffer.
11	RO	0	**DMA Need Reset** When meet complete interrupt, check this bit. If it is 1, issue a DMA reset for this endpoint. Other endpoint always 0. 0: Control data DMA don't need reset 1: Control data DMA need reset
10	RO	0	**Reserved**
9:8	RO	0	**Index of the Next Descriptor the USB Device would Deal (NEXTDES)**
7:6	RO	0	**Index of the Last Descriptor the USB Device would Deal (ENDDES)**
5:4	RO	0	**Index of Current Descriptor the USB Device is Dealing (CURDES)**
3	RW	0	**Endpoint Stalled** This bit stalls this endpoint. If set this bit, the DMA engine may halt at once and will return STALL handshake to USB bus query. The endpoint controller also sets this bit if DMA engine encounters serious error. It can be reset by MMIO Rx2C[2] (Endpoint Light Reset).
2	RW	0	**Endpoint Light Reset** If this bit is set, this endpoint will be reset to initial condition except the endpoint number and maximum packet size. Software should wait until this bit goes to zero before any further operations. 0: Not reset 1: Endpoint light reset
1	RW	0	**Endpoint DMA Engine Enable** Set this bit activates endpoint DMA engine. Software may disable DMA engine by clearing this bit to remove schedule. Software must check DMA active status goes to zero before remove or modify the schedule. 0: Disable 1: Enable
0	RW	0	**Endpoint Run/Stop** When set to 1, the endpoint controller starts executing the specified descriptor. If sets to zero, the controller will not respond to any USB host packets. If serious error occurs, the controller also clears this bit. 0: Stop 1: Run

VIA USB Device Endpoint Transfer Descriptor Registers (30-11Fh)

Offset Address: 37-30h (USBD-MMIO)

Interrupt Buffer **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**Interrupt Buffer**

Offset Address: 38-3Fh (USBD-MMIO) – Reserved

Offset Address: 43-40h (USBD-MMIO)

Control Endpoint Transfer Descriptor - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Data Toggle Initial Value** Initial data toggle of this transfer. Refer to note below. 0: Data0 1: Data1
30:29	RO	0	**Reserved**
28:16	RW	0	**Total Bytes to Transfer** Maximum is 4096 bytes. Refer to note below.
15	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when data phase transfer or setup command transfer is complete or when short packet/babble packet is received.
14:13	RO	0	**Reserved**
12	RW1C	0	**Receive Setup Command Data of Valid 8 Bytes** Controller asserts this bit when a new 8 bytes setup packet is received, and shows the data in the next two double words.
11	RW	0	**Transfer Direction I/O** Transfer direction is from the view of host. Refer to note below. 0: Host out 1: Host in
10:4	RO	0	**Reserved**
3	RW	0	**Enable Endpoint of DMA Engine First** Refer to note below. 0: Inactive 1: Active
2	RW	0	**Short Packet Detect** If bit 15 is set, interrupt will be generated. In D11F0 this chip acts as USB device and therefore functions as a receiver side during Host Out. This bit should be check when receive complete interrupt on Host Out. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected** If bit 15 is set, interrupt will be generated. In D11F0 this chip acts as USB device and therefore functions as a receiver side during Host Out. This bit should be check when receive complete interrupt on Host Out. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error** Babble condition is also included. No interrupts will be generated. This bit should be checked when the transfer is complete. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: 47-44h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx48[0] filed to produce starting buffer address for this transaction.

Offset Address: 4B-48h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:1	RO	0	**Reserved**
0	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list. Valid values are in the range of 0 to 1.

Offset Address: 4F-4Ch (USBD-MMIO)
Control Endpoint Transfer Descriptor - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Command Byte 3**
23:16	RO	0	**Command Byte 2**
15:8	RO	0	**Command Byte 1**
7:0	RO	0	**Command Byte 0**

Offset Address: 53-50h (USBD-MMIO)
Control Endpoint Transfer Descriptor - 5 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Command Byte 7**
23:16	RO	0	**Command Byte 6**
15:8	RO	0	**Command Byte 5**
7:0	RO	0	**Command Byte 4**

Offset Address: 54h (USBD-MMIO)
Interrupt In Endpoint Transfer Descriptor **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Total Bytes to Transfer** Maximum is 8 bytes, can not write under following conditions: 1) Transfer bytes larger than 8 bytes, 2) Unplugged to a host or 3) Fake attached.
3	RW	0	**Data Toggle Initial Value** Initial data toggle of this packet. Refer to note below. 0: Data 0 1: Data 1
2	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when this transaction is completed.
1	RW	0	**Transaction Active Status** Refer to note below. 0: Inactive 1: Active
0	RW	0	**Transaction Error Status** Timeout and PID errors are also included. No interrupts will be generated. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:
1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: 55-57h (USBD-MMIO) – Reserved

Offset Address: 58h (USBD-MMIO)

Fake Attach Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Fake Attach Enable** 0: Disable 1: Enable
0	RO	0	**Fake Attach Detect** 0: PHY clock is not OK in FAKE mode or it is not in FAKE mode 1: PHY clock is OK in Fake Attach mode

Offset Address: 55-59h (USBD-MMIO) – Reserved

Offset Address: 5Ah (USBD-MMIO)

Dynamic Clock Enable - 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**HS_MAC_RX_CLK60M Clock Free Run Enable** 0: Disable 1: Enable
6	RW	0	**HS_MAC_TX_CLK60M Clock Free Run Enable** 0: Disable 1: Enable
5	RW	0	**UTM_CHK_CLK60M Clock Free Run Enable** 0: Disable 1: Enable
4	RW	0	**ENDP3_CTRL_CLK Clock Free Run Enable** 0: Disable 1: Enable
3	RW	0	**ENDP2_CTRL_CLK Clock Free Run Enable** 0: Disable 1: Enable
2	RW	0	**ENDP1_CTRL_CLK Clock Free Run Enable** 0: Disable 1: Enable
1	RW	0	**ENDP0_CTRL_CLK Clock Free Run Enable** 0: Disable 1: Enable
0	RW	0	**DEV_CLK60M Clock Free Run Enable** 0: Disable 1: Enable

Offset Address: 5Bh (USBD-MMIO)

Dynamic Clock Enable -2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**UD_PCLK66_EP3 and UD_PCLK66_SR3 Clock Free Run Enable** 0: Disable 1: Enable
1	RW	0	**UD_PCLK66_EP2 and UD_PCLK66_SR2 Clock Free Run Enable** 0: Disable 1: Enable
0	RW	0	**UD_PCLK66_EP1 and UD_PCLK66_SR1 Clock Free Run Enable** 0: Disable 1: Enable

Offset Address: 5C-5Fh (USBD-MMIO) – Reserved

Offset Address: 63-60h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In/Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is only valid for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble/short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RW	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for BULK IN Descriptor. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: 67-64h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: 6B-68h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: 6F-6Ch (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 1 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: 73-70h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 2 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In/Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RW	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: 77-74h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 2 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: 7B-78h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 2 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: 7F-7Ch (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 2 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: 83-80h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 3 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In / Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RW	0	If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: 87-84h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 3 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: 8B-88h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 3 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: 8F-8Ch (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 3 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: 93-90h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 4 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In/Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RW	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: 97-94h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 4 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: 9B-98h (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 4 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: 9F-9Ch (USBD-MMIO)

Bulk Out Endpoint Transfer Descriptor (Host Out) 4 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: A3-A0h (USBD-MMIO)

Bulk IN Endpoint Transfer Descriptor (Host In) 1 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In/Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RO	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
1	RO	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: A7-A4h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 1 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: AB-A8h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 1 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: AF-ACh (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 1 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: B3-B0h (USBD-MMIO)

Bulk IN Endpoint Transfer Descriptor (Host In) 2 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In / Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RO	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
1	RO	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: B7-B4h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 2 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: BB-B8h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 2 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: BF-BCh (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 2 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: C3-C0h (USBD-MMIO)

Bulk IN Endpoint Transfer Descriptor (Host In) 3 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In / Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RO	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
1	RO	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: C7-C4h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 3 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: CB-C8h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 3 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: CF-CCh (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 3 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: D3-D0h (USBD-MMIO)

Bulk IN Endpoint Transfer Descriptor (Host In) 4 - 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RW	0	**Scratch Register** R/W for software to use. Refer to note below.
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In / Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is valid only for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RO	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
1	RO	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW under following conditions:

1. When MMIO Rx58[1]=1 (Fake Attach Enable).
2. When USBD is plugged to a host.

Offset Address: D7-D4h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 4 - 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 0** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RW	0	**Current Offset** This field is concatenated onto the buffer page pointer indicated in Rx63-60[4] filed to produce starting buffer address for this transaction.

Offset Address: DB-D8h (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 4 - 3 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Buffer Pointer Page 1** The buffer pointer points to the physical memory address which stores all the data to transfer.
11:0	RO	0	**Reserved**

Offset Address: DF-DCh (USBD-MMIO)

Bulk In Endpoint Transfer Descriptor (Host In) 4 - 4 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Reserved**

Offset Address: E3-E0h (USBD-MMIO)

Control PIO Descriptor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Data Toggle Initial Value** Initial data toggle of this transfer. Refer to note below. 0: Data0 1: Data1
30:29	RO	0	**Reserved**
28:16	RW	0	**Total Bytes to Transfer** Maximum is 4096 bytes. Refer to note below.
15	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when data phase transfer or setup command transfer is complete or when short packet / babble packet is received. Refer to note below.
14:13	RO	0	**Reserved**
12	RW1C	0	**Receive Setup Command Data of Valid 8 Bytes** Controller asserts this bit when a new 8 bytes setup packet is received, and shows the data in the next two double words.
11	RW	0	**Transfer Direction I/O** Transfer direction is from the view of host. Refer to note below. 0: Host out 1: Host in
10:4	RO	0	**Reserved**
3	RW	0	**Enable Endpoint of DMA Engine First** Refer to note below. 0: Inactive 1: Active
2	RW	0	**Short Packet Detect** If bit 15 is set, interrupt will be generated. In D11F0, this chip acts as USB device and therefore functions as a receiver side during Host Out. This bit should be checked when receiving complete interrupt on Host Out. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected** If bit 15 is set, interrupt will be generated. In D11F0, this chip acts as USB device and therefore functions as a receiver side during Host Out. This bit should be checked when receiving complete interrupt on Host Out. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error** Babble condition is also included. No interrupts will be generated. This bit should be checked when the transfer is complete. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW only under following situations:

1. MMIO Rx58[1]=1 (Fake Attach Enable).
2. USBD is plugged to a host.
3. MMIO Rx11[7]=1(PIO Enable).

Offset Address: E7-E4h (USBD-MMIO)

Bulk Out PIO Descriptor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RO	0	**Scratch Register**
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In / Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is only valid for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list. Refer to note below.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RW	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
1	RW	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. Refer to note below. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW only under following situations:

1. MMIO Rx58[1]=1 (Fake Attach Enable).
2. USBD is plugged to a host.
3. MMIO Rx11[7]=1(PIO Enable).

Offset Address: EB-E8h (USBD-MMIO)

Bulk In PIO Descriptor **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RW	0	**Total Bytes to Transfer** Refer to note below.
15:9	RO	0	**Scratch Register**
8	RW	0	**Data Toggle Initial Value** Initial data toggle of In / Out transfer. Refer to note below. 0: Data 0 1: Data 1
7	RW	0	**Data Toggle Auto Sync** The data toggle value will be copied to the next valid descriptor DT bit after the current descriptor is complete. This bit is only valid for Bulk Out, not Bulk In. Refer to note below. 0: Disable 1: Enable
6	RW	0	**Buffer Pointer Index** This field is used as an index into the buffer pointer list. Refer to note below.
5	RW	0	**Interrupt on Complete** If asserted, the controller issues an interrupt when the transfer is complete or packet babble / short packet is received. Refer to note below.
4	RW	0	**Concatenate Support** Next descriptor will be concatenated to the current descriptor. If this bit is set, the next descriptor's control information will be ignored except this bit, and only use page information to execute transfer. Refer to note below. 0: Not concatenated 1: Concatenated
3	RW	0	**Activate Descriptor** Refer to note below. 0: Inactive 1: Active
2	RO	0	**Short Packet Detect Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
1	RO	0	**Babble Detected Status** If bit 5 is set, interrupt will be generated. This bit should be checked when receive complete interrupt on Host Out. RO is for Bulk In Descriptor. 0: Not detected 1: Detected
0	RW	0	**Transaction Error Status** Babble condition is also included. No interrupts will be generated. This bit should be checked when receive complete interrupt on Host Out. Refer to note below. 0: No error 1: Transaction error

Note: This register can be RW only under following situations:

1. MMIO Rx58[1]=1 (Fake Attach Enable).
2. USBD is plugged to a host.
3. MMIO Rx11[7]=1(PIO Enable).

Offset Address: EC-FFh (USBD-MMIO) – Reserved

Offset Address: 107-100h (USBD-MMIO)

MAC Address 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**MAC Address 1**

Offset Address: 10F-108h (USBD-MMIO)

MAC Address 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**MAC Address 2**

Offset Address: 117-110h (USBD-MMIO)

USB Serial Number 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**USB Serial Number 1**

Offset Address: 11F-118h (USBD-MMIO)

USB Serial Number 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**USB Serial Number 2**

DEVICE 12 FUNCTION 0 (D12F0): SDIO HOST CONTROLLER

PCI Configuration Space

All registers in D12F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 10 and function number 0~3. All registers in this chapter are for SDIO Host Controller.

Header Registers (00-3Fh)

Offset Address: 01-00h (D12F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D12F0)

Device ID **Default Value: 95D0h**

Bit	Attribute	Default	Description
15:0	RO	95D0h	**Device ID**

Offset Address: 05-04h (D12F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9	RO	0	**Fast Back to Back** Hardwired to 0. (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0. (Not supported)
7	RO	0	**Address Stepping** Hardwired to 0. (Not supported)
6	RO	0	**Parity Error Response** Hardwired to 0. (Not supported)
5	RO	0	**VGA Palette Snooping** Hardwired to 0. (Not implemented)
4	RW	0	**Memory Write and Invalidate** 0: Memory write instead 1: Master can generate the command This bit must be implemented by master devices that can generate the Memory Write and Invalidate command.
3	RO	0	**Respond to Special Cycle** Hardwired to 0. (Not supported)
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	**I/O Space Access** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 07-06h (D12F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR#)** This bit is set whenever the device asserts SERR#. 0: No error 1: Error occurs
13	RO	0	**Received Master Abort** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Signaled Target Abort** 0: No abort signaled 1: Transaction aborted by this chip.
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error Detected** This bit is only set by bus masters. 0: No parity error detected 1: Error detected in data phase
7	RO	0	**Fast Back-to-Back Capability** 0: Device can't accept fast back-to-back transactions 1: Device can accept fast back-to-back transactions
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List** 0: No new capabilities linked list 1: Available implement the pointer for a new capabilities linked at offset 34h
3	RO	0	**Interrupt Status** This read-only bit reflects the state of the interrupt in the device/function. This bit is only valid when Rx04[10] is 0. 0: No interrupt 1: Interrupt asserted
2:0	RO	0	**Reserved**

Note: More detailed information on PCI Command & Status registers please refer to the PCI Local Bus Specification Revision 3.0 Chapter 6.2

Offset Address: 08h (D12F0)

Revision ID **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Revision ID**

Offset Address: 0B-09h (D12F0)

Class Code **Default Value: 08 0501h**

Bit	Attribute	Default	Description
23:0	RO	080501h	**Class Code** 080501h means SDIO host controller.

Offset Address: 0C-0Dh (D12F0) – Reserved

Offset Address: 0Eh (D12F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device.

Offset Address: 0Fh (D12F0) – Reserved

Offset Address: 13-10h (D12F0)

SDIO Memory Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Base Address [31:8]**
7:1	RO	0	**Reserved** Fixed at 0
0	RO	0	**Space Indicator** 0: Memory space 1: IO Space

Offset Address: 17-14h (D12F0)

SDIO IO Base Address **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:3	RW	0	**Base Address [31:3]**
2:0	RO	001b	**Space Indicator** 0: Memory space 1: IO Space

Offset Address: 18-2Bh (D12F0) – Reserved

Offset Address: 2D-2Ch (D12F0)

Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D12F0)

Subsystem ID **Default Value: 95D0h**

Bit	Attribute	Default	Description
15:0	RO	95D0h	**Subsystem ID**

Offset Address: 30-33h (D12F0) – Reserved

Offset Address: 34h (D12F0)

Capabilities Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capabilities Pointer** Points to the power management capability list.

Offset Address: 35-3Bh (D12F0) – Reserved

Offset Address: 3Ch (D12F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D12F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#)

Offset Address: 3E-3Fh (D12F0) – Reserved

SDIO PCI Device Specific Registers (40-FFh)

Offset Address: 40h (D12F0)

Slot Information **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RO	000b	**Number of Slots** 000: One slot 001: Two slots 010: Three slots Others: Reserved
3:0	RO	0	**Reserved**

Offset Address: 41-43h (D12F0) – Reserved

Offset Address: 44h (D12F0)

Back Door Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Subsystem ID / Subsystem Vender ID Back Door Enable** Specify whether Rx2C~2D and 2E~2F are RO or RW 0: Read only 1: Read / Write

Offset Address: 45-7Fh (D12F0) – Reserved

Offset Address: 81-80h (D12F0)

PCI Power Management Capabilities ID **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Next Item** Points to the Next Capability Structure
7:0	RO	01h	**PCI Power Management Capability**

Offset Address: 83-82h (D12F0)

PCI Power Management Capabilities **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME Can Be Generated from D3 and D0 State**
10	RO	1b	**D2 State Support** 0: Not supported 1: Supported
9	RO	1b	**D1 State Support** 0: Not supported 1: Supported
8:6	RO	111b	**Report D3 Max Suspend Current** 111b indicates 375mA required.
5	RO	0	**Device-Specific Initialization** 0: Not required 1: Required
4	RO	0	**Reserved**
3	RO	0	**Hardwired to 0**
2:0	RO	010b	**PCI Power Management Capability** 010b indicates PCI power management 1.1 support.

Offset Address: 87-84h (D12F0)

Power Management Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Hardwired to 0**
21:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit is set when the SDIO Host Controller would assert the PME# independent of the state of bit 8. This bit is in resume-well power domain.
14:9	RO	0	**Reserved**
8	RWS	0	**Enable PME** Enable PME wake up if bit 15 is set. This bit is in resume-well power domain. 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** This field is used both to determinate the current power state and to set a new power state. 00: D0 01: D1 10: D2 11: D3 If software attempts to write an unsupported optional state to this field, the write operation will complete normally on the bus; however, the data is discarded and no state change occurs.

Offset Address: 8B-88h (D12F0)

SDIO Host Capabilities **Default Value: 0568 0181h**

Bit	Attribute	Default	Description
31:29	RO	0	**Reserved**
28	RW	0	**64-bit System Bus Support** Set 1 indicates the host controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus. 0: Not supported 1: Supported
27	RO	0	**Reserved**
26	RW	1b	**Voltage Support 1.8V** 0: Not supported 1: Supported
25	RO	0	**Reserved**
24	RW	1b	**Voltage Support 3.3V** 0: Not supported 1: Supported
23	RW	0b	**Suspend / Resume Support** 0: Not supported 1: Supported
22	RW	1b	**SDMA Support** 0: Not supported 1: Supported
21	RW	1b	**High Speed Support** 0: Not supported 1: Supported
20	RW	0	**ADMA1 Support** 0: Not supported 1: Supported
19	RW	1b	**ADMA2 Support** 0: Not supported 1: Supported
18	RO	0	**Reserved**
17:16	RW	00b	**Max Block Length** 00: 512 bytes 01: 1024 bytes (not supported) 10: 2048 bytes (not supported) 11: Reserved
15:9	RO	0	**Reserved**
8	RW	1b	**Base Clock Frequency For SD Clock** 0: 33MHz 1: 48MHz
7	RW	1b	**Timeout Clock Unit** 0: KHz (Not supported) 1: MHz
6:1	RO	0	**Reserved**
0	RW	1b	**Timeout Clock Frequency** 0: 33MHz 1: 48MHz Must ensure the setting is the same as that of bit 8.

Offset Address: 8Ch (D12F0) – Reserved

Offset Address: 8Dh (D12F0)

SDIO Host Capabilities 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**Receiver Delay Clock Select** 0: 2-clock period 1: 3-clock period
2:1	RO	0	**Reserved**
0	RO	0	**Receiving Logic Control** 0: Using receiving logic 1: Bypass receiving logic

Offset Address: 8Eh (D12F0)

SDIO Host Capabilities 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PAD TNI Enable** 0: Don't bypass PAD TNI 1: Bypass PAD TNI
6:5	RW	00b	**Host CLK Delay Latency** 00: Bypass mode 01: Delay 1.6ns 10: Delay 3.2ns 11: Delay 4.8ns
4:3	RO	00b	**Reserved**
2	RW	0b	**SDMA System Address(MMIO RX00) Register Update Feature Used in ADMA Mode** 0: Disable used in ADMA mode 1: Enable be used in ADMA mode
1:0	RW	00b	**Debug Port Select** 00: SDMA Host controller 01: SDMA engine 10: ADMA Host controller 11: ADMA engine

Offset Address: 8Fh (D12F0)

SDIO Host Capabilities 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Data Output Clock Trigger Edge under High Speed** 0: Rising edge trigger 1: Falling edge trigger

Offset Address: 93-90h (D12F0)
SDIO Host Debug Signals 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**SDIO Host Debug Signals 1**

Offset Address: 97-94h (D12F0)
SDIO Host Debug Signals 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**SDIO Host Debug Signals 2**

Offset Address: 98h (D12F0)
SDIO Host Capabilities 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SDIO Clock Output PAD Slew Rate Control** Reduces the clock pad EMI issue. 0: Default slew rate value (3.3v / 3ns) 1: New slew rate value (3.3.v / 4ns)
6:2	RW	0	**Reserved**
1:0	RW	0	**De-bouncing Time Select** 00: 0.5 sec 01: 1 sec 10: 2 sec 11: Bypass debounce

Offset Address: 99h (D12F0)
SDIO Host Capabilities 6 **Default Value: F8h**

Bit	Attribute	Default	Description
7	RW	1b	**Dynamic Clock for PCI Configuration Clock** 0: Disable 1: Enable
6:3	RW	1b	**Reserved**
2:0	RW	000b	**Number of Slot which SDIO Host Supports** 000: One slot 001: Two slots 010: Three slots Others: Reserved

Offset Address: 9Ah (D12F0)
SDIO Host Capabilities 7 **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	1b	**Dynamic Clock for DMA Transfer Path** 0: Disable 1: Enable
0	RW	1b	**Dynamic Clock for SDIO Host Controller** 0: Disable 1: Enable

Offset Address: 9B-FFh (D12F0) – Reserved

SDIO MMIO Space

SDIO Host Standard Registers (00-FFh)

This section describes memory mapped I/O registers of SDIO controller. Please refer to SD Host Controller Standard Specification 1.0 for details.

Offset Address: 03-00h (SDIO-MMIO)

DMA System Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**SDMA System Address** This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing (i.e., after a transaction has stopped). Read operations during transfers may return an invalid value. The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register (Rx03) is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by settingContinue Request in the Block Gap Control register (Rx2A), the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register. ADMA does not use this register.

Offset Address: 05-04h (SDIO-MMIO)

Data Block Size **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RW	000b	**Host DMA Buffer Boundary** 000: 4K Bytes (Detects A11 carry out) 001: 8K Bytes (Detects A12 carry out) 010: 16K Bytes (Detects A13 carry out) 011: 32K Bytes (Detects A14 carry out) 100: 64K Bytes (Detects A15 carry out) 101: 128K Bytes (Detects A16 carry out) 110: 256K Bytes (Detects A17 carry out) 111: 512K Bytes (Detects A18 carry out)
11:0	RW	0	**Transfer Block Size** These bits specify the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. 0000h: No data transfer 0001h: 1 Byte 0002h: 2 Bytes 0003h: 3 Bytes 0004h: 4 Bytes …… 01FFh: 511 Bytes 0200h: 512 Bytes …… 0800h: 2048 Bytes Others: Reserved

Offset Address: 07-06h (SDIO-MMIO)

Block Count **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Block Count for Current Transfer** This bit is enabled when Block Count Enable in the Data Transfer Mode Register (Rx0C[1]) is set to 1 and is valid only for multiple black transfers. 0000h: Stop counting 0001h: 1 block 0002h: 2 blocks …….. FFFFh: 65535 blocks

Offset Address: 0B-08h (SDIO-MMIO)

Command Argument **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Command Argument**

Offset Address: 0D-0Ch (SDIO-MMIO)

Data Transfer Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RW	0	**Multi / Single Block Select** 0: Single block 1: Multiple block
4	RW	0	**Data Transfer Direction Select** 0: Write (Host to Card) 1: Read (Card to Host)
3	RO	0	**Reserved**
2	RW	0	**Auto CMD12 Enable** 0: Disable 1: Enable
1	RW	0	**Block Count Enable** 0: Disable 1: Enable
0	RW	0	**DMA Enable** This bit can be enabled only when DMA is supported (SDIO-MMIO Rx40[22]=1) 0: Disable 1: Enable

Table 39. Determination of Transfer Type

Rx0C[5] (Multi/Single Block Select)	Rx0C[1] (Block Count Enable)	Rx07-06 (Block Count)	Function
0	Don't care	Don't care	Single Transfer
1	0	Don't care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

Offset Address: 0F-0Eh (SDIO-MMIO)

Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13:8	RW	0	**Command Index**
7:6	RW	00b	**Command Type** 00: Normal (Other commands) 01: Suspend (CMD52 for writing "Bus Suspend" in CCCR) 10: Resume (CMD52 for writing "Function Select" in CCCR) 11: Abort (CMD12, CMD52 for writing "I/O Abort" in CCCR) Note: CCCR (Card Common Control Register)
5	RW	0	**Data Present Select** 0: No data present 1: Data present
4	RW	0	**Command Index Check Enable** 0: Disable 1: Enable
3	RW	0	**Command CRC (Cyclic Redundancy Check) Check Enable** 0: Disable 1: Enable
2	RO	0	**Reserved**
1:0	RW	00b	**Response Type Select** 00: No Response 01: Response length 136 10: Response length 48 11: Response length 48 and check busy after response

Offset Address: 17-10h (SDIO-MMIO)

Command Response 1 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Command Response**

Offset Address: 1F-18h (SDIO-MMIO)

Command Response 2 **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Command Response**

Offset Address: 23-20h (SDIO-MMIO)

Buffer Data Port **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Buffer Data** The host controller buffer can be accessed through this 32-bit data port register.

Offset Address: 27-24h (SDIO-MMIO)

Present State **Default Value: 01F2 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**CMD Line (SDIO[1:0]CMD#) Signal Level** 0: Low level 1: High level
23:20	RO	Fh	**DAT Line (SDIO[1:0]D[3:0]) Signal Level** For each bit: 0: Low level 1: High level
19	RO	0	**Write Protect Signal Level** 0: Write protected (SDIO[1:0]WPD# = 0) 1: Write enabled (SDIO[1:0]WPD# = 1)
18	RO	0	**Card Detect Signal Level** 0: No card present (SDIO[1:0]CD# = 1) 1: Card present (SDIO[1:0]CD# = 0)
17	RO	1b	**Card State Stable** 0: Reset or de-bouncing 1: No card or inserted
16	RO	0	**Card Inserted** 0: Reset or de-bouncing or no card 1: Card inserted
15:12	RO	0	**Reserved**
11	RO	0	**Buffer Read Enable** This status is used for non-DMA read transfers. 0: Read disable 1: Read enable
10	RO	0	**Buffer Write Enable** This status is used for non-DMA write transfers. 0: Write disable 1: Write enable
9	RO	0	**Read Transfer Active** 0: No valid data 1: Transferring data
8	RO	0	**Write Transfer Active** 0: No valid data 1: Transferring data
7:3	RO	0	**Reserved**
2	RO	0	**DAT Line Active** This bit indicates whether one of the data lines on SD Bus is in use. 0: DAT line inactive 1: DAT line active
1	RO	0	**Command Inhibit (DAT)** 0: Can issue command using the DAT line 1: Cannot issue command using the DAT line
0	RO	0	**Command Inhibit (CMD)** 0: Can issue command using only the CMD line 1: Cannot issue command

Offset Address: 28h (SDIO-MMIO)

Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Card Detect Signal Selection** This bit selects source for the card detection. In order to mask the unexpected interrupt caused by the glitch when switching the source for the card detection, the interrupt should be disabled during the switching period by clearing the Rx34-Rx3B registers. 0: SDCD# is selected (for normal use) 1: The Card Detect Test Level is selected (For test purpose)
6	RW	0	**Card Detect Test Level** This bit is enabled when bit 7 is set to 1 and it indicates card inserted or not. 0: No card 1: Card inserted
5	RW	0	**Reserved**
4:3	RW	00b	**DMA Select** One of supported DMA modes can be selected. The host driver shall check the support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode (Rx0C[0]) register. 00: No DMA or SDMA is selected 01: 32-bit address ADMA1 is selected 10: 32-bit address ADMA2 is selected 11: 64-bit address ADMA2 is selected
2	RW	0	**High Speed Enable** 0: Normal speed mode 1: High speed mode
1	RW	0	**Data Transfer Width** 0: 1-bit mode 1: 4-bit mode
0	RW	0	**LED Control** 0: LED off 1: LED on

Offset Address: 29h (SDIO-MMIO)

Power Control **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:1	RW	111b	**SD Bus Voltage Select** 000-100: Reserved 101: 1.8V 110: 3.0V (not supported) 111: 3.3V
0	RW	0	**SD Bus Power** 0: Power off 1: Power on (This bit is RW only when the card is in the slot.)

Offset Address: 2Ah (SDIO-MMIO)

Block Gap Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Interrupt at Block Gap** 0: Disable 1: Enable
2	RW	0	**Read Wait Control** 0: Disable 1: Enable
1	RW	0	**Continue Request** 0: No effect 1: Restart Hardware will clear this bit automatically when the restart action is done.
0	RW	0	**Stop at Block Gap Request** 0: Transfer 1: Stop

Offset Address: 2Bh (SDIO-MMIO)

Wakeup Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Wakeup Event Enable on SD Card Removal** 0: Disable 1: Enable
1	RW	0	**Wakeup Event Enable on SD Card Insertion** 0: Disable 1: Enable
0	RW	0	**Wakeup Event Enable on Card Interrupt** 0: Disable 1: Enable

Offset Address: 2D-2Ch (SDIO-MMIO)

Clock Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RW	00h	**SDCLK (SDIO[1:0]CLK) Frequency Select** 00h: Base clock (10MHz-63MHz) 01h: Base clock divided by 2 02h: Base clock divided by 4 04h: Base clock divided by 8 08h: Base clock divided by 16 10h: Base clock divided by 32 20h: Base clock divided by 64 40h: Base clock divided by 128 80h: Base clock divided by 256 Others: Reserved
7:3	RO	0	**Reserved**
2	RW	0	**SD Clock Enable** 0: Disable 1: Enable (This bit is RW only when the card is in the slot.)
1	RO	0	**Internal Clock Stable** 0: Not ready 1: Ready
0	RW	0	**Internal Clock Enable** 0: Stop 1: Oscillate

Offset Address: 2Eh (SDIO-MMIO)

Timeout Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Data Timeout Counter Value** 0000: TMCLK x 2^{13} 0001: TMCLK x 2^{14} ……. 1110: TMCLK x 2^{27} 1111: Reserved

Offset Address: 2Fh (SDIO-MMIO)

Software Reset **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Software Reset for DAT (SDIO[1:0]D[3:0]) Line** 0: Work 1: Reset
1	RW	0	**Software Reset for CMD (SDIO[1:0]CMD#) Line** 0: Work 1: Reset
0	RW	0	**Software Reset for All** 0: Work 1: Reset

Offset Address: 31-30h (SDIO-MMIO)

Normal Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Error Interrupt** 0: No Error 1: Error
14:9	RO	0	**Reserved**
8	RO	0	**Card Interrupt** 0: No card interrupt 1: Generate card interrupt
7	RW1C	0	**Card Removal** 0: Card state stable or de-bouncing 1: Card removed
6	RW1C	0	**Card Insertion** 0: Card state stable or de-bouncing 1: Card inserted
5	RW1C	0	**Buffer Read Ready** 0: Not ready to read buffer 1: Ready to read buffer
4	RW1C	0	**Buffer Write Ready** 0: Not ready to write buffer 1: Ready to write buffer
3	RW1C	0	**DMA Interrupt** 0: No DMA interrupt 1: DMA interrupt is generated
2	RW1C	0	**Block Gap Event** 0: No block gap event 1: Transaction stopped at block gap
1	RW1C	0	**Transfer Complete** 0: No transfer complete 1: Data transfer complete
0	RW1C	0	**Command Complete** 0: No command complete 1: Command complete

Offset Address: 33-32h (SDIO-MMIO)

Error Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW1C	0	**Vendor Specific Error Status**
11:10	RO	0	**Reserved**
9	RW1C	0	**ADMA Error** This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status register (Rx54). In addition, the Host Controller generates this interrupt when it detects invalid descriptor data (Valid=0) at the ST_FDS state. ADMA Error State (Rx54[1:0]) in the ADMA Error Status register (Rx54) indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor. 0: No error 1: Error Note: ST_FDS stands for ADMA State at Transfer Data State. For definition details, please refer to SD Host Controller Standard SPEC V2.0.
8	RW1C	0	**Auto CMD12 Error** 0: No error 1: Error
7	RW1C	0	**Current Limit Error** 0: No error, the host controller is supplying power. 1: Power failure, the host controller is not supplying power to SD card.
6	RW1C	0	**Data End Bit Error** 0: No error 1: Error
5	RW1C	0	**Data CRC Error** 0: No error 1: Error
4	RW1C	0	**Data Timeout Error** 0: No error 1: Time out
3	RW1C	0	**Command Index Error** 0: No error 1: Error
2	RW1C	0	**Command End Bit Error** 0: No error 1: End bit error generated
1	RW1C	0	**Command CRC Error** 0: No error 1: CRC error generated
0	RW1C	0	**Command Timeout Error** 0: No error 1: Time out

Offset Address: 35-34h (SDIO-MMIO)

Normal Interrupt Status Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved** Fixed at 0
14:9	RO	0	**Reserved**
8	RW	0	**Card Interrupt Status Enable** 0: Mask 1: Enable
7	RW	0	**Card Removal Status Enable** 0: Mask 1: Enable
6	RW	0	**Card Insertion Status Enable** 0: Mask 1: Enable
5	RW	0	**Buffer Read Ready Status Enable** 0: Mask 1: Enable
4	RW	0	**Buffer Write Ready Status Enable** 0: Mask 1: Enable
3	RW	0	**DMA Interrupt Status Enable** 0: Mask 1: Enable
2	RW	0	**Block Gap Event Status Enable** 0: Mask 1: Enable
1	RW	0	**Transfer Complete Status Enable** 0: Mask 1: Enable
0	RW	0	**Command Complete Status Enable** 0: Mask 1: Enable

Offset Address: 37-36h (SDIO-MMIO)

Error Interrupt Status Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Vendor Specific Error Status Enable** 0: Mask 1: Enable
11:10	RO	0	**Reserved**
9	RW	0	**ADMA Error Status Enable** 0: Mask 1: Enable
8	RW	0	**Auto CMD12 Error Status Enable** 0: Mask 1: Enable
7	RW	0	**Current Limit Error Status Enable** 0: Mask 1: Enable
6	RW	0	**Data End Bit Error Status Enable** 0: Mask 1: Enable
5	RW	0	**Data CRC Error Status Enable** 0: Mask 1: Enable
4	RW	0	**Data Timeout Error Status Enable** 0: Mask 1: Enable
3	RW	0	**Command Index Error Status Enable** 0: Mask 1: Enable
2	RW	0	**Command End Bit Error Status Enable** 0: Mask 1: Enable
1	RW	0	**Command CRC Error Status Enable** 0: Mask 1: Enable
0	RW	0	**Command Timeout Error Status Enable** 0: Mask 1: Enable

Offset Address: 39-38h (SDIO-MMIO)

Normal Interrupt Signal Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved** Fixed at 0
14:9	RO	0	**Reserved**
8	RW	0	**Card Interrupt Signal Enable** 0: Mask 1: Enable
7	RW	0	**Card Removal Signal Enable** 0: Mask 1: Enable
6	RW	0	**Card Insertion Signal Enable** 0: Mask 1: Enable
5	RW	0	**Buffer Read Ready Signal Enable** 0: Mask 1: Enable
4	RW	0	**Buffer Write Ready Signal Enable** 0: Mask 1: Enable
3	RW	0	**DMA Interrupt Signal Enable** 0: Mask 1: Enable
2	RW	0	**Block Gap Event Signal Enable** 0: Mask 1: Enable
1	RW	0	**Transfer Complete Signal Enable** 0: Mask 1: Enable
0	RW	0	**Command Complete Signal Enable** 0: Mask 1: Enable

Offset Address: 3B-3Ah (SDIO-MMIO)

Error Interrupt Signal Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Vendor Specific Error Signal Enable** 0: Mask 1: Enable
11:10	RO	0	**Reserved**
9	RW	0	**ADMA Error Signal Enable** 0: Mask 1: Enable
8	RW	0	**Auto CMD12 Error Signal Enable** 0: Mask 1: Enable
7	RW	0	**Current Limit Error Signal Enable** 0: Mask 1: Enable
6	RW	0	**Data End Bit Error Signal Enable** 0: Mask 1: Enable
5	RW	0	**Data CRC Error Signal Enable** 0: Mask 1: Enable
4	RW	0	**Data Timeout Error Signal Enable** 0: Mask 1: Enable
3	RW	0	**Command Index Error Signal Enable** 0: Mask 1: Enable
2	RW	0	**Command End Bit Error Signal Enable** 0: Mask 1: Enable
1	RW	0	**Command CRC Error Signal Enable** 0: Mask 1: Enable
0	RW	0	**Command Timeout Error Signal Enable** 0: Mask 1: Enable

Offset Address: 3D-3Ch (SDIO-MMIO)

Auto CMD12 Error Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RO	0	**Command Not Issued by Auto CMD12 Error** 0: No error 1: Command not issued
6:5	RO	0	**Reserved**
4	RO	0	**Auto CMD12 Index Error** 0: No error 1: Error
3	RO	0	**Auto CMD12 End Bit Error** 0: No error 1: End bit error generated
2	RO	0	**Auto CMD12 CRC Error** 0: No error 1: CRC error generated
1	RO	0	**Auto CMD12 Timeout Error** 0: No error 1: Timeout
0	RO	0	**Auto CMD12 Not Executed** 0: Executed 1: Not executed

Offset Address: 3E-3Fh (SDIO-MMIO) – Reserved

Offset Address: 47-40h (SDIO-MMIO)

Capabilities Register **Default Value: 0000 0000 0568 30B0h**

Bit	Attribute	Default	Description
63:32	RO	0	**Reserved**
31:29	RO	0	**Reserved** Reserved for voltage support.
28	RO	0	**64-bit System Bus Support** 0: Not supported 1: Supported. The Host Controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus.
27	RO	0	**Reserved** Reserved for voltage support
26	RO	1b	**Voltage Support 1.8V** 0: Not supported 1: Supported
25	RO	0	**Voltage Support 3.0V** 0: Not supported 1: Supported
24	RO	1b	**Voltage Support 3.3V** 0: Not supported 1: Supported
23	RO	0	**Suspend / Resume Support** 0: Not supported 1: Supported
22	RO	1b	**SDMA Support** 0: Not supported 1: Supported
21	RO	1b	**High Speed Support** 0: Not supported 1: Supported
20	RO	0	**Reserved**
19	RO	1b	**ADMA2 Support** This bit indicates whether the Host Controller is capable of using ADMA2. 0: Not supported 1: Supported
18	RO	0	**Reserved**
17:16	RO	00b	**Max Block Length** 00: 512 bytes 01: 1024 bytes 10: 2048 bytes 11: Reserved
15:14	RO	0	**Reserved**
13:8	RO	30h	**Base Clock Frequency for SD Clock** 0: Get information via another method Not 0: 1MHz to 63MHz
7	RO	1b	**Timeout Clock Unit** 0: KHz 1: MHz
6	RO	0	**Reserved**
5:0	RO	30h	**Timeout Clock Frequency** These bits indicate the base clock frequency for Data Timeout Error. 0: Get information via another method 01h…3Fh: 1KHz to 63KHz or 1MHz to 63MHz

Offset Address: 4F-48h (SDIO-MMIO)

Maximum Current Capabilities **Default Value: 0000 0000 00F0 01F0h**

Bit	Attribute	Default	Description
63:24	RO	0	**Reserved**
23:16	RO	F0h	**Maximum Current for 1.8V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA …… 255: 1020 mA
15:8	RO	01h	**Maximum Current for 3.0V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA …… 255: 1020 mA
7:0	RO	F0h	**Maximum Current for 3.3V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA …… 255: 1020 mA

Offset Address: 51-50h (SDIO-MMIO)

Force Event Register for Auto CMD12 Error Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	WO	0	**Force Event for Command Not Issued By Auto CMD12 Error** 0: No Interrupt 1: Interrupt is generated
6:5	RO	0	**Reserved**
4	WO	0	**Force Event for Auto CMD12 Index Error** 0: No Interrupt 1: Interrupt is generated
3	WO	0	**Force Event for Auto CMD12 End Bit Error** 0: No Interrupt 1: Interrupt is generated
2	WO	0	**Force Event for Auto CMD12 CRC Error** 0: No Interrupt 1: Interrupt is generated
1	WO	0	**Force Event for Auto CMD12 Timeout Error** 0: No Interrupt 1: Interrupt is generated
0	WO	0	**Force Event for Auto CMD12 Not Executed** 0: No Interrupt 1: Interrupt is generated

Offset Address: 53-52h (SDIO-MMIO)

Force Event Register for Error Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	WO	0	**Force Event for Vendor Specific Error Status** Additional status bits can be defined in this register by the vendor. 0: No Interrupt 1: Interrupt is generated
11:10	RO	0	**Reserved**
9	WO	0	**Force Event for ADMA Error** 0: No Interrupt 1: Interrupt is generated
8	WO	0	**Force Event for Auto CMD12 Error** 0: No Interrupt 1: Interrupt is generated
7	WO	0	**Force Event for Current Limit Error** 0: No Interrupt 1: Interrupt is generated
6	WO	0	**Force Event for Data End Bit Error** 0: No Interrupt 1: Interrupt is generated
5	WO	0	**Force Event for Data CRC Error** 0: No Interrupt 1: Interrupt is generated
4	WO	0	**Force Event for Data Timeout Error** 0: No Interrupt 1: Interrupt is generated
3	WO	0	**Force Event for Command Index Error** 0: No Interrupt 1: Interrupt is generated
2	WO	0	**Force Event for Command End Bit Error** 0: No Interrupt 1: Interrupt is generated
1	WO	0	**Force Event for Command CRC Error** 0: No Interrupt 1: Interrupt is generated
0	WO	0	**Force Event for Command Timeout Error** 0: No Interrupt 1: Interrupt is generated

Offset Address: 54h (SDIO-MMIO)

ADMA Error Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**ADMA Length Mismatch Error** This error occurs in the following 2 cases. (1) While Block Count Enable (Rx0C[1]) is being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length. (2) Total data length can not be divided by the block length. 0: No Error 1: Error
1:0	RW	00b	**ADMA Error State** This field indicates the state of ADMA when error occurred during ADMA data transfer. This field never indicates "10b" because ADMA never stops in this state. SYS_SDR stands for ADMA System Address Register (Rx58-Rx5F). **D01-D00** / **D00 ADMA Error State when error occurred** / **Contents of SYS_SDR Register** 00 — ST_STOP (Stop DMA) — Points next of the error descriptor. 01 — ST_FDS (Fetch Descriptor) — points the error descriptor 10 — Never set this state — (Not used) 11 — ST_TFR (Transfer Data) — Points the next of the error description.

Offset Address: 55-57h (SDIO-MMIO) – Reserved

Offset Address: 5F-58h (SDIO-MMIO)

ADMA System Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**ADMA System Address** This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b. ***For 32-bit Address ADMA:*** Valid Register Value for 32-bit System Address xxxxxxxx 00000000h 00000000h xxxxxxxx 00000004h 00000004h xxxxxxxx 00000008h 00000008h xxxxxxxx 0000000Ch 0000000Ch …… …… xxxxxxxx FFFFFFFCh FFFFFFFCh ***For 64-bit Address ADMA:*** Valid Register Value for 64-bit System Address 00000000 00000000h 00000000 00000000h 00000000 00000004h 00000000 00000004h 00000000 00000008h 00000000 00000008h 00000000 0000000Ch 00000000 0000000Ch …… …… FFFFFFFF FFFFFFFCh FFFFFFFF FFFFFFFCh

Offset Address: 60-FBh (SDIO-MMIO) – Reserved

Offset Address: FD-FCh (SDIO-MMIO)

Slot Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RO	0	**Interrupt Signal for Each Slot** Bit [n] is for slot [n] (n = 0 ~ 7).

Offset Address: FF-FEh (SDIO-MMIO)

Host Controller Version **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Vendor Version Number**
7:0	RO	01h	**Specification Version Number** This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version. 00h: SD Host Specification Version 1.0 01h: SD Host Specification Version 2.0, including the feature of the ADMA and Test Register Others: Reserved

DEVICE 13 FUNCTION 0 (D13F0): MULTIPLE MEMORY CARD CONTROLLER

3 controllers are integrated in the Card Reader Interfaces of this chip:
1. Memory Stick Controller (MSC)
2. Secure Digital Controller (SDC)
3. Extreme Digital-Picture Controller (xDC)

For details of Memory Stick / Memory Stick Pro register information, please contact VIA Technical Support Department.

PCI Configuration Space

All registers in D13F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 13 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D13F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D13F0)
Device ID **Default Value: 9530h**

Bit	Attribute	Default	Description
15:0	RO	9530h	**Device ID**

Offset Address: 05-04h (D13F0)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9:3	RO	0	**Reserved**
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	**I/O Space** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 07-06h (D13F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**Signaled System Error (SERR# Asserted)** 0: No error 1: Error occurs
13	RW1C	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** 0: No abort signaled 1: Transaction aborted by this chip.
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01. 00: Fast 01: Medium 10: Slow 11: Reserved
8:5	RO	0	**Reserved**
4	RO	1b	**Capability List** 0: No new capability linked list 1: Available. Implement the pointer for a new capability linked at Rx34.
3	RO	0	**Interrupt Status** 0: No interrupt 1: Interrupt occurs
2:0	RO	0	**Reserved**

Offset Address: 08h (D13F0)

Revision ID **Default Value: 61h**

Bit	Attribute	Default	Description
7:0	RO	61h	**Revision ID**

Offset Address: 0B-09h (D13F0)

Class Code **Default Value: 05 0100h**

Bit	Attribute	Default	Description
23:0	RO	050100h	**Class Code**

Offset Address: 0Ch (D13F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D13F0)

Latency Timer **Default Value: 16h**

Bit	Attribute	Default	Description
7:0	RW	16h	**Latency Timer**

Offset Address: 0Eh (D13F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device.

Offset Address: 0Fh (D13F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 0.

Offset Address: 13-10h (D13F0)
Card Reader (CR) MMIO Register Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RW	0	**Card Reader MMIO Register Base Address [31:11]**
10:0	RO	0	**Card Reader MMIO Register Base Address [10:0]**

Offset Address: 17-14h (D13F0)
Card Reader (CR) IO Register Base Address **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:3	RW	0	**Card Reader I/O Register Base Address [31:3]**
2:0	RO	001b	**Card Reader I/O Register Base Address [2:0]**

Offset Address: 18-2Bh (D13F0) – Reserved

Offset Address: 2D-2Ch (D13F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D13F0)
Subsystem ID **Default Value: 9530h**

Bit	Attribute	Default	Description
15:0	RO	9530h	**Subsystem ID**

Offset Address: 30-33h (D13F0) – Reserved

Offset Address: 34h (D13F0)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability List Pointer** Points to next capability structure

Offset Address: 35-3Bh (D13F0) – Reserved

Offset Address: 3Ch (D13F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**Interrupt Line Selection** 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Disable 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Disable 1110: IRQ14 1111: IRQ15

Offset Address: 3Dh (D13F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3E-3Fh (D13F0) – Reserved

PCI Card Reader – Specific Configuration Registers (40-FFh)

Offset Address: 40h (D13F0)

Card Reader Working Mode Selection **Default Value: 02h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	1b	**SDC Bus Width Capability** 0: Do not support 8-bit MMC 1: Supports 8-bit MMC
0	RW	0	**Scatter-Gather Mode Select** 0: PIO mode 1: Scatter-Gather DMA mode

Offset Address: 41-7Fh (D13F0) – Reserved

Offset Address: 80h (D13F0)

Power Management Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D13F0)

Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer: Null** 0 indicates there is no next item.

Offset Address: 83-82h (D13F0)

Power Management Capability **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME# Support** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. xxxx1: PME# can be asserted from D0 xxx1x: PME# can be asserted from D1 xx1xx: PME# can be asserted from D2 x1xxx: PME# can be asserted from D3 hot 1xxxx: PME# can be asserted from D3 cold
10	RO	1b	**D2 Support** 0: Not supported 1: Supported
9	RO	1b	**D1 Support** 0: Not supported 1: Supported
8:6	RO	111b	**Aux Current (Maximum Current Required)** 111b indicates the maximum current is 375 mA,
5	RO	0	**Device Specific Initialization <DSI>** 1 indicates that beyond the standard PCI configuration header, the function requires a device specific initialization sequence following transition to the D0 uninitialized state, which is before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this.
4	RO	0	**Reserved**
3	RO	0	**PME# Clock** 0: No PCI clock is required for the function to generate PME#. 1: The function relies on the presence of the PCI clock for PME# operation.
2:0	RO	010b	**Version** 010b indicates the chip complies with Revision 1.1 of the PCI Power Management Interface Specification.

Offset Address: 85-84h (D13F0)

Power Management Capability Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME# Status**
14:9	RO	0	**Reserved**
8	RW	0	**PME# Assertion** 0: Disable PME# assertion 1: Enable PME# assertion
7:2	RO	0	**Reserved**
1:0	RW	00b	**Device Status Control** 00: D0 01: D1 10: D2 11: D3 hot

Offset Address: 86-FBh (D13F0) – Reserved

Offset Address: FCh (D13F0)

Backdoor Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Subsystem ID Write Enable** 0: Disable 1: Enable
2	RW	0	**Subsystem Vender ID Write Enable** 0: Disable 1: Enable
1:0	RW	0	**Reserved**

Offset Address: FD-FFh (D13F0) – Reserved

MMIO Space

Card Reader MMIO Base Address Register: Rx13-10h
Card Reader IO Base Address Register: Rx17-14h

Table 40. PCI Card Reader-Specific MMIO Registers

Offset Range	Function
000h~~0FFh	xDC
200h~~2FFh	SDC
400h~~4FFh	Data DMA
500h~~5FFh	CICH DMA
600h~~6FFh	PCI Control

xDC MMIO Registers (00-FFh)

Offset Address: 03-00h (xDC-MMIO)

XD Configuration 1 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	FFFFh	**Read Data 16-Bit Port** This port is used for single read or status data read while block data transfers through DMA engine.

Offset Address: 07-04h (xDC-MMIO)

XD Configuration 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Turn On Data Phase** 0: Turn on data phase 1: Turn off data phase
6	RW	0	**Enable Data Read** 0: Disable 1: Enable When enabled, it indicates that the data is transferred from Flash Memory to the controller.
5	RW	0	**Enable Single Read / Write** 0: Disable 1: Enable When enabled, it initiates single read / write sequence.
4	RW	0	**Enable End with Command** 0: Disable 1: Enable This is used for command sequence similar to “command 1 + address + command 2”. While in different hardware mode, command 1 / 2 refer to different command port register.
3:1	RW	000b	**Command Phase Byte Number** Total byte number of command: Sequence like (command 1 + address + command 2), (command 1 + address) or (command 1) does not include data phase byte number.
0	RW	0	**New Command** Set 1 will trigger command sequence and this bit will be cleared after initiating command sequence header. (command 1 + address + command 2) or (command 1 + address) or (command 1)

Offset Address: 0B-08h (xDC-MMIO)

XD Configuration 3 **Default Value: 0000 00FFh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	FFh	**xD Card Command Port 0** In command sequence, write command 1 to this port.

Offset Address: 0F-0Ch (xDC-MMIO)

XD Configuration 4 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 2**
7:0	RW	FFh	**xD Card Command Port 1** In command sequence, write address to this port.

Offset Address: 13-10h (xDC-MMIO)

XD Configuration 5 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 4** In command sequence, write row address of device to this port.
7:0	RW	FFh	**xD Card Command Port 3** In command sequence, write row address of device to this port.

Offset Address: 17-14h (xDC-MMIO)

XD Configuration 6 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 6** In command sequence, write command data to this port according to command phase byte number register set.
7:0	RW	FFh	**xD Card Command Port 5** In command sequence, write row address or command data to this port according to command phase byte number register set.

Offset Address: 1B-18h (xDC-MMIO)

XD Configuration 7 **Default Value: 0000 00FFh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	FFh	**xD Card Command Port 7** In HW_ADDR_MAP (Hardware Address Mapping) mode, the command data is written to this port according to command phase byte number register set.

Offset Address: 1F-1Ch (xDC-MMIO)

XD Configuration 8 **Default Value: 0000 FFFFh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	FFh	**xD Card Command Port 9** ***In HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 9 replaces command port 6 (NFC-MMIO Rx15) for the second block address. ***In non-HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 9 replaces command for port 5 (NFC-MMIO Rx14) for the second block address.
7:0	RW	FFh	**xD Card Command Port 8** ***In HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 8 replaces command port 5 (NFC-MMIO Rx14) for the second block address. ***In non-HW_ADDR_MAP mode:*** When second block address is set (Rx24[2]=1b), command port 8 replaces command port 4 (NFC-MMIO Rx11) for the second block address.

Offset Address: 23-20h (xDC-MMIO)

XD Configuration 9 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RW	0	**Reserved**

Offset Address: 27-24h (xDC-MMIO)

XD Configuration 10 **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Enable Second Block Address** 0: Disable 1: Enable ***In HW_ADDR_MAP mode:*** Replace command port 5 / 6 (NFC-MMIO Rx14 / Rx15) with command port 8 / 9 (NFC-MMIO Rx1C / Rx1D) for the second block address. ***In non-HW_ADDR_MAP mode:*** Replace command port 4 / 5 (NFC-MMIO Rx11 / Rx14) with command port 8 / 9 (NFC-MMIO Rx1C / Rx1D) for the second block address.
1	RW	0	**Enable Redundant Area Read Cycle** 0: Disable 1: Enable Store the data from flash into internal FIFO (xDC-MMIO RxC0-FF) This register is used when doing redundant data read only from xD card.
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 2B-28h (xDC-MMIO)

XD Configuration 11 **Default Value: 0000 00D1h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RO	1b	**Write Protect Detect Status** Input signal XD_WPD# status
6	RO	1b	**Reserved**
5	RO	0	**Reserved**
4	RO	1b	**xDC Card Line Status** 0: xD card inserted 1: xD card not inserted
3	RO	0	**Timer-Out Indicator** 0: No time-out 1: Time-out happens
2	RO	0	**New Command Status** 0: The command sequence is finished. The controller is in data phase or idle phase. 1: The command sequence is being initiated to flash I/O bus.
1	RO	0	**All Command Status** 0: The whole transfer in flash I/O bus is finished. 1: The command and data is being transferred in flash I/O bus.
0	RO	1b	**Ready / Busy Status** 0: The selected flash is busy 1: The selected flash is ready

Offset Address: 2F-2Ch (xDC-MMIO)

XD Configuration 12 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW1C	0	**Reserved**
6	RO	0	**Reserved**
5	RW1C	0	**Reserved**
4	RW1C	0	**xDC Card Insertion / Extraction Interrupt** 0: Interrupt is not caused by card insertion. 1: Interrupt is caused by device of xDC card insertion or extraction.
3	RW1C	0	**From Busy to Ready Status** 0: No status change 1: Status change occurs and the flash is from busy to ready now.
2:0	RO	0	**Reserved**

Offset Address: 33-30h (xDC-MMIO)

XD Configuration 13 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RW	0	**XDC DMA Counter0** Set the low 8 bits of data transfer count.
7:0	RW	0	**XDC DMA Counter1** Set the high 8 bits of data transfer count.

Offset Address: 34-43h (xDC-MMIO) – Reserved

Offset Address: 47-44h (xDC-MMIO)

XD Configuration 18 **Default Value: 0000 00FFh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:1	RW	7Fh	**Reserved**
0	RW	1h	**Enable xD Card** ***In indirect map mode:*** 0000x000: xD Card chip 0 enable Others: Reserved ***In direct map mode:*** Bit 0 is used to control chip enable. 0: Enable 1: Disable

Offset Address: 4B-48h (xDC-MMIO)

XD Configuration 19 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Enable Clock Stop** Set 1 will drive output signal xD Card Controller Host Clock Stop high when xDC in idle phase (finish current transfer phase or command phase).
6	RW	0	**Disable Hardware to Generate Page Ok** 0: Check page write correct and output DMA Transfer Complete signal. 1: Disable check page write correct
5	RW	0	**Enable Chip Enable (XD_CE#) Direct Map** 0: Disable direct map 1: Enable direct map
4	RW	0	**Write Protect** 0: Drive output signal XD_WP low (valid) 1: Drive output signal XD_WP high (invalid)
3:0	RW	0	**Reserved**

Offset Address: 4F-4Ch (xDC-MMIO)

XD Configuration 20 **Default Value: 0000 0080h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	1b	**Interrupt Mask Control** 0: Enable all none-mask interrupt 1: Mask all interrupt
6:5	RW	0	**Reserved**
4	RW	0	**xD Card Change Interrupt Mask** 0: Enable xD card status change interrupt 1: Mask xD card status change interrupt
3	RW	0	**From Busy to Ready Status Mask** 0: Enable this interrupt 1: Disable this interrupt
2	RW	0	**Redundant Uncorrectable Error Mask** This bit controls whether the interrupt will be generated when uncorrectable errors occur. 0: Enable this interrupt 1: Disable this interrupt
1	RW	0	**Redundant 1-Bit Error Mask** This bit controls whether the interrupt will be generated when uncorrectable errors occur. 0: Enable this interrupt 1: Disable this interrupt
0	RW	0	**Redundant Code Error Mask** This bit controls whether the interrupt will be generated when ECC code errors occur. 0: Enable this interrupt 1: Disable this interrupt

Offset Address: 53-50h (xDC-MMIO)

XD Configuration 21 **Default Value: 1212 1212h**

Bit	Attribute	Default	Description
31:28	RW	1h	**Read Pulse Time (Unit: ns)** Based on xDC clock, pulse width cycle numbers of XDC Read Pulse Time (XDC_RE tRP).
27:24	RW	2h	**Read Cycle Time (Unit: ns)** Based on xDC clock, read cycle numbers of XDC Read Cycle Time (XDC_REtRC).
23:20	RW	1h	**Write Pulse Time (Unit: ns)** Based on xDC clock, pulse width cycle numbers of XDC Write Pulse Time (XDC_WE tWP).
19:16	RW	2h	**Write Cycle Time (Unit: ns)** Based on xDC clock, write cycle numbers of XDC Write Cycle Time (XDC_WE tWC).
15:12	RW	1h	**Reserved (Do Not Program)**
11:8	RW	2h	**Reserved (Do Not Program)**
7:4	RW	1h	**Reserved (Do Not Program)**
3:0	RW	2h	**Reserved (Do Not Program)**

Offset Address: 57-54h (xDC-MMIO)

XD Configuration 22 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	0	**Reserved**
6	RW	0	**Enable Hardware Address Mapping** 0: Disable this function and programmer should write correct address to the command port registers 1: Enable hardware physical address mapping, which will enable block address / page address mapping according to different kinds of chip.
5	RW	0	**Timer Run Mask** 0: Enable timer run signal output 1: Disable timer run signal output
4	RW	0	**Timer Time Out Mask** 0: Enable timer time out interrupt 1: Disable timer time out interrupt
3	RW	0	**Enable Three Cycles** 0: For xDC 512 bytes/page structure erase operation, address phase is 3 cycles 1: For xDC 512 bytes/page structure erase operation , address phase is 2 cycles
2	RW	0	**Enable ECC Test Mode** 0: Disable 1: Enable, will write redundant area data in the place of ECC code.
1:0	RW	00b	**Bank Select (for 1-Bit Error Location)** Set these two bits to select the appropriate bank, and then read ECC data from ECC register to locate the error bit. 00: Bank 12 selected 01: Bank 34 selected 10: Bank 56 selected 11: Bank 78 selected

Offset Address: 5B-58h (xDC-MMIO)

XD Configuration 23 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:13	RW	0	**Reserved**
12	RW	0	**Enable Dummy High** 0: Insert FFh data before valid data if data source can not pre-fetch enough data. 1: Insert FFh data after valid data if data source can not pre-fetch enough data.
11:0	RW	0	**Dummy 12-Bit Counter** Dummy data counter

Offset Address: 5F-5Ch (xDC-MMIO)

XD Configuration 24 **Default Value: 0000 001Fh**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:5	RW	000b	**Block Size Select** 000: 16 pages per block 001: 32 pages per block 010: 64 pages per block 011: 128 pages per block 100: 256 pages per block 101: 512 pages per block 110 / 111: Reserved
4:0	RW	1Fh	**Reserved (Do Not Program)**

Offset Address: 63-60h (xDC-MMIO)

XD Configuration 25 **Default Value: 0000 0080h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	RW	1b	**Support xD Card ECC Format** 0: Support NFC mode 1: Support XDC mode
6:4	RW	0	**Reserved**
3	RW	0	**Fixed Command Hold** 0: Disable 1: Enable
2	RW	0	**XDC Write Strobe Negative Edge Clock** 0: Disable 1: Enable
1	RW	0	**XDC Read Strobe Sync Delay One Clock** 0: Disable 1: Enable
0	RW	0	**XDC Read Strobe Negative Edge Clock** 0: Disable 1: Enable

Offset Address: 67-64h (xDC-MMIO)

XD Configuration 26 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Enable Bank 8 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
30	RW	0	**Enable Bank 8 Uncorrectable Error Mask** 0: Disable 1: Enable
29	RW	0	**Enable Bank 8 1-Bit Error Mask** 0: Disable 1: Enable
28	RW	0	**Enable Bank 8 Code Error Mask** 0: Disable 1: Enable
27	RW	0	**Enable Bank 7 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
26	RW	0	**Enable Bank 7 Uncorrectable Error Mask** 0: Disable 1: Enable
25	RW	0	**Enable Bank 7 1-Bit Error Mask** 0: Disable 1: Enable
24	RW	0	**Enable Bank 7 Code Error Mask** 0: Disable 1: Enable
23	RW	0	**Enable Bank 6 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
22	RW	0	**Enable Bank 6 Uncorrectable Error Mask** 0: Disable 1: Enable
21	RW	0	**Enable Bank 6 1-Bit Error Mask** 0: Disable 1: Enable
20	RW	0	**Enable Bank 6 Code Error Mask** 0: Disable 1: Enable
19	RW	0	**Enable Bank 5 Bits[3:0] = 0 Mask** 0: Disable 1: Enable
18	RW	0	**Enable Bank 5 Uncorrectable Error Mask** 0: Disable 1: Enable
17	RW	0	**Enable Bank 5 1-Bit Error Mask** 0: Disable 1: Enable
16	RW	0	**Enable Bank 5 Code Error Mask** 0: Disable 1: Enable
15	RW	0	**Enable Bank 4 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
14	RW	0	**Enable Bank 4 Uncorrectable Error Mask** 0: Disable 1: Enable
13	RW	0	**Enable Bank 4 1-Bit Error Mask** 0: Disable 1: Enable
12	RW	0	**Enable Bank 4 Code Error Mask** 0: Disable 1: Enable
11	RW	0	**Enable Bank 3 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
10	RW	0	**Enable Bank 3 Uncorrectable Error Mask** 0: Disable 1: Enable
9	RW	0	**Enable Bank 3 1-Bit Error Mask** 0: Disable 1: Enable
8	RW	0	**Enable Bank 3 Code Error Mask** 0: Disable 1: Enable
7	RW	0	**Enable Bank 2 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
6	RW	0	**Enable Bank 2 Uncorrectable Error Mask** 0: Disable 1: Enable
5	RW	0	**Enable Bank 2 1-Bit Error Mask** 0: Disable 1: Enable
4	RW	0	**Enable Bank 2 Code Error Mask** 0: Disable 1: Enable
3	RW	0	**Enable Bank 1 Bits [3:0] = 0 Mask** 0: Disable 1: Enable
2	RW	0	**Enable Bank 1 Uncorrectable Error Mask** 0: Disable 1: Enable
1	RW	0	**Enable Bank 1 1-Bit Error Mask** 0: Disable 1: Enable
0	RW	0	**Enable Bank 1 Code Error Mask** 0: Disable 1: Enable

Offset Address: 6B-68h (xDC-MMIO)

XD Configuration 27 **Default Value: 0000 0EFFh**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:9	RO	111b	**Odd Bank (Bank 1, 3, 5, 7) Column Parity Bits [2:0] Status** Bit value represents the ECC code.
8:0	RO	0FFh	**Odd Bank (Bank 1, 3, 5, 7) Line Parity Status** Bit value represents the ECC code.

Offset Address: 6F-6Ch (xDC-MMIO)

XD Configuration 28 **Default Value: 0000 0EFFh**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:9	RO	111b	**Even Bank (Bank 2, 4, 6, 8) Column Parity Bits [2:0] Status** Bit value represents the ECC code.
8:0	RO	0FFh	**Even Bank (Bank 2, 4, 6, 8) Line Parity Status** Bit value represents the ECC code.

Offset Address: 73-70h (xDC-MMIO)

XD Configuration 29 **Default Value: 0000 073Fh**

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10:8	RO	111b	**Redundant Area Column Parity Bits [2:0] Status**
7:6	RO	0	**Reserved**
5:0	RO	3Fh	**Redundant Area Line Parity Bits [5:0] Status**

Offset Address: 77-74h (xDC-MMIO)

XD Configuration 30 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**xD Card Controller At Idle Phase** 0: Not idle 1: Idle

Offset Address: 7B-78h (xDC-MMIO)

XD Configuration 31 **Default Value: 00FF FFFFh**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RO	FFFFFFh	**Page Address [23:0]**

Offset Address: 7F-7Ch (xDC-MMIO)

XD Configuration 32 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW1C	0	**Redundant Uncorrectable Error Status** 0: Error bit is less than 2 bits or no error 1: Error bit are 2 bits or more than 2 bits
1	RW1C	0	**Redundant 1-Bit Error Status** 0: No error 1: Error status occurs
0	RW1C	0	**Redundant Code Error Status** 0: No error 1: Error status occurs

Offset Address: 83-80h (xDC-MMIO)

XD Configuration 33 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW1C	0	**Bank 8 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
30	RW1C	0	**Bank 8 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
29	RW1C	0	**Bank 8 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
28	RW1C	0	**Bank 8 Code Error Status** 0: Not ECC code error 1: ECC code error
27	RW1C	0	**Bank 7 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
26	RW1C	0	**Bank 7 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
25	RW1C	0	**Bank 7 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
24	RW1C	0	**Bank 7 Code Error Status** 0: Not ECC code error 1: ECC code error
23	RW1C	0	**Bank 6 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
22	RW1C	0	**Bank 6 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
21	RW1C	0	**Bank 6 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
20	RW1C	0	**Bank 6 Code Error Status** 0: Not ECC code error 1: ECC code error
19	RW1C	0	**Bank 5 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
18	RW1C	0	**Bank 5 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
17	RW1C	0	**Bank 5 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
16	RW1C	0	**Bank 5 Code Error Status** 0: Not ECC code error 1: ECC code error
15	RW1C	0	**Bank 4 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
14	RW1C	0	**Bank 4 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
13	RW1C	0	**Bank 4 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
12	RW1C	0	**Bank 4 Code Error Status** 0: Not ECC code error 1: ECC code error
11	RW1C	0	**Bank 3 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0

10	RW1C	0	**Bank 3 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
9	RW1C	0	**Bank 3 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
8	RW1C	0	**Bank 3 Code Error Status** 0: Not ECC code error 1: ECC code error
7	RW1C	0	**Bank 2 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
6	RW1C	0	**Bank 2 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
5	RW1C	0	**Bank 2 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
4	RW1C	0	**Bank 2 Code Error Status** 0: Not ECC code error 1: ECC code error
3	RW1C	0	**Bank 1 Bits [3:0] = 0 Status** 0: Not equal to 0 1: Equal to 0
2	RW1C	0	**Bank 1 Uncorrectable Error Status** 0: Correctable 1: Uncorrectable
1	RW1C	0	**Bank 1 1-Bit Error Status** 0: Not 1-bit error 1: 1-bit error
0	RW1C	0	**Bank 1 Code Error Status** 0: Not ECC code error 1: ECC code error

Offset Address: 84-BFh (xDC-MMIO) – Reserved

Offset Address: C0-FFh (xDC-MMIO) – Reserved

Refer to xDC-MMIO Rx24[1] for details.

SDC MMIO Registers (00-FFh)

Offset Address: 00h (SDC-MMIO)

Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Command Type** Refer to the *Command Type Field Encoding* table below for valid encoding and descriptions.
3	RW1C	0	**Response FIFO Reset** Writing 1 to this bit will clear the contents of response register Rx10-1**F**h. The response will be loaded to **the** corresponding registers according to response type whether response **FIFO** is reset or not.
2	RW	0	**Read or Write Operation** 0: Specifies that the data transfer direction of the current command is from card to system memory. 1: Specifies that the data transfer direction of the current command is from system memory to card
1	RW	0	**Reserved**
0	RW1C	0	**Command Start / Busy** This bit is set to initiate a command. The bit is reset once the last bit of the command argument is transmitted. Rx00[7:4], **Rx00[2]**, **Rx01**, Rx02[3:0] and **Rx07-04** must be configured before this bit is set.

Table 41. Command Type Field Encodings

Command Type[3:0]	Action Applied to SD Memory	Action Applied to SDIO
0000b	Non-data-write, non-data-read, non-data-stop, non-io-abort commands.	Non-data-write, non-data-read, non-data-stop, non-io-abort commands.
0001b	Single block write. Use when doing a WRITE_BLOCK (CMD24) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (seep.41 of SD spec) and is also programmed into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.	Single block IO write. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 0 (byte mode). The block size is defined in Byte/Block Count. A 0x0 value in Byte/Block Count is considered to be 256 Bytes (see p.18 of SDIO spec). The block size is also programmed Into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.
0010b	Single block read. Use when doing a READ_SINGLE_BLOCK (CMD17) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is also programmed into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.	Single block IO read. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 0 (byte mode). The block size is defined in Byte/Block Count. A 0x0 value in Byte/Block Count is considered to be 256 Bytes (see p.18 of SDIO spec). The block size is also programmed Into **Block Length Register (Rx0D-0C)** field. **Block Count Register (Rx0F-0E)** field is ignored.
0011b	Multiple block write requiring STOP command to end transfer. Use when doing a WRITE_MULTIPLE_BLOCK (CMD25) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a STOP_TRANSMISSION (CMD12) command.	Multiple block IO write requiring writing to CCCR to end transfer. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 1 (block mode) and Byte/Block Count = 0x0 (infinite block count) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size Registers (2 of them) inside CCCR (see p.26 of SDIO spec). For Functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The Block size is also programmed into **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a IO_RW_DIRECT (CMD52) command to write to the abort register in CCCR (bits [2:0] of register 6) (see p.23 of SDIO spec).

0100b	Multiple block read requiring STOP command to end transfer. Use when doing a READ_MULTIPLE_BLOCK (CMD18) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is programmed into **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a STOP_TRANSMISSION (CMD12) command.	Multiple block IO read requiring writing to CCCR to end transfer. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 1 (block mode) and Byte/Block Count = 0x0 (infinite block count) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into **Block Length Register (Rx0D-0C)** field. Based on the Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register (Rx0F-0E)** field is ignored. The transfer has to be terminated by issuing a IO_RW_DIRECT (CMD52) command to write to the abort register in CCCR (bits [2:0] of register 6) (see p.23 of SDIO spec).
0101b	Not applicable.	Multiple block IO write with fixed number of blocks. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 1 (block mode) and Byte/Block Count set to the desired number of blocks to transfer (must Be non-zero) (see p.18 of SDIO spec). For function 0, block size is Programmed by using the IO_RW_DIRECT (CMD52) command To write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into the **Block Length Register (Rx0D-0C)** field. Based on the Byte/Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. Using either 1-bit or 4-bit wire will not affect this number because in the 4-bit wire case, 1 block of data is split into 4 sub-blocks (each 1/4 of the orig-inal block size) on each data wire. The start and stop bits still define the boundary of a block. The transfer will be terminated when the correct number of blocks have been transmitted. No abort action is required.
0110b	Not applicable.	Multiple block IO read with fixed number of blocks. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 1 (block mode) and Byte/Block Count set to the desired number of blocks to transfer (must Be non-zero) (see p.18 of SDIO spec). For function 0, block size is Programmed by using the IO_RW_DIRECT (CMD52) command To write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into the **Block Length Register (Rx0D-0C)** field. Based on the Byte/Block Count, the **Block Count Register (Rx0F-0E)** field is programmed with the correct number of blocks. Using either 1-bit or 4-bit wire will not affect this number because in the 4-bit wire case, 1 block of data is split into 4 sub-blocks (each 1/4 of the orig-inal block size) on each data wire. The start and stop bits still define the boundary of a block. The transfer will be terminated when the correct number of blocks have been transmitted. No abort action is required.
0111b	Terminate transfer of a multiple block write or read. Use when doing a STOP_TRANSMISSION (CMD12) command (see p.41 of SD spec).	Not applicable.
1000b	Not applicable.	Terminate transfer of a multiple block IO write or read without a fixed desired number of block count. Use when issuing a IO_RW_DIRECT (CMD52) command to write to the abort register In CCCR (bits [2:0] of register 6) to stop the transfer (see p.23 of SDIO spec).
1001b	CE-ATA Write_multiple_block command, the data transfer will be terminate by Command_Complete signal issue by device.	Reserved.
1010b	CE-ATA Read_multiple_block command, the data transfer will be terminate by Command_Complete signal issue by device.	Reserved.
1011b	CE-ATA Command Completion Disable.	Reserved.
1010b to 1111b	Reserved.	Reserved.

Offset Address: 01h (SDC-MMIO)

Command Index **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Command Index** Bits [5:0] will be the contents of bits [45:40] in SD command token.

Offset Address: 02h (SDC-MMIO)

Response Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RO	0	**Response Ready** This bit is set by the SD block once the command-response sequence is finished and reset once response FIFO is read.
3:0	RW	0000b	**Response Type** 0000: No response 0001: R1 response (48 bits) 0010: R2 response (136 bits) 0011: R3 response (48 bits) 0100: R4 response (48 bits) 0101: R5 response (48 bits) 0110: R6 response (48 bits) 1001: R1b response (48 bits) All other values are reserved.

Offset Address: 03h (SDC -MMIO) – Reserved

Offset Address: 07-04h (SDC-MMIO)

Command Argument **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Command Argument**

Offset Address: 08h (SDC-MMIO)

Bus Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**SD Host Power Down Clock Stop** Set this bit in order to save power if there is no cycle. It must be cleared before transferring any data or command. In fact, it is a software programmable clock gating.
3:2	RW	0	**Reserved**
1	RW	0	**Bus Width** 0: 1-bit mode 1: 4-bit mode Before changing the value of this bit, set card bus width with corresponding command first.
0	RW	0	**Reserved**

Offset Address: 09-0Bh (SDC-MMIO) – Reserved

Offset Address: 0D-0Ch (SDC-MMIO)
Block Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SD Host Interrupt** 0: Disable 1: Enable
14	RW	0	**Reserved**
13	RW	0	**Select GPI Pin to Detect Card** GPI pin means CR_CD# in top design. Set this bit always. 0: Disable 1: Enable
12	RW	0	**Active Polarity of Card Detection Pin** 0: Indicates the card insertion is active low. Low means the existence of memory card. 1: Indicates the card insertion is active high
11	RW	0	**Enable Transaction Abort When Multiple Blocks R/W Command CRC Error Occurs** 0: Disable 1: Enable
10:0	RW	0	**Block Length** The block length = Bits [10:0] + 1 For example: Block length = 512B, set bits [10:0] = 511.

Offset Address: 0F-0Eh (SDC-MMIO)
Block Count **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Block Count** Block Count = Bits [15:0] When Rx0F-0Eh is set to FFFFh, this field is ignored in multiple blocks R/W command. Data are transferred infinitely until the controller is programmed to generate CMD12 to terminate data transfer.

Offset Address: 1F-10h (SDC-MMIO)
Response Register **Default Value: 0h**

Bit	Attribute	Default	Description
127:0	RO	0	**Bits [5:0]: Index or reserved bit according to response type.** **Bits [15:8], [23:16]: Response Content (except start bit, transmission bit, index or reserved bits, CRC, end bit).** ***For response type R1, R1b, R3, R6:*** Response data bits [7:1] (CRC or reserved) and bit 0 (end bit) will not be updated into the response register. ***For response type R2:*** Response data bit 135 (start bit), bit 134 (transmission bit), bits [133:128] (reserved bits), bits [127:8] (CID beside internal CRC) will be updated into the response register.

Offset Address: 21-20h (SDC-MMIO)
Current Block Count **Default Value: FFFFh**

Bit	Attribute	Default	Description
15:0	RO	FFFFh	**Current Block Count** The number of blocks that has not been transmitted in multiple blocks R/W command. When the command is done, this field value must be 0000h.

Offset Address: 22h (SDC-MMIO)
Current Bus State **Default Value: 08h**

Bit	Attribute	Default	Description
7:0	RO	08h	**Current SD Bus State** Bits [7:4] BUS Data Line State Bits [3:0] CMD Line State

Offset Address: 23h (SDC -MMIO) – Reserved

Offset Address: 24h (SDC-MMIO)

Interrupt Mask 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Card Insertion or Removal Interrupt Enable** Interrupt is generated by CR_CD# pin. 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	0	**Enable Interrupt for Block Data Transfer Done** Generate an interrupt at the completion of each block of data transfer. 0: Disable 1: Enable
4	RW	0	**Enable Interrupt for Multiple Blocks Transfer Done** Generate an interrupt at the completion of all successful data transfer no matter it is single block or multiple blocks data transfer. 0: Disable 1: Enable
3:1	RW	0	**Reserved**
0	RW	0	**CE-ATA Command Completion Interrupt Enable** 0: Disable 1: Enable

Offset Address: 25h (SDC-MMIO)

Interrupt Mask 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Write Data CRC Error Interrupt Enable** 0: Disable 1: Enable
6	RW	0	**Read Data CRC Error Interrupt Enable** 0: Disable 1: Enable
5	RW	0	**Response CRC Error Interrupt Enable** 0: Disable 1: Enable
4	RW	0	**Data Access Timeout Interrupt Enable** 0: Disable 1: Enable
3	RW	0	**Enable Interrupt for Multiple Blocks R/W Auto Stop Command-Response Transfer Done** 0: Disable 1: Enable
2	RW	0	**Enable Interrupt for Command-Response Response Access Timeout** 0: Disable 1: Enable
1	RW	0	**Command-Response Transfer Done Interrupt Enable (or Command Only if the Command Does Not Require A Response)** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 26-27h (SDC -MMIO) – Reserved

Offset Address: 28h (SDC-MMIO)

SD Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Card Detect Interrupt by GPI Pin** Card insertion or removal interrupt, using CR_CD# as card detection pin. 0: No interrupt 1: Card insertion or removal interrupt is detected
6	RW1C	0	**Reserved**
5	RW1C	0	**Block Data Transfer Done Interrupt Status** 0: No interrupt 1: Completion of one block data transfer
4	RW1C	0	**Multiple Blocks Transfer Done Interrupt Status** All data are transferred whether it is single block or multiple blocks data. 0: No interrupt 1: Block transfer complete interrupt
3	RO	0	**SD Slot Status (GPI)** Card insertion and removal share the same interrupt, so software use this bit to determine whether it is insertion or removal. The value is valid only if Rx0C[13] is set; otherwise it always is 0. 0: No card in the slot 1: SD card in the slot
2	RO	0	**Reserved**
1	RO	0	**SD Card Write Protect Status** 0: Write protected 1: Write freely
0	RW1C	0	**CE-ATA Command Completion Interrupt Status** 1 indicates the completion of the CE-ATA command.

Offset Address: 29h (SDC-MMIO)

SD Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Write Data CRC Error Interrupt Status** 0: No error (Normal) 1: Error detected
6	RW1C	0	**Read Data CRC Error Interrupt Status** 0: No error 1: Error detected
5	RW1C	0	**Response CRC Error Interrupt Status** 0: No error 1: Error detected
4	RW1C	0	**Data Access Timeout Interrupt Status (NAC)** 0: Normal 1: Timeout
3	RW1C	0	**Multiple Block R/W Auto Stop Command-Response Transfer Done Interrupt Status** During multiple blocks read and write cycles, when SDC-MMIO Rx21-20 is 0, controller will generate CMD12 automatically. When receiving response of CMD12, this bit is set. 0: No interrupt 1: Interrupt occurs
2	RW1C	0	**Command-Response Response Access Timeout Interrupt (NCR) Status** 0: Normal 1: Timeout. There is no response during the given time.
1	RW1C	0	**Command-Response Transfer Done Interrupt Status (or Command Only if the Command Does Not Require A Response).** 0: No interrupt 1: Interrupt occurred
0	RO	0	**Reserved**

Offset Address: 2Ah (SDC-MMIO)

SD Status 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SD Host Automatic Clock Freezing Enable** 0: Disable. Card always transfers data without stopping clock. 1: Enable. When DMA cannot transfer data, controller can stop the clock of card in order to block the card data. It is highly recommended to set this bit always.
6	RO	0	**Clock Freezing Status** 0: Normal clocking 1: Clock frozen (potential overrun / underrun)
5	RO	0	**SD Data Response Busy Status** 0: SD card has finished programming and is idle. 1: SD card is busy in programming after write block.
4:3	RO	0	**Reserved**
2:0	RO	0	**SD Mode : Write Data CRC Status** These 3 bits contains the CRC status data of write operation. These 3 bits reflect the value which card sends to the host. 010: Transmission is ok. 101: Error occurs. **SPI Mode: Write Data Response**

Offset Address: 2Bh (SDC-MMIO) – Reserved

Offset Address: 2Ch (SDC-MMIO)

Response Timeout **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	**Number of Clocks Before A Response Timeout**

Offset Address: 2D-33h (SDC-MMIO) – Reserved

Offset Address: 34h (SDC-MMIO)

Extended Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Speed Bus Mode Selectioncheck_dff_clock_domain.pl** Set this bit when the controller works under clock frequency 33MHz or 48MHz. 0: Normal speed mode 1: High speed mode
6	RW	0	**Auto Stop Token Generation When Multiple Blocks Write Command Completes** For SPI mode only. 0: No stop token generated after multiple block Write command complete 1: Generate stop token automatically after multiple block Write command complete
5	RW	0	**Issue Bad Data (CRC = 0)** 0: Not issue 1: Issue data with wrong CRC
4	RW	0	**Issue Bad Command (CRC = 0)** 0: Not issue 1: Issue command with wrong CRC
3	RW1C	0	**Reload Block Count** This bit only takes effect during multiple blocks write. If this bit is set, controller will generate the same multiple blocks write transfer directly after finishing current multiple blocks transfer. When the new transfer starts, this bit is cleared.
2	RW	0	**MMC 8-Bit Bus Width Selection** 0: Normal mode 1: 8-bit mode. Before setting this bit, set Rx08[1]=0 first. Otherwise SD bus will meet error.Rx08[1] and this bit can not be set at the same time.
1	RW	0	**Command Argument Shift 9 Bits During R/W Command**
0	RW	0	**Auto Stop Command Generation When Multiple Blocks R/W Command Complete** For SD mode only. It is highly recommended to set this bit. 0: No CMD12 after multiple blocks data transfer. 1: Generate stop command CMD12 automatically after finishing multiple blocks data transfer.

Offset Address: 35-FFh (SDC-MMIO) – Reserved

Data DMA Control Registers (00-FFh)

Offset Address: 03-00h (Data DMA-MMIO)

Data DMA Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data DMA Base Address** ***When Write:*** Base Address for Data DMA. ***When Read:*** Current memory address will be read if DMA is busy or Base Address for Data DMA if DMA is idle. When DMA hang and the transfer direction is from device to memory, read from this register can be referred to judge how many data in bytes are valid in memory. When DMA hang and the transfer direction is from memory to device, read from this register is no meaning for the DMA has a FIFO and shift register.

Offset Address: 07-04h (Data DMA-MMIO)

Data DMA Terminate Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data DMA Terminate Count** ***When Write:*** This register indicates the data length wanted in the next DMA transaction. ***When Read:*** The data count left to transfer if DMA is busy or terminate count if DMA is idle

Offset Address: 0B-08h (Data DMA-MMIO)

Data DMA Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RW	0	**Data DMA Soft Reset** Write 1 to reset data DNA. It's a soft reset bit that changes to 0 automatically.
23:17	RO	0	**Reserved**
16	RW	0	**Enable IRQ after Transfer Finished** 0: Disable 1: Enable
15:11	RO	0	**Reserved**
10	RW	0	**Mode Select for DMA Data Empty / Full** 0: Nature mode. The empty and full from Data DMA will reflect the actual state of internal FIFO; thus, when DMA is idle, full will be 0 and empty will be 1. 1: Hold mode. The empty and full from Data DMA will reflect the actual state of internal FIFO when DMA is busy. But when DMA is idle, full will be 0 and empty will be 1 if bit 8 is 1; full will be 1 and empty will be 0 if bit 8 is 0.
9	RW	0	**Controller Data Bus Width** 0: 8 bits 1: 16 bits
8	RW	0	**Transaction Direction** 0: From card to memory 1: From memory to card
7:0	RO	0	**Reserved**

Offset Address: 0F-0Ch (Data DMA-MMIO)

Data DMA Status 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16	RW1C	0	**IRQ Status** IRQ will assert when this bit is set and IRQ is enabled.
15:0	RO	0	**Reserved**

Offset Address: 13-10h (Data DMA-MMIO)

Data DMA Status 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**DMA Busy Status** 0: DMA is idle. 1: Start DMA transfer and DMA is busy. The controller will set this bit to 1 when trigger data transfer, and it can reset automatically after data transfer.

Offset Address: 14-FFh (Data DMA-MMIO) – Reserved

CICH DMA Control Registers (00-FFh)

Offset Address: 03-00h (CICH DMA-MMIO)

Scatter-Gather Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Scatter-Gather Descriptor Base Address** The starting address of the first descriptor in the Scatter-Gather descriptor list.
1:0	RO	0	**Reserved**

Offset Address: 07-04h (CICH DMA-MMIO)

Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RO	0	**Current Descriptor Address** After Rx08[0] is triggered, this register will keep updating to reflect descriptor execution process. This register always contains the current descriptor starting address.
1:0	RO	0	**Reserved**

Offset Address: 0B-08h (CICH DMA-MMIO)

Engine Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:5	RO	0	**Reserved**
4	RW	0	**Reserved**
3	RW	0	**Stop Current Descriptor List Execution** 0: Disable 1: Enable The driver might cancel current descriptor list execution. When this bit asserts, the descriptor engine will stop after current descriptor execution finishes. This bit will de-assert automatically.
2	RW	0	**Reset Engine** 0: Disable 1: Enable After exception handling, software can set this bit to reset the SG DMA, Descriptor Register File and the Descriptor Interpreter. This will terminate execution of the current descriptor list. This bit will de-assert automatically after several clocks when reset complete.
1	RW	0	**Resume Descriptor Execution** 0: Disable 1: Enable After exception handling, software can set this bit to resume the descriptor execution from the next descriptor in current list. This bit will de-assert automatically after one clock cycle.
0	RW	0	**Start Descriptor Execution** 0: Disable 1: Enable Software can set this bit to start executing a new descriptor list. The starting address of the list is specified by CICH DMA-MMIO Rx00[31:2]. This bit will de-assert automatically after one clock cycle.

Offset Address: 0F-0Ch (CICH DMA-MMIO)

Status Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Reserved**
21:20	RO	00b	**Descriptor Engine Status** 00: Idle. Engine is not executing any descriptor. 01: Busy. Engine is fetching or executing descriptor. 10: Wait. Engine is waiting for controller interrupt. 11: Stall. Exception happens, engine stalls.
19	RO	0	**xDC Interrupt Request** This bit reflects the interrupt request status of xDC. 0: xDC is not requesting to interrupt CPU. 1: xDC is requesting to interrupt CPU.
18	RO	0	**SDC Interrupt Request** This bit reflects the interrupt request status of SDC. 0: SDC is not requesting to interrupt CPU. 1: SDC is requesting to interrupt CPU.
17	RO	0	**Reserved**
16	RO	0	**DMA Interrupt Request** This bit reflects the interrupt request status of normal DMA engine. 0: Normal DMA engine is not requesting to interrupt CPU. 1: Normal DMA engine is requesting to interrupt CPU.
15:10	RO	0	**Reserved**
9	RW1C	0	**Slot Execution Done**
8	RW1C	0	**Current Descriptor List Execution Stopped** This bit will assert after current descriptor finishes when the software tries to stop current descriptor list execution by programming CICH DMA-MMIO Rx08[3]. 0: Normal execution 1: Execution stopped
7	RW1C	0	**Interrupt Clear Failed** This bit will assert when the descriptor engine try to clear the interrupt status but the interrupt signal keeps asserting. 0: Interrupt cleared successfully. 1: Failed to clear interrupt.
6	RW1C	0	**Interrupt Status Error** This bit will assert when the status register bit hits the exception pattern. 0: No exception detected from card controller 1: Exception detected from card controller
5	RO	0	**Reserved**
4	RW1C	0	**Descriptor List Execution Complete** After the last descriptor in the list execution finishes, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: Descriptor list execution is not complete. 1: Descriptor list execution is complete.
3	RW1C	0	**Descriptor Execution Complete** After current descriptor execution finishes, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: Descriptor execution is not complete. 1: Descriptor execution is complete.
2	RW1C	0	**Descriptor Format Errors Interrupt** When there is any error exists within the descriptor itself, this bit will assert and interrupt CPU if interrupt generation is enabled. For example: Reserved encoding used by the software. 0: No error detected 1: Error detected
1	RW1C	0	**Controller Exceptions Interrupt** When the card controllers or the normal DMA engine assert interrupt request signal caused by exception conditions, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: No exception condition reported by controller 1: Exception condition reported by controller
0	RW1C	0	**Interrupt of Waiting for Controller Interrupt Time Out** When the CRDE (Card Reader Description Engine) is waiting for the controller to issue interrupt request signal, if no interrupt is detected after timer expires, this register bit will assert and interrupt CPU if interrupt generation is enabled. 0: Not time out 1: Time-out happens

Offset Address: 13-10h (CICH DMA-MMIO)

Engine Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17:16	RW	00b	**Wait for Controller Interrupt Time-Out Counter** 00: Never time out 01: Time out after 1 us 10: Time out after 1 ms 11: Time out after 1024 ms
15:11	RO	0	**Reserved**
10	RW	0	**Enable Interrupt On Complete** 0: Disable 1: Enable
9	RW	0	**Enable Slot Execution Done Interrupt** 0: Disable 1: Enable
8	RW	0	**Enable Current Descriptor List Execution Stopped Interrupt** 0: Disable 1: Enable
7	RW	0	**Enable Interrupt Clear Failed Interrupt** 0: Disable 1: Enable
6	RW	0	**Enable Interrupt Status Error Interrupt** 0: Disable 1: Enable
5	RW	0	**Enable Wrong Interrupt Source Interrupt** 0: Disable 1: Enable
4	RW	0	**Enable Descriptor List Execution Complete Interrupt** 0: Disable 1: Enable
3	RW	0	**Enable Descriptor Execution Complete Interrupt** 0: Disable 1: Enable
2	RW	0	**Enable Descriptor Format Errors Interrupt** 0: Disable 1: Enable
1	RW	0	**Enable Controller Exceptions Interrupt** 0: Disable 1: Enable
0	RW	0	**Enable Interrupt of Waiting for Controller Interrupt Time Out** 0: Disable 1: Enable

Offset Address: 14-FFh (CICH DMA-MMIO) – Reserved

PCI Control Registers (00-FFh)

Offset Address: 00-01h (PCI Control-MMIO) – Reserved

Offset Address: 02h (PCI Control-MMIO)

Clock Gating Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Power On / Off Select** The signal outputs from pad to control the power supplied for device. If card insert socket, driver should set this bit 1 to let CR socket and pads have power supply. Also driver can clear this bit to shut down the pad and socket power. When CR SD/XD card removed, hardware will automatically clear this bit. 0: Power off 1: Power on
4	RW	1b	**Pad Power Select** Select the pad power according to the device supply voltage. 0: 1.8V 1: 3.3V
3:2	RW	0	**Reserved**
1	RW	0	**Enable Clock Gating** 0: Disable 1: Enable
0	RW	1b	**Soft Reset** 0: Soft reset all the controller and it will be de-asserted automatically 1: Soft reset is de-asserted

Offset Address: 03h (PCI Control-MMIO)

xDC Clock Control **Default Value: 06h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	110b	**Clock Select** 000: 12M 001: 24M 010: 48M 011: Reserved 100: 8M 101: 16M 110: 33M 111: Reserved

Offset Address: 04h (PCI Control-MMIO) – Reserved

Offset Address: 05h (PCI Control-MMIO)

SDC Clock Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	011b	**Clock Select** 000: 12M 001: 24M 010: 48M 011: 375K 100: 8M 101: 16M 110: 33M 111: Reserved

Offset Address: 06h (PCI Control-MMIO) – Reserved

Offset Address: 07h (PCI Control-MMIO)

DMA Clock Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	000b	**Clock Select** 000: xDC 001: Reserved 010: SDC 011: Reserved 1xx: Reserved

Offset Address: 08h (PCI Control-MMIO)

Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable 60M Clock Stop Interrupt** 0: Disable 1: Enable
5	RW	0	**Enable CICH Interrupt** 0: Disable 1: Enable
4	RW	0	**Enable DMA Interrupt** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**Enable SDC Interrupt** 0: Disable 1: Enable
1	RW	0	**Reserved**
0	RW	0	**Enable xDC Interrupt** 0: Disable 1: Enable

Offset Address: 09h (PCI Control-MMIO)

Interrupt Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**60M Clock Stop Interrupt** 0: The clock 60MHz from USBPHY is running 1: The clock 06MHz from USBPHY is stopped
5	RO	0	**CICH Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
4	RO	0	**DMA Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
3	RO	0	**Reserved**
2	RO	0	**SDC Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
1	RO	0	**Reserved**
0	RO	0	**xDC Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred

Offset Address: 0Ah (PCI Control-MMIO)

Time Out Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	000b	**Time-Out Control** 000: No time-out 001: 32 us time-out 010: 256 us time-out 011: 1024 us time-out 100: 256 ms time-out 101: 512 ms time-out 110: 1024 ms time-out 111: Reserved

Offset Address: 0B-FFh (PCI Control-MMIO) – Reserved

DEVICE 15 FUNCTION 0 (D15F0): SERIAL ATA CONTROLLER

Device 15 Function 0 implements only one channel of the ATA controller: the primary channel includes 2 SATA ports, and the secondary channel is empty. Each of those two ports has its own PHY and Link Layer, yet the Transport Layer is shared.

Within the BIOS boot time (before the control is passed to the OS), the access to SATA device is through legacy PIO mode. While in Microsoft Windows system, unless custom driver is installed, OS will use its default driver to access the SATA devices. The standard method to accesses SATA devices is through the standard PCI IDE Bus Master mode.

When SATA controller is configured as Native Mode (refer to the table under Rx0Ah), the SATA controller uses the Interrupt Pin defined in Rx3Dh. For Compatibility Mode, as defined for legacy usage, the Primary Channel (SATA) is assigned with IRQ14. Throughout this chapter when Primary Channel is mentioned it stands for SATA controller.

Top Level Block Diagram

The shaded block in the diagram below is the SATA controller. The definitions for the abbreviation used in the diagram are listed below.

-- **PCCA:** block contains PCI + CCA Module
-- **CCA:** Concurrent CPU Access
-- **SAPCIS:** SATA PCI Slave Control Block

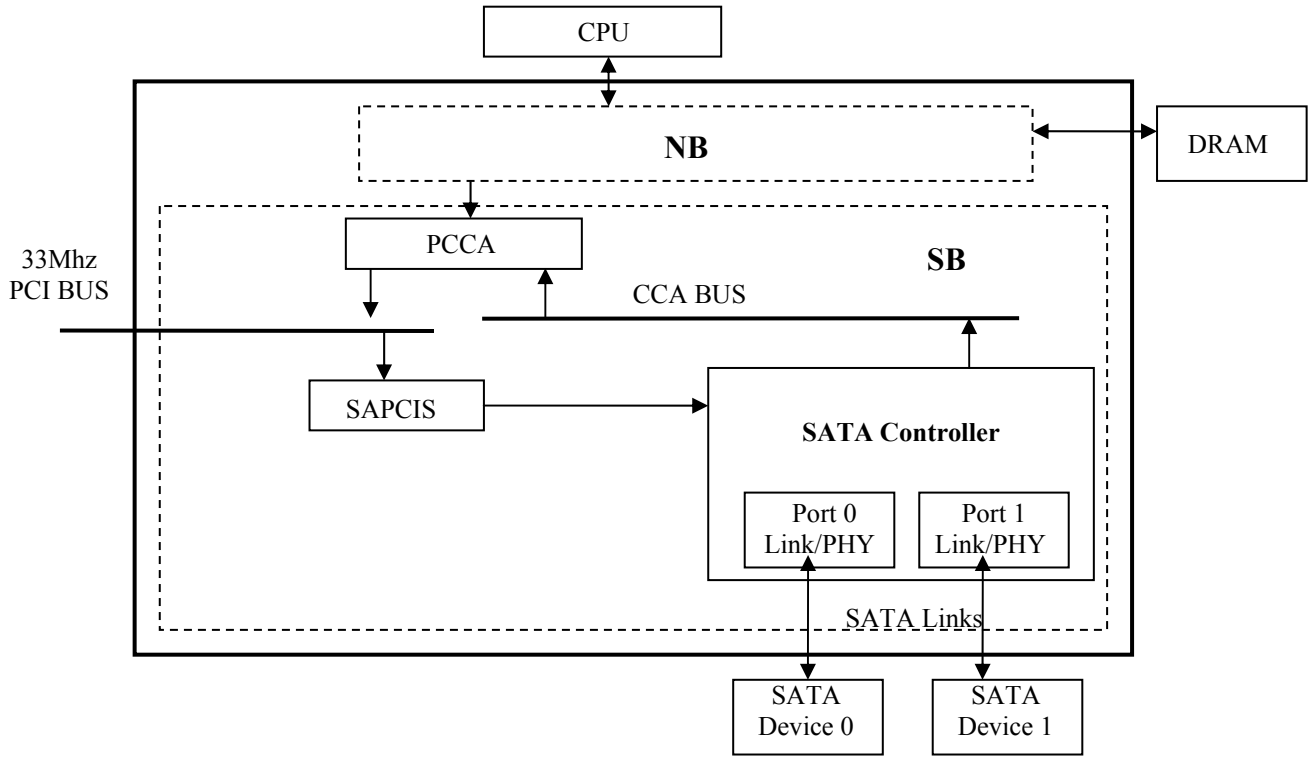


Figure 53. System Block Diagram

ATA Legacy Control, Command and Status Registers (Shadow Registers)

Chip Select CS[1:0]	Address Offset (Native Mode)	IO Address (Compatibility Mode)		RegisterDescription
		Primary	Secondary	
01b	00h	1F0h	170h	Data Register
01b	01h	1F1h	171h	Features(W) / Error(R)
01b	02h	1F2h	172h	Sector Count
01b	03h	1F3h	173h	LBA Low
01b	04h	1F4h	174h	LBA Mid
01b	05h	1F5h	175h	LBA High
01b	06h	1F6h	176h	Device
01b	07h	1F7h	177h	Command(W) / Status(R)
10b	06h	3F6h	376h	Device Control (W)
10b	06h	3F6h	376h	Alternate Status (R)

Status Register:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BSY	DRDY	#	#	DRQ	Obsolete	Obsolete	ERR

-- BSY is set to indicate that the device is busy.
-- DRDY is device ready. DRDY shall be set/clear by the device.
-- DRQ is data request. It is set when the device is ready to transfer a word of data between the device and the host.
-- ERR indicates that an error occurred during the execution of the previous command.

Alternate Status Register:
This register contains the same information as the Status Register in the command block..

Device Control Register:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
HOB	Reserved	Reserved	Reserved	Reserved	SRST	nIEN	0

-- SRST is the Host Software Reset bit
-- nIEN is the enable bit for the device assertion of INTRQ to the host.
-- HOB defines whether the current or previous content of the registers is placed on the Data Bus DD[7:0].
-- HOB is only used for devices implementing 48-bit address feature set.

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D15F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D15F0)

PCI Device ID Register **Default Value: 9001h**

Bit	Attribute	Default	Description
15:0	RO	9001h	**Device ID**

Offset Address: 05-04h (D15F0)

PCI Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable**
9:7	RO	0	**Reserved**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping**
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master**
1	RW	0	**Memory Space Access**
0	RW	0	**I/O Space Access** When the "I/O Space" bit is disabled, the device will not respond to I/O addresses. 0: Not respond to I/O address 1: Respond to I/O address

Offset Address: 07-06h (D15F0)

PCI Status Register **Default Value: 0290h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error**
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 01: Medium (Default)
8	RO	0	**Master Data Parity Error**
7	RO	1b	**Fast Back-to-Back Capability**
6	RO	0	**Reserved**
5	RO	0	**66 MHz Capable**
4	RO	1b	**Power Management Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D15F0)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 09h (D15F0)

Programming Interface: For SATA Mode (Rx0A = 04h) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Hardwired to 0**

Programming Interface: For IDE Compatibility and Native Modes (Rx0A = 01h) **Default Value: 8Ah**

Bit	Attribute	Default	Description
7	RO	1b	**Master IDE Device**
6:4	RO	0	**Fixed at 0.**
3	RO	1b	**Reserved**
2	RW	0	**Reserved**
1	RO	1b	**Programmability Indicator – Primary Channel** 0 : Operating Mode is not programmable, and is indicated by bit 0 1 : Operating Mode is programmable by writing the desired mode to bit 0 This bit is hard-wired to 1.
0	RW	0	**Operating Mode – Primary channel** 0: Compatible mode 1: Native mode Note: Only by configuring this register the operating mode of SATA could be changed.

Note: D15F0 defines one storage host controllers. The Primary Channel is a SATA controller and the Secondary Channel is empty. The host interfaces to two SATA controllers can be configured to five cases as shown in the following table.

Rx0A	Rx09	Interface for Primary Channel (SATA)
01h	8Ah	IDE Compatibility mode
01h	8Eh	IDE Compatibility mode
01h	8Bh	IDE Native mode
01h	8Fh	IDE Native mode
04h	00 h	SATA(Native) mode

Offset Address: 0Ah (D15F0)

Sub Class Code **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Sub Class** 01h: IDE Controller 04h: SATA Controller According to PCI Spec V3.0 Rx0A=04h is for RAID Controller, and Rx0A=06h is for SATA Controller. With historical reason and for being compatible with previous BIOS/Drivers, for Rx0A=04h still means SATA Controller in this chip. Note: The Sub Class code can be modified if the protection is disabled by setting Rx45[7] to.1.

Offset Address: 0Bh (D15F0)

Base Class Code **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Base Class** 01h: Mass Storage Controller

Offset Address: 0Ch (D15F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size** Fixed at 0.

Offset Address: 0Dh (D15F0)

Latency Timer **Default Value: 20h**

Bit	Attribute	Default	Description
7:4	RW	2h	**Latency Timer**
3:0	RO	0	**Fixed at 0.**

Offset Address: 0Eh (D15F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Multiple Function Device**
6:0	RO	0	**Fixed at 0.**

Offset Address: 0Fh (D15F0) – Reserved

Offset Address: 13-10h (D15F0)

Primary Channel: Data / Command Base Address (IDE Compatibility Mode) **Default Value: 0000 0000h**

Specify an 8 bytes I/O address space: **For IDE Compatibility Mode (Rx0A=01h, Rx09[0] = 0)**

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Primary Channel: Data / Command Base Address (SATA Mode) **Default Value: 0000 01F1h**

Specify an 8 bytes I/O address space: **For SATA Mode (Rx0A = 04h)**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:4	RW	01Fh	**IO Port Address [15:4]**
3	RW	0	**IO Port Address [3]**
2:0	RO	001b	**IO Port Address [2:0]**

Offset Address: 17-14h (D15F0)

Primary Channel: Control / Status Base Address (IDE Compatibility Mode) **Default Value: 0000 0000h**

Specify a 4 bytes I/O address space: For IDE Compatibility Mode (Rx0A=01h, Rx09[0] = 0)

Bit	Attribute	Default	Description
31:0	RO	0	**Reserved**

Primary Channel: Control / Status Base Address (SATA Mode) **Default Value: 0000 03F5h**

Specify a 4 bytes I/O address space: For SATA Mode (Rx0A = 04h)

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:4	RW	03Fh	**IO Port Address [15:2]**
3:2	RW	01b	**IO Port Address [3:2]**
1:0	RO	01b	**IO Port Address [1:0]**

Offset Address: 1F-18h (D15F0) - Reserved

Offset Address: 23-20h (D15F0)

IDE Bus Master Registers Base Address for Both Channels **Default Value: 0000 CC01h**

Specify a 16-byte I/O address space for IDE Bus Master (EIDE) mode.

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:4	RW	CC0h	**IO Port Address(Random)**
3:0	RO	0001b	**IO Port Address**

Offset Address: 24-2Bh (D15F0) - Reserved

Offset Address: 2D-2Ch (D15F0)

Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D15F0)

Subsystem ID **Default Value: 9001h**

Bit	Attribute	Default	Description
15:0	RO	9001h	**Subsystem ID**

Offset Address: 30-33h (D15F0) - Reserved

Offset Address: 34h (D15F0)

Power Management Capabilities Pointer **Default Value: B0h**

Bit	Attribute	Default	Description
7:0	RO	B0h	**Power Management Capabilities Pointer**

Offset Address: 35-3Bh (D15F0) - Reserved

Offset Address: 3Ch (D15F0)

Interrupt Line **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:4	RO	0	**IDE Interrupt Routing – High Byte** If bits [7:4] is set to Fh,-interrupt will be masked; otherwise, bits [3:0] are decoded to IRQ0~IRQ15 as following: 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Disable 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Disable 1110: IRQ14 1111: IRQ15
3:0	RO	Eh	**IDE Interrupt Routing – Low Byte** If bits [7:4] is set to Fh,-interrupt will be masked; otherwise, bits [3:0] are decoded to IRQ0~IRQ15 as following: 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Disable 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Disable 1110: IRQ14 1111: IRQ15

Note: This Interrupt Line setting is to route the Interrupt Pin to one of the 16 system IRQs.

Offset Address: 3Dh (D15F0)

Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	000b	**Interrupt Pin** ***For IDE Compatibility Mode:*** Set to 000b. ***Else: (For IDE/SATA Native Mode)*** 001b = INTA# 010b = INTB# 011b = INTC# 100b = INTD#

Offset Address: 3E-3Fh (D15F0) - Reserved

SATA Registers (40-54h)

Offset Address: 40h (D15F0)

SATA Channel Enable **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**Reserved**
1	RW	1b	**Primary Channel (SATA) IO Access** 0: Disable 1: Enable Setting 0 will disable all IO cycles addressed to the Primary Channel. This basically disables the SATA functions in the primary channel. However, the configuration cycles addressed to this Function (D15F0) would still be allowed. Please also check RxB9[7].
0	RW	1b	**Reserved (Do Not Program)**

Note: Here is a comparison of three different ways to partially or completely disable SATA functions:

1. D15F0Rx40[1]=0: Disable all IO cycle accesses to the Primary Channel SATA controller.
2. D17F0Rx50[3]=0: Disable all Downstream cycles, including Configuration cycles, IO and memory cycles to both Primary and Secondary Channels.
3. D15F0RxB9[7]=1: Reset SATA controller, gate out the clock to the PHY logic of both Ports, and also power down the PHY blocks.

Offset Address: 41h (D15F0)

SATA Interrupt **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**PERR Check** When disabled, the interrupt caused by PERR# will not be generated. 0: Disable 1: Enable
2	RW	0	**SERR Check** When disabled, the interrupt caused by SERR# will not be generated. 0: Disable 1: Enable
1	RW	1b	**Block Interrupt Till Read FIFO Empty for A DMA Read** 0: Disable 1: Enable For a normal DMA data read sequence, once the interrupt service bit in the register FIS is set by the device at the end of data transfer, the host controller has to relay the interrupt to the CPU. In an effort to prevent data incoherency (e.g. Interrupt Service software is trying to read data, but the data have not reached the system memory yet.) the host should not issue an interrupt until the data in the read FIFO have been completely flushed to the system memory. Thereby before the read FIFO is empty the interrupt to the CPU must be blocked. Note that this bit should be set to 1 (Enable) in normal operation.
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 43h (D15F0) – Reserved

Offset Address: 44h (D15F0)

Miscellaneous Control 1 **Default Value: 87h**

Bit	Attribute	Default	Description
7	RW	1b	**66MHz for DMA Data Path Dynamic Clock Gating** 0: Enable 1: Disable The Dynamic Clock Gating is designed for power savings. If enabled, the 66Mhz clock for the DMA data path will be blocked when the DMA data path is not actively transferring data.
6:5	RW	0	**Reserved**
4:3	RW	0	**Reserved (Do Not Program)**
2	RW	1b	**Reserved (Do Not Program)**
1	RW	1b	**Reserved (Do Not Program)**
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 45h (D15F0)
Miscellaneous Control 2 **Default Value: AFh**

Bit	Attribute	Default	Description
7	RW	1b	**Sub Class (Rx0A) Write Protect** 0: Enable write 1: Disable write
6	RW	0	**PCICLK and Host Clock Dynamic Clock Gating** a) 33MHz PCICLK is used to clock register configuration. b) 66MHz Host Clock is used for the control logic (as opposed to the clock for data path in Rx44[7]) in DMA controller. 0: Enable clock gating 1: Disable clock gating
5	RW	1b	**Reserved (Do Not Program)**
4	RW	0	**Interrupt Line (Rx3C) Write Protect** 0: Enable Rx3C write 1: Disable Rx3C write
3:2	RW	11b	**Reserved (Do Not Program)**
1	RW	1b	**Flush Primary Channel Read DMA Data After Interrupt** The default value must not be altered. 0: Disable 1: Enable For a normal DMA data read sequence, once the interrupt service bit in the register FIS is set by the device at the end of data transfer, the host controller has to relay the interrupt to the CPU. In an effort to prevent data incoherency (e.g. Interrupt Service software is trying to read data, but the data have not reached the system memory yet.) the host should not issue an interrupt until the data in the read FIFO have been completely flushed to the system memory. Thereby before the interrupt request is sent to the CPU, the DMA read FIFO must be emptied first. Note that in normal operation this bit should never be set to Disable. Also note that compared to Rx41[1], these two bits pretty much serve the same purpose, and should be consolidated in the future to avoid confusion and possible conflict.
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: 46h (D15F0)
Miscellaneous Control 3 **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**Allow Port 1 To Receive D2H FIS When Port 0 Is The Active Port** The default value must not be altered. 0: Enable 1: Disable
6	RW	0	**Transport Layer Logic Dynamic Clock Gating** When the Transport Layer is idle, the supply clock to those logic will be gated out (blocked). 0: Enable clock gating 1: Disable clock gating
5	RW	0	**Assert Interrupt to CPU When a SATA Device is Hot-Plugged** 0: Disable 1: Enable
4	RW	0	**Reserved (Do Not Program)**
3	RW	1b	**Allow Port 0 To Receive D2H FIS When Port 1 Is The Active Port** The default value must not be altered. 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	0	**Early ADS# for PIO Write Cycle** The default value must not be altered. The host side interface of this SATA controller is PCI Bus. For a PIO Write cycle by setting this bit to "1" the internal write cycle can begin (internal ADS# issued) on the next clock after FRAME#/COMMAND is asserted on the PCI Bus. Otherwise, the internal ADS# will not be issued until IRDY# is asserted, i.e. until the data are ready to send to the target. Since the PIO Write data are at most 4 bytes, this savings of 1 to 2 PCI clocks can be significant in the case when the accesses are mostly PIO Writes. 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 47-49h (D15F0) – Reserved

Offset Address: 4Ah (D15F0)
SATA DIPM and Hot Plug Feature **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved** BIOS/SW uses this register to indicate support of DIPM/Hot Plug feature. Hardware never uses this register.
1	RW	0	**SATA Port 1 (Slave) Hot-plug / Link PM Feature Select** 0: Hot-plug. VIA SATA driver will check SATA PHY state change as hot-plug event. 1: Link PM with Device Initiated Power Management. VIA SATA driver enables and maintains the DIPM feature if the connected SATA device supports this feature.
0	RW	0	**SATA Port 0 (Master) Hot-plug / Link PM Feature Select** 0: Hot-plug. VIA SATA driver will check SATA PHY state change as hot-plug event. 1: Link PM with Device Initiated Power Management. VIA SATA driver enables and maintains the DIPM feature if the connected SATA device supports this feature.

Offset Address: 4B-52h (D15F0) - Reserved

Offset Address: 53h (D15F0)
SATA Command Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**TP Layer Idle at least 20us before the Following Command Being Executed** 0: Disable 1: Enable
6	RW	0	**Select the Least Time TP Layer should be Idle Before the Following Command Being Executed** 0:20us 1:40us
5	RW	0	**Reserved**
4	RW	0	**Issuing COMRESET when SATA Controller Receive COMINIT in Power Mode** 0: Disable 1: Enable
3:0	RW	0	**Reserved**

Offset Address: 54h (D15F0) - Reserved

SATA (Primary Channel) Link Control Registers (55-56h)

Offset Address: 55h (D15F0)

SATA Link Control Register 1 **Default Value: DCh**

Bit	Attribute	Default	Description
7	RW	1b	**Host Always Transmits 6 COMRESET for Power-on Sequence** The default value must not be altered. 0: Disable 1: Enable
6	RW	1b	**Limit Continuous Asynchronous Recovery to Five Times Only** 0: Disable 1:Enable
5	RW	0	**Conditions to Allow Back to Back Requests of Entering C4P** The condition defines when a back-to-back Entering C4P Request can be granted while the SATA controller is currently resuming from the C4P state. 0: Allow C4P state to be entered again after PHYRDY. 1: Allow C4P state to be entered again after the Host has received X_RDYp primitive from the Device. Note: 1. C4P state is a special power state for VIA CPU. It is a proprietary sub-state of the normal ACPI C4 state. 2. For a normal resume procedure from a Partial/Slumber state at the end of OOB, the PHYRDY will occur first. Then by reading the Device Status, that is a Register D2H FIS, the Device will have to send X_RDYp primitive to the Host before sending the data.
4	RW	1b	**66MHz GCLK Dynamic Gating** This clock is used to latch the Auto-Compensation (for termination resistance at Rx68) setting at the end of the hardware reset. Once the AutoComp values are latched, this clock is no longer needed. 0: Disable GCLK gating after hardware reset 1: Enable GCLK gating after hardware reset
3	RW	1b	**SATA 33MHz Dynamic Clock Gating for Power Mode – Port 1** 0: Disable 1: Enable The logic of 33 Mhz domain in the Link and PHY layers of Port 1 is only used during entering or exiting Partial/Plumber mode. Setting this bit to "1" will gate the 33 Mhz clock to these logic when they are not actively used.
2	RW	1b	**SATA 33MHz Dynamic Clock Gating for Power Mode – Port 0** 0: Disable 1: Enable The logic of 33 Mhz domain in the Link and PHY layers of Port 0 is only used during entering or exiting Partial/Plumber mode. Setting this bit to "1" will gate the 33 Mhz clock to these logic when they are not actively used.
1:0	RW	0	**Reserved (Do Not Program)**

Offset Address: 56h (D15F0)

SATA Link Control Register 2 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Await Sync Before Returning to D0 (Ready & Idle)** In waking up from Partial/Slumber mode, if this bit is enabled the Host will not return to D0 state until a SYNC primitive is received from the Device. 0: Disable 1: Enable
6	RW	1b	**33MHz Dynamic Clock Gating for Downstream Cycles** This 33Mhz clock controls the logic inside SATA's PCI interface block for PCI slave cycles 0: Enable. The clock would be gated when the controlled logic is idle. 1: Disable. The clock continues running even when the controlled logic is idle.
5	RW	0	**Receiver Scrambler** 0: Enable 1: Disable
4	RW	0	**Transmitter Scrambler** 0: Enable 1: Disable
3	RW	0	**Align Primitive Transmission** 0: Enable 1: Disable
2	RW	0	**Continue Primitive Transmission** 0: Enable 1: Disable
1	RW	0	**(ALIGNp + CONTp) Primitives Transmission** 0: Enable 1: Disable
0	RW	0	**Link Layer Dynamic Clock Gating** This is the 37.5 Mhz clock for Gen1, and 75 Mhz clock for Gen2. 0: Enable. The clock would be gated when the controlled logic is idle. 1: Disable. The clock continues running even when the controlled logic is idle.

SATA PHY Control Registers (57-5Eh)

Offset Address: 57h (D15F0)

PHY Test Mode Control 1 **Default Value: 30h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:3	RW	110b	**Reserved (Do Not Program)**
2:0	RW	0	**Reserved (Do Not Program)**

Note: SATA EPHY is the basic interface to the transmission line. It consists of the high speed differential drivers and receivers as well as the OOB signaling circuitry. Refer to SATA Specification for more details.

Offset Address: 58h (D15F0)

PHY Test Mode Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Select PHY Operating Speed for Test Mode** Select the link speed for TX2RX (TX to RX) or TX only (send patterns) test mode. 0: Gen1 1: Gen2
6	RW	0	**Serial Data Transmit Internal Loopback** 0: Disable look back 1: Enable look back
5	RW	0	**PHY Test Mode Enable** 0: Disable 1: Enable This is the master switch to enable PHY test. Note that in Test Mode the pre-selected/mapped internal signals can be output to the IDE data pins for debugging. For the actual signal mapping refer to the table between Rx60-61h.
4	RW	0	**PHY Test Port Select** 0: Port 0 1: Port 1
3:0	RW	0	**PHY Test Pattern Select** 1001b: LTDP (Low Transition Density pattern) 1010b: HTDP (Half-rate/quarter-rate High Transition Density pattern) 1011b: LFSCP (Low Frequency Spectral Content pattern) 1100b: SSOP (Simultaneous Switching Outputs pattern)

The following table defines the patterns selectable by Rx58[3:0]:

Table 42. Rx58[1]

Rx58[3:0]	Abbreviation	Function Description
0000	Invalid	TxValid =0, The output driver DRV is tri-stated.
0010	Test ComInit	ComInit pattern.
0011	Test ComWake	ComWake pattern.
0100	Test K	All zero pattern.
0101	Test J	All one pattern.
0110	Test D10.2/D24.3/D30.3	Rx57[7:6]: 00: D10.2 HFTP 01: D24.3 MFTP 10: D30.3 LFTP 11: reserved
0111	Test Align	Align primitive for alignment.
1000	Fill Align	The delay from Tx to Rx buffer is ~8.5T ( ). This Align primitive can be selected before and after the actual test patterns to fill the gaps, isolate test patterns, and make it easier to identify the source (which test pattern) of errors (Rx5B[0]=1).
1001	LTDP	Low transition density
1010	HTDP	High transition density
1011	LFSCP	Low frequency spectral
1100	SSOP	Simultaneous switching
1101	LBP patterns	Check lone-bit. There are two versions of LBPs, which can be selected by Rx61[6]. Rx61[6]: 0: LBP pattern in spec (This pattern is obsolete after version 2.6.) 1: LBP Harvey pattern (defined in ECN18. This is the pattern actually got used)
1110	COMP	There are short and long form of COMP patterns. Rx5D[6] will determine which one to send.

Note: The polarity (Rd+ or Rd-) of the selected pattern is determined by Rx5D[7].

Offset Address: 59-5Bh (D15F0) - Reserved

Offset Address: 5Ch (D15F0)

PHY Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved (Do Not Program)**
5	RW	0	**SATA PHY Dynamic Clock Gating** This bit when enabled will gate the 150 Mhz clock in PHY OOB detect circuit and 37.5Mhz clock in PHY layer state machine circuit during Partial or Slumber. 0: Enable 1: Disable
4	RW	0	**Select The Number of Consecutive Data Bursts for COMRESET and COMWAKE** 0: 6 consecutive data bursts 1: 12 consecutive data bursts
3	RW	0	**SATA PHY Dynamic Clock Gating** This bit when enabled will gate the 150 Mhz clock in PHY OOB detect circuit and 37.5Mhz clock in PHY layer state machine circuit during Partial or Slumber. 0: Enable 1: Disable
2	RW	0	**Reserved (Do Not Program)**
1	RW	0	**Disable Port 1 PHY** 0: Disable 1: Enable
0	RW	0	**Disable Port 0 PHY** 0: Disable 1: Enable

Note: The clocks used in PHY are:

1. TX block: For Gen1, 150Mhz and 150/4=37.5 Mhz ; For Gen2, 300 Mhz and 300/4=75 Mhz
2. RX block: For Gen1, 150Mhz and 150/4=37.5 Mhz ; For Gen2, 300 Mhz and 300/4=75 Mhz

Offset Address: 5Dh (D15F0)

PHY Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Determine Polarity of the Selected PHY Test Pattern** Selected in Rx58[3:0] to start with Rd+ or Rd- 0: Rd- 1: Rd+
6	RW	0	**Reserved** 1: Long pattern))
5	RW	0	**Port 1 Gen2 Support** 0: Enable 1: Disable
4	RW	0	**Port 0 Gen2 Support** 0: Enable 1: Disable
3	RW	0	**PHY Link Speed Negotiation Scheme** 0: Try Gen2 speed three times. If fails, continue to retry with Gen1 speed 1: Continue to retry with Gen2 speed only. Never use Gen 1 speed.
2	RW	0	**Reserved (Do Not Program)**
1:0	RW	0	**Reserved**

Offset Address: 5Eh (D15F0) - Reserved

SATA Hot Plug and RAMBIST Status Registers (5F-63h)

Offset Address: 5Fh (D15F0)

SATA Hot Plug Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW1C	0	**Port 1 Plug Out Status** The status bit will be set to 1 only when a currently connected and detected device is disconnected from the port.
2	RW1C	0	**Port 1 Plug In Status** The status bit will be set to 1 only when a currently connected and detected device is disconnected from the port.
1	RW1C	0	**Port 0 Plug Out Status** The status bit will be set to 1 only when a currently connected and detected device is disconnected from the port.
0	RW1C	0	**Port 0 Plug In Status** The status bit will be set to 1 only when a currently connected and detected device is disconnected from the port.

Offset Address: 60h (D15F0)

Debug Signals Grouping and RAM BIST Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RO	0	**Primary Channel (SATA) RAM BIST Error Status** 0: No error 1: Error detected
0	RW	0	**RAM BIST Control (Write) / Status (Read)** ***For Write:*** Write 1 to start RAM BIST. ***For Read:*** 0: Idle 1: Busy

Offset Address: 61h (D15F0) – Reserved

Offset Address: 62h (D15F0)

SATA Control Register 3 **Default Value: 02h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**SATA LED Control** 0: SATALED0 will blink at 10Hz rate when either SATA Port 0 or Port 1 is actively transferring data. 1: SATALED0 will blink at 10Hz rate when SATA Port 0 is transferring data. SATALED1 will blink at 10Hz rate when Port1 is transferring data.

Offset Address: 63h (D15F0)

SATA Control Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Resend COMRESET When Recovering SATA Gen2 Device Error** 0: Disable 1: Enable
6	RW	0	**Enter TPIDLE When Soft Reset** 0: Disable 1: Enable
5	RW	0	**Reset Drive Select to Master when Change Device Control Register Bit[1] (nIEN)** 0: Disable 1: Enable
4	RW	0	**Port0 PHY Clock Gating (random)** Gate the PHY clock used in LINK and PHY (not include the clock in PHY stat machine and OOB detect circuit). 0: Enable 1: Disable
3	RW	0	**Port1 PHY Clock Gating (random)** Gate the PHY clock used in LINK and PHY (not include the clock in PHY stat machine and OOB detect circuit). 0: Enable 1: Disable
2	RW	0	**Reserved**
1	RW	0	**When Slumber, Gate SATA EPHY MPLL/TPLL** 0: Disable 1: Enable When ENSATAPLLG and ENSAMPLLPD is configured at the same time, the system behavior is shown as below: **EN_SLU_PLLG** / **EN_SLU_PLLD** / **Behavior** x / 1 / Turn off SATA MPLL/TPLL when slumber 1 / 0 / Gate SATA TX clock when slumber 0 / 0 / No special actions take. When slumber
0	RW	0	**Turn Off SATA MPLL/TPLL When Enter Slumber** 0: Disable 1: Enable

SATA EPHY Control Register (64-77h) – For Index Register

Please refer to section SATA EPHY Index Register (SATA-EPHYC) for details.

Offset Address: 64h (D15F0)

SATA EPHY Control Register Data0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	8-bit Data of EPHY Control Register which is Linked by EPHY Register Pointer0

Offset Address: 65h (D15F0)

SATA EPHY Control Register Data1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	8-bit Data of EPHY Control Register which is Linked by EPHY Register Pointer1

Offset Address: 66h (D15F0)

SATA EPHY Control Register Data2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	8-bit Data of EPHY Control Register which is Linked by EPHY Register Pointer2

Offset Address: 67h (D15F0)

SATA EPHY Control Register Data3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	8-bit Data of EPHY Control Register which is Linked by EPHY Register Pointer3

Offset Address: 68h (D15F0)

SATA EPHY Control Register Pointer0-1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**EPHY Control Register Address Pointer 1** Indicates the offset of the pointed EPHY register. 0000: 1 0001: 5 0010: 9 0011: 13 0100: 17 0101: 21 0110: 25 0111: 29 1000: 33 1001: 37 1010: 41 1011: 45 1100: 49 1101: 53 1110: 57 1111: 61
3:0	RW	0000b	**EPHY Control Register Address Pointer 0** 0000: Point to EPHY Register which offset is 0 0001: Point to EPHY Register which offset is 4 0010: Point to EPHY Register which offset is 8 0011: Point to EPHY Register which offset is 12 0100: Point to EPHY Register which offset is 16 0101: Point to EPHY Register which offset is 20 0110: Point to EPHY Register which offset is 24 0111: Point to EPHY Register which offset is 28 1000: Point to EPHY Register which offset is 32 1001: Point to EPHY Register which offset is 36 1010: Point to EPHY Register which offset is 40 1011: Point to EPHY Register which offset is 44 1100: Point to EPHY Register which offset is 48 1101: Point to EPHY Register which offset is 52 1110: Point to EPHY Register which offset is 56 1111: Point to EPHY Register which offset is 60

Offset Address: 69h (D15F0)

SATA EPHY Control Register Pointer2-3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**EPHY Control Register Address Pointer 3** 0000: Point to EPHY Register which offset is 3 0001: Point to EPHY Register which offset is 7 0010: Point to EPHY Register which offset is 11 0011: Point to EPHY Register which offset is 15 0100: Point to EPHY Register which offset is 19 0101: Point to EPHY Register which offset is 23 0110: Point to EPHY Register which offset is 27 0111: Point to EPHY Register which offset is 31 1000: Point to EPHY Register which offset is 35 1001: Point to EPHY Register which offset is 39 1010: Point to EPHY Register which offset is 43 1011: Point to EPHY Register which offset is 47 1100: Point to EPHY Register which offset is 51 1101: Point to EPHY Register which offset is 55 1110: Point to EPHY Register which offset is 59 1111: Point to EPHY Register which offset is 63
3:0	RW	0000b	**EPHY Control Register Address Pointer 2** 0000: Point to EPHY Register which offset is 2 0001: Point to EPHY Register which offset is 6 0010: Point to EPHY Register which offset is 10 0011: Point to EPHY Register which offset is 14 0100: Point to EPHY Register which offset is 18 0101: Point to EPHY Register which offset is 22 0110: Point to EPHY Register which offset is 26 0111: Point to EPHY Register which offset is 30 1000: Point to EPHY Register which offset is 34 1001: Point to EPHY Register which offset is 38 1010: Point to EPHY Register which offset is 42 1011: Point to EPHY Register which offset is 46 1100: Point to EPHY Register which offset is 50 1101: Point to EPHY Register which offset is 54 1110: Point to EPHY Register which offset is 58 1111: Point to EPHY Register which offset is 62

Offset Address: 6Ah (D15F0)

SATA PHY Miscellaneous Control Registers **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	10b	**Set Equalizer Duration – Port0** 00: 0.05us 01: 25.6us 10: 30us (default for Host) 11:50us (default for Device)
3	RW	0	**Select the Pattern Sent in OOB– Port0** 0: ALIGN 1: D24.3
2:0	RW	0	**Reserved**

Offset Address: 6Bh (D15F0) – Reserved

Offset Address: 6Ch (D15F0)

SATA PHY Miscellaneous Control Registers **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	10b	**Set Equalizer Duration – Port1** 00: 0.05us 01: 25.6us 10: 30us (default for Host) 11:50us (default for Device)
3	RW	0	**Select the Pattern Sent in OOB– Port1** 0: ALIGN 1: D24.3
2:0	RW	0	**Reserved**

Offset Address: 6D-77h (D15F0) – Reserved

Miscellaneous Registers (78-7Fh)

Offset Address: 78h (D15F0)

SATA (Primary Channel) Transport Layer Status 1 **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**DMA Read Device Cycle Active** 0: DMA Read Device cycle inactive 1: DMA Read Device cycle active
3	RO	0	**DMA Write Device Cycle Active** 0: DMA Write Device cycle inactive 1: DMA Write Device cycle active
2	RO	0	**SG (Scatter/Gather) Operation Active** 0: Inactive 1: Active The SG operation moves data between the system memory and the data buffer (FIFO). The source/target memory addresses and the data length are specified in PRD (Physical Region Descriptor). Note: PRD is defined in the specification: Bus Master Programming Interface for IDE ATA Controllers.
1	RO	0	**Interrupt Status** 0: No interrupt 1: Interrupt is active
0	RO	1b	**FIFO Empty Status** This is the 64DW FIFO in Transport Layer, which serves as the data buffer between device and system memory. 0: Not empty 1: Empty

Offset Address: 79h (D15F0)

SATA (Primary Channel) Transport Layer Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Primary Channel Port Multiple Port (PMP) Error Status** 0: No error 1: PMP error
6:5	RO	0	**Reserved**
4	RO	0	**The Port where the SATA controller is currently parking on** 0: Port 0 1: Port 1
3	RO	0	**PIO Data Write Cycle, Actively Transmitting Data to the Device** 0: Inactively transmitting 1: Actively transmitting
2	RO	0	**PIO Data Read Cycle, Actively Receiving Data from the Device** 0: Inactively receiving 1: Actively receiving
1	RO	0	**DMA Data Write Cycle, Actively Transmitting Data to the Device** 0: Inactively transmitting 1: Actively transmitting
0	RO	0	**DMA Data Read Cycle, Actively Receiving Data from the Device** 0: Inactively receiving 1: Actively receiving

Offset Address: 7A-7Ch (D15F0) - Reserved

Offset Address: 7Dh (D15F0)

SATA PHY Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**PHY Port 1 Receiving COMINIT** (See the note below) 0: Not received 1: Received
2	RO	0	**PHY Port 1 Receiving COMWAKE** (See the note below) 0: Not received 1: Received
1	RO	0	**PHY Port 0 Receiving COMINIT** (See the note below) 0: Not received 1: Received
0	RO	0	**PHY Port 0 Receiving COMWAKE** (See the note below) 0: Not received 1: Received

Note: The status will show "1" from the 1st burst and the 1st space being detected till the end of the COMINIT/COMWAKE burst.

Offset Address: 7E-7Fh (D15F0) - Reserved

SATA Transport Control Registers (80-9Fh)

Offset Address: 80h (D15F0)

SATA PHY Power Management Mode – Entered by Software Request **Default Value: 00h**

These are part of the SControl bits defined in SATA Specification. For the rest of the SControl bits, please reference to RxA4/RxA5

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	***For SPM Field (=0010b):*** **Initiate PHY Port 1 Transition to the Slumber Power Management State** Writing a 1 to this bit will be converted to writing with 0010b to the SPM field of the SControl Register, and as defined in the specification this action shall activate a transition to the Slumber mode. 0: Disable 1: Enable
2	RW	0	**SPM Field (=0001b):** **Initiate PHY Port 1 Transition to the Partial Power Management State** Writing a 1 to this bit will be converted to writing with 0001b to the SPM field of the SControl Register, and as defined in the specification this action shall activate a transition to the Partial mode. Write a 1 to this bit shall activate the transition 0: Disable 1: Enable
1	RW	0	**SPM Field (=0010b):** **Initiate PHY Port 0 Transition to the Slumber Power Management State** Writing a 1 to this bit will be converted to writing with 0010b to the SPM field of the SControl Register, and as defined in the specification this action shall activate a transition to the Slumber mode. Write a 1 to this bit shall activate the transition. 0: Disable 1: Enable
0	RW	0	**SPM Field (=0001b):** **Initiate PHY Port 0 Transition to the Partial Power Management State** Writing a 1 to this bit will be converted to writing with 0001b to the SPM field of the SControl Register, and as defined in the specification this action shall activate a transition to the Partial mode. Write a 1 to this bit shall activate the transition 0: Disable 1: Enable

Note: The transition is activated when the bit is changed from 0 to 1.

Offset Address: 81h (D15F0)

SATA PHY Power Management Mode – Entered by Hardware (Through Timeout) Request **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Set Inactive Port to Partial/Slumber Mode** Since there is only one Transport Layer to serve the two ports, only one port can be active at a time. With this feature enabled, every time the TP switches port the inactive port will immediately (without having to wait till timer (Rx81[2:0]) expires) be put to either Partial or Slumber mode depending on which mode is selected in bit 6. 0: Disable 1: Enable
6	RW	0	**Power Saving Mode Selection for The Inactive Port— Port0** 0: Partial mode 1: Slumber mode
5	RW	0	**Power Saving Mode Selection for The Inactive Port— Port1**
4:3	RW	00b	**Settings for Hardware Timer Activated Partial/Slumber Mode – Port0** ***Rx81[4:3]*** ***Partial*** ***Slumber*** **00** **Enable** **Enable** **01** **Enable** Disable **10** Disable **Enable** **11** Disable Disable 00: When the timer (Rx81[2:0]) for Partial mode expires, PHY will be requested to enter Partial mode. When the same timer for Slumber mode also expires, PHY will be requested to exit Partial mode first and then immediately enter Slumber mode. 01: PHY will be requested to enter Partial mode when the timer for Partial mode expires. Slumber mode is not enabled. 10: PHY will be requested to enter Slumber mode when the timer for Slumber mode expires. Partial mode is not enabled. 11: Both Partial and Slumber modes are disabled.
2:0	RW	000b	**Settings for Power Management Timer (in unit of t = 0.425s) — Port0** 000: T = 1 t or 0.425s 001: T = 2 t or 0.850s 010: T = 3t or 3*0.425s … ***Power Mode Control Process:*** 1. Partial mode will be requested if the Transport Layer has been idle for 2T. For example: If the setting is 001b, T=2t=0.0850s. So, entering Partial mode will be requested after TP has been idle for 0.0850 seconds. 2. Slumber mode will be requested if the Transport Layer has been idle for 10T.

Offset Address: 82h (D15F0)

Transport Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Transport Layer to Issue Early Request to Link Layer** When enabled, the Transport Layer can issue command one 37.5/75 Mhz (Gen1/Gen2) clock earlier to the Link Layer for 1T performance enhancement. 0: Disable 1: Enable
5	RW	0	**Reserved**
4	RW	0	**Data Size Limit for a Single Data FIS** An option provided for devices capable of doing so. 0: Maximum of 8K bytes as it is defined in Spec 1: Allow over 8K bytes
3	RW	0	**Reserved**
2	RW	0	**FIFO Flow Control, Set Water Mark for FIFO Read** 0: When 52DW has been filled 1: When 40DW has been filled This 64DW FIFO is a data buffer between device and system memory. For DMAR, the data are burst from the device to the FIFO first before they are sent (read) to the system memory. For DMAW, the data are read from the system memory to this FIFO before they are burst (read) to the device. This water mark determines when the data in the FIFO can start to be taken out (read).
1:0	RW	0	**Reserved (Do Not Program)**

Offset Address: 83-87h (D15F0) - Reserved

Offset Address: 88h (D15F0)

PHY Wakeup Request Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Assert Wakeup (from Partial/Slumber) Request to Port 1 PHY** This Wakeup Request is mainly for testing / debugging. 0: Disable 1: Enable
0	RW	0	**Assert Wakeup (from Partial/Slumber) Request to Port 0 PHY** This Wakeup Request is mainly for testing / debugging. 0: Disable 1: Enable

Note: The Wakeup request is activated when the request bit is changed from 0 to 1.

Offset Address: 89h (D15F0)

PATA/SATA Miscellaneous Controls **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved**
6	RW	0	**Hold Command Until First D2H FIS Is Received** 0: Disable 1: Enable
5	RO	1b	**Reserved**
4	RW	0	**Allow The 1st PRD (Right After PCIRESET) to Be Only 2-Byte Long** 0: Disable 1: Enable
3	RW	0	**Allow The 1st PRD (Right After PCIRESET) to Be Only 2-Byte Long** 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 8A-8Bh (D15F0) – Reserved

Offset Address: 8Ch (D15F0)

SATA PHY Power Management Mode 2– Entered by Hardware (Through Timeout) Request **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Reset Drive Select to Master When Change Device Control Register Bit[2] (SRST)** 0: Disable 1: Enable
4:3	RW	00b	**Settings for Hardware Timer Activated Partial/Slumber Mode – Port1** ***Rx81[4:3]*** ***Partial*** ***Slumber*** **00** **Enable** **Enable** **01** **Enable** Disable **10** Disable **Enable** **11** Disable Disable 00: When the timer (Rx81[2:0]) for Partial mode expires, PHY will be requested to enter Partial mode. When the same timer for Slumber mode also expires, PHY will be requested to exit Partial mode first and then immediately enter Slumber mode. 01: PHY will be requested to enter Partial mode when the timer for Partial mode expires. Slumber mode is not enabled. 10: PHY will be requested to enter Slumber mode when the timer for Slumber mode expires. Partial mode is not enabled. 11: Both Partial and Slumber modes are disabled.
2:0	RW	000b	**Settings for Power Management Timer (in unit of t = 0.425s) – Port1** 000: T = 1 t or 0.425s 001: T = 2 t or 0.850s 010: T = 3t or 3*0.425s … ***Power Mode Control Process:*** 1. Partial mode will be requested if the Transport Layer has been idle for 2T. For example: If the setting is 001b, T=2t=0.0850s. So, entering Partial mode will be requested after TP has been idle for 0.0850 seconds. 2. Slumber mode will be requested if the Transport Layer has been idle for 10T.

Offset Address: 8D-9Fh (D15F0) - Reserved

SATA SCR (Status and Control) Registers (A0-AFh)

Offset Address: A0h (D15F0)

SATA Port 0 Status (SStatus in SATA Specification) **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**The Negotiated Interface Communication Speed Established (SPD Field)** 0: SATA in Gen1 speed 1: SATA in Gen 2 (3Gb) speed
3	RO	0	**Slumber Mode Power Management Status (IPM Field)** 0: Not in Slumber mode 1: Device and the Host are currently in Slumber mode
2	RO	0	**Partial Mode Power Management Status (IPM Field)** 0: Not in Slumber mode 1: Device and the Host are currently in Slumber mode
1	RO	0	**PHY Communication Established (DET Field)** 0: PHY not ready 1: PHY ready
0	RO	0	**Device Detected (DET Field)** 0: Not present 1: Present

Offset Address: A1h (D15F0)

SATA Port 1 Status (SStatus in SATA Specification) **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**The Negotiated Interface Communication Speed Established (SPD Field)** 0: SATA in Gen1 speed 1: SATA in Gen 2 (3Gb) speed
3	RO	0	**Slumber Mode Power Management Status (IPM Field)** 0: Not in Slumber mode 1: Device and the Host are currently in Slumber mode
2	RO	0	**IPM Field: Partial Mode Power Management Status** 0: Not in Slumber mode 1: Device and the Host are currently in Slumber mode
1	RO	0	**PHY Communication Established (DET Field)** 0: PHY not ready 1: PHY ready
0	RO	0	**Device Detected (DET Field)** 0: Not present 1: Present

Offset Address: A2-A3h (D15F0) - Reserved

Offset Address: A4h (D15F0)

SATA Port 0 Control (SControl in SATA Specification) **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	1b	***For IPM Field = 0010b:*** **Capability of Transition to The Slumber Power Management State** Writing a 1 to this bit will be converted to setting the IPM field of the SControl register with 0010b, which is to make "Transitions to the Slumber power management state disabled". 0: Enable 1: Disable
2	RW	1b	***For IPM Field = 0001b:*** **Capability of Transition to the Partial Power Management State** Writing a 1 to this bit will be converted to setting the IPM field of the SControl register with 0001b, which is to make "Transitions to the Partial power management state disabled". 0: Enable 1: Disable
1	RW	0	***For DET Field = 0100b:*** **Disable The SATA Interface and Put PHY In Offline Mode** Writing a 1 to this bit will be converted to setting the DET field of the SControl register with 0100b, which is to "Disable The SATA Interface and Put PHY In Offline Mode". 0: Enable 1: Disable
0	RW	0	***For DET Field = 0001b:*** **Perform SATA Interface Initialization Sequence to Establish Communication** Writing a 1 followed by writing a 0 shall cause a hardware reset (issue COMRESET) and result in the interface being re-initialized and communication being re-established. To further clarify the function of this bit, the followings is the description excerpted from the SATA Specification: "Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. Upon a write to the SControl register that sets the DET field to 0001b, the host interface shall transition to the HP1: HR_Reset state and shall **remain** in that state **until** the DET field is set to a value other than 0001b by a subsequent write to the SControl register". 0: De-Activate 1: Activate

Note: For the SPM Field in the SControl, please refer to Rx80[3:0].

Offset Address: A5h (D15F0)

SATA Port 1 Control (SControl in SATA Specification) **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	1b	***For IPM Field = 0010b:*** **Capability of Transition to The Slumber Power Management State** Writing a 1 to this bit will be converted to setting the IPM field of the SControl register with 0010b, which is to make "Transitions to the Slumber power management state disabled". 0: Enable 1: Disable
2	RW	1b	***For IPM Field = 0001b:*** **Capability of Transition to the Partial Power Management State** Writing a 1 to this bit will be converted to setting the IPM field of the SControl register with 0001b, which is to make "Transitions to the Partial power management state disabled". 0: Enable 1: Disable
1	RW	0	***For DET Field = 0100b:*** **Disable The SATA Interface and Put PHY In Offline Mode** Writing a 1 to this bit will be converted to setting the DET field of the SControl register with 0100b, which is to "Disable The SATA Interface and Put PHY In Offline Mode". 0: Enable 1: Disable
0	RW	0	***For DET Field = 0001b:*** **Perform SATA Interface Initialization Sequence to Establish Communication** 0: De-activate 1: Activate Writing a 1 followed by writing a 0 shall cause a hardware reset and result in interface being re-initialized and communication being re-established. To further clarify the function of this bit, the followings is the description excerpted from the SATA Specification: "Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. Upon a write to the SControl register that sets the DET field to 0001b, the host interface shall transition to the HP1: HR_Reset state and shall remain in that state until the DET field is set to a value other than 0001b by a subsequent write to the SControl register".

Note: For the SPM Field in the SControl, please refer to Rx80[3:0].

Offset Address: A6-A7h (D15F0) - Reserved

Offset Address: AB-A8h (D15F0)

SATA Port 0 SError Register Defined in SATA Specification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RW1C	0	**Reserved**
27	X	0	**Diag Field A bit: Port Selector Presence Detected** 0: Not detected 1: Detected
26	RW1C	0	**Diag Field X bit: Exchanged as determined by reception of COMINIT** 0: Exchanged not occurred 1: Exchange occurred
25	RW1C	0	**Diag Field F bit: Unrecognized FIS Type** 0: No unrecognized FIS 1: Unrecognized FIS type detected
24	RW1C	0	**Diag Field T bit: Transport State Transition Error** 0: No error 1: Error occurred
23	RW1C	0	**Diag Field S bit: Link Sequence Error** 0: No error 1: Error occurred
22	RW1C	0	**Diag Field H bit: Handshake Error** 0: No error 1: Error occurred
21	RW1C	0	**Diag Field C bit: CRC Error** 0: No error 1: Error occurred
20	RW1C	0	**Diag Field D bit: Disparity Error** 0: No error 1: Error occurred
19	RW1C	0	**Diag Field B bit: 10B to 8B Decode Error** 0: No error 1: Error occurred
18	RW1C	0	**Diag Field W bit: COMWAKE Detected** 0: Not detected 1: Detected
17	RW1C	0	**Diag Field I bit: PHY Internal Error** When no device exists, this bit is RO, and default value will be 1 after Reset inactive. 0: No error 1: Error occurred
16	RW1C	0	**Diag Field N bit: PhyRdy Change** 0: No change 1: Changed
15:12	RW1C	0	**Reserved**
11	RW1C	0	**Err Field E bit: Internal Error** 0: No error 1: Error occurred
10	RW1C	0	**Err Field P bit: Protocol Error** 0: No error 1: Error occurred
9	RW1C	0	**Err Field C bit: Non-recovered Persistent Communication or Data Integrity Error** 0: No error 1: Error occurred
8	RW1C	0	**Err Field T bit: Non-recovered Transient Data Integrity Error** 0: No error 1: Error occurred
7:2	RW1C	0	**Reserved**
1	RW1C	0	**Err Field M bit: Recovered Communications Error** 0: No error 1: Error occurred
0	RW1C	0	**Err Field I bit: Recovered Data Integrity Error** 0: No error 1: Error occurred

Offset Address: AF-ACh (D15F0)

SATA Port 1 SError Register Defined in SATA Specification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW1C	0	**Refer to RxAB-A8 for the register bit definition.**

Legacy / Back Door Registers (B0-FFh)

Offset Address: B1-B0h (D15F0)

Power Management Capability ID **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Fixed at 0**
7:0	RO	01h	**Capability ID** PCI power management capability ID.

Offset Address: B3-B2h (D15F0)

Power Management Interface Revision **Default Value: 0002h**

Bit	Attribute	Default	Description
15:3	RO	0	**Fixed at 0**
2:0	RO	010b	**Power Management Interface Revision** Indicates that this function complies with Revision 1.1 of PCI Power Management Interface Spec.

Offset Address: B5-B4h (D15F0)

Power Management Capability Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Fixed at 0**
1:0	RW	00b	**Power Management Capability Status** 00: D0 11: D3 Hot Others: Reserved

Offset Address: B6-B8h (D15F0) - Reserved

Offset Address: B9h (D15F0)

Interrupt Back Door **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Reset SATA Controller and Power Down PHYs of Both Port 0 and Port 1** By setting the bit to "1", the followings will happen: 1. Reset SATA controller 2. Clock to PHY is gated out 3. Signals output to adjacent blocks are forced to inactive states 4. Power down PHY blocks of both ports Note: When set to 1, SATA controller's registers and IO ports can still be accessed by the CPU cycles if D17F0 Rx50[3] is set at 1. To completely block downstream cycles to SATA controller, set D17F0 Rx 50[3] to 0.
6	RW	0	**Gating SATA EPHY's Input to 0 and Its Output to Inactive** When SATA EPHY Port0 or Port1's power is removed, this bit should be set to 1. Otherwise, it should be set to 0. 0: Does not gate 1: Gate Description / RxB9[6] / RxA4[1] / RxA5[1] **When remove SATA EPHY port 0's power, SATA controller s configuration** / 1 / 1 / 0 **When remove SATA EPHY port 1's power, SATA controller s configuration** / **1** / **0** / **1**
5	RW	0	**OOB Kick-off Control for Port 1** Since the hardware default is 0, at power up the OOB sequence is held up until the bit is altered to 1 by the software (BIOS). 0: Inhibit OOB sequence 1: Start OOB sequence
4	RW	0	**OOB Kick-off Control for Port 0** Since the hardware default is 0, at power up the OOB sequence is held up until the bit is altered to 1 by the software (BIOS). 0: Inhibit OOB sequence 1: Start OOB sequence
3	RW	0	**Reserved**
2:0	RW	001b	**Reserved**

Offset Address: BA-BBh (D15F0) - Reserved

Offset Address: BD-BCh (D15F0)

Subsystem Vendor ID Back Door **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	**Subsystem Vendor ID (Rx2C-2D) Back Door**

Offset Address: BF-BEh (D15F0)

Subsystem ID Back Door **Default Value: 9001h**

Bit	Attribute	Default	Description
15:0	RW	9001h	**Subsystem ID (Rx2E-2F) Back Door**

Offset Address: C0-FFh (D15F0) - Reserved

SATA EPHY Index Register (SATA-EPHYC)

SATA EPHY Control Registers (00-3Fh)

The registers within this section are accessed through index registers, the configuration methods of EPHY registers are listed below.

Step 1: Indicate the offset of EPHY register by do configuration write to Rx68-69. The 16bit data can indicate four registers. Please refer to the content of Rx68-69.
Step 2: Do configuration read/write to Rx64-67. The 4 bytes data will be read/written from/into the four registers indicated in step 1.
Example 1: Read Rx00-03.
Step 1: Configure write 16'h00 to Rx68-69.
Step 2: Configure read from Rx64-67.
The read back data [31:24] is for Rx03,
The read back data[23:16] is for Rx02,
The read back data[15:8] is for Rx01;
The read back data[7:0] is for Rx00.
Example 2: Write Rx00, Rx05, Rx0A, Rx0F.
Step 1: Configure write 16'h0123 to Rx68-69
Step 2: Configure write data to Rx64-67,
The write data [31:24] is for offset Rx0F;
The write data[23:16] is for Rx0A;
The write data[15:8] is for Rx05;
The write data[7:0] is for Rx00.

Offset Address: 00h (SATA-EPHYC)

SATA Miscellaneous Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved**
6	RW	0	**Force to Turn on All Functions in Master Block when EPHY Testing** 0: Disable 1: Enable
5:3	RW	0	**Reserved**
2	RW	0	**Reserved**
1:0	RW	00b	**Set VCO in Free Running Mode** 00: PLL locking mode 01: 1.25V 10: 1.50V 11: 1.75V

Offset Address: 01h (SATA-EPHYC)

SATA EPHY RTN Control Register 0 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**TX Resistance Set Enable** 0: Disable 1: Enable
6:3	RW	1000b	**TX Resistance Set Value** 0000: 73.5 0001: 69.4 0010: 65.8 0011: 62.5 0100: 59.5 0101: 56.8 0110: 54.3 0111: 52.1 1000: 50.0 1001: 48.1 1010: 46.3 1011: 44.6 1100: 43.1 1101: 41.7 1110: 40.3 1111: 39.1
2:0	RO	0	**Reserved**

Offset Address: 02h (SATA-EPHYC)
SATA EPHY RTN Control Register 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**RX Resistance Set Enable** 0: Disable 1: Enable
6:3	RW	1000b	**RX Resistance Set Value** Description same as Rx01[6:3]
2:1	RW	00b	**BIST Control** 00: BIST disable (default) 01: BIST down 10: BIST up 11: BIST free running
0	RW	0	**Reserved**

Offset Address: 03-05h (SATA-EPHYC) - Reserved

Offset Address: 06h (SATA-EPHYC)
SATA EPHY Bias Current Set Register **Default Value: F5h**

Bit	Attribute	Default	Description
7:3	RW	11110b	**Reserved**
2:0	RW	101b	**Bias Current Set** Default TX Diff. Swing = 500mV 000: 2.5mA 001: 3mA 010: 3.5mA 011: 4mA 100: 4.5mA 101: 5mA 110: 5.5mA 111: 6mA

Offset Address: 07-08h (SATA-EPHYC) - Reserved

Offset Address: 09h (SATA-EPHYC)
SATA EPHY SQ and LEQ Control **Default Value: 22h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:5	RW	01b	**SQ Detection Threshold Select** 00:100mV 10:140mV 01:120mV 11:160mV
4:1	RW	0001b	**LEQ Offset Tuning Bandwidth Set** 0000 (1/2) ~ 1111 (1/32)
0	RO	0	**Reserved**

Offset Address: 0Ah (SATA-EPHYC)

SATA EPHY IV Gain and Equalizer Tuning Mode Control **Default Value: A0h**

Bit	Attribute	Default	Description
7:5	RW	101b	**IV Gain Select** 000: 50uA / 25uA 001: 62.5uA / 25uA 010: 50uA / 31.25uA 011: 62.5uA / 31.25uA 100: 50uA / 25uA 101: 75uA / 25uA 110: 50uA / 37.5Ua 111: 75uA / 37.5uA (Proportional Current / Integration Current)
4	RW	0	**Reserved**
3:0	RW	0000b	**Equalizer Tuning Mode Select *(EQTNMODE[3])*** ***EQTNMODE[3]:*** 0: (dc/hf/os/w1/w2)sum resets whenever [(dc/hf/os/w1/w2)CNT is high] and [(dc/hf/os/w1/w2)POS or (dc/hf/os/w1/w2)NEG is high]. (default) 1: (dc/hf/os/w1/w2)sum resets whenever (dc/hf/os/w1/w2)CNT is high ***EQTNMODE[2]: Max W2 Setting*** 0: 12 1: 16 ***EQTNMODE[1:0]: OS Start After Weight Tuning*** 00 : 32 times 01 : 24 times 10 : 16 times 11 : 40 times

Offset Address: 0Bh (SATA-EPHYC)

SATA EPHY LEQ Control **Default Value: 10h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**LEQ DC Gain Tuning Bandwidth Set** 0000 (1) ~ 1111 (1/16)
3:0	RW	0000b	**LEQ HF Gain Tuning Bandwidth Set** 0000 (1/2) ~ 1111 (1/32)

Offset Address: 0Ch (SATA-EPHYC)

SATA EPHY RXCLK and DFE Control **Default Value: 02h**

Bit	Attribute	Default	Description
7:5	RW	000b	**RXCLK Phase Select** 0xx: no offset 100: + 0.2 period 101: + 0.6 period 110: + 0.4 period 111: + 0.8 period
4:1	RW	0001b	**DFE Weight Tuning Bandwidth Set** 0000 (1/2) ~ 1111 (1/32)
0	RO	0	**Reserved**

Offset Address: 0Dh (SATA-EPHYC)
SATA EPHY EQTN Control **Default Value: 89h**

Bit	Attribute	Default	Description
7:6	RW	10b	**DFE Tap Selection** 00: 0 tap (DFE off) 01: 1(G2) / 0(G1) tap 10: 2(G2) / 1(G1) tap 11: Reserved!
5	RW	0	**Equalizer Always Tuning Mode Enable**
4	RW	0	**Enable Low Speed Mode After First Tuning Finished** Under FHSm_EQTNALWY=1 for power saving
3	RW	1b	**Enable DFE in Training Mode** 0: Disable 1: Enable
2	RW	0	**Reserved**
1:0	RW	01b	**Equalizer Tuning Threshold** 00: 300 01: 350 10: 400 11: 450

Offset Address: 0Eh (SATA-EPHYC)
SATA EPHY LEQ DC Gain Control **Default Value: 7Ch**

Bit	Attribute	Default	Description
7	RW	0	**LEQ DC Gain Manual Set Enable**
6:2	RW	11111b	**LEQ DC Gain Initial or Set Value** Min gain ~ max gain.
1:0	RO	0	**Reserved**

Offset Address: 0Fh (SATA-EPHYC)
SATA EPHY LEQ HF Gain Control **Default Value: 7Eh**

Bit	Attribute	Default	Description
7	RW	0	**LEQ HF Gain Manual Set Enable**
6:2	RW	11111b	**LEQ HF Gain Initial or Set Value** Min boost ~ max boost
1	RW	1b	**Reserved**
0	RO	0	**Reserved**

Offset Address: 10h (SATA-EPHYC)
SATA EPHY LEQ Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LEQ Offset Manual Set Enable**
6	RW	0	**Reserved**
5:2	RW	0000b	**LEQ Offset Initial or Set Value** 1111(-7 units)~0111(+7unit) sign magnitude
1:0	RO	0	**Reserved**

Offset Address: 11h (SATA-EPHYC)

SATA EPHY DFE Weight1 Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DFE Weight1 Manual Set Enable**
6	RW	0	**Reserved**
5:2	RW	0000b	**DFE Weight1 Initial or Set Value** 0000 (1 unit) ~ 1111 (16 units)
1:0	RO	0	**Reserved**

Offset Address: 12h (SATA-EPHYC)

SATA EPHY DFE Weight2 Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DFE Weight2 Manual Set Enable**
6	RW	0	**Reserved**
5:2	RW	0000b	**DFE Weight2 Initial or Set Value** 0000 (1 unit) ~ 1111 (16 units)
1:0	RO	0	**Reserved**

Offset Address: 13h (SATA-EPHYC)

SATA EPHY Tuning Function BIST Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Tuning Function BIST Enable**
6:4	RW	000b	**Tuning Function BIST: Event Selection**
3	RW	0	**Reserved**
2:0	RO	0	**Reserved**

Offset Address: 14h (SATA-EPHYC)

SATA EPHY FD Mode Ratio and PD Training Mode Ratio Control **Default Value: 40h**

Bit	Attribute	Default	Description
7:5	RW	010b	**FD Mode Ratio During P1 to P0** 000: 4/16 100: 8/16 001: 5/16 101: 9/16 010: 6/16 110: 10/16 011: 7/16 111: 11/16
4:2	RW	000b	**PD Training Mode Ratio During Partial to Normal** 000: 5/16 100: 9/16 001: 6/16 101: 10/16 010: 7/16 110: 11/16 011: 8/16 111: 12/16
1:0	RW	0	**Reserved**

Offset Address: 15h (SATA-EPHYC)
SATA EPHY P2/P1 Exit Latency Set **Default Value: 30h**

Bit	Attribute	Default	Description
7:5	RW	001b	**P2 Exit Latency** 000: 1.67us 100: Reserved 001: 3.33u 101: Reserved 010: 6.67us 110: Reserved 011: 13.33us 111: Reserved
4:2	RW	100b	**P1 Exit Latency** 000: 427ns 100: 1.706us 001: 427ns 101: 3.413us 010: 427ns 110: 6.827us 011: 853ns 111: Reserved
1:0	RW	0	**Reserved**

Offset Address: 16h (SATA-EPHYC)
SATA EPHY Gain1 and Gain2 Mode Set **Default Value: D4h**

Bit	Attribute	Default	Description
7:6	RW	11b	**Gain1 During Training Mode** 00: x1 10: x4 01: x2 11: x8
5:4	RW	01b	**Gain1Dduring Tracking Mode** 00: x1 10: x4 01: x2 11: x8
3:2	RW	01b	**Gain2 During Training Mode** 00: x1 10: x4 01: x2 11: x8
1:0	RW	00b	**Gain2Dduring Tracking Mode** 00: x1 10: x4 01: x2 11: x8

Offset Address: 17h (SATA-EPHYC)
SATA EPHY LF Select **Default Value: 8Ch**

Bit	Attribute	Default	Description
7:6	RW	10b	**LF Select During Tracking Mode** 00: x4 10: x12 01: x8 11: x16
5:3	RW	001b	**Reserved**
2:0	RW	100b	**Reserved**

Offset Address: 18h (SATA-EPHYC) - Reserved

Offset Address: 19h (SATA-EPHYC)
SATA EPHY Update Time and LF Select Control **Default Value: 26h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	1b	**Update Time During Training Mode** 0: x1 1: x2
4	RW	0	**Update Time During Tracking Mode** 0: x1 1: x2
3:2	RW	01b	**LF Select During Training Mode** 00: x4 10: x12 01: x8 11: x16
1:0	RW	10b	**LF Select During Tracking Mode** 00: x4 10: x12 01: x8 11: x16

Offset Address: 1A-20h (SATA-EPHYC) - Reserved

Offset Address: 21h (SATA-EPHYC)

SATA EPHY Port 0 TX Power and TX Electrical Idle Set **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**TX Power Status Set Enable**
6:5	RW	10b	**Partial / Slumber Mode** Both are active high, default slumber mode, same as RX 00:Normal 01: Slumber 10: Partial 11: Slumber
4	RW	0	**TX Electrical Idle Set**
3:0	RO	0	**Reserved**

Offset Address: 22-23h (SATA-EPHYC) – Reserved

Offset Address: 24h (SATA-EPHYC)

SATA EPHY Port 0 Generation Set and Internal Loopback Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Port0 RX Power Status Set Enable**
6:5	RW	10b	**Port0 Partial / Slumber Mode** Both are active high, default slumber mode. 00: Normal 01: Slumber 10: Partial 11: Slumber
4	RW	0	**Generation Manual Set Enable**
3	RW	0	**Generation Manual Set**
2	RW	0	**Reserved**
1	RW	0	**Enable Internal Loopback from RCV to DT Driver**
0	RW	0	**Reserved**

Offset Address: 25-30h (SATA-EPHYC) - Reserved

Offset Address: 31h (SATA-EPHYC)

SATA EPHY Port 1 TX Power and TX Electrical Idle Set **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**TX Power Status Set Enable**
6:5	RW	10b	**Partial / Slumber Mode** Both are active high, default slumber mode, same as RX 00:Normal 01: Slumber 10: Partial 11: Slumber
4	RW	0	**TX Electrical Idle Set**
3:0	RO	0	**Reserved**

Offset Address: 32-33h (SATA-EPHYC) - Reserved

Offset Address: 34h (SATA-EPHYC)

SATA EPHY Port 1 Generation Set and Internal Loopback Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Port1 RX Power Status Set Enable**
6:5	RW	10b	**Port1 Partial / Slumber Mode** Both are active high, default slumber mode. 00:Normal 01: Slumber 10: Partial 11: Slumber
4	RW	0	**Generation Manual Set Enable**

3	RW	0	**Generation Manual Set**
2	RW	0	**Reserved**
1	RW	0	**Enable Internal Loopback from RCV to DT Driver**
0	RW	0	**Reserved**

Offset Address: 35-3Fh (SATA-EPHYC) – Reserved

Bus Master IDE I/O Space (IDE-IO)

These registers are compliant with the SFF 8038I v1.0 standard. Refer to the SFF 8038I v1.0 specification for further details. D15F0 Rx23-20h is the base address for these Bus Master IDE I/O Registers.

Bus Master Controller (00-0Fh)

Offset Address: 00h (IDE-IO)

PATA Primary Channel Bus Master IDE Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Primary Channel Bus Master IDE Command

Offset Address: 01h (IDE-IO) - Reserved

Offset Address: 02h (IDE-IO)

PATA Primary Channel Bus Master Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	Primary Channel Bus Master Status

Offset Address: 03h (IDE-IO) - Reserved

Offset Address: 07-04h (IDE-IO)

PATA Primary Channel Bus Master IDE Descriptor Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Primary Channel Bus Master IDE Descriptor Table Pointer

Offset Address: 08h (IDE-IO)

PATA Secondary Channel Bus Master IDE Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Secondary Channel Bus Master IDE Command

Offset Address: 09h (IDE-IO) - Reserved

Offset Address: 0Ah (IDE-IO)

PATA Secondary Channel Bus Master Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	Secondary Channel Bus Master Status

Offset Address: 0Bh (IDE-IO) - Reserved

I/O Offset Address: 0F-0Ch (IDE-IO)

PATA Secondary Channel Bus Master IDE Descriptor Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Secondary Channel Bus Master IDE Descriptor Table Pointer

DEVICE 16 FUNCTION 0-3 (D16F0-F3): USB 1.1 UHCI PORTS 0-7

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 0-3 PCI configuration space of the chip. The USB I/O registers are defined in UHCI specification v1.1. The registers are identical in the Device 16 Functions 0-3 where each function controls different USB ports (function 0 for ports 0-1, function 1 for ports 2-3, function 2 for ports 4-5, and function 3 for port 6-7).

PCI Configuration Space

Header Registers (00-3Fh)

Offset Address: 01-00h (D16F0-F3)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D16F0-F3)

Device ID **Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RO	3038h	**Device ID**

Offset Address: 05-04h (D16F0-F3)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable 1: Disable
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles).
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D16F0-F3)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8:4	RO	01h	**Fixed at 01h (for PCI PMI)**
3	RW1C	0	**Interrupt Status**
2:0	RO	0	**Fixed at 0 (for PCI PMI)**

Offset Address: 08h (D16F0-F3)

Revision ID **Default Value: A0h**

Bit	Attribute	Default	Description
7:0	RO	A0h	**Revision ID**

Offset Address: 0B-09h (D16F0-F3)

Class Code **Default Value: 0C 0300h**

Bit	Attribute	Default	Description
23:0	RO	0C0300h	**Class Code** 0C0300h indicates the USB1.1 Host Controller.

Offset Address: 0Ch (D16F0-F3)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D16F0-F3)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Latency Timer**

Offset Address: 0Eh (D16F0-F3)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h indicates a multi-function device.

Offset Address: 0Fh (D16F0-F3)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 0.

Offset Address: 10-1Fh (D16F0-F3) – Reserved

Offset Address: 23-20h (D16F0-F3)
USB I/O Register Base Address **Default Value: 0000 FCE1h**

Bit	Attribute	Default	Description
31:16	RW	0	**Reserved**
15:5	RW	7E7h	**USB I/O Register Base Address [15:5]** Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5].
4:0	RO	01h	**32-Byte Aligned IO Space**

Offset Address: 24-2Bh (D16F0-F3) – Reserved

Offset Address: 2D-2Ch (D16F0-F3)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D16F0-F3)
Subsystem ID **Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RW1	3038h	**Subsystem ID**

Offset Address: 30-33h (D16F0-F3) – Reserved

Offset Address: 34h (D16F0-F3)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Fixed at 80h.

Offset Address: 35-3Bh (D16F0-F3) – Reserved

Offset Address: 3Ch (D16F0-F3)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**USB Interrupt Routing** 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disabled

Offset Address: 3Dh (D16F0-F3)

Interrupt Pin (D16F0) **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Interrupt Pin (D16F1) **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Interrupt Pin** Fixed at 02h (INTB#).

Interrupt Pin (D16F2) **Default Value: 03h**

Bit	Attribute	Default	Description
7:0	RO	03h	**Interrupt Pin** Fixed at 03h (INTC#).

Interrupt Pin (D16F3) **Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	**Interrupt Pin** Fixed at 04h (INTD#).

Offset Address: 3E-3Fh (D16F0-F3) – Reserved

USB 1.1-Specific Configuration Registers (40-FFh)

Offset Address: 40h (D16F0-F3)

Control Register 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	1b	**Babble Option** This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. 0: Automatically disable babbled port when EOF babble occurs. 1: Do not disable babbled port.
5	RW	0	**Reserved**
4	RW	0	**Frame Interval Select** 0: 1ms frame time 1: 0.1ms frame time
3	RW	0	**USB Data Length Option** 0: Supports Transfer Descriptor length up to 1280 bytes 1: Supports Transfer Descriptor length up to 1023 bytes
2	RW	0	**Improve FIFO Latency** 0: Improve latency if packet size < 64 bytes. 1: Disable improvement.
1	RW	0	**DMA Option** 0: Enhanced performance (8 DW burst access with better FIFO latency) 1: Normal performance (16 DW burst access with normal FIFO latency)
0	RW	0	**Reserved**

Offset Address: 41h (D16F0-F3)

Control Register 2 **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW	0	**USB 1.1 Improvement for EOP** This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. ***Under USB specification 1.1:*** when this occurs in the interval just before an EOP, the receiver will accept the packet. ***Under USB specification 1.0:*** the packet is ignored. 0: USB Spec 1.1 Compliant (packet accepted) 1: USB Spec 1.0 Compliant (packet ignored)
6:5	RW	0	**Reserved**
4	RW	1b	**Reserved (Do Not Program)**
3	RW	0	**Reserved**
2	RW	0	**I/ O Port 60/64 Trap Option** Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits. 0: Set trap 60/64 status bits without checking enable bits. 1: Set trap 60/64 status bits only when trap 60/64 enable bits are set.
1	RW	1b	**A20Gate Pass Through Option** This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. 0: A20GATE Pass-through command sequence as defined in UHCI. 1: Last command (write FFh to port 64) is skipped.
0	RO	0	**Reserved**

Offset Address: 42h (D16F0-F3)

Control Register 3 **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	0	**Enable Subsystem ID / Subsystem Vender ID Back Door** 0: Read Only 1: Read / Write
3	RW	0	**Reserved**
2	RW	0	**Hold Data Transmission till FIFO Reaches Transmission Threshold** 0: Enable 1: Disable
1:0	RW	11b	**Reserved (Do Not Program)**

Offset Address: 43h (D16F0-F3)

Control Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Continue Transmitting Erroneous Data When FIFO Underrun** 0: Enable 1: Disable
2	RW	0	**Issue CRC Error Instead of Stuffing Error on FIFO Underrun** 0: Enable 1: Disable
1:0	RW	0	**Reserved**

Offset Address: 44h-47h (D16F0-F3) - Reserved

Offset Address: 48h (D16F0-F3)

Control Register 5 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6:3	RW	0	**Reserved**
2	RW	0	**Issue Bad CRC5 in SOF After FIFO Underrun** 0: Enable 1: Disable
1	RW	0	**Lengthen PreSOF Time** The preSOF time point determines whether there is enough time in the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened. 0: Disable 1: Enable (PreSOF time lengthened)
0	RW	0	**Issue Non-Zero Bad CRC Code on FIFO Underrun** A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the controller invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent. 0: Non zero CRC (recommended) 1: All zero CRC This option isn't really needed now as non-zero CRC always works.

Offset Address: 49h (D16F0-F3)

Control Register 6 **Default Value: 0Bh**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Bypass 32KHz RTC Clock** Use Internal 1.5MHz Clock for USB 1.1 LS Controller instead. 0: Disable (Use 32KHz RTC clock) 1: Enable (Use 1.5MHz Clock for USB 1.1 LS Controller)
4	RW	0	**Reset USBC Internal 12MHz Clock for UHCI Divider from 48MHz Clock** When this bit transfers from 0 to 1, 12MHz Clock for UHCI divider is reset.
3:2	RW	10b	**Reserved (Do Not Program)**
1	RW	1b	**EHCI Supports PME Assertion in D3 Cold State** 0: Not Supported 1: Supported
0	RW	1b	**UHCI Supports PME Assertion in D3 Cold State** 0: Not Supported 1: Supported

Note: Rx49[2:0] can only be written in function 0. Rx49[2:0] is RO for function 1~3.

Offset Address: 4Ah (D16F0-F3)

Control Register 7 **Default Value: A0h**

Bit	Attribute	Default	Description
7:3	RW	14h	**USB 1.1 Bus Timeout Parameter** ***For FS mode:*** Timeout Parameter cycle of 12MHz is taken as the judgment of USB1.1 Bus timeout. ***For LS mode:*** Timeout Parameter cycle of 1.5MHz is taken as the judgment of USB1.1 Bus timeout.
2	RW	0	**Reserved**
1	RW	0	**Enable Stop Bus Master Cycle If HALT Bit Is Asserted** 0: Disable 1: Enable
0	RW	0	**Use External 60 MHz Clock** Set this bit to use external 60 MHz input clock. 0: Disable 1: Enable

Offset Address: 4Bh (D16F0-F3)

Control Register 8 **Default Value: 8Bh**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6	RW	0	**Enable 66MHz New UHCI Dynamic Scheme** 0: Disable 1: Enable
5	RW	0	**Enable 33MHz New UHCI Dynamic Scheme** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	1b	**Reserved (Do Not Program)**
2	RW	0	**Reserved**
1	RW	1b	**Reserved (Do Not Program)**
0	RW	1b	**Enable Clock Auto Stop** 0: Disable (No Stop) 1: Enable (Auto Stop)

Offset Address: 4Ch (D16F0-F3) – Reserved

Offset Address: 4Dh (D16F0-F3)

Control Register 10 **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	1b	**Bus Master Enable Select** 0: If disable "Bus Master Enable", it will work immediately. 1: If disable "Bus Master Enable", it will work after current transaction.
0	RW	1b	**UHCI FIFO Select** UHCI internal FIFO size selection. 0: 18*36b 1: 24*36b

Offset Address: 4E-5Fh (D16F0-F3) – Reserved

Offset Address: 60h (D16F0-F3)

Serial Bus Release Number **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Serial Bus Release Number** Fixed at 10h.

Offset Address: 61-7Fh (D16F0-F3) – Reserved

Offset Address: 83-80h (D16F0-F3)

Power Management Capability **Default Value: FFC2 0001h**

Bit	Attribute	Default	Description
31:0	RO	FFC2 0001h	**Power Management Capability** If Rx49[0] = 1, this register is fixed at FFC2 0001h. If Rx49[0] = 0, this register is fixed at 7E0A 0001h. Please refer to the "PCI Bus Power Management Interface Specification Revision 1.1 Chapter 3.2" for details.

Offset Address: 85-84h (D16F0-F3)

Power Management Capability Status **Default Value: 00h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME Status** 0: Not active 1: Active
14:9	RO	0	**Reserved**
8	RW	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power Management Capability Status** 00: D0 01: Reserved 10: Reserved 11: D3 Hot

Offset Address: 86-BFh (D16F0-F3) – Reserved

Offset Address: C1-C0h (D16F0-F3)

Legacy Support (for UHCI v1.1 Compliant) **Default Value: 2000h**

Bit	Attribute	Default	Description
15	RW1C	0	**End of A20Gate Pass Through Status (A20PTS)** 1 indicates A20Gate pass through sequence has ended.
14	RO	0	**Reserved** Fixed to 0.
13	RW	1b	**USB PIRQ Enable (USBPIRQDEN)** 0: Disable 1: Enable
12	RO	0	**USB IRQ Status (USBIRQS)** 1 indicates USB IRQ is active.
11	RW1C	0	**Trap By 64h Write Status (TBY64W)** 1 indicates a write to port 64h occurred.
10	RW1C	0	**Trap By 64h Read Status (TBY64R)** 1 indicates a read to port 64h occurred.
9	RW1C	0	**Trap By 60h Write Status (TBY60W)** 1 indicates a write to port 60h occurred.
8	RW1C	0	**Trap By 60h Read Status (TBY60R)** 1 indicates a read to port 60h occurred.
7	RW	0	**SMI At End Of Pass Through Enable (SMIEPTE)** 0: Disable 1: Enable
6	RO	0	**Pass Through Status (PSS)** 1 indicates A20Gate pass through sequence is currently in progress.
5	RW	0	**A20Gate Pass Through Enable (A20PTEN)** 0: Disable 1: Enable
4	RW	0	**Trap/SMI ON IRQ Enable (USBSMIEN)** 0: Disable 1: Enable
3	RW	0	**Trap/SMI On 64h Write Enable (64WEN)** 0: Disable 1: Enable
2	RW	0	**Trap/SMI On 64h Read Enable (64REN)** 0: Disable 1: Enable
1	RW	0	**Trap/SMI On 60h Write Enable (60WEN)** 0: Disable 1: Enable
0	RW	0	**Trap/SMI On 60h Read Enable (60REN)** 0: Disable 1: Enable

Note: This register provides control and status capability for the legacy keyboard and mouse functions. Please refer to UHCI Spec. for further details.

Offset Address: C2-FFh (D16F0-F3) – Reserved

USB 1.1 I/O Space (USB 1.1-IO)

USB 1.1 I/O Registers (00-13h)

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset Address: 01-00h (USB 1.1-IO)

USB Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RW	0	**Max Packet**
6	RW	0	**Configure Flag (CF)**
5	RW	0	**Software Debug (SWDBG)**
4	RW	0	**Force Global Resume (FGR)**
3	RW	0	**Enter Global Suspend Mode (EGSM)**
2	RW	0	**Global Reset (GRESET)**
1	RW	0	**Host Controller Reset (HCRESET)**
0	RW	0	**Run / Stop (RS)**

I/O Offset Address: 03-02h (USB 1.1-IO)

USB Status **Default Value: 0020h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	1b	**Host Controller Halted**
4	RW1C	0	**Host Controller Process Error**
3	RW1C	0	**Host System Error**
2	RW1C	0	**Resume Detect**
1	RW1C	0	**USB Error Interrupt**
0	RW1C	0	**USB Interrupt (USBINT)**

I/O Offset Address: 05-04h (USB 1.1-IO)

USB Interrupt Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3	RW	0	**Short Packet Interrupt Enable**
2	RW	0	**Interrupt On Complete (IOC) Enable**
1	RW	0	**Resume Interrupt Enable**
0	RW	0	**Timeout / CRC Interrupt Enable**

I/O Offset Address: 07-06h (USB 1.1-IO)

Frame Number **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10:0	RW	0	**Frame List Current Index / Frame Number**

I/O Offset Address: 0B-08h (USB 1.1-IO)

Frame List Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Frame List Base Address**
11:0	RO	0	**Reserved**

I/O Offset Address: 0Ch (USB 1.1-IO)

Start of Frame Modify **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RW	40h	**Start of Frame Timing Value**

I/O Offset Address: 0D-0Fh (USB 1.1-IO) – Reserved

I/O Offset Address: 11-10h (USB 1.1-IO)

Port 0 Status / Control **Default Value: 0480h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved.**
12	RW	0	**Suspend**
11:10	RO	01b	**Reserved**
9	RW	0	**Port Reset**
8	RO	0	**Low Speed Device Attached**
7	RO	1b	**Reserved (Do Not Program)**
6	RW	0	**Resume Detect**
5:4	RO	0	**Line Status**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 13-12h (USB 1.1-IO)

Port 1 Status / Control **Default Value: 0480h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Suspend**
11:10	RO	01b	**Reserved**
9	RW	0	**Port Reset**
8	RO	0	**Low Speed Device Attached**
7	RO	1b	**Reserved (Do Not Program)**
6	RW	0	**Resume Detect**
5:4	RO	0	**Line Status**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

DEVICE 16 FUNCTION 4 (D16F4): USB 2.0 EHCI

This Universal Serial Bus host controller interface is fully compatible with EHCI specification v1.0. There are two sets of software accessible registers: PCI configuration registers and USB memory mapped I/O registers. The PCI configuration registers are located in the Device 16 Function 4 PCI configuration space of the chip. The USB memory mapped I/O registers are defined in EHCI specification v1.0.

The EHCI memory mapped I/O base address is located in Rx13-10.

PCI Configuration Space

All registers in D16F4 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 16 and function number 4.

Header Registers (00-3Fh)

Offset Address: 01-00h (D16F4)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D16F4)

Device ID **Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RO	3104h	**Device ID Code**

Offset Address: 05-04h (D16F4)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** Fixed at 0b (Not supported).
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Reserved** Special cycle monitoring. Fixed at 0b (Not supported).
2	RW	0	**Bus Master**
1	RW	0	**Memory Space**
0	RW	0	**I/O Space**

Offset Address: 07-06h (D16F4)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8:4	RO	01h	**Fixed at 01h (for PCI PMI)**
3	RW1C	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D16F4)

Revision ID **Default Value: 90h**

Bit	Attribute	Default	Description
7:0	RO	90h	**Revision ID**

Offset Address: 0B-09h (D16F4)

Class Code **Default Value: 0C 0320h**

Bit	Attribute	Default	Description
23:0	RO	0C0320h	**Class Code for USB2.0 EHCI Host Controller**

Offset Address: 0Ch (D16F4)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D16F4)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Latency Timer**

Offset Address: 0Eh (D16F4)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D16F4)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 00h.

Offset Address: 13-10h (D16F4)
EHCI Memory Mapped I/O Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**EHCI Memory Mapped I/O Registers Base Address** Memory Address for the base of the USB 2.0 EHCI I/O Register block is corresponding to AD[31:8].
7:3	RO	0	**Reserved**
2:1	RO	00b	**Memory Mapping** Reads 00b for 32-bit addressing if Rx40[2] is 0. If Rx40[2] is set, these 2 bits are read as 10b for 64-bit addressing.
0	RO	0	**Reserved**

Offset Address: 17-14h (D16F4)
EHCI Memory Mapped I/O Base Address (High 32-bit) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO/RW	0	**EHCI Memory Mapped I/O Registers High 32-bit Base Address** If Rx40[2] is 0b, this register is RO as 0h. If Rx40[2] is 1b, this register is RW as high 32-bit Memory Base Address for the USB 2.0 EHCI Memory Mapped I/O Register block, corresponding to AD[63:32].

Offset Address: 18-2Bh (D16F4) – Reserved

Offset Address: 2D-2Ch (D16F4)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D16F4)
Subsystem ID **Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RW1	3104h	**Subsystem ID**

Offset Address: 30-33h (D16F4) – Reserved

Offset Address: 34h (D16F4)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Fixed at 80h.

Offset Address: 35-3Bh (D16F4) – Reserved

Offset Address: 3Ch (D16F4)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3:0	RW	0000b	**USB Interrupt Routing** 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disable

Offset Address: 3Dh (D16F4)

Interrupt Pin **Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	**Interrupt Pin** Fixed at 04h (INTD#).

Offset Address: 3E-3Fh (D16F4) – Reserved

USB 2.0-Specific Configuration Registers (40-FFh)

Offset Address: 40h (D16F4)

Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Babble Option** This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled. 0: Automatically disable babbled port when EOF babble occurs 1: Do not disable babbled port
5	RW	0	**Reserved**
4	RW	0	**Micro-Frame Interval Select** 0: 125 us micro-frame time 1: 31.25 us micro-frame time
3	RW	0	**Reserved**
2	RW	0	**DAC Enable** This is a PCI 64-bit DAC cycle enable bit. If this bit is enabled, USB2.0 controller could respond both DAC memory cycle and normal 32-bit PCI cycle. After setting this bit to 1b, Rx14[31:0] could be written as high 32-bit PCI memory base address and Rx10[2:1] is read as 10b. 0: Disable DAC cycle 1: Enable DAC cycle
1	RW	0	**DMA Option** Also used to control FIFO over/under run criteria. 0: 16 DW burst access 1: 8 DW burst access
0	RW	0	**Reserved**

Offset Address: 41h (D16F4)

Test Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Enable Evaluate PERIODIC Enable Bit only At the Beginning of Micro-Frame 0** 0: Evaluate PERIODIC Enable Bit at allover Micro-Frame 0 1: Enable evaluate PERIODIC Enable Bit only at the beginning of Micro_Frame 0
4:1	RW	0	**Reserved**
0	RO	0	**Reserved**

Offset Address: 42h (D16F4)

Control Register 2 **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Enable Check PRESOF for ITD (Isochronous Transfer Descriptor) OUT Transaction During Fetching Data from DRAM** If SB data bandwidth is slow down much more, ITD controller could not fetch enough data to be transmitted at current micro-Frame. So this transaction will cross the SOF, mostly for Multiple ITD transactions. Enable this bit, ITD controller will check PRESOF even at data fetching period. 0: Disable 1: Enable
5:3	RW	0	**Reserved**
2:0	RW	011b	**Reserved (Do Not Program)**

Offset Address: 43-47h (D16F4) – Reserved

Offset Address: 48h (D16F4)

Control Register 4 **Default Value: BEh**

Bit	Attribute	Default	Description
7	RW	1b	**USB 2.0 EOP Pattern (FEh) Error Check** 0: Disable 1: Enable
6	RW	0	**Extra Handshake Error Checking in Isochronous Transaction** 0: Disable 1: Enable
5	RW	1b	**DMA Burst Access** 0: Burst Enable 1: Burst Disable
4	RW	1b	**USB 2.0 Reference Bus Idle Status** When this bit is set to 1, the hardware refers to the bus idle status from PHY to check the start and the end of an incoming packet. 0: Disable 1: Enable
3	RW	1b	**Reserved (Do Not Program)**
2	RW	1b	**Reserved (Do Not Program)**
1	RW	1b	**USB 2.0 CRC16 Check Enable for Toggle Mismatch** 0: Disable 1: Enable
0	RW	0	**HS (High Speed) Port Align to Micro-Frame Boundary** 0: Align 1: Not align

Offset Address: 49h (D16F4)

Control Register 5 **Default Value: 68h**

Bit	Attribute	Default	Description
7	RW	0	**MAC Allows More Delay between Transactions** The delay parameter could be specified in Rx4A. Unit is period of 60MHz clock. 0: Disable 1: Enable
6	RW	1b	**MAC Provides Timeout to Device When Receiver Detects Error** The delay parameter could be specified in Rx51. Unit is period of 33MHz PCI clock. 0: Disable 1: Enable
5	RW	1b	**EHCI Clock Auto Stop** 0: Disable (No stop) 1: Enable (Auto stop)
4	RW	0	**Auto Power Down Receiver Squelch Detector** 0: Auto power down 1: Always power on
3	RW	1b	**Enable New USB C4P State** 0: Disable 1: Enable
2	RW	0	**USB Analog PLL Control When Entering C4P State** 0: Not turn off 48MHz PLL 1: PMU controls whether to turn off the PHY PLL in USBC (USB Controller) or not
1:0	RW	00b	**USB HS NULL-SOF (**Null Start Of Frame) **Valid Time Selection (for C4P Support)** Rx64[2] and these 2 bits are combined to select NULL-SOF valid time {Rx64[2], Rx49[1:0]}: 000: 2 micro frames 001: 4 micro frames 010: Invalid value 011: Invalid value 100: 8 micro frames 101: 16 micro frames 110: 24 micro frames 111: 32 micro frames

Offset Address: 4Ah (D16F4)

MAC Inter-Transaction Delay Parameter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**MAC Inter-Transaction Delay Parameter** Unit is period of 60MHz clock.

Offset Address: 4Bh (D16F4)

MAC Turn Around Time Parameter **Default Value: 09h**

Bit	Attribute	Default	Description
7	RW	0	**SOF (Start of Frame) Disconnects Detection Period** 0: SOF disconnects detection with the narrow window. 1: SOF disconnects detection with the larger window, 2 more periods of 60MHz clock.
6:5	RW	00b	**EHCI Sleep Time Select** 00: 1 us 01: 10 us 10: 10 us 11: 80 us
4	RW	0	**Disable Sending UTM_SOF (Start of Frame of USB Transceiver Macrolcell) When RUN Bit is Cleared** 0: Sending UTM_SOF when RUN bit (USB 2.0-MMIO Rx10[0]) is cleared 1: Do not send UTM_SOF when RUN bit is cleared
3:0	RW	9h	**USB 2.0 MAC Transmit Turn Around Time Parameter** Unit is period of 60MHz clock.

Offset Address: 4Ch (D16F4)

PHY Control 1 **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW	0	**Resume ACK Control** 0: 20ms resume, then send ACK to C4P state resume request 1: Quickly send ACK to C4P state resume request
6	RW	0	**Reserved**
5	RW	0	**USB1.0 UTM (USB Transceiver Macrocell) Tx Speed Up** 0: Disable 1: Enable
4	RW	1b	**USB2.0 EHCI Debug Port Support Enable** 0: Disable 1: Enable
3	RW	0	**USB2.0 Receiver Fast Sync Pattern Detect** 0: Detect sync pattern only after receiving 1010b or 0101b data sequence 1: Always detect sync pattern
2	RW	0	**Enable USB2.0 Receiver Sync Pattern Detect with 'J'_End** 0: Disable 1: Enable
1:0	RW	10b	**Squelch Detector Fine Tune** 125mv squelch level fine tune (USB2.0 PHY control signal) 00: 100mv 01: 112.5mv 10: 125mv 11: 137.5mv

Offset Address: 4Dh (D16F4)

PHY Control 2 **Default Value: 84h**

Bit	Attribute	Default	Description
7	RW	1b	**Reserved (Do Not Program)**
6:3	RW	0	**Reserved**
2:0	RW	100b	**Reserved (Do Not Program)**

Offset Address: 4Eh (D16F4)
USB CP4 Control 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Suspend Time Select** Select suspend time when entering C4P state. As USB2.0 Spec requirement, if USB device has entered into suspend state after USB bus Idle for over 3ms, please configure this register to select different suspend time for different devices condition. 0: 3ms 1: 3.5ms
6:4	RW	0	**Reserved**
3	RW	0	**Long Time Sleep Method Selection to Get the New Asynchronous List** If Rx4B[6:5] = 10b, sleep time is adjusted to 10us. If Rx4B[6:5] = 11b, sleep time is adjusted to 80us. 0: If there is no asynchronous transaction for indicated microFrames, sleep for a long time. The number of idle microFrames is configured from bits [2:1]. 1: If CPU enters C3 state or deeper state, sleep for a long time.
2:1	RW	00b	**Standard of Asynchronous List IDLE** If Idle, sleep for long time to get the new async list. 00: No asynchronous transaction for 4 microFrames 01: No asynchronous transaction for 8 microFrames 10: No asynchronous transaction for 16 microFrames 11: No asynchronous transaction for 31 microFrames Since only 5 bit counter is used for the idle microFrame, the maximized value is 31 microframes.
0	RW	0	**Enable Patch Golden Tree** 0: Disable reset internal EHCI FSM when RUN bit (USB 2.0-MMIO Rx10[0]) is cleared 1: Enable reset internal EHCI FSM when RUN bit is cleared

Offset Address: 4Fh (D16F0-F4)
USB CP4 Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Reset NULLSOF Counter During PortRst Process** 0: Disable 1: Enable
6	RW	0	**Enable Waiting Over 1 microFrame After C4P 20ms Resume time, Before Sending 1st SOF** 0: Disable 1: Enable
5	RW	0	**Select When Recovering RUN Bit After C4P State** 0: Recover RUN bit (USB 2.0-MMIO Rx10[0]) just at the end of resumeK signal, after exiting C4P state 1: Recover RUN bit at 1st SOF sending to USB bus, after exiting C4P state
4	RW	0	**Enable Clear RUN Bit when EHCI_IDLE, if S/W Clears RUN Bit** 0:Enable clear RUN bit (USB 2.0-MMIO Rx10[0]) at any time, if S/W clear this bit 1:Enable clear RUN bit only when EHCI is idle, if S/W clear this bit
3	RW	0	**Reserved**
2	RW	0	**Select Signal to Detect NULLSOF_VALID** 0: Use internal SOF generate signal to detect idle microframes, and generate NULLSOF_VALID for C4P function 1: Detect idle microframes after sending SOF to USB bus, and generate NULLSOF_VALID for C4P function
1	RW	0	**Enable HCHALT Bit in USBSTS S/W Transparent Under C4P State** 0: Disable HCHALT bit in USBSTS S/W transparent 1: Enable HCHALT bit in USBSTS S/W transparent
0	RW	0	**Reserved**

Offset Address: 50h (D16F4)
Test Command **Default Value: 00h**

Bit	Attribut	Default	Description
7	RW	0	**USB 2.0 Doorbell Bit Function Patch** 0: Keep original setting 1: Fetch one more QH before de-asserting Doorbell bit
6:5	RW	0	**Reserved**
4:2	RO	0	**Reserved**
1	RW	0	**Reserved**
0	RO	0	**Reserved**

Offset Address: 51h (D16F4)
USB 2.0 MAC Timeout Parameter **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RW	60h	**USB 2.0 Receiver Timeout Parameter** The unit is byte time.

Offset Address: 52h (D16F4)
Control Register 6 **Default Value: D0h**

Bit	Attribute	Default	Description
7	RW	1b	**C4P State Request Control** 0: USBC (USB controller) feedback to C4P request does not consider RUN bit (USB 2.0-MMIO Rx10[0]) and connect status 1: When RUN bit = 0, or when no device is connected, USBC feedback to C4P request is from PMU instantly.
6	RW	1b	**PLLOK Selection Control** 0: Use logic control PLLOK 1: Use circuit control PLLOK
5	RO	0b	**Reserved**
4	RW	1b	**Reset NULLSOF and NULLSOF Counter When Exiting C4P State** 0: Disable 1: Enable
3	RW	0	**Send Out Interrupt of IOC (Interrupt On Complete) and Roll Over When USB is in C4P State** 0: Disable 1: Enable
2	RW	0	**Enable USB Responding to PMU C4P State Request by Entering / Exiting D3 State** 0: Enable 1: Disable (without entering / exiting D3 state)
1	RW	0	**Enable New PLL Power Down Scheme** When there is no high-speed device connection, power down PLL 0: Disable 1: Enable
0	RW	0	**USB Physical Circuitry Power Down Condition** 0: When the port is disabled or suspended. 1: When the port is disabled or suspended, or when there is no TX (transmit) activity.

Offset Address: 53h (D16F4)
Port Control Register **Default Value: FFh**

Bit	Attribute	Default	Description
7	RW	1b	**PORT8 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT8 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT8 is enabled
6	RW	1b	**PORT7 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT7 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT7 is enabled
5	RW	1b	**PORT6 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT6 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT6 is enabled
4	RW	1b	**PORT5 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT5 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT5 is enabled
3	RW	1b	**PORT4 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT4 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT4 is enabled
2	RW	1b	**PORT3 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT3 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT3 is enabled
1	RW	1b	**PORT2 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT2 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT2 is enabled
0	RW	1b	**PORT1 Resume Enable** 0: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT1 is disabled 1: Remote wakeup and connect/disconnect event of USB1.1 Device in PORT1 is enabled

Offset Address: 54h (D16F4)

PHY Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DPLL Non-Squelch (NSQ) Offset Setting** 00: 0ps 10: 43~135ps 01: -43~-135ps 11: 86~270ps
5	RO	0	**Reserved**
4	RO	0	**DPLL BIST Pattern Matching Flag**
3	RW	0	**Reset DPLL for BIST** 0: Disable 1: Enable
2	RW	0	**DPLL BIST Setting for Different Test Pattern 2** 0: Off 1: 1T phase-shift
1	RW	0	**DPLL BIST Setting for Different Test Pattern 1** 0: Off 1: 1T duty-offset
0	RW	0	**DPLL BIST Setting for Different Test Pattern 0** 0: Off 1: 1T pulse-shift

Offset Address: 55h (D16F4)

PHY Control 4 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**Disconnection Level Fine Tune – For Port 4** 00: 525mv 10:575mv 10: 550mv 11:600mv
5:4	RW	10b	**Disconnection Level Fine Tune – For Port 3** 00: 525mv 10:575mv 10: 550mv 11:600mv
3:2	RW	10b	**Disconnection Level Fine Tune – For Port 2** 00: 525mv 10:575mv 10: 550mv 11:600mv
1:0	RW	10b	**Disconnection Level Fine Tune – For Port 1** 00: 525mv 10:575mv 10: 550mv 11:600mv

Offset Address: 56h (D16F4)

PHY Control 5 **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**Disconnection Level Fine Tune – For Port 8** 00: 525mv 10:575mv 10: 550mv 11:600mv
5:4	RW	10b	**Disconnection Level Fine Tune – For Port 7** 00: 525mv 10:575mv 10: 550mv 11:600mv
3:2	RW	10b	**Disconnection Level Fine Tune – For Port 6** 00: 525mv 10:575mv 10: 550mv 11:600mv
1:0	RW	10b	**Disconnection Level Fine Tune – For Port 5** 00: 525mv 10:575mv 10: 550mv 11:600mv

Offset Address: 57h (D16F4)

PHY Control 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High-Speed Tx Test Mode Register H** 0: Normal 1: Enter EPHY self-test mode
6	RW	0	**High-Speed Tx Test Mode Register G** 0: Normal 1: Enter EPHY self-test mode
5	RW	0	**High-Speed Tx Test Mode Register F** 0: Normal 1: Enter EPHY self-test mode
4	RW	0	**High-Speed Tx Test Mode Register E** 0: Normal 1: Enter EPHY self-test mode
3	RW	0	**High-Speed Tx Test Mode Register D** 0: Normal 1: Enter EPHY self-test mode
2	RW	0	**High-Speed Tx Test Mode Register C** 0: Normal 1: Enter EPHY self-test mode
1	RW	0	**High-Speed Tx Test Mode Register B** 0: Normal 1: Enter EPHY self-test mode
0	RW	0	**High-Speed Tx Test Mode Register A** 0: Normal 1: Enter EPHY self-test mode

Offset Address: 58h (D16F4)

PHY Control 7 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**Async Advance Interrupt Lost Issue Patch** 1: Enable 0: Disable
6	RW	0	**Async Enable Condition Selection** Select whether or not EHCI sleep restart condition controlled by Async enable. 0: Do not go under ASYEN control 1: Under ASYEN control
5:4	RW	0	**Reserved**
3	RW	1	**High-Speed Disconnect During SOF Period Time Select** 0: Short Time (SOF) 1: Long Time (SOF_5T)
2	RW	1b	**Detect High-Speed Disconnect During SOF Period** 0: Disable 1: Enable
1:0	RW	0	**Reserved**

Offset Address: 59h (D16F4)

PHY Control 8 **Default Value: 0Bh**

Bit	Attribute	Default	Description
7	RW	0	**Disable PHY Auto Power-Down Feature** When set this bit to 0, if port is suspended or is not owned by EHCI, the port will auto power-down. 0: Auto power-down 1: Disable Auto power-down
6	RW	0	**Transit POwner (Port Owner) Control** This bit controls port route logic to be programmable if port connection is not present, default is to transit POwner only at falling edge of connect status. 0: Falling edge 1: Level
5:4	RW	0	**Reserved**
3	RW	1b	**DPLL Fast Lock Enable** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	1b	**Disable PHY Receiver Including Squelch Detector Power up Time Improvement** 0: Enable improvement 1: Disable improvement
0	RW	1b	**Reserved**

Offset Address: 5B-5Ah (D16F4)

High-Speed Port Pad Termination Resistor Fine Tune 1 **Default Value: 8888h**

Bit	Attribute	Default	Description
15:12	RW	1000b	**Control Bits for HS Termination Resistor Bit[15, 14, 12] and LS Falling Time Fine Tune Bit[13] – For USB Port 1** Bits [15, 14, 12] 001: 52ohm 010: 48ohm 100: 45ohm Others: Reserved Bit [13] 0: 0% 1: -33%
11:8	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 2** Refer to the information provided in bits [15:12].
7:4	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 3** Refer to the information provided in bits [15:12].
3:0	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 4** Refer to the information provided in bits [15:12].

Offset Address: 5Ch (D16F4)

PHY Control 9 **Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	**DPLL Zero Phase Start Select** 0: ZPS takes 8-bit times to start 1: ZPS takes 4-bit times to start
6	RW	0	**High Speed Transmitter** Used for high-speed transmitter, no DPLL. 0: Normal 1: Rise / fall time increase 100ps
5:4	RW	00b	**DPLL Input Data Delay Select** 00: 0ps 01: -43~-135ps 10: 43~135ps 11: 86~270ps
3:2	RW	01b	**DPLL Track Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)
1:0	RW	11b	**DPLL Lock Speed Select** 00: 2 01: 4 10: 8 11: 16 (Counter)

Offset Address: 5Dh (D16F4)

High-Speed Port Pad Termination Resistor Fine Tune 2 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 5** Refer to the information provided in Rx5B-5A [15:12].
3:0	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 6** Refer to the information provided in Rx5B-5A [15:12].

Offset Address: 5Eh (D16F4)

PHY Control 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**USB Port 8 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
6	RW	0	**USB Port 7 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
5	RW	0	**USB Port 6 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
4	RW	0	**USB Port 5 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
3	RW	0	**USB Port 4 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
2	RW	0	**USB Port 3 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
1	RW	0	**USB Port 2 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.
0	RW	0	**USB Port 1 Tx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Tx test mode register, active high.

Offset Address: 5Fh (D16F4)

PHY Control 11 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**USB Port 8 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
6	RO	0	**USB Port 7 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
5	RO	0	**USB Port 6 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
4	RO	0	**USB Port 5 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
3	RO	0	**USB Port 4 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
2	RO	0	**USB Port 3 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
1	RO	0	**USB Port 2 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.
0	RO	0	**USB Port 1 Rx Data (For Test Mode)** Full Speed (FS) / Low Speed (LS) Rx receiver comparator output.

Offset Address: 60h (D16F4)
Serial Bus Release Number **Default Value: 20h**

Bit	Attribute	Default	Description
7:0	RO	20h	**Serial Bus Release Number** Fixed at 20h for USB2.0.

Offset Address: 61h (D16F4)
Frame Length Adjustment **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	20h	**Frame Length Adjustment** This feature is used to adjust any offset from the clock source that generates the clock that drives the SOF counter. Please refer to "EHCI Specification for USB" Section 2.1.5.

Offset Address: 63-62h (D16F4)
Port Wake Capability **Default Value: 0001h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8:1	RW	0	**Port Wake Up Capability Mask** Bits [8:1] in the mask correspond to a physical port implemented on the current EHCI controller. Please refer to "EHCI Specification for USB" Section 2.1.6. 0: A zero in a bit position indicates that a device connected below the port can NOT be enabled as a wake-up device and the port may be NOT enabled for disconnect/connect or over-current events as wake-up events. 1: A one in a bit position indicates that a device connected below the port can be enabled as a wake-up device and the port may be enabled for disconnect/connect or over-current events as wake-up events.
0	RO	1b	**Port Wake Capability Register Implementation** This bit indicates whether this Port Wake Capability register is implemented. Please refer to "EHCI Specification for USB" Section 2.1.6. 0: Port Wake Capability register is NOT implemented 1: Port Wake Capability register is implemented

Offset Address: 64h (D16F4)
USB CP4 Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**USB HS NULL-SOF (**Null Start Of Frame) **Valid Time Selection Extend Bit-2 (for C4P Support)** Bit-2 and Rx49[1:0] are combined to select NULL-SOF valid time {Rx64[2], Rx49[1:0]}: 000: 2 micro frames 001: 4 micro frames 010: Invalid value 011: Invalid value 100: 8 micro frames 101: 16 micro frames 110: 24 micro frames 111: 32 micro frames
1:0	RW	0	**Reserved**

Offset Address: 65h (D16F4)

Control Register **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:6	RW	0	**Internal Current Source Increment** 00: No increment 01: 1% 10: 2 % 11: 4%
5	RW	0	**Enable 33MHz Dynamic Scheme** 0: Disable 1: Enable
4	RW	0	**Enable 66MHz Dynamic Scheme** 0: Disable 1: Enable
3	RW	1b	**Async Controller Bus Authority Selection** 0: Async controller bus authority could change at any time 1: Async controller bus authority could only change after either async controller finished current transaction
2	RW	1b	**Reserved**
1	RW	0	**Bus Master Enable Select** 0: If disable Bus Master Enable, it will works immediately 1: If disable Bus Master Enable, it will works after current transaction
0	RW	0	**Reserved**

Offset Address: 66h (D16F4)

High-Speed Port Pad Termination Resistor Fine Tune 4 **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 7** Refer to the information provided in Rx5B-5A[15:12].
3:0	RW	1000b	**Control Bits for HS Termination Resistor and LS Falling Time Fine Tune – For USB Port 8** Refer to the information provided in Rx5B-5A [15:12].

Offset Address: 67h (D16F4) – Reserved

Offset Address: 6B-68h (D16F4)

USB Legacy Support Extended Capability **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RW	0	**USB Host Controller OS-owned Semaphore**
23:17	RO	0	**Reserved**
16	RW	0	**USB Host Controller BIOS-owned Semaphore**
15:8	RO	0	**Next EHCI Extended Capability Pointer**
7:0	RO	01h	**Capability ID** 01h identifies the capability as Legacy Support. Please also refer to EHCI Spec. Section 2.1.7 for more details.

Offset Address: 6F-6Ch (D16F4)

USB Legacy Support Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW1C	0	**SMI on BAR**
30	RW1C	0	**SMI on PCI Command**
29	RW1C	0	**SMI on OS Ownership Change**
28:22	RO	0	**Reserved**
21	RO	0	**SMI on Ssync Advance**
20	RO	0	**SMI on Host System Error**
19	RO	0	**SMI on Frame List Rollover**
18	RO	0	**SMI on Port Change Detect**
17	RO	0	**SMI on USB Error**
16	RO	0	**SMI on USB Complete**
15	RW	0	**SMI on BAR Enable**
14	RW	0	**SMI on PCI Command Enable**
13	RW	0	**SMI on OS Ownership Enable**
12:6	RO	0	**Reserved**
5	RW	0	**SMI on Async Advance Enable**
4	RW	0	**SMI on Host System Error Enable**
3	RW	0	**SMI on Frame List Rollover Enable**
2	RW	0	**SMI on Port Change Enable**
1	RW	0	**SMI on USB Error Enable**
0	RW	0	**USB SMI Enable**

Offset Address: 70-7Fh (D16F4) – Reserved

Offset Address: 80h (D16F4)

Power Management Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D16F4)

Next Item Pointer 1 **Default Value: 88h**

Bit	Attribute	Default	Description
7:0	RO	88h	**Next Item Pointer 1** If Rx4C[4] = 1, this register is fixed at 88h. If Rx4C[4] = 0, this register is fixed at 00h.

Offset Address: 83-82h (D16F4)
Power Management Capability **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:0	RO	FFC2h	**Power Management Capability** If D16F0-F2 Rx49[1] = 1, this register is fixed at FFC2h. If D16F0-F2 Rx49[1]= 0, this register is fixed at 7E0Ah. Please refer to the "PCI Bus Power Management Interface Specification Revision 1.1 Chapter 3.2" for details.

Offset Address: 85-84h (D16F4)
Power Management Capability Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME Status** 0: Not active 1: Active
14:9	RO	0	**Reserved**
8	RW	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 01: D1 10: D2 11: D3 Hot

Offset Address: 86-87h (D16F4) – Reserved

Offset Address: 88h (D16F4)
Debug Port Capability ID **Default Value: 0Ah**

Bit	Attribute	Default	Description
7:0	RO	0Ah	**Debug Port Capability ID** If Rx4C[4] = 1, this register is fixed at 0Ah. If Rx4C[4] = 0, this register is fixed at 00h.

Offset Address: 89h (D16F4)
Next Item Pointer 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer 2**

Offset Address: 8B-8Ah (D16F4)
Debug Port Base Offset **Default Value: 20A0h**

Bit	Attribute	Default	Description
15:0	RO	20A0h	**Debug Port Base Offset** If Rx4C[4] = 1, this register is fixed at 20A0h If Rx4C[4] = 0, this register is fixed at 0000h

Offset Address: 8C-FFh (D16F4) – Reserved

EHCI USB 2.0 Memory Mapped I/O Registers

These registers are compliant with the EHCI v1.0 standard. Refer to the EHCI v1.0 specification for further details.

EHCI Capabilities (00-0Bh)

Offset Address: 00h (USB 2.0-MMIO)

Capability Register Length **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Capability Register Length**

Offset Address: 01h (USB 2.0-MMIO)– Reserved

Offset Address: 03-02h (USB 2.0-MMIO)

Interface Version Number **Default Value: 0100h**

Bit	Attribute	Default	Description
15:0	RO	0100h	**Interface Version Number**

Offset Address: 07-04h (USB 2.0-MMIO)

Structure Parameters **Default Value: 0000 4208h**

Bit	Attribute	Default	Description
31:0	RO	0000 4208h	**Structure Parameters** If Rx4C[4] = 1, fixed at 0010 4208h. If Rx4C[4] = 0, fixed at 0000 4208h.

Offset Address: 0B-08h (USB 2.0-MMIO)

Capability Parameters **Default Value: 0000 6872h**

Bit	Attribute	Default	Description
31:0	RO	0000 6872h	**Capability Parameters**

Offset Address: 0C-0Fh (USB 2.0-MMIO) – Reserved

Host Controller Operations (10-9Fh)

Offset Address: 13-10h (USB 2.0-MMIO)

USB Command **Default Value: 0008 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RW	08h	**Interrupt Threshold Control**
15:8	RO	0	**Reserved**
7	RW	0	**Light Host Controller Reset**
6	RW	0	**Interrupt on Async Advance Doorbell**
5	RW	0	**Asynchronous Schedule Enable**
4	RW	0	**Periodic Schedule Enable**
3:2	RW	0	**Frame List Size**
1	RW	0	**Host Controller Reset**
0	RW	0	**Run / Stop**

I/O Offset Address: 17-14h (USB 2.0-MMIO)

USB Status **Default Value: 0000 1000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15	RO	0	**Asynchronous Schedule Status**
14	RO	0	**Periodic Schedule Status**
13	RO	0	**Reclamation**
12	RO	1b	**Host Controller Halted**
11:6	RO	0	**Reserved**
5	RW1C	0	**Interrupt on Async Advance**
4	RW1C	0	**Host System Error**
3	RW1C	0	**Frame List Rollover**
2	RW1C	0	**Port Change Detect**
1	RW1C	0	**USB Error Interrupt**
0	RW1C	0	**USB Interrupt**

I/O Offset Address: 1B-18h (USB 2.0-MMIO)

USB Interrupt Enable **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:6	RO	0	**Reserved**
5:0	RW	0	**USB Interrupt Enable** 0: Disable 1: Enable

I/O Offset Address: 1F-1Ch (USB 2.0-MMIO)

USB Frame Index **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	RO	0	**Reserved**
12:0	RW	0	**USB Frame Index**

I/O Offset Address: 23-20h (USB 2.0-MMIO)

4G Segment Selector **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**4G Segment Selector**

I/O Offset Address: 27-24h (USB 2.0-MMIO)

Frame List Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**Frame List Base Address**
11:0	RO	0	**Reserved**

I/O Offset Address: 2B-28h (USB 2.0-MMIO)

Next Asynchronous List Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:5	RW	0	**Next Asynchronous List Address**
4:0	RO	0	**Reserved**

I/O Offset Address: 2C-4Fh (USB 2.0-MMIO) - Reserved

I/O Offset Address: 53-50h (USB 2.0-MMIO)

Configured Flag **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Configured Flag**

I/O Offset Address: 57-54h (USB 2.0-MMIO)

Port 0 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 5B-58h (USB 2.0-MMIO)

Port 1 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 5F-5Ch (USB 2.0-MMIO)

Port 2 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 63-60h (USB 2.0-MMIO)

Port 3 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 67-64h (USB 2.0-MMIO)

Port 4 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 6B-68h (USB 2.0-MMIO)

Port 5 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 6F-6Ch (USB 2.0-MMIO)

Port 6 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

I/O Offset Address: 73-70h (USB 2.0-MMIO)

Port 7 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:23	RO	0	**Reserved**
22	RW	0	**Wake on Over-current Enable**
21	RW	0	**Wake on Disconnect Enable**
20	RW	0	**Wake on Connect Enable**
19:16	RW	0	**Port Test Control**
15:14	RO	0	**Reserved**
13	RW	1b	**Port Owner**
12	RO	1b	**Port Power**
11:10	RO	0	**Line Status**
9	RO	0	**Reserved**
8	RW	0	**Port Reset**
7	RW	0	**Suspend**
6	RW	0	**Force Port Resume**
5	RW1C	0	**Over-current Change**
4	RO	0	**Over-current Active**
3	RW1C	0	**Port Enable / Disable Change**
2	RW	0	**Port Enabled / Disabled**
1	RW1C	0	**Connect Status Change**
0	RO	0	**Current Connect Status**

Offset Address: 74-9Fh (USB 2.0-MMIO) – Reserved

Debug Port Controller Operational Registers (A0-B3h)

Offset Address: A3-A0h (USB 2.0-MMIO)

Debug Port Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30	RW	0	**Force the Ownership of the Debug Port to the EHCI Controller (Owner)** 0: Disable 1: Enable
29	RO	0	**Reserved**
28	RW	0	**Enable Debug Port (Enabled)** 0: Disable 1: Enable
27:17	RO	0	**Reserved**
16	RW1C	0	**Transaction Request Complete (Done)** 0: Not complete 1: Complete
15:11	RO	0	**Reserved**
10	RW	0	**Port In Use (In Use)** 0: Port available. 1: Port in use
9:7	RO	000b	**Exception Error Type (Exception)** 000: None 001: Transaction error or babble: indicates the USB2 transaction had an error (CRC, bad PID, timeout, packet babble, etc.) 010: HW error. Request was attempted (or in progress) when port was suspended or reset. Others: Reserved
6	RO	0	**Error Status (Error / Good#)** 0: No error occurred 1: Error occurred
5	RW	0	**Start a Request (Go)** 0: Not start a request 1: Notify hardware to perform a request
4	RW	0	**Current Request Type (Write / Read#)** 0: Current request for read 1: Current request for write
3:0	RW	0	**Data Length**

Offset Address: A7-A4h (USB 2.0-MMIO)

Debug Port USB PIDs (Packet Identifier) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RO	0	**Received PID**
15:8	RW	0	**Send PID**
7:0	RW	0	**Token PID**

Offset Address: AF-A8h (USB 2.0-MMIO)

Debug Port Data Buffer **Default Value: FFFF FFFF FFFF FFFFh**

Bit	Attribute	Default	Description
63:0	RW	FFFF FFFF FFFF FFFFh	**Debug Port Data Buffer** The default value will change after power up as it from SRAM. Only debug mode will use it.

Offset Address: B3-B0h (USB 2.0-MMIO)

Debug Port Device Address **Default Value: 0000 7F01h**

Bit	Attribute	Default	Description
31:15	RO	0	**Reserved**
14:8	RW	7Fh	**USB Address**
7:4	RO	0	**Reserved**
3:0	RW	1h	**USB Endpoint**

DEVICE 17 FUNCTION 0 (D17F0): BUS CONTROL AND POWER MANAGEMENT

PCI Configuration Space

All registers are located in D17F0 Configuration Space. These registers are accessed through PCI configuration mechanism #1 via I/O address 0CF8h / 0CFCh with bus number 0, device number 17 and function number 0. All registers in this chapter are for Bus Control.

There are 4 sets of PCI UART IO base addresses within D17F0:

- PCI UART1 I/O base address is located in D17F0 RxB3
- PCI UART2 I/O base address is located in D17F0 RxB4
- PCI UART3 I/O base address is located in D17F0 RxB5
- PCI UART4 I/O base address is located in D17F0 RxB6

Header Registers (00-3Fh)

Offset Address: 01-00h (D17F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D17F0)
Device ID **Default Value: 8410h**

Bit	Attribute	Default	Description
15:0	RO	8410h	**Device ID**

Offset Address: 05-04h (D17F0)
PCI Command **Default Value: 0003h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	**Reserved**
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	0	**PCI Master Function**
1	RW	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RW	1b	**I/O Space Access** Hardwired to 1 (Responds to I/O space access)

Offset Address: 07-06h (D17F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus Master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6:0	RO	10h	**Reserved (Do Not Program)**

Offset Address: 08h (D17F0)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-09h (D17F0)

Class Code **Default Value: 06 0100h**

Bit	Attribute	Default	Description
23:0	RO	060100h	**Class Code**

Offset Address: 0C-0Dh (D17F0) – Reserved

Offset Address: 0Eh (D17F0)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h means multi-function device.

Offset Address: 0Fh (D17F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST** Fixed at 00h.

Offset Address: 10-2Bh (D17F0) – Reserved

Offset Address: 2D-2Ch (D17F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D17F0)
Subsystem ID **Default Value: 8410h**

Bit	Attribute	Default	Description
15:0	RO	8410h	**Subsystem ID**

Offset Address: 30-33h (D17F0) – Reserved

Offset Address: 34h (D17F0)
Power Management Capabilities Pointer **Default Value: C0h**

Bit	Attribute	Default	Description	Mnemonic	ChipRev	PwrDm	S	P	E
7:0	RO	C0h	**Power Management Capabilities Pointer**				R	x	x

Offset Address: 35-3Fh (D17F0) – Reserved

ISA Bus Control (40-49h)

Offset Address: 40h (D17F0)

ISA Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Extra / Normal ISA Command Delay** 0: Normal 1: External
6	RW	0	**I/O Recovery Time** 0: Disable 1: Enable
5	RW	0	**Reserved**
4	RW	0	**ROM Write** 0: Disable 1: Enable
3	RW	0	**Double DMA Clock** 0: Disable 1: Enable
2	RW	0	**4D0 / 4D1 Support** 0: Disable 1: Enable
1	RW	0	**MEGA Cells (DMAC, INTC and TMRC) Shadow Register Read** 0: Disable 1: Enable
0	RW	0	**BCLK (Bus Clock) = PCLK (PCI Bus Clock) / 2** 0: Disable 1: Enable

Offset Address: 41h (D17F0)

ROM Decode Control **Default Value: 80h**

Setting these bits to 1 enables the indicated address range to be included in the LPC BIOS ROM address decoding.

Bit	Attribute	Default	Description
7	RW	1b	**For Memory Address 000E0000h-000EFFFFh**
6	RW	0	**For Memory Address FFF00000h-FFF7FFFFh and FFB00000h-FFB7FFFFh**
5	RW	0	**For Memory Address FFE80000h-FFEFFFFFh and FFA80000h-FFAFFFFFh**
4	RW	0	**For Memory Address FFE00000h-FFE7FFFFh and FFA00000h-FFA7FFFFh**
3	RW	0	**For Memory Address FFD80000h-FFDFFFFFh and FF980000h-FF9FFFFFh**
2	RW	0	**For Memory Address FFD00000h-FFD7FFFFh and FF900000h-FF97FFFFh**
1	RW	0	**For Memory Address FFC80000h-FFCFFFFFh and FF880000h-FF8FFFFFh**
0	RW	0	**For Memory Address FFC00000h-FFC7FFFFh and FF800000h-FF87FFFFh**

Offset Address: 42h (D17F0)

Line Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DMA Line Buffer** 0: Disable 1: Enable. Setting this bit to 1 indicates Master DMA waits until the line buffer is full (8 DW) before transmitting data (bit-6 must also be enabled to ensure that there are no coherency issues).
6	RW	0	**Gate INTR Assertion Until Line Buffer Flush Is Complete** 0: Disable 1: Enable. INTR assertion is gated until the line buffer is flushed. This bit should be enabled if bit-7 is enabled.
5	RW	0	**IRQ Flush Line Buffer When No DMA is Granted** 0: Disable 1: Enable This bit is to enable line buffer flushing when interrupt request is received. However, the line buffer flushing is performed only when no DMA is granted.
4	RW	0	**Uninterruptible Burst Read** 0: Disable 1: Enable. The PCI bus is not granted to DMA until burst read transactions from the host are completed.
3	RW	0	**Gate Serial IRQ Inputs Until Line Buffer Flush Is Complete** 0: Disable 1: Enable
2	RW	0	**IRQ Flush Line Buffer Even When DMA Is Granted** Line buffer is flushed even if DMA is granted with bit 5 =1 0: Disable 1: Enable
1:0	RW	00b	**SMBus Test Mode Select** 00: Normal Mode 01:Slow Mode 1 10: Slow Mode 2 11: Test Mode

Offset Address: 43h (D17F0)

Delay Transaction Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:5	RO	0	**Reserved**
4	RW	0	**Reserved**
3	RW	1b	**Delayed Transactions (PCI Spec Rev 2.1)** This bit controls whether delayed transactions (delayed read / write and posted write) are enabled. 0: Disable 1: Enable
2	RW	0	**Delayed Transaction – Posted Write Only** 0: Disable 1: Enable
1	RW	0	**Write Delay Transaction Timeout Timer** When enabled, if a delayed transaction (write cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable
0	RW	0	**Read Delay Transaction Timeout Timer** When enabled, if a delayed transaction (read cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable

Offset Address: 44h (D17F0)

PCI PnP Interrupt Routing − INTE#, INTF# **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTF# Routing** Refer to Table 43 PnP IRQ Routing Table
3:0	RW	0	**PCI INTE# Routing** Refer to Table 43 PnP IRQ Routing Table

Offset Address: 45h (D17F0)

PCI PnP Interrupt Routing − INTG#, INTH# **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTH# Routing** Refer to Table 43 PnP IRQ Routing Table
3:0	RW	0	**PCI INTG# Routing** Refer to Table 43 PnP IRQ Routing Table

Offset Address: 46h (D17F0)

PCI INT[H:E]# UART Multiplex Select Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SERIRQ Pull-up Enable Signal** 0: Disable 1: Enable
6	RW	0	**UART Function Multiplex with DVP or VCP Pad** 0: Disable 1: Enable
5	RW	0	**Control the Destination of IO Port 0x80** Reference with Rx5B[6].
4	RW	0	**PCI INT Sharing Control** 0: INTH# shared with INTD# INTG# shared with INTC# INTF# shared with INTB# INTE# shared with INTA# 1: INTH# routing according to Rx45[7:4] INTG# routing according to Rx45[3:0] INTF# routing according to Rx44[7:4] INTE# routing according to Rx44[3:0] If Rx55[3]=1, and external general interrupt selects INTE#, INTF#, INTG# or INTH#, this bit must be programmed to 1.
3	RW	0	**Invert PCI INTH# Trigger** 0: Non invert 1: Invert
2	RW	0	**Invert PCI INTG# Trigger** 0: Non invert 1: Invert
1	RW	0	**Invert PCI INTF# Trigger** 0: Non invert 1: Invert
0	RW	0	**Invert PCI INTE# Trigger** 0: Non invert 1: Invert

Note: For routing control of PCI INTA# ~ INTD#, see Device 17 Function 0 Rx54-57 and PnP IRQ Routing Table (Refer to Table 43).

Offset Address: 47h (D17F0)

PATA PAD Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Control of VRDSLP Pull-up Control** 0: Enable 1: Disable
6	RW	0	**CEC Positive Decode Control** 0: Disable 1: Enable
5:4	RW	0	**SMB Master Debounce Mode Select** 00: Bypass mode 01: Master debounce mode1 10: Master debounce mode2 11: Master debounce mode3
3:0	RW	0	**Reserved**

Offset Address: 48h (D17F0)

APIC FSB Data Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FSB Fixed at Low DW** 0: Disable. Address bit-2 (A2) is not masked. 1: Enable. Force A2 from APIC FSB to low. Address bit A2 controls whether data is in the lower (0) or upper (1) doubleword of a quadword sent to the CPU. When this bit is enabled, A2 is masked which means it is always 0 to select the lower doubleword.
6	RO	0	**Reserved**
5	RW	0	**PCI UART 3 Legacy Mode Enable** 0: Disable 1: Enable
4	RW	0	**PCI UART 2 Legacy Mode Enable** 0: Disable 1: Enable
3	RW	0	**PCI UART 1 Legacy Mode Enable** 0: Disable 1: Enable
2	RW	0	**PCI UART 0 Legacy Mode Enable** 0: Disable 1: Enable
1	RW	0	**Reserved**
0	RW	0	**PCI UART Enable** 0: Disable 1: Enable

Offset Address: 49h (D17F0)

SM Peripheral Device Control **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**SERR from Host Directed to PMU (SMI, SCI)** 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	1b	**Gated IRQ before SM Buffer Clean** Controls whether interrupt requests are gated until data is written to memory. 0: Disable 1: Enable
4	RW	0	**PCIM Address Stepping** 0: Disable 1: Enable
3	RW	0	**PCIM Wait State** 0: Disable 1: Enable
2	RW	0	**WSC Mask Off INTR** Controls whether INTR is masked until write snoop is complete. 0: Disable 1: Enable
1:0	RW	0	**Reserved**

LPC Firmware Memory Control (4A-4Bh)

Offset Address: 4Ah (D17F0)

LPC Firmware Memory Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**LPC Firmware Memory Base Address [23:17]**
0	RW	0	**LPC Firmware Memory Programmable IDSEL** 0: Disable 1: Enable When this bit is enabled, the memory cycles in the address range, specified by Rx4A-4Bh, will be transferred into LPC firmware memory cycles no matter what the setting of Rx59 is.

Offset Address: 4Bh (D17F0)

LPC Firmware Memory Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Firmware Read Cycle New Hit Method** 0: Disable 1: Enable
6:4	RW	000b	**LPC Firmware Memory Base Address Mask** Set bit 6 to 1 to mask A19 decoding. Set bit 5 to 1 to mask A18 decoding. Set bit 4 to 1 to mask A17 decoding.
3:0	RW	0	**LPC Firmware Memory IDSEL Value**

Miscellaneous Control (4C-4Fh)

Offset Address: 4Ch (D17F0)

IDE Interrupt Select **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	**I/O Recovery Time Select** When Rx40[6] is enabled, this field determines the I/O recovery time. 00: 1 bus clock 01:2 bus clocks 10: 4 bus clocks 11:8 bus clocks
5:4	RW	0	**Reserved**
3:2	RW	01b	**Reserved**
1:0	RW	00b	**EIDE Primary Channel IRQ Routing** 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11

Offset Address: 4Dh (D17F0)

Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LPC Firmware Memory 16 Bytes Burst Read** 0: Disable 1: Enable
6	RW	0	**LPC Firmware Memory 4 Bytes Burst Read / Write Access** 0: Disable 1: Enable
5	RW1	0	**Firmware Memory Burst Detection** Write 1 to start to detect the Firmware memory burst ability 0: Complete 1: Incomplete If the LPC Firmware memory supports 16-byte burst, bit 7 will be set to 1 after burst detection complete. If the LPC Firmware memory support 4-byte burst, the bit 6 will be set 1 after burst detection complete.
4	RW	0	**LPC Firmware Memory IDSEL Value** 0: IDSEL is from Rx75[7:4] 1: IDSEL is from AD28-AD31 This control bit is valid when Rx4D[1] is set to 1.
3	RW	0	**Enable Fixed Path of External Interrupt Delivery Only in APIC IRQ0 When the Interrupt Controller Has Not Been Masked Yet** 0: Disable 1: Enable
2	RW	0	**Serial IRQs Always be Shared in APIC Mode** 0: Disable 1: Enable
1	RW	0	**LPC Firmware Memory Cycle Configuration** 0: Only cycles which are targeting the specified programmable ROM space are converted into LPC firmware memory cycles (LPC ROM range and IDSEL value is determined by registers in Rx75-76h and Rx7C-7Fh) 1: All memory cycles are converted into LPC firmware memory cycles (IDSEL value is decided by bit 4) This register is used to select the memory ranges that are treated as LPC Firmware Memory space when Rx59[7] is set to 0.
0	RW	0	**LPC TPM Function** 0: Disable 1: Enable

Offset Address: 4Eh (D17F0)

Internal RTC Test Mode and Extra Feature Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**RTC High Bank Rx3F-38 R/W Protect** 0: Disable (allow R/W) 1: Enable (Protect)
6	RW	0	**RTC Low Bank Rx3F-38 R/W Protect** 0: Disable (allow R/W) 1: Enable (Protect)
5	RW	0	**Reserved**
4	RO	0	**RTC Last Write Status** 0: Last write was to port 70 1: Last write was to port 74
3	RW	0	**Enable RTC Port 74/75** The RTC is normally accessed though ports 70/74. This bit controls whether two extra ports (74/75) can be used to access the RTC. 0: Disable 1: Enable
2:0	RW	0	**Reserved**

Offset Address: 4Fh (D17F0)

PCI Reset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Software PCI Reset** 0: Disable 1: Enable Write 1 to generate PCI reset. Software reset can also be initiated through I/O port CF9 as follows: Write 1 to I/O port CF9 bit-2 for software reset: If CF9 bit 1 is 0, INIT will be asserted; If CF9 bit 1 is 1 (default), PCIRST will be asserted.

Function Control (50-51h)

Offset Address: 50h (D17F0)

Function Control 1 **Default Value:00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**USB Device Mode Enable** 0: Enable 1: Disable
5	RW	0	**Device 16 Function 1 (USB 1.1 UHCI Port 2-3)** 0: Enable 1: Disable
4	RW	0	**Device 16 Function 0 (USB 1.1 UHCI Port 0-1)** 0: Enable 1: Disable
3	RW	0	**Device 15 Function 0 (SATA/EIDE)** 0: Enable 1: Disable
2	RW	0	**Device 16 Function 2 (USB 1.1 UHCI Port 4-5)** 0: Enable 1: Disable
1	RW	0	**Device 16 Function 4 (USB 2.0 EHCI Port 0-7)** 0: Enable 1: Disable
0	RW	0	**Device 16 Function 3 (USB 1.1 UHCI Port 6-7)** 0: Enable 1: Disable

Offset Address: 51h (D17F0)

Function Control 2 **Default Value: 0Dh**

Bit	Attribute	Default	Description
7	RW	0	**Multiple Memory Card Controller Disable** 0: Enable 1: Disable
6	RW	0	**Reserved**
5	RO	0	**Reserved**
4	RW	0	**SDIO Disable** 0: Enable 1: Disable
3	RW	1b	**Internal RTC** 0: Disable 1: Enable
2	RW	1b	**Internal PS2 Mouse** 0: Disable 1: Enable
1	RW	0	**Internal Keyboard Controller Configuration** 0: Disable 1: Enable
0	RW	1b	**Internal Keyboard Controller** 0: Disable 1: Enable

Serial IRQ, LPC and PC / PCI DMA Control (52-53h)

Offset Address: 52h (D17F0)

Serial IRQ, PCI / DMA Control and LPC Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**LPC Short Wait Abort** 0: Disable 1: Enable. In a short wait, the cycle is aborted after 8Ts.
5	RW	0	**LPC Frame Wait State** 0: Disable 1: Enable
4	RW	0	**Serial IRQ Stop to Start Frame Wait State** 0: Disable. One idle state is inserted between Stop and Start. 1: Enable. Stop is followed immediately by Start.
3	RW	0	**Serial IRQ** 0: Disable 1: Enable. (IRQ asserted via SERIRQ)
2	RW	0	**Serial IRQ Quiet Mode** 0: Continuous Mode 1: Quiet Mode
1:0	RW	00b	**Serial IRQ Start-Frame Width** 00: 4 PCI clocks 01: 6 PCI clocks 10: 8 PCI clocks 11: 10 PCI clocks

Offset Address: 53h (D17F0)

PC / PCI DMA Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PC/PCI DMA Control** 0: Disable PC/PCI DMA. (The signal balls are used for GPIO) 1: Enable PC/PCI DMA
6	RW	0	**DMA Channel 7 for PC/PCI DMA** 0: Disable 1: Enable
5	RW	0	**DMA Channel 6 for PC/PCI DMA** 0: Disable 1: Enable
4	RW	0	**DMA Channel 5 for PC/PCI DMA** 0: Disable 1: Enable
3	RW	0	**DMA Channel 3 for PC/PCI DMA** 0: Disable 1: Enable
2	RW	0	**DMA Channel 2 for PC/PCI DMA** 0: Disable 1: Enable
1	RW	0	**DMA Channel 1 for PC/PCI DMA** 0: Disable 1: Enable
0	RW	0	**DMA Channel 0 for PC/PCI DMA** 0: Disable 1: Enable

Plug and Play Control – PCI (54-57h)

Offset Address: 54h (D17F0)

PCI Bus and CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved** The following bits all default to "Low Active Level " triggered (0)
4	RW	0	**Enable PCI Debug Mode** If enabled, reuse SDIO/CR/SPI Pads as PCI bus signal. 0: Disable 1: Enable
3	RW	0	**Invert PCI INTA# Trigger** 0: Non invert 1: Invert
2	RW	0	**Invert PCI INTB# Trigger** 0: Non invert 1: Invert
1	RW	0	**Invert PCI INTC# Trigger** 0: Non invert 1: Invert
0	RW	0	**Invert PCI INTD# Trigger** 0: Non invert 1: Invert

Note: PCI INTA-D# normally connect to PCI interrupt pins INTA-D# (see signal descriptions for more information).

Offset Address: 55h (D17F0)

PCI PnP Interrupt Routing 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTA# Routing (Refer to Table 43- PnP IRQ Routing Table)**
3	RW	0	**Enable External General Interrupt from GPIO14** 1: Enable 0: Disable
2:0	RW	000b	**External General Interrupt Routing Selection** 000: Routing to INTA# 001: Routing to INTB# 010: Routing to INTC# 011: Routing to INTD# 100: Routing to INTE# 101: Routing to INTF# 110: Routing to INTG# 111: Routing to INTH#

Offset Address: 56h (D17F0)

PCI PnP Interrupt Routing 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTC# Routing** Refer to Table 43 PnP IRQ Routing Table
3:0	RW	0	**PCI INTB# Routing** Refer to Table 43 PnP IRQ Routing Table

Offset Address: 57h (D17F0)

PCI PnP Interrupt Routing 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTD# Routing** Refer to Table 43 PnP IRQ Routing Table
3:0	RO	0	**Reserved** Always reads 0.

Table 43. PnP IRQ Routing Table

INTA#~INTH# Routing Register	PIC Mode
0000	Reserved
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

APIC Mode	INTA#~INTH#
PIRQ16	INTA#
PIRQ17	INTB#
PIRQ18	INTC#
PIRQ19	INTD#
PIRQ20	INTE#
PIRQ21	INTF#
PIRQ22	INTG#
PIRQ23	INTH#

When enable internal APIC, PCI devices and internal function, IRQ routings are shown as below:

Table 44. Internal APIC, PCI Devices IRQ Routing Table

HPET IRQ, PCI UART 0 IRQ	IRQ16
HPET IRQ, HDAC IRQ, PCI UART 1 IRQ	IRQ17
HPET IRQ, PCI UART 2 IRQ	IRQ18
HPET IRQ, USBD IRQ, PCI UART 3 IRQ	IRQ19
UHCI Port 0-1 IRQ	IRQ20
UHCI Port 4-5 IRQ, SATA IRQ in native mode.	IRQ21
UHCI Port 2-3 IRQ and SDIO IRQ	IRQ22
Card Reader IRQ and EHCI Port 0-7, UHCI Port 6-7 IRQ	IRQ23

Table 45. HPET IRQ Routing Table

Mode	Timer 0	Timer 1	Timer 2
Legacy Mode	IRQ0(PIC) / IRQ2(APIC)	IRQ8(PIC) / IRQ8(APIC)	—
Non-legacy Mode	IRQ16-19 for APIC only	IRQ16-19 for APIC only	IRQ11, IRQ16-19 for APIC only

GPIO and Miscellaneous Control (58-5Bh)

Offset Address: 58h (D17F0)

South Module Miscellaneous Control 1 **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Internal APIC** 0: Disable 1: Enable
5	RW	1b	**South Module Interrupt Cycles Sync. with 33 MHz Clock** 0: Disable (8 MHz) 1: Enable
4	RW	0	**South Module PCI Cycle Decode** 0: Subtractive 1: Positive
3	RW	0	**RTC High Bank Access** 0: Disable 1: Enable
2	RW	0	**RTC Rx32 Write Protect** 0: Disable (not protected) 1: Enable (write protected)
1	RW	0	**RTC Rx0D Write Protect** 0: Disable (not protected) 1: Enable (write protected)
0	RW	0	**RTC Rx32 Map to Century Byte** Controls whether RTC Rx32 is mapped to the century byte. 0: Disable 1: Enable

Offset Address: 59h (D17F0)

South Module Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LPC/SPI Memory Space** 0: All memory cycles are forwarded to LPC/SPI 1: Memory cycles with address in the ranges specified by the ROM Memory Address Range registers are forwarded to LPC/SPI.
6	RW	0	**Reserved**
5	RW	0	**LPC RTC** 0: Disable 1: Enable
4	RW	0	**LPC Keyboard** 0: Disable (ISA Keyboard) 1: Enable (LPC Keyboard)
3	RW	0	**Port 62h / 66h (MCCS#) to LPC** 0: Disable 1: Enable
2	RW	0	**Port 62h / 66h (MCCS#) Decode** 0: Disable 1: Enable
1	RW	0	**Mask A20M# Active** 0: Disable (A20M# acts normally) 1: Enable (A20M# signal de-asserted)
0	RW	0	**NMI on PCI Parity Error** 0: Disable 1: Enable (to generate NMI, Port 61[3] and Port 70[7] must also be set)

Note: To trigger NMI assertion correctly, both IO port 61 bit3 and IO port70 bit7 must be set to 0 since data parity error report is combined with IOCHK.

Offset Address: 5Ah (D17F0)

DMA Bandwidth Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DMA Channel 7 Bandwidth** 0: Normal 1: Improved
6	RW	0	**DMA Channel 6 Bandwidth** 0: Normal 1: Improved
5	RW	0	**DMA Channel 5 Bandwidth** 0: Normal 1: Improved
4	RW	0	**DMA Single Transfer Mode Bandwidth** 0: Normal 1: Improved
3	RW	0	**DMA Channel 3 Bandwidth** 0: Normal 1: Improved
2	RW	0	**DMA Channel 2 Bandwidth** 0: Normal 1: Improved
1	RW	0	**DMA Channel 1 Bandwidth** 0: Normal 1: Improved
0	RW	0	**DMA Channel 0 Bandwidth** 0: Normal 1: Improved

Note: The above bits determine if DMA bandwidth is improved for the specified channel. If enabled, bandwidth improvement is accomplished by reducing the transaction latency between the DMA Controller and the LPC Bus Controller.

Offset Address: 5Bh (D17F0)

Miscellaneous Control **Default Value: 41h**

Bit	Attribute	Default	Description
7	RW	0	**LPC Firmware Memory Read TRDY 1 Wait State** 0: Disable 1: Enable
6	RW	1b	**Destination Selection of IO Port 0x80** The Function with Rx46[5] are LPC_Rx5B[6], LPC_Rx46[5]: 0X: IO Port 0x80 goes to ISA bus. 10: IO Port 0x80 goes to LPC bus. 11: IO Port 0x80 goes to SPI bus.
5	RW	0	**PCI/DMA Memory Cycles Output to PCI Bus** 0: Disable 1: Enable
4	RW	0	**APIC Clock Gating Enable** 0: Disable 1: Enable
3	RW	0	**Bypass APIC De-Assert Message** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	1b	**Dynamic Clock Stop** 0: Disable 1: Enable

Programmable Chip Select (PCS) Control (5C-67h)

Offset Address: 5D-5Ch (D17F0)

PCS 0 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 0 I/O Port Address**

Offset Address: 5F-5Eh (D17F0)

PCS 1 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 1 I/O Port Address**

Offset Address: 61-60h (D17F0)

PCS 2 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 2 I/O Port Address**

Offset Address: 63-62h (D17F0)

PCS 3 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 3 I/O Port Address**

Offset Address: 65-64h (D17F0)

PCS I/O Port Address Mask **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0000b	**PCS 3 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
11:8	RW	0000b	**PCS 2 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
7:4	RW	0000b	**PCS 1 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
3:0	RW	0000b	**PCS 0 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.

Offset Address: 66h (D17F0)

PCS Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**PCS 3** 0: Disable 1: Enable
2	RW	0	**PCS 2** 0: Disable 1: Enable
1	RW	0	**PCS 1** 0: Disable 1: Enable
0	RW	0	**PCS 0** 0: Disable 1: Enable

Offset Address: 67h (D17F0)

Output and PCS Control **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**PCS 3 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
6	RW	0	**PCS 2 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
5	RW	0	**PCS 1 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
4	RW	0	**PCS 0 IO Cycle is Directed to** 0: Internal ISA Bus 1: LPC Bus
3	RW1C	0	**SPI external interrupt status** 0: No interrupt 1: Interrupt pending
2	RW	1b	**FERR# Voltage** 0: 2.5V 1: 1.5V
1:0	RW	00b	**Reserved**

Note: PCS IO cycle can be claimed in two ways:
1. Positive decoding: Set Rx58[4] and the corresponding bits in Rx6C[1:0] and Rx6F[5] to 1, and program the PCS address range.
2. Subtractive decoding: Program the PCS address range.

High Precision Event Timers (HPET) (68-6Bh)

Offset Address: 68h (D17F0)

HPET Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Precision Event Timers** 0: Disable 1: Enable
6:4	RW	0	**Reserved**
3	RW	0	**PCS 3 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
2	RW	0	**PCS 2 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
1	RW	0	**PCS 1 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
0	RW	0	**PCS 0 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable

Offset Address: 6B-69h (D17F0)

HPET Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:2	RW	0	**HPET Memory Base Address [31:10]**
1:0	RW	0	**Reserved**

ISA Decoding Control (6C-73h)

Offset Address: 6Ch (D17F0)

ISA Positive Decoding Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**On-board I/O (Ports 00-FFh) Positive Decoding** 0: Disable 1: Enable
6	RW	0	**Microsoft Sound System I/O Port Positive Decoding** 0: Disable 1: Enable (bits [5:4] determine the decode range)
5:4	RW	00b	**Microsoft Sound System I/O Decode Range** 00: 0530h-0537h 01: 0604h-060Bh 10: 0E80h-0E87h 11: 0F40h-0F47h
3	RW	0	**APIC Positive Decoding** 0: Disable 1: Enable
2	RW	0	**ROM Positive Decoding** 0: Disable 1: Enable
1	RW	0	**PCS1# Positive Decoding** 0: Disable 1: Enable
0	RW	0	**PCS0# Positive Decoding** 0: Disable 1: Enable

Offset Address: 6Dh (D17F0)

ISA Positive Decoding Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FDC Positive Decoding** 0: Disable 1: Enable
6	RW	0	**LPT Positive Decoding** 0: Disable 1: Enable
5:4	RW	00b	**LPT Decode Range** 00: 3BCh-3BFh, 7BCh-7BEh 01: 378h-37Fh, 778h-77Ah 10: 278h-27Fh, 678h-67Ah 11: Reserved
3	RW	0	**Game Port Positive Decoding** 0: Disable 1: Enable
2	RW	0	**MIDI Positive Decoding** 0: Disable 1: Enable
1:0	RW	00b	**MIDI Decode Range** 00: 300h-303h 01: 310h-313h 10: 320h-323h 11: 330h-333h

Offset Address: 6Eh (D17F0)

Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Reserved**
1	RW	0	**Use New SPI Hit Mechanism** 0: Disable 1: Enable
0	RW	0	**Control the Destination of IO Port 68/6C/6A/6Eh** 0: Go to ISA bus 1: Go to LPC bus

Offset Address: 6Fh (D17F0)

ISA Positive Decoding Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SPI Positive Decoding Control** 0: Disable 1: Enable
6	RW	0	**LPC TPM Positive Decoding** 0: Disable 1: Enable
5	RW	0	**PCS2# and PCS3# Positive Decoding** 0: Disable 1: Enable
4	RW	0	**I/O Port 0CF9h Positive Decoding** 0: Disable 1: Enable
3	RW	0	**Floppy Disk Controller (FDC) Decoding Range** 0: Primary 1: Secondary
2	RW	0	**Sound Blaster Positive Decoding** 0: Disable 1: Enable
1:0	RW	00b	**Sound Blaster Decode Range** 00: 220-22F, 230-233h 01: 240-24F, 250-253h 10: 260-26F, 270-273h, 11: 280-28F, 290-293h

Offset Address: 71-70h (D17F0)

Subsystem Vendor ID Backdoor Registers **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	**Subsystem Vendor ID (Rx2D-2C) Back Door**

Offset Address: 73-72h (D17F0)

Subsystem ID Backdoor Registers **Default Value: 8410h**

Bit	Attribute	Default	Description
15:0	RW	8410h	**Subsystem ID (Rx2F-2E) Back Door**

PCI I/O Cycle Control (74-7Fh)

Offset Address: 74h (D17F0) – Reserved

Offset Address: 75h (D17F0)
LPC ROM Memory Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for All Memory Range** Used when Rx4D[1] is 1 and Rx4D[4] is 0.
3	RW	0	**Select LPC ROM Memory Address Range 1 {FF700000h-FF7FFFFFh, FF300000h-FF3FFFFFh}** 0: Not select 1: Select
2	RW	0	**Select LPC ROM Memory Address Range 2 {FF600000h-FF6FFFFFh, FF200000h-FF2FFFFFh}** 0: Not select 1: Select
1	RW	0	**Select LPC ROM Memory Address Range 3 {FF500000h-FF5FFFFFh, FF100000h-FF1FFFFFh}** 0: Not select 1: Select
0	RW	0	**Select LPC ROM Memory Address Range 4 {FF400000h-FF4FFFFFh, FF000000h-FF0FFFFFh}** 0: Not select 1: Select

Offset Address: 76h (D17F0)
Firmware Memory IDSEL 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF500000h-FF5FFFFFh, FF100000h-FF1FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF400000h-FF4FFFFFh, FF000000h-FF0FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 77h (D17F0)
Firmware Memory IDSEL 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF700000h-FF7FFFFFh, FF300000h-FF3FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF600000h-FF6FFFFFh, FF200000h-FF2FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 78-7Bh (D17F0) – Reserved

Offset Address: 7Ch (D17F0)
Firmware Memory IDSEL 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFC80000h-FFCFFFFFh, FF880000h-FF8FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFC00000h-FFC7FFFFh, FF800000h-FF87FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Dh (D17F0)
Firmware Memory IDSEL 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFD80000h-FFDFFFFFh, FF980000h-FF9FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFD00000h-FFD7FFFFh, FF900000h-FF97FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Eh (D17F0)
Firmware Memory IDSEL 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFE80000h-FFEFFFFFh, FFA80000h-FFAFFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000b	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFE00000h-FFE7FFFFh, FFA00000h-FFA7FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Fh (D17F0)
Firmware Memory IDSEL 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges { FFB80000h-FFBFFFFFh, 000E0000h-000FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFF00000h-FFF7FFFFh, FFB00000h-FFB7FFFFh }** 0000: IDSEL0 … 1111: IDSEL15

Power Management-Specific Configuration Registers (80-AFh)

Offset Address: 80h (D17F0)

PM General Configuration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Enable GPIO12 as SLPBTN#** 0: Disable 1: Enable
5	RW	0	**Power Button De-bounce** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	0	**Enable Microsoft Sound Monitor in Audio Access** This access means an I/O cycle to the sound port as specified in D17F0 Rx6C[5:4]. 0: Disable 1: Enable
2	RW	0	**Enable Game Port Monitor in Audio Access** This access means an I/O cycle to the game port: 200h-207h. 0: Disable 1: Enable
1	RW	0	**Enable Sound Blaster Monitor in Audio Access** This access means an I/O cycle to the sound blaster port as specified in D17F0 Rx6F[1:0] or 388h-38Bh. 0: Disable 1: Enable
0	RW	0	**Enable MIDI Monitor in Audio Access** This access means an I/O cycle to the midi port as specified in D17F0 Rx6D[1:0]. 0: Disable 1: Enable

Offset Address: 81h (D17F0)

PM General Configuration 2 **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**Enable ACPI I/O** 0: Disable access to ACPI I/O block 1: Allow access to Power Management I/O register block (See Rx89-88h to set the base address for this register block). Please refer to section "Power Management I/O Space" for register descriptions.
6:4	RW	0	**Reserved**
3	RW	0	**ACPI Timer with 32-Bit Width Control** 0: ACPI timer counts with 24-bit width. 1: ACPI timer counts with 32-bit width.
2	RW	1b	**Enable RTC Control Signal Gated with PSON (SUSC#) in Soft-Off Mode** 0: Disable 1: Enable This is to prevent CMOS and Power-Well register data from being corrupted during system on/off when the RTC control signal (PWRGD) may not be stable.
1	RW	0	**Throttle Timer Base Clock Period (for STPCLK#)** This bit controls the timer tick base for the throttle timer. 0: 30 usec (480 usec cycle time when using a 4-bit timer) 1: 1 msec (16 msec cycle time when using a 4-bit timer) The timer tick base can be further lowered to 7.5 usec (120 usec cycle time when using a 4-bit timer) by setting Rx8D[4] = 1. When Rx8D[4] = 1, the setting of this bit is ignored.
0	RW	0	**Reserved**

Offset Address: 82h (D17F0)

ACPI Interrupt Select **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**ATX / AT Power Indicator** 0: ATX 1: AT
6	RO	1b	**PSON (SUSC#) Current State** 0: PSON gating active 1: PSON Gating Complete During system on/off, this status bit reports whether PSON gating state has been completed. 0 means that gating is active now; 1 means that gating is complete. Software should not access any CMOS or Power-Well registers until this bit becomes 1 if Rx81[2] = 1.
5	RW	0	**Reserved**
4	RO	1b	**SUSC# AC-Power-On Default** This bit reflects the value of RTC Index 0D bit-7. If this bit is 0, the system is configured to "default on" when power is connected.
3:0	RW	0000b	**ACPI IRQ Select** This field determines the routing of the ACPI IRQ. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: IRQ15

Offset Address: 83h (D17F0)

Internal Timer Read Test **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Internal Timer Read Test**

Offset Address: 85-84h (D17F0)

IRQn as Primary Interrupt **Default Value: 0000h**

If an IRQ is enabled as a Primary IRQ, its assertion can be used as a wakeup event in system power management. This register is used in conjunction with:

- PMIO Rx28[7] – Primary Resume Status
- PMIO Rx2A[7] – Primary Resume Enable

If a device's IRQ is enabled as a Primary Interrupt, once the device asserts the IRQ, the PMIO Rx28[7] status bit will be set to 1 to report the occurrence of the Primary IRQ. If PMIO Rx2A[7] is set to 1 to enable the Resume-on-Primary-IRQ function, the IRQ becomes a wakeup event.

Bit	Attribute	Default	Description
15	RW	0	**IRQ15 as Primary Interrupt Channel** 0: Disable 1: Enable
14	RW	0	**IRQ14 as Primary Interrupt Channel** 0: Disable 1: Enable
13	RW	0	**IRQ13 as Primary Interrupt Channel** 0: Disable 1: Enable
12	RW	0	**IRQ12 as Primary Interrupt Channel** 0: Disable 1: Enable
11	RW	0	**IRQ11 as Primary Interrupt Channel** 0: Disable 1: Enable
10	RW	0	**IRQ10 as Primary Interrupt Channel** 0: Disable 1: Enable
9	RW	0	**IRQ9 as Primary Interrupt Channel** 0: Disable 1: Enable
8	RW	0	**IRQ8 as Primary Interrupt Channel** 0: Disable 1: Enable
7	RW	0	**IRQ7 as Primary Interrupt Channel** 0: Disable 1: Enable
6	RW	0	**IRQ6 as Primary Interrupt Channel** 0: Disable 1: Enable
5	RW	0	**IRQ5 as Primary Interrupt Channel** 0: Disable 1: Enable
4	RW	0	**IRQ4 as Primary Interrupt Channel** 0: Disable 1: Enable
3	RW	0	**IRQ3 as Primary Interrupt Channel** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	0	**IRQ1 as Primary Interrupt Channel** 0: Disable 1: Enable
0	RW	0	**IRQ0 as Primary Interrupt Channel** 0: Disable 1: Enable

Offset Address: 87-86h (D17F0)

IRQn as Secondary Interrupt **Default Value: 0000h**

This register is used in conjunction with:

- PMIO Rx28[1] – Secondary Event Timer Timeout Status
- PMIO Rx2A[1] – SMI on Secondary Event Timer Timeout

Secondary IRQ is different from Primary IRQ in systems that resume due to a Secondary IRQ event can return to the suspend state after the secondary event timer times out. For this to work, PMIO Rx2A[1] needs to be set to one to enable SMI-on-Secondary-Event-Timer-Timeout (when PMIO Rx28[1] = 1). The timer's count value can be set via Rx90[27:26].

Bit	Attribute	Default	Description
15	RW	0	**IRQ15 as Secondary Interrupt Channel** 0: Disable 1:Enable
14	RW	0	**IRQ14 as Secondary Interrupt Channel** 0: Disable 1:Enable
13	RW	0	**IRQ13 as Secondary Interrupt Channel** 0: Disable 1:Enable
12	RW	0	**IRQ12 as Secondary Interrupt Channel** 0: Disable 1:Enable
11	RW	0	**IRQ11 as Secondary Interrupt Channel** 0: Disable 1:Enable
10	RW	0	**IRQ10 as Secondary Interrupt Channel** 0: Disable 1:Enable
9	RW	0	**IRQ9 as Secondary Interrupt Channel** 0: Disable 1:Enable
8	RW	0	**IRQ8 as Secondary Interrupt Channel** 0: Disable 1:Enable
7	RW	0	**IRQ7 as Secondary Interrupt Channel** 0: Disable 1:Enable
6	RW	0	**IRQ6 as Secondary Interrupt Channel** 0: Disable 1:Enable
5	RW	0	**IRQ5 as Secondary Interrupt Channel** 0: Disable 1:Enable
4	RW	0	**IRQ4 as Secondary Interrupt Channel** 0: Disable 1:Enable
3	RW	0	**IRQ3 as Secondary Interrupt Channel** 0: Disable 1:Enable
2	RW	0	**Reserved** Always reads 0.
1	RW	0	**IRQ1 as Secondary Interrupt Channel** 0: Disable 1:Enable
0	RW	0	**IRQ0 as Secondary Interrupt Channel** 0: Disable 1:Enable

Offset Address: 89-88h (D17F0)

Power Management I/O Base **Default Value: 0001h**

Bit	Attribute	Default	Description
15:7	RW	0	**ACPI IO Base [15:7]**
6:0	RO	01h	**Hardwired to 01h**

Offset Address: 8Ah (D17F0)

Auto-Switching Processor Power State **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Slow C4 Recovery Mode in Short C4 Setting** 0: Normal entry and recovery latencies 1: Slow recovery latencies When enabled with short C4 setting fast, slow recovery latencies of C3/C4 state are performed. In detail, please refer to C3/C4 latency configuration tables.
6	RW	0	**Enable Special STPGNT (Disable Snoop) to Enter C5 State** 0: Disable special STPGNT to enter C5 state 1: Enable special STPGNT to enter C5 state. If chipset receive special STPNGT (disable snoop), chipset will enter C5 state even if CPU sends C2/3/4 command.
5	RW	0	**Enable C5 / C6 State** 0: Disable C5 / C6 state 1: Enable C5 / C6 state
4	RW	0	**C2 to C3 / C4 Auto Mode** 0: Not automatically switch from C2 to C3 or C4 state 1: In C2 state, if no bus master activity after a period of time, it will return to C3 or C4 state. This bit is used in conjunction with bit 3. If bit 3 is 0, this bit must be 0.
3	RW	0	**C3/C4 to C2 Auto Mode** 0: When bus master request is treated as a break event, the processor power state will switch from C3/C4 to C0. 1: When bus master request asserted, the processor power state will switch from C3/C4 to C2 and automatically enable the bus arbiter, so that snooping and memory access could be processed correctly.
2	RW	0	**Bus Master Status Report Disable** 0: PMIO Rx00[4] is set when there is bus master activity. 1: PMIO Rx00[4] is not set by bus master activity. Must set this bit when bit 3 is set. PMIO Rx00[4] will be set by LPC DMA or LPC masters even if this bit is set.
1	RW	0	**C4 to C3 Auto Mode** 0: Disable, when entering C4 state, even if bus master request occurs before VRDSLP assertion, the processor will enter C4 state. 1: Enable, when entering C4 state, if bus master request occurs before VRDSLP assertion, the C4 state transition will be aborted and the processor will stay in C3 state.
0	RW	0	**Bus Master Request Delay C3/C4 Mode** 0: Disable 1: Enable ***If disabled:*** When entering C3/C4 state, if bus master request occurs before SLP# assertion, the processor will enter C3/C4 without waiting. ***If enabled:*** When entering C3/C4 state, if bus master request occurs before SLP# assertion, the processor will stay in C2 state and then enter C3/C4 state when bus master request is finished.

Offset Address: 8Bh (D17F0) – Reserved

Offset Address: 8Ch (D17F0)

Host Power Management Control **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Thermal Duty Cycle** This field determines STPCLK# duty cycle when the THRM# signal is asserted. The duty cycle of STPCLK#, if not activated by the assertion of THRM#, is controlled by PMIO Rx10[3:0]. The duty cycle indicates the percentage of host bus activation (the lower the percentage, the lower the performance and the higher the power savings). If the Throttling Timer Width (Rx8D[6:5]) is set to 3-bit width, bit 0 of this field should be set to 0 (and the performance increment is in unit of 12.5%). If the Throttling Timer Width is set to 2-bit width, bits [1:0] of this field should be set to 0 (and the performance increment is in unit of 25%). **Throttling Timer Width**
3	RW	0	**THRM# Enable** 0: Disable 1: Enable
2	RW	1b	**Processor Break Events** 0: Disable 1: Enable Allows processor break events, such as FERR#, to wake up processor from C1/C2/C3/C4 to C0.
1	RW	1b	**Disable Bus Arbiter C3/C4 Auto Gating** 0: Bus arbiter is auto-disabled when processor state is switched to C3/C4 state. 1: Disable the bus arbiter auto-disabled mode. The arbiter is disabled through IO Port 22h.
0	RW	1b	**Reserved (Do Not Program)**

	4-Bit	3-Bit	2-Bit
0000	-	-	-
0001	6.25%	-	-
0010	12.50%	12.50%	-
0011	18.75%	-	-
0100	25.00%	25.00%	25.00%
0101	31.25%	-	-
0110	37.50%	37.50%	-
0111	43.75%	-	-
1000	50.00%	50.00%	50.00%
1001	56.25%	-	-
1010	62.50%	62.50%	-
1011	68.75%	-	-
1100	75.00%	75.00%	75.00%
1101	81.25%	-	-
1110	87.50%	87.50%	-
1111	93.75%	-	-

Offset Address: 8Dh (D17F0)

Throttle / Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Throttle Timer Reset** Write 1 to reset the throttle timer.
6:5	RW	00b	**Throttle Timer Counter Width** 0x: 4-Bit 10: 3-Bit 11: 2-Bit (See also Rx8C[7:4] and PMIO Rx10[3:0].) This field determines the counter width of the throttle timer, which in conjunction with the throttle timer tick determines the cycle time of STPCLK#. For example, if a 2-bit timer and a 7.5 usec timer tick are selected, the STPCLK# cycle time would be 30 usec (2**2 x 7.5). If a 4-bit timer and a 7.5 usec timer tick is selected, the cycle time would be 120 usec (2**4 x 7.5).
4	RW	0	**Use Fast Clock (7.5us) as Throttle Timer Tick** 0: Timer tick is selected by Rx81[1]. 1: Timer tick is 7.5usec (setting of Rx81[1] is ignored).
3	RW	0	**SMI# Low Level Output** 0: Disable 1: Enable; during an SMI event, SMI# is held low until SMI event status is cleared
2	RW	0	**Reserved**
1	RW	0	**Internal Clock Stops During C3/C4** This bit controls whether the internal PCI clock stops during C3/C4 state. 0: PCI clock does not stop 1: PCI clock stops
0	RW	0	**Internal Clock Stops During Suspend** This bit controls whether the internal PCI clock stops during suspend state. 0: PCI clock does not stop 1: PCI clock stops

Offset Address: 8E-8Fh (D17F0) – Reserved

Offset Address: 93-90h (D17F0)

Power Management Timer Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	00b	**Power Conserve Mode Timer Period** 00: 1/16 second 01: 1/8 second 10: 1 second 11: 1 minute
29	RW1C	0	**Power Conserve Mode Status** This bit reads 1 when in Conserve Mode
28	RW	0	**Power Conserve Mode** This bit controls whether conserve mode (through throttling) is enabled. 0: Disable 1: Enable When this bit is set, the system can enter conserve mode when primary activity is not detected within a given time period (determined by bits [31:30]). Primary activity is defined in PMIO Rx33-30.
27:26	RW	00b	**Secondary Event Timer Count Value** 00: 2 milliseconds 01: 64 milliseconds 10: 1/2 second 11: by EOI + 0.25 milliseconds
25	RW1C	0	**Secondary Event Occurred Status** This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.
24	RW	0	**Secondary Event Timer Enable** 0: Disable 1: Enable
23:16	RW	0	**GP1 Timer Count Value** Unit defined by bits [5:4]. Write to load count value; read to get current count. The value needs to plus 1 when programmed to load the count value. For example, 05h should be written here if 4 timer ticks are expected.
15:8	RW	0	**GP0 Timer Count Value** Base defined by bits [1:0]. Write to load count value; read to get current count. The value needs to plus 1 when programmed to load the count value. For example, 05h should be written here if 4 timer ticks are expected.
7	RW	0	**GP1 Timer Enable** 0: Disable 1: Enable When this bit is set, the GP1 timer loads the value defined in bits [23:16] and starts counting down. The GP1 timer will be reloaded at the occurrence of peripheral events that are enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit PMIO Rx28[3] is set to one. Additionally, if the GP1 Timer Timeout Enable bit PMIO Rx2A[3] is set, an SMI is generated.
6	RW	0	**GP1 Timer Automatic Reload** 0: GP1 timer stops at 0. 1: Reload GP1 timer automatically after counting down to 0.
5:4	RW	00b	**GP1 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute
3	RW	0	**GP0 Timer Start** 0: Disable 1: Enable When this bit is set, the GP0 timer loads the value defined by bits [15:8] and starts counting down. The GP0 timer is reloaded at the occurrence of peripheral events that are enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit PMIO Rx28[2] is set to one. Additionally, if the GP0 Timer Timeout Enable bit PMIO Rx2A[2] is set, an SMI is generated.
2	RW	0	**GP0 Timer Automatic Reload** 0: GP0 Timer stops at 0 1: Reload GP0 timer automatically after counting down to 0.
1:0	RW	00b	**GP0 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute

Offset Address: 94h (D17F0)

Miscellaneous Configuration 1 (Power Well) **Default Value: 88h**

Bit	Attribute	Default	Description
7	RW	1b	**SMBus Clock Select** 0: From divider of 14.318 Mhz 1: From RTC clock If set, SMBus always uses RTC clock. If not set, SMBus uses RTC clock in suspend mode and uses 128K when RxD2[2] is set.
6	RW	0	**Check Power Button Enable When PWRBTN# Asserted to Resume from STR / STD** 0: Not check 1: Check Power Button Enable is controlled through register ACPI I/O Space Rx03[0].
5	RW	0	**Reserved**
4	RW	0	**KBC D2 Command Interrupt Gating** 0: Disable 1: Enable
3	RW	1b	**Pull up Pad of Card Reader / SDIO Power Switch** 0: Disable 1: Enable
2	RW	0	**Multi-Function Signal Select: GPO[9:8] vs. SUS[C:B]#** 0: SUS[C:B]# 1: GPO[9:8]
1:0	RW	00b	**GPO7 Output Select** This field controls the GPO7 output signal for Pulse Width Modulation. 00: Fixed output port (output value is defined by PMIO Rx4C[7]). 01: GPO7 output is 1 Hz slow clock rate. 10: GPO7 output is 4 Hz slow clock rate. 11: GPO7 output is 16 Hz slow clock rate. Note: The register setting only works when D17F0 Rx9B[4] = 1

Offset Address: 95h (D17F0)

Miscellaneous Configuration 2 (Power Well) **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**SUS[A:C]# to CPUSTP# and CPUSTP# to NM PLL Resume Delay Select** This bit controls the following two minimum delays of the resume process: (A) De-assertion of SUS[A:C]# to the de-assertion of CPUSTP#. (B) De-assertion of CPUSTP# to NM PLL start. 0: (A) 16 msec, (B) 1 msec 1: (A) 1 msec, (B) 125 usec
6	RW	1b	**Start NM PLL Before PWRGD when Resume from STD** 0: Disable 1: Enable
5	RW	0	**Keyboard / Mouse Port Swap** This bit determines whether the keyboard and mouse ports can be swapped. 0: Disable 1: Enable
4	RW	0	**PWRGD Reset** This bit is used to disable chipset PWRGD input. 0: Normal 1: PWRGD input has no effect
3	RW	0	**Multi-Function Signal Select: SMBDT2, SMBCK2 vs. GPIO0, GPIO1** 0: SMBDT2, SMBCK2 1: GPIO0, GPIO1
2	RW	0	**AOL 2 SMB Slave (through SMB Port 2)** This bit controls whether external SMB masters can access internal SMB registers (for Alert-On-LAN). 0: Enable 1: Disable
1	RW	0	**Multi-Function Signal Select: GPO7 vs. SUSA#** 0: SUSA# 1: GPO7
0	RW	0	**USB Wakeup for POS / STR / STD** This bit controls whether USB device wakeup is enabled when PMIO Rx20[14]=1. It allows system wakeup from POS / STR / STD state when OS (or BIOS) turns on USB device remote wakeup feature and the system software enables USB wakeup register (PMIO Rx22[14]=1) also. 0: Disable 1: Enable

Offset Address: 96h (D17F0)

Miscellaneous Configuration 3 (Battery Well) **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RW	0	**Reserved**
4	RW	0	**Enable SMB GPOUT6 and GPOUT7 as PWRGD and PWRBTN#** 0: Disable 1: Enable Enable ASF function. Used by Alert-on-LAN to reset the system.
3:0	RW	Fh	**Reserved**

Offset Address: 97h (D17F0)

Miscellaneous Configuration 3 (Power Well) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Wait for PWRGD Low Before Wake-up during S3/S4 State** 0: Not wait 1: Wait
6	RW	0	**Multi-Function Signal Select: (MSDT, MSCK) vs. (GPIO2, GPIO3)** 0: (MSDT, MSCK) 1: (GPIO2, GPIO3)
5	RW	0	**Reserved**
4	RW	0	**Enable PCIe PME S1 State Wake Event** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**Disable PWRBTN Pull-up** 0: Enable 1: Disable (not pull up)
1	RW	0	**Reserved**
0	RW	0	**Multi-Function Signal Select: (KBDT, KBCK) / (KBC_CPURST#, A20GATE) vs. (GPIO4, GPIO5)** 0: (KBDT, KBCK) or (KBC_CPURST#, A20GATE) 1: (GPIO4, GPIO5)

Offset Address: 98h (D17F0)

GP2 / GP3 Timer Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**GP3 Timer Start** 0: Disable 1: Enable When this bit is set, the GP3 timer loads the value specified by Rx9A and starts counting down. The GP3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP3 timer counts down to zero, then the GP3 Timer Timeout Status bit PMIO Rx28[13] is set to one, a SMI will be asserted if the GP3 Timer Timeout Enable bit PMIO Rx2A[13] is set.
6	RW	0	**GP3 Timer Automatic Reload** 0: GP3 timer stops at 0. 1: Reload GP3 timer automatically after counting down to 0.
5:4	RW	01b	**GP3 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute
3	RW	0	**GP2 Timer Start** 0: Disable 1: Enable When this bit is set, the GP2 timer loads the value specified by Rx99 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx 38). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit PMIO Rx28[12] is set to one, a SMI will be asserted if the GP2 Timer Timeout Enable bit PMIO Rx2A[12] is set.
2	RW	0	**GP2 Timer Automatic Reload** 0: GP2 timer stops at 0. 1: Reload GP2 timer automatically after counting down to 0.
1:0	RW	00b	**GP2 Timer Tick Select** 00: Disable 01: 1 ms 10: 1 second 11: 1 minute

Offset Address: 99h (D17F0)
GP2 Timer Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI2 Timer Counter** Write will set GP2 timer load value. Read will get GP2 timer current count. The value needs to plus 1 when programmed to load the count value. For example, 05h should be written here if 4 timer ticks are expected.

Offset Address: 9Ah (D17F0)
GP3 Timer Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI3 Timer Counter** Write will set GP3 timer load value. Read will get GP3 timer current count. The value needs to plus 1 when programmed to load the count value. For example, 05h should be written here if 4 timer ticks are expected.

Offset Address: 9Bh (D17F0)
Boot Option Bit Mask (ASF) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Lock Sleep Button** To lock sleep button means SLPBTN# is always de-asserted. 0: Disable 1: Enable
5	RW	0	**Lock Keyboard Controller Access** 0: Enable 1: Disable
4	RW	0	**GPIO7 Multi-Function Select** 0: Output suspend power internal 32K clock 1: GPIO7
3	RW	0	**USB Device Mode Wakeup for POS / STR / STD / Soft Off** This bit controls whether USB device mode wakeup is enabled. This allows wakeup from STR, STD, Soft Off and POS. 0: Disable 1: Enable
2	RW	0	**Lock Reset Button** To lock reset button means Reset button is always de-asserted. 0: Disable 1: Enable
1	RW	0	**Lock Power Button** To lock power button means PWRBTN# button is always de-asserted. 0: Disable 1: Enable
0	RW	0	**Multi-Function Signal Select: (CR_PWSEL, CR_PWOFF) vs. (GPO11, GPO12)** 0: (CR_PWSEL, CR_PWOFF) 1: (GPO11, GPO12)

Offset Address: 9Ch (D17F0)
ASF Byte Write Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Command Decode Table** 00h: Reserved 01h: Generate ASF wakeup event and SCI or SMI event. PMIO Rx3A[0]: SCI enable, PMIO Rx3B[0]: SMI enable. 02h: Unconditional Power Down 03h: System Reset 04h: Power Cycle Reset 05h: Reserved 06h: Watch Dog Timer Reload 07h: Reserved

Offset Address: 9Dh (D17F0)

ASF Data Message1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**ASF Data Message 1**

Offset Address: 9Eh (D17F0)

ASF Data Message 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**ASF Data Message 2**

Offset Address: 9Fh (D17F0)

CR / SDIO Voltage Change Function **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**KB/MS and SMBALRT_ PAD Pull-up Select** 0: Not pull-up 1: Pull-up
6	RW	0	**SMB Bus Collision Monitor Enable** 0: Disable 1: Enable
5	RW	0	**New SMB Device Switch** 0: New SMBus Device 1: Old SMBus Device
4:3	RW	00b	**CR/SDIO Pads Power up Delay Select** 00: Bypass mode 01: 1 ms 10: 0.5 ms 11: 30 ms
2	RW	0	**Select SDIO or CR to Serve SD/MMC Card** 0: SDIO 1:CR
1:0	RW	00b	**SMB Slave Debounce Mode Select** 00: Bypass mode 01: Slave debounce mode1 10: Slave debounce mode2 11: Slave debounce mode3

Offset Address: A0-AFh (D17F0) – Reserved

PCI UART Control Registers (B0-FFh)

Offset Address: B0h (D17F0)

APIC C4P State Mode Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**UART Multiplex with DVP or VCP Pad** Must set Rx46[6] to enable this function, if UART is disabled, neither DVP nor VCP pad is used 0: Multiplex with VCP pad when UART enabled 1: Multiplex with DVP pad when UART enabled
6:4	RW	0	**Reserved**
3	RW	1b	**APIC C4P State Mode Control** 0: APIC will switch to use PCICLK in C4P state, and APICPME is not supported 1: APIC uses the clock from PLL, and support APCIPME to wakeup PMU from C4P
2:0	RW	0	**Reserved**

Offset Address: B1h (D17F0)

PCI UART IRQ Routing - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI UART 3 IRQ Routing** Refer to Table 43 PnP IRQ Routing Table
3:0	RW	0	**PCI UART 2 IRQ Routing** Refer to Table 43 PnP IRQ Routing Table

Offset Address: B2h (D17F0)

PCI UART IRQ Routing - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI UART 1 IRQ Routing** Refer to Table 43 PnP IRQ Routing Table
3:0	RW	0	**PCI UART 0 IRQ Routing** Refer to Table 43 PnP IRQ Routing Table

Offset Address: B3h (D17F0)

PCI UART 0 I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCI UART 0 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**PCI UART 0 I/O Base Address [9:3]**

Offset Address: B4h (D17F0)

PCI UART 1 I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCI UART 1 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**PCI UART 1 I/O Base Address [9:3]**

Offset Address: B5h (D17F0)

PCI UART 2 I/O base address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCI UART 2 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**PCI UART 2 I/O Base Address [9:3]**

Offset Address: B6h (D17F0)
PCI UART 3 I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCI UART 3 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**PCI UART 3 I/O Base Address [9:3]**

Offset Address: B7-BBh (D17F0) – Reserved

Offset Address: BE-BCh (D17F0)
MMIO Space Base Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:4	RW	0	**MMIO Space Base Address [31:12]**
3:0	RO	0	**Reserved**

Offset Address: BD-FFh (D17F0) – Reserved

Offset Address: C3-C0h (D17F0)
Power Management Capability **Default Value: 0002 0001h**

Bit	Attribute	Default	Description
31:16	RO	0002h	**Power Management Capability** 0002h indicates following capabilities: This function does not support D2 or D1 power state. This function does not require PCI clock to generate PME#. This function complies with PCI Power Management Interface Specification Revision 1.1.
15:8	RO	0	**Next Pointer** 0 indicates that there are no additional items in the Capabilities List.
7:0	RO	01h	**Capability ID**

Offset Address: C7-C4h (D17F0)
Power Management Capability **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Capability Data**
23:16	RO	0	**PM CSR (Certificate Signing Request) P2P Support Extensions**
15:2	RO	0	**PM Control / Status (D0/D3 Only) High**
1:0	RW	00b	**PM Control / Status (D0/D3 Only) Low** 00: D0 11: D3 Others: Reserved

Offset Address: C8-FFh (D17F0) – Reserved

System Management Bus-Specific Configuration Registers (D0-E7h)

Offset Address: D1-D0h (D17F0)

SMBus I/O Base **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**SMBus I/O Base [15:4] (16-byte I/O space)**
3:0	RO	1h	**Hardwire to 01h**

Offset Address: D2h (D17F0)

SMBus Host Configuration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**SMBus Alert IRQ SCI / SMI Select** 0: SMI 1: SCI
2	RW	0	**SMBus Clock from 128K Source** Divider from 14.318Mhz 0: 33.14 KHz 1: 132.57 KHz
1	RW	0	**Enable SMBus IRQ** 0: Disable 1: Enable
0	RW	0	**Enable SMBus Host Controller** 0: Disable 1: Enable

Offset Address: D3h (D17F0)

SMBus Host Slave Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Host Slave Command**

Offset Address: D4h (D17F0)

SMBus Slave Address for Port 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Slave Address [7:1] for Port 1**
0	RW	0	**Read / Write for Shadow Port 1** 0: Read 1: Write

Offset Address: D5h (D17F0)

SMBus Slave Address for Port 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Slave Address [7:1] for Port 2**
0	RW	0	**Read / Write for Shadow Port 2** 0: Read 1: Write

Offset Address: D6h (D17F0)

SMBus Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**SMBus Revision ID**

Offset Address: D7-DFh (D17F0) – Reserved

Offset Address: E0h (D17F0)
GPI Trigger Level for SCI / SMI Generation **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI Input Trigger Mode for SCI/SMI Generation** Bit 7: GPI13 (Not used in this product) Bit 6: GPI12 (Not used in this product) Bit 5: GPIO11 Bit 4: GPIO10 Bit 3: GPIO1 Bit 2: GPIO0 Bit 1: GPI1 Bit 0: GPI14 0: Falling edge 1: Rising edge

Offset Address: E1h (D17F0)
GPI SCI / SMI Select **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI SCI / SMI Select** Bit [7:6]: GPI [13:12] (Not used in this product) Bit [5:2]: GPIO[11:10, 1:0] Bit 1: GPI1 Bit 0: GPI14 0: SCI 1: SMI

Offset Address: E2h (D17F0)
Internal NM PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Inhibit C4 State During USB Isochronous Transaction** 0: Disable 1: Enable
6:3	RW	0	**Reserved**
2	RW	0	**Enable Internal Hot Plug to Generate SCI/SMI** 0: Disable 1: Enable
1	RW	0	**Enable Internal PM_PME to Generate SCI/SMI** 0: Disable 1: Enable
0	RW	0	**Inhibit C3/C4 State When HD Audio Transfers Big Format Data** 0: Disable 1: Enable

Offset Address: E3h (D17F0)
Pull-up Option **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**SPI Bus Master as Break Event** 0: Disable 1: Enable
6	RW	0	**VR Change Timer Select** 0: 7.5 us 1: 45us
5:4	RW	0	**Reserved**
3	RW	0	**Enable VART Break Event** 0: Disable 1: Enable
2	RW	0	**PCIe Hot Plug Wakeup in S1 State** 0: Not supported 1: Supported
1	RW	1b	**Pull-Up Enable for IO Pads (INTR, IGNNE#, A20M#, SMI#, INIT#, FERR#, NMI#)** 0: Disable 1: Enable
0	RW	1b	**Pull-Up Enable for IO Pads (THRMTRIP#, NAP#, DPSLP#, STPCLK#, SLP#)** 0: Disable 1: Enable

Offset Address: E4h (D17F0)

Multi-Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Short C3/C4 Mode** When this bit is enabled, fast entry and recovery latencies of C3/C4 state are performed. In detail, please refer to C3/C4 latency configuration tables. 0: Normal entry and recovery latencies 1: Fast entry and recovery latencies
6	RW	0	**Multi-Function Signal Select: SYSIDLE vs. GPO10** 0: SYSIDLE 1: GPO10
5	RW	0	**Multi-Function Signal Select: (CPUSTP#, C4PSTOP#) vs. (GPO5, GPO6)** 0: (CPUSTP#, C4PSTOP#) 1: (GPO5, GPO6)
4	RW	0	**Multi-Function Signal Select: SPKR vs. GPO0** 0: SPKR 1: GPO0
3:2	RW	0	**Reserved**
1	RW	0	**Multi-Function Signal Select: SPI vs. GPIO** 0: MSPIDI, MSPICLK, MSPIDO, MSPISS1#, MSPISS0# 1: GPI0, GPIO6, GPO1, GPO2, GPO3
0	RW	0	**Multi-Function Signal Select: SATALED[1:0]# vs. (GPIO11,GPIO10)** 0: GPIO11, GPIO10 1: SATALED[1:0]#

Table 46. C3 Latency Configuration Table

RxEC[2]	RxE4[7]	STOP GRANT to SLP# 1->0	SLP# 1->0 to CPUSTP# 1->0	Break Event to CPUSTP# 0->1	CPUSTP# 0->1 to SLP# 0->1	SLP# 0->1 to STPCLK# 0->1
0	0	7.5~15 us	8~11.25 us	7.5~15 us	RxFC[2:1] / DPSLP# 0->1 to SLP# 0->1 00 / 7~8 us 01 / 14.5~15.5 us 10 / 22~23 us 11 / 29.5~30.5 us	7.5 us
0	1	0.83~1.66 us	1~1.25 us	0.83~1.66 us	RxFC[2:1] / DPSLP# 0->1 to SLP# 0->1 00 / 0.83 us 01 / 7.5~16 us 10 / 15~23.5 us 11 / 22.5~31 us	0.83 us
1	x	0.56~1.12 us	0.84 us	0.56~1.12 us	0.56 us	0.56 us

Table 47. C4 Latency Configuration Table

<table>
<tr><th>RxEC[2]</th><th>RxE4[7]</th><th>STOP GRANT
to
SLP# 1->0</th><th>SLP# 1->0
to
CPUSTP# 1->0</th><th>CPUSTP# 1->0
to
VRDSLP 0->1</th><th>Break Event
to
VRDSLP 1->0</th><th>VRDSLP 1->0
to
CPUSTP# 0->1</th><th>CPUSTP# 0->1
to
SLP# 0->1</th><th>SLP# 0->1
to
STPCLK# 0->1</th></tr>
<tr><td>0</td><td>0</td><td>7.5~15 us</td><td>8~11.25 us</td><td>3.75~7.5 us</td><td>0~7.5 us</td><td>
<table>
<tr><th>RxE5[7]
&
RxE3[6]</th><th>VRDSLP 1->0 to
CPUSTP# 0->1</th></tr>
<tr><td>0x</td><td>90~132 us</td></tr>
<tr><td>10</td><td>31~39 us
or 7.5 us</td></tr>
<tr><td>11</td><td>30~70 us</td></tr>
</table>
</td><td>
<table>
<tr><th>RxFC[2:1]</th><th>DPSLP# 0->1
to SLP# 0->1</th></tr>
<tr><td>00</td><td>7~8 us</td></tr>
<tr><td>01</td><td>14.5~15.5 us</td></tr>
<tr><td>10</td><td>22~23 us</td></tr>
<tr><td>11</td><td>29.5~30.5 us</td></tr>
</table>
</td><td>7.5 us</td></tr>
<tr><td>0</td><td>1</td><td>0.83~1.66 us</td><td>1~1.25 us</td><td>0.63~0.83 us</td><td>0~0.83 us</td><td>
<table>
<tr><th>Rx8A[7]</th><th>RxE5[7]
&
RxE3[6]</th><th>VRDSLP 1->0 to
CPUSTP# 0->1</th></tr>
<tr><td rowspan="3">0</td><td>0x</td><td>11.5~13.5 us</td></tr>
<tr><td>10</td><td>3.3~4.5 us
or 0.84 us</td></tr>
<tr><td>11</td><td>3.5~7.5 us</td></tr>
<tr><td rowspan="3">1</td><td>0x</td><td>35~45us</td></tr>
<tr><td>10</td><td>Not suggested</td></tr>
<tr><td>11</td><td>20~25 us</td></tr>
</table>
</td><td>
<table>
<tr><th>RxFC[2:1]</th><th>DPSLP# 0->1
to SLP# 0->1</th></tr>
<tr><td>00</td><td>0.83 us</td></tr>
<tr><td>01</td><td>7.5~16 us</td></tr>
<tr><td>10</td><td>15~23.5 us</td></tr>
<tr><td>11</td><td>22.5~31 us</td></tr>
</table>
</td><td>0.83 us</td></tr>
<tr><td>1</td><td>x</td><td>0.56~1.12 us</td><td>0.84 us</td><td>0.28~0.56 us</td><td>0~0.56 us</td><td>0.56 us</td><td>0.56 us</td><td>0.56 us</td></tr>
</table>

Offset Address: E5h (D17F0)

Multi-Function Select 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**C4 VR Recovery Latency Selection Bit** VRDSLP de-assertion to DPSLP de-assertion latency. In detail, please refer to C3/C4 latency configuration tables. RxE5[7] / RxE3[6] — VR Change Timer Select 00 — 90~100 us 01 — 90~100 us 10 — 7.5~15 us 11 — 30~45 us RxE4[7] and RxEC[2] must set to 0.
6	RW	0	**NM Bus Master as Source of Bus Master Status** 0: Disable 1: Enable
5	RW	0	**Enable North Bridge Interrupt to Wake up Cx State** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	0	**CPU Frequency Change** 0: DPSLP# 1: Disable (output high) 0: VRDSLP 1: Disable (output high)
2	RW	0	**PCS1 Chip Select Output via PDIOW#** 0: Disable 1: Enable When enabled, if any C2P cycle hits PCS1 I/O port address range (D17F0 Rx5E-5F), the chip select of PCS1 is asserted and output via PDIOW#.
1	RW	0	**PCS0 Chip Select Output via PDIOR#** 0: Disable 1: Enable When enabled, if any C2P cycle hits PCS0 I/O port address range (D17F0 Rx5C-5D), the chip select of PCS0 is asserted and output via PDIOR#
0	RW	0	**Enable SDIO Device 3 Break Event** 0: Disable 1: Enable

Offset Address: E6h (D17F0)

Cx State Break Event Enable 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parallel IDE/SATA Bus Master as Break Event** 0: Disable 1: Enable
6	RW	0	**USB Device Mode Bus Master as Break Event** 0: Disable 1: Enable
5	RW	0	**PCI Bus Master as Break Event**
4	RW	0	**Card Reader as Break Event** 0: Disable 1: Enable
3	RW	0	**NM Bus Master as Break Event** 0: Disable 1: Enable
2	RW	0	**EHCI Bus Master as Break Event** 0: Disable 1: Enable
1	RW	0	**UHCI Bus Master as Break Event** 0: Disable 1: Enable
0	RW	0	**HDAC / PCI DMA Bus Master as Break Event** 0: Disable 1: Enable

Offset Address: E7h (D17F0)

Cx State Break Event Enable 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable APIC Cycle Reflect to All Bus Master Activity Effective Signal** 0: Disable 1: Enable
6	RW	0	**HD Audio Record FIFO Status Reflect Control** When enabled, "HD Audio Record FIFO Not Empty" signal will be reflected on HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. 0: Disable 1: Enable
5	RW	0	**Enable HD Audio Play Run Bit to Inhibit C4P** When HD audio play run bit is open, C4P can be inhibited. 0: Disable 1: Enable
4	RW	0	**Enable HD Audio Record Run Bit to Inhibit C4P** When HD audio record run bit is open, C4P can be inhibited. 0: Disable 1: Enable
3	RW	0	**HD Audio CORB / RIRB RW Pointer Compare Reflect to DMA Control** When enabled, "HD Audio CORB / RIRB Write / Read Pointer Compare" signal will be reflected on HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx00[4]). 0: Disable 1: Enable
2	RW	0	**HD Audio CORB / RIRB Run Bit Reflect to DMA Control** When enabled, "HD Audio CORB / RIRB Run Bit" will be reflected on HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx0[4]). 0: Disable 1: Enable
1	RW	0	**HD Audio Record Run Bit Reflect to DMA Control** When enabled, "HD Audio Record Run Bit" will be reflected on HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx00[4]). 0: Disable 1: Enable
0	RW	0	**HD Audio Play Run Bit Reflect to DMA Control** When enabled, "HD Audio Play Run Bit" will be reflected to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx00[4]). 0: Disable 1: Enable

Watchdog Timer Registers (E8-FFh)

Offset Address: EB-E8h (D17F0)

Watchdog Timer Memory Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Watchdog Timer Memory Base [31:8]**
7:0	RO	0	**Hardwire to 0**

Offset Address: ECh (D17F0)

Watchdog Timer Control & C3 Latency Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Extend Delay from SLP# De-assert to STPCLK# De-assert** In detail, please refer to C3/C4 latency configuration tables. 0: Disable 1: Enable
2	RW	0	**Enable Fast C3 Mode** 0: Depends on RxE4[7] setting 1: Enable fast C3 mode Enable C4 is not allowed. In detail, please refer to C3/C4 latency configuration tables.
1	RW	0	**Enable Watch Dog Timer** If set, this bit can be reset only by PCIRST#. 0: Disable 1: Enable
0	RW	0	**Watchdog Timer Memory** 0: Disable 1: Enable

Offset Address: ED-FBh (D17F0) – Reserved

Offset Address: FCh (D17F0)

Processor Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:3	RW	0	**Reserved**
2:1	RW	0	**DPSLP# to SLP# Latency Adjustment** ***When RxE4[7]=0:*** 00: 7.5 us 01: 15 us 10: 22.5 us 11: 30 us ***When RxE4[7]=1:*** 00: 0.83 us 01: 1.5~7.5 us 10: 7.5~15 us 11: 10~22.5 us
0	RW	0	**Reserved**

Offset Address: FD-FFh (D17F0) – Reserved

MMIO Space Registers

The base address of MMIO space registers is located in D17F0 RxBC-BEh.

Control Registers (000-009h)

Offset Address: 000h (D17F0 MMIO)

SPI Bus0 Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**SPI Bus0 Enable** 0: Disable 1: Enable

Offset Address: 003-001h (D17F0 MMIO)

SPI Bus0 Memory Map Base Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:0	RW	0	**SPI Bus0 Memory Map Base Address**

Offset Address: 004-007h (D17F0 MMIO) – Reserved

Offset Address: 008h (D17F0 MMIO)

SPI Bus Misc. Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**SPI External Device Interrupt Enable:** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 009h (D17F0 MMIO)

SPI Bus Interrupt Routing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**SPI IRQ Routing** 0000: IRQ0 0001: IRQ1 … … 1111: IRQ15

Offset Address: 00A-00Bh (D17F0 MMIO) – Reserved

Offset Address: 00Ch (D17F0 MMIO)

CEC Interrupt Routing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CEC IRQ routing** 0000: IRQ0 0001: IRQ1 … … 1111: IRQ15
3:2	RW	0	**Reserved**
1	RW	0	**CEC RX/TX Clock Select** 0: Select 32kHz clock 1: Select 33M Hz clock (test mode)
0	RW	0	**CEC Function Control** 1: Enable 0: Disable

Offset Address: 00F-00Dh (D17F0 MMIO)

CEC Memory Map Base Address **Default Value: 00 0000h**

Bit	Attribute	Default	Description
23:0	RW	0	**CEC Memory Map Base Address**

MMIO Space Registers (010-FFFh)

Offset Address: 010-FFFh (D17F0 MMIO) – Reserved

Power Management IO Space

ACPI IO Space Registers (PMIO 00-0Fh)

Offset Address: 01-00h (PMIO)

Power Management Status **Default Value: 0000h**

The bits in this register are set by hardware and can be reset by software by writing a one to the desired bit position.

Bit	Attribute	Default	Description
15	RW1C	0	**Wakeup Status** This bit is set when the system is in the suspend state (S1 ~ S5) and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3/C4 to C0 for the processor).
14	RW1C	0	**PCIe Wakeup Status** This bit is set when PCIe is waken up.
13:12	RO	0	**Reserved**
11	RW1C	0	**Power Status** 0: Core power on 1: Abnormal power off
10	RW1C	0	**RTC Alarm Status** This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).
9	RW1C	0	**Sleep Button Status** This bit is set when the sleep button is pressed (SLPBTN# signal asserted low).
8	RW1C	0	**Power Button Status** This bit is set when the PWRBTN# signal is asserted low. If the PWRBTN# signal is held low for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will change into the soft off state.
7:6	RO	0	**Reserved**
5	RW1C	0	**Global Status** This bit is set by hardware when the BIOS Release bit (Rx2C[1]) is set (typically by an SMI routine to release control of the SCI / SMI lock). When this bit is cleared by software (by writing a one to this bit position), the BIOS Release bit is also cleared at the same time by hardware.
4	RW1C	0	**Bus Master Status** This bit is set when a bus master request is asserted. All PCI master, ISA master and ISA DMA devices are included.
3:1	RO	0	**Reserved**
0	RW1C	0	**ACPI Timer Carry Status** The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

Offset Address: 03-02h (PMIO)

Power Management Enable **Default Value: 0100h**

The bits defined in this register correspond to the same location of Rx01-00h, Power Management Status Register.

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RW	0	**Disable PCIe Wakeup** 0: Enable PCIe wakeup 1: Disable PCIe wakeup
13:11	RO	0	**Reserved**
10	RW	0	**RTC Alarm Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set. 0: Disable 1: Enable
9	RW	0	**Sleep Button Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Sleep Button Status bit is set. 0: Disable 1: Enable
8	RW	1b	**Power Button** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set. 0: Disable 1: Enable
7:6	RO	0	**Reserved**
5	RW	0	**Global Enable** This bit, when set, triggers a SCI to be generated when the Global Status bit (Rx00[5]) is set. 0: Disable 1: Enable
4:1	RO	0	**Reserved**
0	RW	0	**ACPI Timer Enable** This bit, when set, triggers a SCI to be generated when the Timer Status bit is set. 0: Disable 1: Enable

Offset Address: 05-04h (PMIO)

Power Management Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Reserved**
14	RO	0	**Reserved**
13	WO	0	**Sleep Enable** Reads from this bit always return zero. Writing a one to this bit causes the system to enter the sleep (suspend) state defined by the Sleep Type, bits [12:10].
12:10	RW	000b	**Sleep Type** 000: Normal On 001: Suspend to RAM (STR) 010: Suspend to Disk (STD, also called Soft Off). The VCC power plane is turned off while the VSUS33 and VBAT planes remain on. 011: Reserved 100: Power On Suspend without Reset 101: Power On Suspend with CPU/PCI Reset 11x: Reserved In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.
9	RO	0	**Reserved**
8	RW	0	**Reserved**
7:3	RO	0	**Reserved**
2	WO	0	**Global Release** This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit (Rx28[5]). This bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that setting on this bit will cause an SMI to be generated if the BIOS Enable bit (Rx2A[5]) is set.
1	RW	0	**Bus Master Reload** This bit controls whether bus master request (Rx00[4]) resumes the processor from C3/C4 to C0 state. 0: Bus master requests are ignored by power management logic. 1: Bus master requests resume the processor from the C3/C4 state to the C0 state.
0	RW	0	**SCI / SMI Select** This bit controls either SCI or SMI is generated for power management events triggered by the Power Button, Sleep Button and RTC (when PMIO Rx00 bits 8, 9, or 10 equal one). 0: SMI 1: SCI Note that certain power management events can be programmed to select either SCI or SMI interrupt independently of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at PMIO Rx22 and 24). Also, Timer Status & Global Status always generate SCI and BIOS Status always generates SMI.

Offset Address: 06-07h (PMIO) – Reserved

Offset Address: 0B-08h (PMIO)

ACPI Timer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Extended Timer Value** This field reads back 0 if the 24-bit timer option is selected (D17F0 Rx81[3]).
23:0	RO	0	**Timer Value** This field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during system reset, and then continues counting until the 14.31818 MHz input clock of the chip is stopped. If the clock is restarted without a reset, the counter will continue counting from where it was stopped.

Offset Address: 0C-0Fh (PMIO) – Reserved

Processor Power Management Registers (PMIO 10-1Fh)

Offset Address: 13-10h (PMIO)

Processor Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:5	RW	0	**Reserved**
4	RW	0	**Throttling Enable** Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. Its duty cycle is determined by bits [3:0] of this register.
3:0	RW	0	**Throttling Duty Cycle**

Offset Address: 14h (PMIO)

Processor Level 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 2 (LVL2)**

Offset Address: 15h (PMIO)

Processor Level 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 3 (LVL3)**

Offset Address: 16h (PMIO)

Processor Level 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 4 (LVL4)**

Offset Address: 17h (PMIO)

Processor Level 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 5 (LVL5)**

Offset Address: 18-1Fh (PMIO) – Reserved

General Purpose Power Management Registers (PMIO 20-53h)

Offset Address: 21-20h (PMIO)

General Purpose Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**North Module SERR# Status**
14	RW1C	0	**USB Wakeup in Suspend** For suspend states: POS / STR / STD.
13	RW1C	0	**HDAC Wakeup Status** It can be set only in suspend mode.
12	RW1C	0	**Battery Low Status** Set when the BATLOW# input is asserted low.
11	RW1C	0	**LID# Status** Set when the edge changes as selected by Rx2C[7] on the LID# input is detected.
10	RW1C	0	**Thermal Detect Status** Set when the edge changes as selected by Rx2C[6] on the THRM# input is detected.
9	RW1C	0	**Mouse Controller PME Status**
8	RW1C	0	**RING# Status** Set when the RING# input is asserted low.
7	RW1C	0	**GP3 Timer Time Out Status**
6	RW1C	0	**INTRUDER# Status** Set when the INTRUDER# pin is asserted low.
5	RW1C	0	**PME# Status** Set when the PME# pin is asserted low.
4	RW1C	0	**EXTSMI# Status** Set when the EXTSMI# pin is asserted low.
3	RW1C	0	**Reserved**
2	RW1C	0	**Internal KBC (Keyboard Controller) PME Status** Set when the internal KBC PME signal is asserted.
1	RW1C	0	**GPI1 Status** Set when the GPI1 pin is asserted low.
0	RW1C	0	**GPI0 Status** Set when the GPI0 pin is asserted low.

Note that the above bits correspond to the respective bits at the same location of the General Purpose SCI Enable and General Purpose SMI Enable registers at offset address 22h and 24h: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one. The above bits are set by hardware only and can only be cleared by writing a one.

Offset Address: 23-22h (PMIO)

General Purpose SCI / RESUME Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SCI on North Module SERR Event** 0: Disable 1: Enable
14	RW	0	**Enable SCI on USB Wake-up Event** 0: Disable 1: Enable
13	RW	0	**Enable SCI on HDAC Wake-up Event** 0: Disable 1: Enable
12	RW	0	**Enable SCI on BATLOW# Event** 0: Disable 1: Enable
11	RW	0	**Enable SCI on LID# Event** 0: Disable 1: Enable
10	RW	0	**Enable SCI on THRM# Event** 0: Disable 1: Enable
9	RW	0	**Enable SCI on Mouse PME** 0: Disable 1: Enable
8	RW	0	**Enable SCI on RING# Event** 0: Disable 1: Enable
7	RW	0	**Enable SCI on GP3 Timer Timeout** 0: Disable 1: Enable
6	RW	0	**Enable SCI on INTRUDER# Event** 0: Disable 1: Enable
5	RW	0	**Enable SCI on PME# Assertion** 0: Disable 1: Enable
4	RW	0	**Enable SCI on EXTSMI# Assertion** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**Enable SCI on Internal KBC PME** 0: Disable 1: Enable
1	RW	0	**Enable SCI on GPI1 Assertion** 0: Disable 1: Enable
0	RW	0	**Enable SCI on GPI0 Assertion** 0: Disable 1: Enable

Offset Address: 25-24h (PMIO)

General Purpose SMI / Resume Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SMI on North Module SERR Event** 0: Disable 1: Enable
14	RW	0	**Enable SMI on USB Wake-up Event** 0: Disable 1: Enable
13	RW	0	**Enable SMI on HDAC Wake-up Event** 0: Disable 1: Enable
12	RW	0	**Enable SMI on BATLOW# Event** 0: Disable 1: Enable
11	RW	0	**Enable SMI on LID# Event** 0: Disable 1: Enable
10	RW	0	**Enable SMI on THRM# Event** 0: Disable 1: Enable
9	RW	0	**Enable SMI on Mouse PME** 0: Disable 1: Enable
8	RW	0	**Enable SMI on RING# Event** 0: Disable 1: Enable
7	RW	0	**Reserved**
6	RW	0	**Enable SMI on INTRUDER# Event** 0: Disable 1: Enable
5	RW	0	**Enable SMI on PME# Assertion** 0: Disable 1: Enable
4	RW	0	**Enable SMI on EXTSMI# Assertion** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**Enable SMI on Internal KBC PME** 0: Disable 1: Enable
1	RW	0	**Enable SMI on GPI1** 0: Disable 1: Enable
0	RW	0	**Enable SMI on GPI0** 0: Disable 1: Enable

Offset Address: 26h (PMIO)

Processor Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2	RW	0	**Host Clock Stop (CPUSTP#/DPSLP#) Control** This bit controls whether CPUSTP#/DPSLP# is asserted in C3/C4 states. Normally CPUSTP#/DPSLP# is not asserted in C3/C4 states, only STPCLK# is asserted. 0: CPUSTP#/DPSLP# will not be asserted in C3/C4 states (only STPCLK# is asserted). 1: CPUSTP#/DPSLP# will be asserted in C3/C4 states. Note: This register won't affect CPUSTP#/DPSLP# in S1 state.
1	RW	0	**SLP# Assertion in Processor Level 3 Read** This bit controls whether SLP# is asserted in C3 state. 0: SLP# is not asserted in C3 state 1: SLP# is asserted in C3 state
0	RW	0	**Lower CPU Voltage (Activate VRDSLP) During C3 / S1** This bit controls whether the CPU voltage is lowered in C3/S1 state. The CPU voltage is lowered using the VRDSLP signal to the voltage regulator. To activate this control bit, bits 1 and 2 of this register must be set to 1. 0: Disable (normal voltage during C3/S1) 1: Enable (lower voltage during C3/S1) Notes: 1. To enter C4 state in C3 command read, register bits [2:0] must be set. 2. Reading LVL4 (PMIO Rx16) has the same effect as reading LVL3 with bits [2:0] are set to1. 3. VRDSLP will be activated either in C3 with this control bit set or LVL4 is read.

Offset Address: 27h (PMIO) – Reserved

Offset Address: 29-28h (PMIO)

Global Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**GPIO Range 1 Access Status** This bit is set when GPIO range 1 is accessed.
14	RW1C	0	**GPIO Range 0 Access Status** This bit is set when GPIO range 0 is accessed.
13	RW1C	0	**GP3 Timer Timeout Status** This bit is set when GP3 timer times out.
12	RW1C	0	**GP2 Timer Timeout Status** This bit is set when GP2 timer times out.
11	RW1C	0	**SERIRQ SMI Status** This bit is set when serial interrupt IRQ2 is asserted.
10	RW1C	0	**PMIO Rx5[5] (Sleep Enable) Write Status** This bit reports whether PMIO Rx5[5] has been write-accessed. If PMIO Rx2B[3] is set to enable SMI, an SMI in generated when this bit is 1.
9	RW1C	0	**THRMTRIP# Activity Status** This bit is set when THRMTRIP# is asserted.
8	RW1C	0	**CLKRUN# Resume Status** This bit is set when PCI bus peripherals asserting CLKRUN#.
7	RW1C	0	**Primary IRQ/INIT/NMI/SMI Resume Status** This bit is set at the occurrence of primary IRQs as defined in Rx85-84 of PCI configuration space.
6	RW1C	0	**Software SMI Status** This bit is set when the SMI Command port (Rx2F) is write-accessed.
5	RW1C	0	**BIOS Status** This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one) the Global Release bit is reset at the same time by hardware.
4	RW1C	0	**Legacy USB Status** This bit is set when a legacy USB event occurs. This is normally used for USB keyboards.
3	RW1C	0	**GP1 Timer Timeout Status** This bit is set when the GP1 timer times out.
2	RW1C	0	**GP0 Timer Timeout Status** This bit is set when the GP0 timer times out.
1	RW1C	0	**Secondary Event Timer Timeout Status** This bit is set when the secondary event timer times out.
0	RO	0	**Primary Activity Status** This bit can be cleared by writing 1 to clear Rx30-33.

Notes:

1. SMI can be generated when any of the above bits is set if the corresponding control bit is enabled (see the Rx2A Global Enable register bit descriptions).
2. The above status bits are set by hardware and can only be cleared by writing a one to the desired bit position.
3. The above status bits, when set, will trigger assertion of SMI.

Offset Address: 2B-2Ah (PMIO)

Global Enable **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW	0	**SMI Enable on GPIO Range 1 Access** 0: Disable 1: Enable
14	RW	0	**SMI Enable on GPIO Range 0 Access** 0: Disable 1: Enable
13	RW	0	**SMI Enable on GP3 Timer Timeout** 0: Disable 1: Enable
12	RW	0	**SMI Enable on GP2 Timer Timeout** 0: Disable 1: Enable
11	RW	0	**SMI Enable on SERIRQ SMI** 0: Disable 1: Enable
10	RW	0	**SMI Enable on Rx05[5] Write** 0: Disable 1: Enable
9	RW	1b	**THRMTRIP# Activity Power Off Enable** 0: Disable 1: Enable
8	RW	0	**Reserved**
7	RW	0	**Primary IRQ/INIT/NMI/SMI Resume Enable in POS State** This bit may be set to trigger an SMI assertion when the Primary IRQ / INIT / NMI / SMI Resume Status bit is set.
6	RW	0	**SMI Enable on Software SMI** This bit may be set to trigger an SMI assertion when the Software SMI Status bit is set.
5	RW	0	**SMI Enable on BIOS** This bit may be set to trigger an SMI assertion when the BIOS Status bit is set.
4	RW	0	**SMI Enable on Legacy USB** This bit may be set to trigger an SMI assertion when the Legacy USB Status bit is set.
3	RW	0	**SMI Enable on GP1 Timer Timeout** This bit may be set to trigger an SMI assertion when the GP1 Timer Timeout Status bit is set.
2	RW	0	**SMI Enable on GP0 Timer Timeout** This bit may be set to trigger an SMI assertion when the GP0 Timer Timeout Status bit is set.
1	RW	0	**SMI Enable on Secondary Event Timeout** This bit may be set to trigger an SMI assertion when the Secondary Event Timer Timeout Status bit is set.
0	RW	0	**SMI Enable on Primary Activity** This bit may be set to trigger an SMI assertion when the Primary Activity Status bit is set.

Offset Address: 2D-2Ch (PMIO)
Global Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13:11	RW	0	**Reserved**
10	RW	0	**IDE Bus Power-Off** 0: Disable 1: Enable
9	RO	0	**Reserved**
8	RW1C	0	**SMI Active Status** 0: SMI inactive 1: SMI active If D17F0 Rx8D[3] is set to 0, this bit must be written 1 to clear it before the next SMI can be generated.
7	RW	0	**LID# Triggering Polarity** 0: Rising edge 1: Falling edge
6	RW	0	**THRM# Triggering Polarity** 0: Rising edge 1: Falling edge
5	RW	0	**Disable Battery Low Resume** 0: Enable resume 1: Disable resume from suspend when BATLOW# is asserted.
4	RO	0	**Reserved** Always reads 0.
3	RO	0	**Reserved.** Always reads 0.
2	RW	0	**Power Button Triggering Polarity** 0: Rising edge 1: Falling edge Set to zero to avoid the situation where the Power Button Status bit is set to wake up the system then reset again by 4's-Override status to switch the system into the soft-off state.
1	RW	0	**BIOS Release** This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software. Note that if the Global Enable bit is set (Power Management Enable register Rx02[5]), setting this bit causes an SCI or SMI to be generated (since setting on this bit causes the Global Status bit to be set).
0	RW	0	**SMI Enable** 0: Disable all SMI generation 1: Enable SMI generation

Offset Address: 2Eh (PMIO) – Reserved

Offset Address: 2Fh (PMIO)
Software SMI Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMI Command** Writing to this port triggers SMI assertion.

Offset Address: 33-30h (PMIO)

Primary Activity Detect Status **Default Value: 0000 0000h**

The Primary Activity Detect Status bits have one-to-one correspondence to the Primary Activity Detect Enable bits in Rx37-34. If the corresponding bit is set in the Enable register, setting of a bit in the Status register will cause the Primary Activity Status (Rx28[0]) bit to be set. Bit in this register default to be 0, is set by hardware only and it could only be cleared by writing 1 to the desired bit.

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW1C	0	**Audio Status** Set if Audio is accessed.
9	RW1C	0	**Keyboard Controller Access Status** Set if the KBC is accessed via I/O port 60h.
8	RW1C	0	**VGA Access Status** Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.
7	RW1C	0	**LPT Port Status** Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).
6	RW1C	0	**Serial Port B Access Status** Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2EFh (COM2 and COM4 respectively).
5	RW1C	0	**Serial Port A Access Status** Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 and COM3, respectively).
4	RW1C	0	**Floppy Access Status** Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.
3	RW1C	0	**IDE Access Status** Set if the EIDE controller is accessed via I/O ports 170-177h or 376h.
2	RW1C	0	**SATA Access Status** Set if the SATA controller is accessed via I/O ports 1F0-1F7h or 3F6h.
1	RW1C	0	**Primary Interrupt Activity Status** Set on the occurrence of a primary interrupt (enabled via the register at D17F0 PCI configuration Rx84h.).
0	RW1C	0	**PCI Master Access Status** Set on the occurrence of PCI master activity.

Notes:

1. Setting of Primary Activity Status may be done to enable a "Primary Activity Event": an SMI will be generated if the Primary Activity Enable bit (Rx2A[0]) is set and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit (Rx38[0]) is set.
2. Bits [9:2] above also correspond to bits of GP Timer Reload Enable register Rx38: If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

Offset Address: 37-34h (PMIO)

Primary Activity Detect Enable

Default Value: 0000 0000h

The Primary Activity Detect Enable bits have one-to-one correspondence to the Primary Activity Detect Status bits in Rx33-30. Setting of any of Status bits also sets the Primary Activity Status (Rx28[0]) bit which causes the GP0 timer to be reloaded (if the Primary Activity GP0 Enable bit is set) or generates an SMI (if Primary Activity Enable is set).

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW	0	**SMI on Audio Status** 0: Do not set Rx28[0] if Rx30[10] is set. 1: Set Rx28[0] if Rx30[10] is set.
9	RW	0	**SMI on Keyboard Controller Status** 0: Do not set Rx28[0] if Rx30[9] is set. 1: Set Rx28[0] if Rx30[9] is set.
8	RW	0	**SMI on VGA Status** 0: Do not set Rx28[0] if Rx30[8] is set. 1: Set Rx28[0] if Rx30[8] is set.
7	RW	0	**SMI on LPT Status** 0: Do not set Rx28[0] if Rx30[7] is set. 1: Set Rx28[0] if Rx30[7] is set.
6	RW	0	**SMI on Serial Port B Status** 0: Do not set Rx28[0] if Rx30[6] is set. 1: Set Rx28[0] if Rx30[6] is set.
5	RW	0	**SMI on Serial Port A Status** 0: Do not set Rx28[0] if Rx30[5] is set. 1: Set Rx28[0] if Rx30[5] is set.
4	RW	0	**SMI on Floppy Status** 0: Do not set Rx28[0] if Rx30[4] is set. 1: Set Rx28[0] if Rx30[4] is set.
3	RW	0	**SMI on IDE Status** 0: Do not set Rx28[0] if Rx30[3] is set. 1: Set Rx28[0] if Rx30[3] is set.
2	RW	0	**SMI on SATA Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[2] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[2] is set.
1	RW	0	**SMI on Primary IRQ Status** 0: Do not set Rx28[0] if Rx30[1] is set. 1: Set Rx28[0] if Rx30[1] is set.
0	RW	0	**SMI on PCI Master Status** 0: Do not set Rx28[0] if Rx30[0] is set. 1: Set Rx28[0] if Rx30[0] is set.

Offset Address: 38h (PMIO)
GP Timer Reload Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**GP1 Timer Reload on KBC Access** 0: Normal GP1 timer operation 1: Setting of Rx30[9] causes the GP1 timer to reload.
6	RW	0	**GP1 Timer Reload on Serial Port Access** 0: Normal GP1 timer operation 1: Setting of Rx30[5] or Rx30[6] causes the GP1 timer to reload.
5	RW	0	**Reserved**
4	RW	0	**GP1 Timer Reload on VGA Access** 0: Normal GP1 timer operation 1: Setting of Rx30[8] causes the GP1 timer to reload.
3	RW	0	**GP1 Timer Reload on Drive Access** 0: Normal GP1 timer operation 1: Setting of Rx30[4:2] causes the GP1 timer to reload.
2	RW	0	**GP3 Timer Reload on GPIO Range 1 Access** 0: Normal GP3 timer operation 1: Setting of Rx28[15] causes the GP3 timer to reload.
1	RW	0	**GP2 Timer Reload on GPIO Range 0 Access** 0: Normal GP2 timer operation 1: Setting of Rx28[14] causes the GP2 timer to reload.
0	RW	0	**GP0 Timer Reload on Primary Activity** 0: Normal GP0 timer operation 1: Setting of Rx28[0] causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (Rx37-34) with status recorded in the Primary Activity Detect Status register (Rx33-30).

Offset Address: 39h (PMIO)
General Purpose Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved** Always reads 0.
0	RW1C	0	**ASF Wake-up Status**

Offset Address: 3Ah (PMIO)
General Purpose SCI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved** Always reads 0.
0	RW	0	**SCI Enable on ASF Wake** 0: Disable 1: Enable

Offset Address: 3Bh (PMIO)
General Purpose SMI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved** Always reads 0.
0	RW	0	**SMI Enable on ASF Wake** 0: Disable 1: Enable

Offset Address: 3F-3Ch (PMIO)

General Purpose Output / Input **Default Value: FFFF 0000h**

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output, the output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
31:16	RW	FFFFh	**General Purpose Output** Bit 0: GPIO17 Bit 1: GPIO18 Bit 2: GPIO19 Bit 3: GPIO20 Bit 4: GPIO21 Bit 5: GPIO22 Bit 6: GPIO23 Bit 7: GPIO24 Bit 8: GPIO25 Bit 9: GPIO26 Bit 10: GPIO27 Bit 11: GPIO28 Bit 12: GPIO29 Bit 13: GPIO30 Bit 14: GPIO31 Bit 15: GPIO32
15:0	RO	0000h	**General Purpose Input** Bit 0: GPIO17 Bit 1: GPIO18 Bit 2: GPIO19 Bit 3: GPIO20 Bit 4: GPIO21 Bit 5: GPIO22 Bit 6: GPIO23 Bit 7: GPIO24 Bit 8: GPIO25 Bit 9: GPIO26 Bit 10: GPIO27 Bit 11: GPIO28 Bit 12: GPIO29 Bit 13: GPIO30 Bit 14: GPIO31 Bit 15: GPIO32

Offset Address: 40h (PMIO)

Extend SMI/IO Trap Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW1C	0	**BIOS Write Access Status**
3	RW1C	0	**GP3 Timer Second Timeout With No Cycles** 0: No cycles occurred in between GP3 timer 2nd timeout and reset assertion. 1: One or more cycles occurred in between GP3 timer 2nd timeout and reset assertion.
2	RW1C	0	**GP3 Timer Second Timeout Status** Set to 1 when GP3 timer has two consecutive timeouts.
1	RW1C	0	**GPIO Range 3 Access Status** This bit is set when GPIO range 3 is accessed.
0	RW1C	0	**GPIO Range 2 Access Status** This bit is set when GPIO range 2 is accessed.

Offset Address: 41h (PMIO) – Reserved

Offset Address: 42h (PMIO)
Extend SMI/IO Trap Enable **Default Value: 04h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**SMI on BIOS Write Access** This bit controls whether SMI is asserted when BIOS Write Access Status Rx40[4] is set. 0: Disable 1: Enable (can be reset only through PCI Reset)
3	RW	0	**Override GP3 Timer Second Timeout Reboot** 0: No override. GP3 timer second timeout resets the system only when bit 2 is set and AZSDOUT is strapped to enable auto reboot. 1: Enable GP3 timer second timeout reset anyway (override bit 2 and strapping)
2	RW	1b	**GP3 Timer Second Timeout Reboot** This bit controls whether the system is rebooted when the GP3 timer times out twice (Rx40[2] = 1). 0: Disable 1: Enable
1	RW	0	**SMI on GPIO Range 3 Access** This bit controls whether SMI is generated when Rx40[1] = 1. 0: Disable 1: Enable
0	RW	0	**SMI on GPIO Range 2 Access** This bit controls whether SMI is generated when Rx40[0] = 1. 0: Disable 1: Enable

Offset Address: 43h (PMIO) – Reserved

Offset Address: 45-44h (PMIO)
EXTSMI and Miscellaneous Input Value **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RO	0	**Latest PCS (PCS0-PCS3) IOR/IOW Status** 0: IOR 1: IOW
11	RO	0	**Serial SMI Status**
10	RO	0	**Reserved**
9	RO	0	**SMBus IRQ Status**
8	RO	0	**SMBus Resume Status**
7:0	RO	0	**Reserved**

Offset Address: 47-46h (PMIO)

General Purpose Output / Input **Default Value: FFF8h**

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output, the output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
15:8	RW	FFh	**General Purpose Output** Bit 0: GPIO33 Bit 1: GPIO34 Bit 2: GPIO35 Bit 3: GPIO36 Bit 4: GPIO37 Bit 5: GPIO38 Bit 6: GPIO39 Bit 7: GPIO40
7:0	RO	F8h	**General Purpose Input** Bit 0: GPIO33 Bit 1: GPIO34 Bit 2: GPIO35 Bit 3: GPIO36 Bit 4: GPIO37 Bit 5: GPIO38 Bit 6: GPIO39 Bit 7: GPIO40

Offset Address: 4B-48h (PMIO)

General Purpose Input **Default Value: 10FA 03F2h**

Bit	Attribute	Default	Description
31:0	RO	10FA 03F2h	**General Purpose Input** Bit 0: GPI0 Bit 1: GPI1 Bit 2: GPI2 Bit 3: GPI3 Bit 4: GPI4 Bit 5: GPI5 Bit 6: GPI6 Bit 7: GPI7 Bit 8: GPI8 Bit 9: GPI9 Bit 10: GPIO0 Bit 11: GPIO1 Bit 12: GPIO2 Bit 13: GPIO3 Bit 14: GPIO4 Bit 15: GPIO5 Bit 16: GPIO6 Bit 17: GPIO7 Bit 18: GPIO8 Bit 19: GPIO9 Bit 20: GPIO10 Bit 21: GPIO11 Bit 22: GPIO12 Bit 23: GPIO13 Bit 24: GPI10 Bit 25: GPI11 Bit 26: GPI12 Bit 27: GPI13 Bit 28: GPIO14 Bit 29: GPI14 Bit 30: GPIO15 Bit 31: GPIO16

Offset Address: 4F-4Ch (PMIO)

General Purpose Output **Default Value: FFFF FFFFh**

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output, the output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
31:30	RW	11b	**General Purpose Output** Bit 30: GPIO15 Bit 31: GPIO16
29:28	RW	11b	**Reserved**
27:0	RW	FFF FFFFh	**General Purpose Output** Bit 0: GPO0 Bit 1: GPO1 Bit 2: GPO2 Bit 3: GPO3 Bit 4: GPO4 Bit 5: GPO5 Bit 6: GPO6 Bit 7: GPO7 Bit 8: GPO8 Bit 9: GPO9 Bit 10: GPO10 Bit 11: GPIO0 Bit 12: GPIO1 Bit 13: GPIO2 Bit 14: GPIO3 Bit 15: GPIO4 Bit 16: GPIO5 Bit 17: GPIO6 Bit 18: GPIO7 Bit 19: GPIO8 Bit 20: GPIO9 Bit 21: GPIO10 Bit 22: GPIO11 Bit 23: GPIO12 Bit 24: GPIO13 Bit 25: GPO11 Bit 26: GPO12 Bit 27: GPIO14 Bit 30: GPIO15 Bit 31: GPIO16

Offset Address: 50h (PMIO)

GPI Change Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	**Pin Change Status** Bit 0: GPI14 Bit 1: GPI1 Bit 2: GPIO0 Bit 3: GPIO1 Bit 4: GPIO10 Bit 5: GPIO11 Bit 6: GPI12 (Not used in this product) Bit 7: GPI13 (Not used in this product) 0: No change 1: Change occurs

Offset Address: 51h (PMIO) – Reserved

Offset Address: 52h (PMIO)
GPI Change SCI/SMI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Pin Change SCI / SMI** Bit 0: GPI14 Bit 1: GPI1 Bit 2: GPIO0 Bit 3: GPIO1 Bit 4: GPIO10 Bit 5: GPIO11 Bit 6: GPI12 (Not used in this product) Bit 7: GPI13 (Not used in this product) 0: Disable SMI / SCI on pin input change 1: Enable SMI / SCI on pin input change

Offset Address: 53h (PMIO) – Reserved

IO Trap Registers (PMIO 54-6Fh)

Offset Address: 57-54h (PMIO)

I/O Trap PCI Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**PCI Data During I/O Trap SMI**

Offset Address: 59-58h (PMIO)

I/O Trap PCI I/O Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**PCI Address During I/O Trap SMI**

Offset Address: 5Ah (PMIO)

I/O Trap PCI Command / Byte Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**PCI Command Type During I/O Trap SMI**
3:0	RO	0	**PCI Byte Enable During I/O Trap SMI**

Offset Address: 5B-5Ch (PMIO) – Reserved

Offset Address: 5Dh (PMIO)

Scratch Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Register**

Offset Address: 5E-5Fh (PMIO) – Reserved

Offset Address: 60h (PMIO)
C4P State Event Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable to Support PLL Gating State during C4 State** If this bit is set to 1, the bus master monitor timer is enabled. 0: Disable 1: Enable
6	RW	0	**Enable to Support PLL Gating during C3 State** If this bit is set to 1, the bus master monitor timer is enabled. 0: Disable 1: Enable
5	RW	0	**Enable VART Master Reset Bus Master Idle Timer** 0: Ignore VART master reset bus master idle timer. 1: Enable VART bus master idle timer reset signal.
4	RW	0	**Enable VART transaction to Inhibit C4P** When VART controller is doing transaction, C4P can be inhibited. 0: Disable 1: Enable
3	RW	0	**Enable RTC Interrupt to Wake Up C4P State** 0: Disable 1: Enable
2	RW	0	**C4PSTP# Output to the Clock Generator** 0: Disable 1: Enable
1	RW	0	**Enable Keyboard Interrupt to Wake up C4P State** 0: Disable 1: Enable
0	RW	0	**Enable Mouse Interrupt to Wake up C4P State** 0: Disable 1: Enable

Offset Address: 61h (PMIO)
C4P State Bus Master Idle Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RO	0	**Current Count Value of the Bus Master Idle Timer** If this timer is not time out, a C4P state is inhibitive.

Offset Address: 62h (PMIO)
C4P State Bus Master Idle Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
2:0	RW	0	**Initial Value of the Bus Master Idle Timer** The timer tick is 32KHz..

Offset Address: 63h (PMIO)
C4P State H2R Timer Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Initial Value of Resume Timeout Using 4KHz Clock**

Offset Address: 64h (PMIO)
C4P State Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5	RW	0	**Enable SATA Master Reset Bus Master Idle Timer** 0: Ignore SATA master reset bus master idle timer. 1: Enable bus master idle timer reset signal. Note: If SATA is not used, this bit and bit 3 can be set to 0
4	RW	0	**PMIO Rx26[4:0] Write Protection Bit** 0: PMIO Rx26[4:0] can be written 1: PMIO Rx26[4:0] can not be written
3	RW	0	**PMU Request to SATA to Enter C4P State and Wait for SATA Slumber Mode Acknowledge Signal** 0: Disable 1: Enable
2	RW	0	**SATA PHY Clock Gating** 0: Disable 1: Enable
1	RW	0	**Reserved**
0	RW	0	**SATA C4 PLL Wake Up Event from C4P State** 0: Disable 1: Enable

Offset Address: 65h (PMIO)
C4P State USB and NM Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**APIC Interrupt Wake Up System from C4P State** 0: Disable 1: Enable
6	RW	0	**Enable PIC Wakeup Event in C4P** 0: Disable 1: Enable
5	RW	0	**Reserved**
4	RW	0	**USB Wakeup Event for C4P State** 0: Disable 1: Enable
3	RW	0	**Enable USB Controller Master Reset Bus Master Idle Timer** 0: Ignore USB controller master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
2	RW	0	**Enable USBD to Prevent the Entry of C4P** 0: Disable. C4P state will be entered regardless of the state of USBD, and USBD_C4PPME is disabled; 1: Enable. C4P state will be prohibited when USB device plug to host.
1	RW	0	**PMU Request to USB to Enter C4P State And Wait for USB D3 Mode Acknowledge Signal** 0: Disable 1: Enable
0	RW	0	**Enable USB PHY 120MHz PLL Gating** 0: Disable 1: Enable

Offset Address: 66h (PMIO)
C4P State NM and HDAC Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable HDAC Master Reset Bus Master Idle Timer** 0: Ignore HDAC master reset bus master idle time. 1: Enable bus master idle timer reset signal.
6	RW	0	**HD Wakeup Event for C4P State** 0: Disable 1: Enable
5	RW	0	**NM PLL Gating** 0: Disable 1: Enable
4	RW	0	**Reserved**
3	RW	0	**NM Wakeup Event for C4P State** 0: Disable 1: Enable
2	RW	0	**Enable NM Master Reset Bus Master Idle Timer** 0: Ignore NM master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
1	RW	0	**Option Register to Select Signal from V4IF or PCIS to Indicate STPGNT Special Cycle** 0: PCIS signal 1: V4IF signal
0	RW	0	**PMU Request to NM to Enter C4P State And Wait for NM D3 Mode Acknowledge Signal** 0: Disable 1: Enable

Offset Address: 67h (PMIO)
C4P State IDE Related Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable C4P State Back to C2** 0: Disable 1: Enable
6	RW	0	**Enable SPI Master Reset Bus Master Idle Timer** 0: Ignore SPI master reset bus master idle timer. 1: Enable SPI bus master idle timer reset signal.
5	RW	0	**Enable C4P State Wakeup for Resume Timeout** 0: Disable 1: Enable
4	RW	0	**Enable UART Wakeup Event in C4P State** 0: Disable 1: Enable
3:0	RW	0	**Reserved**

Offset Address: 68h (PMIO)
C4P State Other Devices Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Enable PCI Master Reset Bus Master Idle Timer** 0: Disable 1: Enable
6	RW1C	0	**PWRGD Status** This bit records PWRGD signal state change: 1: The PWRGD signal state has been toggled since last clear to 0 or power up. It indicates that the last system reset is due to core power lost. 0: The PWRGD signal state remains unchanged since last clear to 0. It indicates that no core power lost since then.
5	RW	0	**Enable PCI REQ# as a C4 PME Event** 0: Disable 1: Enable Note: If PCICLK keeps running (disable CLKRUN# or PCISTP#) during C4P state, this bit must be set to make PCI REQ# be a C4 PME event.
4	RW	0	**Enable USB Device Mode Bus Master Reset Bus Master Idle Timer** 0: Disable 1: Enable
3	RW	0	**Enable CR (Card Reader) Master Reset Bus Mater Idle Timer** 0: Disable 1: Enable
2	RW	0	**Enable Card Reader Wakeup Event in C4P State** 0: Disable 1: Enable
1	RW	0	**Enable SDIO Master Reset Bus Mater Idle Timer** 0: Ignore SDIO master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
0	RW	0	**Enable SDIO Wakeup Event for C4P in State** 0: Disable 1: Enable

Offset Address: 69-6Eh (PMIO) – Reserved

Offset Address: 6Fh (PMIO)
Suspend Power Domain **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**Reserved**
4	RW	0	**Enable PCI Master Mode** 0: Disable 1: Enable Note: During POST stage, software needs to read D17F7 Rx56[5], then write PMIO Rx6F[4] if PCI Master is enabled.
3	RW	0	**Mask INTR Before 8259 Initialization Disable** 0: Mask INTR before IOW 8259 A1 or 21 port 1: Unmask INTR
2	WO	0	**Soft Resume** This bit is used to allow a system using an AT power supply to operate as if an ATX power supply were being used. Refer to the BIOS Porting Guide for implementation details. 0: Disable 1: Enable
1	RW	0	**Multi-Function Signal Select: PEXWAKE_ vs. GPI14** 0: PEXWAKE_ 1: GPI14

0	RW	0	**Enable GPO7 to output NM PLL Stop** 0: GPO7 normal function. 1: Stop NM PLL

Power Management Memory Mapped IO Space

Watchdog Timer Memory Base (PM-MMIO 00-07h)

The memory base address of these registers is defined in RxEB-E8h of the D17F0 PCI configuration registers.

Offset Address: 03-00h (PM-MMIO)

Watchdog Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	WO	0	**Watchdog Trigger** Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the Watchdog Count Register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disabled or stopped.
6:4	RO	0	**Reserved**
3	RO	0	**Disable Watchdog** This bit reflects the state of the watchdog timer hardware. 0: Enable 1: Disable
2	RW	0	**Watchdog Action** This bit determines the action to be taken when the watchdog timer expires. 0: System reset 1: System power off The bit is only valid when the watchdog is enabled.
1	RW1C	0	**Watchdog Fired** When set, the watchdog timer expires and causes the current restart. The bit is cleared by writing a 1 to bit 1 in the Watchdog Control register. Writing a 0 has no effect. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
0	RW	0	**Watchdog Enable** This bit is used to control or indicate whether the watchdog is in the Enabled\Running and Enabled\Stopped states. 0: Watchdog is in the Enabled\Stopped state 1: Watchdog is in the Enabled\Running state If the watchdog is in the Enabled\Stopped state and a 1 is written to bit 0, the watchdog moves to the running state but a count interval is not started until a 1 is written to bit 7. If the watchdog is in the Enabled\Running state, writing a 1 to bit 0 has no effect. The bit is only valid when the watchdog is enabled.

Offset Address: 07-04h (PM-MMIO)

Watchdog Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
9:0	WO	0	**Count Register** This defines the countdown time for the counter. A value of zero is reserved. Reading this register results in the current counter value. Writing to the register has no effect until a one is written to the watchdog trigger bit of the Watchdog Control/Status Register. These bits are only valid when the watchdog is enabled.

System Management IO Space

System Management Bus I/O Space Registers (SMIO 00-0Fh)

The base address for these registers is defined in RxD1-D0 of the D17F0 PCI configuration registers. The System Management Bus I/O space is enabled for access if D17F0 RxD2[0] = 1.

Offset Address: 00h (SMIO)

SMBus Host Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**SMB Host PEC Error** 0: SMBus Host PEC calculation is correct. 1: SMBus Host PEC calculation is error.
6	RW1C	0	**SMB Semaphore** This bit is used as a semaphore among various independent software threads that may need to use the Host SMBus logic and it has no effect on hardware. After reset, this bit reads 0. Write 1 to this bit causes the next read to return 0, all reads after that return 1. Write 0 to this bit has no effect. Software can therefore write 1 to request control and if readback is 0 then it will own usage of the host controller.
5	RW	0	**New SMBus Softwate Reset** 0: Exit reset 1: Enter reset
4	RW1C	0	**Failed Bus Transaction** 0: SMBus interrupt is not caused by failed bus transaction 1: SMBus interrupt is caused by failed bus transaction. This bit may be set when the Rx02[1] is set and can be cleared by write 1 to this bit position.
3	RW1C	0	**Bus Collision** 0: SMBus interrupt not caused by transaction collision 1: SMBus interrupt caused by transaction collision.
2	RW1C	0	**Device Error** 0: SMBus interrupt is not caused by SMBus transaction error 1: SMBus interrupt is caused by SMBus transaction error.
1	RW1C	0	**SMBus Interrupt** 0: SMBus interrupt is not caused by host command completion 1: SMBus interrupt is caused by host command completion.
0	RO	0	**Host Busy** 0: SMBus controller host interface is not processing a command 1: SMBus host controller is busy in processing a command. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 01h (SMIO)

SMBus Slave Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**SMB GPIO Slave PEC Error** 0: SMBus GPIO slave PEC calculation is correct. 1: SMBus GPIO slave PEC calculation is incorrect.
6	RW1C	0	**SMB Host Slave PEC Error** 0: SMBus Host Slave PEC calculation is correct. 1: SMBus Host Slave PEC calculation is incorrect.
5	RW1C	0	**Alert Status** 0: SMBus interrupt is not caused by SMBALRT# signal. 1: SMBus interrupt is caused by SMBALRT# signal. This bit will be set only if the Alert Enable bit in Rx08[3] is set.
4	RW1C	0	**Shadow 2 Status** 0: SMBus interrupt is not caused by address match to SMBus Slave Address Port 2 1: SMBus interrupt / resume event is caused by slave cycle address match to SMBus Shadow Address Port 2.
3	RW1C	0	**Shadow 1 Status** 0: SMBus interrupt is not caused by address match to SMBus Slave Address Port 1 1: SMBus interrupt / resume event is caused by slave cycle address match to SMBus Shadow Address Port 1.
2	RW1C	0	**Slave Status** 0: SMBus interrupt is not caused by slave event match. 1: SMBus interrupt / resume event is caused by slave cycle event match of the SMBus Slave Command Register at RxD3 (command match) and the SMBus Slave Event Register at Rx0A (data event match).
1	RO	0	**Reserved**
0	RO	0	**Slave Busy** 0: SMBus controller slave interface is not processing data 1: SMBus controller slave interface is busy receiving data. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 02h (SMIO)

SMBus Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PEC Enable** 0: Disable 1: Enable SMBus Host to support PEC calculation.
6	RW	0	**Start** 0: Write 0 has no effect 1: Start Execution of Command Write 1 to this bit causes the SMBus controller host interface to initiate execution of the command in the SMBus Command Protocol field (bits [5:2]). All necessary registers should be programmed prior to writing 1 to this bit. The Host Busy bit at Rx00[0] can be used to identify when the SMBus controller has completed command execution.
5:2	RW	0000b	**SMBus Command Protocol** Selects the command type that the SMBus host controller will execute. Reads or Writes are determined by Rx04[0]. **Protocol** 0000: Quick — 0001: Byte 0010: Byte Data — 0011: Word Data 0100: Process Call — 0101: Block 0110: I2C with 10-bit Address — 0111: Reserved 10xx: Reserved — 1100: I2C Process Call 1101: I2C Block — 1110: I2C with 7-bit Address 1111: Universal
1	RW	0	**Kill Transaction in Progress** 0: Normal host controller operation 1: Stop host transaction currently in progress. Setting this bit also sets the status bit Rx00[4] and asserts the interrupt selected by the SMB Interrupt Select bit at RxD2[3].
0	RW	0	**Interrupt Enable** 0: Disable interrupt generation 1: Enable generation of interrupts on completion of the current host transaction

Offset Address: 03h (SMIO)
SMBus Host Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Host Command** This field contains the data transmitted in the command field of the SMBus host transaction.

Offset Address: 04h (SMIO)
SMBus Host Address **Default Value: 00h**

The contents of this register are transmitted in the address field of the SMBus host transaction.

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Address** This field contains the 7-bit address of the targeted slave device.
0	RW	0	**SMBus Read or Write** 0: Execute a WRITE command 1: Execute a READ command

Offset Address: 05h (SMIO)
SMBus Host Data 0 **Default Value: 00h**

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 byte is stored here.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Data 0** For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

Offset Address: 06h (SMIO)
SMBus Host Data 1 **Default Value: 00h**

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 byte is stored here.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Data 1** This register should be programmed with the value to be transmitted in the Data 1 field of an SMBus host interface transaction

Offset Address: 07h (SMIO)
SMBus Block Data **Default Value: 00h**

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the Rx02 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during a SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Block Data Byte**

Offset Address: 08h (SMIO)

SMBus Slave Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SMBus GPIO Slave PEC Enable** 0: Disable 1: Enable SMBus GPIO Slave to support PEC calculation.
6	RW	0	**SMBus Host Slave PEC Enable** 0: Disable 1: Enable SMBus Host Slave to support PEC calculation.
5	RW	0	**PEC Abort** 0: Disable 1: Enable SMBus to abort PEC calculation error.
4	RW	0	**SMBus GPIO Slave Enable** 0: Disable 1: Enable the generation of a resume event when an external SMBus master generates a transaction with an address that matches the GPIO Slave Address register (SMIO Rx0F).
3	RW	0	**SMBus Alert Enable** 0: Disable 1: Enable generation of an interrupt or resume event on the assertion of the SMBALRT# signal
2	RW	0	**SMBus Shadow Port 2 Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI configuration register: F0RxD5).
1	RW	0	**SMBus Shadow Port 1 Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI configuration register: F0RxD4).
0	RW	0	**SMBus Slave Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI configuration register: F0RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (Rx0A).

Offset Address: 09h (SMIO)
SMBus Shadow Command **Default Value: 00h**

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

Bit	Attribute	Default	Description
7:0	RO	0	**Shadow Command** This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

Offset Address: 0B-0Ah (SMIO)
SMBus Slave Event **Default Value: 0000h**

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

Bit	Attribute	Default	Description
15:0	RW	0	**SMBus Slave Event** This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (Rx0C). When a bit in this register is set and the corresponding bit in Rx0C is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

Offset Address: 0D-0Ch (SMIO)
SMBus Slave Data **Default Value: 0000h**

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

Bit	Attribute	Default	Description
15:0	RO	0	**SMBus Slave Data** This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

Offset Address: 0Eh (SMIO) – Reserved

Offset Address: 0Fh (SMIO)
SMBus GPIO Slave Address **Default Value: 00h**

This register is used to store data values of SMBus GPIO Slave address.

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus GPIO Slave Address** Specifies the address used to match against incoming SMBus addresses for GPIO slave.
0	RO	0	**Reserved**

CEC MMIO Registers (Consumer Electronics Controller Registers)

The registers listed in this section is used to control the frame transmission on CEC line (based on HDMI specification version 1.3). The base address of CEC MMIO space registers is located in D17F0 MMIO Rx00F-00Dh.

CEC Controller MMIO Registers (00-FFh)

Offset Address: 00h (CEC-MMIO)

CEC Host Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CEC Soft Reset** ***For Read:*** 0: Normal 1: Under soft reset ***For Write:*** 0: No effect 1: To rest all the CEC registers. This bit will be cleared to 0 automatically when soft reset is completed.
6	RW	0	**CEC Status Reset** ***For Read*** 0: Normal 1: Under soft reset ***For Write*** 0: No effect 1: To reset Host Status, Host Interrupt, Host Error Interrupt Status, TX Block Size, TX Data Block Registers, RX Block Size and RX Data Block Registers (The register values of CEC Host Control, CEC Logic Address Occupation and Host Interrupt Enable remain the same). This bit will be cleared to 0 automatically when status reset is completed.
5:4	RO	0	**Reserved**
3	RW	0	**Enable Clock Gating** 0: Disable 1: Enable
2	RW	0	**Disable Slave Mode** 0: Enable host controller RX mode 1: Disable host controller RX mode
1	RW	0	**Enable Negative Acknowledge** 0: Enable positive acknowledge 1: Enable negative acknowledge Host controller will negative acknowledge and ignore the message if this bit is programmed to 1. According to CEC protocol, the initiator will deal the negative-acknowledged message with retry mechanism.
0	RW	0	**Abort TX Transmission** ***For Read*** 0: Normal 1: Aborts current message transmission ***For Write*** 0: No effect 1: Host controller will abort transmission. When the abortion done, TXABTDONE will assert if the message is aborted successfully, or TXABTFAIL will assert if no message is aborted (transmission complete). This bit will be cleared to 0 automatically when the abortion is completed.

Offset Address: 01-03h (CEC-MMIO) – Reserved

Offset Address: 04h (CEC-MMIO)

CEC Host Status Register **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**RX Blockage** ***For Read*** 0: Host controller can accept message from CEC line 1: Host controller can not accept message from CEC line ***For Write*** 0: No effect 1: To reset this bit to 0. Enable RX positive acknowledge This bit will be automatically asserted if RX receiving complete or any error is found. Host controller will negative acknowledge for the direct addressed message aimed to it and the broadcast message until this bit is reset to 0.
6:4	RO	0	**Reserved**
3	RO	0	**CEC Plug Event** 0: Host controller connection status is not changed 1: Host controller is plugged or unplugged to/from CEC line This bit will be automatically de-asserted when Rx08[14] is cleared.
2	RO	0	**CEC Device Connection Status** 0: Host controller is not connected to CEC line 1: Host controller is connected to CEC line
1	RO	0	**CEC TX Busy** 0: Host controller is not issuing message on CEC line 1: Host controller is issuing message on CEC line
0	RW	0	**Trigger Message Transfer** ***For Read*** 0: No transmission 1: Message is being transmitted ***For Write*** 0: No effect 1: Triggers message transfer. This bit will be cleared to 0 automatically when current message transmission is completed.

Offset Address: 05-07h (CEC-MMIO) – Reserved

Offset Address: 09-08h (CEC-MMIO)

CEC Host Interrupt Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**CEC TX Get No Response For the Head Block Interrupt** 0: Normal 1: CEC TX get no response for the head block
14	RW1C	0	**CEC Device Detection / TX Timeout Interrupt** 0: Normal 1: CEC Device detection or TX timeout The meaning of this interrupt can be judged by Rx04[3:2] 00: Reserved 01: TX transmission timeout interrupt 10: Device unplug interrupt 11: Device plug interrupt
13	RW1C	0	**CEC TX Lose Arbitration Interrupt** 0: Normal 1: CEC TX lose arbitration
12	RW1C	0	**CEC Receive Invalid Bit Format Report Interrupt** 0: Normal 1: CEC Receive invalid bit format report
11	RW1C	0	**CEC TX Abortion Fail Interrupt** 0: Normal 1: CEC TX abortion fail
10	RW1C	0	**CEC TX Abortion Complete Interrupt** 0: Normal 1: CEC TX abortion complete
9	RW1C	0	**CEC TX Fail Interrupt** 0: Normal 1: CEC message transmission fail (the detailed Error status is shown in Rx11)
8	RW1C	0	**CEC Message Transmission Complete Interrupt** 0: Normal 1: CEC message transmission complete
7:3	RO	0	**Reserved**
2	RW1C	0	**CEC Receive Invalid Bit Format Interrupt** 0: Normal 1: CEC reports an invalid bit format
1	RW1C	0	**CEC RX Fail Interrupt** 0: Normal 1: CEC message receiving fail (the detailed Error status is shown in Rx10)
0	RW1C	0	**CEC Message Receiving Complete Interrupt** 0: Normal 1: CEC message receiving complete

Offset Address: 0A-0Bh (CEC-MMIO) – Reserved

Offset Address: 0D-0Ch (CEC-MMIO)

CEC Host Interrupt Enable Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**CEC TX Get No Response For the Head Block Interrupt Enable** 0: Mask 1: Enable
14	RW	0	**CEC Device Detection/TX Timeout Interrupt Enable** 0: Mask 1: Enable
13	RW	0	**CEC TX Lose Arbitration Interrupt Enable** 0: Mask 1: Enable
12	RW	0	**CEC Receive Invalid Bit Format Report Interrupt Enable** 0: Mask 1: Enable
11	RW	0	**CEC TX Abortion Fail Interrupt Enable** 0: Mask 1: Enable
10	RW	0	**CEC TX Abortion Complete Interrupt Enable** 0: Mask 1: Enable
9	RW	0	**CEC TX Fail Interrupt Enable** 0: Mask 1: Enable
8	RW	0	**CEC Message Transmission Complete Interrupt Enable** 0: Mask 1: Enable
7:3	RO	0	**Reserved**
2	RW	0	**CEC Invalid Bit Format Interrupt Enable** 0: Mask 1: Enable
1	RW	0	**CEC RX Fail Interrupt Enable** 0: Mask 1: Enable
0	RW	0	**CEC Message Receiving Complete Interrupt Enable** 0: Mask 1: Enable

Offset Address: 0E-0Fh (CEC-MMIO) – Reserved

Offset Address: 11-10h (CEC-MMIO)

CEC Host Error Status Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RO	0	**CEC TX Sample Error Data in a Data/EOM Bit** 0: Mask 1: CEC TX sampled low impedance or unexpected toggle when it was sending high impedance (except the head block)
9	RO	0	**CEC TX Sample Error Data in a ACK Bit** 0: Mask 1: CEC TX get ACK bit with an invalid bit format
8	RO	0	**CEC TX Get No Response for the Data Block** 0: Mask 1: CEC TX get ACK=1 for the data block (except the head block)
7:5	RO	0	**Reserved**
4	RO	0	**CEC RX Sample Error During 1.7-2.05ms in a Data Bit** 0: Normal 1: CEC RX sample low impedance or unexpected toggle during 1.7-2.05ms in a data bit
3	RO	0	**CEC RX Sample Error During 0.85-1.25ms in a Data Bit (Except the initiator address)** 0: Normal 1: CEC RX sample unexpected toggle during 0.85-1.25ms in a data bit
2	RO	0	**CEC RX Sample Error During 0-0.4ms in a Data Bit** 0: Normal 1: CEC RX sample high impedance or toggle during 0-0.4ms in a data bit
1:0	RO	0	**Reserved**

Offset Address: 12-1Fh (CEC-MMIO) – Reserved

Offset Address: 21-20h (CEC-MMIO)
CEC Logical Address Occupation Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RW	0	**CEC Logical Address 14 Occupation** 0: CEC Logical Address 1110b is not taken by this CEC device 1: CEC Logical Address 1110b is taken by this CEC device
13	RW	0	**CEC Logical Address 13 Occupation** 0: CEC Logical Address 1101b is not taken by this CEC device 1: CEC Logical Address 1101b is taken by this CEC device
12	RW	0	**CEC Logical Address 12 Occupation** 0: CEC Logical Address 1100b is not taken by this CEC device 1: CEC Logical Address 1100b is taken by this CEC device
11	RW	0	**CEC Logical Address 11 Occupation** 0: CEC Logical Address 1011b is not taken by this CEC device 1: CEC Logical Address 1011b is taken by this CEC device
10	RW	0	**CEC Logical Address 10 Occupation** 0: CEC Logical Address 1010b is not taken by this CEC device 1: CEC Logical Address 1010b is taken by this CEC device
9	RW	0	**CEC Logical Address 9 Occupation** 0: CEC Logical Address 1001b is not taken by this CEC device 1: CEC Logical Address 1001b is taken by this CEC device
8	RW	0	**CEC Logical Address 8 Occupation** 0: CEC Logical Address 1000b is not taken by this CEC device 1: CEC Logical Address 1000b is taken by this CEC device
7	RW	0	**CEC Logical Address 7 Occupation** 0: CEC Logical Address 0111b is not taken by this CEC device 1: CEC Logical Address 0111b is taken by this CEC device
6	RW	0	**CEC Logical Address 6 Occupation** 0: CEC Logical Address 0110b is not taken by this CEC device 1: CEC Logical Address 0110b is taken by this CEC device
5	RW	0	**CEC Logical Address 5 Occupation** 0: CEC Logical Address 0101b is not taken by this CEC device 1: CEC Logical Address 0101b is taken by this CEC device
4	RW	0	**CEC Logical Address 4 Occupation** 0: CEC Logical Address 0100b is not taken by this CEC device 1: CEC Logical Address 0100b is taken by this CEC device
3	RW	0	**CEC Logical Address 3 Occupation** 0: CEC Logical Address 0011b is not taken by this CEC device 1: CEC Logical Address 0011b is taken by this CEC device
2	RW	0	**CEC Logical Address 2 Occupation** 0: CEC Logical Address 0010b not taken by this CEC device 1: CEC Logical Address 0010b is taken by this CEC device
1	RW	0	**CEC Logical Address 1 Occupation** 0: CEC Logical Address 0001b is not taken by this CEC device 1: CEC Logical Address 0001b is taken by this CEC device
0	RW	0	**CEC Logical Address 0 Occupation** 0: CEC Logical Address 0000b is not taken by this CEC device 1: CEC Logical Address 0000b is taken by this CEC device

Offset Address: 22-2Fh (CEC-MMIO) – Reserved

Offset Address: 30h (CEC-MMIO)
CEC TX Block Size Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0	**CEC Message Block Size** This register indicates the block count to be issued by initiator which is configured by SW. The message block size = The value of this register + 1.

Offset Address: 31-33h (CEC-MMIO) – Reserved

Offset Address: 34h (CEC-MMIO)

CEC RX Block Count Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RO	0	**CEC Line Block count** This register should be accessed only when a read transaction is just finished. Rx08[0] =1 and Rx04[7] =1. It indicates the received block count. The received message block size = The value of this register + 1. Read this register in any other time may get an invalid value.

Offset Address: 35-39h (CEC-MMIO) – Reserved

Offset Address: 3B-3Ah (CEC-MMIO)

CEC RX EOM Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**CEC RX EOM** This register stores the received EOM of every byte. Bit [15] is EOM for RX Data block register [127:120], bit [0] is EOM for RX Data block register [7:0].

Offset Address: 3C-3Dh (CEC-MMIO) – Reserved

Offset Address: 3F-3Eh (CEC-MMIO)

CEC TX ACK Register **Default Value: FFFFh**

Bit	Attribute	Default	Description
15:0	RO	FFFFh	**CEC TX ACK** This register stores the received ACK of every byte. Bit [15] is ACK for TX Data block register [127:120],…, bit [0] is ACK for TX Data block register [7:0]

Offset Address: 40-4Fh (CEC-MMIO) – Reserved

Offset Address: 5F-50h (CEC-MMIO)
CEC TX Data Block Register **Default Value: FF00 0000 0000 0000 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
127:124	RW	1111b	**CEC TX Initiator Logic Address** This field contains the 4-bit address of the initiator.
123:120	RW	1111b	**CEC TX Destination Logic Address** This field contains the 4-bit address of the follower.
119:112	RW	0	**CEC TX Opcode Block Data** This field contains the opcode data of CEC message.
111:0	RW	0	**CEC TX Operand Block Data** This field contains the operand data of CEC message.

Offset Address: 60-6Fh (CEC-MMIO) – Reserved

Offset Address: 7F-70h (CEC-MMIO)
CEC RX Data Block Register **Default Value: 0000 0000 0000 0000 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
127:124	RO	0	**CEC RX Initiator Logic Address** This field contains the 4-bit address of the initiator.
123:120	RO	0	**CEC RX Destination Logic Address** This field contains the 4-bit address of the follower.
119:112	RO	0	**CEC RX Opcode Block Data** This field contains the opcode data of CEC message.
111:0	RO	0	**CEC RX Operand Block Data** This field contains the operand data of CEC message (not more than 14 Bytes).

Offset Address: 80-BFh (CEC-MMIO) – Reserved

Offset Address: C1-C0h (CEC-MMIO)
CEC TX Timeout Control Register **Default Value: FFFFh**

Bit	Attribute	Default	Description
15:0	RW	FFFFh	**CEC TX Timeout Control** 0000: Do not check TX time out 0001: 1/32 ms …… FFFF: 2048 ms The TX timeout report time is the value of this register * 1/32 (ms)

Offset Address: C2-FFh (CEC-MMIO) – Reserved

HPET MMIO Space

These register addresses are offsets from the "HPET (High Precision Event Timer) Memory Base Address" in the MMIO space, which are located in D17F0 Rx6B-69.

HPET MMIO Control Registers (00-148h)

Offset Address: 07-00h (HPET-MMIO)

General Capabilities and ID **Default Value: 0429 B17F 1106 8201h**

Bit	Attribute	Default	Description
63:32	RO	0429 B17Fh	**Main Counter Tick Period** This read-only field indicates the period at which the counter increments in femtoseconds (10^-15 seconds). A value of 0 in this field is not permitted. The value in this field must be less than or equal to 05F5 E100h (10^8 femtoseconds = 100 nanoseconds). The resolution must be in femtoseconds (rather than picoseconds) in order to achieve a resolution of 50 ppm.
31:16	RO	1106h	**VIA Technologies ID Code**
15	RO	1b	**LegacyReplacement Route Capable** 1 indicates that the hardware supports the LegacyReplacement Interrupt Route option.
14	RO	0	**Reserved**
13	RO	0	**Counter Size** 0: Indicates that the main counter is 32 bits wide (and cannot operate in 64-bit mode). 1: Indicates that the main counter is 64 bits wide (although this does not preclude it from being operated in a 32-bit mode).
12:8	RO	02h	**Number of Timers** This indicates the number of timers in this block. The number in this field indicates the last timer (i.e. if there are three timers, the value will be 02h, four timers will be 03h, five timers will be 04h, etc.).
7:0	RO	01h	**Revision ID** This indicates which revision of the function is implemented. The value must not be 01h.

Offset Address: 08-0Fh (HPET-MMIO) – Reserved

Offset Address: 17-10h (HPET-MMIO)

General Configuration **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:2	RO	0	**Reserved**
1	RW	0	**LegacyReplacement Route** 0: Not support LegacyReplacement Route 1: Support LegacyReplacement Route If bit 0 and the this bit are both set, the interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in Non-APIC or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in Non-APIC or IRQ8 in the I/O APIC Timer 2 will be routed as per routings in Timer 2 configure registers. If the LegacyReplacement Route bit is set, the individual routing bits for timers 0 and 1 will have no impact. If the LegacyReplacement Route bit is not set, the individual routing bits for each of the timers will be used.
0	RW	0	**Overall Enable** 0: Halt main counter and disable all timer interrupts 1: Allow main counter to run and enable timer interrupts This bit must be set to enable whichever timers to generate interrupts. If this bit is 0, the main counter will not increment and no interrupts will be caused by any of these timers.

Offset Address: 18-1Fh (HPET-MMIO) – Reserved

Offset Address: 27-20h (HPET-MMIO)

General Interrupt Status **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:3	RO	0	**Reserved**
2	RW1C	0	**Timer 2 Interrupt Active** Same functionality as Timer 0. Refer to the description of bit[0].
1	RW1C	0	**Timer 1 Interrupt Active** Same functionality as Timer 0. Refer to the description of bit[0].
0	RW1C	0	**Timer 0 Interrupt Active** The functionality of this bit depends on whether the edge or level-triggered mode is used for this timer. ***Level-triggered Mode*:** In this mode, this bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a 1 to the same bit position. In this case, writes of 0 to this bit will have no effect. That is, if the bit is already set, a write of 0 will not clear the bit. ***Edge-triggered Mode*:** In this mode, this bit should be ignored by software. Software should always write 0 to this bit.

Offset Address: 28-EFh (HPET-MMIO) – Reserved

Offset Address: F3-F0h (HPET-MMIO)

Main Counter Value **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Main Counter Value** Bits [31:0] of the counter.

Offset Address: F4-FFh (HPET-MMIO) – Reserved

Offset Address: 107-100h (HPET-MMIO)

Timer 0 Configuration & Capability **Default Value: 000F 0000 0000 0010h**

Bit	Attribute	Default	Description
63:32	RO	000F 0000h	**Timer 0 Interrupt Routing Capability** This 32-bit field indicates to which interrupts in the I/O (x) APIC this timer's interrupt can be routed. This is used in conjunction with bits [13:9] field. Each bit in this field corresponds to a particular interrupt. For example, if this timer's interrupt is mapped to interrupts 16, 18, 20, 22, or 24, bits 16, 18, 20, 22 and 24 in this field will be set to 1 while all other bits will be 0.
31:15	RO	0	**Reserved**
14	RW	0	**Reserved**
13:9	RW	0	**Timer 0 Interrupt Route** This 5-bit read/write field indicates the routing for the interrupt to the I/O APIC. A maximum value of 32 interrupts is supported. Default is 00h. Software writes to this field to select which interrupt in the I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, the value read back will not match what is written. The software must only write valid values. Note: If the LegacyReplacement Route bit is set, Timers 0 and 1 will have different routings, and this bit field has no effect on both timers.
8	RO	0	**Timer 0 32-Bit Mode** Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is particularly needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, this bit will always be read as 0 and writes will have no effect.
7	RO	0	**Reserved**
6	RO	0	**Timer 0 Value Set** Software uses this read/write bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set a periodic timer's accumulator. Software does not have to write this bit back to 0 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode.
5	RO	0	**Timer 0 Size** This read-only field indicates the size of the timer. 0: 32 bits 1: 64 bits
4	RO	1b	**Timer 0 Periodic Interrupt Capable** If this read-only bit is 1, the hardware will support a periodic mode for this timer's interrupt.
3	RW	0	**Timer 0 Type** ***If bit 4 is 0:*** this bit will always return 0 when read and writes have no impact. ***If bit 4 is 1:*** this bit is in read/write mode, and can be used to enable the timer to generate a periodic interrupt. Writing a 1 to this bit enables the timer to generate a periodic interrupt. Writing a 0 to this bit enables the timer to generate a non-periodic interrupt.
2	RW	0	**Timer 0 Interrupt Enable** This read/write-able bit must be set to enable timer n to cause an interrupt when the timer event fires. 0: Disable 1: Enable Note: If this bit is 0, the timer will still operate and generate appropriate status bits, but will not cause an interrupt.
1	RW	0	**Timer 0 Interrupt Type** 0: The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1: The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active.
0	RO	0	**Reserved**

Offset Address: 10F-108h (HPET-MMIO)

Timer 0 Comparator Value **Default Value: 0000 0000 FFFF FFFFh**

Bit	Attribute	Default	Description
63:32	RO	0	**Reserved**
31:0	RW	FFFF FFFFh	**Timer 0 Comparator** Bits [31:0] of the comparator value.

Offset Address: 110-11Fh (HPET-MMIO) – Reserved

Offset Address: 127-120h (HPET-MMIO)

Timer 1 Configuration & Capability **Default Value: 000F 0000 0000 0010h**

Bit	Attribute	Default	Description
63:32	RO	000F 0000h	**Timer 1 Interrupt Routing Capability** This 32-bit field indicates to which interrupts in the I/O (x) APIC this timer's interrupt can be routed. This is used in conjunction with bits [13:9] field. Each bit in this field corresponds to a particular interrupt. For example, if this timer's interrupt is mapped to interrupts 16, 18, 20, 22, or 24, bits 16, 18, 20, 22 and 24 in this field will be set to 1 while all other bits will be 0.
31:15	RO	0	**Reserved**
14	RW	0	**Reserved**
13:9	RW	0	**Timer 1 Interrupt Route** This 5-bit read/write field indicates the routing for the interrupt to the I/O APIC. A maximum value of 32 interrupts is supported. Default is 00h. Software writes to this field to select which interrupt in the I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, the value read back will not match what is written. The software must only write valid values. Note: If the LegacyReplacement Route bit is set, Timers 0 and 1 will have different routings, and this bit field has no effect on both timers.
8	RO	0	**Timer1 32-Bit Mode** Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is particularly needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, this bit will always be read as 0 and writes will have no effect.
7	RO	0	**Reserved**
6	RO	0	**Timer 1 Value Set** Software uses this read/write bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set a periodic timer's accumulator. Software does not have to write this bit back to 0 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode.
5	RO	0	**Timer1 Size** This read-only field indicates the size of the timer. 0: 32 bits 1: 64 bits
4	RO	1b	**Timer 1 Periodic Interrupt Capable** If this read-only bit is 1, the hardware will support a periodic mode for this timer's interrupt.
3	RW	0	**Timer 1 Type** ***If bit 4 is 0:*** this bit will always return 0 when read and writes have no impact. ***If bit 4 is 1:*** this bit is in read/write mode, and can be used to enable the timer to generate a periodic interrupt. Writing a 1 to this bit enables the timer to generate a periodic interrupt. Writing a 0 to this bit enables the timer to generate a non-periodic interrupt.
2	RW	0	**Timer 1 Interrupt Enable** This read/write-able bit must be set to enable timer n to cause an interrupt when the timer event fires. 0: Disable 1: Enable Note: If this bit is 0, the timer will still operate and generate appropriate status bits, but will not cause an interrupt.
1	RW	0	**Timer 1 Interrupt Type** 0: The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1: The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active.
0	RO	0	**Reserved**

Offset Address: 12F-128h (HPET-MMIO)

Timer 1 Comparator Value **Default Value: 0000 0000 FFFF FFFFh**

Bit	Attribute	Default	Description
63:32	RO	0	**Reserved**
31:0	RW	FFFF FFFFh	**Timer 1 Comparator** Bits [31:0] of the comparator value.

Offset Address: 130-13Fh (HPET-MMIO) – Reserved

Offset Address: 147-140h (HPET-MMIO)

Timer 2 Configuration & Capability **Default Value: 000F 0800 0000 0010h**

Bit	Attribute	Default	Description
63:32	RO	000F 0800h	**Timer 2 Interrupt Routing Capability** This 32-bit field indicates to which interrupts in the I/O (x) APIC this timer's interrupt can be routed. This is used in conjunction with bits [13:9] field. Each bit in this field corresponds to a particular interrupt. For example, if this timer's interrupt is mapped to interrupts 16, 18, 20, 22, or 24, bits 16, 18, 20, 22 and 24 in this field will be set to 1 while all other bits will be 0.
31:15	RO	0	**Reserved**
14	RW	0	**Reserved**
13:9	RW	0	**Timer 2 Interrupt Route** This 5-bit read/write field indicates the routing for the interrupt to the I/O APIC. A maximum value of 32 interrupts is supported. Default is 00h. Software writes to this field to select which interrupt in the I/O (x) will be used for this timer's interrupt. If the value is not supported by this particular timer, the value read back will not match what is written. The software must only write valid values. Note: If the LegacyReplacement Route bit is set, Timers 0 and 1 will have different routings, and this bit field has no effect on both timers.
8	RO	0	**Timer 2 32-Bit Mode** Software can set this read/write bit to force a 64-bit timer to behave as a 32-bit timer. This is particularly needed if the software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of doing an atomic 64-bit read to the timer. If the timer is not 64 bits wide, this bit will always be read as 0 and writes will have no effect.
7	RO	0	**Reserved**
6	RO	0	**Timer 2 Value Set** Software uses this read/write bit only for timers that have been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set a periodic timer's accumulator. Software does not have to write this bit back to 0 (it automatically clears). Software should not write a 1 to this bit position if the timer is set to non-periodic mode.
5	RO	0	**Timer 2 Size** This read-only field indicates the size of the timer. 0: 32 bits 1: 64 bits
4	RO	1b	**Timer 2 Periodic Interrupt Capable** If this read-only bit is 1, the hardware will support a periodic mode for this timer's interrupt.
3	RW	0	**Timer 2 Type** ***If bit 4 is 0:*** this bit will always return 0 when read and writes have no impact. ***If bit 4 is 1:*** this bit is in read/write mode, and can be used to enable the timer to generate a periodic interrupt. Writing a 1 to this bit enables the timer to generate a periodic interrupt. Writing a 0 to this bit enables the timer to generate a non-periodic interrupt.
2	RW	0	**Timer 2 Interrupt Enable** This read/write-able bit must be set to enable timer n to cause an interrupt when the timer event fires. 0: Disable 1: Enable Note: If this bit is 0, the timer will still operate and generate appropriate status bits, but will not cause an interrupt.
1	RW	0	**Timer 2 Interrupt Type** 0: The timer interrupt is edge triggered. This means that an edge-type interrupt is generated. If another interrupt occurs, another edge will be generated. 1: The timer interrupt is level triggered. This means that a level-triggered interrupt is generated. The interrupt will be held active until it is cleared by writing to the bit in the General Interrupt Status Register. If another interrupt occurs before the interrupt is cleared, the interrupt will remain active.
0	RO	0	**Reserved**

Offset Address: 14F-148h (HPET-MMIO)

Timer 2 Comparator Value **Default Value: 0000 0000 FFFF FFFFh**

Bit	Attribute	Default	Description
63:32	RO	0	**Reserved**
31:0	RW	FFFF FFFFh	**Timer 2 Comparator** Bits [31:0] of the comparator value.

SPI Bus 0 MMIO Register Space

MMIO Register (00-87h)

The SPI Bus 0 MMIO base register (SPI0BAR) is located in D17F0 MMIO Rx003-001, whose base register is derived from D17F0 RxBE-BC.

Offset Address: 01-00h (SPI0-MMIO)

SPI Status (SPIS) **Default Value: 0002h**

Bit	Attribute	Default	Description
15	RO/RW	0	**SPI Configuration Lock-Down** 0: No lock-down 1: SPI static configuration information from Rx50 to Rx6F cannot be overwritten. Once set to 1, this bit can only be cleared through hardware reset.
14:5	RO	0	**Reserved**
4	RO	0	**Strapping Value of BIOS Boot from SPI ROM** 0: Boot from other device 1: Boot from SPI ROM Default sets from the strapping signal AZBITCLK during system initialization.
3	RW1C	0	**Blocked Access Status** 0: Not blocked 1: Blocked Hardware sets this bit to 1 when an access is blocked from running on the SPI interface due to one of the protection policies, or when any of the programmed cycle register is written while a programmed access is already in progress. This bit is set for both programmed accesses and direct memory reads that get blocked. This bit remains asserted until cleared by software writing a 1 or hardware reset.
2	RW1C	0	**SPI Bus 0 Cycle Done Status** 0: Not done 1: SPI controller completes the SPI cycle after software sets bit Rx02[1]. This bit remains asserted until cleared by software writing a 1 or hardware reset. Software must make sure this bit is cleared prior to a new programmed access. This bit must be set to "0" after the Status Register Polling sequence completes. It is cleared before and during that sequence.
1	RO	1b	**SPI Bus Internal FIFO Empty Flag** 0: FIFO is not empty 1: FIFO is empty
0	RO	0	**SPI Cycle Progress** 0: Cycle not in progress 1: Cycle in progress Hardware sets this bit when software sets Rx02[1]. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must program the next command only when this bit is 0. This bit is only valid at PIO mode.

Offset Address: 03-02h (SPI0-MMIO)

SPI Control (SPIC) **Default Value: 4004h**

Bit	Attribute	Default	Description
15	RW	0	**SPI SMI# Enable** 0: Disable 1: Enable The SPI asserts the SMI# request whenever Rx00[2] Cycle Done Status bit is set.
14	RW	1b	**Data Cycle** 0: No data is delivered for this cycle. The Data Byte Count (DBC) and data fields are ignored. 1: There are data corresponding to this transaction.
13:12	RW	00b	**Bus 0 Port Select[1:0]** Bus 0 can connect three devices, these two bits select to which device the cycle will go. 00: Select device 0 (CS0). When SPI Strapping Pin = 1, this port connects to SPI ROM. When SPI Strapping Pin = 0, this port connects to SPI device. 01: Select device 1 (CS1). Connects to SPI device. 10: Reserved 11: Reserved
11:8	RW	0	**Data Byte Count** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid setting can be any value from 0 to 15. The number of bytes transferred is the value of this field plus 1.
7	RW	0	**Data Atomic Cycle Sequence** 0: No data atomic cycle sequence. 1: When set to 1 along with the SPI Cycle Go (bit 1) assertion, the chip will execute a sequence of data on the SPI interface. SPI will not transfer address again.
6:4	RW	0	**Cycle Opcode Pointer** The field selects one of the programmed opcodes in the Opcode Menu and uses it as the SPI command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	RW	0	**Sequence Prefix Opcode Pointer** 0: Points to the opcode in the ***least*** significant byte of the Prefix Opcodes register 1: Points to the opcode in the ***maximum*** significant byte of the Prefix Opcodes register This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. By making this programmable, this chip supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	RW	1b	**Atomic Cycle Sequence** 0: No atomic cycle sequence 1: When set to 1 along with bit 1 assertion, the chip will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles.
1	RW	0	**SPI Cycle Go** 0: SPI cycle not started 1: Set this bit to 1 to start the SPI cycle defined by the other bits in this register. Rx00[0] SPI Cycle in Progress gets set through this action. This bit always returns 0 on reads. Writes to this bit will be ignored if Cycle In Progress bit is set. Other bits in this register can be programmed for the same transaction when writing this bit to 1.
0	RW	0	**SPI Fast Read Enable** 0: Disable 1: Enable

Offset Address: 07-04h (SPI0-MMIO)
SPI Address (SPIA) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**SPI Cycle Address [23:0]** This field is shifted out as the SPI Address (MSb first).

Offset Address: 0F-08h (SPI0-MMIO)
SPI Data 0 Register (SPID0) **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**SPI Cycle Data[0]** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin during the data portion of the SPI cycle. The register also shifts in the data from the Master-In Slave-Out pin into this register during the data portion of the SPI cycle. The data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

Offset Address: 17-10h (SPI0-MMIO)
SPI Data 1 Register (SPID1) **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RW	0	**SPI Cycle Data[1]** (Same as SPID0)

Notes for SPI Cycle Data:

SCD Memory Address
SPI Data[0]: SPI0BAR + 08h (Size:64bits)
SPI Data[1]: SPI0BAR + 10h (Size:64bits)
SPI Data[2..7]: SPI0BAR + (18h~47h) Reserved

SCD Shift Order
The SCD[N] register does not begin shift until SPID[N-1] has completely shifted in/out. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-…-8-23-22-…-16-31…-24-39..32…-etc. Bit 56 is the last bit shifted out/in.

Default
1. For SPI Data [7:1]: Default values are 0.
2. For SPI Data 0: This register is initialized to 0 by the reset assertion. However, the least significant byte of this register is loaded with the first Status Register read of the Atomic Cycle Sequence that the hardware automatically runs out of reset. Therefore, bit 0 of this register can be read later to determine if the platform encountered the boundary case in which the SPI flash was busy with an internal instruction when the platform reset deasserted.

Offset Address: 18-4Fh (SPI0-MMIO) – Reserved

Offset Address: 53-50h (SPI0-MMIO)

BIOS Base Address (BBAR) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:8	RW	0	**Bottom of System Flash** This field determines the bottom of the System BIOS. The chip will not run programmed commands nor memory reads whose address field is less than this value. This field corresponds to bit [23:8] of the 3-Bytes address; bit [7:0] are assumed to be 00h for this vector when comparing to a potential SPI address. Software must always program 1s into the upper, don't-care bits of this field based on the flash size. Hardware does not know the size of the flash array and relies upon the correct programming by software. The default value of 0000h results in all cycles allowed. In the event that this value is programmed below some of the BIOS Memory segments, this protection policy takes precedence.
7:0	RO	0	**Reserved**

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 55-54h (SPI0-MMIO)

Prefix Opcode Configuration (PREOP) **Default Value: 0004h**

Bit	Attribute	Default	Description
15:8	RW	0	**Prefix Opcode 1** Software programs an SPI Opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	RW	04h	**Prefix Opcode 0** Software programs an SPI Opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 57-56h (SPI0-MMIO)

Opcode Type Configuration (OPTYPE) **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RW	00b	**Opcode Type7** (Refer to the description in bits [1:0])
13:12	RW	00b	**Opcode Type6** (Refer to the description in bits [1:0])
11:10	RW	00b	**Opcode Type5** (Refer to the description in bits [1:0])
9:8	RW	00b	**Opcode Type4** (Refer to the description in bits [1:0])
7:6	RW	00b	**Opcode Type3** (Refer to the description in bits [1:0])
5:4	RW	00b	**Opcode Type2** (Refer to the description in bits [1:0])
3:2	RW	00b	**Opcode Type1** (Refer to the description in bits [1:0])
1:0	RW	00b	**Opcode Type0** This field specifies information about the corresponding Opcode 0. This information allows the hardware to: 1) Decide whether to use the address field and 2) Provide BIOS and Shared Flash protection capabilities. The encodings of the two bits are: 00: No address associated with this opcode; read cycle type 01: No address associated with this opcode; write cycle type 10: Address required; read cycle type 11: Address required; write cycle type

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 5F-58h (SPI0-MMIO)
Opcode Menu Configuration (OPMENU) **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:56	RW	0	**Opcode 7** (See the description in bits [7:0].)
55:48	RW	0	**Opcode 6** (See the description in bits [7:0].)
47:40	RW	0	**Opcode 5** (See the description in bits [7:0].)
39:32	RW	0	**Opcode 4** (See the description in bits [7:0].)
31:24	RW	0	**Opcode 3** (See the description in bits [7:0].)
23:16	RW	0	**Opcode 2** (See the description in bits [7:0].)
15:8	RW	0	**Opcode 1** (See the description in bits [7:0].)
7:0	RW	0	**Opcode 0** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 63-60h (SPI0-MMIO)
Protected BIOS Range[0] (PBR0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Write Protection Enable** 0: Disable. The base and limit field are ignored when this bit is cleared. 1: Enable. The base and limit fields in this register are valid.
30:24	RW	0	**Reserved**
23:12	RW	0	**Protected Range Limit** This field corresponds to SPI address bits [23:12] and specifies the upper limit of the protected range. Any address greater than the value programmed in this field is unaffected by this protected range.
11:0	RW	0	**Protected Range Base** This filed corresponds to SPI address [23:12] and specifies the lower base of the protected range. Address bits [11:0] are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Note: This register is not writable when SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 67-64h (SPI0-MMIO)
Protected BIOS Range[1] (PBR1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Register description same as Rx63-60 (PBR[0]).**

Offset Address: 6B-68h (SPI0-MMIO)
Protected BIOS Range[2] (PBR2) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Register description same as Rx63-60 (PBR[0]).**

Offset Address: 6Ch (SPI0-MMIO)
SPI Bus 0 Clock Divider **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**SPI Bus 0 Master Mode Clock Divider Value** 00h indicates original CLK , 48MHz/33MHz. 01h indicates CLK/2*1 MHz. 02h indicates CLK/2*2 MHz. n = value (Rx6C) The exact frequency: CLK/2n MHz For PIO Mode, supports up to 48MHz/33MHz, For DMA Mode, supports up to 33/2 MHz

Offset Address: 6Dh (SPI0-MMIO)
SPI Bus 0 Miscellaneous Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SPI Bus0 Clock Select** 0: 33MHz 1: 48MHz
6	RW	0	**SPI Bus 0 Working Node Select** 0: PIO mode 1: DMA mode
5	RW	0	**Reserved**
4	RW	0	**SPI Bus 0 cycle done Interrupt Enable** 0: Disable (SPI will not send interrupt) 1: Enable (SPI will send interrupt when bus cycle is done)
3	RW	0	**SPI Bus 0 Dynamic Clock On** 0: Free clock 1: Dynamic clock (when SPI controller doesn't receive request from Host, there is no clock in SPI controller)
2:1	RW	0	**Reserved**
0	RW	0	**PIO Mode Command Post Write Enable** 0: Disable 1: Enable (when Host send write cycle to SPI controller in PIO mode, if this bit set to 1,SPI controller will assert write done signal to Host before data transmit done in SPI bus)

Offset Address: 6Eh (SPI0-MMIO)
SPI Bus 0 Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Fix FIFO Underrun Flag Set Condition Incomplete Issue** 0: Disable 1: Enable
2	RW	0	**Latch Master Input Data Edge Selection of Bus CLK** 0: Pos-edge. Latch input data at positive edge of SPI bus clk. 1: Neg-edge. Latch input data at negative edge of SPI bus clk. Note: In PIO mode, when Rx6C is 33MHz / 48MHz, set this bit to 1b.
1:0	RW	00b	**SPI Bus 0 Clock Latency Select When SPI Samples Data** 00: Bypass mode 01: Delay line mode 1 10: Delay line mode 2 11: Delay line mode 3 Note: In DMA mode, when offset Rx6C is 33/2MHz, set this bit to 11b.

Offset Address: 6Fh (SPI0-MMIO) – Reserved

Offset Address: 70h (SPI0-MMIO)

SPI Bus 0 Interrupt Control **Default Value: FFh**

Bit	Attribute	Default	Description
7	RW	1b	**Bus 0 DMA Write Buffer Block B (High Half) Full Interrupt Enable** 0: Disable 1: Enable
6	RW	1b	**Bus 0 DMA Write Buffer Block A (Low Half) Full Interrupt Enable** 0: Disable 1: Enable
5	RW	1b	**Bus 0 DMA Read Buffer Block B (High Half) Empty Interrupt Enable** 0: Disable 1: Enable
4	RW	1b	**Bu s0 DMA Read Buffer Block A (Low Half) Empty Interrupt Enable** 0: Disable 1: Enable
3	RW	1b	**Bus 0 DMA Read Buffer Under Run Interrupt Enable** 0: Disable 1: Enable
2	RW	1b	**Bus 0 DMA Write Buffer Over Run Interrupt Enable** 0: Disable 1: Enable
1	RW	1b	**Bus 0 Data FIFO Under Run Interrupt Enable** 0: Disable 1: Enable
0	RW	1b	**Bus 0 Data FIFO Over Run Interrupt Enable** 0: Disable 1: Enable

Offset Address: 72-71h (SPI0-MMIO)

SPI Bus 0 Cycle Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Bus 0 Length Check Enable** 0: Disable. SPI will continue to transfer/receive data till Rx02[1] is set to 0. The value of Rx72-71[12:0] is "don't care" to SPI controller. 1: Enable. In receive mode, SPI controller will receive data with data length = Rx72-71[12:4]. In transmit mode, SPI controller will send data with data length = Rx71[3:0]. Valid only when Rx02[1] is set to 1.
14:13	RW	00b	**Bus 0 Cycle Type** 00: SPI receive data from device. 01: SPI transmit data to device. 10: SPI transmit data first, then receive data from device (this type needs bit [15]=1). 11: Reserved
12:4	RW	0	**Bus 0 Read Length** Data length which SPI receives from the device.
3:0	RW	0	**Bus 0 Write Length** Data length which SPI sends to the device. Valid when bit 15 = 1. The real length = This register value + 1. Supports up to 16 bytes.

Offset Address: 73h (SPI0-MMIO)

SPI Bus 0 Interrupt Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Bus 0 DMA Write Buffer Block B (High Half) Status** 0: Not full 1: Full When DMA Write Buffer has been fully written, it means from (Rx7B-78 + Rx7F-7E/2) to (Rx7B-78 + Rx7F-7E) has been written, and this status is set to 1.
6	RW1C	0	**Bus 0 DMA Write Buffer Block A (Low Half) Status** 0: Not full 1: Full When DMA Write Buffer has been half written, it means from Rx7B-78 to (Rx7B-78 + Rx7F-7E/2) has been written, and this status is set to 1.
5	RW1C	0	**Bus 0 DMA Read Buffer Block B (High Half) Status** 0: Not empty 1: Empty When DMA Read Buffer has been fully read, it means from (Rx77-74 + Rx7D-7C/2) to (Rx77-74 + Rx7D-7C) has been read, and this status is set to 1.
4	RW1C	0	**Bus 0 DMA Read Buffer Block A (Low Half) Status** 0: Not empty 1: Empty When DMA Read Buffer has been half read, from Rx77-74 to (Rx77-74 + Rx7D-7C/2) has been read, and this status is set to 1.
3	RW1C	0	**Bus 0 DMA Read Buffer Underrun Status** 0: Not underrun 1: Underrun
2	RW1C	0	**Bus 0 DMA Write Buffer Overrun Status** 0: Not overrun 1: Overrun
1	RW1C	0	**Bus 0 Data FIFO Underrun Status** 0: Not underrun 1: Underrun
0	RW1C	0	**Bus 0 Data FIFO Overrun Status** 0: Not overrun 1: Overrun

Offset Address: 77-74h (SPI0-MMIO)

SPI Bus 0 DMA Read Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Bus 0 DMA Read Buffer Base Address[31:2]** 4-byte alignment.
1:0	RW	0	**Reserved**

Offset Address: 7B-78h (SPI0-MMIO)

SPI Bus 0 DMA Write Buffer Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Bus 0 DMA Write Buffer Base Address [31:2]** 4-byte alignment.
1:0	RW	0	**Reserved**

Offset Address: 7D-7Ch (SPI0-MMIO)

SPI Bus 0 DMA Read Buffer Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Bus 0 DMA Read Buffer Length** 4-byte alignment.

Offset Address: 7F-7Eh (SPI0-MMIO)

SPI Bus 0 DMA Write Buffer Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Bus 0 DMA Write Buffer Length** 4-byte alignment.

Offset Address: 83-80h (SPI0-MMIO)

SPI Bus 0 DMA Read Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Bus 0 DMA Read Pointer** Indicates the address for SPI controller to get data from DMA read buffer. These registers can be used to monitor SPI cycle process during DMA mode. The max length that SPI request CCA bus is 8DW.

Offset Address: 87-84h (SPI0-MMIO)

SPI Bus 0 DMA Write Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Bus 0 DMA Write Pointer** Indicates the address for SPI controller to put data to DMA write buffer. These registers can be used to monitor SPI cycle process during DMA mode. The max length that SPI request CCA bus is 8DW.

DEVICE 17 FUNCTION 7 (D17F7): SOUTH-NORTH MODULE INTERFACE CONTROL

PCI Configuration Space

This configuration is provided to facilitate the configuration of the North Module Interface logic of the South Module ("SM") without requiring new enumeration code. This function is represented as Device 17, Function 7.

Header Registers (00-3Fh)

Offset Address: 01-00h (D17F7)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D17F7)

Device ID **Default Value: A353h**

Bit	Attribute	Default	Description
15:0	RO	A353h	**Device ID**

Offset Address: 05-04h (D17F7)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RW	0	**SERR# Enable** 0: Disable 1: Enable
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0. (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0. (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0. (Not supported)
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RO	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D17F7)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RW1C	0	**Signaled System Error (SERR# Asserted)**
13	RW1C	0	**Received Master-Abort (Except Special Cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion**
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Set When Set or Observed SERR# and Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Reserved
6	RO	0	**Reserved**
5	RO	0	**66 MHz Capable**
4	RO	0	**Capability List** 0: No new capability linked list 1: Available. Implement the pointer for a new capability linked at Rx34.
3:0	RO	0	**Reserved**

Offset Address: 08h (D17F7)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-09h (D17F7)

PCI Header Registers **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D17F7) – Reserved

Offset Address: 0Dh (D17F7)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice Bits [7:3] for CPU as A Master (In Unit of PCI Clocks)** Bits [7:3] is programmable; however it is always read as 0 if RxE0[5] = 1.
2:0	RO	0	**Reserved**

Offset Address: 0Eh (D17F7)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device. It adheres to the PCI-PCI Bridge Configuration.

Offset Address: 0Fh (D17F7)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST**
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D17F7) – Reserved

Offset Address: 2D-2Ch (D17F7)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D17F7)
Subsystem ID **Default Value: A353h**

Bit	Attribute	Default	Description
15:0	RO	A353h	**Subsystem ID**

Offset Address: 30-33h (D17F7) – Reserved

Offset Address: 34h (D17F7)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer** Byte offset in configuration space, points to next capability list. 0 indicates the end of the list.

Offset Address: 35-3Fh (D17F7) – Reserved

South -North Module Interface Control (40-5F)

Offset Address: 40-4Eh (D17F7) – Reserved

Offset Address: 4Fh (D17F7)

South-North Module Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Improve P2CR (PCI Master to DRAM Read Cycle) Performance** 0: Disable 1:Enable
2	RW	0	**Reserved**
1	RW	0	**Support Extended Configuration Space Up to 4096 Bytes** 0: Disable 1: Enable
0	RW	0	**C2P Cycle Wait till P2C Write Flushed (Except C2P Post-Write)** 0: Disable. CPU to PCI Peripheral Device Read is not blocked. 1: Enable. CPU to PCI Peripheral Device Read waits for PCI1 P2C write FIFO empty. For details, please refer to Rx77[6].

Offset Address: 50h (D17F7)

Bus Priority of SM Peripheral Device 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Card Reader Priority** 0: Low Priority 1: High Priority
6	RW	0	**SDIO Priority** 0: Low Priority 1: High Priority
5	RW	0	**SATA Priority** 0: Low Priority 1: High Priority
4	RW	0	**USB Priority** 0: Low Priority 1: High Priority
3	RW	0	**HDAC Priority** 0: Low Priority 1: High Priority
2	RW	0	**Reserved**
1	RW	0	**LPC / UART / FIR Priority** 0: Low Priority 1: High Priority
0	RW	0	**PCI1 Priority** 0: Low Priority 1: High Priority

Offset Address: 51h (D17F7)

P2P Bridge Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**P2P Cycle Whose AD Not Fall in DRAM Range Will Be Up to NB** This bit becomes effective when Rx4F[6] = 1. 0: Disable 1: Enable
6	RW	0	**Bypass Asynchronous Circuit in Speed Mode**
5:3	RW	0	**Reserved**
2	RW	0	**Enable PCI Master Function** 0: Enable PCI master function by D19F0 Rx04[2]. 1: Enable PCI master function even when D19F0 Rx04[2] is disabled.
1	RW	0	**Patch for PCCA Decode Bus 0 Device 1 Function 0** 0: Decode B0D1F0 configuration cycle 1: Do not decodeB0D1F0 configuration cycle
0	RW	0	**Support Subtract Decode in PCI to PCI Bridge Class Code** 0: Class code will be 060400 as positive decode P2P Bridge 1: Class code will be 060401 as subtractive decode P2P Bridge

Offset Address: 52h (D17F7)

CCA Arbitration Occupy Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**SM Internal Device Occupy Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants
3:0	RW	0001b	**HDAC Occupy Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants

Offset Address: 53h (D17F7)

CCA Arbitration Promote Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**SM Internal Device Promote Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants
3:0	RW	0001b	**HDAC Promote Timer** 0000: Disable timer, granted as long as request asserted 0001 : Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants

Offset Address: 54h (D17F7)

CCA REQ Timing Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Synchronize VART REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
6	RW	0	**Synchronize SPI REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
5	RW	0	**Synchronize Card Reader REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
4	RW	0	**Synchronize SDIO REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
3	RW	0	**Synchronize USBD REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
2	RW	0	**Synchronize SATA REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
1	RW	0	**Synchronize USB REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
0	RW	0	**Synchronize LPC / ISA REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using

Offset Address: 55h (D17F7)

RIOPU for PAD **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:3	RW	00001b	**Reserved (Do Not Program)**
2	RW	1b	**IRQ14, PDIOR#, PDIOW# Signal Pad Internal Pull-Up** 0: Disable 1: Enable
1	RW	1b	**Reserved (Do Not Program**
0	RW	1b	**FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR# Signal Pad Internal Pull-Up** 0: Disable 1: Enable

Offset Address: 56h (D17F7)

Strapping Pin Value **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Enable Debug Link** 0: Disable 1: Enable Default sets from the strapping signals MSPISS1# during system initialization.
6	RO	0	**Reserved**
5	RO	0	**Enable PCI Master Mode** 0: Disable 1: Enable Default sets from the strapping signals MSPISS0# during system initialization.
4	RO	0	**Enable Debug Link** 0: Disable 1: Enable Default sets from the strapping signals MSPISS1# during system initialization.
3	RO	0	**Reserved**
2	RO	0	**LPC FWH Command** 0: Disable 1: Enable Default sets from the strapping signal AZSYNC during system initialization.
1	RO	0	**System Auto Reboot** 0: Enable 1: Disable Default sets from the strapping signal AZSDOUT during system initialization.
0	RO	0	**SPI / LPC ROM Select** 0: LPC ROM 1: SPI ROM Default sets from the strapping signal AZBITCLK during system initialization.

Offset Address: 57-5Fh (D17F7) – Reserved

DRAM Configuration (60h)

Offset Address: 60h (D17F7)

DRAM Ending for Bank 7 **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**DRAM Bank 7 Ending Address High (Host Address Bits[31:24])**

Shadow RAM Control (61-6Fh)

Offset Address: 61h (D17F7)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFFh Memory Space Access Control** 00: Disable both read and write 01: Enable write 10: Enable read 11: Enable both read and write
5:4	RW	00b	**C8000-CBFFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
3:2	RW	00b	**C4000-C7FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
1:0	RW	00b	**C0000-C3FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)

Offset Address: 62h (D17F7)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**D8000-DBFFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
3:2	RW	00b	**D4000-D7FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
1:0	RW	00b	**D0000-D3FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)

Offset Address: 63h (D17F7)

Page-E / F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**E0000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**F0000-FFFFFh Memory Space Access Control** See bits [7:6] descriptions.
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1:0	RW	0	**Reserved**

Offset Address: 64h (D17F7)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**E8000-EBFFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
3:2	RW	00b	**E4000-E7FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)
1:0	RW	00b	**E0000-E3FFFh Memory Space Access Control** (See bits [7:6] for bit value descriptions.)

Offset Address: 65-6A (D17F7) – Reserved

Offset Address: 6Bh (D17F7)

Reserved **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RW	80h	**Reserved**

Offset Address: 6C-6Fh (D17F7) – Reserved

Conventional PCI Bus Control (70-7Fh)

Offset Address: 70h (D17F7)

CPU to PCI Flow Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU to PCI(C2P) Post-Write** 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).
6	RW	0	**PCI Delay Transaction for Master Read when Timer Time-Out** 0: Disable 1: Enable To enable this function, RxE3[0] must be set to 1. When this bit is set, the PCI controller will assert STOP# when a PCI master read occupies the PCI bus longer than the PCI Master Timer period. PCI Master Timer is set up through Rx75[2:0]. If RxE3[0] is not set concurrently, then STOP# will NOT be asserted even after the timer times out in the following conditions: GNTPK is on. There is only one PCI master request.
5:4	RW	00b	**PCI Master to DRAM Prefetch Control** 00: Always prefetch 10: Prefetch only for enhancing command x1: Disable prefetch
3	RW	0	**PCI Delay Transaction for Master Read** 0: Disable 1: Assert STOP# for PCI master read cycle and start delay transaction.
2	RW	0	**Reserved**
1	RW	0	**Delay Transaction** 0: Disable 1: Enable
0	RW	0	**Cache Line Size** 0: 4QW 1: 8QW

Offset Address: 71h (D17F7)

CPU to PCI Flow Control 2 **Default Value: 48h**

Bit	Attribute	Default	Description
7	RW1C	0	**Retry Status** 0: No retry occurred 1: Retry occurred
6	RW	1b	**Action When Retry Timeout** 0: Continuous retry (record status only) 1: Flush buffer (write) or return 0FFFFFFFFh (read)
5:4	RW	00b	**Retry Count (Before Back Off CPU)** 00: Retry 2 times 01: Retry 16 times 10: Retry 4 times 11: Retry 64 times
3	RW	1b	**PCI Burst Timeout Enable** 0: Disable 1: Enable
2	RW	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle AD31** 0: Fixed AD31 1: Support type#1 configuration cycle
0	RW	0	**Reserved**

Offset Address: 72h (D17F7)

PCI P2C Read Caching and Prefetch Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**No Arbitration on PCI Bus during PCI-DMA Period** 0: Disable 1: Enable
6	RW	0	**Reserved**
5	RW	0	**Conservative Read Caching** 0: Disable 1: Enable If this bit is set to 1, the previous prefetched data will be flushed when PCI master changes or starting address is not consecutive.
4	RW	0	**Reserved**
3	RW	0	**P2CR Pre-fetched Data Flushing Condition** 0: Pre-fetched data will only be flushed when C2P cycle occurs or when interrupt comes. 1: Besides the above conditions, the pre-fetched data will also be flushed when the next FRAME# comes with different REQ/GNT or address.
2	RW	0	**P2CR Pre-fetched Data Control** 0: Pre-fetched data is invalidated when FRAME# is de-asserted without STOP. 1: Pre-fetched data is invalidated based on the setting of bit 3.
1:0	RW	00b	**P2CR FIFO Prefetch Depth** 00: Prefetch if outstanding read <= 1 line 01: Prefetch if outstanding read <= 2 line 10: Prefetch if outstanding read <= 3 line 11: Prefetch if outstanding read <= 5 line

Offset Address: 73h (D17F7)

PCI Master Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**PCI Master 1-Wait State Write** 0: Disable 1: Enable
5	RW	0	**PCI Master 1-Wait State Read** 0: Disable 1: Enable
4	RW	0	**APIC Cycle Block P2C Write Cycle** 0: Enable 1: Disable
3	RW	0	**P2CR Caching Flush by NM Special Cycle** 0: Disable 1: Enable
2:1	RW	0	**Reserved**
0	RW	0	**PCI Master Broken Timer Enable** 0: Disable 1: Enable. Force into arbitration when there is no FRAME# 16 PCICLK after GNT.

Offset Address: 74h (D17F7)

South-North Module Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic CCA Clock Stop** 0: Enable 1: Disable
6	RW	0	**Dynamic PCI1 Clock Stop (Including VKCKG)** 0: Enable 1: Disable
5	RW	0	**Reserved**
4	RW	0	**Lock Cycle Issued by CPU Flush P2C Cycles Before C2P**
3	RW	0	**Lock Cycle Issued by CPU Block P2C Cycles**
2:0	RW	0	**Reserved**

Offset Address: 75h (D17F7)
PCI Arbitration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Arbitration Mode** 0: REQ-based (arbitrate at the end of REQ#) 1: Frame-based (arbitrate as FRAME# asserts)
6:4	RW	0	**PCI Bus Time Slice Bits [2:0] for CPU as A Master (in unit of PCI clocks)**
3	RW	0	**PCI Master Time-out / New Grant Mechanism Control** 0: Enable PCI Master time-out and disable new grant mechanism 1: Disable PCI Master time-out and enable new grant mechanism
2:0	RW	000b	**PCI Master Bus Timeout** 000: Disable 001: 1x16 PCICLKs 010: 2x16 PCICLKs 011: 3x16 PCICLKs 100: 4x16 PCICLKs 101: 5x16 PCICLKs 110: 6x16 PCICLKs 111: 7 x 16 PCICLKs

Offset Address: 76h (D17F7)
PCI Arbitration 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IO Port 22 Enable (SM)** 0: CPU access to IO address 22 is passed onto the PCI bus 1: CPU access to IO address 22 is processed as internal IO
6	RW	0	**PCI Bus Parking at the Last PCI Master** 0: Disable 1: Enable
5:4	RW	00b	**Master Priority Rotation Control** 00: Disable 01: Grant to CPU after every PCI master grant 10: Grant to CPU after every 2 PCI master grants 11: Grant to CPU after every 3 PCI master grants
3:2	RW	00b	**Selected REQ# as REQ4 for PCI1** 00: REQ4 01: REQ0 10: REQ1 11: REQ2
1	RW	0	**Synchronize REQ before Using** 0: Disable 1: Enable
0	RW	0	**Enable REQ4 for PCI1 as High Priority Master** 0: Disable 1: Enable

Offset Address: 77h (D17F7)
South Module Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**CPU to PCI Peripheral Device Read Blocked by PCI1 FIFO Empty** This function is available only when Rx4F[0] = 1. 0: CPU to PCI peripheral device read blocked by PCI master to memory write. 1: CPU to PCI peripheral device read blocked by PCI1 FIFO empty
5	RW	0	**Reserved**
4:3	RW	00b	**Read FIFO Timer** 00: No timeout 01: Timeout after 1 ms 10: Timeout after 4 ms 11: Timeout after 16 ms
2:0	RW	0	**Reserved**

Offset Address: 78-7Fh (D17F7) – Reserved

CCA Related Control (80-CFh)

Offset Address: 80h (D17F7)

CCA New Feature Option **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**PCI1 New P2CR Flush Mechanism Control** 000: PCI1 old P2CR flush mechanism 001: PCI1 new P2CR flush mechanism 1 enable 010: PCI1 new P2CR flush mechanism 2 enable 100: PCI1 new P2CR flush mechanism 3 enable Others: Reserved
4	RW	0	**PCI1 P2CW New Merge Mechanism** 0: Use PCI1 old P2CW merge mechanism 1: Use PCI1 new P2CW merge mechanism (Use to fix P2CW merge bug)
3	RW	0	**PCIDMA Cycle Not Disable PCI1 Arbitration in C3 State** 0: PCI1DMA cycle still disable PCI1 arbitration in C3 state 1: PCIDMA cycle not disable PCI1 arbitration in C3 state
2	RW	0	**PCI1 Upstream Read Cycle Does Not Pass Write** 0: PCI1 upstream read passes write 1: PCI1 upstream read does not pass write
1	RW	0	**HDAC Upstream Read Cycle Does Not Pass Write** 0: HDAC upstream read cycle passes write 1: HDAC upstream read cycle does not pass write
0	RW	0	**APIC Cycle Blocks Upstream Write** 0: APIC cycle does not block HDAC upstream write cycle 1: APIC cycle blocks HDAC upstream write cycle

Offset Address: 81h (D17F7)

Bus Priority of SM Peripheral Device 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**SPI Priority** 0: Low priority 1: High priority

Offset Address: 82h (D17F7)

CCA Test Mode Address Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:2	RW	0	**CCA Interface Monitor Action Selection** 1h: Monitor the action of the interface between CCA and legacy devices 2h: Monitor the action of the interface between CCA and IDE 3h: Monitor the action of the interface between CCA and CR 4h: Monitor the action of the interface between CCA and UHCI 5h: Monitor the action of the interface between CCA and SDIO3 6h: Monitor the action of the interface between CCA and SDIO1 7h: Reserved 8h: Monitor the action of the interface between CCA and SDIO2 9h: Monitor the action of the interface between CCA and EHCI Ah: Monitor the action of the interface between CCA and Card Boot (CB) Bh: Monitor the action of the interface between CCA and USBD Ch: Monitor the action of the interface between CCA and SPI Dh-Fh: Reserved
1	RW	0	**CCA Debug Mode Signals Selection** 0: Select group 0 CCA debug signals 1: Select group 1 CCA debug signals
0	RW	0	**Reserved**

Offset Address: 83h (D17F7) – Reserved

Offset Address: 84h (D17F7)

Read Passes Write Control **Default Value: 00h**

Read Passes Write: If this function is disabled, a read cannot be performed before a preceding write has been completed; if this function is enabled, the internal controller is allowed to perform a read before a preceding write.

Bit	Attribut	Default	Description
7	RW	0	**Reserved**
6	RW	0	**SPI Slave Mode Read Passes Write** 0: Disable 1: Enable
5	RW	0	**Card Reader Read Passes Write** 0: Disable 1: Enable
4	RW	0	**SDIO Read Passes Write** 0: Disable 1: Enable
3	RW	0	**LPC Read Passes Write** 0: Disable 1: Enable
2	RW	0	**IDE Read Passes Write** 0: Disable 1: Enable
1	RW	0	**USB Read Passes Write** 0: Disable 1: Enable
0	RW	0	**Reserved**

Offset Address: 85h (D17F7)

PCCA New Feature Control **Default Value: 00h**

Bit	Attribut	Default	Description
7	RW	0	**Control Whether PCI Bus's TRDY, STOP, DEVSEL PAD's OE to be Register out** 0: PCI bus's TRDY, STOP, DEVSEL PAD's OE is combinational out 1: PCI bus's TRDY, STOP, DEVSEL PAD's OE is register out
6	RW	0	**Block Configure Cycle to PCI Bus when the Bus Number is not in Secondary PCI Bus Range** 0: Not block configure cycle to PCI bus when the bus number is not in secondary PCI bus range. 1: Block configure cycle to PCI bus when the bus number is not in secondary PCI bus range.
5	RW	0	**MTARD (C2P Cycle In Turn Around State) State Blocks CCA to PCI1's Request** 0: MTARD state blocks CCA to PCI1's request 1: MTARD state dosen't blocks CCA to PCI1's request
4	RW	0	**WCMPLID (Upstream Write Complete ID) Queue Full Block P2CW Request** 0: WCMPLID queue full didn't block P2CW request 1: WCMPLID queue full blocks P2CW request
3	RW	0	**Disable CCA Output to be Register Out** 0: CCA's output is register out 1: CCA's output is combinational out
2	RW	0	**Disable A0000h to FFFFFh Memory Hole** 0: Enable A0000h to FFFFFh memory hole in PCI1 decode 1: Disable A0000h to FFFFFh memory hole in PCI1 decode (Used for Azalia test path)
1	RW	0	**New P2CR FIFO Invalid Mechanism** 0: Disable new P2CR fifo invalid mechanism 1: Enable new P2CR fifo invalid mechanism
0	RW	0	**Reserved**

Offset Address: 86-CFh (D17F7) – Reserved

HDAC Control (D0-DFh)

Offset Address: D0h (D17F7) – Reserved

Offset Address: D1h (D17F7)

HDAC and P2P Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Enable the Capability / Status Write of the P2P Bridge Configuration Capability** 0: Disable 1: Enable
2	RW	0	**Disable HDAC** 0: Enable HDAC 1: Disable HDAC
1:0	RW	0	**Reserved**

Offset Address: D2-D3h (D17F7) – Reserved

Offset Address: D5-D4h (D17F7)

Backdoor Register for Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Backdoor Register for Subsystem Vendor ID**

Offset Address: D7-D6h (D17F7)

Backdoor Register for Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Backdoor Register for Subsystem ID**

Offset Address: D8-DFh (D17F7) – Reserved

Dynamic Clock Control (E0-E3h)

Offset Address: E0h (D17F7)

Dynamic Clock Control 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**CCA New Dynamic Clock Scheme Enable** 0: Old dynamic clock scheme 1: New dynamic clock scheme
6	RW	1b	**CCA Dynamic Clock On** 0: CCA uses dynamic clock 1: CCA uses free running clock
5	RW	0	**Enable D19F0 Rx0D Latency Timer** Always reads as 0. 0: Disable 1: Enable
4	RW	0	**Retry P2C Cycle When in C3 State** 0: Not retry P2C cycle when in C3 state 1: Retry P2C cycle when in C3 state
3:0	RW	0	**Reserved**

Offset Address: E1h (D17F7) – Reserved

Offset Address: E2h (D17F7)

Dynamic Clock Control 3 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:5	RW	0	**Reserved**
4	RW	1b	**Downstream Interface Clock Control** 0: Dynamic clock scheme 1: Free run
3	RW	1b	**PCI1 Clock Control** 0: Dynamic clock scheme 1: Free run
2	RW	1b	**Downstream HDAC Clock Control** 0: Dynamic clock scheme 1: Free run
1	RW	1b	**Downstream SM Internal PCI Device Clock Control** 0: Dynamic clock scheme 1: Free run
0	RW	1b	**Reserved (Do Not Program)**

Offset Address: E3h (D17F7)

PCI1 Internal 33/66MHz Dynamic Clock Control **Default Value: 6Eh**

Bit	Attribute	Default	Description
7	RW	0	**Improve P2CR Performance** 0: Allocate one cacheline of FIFO for P2CR prefetch. 1: Allocate two cachelines of FIFO for P2CR prefetch. Set 1 when only one PCI master has requested (no pending PCI REQ); otherwise, allocate one cacheline of FIFO for prefetch.
6	RW	1b	**Improve the PCI1 Dynamic Clock** 0: Clock enable until FIFO release. 1: Clock enable until cycle is done. Set this bit for better power saving.
5	RW	1b	**PCI1 33/66MHz Dynamic Clock Control** 0: PCI clock (33/66MHz) is kept ON as long as GRANT# is asserted to PCI device. 1: PCI clock (33/66 MHz) will be gated OFF whenever PCI1 is idle (with or without GRANT# asserted).
4	RW	0	**P2CR Data Timeout Enable** Back off PCI Master while not getting TRDY and PCI time out (PCI timer is at Bit [3:1]). 0: Disable 1: Enable
3:1	RW	111b	**P2CR Data Timer (PCI Master TRDY Timeout)** 000: Disable 001: 1*8 PCICLKs 010: 2*8 PCICLKs 011: 3*8 PCICLKs 100: 4*8 PCICLKs 101: 5*8 PCICLKs 110: 6*8 PCICLKs 111: 7*8 PCICLKs
0	RW	0	**Enable P2C Read Backoff Even when Only One PCI Master** It can't retry when only one PCI master and Rx76[6] = 1. (This bit works with Rx70[6] =1.) 0: Not retry when only one PCI Master and bus times out. 1: Retry when bus times out, even though there is only one PCI Master.

DRAM Above 4G Support (E4-FFh)

Offset Address: E4h (D17F7)

Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address [23:20]**
3:0	RW	0	**DRAM Granularity (Powell)** Total DRAM Bits [3:0] — Less than — Granularity 0h — 4G — 16M 1h — 8G — 32M 2h — 16G — 64M 3h — 32G — 128M 4h — 64G — 256M RANK Ending Address Formula: ENDxA[35:24] = RENDxA << Bits [3:0]; (x = 0,1,2,3,4,5,6,7)

Offset Address: E5h (D17F7)

Low Top Address - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Low Top Address [31:24]**

Offset Address: E6h (D17F7)

System Management Mode (SMM) and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxx from masters are passed to PCI1. (PCIC will not claim). 1: Cycles accessing FEEx_xxxx from masters are passed to the Host side for snooping.
2	RW	0	**Top SMM Enable** 0: Disable 1: Enable
1	RW	0	**Reserved**
0	RW	1b	**Compatible SMM Enable** 0: Disable 1: Enable

Offset Address: E7-FBh (D17F7) – Reserved

Offset Address: FCh (D17F7)

PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Enable CCA Read Clock When The State Machine of MTXCTL Is Not Idle** 0: Disable 1: Enable
5:0	RW	0	**Reserved**

Offset Address: FD-FFh (D17F7) – Reserved

DEVICE 19 FUNCTION 0 (D19F0): PCI TO PCI BRIDGE

PCI Configuration Space

All registers in D19F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 19 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D19F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D19F0)

Device ID **Default Value: B353h**

Bit	Attribute	Default	Description
15:0	RO	B353h	**Device ID**

Offset Address: 05-04h (D19F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable error report
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	**Reserved**
3	RO	0	**Respond to Special Cycle** Hardwired to 0.
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D19F0)

PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RW1C	0	**Detected SERR#** 0: No SERR# error 1: SERR# error occurred
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion**
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-Back as a Target** Reserved
6:0	RO	10h	**Reserved**

Offset Address: 08h (D19F0)

Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Revision ID**

Offset Address: 0B-09h (D19F0)

Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D19F0) – Reserved

Offset Address: 0Dh (D19F0)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer; Reserved** Guarantee time slice for CPU master

Offset Address: 0Eh (D19F0)
Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type** 01h indicates the register layout follows PCI-to-PCI bridge specification.

Offset Address: 0Fh (D19F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST** Hardwired to 0. (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-17h (D19F0) – Reserved

Offset Address: 18h (D19F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D19F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D19F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D19F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer**

Offset Address: 1Ch (D19F0)
IO Base Address **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**IO Base Address**
3:0	RO	0	**Reserved**

Offset Address: 1Dh (D19F0)

IO Limit Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**IO Limit Address**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1Eh (D19F0)

Secondary Status Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Fast Back-to-Back Cycle** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RO	0	**66MHz Capability** 0: 33MHz capability 1: 66MHz capability
4:0	RO	0	**Reserved**

Offset Address: 1Fh (D19F0)

Secondary Status Register 2 **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
6	RW1C	0	**Detected SERR#** 0: No SERR# error 1: SERR# error occurred
5	RO	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
4	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the target
3	RO	0	**Target-Abort Assertion**
2:1	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 01: Slow 11: Reserved
0	RW1C	0	**Master Data Parity Error** Reserved

Offset Address: 23-20h (D19F0)

Memory Limit and Base **Default Value: 0000 FFF0h**

Bit	Attribute	Default	Description
31:20	RW	0	**Memory Limit [31:20]**
19:16	RO	0	**Reserved**
15:4	RW	FFFh	**Memory Base [31:20]**
3:0	RO	0	**Reserved**

Offset Address: 27-24h (D19F0)

Prefetchable Memory Limit and Base **Default Value: 0001 FFF1h**

Bit	Attribute	Default	Description
31:20	RW	0	**Prefetchable Memory Limit [31:20]**
19:16	RO	1h	**Reserved**
15:4	RW	FFFh	**Prefetchable Memory Base [31:20]**
3:0	RO	1h	**Reserved**

Offset Address: 2F-28h (D19F0)

Prefetchable Upper Limit and Base **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:36	RW	0	**Prefetchable Upper Limit 32 Bits [31:4] (Not Supported)**
35:32	RW	0	**Prefetchable Upper Limit 32 Bits [3:0]**
31:4	RW	0	**Prefetchable Upper Base 32 Bits [31:4] (Not Supported)**
3:0	RW	0	**Prefetchable Upper Base 32 Bits [3:0]**

Offset Address: 33-30h (D19F0)

Upper IO Base and Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Upper IO Limit [15:0]**
15:0	RO	0	**Upper IO Base [15:0]**

Offset Address: 34h (D19F0)

Capability Pointer **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**Capability Pointer**

Offset Address: 35-3Dh (D19F0) – Reserved

Offset Address: 3F-3Eh (D19F0)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11	RW	0	**Discard Timer SERR# Enable** 0: Disable 1: Enable
10	RW1C	0	**Discard Timer Status** 0: Disable 1: Enable
9	RW	0	**Secondary Discard Timer**
8	RW	0	**Primary Discard Timer**
7	RO	0	**Fast Back-to-Back Enable** 0: Disable 1: Enable
6	RW	0	**Secondary Bus Reset** 0: Disable 1: Enable
5	RW	0	**Master Abort Mode** 0: Disable 1: Enable
4	RW	0	**VGA 16-Bit Decode** 0: Disable 1: Enable
3	RW	0	**VGA Enable** 0: Disable 1: Enable
2	RW	0	**ISA Enable** 0: Disable 1: Enable
1	RW	0	**SERR# Enable** 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Disable 1: Enable

PCI Device-Specific Registers (40-FFh)

Offset Address: 40h (D19F0)

External PCI Device Enable Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6	RW	0	**Hide AD25 on External PCI Bus when Assert** 0: Disable 1: Enable
5	RW	0	**Hide AD24 on External PCI Bus when Assert** 0: Disable 1: Enable
4	RW	0	**Hide AD23 on External PCI Bus when Assert** 0: Disable 1: Enable
3	RW	0	**Hide AD22 on External PCI Bus when Assert** 0: Disable 1: Enable
2	RW	0	**Hide AD21 on External PCI Bus when Assert** 0: Disable 1: Enable
1	RW	0	**Hide AD20 on External PCI Bus when Assert** 0: Disable 1: Enable
0	RW	0	**Hide AD19 on External PCI Bus when Assert** 0: Disable 1: Enable

Offset Address: 41-6Fh (D19F0) – Reserved

Offset Address: 73-70h (D19F0)

Capability ID and Pointer **Default Value: 0000 000Dh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RO	0	**Capability Next Pointer**
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for “Subsystem ID / Subsystem Vendor ID”.

Offset Address: 77-74h (D19F0)

Subsystem ID and Subsystem Vendor ID **Default Value: B353 1106h**

Bit	Attribute	Default	Description
31:16	RO	B353h	**Subsystem ID**
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 78-FFh (D19F0) – Reserved

DEVICE 20 FUNCTION 0 (D20F0): HIGH DEFINITION AUDIO CONTROLLER (HDAC)

PCI Configuration Space

All registers in D20F0 are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 20 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D20F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D20F0)

Device ID **Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RO	3288h	**Device ID**

Offset Address: 05-04h (D20F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Control** 0: Enable interrupt 1: Disable interrupt
9	RO	0	**Fast Back to Back**
8	RO	0	**SERR# Enable**
7	RO	0	**Address Stepping**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping**
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RO	0	**I/O Space Access**

Offset Address: 07-06h (D20F0)

PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error**
14	RO	0	**Signaled System Error (SERR# Asserted)**
13	RO	0	**Received Master Abort**
12	RO	0	**Received Target Abort**
11	RO	0	**Signaled Target Abort**
10:9	RO	0	**DEVSEL# Timing**
8	RO	0	**Master Data Parity Error**
7	RO	0	**Fast Back-to-Back Capability**
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D20F0)

Revision ID **Default Value: 20h**

Bit	Attribute	Default	Description
7:0	RO	20h	**Revision ID**

Offset Address: 0B-09h (D20F0)

Class Code **Default Value: 04 0300h**

Bit	Attribute	Default	Description
23:0	RO	040300h	**Class Code**

Offset Address: 0Ch (D20F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D20F0)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D20F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type** 00h indicates this is a single-function device.

Offset Address: 0Fh (D20F0)

Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST**

Offset Address: 13-10h (D20F0)
HDAC Lower Base Address **Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:14	RW	0	**Lower Base Address** 16 KB are required by hardwiring [13:4] to 0.
13:4	RO	0	**Hardwired to 0**
3	RO	0	**Not Prefetchable**
2:1	RO	10b	**Reserved (Do Not Program)**
0	RO	0	**Reserved**

Offset Address: 17-14h (D20F0)
HDAC Upper Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**HDAC Upper Base Address**

Offset Address: 18-2Bh (D20F0) – Reserved

Offset Address: 2D-2Ch (D20F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D20F0)
Subsystem ID **Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RO	3288h	**Subsystem ID**

Offset Address: 33-30h (D20F0)
Expansion ROM **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Expansion ROM**

Offset Address: 34h (D20F0)
Capability Pointer **Default Value: 50h**

Bit	Attribute	Default	Description
7:0	RO	50h	**Capability Pointer** Points to the power management capability.

Offset Address: 35-3Bh (D20F0) – Reserved

Offset Address: 3Ch (D20F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D20F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTB#).

Offset Address: 3Eh (D20F0)

Minimum Grant Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Minimum Grant Period** Used to specify how long a burst period is needed.

Offset Address: 3Fh (D20F0)

Maximum Latency **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Latency**

HDAC Device-Specific Configuration (40-FFh)

Offset Address: 40h (D20F0)

Back Door Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**Reserved**
0	RW	0	**Subsystem ID / Subsystem Vender ID Back Door Enable** Specifies whether Rx2C~2F are RO or RW. 0: Read Only 1: Read / Write

Offset Address: 41h (D20F0)

HDAC Control **Default Value: 30h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	11b	**Reserved**
3:1	RW	0	**Reserved**
0	RW	0	**HDAC Dynamic Stop** 0: Free running 1:Enable dynamic stop clock

Offset Address: 42-43h (D20F0) – Reserved

Offset Address: 44h (D20F0)

Traffic Class Select **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	000b	**HDAC Traffic Class Assignment** 000b indicates TC0.

Offset Address: 45-4Fh (D20F0) – Reserved

Offset Address: 51-50h (D20F0)

PCI Power Management Capabilities ID **Default Value: 6001h**

Bit	Attribute	Default	Description
15:8	RO	60h	**Next Capability Pointer** Points to the MSI (Message Signaled Interrupt) capability structure
7:0	RO	01h	**PCI Power Management Capability** 01h indicates the linked list item as being the PCI Power Management register.

Offset Address: 53-52h (D20F0)
PCI Power Management Capabilities **Default Value: C842h**

Bit	Attribute	Default	Description
15:11	RO	19h	**PME# Can Be Generated from D3 ~ D0 State** Indicates the power states in which the function may assert PME#. Bit 15: PME# can be asserted from D3 cold Bit 14: PME# can be asserted from D3 hot Bit 13: PME# can be asserted from D2 Bit 12: PME# can be asserted from D1 Bit 11: PME# can be asserted from D0
10	RO	0	**D2 State Supported** 0: Not supported 1: Supported
9	RO	0	**D1 State Supported** 0: Not supported 1: Supported
8:6	RO	001b	**Report D3 Max Suspend Current** Reports the 3.3V auxiliary current requirements for the PCI function. 000: 0 mA 001: 55 mA 010: 100 mA 011: 160 mA 100: 220 mA 101: 270 mA 110: 320 mA 111: 375 mA
5	RO	0	**Device-Specific Initialization Requirement** 0: Not required 1: Required
4	RO	0	**Reserved**
3	RO	0	**Hardwired to 0**
2:0	RO	010b	**PCI Power Support** 010b indicates that this function complies with the PCI Power Management Interface specification version 1.1.

Offset Address: 57-54h (B0D20F0)
Power Management Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Hardwired to 0**
21:16	RO	0	**Reserved**
15	RW1C	0	**PME Status** This bit is set when the HDAC would assert the PME# independent of the state of the bit 8. This bit is in resume well.
14:9	RO	0	**Reserved**
8	RWS	0	**PME Enable** Enable PME wake up if bit 15 is set. This bit is in resume well.
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** This field is used both to determinate the current power state and to set a new power state. 00: D0 01: D1 10: D2 11: D3 If software attempts to write a value of 10b or 01b into this field, the write operation will complete normally; however, no state change will occur.

Offset Address: 58-5Fh (D20F0) – Reserved

Offset Address: 61-60h (D20F0)
MSI Capability ID **Default Value: 7005h**

Bit	Attribute	Default	Description
15:8	RO	70h	**Next Capability Pointer** Points to the PCI Express capability structure
7:0	RO	05h	**MSI Capability**

Offset Address: 63-62h (D20F0)

MSI Message Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RO	1b	**64-Bit Address Capability** 0: 32-bit 1: 64-bit
6:4	RO	0	**Multiple Message Enable** Normally these are RW bits, but software will always read 000b to indicate only 1 message is supported.
3:1	RO	0	**Multiple Message Capable** 0 indicates the number of requested vector is 1.
0	RW	0	**MSI Enable** 0: Assert INTx instead of MSI. 1: MSI will be generated instead of INTx assertion.

Offset Address: 67-64h (D20F0)

MSI Message Lower Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Message Lower Address**
1:0	RO	0	**Reserved**

Offset Address: 6B-68h (D20F0)

MSI Message Upper Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Message Upper Address**

Offset Address: 6D-6Ch (D20F0)

MSI Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Data Used for MSI Message**

Offset Address: 6E-6Fh (D20F0) – Reserved

Offset Address: 71-70h (D20F0)

PCI Express Capability ID **Default Value: 0010h**

Bit	Attribute	Default	Description
15:8	RO	0	**Capability Link** This is the last capability structure of the list.
7:0	RO	10h	**PCI Express Capability**

Offset Address: 73-72h (D20F0)
PCI Express Capability **Default Value: 0091h**

Bit	Attribute	Default	Description
15:8	RO	0	**Hardwired to 0**
7:0	RO	91h	**Capability Version #1** ***Bits [7:4]:*** **Device / Port Type** 0000: PCI Express Endpoint device 0001: Legacy PCI Express Endpoint device 0100: Root Port of PCI Express Root Complex 0101: Upstream Port of PCI Express Switch 0110: Downstream Port of PCI Express Switch 0111: PCI Express -_to-_PCI/PCI-X Bridge 1000: PCI/PCI-X to PCI Express Bridge 1001: Root Complex Integrated Endpoint Device 1010: Root Complex Event Collector ***Bits [3:0]:*** **Capability Version**

Offset Address: 77-74h (D20F0)
Device Capabilities **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Device Capabilities** Hardwired to 0.

Offset Address: 79-78h (D20F0)
Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	0	**Hardwired to 0**
11	RO	0	**Snoop**
10:0	RO	0	**Hardwired to 0**

Offset Address: 7B-7Ah (D20F0)
Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transaction Pending** 0: All non-posted requests have been executed. 1: Some non-posted requests are still pending.
4	RO	1b	**AUX Power Detected** Hardwired to 1b.
3:0	RO	0	**Hardwired to 0**

Offset Address: 7C-FFh (D20F0) – Reserved

HDAC PCI Extended Configuration Space

HDAC PCI Extended Configuration (100-260h)

Offset Address: 103-100h (D20F0)

Virtual Channel Enhanced Capability **Default Value: 1301 0002h**

Bit	Attribute	Default	Description
31:20	RO	130h	**Next Capability Pointer** Hardwired to 130h.
19:16	RO	1h	**Capability Structure Revision** This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Hardwired to 1h to indicate PCIe version 1.1.
15:0	RO	0002h	**Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. Hardwired to 0002h to indicate the virtual channel capability.

Offset Address: 107-104h (D20F0)

Port VC Capability 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:3	RO	0	**Hardwired to 0**
2:0	RO	0	**Hardwired to 0** Indicates that one extended VC is supported by the controller.

Offset Address: 10B-108h (D20F0)

Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Hardwired to 0** Indicates that a VC arbitration table is not present.
23:8	RO	0	**Reserved**
7:0	RO	0	**Hardwired to 0**

Offset Address: 10D-10Ch (D20F0)

Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Port VC Control** Reserved.

Offset Address: 10F-10Eh (D20F0)

Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**Hardwired to 0** Indicates that VC arbitration table is not present.

Offset Address: 113-110h (D20F0)

VC0 Resource Capability **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Hardwired to 0** This field is not valid for endpoint devices.

Offset Address: 117-114h (D20F0)

VC0 Resource Control **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC0 Enable** Hardwired to 1 for VC0.
30:27	RO	0	**Reserved**
26:24	RO	0	**VC0 ID** Hardwired to 0 since this field is assigned to VC0.
23:20	RO	0	**Reserved**
19:16	RO	0	**Hardwired to 0**
15:8	RO	0	**Reserved**
7:1	RW	7Fh	**TC/VC0 Map** Bits [7:1] are implemented as RW bits.
0	RO	1b	**TC/VC0 Map** Hardwired to 1b since TC0 is always mapped to VC0.

Offset Address: 118-119h (D20F0) – Reserved

Offset Address: 11B-11Ah (D20F0)

VC0 Resource Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1	RO	0	**Hardwired to 0** This bit is not applied to integrated device.
0	RO	0	**Hardwired to 0** This bit is not valid for endpoint devices.

Offset Address: 11C-12Fh (D20F0) – Reserved

Offset Address: 133-130h (D20F0)

Root Complex Link Declaration Enhanced Capability Header Register **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:16	RO	0001h	**Next Capability** Hardwired to 0001h.
15:0	RO	0005h	**PCI Express Extended Capability ID** Hardwired to 0005h.

Offset Address: 137-134h (D20F0)

Element Self Description **Default Value: 0401 0100h**

Bit	Attribute	Default	Description
31:24	RO	04h	**Port Number** 04h indicates HDAC controller is assigned as port #5.
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries** Hardwired to 01h.
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** The HDAC controller is an integrated root complex device, and this field reports a value of 0h.

Offset Address: 138-13Fh (D20F0) – Reserved

Offset Address: 143-140h (D20F0)

Link Description **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Target Port Number** Hardwired to 00h.
23:16	RO	01h	**Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Indicates that the link points to RCRB.
0	RO	1b	**Link Valid**

Offset Address: 144-147h (D20F0) – Reserved

Offset Address: 14B-148h (D20F0)

Link Lower Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Link Lower Address** (RCRBH Memory Address)
11:0	RO	0	**Reserved** Always reads 0.

Offset Address: 14F-14Ch (D20F0)

Link Upper Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved** Always reads 0.
3:0	RO	0	**Link Upper Address**. (RCRBH Memory Address)

Offset Address: 150-260h (D20F0) – Reserved

High Definition Audio Controller Memory Mapped I/O Space (HDAC-MMIO)

This section describes the memory mapped HDAC registers. Please refer to High Definition Audio Specification 1.0 for details.

Global Capabilities and Control (00-1Bh)

Offset Address: 01-00h (HDAC-MMIO)

Global Capabilities – GCAP **Default Value: 4401h**

Bit	Attribute	Default	Description
15:12	RO	4h	**Number of Output Streams Supported** 0h: No output streams supported. 1h: 1 output streams supported. 2h: 2 output streams supported. Fh: 15 output streams supported. Hardware fixed to support 4 input streams.
11:8	RO	4h	**Number of Input Streams Supported** 0h: No input streams supported. 1h: 1 input streams supported. 2h: 2 input streams supported. Fh: 15 input streams supported. Hardware fixed to support 4 input streams.
7:3	RO	0	**Number of Bidirectional Streams Supported** 0h: No bidirectional stream supported. 1h: 1 bidirectional stream supported. 2h: 2 bidirectional streams supported. 1Eh: 30 bidirectional streams supported. Hardware fixed to be no bidirectional stream supported.
2	RO	0	**Reserved**
1	RO	0	**Number of Serial Data Out Signals** 0: 1 SDOUT line is supported. 1: 2 SDOUTs are supported. Hardware fixed to support 1 SDOUT line.
0	RO	1b	**64-Bit Address Supported** 0: Only 32-bit addressing is available. 1: 64-bit addressing is supported.

Offset Address: 03-02h (HDAC-MMIO)

Version Number **Default Value: 0100h**

Bit	Attribute	Default	Description
15:8	RO	01h	**Major Version**
7:0	RO	0	**Minor Version**

The version number "0100h" indicates this chip complies with High Definition Audio Specification Rev 1.0.

Offset Address: 07-04h (HDAC-MMIO)

Payload Capability **Default Value: 001D 003Ch**

Bit	Attribute	Default	Description
31:16	RO	001Dh	**Input Payload Capability** 001Dh indicates 29-word payload (464 bits). Note: This does not include bandwidth used for command and control.
15:0	RO	003Ch	**Output Payload Capability** 003Ch indicates 60-word payload (960 bits). It indicates the total output payload available on the link is 60 word (960 bits).

Offset Address: 0B-08h (HDAC-MMIO)
Global Control – GCTL **Default Value: 0000 000nh**

Bit	Attribute	Default	Description
31:9	RO	0	**Reserved**
8	RW	0	**Accept Unsolicited Response Enable** 0: Unsolicited responses from codec are not accepted. 1: Unsolicited responses from codec are accepted by the controller.
7:2	RO	0	**Reserved**
1	RW	0	**Flush Control** Writing a 1 to this bit initiates a flush.
0	RWS	HwInit	**Controller Reset** For read: 0: In reset state. 1: Controller is ready for operations. For write: 0: Reset the controller. 1: Write 1 causes the controller exit its reset state and de-assert link AZRST#.

Offset Address: 0D-0Ch (HDAC-MMIO)
Wake Enable – WAKEEN **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1:0	RWS	0	**AZSDIN Wake Enable Flags** 0: Not allow the associated AZSDIN signal to generate a wake or processor interrupt. 1: Allow the associated AZSDIN signal to generate a wake or processor interrupt. The bit[i] corresponds to AZSDIN[i] signal.

Offset Address: 0F-0Eh (HDAC-MMIO)
AZSDIN State Change Status – STATESTS **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1:0	RW1CS	0	**AZSDIN State Change Status Flags** 0: No state change 1: The associated AZSDIN signal received a “State Change” event. The bit[i] corresponds to AZSDIN[i] signal.

Offset Address: 11-10h (HDAC-MMIO)
Global Status – GSTS **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1	RW1C	0	**Flush Status** 0: No flush cycle completed 1: Flush cycle completed This bit is set to 1 by the hardware to indicate that the flush cycle initiated by the Rx08[1] has completed. Software must write 1 to clear this bit before the next time Rx08[1] is set.
0	RO	0	**Reserved**

Offset Address: 12-17h (HDAC-MMIO) – Reserved

Offset Address: 1B-18h (HDAC-MMIO)

Stream Payload Capability **Default Value: 001D 003Ch**

Bit	Attribute	Default	Description
31:16	RO	001Dh	**Input Stream Payload Capability** 001Dh indicates 29-word payload (464 bits).
15:0	RO	003Ch	**Output Stream Payload Capability** 003Ch indicates 60-word payload (960 bits).

Reserved Registers (1C-1Fh)

Offset Address: 1C-1Fh (HDAC-MMIO) – Reserved

Interrupt Control (20-27h)

Offset Address: 23-20h (HDAC-MMIO)

Interrupt Control – INTCTL **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Global Interrupt Enable** 0: Disable 1: Enable device interrupt generation
30	RW	0	**Controller Interrupt Enable** 0: Disable 1: Enable controller's general interrupt. When set to 1, the controller generates an interrupt when the corresponding status bit is set due to a response interrupt, a response buffer overrun, and wake events.
29:8	RO	0	**Reserved**
7:4	RW	0	**Stream Interrupt Enable – for Output Stream [3:0]** 0: Disable 1: Enable
3:0	RW	0	**Stream Interrupt Enable – for Input Stream [3:0]** 0: Disable 1: Enable

Offset Address: 27-24h (HDAC-MMIO)

Interrupt Status – INTSTS **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Global Interrupt Status** This bit is set when one of the interrupt status bits is set. 0: No interrupt occurred 1: Some interrupt(s) occurred
30	RO	0	**Controller Interrupt Status** 0: No interrupt occurred 1: Some interrupt(s) occurred A 1 indicates that an interrupt condition occurred due to a response interrupt, a response overrun, or a codec state change request. The exact cause can be determined by interrogating the RIRB status register and the state change status register.
29:8	RO	0	**Reserved**
7:4	RO	0	**Stream Interrupt Status – for Output Stream [3:0]** 0: No interrupt occurred 1: Interrupt occurred
3:0	RO	0	**Stream Interrupt Status – for Input Stream [3:0]** 0: No interrupt occurred 1: Interrupt occurred

Reserved Registers (28-2Fh)

Offset Address: 28-2Fh (HDAC-MMIO) – Reserved

Synchronization Control (30-3Bh)

Offset Address: 33-30h (HDAC-MMIO)

Wall Clock Counter **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Wall Clock Counter** 32 bits counter that is incremented at the link bitclk rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds.

Offset Address: 34-37h (HDAC-MMIO) – Reserved

Offset Address: 3B-38h (HDAC-MMIO)

Stream Synchronization – SSYNC **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:4	RW	0	**Stream Synchronization Bits – for Output Stream [3:0]** 0: Do not block data. 1: Stop in sending data to the link.
3:0	RW	0	**Stream Synchronization Bits – for Input Stream [3:0]** 0: Do not block data 1: Stop in receiving data from the link.

Reserved Registers (3C-3Fh)

Offset Address: 3C-3Fh (HDAC-MMIO) – Reserved

HDAC CORB (Command Output Ring Buffer) Control (40-4Fh)

Offset Address: 43-40h (HDAC-MMIO)
CORB Lower Base Address – CORBLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	**CORB Lower Base Address** Lower address of the Command Output Ring Buffer.
6:0	RO	0	**Reserved** Hardwired to 0 for alignment to 128-byte boundary.

Offset Address: 47-44h (HDAC-MMIO)
CORB Upper Base Address – CORBUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**CORB Upper Base Address** Upper 32 bits of address of the Command Output Ring Buffer.

Offset Address: 49-48h (HDAC-MMIO)
CORB Write Pointer **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	0	**CORB Write Pointer** Software writes the last valid CORB entry offset into this field in DW granularity. The DMA engine fetches commands from the CORB until the read point matches the write pointer. The field may be written while the DMA engine is running.

Offset Address: 4B-4Ah (HDAC-MMIO)
CORB Read Pointer **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**CORB Read Pointer Reset** Writes a 1 to reset the CORB Read Pointer to 0. DMA engine must be stopped prior to resetting the read pointer or DMA transfer may be corrupted. This bit is always read 0.
14:8	RO	0	**Reserved**
7:0	RO	0	**CORB Read Pointer** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB read pointer offset in DW granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports up to 256 CORB entries (256*4B = 1KB) in the cyclic buffer.

Offset Address: 4Ch (HDAC-MMIO)
CORB Control – CORBCTL **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Enable CORB DMA Engine** 0: DMA stop 1: DMA run (when read pointer lags write pointer). Software must read the value back.
0	RW	0	**CORB Memory Error Interrupt Enable** 0: Disable 1: Enable. The controller will generate an interrupt when Rx4D[0] is set to 1.

Offset Address: 4Dh (HDAC-MMIO)

CORB Status – CORBSTS **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW1C	0	**CORB Memory Error Indication** 0: No error. 1: Error detected. The controller has detected an error in the pathway between the controller and memory. An interrupt is asserted if Rx4C[0] is set to 1.

Offset Address: 4Eh (HDAC-MMIO)

CORB Size – CORBSIZE **Default Value: 42h**

Bit	Attribute	Default	Description
7:4	RO	4h	**CORB Size Capability** 4h indicates 256 entries (1 KB).
3:2	RO	0	**Reserved**
1:0	RO	10b	**CORB Size** 00: 2 entries (8 bytes) 01: 16 entries (64 bytes) 10: 256 entries (1 KB) 11: Reserved

Offset Address: 4Fh (HDAC-MMIO) – Reserved

HDAC RIRB (Response Input Ring Buffer) Control (50-5Fh)

Offset Address: 53-50h (HDAC-MMIO)
RIRB Lower Base Address – RIRBLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	**RIRB Lower Base Address** Lower address of the Response Input Ring Buffer.
6:0	RO	0	**Reserved** Hardwired to 0 for alignment to 128-byte boundary.

Offset Address: 57-54h (HDAC-MMIO)
RIRB Upper Base Address – RIRBUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**RIRB Upper Base Address** Upper 32 bits of address of the Response Input Output Ring Buffer.

Offset Address: 59-58h (HDAC-MMIO)
RIRB Write Pointer – RIRBWP **Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	**RIRB Write Pointer Reset** Writes 1 to reset the RIRB Write Pointer to 0. The DMA engine must be stopped prior to resetting the write pointer or DMA transfer may be corrupted. This bit is always read as 0.
14:8	RO	0	**Reserved**
7:0	RO	0	**RIRB Write Pointer** This register indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB write pointer offset in 2 DW units. Up to 256 RIRB entries in the cyclic buffer is supported.

Offset Address: 5B-5Ah (HDAC-MMIO)
Response Interrupt Count – RINTCNT **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	00h	**Response Interrupt Count – N Response** 00h: 256 responses 01h to FFh: 1 to 255 responses The DMA engine should be stopped when changing this field or else an interrupt may be lost.

Offset Address: 5Ch (HDAC-MMIO)
RIRB Control – RIRBCTL **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Response Overrun Interrupt Control** 0: Disable 1: Enable
1	RW	0	**Enable RIRB DMA Engine** 0: DMA stop 1: DMA run (when response queue is not empty).
0	RW	0	**Response Interrupt Control** 0: Disable 1: Enable. Generate an interrupt after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx input after a frame which returned a response. The N counter is reset when the interrupt is generated.

Offset Address: 5Dh (HDAC-MMIO)
RIRB Status – RIRBSTS **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW1C	0	**Response Overrun Interrupt Status** Hardware sets this bit to 1 when an overrun occurs in the RIRB. An interrupt may be generated if the response overrun interrupt control bit is set. 0: No overrun 1: Overrun occurred
1	RO	0	**Reserved**
0	RW1C	0	**Response Interrupt** Hardware sets this bit to 1 when an interrupt has been generated after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx inputs. 0: No response interrupt 1: Response interrupt occurred

Offset Address: 5Eh (HDAC-MMIO)
RIRB Size – RIRBSIZE **Default Value: 42h**

Bit	Attribute	Default	Description
7:4	RO	0100b	**RIRB Size Capability** 0100b indicates 256 entries (2 KB).
3:2	RO	0	**Reserved**
1:0	RO	10b	**RIRB Size** 00: 2 entries (16 bytes) 01: 16 entries (128 bytes) 10: 256 entries (2 KB) 11: Reserved

Offset Address: 5Fh (HDAC-MMIO) – Reserved

HDAC Immediate Command Control (60-69h)

Offset Address: 63-60h (HDAC-MMIO)

Immediate Command Input / Output Interface **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Immediate Command Write** The written value will be sent out over the link in the next available frame. Reads always return 0's. Software must ensure that the ICB bit (bit-0) in the Immediate Command Status register is cleared before writing a value into this register or undefined behavior will result.

Offset Address: 67-64h (HDAC-MMIO)

Immediate Response Input Interface **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Immediate Response Read** Reads return the last response came over the link.

Offset Address: 69-68h (HDAC-MMIO)

Immediate Command Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:4	RO	0	**Immediate Response Result Address** This is the address of the codec which sent the response currently been latched in the Immediate Response Input register.
3	RO	0	**Immediate Response Result Unsolicited** This bit indicates whether the response latched in the Immediate Response Input register is solicited or unsolicited. 0: A solicited response latched 1: An unsolicited response latched
2	RO	0	**Immediate Command Version** This bit is corresponding to Rx40[4]. 0: Bits [7:4] and bit 3 are reserved. 1: Both bits [7:4] and bit [3] are implemented.
1	RW1C	0	**Immediate Result Valid** This bit is set to 1 by hardware when a new response has been received. 0: No new response 1: A new response arrived
0	RO	0	**Immediate Command Busy** 0: Ready for accepting an immediate command. 1: Not ready. Software must wait until this bit becomes 0 before writing a value in Rx63-60. Before codec initialization finishes, this bit is 1.

Reserved Registers (6A-6Fh)

Offset Address: 6A-6Fh (HDAC-MMIO) – Reserved

DMA Position Base Address (70-77h)

Offset Address: 73-70h (HDAC-MMIO)

DMA Position Lower Base Address – DPLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:7	RW	0	**DMA Position Lower Base Address**
6:1	RO	0	**DMA Position Lower Base Unimplemented Bits** Hardwired to 0.
0	RW	0	**DMA Position Buffer Enable** 0: Disable 1: Enable

Offset Address: 77-74h (HDAC-MMIO)

DMA Position Upper Base Address – DPUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**DMA Position Upper Base Address** Upper 32 bits of address of the DMA Position Buffer Base Address.

Reserved Registers (78-7Fh)

Offset Address: 78-7Fh (HDAC-MMIO) – Reserved

HDAC Stream Descriptors (80-17Fh)

HDAC Stream Descriptor Control

Default Value: 00 0000h

Offset Address: 82-80h (HDAC-MMIO) – Input Stream 0
Offset Address: A2-A0h (HDAC-MMIO) – Input Stream 1
Offset Address: C2-C0h (HDAC-MMIO) – Input Stream 2
Offset Address: E2-E0h (HDAC-MMIO) – Input Stream 3
Offset Address: 102-100h (HDAC-MMIO) – Output Stream 0
Offset Address: 122-120h (HDAC-MMIO) – Output Stream 1
Offset Address: 142-140h (HDAC-MMIO) – Output Stream 2
Offset Address: 162-160h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
23:20	RW	0h	**Stream ID** A tag corresponds to the transferred data on the link. 0h: Unused 1h to 0Fh: Stream 1 to 15
19	RO	0	**Bidirectional Direction Control** Hardwired to 0. Bidirectional engine is not supported.
18	RW	0	**Traffic Priority** Hardwired to 0. The traffic will be handled on a best effort basis. 0: Handles on a "best effort" basis 1: Handles as preferred traffic
17:16	RO	00b	**Stripe Control** Hardwired to 0 indicating that the controller supports 1 SDO line. 00: 1 SDO 01: 2 SDOs 10: 4 SDOs 11: Reserved (Read Only for input streams)
15:8	RO	0	**Reserved**
7:5	RO	0	**Reserved**
4	RW	0	**Descriptor Error Interrupt Enable** Controls whether an interrupt is generated when the descriptor error status bit is set. 0: Disable 1: Enable
3	RW	0	**FIFO Error Interrupt Enable** Controls whether an interrupt is generated when FIFO error (underrun/overrun) occurs. 0: Disable 1: Enable
2	RW	0	**Interrupt On Completion Enable** Controls whether an interrupt occurs when a buffer completion with the IOC bit set in its descriptor. 0: Disable 1: Enable.
1	RW	0	**Stream Run** 0: DMA disable. The DMA engine associated with this input stream will be disabled. If the corresponding Rx38 (SSYNC) bit is 0, input stream data will be taken from the link and moved to the FIFO and an overrun may occurs. 1: DMA enable. The DMA engine associated with this input stream is enabled to transfer data in the FIFO to main memory.
0	RW	0	**Stream Reset** ***For Read:*** 0: Ready (not in reset state) 1: In reset state ***For Write:*** 0: Exit reset 1: Reset the steam Writing a 1 causes the corresponding stream to be reset. The stream descriptor registers (except this bit), FIFOs, and cadence generator for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to being operation, it will report 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The run bit must be cleared before SRST is asserted.

HDAC Stream Descriptor Status

Default Value: 00h

Offset Address: 83h (HDAC-MMIO) – Input Stream 0
Offset Address: A3h (HDAC-MMIO) – Input Stream 1
Offset Address: C3h (HDAC-MMIO) – Input Stream 2
Offset Address: E3h (HDAC-MMIO) – Input Stream 3
Offset Address: 103h (HDAC-MMIO) – Output Stream 0
Offset Address: 123h (HDAC-MMIO) – Output Stream 1
Offset Address: 143h (HDAC-MMIO) – Output Stream 2
Offset Address: 163h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**FIFO Ready** ***For an output stream:*** 0: Not enough data for transferring. 1: The output DMA FIFO contains enough data to maintain the output stream on the link. This bit default to 0 on reset because the FIFO is cleared on a reset. ***For an input stream:*** This bit is not meaningful for an input stream. Therefore, it is always read 0 for input stream.
4	RW1C	0	**Descriptor Error** 0: No error 1: Error occurred during the fetch of a descriptor - something bad happened. This could be a result of a master abort, a parity error, or ECC error on the bus, or any other error which renders the current buffer descriptor or BDL list useless.
3	RW1C	0	**FIFO Error** For an input stream, it indicates a FIFO overrun occurred while run bit is set. For an output stream, it indicates a FIFO underrrun occurred while there are still buffers to send. 0: No error 1: Error occurred
2	RW1C	0	**Buffer Completion Interrupt Status** 0: Not completed 1: Buffer operation completed This bit is set to 1 by the controller after the last sample of a buffer has been processed and the interrupt on completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit.
1:0	RO	0	**Reserved**

HDAC Stream Descriptor Link Position in Buffer

Default Value: 0000 0000h

Offset Address: 87-84h (HDAC-MMIO) – Input Stream 0
Offset Address: A7-A4h (HDAC-MMIO) – Input Stream 1
Offset Address: C7-C4h (HDAC-MMIO) – Input Stream 2
Offset Address: E7-E4h (HDAC-MMIO) – Input Stream 3
Offset Address: 107-104h (HDAC-MMIO) – Output Stream 0
Offset Address: 127-124h (HDAC-MMIO) – Output Stream 1
Offset Address: 147-144h (HDAC-MMIO) –Output Stream 2
Offset Address: 167-164h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RO	0	**Link Position in Buffer** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the cyclic buffer length register and then wrap to 0.

HDAC Stream Descriptor Cyclic Buffer Length

Default Value: 0000 0000h

Offset Address: 8B-88h (HDAC-MMIO) – Input Stream 0
Offset Address: AB-A8h (HDAC-MMIO) – Input Stream 1
Offset Address: CB-C8h (HDAC-MMIO) – Input Stream 2
Offset Address: EB-E8h (HDAC-MMIO) – Input Stream 3
Offset Address: 10B-108h (HDAC-MMIO) – Output Stream 0
Offset Address: 12B-128h (HDAC-MMIO) – Output Stream 1
Offset Address: 14B-148h (HDAC-MMIO) – Output Stream 2
Offset Address: 16B-168h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RW	0	**Cyclic Buffer Length** Indicates the number of bytes in the cyclic buffer. Link position in buffer will be reset when it reaches this value.

HDAC Stream Descriptor Last Valid Index (HDAC-MMIO)

Default Value: 0000h

Offset Address: 8D-8Ch (HDAC-MMIO) – Input Stream 0
Offset Address: AD-ACh (HDAC-MMIO) – Input Stream 1
Offset Address: CD-CCh (HDAC-MMIO) – Input Stream 2
Offset Address: ED-ECh (HDAC-MMIO) – Input Stream 3
Offset Address: 10D-10Ch (HDAC-MMIO) – Output Stream 0
Offset Address: 12D-12Ch (HDAC-MMIO) – Output Stream 1
Offset Address: 14D-14Ch (HDAC-MMIO) – Output Stream 2
Offset Address: 16D-16Ch (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	0	**Last Valid Index** The value written to this register indicates the index for the last valid buffer descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list on continue processing. This register must be at least 1.

Offset Address: 8E-8Fh (HDAC-MMIO) – Reserved

HDAC Input Stream Descriptor FIFO Size

Default Value: 0060h

Offset Address: 91-90h (HDAC-MMIO) – Input Stream 0
Offset Address: B1-B0h (HDAC-MMIO) –Input Stream 1
Offset Address: D1-D0h (HDAC-MMIO) – Input Stream 2
Offset Address: F1-F0h (HDAC-MMIO) – Input Stream 3

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RO	60h	**FIFO Size** The max number of bytes that can be fetched by the controller at one time.

HDAC Stream Descriptor Format **Default Value: 0000h**

Offset Address: 93-92h (HDAC-MMIO) – Input Stream 0
Offset Address: B3-B2h (HDAC-MMIO) – Input Stream 1
Offset Address: D3-D2h (HDAC-MMIO) – Input Stream 2
Offset Address: F3-F2h (HDAC-MMIO) – Input Stream 3
Offset Address: 113-112h (HDAC-MMIO) – Output Stream 0
Offset Address: 133-132h (HDAC-MMIO) – Output Stream 1
Offset Address: 153-152h (HDAC-MMIO) – Output Stream 2
Offset Address: 173-172h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RW	0	**Sample Base Rate** 0: 48 KHz 1: 44.1 KHz
13:11	RW	000b	**Sample Base Rate Multiple** 000: x1 001: x2 010: x3 011: x4 Others: Reserved
10:8	RW	000b	**Sample Base Rate Divisor** 000: Divide by 1 (48 kHz, 44.1 kHz) 001: Divide by 2 (24 kHz, 22.05 kHz) 010: Divide by 3 (16 kHz, 32 kHz) 011: Divide by 4 (11.025 kHz) 100: Divide by 5 (9.6 kHz) 101:= Divide by 6 (8 kHz) 110: Divide by 7 111: Divide by 8 (6 kHz)
7	RO	0	**Reserved**
6:4	RW	000b	**Bits Per Sample** 000: 8 bits, packed in memory in 8-bit containers on 16-bit boundary. 001: 16 bits, packed in memory in 16-bit containers on 16-bit boundary. 010: 20 bits, packed in memory in 32-bit containers on 32-bit boundary. 011: 24 bits, packed in memory in 32-bit containers on 32-bit boundary. 100: 32 bits, packed in memory in 32-bit containers on 32-bit boundary. Others: Reserved
3:0	RW	0	**Number of Channels** 0000 to 1111: 1 to 16 channels

Offset Address: 94-97h (HDAC-MMIO) – Reserved

Offset Address: B4-B7h (HDAC-MMIO) – Reserved

Offset Address: D4-D7h (HDAC-MMIO) – Reserved

Offset Address: F4-F7h (HDAC-MMIO) – Reserved

Offset Address: 114-117h (HDAC-MMIO) – Reserved

Offset Address: 134-137h (HDAC-MMIO) – Reserved

Offset Address: 154-157h (HDAC-MMIO) – Reserved

Offset Address: 174-177h (HDAC-MMIO) – Reserved

HDAC Stream Descriptor BDL Pointer Lower Base Address **Default Value: 0000 0000h**

Offset Address: 9B-98h (HDAC-MMIO) – Input Stream 0
Offset Address: BB-B8h (HDAC-MMIO) – Input Stream 1
Offset Address: DB-D8h (HDAC-MMIO) – Input Stream 2
Offset Address: FB-F8h (HDAC-MMIO) – Input Stream 3
Offset Address: 11B-118h (HDAC-MMIO) – Output Stream 0
Offset Address: 13B-138h (HDAC-MMIO) – Output Stream 1
Offset Address: 15B-158h (HDAC-MMIO) – Output Stream 2
Offset Address: 17B-178h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:7	RW	0	**Buffer Descriptor List Lower Base Address**
6:0	RO	0	**Unimplemented Bits** Hardwired to 0 to force 128-byte alignment of the BDL.

Stream Descriptor BDL Pointer Upper Base Address **Default Value: 0000 0000h**

Offset Address: 9F-9Ch (HDAC-MMIO) –Input Stream 0
Offset Address: BF-BCh (HDAC-MMIO) – Input Stream 1
Offset Address: DF-DCh (HDAC-MMIO) – Input Stream 2
Offset Address: FF-FCh (HDAC-MMIO) – Input Stream 3
Offset Address: 11F-11Ch (HDAC-MMIO) – Output Stream 0
Offset Address: 13F-13Ch (HDAC-MMIO) – Output Stream 1
Offset Address: 15F-15Ch (HDAC-MMIO) – Output Stream 2
Offset Address: 17F-17Ch (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RW	0	**Buffer Descriptor List Upper Base Address**

Offset Address: AE-AFh (HDAC-MMIO) – Reserved

Offset Address: CE-CFh (HDAC-MMIO) – Reserved

Offset Address: EE-EFh (HDAC-MMIO) – Reserved

Offset Address: 10E-10Fh (HDAC-MMIO) – Reserved

Offset Address: 12E-12Fh (HDAC-MMIO) – Reserved

Offset Address: 14E-14Fh (HDAC-MMIO) – Reserved

Offset Address: 16E-16Fh (HDAC-MMIO) – Reserved

HDAC Output Stream Descriptor FIFO Size **Default Value: 00C0h**

Offset Address: 111-110h (HDAC-MMIO) – Output Stream 0
Offset Address: 131-130h (HDAC-MMIO) – Output Stream 1
Offset Address: 151-150h (HDAC-MMIO) – Output Stream 2
Offset Address: 171-170h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8:0	RO	0C0h	**FIFO Size** The max number of bytes that can be fetched by the controller at one time. Note: Bit [8] can *only* be modified together with bits [7:0].

Reserved Registers (180-202Fh)

Offset Address: 180-202Fh (HDAC-MMIO) - Reserved

Alias Registers (2030-2167h)

Offset Address: 2033-2030h (HDAC-MMIO)

Wall Clock Counter Alias – WALCLKA **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Wall Clock Counter Alias**

Offset Address: 2034-2083h (HDAC-MMIO) - Reserved

HDAC Stream Descriptor Link Position in Buffer Alias **Default Value: 0000 0000h**

Offset Address: 2087-2084h (HDAC-MMIO) – Input Stream 0
Offset Address: 20A7-20A4h (HDAC-MMIO) – Input Stream 1
Offset Address: 20C7-20C4h (HDAC-MMIO) – Input Stream 2
Offset Address: 20E7-20E4h (HDAC-MMIO) – Input Stream 3
Offset Address: 2107-2104h (HDAC-MMIO) – Output Stream 0
Offset Address: 2127-2124h (HDAC-MMIO) – Output Stream 1
Offset Address: 2147-2144h (HDAC-MMIO) – Output Stream 2
Offset Address: 2167-2164h (HDAC-MMIO) – Output Stream 3

Bit	Attribute	Default	Description
31:0	RO	0	**Link Position in Buffer Alias** An alias of the link position in buffer register for each stream descriptor.

Offset Address: 2088-2163h (HDAC-MMIO) – Reserved